Notes

Revision History

February 5, 2002: Initial publication.

Introduction

The RC32351 Integrated Communications Processor meets the requirements of various embedded communications applications including residential gateways, SOHO routers, and wireless systems. It is a single-chip solution that incorporates many of the generic, system functionality and application-specific, communication interfaces to enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate for these applications.

In addition to a high performance 32-bit CPU core, the RC32351 device incorporates a number of on-chip generic peripherals, including an SDRAM controller, a separate memory/IO controller supporting 8-, 16- and 32-bit peripherals, an interrupt controller, timers, and serial ports. The RC32351 device also integrates three on-chip peripherals specifically targeted for communications applications:

– A 10/100Mbps Ethernet controller
– An ATM segmentation and reassembly (SAR) capable of operating up to 25Mbps
– A USB device controller supporting data rates up to 12Mbps, fully compatible with version 1.1 of the USB specification

The RC32351 can be used in a variety of systems, and it can interface to a variety of different devices on each of its ports depending on system needs.

This application note presents the external devices that have been tested and are known to work with the RC32351. These devices can be used a guideline when designing systems based on the RC32351.

System Block Diagram

Figure 1 on page 2 represents a generic system block diagram based on the RC32351 and the different types of external peripherals that can be attached to the RC32351, from standard memory (FLASH, EPROM, SRAM, and SDRAM) to communications peripherals.

This document lists the various devices that have been tested and are known to work with the RC32351. These devices or similar ones are recommended for use with the RC32351.

The system testing of the various interfaces on the RC32351 occurred primarily on the 79RP351 reference design. The schematics and manual for this board are available on the IDT web site.

The information in the following sections lists only the major capabilities for each interface. The complete information about the capability of each of the interfaces on the RC32351 and all the possible configurations each interface supports is listed in the RC32351 User Reference Manual.
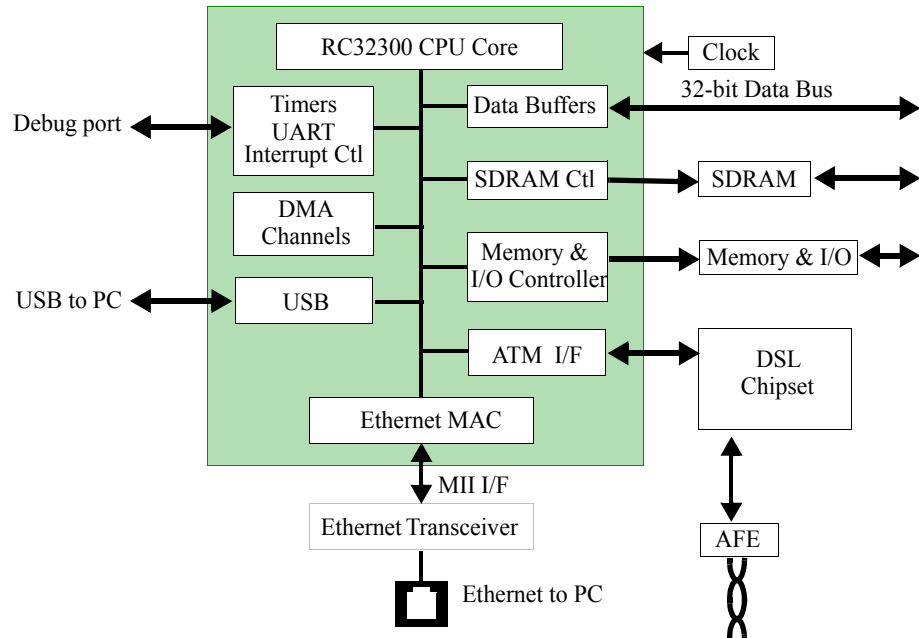
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Figure 1 Example of xDSL Residential Gateway Using RC32351

Peripheral Device Controller (Memory and IO Port)

The memory and IO port on the RC32351 is a generic port used to connect the RC32351 to a variety of memory and IO devices. It can be programmed to support various options such as:

- – *8-, 16- or 32-bit port width*
- – *FLASH, PROM, SRAM, and Dual-port memory*
- – *Up to 6 banks available, each controlled by a chip Select (CS), 64 MB per bank*
- – *Write protect capability per CS*
- – *Intel or Motorola style peripherals*
- – *Programmable access timing per bank*
- – *External wait-state generation*
- – *Direct control of optional external bus transceivers.*

All the modes and features of the Memory and IO port interface has been tested and validated. This module has been tested with the following devices and in the following configurations:

- – *FLASH:* **STMicroelectronics M28W160BT - 1M x 16**. *It is a single x16 FLASH (16-bit data path) device used on the 79RP351 reference design.*
- – *FLASH:* **AMD AM 29DL163CT - 90ET**. *2 x16 devices (32-bit data path) used on the 79RP355.*
- – *FLASH:* **AMD AM 29LV040B - 90JC**. *single x8 device (8-bit data path) used as the boot ROM on the 79RP355 reference design.*
- – *FLASH:* **28F016S3-120 2MB x 8 Intel**. *4 x8 devices (32-bit data path) used on the 79EB355 evaluation board.*
- – *SRAM:* **IDT71V016S-15 64K x 16**. *2 x16 devices (32-bit data path) used on the 79S355 board. The 79S355 board was developed to validate the functionality of the RC32351 device and is no longer available.*
- – *SRAM:* **IDT71V416S-15 256K x 16 IDT**. *2 x16 devices (32-bit data path) used on the 79S355 board.*
- – *EPROM:* **M27C801-100 ST Microelectronics**. *4 x8 devices (32-bit data path) used on the 79EB355 evaluation board.*
- – *IO:* **Dallas DS1511W RTC**. *Single x8 Real-time Clock used on the 79EB355 evaluation board.*
- – *IO:* **Seiko L1682B1J000**. *Single, x8 LCD display used on the 79EB355 evaluation board.*

SDRAM Controller

The SDRAM controller on the RC32351 is used to connect the device to the SDRAM memory. The SDRAM port is always 32-bit wide and can be programmed to support different types of SDRAMs and different configurations such as:

– *DIMM or SoDIMM*
– *4-bit, 8-bit, 16-bit, or 32-bit wide SDRAMs*
– *2 banks available, up to 512 MB per bank.*

All the modes and features of the SDRAM controller have been tested and validated. The SDRAM controller has been tested with the following devices and in the following configurations. The SDRAM interface has been tested at maximum speed (66MHz) on the board.

– **Hyundai HY57V653220B - 512K x 32 x 4**. *It is a single x32 SDRAM device that is used on the 79RP351 reference design.*
– **Hyundai HY57V651620B - 4Mb x 16**. *It is 2 devices, x16 SDRAM that are used on the 79RP355 reference design.*
– **Micron MT4LSDT464HG-10EC3 - 4Mb x 16**. *It is an SODIMM SDRAM module that is used on the 79EB355 evaluation board.*
– **MT8LSDT1664AG-10EB1**. *128MB (16Mx64) SODIMM 8chips x16 on the module, used on the 79EB355 evaluation board.*
– **MT8LSDT264AG-10BC4 16MB DIMM.** *8chips x16 on the module, used on the 79S355 evaluation board.*

Ethernet Controller

The RC32351 contains an on-chip Ethernet MAC capable of 10 and 100 Mbps line speed with a standard MII interface. It uses the MII interface to connect to external Ethernet transceivers. Some of the features of the Ethernet MAC on the RC32351 are listed below:

– *Full duplex support for 10 and 100 Mb/s*
– *IEEE 802.3u compatible Media Independent Interface MII with serial management interface*
– *IEEE 802.3u auto negotiation for automatic speed selection*
– *Flexible address filtering modes*
– *64-entry hash table based multicast address filtering.*

The Ethernet MAC controller has been tested with the following Ethernet transceivers, running at both 10 and 100 Mbps and in various modes and configurations:

– **Level one LXT972LC**. *3.3V, single port 10/100 Ethernet transceiver. This is used on the 79RP351, 79RP355, and the 79EB355 boards.*

ATM Interface

The RC32351 includes a configurable ATM interface that offers the following features and functions:

– *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
– *Supports 25Mb/s and faster ATM*
– *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
– *Supports standard 53-byte ATM cells*
– *Performs HEC generation and checking*
– *Discards short cells and clips long cells*
– *Provides 16 cells worth of buffering (8 cell input buffer and 8 cell output buffer)*
– *Hardware support for CRC-32 generation and checking for AAL5*
– *Hardware support for CRC-10 generation and checking*
– *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
– *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention.*

The ATM controller has been tested with the following devices and in various configurations:
– *DSL Chip set:* **Alcatel-ADSL Dynamite MTC 20156TQ-C (controller) and MTC 20154TQ-C (AFE)** *used on the 79RP351 and the 79RP355 reference designs.*
– *ATM PHY:* **IDT77V1053 IDT Triple Port Utopia II** *used on the 79EB355 evaluation board.*

USB Interface

The RC32351 includes the industry standard USB device interface to enable consumer appliances to directly connect to the PC. The USB interface on the RC32351 has a built-in transceiver to directly drive the USB cable / connector. USB features include the following:
– *Revision 1.1 compliant*
– *USB slave device controller*
– *A 6th USB endpoint*
– *Full speed operation at 12 Mb/s*
– *Control, interrupt, bulk and isochronous endpoints*
– *USB remote wakeup*
– *Integrated USB transceiver.*

The USB interface has been tested using a USB analyzer, as well as being connected to a single PC using the USB link.

Enhanced JTAG / ICE Interface

For low cost In-Circuit-Emulators, the RC32300 CPU core includes an enhanced JTAG (EJTAG) interface. The EJTAG / ICE interface has been tested in various configurations with the following In-Circuit-Emulators (ICEs):
– **MAJIC/MAJIC^{Plus} available from Embedded Performance Inc. (EPI)**
– **NetICE and ScanICE JTAG Emulator** *available from* **Corelis Inc.**
– **VisionClick ICE** *available from* **EST (Wind River Systems)**.

Software

Several Real Time Operating Systems (RTOS) have been ported and tested to the various boards built around the RC32351 (79EB351and 79RP351), as well as on various systems from end customers. These RTOS are either available through IDT or through the 3rd party vendor. The following is a list of the RTOS currently available for the RC32351:
– **VxWorks** *based on Tornado V2.1 from* **Wind River Systems**
– **Embedded Linux** *(based on* **Embedix** *from* **Lineo***) revision 2.4 available from* **IDT**
– **Nucleus** *PLus revision "IDT32364_GNU; v1.11.1" available from* **Accelerated Technology Inc***.*
– **ThreadX** *v4 available from* **Express Logic**.

Other systems are currently under development:

Summary

The RC32351 has been tested and validated on several boards at IDT as well as in several systems designed by customers. The devices listed in this document represent a sub-set of the devices that can be used with the RC32351. They are presented here as a guideline when designing systems around the RC32351.