PowerSpan II™ Schematic Review Checklist

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1. PowerSpan II Schematic Review Checklist

This checklist discusses the following schematic review topics for the PowerSpan II:

1.1 Overview

The *Schematic Review Checklist* offers design and termination recommendations for PowerSpan II applications. This document is intended for designers that are in the process of completing their PowerSpan II board schematics. For this reason, it is beneficial to review the contents of the checklist before routing your PowerSpan II-based board.

For more information about PowerSpan II hardware and software, see the *PowerSpan II User Manual*.

1.1.1 Signals

Table 1 describes the signal types found in the PowerSpan II.

Table 1: Signal Types

Signal Type	Definition
Input	Standard input only signal
Output	Standard output only signal
Tri-state Output	Standard tri-state output only signal
Open Drain	Open drain output — allows multiple devices to share as a wire-OR
Tri-state Bi-directional	Tri-state input/output signal
Bi-directional Open Drain	Open drain input/output — allows multiple devices to share as a wired-OR when used as output

1.1.2 Design Recommendation

It is advantageous to pull power up option signals high and have a jumper option to ground so the option can be changed after board production. Alternatively these can be controlled with a CPLD.

IDT experience has shown that designers who have built either jumpers or a CPLD into their designs have been able to significantly reduce the time it takes to bring their design up.

High Z or Weak pull-up is suggested to be 10K.
Regular pull-ups are suggested to be 4.7K unless otherwise noted.

1.1.3 Recommended Terminations

It is important to note that there is a distinction between host and adapter card recommendations on the PCI signals. If you are designing an adapter card only, you may not have to add certain terminations such as pull-ups on control signal lines. However, the pull-ups must exist somewhere in the complete system. Usually the host bridge to which you are connecting handles signals such as these. Here, we intend that the host bridge will be physically mounted on the system card or back plane.

The PCI signal section includes two recommendations for each signal: the first for the adapter card design (non-Host), the second for the host bridge. The second recommendation appears in parentheses, for example, (Host or Source Bridge: Weak Pull-up - 10K). This simply means that a 10K pull-up is expected somewhere on the host bridge side.

All of these recommendations are from the PCI 2.2 specification. If you have any questions about signal termination, it is recommended you review the appropriate sections of the latest PCI specification, available at www.pcisig.com.

1.1.4 Checkpoint

A Checkpoint section is included at the end of every signal. This is for the user to track the results of each signal recommendation in the Schematic Review.

- Pass — correct action taken
- Fail — no action or incorrect action taken
- Caution — problem with recommendation
- Help — user requires assistance or additional information

1.2 PB Signals

This section gives recommended terminations for PowerSpan II signals that connect to the PB bus.

1.2.1 PB_AACK_

PB Address Acknowledge: Tristate bidirectional

A processor bus slave asserts this signal to indicate that it identified the address tenure. Assertion of this signal terminates the address tenure.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.2 PB_ABB_

Address Bus Busy: Tristate output

Indicates ownership of the processor address bus.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.3 PB_AP[0:3]

Address Parity: Tristate bidirectional

The processor address bus master drives this signal to indicate the parity of the address bus.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.4 PB_ARTRY_

Address Retry: Tristate bidirectional

Assertion of this signal indicates that the bus transaction must be retried by the processor bus master.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.5 PB_A[0:31]

Address Bus: Tristate bidirectional

Address for the current bus cycle. It is driven by PowerSpan II when it is the bus master. At all other times it is an input to PowerSpan II.

Recommended termination: Pull-up resistors are not required on the processor bus address (PB_A[0:31]) signals to guarantee functional operation of the PowerSpan II. However, adding resistors to the address signals minimizes the current drawn by the PowerSpan II's tristated buffers when the bus is in an idle condition. The system designer must decide whether to add these resistors to the address signals.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.6 PB_BG[1]_

Address Bus Grant: Tristate bidirectional

This is an input when an external arbiter is used and an output when the internal arbiter is used. As input it is used by an external arbiter to grant the processor address bus to PowerSpan II. As output it is used by the internal arbiter to grant the processor address bus to an external bus master.

Recommended termination: Hi-Z weak pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.7 PB_BG[2:3]_

Address Bus Grant: Tristate output

Used by the internal arbiter to grant the processor address bus to the external bus masters.

Recommended termination: Hi-Z weak pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.8 PB_BR[1]_

Address Bus Request: Tristate bidirectional

This is an output when an external arbiter is used and an input when an internal arbiter is used. As output it indicates that PowerSpan II requests the ownership of the processor address bus. As input an external master should assert this signal to request the ownership of the processor address bus from PowerSpan II's internal arbiter.

Recommended termination: Hi-Z weak pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.9 PB_BR[2:3]_

Address Bus Request: Input

These are inputs only. They are used by external masters to request the processor address bus from the internal arbiter.

Recommended termination: Hi-Z weak pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.10 PB_CI_

Cache Inhibit: Tristate output

It is used for L2 cache control. It indicates whether the transaction should be cached or not.

Recommended termination: Hi-Z pull-up resistor (can be NC if unused)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.11 PB_CLK

Processor Bus Clock: Input

All devices intended to interface with the bus processor side of the PowerSpan II must be synchronized to this clock. It must be provided by external clock generator and must be a free-running clock (The clock frequency must be stable before the deassertion of PO_RST_).

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.12 PB_DBB_

Data Bus Busy: Tristate output

Indicates the ownership of the data bus. The master who owns the processor data bus asserts this signal.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.13 PB_DBG[1]_

Data Bus Grant: Tristate bidirectional

This is an input when an external arbiter is used and an output when the internal arbiter is used. As input it is used by an external arbiter to grant the processor data bus to PowerSpan II. As output it is used by the internal arbiter to grant the processor data bus to an external bus master.

Recommended termination: Hi-Z weak pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.14 PB_DBG[2:3]_

Data Bus Grant: Tristate output

This is an output only. It is used by the internal arbiter to grant the processor data bus to external bus masters.

Recommended termination: Hi-Z weak pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.15 PB_DP[0:7]

Data Parity: Tristate bidirectional

The processor data bus slave drives on reads, master drives on writes to indicate the parity of the data bus.

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.16 PB_DVAL_

Data Valid: Tristate bidirectional

Indicates if the data beat is valid on PB_D[0:63].

Recommended termination: Hi-Z Pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.17 PB_D[0:63]

Data Bus: Tristate bidirectional

Recommended termination: Pull-up resistors are not required on the processor bus data (PB_D[0:63]) signals to guarantee functional operation of the PowerSpan II. However, adding resistors to the data signals minimizes the current drawn by the PowerSpan II's tristated buffers when the bus is in an idle condition. The system designer must decide whether to add these resistors to the data line.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.18 PB_FAST

PLL Configuration/PB arbiter selection: Input

This pin is a multiplexed system pin in the power-up options. When PO_RST_ is low, it is used for PowerSpan II selecting internal PB Interface PLL frequency. When PO_RST_ is negated, it is used for a power-up option enabling/disabling the PB arbiter.

Recommended termination: Jumper or CPLD

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.19 PB_GBL_

Global: Tristate output

Indicates that the transfer is coherent and it should be snooped by bus masters.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.20 PB_RSTCONF_

Reset Configuration: Input (Schmitt trigger)

Asserted by MPC8260 master to indicate to PowerSpan II to load power-up options. This pin must be pulled high if the multiplexed system pin mechanism is used to load the power-up options.

Recommended termination: For MPC8260 configuration slave mode, the signal must be connected to one of the 60x address lines from A0 to A6, pull-up.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.21 PB_RST_

Reset: open drain bidirectional (Schmitt trigger)

Reset: Asynchronous active low reset. Normally, this pin is connected to HRESET_ pin of the MPC8260. In PCI host application, this pin is configured as an input by PB_RST_DIR pin. While in non-Host application, this pin is configured as output. Please note, even though this pin is configured as output, its input buffer still open to sense the 60x bus reset from HRESET_ of MPC8260.

Recommended termination: Pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.22 PB_RST_DIR

Reset Direction: Input

Power-up option Processor Bus Reset Direction

Recommended termination: Logic low = PB_RST is input; Logic high = PB_RST_ is output

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.23 PB_TA_

Transfer Acknowledge: Tristate bidirectional

Indicates that a data beat is valid on the data bus. For single beat transfers, it indicates the termination of the transfer. For burst transfers, it will be asserted four times to indicate the transfer of four data beats with the last assertion indicating the termination of the burst transfer.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.24 PB_TBST_

Transfer Burst: Tristate bidirectional

The bus master asserts this pin to indicate that the current transaction is a burst transaction

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.25 PB_TEA_

Transfer Error Acknowledge: Tristate bidirectional

Indicates a bus error.

Recommended termination: Hi-Z Pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.26 PB_TSIZ[0:3]_

Transfer Size: Tristate bidirectional

Indicates the number of bytes to be transferred during a data tenure.

Recommended termination: Disconnect and pull-down on TSIZ[0] for non-MPC8260 applications. When using MPC8260, connect point-to-point (for example, Tsiz[0] to Tsiz[0],etc.)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.27 PB_TS_

Transfer Start: Tristate bidirectional

Indicates the beginning of a new address bus tenure.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.28 PB_TT[0:4]

Transfer Type: Tristate bidirectional

The bus master drives these pins to specify the type of the transaction.

Recommended termination: Pull-up resistors are not required to guarantee functional operation of the PowerSpan II. However, adding resistors to the signals minimizes the current drawn by the PowerSpan II's tristated buffers when the bus is in an idle condition. The system designer must decide whether to add these resistors to this signal.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.29 PB_DVDD

PB PLL digital power: Supply

Voltage supply pin to the analog circuits in the PB Phase Locked Loop (nominally 2.5V). Suggested design is to use a separated power supply apart from MPC8260's Vdd_Core for supporting future MPC8260 revision.

Recommended termination: Refer to the recommended external decoupling circuit design in PowerSpan II User's Manual.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.30 PB_AVSS

PB PLL analog ground: Supply

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.31 PB_DVSS

PB PLL digital ground: Supply

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3 PCI-1 Signals

This section gives recommended terminations for PowerSpan II signals that connect to the PCI-1 bus.

1.3.1 P1_AD [63:0]

PCI-1 Address/Data Bus: Tristate bidirectional

Address and data are multiplexed over these pins providing a 64-bit address/data bus. In a 32 Bit system, unused upper 32-bit portion need not be connected and can left open. PowerSpan II drives upper 32-bit AD lines stable in 32-bit environment.

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.2 P1_ACK64_

PCI-1 Acknowledge 64-bit Transaction: Tristate bidirectional

Active low signal asserted by a target to indicate its willingness to participate in a 64-bit transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.

Recommended termination:

- Host with 64-bit agents: Pull-up
- Non-host with 64-bit agents: No requirement
- Host with 32-bit agents only: No requirement
- Non-host with 32-bit agents only: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.3 P1_CBE[7:0]_

Bus Command and Byte Enable Lines: Tristate bidirectional

PCI-1 bus Command and byte enable information is multiplexed over all eight CBE lines.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.4 P1_DEVSEL_

PCI-1 Device Select: Tristate bidirectional

An active low indication from an agent that is the target of the current transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.5 P1_FRAME_

PCI-1 Cycle Frame for PCI Bus: Tristate bidirectional.

An active low indication from the current bus master of the beginning and end of a transaction. Driven by the bus master; sampled by the selected target. Rescinded by the bus master at the end of the transaction.

Recommended termination:

- Host: pull-up
- non-Host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.6 P1_GNT[1]_

PCI-1 Grant: Tristate bidirectional

This is an input when an external arbiter is used and an output when the internal arbiter is used. As an input it is used by the external arbiter to grant the bus to PowerSpan II. As an output it is used by the internal arbiter to grant the bus to an external master.

Recommended termination: Weak Pull-up or none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.7 P1_GNT[4:2]_

PCI-1 Grant: Tristate output

These are outputs only. Used by the PCI-1 internal arbiter to grant the bus to external masters.

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.8 PCI_GNT[7:5]_

PCI-1 Grant: Tristate output

These outputs may be driven by the PCI-1 or PCI-2 internal arbiter to grant the bus to external masters. They are assigned to PCI-1 or PCI-2 by software.

Recommended termination: Weakly pulled high

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.9 P1_IDSEL

PCI-1 Initialization Device Select: Input

Used as a chip select during PCI Configuration read and write transactions.

Recommended termination:

- Host: Pull-down
- Non-host: Connect to one of address line P1_AD[31]~[16]

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.10 P1_INTA_

PCI-1 Interrupt A: Bidirectional open drain

An active low level sensitive indication of an interrupt. Asynchronous to P1_CLK.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.11 P1_IRDY_

PCI-1 Initiator Ready: Tristate bidirectional

An active low indication of the current bus master's ability to complete the current data phase. Driven by the master; sampled by the selected target.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.12 P1_PAR

PCI-1 parity: Tristate bidirectional

Carries even parity across P1_AD[31:0] and P1_C/BE[3:0]. Driven by the master for the address and write data phases. Driven by the target for read data phases.

Recommended termination: Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.13 P1_PAR64

PCI-1 Parity Upper Dword: Tristate bidirectional

Carries even parity across P1_AD[63:32] and P1_CBE[7:4]. Driven by the master for address and write data phases. Driven by the target for read data phases.

Recommended termination:

- 64 bit mode: pull-up
- 32 bit mode: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.14 P1_CLK

PCI-1 Clock: Input

Clock input for the PCI-1 Interface: P1_CLK operates between 25 and 66MHz.The P1_CLK must be provided by external clock generator and must be a free-running clock (The clock frequency must be stable before the deassertion of PO_RST_).

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.15 P1_M66EN

PCI-1 66 MHz Enable: Input

This pin is a multiplexed system pin in Power-up option. When PO_RST is low, it is used for PowerSpan II selecting internal PCI-1 Interface PLL frequency. When PO_RST_ negation, it is used for power-up option enabling/disabling PCI-1 arbiter.

Recommended termination: Jumper or CPLD.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.16 P1_PERR_

PCI-1 Parity Error: Tristate bidirectional

An active low indication of a data parity error.Driven by the target receiving data. Rescinded by that agent at the end of the transaction.

Recommended termination: No requirement

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.17 P1_REQ[1]_

PCI-1 Bus Request: Tristate bidirectional

This is an output when an external arbiter is used and an input when the PCI-1 internal arbiter is used. As input it is used by an external master to request the bus. As output it is used by PowerSpan II to request the bus.

Recommended termination: Weak pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.18 P1_REQ[4:2]_

PCI-1 Bus Request: Input

These are inputs only. Can be used by external masters to request the bus through the PCI-1 arbiter. PCI_REQ[7:4]_ signals do not meet the PCI 66 MHz Specification, but they do meet the PCI 33 MHz Specification.

Recommended termination: Weak pull-up. For unused lines, one pull-up resistor can be used for all unused pins to save space.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.19 PCI_REQ[7:5]_

PCI-1 Bus Request: Input

These inputs are used by external masters to request the bus from the PCI-1 or PCI-2 arbiter. They are assigned to PCI-1 or PCI-2 by software.

Recommended termination: Weak pull-up. For unused pins, one pull-up resistor can be used for all unused pins to save space.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.20 P1_REQ64_

PCI-1 Request 64-bit Transfer: Tristate bidirectional

An active low indication from the current master of its choice to perform 64-bit transactions. Rescinded by the bus master at the end of the transaction.

Recommended termination:

- 64-bit environment: pull high
- 32-bit environment: pull high (not bussed)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.21 P1_RST_

PCI-1 Reset: Tristate bidirectional

Asynchronous active low reset for PCI-1 Interface. Can be selected as either input or output by P1_RST_DIR pin. Normally, it is selected as input in PCI non-Host application or output in PCI host application.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.22 P1_SERR_

PCI-1 System Error: Open drain

An active low indication of address parity error.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.23 P1_STOP_

PCI-1 Stop: Tristate bidirectional

An active low indication from the target of its desire to stop the current transition. Sampled by the master. Rescinded by the target at the end of the transaction.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.24 P1_TRDY_

PCI-1 Target Ready: Tristate bidirectional

An active low indication of the current target's ability to complete the data phase. Driven by the target; sampled by the current bus master. Rescinded by the target at the end of the transaction.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.25 P1_64EN_

PCI-1 64-bit Enable: Input

An active low indication that a CompactPCI Hot Swap board is in a 64-bit slot.

Recommended termination for non-Hot swap application:

- Host application: pull low. In order to enable driving P1_REQ64_ during P1_RST negation when Power Up option choose P1_R64_EN.
- Non-Host application: pull high. In order to enable sampling of P1_REQ64_ during P1_RST negation to determine the width of the datapath. Please refer to Chapter 3 in the *PowerSpan II User's Manual* for the details.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.26 P1_RST_DIR

PCI-1 bus reset direction: Input (LVTTL)

Recommended termination:

- Logic low = P1_RST_ is input
- Logic high= P1_RST_ is output

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.27 P1_DVDD

PCI-1 PLL's digital power: Supply

Voltage supply pin to the circuits in the PCI-1 Phase Locked Loop, nominally 2.5 volts.

Recommended termination: Refer to the recommended external decoupling circuit design in PowerSpan II User's Manual.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.28 P1_AVSS

PCI-1 PLL's analog ground: Supply

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.29 P1_DVSS

PCI-1 PLL's digital ground: Supply

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4 PCI-2 Signals

This section is only valid for PowerSpan II Dual PCI port device (CA91L8200B-100CE). It gives recommended terminations for PowerSpan II signals that connect to the PCI-2 bus.

1.4.1 P2_AD[31:0]

PCI-2 Address/Data Bus: Tristate bidirectional

Address and data are multiplexed over these pins providing a 32-bit address/data bus.

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.2 P2_CBE[3:0]_

PCI-2 Bus Command and Byte Enable Lines: Tristate bidirectional

Command and byte enable information is multiplexed over all four CBE lines.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.3 P2_DEVSEL_

PCI-2 Device Select: Tristate bidirectional

An active low indication from an agent that is the target of the current transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.

Recommended termination: No requirement

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.4 P2_FRAME_

PCI-2 Cycle Frame for PCI Bus: Tristate bidirectional

An active low indication from the current bus master of the beginning and end of a transaction. Driven by the bus master, sampled by the selected target. Rescinded by the bus master at the end of the transaction.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.5 P2_GNT[1]_

PCI-2 Grant: Tristate bidirectional

This is an input when an external arbiter is used and an output when the PCI-2 internal arbiter is used. As input it is used by the external arbiter to grant the bus to PowerSpan II. As output it is used by the PCI-2 internal arbiter to grant the bus to an external master.

Recommended termination: Weakly pulled high

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.6 P2_GNT[4:2]_

PCI-2 Grant: Tristate output

These are outputs only. They are used by the PCI-2 internal arbiter to grant the bus to external masters.

Recommended termination: Weakly pulled high

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.7 P2_IDSEL

PCI-2 Initialization Device Select: Input

Used as a chip select during Configuration read and write transactions.

Recommended termination:

- Host = pull-low.
- non-Host = Connect to one of address line P2_AD[31]~[16].

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.8 P2_INTA_

PCI -2 Interrupt A: Bidirectional open drain

An active low, level sensitive indication of an interrupt. Asynchronous to P2_CLK.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.9 P2_IRDY_

PCI-2 Initiator Ready: Tristate bidirectional

An active low indication of the current bus master's ability to complete the current data phase. Driven by the master; sampled by the selected target.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.10 P2_PAR

PCI-2 Parity: Tristate bidirectional

Carries even parity across P2_AD[31:0] and P2_CBE[3:0]. Driven by the master for the address and write data phases. Driven by the target for read data phases.

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.11 P2_CLK

PCI-2 Clock: Input

Clock input for the PCI-2 Interface. P2_CLK operates between 25 and 66MHz.The P2_CLK must be provided by external clock generator and must be a free-running clock (The clock frequency must be stable before the deassertion of PO_RST

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.12 P2_M66EN

PCI-2 66 MHz Enable: Input

This pin is a multiplexed system pin in Power-up option. When PO_RST is low, it is used for ***PowerSpan II*** *selecting internal PCI-2 Interface PLL frequency. When PO_RST negation, it is used for Power Up option enabling/disabling PCI-2 arbiter*

Recommended termination: A jumper or CPLD

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.13 P2_PERR_

PCI-2 Parity Error: Tristate bidirectional

An active low indication of a data parity error.Driven by the target receiving data. Rescinded by that agent at the end of the transaction.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.14 P2_REQ[1]

PCI-2 Bus Request: Tristate bidirectional

This is an output when an external arbiter is used and an input when the PCI-2 Interface internal arbiter is used. As input it is used by an external master to request the bus. As output it is used by PowerSpan II to request the bus.

Recommended termination: Weakly pulled high.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.15 P2_REQ[4:2]_

PCI-2 Bus Request: Input

These are inputs only. They can be used by external masters to request the bus from the PCI-2 arbiter.

Recommended termination: Weakly pulled high.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.16 P2_RST_

PCI-2 Reset: Tristate bidirectional

Asynchronous active low reset for PCI-2 Interface.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.17 P2_SERR_

PCI-2 System Error: Open drain

An active low indication of address parity error.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.18 P2_STOP_

PCI-2 Stop: Tristate bidirectional

An active low indication from the target of its desire to stop the current transition. Sampled by the master. Rescinded by the target at the end of the transaction.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.19 P2_TRDY_

PCI-2 Target Ready: Tristate bidirectional

An active low indication of the current target's ability to complete the data phase. Driven by the target; sampled by the current bus master. Rescinded by the target at the end of the transaction.

Recommended termination:

- Host: pull-up
- Non-host: no pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.20 P2_RST_DIR

PCI-2 Bus Reset Direction: Input (LVTTL)

Recommended termination:

- Logic Low: P2_RST is output
- Logic high: P2_RST is output

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.21 P2_DVDD

PCI-2 PLL's digital power: Supply

Voltage supply pin to the analog circuits in the PCI-2 Phase Locked Loop, (nominally 2.5V).

Recommended termination: Refer to the recommended external decoupling circuit design in PowerSpan II User's Manual

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.22 P2_AVSS

PCI-2 PLL's analog ground: Supply

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.23 P2_DVSS

PCI-2 PLL's digital ground: Supply

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5 Miscellaneous Signals

1.5.1 INT[5:0]

Interrupt: Bidirectional open drain (5V tolerant LVTTL Schmitt trigger)

General purpose interrupt pins

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.2 ENUM_

System Enumeration: Open drain output (PCI)

Used to notify system host that a board has been freshly inserted or extracted from the system.

Recommended termination: Hi-Z pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.3 ES

Ejector Switch: Input (5V tolerant LVTTL Schmitt trigger)

Indicates the status of Hot Swap board ejector switch. A logic high value indicates the switch is closed.

Recommended termination:

- non-Hot Swap environment= pull down,
- Hot swap = connect to ejector switch

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.4 LED_

LED: Open drain output (5V tolerant LVTTL)

Controls the Hot Swap status LED

Recommended termination:

- Hot Swap = Connect to LED circuit on the board.
- non-Hot Swap = no resistor requirement.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.5 HEALTHY_

Board Healthy: Input (5 V tolerant LVTTL Schmitt trigger)

In a Hot Swap environment, indicates the board is ready to be released from reset and become an active agent on PCI. Negation of this signal resets all PowerSpan II resources, including PLL's. Additionally, all PowerSpan outputs are tristated when this pin is negated; inputs and bidirects are inhibited. There is timing requirement between HEALTHY_ and PO_RST_, please refer to AC timing section in PowerSpan II User's Manual.

Recommended termination:

- non-Hot Swap environment = pull down via a jumper.(Jumper make debugging flexible)
- Hot Swap = connect to Hot Swap controller

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.6 PO_RST_

Power On Reset: Input (5 V tolerant LVTTL Schmitt trigger)

Assertion of this signal resets all PowerSpan II resources, including PLL's. The designer must make sure all the external clocks running at expected frequency before the negation of PO_RST_.

Recommended termination:

Usually connected to main reset signal circuitry

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.7 I2C_SCLK

Serial Clock: Open drain Output (5 V tolerant LVTTL)

EEPROM Serial clock. In design, whether to use an EEPROM is up to the designer. In most application, EEPROM is not needed. The I2C_CLK signal can be pulled up by a resistor. However, when choosing serial EEPROM, it is recommended to use the one with WP ("write protection") feature (e.g. ATMEL AT24C08A) and implement a jumper on WP pin.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.8 I2C_SDA

Serial Data: Bidirectional open drain (5 V tolerant LVTTL)

EPROM Serial data line.In design, whether to use an EEPROM is up to the designer. In most application, EEPROM is not needed. The I2C_SDA signal can be pulled up by a resistor.

Recommended termination: Hi-Z pull-up resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.9 Vdd25

Core power: Supply

Nominally 2.5V

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.10 Vdd33

IO power: Supply

Nominally 3.3V

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.11 VSS

Core ground: Supply

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.12 VSS_IO

IO ground: Supply

Recommended termination: No requirement

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.13 TCK

Test Clock (JTAG): Input (LVTTL)

Used to clock state information and data into and out of the device during boundary scan.

Recommended termination:

- Used =Hi-Z pull-up
- Unused = pull-up or pull-down

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.14 TMS

Test Mode Select (JTAG): Input (LVTTL) with Internal pull-up resistor

Used to control the state of the Test Access Port controller

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.15 TDI

Test Data Input (JTAG): Input (LVTTL) with Internal pull-up resistor

Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream.

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.16 TDO

Test Data Output (JTAG): Tristate output (LVTTL)

Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream.

Recommended termination: none

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.17 TRST_

Test Reset (JTAG): Input (LVTTL) (Schmitt trigger)

Asynchronous reset for the JTAG controller. This pin must be asserted during the power-up reset sequence to ensure that the Boundary Scan Register elements are configured for normal system operation. Customers must assert TRST concurrently with PO_RST as part of the power-up reset sequence.

Recommended termination: Pull-down resistor (=1 Kohm) if JTAG is not used in the system. Otherwise the signal must be toggled with the PO_RST signal.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.18 TE

Test Enable: Input

Enables manufacturing test.

Recommended termination: Pull-down resistor

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.19 PB_TEST1

IDT Internal Test Input (internal pull-down)

Enables manufacturing test.

Recommended termination: Pull-down resistor or open

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.20 PB_TEST2

IDT Internal Test Input (internal pull-down)

Enables manufacturing test.

Recommended termination: Pull-down resistor or open

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.21 P1_TEST1

IDT Internal Test Input (internal pull-down)

Enables manufacturing test.

Recommended termination: Pull-down resistor or open

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.22 P1_TEST2

IDT Internal Test Input (internal pull-down)

Enables manufacturing test.

Recommended termination: Pull-down resistor or open

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.23 P2_TEST1

IDT Internal Test Input (internal pull-down)

Enables manufacturing test.

Recommended termination: Pull-down resistor or open

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.24 P2_TEST2

IDT Internal Test Input (internal pull-down)

Enables manufacturing test.

Recommended termination: Pull-down resistor or open

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

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