

User Manual

DA9231 DA9230 Evaluation Board - 342-03-A

UM-PM-040

DA9231 DA9230 Evaluation Board - 342-03-A

Contents

Contents	2
Figures	2
Tables	3
1 Introduction	4
2 Board Descriptions	5
2.1 Board Overview	5
2.2 Connectors and Test Points Descriptions	6
2.3 Default Board Setup	7
3 Test Setup	8
3.1 Recommended Operating Conditions	8
3.2 Recommended Test Equipment	9
3.2.1 Power Supply Requirement	9
3.2.2 Load Requirement	9
3.2.3 Multimeters	9
3.3 Recommended Test Setup	9
3.3.1 No-Load Input Current Measurement Setup	9
3.3.2 Buck Efficiency Measurement Setup	10
3.3.3 LDO Measurement	11
3.3.4 I ² C and GPO Pull-Up Supply	11
3.4 Software GUI	12
3.4.1 I ² C Address Re-configuration	12
3.4.2 Device OTP Information	12
3.4.3 Device Configuration and Status Monitor	13
4 Schematic	15
5 Board Layout and Bill of Materials	16
5.1 Board Layout	16
5.2 Bill of Materials	20

Figures

Figure 1: 342-03-A Evaluation Board Top View	5
Figure 2: 342-03-A Evaluation Board Top Overlay (Solution Size: 18 mm ²)	5
Figure 3: Recommended Setup for No-Load Input Current Measurement	10
Figure 4: Recommended Setup for Buck Efficiency Measurement	10
Figure 5: Recommended Setup for LDO Measurement	11
Figure 6: Dialog USB Module 162-09	12
Figure 7: Open GUI Settings	12
Figure 8: Example of Re-configure GUI I ² C address	12
Figure 9: Read Device OTP information	13
Figure 10: DA9231 GUI Control Page	14
Figure 11: 342-03-A Evaluation Board Schematic	15
Figure 12: Top Layer	16
Figure 13: Inner Layer-2	17
Figure 14: Inner Layer-3	18
Figure 15: Bottom Layer	19

DA9231 DA9230 Evaluation Board - 342-03-A

Tables

Table 1: Descriptions of Connectors and test points on Board 342-03-A 6
Table 2: Descriptions of Default OTP Settings 7
Table 3: Default Jumper Position 7
Table 4: Recommended Operating Conditions 8

DA9231 DA9230 Evaluation Board - 342-03-A

1 Introduction

DA9231 is an ultra-low quiescent current PMIC, highly optimized for wearables and home-automation applications. The device has a buck converter that is efficient down to 10 μA and a nano-ampere LDO with an independent power input which can be connected to either the battery or buck output.

DA9230 is the device with only a single ultra-low quiescent buck converter.

Both DA9231 and DA9230 have the same compact WLCSP package and compatible footprint.

The 342-03-A evaluation board accommodates either DA9231 or DA9230 device. It operates from 5.5 V to 2.5 V input voltage and supports full performance of DA9231 or DA9230. The key feature of evaluation board 342-03-A includes:

- Ultra-low no load operating current:
 - 750 nA typical input current when buck switching at no load (DA9230)
 - 1.35 μA typical total input current when buck switching at no load and LDO enabled at no load (DA9231)
- 1.25 mm x 1.65 mm WLCSP package and 5 external components for a compact solution size of 18 mm²
- Configurable wide buck output range: 0.6 V to 1.9 V with 50 mV step, and support up to 300 mA load current.
- Configurable wide LDO output range: 0.7 V to 3.3 V with 100 mV step, and support up to 100 mA load current.
- Interface for I²C control. Paired with Dialog's USB module and SmartCanvas GUI.

DA9231 DA9230 Evaluation Board - 342-03-A

2 Board Descriptions

2.1 Board Overview

Figure 1 is the top view of the board 342-03-A and Figure 2 shows the top overlay with 18 mm² layout solution size highlighted.



Figure 1: 342-03-A Evaluation Board Top View

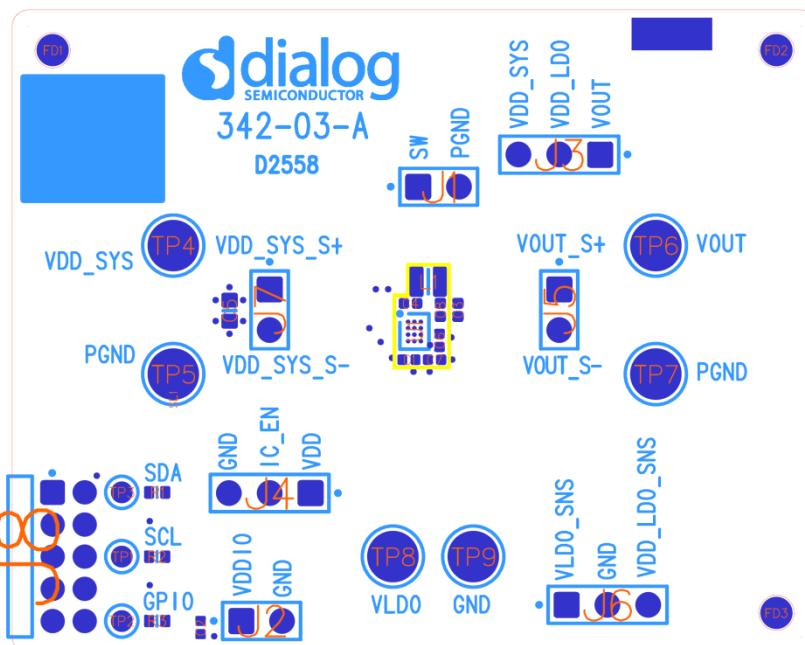


Figure 2: 342-03-A Evaluation Board Top Overlay (Solution Size: 18 mm²)

DA9231 DA9230 Evaluation Board - 342-03-A

2.2 Connectors and Test Points Descriptions

Table 1 describes the pin names and functions of the connectors and test points used on the board.

Table 1: Descriptions of Connectors and test points on Board 342-03-A

Connectors/ Test Points	Pin1 / Pin2 / Pin3 Name	Descriptions
J1	SW / PGND	Connector for sensing buck switching node.
J2	VDDIO / GND	Connector for external pull-up voltage on SDA, SCL and GPO pins.
J3	VOOUT / VDD_LDO / VDD_SYS	LDO input source selector. LDO input VDD_LDO can be selected from either VDD_SYS or buck VOOUT.
J4	VDD / IC_EN / GND	IC_EN input signal selector. Connect IC_EN to VDD enables the IC; connect IC_EN to GND completely disable the IC.
J5	VOOUT_S+ / VOOUT_S-	Buck output voltage Kelvin sense. Measure the buck output voltage at this connector for best accuracy.
J6	VLDO_SNS / GND / VDD_LDO_SNS	VDD_LDO_SNS: LDO input voltage Kelvin sense point. VLDO_SNS: LDO output voltage Kelvin sense point. Measure the LDO input and output voltage at this connector for best accuracy.
J7	VDD_SYS_S+ / VDD_SYS_S-	Buck input VDD_SYS voltage Kelvin sense. Measure the buck input voltage at this connector for best accuracy.
J8		10-pin connector. Connect to Dialog USB module for I ² C communication to GUI.
TP1	SCL	Test point. Connect to SCL pin of DUT (U1).
TP2	GPIO	Test point. Connect to GPO pin of DUT (U1).
TP3	SDA	Test point. Connect to SDA pin of DUT (U1).
TP4	VDD_SYS	Terminal for buck power input. Apply buck supply voltage between TP4 and TP5.
TP5, TP7	PGND	Terminals for power ground.
TP6	VOOUT	Terminal for buck output. Connect electronic load between TP6 and TP7.
TP8	VLDO	Terminal for LDO output. Connect electronic load between TP8 and TP9.
TP9	GND	Terminal for analog ground.

DA9231 DA9230 Evaluation Board - 342-03-A

2.3 Default Board Setup

The 342-03-A evaluation board is pre-programmed to the default OTP settings according to the device OTP number shown in [Table 2](#) and using the default jumper positions as shown in [Table 3](#).

I²C communication is not required for powering up the board though it can be used to re-configure the device features or monitor the device status.

Table 2: Descriptions of Default OTP Settings

Device OTP number	Buck V _{OUT} (V)	LDO V _{OUT} (V)	I ² C Address
DA9230_07VZ2	0.6 V	N/A	2F
DA9230_08VZ2	0.8 V	N/A	2F
DA9230_09VZ2	1.2 V	N/A	2F
DA9230_0AVZ2	1.8 V	N/A	2F
DA9231_0BVZ2	1.8 V	3.3	2F
DA9231_0CVZ2	0.6 V	3.3	2F
DA9231_0DVZ2	1.2	3.0	2D
DA9231_0EVZ2	1.8	Load Switch	2F

Table 3: Default Jumper Position

Jumper	Default Position
J3	VDD_LDO = VDD_SYS
J4	IC_EN = VDD
J1, J2, J5, J6, J7, J8	Open

3 Test Setup

3.1 Recommended Operating Conditions

The recommended operating conditions for board 342-03-A are shown in [Table 4](#).

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDD_SYS, VDD	Input voltage Range	VDD_SYS = VDD	2.5 Note 1		5.5	V
VDD_LDO	Input Voltage Range for LDO mode		1.8		VDD	V
	Input Voltage Range for Load Switch mode		0.8		VDD	V
I _{SW}	Output DC Current from SW				300	mA
I _{LDO}	Output DC Current from LDO				100	mA
T _A	Operation ambient Temperature Range		-40		85	°C

Note 1 Requires minimal 2.75 V for start-up. Once started, input voltage range can down to 2.5 V.

DA9231 DA9230 Evaluation Board - 342-03-A

3.2 Recommended Test Equipment**3.2.1 Power Supply Requirement**

To support full-load operation, it requires one DC power supply (PS#1) capable of supplying VDD_SYS with 5.5 V at 0.5 A.

3.2.2 Load Requirement

Load #1: To support full-load operation of buck, it requires an electronic load or source meter that is capable of sinking 300 mA load current with 1 μ A resolution. Fine resolution is required for efficiency sweep over load current at light load condition, for example Keithley 2460.

Load #2: To support full-load operation of LDO, it requires an electronic load or source meter that is capable of sinking 100 mA load current.

3.2.3 Multimeters

Voltage meter VM#1, VM#2, VM#3, VM#4: The voltage meters must have an input resistance > 10 G Ω to prevent drawing too much current that can affect quiescent current and efficiency measurement, for example Keithley 2700, 2000/1/2.

Current meter CM#1: The buck input current meter must be able to measure 500 mA current. It also requires current resolution at least 1 nA to measure no-load operating current, for example Keithley 2001/2.

Current meter CM#2: The buck output current meter must be able to measure 300 mA current. It also requires current resolution at least 1 μ A for efficiency sweep over load current.

3.3 Recommended Test Setup

Set the jumper position according to [Table 3](#) or refer to [Figure 1](#) (Install J3 and J4). Then follow the guideline for recommended test equipment setup.

3.3.1 No-Load Input Current Measurement Setup

Due to the ultra-low no-load operating current of DA9231 or DA9230, any in-proper setup can result in a significant measurement error. The following guidelines provide the recommended setup for no-load input current measurement, also shown in [Figure 3](#).

1. Select a proper DC power supply PS#1 according to [Section 3.2.1](#) and turn it off. Connect the positive output of PS#1 through a current meter (CM#1) to VDD_SYS terminal (TP4) and negative output to Terminal PGND (TP5).
2. Remove all oscilloscope probes from the board as they could draw significant current from the board if their input impedance is not high enough.
3. Disconnect VOUT terminal (TP6) from any load equipment since the load equipment could still draw leakage current from VOUT even if it is in OFF state.
4. Turn on PS#1. Read CM#1 after it is settled.

DA9231 DA9230 Evaluation Board - 342-03-A

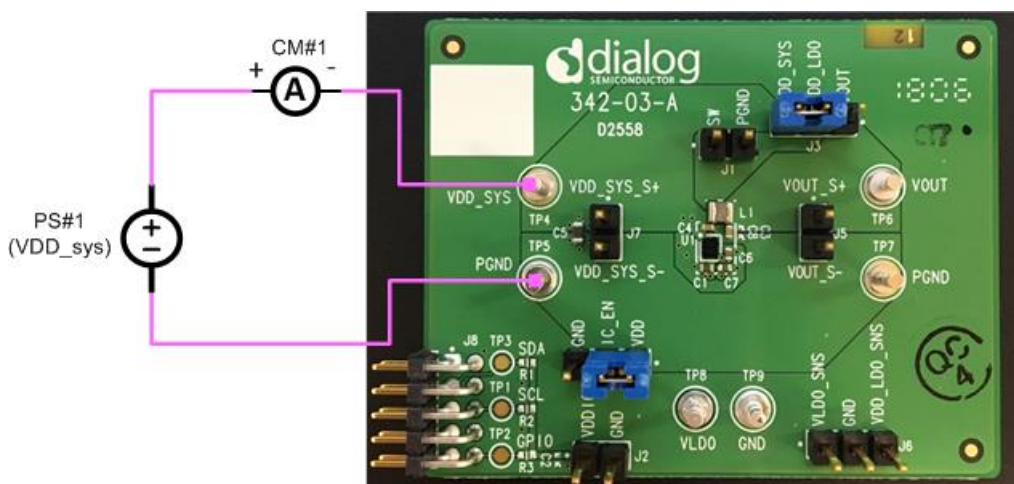


Figure 3: Recommended Setup for No-Load Input Current Measurement

3.3.2 Buck Efficiency Measurement Setup

The following guidelines provide the recommended test equipment setup for buck efficiency measurement. The test setup is also shown in Figure 4.

1. Select a proper DC power supply PS#1 according to Section 3.2.1 and turn it off. Connect the positive output of PS#1 through a current meter (CM#1) to VDD_SYS terminal (TP4) and negative output to Terminal PGND (TP5).
2. Connect a voltage meter (VM#1) to J7. Connect a voltage meter (VM#2) to J5.
3. Select a proper load equipment Load#1 according to Section 3.2.2 and turn it off. Connect Load#1 terminal through a current meter (CM#2) to VOUT terminal (TP6) and the other terminal to Terminal PGND (TP7). Make sure the current always drawn from VOUT (TP6) and flow into PGND (TP7).
4. Turn on PS#1. Check VM#2 is showing OTP programmed buck V_{OUT} voltage.
5. Turn on Load#1. Adjust Load#1 current to measure VM#1, VM#2, CM#1 and CM#2 and calculate efficiency over load current.



Figure 4: Recommended Setup for Buck Efficiency Measurement

DA9231 DA9230 Evaluation Board - 342-03-A

3.3.3 LDO Measurement

The following guidelines provide the recommended test equipment setup for LDO measurement. The test setup is also shown in [Figure 5](#).

1. Select a proper DC power supply PS#1 according to Section 3.2.1 and turn it off. Connect the positive output of PS#1 to VDD_SYS terminal (TP4) and negative output to Terminal PGND (TP5).
2. Connect a voltage meter (VM#3) to J6 between VLDO_SNS and GND pins. Connect a voltage meter (VM#4) to J6 between VDD_LDO_SNS and GND pins.
3. Select a proper load equipment Load#2 according to Section 3.2.2 and turn it off. Connect Load#2 terminal to VLDO terminal (TP8) and the other terminal to Terminal GND (TP9). Make sure the current always drawn from VLDO (TP8) and flow into GND (TP9).
4. Turn on PS#1. Check VM#3 is showing OTP programmed LDO output voltage.
5. Turn on Load#2. Adjust Load#2 current to measure VM#3, VM#4.

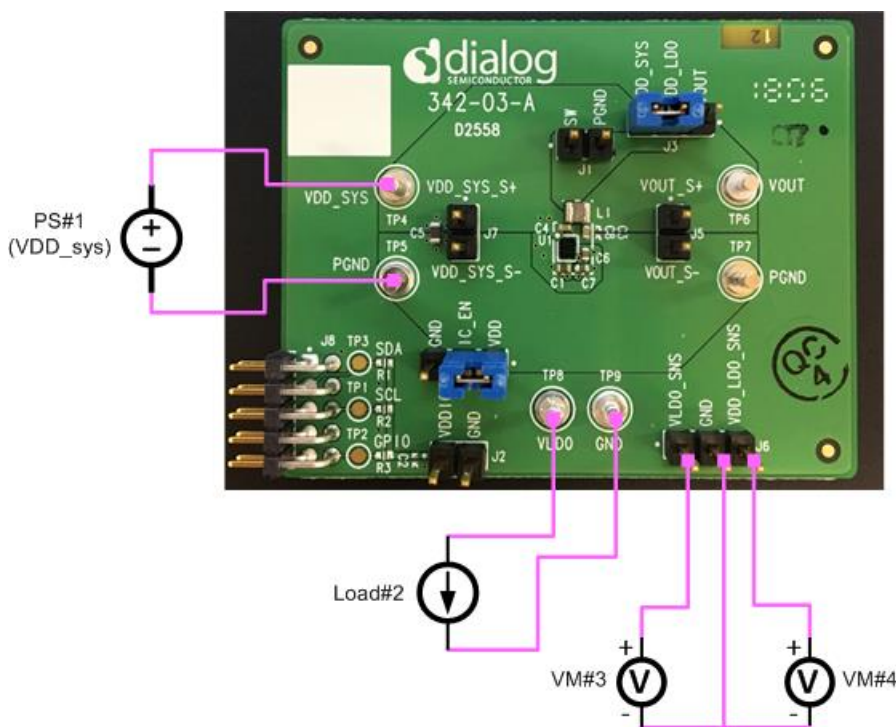


Figure 5: Recommended Setup for LDO Measurement

3.3.4 I²C and GPO Pull-Up Supply

342-03-A has the option to use on-board pull-up resistor and external VDDIO supply to drive SDA, SCL and GPO lines. If there are no pull-up resistors on the host side, simply populate R1 for SDA, R2 for SCL and R3 for GPO lines on 342-03-A board. Then apply an external voltage supply (\leq VDD_SYS) to J2 between VDDIO and GND.

Dialog USB module 162-09 provides pull-up resistors on SDA and SCL lines, but no pull-up on GPO line.

DA9231 DA9230 Evaluation Board - 342-03-A

3.4 Software GUI

To use software GUI for IC re-configuration and status monitoring, connect Dialog's USB module 162-09 to the 10-pin connector J8 with the header on the module facing up, as shown in Figure 6.



Figure 6: Dialog USB Module 162-09

3.4.1 I²C Address Re-configuration

By default, the GUI will automatically communicate to the device when its I²C address is 0x2F. However, if the device has an I²C address other than 0x2F, the GUI needs to be re-configured in order to build a communication with the device.

1. Open DA9230/DA9231 GUI and go to menu -> Options-> Settings. See Figure 7.

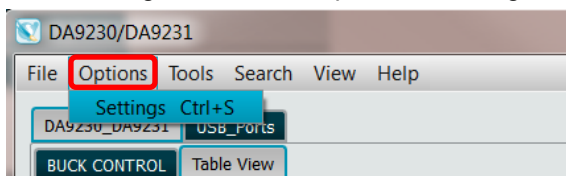


Figure 7: Open GUI Settings

2. In the Settings window, go to Bus Interface. See Figure 8. The default I²C address is “0x5E on bus 47 : Bus_0x2F”. Select the correct I²C address from the drop-down list based on device OTP versions. For example: Select “0x5A on bus 45 : Bus_0x2D” for DA9231_0DVZ2. Then make sure “Interface Enabled” is highlighted. The GUI I²C address is selectable from 00-7F.

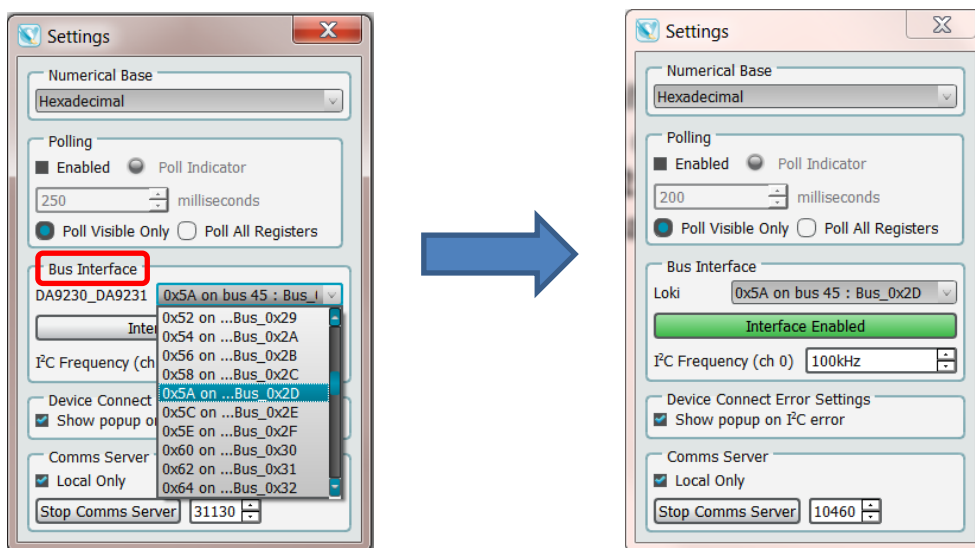


Figure 8: Example of Re-configure GUI I²C address

3.4.2 Device OTP Information

Device OTP information can be read from GUI as well.

1. Open DA9230/DA9231 GUI and go to SYSTEM MODULE page. See Figure 9.

DA9231 DA9230 Evaluation Board - 342-03-A

2. Read Register 0x82. It will show the OTP version of the device. For example: it shows 0x0B when the device on board is DA9231_0BVZ2.

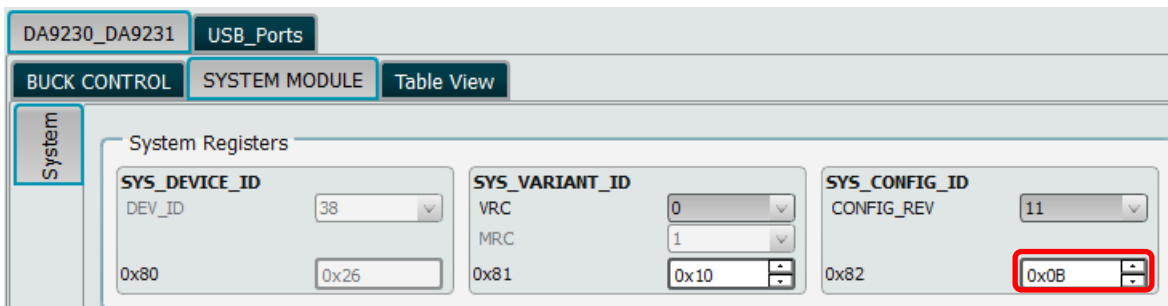


Figure 9: Read Device OTP information

3.4.3 Device Configuration and Status Monitor

1. Open DA9230/DA9231 GUI and go to BUCK CONTROL page, see Figure 10.
2. Uncheck all boxes in MASK section to enable all fault event indicators.
3. Configure the GPO pin function in GPO section.
4. Set the desired voltages using the droplist of BUCK_VOUT and LS_LDO.
5. Select buck peak current limit through SEL_BUCK_ILIM (default is 600 mA).
6. Choose to Enable/Disable buck output pull-down resistor through BUCK_PD_CFG1 and BUCK_PD_CFG2.
7. Configure the FAULT_CTL registers. Choose to disable or not disable buck/LDO during VIN_UV/OT/OV_BUCK/OC_BUCK/UV_BUCK event. Set the recovery number through RCVRY_NUM.
8. Click BUCK_EN and EN_LS_LDO buttons to turn ON/OFF buck and LDO/LS respectively.

DA9231 DA9230 Evaluation Board - 342-03-A

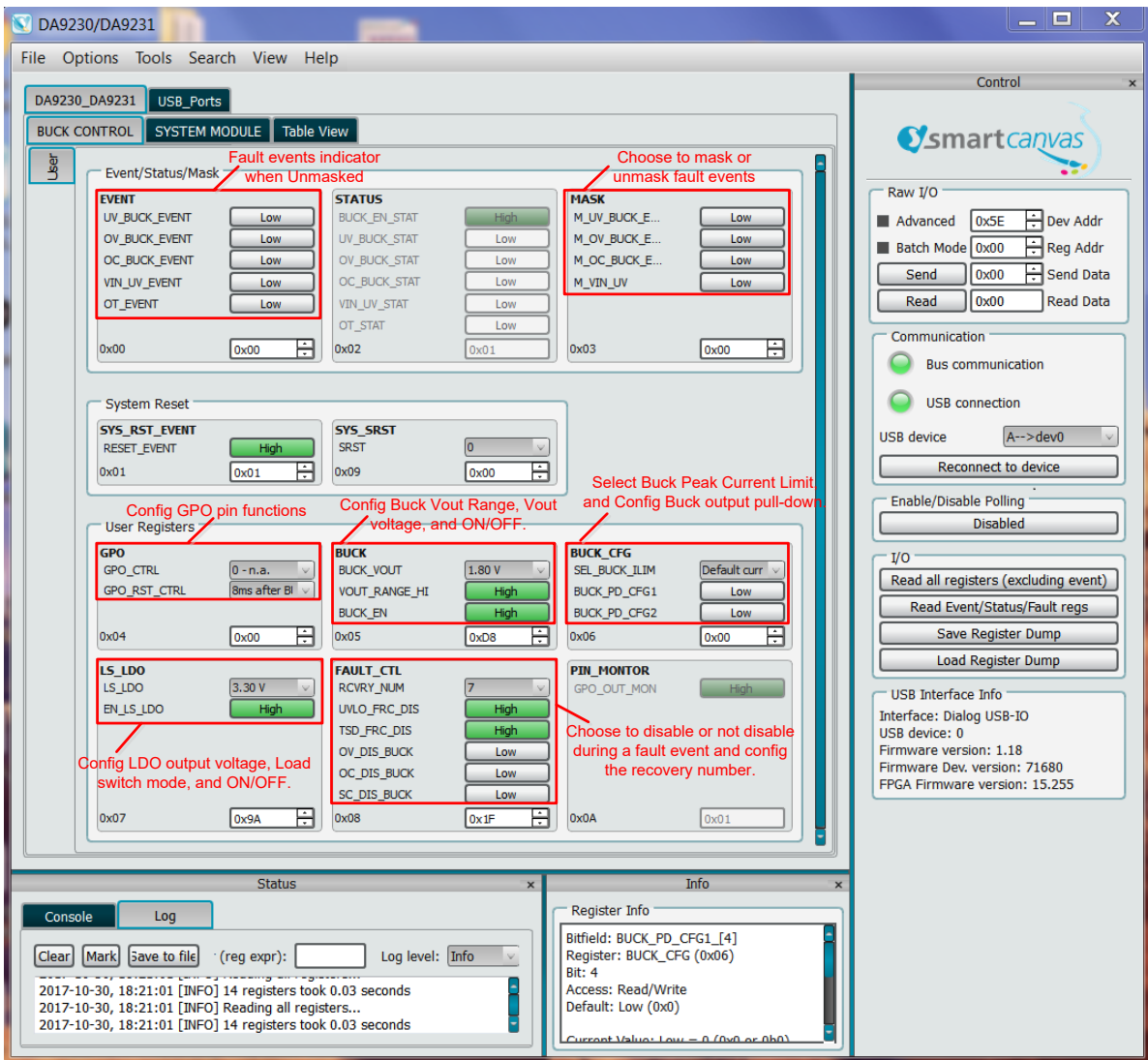


Figure 10: DA9231 GUI Control Page

DA9231 DA9230 Evaluation Board - 342-03-A

4 Schematic

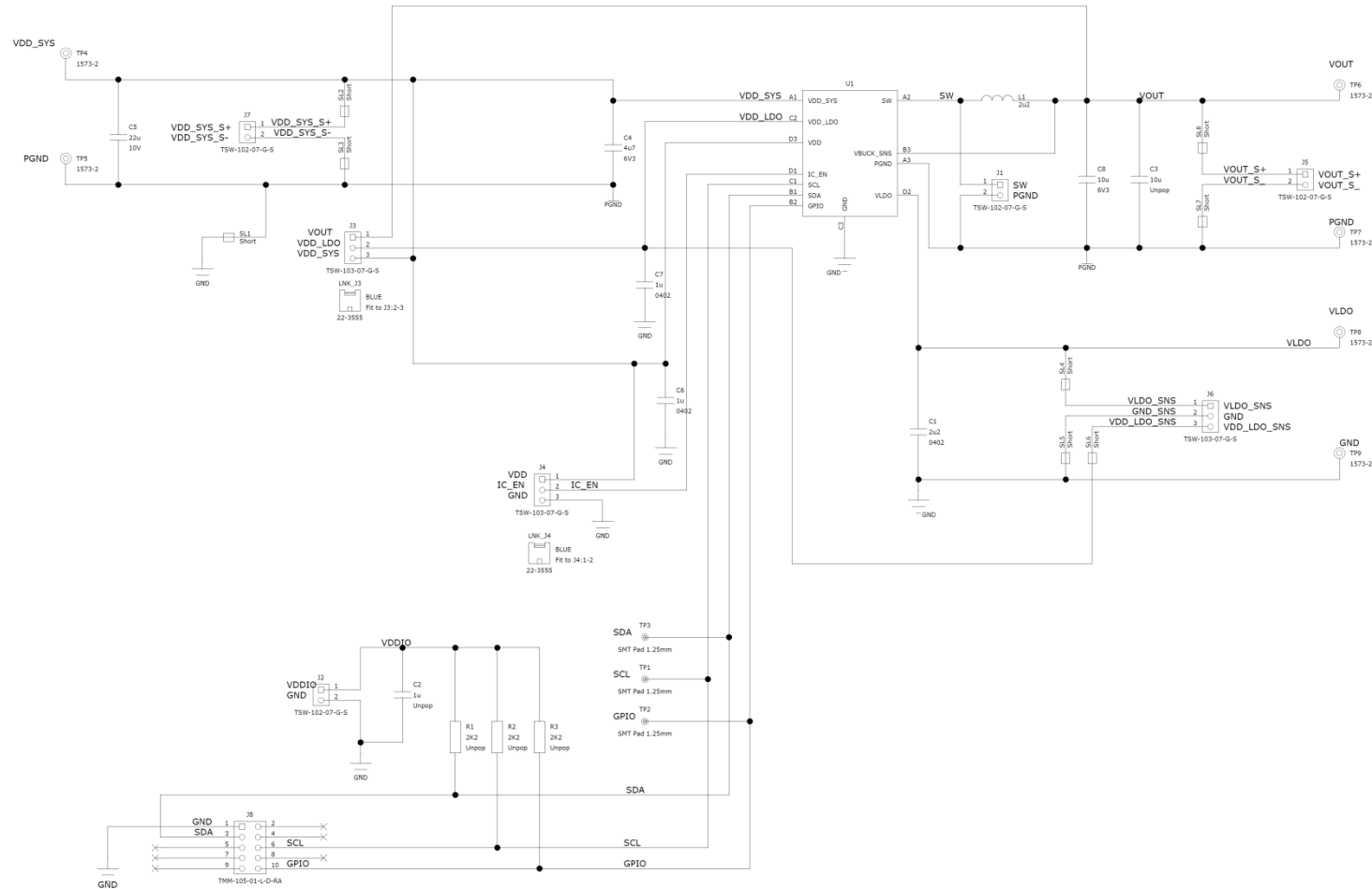


Figure 11: 342-03-A Evaluation Board Schematic

5 Board Layout and Bill of Materials

5.1 Board Layout

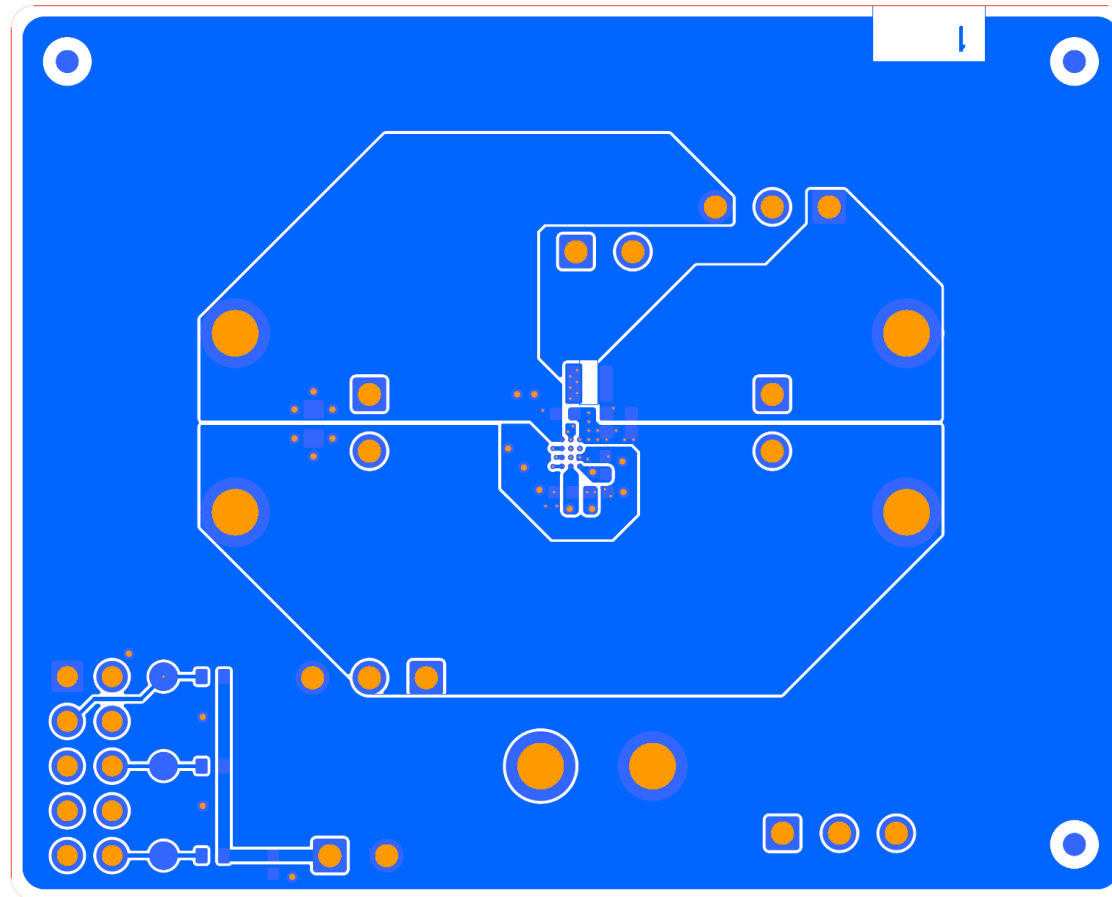


Figure 12: Top Layer

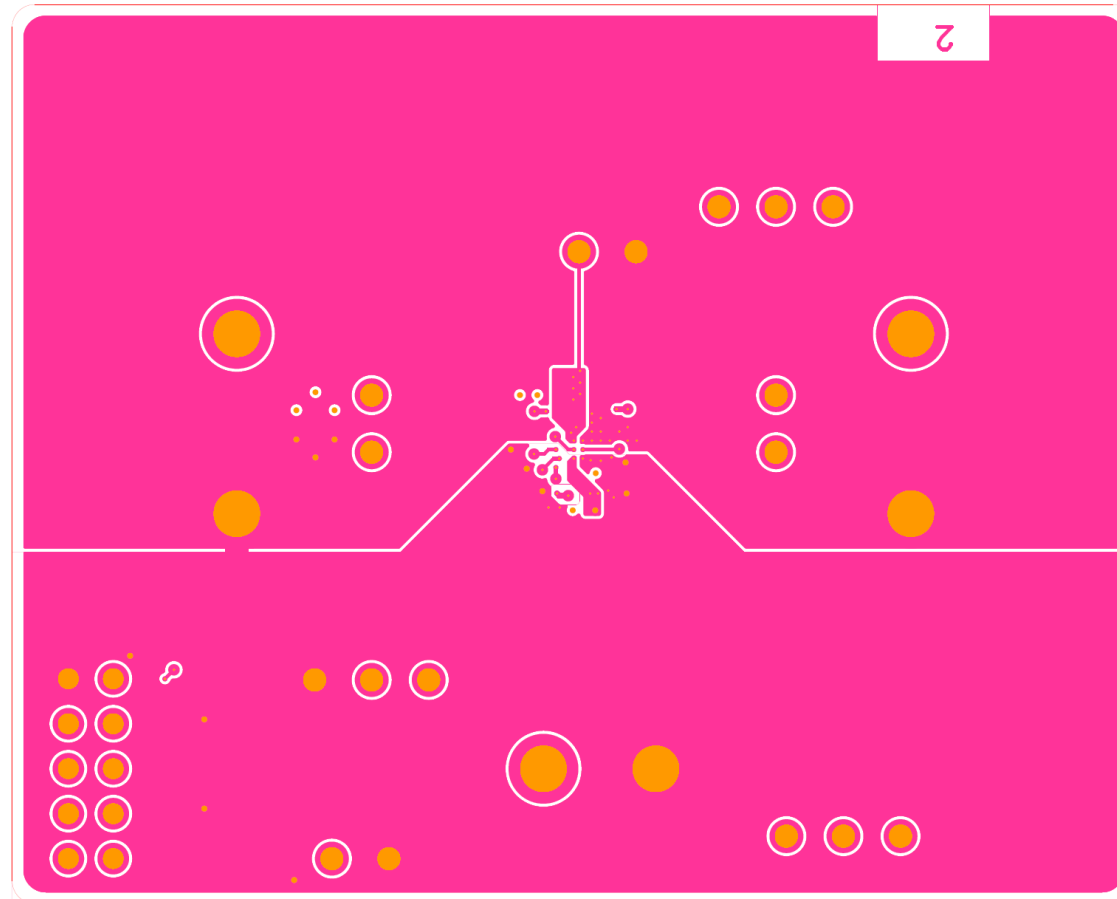


Figure 13: Inner Layer-2

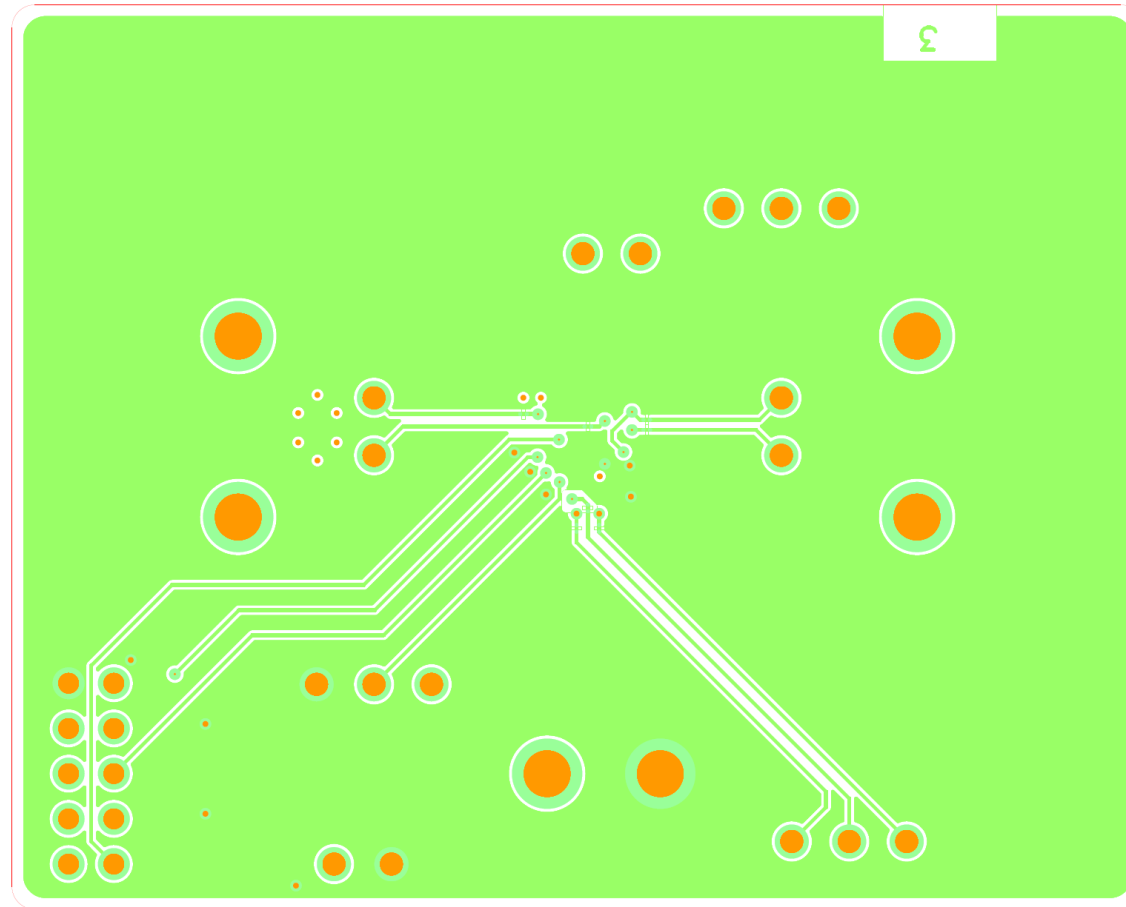


Figure 14: Inner Layer-3

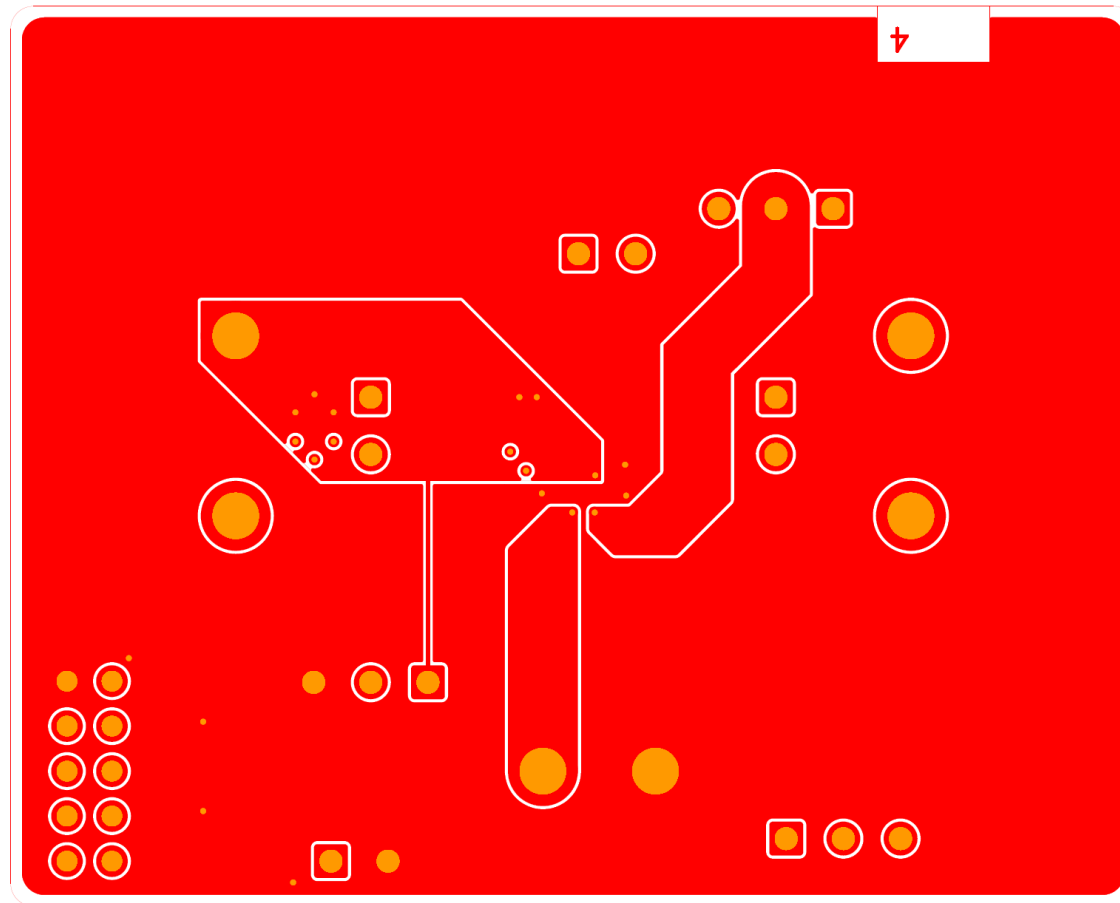


Figure 15: Bottom Layer

DA9231 DA9230 Evaluation Board - 342-03-A

5.2 Bill of Materials

Table 5: Bill of Materials of Evaluation Board 342-03-A

QTY	Ref Designator	Description	Value	Tol.	Rating	Dielectric	Pop /Unpop	Manufacturer	Manufacturer Part Number
1	U1	WLCSP12 IC					Populated	Dialog Semiconductor	DA9230, DA9231
2	LNK_J3, LNK_J4	Jumper Link 2.54mm Open Blue	22-3555				Populated	Rapid	22-3555
1	C4	1005 (0402 EIA) SMD Capacitor	4u7	±20%	6V3	X5R	Populated	Murata	GRM155R60J475ME47D
1	C5	1608 (0603 EIA) SMD Capacitor	22u	±20%	10V	X5R	Populated	Murata	GRM188R61A226ME15D
1	C1	1005 (0402 EIA) SMD Capacitor	2u2	±10%	16V	X5R	Populated	TDK	C1005X5R1C225K050BC
1	C8	1005 (0402 EIA) SMD Capacitor	10u	±20%	6V3	X5R	Populated	Murata	GRM155R60J106ME15
2	C6,C7	1005 (0402 EIA) SMD Capacitor	1u	±10%	25V	X5R	Populated	Murata	GRM155R61E105KA12D
1	L1	DFE201610 Series SMD Inductor	2u2	±20%	Isat=2.4A		Populated	Murata	DFE201610E-2R2M
4	J1,J2,J5, J7	1x2 2.54mm pitch PCB Pin Header VERTICAL (2.54mm tail)	TSW-102-07-G-S				Populated	Samtec	TSW-102-07-G-S
3	J3,J4,J6	1x3 2.54mm pitch PCB Pin Header VERTICAL (2.54mm tail)	TSW-103-07-G-S				Populated	Samtec	TSW-103-07-G-S
1	J8	2x5 2.00mm pitch PCB Header Right Angle (3.13mm tail)	TMM-105-01-L-D-RA				Populated	Samtec	TMM-105-01-L-D-RA

DA9231 DA9230 Evaluation Board - 342-03-A

QTY	Ref Designator	Description	Value	Tol.	Rating	Dielectric	Pop /Unpop	Manufacturer	Manufacturer Part Number
6	TP4-TP9	Double Turret Terminal, tail length 2.08mm	1573-2				Populated	Keystone Electronics	1573-2
1	C3	1005 (0402 EIA) SMD Capacitor	10u	±20%	6V3	X5R	Unpop	Murata	GRM155R60J106ME15
1	C2	1005 (0402 EIA) SMD Capacitor	1u	±10%	25V	X5R	Unpop	Murata	GRM155R61E105KA12D
3	R1-R3	1005 (0402 EIA) SMD Resistor	2K2	±1%	63mW		Unpop	Yageo	RC0402FR-072K2L

DA9231 DA9230 Evaluation Board - 342-03-A
Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

Important Notice and Disclaimer

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

© 2022 Renesas Electronics Corporation. All rights reserved.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

<https://www.renesas.com/contact/>

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.