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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

User's Manual

μPD78F8014A, 78F8015A, 78F8016A

8-Bit Single-Chip Microcontroller
With LIN Transceiver & Power Supply

μPD78F8014A(A)
μPD78F8015A(A)
μPD78F8016A(A)

Document No. U18867EJ4V0UD00 (4th edition)
Date Published May 2009 NS

Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E0904E

INTRODUCTION

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD78F8014A, 78F8015A, and 78F8016A, and to design and develop application systems and programs for these devices.

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The μPD78F8014A, 78F8015A, and 78F8016A's manuals are separated into three manuals: this manual, 78K0/Kx2 User's Manual, and the Instructions edition (common to the 78K0 Series).

μPD78F8014A, 78F8015A, 78F8016A User's Manual (This Manual)	**78K0/Kx2 User's Manual**	**78K/0 Series User's Manual Instructions**
• Pin functions • Internal block functions • On-chip peripheral functions • Electrical specifications (target)	• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

- The notation of the product name
  → Description of (A) is omitted in this manual. "(A)" product names should be read as follows
    • μPD78F8014A→ μPD78F8014A(A)
    • μPD78F8015A→ μPD78F8015A(A)
    • μPD78F8016A→ μPD78F8016A(A)

- To know details of the microcontroller part:
  → Refer to the separate document **78K0/Kx2 User's Manual (U18598E)**.

78K0/KC2 microcontroller products	The products corresponding to the 78K0/KC2 microcontroller products
μPD78F0511A	μPD78F8014A
μPD78F0512A	μPD78F8015A
μPD78F0513A	μPD78F8016A

- To know details of the 78K0 microcontroller instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD78F8014A, 78F8015A, 78F8016A User's Manual	This Manual
78K0/Kx2 User's Manual	U18598E
78K/0 Series Instructions User's Manual	U12326E
78K0/Kx2 Flash Memory Programming (Programmer) Application Note	U17739E
78K0 Microcontrollers Self Programming Library Type01 User's Manual	U18274E
78K0 Microcontrollers EEPROM™ Emulation Library Type01 User's Manual	U18275E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
QB-78K0KX2 In-Circuit Emulator	U17341E
QB-MINI2 On-Chip Debug Emulator with Programming Function	U18371E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	U18865E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0 Ver.3.80 Assembler Package User's Manual Note 1	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
78K0 Assembler Package RA78K0 Ver.4.01 Operating Precautions (Notification Document) Note 1		ZUD-CD-07-0181-E
CC78K0 Ver.3.70 C Compiler User's Manual Note 2	Operation	U17201E
	Language	U17200E
78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions (Notification Document) Note 2		ZUD-CD-07-0103-E
ID78K0-QB Ver.2.94 Integrated Debugger User's Manual	Operation	U18330E
ID78K0-QB Ver.3.00 Integrated Debugger User's Manual	Operation	U18492E
PM plus Ver.5.20 Note 3 User's Manual		U16934E
PM+ Ver.6.30 Note 4 User's Manual		U18416E

Notes 1. This document is installed into the PC together with the tool when installing RA78K0 Ver. 4.01. For descriptions not included in "78K0 Assembler Package RA78K0 Ver. 4.01 Operating Precautions", refer to the user's manual of RA78K0 Ver. 3.80.

2. This document is installed into the PC together with the tool when installing CC78K0 Ver. 4.00. For descriptions not included in "78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions", refer to the user's manual of CC78K0 Ver. 3.70.

3. PM plus Ver. 5.20 is the integrated development environment included with RA78K0 Ver. 3.80.

4. PM+ Ver. 6.30 is the integrated development environment included with RA78K0 Ver. 4.01. Software tool (assembler, C compiler, debugger, and simulator) products of different versions can be managed.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE – Product and Packages –	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
Review of Quality and Reliability Handbook Information	C12769E

Note See the "Semiconductor Device Mount Manual" website (http://www.necel.com/pkg/en/mount/index.html)

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

CONTENTS

CHAPTER 1 OUTLINE

μPD78F8014A, 78F8015A, and 78F8016A are MCP (Multi-Chip Package) which combined 2 chips in 1 package: an analog chip (including LIN transceiver, power supply, and several drivers) and a microcontroller chip.

8-bit microcontroller block is 78K0/KC2.

1.1 Features

○ ROM, RAM capacities

Item \ Part Number	Program Memory (ROM)		Data Memory Internal High-Speed RAM[Note]
μPD78F8014A	Flash memory[Note]	16 KB	768 bytes
μPD78F8015A		24 KB	1 KB
μPD78F8016A		31 KB	

Note The internal flash memory, internal high-speed RAM capacities, can be changed using the internal memory size switching register (IMS).

○ On-chip single-power-supply flash memory
○ Self-programming (with boot swap function)
○ On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
○ On-chip watchdog timer (operable with the on-chip internal low speed oscillation clock)
○ On-chip key interrupt function
○ I/O ports: 25 (N-ch open drain: 2)
○ Timer: 7 channels
- 16-bit timer/event counters: 1 channel
- 8-bit timer/event counters: 2 channels
- 8-bit timer: 2 channels
- Watch timer: 1 channel
- Watch dog timer: 1 channel

○ Serial interface: 3 channels
- UART (LIN (Local Interconnect Network)-bus supported): 1 channel
- CSI/UART[Note]: 1 channel
- IIC: 1 channel

○ 10-bit resolution A/D converter: 5 channels

Note Select either of the functions of these alternate-function pins.

- On-chip power supply circuit
  - Output voltage: 5 V ± 3%
  - On-chip overcurrent protection circuit
  - On-chip thermal shutdown circuit
- LIN transceiver
  - The LIN transceiver complies with LIN Specifications Rev.2.0
  - Low power consumption achieved with on-chip sleep function
  - On-chip pull-up resistors for slave applications
  - On-chip LIN driver overcurrent protection circuit
  - On-chip LIN driver thermal shutdown circuit
- Driver
  - Low side driver: 3 channels
  - Low side pre driver: 1 channel
  - High side driver: 1 channel
- Package: 52-pin plastic LQFP (10×10)
- Operation ambient temperature: T_A = −40 to +85 °C

1.2 Applications

○ Automotive equipment

System control for body electronic control units

- Power windows
- Power slide door
- Mirror control, etc.

1.3 Ordering Information

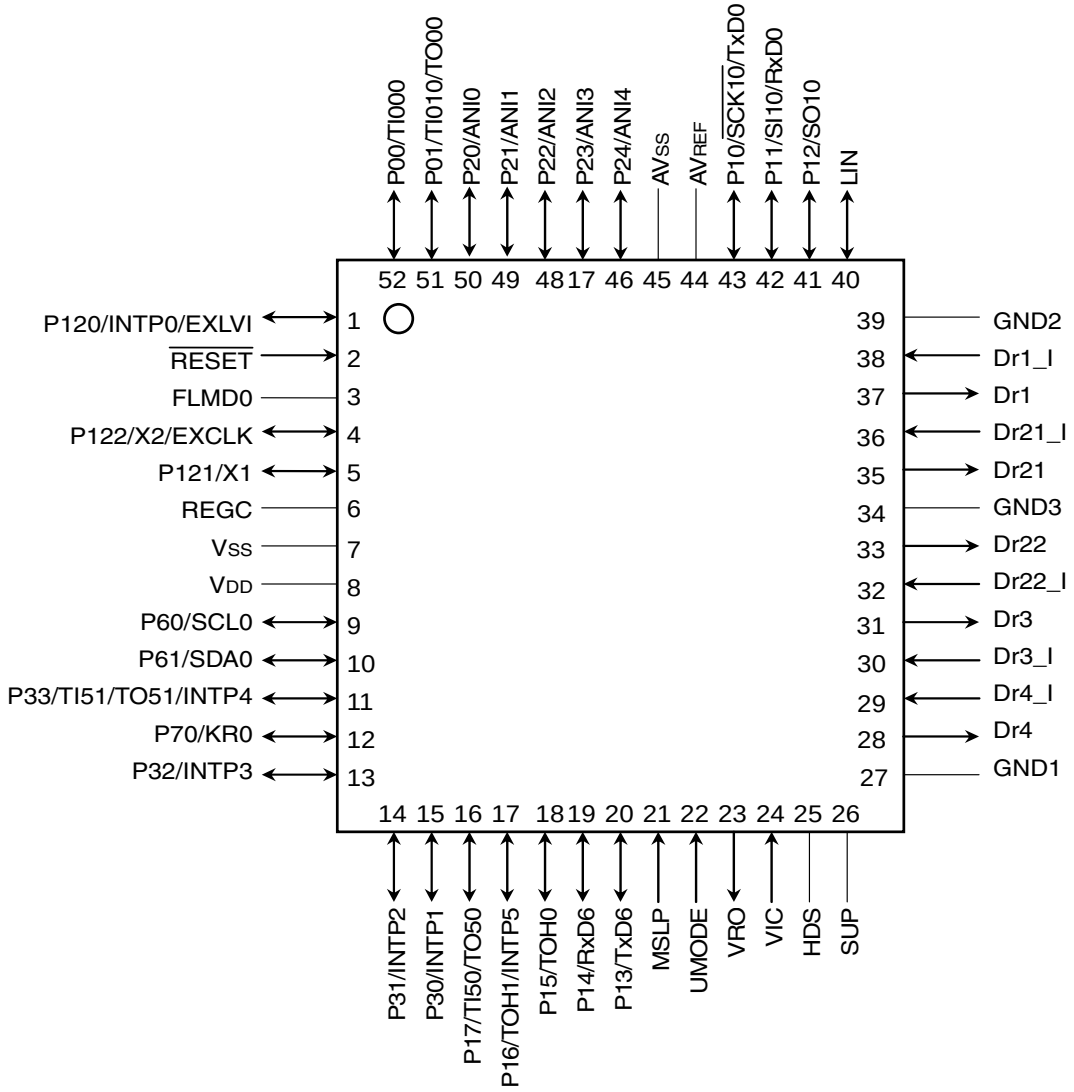
	Part Number	Package	Quality Grade
<R>	μPD78F8014AGBA-GAG-G Note	52-pin plastic LQFP (10×10)	Special
<R>	μPD78F8015AGBA-GAG-G Note	52-pin plastic LQFP (10×10)	Special
<R>	μPD78F8016AGBA-GAG-G Note	52-pin plastic LQFP (10×10)	Special

Note (A) grade product

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of quality grade on the devices and its recommended applications.

1.4 Pin Configuration (Top View)

- 52-pin plastic LQFP (10×10)



Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to VSS via a capacitor (0.47 μF to 1 μF: recommended).

3. ANI0/P20 to ANI4/P24 are in the analog input mode after reset release.

4. Make VSS the same potential as GND1 to GND3.

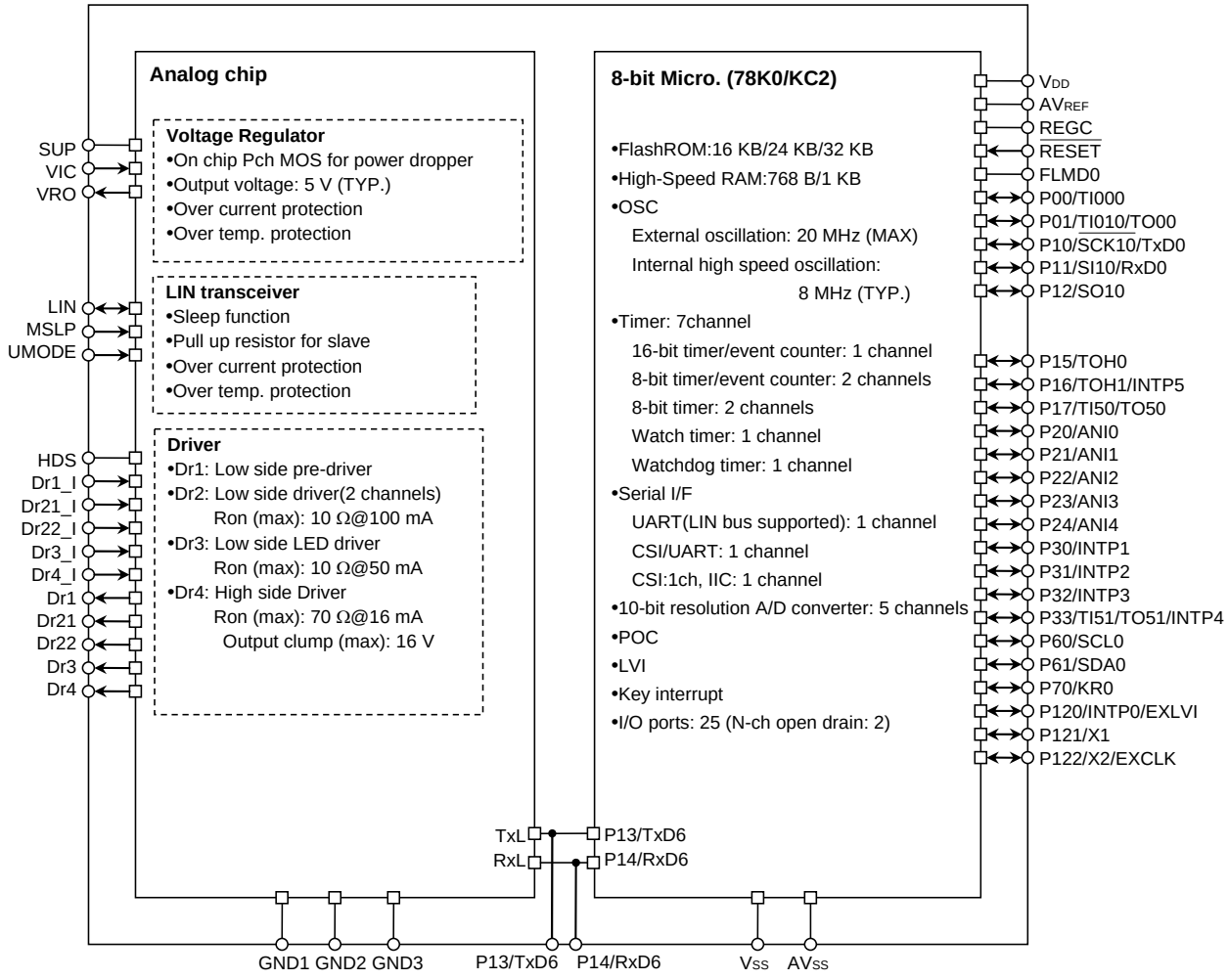
5. Make SUP the same potential as HDS.

6. Make VRO the same potential as VDD.

Pin Identification

ANI0 to ANI4	: Analog Input
AV_{REF}	: Analog Reference Voltage
AV_{SS}	: Analog Ground
Dr1, Dr21, Dr22, Dr3, Dr4	: Driver Output
Dr1_I, Dr21_I, Dr22_I, Dr3_I, Dr4_I	: Driver Control
EXCLK	: External Clock Input (Main System Clock)
EXLVI	: External potential Input for Low-voltage detector
FLMD0	: Flash Programming Mode
GND1 to GND3	: Ground
HDS	: High-side Driver Power Supply
INTP0 to INTP5	: External Interrupt Input
KR0	: Key Return
LIN	: LIN Bus
MSLP	: Sleep Mode
P00, P01	: Port 0
P10 to P17	: Port 1
P20 to P24	: Port 2
P30 to P33	: Port 3
P60, P61	: Port 6
P70	: Port 7
P120 to P122	: Port 12
REGC	: Regulator Capacitance
$\overline{\text{RESET}}$	: Reset
RxD0, RxD6	: Receive Data
$\overline{\text{SCK10}}$, SCL0	: Serial Clock Input/Output
SDA0	: Serial Data Input/Output
SI10	: Serial Data Input
SO10	: Serial Data Output
SUP	: Power Supply
TI000, TI010, TI50, TI51	: Timer Input
TO00, TO50, TO51, TOH0, TOH1	: Timer Output
TxD0, TxD6	: Transmit Data
UMODE	: LIN Mode
V_{DD}	: Power Supply
VIC	: Power Supply and Current Monitor
VRO	: Voltage Regulator Output
V_{SS}	: Ground
X1, X2	: Crystal Oscillator (Main System Clock)

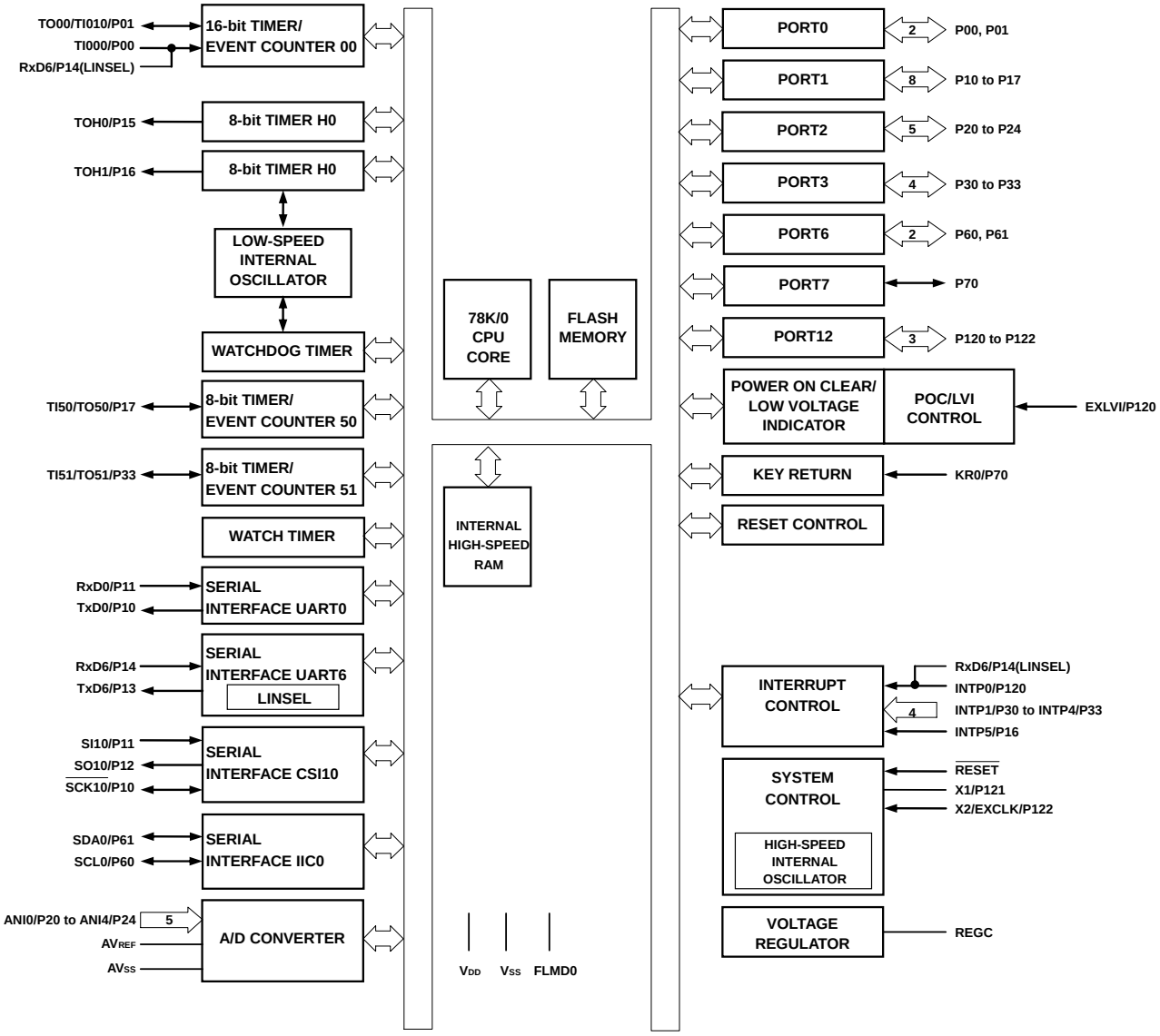
1.5 Block Diagram



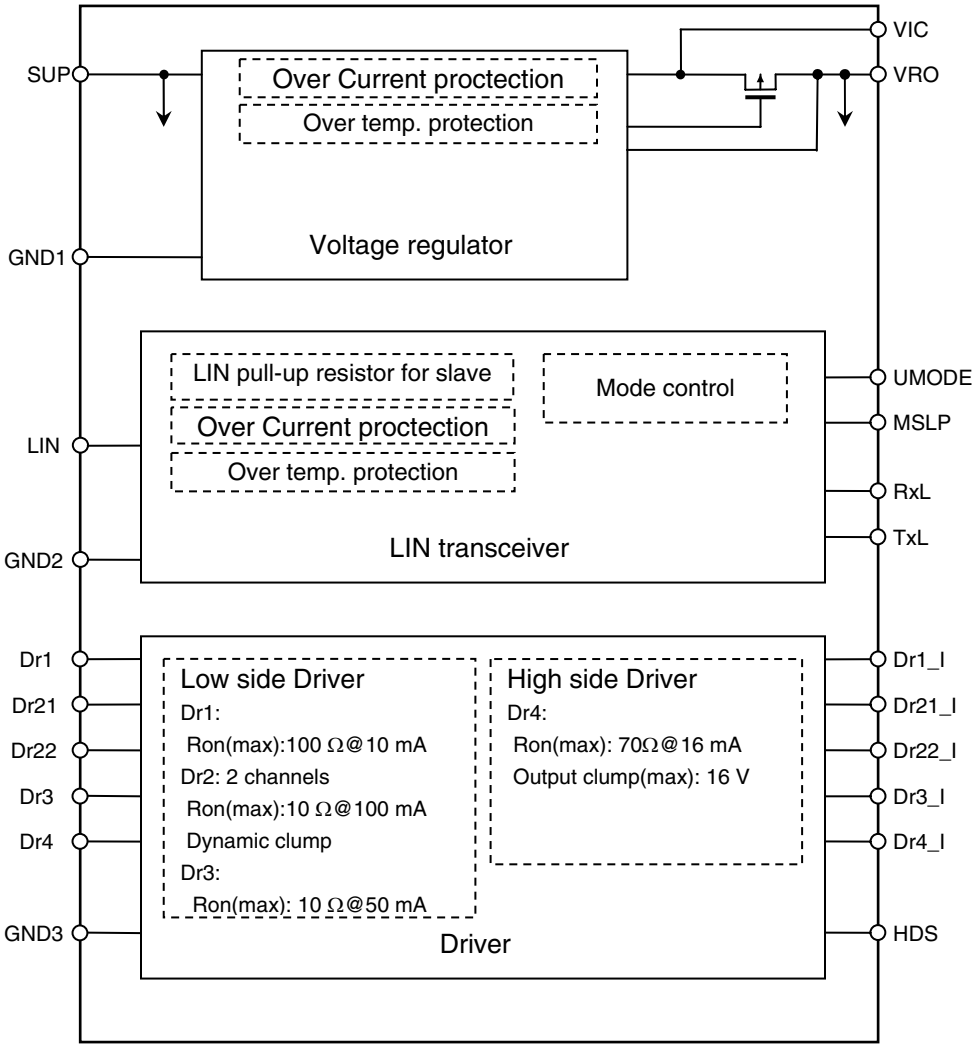
Cautions 1. μPD78F8014A, 78F8015A, and 78F8016A are developed as MCP (Multi-Chip Package) which includes 2 chips in the package, a microcontroller and an analog chip.

2. The P13/TxD6 and P14/RxD6 terminals are connected with the LIN transceiver inside the package.

1.5.1 Microcontroller block diagram



1.5.2 Analog block diagram



1.6 Outline of Functions

(1/2)

Item			μPD78F8014A	μPD78F8015A	μPD78F8016A
Flash memory (KB)			16	24	32
High-Speed RAM (KB)			0.75	1	
Power supply voltage			V_{DD} = 1.8 to 5.5 V		
Regulator			Provided		
Minimum instruction execution time			0.1 μs (20 MHz: V_{DD} = 2.7 to 5.5 V)/0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)		
Clock	Main	High-speed system	20 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V		
		Internal high-speed oscillation	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V		
	Internal low-speed oscillation		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V		
Port	Total		25		
	N-ch O.D. (6 V tolerance)		2		
Timer	16 bits (TM0)		1 ch		
	8 bits (TM5)		2 ch		
	8 bits (TMH)		2 ch		
	Watch		1 ch		
	WDT		1 ch		
Serial interface	UART/3-wire CSI[Note]		1 ch		
	UART supporting LIN-bus		1 ch		
	I^2C bus		1 ch		
10-bit A/D			5 ch		
Interrupt	External		7		
	Internal		16		
Key interrupt			1 ch		
Reset	$\overline{\text{RESET}}$ pin		Provided		
	POC		1.59 V ±0.15 V		
	LVI		The detection level of the supply voltage is selectable.		
	WDT		Provided		
Multiplier/divider			Provided		
On-chip debug function			–		
Operating ambient temperature			T_A = –40 to +85°C		

Note Select either of the functions of these alternate-function pins.

(2/2)

Item	μPD78F8014A	μPD78F8015A	μPD78F8016A
Power Supply	• Input voltage : V_{SUP} = 7 to 19 V • Output voltage: 5 V ± 3% • Include P-ch MOS for dropper • On-chip overcurrent protection circuit • On-chip thermal shutdown circuit		
LIN transceiver	• The LIN transceiver complies with LIN Specifications Rev.2.0 • Low power consumption achieved with on-chip sleep function • On-chip pull-up resistors for slave applications • On-chip LIN driver current protection circuit • On-chip LIN driver thermal shutdown circuit		
Driver	• Low side driver[4 channels] Pre-driver :1 channel Relay-driver :2 channels (Include dynamic clamp) LED driver :1 channel • High side driver :1 channel (Includes 16 V clamp circuit)		

An outline of the timer is shown below.

		16-Bit Timer/ Event Counters 00 and 01	8-Bit Timer/ Event Counters 50 and 51		8-Bit Timers H0 and H1		Watch Timer	Watchdog Timer
		TM00	TM50	TM51	TMH0	TMH1		
Function	Interval timer	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel **Note 1**	–
	External event counter	1 channel	1 channel	1 channel	–	–	–	–
	PPG output	1 output	–	–	–	–	–	–
	PWM output	–	1 output	1 output	1 output	1 output	–	–
	Pulse width measurement	2 inputs	–	–	–	–	–	–
	Square-wave output	1 output	1 output	1 output	1 output	1 output	–	–
	Carrier generator	–	–	–	–	1 output **Note 2**	–	–
	Watch Timer	–	–	–	–	–	1 channel **Note 1**	–
	Watchdog timer	–	–	–	–	–	–	1 channel
Interrupt source		2	1	1	1	1	1	–

Notes 1. The watch timer function and interval timer function of the watch timer can be used simultaneously.

2. TM51 and TMH1 can be used in combination as a carrier generator mode.

CHAPTER 2 PIN FUNCTIONS

The differences in microcontroller pin functions between the μPD78F8014A, 78F8015A, 78F8016A and the 78K0/KC2 are as follows.

(1) Port and alternate function pins

μPD78F8014A, 78F8015A, 78F8016A		**78K0/KC2** μPD78F0511A, 78F0512A, 78F0513A	
Pin name	Alternate function	Pin name	Alternate function
P00	TI000	P00	TI000
P01	TI010/TO00	P01	TI010/TO00
P10	$\overline{SCK10}$/TxD0	P10	$\overline{SCK10}$/TxD0
P11	SI10/RxD0	P11	SI10/RxD0
P12	SO10	P12	SO10
P13	TxD6	P13	TxD6
P14	RxD6	P14	RxD6
P15	TOH0	P15	TOH0
P16	TOH1/INTP5	P16	TOH1/INTP5
P17	TI50/TO50	P17	TI50/TO50
P20 to P24	ANI0 to ANI4	P20 to P27	ANI0 to ANI7
P30	INTP1	P30	INTP1
P31	INTP2	P31	INTP2

μPD78F8014A, 78F8015A, 78F8016A		**78K0/KC2** μPD78F0511A, 78F0512A, 78F0513A	
Pin name	Alternate function	Pin name	Alternate function
P32	INTP3	P32	INTP3
P33	INTP4/TI51/TO51	P33	INTP4/TI51/TO51
–	–	P40 to P41	–
P60	SCL0	P60	SCL0
P61	SDA0	P61	SDA0
–	–	P62	EXSCL0
–	–	P63	–
P70	KR0	P70 to P73	KR0 to KR3
P120	INTP0/EXLVI	P120	INTP0/EXLVI
P121	X1	P121	X1
P122	X2/EXCLK	P122	X2/EXCLK
–	–	P123	XT1
–	–	P124	XT2/EXCLKS

(2) Non-port pins

μPD78F8014A, 78F8015A, 78F8016A	**78K0/KC2** μPD78F0511A, 78F0512A, 78F0513A
Pin name	Pin name
V_{DD}	V_{DD}
V_{SS}	V_{SS}
$\overline{RESET}$	$\overline{RESET}$

μPD78F8014A, 78F8015A, 78F8016A	**78K0/KC2** μPD78F0511A, 78F0512A, 78F0513A
Pin name	Pin name
FLMD0	FLMD0
AV_{REF}	AV_{REF}
AV_{SS}	AV_{SS}
REGC	REGC

2.1 Microcontroller Part Pin Functions

There are two types of pin I/O buffer power supplies: AV_{REF}, and V_{DD}. The relationship between these power supplies and the pins are shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}	P20 to P24
V_{DD}	Pins other than P20 to P24

(1) Port pins

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK10}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20 to P24	I/O	Port 2. 5-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0 to ANI4
P30 to P32	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1 to INTP3
P33				INTP4/TI51/TO51
P60	I/O	Port 6. 2-bit I/O port. Output of P60 to P61 is N-ch open-drain output Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P70	I/O	Port 7. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0
P120	I/O	Port 12. 3-bit I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121				X1
P122				X2/EXCLK

(2) Non-port functions

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI4	Input	A/D converter analog input	Analog input	P20 to P24
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
FLMD0	–	Flash memory programming mode setting	–	–
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1 to INTP3				P30 to P32
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
KR0	Input	Key interrupt input	Input port	P70
REGC	–	Connecting regulator output stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 μF to 1 μF: recommended).	–	–
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to asynchronous serial interface (UART0)	Input port	P11/SI10
RxD6	Input	Serial data input to asynchronous serial interface (UART6)	Input port	P14
$\overline{\text{SCK10}}$	I/O	Clock input/output for CSI10	Input port	P10/TxD0
SCL0	I/O	Clock input/output for IIC	Input port	P60
SDA0	I/O	Serial data input/output for IIC	Input port	P61
SO10	Output	Serial data output for CSI10	Input port	P12
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P01/TO00
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TI010
TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50
TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
TOH0		8-bit timer H0 output		P15
TOH1		8-bit timer H1 output		P16/INTP5
TxD0	Output	Serial data output for UART0	Input port	P10/$\overline{\text{SCK10}}$
TxD6	Output	Serial data output for UART6	Input port	P13
X1	Input	Connecting resonator for main system clock	Input port	P121
X2	–			P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
V_{DD}	–	Positive power supply (except for ports)	–	–
AV_{REF}	Input	A/D converter reference voltage input and positive power supply for P20 to P24 and A/D converter	–	–
V_{SS}	–	Ground potential (P121 to P124 and except for ports)	–	–
AV_{SS}	–	A/D converter ground potential. Make the same potential as EV_{SS} or V_{SS}.	–	–

2.2 Analog Part Pins

Function Name	I/O	Function
Dr1	Output	Driver 1 output
Dr21	Output	Driver 21 output
Dr22	Output	Driver 22 output
Dr3	Output	Driver 3 output
Dr4	Output	Driver 4 output
Dr1_I	Input	Driver 1 control signal input
Dr21_I	Input	Driver 21 control signal input
Dr22_I	Input	Driver 22 control signal input
Dr3_I	Input	Driver 3 control signal input
Dr4_I	Input	Driver 4 control signal input
GND1	–	Power supply circuit GND
GND2	–	LIN transceiver circuit GND
GND3	–	Driver circuit GND
HDS	–	High side driver power supply
LIN	I/O	LIN Bus connection pin
MSLP	Input	Sleep / Normal mode select for LIN
SUP	–	Power supply connection pin
UMODE	Input	LIN transceiver function enable / disable selection pin Low: Enable LIN transceiver High: Disable LIN transceiver
VIC	Input	Power supply and current monitor
VRO	Output	Voltage regulator output and monitor

Cautions 1. Make GND1, GND2, GND3 the same potential as V_{SS} and AV_{SS}

2. Make SUP the same potential as HDS.

3. Make VRO the same potential as V_{DD}.

2.3 Description of Pin Functions

2.3.1 P00, P01 (port 0)

2-bit I/O port. These pins also function as timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

2-bit I/O port. P00, P01can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00, P01 function as timer I/O.

(a) TI000

This is the pins for inputting an external count clock to 16-bit timer/event counter 00 and is also for inputting a capture trigger signal to the capture registers (CR000, CR010) of 16-bit timer/event counter 00.

(b) TI010

This is the pin for inputting a capture trigger signal to the capture register (CR000) of 16-bit timer/event counter 00.

(c) TO00

This is a timer output pin of 16-bit timer/event counters 00.

2.3.2 P10 to P17 (port 1)

P10 to P17 function as an 8-bit I/O port. These pins also function as pins for external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an 8-bit I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

(a) SI10

This is a serial data input pin of serial interface CSI10.

(b) SO10

This is a serial data output pin of serial interface CSI10.

(c) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(d) RxD0

This is a serial data input pin of serial interface UART0.

(e) RxD6

This is a serial data input pin of serial interface UART6.

(f) TxD0

This is a serial data output pin of serial interface UART0.

(g) TxD6

This is a serial data output pin of serial interface UART6.

(h) TI50

This is the pin for inputting an external count clock to 8-bit timer/event counter 50.

(i) TO50

This is a timer output pin of 8-bit timer/event counter 50.

(j) TOH0, TOH1

These are the timer output pins of 8-bit timers H0 and H1.

(k) INTP5

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.3.3 P20 to P24 (port 2)

P20 to P24 function as a 5-bit I/O port. These pins also function as pins for A/D converter analog input.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P24 function as a 5-bit I/O port. P20 to P24 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P24 function as A/D converter analog input pins (ANI0 to ANI4). When using these pins as analog input pins, see **13.6 Cautions for A/D Converter in 78K0/Kx2 User's Manual (U18598E)**.

Caution ANI0/P20 to ANI4/P24 are set to analog input mode after reset release.

2.3.4 P30 to P33 (port 3)

P30 to P33 function as a 4-bit I/O port. These pins also function as pins for external interrupt request input and timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as a 4-bit I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as external interrupt request input and timer I/O.

(a) INTP1 to INTP4

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI51

This is an external count clock input pin to 8-bit timer/event counter 51.

(c) TO51

This is a timer output pin from 8-bit timer/event counter 51.

2.3.5 P60 to P61 (port 6)

P60 to P61 function as a 2-bit I/O port. These pins also function as pins for serial interface data I/O, clock I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P60 to P61 function as a 2-bit I/O port. P60 to P61 can be set to input port or output port in 1-bit units using port mode register 6 (PM6).

Output of P60 to P61 is N-ch open-drain output (6V tolerance).

(2) Control mode

P60 to P61 function as serial interface data I/O, clock I/O.

(a) SDA0

This is a serial data I/O pin for serial interface IIC0.

(b) SCL0

This is a serial clock I/O pin for serial interface IIC0.

2.3.6 P70 (port 7)

P70 function as a 1-bit I/O port. These pins also function as key interrupt input pins.

The following operation modes can be specified.

(1) Port mode

P70 function as a 1-bit I/O port. P70 can be set to input or output port using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

(2) Control mode

P70 function as key interrupt input pins.

(a) KR0

This is a key interrupt input pins

2.3.7 P120 to P122 (port 12)

P120 to P122 function as a 3-bit I/O port. These pins also function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock. The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 to P122 function as a 3-bit I/O port. P120 to P122 can be set to input or output port using port mode register 12 (PM12). Only for P120, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

(2) Control mode

P120 to P122 function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock.

(a) INTP0

This functions as an external interrupt request input (INTP0) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

2.3.8 AV_{REF}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P24 and A/D converter.

When the A/D converter is not used, connect this pin directly to V_{DD}[Note].

Note Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

2.3.9 AV_{SS}

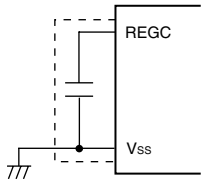
This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the VSS pin.

2.3.10 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

2.3.11 REGC

This is the pin for connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF: recommended).



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

2.3.12 V_{DD}

V_{DD} is the positive power supply pin for Micro.

2.3.13 V_{SS}

V_{SS} is the ground potential pin.

2.3.14 FLMD0

This is a pin for setting flash memory programming mode.

Connect FLMD0 to V_{SS} in the normal operation mode.

In flash memory programming mode, connect this pin to the flash programmer.

2.3.15 Dr1, Dr21, Dr22, Dr3, Dr4

These are high voltage driver output pin.

Each driver output can control with the Dr1_I, Dr21_I, Dr22_I, Dr3_I, Dr4_I input signal.

(a) Dr1

This is a Low side driver output pin.

(b) Dr21, Dr22

This is a Low side driver output pin.

These pin has dynamic clump function for high voltage protection.

(c) Dr3

This is a Low side driver output pin.

(d) Dr4

This is a High side driver output pin.

This pin has output voltage clump function, overcurrent protection and thermal shutdown function.

2.3.16 Dr1_I, Dr21_I, Dr22_I, Dr3_I, Dr4_I

These are input pins for high voltage driver control.

These pin have a pull-down resistor inside the IC.

Table 2-2. Truth table

Input		Dr1	Dr21	Dr22	Dr3	Dr4
Dr1_I	High	ON	–	–	–	–
	Low	OFF	–	–	–	–
Dr21_I	High	–	ON	–	–	–
	Low	–	OFF	–	–	–
Dr22_I	High	–	–	ON	–	–
	Low	–	–	OFF	–	–
Dr3_I	High	–	–	–	ON	–
	Low	–	–	–	OFF	–
Dr4_I	High	–	–	–	–	ON
	Low	–	–	–	–	OFF

2.3.17 GND1, GND2, GND3

GND1 is a power supply circuit GND.

GND2 is an LIN transceiver circuit GND.

GND3 is a driver circuit GND.

Connect GND1, GND2, and GND3 to the same potential as V_{SS} and AV_{SS}.

2.3.18 HDS

This is a power supply pin for high side driver.

Connect HDS to the same potential as SUP.

2.3.19 LIN

This is a LIN Bus connection pin.

2.3.20 MSLP

This pin is used to switch the LIN transceiver between normal and sleep mode. In the normal mode the LIN transceiver goes into sleep mode when MSLP is set to low and in the sleep mode the LIN transceiver goes into normal mode when MSLP is set to high.

Moreover, this pin has a pull-down resistor inside the IC.

2.3.21 SUP

SUP is the positive power supply pin.

2.3.22 UMODE

This pin is used as mode pin to enable/disable the LIN transceiver function. This pin is pulled-down inside the IC.

UMODE	LIN Transceiver Circuit Status	P13/TxD6 Pin Status	P14/RxD6 Pin Status
Low	Active	Output[Note] (TxL: Pull up input)	Input[Note] (RxL: Output)
High	Non active (Driver OFF)	Input /Output (TxL: Hi-Z)	Input /Output (RxL: Hi-Z)

Note When the LIN transceiver function is enabled, leave the P13/TxD6 and P14/RxD6 pins open. Clear PM13 to 0 (P13/TxD6 output setting) and set PM14 to 1 (P14/RxD6 input setting).

2.3.23 VIC

VIC is the supply voltage and current monitor pin for voltage regulator.

2.3.24 VRO

VRO is voltage regulator output and monitor.

2.4 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuit and the recommended connections of unused pins.
Refer to Figure 2-1 for the configuration of the I/O circuits of each type.

Table 2-3. Pin I/O Circuit Types (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000	5-AH	I/O	Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P01/TI010/TO00			
P10/$\overline{SCK10}$/TxD0			
P11/SI10/RxD0			
P12/SO10	5-AG		
P13/TxD6[Note 1]			
P14/RxD6[Note 1]	5-AH		
P15/TOH0	5-AG		
P16/TOH1/INTP5	5-AH		
P17/TI50/TO50/FLMD1			
P20/ANI0 to P24/ANI4[Note 2]	11-G		<Analog setting> Connect to AV_{REF} or AV_{SS}. <Digital setting> Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P30/INTP1 to P32/INTP3	5-AH		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P33/TI51/TO51/INTP4			
P60/SCL0	13-AD		Input: Connect to V_{SS}. Output: Leave this pin open at low-level output after clearing the output latch of the port to 0.
P61/SDA0			
P70/KR0	5-AH		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P120/INTP0/EXLVI			
P121/X1[Note 3]	37		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P122/X2/EXCLK[Note 3]			
$\overline{RESET}$	2	Input	–
FLMD0	38	–	Connect to V_{SS}.
AV_{REF}	–	–	Connect directly to V_{DD}[Note 4].
AV_{SS}	–	–	Connect directly to V_{SS}.

Notes 1. This pin has alternate functions as UART pin of the microcontroller or as LIN transceiver function pin. When this pin is used as the LIN transceiver function pin, leave it open. When it is used as microcontroller function pin, the UMODE pin must be externally pulled to V_{DD} with a resistor.

2. P20/ANI0 to P24/ANI4 are in the analog input mode after reset release.

3. Use the recommended connection method described above in I/O port mode when these pins are not used.

4. Use the same potential as the V_{DD} pin when port 2 is used as a digital port.

Table 2-3. Pin I/O Circuit Types (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
Dr1	LIN1	Output	Leave open
Dr21	LIN2		
Dr22			
Dr3	LIN1		
Dr4	LIN3		
Dr1_I	LIN4	Input	Leave open
Dr21_I	LIN5		
Dr22_I			
Dr3_I	LIN4		
Dr4_I			
LIN	LIN6	I/O	Leave open
MSLP	LIN4	Input	Leave open
UMODE	LIN4	Input	Leave open.
VIC	LIN7	Input	Connect directly to SUP
VRO		Output	Connect directly to V_{DD}
RxL	LIN8	Output	Note 1
TxL	LIN9	Input	Note 2

Notes 1. RxL terminal is connected with P14/RxD6 in package.

2. TxL terminal is connected with P13/TxD6 in package.

Figure 2-1. Pin I/O Circuit List (1/4)

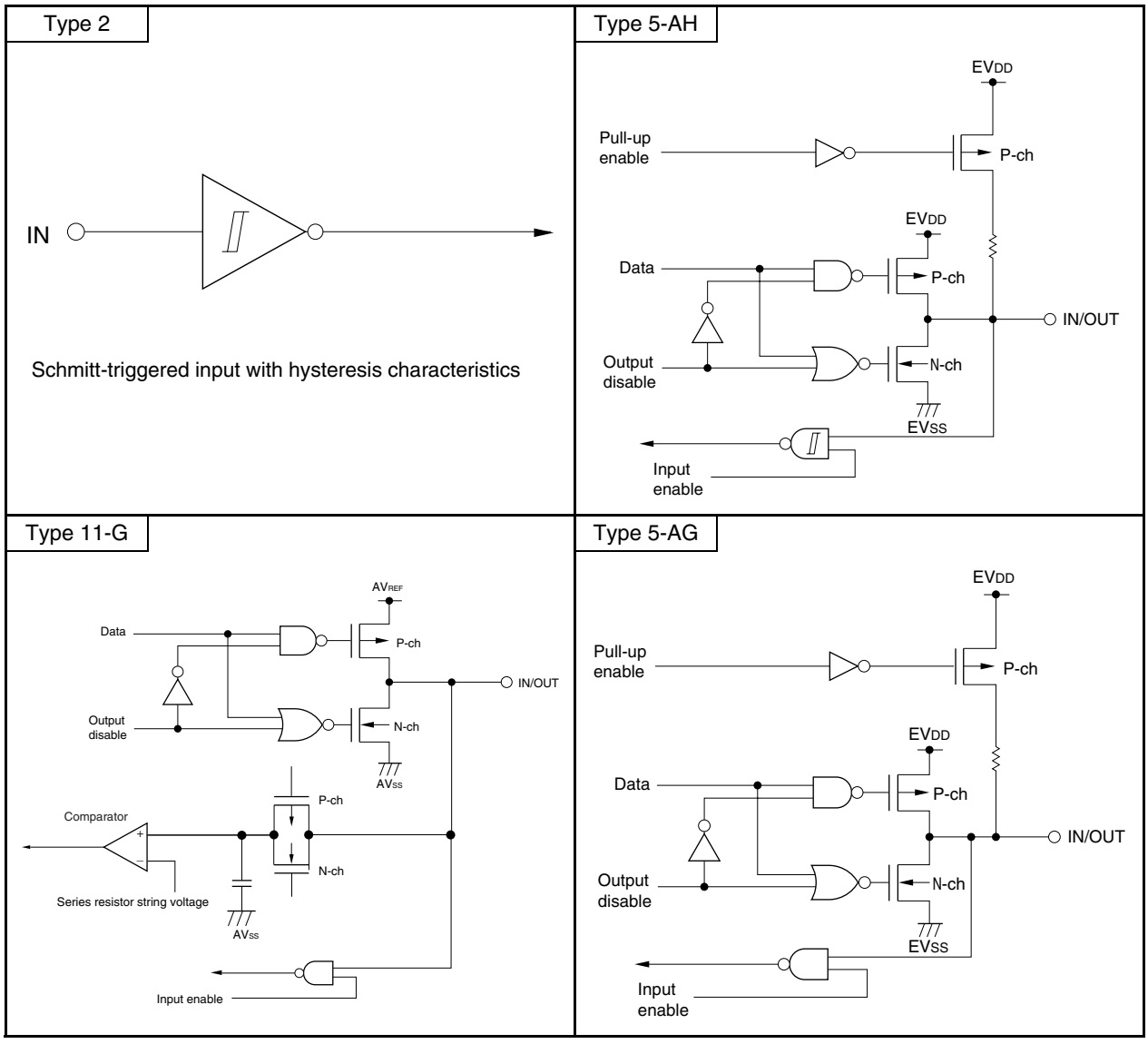
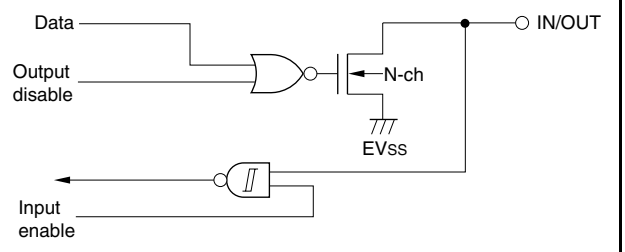
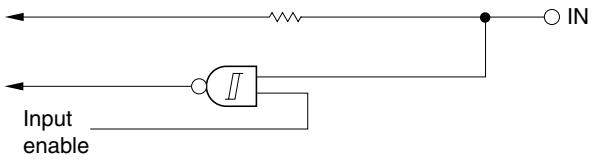


Figure 2-1. Pin I/O Circuit List (2/4)

Type 13-AD



Type 38



Type 37

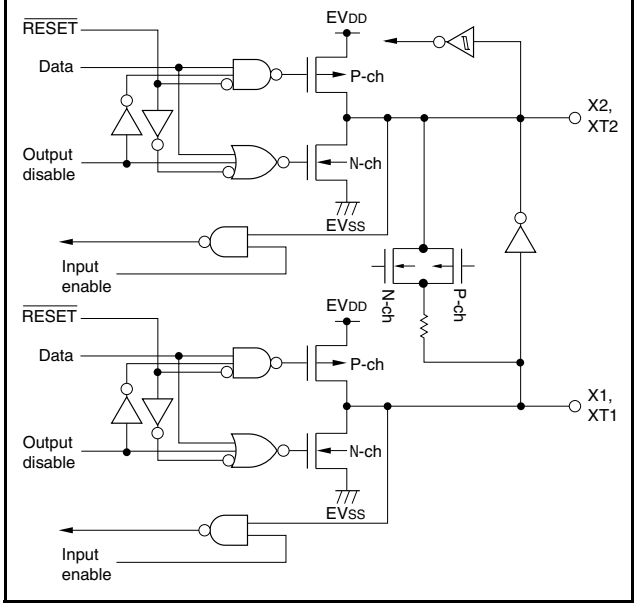


Figure 2-1. Pin I/O Circuit List (3/4)

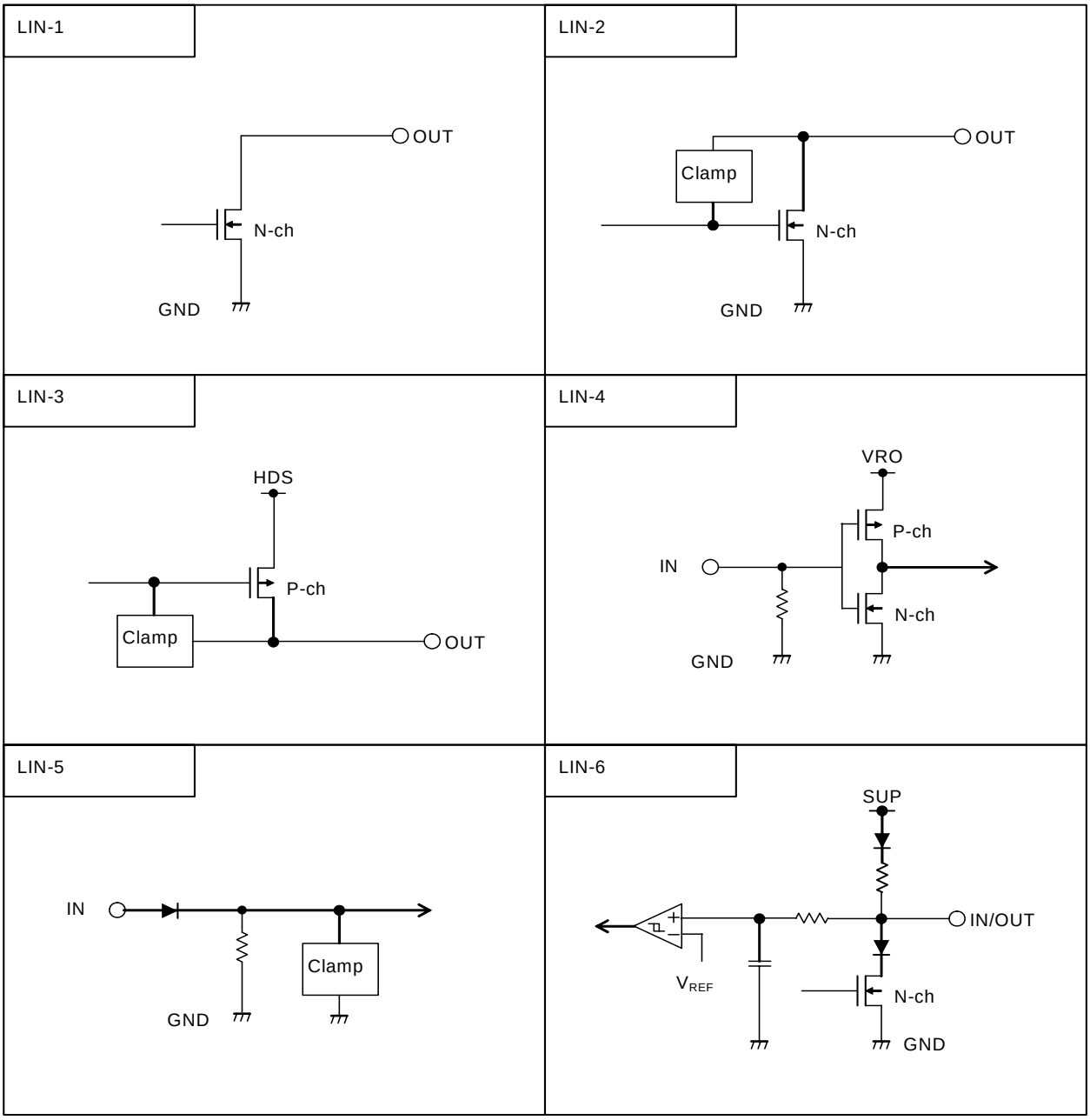
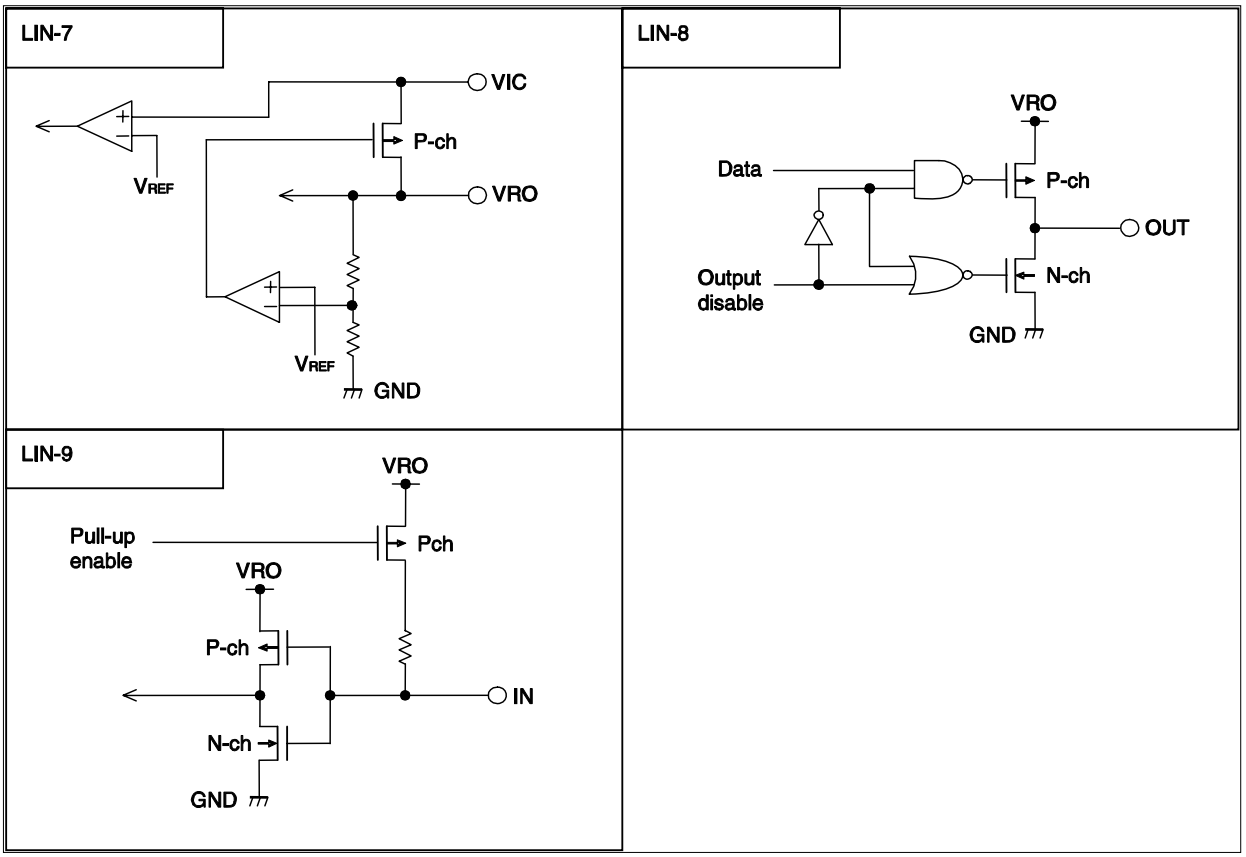


Figure 2-1. Pin I/O Circuit List (4/4)



CHAPTER 3 MICROCONTROLLER FUNCTIONS

The 8-bit microcontroller is the same as 78K0/KC2. The supported functions of the μPD78F8014A, 78F8015A and 78F8016A are different from 78K0/KC2, because the μPD78F8014A, 78F8015A, and 78F8016A do not support 78K0/KC2 all function pins.

This manual describes the differences between this micro's functions and 78K0/KC2.

See each function of microcontroller parts in **78K0/Kx2 User's Manual (U18598E).**

3.1 Differences between This Micro's Functions and 78K0/KC2

The differences between the μPD78F8014A, 78F8015A and 78F8016A's functions and 78K0/KC2 are as follows.

Item	**μPD78F8014A, 78F8015A, 78F8016A**	**78K0/KC2 (44-pin)** μPD78F0511A, 78F0512A, 78F0513A
Subsystem clock	–	XT1 (crystal) oscillation External subsystem clock input (EXCLK) 32.768 kHz (TYP.) : V_{DD} = 1.8 to 5.5 V
I/O port	Total: 25 CMOS I/O: 23 N-ch open-drain I/O(tolerance): 2	Total: 37 CMOS I/O: 33 N-ch open-drain I/O(tolerance): 4
Clock out	–	• 156.25 kHz, 312.5 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: f_{PRS} = 20 MHz operation) • 32.768 kHz (subsystem clock: f_{SUB} = 32.768 kHz operation)
A/D converter	10 bit resolution x 5 channels (AV_{REF} = 2.3 to 5.5 V)	10 bit resolution x 8 channels (AV_{REF} = 2.3 to 5.5 V)
Key interrupt	Key interrupt (INTKR) occurs by detecting falling edge of key input pins (KR0).	Key interrupt (INTKR) occurs by detecting falling edge of key input pins (KR0 to KR3).

3.2 Differences between the Special Function Registers and 78K0/KC2

The differences between the μPD78F8014A, 78F8015A and 78F8016A's special function registers and 78K0/KC2 (44pin) are as follows.

Address	μPD78F8014A, 78F8015A, 78F8016A		78K0/KC2 μPD78F0511A 78F0512A, 78F0513A	
	Special function register (SFR) name	Symbol	Special function register (SFR) name	Symbol
FF02H	Port register 2 Note 1	P2	Port register 2	P2
FF04H	– Note 2	–	Port register 4	P4
FF06H	Port register 6 Note 1	P6	Port register 6	P6
FF07H	Port register 7 Note 1	P7	Port register 7	P7
FF0CH	Port register 12 Note 1	P12	Port register 12	P12
FF22H	Port mode register 2 Note 1	PM2	Port mode register 2	PM2
FF24H	– Note 2	–	Port mode register 4	PM4
FF26H	Port mode register 6 Note 1	PM6	Port mode register 6	PM6
FF27H	Port mode register 7 Note 1	PM7	Port mode register 7	PM7
FF29H	Analog input channel specification register Note 1	ADS	Analog input channel specification register	ADS
FF2CH	Port mode register 12 Note 1	PM12	Port mode register12	PM12
FF2FH	A/D port configuration register Note 1	ADPC	A/D port configuration register	ADPC
FF34H	– Note 2	–	Pull-up resistor option register4	PU4
FF37H	Pull-up resistor option register7 Note 1	PU7	Pull-up resistor option register7	PU7
FF6EH	Key return mode register Note 1	KRM	Key return mode register	KRM
FF6FH	Watch timer operation mode register Note 1	WTM	Watch timer operation mode register	WTM
FF9FH	Clock operation mode select register Note 1	OSCCTL	Clock operation mode select register	OSCCTL
FFA8H	IIC clock selection register Note 1	IICCL0	IIC clock selection register	IICCL0
FFFBH	Processor clock control register Note 1	PCC	Processor clock control register	PCC

Notes 1. Different in bit setting.

2. Be sure not to write this register.

3.3 Differences in Register Bit Setting from 78K0/KC2 (44-pin)

3.3.1 Port mode register

μPD78F8014A, 78F8015A, 78F8016A

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	1	1	1	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	1	1	1	1	1	PM70	FF27H	FFH	R/W
PM12	1	1	1	1	1	PM122	PM121	PM120	FF2CH	FFH	R/W

Cautions 1. Be sure to set '1' on PM2 bit 5 to 7.

2. Be sure to set '1' on PM6 bit 2 and 3.

3. Be sure to set '1' on PM7 bit 1 to 3.

4. Be sure to set '1' on PM12 bit 3 and 4.

78K0/KC2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	1	1	PM73	PM72	PM71	PM70	FF27H	FFH	R/W
PM12	1	1	1	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W

3.3.2 Port register

μPD78F8014A, 78F8015A, 78F8016A

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P2	0	0	0	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P6	0	0	0	0	0	0	P61	P60	FF06H	00H (output latch)	R/W
P7	0	0	0	0	0	0	0	P70	FF07H	00H (output latch)	R/W
P12	0	0	0	0	0	P122	P121	P120	FF0CH	00H (output latch)	R/W

78K0/KC2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P6	0	0	0	0	P63	P62	P61	P60	FF06H	00H (output latch)	R/W
P7	0	0	0	0	P73	P72	P71	P70	FF07H	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FF0CH	00H (output latch)	R/W

3.3.3 Pull-up resistor option register

μPD78F8014A, 78F8015A, 78F8016A

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU7	0	0	0	0	0	0	0	PU70	FF37H	00H	R/W

Caution Be sure to clear '0' on PU7 bit 3 to 7.

78K0/KC2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU7	0	0	0	0	PU73	PU72	PU71	PU70	FF37H	00H	R/W

3.3.4 Analog input channel specification register

μPD78F8014A, 78F8015A, 78F8016A

Address: FF29H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	Setting prohibited
1	1	0	Setting prohibited
1	1	1	Setting prohibited

Caution Be sure to clear '0' on bit 3 to 7.

78K0/KC2

Address: FF29H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Caution Be sure to clear '0' on bit 3 to 7.

3.3.5 A/D port configuration register

μPD78F8014A, 78F8015A, 78F8016A

Address: FF2FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0

ADPC2	ADPC1	ADPC0	Analog Input(A)/Digital I/O(D)switching				
			ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	A	A	A	A	A
0	0	1	A	A	A	A	D
0	1	0	A	A	A	D	D
0	1	1	A	A	D	D	D
1	0	0	A	D	D	D	D
1	0	1	D	D	D	D	D
Other than above			Setting prohibit				

Caution Be sure to clear '0' on bit 3.

78K0/KC2

Address: FF2FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Analog input(A) / Digital I/O (D) switching							
				ANI7/ P27	ANI6/ P26	ANI5/ P25	ANI4/ P24	ANI3/ P23	ANI2/ P22	ANI1/ P21	ANI0/ P20
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	A	A	A	A	A	A	D
0	0	1	0	A	A	A	A	A	A	D	D
0	0	1	1	A	A	A	A	A	D	D	D
0	1	0	0	A	A	A	A	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

3.3.6 Key return mode register

μPD78F8014A, 78F8015A, 78F8016A

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	0	0	0	KRM0

Caution Be sure clear '0' on bit 1 to 7.

78K0/KC2

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	KRM3	KRM2	KRM1	KRM0

3.3.7 Watch timer operation mode register

μPD78F8014A, 78F8015A, 78F8016A

Address: FF6FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WTM	0	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

Caution Bit 7 must always be set to '0'. It is read-only.

78K0/KC2

Address: FF6FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WTM	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM7	Watch timer count clock selection (f_W)					
		f_{SUB}= 32.768 kHz	f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	$f_{PRS}/2^7$	–	15.625 kHz	39.062 kHz	78.125 kHz	156.25 kHz
1	f_{SUB}	32.768 kHz	–			

Remarks 1. f_W: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

3.3.8 Clock operation mode select register

μPD78F8014A, 78F8015A, 78F8016A

Address: FF9FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSCCTL	EXCLK	OSCSEL	0	0	0	0	0	AMPH

Caution Be sure to clear '0' on bit 4 to 5.

78K0/KC2

Address: FF9FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSCCTL	EXCLK	OSCSEL	EXCLKS	OSCSELS	0	0	0	AMPH

3.3.9 Processor clock control register

μPD78F8014A, 78F8015A, 78F8016A

Address: FFFBH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
PCC	0	0	0	0	0	PCC2	PCC1	PCC0

Cautions 1. Bit 5 is read-only.

2. Be sure to clear '0' on bit 4 and bit 6.

78K0/KC2

Address: FFFBH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
PCC	0	XTSTART	CLS	CSS	0	PCC2	PCC1	PCC0

Caution Bit 5 is read-only.

3.3.10 IIC clock selection register 0

μPD78F8014A, 78F8015A, 78F8016A

Address: FFA8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

Selection Clock Setting

IICX0	IICCL0			Selection Clock	Transfer Clock	Settable Selection Clock	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0	(f_W)	(f_W/m)	(f_W) Range	
CLX0	SMC0	CL01	CL00				
0	0	0	0	f_{PRS}/2	f_W/44	2.00 MHz to 4.19 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	f_{PRS}/2	f_W/86	4.19 MHz to 8.38 MHz	
0	0	1	0	f_{PRS}/4	f_W/86		
0	0	1	1	Setting prohibited			
0	1	0	×	f_{PRS}/2	f_W/24	4.00 MHz to 8.38 MHz	High-speed mode (SMC0 bit = 1)
0	1	1	0	f_{PRS}/4	f_W/24		
0	1	1	1	Setting prohibited			
1	0	×	×	Setting prohibited			
1	1	0	×	f_{PRS}/2	f_W/12	4.00 MHz to 4.19 MHz	High-speed mode (SMC0 bit = 1)
1	1	1	0	f_{PRS}/4	f_W/12		
1	1	1	1	Setting prohibited			

78K0/KC2

Address: FFA8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

Selection Clock Setting

IICX0	IICCL0			Selection Clock	Transfer Clock	Settable Selection Clock	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0	(f_W)	(f_W/m)	(f_W) Range	
CLX0	SMC0	CL01	CL00				
0	0	0	0	f_{PRS}/2	f_W/44	2.00 to 4.19 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	f_{PRS}/2	f_W/86	4.19 to 8.38 MHz	
0	0	1	0	f_{PRS}/4	f_W/86		
0	0	1	1	f_{EXSCL0}	f_W/66	6.4 MHz	
0	1	0	×	f_{PRS}/2	f_W/24	4.00 to 8.38 MHz	High-speed mode (SMC0 bit = 1)
0	1	1	0	f_{PRS}/4	f_W/24		
0	1	1	1	f_{EXSCL0}	f_W/18	6.4 MHz	
1	0	×	×	Setting prohibited			
1	1	0	×	f_{PRS}/2	f_W/12	4.00 to 4.19 MHz	High-speed mode (SMC0 bit = 1)
1	1	1	0	f_{PRS}/4	f_W/12		
1	1	1	1	Setting prohibited			

Remarks 1. ×: Don't care

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{EXSCL0}: External clock frequency from EXSCL0 pin

CHAPTER 4 WRITING WITH FLASH PROGRAMMER

Data can be written to the flash memory on-board or off-board, by using a dedicated flash programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the device has been mounted on the target system. The connectors that connect the dedicated flash programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the device is mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

Table 4-1. Wiring Dedicated Flash Programmer

Pin Configuration of Dedicated Flash Programmer			With CSI10		With UART6	
Signal Name	I/O	Pin Function	Pin name	Pin No.	Pin Name.	Pin No.
SI/RxD	Input	Receive signal	SO10/P12	41	TxD6/P13	20
SO/TxD	Output	Transmit signal	SI10/RxD0/P11	42	RxD6/P14	19
SCK	Output	Transfer clock	$\overline{\text{SCK10}}$/TxD0/P10	43	–	–
CLK	Output	Clock to Micro	–Note 1	–	**Note 2**	**Note 2**
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	2	$\overline{\text{RESET}}$	2
FLMD0	Output	Mode signal	FLMD0	3	FLMD0	3
V_{DD}	I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	8	V_{DD}	8
			AV_{REF}	44	AV_{REF}	44
			SUP	26	SUP	26
			HDS	25	HDS	25
			VIC	24	VIC	24
			VRO	23	VRO	23
			–	–	UMODE	22
V_{SS}	–	GND	V_{SS}	7	V_{SS}	7
			AV_{SS}	45	AV_{SS}	45
			GND1	27	GND1	27
			GND2	39	GND2	39
			GND3	34	GND3	34

Notes 1. Only the internal high-speed oscillation clock (f_{RH}) can be used when CSI10 is used.

2. Only the X1 clock (f_X) or external main system clock (f_{EXCLK}) can be used when UART6 is used. When using the clock out of the flash programmer, connect CLK and EXCLK of the programmer.

- PG-FP5, FL-PR5, PG-FP4, FL-PR4: Please connect the programmer's CLK to EXCLK/X2/P122 (pin 4)

CHAPTER 5 POWER SUPPLY CIRCUIT

5.1 Power Supply Function

The power supply circuit is a stabilization power supply circuit that generates 5 V (typ.) output voltage from 12 V battery supply voltage.

The power supply circuit has the following function.

- Overcurrent protection function
- Thermal shutdown function

5.2 Power Supply Overcurrent Protection Function

This circuit protects the dropper by limiting the current when an overcurrent occurs in the power supply line due to a cause such as a load short.

The overcurrent is detected by using the potential difference on a register connected between the SUP and VIC pins.

The resistor needs to be connected so that the maximum current between the SUP and VIC pins, is kept less than 65 mA.

Current limit = Overcurrent detect voltage (V_{SUPlim}) / R_{OCD}

Overcurrent detect voltage (V_{SUPlim}) = $V_{SUP} - V_{IC}$

V_{SUPlim} = 150 mV (typ.)

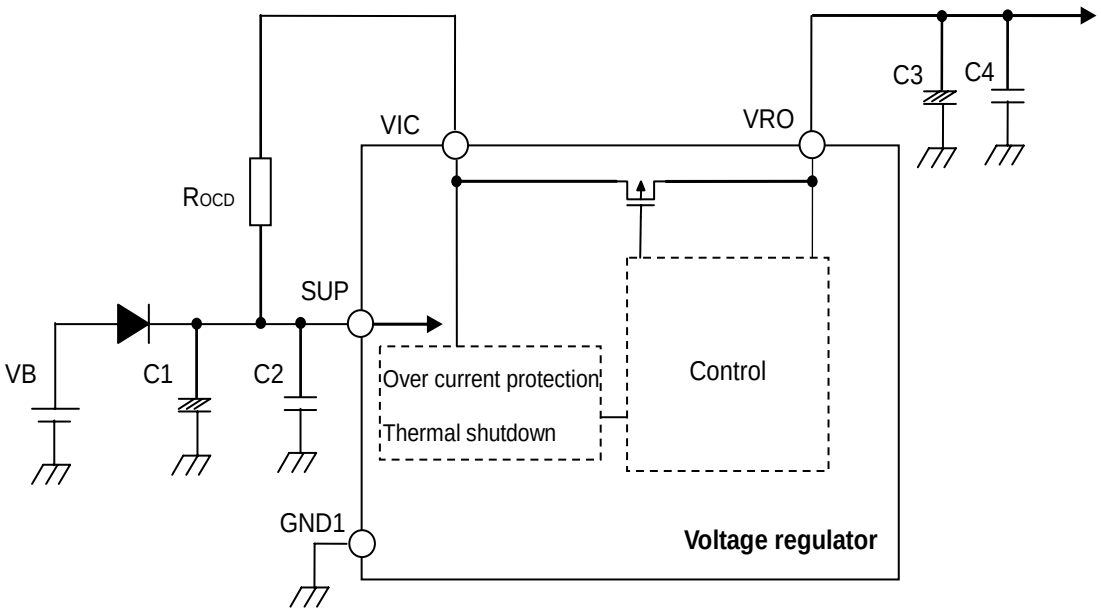
5.3 Power Supply Thermal Shutdown Function

This is a protection circuit for preventing destruction because of over temperature.

The temperature of the internal circuit is monitored and when the temperature exceeds the maximum limit the overheating detection temperature is detected and the internal P-ch MOS is forcibly switched off. After the dropper is forcibly switched off, it automatically switches back on after the temperature declines.

Caution The purpose of the built-in protection functions is to protect the device from abnormal operation. Try to avoid the use of these functions by designing the system properly.

Figure 5-1. Voltage regulator circuit application example



External parts target

C1 ≥ 33 μF

C2 ≥ 0.01 μF

4.7 μF ≤ C3 ≤ 100 μF

C4 ≥ 0.01 μF

Caution Place the ceramic capacitor (C2, C4) between the SUP and GND pin, the VRO and GND pins adjacent to the SUP, VRO pin and use the shortest possible wiring.

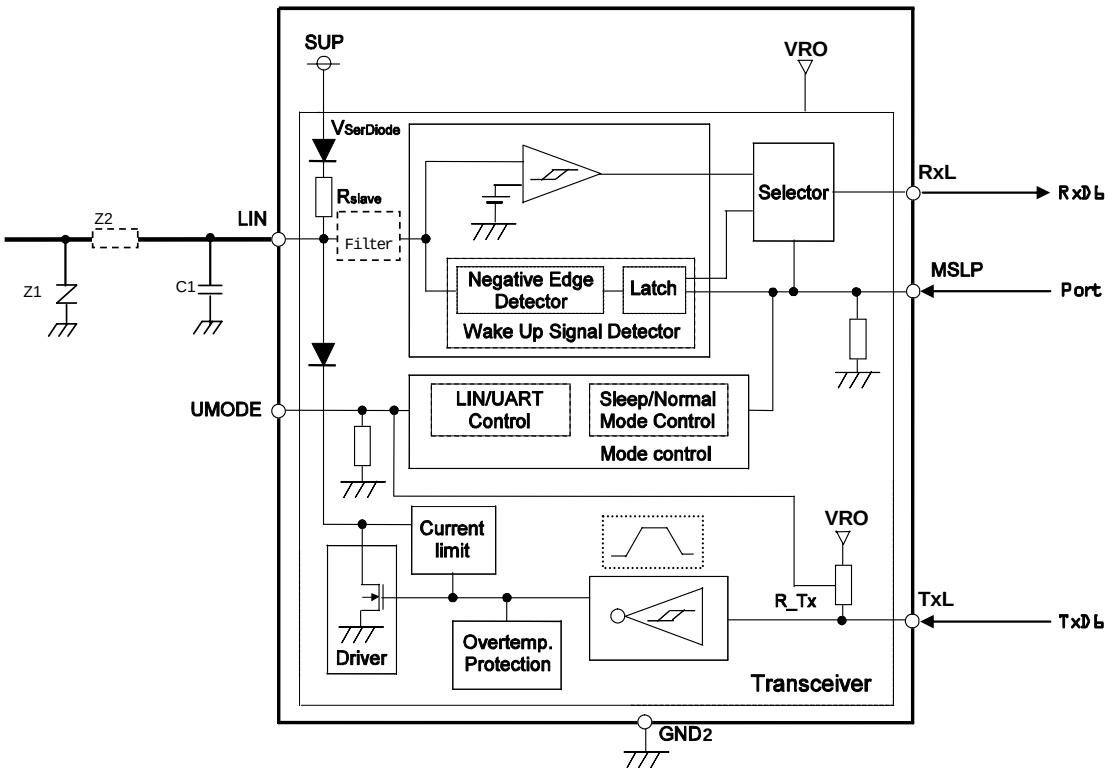
CHAPTER 6 LIN TRANSCEIVER FUNCTION

6.1 LIN Transceiver Function

The LIN transceiver and external specifications comply with LIN Specifications Rev.2.0.
The LIN transceiver has the following functions.

- Sleep function
- Overcurrent protection function
- Thermal shutdown function

Figure 6-1. LIN Transceiver Block Diagram



Remarks 1. RxL terminal is connected to P14/RxD6.

2. TxL terminal is connected to P13/TxD6.

3. LIN terminal includes slave pull-up register and diode.

6.2 Operation Mode

(1) UMODE = Low (LIN transceiver in operation mode)

The LIN transceiver has the following two modes.

Figure 6-2. Mode Transition Diagram

- Sleep mode

  When MSLP becomes low, the sleep mode is entered.

  In the sleep mode, the LIN driver output becomes OFF (recessive) regardless of the Tx pin input state.

  To reduce the current consumption, set the microcontroller's operation mode either to HALT or STOP mode.

- Normal mode

  When MSLP becomes high, the normal mode is entered. In the normal mode, the Tx input data can be output to the LIN bus.

Cautions 1. When using the LIN transceiver function, leave the UMODE pin open. (The UMODE pin is pulled down within the IC.)

2. When not using the LIN transceiver function, directly connect the UMODE pin to V_{DD} and set it to high level. When the UMODE pin is set to high level, the pull-up resistor of the LIN transceiver circuit (R_Tx) becomes unconnected.

3. The MSLP pin is pulled down within the IC.

(2) UMODE = High (LIN transceiver not in operation mode)

Unconditionally, LIN communication is OFF.

TxL and RxL are High impedance.

LIN terminal (N-ch open drain output) is OFF.

6.3 Overcurrent Limiter

The overcurrent limiter prevents the destruction of the device caused by overcurrent during a load short.

When a current occurs that exceeds the overcurrent detection value flows to the LIN driver due to a load short, etc., the output current is limited by inhibiting the gate voltage of the LIN driver.

6.4 Thermal Shutdown Circuit

This is a protection circuit for preventing destruction of the device due to over temperature.

The temperature of the LIN driver is monitored and when a temperature that exceeds the overheating detection temperature (MIN: 150°C) is detected, the LIN driver is forcibly switched off. After the LIN driver is forcibly switched off, it automatically switches back on after the temperature declines.

Caution The purpose of the built-in protection functions is to protect the device from abnormal operation.
Try to avoid the use of these functions by designing the system properly.

CHAPTER 7 DRIVER CIRCUIT

The driver circuit has 4 channels of a low side driver and 1 channel of a high side driver circuit.

7.1 Low Side Driver

(a) Dr1: 1 ch

Application: Pre driver for high side driver

The driver control input signal pin is Dr1_I. This pin has a pull-down resistor within the IC.

(b) Dr2: 2 ch

Application: Relay driver

The driver control input signal pins are Dr21_I and Dr22_I. This pin has a pull-down resistor and clamp circuit within the IC.

As driver input of Dr21_I and Dr22_I can either the 5V signal or the battery voltage signal either be used. When the battery voltage is input to Dr21_I and Dr22_I the system needs an external resistor. For details, please refer to the application example.

The drivers Dr21 and Dr22 have a dynamic clamp circuit for high voltage protection. The dynamic clamp circuit does not operate when the supply voltage V_{SUP} is more than 28V.

(c) Dr3: 1 ch

Application: LED driver

The driver control input signal pin is Dr3_I. This pin has a pull-down resistor within the IC.

7.2 High Side Driver

(a) Dr4: 1 ch

Application: Hall sensor power supply driver

The driver control input signal pin is Dr4_I. This pin has a pull-down resistor within the IC.

The driver Dr4 has an output voltage clump function, an overcurrent protection and a thermal shutdown function.

The overcurrent limiter prevents destruction of the driver caused by an overcurrent during a load short. When a current that exceeds the overcurrent detection value flows to the Dr4 due to a load short, etc. the output current is limited by inhibiting the gate voltage of Dr4.

The temperature of the Dr4 is monitored and when a temperature that exceeds the overheating detection temperature (MIN: 150°C) is detected, the Dr4 is forcibly switched off.

After the Dr4 is forcibly switched off, it automatically switches back on after the temperature declines.

Caution The purpose of the built-in protection functions is to protect the device from abnormal operation.
Try to avoid the use of these functions by designing the system properly.

Table 7-1. Truth Table

Input		Dr1	Dr21	Dr22	Dr3	Dr4
Dr1_I	High	ON	–	–	–	–
	Low	OFF	–	–	–	–
Dr21_I	High	–	ON	–	–	–
	Low	–	OFF	–	–	–
Dr22_I	High	–	–	ON	–	–
	Low	–	–	OFF	–	–
Dr3_I	High	–	–	–	ON	–
	Low	–	–	–	OFF	–
Dr4_I	High	–	–	–	–	ON
	Low	–	–	–	–	OFF

Figure 7-1. Low Side Driver Circuit Application Example

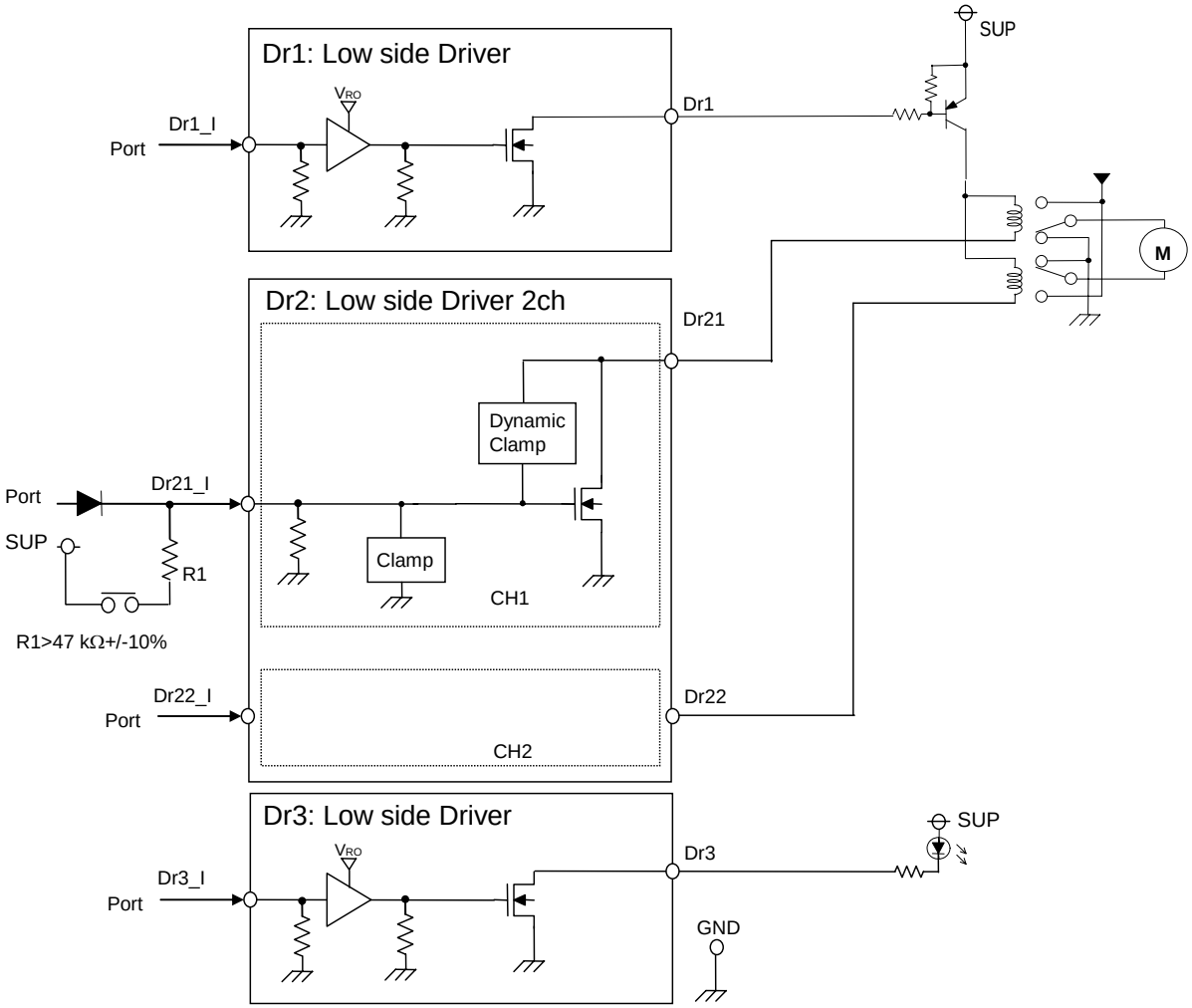
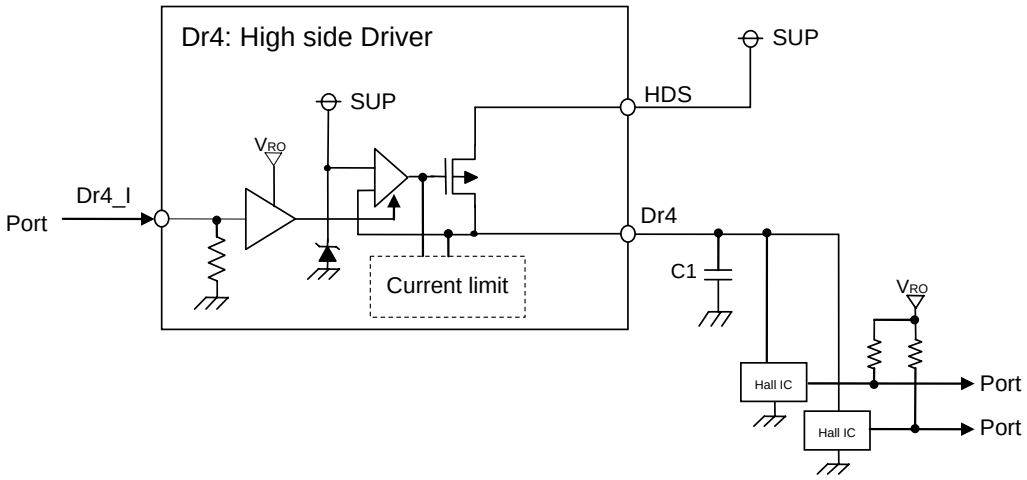


Figure 7-2. High Side Driver Circuit Application Example



CHAPTER 8 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS

8.1 Absolute Maximum Ratings

Absolute Maximum Ratings for Microcontroller block (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			−0.5 to +6.5	V
	V_{SS}			−0.5 to +0.3	V
	AV_{REF}			−0.5 to V_{DD}+0.3 Note	V
	AV_{SS}			−0.5 to +0.3	V
Input voltage	V_{I1}	P00, P01, P10 to P17, P20 to P24, P30 to P33, P70, P120 to P122, $\overline{\text{RESET}}$, FLMD0		−0.3 to V_{DD}+0.3	V
	V_{I2}	P60, P61 (N-ch open drain)		−0.3 to +6.5	V
REGC pin input voltage	V_{IREGC}			−0.5 to +3.6 and −0.5 to V_{DD}	V
Output voltage	V_O			−0.3 to V_{DD}+0.3 Note	V
Analog input voltage	V_{AN}	ANI0 to ANI4		−0.3 to AV_{REF}+0.3 Note and −0.3 to V_{DD}+0.3 Note	V
Output current, high	I_{OH1}	Per pin		−10	mA
		Total of all pins −80 mA	P00, P01, P120	−25	mA
			P10 to P17, P30 to P33, P70	−55	
	I_{OH2}	Per pin	P20 to P24	−0.5	mA
		Total of all pins		−2	
	I_{OH3}	Per pin	P121, P122	−1	mA
		Total of all pins		−4	
Output current, low	I_{OL1}	Per pin		30	mA
		Total of all pins 200 mA	P00, P01, P120	60	mA
			P10 to P17, P30 to P33, P60, P61, P70	140	
	I_{OL2}	Per pin	P20 to P24	1	mA
		Total of all pins		5	
	I_{OL3}	Per pin	P121, P122	4	mA
		Total of all pins		10	

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings for Analog block (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VSUP1	VSUP, HDS, 400 ms	−0.3 to +60	V
	VSUP2	VSUP, HDS, 2 min	−0.3 to +28	V
	VSUP3	VSUP, HDS	−0.3 to +20	V
	VRO	VRO	−0.3 to +6.5	V
Input voltage	VIA1	VIC, LIN, Dr21_I, Dr22_I, 400 ms, Dr21_I and Dr22_I are input pin potentials with external 47 kΩ resistors.	−0.3 to +60	V
	VIA2	VIC, LIN, Dr21_I, Dr22_I, 2 min, Dr21_I and Dr22_I are input pin potentials with external 47 kΩ resistors.	−0.3 to +28	V
	VIA3	VIC, LIN	−0.3 to +20	V
	VIA4	MSLP, UMODE, Dr1_I, Dr3_I, Dr4_I	−0.3 to VRO+0.3 Note	V
Input current	IDRin	Dr21_I, Dr22_I	1.5	mA
LIN negative voltage	VILlin	LIN, 7 V≤VSUP≤19 V, 1 s	VSUP−60	V
Output voltage	VOA1	LIN, Dr1, Dr21, Dr22, Dr3, Dr4, 400 ms	−0.3 to +60	V
	VOA2	LIN, Dr1, Dr21, Dr22, Dr3, Dr4, 2 min	−0.3 to +28	V
	VOA3	LIN, Dr1, Dr21, Dr22, Dr3, Dr4	−0.3 to +20	V
Output current	ICM1	VRO	25	mA
	ICM2	VRO 1 s	65	mA
	ILIN	LIN	200	mA
	IDr1	Dr1	10	mA
	IDr2	Dr21, Dr22	150	mA
	IDr3	Dr3	50	mA
	IDr4	Dr4	−40	mA

Note Must be 6.5 V or lower.

Absolute Maximum Ratings for Common Item (T_A = 25°C)

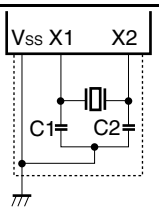
Parameter	Symbol	Conditions	Ratings	Unit
Operation ambient temparatuer	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_{jmaxv}		140	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

8.2 Microcontroller Block Characteristics

X1 Oscillator Characteristics

(T_A = –40 to +85 °C, 1.8 V≤V_{DD}≤5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator, Crystal resonator		X1 Clock Oscillation frequency (f_X) Note 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0 Note 2		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		5.0	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the Internal oscillator after reset is released, check the oscillation stabilization time of the X1 oscillation clock using the oscillation stabilization time status register (OSTC). Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Internal Oscillator Characteristics

(T_A = –40 to +85 °C, 1.8 V≤V_{DD}≤5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
8 MHz Internal oscillator	Internal high-speed oscillation Clock frequency (f_{RH})[Note]	RSTS = 1	2.7 V≤V_{DD}≤5.5 V	7.6	8.0	8.4	MHz
			1.8 V≤V_{DD}<2.7 V	7.6	8.0	10.4	MHz
		RSTS = 0		2.48	5.6	9.86	MHz
240 kHz Internal oscillator	Internal low-speed oscillation Clock frequency (f_{RL})		2.7 V≤V_{DD}≤5.5 V	216	240	264	kHz
			1.8 V≤V_{DD}<2.7 V	192	240	264	kHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Remark RSTS: internal oscillator mode resister (RCM) bit7

DC Characteristics (1/5)

(T_A = −40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00, P01, P10 to P17, P30 to P33, P70, P120	4.0 V≤V_{DD}≤5.5 V			−3.0	mA
			2.7 V≤V_{DD}<4.0 V			−2.5	mA
			1.8 V≤V_{DD}<2.7 V			−1.0	mA
		Total of pins[Note 2] P00, P01, P120	4.0 V≤V_{DD}≤5.5 V			−12.0	mA
			2.7 V≤V_{DD}<4.0 V			−7.0	mA
			1.8 V≤V_{DD}<2.7 V			−5.0	mA
		Total of pins[Note 2] P10 to P17, P30 to P33, P70	4.0 V≤V_{DD}≤5.5 V			−18.0	mA
			2.7 V≤V_{DD}<4.0 V			−15.0	mA
			1.8 V≤V_{DD}<2.7 V			−10.0	mA
		Total of pins[Note 2]	4.0 V≤V_{DD}≤5.5 V			−23.0	mA
			2.7 V≤V_{DD}<4.0 V			−20.0	mA
			1.8 V≤V_{DD}<2.7 V			−15.0	mA
	I_{OH2}	Per pin for P20 to P24	AV_{REF} = V_{DD}			−0.1	mA
		Per pin for P121, P122				−0.1	mA
Output current, low[Note 3]	I_{OL1}	Per pin for P00, P01, P10 to P17, P30 to P33, P70, P120	4.0 V≤V_{DD}≤5.5 V			8.5	mA
			2.7 V≤V_{DD}<4.0 V			5.0	mA
			1.8 V≤V_{DD}<2.7 V			2.0	mA
		Per pin for P60, P61	4.0 V≤V_{DD}≤5.5 V			15.0	mA
			2.7 V≤V_{DD}<4.0 V			5.0	mA
			1.8 V≤V_{DD}<2.7 V			2.0	mA
		Total of pins[Note 2] P00, P01, P120	4.0 V≤V_{DD}≤5.5 V			20.0	mA
			2.7 V≤V_{DD}<4.0 V			15.0	mA
			1.8 V≤V_{DD}<2.7 V			9.0	mA
		Total of pins[Note 2] P10 to P17, P30 to P33, P60, P61, P70	4.0 V≤V_{DD}≤5.5 V			45.0	mA
			2.7 V≤V_{DD}<4.0 V			35.0	mA
			1.8 V≤V_{DD}<2.7 V			20.0	mA
		Total of pins[Note 2]	4.0 V≤V_{DD}≤5.5 V			65.0	mA
			2.7 V≤V_{DD}<4.0 V			50.0	mA
			1.8 V≤V_{DD}<2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P24	AV_{REF} = V_{DD}			0.4	mA
		Per pin for P121, P122				0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7) / (n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = 20.0 mA

Total output current of pins = (20.0 × 0.7) / (50 × 0.01) = 28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/5)

(T_A = −40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P12, P13, P15, P121, P122		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70, P120, RESET		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P24	AV_{REF} = V_{DD}	0.7 AV_{REF}		AV_{REF}	V
	V_{IH4}	P60, P61		0.7 V_{DD}		6.0	V
Input voltage, low	V_{IL1}	P12, P13, P15, P60 to P61, P121, P122		0		0.3 V_{DD}	V
	V_{IL2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70, P120, RESET		0		0.2 V_{DD}	V
	V_{IL3}	P20 to P24	AV_{REF} = V_{DD}	0		0.3 AV_{REF}	V
Output voltage, high	V_{OH1}	P00, P01, P10 to P17, P30 to P33, P70, P120	4.0 V≤V_{DD}≤5.5 V, I_{OH1} = −3.0 mA	V_{DD}−0.7			V
			2.7 V≤V_{DD}<5.5 V, I_{OH1} = −2.5 mA	V_{DD}−0.5			V
			1.8 V≤V_{DD}<5.5 V, I_{OH1} = −1.0 mA	V_{DD}−0.5			V
	V_{OH2}	P20 to P24	AV_{REF} = V_{DD}, I_{OH2} = −100 μA	V_{DD}−0.5			V
		P121, P122	I_{OH2} = −100 μA	V_{DD}−0.5			V
Output voltage, low	V_{OL1}	P00, P01, P10 to P17, P30 to P33, P120	4.0 V≤V_{DD}≤5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V≤V_{DD}<5.5 V, I_{OL1} = 5.0 mA			0.7	V
			I_{OL1} = 2.0 mA			0.5	V
			I_{OL1} = 0.5 mA			0.4	V
	V_{OL2}	P20 to P24	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V
		P121, P122	I_{OL2} = 0.4 mA				
	V_{OL3}	P60, P61	4.0 V≤V_{DD}≤5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V≤V_{DD}≤5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V≤V_{DD}<4.0 V, I_{OL1} = 5.0 mA			0.6	V
			2.7 V≤V_{DD}<5.5 V, I_{OL1} = 3.0 mA			0.4	V
			I_{OL1} = 2.0 mA			0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/5)

(T_A = −40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P10 to P17, P30 to P33, P60, P61, P70, P120	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P24	$V_I = AV_{REF}$, $AV_{REF} = V_{DD}$				1	μA
	I_{LIH3}	P121, P122 (X1, X2)	$V_I = V_{DD}$	I/O port mode			1	μA
				OSC mode			20	μA
Input leakage current , low	I_{LIL1}	P00, P01, P10 to P17, P30 to P33, P60, P61, P70, P120	$V_I = V_{SS}$				−1	μA
	I_{LIL2}	P20 to P24	$V_I = V_{SS}$, $AV_{REF} = V_{DD}$				−1	μA
	I_{LIL3}	P121, P122 (X1, X2)	$V_I = V_{SS}$	I/O port mode			−1	μA
				OSC mode			−20	μA
Pull-up resister	R_U	$V_I = V_{DD}$			10	20	100	kΩ
FLMD0 supply voltage	V_{IL}	In normal operation mode			0		0.2 V_{DD}	V
	V_{IH}	In self-programming mode			0.8 V_{DD}		V_{DD}	V
External clock input voltage	V_{IL}	P122 in external clock mode			0		0.2 V_{DD}	V
	V_{IH}	P122 in external clock mode			0.8 V_{DD}		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (4/5)

(T_A = –40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current **Note 1**	I_{DD1}	Operation mode	f_{XH} = 20 MHz[Note 2], V_{DD} = 5.0 V	Square-wave input		3.2	5.5	mA
				Connect resonator		4.5	6.9	mA
			f_{XH} = 10 MHz[Notes 2, 3], V_{DD} = 5.0 V	Square-wave input		1.6	2.8	mA
				Connect resonator		2.3	3.9	mA
			f_{XH} = 10 MHz[Notes 2, 3], V_{DD} = 3.0 V	Square-wave input		1.5	2.7	mA
				Connect resonator		2.2	3.2	mA
			f_{XH} = 5 MHz[Notes 2, 3], V_{DD} = 3.0 V	Square-wave input		0.9	1.6	mA
				Connect resonator		1.3	2.0	mA
			f_{XH} = 5 MHz[Notes 2, 3], V_{DD} = 2.0 V	Square-wave input		0.7	1.4	mA
				Connect resonator		1.0	1.6	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V[Note 4]			1.4	2.5	mA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz[Note 2], V_{DD} = 5.0 V	Square-wave input		0.8	2.6	mA
				Connect resonator		2.0	4.4	mA
			f_{XH} = 10 MHz[Notes 2, 3], V_{DD} = 5.0 V	Square-wave input		0.4	1.3	mA
				Connect resonator		1.0	2.4	mA
			f_{XH} = 5 MHz[Notes 2, 3], V_{DD} = 3.0 V	Square-wave input		0.2	0.65	mA
				Connect resonator		0.5	1.1	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V[Note 4]			0.4	1.2	mA
	I_{DD3}	STOP mode[Note 5]	V_{DD} = 5.0 V			1	20	μA
			V_{DD} = 5.0 V, T_A = –40 to +70 °C			1	10	μA

Notes 1. Total current flowing into the internal power supply (V_{DD}), including the peripheral operation current. Port output current and current flowing through on-chip pull-up resistor are not included. Input leakage current with input pin fixed to V_{DD} or V_{SS} is included.

2. Operational current of the 8 MHz internal oscillator and 240 kHz internal oscillator is not included. TYP. value indicates current when only the CPU is operating. MAX. value includes peripheral operating current. However, WDT, LVI, and ADC stop (ADCE = 0).

3. When AMPH (bit 0 of clock operation mode select register (OSCCTL)) = 0

4. Operational current of the X1 oscillator and 240 kHz internal oscillator is not included. TYP. value indicates current when only the CPU is operating. MAX. value includes peripheral operating current. However, WDT, LVI, and ADC stop (ADCE = 0).

5. Operational current of the 240 kHz internal oscillator is not included. MAX. value includes peripheral operating current. However, WDT, LVI, and ADC stop (ADCE = 0).

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency) .

2. f_{RH}: Internal high-speed oscillation clock frequency.

DC Characteristics (5/5)

(T_A = –40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A/D converter operation current	I_{ADC} Note 1			0.86	1.9	mA
Watchdog timer operating current	I_{WDT} Note 2	During 240 kHz internal low-speed oscillation clock operation		5	10	μA
LVI operating Current	I_{LVI} Note 3			9	18	μA

Notes 1. Current flowing only to the A/D converter. The current value of the microcontroller is the sum of I_{DD} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

2. Current flowing only to the watchdog timer. The current value of the, microcontroller is the sum of I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in the HAT or STOP mode.

3. Current flowing only to the LVI circuit. The current value of the microcontroller is the sum of I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates in the HALT or STOP mode.

AC Characteristics

(1) Basic operation

(T_A = –40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	UNIT
Instruction cycle (minimum instruction execution time	T_{CY}	Main system clock operation (f_{XP})	2.7 V≤V_{DD}≤5.5 V	0.1		32	μs
			1.8 V≤V_{DD}<2.7 V	0.4 Note 1		32	μs
Peripheral hardware clock frequency	f_{PRS}	XSEL = 1	2.7 V≤V_{DD}≤5.5 V			20	MHz
			1.8 V≤V_{DD}<2.7 V			5	MHz
		XSEL = 0	2.7 V≤V_{DD}<4.0 V	7.6		8.4	MHz
			1.8 V≤V_{DD}<2.7 V Note 2	7.6		10.4	MHz
External main system clock frequency	f_{EXCLK}	2.7 V≤V_{DD}≤5.5 V		1.0 Note 3		20.0	MHz
		1.8 V≤V_{DD}<2.7 V		1.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXCLKH}, t_{EXCLKL}	2.7 V≤V_{DD}≤5.5 V		24			ns
		1.8 V≤V_{DD}<2.7 V		96			ns
TI000, TI010 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	4.0 V≤V_{DD}≤5.5 V		$2/f_{sam}$+0.1 Note 4			μs
		2.7 V≤V_{DD}<4.0 V		$2/f_{sam}$+0.2 Note 4			μs
		1.8 V≤V_{DD}<2.7 V		$2/f_{sam}$+0.5 Note 4			μs
TI50, TI51 input frequency	f_{TI5}	4.0 V≤V_{DD}≤5.5 V				10	MHz
		2.7 V≤V_{DD}<4.0 V				10	MHz
		1.8 V≤V_{DD}<2.7 V				5	MHz
TI50, TI51 input high-level width, low-level width	t_{TIH5}, t_{TIL5}	4.0 V≤V_{DD}≤5.5 V		50			ns
		2.7 V≤V_{DD}<4.0 V		50			ns
		1.8 V≤V_{DD}<2.7 V		100			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
Key interrupt input low-level width	t_{KR}			250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

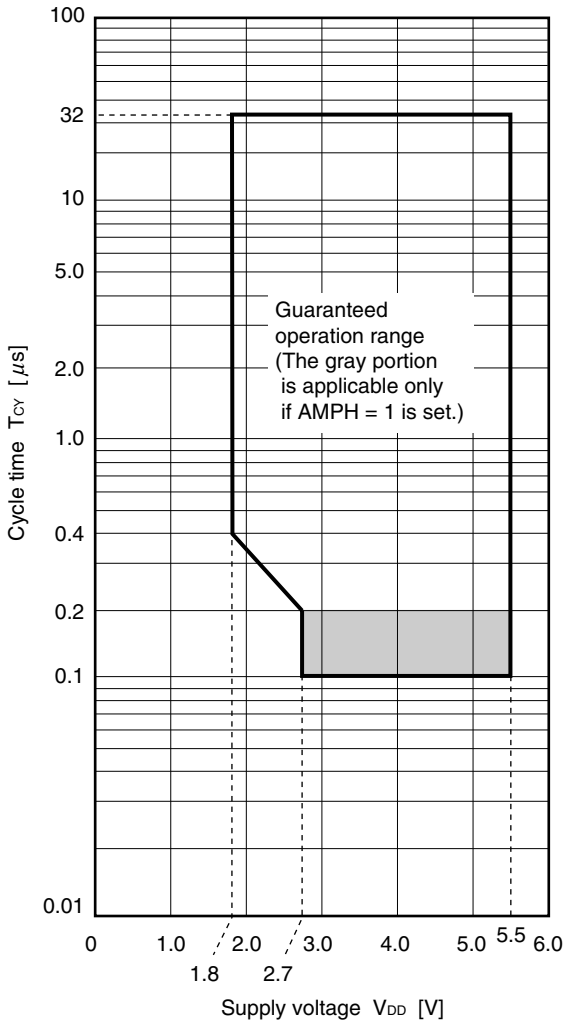
Notes 1. 0.38 μs when operating with the 8 MHz internal oscillator.

2. This specification defines the selection clock primary frequency. Therefore, select the division clock that sets the peripheral hardware clock frequency to 5.2 MHz (MAX.).

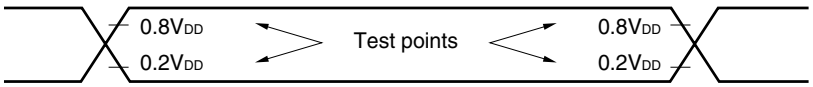
3. It is 2.0 MHz (MIN.) when programming on the board via UART6.

4. Selection of f_{sam} = f_{PRS}/4, f_{PRS}/256 is possible using bits 0 and 1 (PRM000, PRM001) of Prescaler mode register 00 (PRM00). Note that when selecting the TI00 valid edge asthe clock, f_{sam} = f_{PRS}.

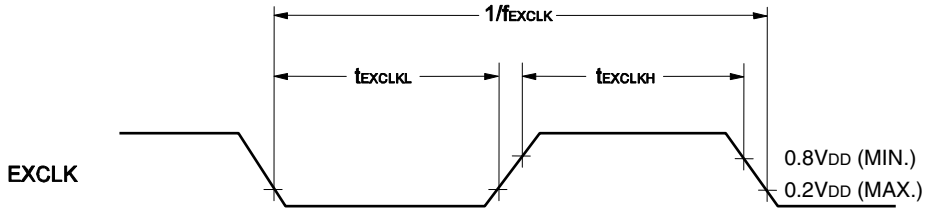
T_{CY} vs V_{DD} (Main System Clock Operation)



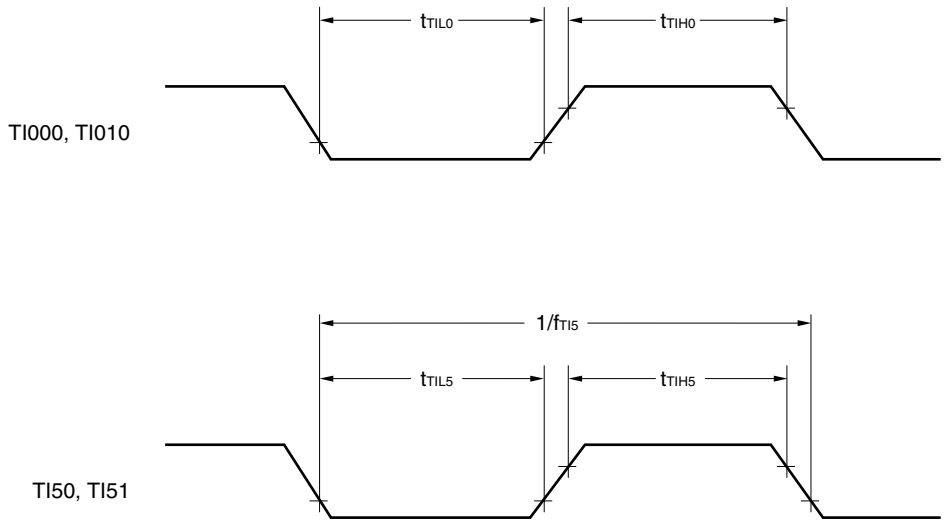
AC Timing Test Points (Excluding External Main System Clock)



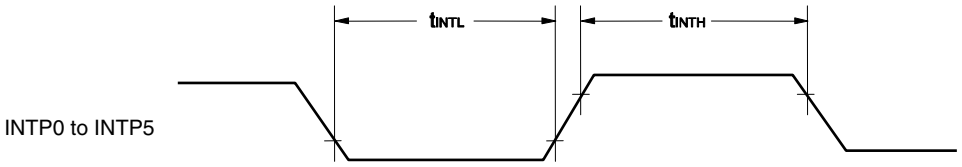
External Main System Clock Timing



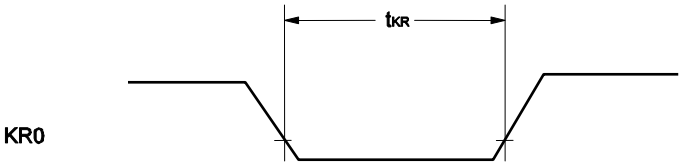
TI Timing



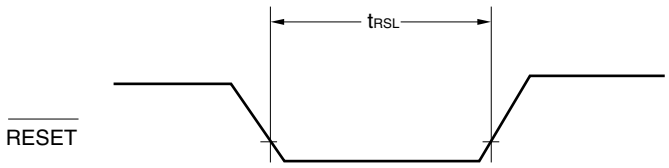
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(2) Serial Interface

(T_A = –40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

(a) UART6 (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	Kbps

(b) UART0 (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(c) IIC0

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{CLK}		0	100	0	400	kHz
Reset condition setup time	$t_{SU: STA}$		4.7		0.6		μs
Hold time Note 1	$t_{HD: STA}$		4.0		0.6		μs
Hold tome when SCL0 = "L"	t_{LOW}	Internal clock operation	4.7		1.3		μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU: DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	When $f_W = f_{XH}/2^N$ is selected Note 3	0	3.45	0	0.9 Note 4	μs
						1.0 Note 5	μs
		When $f_W = f_{RH}/2^N$ is selected Note 3	0	3.45	0	1.05	μs
Stop condition setup time	$t_{SU: STO}$		4.0		0.6		μs
Bus free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/reset condition is detected.

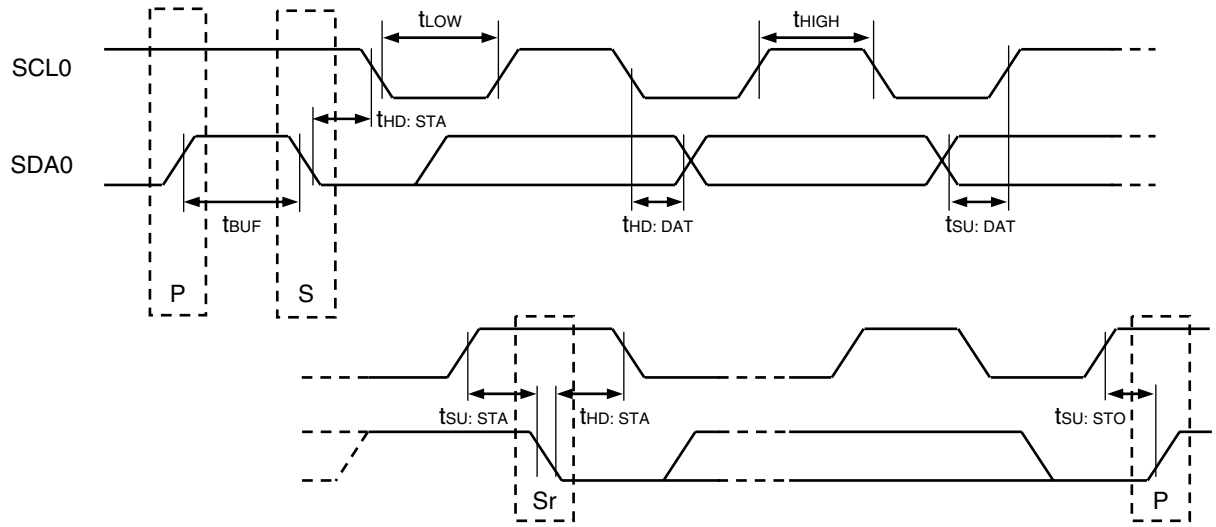
2. The maximum value (MAX.) of $t_{HD:DAT}$ is normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. f_W indicates the IIC0 transfer clock selected by the IICCL0 and IICX0 registers.

4. When $f_W \geq 4.4$ MHz is selected

5. When $f_W < 4.4$ MHz is selected

IIC0 Transfer Timing



P : Stop condition
S : Start condition
Sr : Restart condition

(d) CSI10 (master mode, $\overline{\text{SCK10}}$…internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK10}}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	200			ns
		2.7 V ≤ V_{DD} < 4.0 V	400			ns
		1.8 V ≤ V_{DD} < 2.7 V	600			ns
$\overline{\text{SCK10}}$ high/low level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2-20$ Note 1			ns
		2.7 V ≤ V_{DD} < 4.0 V	$t_{KCY1}/2-30$ Note 1			ns
		1.8 V ≤ V_{DD} < 2.7 V	$t_{KCY1}/2-60$ Note 1			ns
SI10 setup time (to $\overline{\text{SCK10}}$↑)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	70			ns
		2.7 V ≤ V_{DD} < 4.0 V	100			ns
		1.8 V ≤ V_{DD} < 2.7 V	190			ns
SI10 hold time (to $\overline{\text{SCK10}}$↑)	t_{KSI1}		30			ns
Delay time from $\overline{\text{SCK10}}$↓→ (to SO10 output)	t_{KSO1}	C = 50 pF Note 2			40	ns

Notes 1. This value is when high-speed system clcok (f_{XH}) is used.

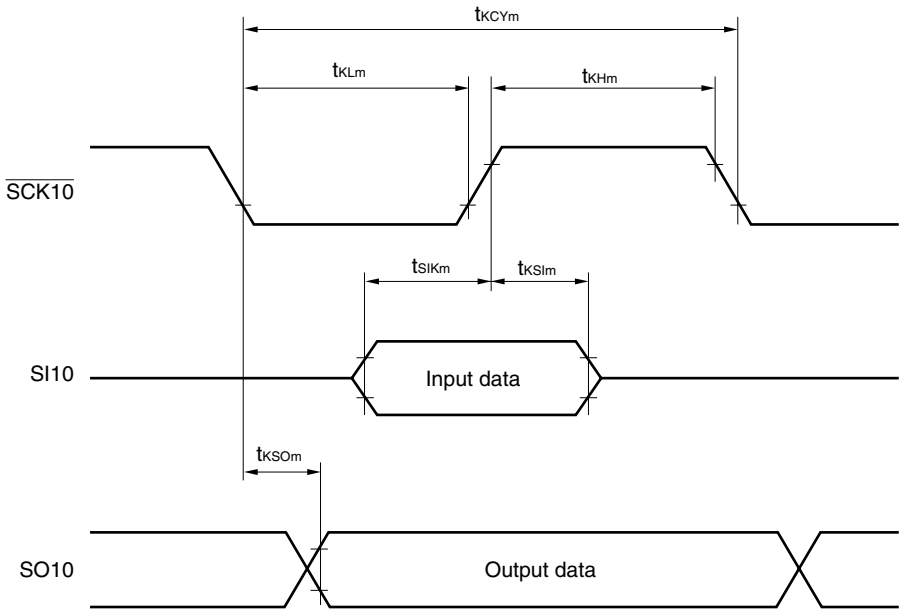
2. C is the load capacitance of the $\overline{\text{SCK10}}$ and SO10 output lines.

(e) CSI10 (slave mode, $\overline{SCK10}$...extenel clcok input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY2}			400			ns
$\overline{SCK10}$ high/low level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SI10 setup time (to $\overline{SCK10}\uparrow$)	t_{SIK2}			80			ns
SI10 hold time (to $\overline{SCK10}\uparrow$)	t_{KSI2}			50			ns
Delay time from $\overline{SCK10}\downarrow\rightarrow$ to SO10	t_{KSO2}	C = 50 pF[Note]	4.0 V≤V_{DD}≤5.5 V			120	ns
			2.7 V≤V_{DD}<4.0 V			120	ns
			1.8 V≤V_{DD}<2.7 V			180	ns

Note C is the load capacitance of the SO10 output line.

CSI10 Transfer Timing



Remark m = 1, 2

A/D Converter Characteristics

(T_A = –40 to +85°C, 1.8 V≤V_{DD}≤5.5 V, 2.3 V≤AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				10	bit
Overall error[Notes 1, 2]	AINL	4.0 V≤AV_{REF}≤5.5 V			±0.4	%FSR
		2.7 V≤AV_{REF}<4.0 V			±0.6	%FSR
		2.3 V≤AV_{REF}<2.7 V			±1.2	%FSR
Conversion time	tCONV	4.0 V≤AV_{REF}≤5.5 V	6.1		66.6	μs
		2.7 V≤AV_{REF}<4.0 V	12.2		66.6	μs
		2.3 V≤AV_{REF}<2.7 V	27		66.6	μs
Zero-scale error[Notes 1, 2]	EZS	4.0 V≤AV_{REF}≤5.5 V			±0.4	%FSR
		2.7 V≤AV_{REF}<4.0 V			±0.6	%FSR
		2.3 V≤AV_{REF}<2.7 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	EFS	4.0 V≤AV_{REF}≤5.5 V			±0.4	%FSR
		2.7 V≤AV_{REF}<4.0 V			±0.6	%FSR
		2.3 V≤AV_{REF}<2.7 V			±0.6	%FSR
Integral non-linearity error[Note 1]	ILE	4.0 V≤AV_{REF}≤5.5 V			±2.5	LSB
		2.7 V≤AV_{REF}<4.0 V			±4.5	LSB
		2.3 V≤AV_{REF}<2.7 V			±6.5	LSB
Differential non-linearity error[Note 1]	DLE	4.0 V≤AV_{REF}≤5.5 V			±1.5	LSB
		2.7 V≤AV_{REF}<4.0 V			±2.0	LSB
		2.3 V≤AV_{REF}<2.7 V			±2.0	LSB
Analog input voltage	VAIN		AV_{SS}		AV_{REF}	V

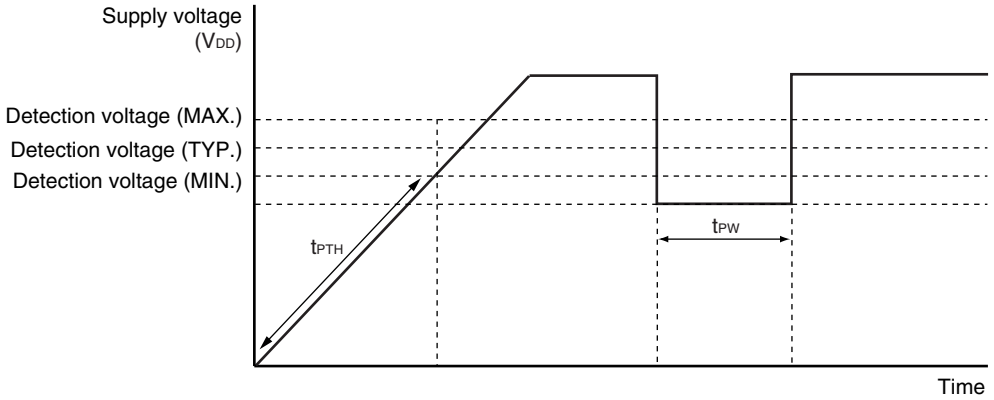
Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

1.59 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOC		1.44	1.59	1.74	V
Power voltage rise inclination	tPTH	V_{DD}: 0 V V_{POC} change inclination of V_{POC}	0.5			V/ms
Minimum pulse width	tPW		200			μs

POC Circuit timing

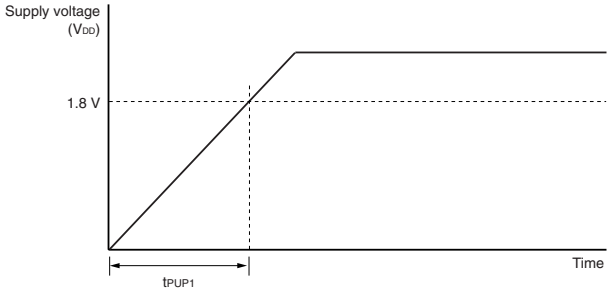


Supply Voltage Rise Time (T_A = –40 to +85°C, V_{SS} = 0 V)

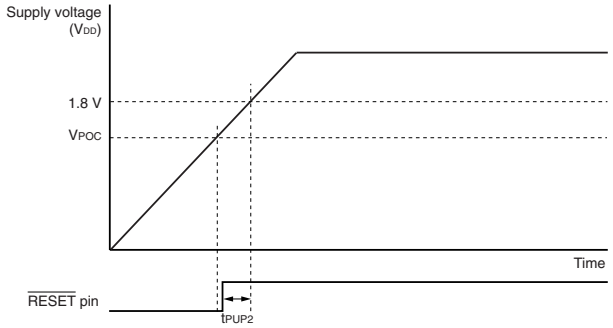
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (V_{DD}: 0 V→1.8 V)	t_{PUP1}	POCMODE (option byte) = 0, When $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (releasing $\overline{\text{RESET}}$ input →V_{DD}: 1.8 V)	t_{PUP2}	POCMODE (option byte) = 0, When $\overline{\text{RESET}}$ input is used.			1.9	ms

Supply voltage Rise Time Timing

- **When $\overline{\text{RESET}}$ pin input is not used.**



- **When $\overline{\text{RESET}}$ pin input is used.**



2.7 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option byte) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until V_{POC} = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC}, similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until V_{DDPOC} = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at V_{POC} = 1.59 V (TYP.) and not at V_{DDPOC}. The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH}.

LVI Circuit Characteristics (T_A = –40 to +85 °C, $V_{POC} \leq V_{DD} \leq 5.5$ V, $AV_{REF} \leq V_{DD}$, V_{SS} = 0 V)

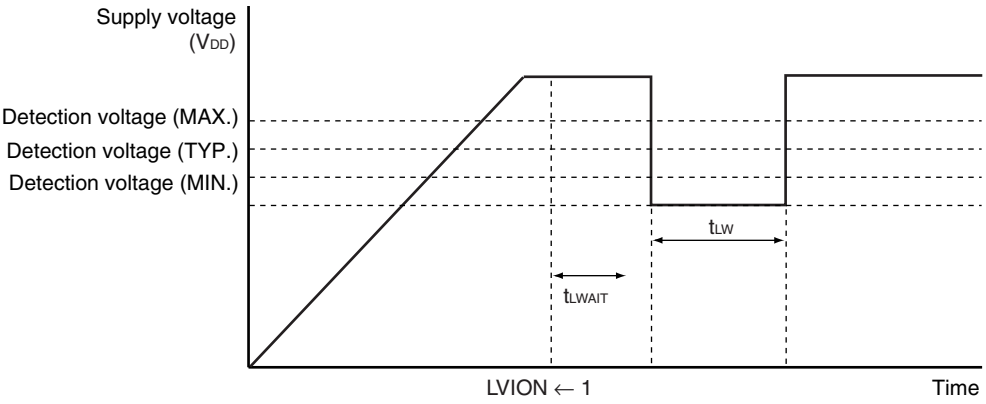
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.14	4.24	4.34	V
		V_{LVI1}		3.99	4.09	4.19	V
		V_{LVI2}		3.83	3.93	4.03	V
		V_{LVI3}		3.68	3.78	3.88	V
		V_{LVI4}		3.52	3.62	3.72	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.06	3.16	3.26	V
		V_{LVI8}		2.91	3.01	3.11	V
		V_{LVI9}		2.75	2.85	2.95	V
		V_{LVI10}		2.60	2.70	2.80	V
		V_{LVI11}		2.45	2.55	2.65	V
		V_{LVI12}		2.29	2.39	2.49	V
		V_{LVI13}		2.14	2.24	2.34	V
		V_{LVI14}		1.98	2.08	2.18	V
		V_{LVI15}		1.83	1.93	2.03	V
	External input pin[Note 1]	EXLVI	EXLVI<V_{DD}, 1.8 V≤V_{DD}≤5.5 V	1.11	1.21	1.31	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note 2]		t_{LWAIT}		10			μs

Notes 1. The EXLVI/P120/INTP0 Pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization.

Remark $V_{LVI\,(n-1)} > V_{LVIn}$: n = 1 to 15

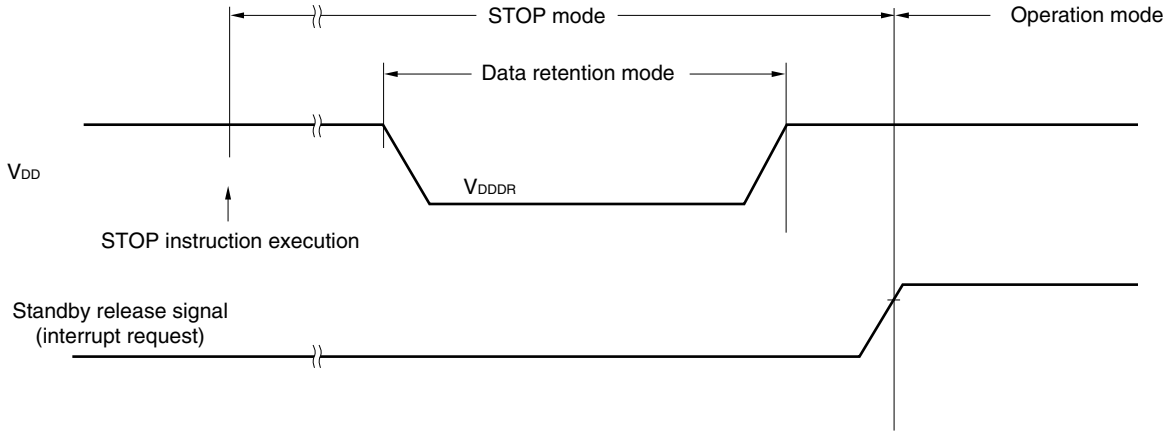
LVI Circuit Timing



Data Memory STOP mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POCreset is effected, but data is not retained when a POC reset is effected.



Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V≤V_{DD}≤5.5 V, AV_{REF}≤V_{DD}, V_{SS} = AV_{SS} = 0 V)

• Basic characteristics

Parameter		Symbol	Conditions			MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}	f_{XP} = 10 MHz (TYP.), 20 MHz (MAX.)				4.5	11.0	mA
Erase time[Notes 1, 2]	All block	T_{eraca}					20	200	ms
	Block unit	T_{erasa}					20	200	ms
Write time (in 8-bit units)[Note 1]		T_{wrwa}					10	100	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite[Note 3]	• When a flash memory programmer is used, and the libraries[Note 4] provided by NEC Electronics are used • For program update	15 years	1000			Times
				• When the EEPROM emulation libraries[Note 5] provided by NEC Electronics are used • The rewritable ROM size: 4 KB • For data update	5 years	10000			Times
				Conditions other than the above[Note 6]	10 years	100			Times

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP4 or PG-FP5, is used and the rewrite time during self programming, see refer to **CHAPTER 27 FLASH MEMORY** on **78K0/Kx2 User's Manual (U18598E)**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

4. The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual** (**U17516E**) is excluded.

5. The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (**U17517E**) is excluded.

6. These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual** (**U17516E**) and the sample program specified by **the 78K0/Kx2 EEPROM Emulation Application Note** (**U17517E**) are used.

Remarks 1. f_{XP}: Main system clock oscillation frequency

2. For serial write operation characteristics, refer to **78K0/Kx2 Flash Memory Programming (Programmer) Application Note (U17739E)**.

8.3 Analog Block Characteristics

Voltage regulator circuit characteristics (T_A = –40 to +85°C, 4.85 V ≤ V_{RO} ≤ 5.15 V, I_{RO} ≤ 15 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	V_{CCOUT1}	7 V≤V_{SUP}≤19 V V_{CCOUT} = V_{RO}, I_{RO} = 15 mA	4.85	5	5.15	V
	V_{CCOUT2}	19 V<V_{SUP}≤ 60 V V_{CCOUT} = V_{RO}, I_{RO} = 1 mA	(4.5)	(5)	(5.5)	V
Overcurrent detect voltage	V_{SUPlim}		100	150	230	mV
Load regulation	REG_L	1 mA<I_{RO}≤15 mA, V_{SUP} = 14 V			60	mV
Input regulation	REG_{IN1}	I_{CCOUT} = 15 mA			60	mV
Thermal shutdown	V_{Rth}		(150)			°C

Remark The values in parentheses are based on design for which no outgoing inspection has been performed.

Supply current Characteristics (T_A = –40 to +85°C, 4.85 V ≤ V_{RO} ≤ 5.15 V, 7 V ≤ V_{SUP} ≤ 19 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current[Note]	I_{BAT1}	DR4: OFF T_A = 25°C, V_{SUP} = 14V, LIN: Sleep			35	μA
	I_{BAT2}	DR4: OFF LIN: Sleep			60	μA
	I_{BAT3}	DR4: OFF LIN: Normal (LIN bus :Recessive)			3	mA

Note This is the total current flowing to the SUP, VRO internal power supply. The peripheral operating current is included. However, the current flow through the port pull-up resistor is not included. Not included V_{DD} current. For microcontroller supply current, refer to **78K0/Kx2 User's Manual (U18598E)**.

LIN Transceiver circuit Characteristics

DC Characteristics (T_A = –40 to +85°C, 7 V ≤ V_{SUP} ≤ 18 V, 4.85 V ≤ V_{RO} ≤ 5.15 V, I_{RO} ≤ 15 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LIN Bus dominant leak current	$I_{BUS\_PAS\_dom}$	Driver off (V_{TxD} = V_{RO}), V_{BUS} = 0 V, V_{SUP} = 12 V	−1			mA
LIN Bus recessive leak current	$I_{BUS\_PAS\_rec}$	Driver off (V_{TxD} = V_{RO}), 8 V < V_{SUP} < 18 V, 8 V < V_{BUS} <18 V, V_{BUS} ≥ V_{SUP}			20	μA
LIN Bus current 1	$I_{BUS\_NO\_GND}$	GND_{Device} = V_{SUP}, 0 V < V_{BUS} < 18 V, V_{SUP} = 12 V	(−1)		(+1)	mA
LIN Bus current 2	I_{BUS}	V_{SUP_Device} = GND, 0 V < V_{BUS} < 18 V		(1)	(10)	μA
Receive dominant-level input voltage	V_{BUSdom}				0.4 V_{SUP}	V
Receive recessive-level Input voltage	V_{BUSrec}		0.6 V_{SUP}			V
Receive centre-level threshold	V_{BUS_CNT}	(V_{th_dom} + V_{th_rec})/2	0.475 V_{SUP}	0.5 V_{SUP}	0.525 V_{SUP}	V
Receive hysteresis	V_{HYS}				0.175 V_{SUP}	V
LIN dominant-level output voltage 1	$V_{BUSdom\_DRV\_LoSUP}$	V_{SUP} = 7.3V, I_{lin} = 15 mA			1.2	V
LIN dominant-level output voltage 2	$V_{BUSdom\_DRV\_HiSUP}$	V_{SUP} = 18V, I_{lin} = 36 mA			2	V
LIN serial diode drop voltage	$V_{SerDiode}$	V_{TxD} = V_{RO}, I_{lin} = −10 μA	0.4	0.7	1.0	V
LIN pull-up resistance	R_{slave}		20	30	60	kΩ
MSLP high level input voltage	V_{slph}		3.5			V
MSLP low level input voltage	V_{slpL}				1.5	V
MSLP pull-down resistance	R_{mslp}		50		200	kΩ
UMODE high level input voltage	V_{umh}		0.7 V_{RO}			V
UMODE low level input voltage	V_{uml}				0.3 V_{RO}	V
UMODE pull-down resistance	R_{umode}		50		200	kΩ
LIN thermal shutdown	LIN_{th}		(150)			°C
LIN overcurrent limitation	I_{CONST}	LIN pin inflow current limited value	40	80	200	mA

Remark The values in parentheses are based on design for which no outgoing inspection has been performed

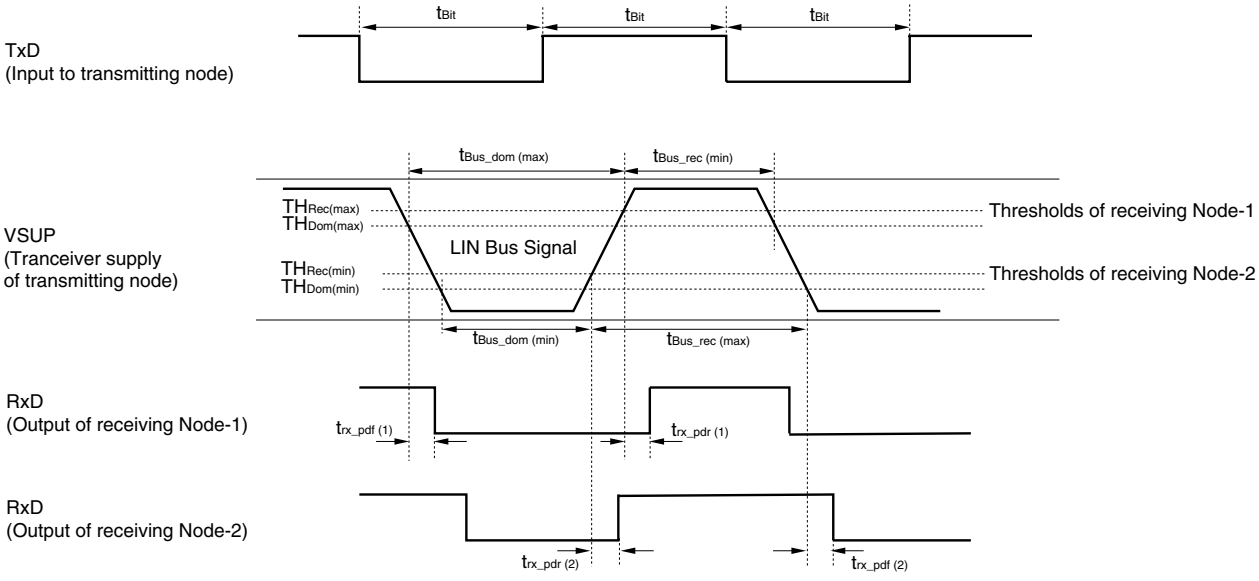
AC Characteristics

(T_A = –40 to +85°C, 7 V ≤ V_{SUP} ≤ 18 V, 4.85 V ≤ V_{RO} ≤ 5.15 V, I_{RO} ≤ 15 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Duty_Cycle1	D1	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 50 μs $TH_{Rec(max)}$ = 0.744×V_{SUP}, $TH_{Dom(max)}$ = 0.581×V_{SUP} D_1 = $t_{BUS\_rec(min)}$/(2×t_{BIT})	0.396			–
Duty_Cycle2	D2	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 50 μs $TH_{Rec(min)}$ = 0.422×V_{SUP}, $TH_{Dom(min)}$ = 0.284×V_{SUP} D_2 = $t_{BUS\_rec(max)}$/(2×t_{BIT}) 7.6 V≤VSUP≤18 V			0.581	–
Duty_Cycle3	D3	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 96 μs $TH_{Rec(max)}$ = 0.778×V_{SUP}, $TH_{Dom(max)}$ = 0.616×V_{SUP} D_3 = $t_{BUS\_rec(min)}$/(2×t_{BIT})	0.417			–
Duty_Cycle4	D4	C_{bus}; R_{bus} = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω t_{BIT} = 96 μs $TH_{Rec(min)}$ = 0.389×V_{SUP}, $TH_{Dom(min)}$ = 0.251×V_{SUP} D_3 = $t_{BUS\_rec(max)}$/(2×t_{BIT}) 7.6 V≤V_{SUP}≤18 V			0.590	–
Propagation delay	t_{rx_pd}	$t_{rx\_pdf\ (1)}$, $t_{rx\_pdf\ (2)}$, $t_{rx\_pdr\ (1)}$, $t_{rx\_pdr\ (2)}$			6	μs
LIN rising and falling transmitter delay symmetry	t_{rx_sym}	t_{rx_sym} = $t_{rx\_pdf\ (1)}$ –$t_{rx\_pdr\ (1)}$, t_{rx_sym} = $t_{rx\_pdf\ (2)}$ –$t_{rx\_pdr\ (2)}$,	–2		+2	μs

Definition of Bus Timing Parameters

Timing diagram:



Driver circuit Characteristics

(T_A = –40 to +85°C, 7 V≤V_{SUP}≤19 V, 4.85 V ≤ V_{RO} ≤ 5.15 V, I_{RO} ≤ 15 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	UNit
Ron	Dr_{1_RON}	I_O = 10 mA, Dr1_I = V_{RO}			100	Ω
	Dr_{2_RON}	I_O = 100 mA, Dr2n_I ≥ 4 V			10	Ω
	Dr_{3_RON}	I_O = 50 mA, Dr3_I = V_{RO}			10	Ω
	Dr_{4_RON}	I_O = 16 mA, 7 V ≤ V_{SUP} ≤ 14 V, Dr4_I = V_{RO}			70	Ω
Dr2 dynamic clamp voltage	CLV1	**Note 1**			32	V
Dr4 output voltage	CLV2	Dr4, I_O = 16 mA			16	V
Dr4 limited current	CLI4	Peak Current when I_O increase	(40)			mA
Dr2 input clamp voltage	CLV3	In ≤ 400 μA	5		8	V
Pull down resistance	$Dr_{\_Rdown}$	Dr1_I, Dr3_I, Dr4_I	50	100	200	kΩ
High level input voltage	V_{IH_Dr1}	Dr1_I, Dr3_I, Dr4_I	0.7 V_{RO}		V_{RO}	V
	V_{IH_Dr2}	Dr2n_I	4		CLV3	V
Low level input voltage	V_{IL_Dr1}	Dr1_I, Dr3_I, Dr4_I	0		0.3 V_{RO}	V
	V_{IL_Dr2}	Dr2n_I, I_O≤2 mA	0		1.5	V
High level input leak current **Note 2**	I_{LIHD1}	Dr1_I, Dr3_I, Dr4_I, V_I = 5 V			105	μA
	I_{LIHD2}	Dr2n_I, V_I = 5 V			300	μA
Low level input leak current	I_{LILD}	Dr1_I, Dr2n_I, Dr3_I, Dr4_I, V_I = 0 V	–3			μA
Output off leak current	I_{OHD1}	Dr1, Dr2n, Dr3, V_O = 19 V			10	μA
	I_{OHD2}	Dr4, V_O = 0 V	–10			μA

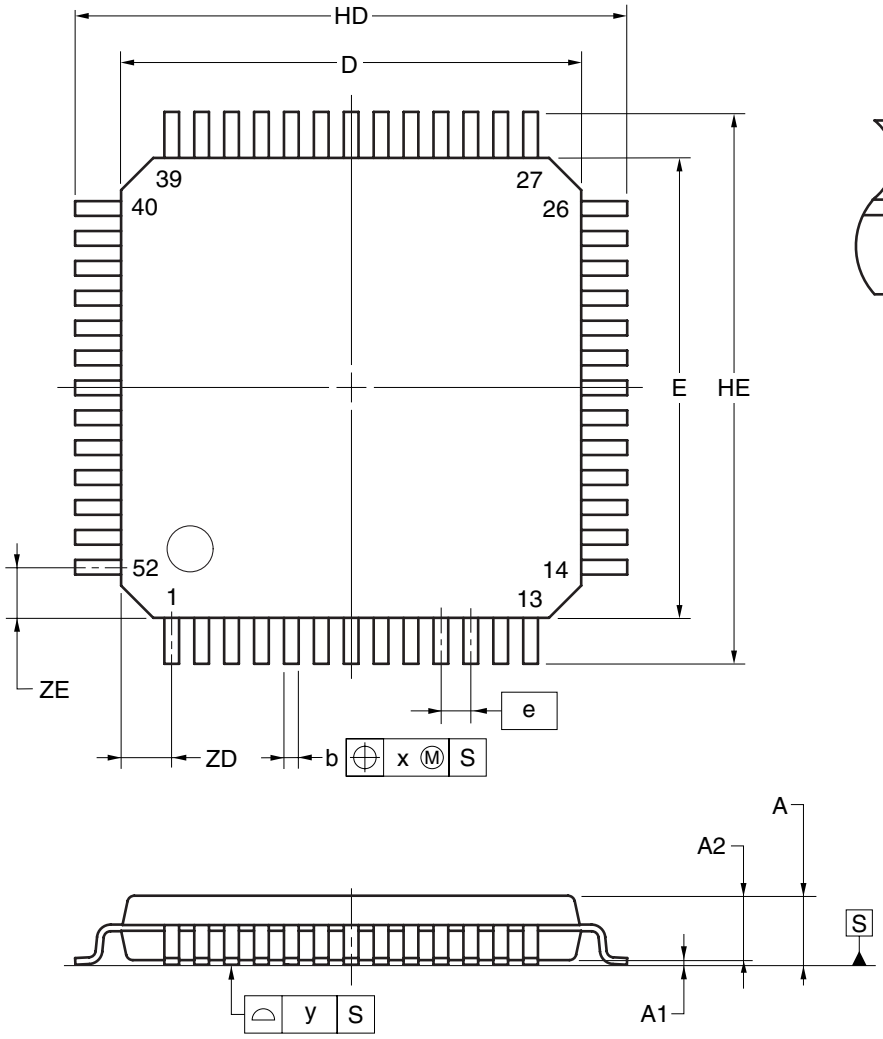
Notes 1. When V_{SUP} is more than 28V, turn on or turn off the operation of Dr21 and Dr22 are prohibited, because the dynamic clamp circuit does not operate under this condition.

2. Including the current flowing into the Pull down resistance.

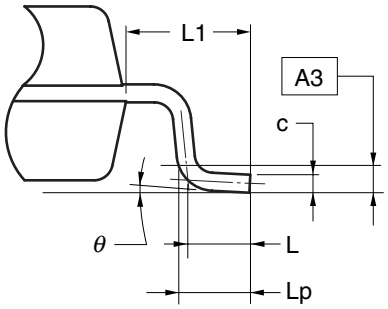
Remarks 1. The values in parentheses are design guaranteed values for which no shipping test has been performed.

2. Dr2n_I: n = 1, 2

52-PIN PLASTIC LQFP (10x10)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.10
ZE	1.10

P52GB-65-GAG

NOTE
Each lead centerline is located within 0.13mm of its true position at maximum material condition.

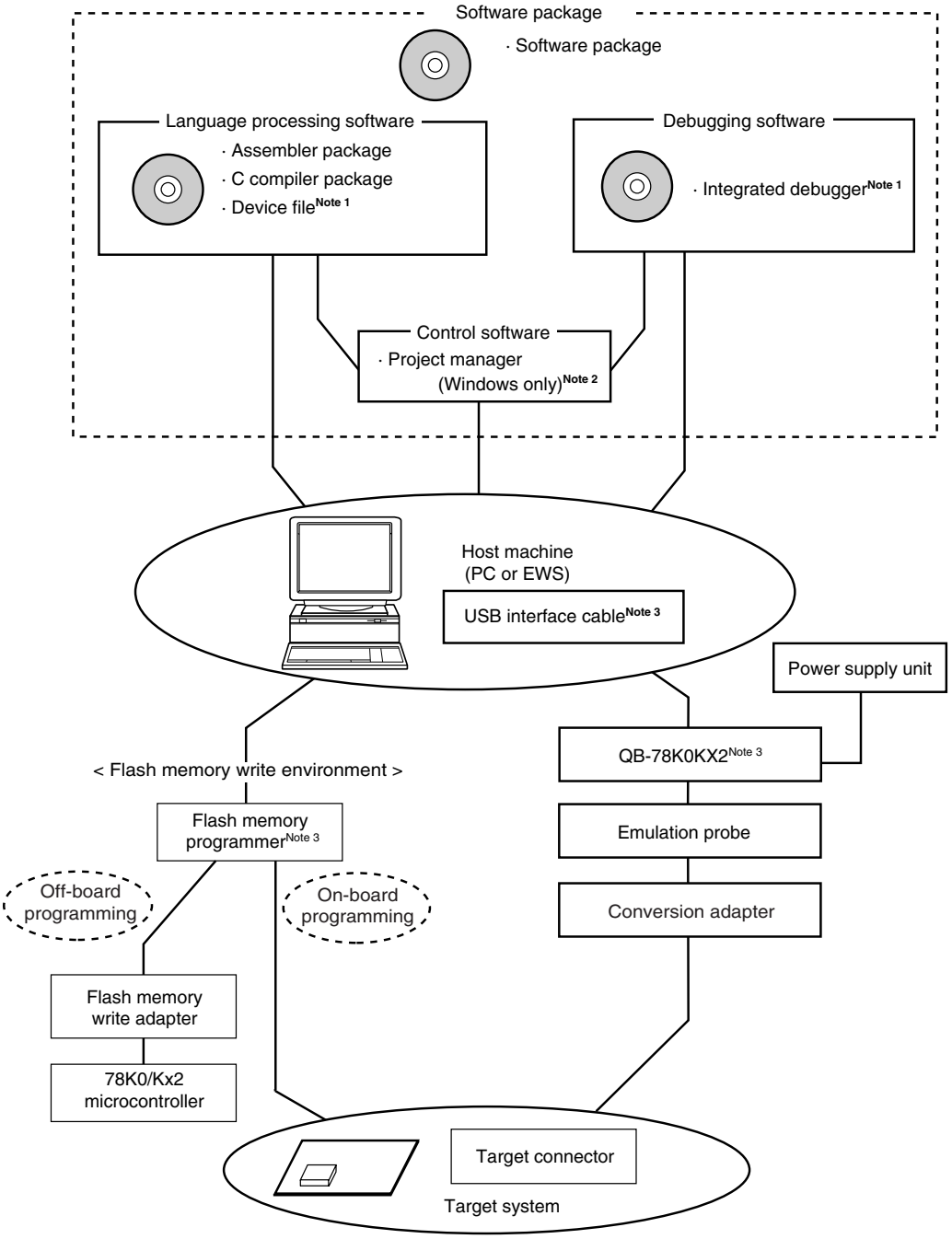
APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the μPD78F8014A, 78F8015A, 78F8016A.

Figure A-1 shows the development tool configuration.

Figure A-1. Development Tool Configuration (1/2)

(1) When using the in-circuit emulator QB-78K0KX2



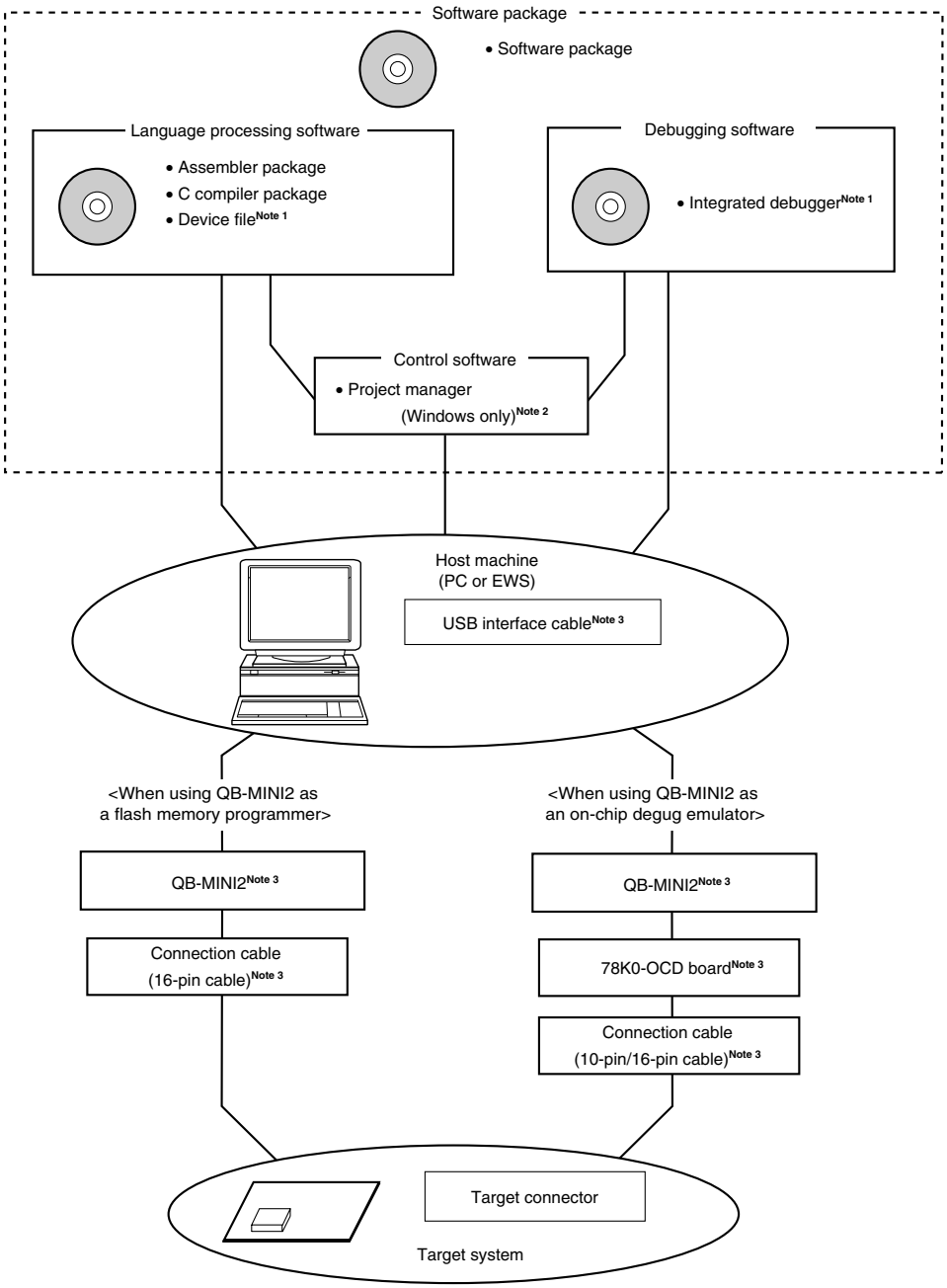
Notes 1. Download the device file for μPD78F8014A, 78F8015A, 78F8016A (DF788016) and the integrated debugger ID78K0-QB from the download site for development tools (http://www.necel.com/micro/en/ods/index.html).

2. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows™.

3. QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator with programming function QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Any other products are sold separately.

Figure A-1. Development Tool Configuration (2/2)

(2) When using the on-chip debug emulator with programming function QB-MINI2



Notes 1. Download the device file for μPD78F8014A, 78F8015A, 78F8016A (DF788016) and the integrated debugger ID78K0-QB from the download site for development tools (http://www.necel.com/micro/en/ods/index.html).

2. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows.

3. QB-MINI2 is supplied with USB interface cable, connection cables (10-pin cable and 16-pin cable), and 78K0-OCD board. Any other products are sold separately. In addition, download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/en/ods/index.html).

A.1 Software Package

SP78K0 78K/0 microcontroller software package	Development tools (software) common to the 78K/0 microcontroller are combined in this package.

A.2 Language Processing Software

RA78K0 Note 1 Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF788016). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
CC78K0 Note 1 C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file. **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
DF788016 Note 2 Device file	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, ID78K0-QB, and the system simulator). The corresponding OS and host machine differ depending on the tool to be used.

Notes 1. If the versions of RA78K0 and CC78K0 are Ver.4.00 or later, different versions of RA78K0 and CC78K0 can be installed on the same machine.

2. The DF788016 can be used in common with the RA78K0, CC78K0, ID78K0-QB, and. and the system simulator. Download the DF788016 from the download site for development tools (http://www.necel.com/micro/en/ods/index.html).

A.3 Flash Memory Writing Tools

A.3.1 When using flash memory programmer FG-FP5, FL-PR5, FG-FP4, and FL-PR4

FG-FP5, FL-PR5, PG-FP4, FL-PR4 [Note] Flash memory programmer	Flash memory programmer dedicated to microcontrollers with on-chip flash memory.
FA-78F8016GB-GAG-MX Flash memory writing adapter	Flash memory programming adapter used connected to the flash memory programmer for use. FA-78F8016GB-GAG-MX: For 52-pin plastic LQFP

Note Phase-out

Remarks 1. FL-PR5, FL-PR4, and FA-78F8016GB-GAG-MX are products of Naito Densei Machida Mfg. Co., Ltd. (http://www.ndk-m.co.jp/, TEL: +81-42-750-4172).

2. Use the latest version of the flash memory programming adapter.

A.3.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This is a flash memory programmer dedicated to microcontrollers with on-chip flash memory. It is available also as on-chip debug emulator which serves to debug hardware and software when developing application systems using the 78K0/Kx2 microcontrollers. When using this as flash memory programmer, it should be used in combination with a connection cable (16-pin cable) and a USB interface cable that is used to connect the host machine.
Target connector specifications	16-pin general-purpose connector (2.54 mm pitch)

Remarks 1. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. A connection cable (10-pin cable) and the 78K0-OCD board are used only when using the on-chip debug function.

2. Download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/en/ods/index.html).

A.4 Debugging Tools (Hardware)

A.4.1 When using in-circuit emulator QB-78K0KX2

QB-78K0KX2 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0/Kx2 microcontrollers. It supports to the integrated debugger (ID78K0-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-80-EP-01T Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-788016-EA-01T, Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector. Exchange adapter has the LIN transceiver, voltage regulator and driver functions.
QB-52GB-YS-01T, Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator. QB-52GB-YS-01T: 52-pin plastic LQFP
QB-52GB-YQ-01T, YQ connector	This YQ connector is used to connect the target connector and exchange adapter. QB-52GB-YQ-01T: 52-pin plastic LQFP
QB-52GB-HQ-01T, Mount adapter	This mount adapter is used to mount the target device with socket. QB-52GB-HQ-01T: 52-pin plastic LQFP
QB-52GB-NQ-01T, Target connector	This target connector is used to mount on the target system. QB-52GB-NQ-01T: 52-pin plastic LQFP

Remark The QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, a power supply unit, the on-chip debug emulator QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board.

Download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/en/ods/index.html) when using the QB-MINI2.

A.4.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This on-chip debug emulator serves to debug hardware and software when developing application systems using the 78K0/Kx2. It is available also as flash memory programmer dedicated to microcontrollers with on-chip flash memory. When using this as on-chip debug emulator, it should be used in combination with a connection cable (10-pin cable or 16-pin cable), a USB interface cable that is used to connect the host machine, and the 78K0-OCD board.
Target connector specifications	10-pin general-purpose connector (2.54 mm pitch) or 16-pin general-purpose connector (2.54 mm pitch)

Remarks 1. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. A connection cable (10-pin cable) and the 78K0-OCD board are used only when using the on-chip debug function.

2. Download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/en/ods/index.html).

A.5 Debugging Tools (Software)

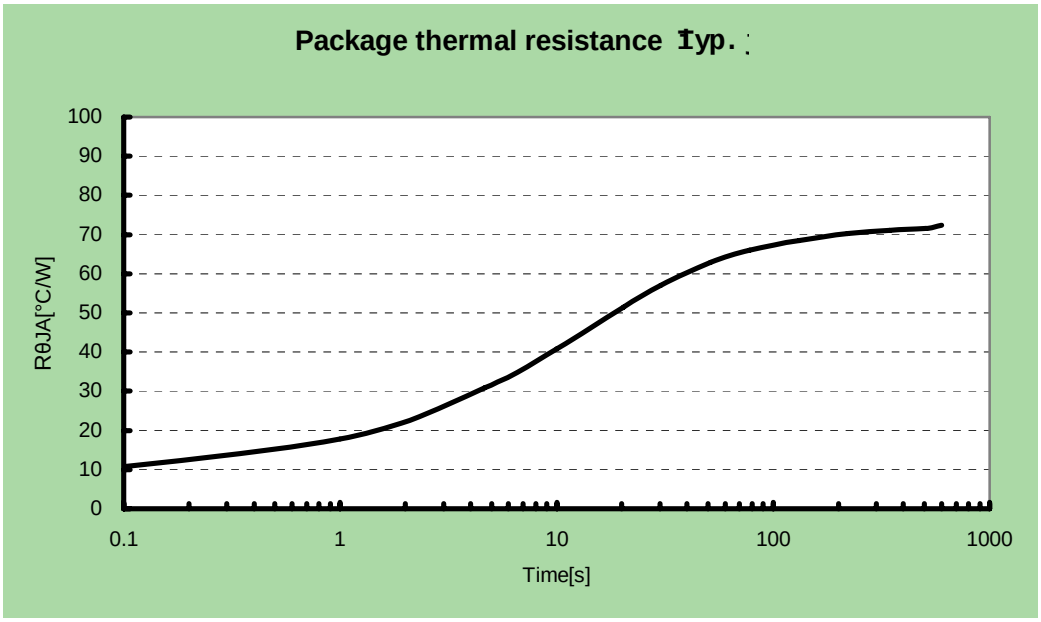
ID78K0-QB[Note] Integrated debugger	This debugger supports the in-circuit emulators for the 78K0 microcontrollers. The ID78K0-QB is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file (DF788016).

Note Download the ID78K0-QB from the download site for development tools (http://www.necel.com/micro/en/ods/index.html).

APPENDIX B PACKAGE THERMAL RESISTANCE

Conditions

Board size : 100 × 100 mm 1.6 mm thickness
Wiring : 2 layers (0.033 mm thickness)
Wiring density : 50%
Material : FR4



APPENDIX C CALCULATION EXAMPLE OF POWER DISSIPATION AND JUNCTION TEMPERATURE

Calculation Example of Total Power Dissipation

Conditions

V_{SUP} = 12V
I_{RO} = 15mA
LIN = Normal mode
T_A = 85°C

$P1 = V_{SUP} \times I_{BAT3}$ = 36 mW
$P2 = (V_{SUP} - V_{RO}) \times I_{RO}$ = 105 mW
$P3 = V_{RO} \times I_{DD}$ = 75 mW

$R_{ON} \times I_O^2$ does the dissipation of one driver.
If only 1 ch is on for Dr2, P4 will be as the following

$P4 = RON \times I^2$
$= Dr1\_R_{ON} \times I_O^2 + Dr2\_R_{ON} \times I_O^2 + Dr3\_R_{ON} \times I_O^2 + Dr4\_R_{ON} \times I_O^2$
= 10 mW + 100 mW + 25 mW + 18 mW
= 153 mW
PD = P1 + P2 + P3 + P4 = 369 mW

Calculation Example of Junction Temperature

$T_j = PD \times R_{\Theta JA}^{Note} + T_A$
= 113°C

Note $R_{\Theta JA}$ uses the value of Package thermal resistance (Appendix B T is more than 400 sec)

Caution Please make sure not to go beyond 140°C.

APPENDIX D REVISION HISTORY

D.1 Main Revisions in this Edition

Page	Description
p.13	Change of Part Number

D.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

(1/2)

Edition	Description	Chapter
2nd	Change of item μPD78F0511, 78F0512, 78F0513→μPD78F0511A, 78F0512A, 78F0513A	Throughout
	Addition of Flash Memory Programmer PG-FP5	
	Change of **To know details of the microcontroller part**	**INTRODUCTION**
	Change of **Documents Related to Devices**	
	Change of **Documents Related to Development Tools (Hardware) (User's Manuals)**	
	Change of **Documents Related to Flash Memory Programming**	
	Change of the explanation in **1.1 Features**	**CHAPTER 1 OUTLINE**
	Change of **1.6 Outline of Functions**	
	Change of **2.3.3 (2) Control mode**	**CHAPTER 2 PIN FUNCTIONS**
	Change of the explanation in **CHAPTER 3 MICROCONTROLLER FUNCTIONS**	**CHAPTER 3 MICROCONTROLLER FUNCTIONS**
	Change of **3.3.2 Port register**	
	Change of the explanation **5.2 Power Supply Overcurrent Protection Function**	**CHAPTER 5 POWER SUPPLY CIRCUIT**
	8.1 Absolute Maximum Ratings Change of **Absolute Maximum Ratings for Microcontroller Block (T_A = 25°C)**	**CHAPTER 8 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS (TARGET)**
	8.2 Microcontroller Block Characteristics Change of **A/D Converter Characteristics** Addition of **Remark** in **2.7 V POC Circuit Characteristics (T_A = • 40 to +85°C, V_{SS} = 0 V)** Change of table and **Note 1**, addition of **Note 4 to 6** in **Flash Memory Programming Characteristics**	
	8.3 Analog Block Characteristics Change of **Voltage regulator circuit characteristics** Change of **Note** in **Supply current Characteristics**	
	Change of **Note 3** in **Figure A-1. Development Tool Configuration (1/3) (1) When using the in-circuit emulator QB-78K0KX2**	**APPENDIX A DEVELOPMENT TOOLS**
	Addition of **Figure A-1. Development Tool Configuration (2/3) (2) When using the on-chip debug emulator QB-78K0MINI**	
	Addition of **Figure A-1. Development Tool Configuration (3/3) (3) When using the on-chip debug emulator with programming function QB-MINI2**	
	Addition of **A.4.1 When using flash memory programmer FG-FP5, FL-PR5, FG-FP4, FL-PR4, PG-FPL3, and FP-LITE3**	

(2/2)

Edition	Description	Chapter
2nd	Addition of **A.4.2 When using on-chip debug emulator with programming function QB-MINI2**	**APPENDIX A DEVELOPMENT TOOLS**
	Change of **Note** in **A.5.1 When using in-circuit emulator QB-78K0KX2**	
	Addition of **A.5.2 When using on-chip debug emulator QB-78K0MINI**	
	Addition of **A.5.3 When using on-chip debug emulator with programming function QB-MINI2**	
	Addition of **APPENDIX D REVISION HISTORY**	**APPENDIX D REVISION HISTORY**
3rd	Deletion of QB-78K0MINI, PG-FPL3, and FP-LITE3 (because of discontinued products)	Throughout
	Change of **How to Read This Manual**	**INTRODUCTION**
	Change of **Related Documents**	
	Change of **1.6 Outline of Functions**	**CHAPTER 1 OUTLINE**
	Change of **Note 2** in **Table 4-1. Wiring Dedicated Flash Programmer**	**CHAPTER 4 WRITING WITH FLASH PROGRAMMER**
	Change of **Absolute Maximum Ratings for Microcontroller block**	**CHAPTER 8 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS**
	Change of **Absolute Maximum Ratings for Common Item**	
	Change of table and Note 2 in **X1 Oscillator Characteristics**	
	Change of **(1) Basic operation** and **Note 3** in **AC Characteristics**	
	Change of **(c) IIC0** in **(2) Serial interface** in **AC Characteristics**	
	Change of **LVI Circuit Characteristics**	
	Change of **Basic characteristics**	
	Change of **Voltage regulator circuit characteristics** and **Supply current Characteristics**	
	Change of **DC Characteristics**	
	Change of **AC Characteristics**	
	Change of **Driver circuit Characteristics**	
	Change of **APPENDIX A DEVELOPMENT TOOLS**	**APPENDIX A DEVELOPMENT TOOLS**
	Addition of **D.2 Revision History of Preceding Editions**	**APPENDIX D REVISION HISTORY**

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