CCE4510 Evaluation Board

1. ABSTACT

The CCE4510 evaluation board is designed to evaluate and demonstrate the CCE4510 IO-Link Master IC with integrated frame handler.

Contents

2. INTRODUCTION

The board is divided into two sections:

- **IO-Link Section**
  The IO-Link section contains two CCE4510 including all necessary periphery to use the two CCE4510 for IO-Link communication.
- **MCU Section**
  The MCU section contains a LPC1549 32-bit ARM Cortex-M3 microcontroller from NXP to control the CCE4510 Master ICs. The MCU is powered by an LDO with 3.3 V output voltage.

For maximum flexibility, the sections can be used separately and independently from each other. This allows to evaluate the CCE4510 Master IC with every suitable MCU.

The evaluation board is compliant to IO-Link Interface and System Specification V1.1.2

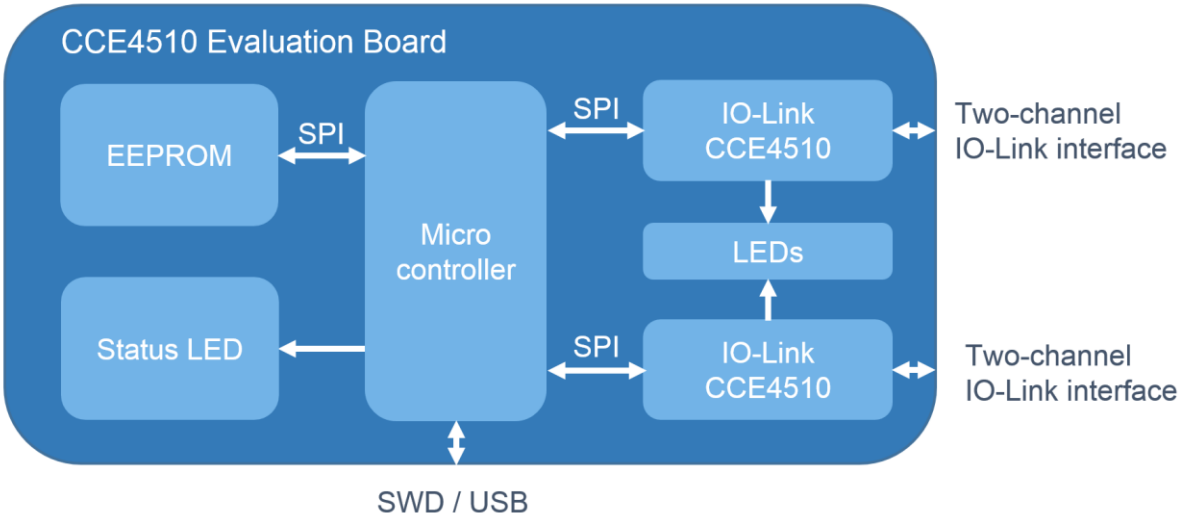

Figure 1: System Diagram

3. SYSTEM REQUIREMENTS

The CCE4510 evaluation board is ready to use with a preinstalled IO-Link master stack.

To get started, the following tools are required:

- Power Supply 24V
- USB Cable (Micro USB type B)
- Debug probe (for programming via SWD)

4. FEATURE OVERVIEW

- ARM Cortex-M3 Microcontroller
- On-Board 3.3 V LDO
- 16 kB EEPROM
- Programmable via USB or Serial Wire Debug (SWD)
- Status LED indicator
- External NMOS gate drivers
- 24 V supply voltage
- Two CCE4510 IO-Link Master Transceiver ICs
- 4 IO-Link channels
- 4 Status LED indicators for IO-Link channels
- Additional on-board protection circuitry
- All pins accessible via pin-headers
  - For microcontroller and IO-Link Master ICs
- Independent use of sections

5. GETTING STARTED

There are two different possibilities to program the CCE4510 evaluation board:

- Programming via USB
- Programming via SWD

To program via USB:

1. Connect pin MAS_INT (JP1 pin 5) to GND
2. Connect USB to PC
3. Power on the Evaluation Board (24V)
4. The microcontroller will now be recognized as USB mass storage
5. Copy any program on the microcontroller

To program via SWD

1. Connect debug probe to SWD connector
2. Connect USB to PC (USB 5V supply is needed) OR Connect USB_VBUS (JP1 pin 3) to +3.3V
3. Power on the Evaluation Board (24V)
4. Start programming with your preferred SDK

6. POWER SUPPLY

The CCE4510 Evaluation Board needs a 24 V power supply connected to JP2 pins 23 / 24. An on-board 3.3 V LDO (placed on the MCU section) supplies the microcontroller as well as the CCE4510 ICs.

When using the IO-Link section independently from the MCU section it must be ensured that both voltages (3.3 V and 24 V) are present at the IO-Link section.

7. SECTIONS OF THE CCE4510 EVALUATION BOARD

The CCE4510 Evaluation Board is divided into two sections.

Both sections can be used in combination with an IO-Link Master software stack to evaluate a fully functional, ready-to-use IO-Link Master.

If required, both sections can also be used independently of each other. The connection between the sections can be disconnected by cutting them open between the cutting marks (see Figure 2). Make sure not to break the evaluation board in this process.

To reestablish the connections, pin-headers with 2.54 mm pitch can be used.

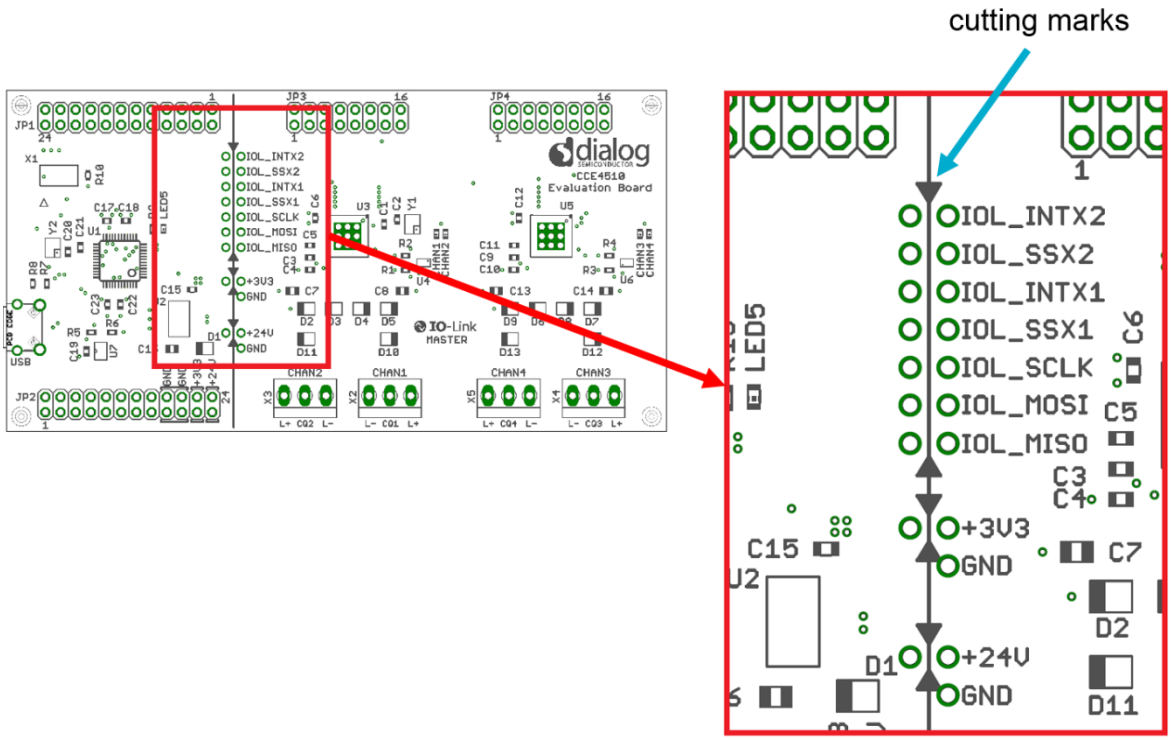

Figure 2: Cutting Marks

IO-Link Section

The IO-Link section contains two CCE4510 IO-Link master ICs, external NMOS gate drivers (U4, U6), four LED indicators for channel activities and protection circuitry. Each IO-Link channel (L+, CQ, L-) can be accessed via a terminal block (X2, X3, X4, X5). For maximum accessibility to the CCE4510 IO-Link Master ICs, all relevant pins of the CCE4510 ICs are connected to pin-headers JP3 and JP4.

MCU Section

The MCU section contains an ARM Cortex-M3 processor from NXP (LPC1549), a 3.3 V LDO (U2) for power supply, a 16 kB EEPROM (U7) and a status LED (LED5). The microcontroller can be programmed via USB (mass storage device) or via SWD. For maximum accessibility of the LPC1549, all relevant pins are connected to pin-headers JP1 and JP2.

8. SCHEMATIC AND LAYOUT

Connectors

Figure 3 shows all connectors of the CCE4510 Evaluation Board. It is possible to access all pins of the MCU and the CCE4510 master ICs through these connectors.

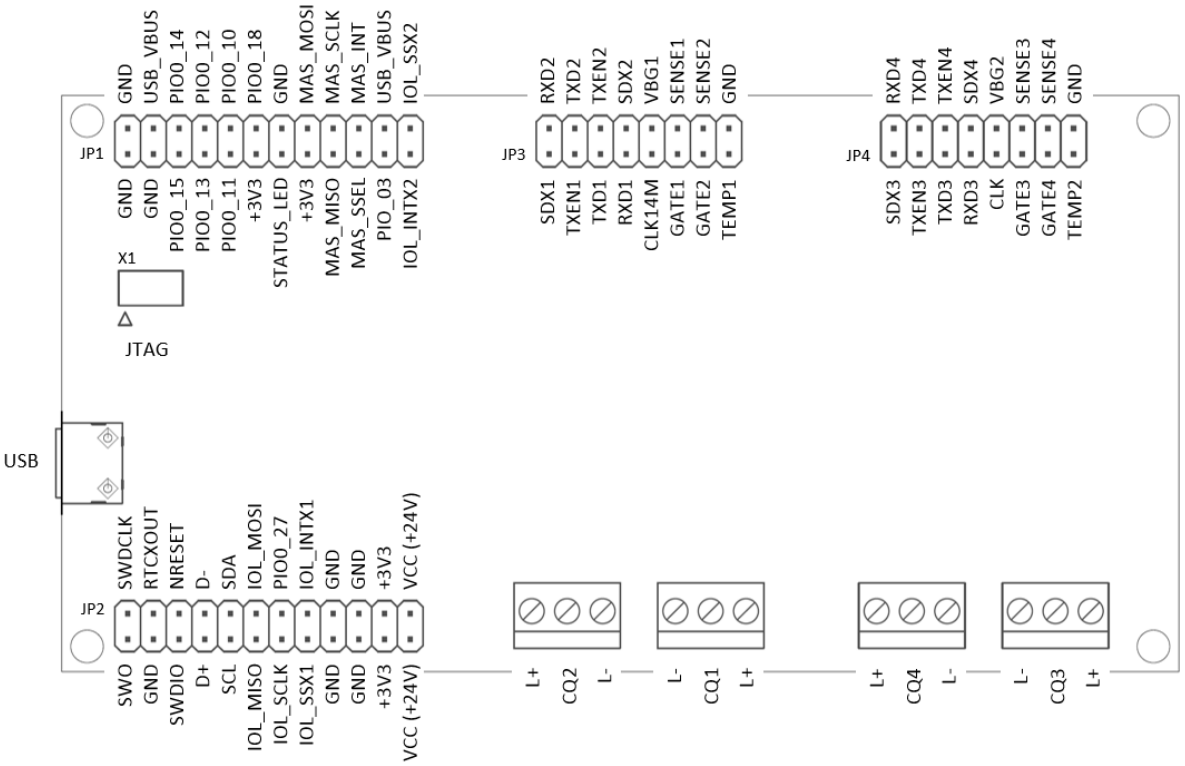

Figure 3: Connectors

Schematic

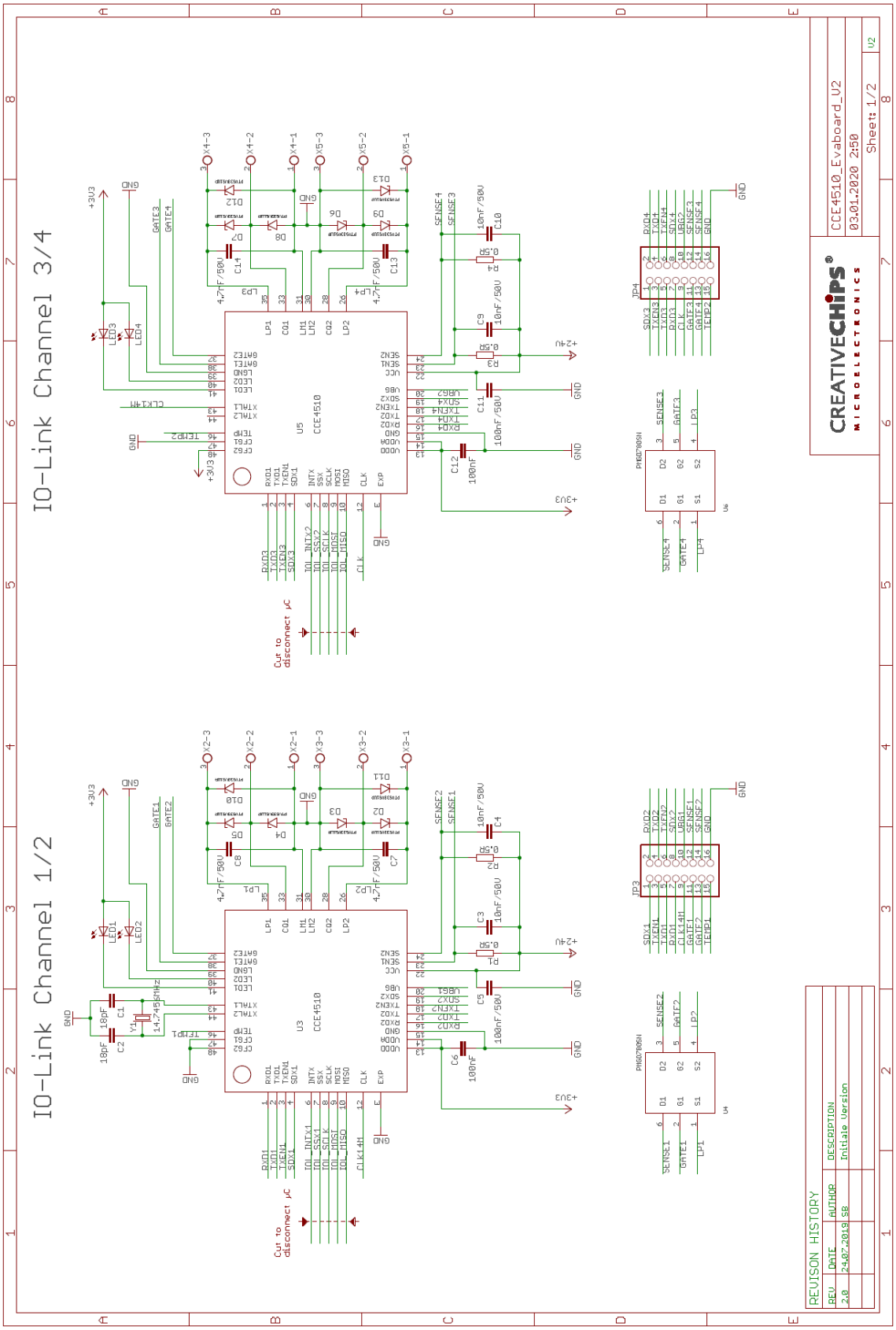

Figure 4: Schematic 1

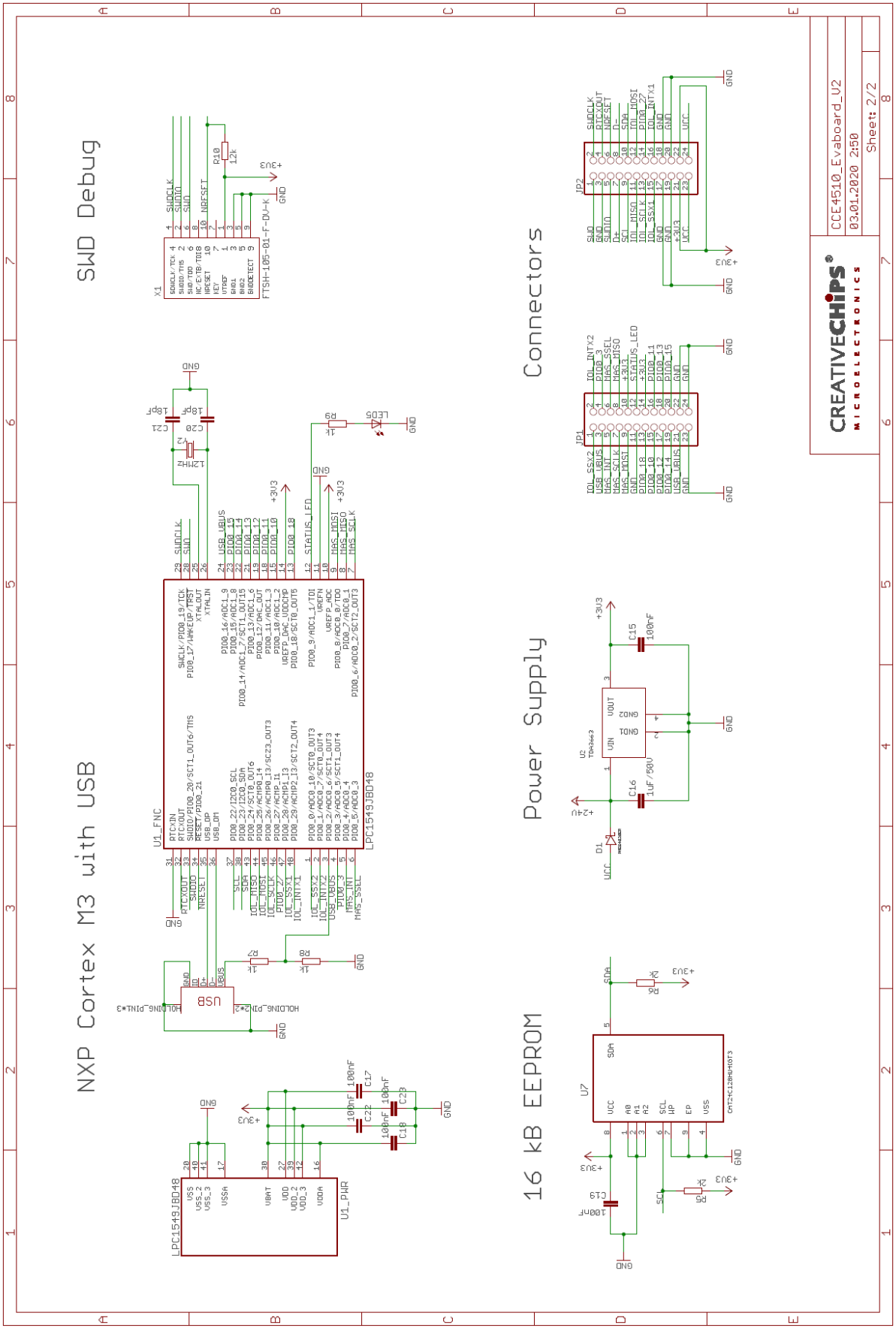

Figure 5: Schematic 2

Layout

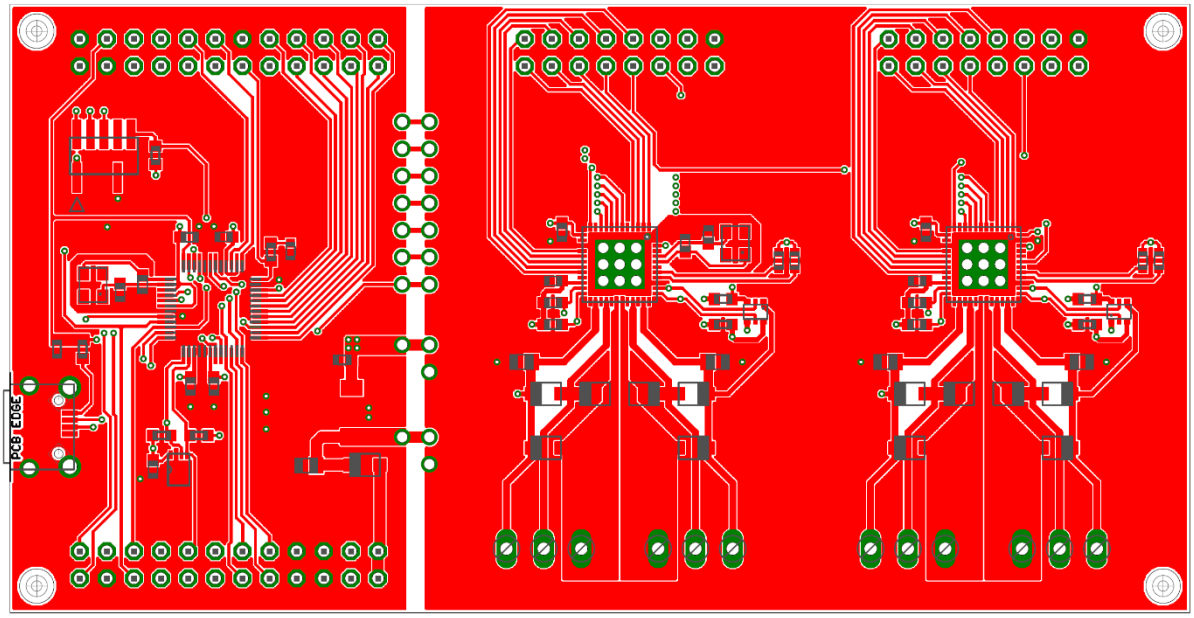

Figure 6: Layout TOP

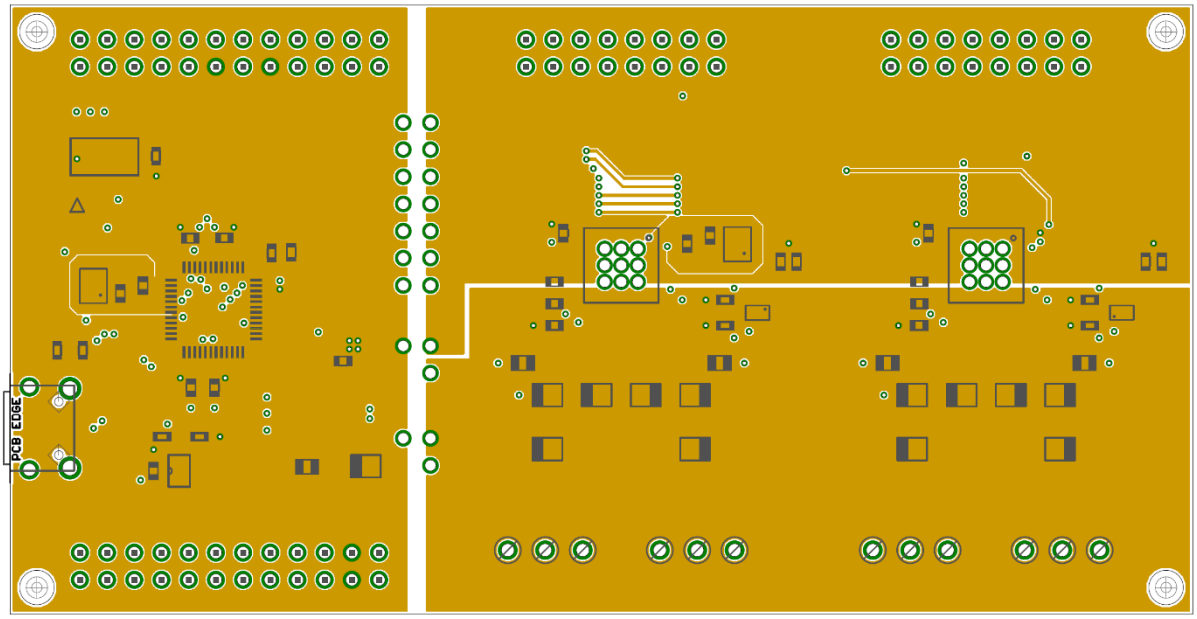

Figure 7: Layout MID1 (Supply)

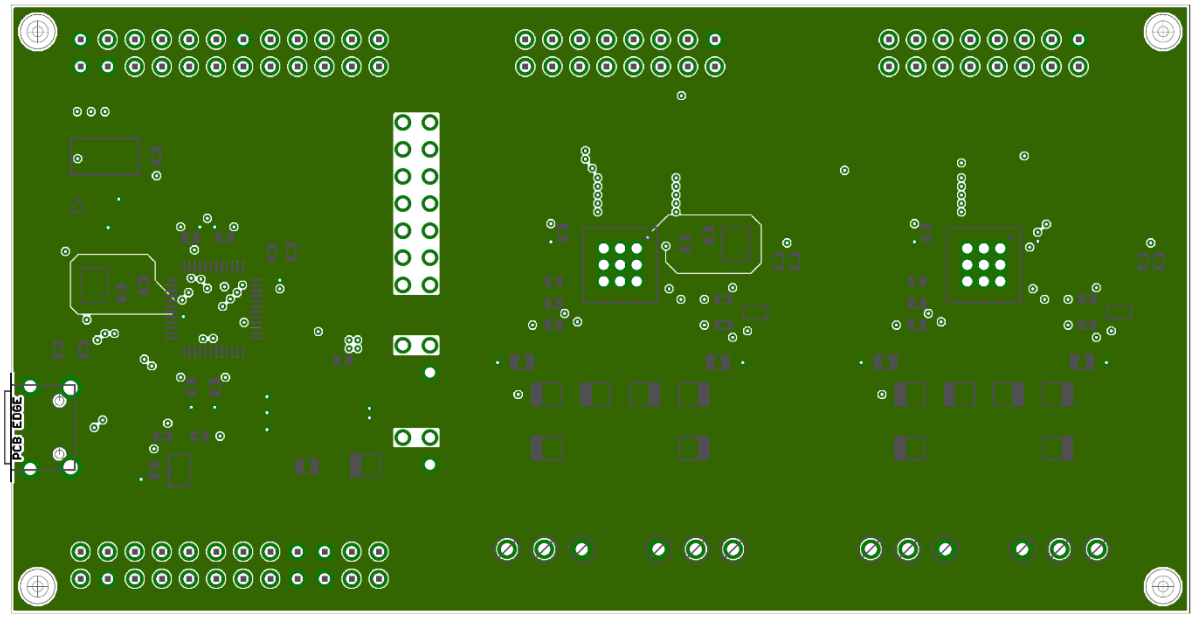

Figure 8: Layout MID2 (GND)

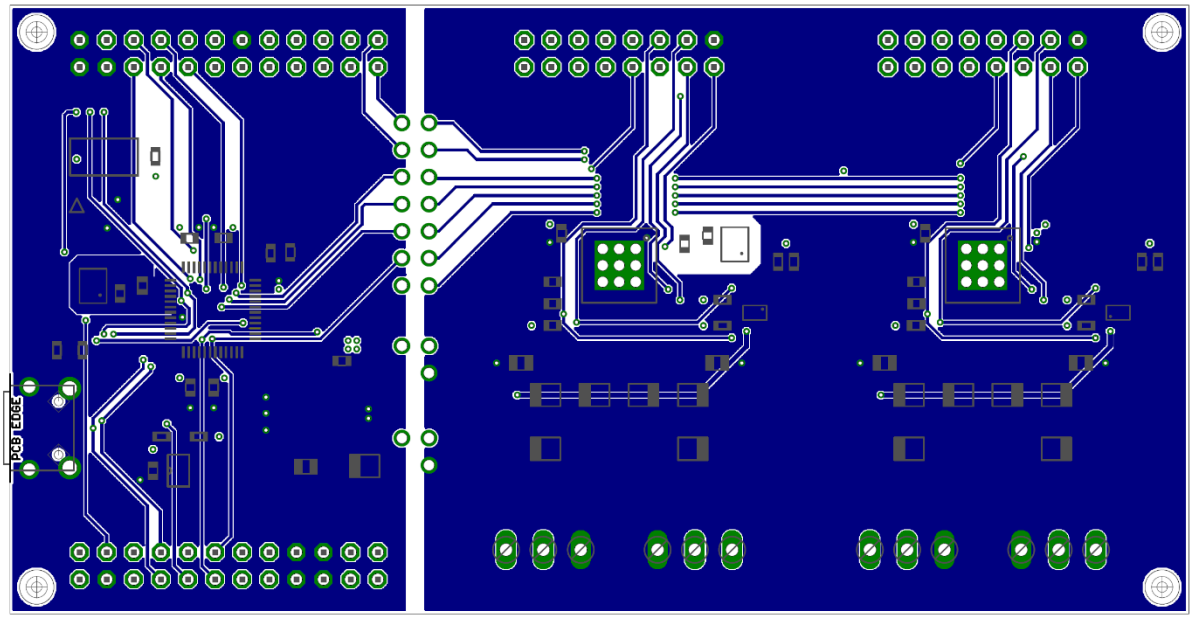

Figure 9: Layout BOTTOM

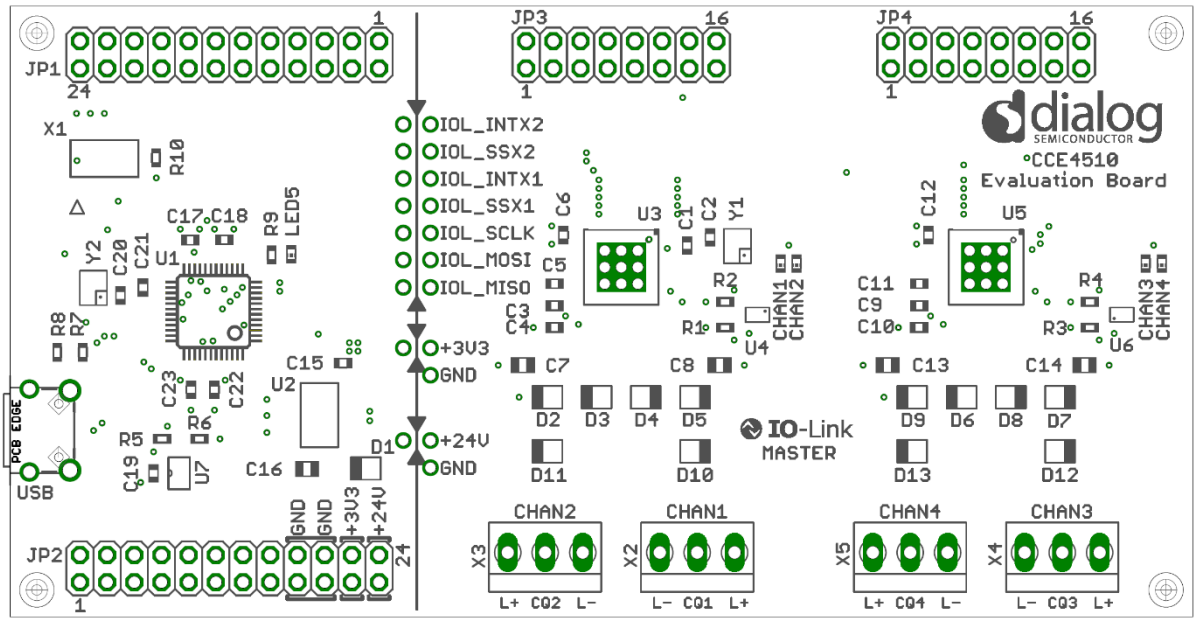

Figure 10: Layout Assembly

9. BILL OF MATERIALS

Part	Value / Description	Manufacturer	Manufacturer Part Number
C1,C2,C20,C21	18 pF 50V C0G 5 % 0603	Any	Any
C3,C4,C9,C10	10 nF 50V X7R 10 % 0603	Any	Any
C5,C6,C11,C12, C15,C17,C18,C19, C22,C23	100 nF 50V X7R 10 % 0603	Any	Any
C7,C8,C13,C14	4.7 nF 50V X7R 10 % 0805	Any	Any
C16	1 µF 50V X5R 10 % 0603	Any	Any
D1	Shottky-Diode 40V 2A	NXP	PMEG4020ER,115
D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13	TVS-Diode 33V	NXP	PTVS33VS1UR,115
JP1,JP2	Pin Header 24-Pin 2.54 mm	Any	Any
JP3,JP4	Pin Header 16-Pin 2.54 mm	Any	Any
LED1, LED2,LED3, LED4	LED Orange	OSRAM Opto Semiconductors Inc.	LO L29K-H2L1-24-Z
LED5	LED Green	OSRAM Opto Semiconductors Inc.	LG L29K-F2J1-24-Z
R1,R2,R3,R4	0.5R 100V 100 mW 1 % 0603	Any	Any
R5,R6	2 k 75 V 100 mW 1 % 0603	Any	Any
R7,R8,R9	1 k 75 V 100 mW 1 % 0603	Any	Any
R10	12 k 75 V 100 mW 1 % 0603	Any	Any
U1	Microcontroller LPC1549	NXP	LPC1549JBD48QL
U2	LDO TDA3663 3.3 V SOT223-1	NXP	TDA3663/N1,135
U3,U5	IO-Link Master Transceiver	Dialog Semiconductor	CCE4510_QFN48
U4,U6	Dual-MOSFET n-channel 60 V	NXP	PMGD780SN
U7	EEPROM 16 kB I^2C	ON Semiconductor	CAT24C128HU4IGT3
USB	Micro USB-B Connector	WURTH Elektronik	629105150521
X1	SMT Micro Header	SAMTEC	FTSH-105-01-F-DV-K
X2,X3,X4,X5	Wire-to-Board Connector	METZ CONNECT	31059103
Y1	Crystal 14.7456 MHz	ABRACON	ABM8G-14.7456MHZ-18-D2Y-T
Y2	Crystal 12 MHz	ABRACON	ABM8G-12.000MHZ-18-D2Y-T

10. REVISION HISTORY

Revision	Date	Description
1	03-Mar-2020	Initial version.
2	28-Jan-2022	Rebrand

11. REFERENCES

[1] CCE4510, Datasheet, Dialog Semiconductor.
[2] LPC1549JBD48QL, Datasheet, NXP.
[3] IO-Link Interface and System Specification V1.1.2, IO-Link Community.

12. STATUS DEFINITIONS

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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