SuperH™ RISC engine Simulator/Debugger V.9.10.00

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Supplementary Information for User's Manual

Introduction

This document describes how V.9.10.00 of the SuperH™ RISC engine Simulator/Debugger differs from V.9.07.00, V.9.08.00, and V.9.09.00. Before using the simulator/debugger, carefully read this document, the SuperH™ RISC engine Simulator/Debugger User's Manual, and the online help for the SuperH™ RISC engine Simulator/Debugger.

Contents

1. New Features in V.9.08.00

1.1 Support for the Enhanced SH-4A Series MPUs

Enhanced MPUs have been added to the SH-4A series. The target names for the enhanced MPUs are "SH4AL-DSP (SH-X2) Simulator" and "SH-4A (SH-X2) Simulator". Both targets support pipeline and instruction-unit simulation.

1.1.1 Range of Simulation

The simulator/debugger for the enhanced SH-4A MPUs support the following CPU functions.

Table 1.1 CPU Functions Supported by the Simulator/Debugger for the Enhanced SH-4A MPUs

Names of Debugging Platforms	Endian	MMU	Cache	Control Register	BSC	DMAC	Timer
SH-4A (SH-X2)	○	○	○	○	—	—	△
SH4AL-DSP (SH-X2)	○	○	○	○	—	—	△

[Note] ○: Supported
—: Not supported
△: Partly supported

Differences in the simulator/debugger operation compared to that for the other SH-4A series MPUs are given in the following sections.

1.1.2 Type of Simulation and Endian

The type of simulation and endian can be selected on the [CPU Configuration] tabbed page of the [Set Simulator] dialog box that appears when the simulator/debugger is started up.

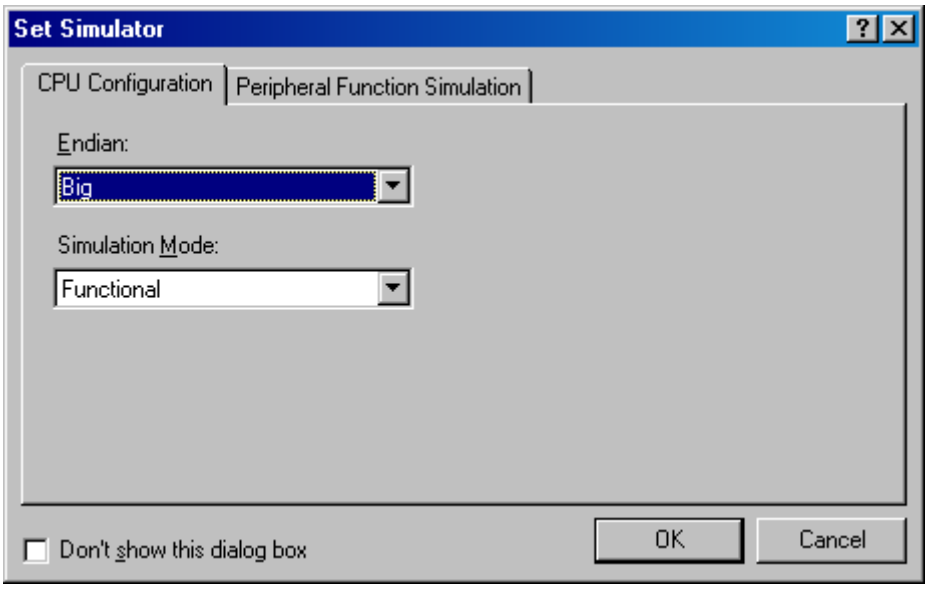

Figure 1.1 [Set Simulator] Dialog Box ([CPU Configuration] Page)

The following items are selectable on the [CPU Configuration] page.

[Endian] Endian for the CPU.
- [Big]: Big endian
- [Little]: Little endian

[Simulation Mode] Simulation mode.
- [Functional]: Instruction-unit simulation
- [Cycle Base]: Pipeline simulation

1.1.3 Cache

The cache capacity specifiable in the [Cache Capacity] dialog box is 8, 16, 32, or 64 Kbytes.

For details on cache, see sections 2.8, Cache, and 3.12, Viewing the Cache Contents, in the SuperH™ RISC engine Simulator/Debugger User's Manual.

1.1.4 Memory Management Unit (MMU)

The page size and protection key are shown as 4- and 6-bit data, respectively, in the [TLB] window.

For details on the MMU, see sections 2.7, Memory Management Unit (MMU), and 3.11, Viewing the TLB Contents, in the SuperH™ RISC engine Simulator/Debugger User's Manual.

1.2 Simulating Peripheral Functions

1.2.1 Settings for Simulation of Peripheral Functions

Settings for simulation of peripheral functions can be made on the [Peripheral Function Simulation] tabbed page of the [Set Simulator] dialog box.

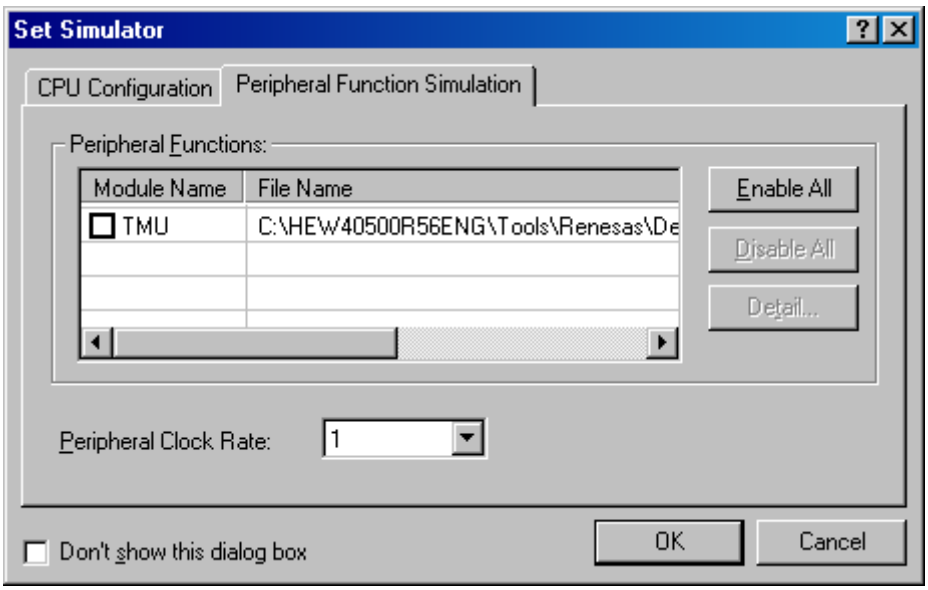

Figure 1.2 [Set Simulator] Dialog Box ([Peripheral Function Simulation] Page)

For details on simulation of peripheral functions, see section 3.3, Simulating Peripheral Functions, in the SuperH™ RISC engine Simulator/Debugger User's Manual.

1.3 Memory Mapping

The specification of memory mapping for the SH-2A was changed. This section describes the new specification of memory mapping.

1.3.1 Modifying the Memory Map and Memory Resource Settings

The [Memory] tabbed page in the [Simulator System] dialog box is used to set and modify the memory map and memory resource settings.

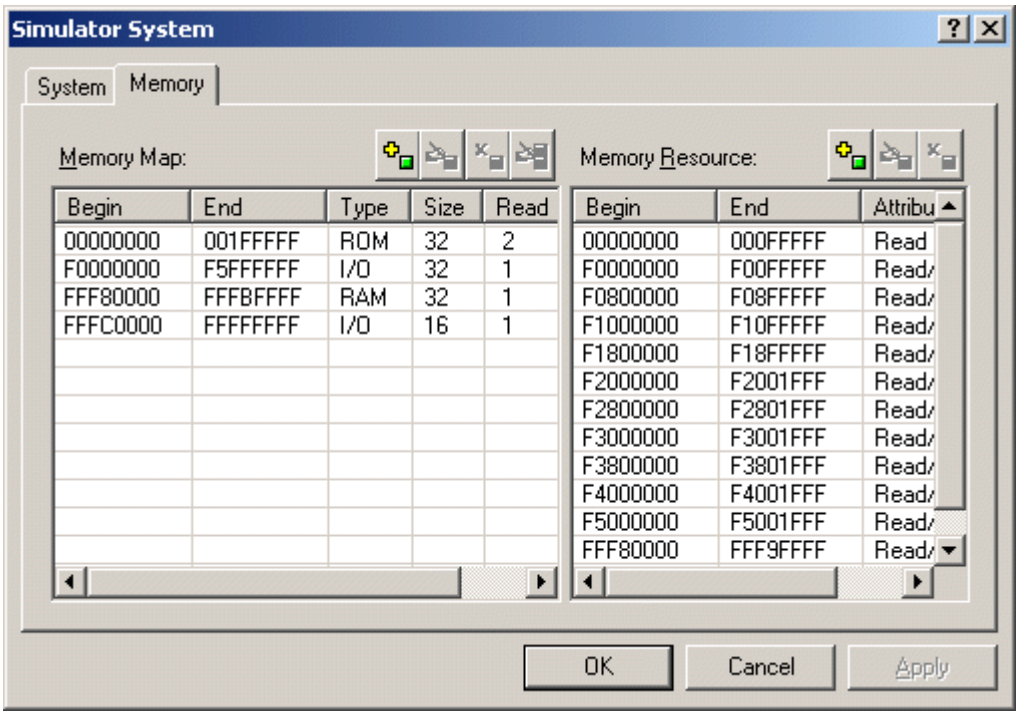

Figure 1.3 [Simulator System] Dialog Box ([Memory] Page)

The following items can be specified in this dialog box.

[Memory Map] Displays the types of memory, addresses where each starts and ends, data bus width, and number of access cycles.

[Memory Resource] Displays the access type and start and end addresses of the current memory resource.

The following buttons are used to alter [Memory Map] (add, modify, or delete entries).

Add items to [Memory Map]. Clicking on this button opens the [Set Memory Map] dialog box (figure 1.4), in which an item can be added to the map.

Modify an item in [Memory Map]. Select the item to be modified in the list box and click on this button. This opens the [Set Memory Map] dialog box (figure 1.4), in which the selected memory map item can be modified.

Delete an item from [Memory Map]. Select the item to be deleted in the list box and click on this button.

In [Memory Map], the start address, end address, memory type, data bus width, number of cycles for reading, and number of cycles for writing are displayed, in that order. The memory types are as follows:

- SH2A-FPU

ROM (internal ROM), RAM (internal RAM), EXT (external memory), I/O (internal I/O), EEPROM

- SH4A

LRAM (internal RAM), EXT (external memory), I/O (internal I/O), ILRAM (internal RAM: enhanced version only)

- SH4AL-DSP

XRAM (internal XRAM), YRAM (internal YRAM), URAM (user RAM), EXT (external memory), I/O (internal I/O), ILRAM (internal RAM: enhanced version only)

Click on the [OK] or [Apply] button to store the modified settings. Click on the [Cancel] button to close this dialog box without modifying the settings.

1.3.2 [Set Memory Map] Dialog Box

The [Set Memory Map] dialog box specifies the memory map of the target CPU. The contents of this dialog box depend on the target CPU. The simulator/debugger uses the data specified in this box to calculate numbers of cycles for memory access.

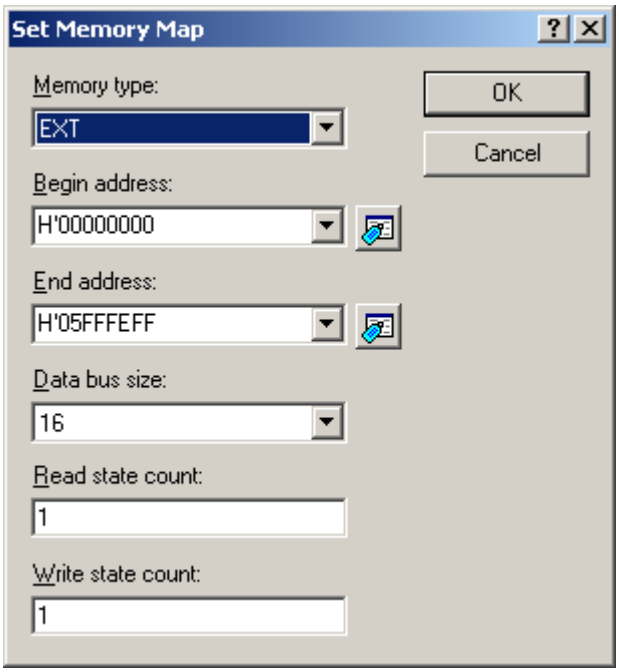

Figure 1.4 [Set Memory Map] Dialog Box

The following items are specified:

[Memory type]	Memory type
[Begin address]	Address where the area of the given type starts.
[End address]	Address where the area of the given type ends.
[Data bus size]	Memory data bus width
[Read state count]	When the memory type is ROM: Latency When the memory type is not ROM: Number of cycles ("states") for read access to the specified type of memory

[Write state count] When the memory type is ROM: Throughput

When the memory type is not ROM: Number of cycles ("states") for write access to the specified type of memory

Notes: 1. In terms of the memory resources of the SH2A-FPU, note the following.

- In the memory areas that are fixed as ROM or RAM, selection of another memory type or allocation in two or more ranges is not possible. The memory areas that are fixed as ROM and RAM are given below.

Area	Address Range	Remark
ROM	0x00000000 - 0x01FFFFFF	When the internal ROM has been enabled
RAM	0xFFF80000 - 0xFFFBFFFF	

- No addresses in reserved areas can be specified. The reserved areas are given below.

Area	Address Range	Remark
Reserved	0x20000000 - 0x21FFFFFF	When the internal ROM has been enabled
	0x84000000 - 0xE7FFFFFF	

- Memory can only be allocated on 8-kbyte boundaries. If memory is allocated to an address range that does not have 8-kbyte boundaries, the boundaries will be adjusted to 8-kbyte boundaries that encompass the specified range.
- Numbers of cycles for access to the areas fixed as ROM and RAM are as follows.

Area	Number of Cycles for Reading (Latency)	Number of Cycles for Writing (Throughput)
ROM	1 to 4	
RAM	1 or 2	1 to 4

2. The memory map setting for area that is allocated to a system memory resource cannot be deleted or modified. Start by deleting the system memory-resource allocation on the [Memory] tab of the [Simulator System] dialog box, then delete or modify the memory map setting.

Clicking on the [OK] button stores the modified settings. Clicking on the [Cancel] button closes the dialog box without modifying the settings.

1.3.3 [Set Memory Resource] Dialog Box

The [Set Memory Resource] dialog box is used to set and modify memory resources.

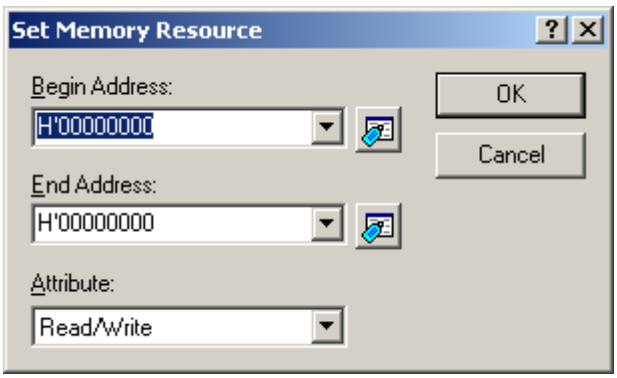

Figure 1.5 [Set Memory Resource] Dialog Box

The following items are specified:

[Begin Address] Address where the memory area to be allocated starts

[End Address] Address where the memory area to be allocated ends

[Attribute] Access type

[Read]	Read only
[Write]	Write only
[Read/Write]	Readable/writable

Click on the [OK] button after specifying [Begin Address], [End Address], and [Attribute]. Click on the [Cancel] button to close the dialog box without modifying the settings.

Notes: 1. When a memory resource is set, memory in the host computer will be used. If the user allocates excessive memory resources, operation of the host computer will be extremely slow.

2. The following notes apply to memory resources for the SH2A-FPU series.
   - Memory resources can only be allocated on 8-kbyte boundaries. If a memory resource is allocated to an address range that does not have 8-kbyte boundaries, the boundaries will be adjusted to 8-kbyte boundaries that encompass the specified range. Accordingly, address ranges of attributes are allocated on 8-kbyte boundaries. When a memory resource does not take up a full 8-kbyte range, the memory that is actually used must be within the range defined in the hardware manual.
   - Do not clear the default allocation of a memory resource as I/O area. If such an allocation is cleared, operation of the cache memory will be incorrect.

1.4 Profile

The specification of the profiler function for the SH-2A was changed. This section describes the new specification of the profiler function.

1.4.1 Types and Purposes of the Profile Data Displayed by the Profiler Function

The profile data to be displayed depends on the CPU. In the case of the SH2A-FPU, the profile data consists of the items listed below.

(a) When the internal ROM has been disabled:
[Cycle] (the number of cycles for execution),
[ICache miss] (the number of instruction cache misses),
[OCache miss] (the number of operand cache misses),
[Ext_mem] (the number of times external memory was accessed),
[I/O_area] (the number of times internal I/O area was accessed),
[Int_mem] (the number of times internal memory was accessed)

(b) When the internal ROM has been enabled:
[Cycle] (the number of cycles for execution),
[ROM ICache miss] (the number of instruction ROM cache misses),
[ROM OCache miss] (the number of operand ROM cache misses),
[Ext_mem] (the number of times external memory was accessed),
[I/O_area] (the number of times internal I/O area was accessed),
[Int_mem] (the number of times internal memory was accessed)

1.5 Windows

Table 1.2 lists the windows that have been added. For details on these windows, refer to the online help for the SuperH™ RISC engine Simulator/Debugger.

Table 1.2 New Windows

Window Name	Description
OS Object	Shows the states of OS objects such as tasks and semaphores.
Task Trace	Shows the history of task execution in a program that uses a real time OS.
Task Analyze	Shows the current CPU occupancy.

1.6 Command Line

Table 1.3 lists the commands that have been added. For details on the command syntax, refer to the online help for the SuperH™ RISC engine Simulator/Debugger.

Table 1.3 New Commands

Command	Abbreviation	Description
OSOBJECT_ALL_ADD	OAA	Adds OS objects (of a specific object type)
OSOBJECT_ALL_DELETE	OAD	Deletes OS objects (in a specific sheet)
OSOBJECT_AUTO_UPDATE	OAU	Changes the automatic-update setting to "Auto" and "Break".
OSOBJECT_DATA_LOWLINE	ODU	Moves an OS object to the next line.
OSOBJECT_DATA_SAVE	ODS	Saves the information on an OS object to a file.
OSOBJECT_DATA_UPLINE	ODL	Moves an OS object to the previous line.
OSOBJECT_DISPLAY	OD	Shows the information on an OS object.
OSOBJECT_NO_UPDATE	ONU	Changes the automatic-update setting to "Lock".
OSOBJECT_ONE_ADD	OOA	Adds an OS object.
OSOBJECT_ONE_DELETE	OOD	Deletes an OS object.
OSOBJECT_ONE_EDIT	OOE	Edits an OS object.
OSOBJECT_SETTING_LOAD	OSL	Loads OS-object settings from a file.
OSOBJECT_SETTING_SAVE	OSS	Saves OS-object settings in a file.
OSOBJECT_STOP_UPDATE	OSU	Changes the automatic-update setting to "Break".

1.7 Messages

1.7.1 Error Messages

Table 1.4 lists the error messages that have been added or modified.

Table 1.4 New or Modified Error Messages

Message	Description
Incorrect memory type. The specified address range includes an area fixed as rr. (Area fixed as rr: 0xmmmmmmmm - 0xnnnnnnnn)	An attempt was made to assign another memory type to an area fixed as ROM or RAM. rr: ROM or RAM 0xmmmmmmmm: Address where the fixed area starts 0xnnnnnnnn: Address where the fixed area ends
Allocating two or more ranges in an area fixed as rr is not possible. (Area fixed as rr: 0xmmmmmmmm - 0xnnnnnnnn)	An attempt was made to allocate two or more ranges in an area fixed as ROM or RAM. rr: ROM or RAM 0xmmmmmmmm: Address where the fixed area starts 0xnnnnnnnn: Address where the fixed area ends
Incorrect address. The specified address range includes a reserved area. (Reserved area: 0xmmmmmmmm - 0xnnnnnnnn)	An attempt was made to map memory to a reserved area. 0xmmmmmmmm: Address where the reserved area starts 0xnnnnnnnn: Address where the reserved area ends
I/O area does not exist. (I/O area: 0xF0000000 - 0xF5FFFFFF)	No memory has been mapped as the I/O area.
Incorrect address. The specified address range is outside an area fixed as rr. (Area fixed as rr: 0xmmmmmmmm - 0xnnnnnnnn)	An attempt was made to map memory beyond the boundaries of an area fixed as ROM or RAM. rr: ROM or RAM 0xmmmmmmmm: Address where the fixed area starts 0xnnnnnnnn: Address where the fixed area ends

2. New Features in V.9.09.00

2.1 Simulating Peripheral Functions

2.1.1 Simulation of Timer Modules

V.9.09.00 of the simulator/debugger has additional channels for simulation of timer modules in the SH-2A and SH-4A.

Table 2.1 Simulation of Timer Modules

	SH-2A	SH-4A
Timer	CMT	TMU
Number of channels	2 (channel 1 added)	6 (channels 1, 2, 4, and 5 added)
Counter	16-bit counter	Auto-reload 32-bit counter
Counter input clock	Four types of internal clock (Pϕ/8, Pϕ/32, Pϕ/128, and Pϕ/512) are selectable.	• Five types of internal clock (Pϕ/4, Pϕ/16, Pϕ/64, Pϕ/256, and Pϕ/1024) are selectable. • External clock and output clock from the on-chip RTC are not supported.
Input capture	—	Not supported (channel 2)
Interrupts	• Compare match interrupts are supported (both channels). • Interrupts as a trigger of a DMA transfer are not supported.	• Underflow interrupts are supported (all channels). • Input-capture interrupts are not supported (channel 2).

Table 2.2 lists the timer control registers in the CMT and TMU supported by the simulator/debugger.

Table 2.2 Timer Control Registers

Debugging Platform	Timer	Control Register	Support
SH-2A	CMT	CMSTR	○
		CMCSR0	○
		CMCNT0	○
		CMCOR0	○
		CMCSR1	○
		CMCNT1	○
		CMCOR1	○
SH-4A	TMU	TOCR	—
		TSTR0	○
		TCOR0	○
		TCNT0	○
		TCR0	△
		TCOR1	○
		TCNT1	○
		TCR1	△
		TCOR2	○
		TCNT2	○
		TCR2	△
		TCPR2	—
		TSTR1	○
		TCOR3	○
		TCNT3	○
		TCR3	△
		TCOR4	○
		TCNT4	○
		TCR4	△
		TCOR5	○
		TCNT5	○
		TCR5	△

Note: ○: Supported
△: Partly supported (only for the bits associated with the functions given in table 2.1)
—: Not supported (only memory resources have been allocated)

2.2 Windows

Table 2.3 shows a window that has been modified. For details on these windows, refer to the online help for the SuperH™ RISC engine Simulator/Debugger.

Table 2.3 Modified Window

Window Name	Description
Memory	Modified to support the automatic update function.

3. New Features in V.9.10.00

3.1 Starting up the Simulator/Debugger

V.9.10.00 of the simulator/debugger can be connected or disconnected via the [Debug] menu or by clicking on a toolbar button. This section describes how to connect or disconnect the simulator/debugger in that way.

You can connect to the simulator/debugger by selecting a session file in which simulator/debugger settings have already been defined. When you have selected targets in the process of creating a project, the number of session files is the same as the number of selected targets. Select the session file that corresponds to the current target from the drop-down list shown in figure 3.1.

Figure 3.1 Selecting a Session File

If you have selected a session file with which the simulator/debugger has been registered but the simulator/debugger is disconnected, select [Debug -> Connect] or click on the [Connect] toolbar button .

To disconnect the simulator/debugger, on the other hand, select [Debug -> Disconnect] or click on the [Disconnect] toolbar button .

3.2 Using the Simulator/Debugger Breakpoints

New items have been added to options for comparing data. This section gives the new specifications for [Break Data].

3.2.1 Setting a Breakpoint

- [Break Data]

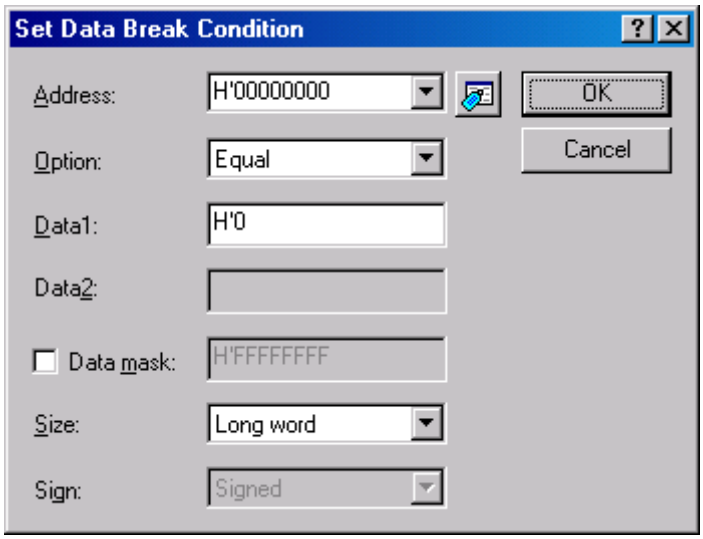

Figure 3.2 [Set Data Break Condition] Dialog Box

Data break conditions should be set as follows.

Up to 1024 data break conditions can be specified.

[Address]: Address in memory for which the break condition is specified

[Option]: How the data value is used to form the condition that must be satisfied for break generation

- [Equal]: The value written to memory matches [Data 1].
- [Not equal]: The value written to memory does not match [Data 1].
- [Inverse sign]*: The sign of the value written to memory is the inverse of that for the previous value.
- [Difference]*: The difference between the current and previous values written to memory exceeds [Data 1].
- [GT(>)]: A value written to memory is greater than [Data 1].
- [LT(<)]: A value written to memory is less than [Data 1].
- [GE(>=)]: A value written to memory is greater than or equal to [Data 1].
- [LE(<=)]: A value written to memory is less than or equal to [Data 1].
- [In]: A value written to memory is within the range between [Data 1] and [Data 2] ([Data 1] <= value written to memory <= [Data 2]).
- [Out]: A value written to memory is outside the range between [Data 1] and [Data 2] (value written to memory < [Data 1] | [Data 2] < value written to memory).

[Data 1]: Data value used in the break condition. When [In] or [Out] has been selected, [Data 1] is the beginning of a range for use in the break condition.

[Data 2]: Data value that is the end of a range for use in the break condition.
This option is only available when [In] or [Out] has been selected.

[Data mask]: Mask condition (specifying 0 for a bit masks the bit). This option is not available when [Inverse sign] or [Difference] has been selected.

[Size]: Data size

[Sign]: Sign of the data. This option is only available in the following cases.
- The selection for [Option] is [Difference].
- The selection for [Option] is [GT(>)], [LT(<)], [GE(>=)], [LE(<=)], [In], or [Out] and the selection for [Size] is [Byte], [Word], or [Long word].

Note: Since [Inverse sign] and [Difference] require comparison of the data with the value previously written to memory, the break will never occur on the first test after a reset or break generation when either of these conditions has been selected.

3.3 Command Line

Table 3.1 shows the command that has been added. For details on the command syntax, refer to the online help for the SuperH™ RISC engine Simulator/Debugger.

Table 3.1 New Command

Command	Abbreviation	Description
BREAK_DATA_RANGE	BDR	Specifies a range of values in memory as a break condition

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