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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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User's Manual

SH-4A, SH4AL-DSP E200F Emulator

Additional Document for User's Manual Supplementary Information on Using the SH7350

Renesas Microcomputer Development Environment System

SuperH™ Family

E200F for SH7350 R0E873500EMU00E

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Contents

Section 1 Connecting the Emulator with the User System

1.1 Components of the Emulator

The E200F emulator supports the AP realtime CPU (SH4AL-DSP) of the SH7350. Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator

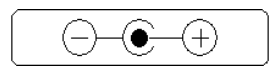
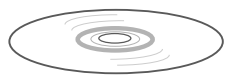
Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Emulator main unit		1	R0E0200F0EMU00: Depth: 185.0 mm, Width: 130.0 mm, Height: 45.0 mm, Mass: 321.0 g
	AC adapter (serial numbers: 0081 or before)		1	Input: 100 to 240 V Output: 12 V 4.0 A Depth: 120.0 mm, Width: 72.0 mm, Height: 27.0 mm, Mass: 400.0 g 
	AC adapter (serial numbers: 0082 or after)		1	Input: 100 to 240 V Output: 12 V 3.0 A Depth: 99.0 mm, Width: 62.0 mm, Height: 26.0 mm, Mass: 270.0 g 
	AC cable		1	Length: 200 mm

Table 1.1 Components of the Emulator (cont)

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware (cont)	USB cable		1	Length: 1500 mm, Mass: 50.6 g
	External probe (serial numbers: 0081 or before)		1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
	External probe (serial numbers: 0082 or after)		1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
Soft-ware	E200F emulator setup program, SH-4A, SH4AL-DSP E200F Emulator User's Manual, Supplementary Information on Using the SH7350*		1	R0E0200F0EMU00S, R0E0200F0EMU00J, R0E0200F0EMU00E, R0E873500EMU00J, R0E873500EMU00E (provided on a CD-R)

Note: Additional document for the devices supported by the emulator is included. Check the target device and refer to its additional document.

1.2 Connecting the Emulator with the User System

To connect the E200F emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the device.

It is impossible to connect the emulator to the 14-pin type connector that is recommended for the E10A-USB emulator. The 36-pin type connector is the same as that of the E10A-USB emulator. When designing the user system, read the E200F emulator user's manual and hardware manual for the related device.

The H-UDI port connector has the 36-pin and 14-pin types as described below. Use them according to the purpose of the usage.

1. 36-pin type (with AUD function)
   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)
   The AUD trace function cannot be used because only the H-UDI function is supported. This connector type is not available for the E200F emulator; the E10A-USB emulator is available.

1.3 Installing the H-UDI Port Connector on the User System

Table 1.2 shows the recommended H-UDI port connectors for the emulator.

Table 1.2 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type

Note: When designing the 36-pin connector layout on the user board, do not place any other signals under the H-UDI connector to reduce cross-talk noises, etc.

1.4 Pin Assignments of the H-UDI Port Connector

Figure 1.1 shows the pin assignments of the 36-pin H-UDI port connector.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following page differs from those of the connector manufacturer.

Pin No.	Signal	Input/ Output*1	Package Pin No.	Note	Pin No.	Signal	Input/ Output*1	Package Pin No.	Note
1	AUDCK	Output	G16		19	TMS	Input	J22	
2	GND	——			20	GND	——		
3	AUDATA0	Output	G17		21	_TRST	Input	H22	
4	GND	——			22	GND	——		
5	AUDATA1	Output	C16		23	TDI	Input	J25	
6	GND	——			24	GND	——		
7	AUDATA2	Output	E16		25	TDO	Output	J23	
8	GND	——			26	GND	——		
9	AUDATA3	Output	F16		27	_ASEBRK/ BRKACK*2	Input/ output	C15	
10	GND	——			28	GND	——		
11	_AUDSYNC *2	Output	F17		29	VCCQ	——		
12	GND	——			30	GND	——		
13	N.C.	——			31	_RESET *2, *4	Output	G13	Reset signal
14	GND	——			32	GND	——		
15	N.C.	——			33	GND*3	——		
16	GND	——			34	GND	——		
17	TCK	Input	J26		35	N.C.	——		
18	GND	——			36	GND	——		

Notes: 1. Input to or output from the user system.
2. The symbol "_" as the prefix to a signal name means that the signal is active-low.
3. The emulator monitors the GND signal of the user system to detect whether or not the user system is connected.
4. For the scope of the effect of the resets, refer to the hardware manual of the device; the scope may affect other CPUs in certain debugging modes.
5. Operation of the SH7350 will differ according to the levels on pins MD2 to MD4 and JTAG_CFG0 to JTAG_CFG3, and internal register values. For details, refer to the hardware manual of the device.

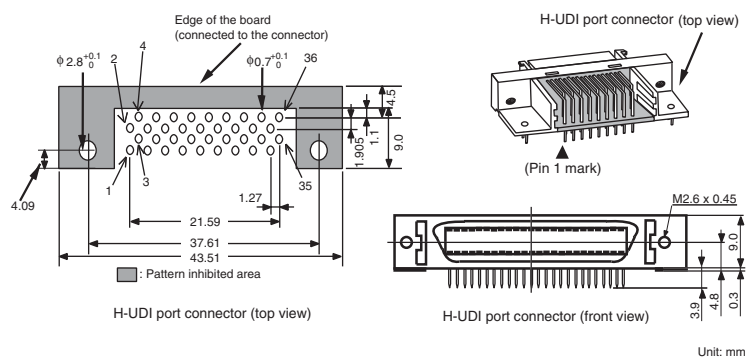


Figure 1.1 Pin Assignments of the H-UDI Port Connector (36 Pins)

1.5 Recommended Circuit between the H-UDI Port Connector and the Device

1.5.1 Recommended Circuit (36-Pin Type)

Figure 1.2 shows a recommended circuit for connection between the H-UDI and AUD port connectors (36 pins) and the device when the emulator is in use.

Notes: 1. Do not connect anything to pins of the H-UDI port connector labeled NC.

2. Debugging of the AP realtime CPU of the SH7350 requires specific settings for pins MD2 to MD4 and JTAG_CFG0 to JTAG_CFG3. For details, refer to the hardware manual of the device.
   Also see the hardware manual of the device for handling of these pins in cases where the emulator is not in use.
3. Lines of the pattern between the H-UDI port connector and the device must be as short as possible. We recommend that the signal lines **not** be connected to other components on the board. If AUD pins are connected to other components, the signal lines should be disconnected from other pin functions by switches, etc., in debugging.
4. Connect the VCCQ pin of the H-UDI port connector to the pattern that supplies VCCQ to the device.
5. The resistance value shown in figure 1.2 is for reference.
6. Since AUDCK is high-speed signal, guard the pattern between the H-UDI port connector and the device at GND level.

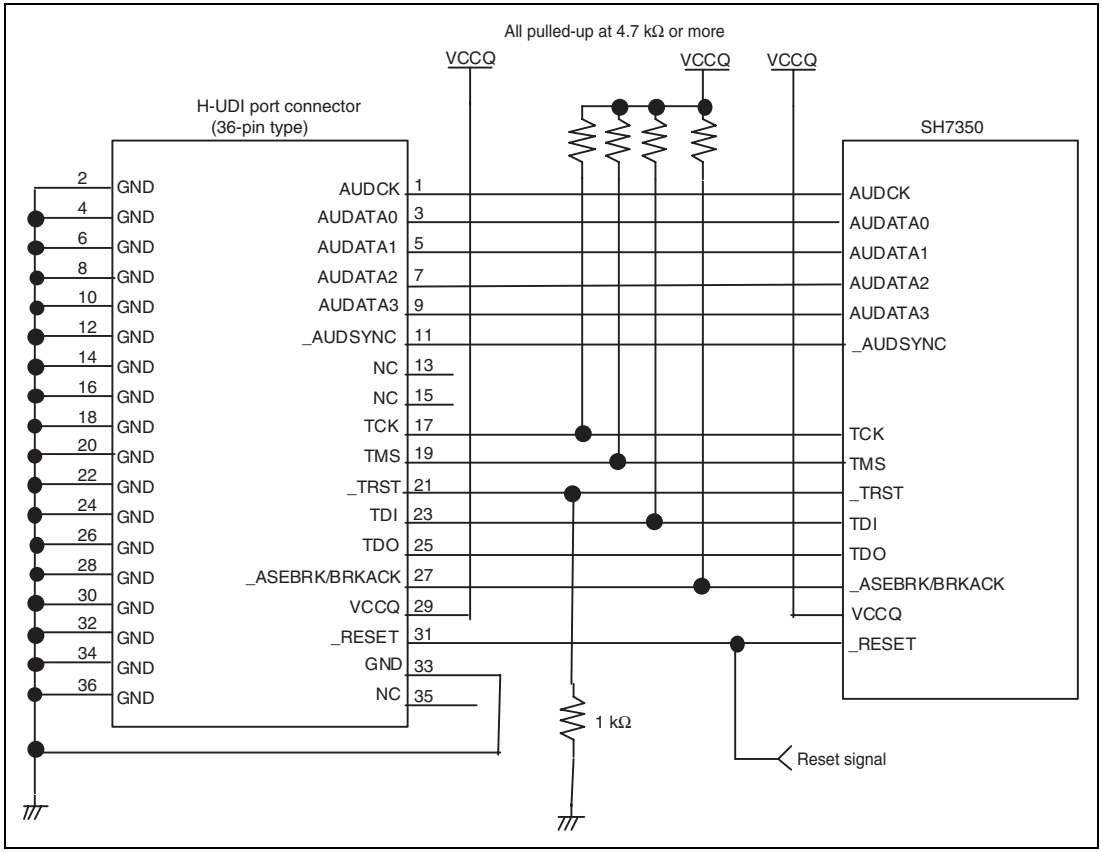


Figure 1.2 Recommended Circuit for Connection between the H-UDI Port Connector and Device when the Emulator is in Use (36-Pin Type)

Note: The symbol "_" as the prefix to a signal name means that the signal is active-low.

Section 2 Software Specifications when Using the SH7350

2.1 Differences between the SH7350 and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the AP realtime CPU (SH4AL-DSP) of the SH7350 registers are undefined. When the emulator is initiated from the workspace, a value to be entered is saved in a session.

Table 2.1 Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	H'A0000000
R0_BANK to R7_BANK	H'00000000
PC	H'A0000000
SR	H'700000F0
GBR	H'00000000
VBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
SPC	H'00000000
SSR	H'000000F0
RS	H'00000000
RE	H'00000000
MOD	H'00000000
A0G, A1G	H'00000000
A0, A1	H'00000000
X0, X1	H'00000000
Y0, Y1	H'00000000
M0, M1	H'00000000
DSR	H'00000000

2. The emulator uses the H-UDI; do not access the H-UDI.

3. Low-Power States (Sleep, Software Standby, and Module Standby)

   (1) For low-power consumption, the SH7350 has sleep, software standby, and module standby states. When the emulator is used, the sleep and software standby states can be cleared with either the normal clearing function or with the [STOP] button, and a break will occur.

   (2) Note the following when the AP realtime CPU (SH4AL-DSP) enters the power-off state or module-stopped state in the ARM side.

   - When the AP realtime CPU (SH4AL-DSP) enters the module-stopped state during execution of the GO command:
     Do not update the memory-type window.
   - When the AP realtime CPU (SH4AL-DSP) enters the module-stopped state during a break:
     Do not operate the emulator while the module is stopped.
   - Debugging is not supported when the AP realtime CPU (SH4AL-DSP) enters the power-off state.

Note: The memory must not be accessed or modified in sleep state.

4. Reset Signals

   The SH7350 reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the SH7350.

Note: Do not break the user program when the RESET_N pin is being low or the wait control and BUSY pins are being active. A Timeout error will occur. If the wait control and BUSY pins are fixed as active during break, a Timeout error will occur at memory access. Do not assert the RESET_N pin after the emulator has been activated; a Timeout error will occur.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   When a memory is accessed from the memory window, etc. during user program execution, the user program is resumed after it has stopped in the emulator to access the memory. Therefore, realtime emulation cannot be performed.

   The stopping time of the user program is as follows:

   Environment:

   Host computer: 800 MHz (Pentium® III)
   JTAG clock: 30 MHz

   When a one-byte memory is read from the command-line window, the stopping time will be about 45 ms.

7. Memory Access during User Program Break

   The emulator can download the program for the flash memory area (for details, refer to section 6.22, Download Function to the Flash Memory Area, in the SH-4A, SH4AL-DSP E200F Emulator User's Manual). Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM area.

8. Cache Operation during User Program Break

   When cache is enabled, the emulator accesses the memory by the following methods:

   - At memory write: Writes through the cache, then issues a single write to outside. The LRU is not updated.
   - At memory read: Reads memory from the cache. The LRU is not updated.

   Therefore, when memory read or write is performed during user program break, the cache state does not change.

   - At breakpoint set: Disables the instruction cache.

9. Port G

   The AUD pin is multiplexed as shown in table 2.2.

Table 2.2 Multiplexed Functions

Port	Function 1	Function 2
G	PTG4 input/output (port)*	/AUDSYNC (AUD)
G	PTG3 input/output (port)*	AUDATA3 (AUD)
G	PTG2 input/output (port)*	AUDATA2 (AUD)
G	PTG1 input/output (port)*	AUDATA1 (AUD)
G	PTG0 input/output (port)*	AUDATA0 (AUD)

Note: Function 1 can be used when the AUD pins of the device are not connected to the emulator. When the AUD trace function is enabled, the emulator changes settings so that function 2 is forcibly used.

10. UBC

    When [User] is specified in the [UBC mode] list box in the [Configuration] dialog box, the UBC can be used in the user program.
    Do not use the UBC in the user program as it is used by the emulator when [EML] is specified in the [UBC mode] list box in the [Configuration] dialog box.

11. Memory Access during Break

    In the enabled MMU, when a memory is accessed and a TLB error occurs during break, it can be selected whether the TLB exception is controlled or the program jumps to the user exception handler in [TLB Mode] in the [Configuration] dialog box. When [TLB miss exception is enable] is selected, a “Communication Timeout error” will occur if the TLB exception handler does not operate correctly. When [TLB miss exception is disable] is selected, the program does not jump to the TLB exception handler even if a TLB exception occurs. Therefore, if the TLB exception handler does not operate correctly, a “Communication Timeout error” will not occur but the memory contents may not be correctly displayed.

12. Loading Sessions

    Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be 2.5 MHz.

13. [IO] Window

    - Display and modification

      The I/O-register definition file can be customized depending on its format. Note that, however, the emulator does not support the bit-field function.

    - Verify

      In the [IO] window, the verify function of the input value is disabled.

14. Illegal Instructions

If illegal instructions are executed by STEP-type commands, the emulator cannot go to the next program counter.

15. Note on the Slave Mode of the Realtime CPU (SH4AL-DSP)

When the AP realtime CPU (SH4AL-DSP) is running in slave mode, the CPU will be in the module-stopped state immediately after a reset. To activate the emulator, follow the procedure below.

(1) When the emulator is activated, the message shown in figure 2.1 is displayed and remains on display until the CPU is taken out of the module-stopped state.

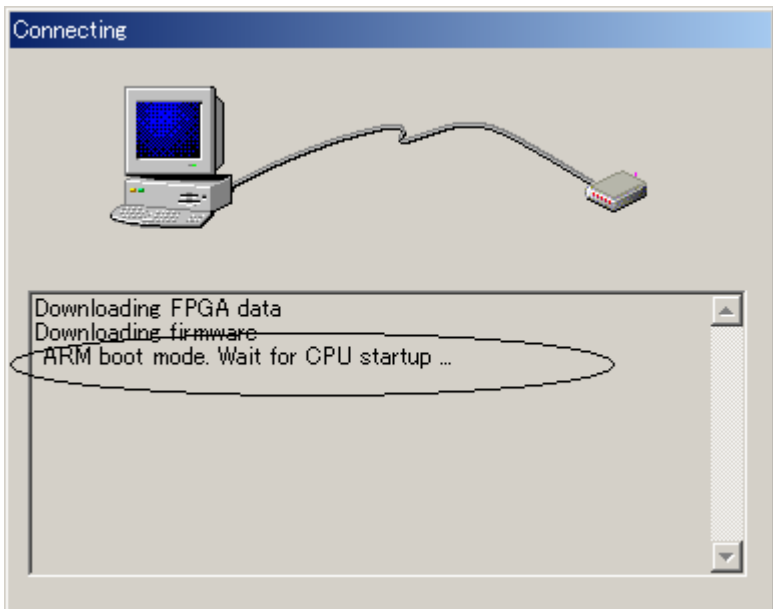


Figure 2.1 [Connecting] Dialog Box

(2) Take the AP realtime CPU (SH4AL-DSP) out of the module-stopped state on the ARM side.

(3) The emulator is activated.

2.2 Specific Functions for the Emulator when Using the SH7350

In the SH7350, a reset must be input when the emulator is activated.

2.2.1 Notes on Using the Trace Functions

The emulator supports the trace functions listed in table 2.4.

Table 2.4 Trace Functions

Function	Internal Trace	AUD Trace	Memory Output Trace
Branch trace	Supported (eight branches)	Supported	Supported
Range memory access trace	Supported (eight events)	Supported	Supported
Software trace	Supported (eight events)	Supported	Supported

Internal Trace Function: This function is activated by selecting the [Internal trace] radio button in the [Trace type] group box of the [Trace mode] page. Set the trace condition to be used.

Notes: 1. If an interrupt is generated at the program execution start or end, including a step operation, the emulator address may be acquired. In such a case, the following message will be displayed. Ignore this address because it is not a user program address.
*** EML ***

2. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.
3. Trace information cannot be acquired for the following branch instructions:
   - The BF and BT instructions whose displacement value is 0
   - Branch to H'A0000000 by reset

AUD Trace Function: This function is operational when the AUD pin of the device is connected to the emulator. It is activated by selecting the [AUD trace] radio button in the [Trace type] group box of the [Trace mode] page.

Notes: 1. When the trace display is performed during user program execution, the mnemonics, operands, or source is not displayed.

2. The AUD branch trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previously output address is the same as the upper 16 bits, the lower

16 bits are output. If it matches the upper 24 bits, the lower 8 bits are output. If it matches the upper 28 bits, the lower 4 bits are output.
The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.

3. If the 32-bit address cannot be displayed, the source line is not displayed.
4. In the emulator, when multiple loops are performed to reduce the number of AUD trace displays, only the IP counts up.
5. In the emulator, the maximum number of trace displays is 524288 lines. However, the maximum number of trace displays differs according to the AUD trace information to be output. Therefore, the above pointers cannot be always acquired.
6. The AUD trace acquisition is not available when [User] is selected in the [UBC mode] list box of the [Configuration] dialog box. In this case, close the [Trace] window.
7. Do not use the AUD full-trace mode for the VIO function.
8. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.

Memory Output Trace Functions: This function is activated by selecting the [Use Memory trace] radio button in the [Trace type] group box of the [Trace mode] page.
In this function, write the trace data in the specified user memory range.
Specify the start address to output a trace for the [Start] edit box in the [User memory area] group box, and the end address for the [End Address] edit box.

Notes: 1. The memory range for which trace is output is the address on the system bus and not supported for the MMU or cache.
2. In the memory range for output, do not specify the ranges that the user program has been downloaded or the user program accesses.
3. The range for trace output must be 1 MB or less.

2.2.2 Notes on Using the JTAG (H-UDI) Clock (TCK) and AUD Clock (AUDCK)

1. Set the JTAG clock (TCK) frequency to lower than the frequency of the SH7350 peripheral module clock (CKP).
2. Set the AUD clock (AUDCK) frequency to 54 MHz or lower. If the frequency is higher than 54 MHz, the emulator will not operate normally.
3. The set value of the JTAG clock (TCK) is initialized by executing [Reset CPU] or [Reset Go]. Thus the TCK value will be 2.5 MHz.

2.2.3 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address. Accordingly, it can be set only to the RAM areas in CS0 to CS6 and the internal RAM areas. A BREAKPOINT cannot be set to the following addresses:
   - ROM areas in CS0 to CS6
   - Areas other than CS0 to CS6 except for the internal RAM
   - A slot instruction of a delayed branch instruction
   - An area that can be only read by MMU
3. During step operation, BREAKPOINTs are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified, single-step operation is performed at the address and execution is continued from the next PC value. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.
6. Note on DSP repeat loop:
   A BREAKPOINT is equal to a branch instruction. In some DSP repeat loops, branch instructions cannot be set. For these cases, do not set BREAKPOINTs. Refer to the hardware manual of the device for details.
7. When the [Normal] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address or a virtual address according to the SH7350 MMU status during command input when the VPMAP_SET command setting is disabled. The ASID value of the SH7350 PTEH register during command input is used. When VPMAP_SET command setting is enabled, a BREAKPOINT is set to a physical address into which address translation is made according to the VP_MAP table. However, for addresses out of the range of the VP_MAP table, the address to which a BREAKPOINT is set depends on the SH7350 MMU status during command input. Even

when the VP_MAP table is modified after BREAKPOINT setting, the address translated when the BREAKPOINT is set valid.

8. When the [Physical] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address. A BREAKPOINT is set after disabling the SH7350 MMU upon program execution. After setting, the MMU is returned to the original state. When a break occurs at the corresponding virtual address, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
9. When the [Virtual] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a virtual address. A BREAKPOINT is set after enabling the SH7350 MMU upon program execution. After setting, the MMU is returned to the original state. When an ASID value is specified, the BREAKPOINT is set to the virtual address corresponding to the ASID value. The emulator sets the BREAKPOINT after rewriting the ASID value to the specified value, and returns the ASID value to its original value after setting. When no ASID value is specified, the BREAKPOINT is set to a virtual address corresponding to the ASID value at command input.
10. An address (physical address) to which a BREAKPOINT is set is determined when the BREAKPOINT is set. Accordingly, even if the VP_MAP table is modified after BREAKPOINT setting, the BREAKPOINT address remains unchanged. When a BREAKPOINT is satisfied with the modified address in the VP_MAP table, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
11. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the event condition, the mark ● disappears.

2.2.4 Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.
3. If a PC break address condition is set to the slot instruction after a delayed branch instruction, user program execution cannot be terminated before the slot instruction execution; execution stops before the branch destination instruction.

2.2.5 Note on Setting the UBC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [UBC mode] list box has been set, Ch10 (IA_OA_R) and Ch11 (IA_OA_DT_CT_R) of Event Condition cannot be used.

2.2.6 Note on Setting the PPC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [PPC mode] list box has been set, Ch1 and Ch2 of the performance analysis function and options 1 and 2 of the profile function cannot be used.

Section 3 Preparing to Connect the Trace Unit

3.1 Connecting the E200F Trace Unit with the User System

To use the external bus trace function in the emulator, the emulator and the user system must be connected via the external bus trace unit (R0E0200F0ETU00). Install the trace unit connector on the user system for connection of the trace unit, referring to section 3.2, Installing the Trace Unit Connector, in this manual. When designing the user system, read the SH-4A, SH4AL-DSP E200F Emulator User's Manual and hardware manual for the related device.

3.2 Installing the Trace Unit Connector

3.2.1 Trace Unit Connector Installed on the User System

Table 3.1 shows the recommended trace unit connector.

Table 3.1 Recommended Connector

Type Number	Manufacturer	Specification
QTH-090-04-L-D-A	Samtec, Inc.	QTH series, 0.5-mm pitch, 180 pins

Note: To connect the connector on the trace unit, do not place any components within 6 mm of the trace unit connector.

3.2.2 Pin Assignments of the User System Connector

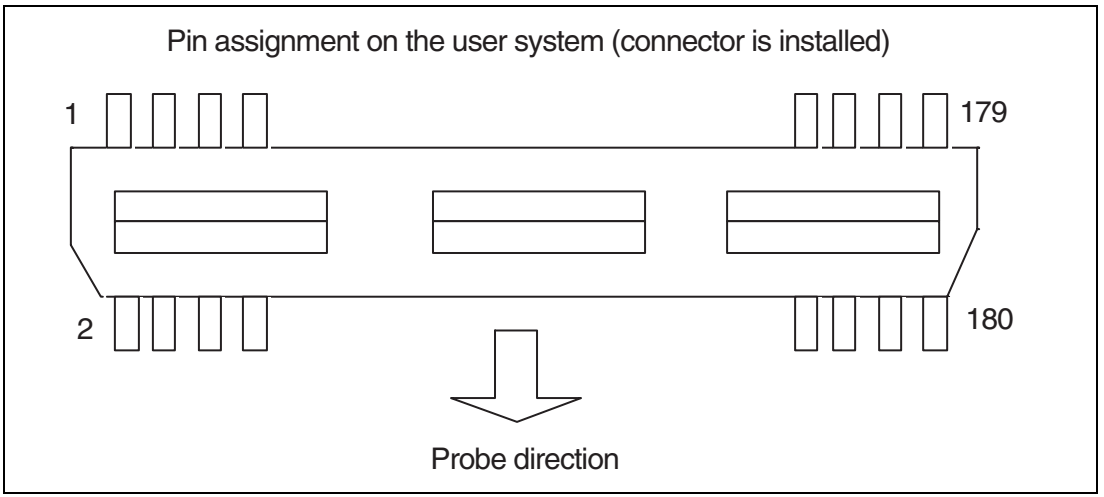


Figure 3.1 Pin Assignments of the User System Connector

3.2.3 Recommended Foot Pattern

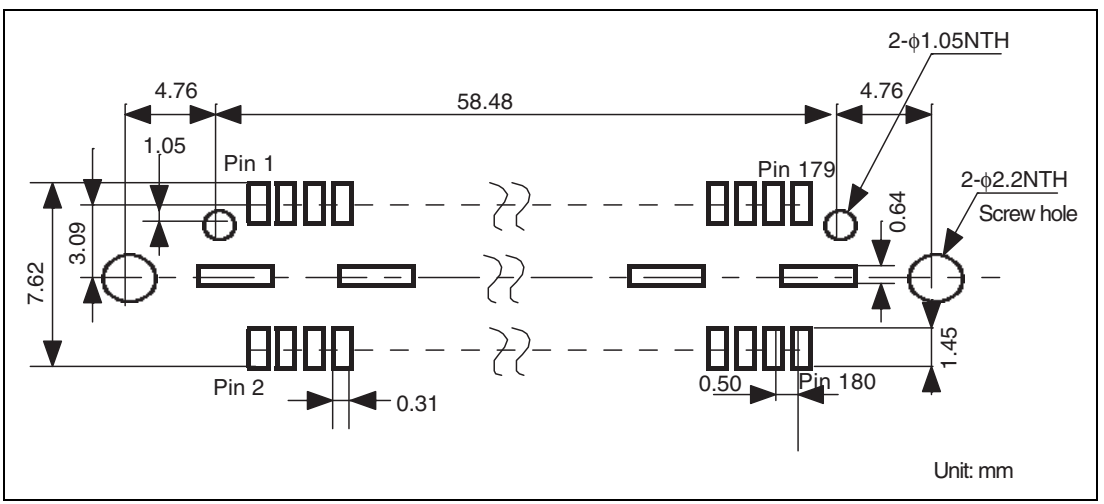


Figure 3.2 Recommended Foot Pattern (on which the Connector is Installed)

3.2.4 Restrictions on Component Installation

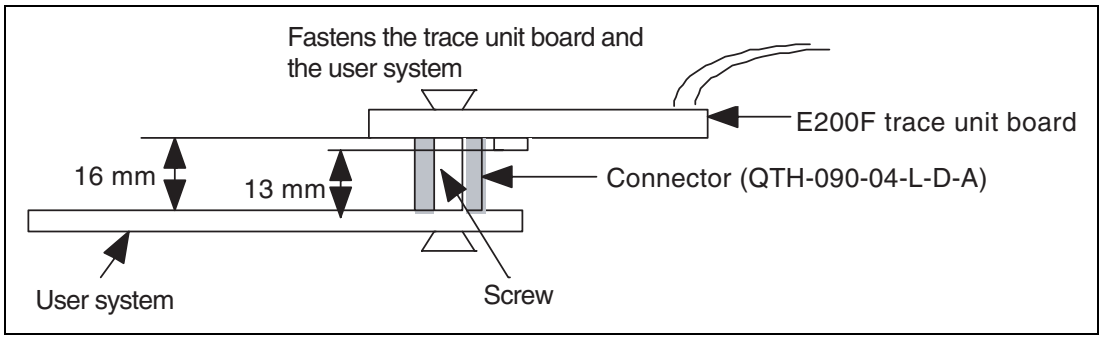


Figure 3.3 Restrictions on Component Installation

3.2.5 Pin Assignments of the Trace Unit Connector

Table 3.2 shows the pin assignments of the trace unit connector.

Table 3.2 Pin Assignments of the Trace Unit Connector

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
1	I	UA-P0	A0/BS_N/ PTK4	Port/address bus	Connect the address bus of the SH7350.
2	I	UA-P1	A1/PTN0	Address bus	Connect the address bus of the SH7350.
3	I	UA-P2	A2/PTN1	Address bus	Connect the address bus of the SH7350.
4	I	UA-P3	A3/PTN2	Address bus	Connect the address bus of the SH7350.
5	I	UA-P4	A4/PTN3	Address bus	Connect the address bus of the SH7350.
6	I	UA-P5	A5/PTN4	Address bus	Connect the address bus of the SH7350.
7	I	UA-P6	A6/PTN5	Address bus	Connect the address bus of the SH7350.
8	I	UA-P7	A7/MSIOF_ MCK0/PTJ0	Address bus	Connect the address bus of the SH7350.
9		GND	GND		
10		GND	GND		
11	I	UA-P8	A8/MSIOF_ MCK1/PTJ1	Address bus	Connect the address bus of the SH7350.
12	I	UA-P9	A9/MSIOF_ TSCK/PTJ2	Address bus	Connect the address bus of the SH7350.
13	I	UA-P10	A10/MSIOF_ TSYNC/PTJ3	Address bus	Connect the address bus of the SH7350.
14	I	UA-P11	A11/MSIOF_ SS1/PTJ4	Address bus	Connect the address bus of the SH7350.
15	I	UA-P12	A12/MSIOF_ SS2/PTJ5	Address bus	Connect the address bus of the SH7350.
16	I	UA-P13	A13/MSIOF_ RSCK/PTJ6	Address bus	Connect the address bus of the SH7350.
17	I	UA-P14	A14/MSIOF_ RSYNC/PTJ7	Address bus	Connect the address bus of the SH7350.
18	I	UA-P15	A15/MSIOF_ TXD/PTH0	Address bus	Connect the address bus of the SH7350.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
19		GND	GND		
20		GND	GND		
21	I	UA-P16	A16/MSIOF_ RXD/PTH1	Address bus	Connect the address bus of the SH7350.
22	I	UA-P17	A17/SIM_RST/ PTH2	Address bus	Connect the address bus of the SH7350.
23	I	UA-P18	A18/SIM_CLK/ PTH3	Address bus	Connect the address bus of the SH7350.
24	I	UA-P19	A19/SIM_D/ PTH4	Address bus	Connect the address bus of the SH7350.
25	I	UA-P20	A20/SCIF2_ RTS/PTH5	Address bus	Connect the address bus of the SH7350.
26	I	UA-P21	A21/SCIF2_ CTS/PTH6	Address bus	Connect the address bus of the SH7350.
27	I	UA-P22	A22/IRQ6/ PTH7	Address bus	Connect the address bus of the SH7350.
28	I	UA-P23	A23/FSC/PTK5	Address bus	Connect the address bus of the SH7350.
29		GND	GND		
30		GND	GND		
31	I	UA-P24	A24/FOE/PTK6	Address bus	Connect the address bus of the SH7350.
32	I	UA-P25	A25/FCDE/ PTK7	Address bus	Connect the address bus of the SH7350.
33	I	UA-P26	N.C.*1	N.C.	
34	I	UA-P27	N.C.*1	N.C.	
35	I	UA-P28	N.C.*1	N.C.	
36	I	UA-P29	N.C.*1	N.C.	
37	I	UA-P30	N.C.*1	N.C.	
38	I	UA-P31	N.C.*1	N.C.	
39		GND	GND		
40		GND	GND		

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
41	IO	UD-P0	D0/NAF0	Data bus	Connect the data signal of the SH7350.
42	IO	UD-P1	D1/NAF1	Data bus	Connect the data signal of the SH7350.
43	IO	UD-P2	D2/NAF2	Data bus	Connect the data signal of the SH7350.
44	IO	UD-P3	D3/NAF3	Data bus	Connect the data signal of the SH7350.
45	IO	UD-P4	D4/NAF4	Data bus	Connect the data signal of the SH7350.
46	IO	UD-P5	D5/NAF5	Data bus	Connect the data signal of the SH7350.
47	IO	UD-P6	D6/NAF6	Data bus	Connect the data signal of the SH7350.
48	IO	UD-P7	D7/NAF7	Data bus	Connect the data signal of the SH7350.
49		GND	GND		
50		GND	GND		
51	IO	UD-P8	D8/NAF8	Data bus	Connect the data signal of the SH7350.
52	IO	UD-P9	D9/NAF9	Data bus	Connect the data signal of the SH7350.
53	IO	UD-P10	D10/NAF10	Data bus	Connect the data signal of the SH7350.
54	IO	UD-P11	D11/NAF11	Data bus	Connect the data signal of the SH7350.
55	IO	UD-P12	D12/NAF12	Data bus	Connect the data signal of the SH7350.
56	IO	UD-P13	D13/NAF13	Data bus	Connect the data signal of the SH7350.
57	IO	UD-P14	D14/NAF14	Data bus	Connect the data signal of the SH7350.
58	IO	UD-P15	D15/NAF15	Data bus	Connect the data signal of the SH7350.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
59		GND	GND		
60		GND	GND		
61	IO	UD-P16	N.C.*1	N.C.	
62	IO	UD-P17	N.C.*1	N.C.	
63	IO	UD-P18	N.C.*1	N.C.	
64	IO	UD-P19	N.C.*1	N.C.	
65	IO	UD-P20	N.C.*1	N.C.	
66	IO	UD-P21	N.C.*1	N.C.	
67	IO	UD-P22	N.C.*1	N.C.	
68	IO	UD-P23	N.C.*1	N.C.	
69		GND	GND		
70		GND	GND		
71	IO	UD-P24	N.C.*1	N.C.	
72	IO	UD-P25	N.C.*1	N.C.	
73	IO	UD-P26	N.C.*1	N.C.	
74	IO	UD-P27	N.C.*1	N.C.	
75	IO	UD-P28	N.C.*1	N.C.	
76	IO	UD-P29	N.C.*1	N.C.	
77	IO	UD-P30	N.C.*1	N.C.	
78	IO	UD-P31	N.C.*1	N.C.	
79		GND	GND		
80		GND	GND		
81	IO	UD-P32	N.C.*1	N.C.	
82	IO	UD-P33	N.C.*1	N.C.	
83	IO	UD-P34	N.C.*1	N.C.	
84	IO	UD-P35	N.C.*1	N.C.	
85	IO	UD-P36	N.C.*1	N.C.	
86	IO	UD-P37	N.C.*1	N.C.	
87	IO	UD-P38	N.C.*1	N.C.	
88	IO	UD-P39	N.C.*1	N.C.	

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
89		GND	GND		
90		GND	GND		
91	IO	UD-P40	N.C.*1	N.C.	
92	IO	UD-P41	N.C.*1	N.C.	
93	IO	UD-P42	N.C.*1	N.C.	
94	IO	UD-P43	N.C.*1	N.C.	
95	IO	UD-P44	N.C.*1	N.C.	
96	IO	UD-P45	N.C.*1	N.C.	
97	IO	UD-P46	N.C.*1	N.C.	
98	IO	UD-P47	N.C.*1	N.C.	
99		GND	GND		
100		GND	GND		
101	IO	UD-P48	N.C.*1	N.C.	
102	IO	UD-P49	N.C.*1	N.C.	
103	IO	UD-P50	N.C.*1	N.C.	
104	IO	UD-P51	N.C.*1	N.C.	
105	IO	UD-P52	N.C.*1	N.C.	
106	IO	UD-P53	N.C.*1	N.C.	
107	IO	UD-P54	N.C.*1	N.C.	
108	IO	UD-P55	N.C.*1	N.C.	
109		GND	GND		
110		GND	GND		
111	IO	UD-P56	N.C.*1	N.C.	
112	IO	UD-P57	N.C.*1	N.C.	
113	IO	UD-P58	N.C.*1	N.C.	
114	IO	UD-P59	N.C.*1	N.C.	
115	IO	UD-P60	N.C.*1	N.C.	
116	IO	UD-P61	N.C.*1	N.C.	
117	IO	UD-P62	N.C.*1	N.C.	
118	IO	UD-P63	N.C.*1	N.C.	

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
119		GND	GND		
120		GND	GND		
121	I	UCONT-P0	WE0_N/PTK0	Lower byte write signal (D7-D0)	Connect the WE0 signal of the SH7350.
122	I	UCONT-P1	WE1_N/PTK1	Upper byte write signal (D15-D8)	Connect the WE1 signal of the SH7350.
123	I	UCONT-P2	N.C.*1	N.C.	
124	I	UCONT-P3	N.C.*1	N.C.	
125	I	UCONT-P4	N.C.*1	N.C.	
126	I	UCONT-P5	N.C.*1	N.C.	
127	I	UCONT-P6	N.C.*1	N.C.	
128	I	UCONT-P7	N.C.*1	N.C.	
129	I	UCONT-P8	N.C.*1	N.C.	
130	I	UCONT-P9	N.C.*1	N.C.	
131	I	UCONT-P10	RDWR_N/ FWE/PTK3	Read/write signal	Connect the RDWR signal of the SH7350.
132	I	UCONT-P11	RD_N/NBRST OUT_/PTV3	Read signal	Connect the RD signal of the SH7350.
133	I	UCONT-P12	RESET_N	Power-on reset	Connect the RESET_N signal of the SH7350.
134	I	UCONT-P13	NBRST_N	Boot inhibited	Connect the NBRST_N signal of the SH7350.
135	I	UCONT-P14	N.C.*1	N.C.	
136	I	UCONT-P15	N.C.*1	N.C.	

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
137	I	UCONT-P16	WAIT_N/FRB/ PTK2	Wait/ I/O port K	Connect the wait signal of the SH7350. When WAIT is not used, this is N.C.
138	I	UCONT-P17	IRDA_IN/ STATUS0/ PTC2	Status 0	Connect the STATUS0 signal of the SH7350.
139	I	UCONT-P18	IRDA_OUT/ STATUS1/ PTC3	Status 1	Connect the STATUS2 signal of the SH7350.
140	I	UCONT-P19	IRDA_FIRSEL/STATUS2/ PTC4	Status 2	Connect the PDSTATUS signal of the SH7350.
141	I	UCONT-P20	NMI	NMI	Connect the NMI signal of the SH7350.
142	I	UCONT-P21	IRQ0/PTF0	External interrupt request/input port F	Connect the interrupt request signal. When interrupt is not used, this is N.C.
143	I	UCONT-P22	IRQ1/PTF1	External interrupt request/input port F	Connect the interrupt request signal. When interrupt is not used, this is N.C.
144	I	UCONT-P23	IRQ2/PTF2	External interrupt request/input port F	Connect the interrupt request signal. When interrupt is not used, this is N.C.
145	I	UCONT-P24	IRQ3/PTF3	External interrupt request/input port F	Connect the interrupt request signal. When interrupt is not used, this is N.C.
146	I	UCONT-P25	IRQ4/PTF4	External interrupt request/input port F	Connect the interrupt request signal. When interrupt is not used, this is N.C.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
147	I	UCONT-P26	IRQ5	External interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.
148	I	UCONT-P27	A22/IRQ6/PTH7	External interrupt request/input port H	Connect the interrupt request signal. When interrupt is not used, this is N.C.
149	I	UCONT-P28	N.C.*1	N.C.	
150	I	UCONT-P29	N.C.*1	N.C.	
151	I	UCONT-P30	N.C.*1	N.C.	
152	I	UCONT-P31	N.C.*1	N.C.	
153	I	GND	GND		
154	I	GND	GND		
155	I	MPUCLK	CKO	CKO clock	Be sure to connect the CKO clock of the SH7350.
156	I	GND	GND		
157	I	GND	GND		
158	I	DDRCLK	N.C.*1	N.C.	
159	I	GND	GND		
160	I	DDRCLK-N	N.C.*1	N.C.	
161	I	GND	GND		
162	I	GND	GND		
163	I	CS0IN-N	CS0_N	Chip select 0	Connect CS (chip select). Fix the unused CS pin to high level.
164	I	CS1IN-N	CS2_N/PTM0	Chip select 2/ I/O port M	Connect CS (chip select). Fix the unused CS pin to high level.
165	I	CS2IN-N	N.C.*1	N.C.	

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7350 Signal Name	Meaning of Signal	Note
166	I	CS3IN-N	CS4_N/PTM1	Chip select 4/ I/O port M	Connect CS (chip select). Fix the unused CS pin to high level.
167	I	CS4IN-N	CS5A_N/PTM 2	Chip select 5A/ I/O port M	Connect CS (chip select). Fix the unused CS pin to high level.
168	I	CS5IN-N	CS5B_N/PTM 3	Chip select 5B/ I/O port N	Connect CS (chip select). Fix the unused CS pin to high level.
169	I	CS6IN-N	CS6A_N/ FCE0_/PTN6	Chip select 6A/ FCE0/ I/O port N	Connect CS (chip select). Fix the unused CS pin to high level.
170	I	CS7IN-N	CS6B_N/ FCE1_/PTN7	Chip select 6B/ FCE1/ I/O port N	Connect CS (chip select). Fix the unused CS pin to high level.
171	I	CS8IN-N	-		
172	I	CS9IN-N	-		
173	O	EM0OUT-N	EM0OUT-N	Emulation-memory select output	Connect this signal instead of CS of the device when an emulation memory is used.[*2]
174	O	EM1OUT-N	N.C.[*1]		
175	O	EM2OUT-N	N.C.[*1]		
176	O	EMEN-P	N.C.[*1]		
177	I	UVCC1	Vcc_SL	Vcc_SL	1.8 V / 2.85 V
178	I	UVCC2	VccQ3	VccQ3	1.8 V
179	I	UVCC3	Power supply for user system: 2.85 V	Power supply for user system: 2.85 V	2.85 V
180	I	UCNN-N	Connect to user connector	GND	Fix this signal to low level.

Notes: 1. Do not connect anything to this pin.
2. Refer to section 3.2.8, Description of Emulation Memory Control Signal.

3.2.6 Layout of the Trace Unit Connector

When designing the user system, there are restrictions on the position to install the trace unit connector. Figure 3.4 shows the external dimensions of the trace unit.

The size of the printed-circuit board of the E200F trace unit is 90 mm × 125 mm. The size of components around the user system connector must not exceed the limit on component installation (the height must be 10 mm or less).

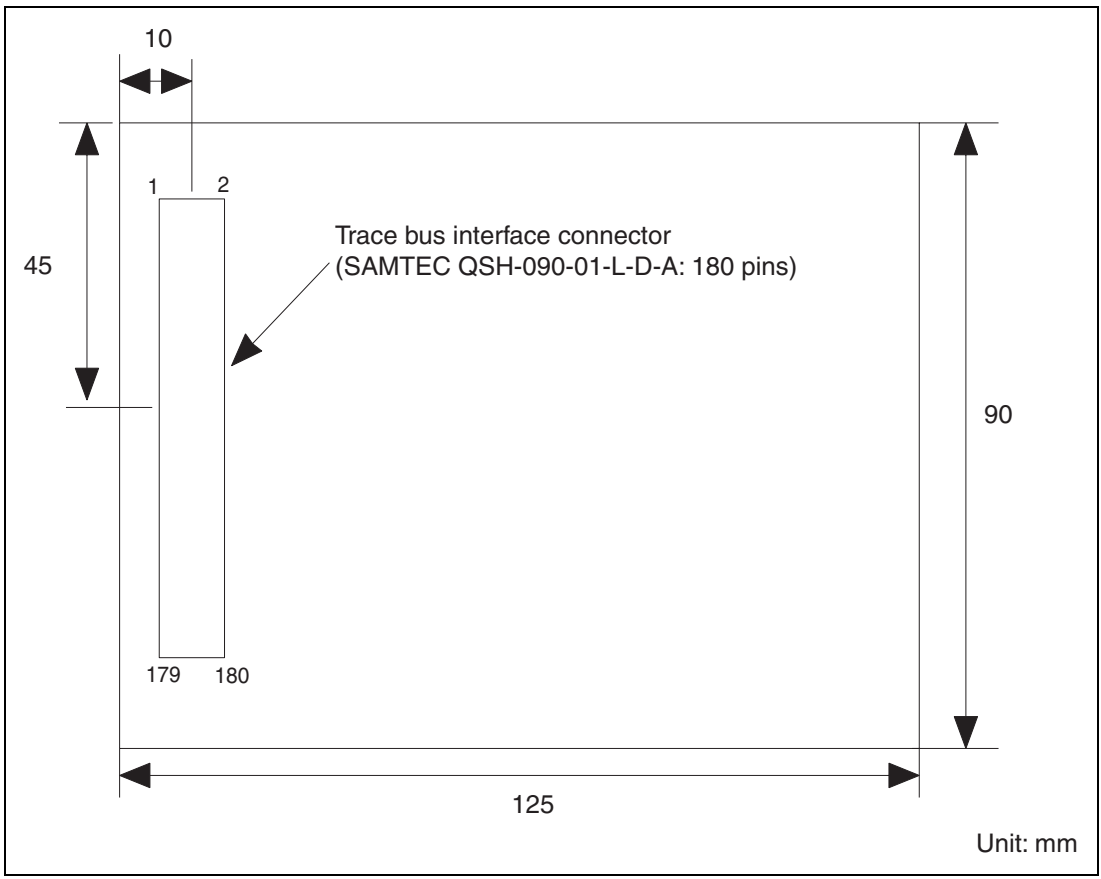


Figure 3.4 External Dimensions of the Trace Unit (on which the Connector is Installed)

Notes: 1. The external bus trace interface connector installed on the user system must be as close to the device as possible.

2. Wiring pattern of clock lines (CKO)
   The followings are notes on wiring of clock lines for the E200F trace interface signals. Take them into consideration when designing the user system to embed suitable clock lines.
   (a) Clock lines must be as short as possible.
   (b) Clock lines must be surrounded by the GND pattern for protection so that the signals will be of low-impedance.
   (c) Other layers next to the layer with clock line wiring should have solid patterns of GND/VCC so that the signals will be of low-impedance.
   (d) To prevent affect by the crosstalk noise, other signal patterns must not be embedded along with the clock lines.

3.2.7 Restrictions on Using the Trace Unit

(1) This trace unit supports the external bus memory interfaces of SH7350; SRAM interface and byte-selection SRAM interface (except for SRAM page mode). For burst ROM and SDRAM interfaces, bus trace acquisition and bus event detection are not supported.

(2) When the sequential trace stop condition or delay-count trace stop condition is specified, trace acquisition will stop after several cycles have been passed from the stop condition match cycle.

(3) During break mode, a timestamp value of the external bus trace information that has been acquired by a trace is not counted up.

(4) When an emulation memory is used, it is not possible to access the memory on the user system which is in the same area as an area where the emulation memory has been set.

(5) When an emulation memory is accessed, at least six wait cycles are required. Set the number of wait cycles by using bits WR3 to WR0 in the CS0 area wait control register (CS0WCR).

(6) The emulator occupies the CS0 area where the emulation memory has been set. Accordingly, it is not possible to access the memory in the user system side of that area.

(7) This trace unit is available for the external 8- or 16-bit data bus width. When the data bus width is 8 bits, unused data bus pins D15 to D8 of the trace unit connector must be fixed to high or low level. In addition, when area 0 is used with the emulation memory, the bus width of the emulation memory needs to be set. For details, refer to section 5.1.8, Changing the Memory Map Setting, in the SH-4A, SH4AL-DSP E200F Emulator User's Manual.

3.2.8 Description of Emulation Memory Control Signal

When the CS signal of the device is connected directly to the memory or used to generate the CS signal of the memory, connect the EM0OUT-N signal (pin 173) of the external bus connector instead of the CS signal of the device.

Even if the emulator is not used, prepare the jumper pins as shown in figure 3.5 so that connection of the CS signal can be easily changed.

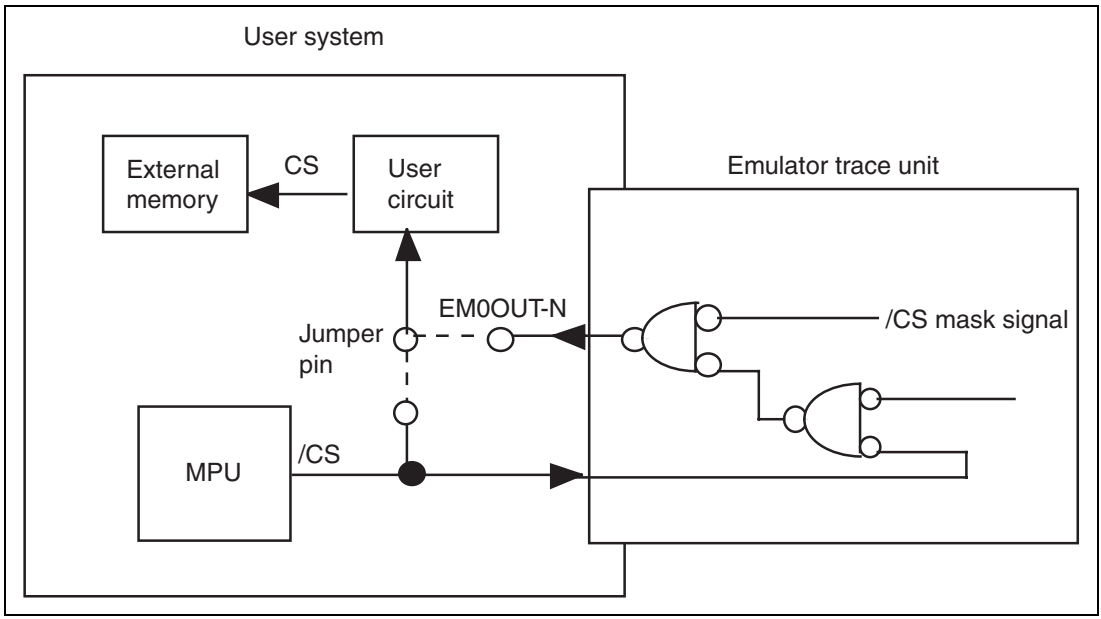


Figure 3.5 EM0OUT-N Signal (Pin 173)

SH-4A, SH4AL-DSP E200F Emulator
Additional Document for User's Manual
Supplementary Information on Using the SH7350

Publication Date: Rev.1.00, July 25, 2007
Published by: Sales Strategic Planning Div.
Renesas Technology Corp.
Edited by: Customer Support Department
Global Strategic Communication Div.
Renesas Solutions Corp.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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REJ10J1701-0100