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April 1st, 2010
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User's Manual

SH-2A, SH-2 E200F Emulator

Additional Document for User's Manual Supplementary Information on Using the SH7214 and SH7216

Renesas Microcomputer Development Environment System
SuperH™ Family / SH7216 Series

E200F for SH7216 R0E572160EMU00E

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Contents

Section 1 System Configuration

1.1 Components of the Emulator

The E200F emulator supports the SH7214 and SH7216 group. Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator

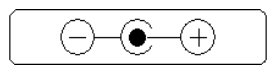
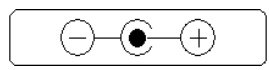
Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Emulator main unit		1	R0E0200F1EMU00: Depth: 185.0 mm, Width: 130.0 mm, Height: 45.0 mm, Mass: 321.0 g
	AC adapter	E200F serial numbers: 0001 to 0113		
			1	Input: 100 to 240 V Output: 12 V 4.0 A Depth: 120.0 mm, Width: 72.0 mm, Height: 27.0 mm, Mass: 400.0 g 
		E200F serial numbers: 0114 or later		
			1	Input: 100 to 240 V Output: 12 V 3.0 A Depth: 99.0 mm, Width: 62.0 mm, Height: 26.0 mm, Mass: 270.0 g 
	AC cable		1	Length: 2000 mm

Table 1.1 Components of the Emulator (cont)

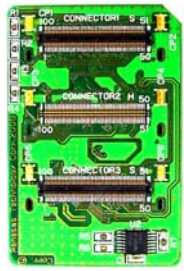
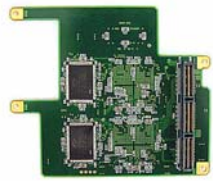
Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware (cont)	USB cable		1	Length: 1500 mm, Mass: 50.6 g
	External probe	E200F serial numbers: 0001 to 0113		
			1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
		E200F serial numbers: 0114 or later		
			1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
Soft-ware	E200F emulator setup program, SH-2A, SH-2 E200F Emulator User's Manual, and Supplementary Information on Using the Sh7214 and SH7216*		1	R0E0200F1EMU00S, R0E0200F1EMU00J, R0E0200F1EMU00E, R0E572160EMU00J, and R0E572160EMU00E (provided on a CD-R)

Note: Additional document for the MCUs supported by the emulator is included. Check the target MCU and refer to its additional document.

Table 1.2 Optional Components of the Emulator

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	External bus trace unit		1	R0E0200F1ETU00: Depth: 90.0 mm, Width: 125.0 mm, Height: 15.2 mm, Mass: 100 g
	Emulation memory unit (Memory capacity: 8 Mbytes or 16 Mbytes)		1	R0E0200F1MSR00 (8 Mbytes), R0E0200F1MSR01 (16 Mbytes): Depth: 90.0 mm, Width: 125.0 mm, Height: 15.2 mm, Mass: 81 g (R0E0200F1MSR00), 85 g (R0E0200F1MSR01) Note that it is not possible to connect these emulation memory units at the same time.
	EV-chip unit		1	R0E572160VKK00: Depth: 110.0 mm, Width: 125.0 mm, Height: 15.2 mm, Mass: 108 g
	Trace cable		1	R0E0200F0ACC00: Length: 300 mm, Mass: 65 g
	Common user-system interface adaptor cable (board unit and flexible cable unit)		1	R0E0200F1CKL11 (board unit): Depth: 60.0 mm, Width: 90.0 mm, Height: 26.0 mm, Mass: 37 g
			1	R0E0200F1CKL11 (flexible cable unit): Depth: 35.0 mm, Width: 267.0 mm, Height: 5.05 mm, Mass: 8 g

Table 1.2 Optional Components of the Emulator (cont)

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware (cont)	SH7214 and SH7216 (PLQP0176KB-A) user-system interface converter board		1	R0E572167CFK10: Depth: 53.0 mm, Width: 35.0 mm, Height: 11.0 mm, Mass: 22 g
	SH7214 and SH7216 (PLQP0176LB-A) user-system interface converter board		1	R0E572167CFL10: Depth: 53.0 mm, Width: 35.0 mm, Height: 11.0 mm, Mass: 21 g
	Expansion profiling unit		1	R0E0200F0EPU00: Depth: 98.0 mm, Width: 115.0 mm, Height: 15.2 mm, Mass: 52 g

1.2 System Configuration

Figure 1.1 shows an example of the emulator system configuration.

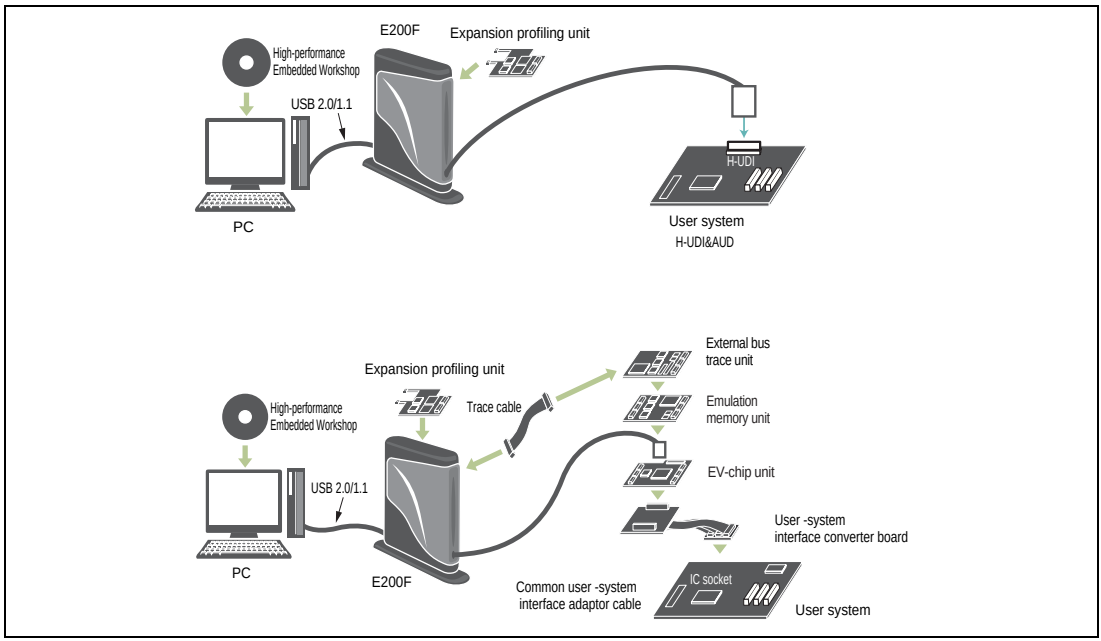


Figure 1.1 System Configuration Using the Emulator

(1) System Configuration of the SH7214 and SH7216 group

Table 1.3 shows the system configuration supported by the SH7214 and SH7216 group.

Table 1.3 System Configuration Supported by the SH7214 and SH7216 Group

	E200F Emulator	EV-chip Unit	External Bus Trace Unit	Emulation Memory Unit	Expansion Profiling Unit	Trace Cable	Common User-System Interface Adaptor Cable	User-System Interface Converter Board
	R0E0200F1EMU00	R0E572160VKK00	R0E0200F1ETU00	R0E0200F1MSR00 R0E0200F1MSR01	R0E0200F0EPU00	R0E0200F0ACC00	R0E0200F1CKL11	R0E572167CFK10 R0E572167CFL10
System configuration 1*1	Supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported	Not supported
System configuration 2*2	Supported	Supported	Not supported	Not supported	Not supported	Supported	Supported	Supported
System configuration 3*2	Supported	Supported	Not supported	Supported	Not supported	Supported	Supported	Supported
System configuration 4*2	Supported	Supported	Supported	Not supported	Not supported	Supported	Supported	Supported
System configuration 5*2	Supported	Supported	Supported	Supported	Not supported	Supported	Supported	Supported
System configuration 6*1	Supported	Not supported	Not supported	Not supported	Supported	Not supported	Not supported	Not supported
System configuration 7*2	Supported	Supported	Not supported	Not supported	Supported	Supported	Supported	Supported
System configuration 8*2	Supported	Supported	Not supported	Supported	Supported	Supported	Supported	Supported
System configuration 9*2	Supported	Supported	Supported	Not supported	Supported	Supported	Supported	Supported
System configuration 10*2	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported

Notes: 1. When the EV-chip unit is not used, the H-UDI port connector must be installed on the user system. When designing the user system, refer to section 2.3, Connecting the Emulator to the User System by Using the H-UDI Port Connector. For this system configuration, note that the H-UDI and AUD pins of the MCU are occupied by the emulator.

2. The common user-system interface adaptor cable and user-system interface converter board are only used when the emulator is connected to the user system; they are not required when the emulator system operates alone.

Section 2 Connecting the Emulator to the User System

2.1 Connecting the Emulator to the User System

When the emulator is connected to the user system, use the optional EV-chip unit, common user-system interface adaptor cable, user-system interface converter board and trace cable.

2.2 Connecting the Emulator to the User System by Using the EV-chip Unit

The following describes how to connect the emulator to the EV-chip unit, external bus trace unit, emulation memory unit, trace cable, common user-system interface adaptor cable, and user-system interface converter board.

2.2.1 Connecting the EV-chip Unit to the Emulator

- Open the cover of TRACE I/F on the side of the main unit case.
- Connect the trace cable to the EV-chip unit as shown in figure 2.1.

Figure 2.1 Connecting the Trace Cable to E200F when Using the EV-chip Unit

- Connect the EV-chip unit to the trace cable (CN1 side).

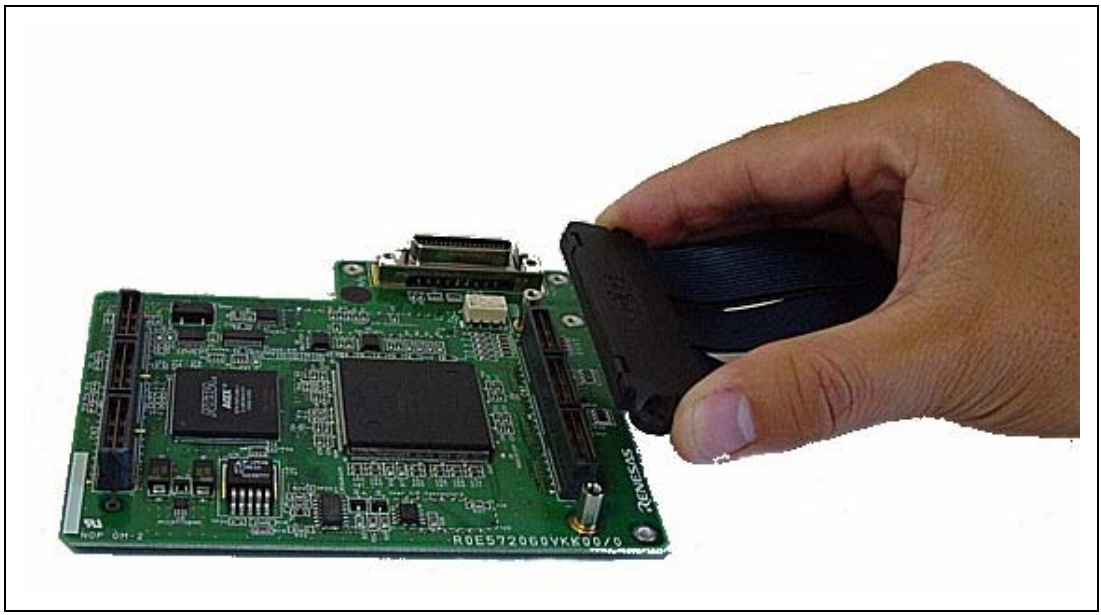


Figure 2.2 Connecting the Trace Cable to the EV-chip Unit

⚠ CAUTION
Check the orientation of pin 1 before connecting parts.

2.2.2 Connecting the E200F External Bus Trace Unit to the EV-chip Unit

- When the external bus trace unit is used with the EV-chip unit, connect the external bus trace unit to the EV-chip unit as shown in figure 2.3.

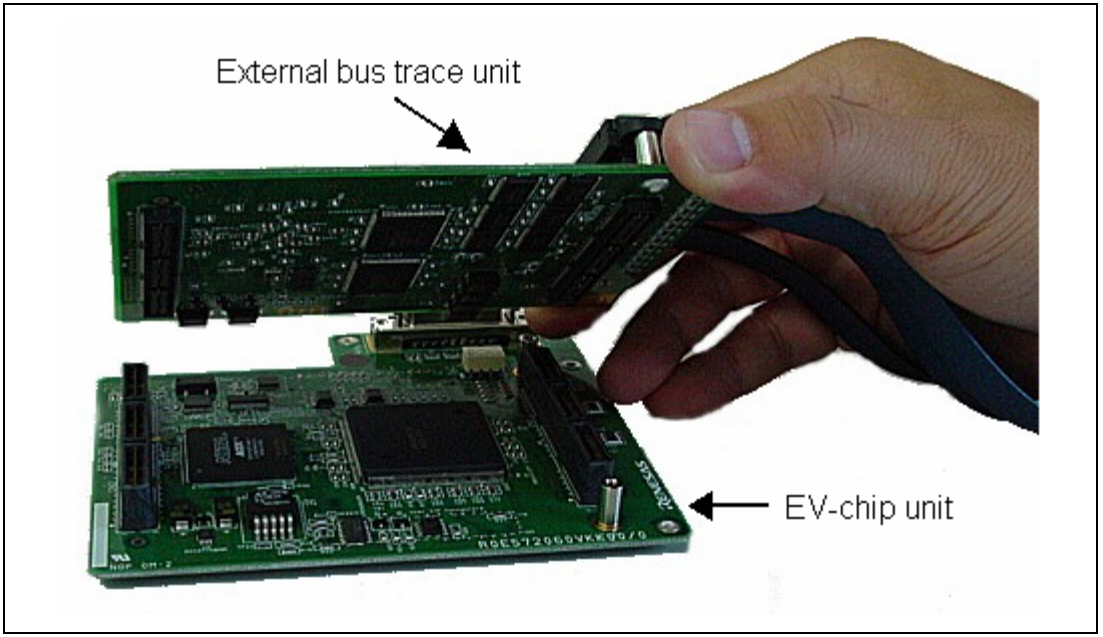


Figure 2.3 Connecting the External Bus Trace Unit to the EV-chip Unit

- After checking the location of pin 1, connect the EV-chip unit, external bus trace unit, and trace cable.

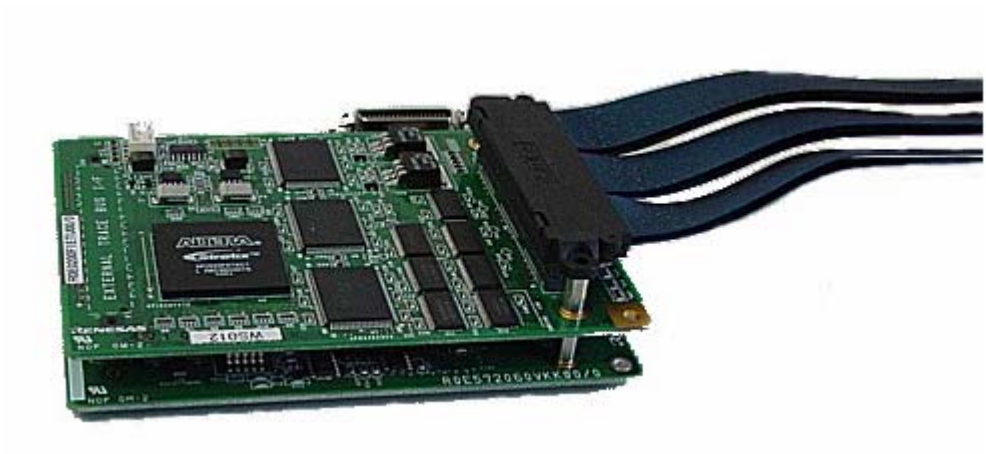


Figure 2.4 Connecting the EV-chip Unit, External Bus Trace Unit, and Trace Cable

⚠ CAUTION
Check the orientation of pin 1 before connecting parts.

2.2.3 Connecting the H-UDI/AUD Probe to the EV-chip Unit

- Connect the H-UDI/AUD probe to the EV-chip unit as shown in figure 2.5.

Figure 2.5 Connecting the H-UDI/AUD Probe to the EV-chip Unit

⚠ CAUTION
Check the orientation of pin 1 before connecting parts.

2.2.4 Connecting the E200F Emulation Memory Unit to the EV-chip Unit

- When the emulation memory unit is used with the EV-chip unit, connect the emulation memory unit to the EV-chip unit (figure 2.6).

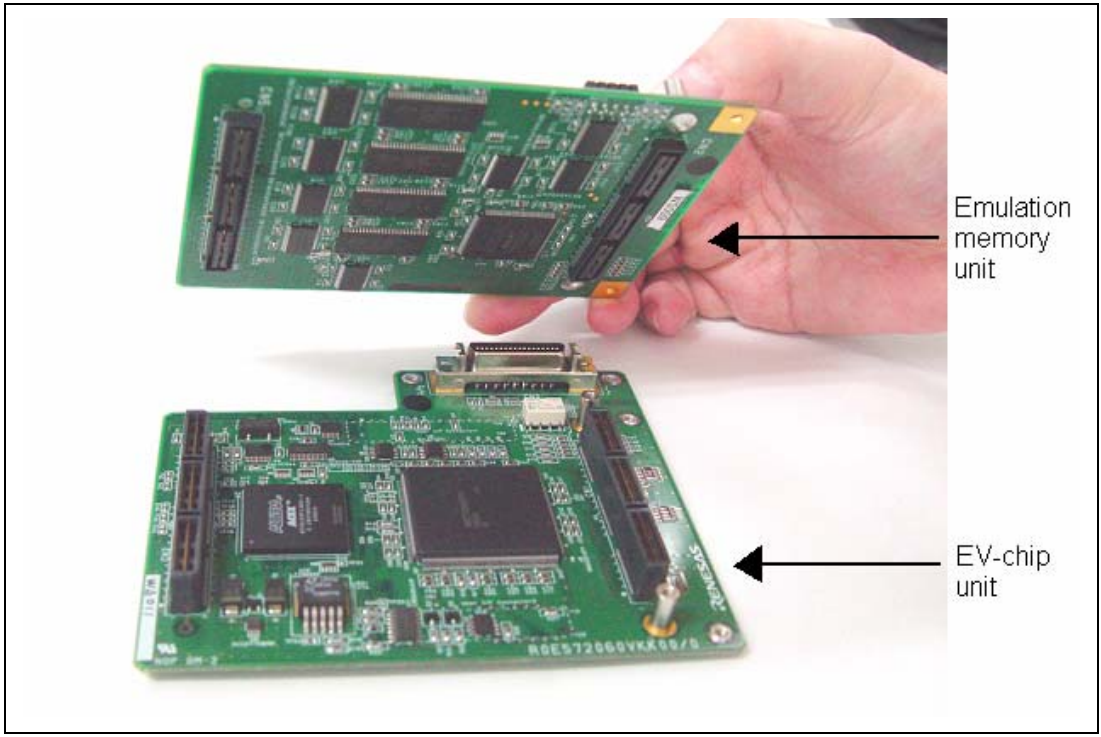


Figure 2.6 Connecting the Emulation Memory Unit to the EV-chip Unit

- After checking the location of pin 1, connect the EV-chip unit, emulation memory unit, and trace cable.

Figure 2.7 Connecting the Emulation Memory Unit, EV-chip Unit, and Trace Cable

⚠ CAUTION
Check the orientation of pin 1 before connecting parts.

2.2.5 Connecting the E200F External Bus Trace Unit, Emulation Memory Unit, and EV-chip Unit

- When the external bus trace unit is used with the emulation memory unit and EV-chip unit, as shown in figure 2.8, connect them in the positions of (a), (b), and (c) for the external bus trace unit, emulation memory unit, and EV-chip unit, respectively.
- After checking the location of pin 1, connect the external bus trace unit, emulation memory unit, and EV-chip unit.

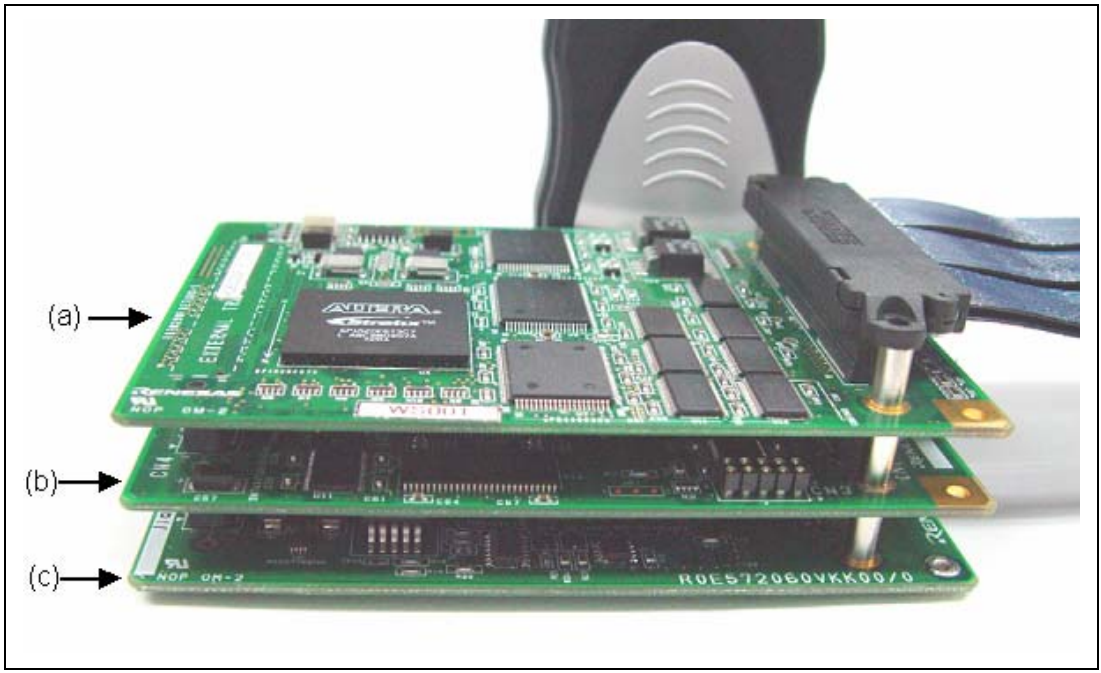


Figure 2.8 Connecting the External Bus Trace Unit, Emulation Memory Unit, and EV-chip Unit

⚠ CAUTION

Check the orientation of pin 1 and the position of each unit before connecting parts.

2.2.6 Connecting the EV-chip Unit to the User System

- After checking the location of pin 1, connect the EV-chip unit to the user system.

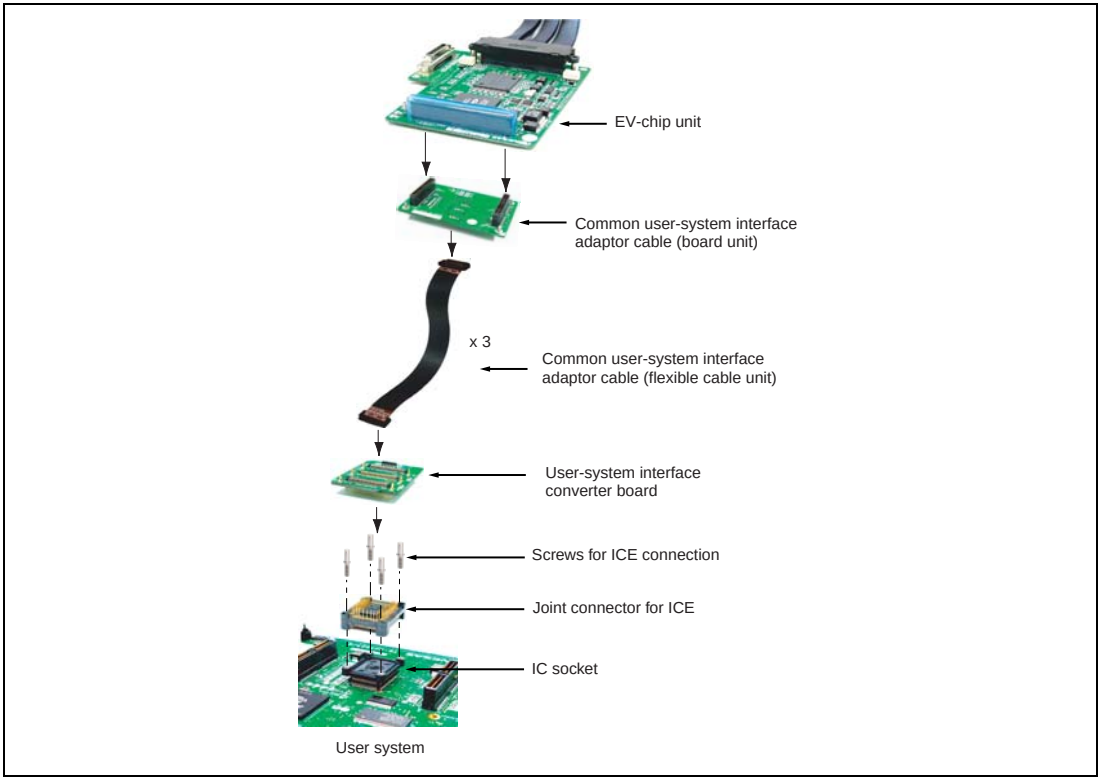


Figure 2.9 Connecting the User System Interface Board to the EV-chip Unit

⚠ CAUTION

Check the orientation of pin 1 before connecting parts.

Note: For the method to connect the user-system interface converter board to the user system, refer to the user-system interface converter board user's manual for each MCU.

2.2.7 Using the E200F Emulator as a Stand-Alone Unit

- If you are using the E200F emulator unit without connecting it to a user system, refer to table 1.3 in section 1.2, System Configuration, and make connections as shown in figure 2.10 until the EV-chip unit becomes available.

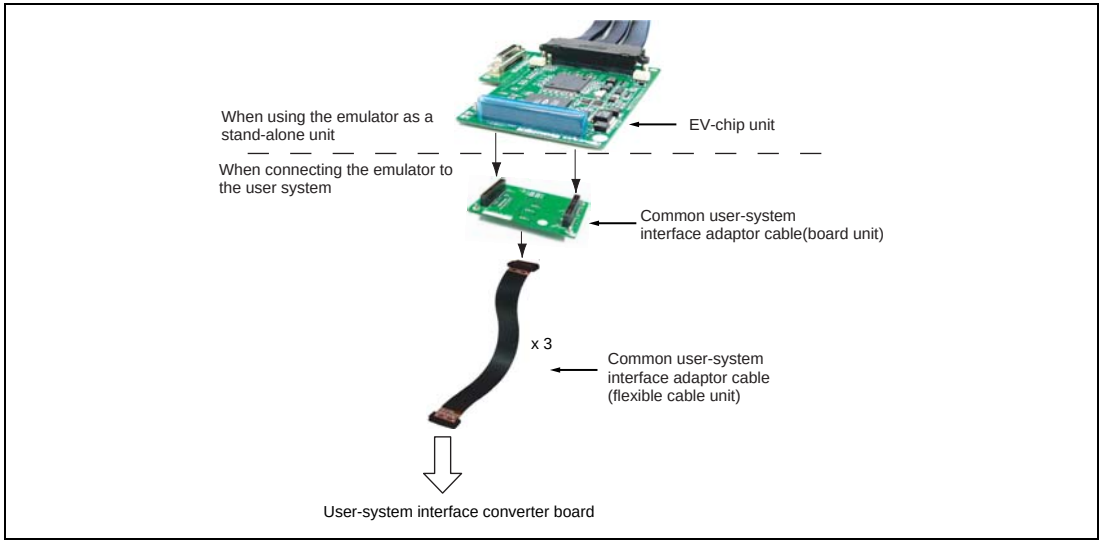


Figure 2.10 Connecting the E200F Emulator as a Stand-Alone Unit

2.3 Connecting the Emulator to the User System by Using the H-UDI Port Connector

To connect the E200F emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MCU.

It is impossible to connect the emulator to the 14-pin type connector that is recommended for the E10A-USB emulator. The 36-pin type connector is the same as that of the E10A-USB emulator. When designing the user system, read the E200F emulator user's manual and hardware manual for the related device.

Table 2.1 shows the type number of the emulator, the corresponding connector type, and the use of AUD function.

Table 2.1 Type Number, AUD Function, and Connector Type

Type Number	Connector	AUD Function
R0E200F1EMU00	14-pin connector	Not available
R0E200F1EMU00	36-pin connector	Available

The H-UDI port connector has the 36-pin and 14-pin types as described below. Use the 36-pin connector when using the emulator.

1. 36-pin type (with AUD function)
   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)
   The AUD trace function cannot be used because only the H-UDI function is supported. This connector type is not available for the emulator. Use the E10A-USB emulator.

2.4 Installing the H-UDI Port Connector on the User System

Table 2.2 shows the recommended H-UDI port connectors for the emulator.

Table 2.2 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type

Note: When designing the 36-pin connector layout on the user board, do not connect any components under the H-UDI connector.

2.5 Pin Assignments of the H-UDI Port Connector

Figure 2.11 shows the pin assignments of the 36-pin H-UDI port connectors.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following page differ from those of the connector manufacturer.

Pin No.	Signal	Input/ Output*1	Note	Pin No.	Signal	Input/ Output*1	Note
1	AUDCK	Output		19	TMS	Input	
2	GND	——		20	GND	——	
3	AUDATA0	Output		21	_TRST*2	Input	
4	GND	——		22	(GND)*4	——	
5	AUDATA1	Output		23	TDI	Input	
6	GND	——		24	GND	——	
7	AUDATA2	Output		25	TDO	Output	
8	GND	——		26	GND	——	
9	AUDATA3	Output		27	_ASEBRKAK /_ASEBRK*2	Input/ output	
10	GND	——		28	GND	——	
11	_AUDSYNC*2	Output		29	UVCC	Output	
12	GND	——		30	GND	——	
13	N.C.	——		31	_RES*2	Output	User reset
14	GND	——		32	GND	——	
15	N.C.	——		33	GND*3	Output	
16	GND	——		34	GND	——	
17	TCK	Input		35	N.C.	——	
18	GND	——		36	GND	——	

Notes: 1. Input to or output from the user system.
2. The symbol (_) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
4. When the H-UDI/AUD probe is connected to this pin and the ASEMD0# pin is set to 0, do not connect to GND but to the ASEMD0# pin directly.

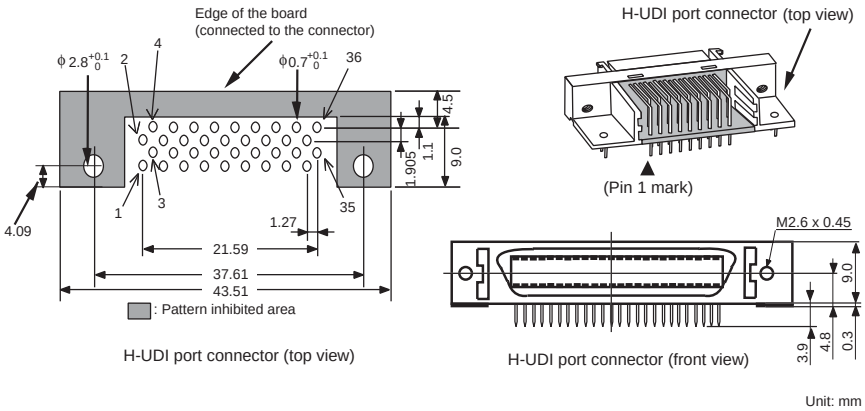


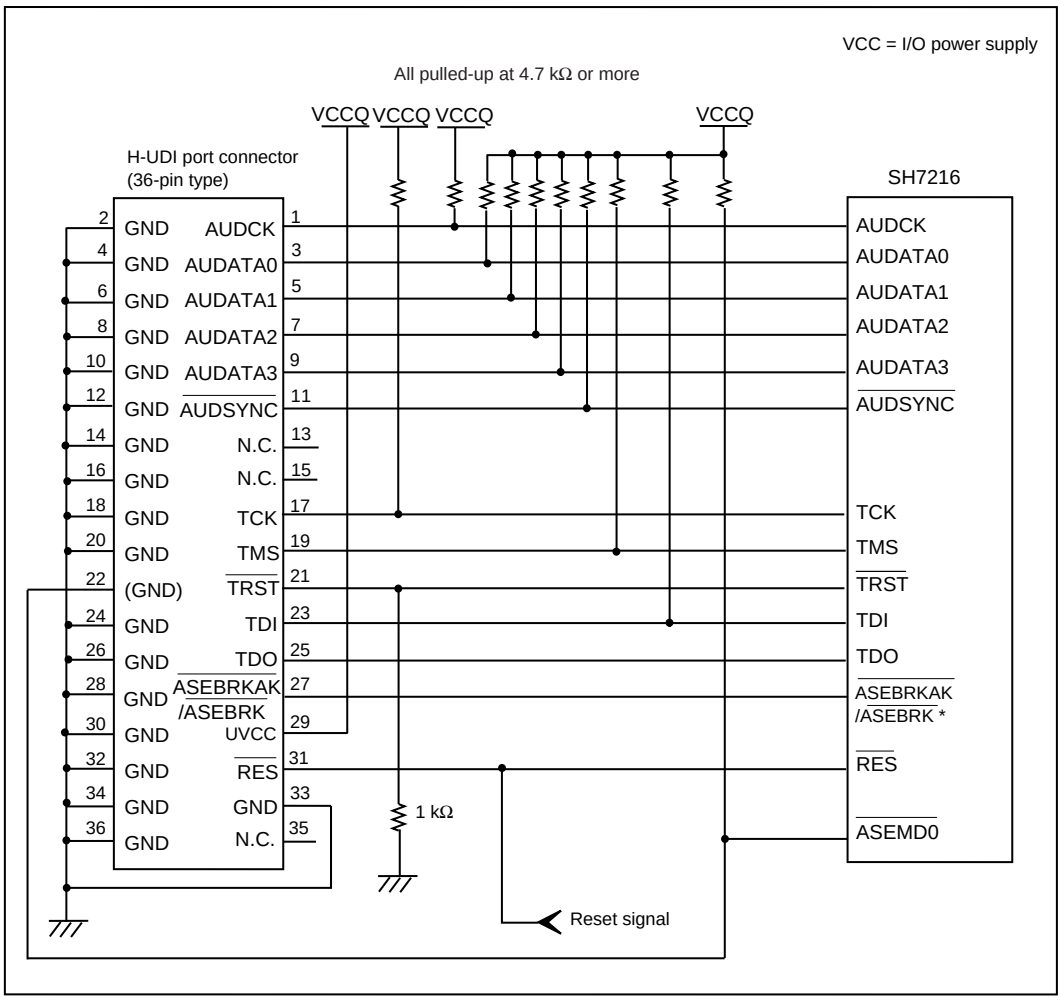
Figure 2.11 Pin Assignments of the H-UDI Port Connector (36 Pins)

2.6 Recommended Circuit between the H-UDI Port Connector and the MCU

2.6.1 Recommended Circuit (36-Pin Type)

Figure 2.12 shows recommended circuits for connection between the H-UDI and AUD port connectors (36 pins) and the MCU when the emulator is in use.

Notes:
1. Do not connect anything to the N.C. pins of the H-UDI port connector.
2. The ASEMD0# pin must be 0 when the emulator is connected and 1 when the emulator is not connected, respectively.
   (1) When the emulator is used: ASEMD0# = 0
   (2) When the emulator is not used: ASEMD0# = 1
   Figure 2.12 shows examples of circuits that allow the ASEMD0# pin to be GND (0) whenever the emulator is connected by using the H-UDI/AUD probe. When the ASEMD0# pin is changed by switches, etc., ground pin 22. Do not connect this pin to the ASEMD0# pin.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The pattern between the H-UDI port connector and the MCU must be as short as possible. Do not connect the signal lines to other components on the board.
5. The AUD signals (AUDCK, AUDATA3 to AUDATA0, and _AUDSYNC) operate in high speed. Isometric connection is needed if possible. Do not separate connection nor connect other signal lines adjacently.
6. Supply the operating voltages of the H-UDI and AUD of the MCU to the UVCC pin.
7. The resistance values shown in figure 2.12 are for reference.
8. For the AUDCK pin, guard the pattern between the H-UDI port connector and the MCU at GND level.
9. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MCU.



Note: The ASEBRKAK#/ASEBRK# pin (I/O pin) is multiplexed with the FWE pin (input pin). For the pin processing when the emulator is used and the user system is independently in operation, pins must be pulled up at 4.7 kΩ or more or pulled down at 100 kΩ. For the pin processing when the emulator is not used, refer to the hardware manual of the related MCU.

Figure 2.12 Recommended Circuit for Connection between the H-UDI Port Connector and MCU when the Emulator is in Use (36-Pin Type)

2.7 Using the IC Socket to Mount an MCU on the User System

Figure 2.13 shows an example of the external appearance of the configuration when the IC socket is used to mount an MCU on the user system using and the E200F emulator is connected in on-chip debugging mode.

(1) External appearance of the configuration of the on-chip connection when the IC socket is used for the SH7214 and SH7216 group.

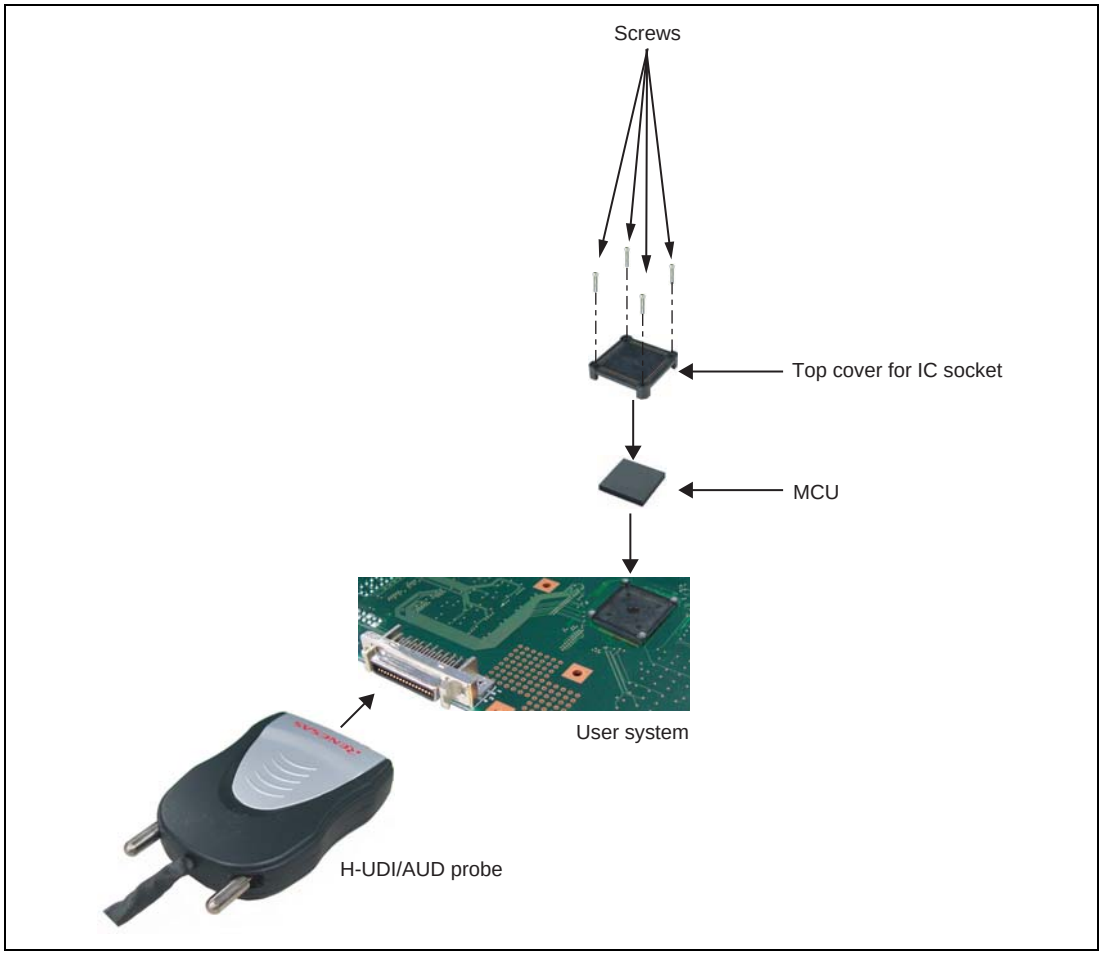


Figure 2.13 External Appearance of the Configuration of the On-Chip Connection when the IC Socket is Used for the SH7214 and SH7216 Group

⚠ CAUTION

1. **Check the orientation of pin 1 before connecting parts.**
2. **We recommend the following IC socket products.**

— IC socket for SH7214 and SH7216 group
(package: PLQP0176KB-A, former package: FP-176EV)
IC socket: NQPACK176SD-ND socket
(manufactured by Tokyo Eletech Corporation)
Top cover for IC socket: HQPACK176SD cover
(manufactured by Tokyo Eletech Corporation)

— IC socket for SH7214 and SH7126 group
(package: PLQP0176LB-A, former package: FP-176AV)
IC socket: NQPACK176SE socket
(manufactured by Tokyo Eletech Corporation)
Top cover for IC socket: HQPACK176SE cover
(manufactured by Tokyo Eletech Corporation)

Section 3 Software Specifications when Using the SH7214 and SH7216 Group

3.1 Differences between the MCU and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 3.1. The initial values of the MCU are undefined. When the emulator is initiated from the workspace, a value to be entered is saved in a session.

Table 3.1 Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	Value of the SP in the power-on reset vector table
PC	Value of the PC in the power-on reset vector table
SR	H'000000F0
GBR	H'00000000
VBR	H'00000000
TBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000

Note: When a value of the interrupt mask bit in the SR register is changed in the [Registers] window, it is actually reflected in that register immediately before execution of the user program is started. It also applies when the value is changed by the REGISTER_SET command.

2. The emulator uses the H-UDI; do not access the H-UDI.
3. Low-Power States (Sleep, Software Standby, and Module Standby)
   - When the emulator is used, the sleep state can be cleared with either the clearing function or with the [STOP] button, and a break will occur.
   - The memory must not be accessed or modified in software standby state.
   - Do not stop inputting the clock to the H-UDI module by using the module standby function.

4. Reset Signals

   The MCU reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the MCU.

Note: Do not break the user program when the _RES, _BREQ, or _WAIT signal is being low. A TIMEOUT error will occur. If the _BREQ or _WAIT signal is fixed to low during break, a TIMEOUT error will occur at memory access.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   During execution of the user program, memory is accessed by the following two methods, as shown in table 3.2.

Table 3.2 Memory Access during User Program Execution

Method	Description
H-UDI read/write	The stopping time of the user program is short because memory is accessed by the dedicated bus master.
Short break	This function is not available in this emulator. (Do not set)

The method for accessing memory during execution of the user program is specified by using the [Configuration] dialog box.

Table 3.3 Stopping Time by Memory Access (Reference)

Method	Condition	Stopping Time
H-UDI read/write	Reading of one longword for the internal RAM	Reading: Maximum three bus clock cycles (Bϕ)
	Writing of one longword for the internal RAM	Writing: Maximum two bus clock cycles (Bϕ)

7. Memory Access to the External Flash Memory Area

   The emulator can download the load module to the external flash memory area (for details, refer to section 6.21, Download Function to the Flash Memory Area, in the SH-2A, SH-2 E200F Emulator User's Manual). Neither memory write nor BREAKPOINT setting is enabled for the external flash memory area. To set the break condition for the program on the external flash memory, use the Event Condition function. Some MCUs will incorporate no external flash memory area.

8. ROM Cache

   For ROM cache in the MCU, the emulator operates as shown in table 3.4.

Table 3.4 Operation for ROM Cache

Function	Operation
Write and erase	Writes or erases all contents of ROM cache.
Memory read	Accesses the disabled cache area to read the content of internal flash memory.

9. Multiplexing the AUD Pins in On-Chip Debugging Mode

   The AUD pins are multiplexed as shown in table 3.5.

Table 3.5 Multiplexed Functions

MCU	Function 1	Function 2
SH7214 and SH7216 group	FWE	_ASEBRKAK/_ASEBRK
	PD16/D16/IRQ0/POE0/UBCTRG	AUDATA0
	PD17/D17/IRQ1/POE4/ADTRG	AUDATA1
	PD18/D18/IRQ2/MDIO	AUDATA2
	PD19/D19/IRQ3/LNKSTA	AUDATA3
	PD21/D21/IRQ5/TEND1/EXOUT	AUDCK
	PD20/D20/IRQ4/AUDSYNC/MDC	_AUDSYNC

Note: Function 1 can be used when the AUD pins of the device are not connected to the emulator.

The AUD pins are multiplexed with other pins. When the AUD function is used by the SH7214 and SH7216 E200F emulator, AUD pins are used regardless of the settings of the pin function controller (PFC).

Note that the AUD function can be used regardless of the above AUD pin settings in EV-chip unit debugging mode.

10. Using the Watchdog Timer (WDT)

    The WDT does not operate during a break.

11. Loading Sessions

    Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be 10 MHz.

12. [IO] Window

    — Display and modification

    For each watchdog timer register, there are two registers to be separately used for write and read operations.

Table 3.6 Watchdog Timer Register

Register Name	Usage	Register
WTCSR(W)	Write	Watchdog timer control/status register
WTCNT(W)	Write	Watchdog timer counter
WTCSR(R)	Read	Watchdog timer control/status register
WTCNT(R)	Read	Watchdog timer counter
WRCSR(W)	Write	Watchdog reset control/status register
WRCSR(R)	Read	Watchdog reset control/status register

— Customization of the I/O-register definition file

The internal I/O registers can be accessed from the [IO] window. However, note the following when accessing the SDMR register of the bus state controller. Before accessing the SDMR register, specify addresses to be accessed in the I/O-register definition file (R5F72145BDF.io, R5F72146BDF.io, R5F72147BDF.io, R5F72145BDB.io, R5F72146BDB.io, R5F72147BDB.io, R5F72145ADF.io, R5F72146ADF.io, R5F72147ADF.io, R5F72145ADB.io, R5F72146ADB.io, R5F72147ADB.io, R5F72165BDF.io, R5F72166BDF.io, R5F72167BDF.io, R5F72165BDB.io, R5F72166BDB.io, R5F72167BDB.io, R5F72165ADF.io, R5F72166ADF.io, R5F72167ADF.io, R5F72165ADB.io, R5F72166ADB.io, R5F72167ADB.io) and then activate the High-performance Embedded Workshop. After the I/O-register definition file is created, the MCU's specifications may be changed. If each I/O register in the I/O-register definition file differs from addresses described in the hardware manual, change the I/O-register definition file according to the description in the hardware manual. The I/O-register

definition file can be customized in accordance to its format. However, the emulator does not support the bit-field function.

— Verification

In the [IO] window, the input values cannot be verified.

13. Illegal Instructions

Do not execute illegal instructions with STEP-type commands.

14. Reset Input

During execution of the user program, the emulator may not operate correctly if a contention occurs between the following operations for the emulator and the reset input to the target device:

— Setting an Event Condition
— Setting an internal trace
— Displaying the content acquired by an internal trace
— Reading or writing of a memory

Note that those operations should not contend with the reset input to the target device.

15. Contention between the Change of the FRQCR Register and the Debugging Functions

The following notes are required for the user program for changing the multiplication rate of PLL circuit 1 to change the frequency:

— Avoid contention between the change of the FRQCR register in the user program and the memory access from the [Memory] window, etc.
— When the automatic updating function is used in the [Monitor] window or [Watch] window, generate and set a break of Event Condition for an instruction immediately before changing the FRQCR register. Contention will be avoided by generating a break and executing the user program again.

For the change of the multiplication rate of PLL circuit 1 and the FRQCR register, refer to the hardware manual for the MCU.

16. MCU operation mode

Boot or the User boot mode is not supported in this emulator.

17. Access to the Data Flash Memory (FLD)

Do not access the FLD by an emulator operation during execution of a user program which is located in the CS area. Such access may lead to the FLD instruction fetch violation bit of the flash access status register (FASTAT) becoming set, indicating an FLD instruction violation.

18. Emulation of Programming and Erasure of the Internal Flash Memory

The setting of the FEW pins is ignored while the emulator is connected. The flash write enable bit (FWE) of the flash pin monitor register (FPMON) becomes undefined. Note this point if the bit is referred to during execution of the user program.

When the MCU is operating in mode 2 (MCU expansion mode) or in mode 3 (MCU single chip mode), writing and erasing of the internal flash memory by programs is possible. Thus, if emulation is to include writing or erasure of the internal flash memory, the MCU operating mode must be mode 2 (MCU expansion mode) or mode 3 (MCU single chip mode). Do not select mode 6 (user program mode) or mode 7 (USB boot mode and user program mode) while the emulator is connected.

Break processing is not possible during calls of the programs for writing and erasing the internal flash memory. Note that the following processing cannot be performed.

- STOP button
- Automatic updating and tool chip watching for the watch function
- Memory operations during emulation
- Profiling function
- Monitor function
- AUD trace function (non-realtime trace mode)

Do not set the breakpoint in a block of the internal flash memory that will be a target for writing or erasure.

For emulating programming or erasure of the internal flash memory, select the [Flash memory to PC] or [PC to flash memory, Flash memory to PC] item from the [Flash memory synchronization] dialog box; do not select the [Disable] or [PC to flash memory] items.

3.2 Specific Functions for the Emulator when Using the SH7214 and SH7216

In on-chip debugging mode, a reset must be input when the emulator is activated.

3.2.1 Event Condition Functions

The emulator is used to set event conditions for the following three functions:

- Break of the user program
- Internal trace
- Start or end of performance measurement

Table 3.7 lists the types of Event Condition.

Table 3.7 Types of Event Condition

Event Condition Type	Description
Address bus condition (Address)	Sets a condition when the address bus (data access) value or the program counter value (before or after execution of instructions) is matched.
Data bus condition (Data)	Sets a condition when the data bus value is matched. Byte, word, or longword can be specified as the access data size.
Bus state condition (Bus State)	There are two bus state condition settings: Bus state condition: Sets a condition when the data bus value is matched. Read/write condition: Sets a condition when the read/write condition is matched.
Count	Sets a condition when the other specified conditions are satisfied for the specified counts.
Reset point	A reset point is set when the count and the sequential condition are specified.
Action	Selects the operation when a condition (such as a break, a trace halt condition, a trace acquisition condition, or a trigger output) is matched.

Use the [Combination action(Sequential or PtoP)] dialog box to specify the sequential condition, the point-to-point operation of the internal trace, and the start or end of performance measurement.

Table 3.8 lists the combinations of conditions that can be set under Ch1 to Ch11 and the software trace.

Table 3.8 Dialog Boxes for Setting Event Conditions

		Function				
Dialog Box		Address Bus Condition (Address)	Data Bus Condition (Data)	Bus State Condition (Bus Status)	Count Condition (Count)	Action
[Event Condition 1]	Ch1	O	O	O	O	O (B, T1, and P)
[Event Condition 2]	Ch2	O	O	O	X	O (B, T1, and P)
[Event Condition 3]	Ch3	O	X	X	X	O (B and T2)
[Event Condition 4]	Ch4	O	X	X	X	O (B and T3)
[Event Condition 5]	Ch5	O	X	X	X	O (B and T3)
[Event Condition 6]	Ch6	O	X	X	X	O (B and T2)
[Event Condition 7]	Ch7	O	X	X	X	O (B and T2)
[Event Condition 8]	Ch8	O	X	X	X	O (B and T2)
[Event Condition 9]	Ch9	O	X	X	X	O (B and T2)
[Event Condition 10]	Ch10	O	X	X	X	O (B and T2)
[Event Condition 11]	Ch11	O (reset point)	X	X	X	X

Notes: 1. O: Can be set in the dialog box.
X: Cannot be set in the dialog box.

2. For the Action item,
B: Setting a break is enabled.
T1: Setting the trace halt and acquisition conditions are enabled for the internal trace.
T2: Setting the trace halt is enabled for the internal trace.
T3: Setting the trace halt and point-to-point is enabled for the internal trace.
P: Setting a performance-measurement start or end condition is enabled.

The [Event Condition 11] dialog box is used to specify the count of [Event Condition 1] and becomes a reset point when the sequential condition is specified.

Sequential Setting: Use the [Combination action(Sequential or PtoP)] dialog box to specify the sequential condition and the start or end of performance measurement.

Table 3.9 Conditions to Be Set

Classification	Item	Description
[Ch1, 2, 3] list box	Sets the sequential condition and the start or end of performance measurement using Event Conditions 1 to 3 and 11.	
	Don't care	Sets no sequential condition or the start or end of performance measurement.
	Break: Ch3-2-1	Breaks when a condition is satisfied in the order of Event Condition 3, 2, 1.
	Break: Ch3-2-1, Reset point	Breaks when a condition is satisfied in the order of Event Condition 3, 2, 1. Enables the reset point of Event Condition 11.
	Break: Ch2-1	Breaks when a condition is satisfied in the order of Event Condition 2, 1.
	Break: Ch2-1, Reset point	Breaks when a condition is satisfied in the order of Event Condition 2, 1. Enables the reset point.
	I-Trace stop: Ch3-2-1	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 3, 2, 1.
	I-Trace stop: Ch3-2-1, Reset point	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 3, 2, 1. Enables the reset point.
	I-Trace stop: Ch2-1	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 2, 1.
	I-Trace stop: Ch2-1, Reset point	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 2, 1. Enables the reset point.

Table 3.9 Conditions to Be Set (cont)

Classification	Item	Description
[Ch1, 2, 3] list box (cont)	Ch2 to Ch1 PA	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 2 (start condition) to the satisfaction of the condition set in Event Condition 1 (end condition).
	Ch1 to Ch2 PA	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 1 (start condition) to the satisfaction of the condition set in Event Condition 2 (end condition).
[Ch4, 5] list box	Sets the point-to-point of the internal trace (the start or end condition of trace acquisition) using Event Conditions 4 and 5.	
	Don't care	Sets no start or end condition of trace acquisition.
	I-Trace: Ch5 to Ch4 PtoP	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition).
	I-Trace: Ch5 to Ch4 PtoP, Power-on reset	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition) or the power-on reset.

Notes: 1. After the sequential condition and the count specification condition of Event Condition 1 have been set, break and trace acquisition will be halted if the sequential condition is satisfied for the specified count.

2. If a reset point is satisfied, the satisfaction of the condition set in Event Condition will be disabled. For example, if the condition is satisfied in the order of Event Condition 3, 2, reset point, 1, the break or trace acquisition will not be halted. If the condition is satisfied in the order of Event Condition 3, 2, reset point, 3, 2, 1, the break and trace acquisition will be halted.
3. If the start condition is satisfied after the end condition of the performance measurement has been satisfied, performance measurement will be restarted. For the measurement result after a break, the measurement results during performance measurement are added.
4. If the start condition is satisfied after the end condition has been satisfied by the point-to-point of the internal trace, trace acquisition will be restarted.

Usage Example of Sequential Break Extension Setting: A tutorial program provided for the product is used as an example. For the tutorial program, refer to section 6, Tutorial, in the SH-2A, SH-2 E200F Emulator User's Manual.

The conditions of Event Condition are set as follows:

1. Ch1

   Breaks address H'00001086 when the condition [Prefetch address break after executing] is satisfied.
2. Ch2

   Breaks address H'00001068 when the condition [Prefetch address break after executing] is satisfied.
3. Ch3

   Breaks address H'00001058 when the condition [Prefetch address break after executing] is satisfied.

   Note: Do not set other channels.
4. Sets the contents of the [Ch1,2,3] list box to [Break: Ch 3-2-1] in the [Combination action] dialog box.

Then, set the program counter and stack pointer (PC = H'00000800, R15 = H'FFF9F000) in the [Registers] window and click the [Go] button. If this does not execute normally, issue a reset and execute the above procedures.

The program is executed up to the condition of Ch1 and halted. Here, the condition is satisfied in the order of Ch3 -> 2 -> 1.

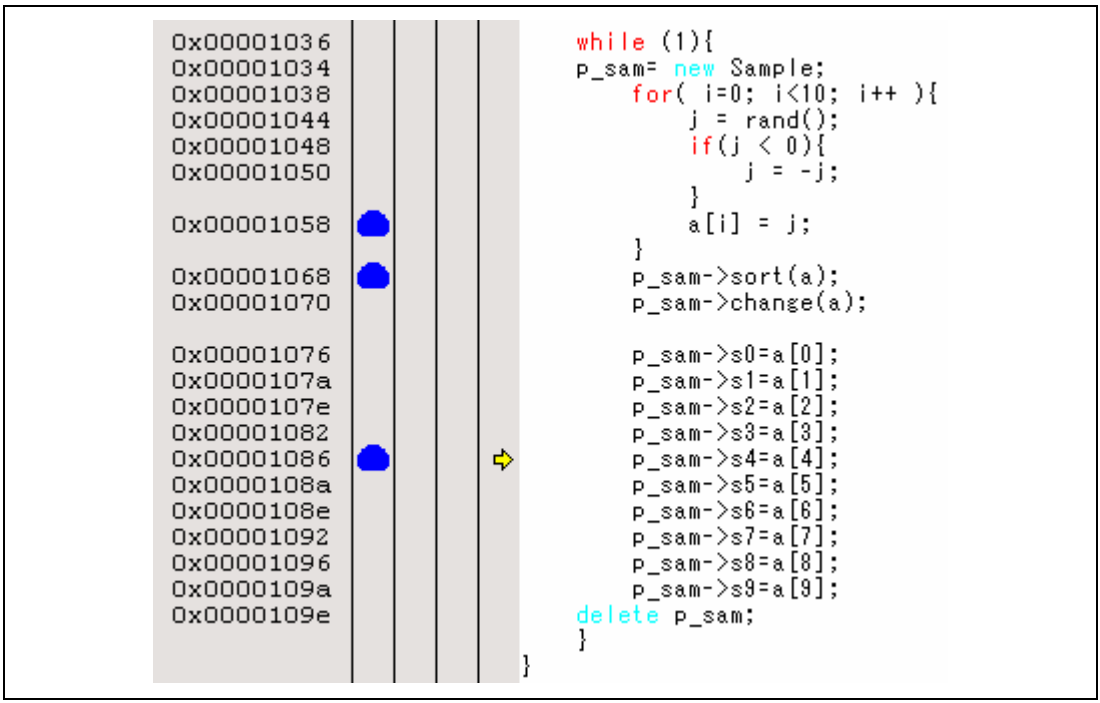


Figure 3.1 [Source] Window at Execution Halt (Sequential Break)

If the sequential condition, performance measurement start/end, or point-to-point for the internal trace is set, conditions of Event Condition to be used will be disabled. Such conditions must be enabled from the popup menu by clicking the right mouse button on the [Event Condition] sheet.

Notes: 1. If the Event condition is set for the slot in the delayed branch instruction by the program counter (after execution of the instruction), the condition is satisfied before executing the instruction in the branch destination (when a break has been set, it occurs before executing the instruction in the branch destination).

2. Do not set the Event condition for the SLEEP instruction by the program counter (after execution of the instruction).
3. When the Event condition is set for the 32-bit instruction by the program counter, set that condition in the upper 16 bits of the instruction.
4. If the power-on reset and the Event condition are matched simultaneously, no condition will be satisfied.
5. Do not set the Event condition for the DIVU or DIVS instruction by the program counter (after execution of the instruction).

6. If a condition of which intervals are satisfied closely is set, no sequential condition will be satisfied.
   - Set the Event conditions, which are satisfied closely, by the program counter with intervals of two or more instructions.
   - After the Event condition has been matched by accessing data, set the event condition by the program counter with intervals of 17 or more instructions.
7. If the settings of the Event condition or the sequential conditions are changed during execution of the program, execution will be suspended. (The number of clock cycles to be suspended during execution of the program is a maximum of about 102 bus clock cycles (Bϕ). If the bus clock (Bϕ) is 20 MHz, the program will be suspended for 5.1 μs.)
8. If the settings of Event conditions or the sequential conditions are changed during execution of the program, the emulator temporarily disables all Event conditions to change the settings. During this period, no Event conditions will be satisfied.
9. If the break condition before executing an instruction is set to the instruction followed by DIVU and DIVS, the factor for halting a break will be incorrect under the following condition:
   If a break occurs during execution of the above DIVU and DIVS instructions, the break condition before executing an instruction, which has been set to the next instruction, may be displayed as the factor for halting a break.
10. If the break conditions before and after executing instructions are set to the same address, the factor for halting a break will be incorrectly displayed. The factor for halting a break due to the break condition after executing an instruction will be displayed even if a break is halted by the break condition before executing an instruction.
11. Do not set the break condition after executing instructions and BREAKPOINT (software break) to the same address.
12. When the emulator is being connected, the user break controller (UBC) function is not available.

3.2.2 Trace Functions

The emulator supports the trace functions listed in table 3.10.

Table 3.10 Trace Functions

Function	Internal Trace	AUD Trace
Branch trace	Supported	Supported
Memory access trace	Supported	Supported
Software trace	Not supported	Supported

The internal and AUD traces are set in the [I-Trace/AUD-Trace acquisition] dialog box of the [Trace] window.

Internal Trace Function: When [I-Trace] is selected for [Trace type] on the [Trace mode] page of the [I-Trace/AUD-Trace acquisition] dialog box, the internal trace can be used.

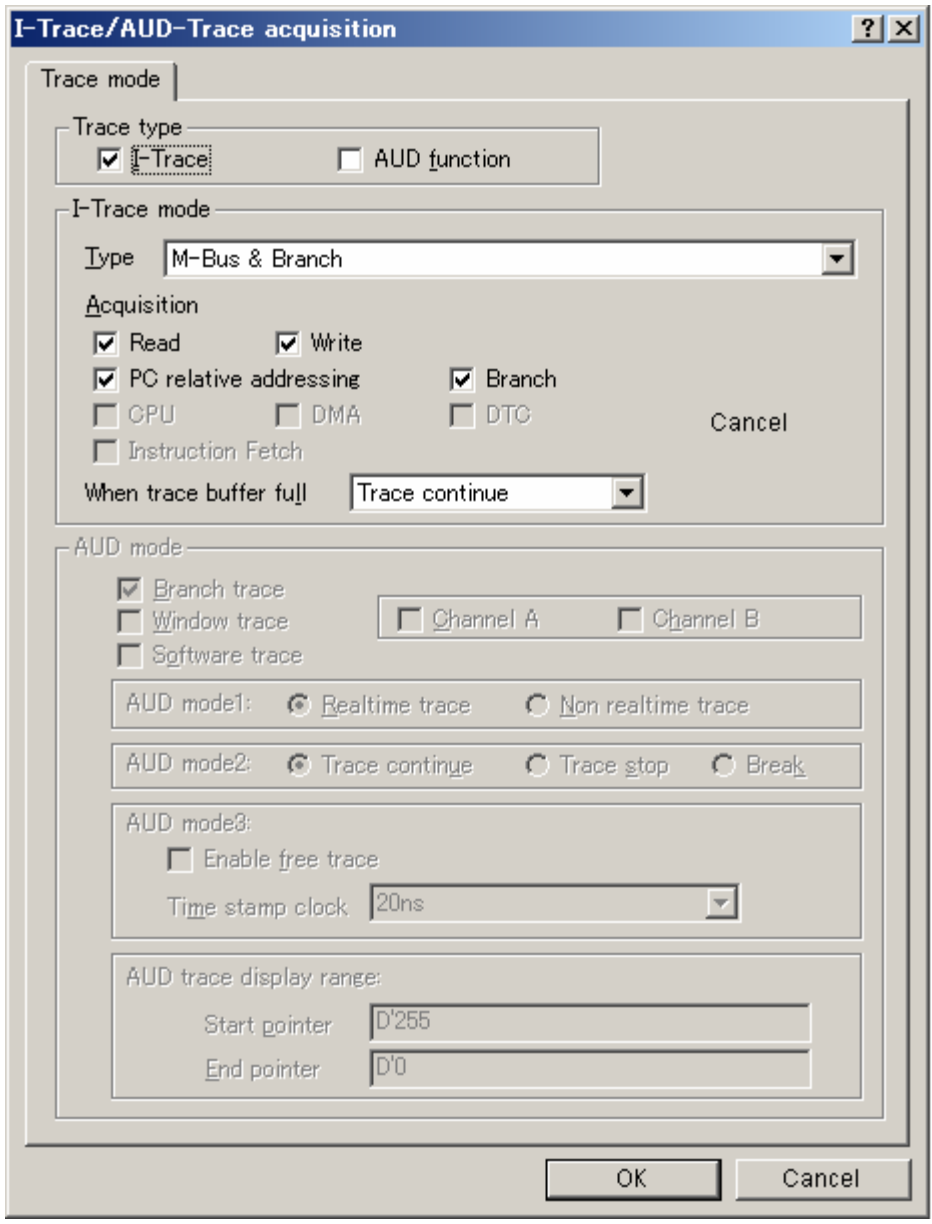


Figure 3.2 [I-Trace/AUD-Trace acquisition] Dialog Box (Internal Trace Function)

The following three items can be selected as the internal trace from [Type] of [I-Trace mode].

Table 3.11 Information on Acquiring the Internal Trace

Item	Acquisition Information
[M-Bus & Branch]	Acquires the data and branch information on the M-bus. • Data access (read/write) • PC-relative access • Branch information
[I-Bus]	Acquires the data on the I-bus. • Data access (read/write) • Selection of the bus master on the I-bus (CPU/DMA/DTC) • Instruction fetch
[I-Bus, M-Bus & Branch]	Acquires the contents of [M-Bus & Branch] and [I-Bus].

After selecting [Type] of [I-Trace mode], select the contents to be acquired from [Acquisition]. Typical examples are described below (note that items disabled for [Acquisition] are not acquired).

- Example of acquiring branch information only:
  Select [M-Bus & Branch] from [Type] and enable [Branch] on [Acquisition].
- Example of acquiring the read or write access (M-bus) only by the user program:
  Select [M-Bus & Branch] from [Type] and enable [Read], [Write], and [Data access] on [Acquisition].
- Example of acquiring the read access only by DMAC (I-bus):
  Select [I-Bus] from [Type] and enable [Read], [DMA], and [Data access] on [Acquisition].

Using the Event Condition restricts the condition; the following three items are set as the internal trace conditions.

Table 3.12 Trace Conditions of the Internal Trace

Item	Acquisition Information
Trace halt	Acquires the internal trace until the Event Condition is satisfied. (The trace content is displayed in the [Trace] window after a trace has been halted. No break occurs in the user program.)
Trace acquisition	Acquires only the data access where the Event Condition is satisfied.
Point-to-point	Traces the period from the satisfaction of Event Condition 5 to the satisfaction of Event Condition 4.

To restrict trace acquisition to access only a specific address or specific function of a program, an Event Condition can be used. Typical examples are described below.

- Example of halting a trace with a write access (M-bus) to H'FFF80000 by the user program as a condition (trace halt):

  Set the condition to be acquired on [I-Trace mode].

  Set the following in the [Event Condition 1] or [Event Condition 2] dialog box:

  Address condition: Set [Address] and H'FFF80000.

  Bus state condition: Set [M-Bus] and [Write].

  Action condition: Disable [Acquire Break] and set [Acquire Trace] for [Stop].

- Example of acquiring the write access (M-bus) only to H'FFF80000 by the user program (trace acquisition condition):

  Select [M-Bus & Branch] from [Type] and enable [Write] and [Data access] on [Acquisition].

  Set the following in the [Event Condition 1] or [Event Condition 2] dialog box:

  Address condition: Set [Address] and H'FFF80000.

  Bus state condition: Set [M-Bus] and [Write].

  Action condition: Disable [Acquire Break] and set [Acquire Trace] for [Condition].

For the trace acquisition condition, the condition to be acquired by the Event Condition should be acquired by setting the [I-Trace mode].

- Example of acquiring a trace for the period while the program passes H'1000 through H'2000 (point-to-point):

  Set the condition to be acquired on [I-Trace mode].

  Set the address condition as H'1000 in the [Event Condition 4] dialog box.

  Set the address condition as H'2000 in the [Event Condition 5] dialog box.

Set [I-Trace] as [Ch4 to Ch5 PtoP] in the [Combination action (Sequential or PtoP)] dialog box.

When point-to-point and trace acquisition condition are set simultaneously, they are ANDed.

Notes on Internal Trace:

- Timestamp

  The timestamp is the clock counts of Bϕ (48-bit counter). Table 3.13 shows the timing for acquiring the timestamp.

Table 3.13 Timing for the Timestamp Acquisition

Item	Acquisition Information	Counter Value Stored in the Trace Memory
M-bus data access		Counter value when data access (read or write) has been completed
Branch		Counter value when the next bus cycle has been completed after a branch
I-bus	Fetch	Counter value when a fetch has been completed
	Data access	Counter value when data access has been completed

- Point-to-point

  The trace-start condition is satisfied when the specified instruction has been fetched. Accordingly, if the trace-start condition has been set for the overrun-fetched instruction (an instruction that is not executed although it has been fetched at a branch or transition to an interrupt), tracing is started during overrun-fetching of the instruction. However, when overrun-fetching is achieved (a branch is completed), tracing is automatically suspended.
  If the start and end conditions are satisfied closely, trace information will not be acquired correctly.
  The execution cycle of the instruction fetched before the start condition is satisfied may be traced.
  When the I-bus is acquired, do not specify point-to-point.
  Memory access may not be acquired by the internal trace if it occurs at several instructions immediately before satisfaction of the point-to-point end condition.

- Halting a trace

  Do not set the trace-end condition for the SLEEP instruction and the branch instruction that the delay slot becomes the SLEEP instruction.

- Trace acquisition condition

  Do not set the trace-end condition for the SLEEP instruction and the branch instruction according to which the delay slot becomes the SLEEP instruction.
  When [I-BUS, M-Bus & Branch] is selected and the trace acquisition condition is set for the M-bus and I-bus with the Event Condition, set the M-bus condition and the I-bus condition for [Event Condition 1] and [Event Condition 2], respectively.
  If the settings of [I-Trace mode] are changed during execution of the program, execution will be suspended. (The number of clock cycles to be suspended during execution of the program is 66 bus clock cycles (Bϕ). If the bus clock (Bϕ) is 20 MHz, the program will be suspended for 3.3 μs.)

- Displaying a trace

  If a trace is displayed during execution of the program, execution will be suspended to acquire the trace information. (The number of clock cycles to be suspended during execution of the program is 24576 bus clock cycles (Bϕ). If the bus clock (Bϕ) is 20 MHz, the program will be suspended for 1228.8 μs.)

- Branch trace

  If breaks occur immediately after executing non-delayed branch and TRAPA instructions and generating a branch due to exception or interrupt, a trace for one branch will not be acquired immediately before such breaks.
  However, this does not affect on generation of breaks caused by a BREAKPOINT and a break before executing instructions of Event Condition.

- Writing memory immediately before generating a break

  If an instruction is executed to write memory immediately before generating a break, trace acquisition may not be performed.

AUD Trace Functions: This function is operational when the AUD pins of the MCU are connected to the emulator. Table 3.14 shows the AUD trace acquisition mode that can be set in each trace function.

Table 3.14 AUD Trace Acquisition Mode

Type	Mode	Description
Continuous trace occurs	Realtime trace	When the trace information is being generated intensely that the output from the AUD pin incapable of keeping up, the CPU temporarily suspends the output of trace information. Therefore, although the user program is run in real time, the acquisition of some trace information might not be possible.
	Non realtime trace	When trace information is being generated so intensely that the output from the AUD pin is incapable of keeping up, CPU operations are temporarily suspended and the output of trace information takes priority. In such cases, the realtime characteristics of the user program are lost.
Trace buffer full	Trace continue	This function writes the latest trace information on the oldest information to store the latest trace information.
	Trace stop	After the trace buffer becomes full, the trace information is no longer acquired. The user program is continuously executed.
	Break	A break occurs when the trace buffer becomes full.
AUD trace function used	Enable free trace	When this box is checked, the emulator ignores the AUD eventpoint setting and acquires all trace information.
	Time stamp clock	The resolution of the timer for timestamps can be specified. Select 20 ns, 100 ns, 400 ns, or 1.6 μs.

To set the AUD trace acquisition mode, click the [Trace] window with the right mouse button and select [Setting] from the pop-up menu to display the [I-Trace/AUD-Trace acquisition] dialog box. The AUD trace acquisition mode can be set in the [AUD mode1], [AUD mode2], or [AUD mode3] group box in the [Trace mode] page of the [I-Trace/AUD-Trace acquisition] dialog box.

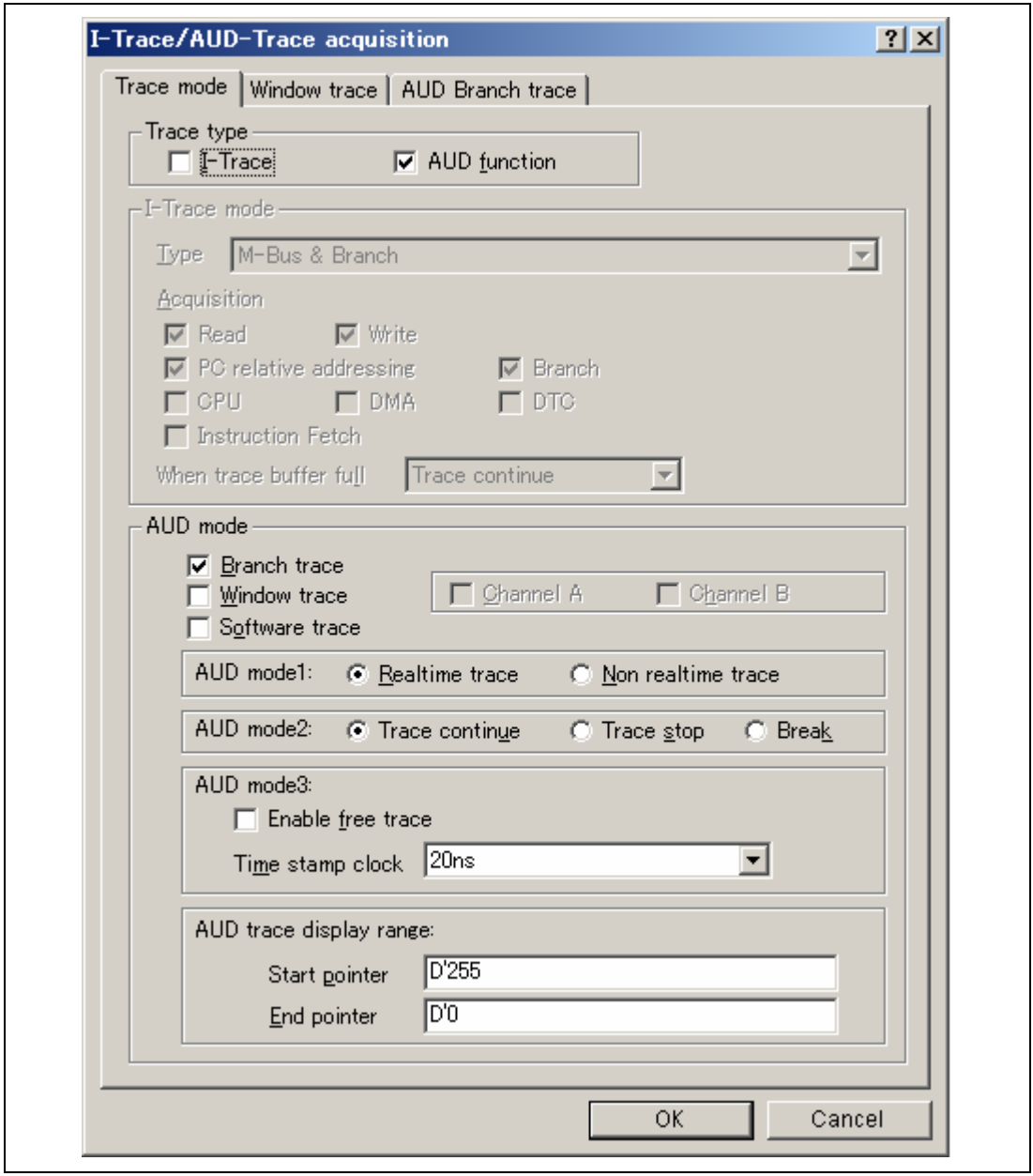


Figure 3.3 [Trace mode] Page

When the AUD trace function is used, select the [AUD function] radio button in the [Trace type] group box of the [Trace mode] page.

(a) Branch Trace Function

The branch source and destination addresses and their source lines are displayed.

Branch trace can be acquired by selecting the [Branch trace] check box in the [AUD function] group box of the [Trace mode] page.

The branch type can be selected in the [AUD Branch trace] page.

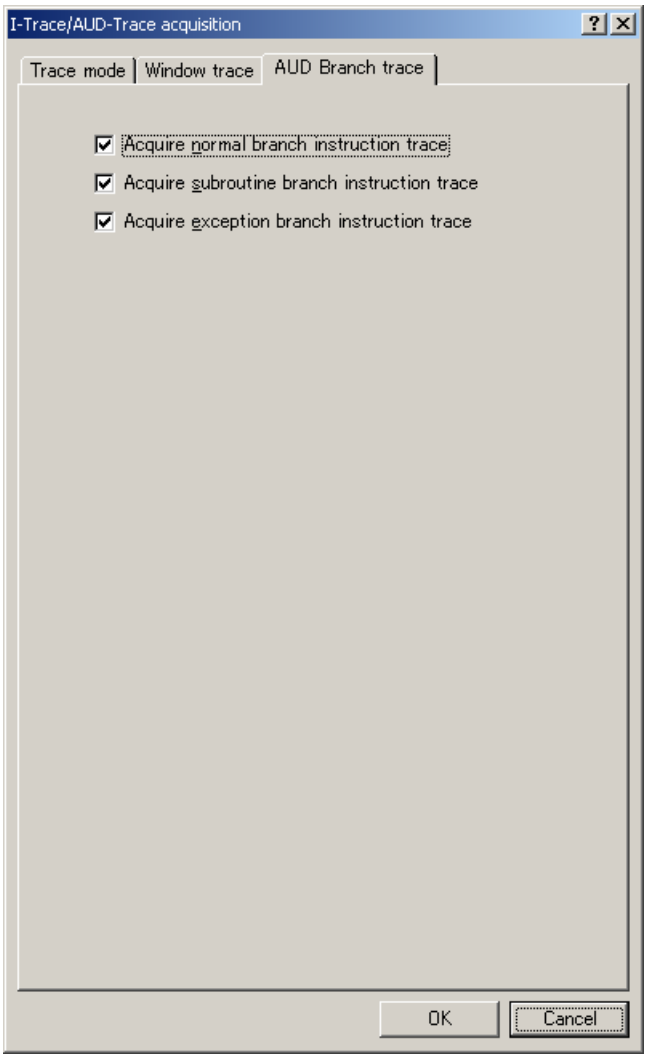


Figure 3.4 [AUD Branch trace] Page

(b) Window Trace Function

Memory access in the specified range can be acquired by trace.

Two memory ranges can be specified for channels A and B. The read, write, or read/write cycle can be selected as the bus cycle for trace acquisition.

Setting Method:

(i) Select the [Channel A] and [Channel B] check boxes in the [AUD function] group box of the [Trace mode] page. Each channel will become valid.

(ii) Open the [Window trace] page and specify the bus cycle and memory range that are to be set for each channel.

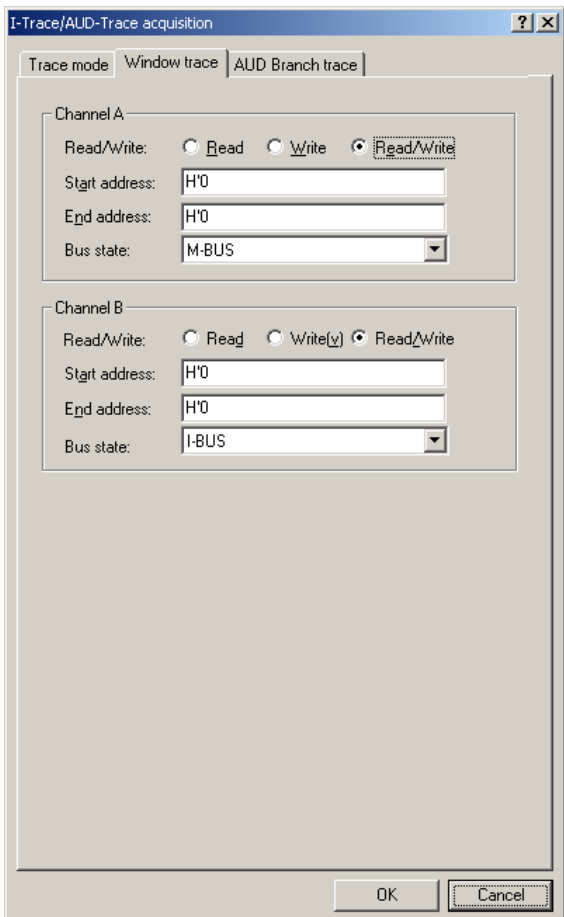


Figure 3.5 [Window trace] Page

Note: When [M-BUS] or [I-BUS] is selected, the following bus cycles will be traced.

- M-BUS: A bus cycle generated by the CPU is acquired.
- I-BUS: A bus cycle generated by the CPU or DMA is acquired.

(c) Software Trace Function

Note: This function can be supported with SuperH C/C++ compiler (manufactured by Renesas Technology Corp.; including OEM and bundle products) V7.0 or later.

When a specific instruction is executed, the PC value at execution and the contents of one general register are acquired by trace. Describe the Trace(x) function (x is a variable name) to be compiled and linked beforehand. For details, refer to the SuperH™ RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual.

When the load module is downloaded on the emulator and is executed while a software trace function is valid, the PC value that has executed the Trace(x) function, the general register value for x, and the source lines are displayed.

To activate the software trace function, select the [Software trace] check box in the [AUD function] group box of the [Trace mode] page.

Notes on AUD Trace:

1. When the trace display is performed during user program execution, the mnemonics, operands, or source is not displayed.
2. The AUD trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previous branch source address is the same for the upper 16 bits, the lower 16 bits are output. If it matches the upper 24 bits, the lower 8 bits are output. If it matches the upper 28 bits, the lower 4 bits are output.
   The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.
3. If the 32-bit address cannot be displayed, the source line is not displayed.
4. In the emulator, when multiple loops are performed to reduce the number of AUD trace displays, only the IP counts up.
5. In the emulator, the maximum number of trace displays is 262144 lines (131072 branches). However, the maximum number of trace displays differs according to the AUD trace information to be output. Therefore, the above pointers cannot always be acquired.
6. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.

7. The AUD trace is disabled while the profiling function is used.
8. If breaks occur immediately after executing non-delayed branch and TRAPA instructions and generating a branch due to exception or interrupt, a trace for one branch will not be acquired immediately before such breaks.
   However, this does not affect on generation of breaks caused by a BREAKPOINT and a break before executing instructions of Event Condition.
9. The value of [Data] is not appropriate in the trace result by the software trace (that value is appropriate in the window trace result.).

3.2.3 Notes on Using the JTAG (H-UDI) Clock (TCK) and AUD Clock (AUDCK)

1. Set the JTAG clock (TCK) frequency to less than the frequency of the SH7214 and SH7216 peripheral module clock (CKP) and 25 MHz or lower.
2. The initial value of the JTAG clock (TCK) is 10 MHz.
3. A value to be set for the JTAG clock (TCK) is initialized after executing [Reset CPU] or [Reset Go]. Thus the TCK value will be 10 MHz.
4. When debugging is performed without connecting the EV-chip unit, set the AUD clock (AUDCK) frequency to 25 MHz or lower. When debugging is performed with the EV-chip unit connected, set the AUD clock (AUDCK) frequency to 50 MHz or lower. If the higher frequency is input, the emulator will not operate normally.

3.2.4 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address.
   It cannot be set to the following addresses:
   — An area other than CS and the internal RAM
   — An instruction in which Event Condition 2 is satisfied
   — A slot instruction of a delayed branch instruction
3. During step operation, the specified BREAKPOINT and Event Condition breaks are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified and a break occurs before the Event Condition execution, single-step operation is performed at the address before execution resumes. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.

6. If a BREAKPOINT cannot be correctly set to an address in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the break condition, the mark ● disappears.
7. If you wish to use a BREAKPOINT (software break), specify the SH2A_SBSTK command to enable use of a user stack before setting a PC break. While enabled, extra four bytes of a user stack are used when a break occurs. The value of the stack pointer (R15) must be correctly set in advance because a user stack is to be used. By default, use of a user stack is disabled. For details on the command, refer to the help file.

- Example
  To enable use of a user stack:
  >SH2A_SBSTK enable

3.2.5 Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.

3.2.6 Performance Measurement Function

The emulator supports the performance measurement function.

1. Setting the performance measurement conditions
   To set the performance measurement conditions, use the [Performance Analysis] dialog box or the PERFORMANCE_SET command. When any line in the [Performance Analysis] window is clicked with the right mouse button, a popup menu is displayed and the [Performance Analysis] dialog box can be displayed by selecting [Setting].

Note: For the command line syntax, refer to the online help.

(a) Specifying the measurement start/end conditions

The measurement start/end conditions are specified by using Event Condition 1,2. The [Ch1,2,3] list box of the [Combination action] dialog box can be used.

Table 3.15 Measurement Period

Classification	Item	Description
Selection in the [Ch1, 2, 3] list box	Ch2 to Ch1 PA	The period from the satisfaction of the condition set in Event Condition 2 (start condition) to the satisfaction of the condition set in Event Condition 1 (end condition) is set as the performance measurement period.
	Ch1 to Ch2 PA	The period from the satisfaction of the condition set in Event Condition 1 (start condition) to the satisfaction of the condition set in Event Condition 2 (end condition) is set as the performance measurement period.
	Other than above	The period from the start of execution of the user program to the occurrence of a break is measured.

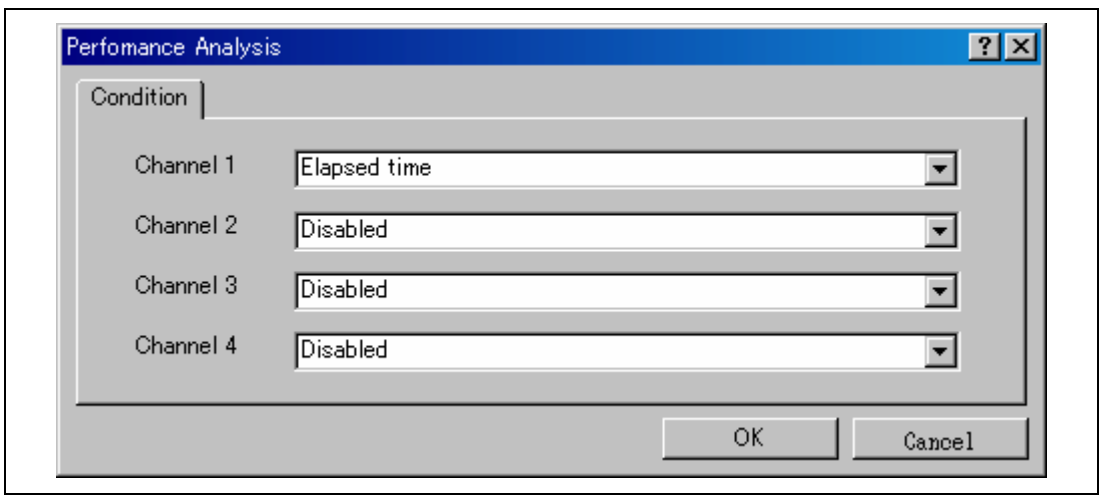


Figure 3.6 [Performance Analysis] Dialog Box

For measurement tolerance,

- The measured value includes tolerance.
- Tolerance will be generated before or after a break.

Note: When [Ch2 to Ch1 PA] or [Ch1 to Ch2 PA] is selected, to execute the user program, specify conditions set in Event Condition 2 and Event Condition 1 and one or more items for performance measurement.

(b) Measurement item

Items are measured with [Channel 1 to 4] in the [Performance Analysis] dialog box. Maximum four conditions can be specified at the same time. Table 3.16 shows the measurement items (Options in table 3.16 are parameters for <mode> of the PERFORMANCE_SET command. They are displayed for CONDITION in the [Performance Analysis] window).

Table 3.16 Measurement Item

Selected Name	Option
Disabled	None
Elapsed time	AC
Branch instruction counts	BT
Number of execution instructions	I
Number of execution 32bit-instructions	I32
Exception/interrupt counts	EA
Interrupt counts	INT
Data cache-miss counts	DC
Instruction cache-miss counts	IC
All area access counts	ARN
All area instruction access counts	ARIN
All area data access counts	ARND
Cacheable area access counts	CDN (data access)
Cacheable area instruction access counts	CIN
Non cacheable area data access counts	NCN
URAM area access counts	UN
URAM area instruction access counts	UIN
URAM area data access counts	UDN
Internal I/O area data access counts	IODN
Internal ROM area access counts	RN
Internal ROM area instruction access counts	RIN
Internal ROM area data access counts	RDN
All area access cycle	ARC
All area instruction access cycle	ARIC
All area data access cycle	ARDC
All area access stall	ARS
All area instruction access stall	ARIS
All area data access stall	ARDS

Notes: 1. In the non-realtime trace mode of the AUD trace, normal counting cannot be performed because the generation state of the stall or the execution cycle is changed.
2. If the internal ROM is not installed on the product, do not set the measurement item for the internal ROM area.
3. For SH7214 and SH7216 group, do not set measurement items for the cache-miss counts, cacheable area, or non-cacheable area.

2. Displaying the measured result

The measured result is displayed in the [Performance Analysis] window or the PERFORMANCE_ANALYSIS command in hexadecimal (32 bits).

Note: If a performance counter overflows as a result of measurement, "********" will be displayed.

3. Initializing the measured result

To initialize the measured result, select [Initialize] from the popup menu in the [Performance Analysis] window or specify INIT with the PERFORMANCE_ANALYSIS command.

Section 4 User System Interface Circuits

4.1 User System Interface Circuits

Figures 4.1 through 4.6 show user system interface circuits. Use them as a reference to determine the value of the pull-up resistance.

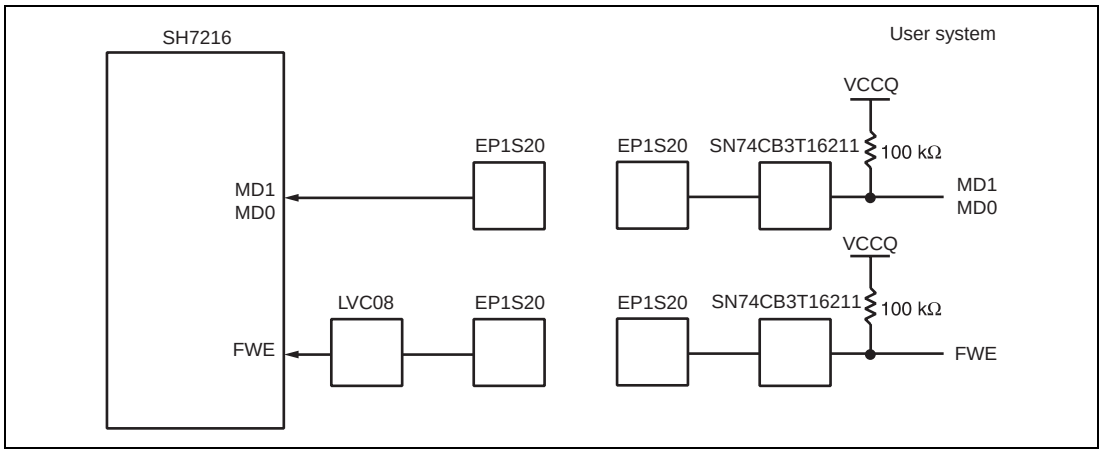


Figure 4.1 User System Interface Circuits (1)

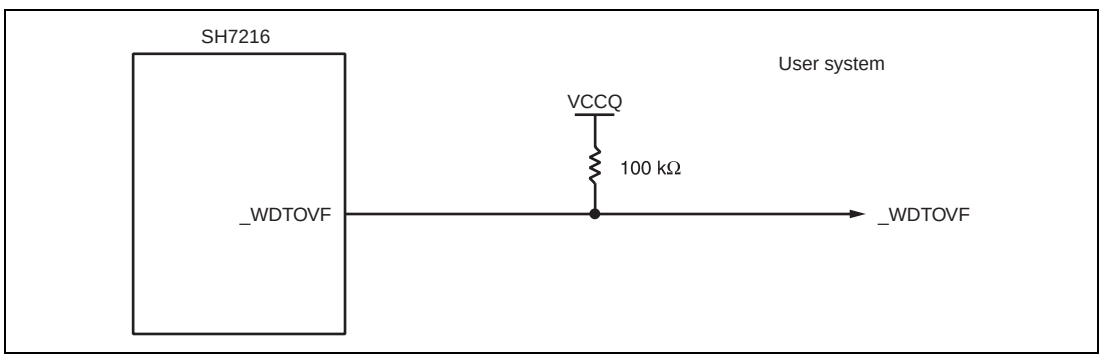


Figure 4.2 User System Interface Circuits (2)

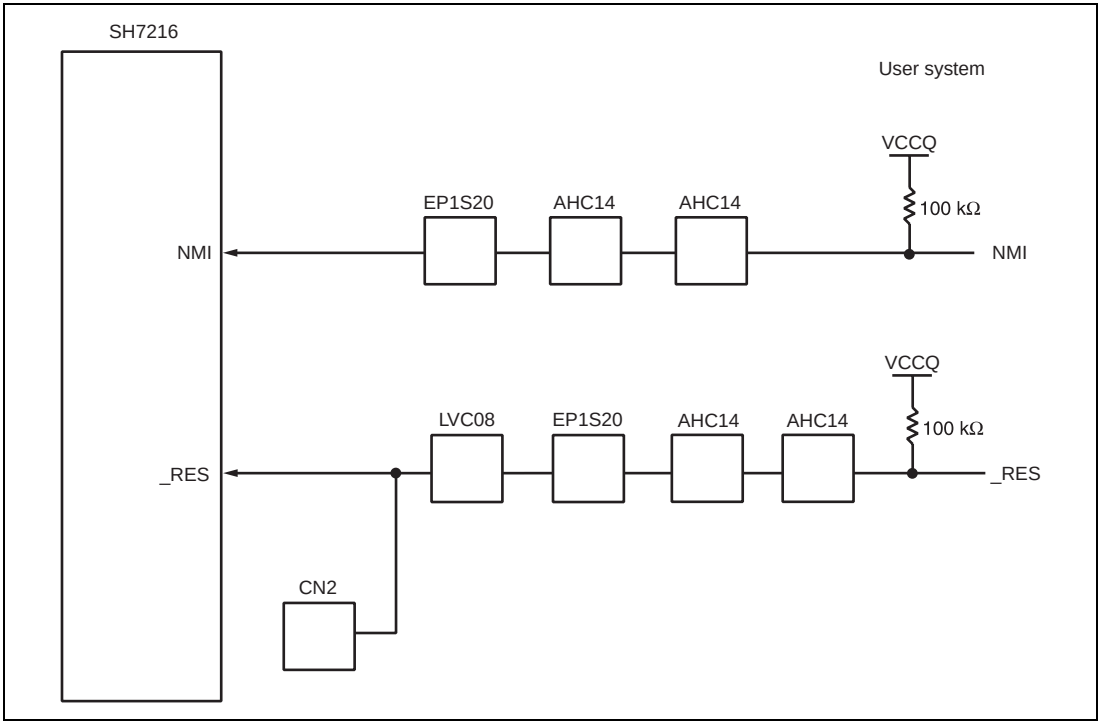


Figure 4.3 User System Interface Circuits (3)

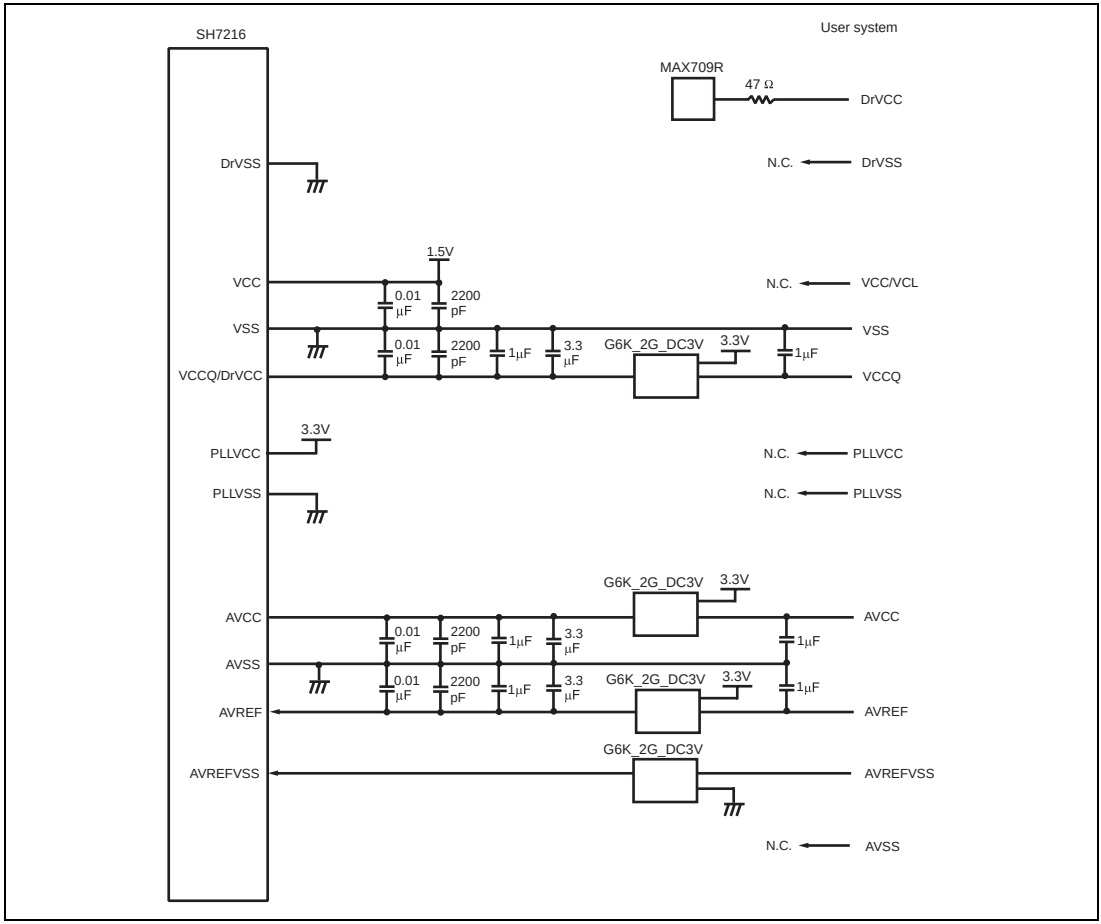


Figure 4.4 User System Interface Circuits (4)

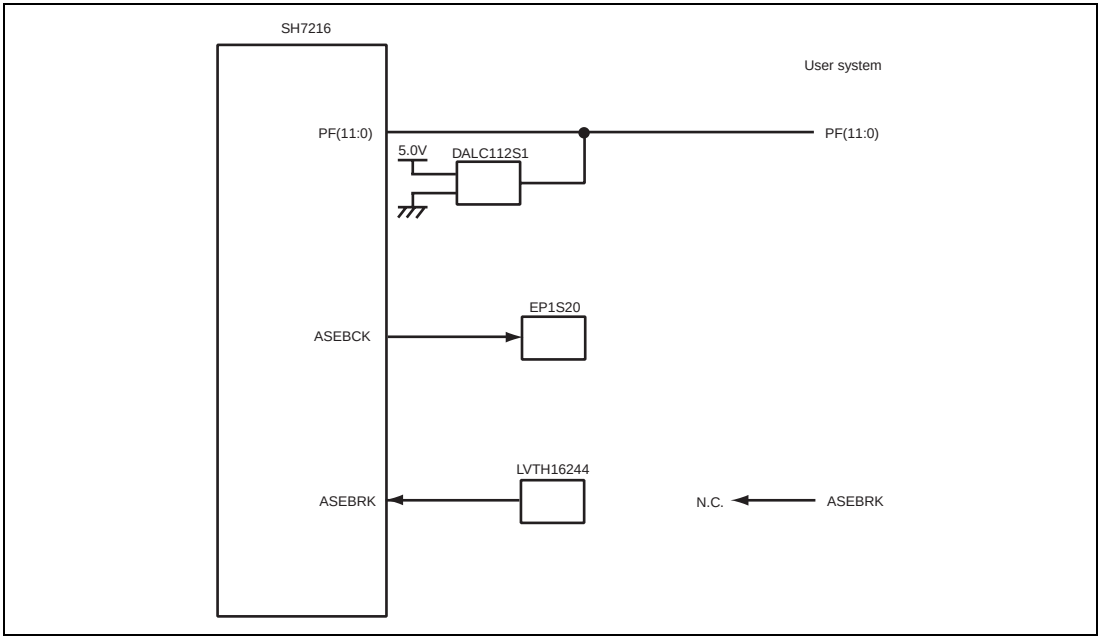


Figure 4.5 User System Interface Circuits (5)

Note: A part of port pin names shown in figure 4.5 may not be included in the pin assignment diagram of the SH7214 and SH7216 group. These pins are not connected to the user system.

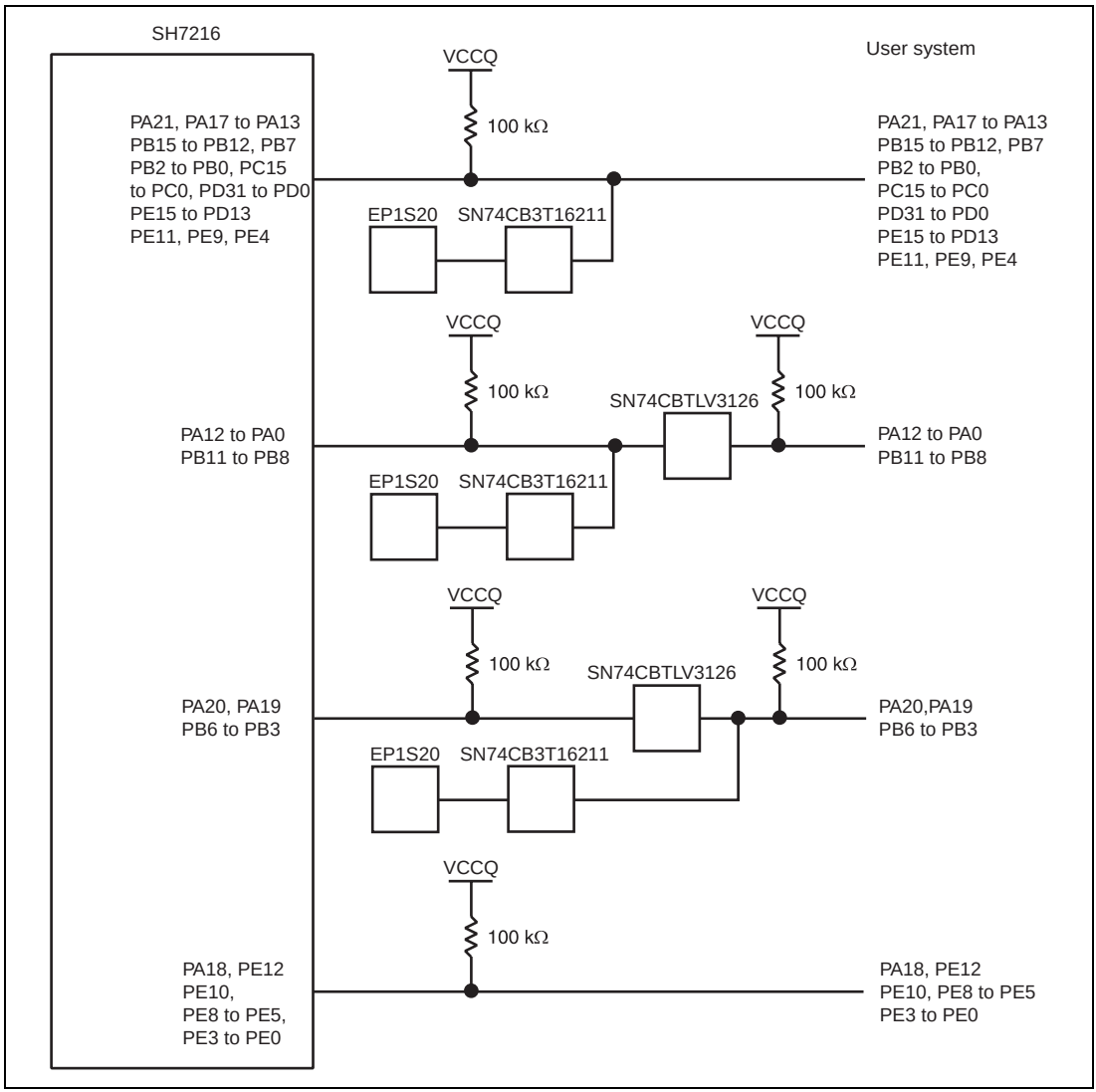


Figure 4.6 User System Interface Circuits (6)

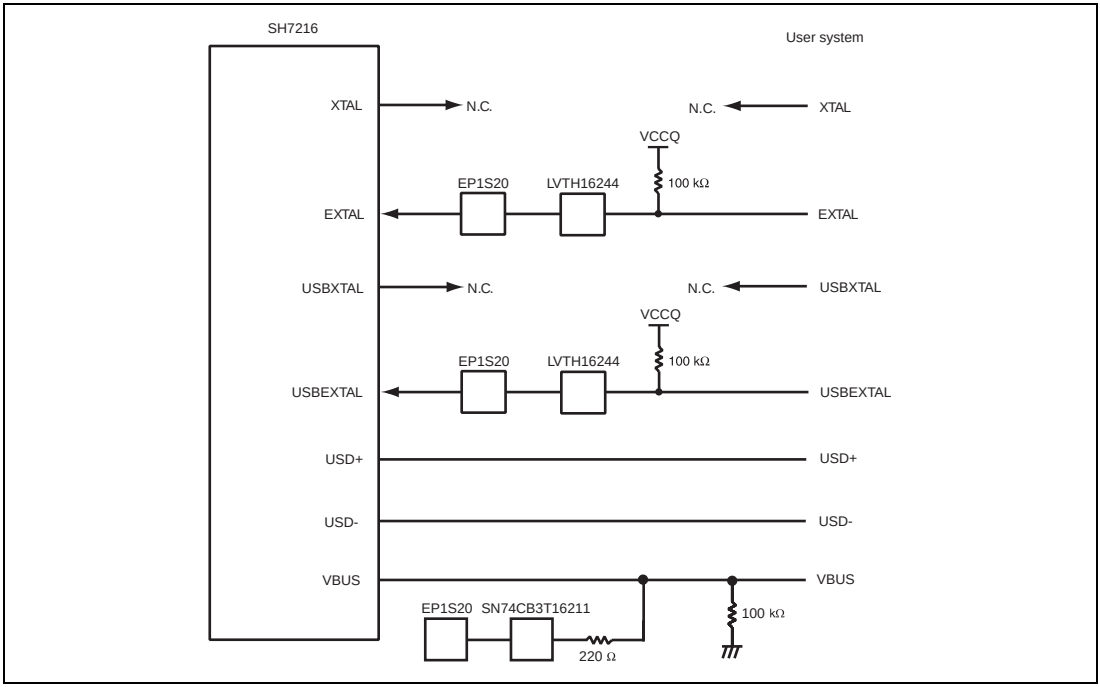


Figure 4.7 User System Interface Circuits (7)

4.2 Delay Time for the User System Interface

(1) When using the common user-system interface adaptor cable and user-system converter board to connect the E200F emulator and user system, the wiring of the circuit between the IC socket pins and pins of the devices on the user system leads to delay times for the signals. Since the _RES and NMI signals are connected to the user system via the logic on the EV-chip unit, a delay time will be generated until the signal is input from the user system to the MCU.
Table 4.1 gives the delay times when connecting the common user-system interface adaptor cable and user-system interface converter board.

Table 4.1 Delay Times Created by Connection with the Flexible Cable

No.	Signal Name	Delay Time (ns)
1	_RES	22
2	NMI	19
3	Other signals	6

(2) The flexible cable unit of the common user-system interface adaptor cable is removable. Delay times for signals can be reduced by removing the flexible cable then directly connecting the board unit of the common user-system interface adaptor cable and user-system interface converter board. Refer to the user's manual for the user-system interface converter board for the procedure for this connection.
Table 4.2 shows the delay time generated when the flexible cable unit of the common user-system interface adaptor cable has been removed.

Table 4.2 Delay Times Created on Removing the Flexible Cable

No.	Signal Name	Delay Time (ns)
1	_RES	19
2	NMI	16
3	Other signals	3

SH-2A, SH-2 E200F Emulator
Additional Document for User's Manual
Supplementary Information on Using the SH7214 and SH7216

Publication Date: Rev.1.00, October 15, 2009
Published by: Sales Strategic Planning Div.
Renesas Technology Corp.
Edited by: Customer Support Department
Global Strategic Communication Div.
Renesas Solutions Corp.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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REJ10J2072-0100