User's Manual

RZ/G3S SMARC Module Board

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G Series

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Rev.2.00 July 2026

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(Rev.5.0-1 October 2020)

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Precautions

This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1. Introduction

The RZ/G3S SMARC Module board (hereinafter referred to as “G3S SMARC Module”) is a platform designed according to the SMARC 2.1.1 Specification to evaluate the Renesas RZ/G3S microprocessor.

Basically, the G3S SMARC Module is connected to the Renesas RZ SMARC Series Carrier Board II (hereinafter referred to as “RZ SMARC Carrier II”) and used as the RZ/G3S SMARC Evaluation Board (hereinafter referred to as “G3S SMARC EVK”).

This guide includes system setup and configuration. This guide also provides detailed information on the overall design and use of the G3S SMARC Module from a hardware system perspective.

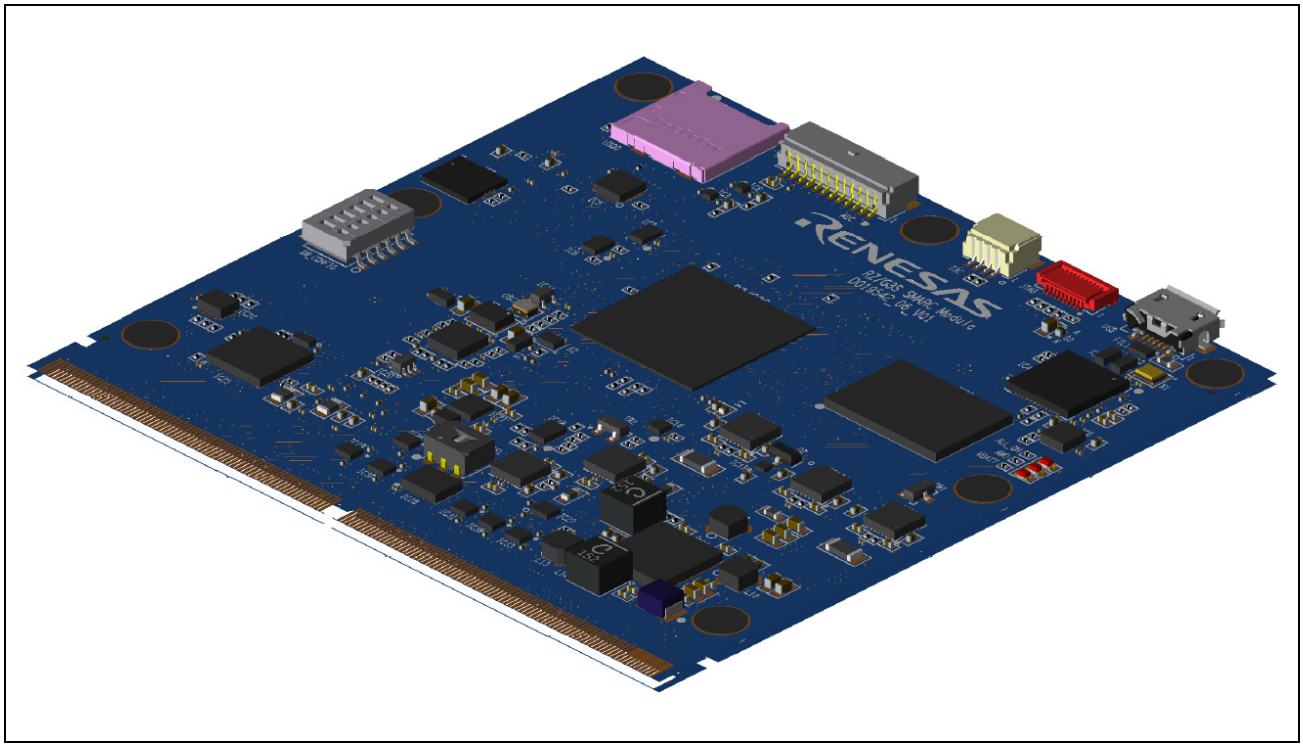


Figure 1.1 RZ/G3S SMARC Module Board

Table 1.1 shows the key features of the G3S SMARC Module.

Table 1.1 Key Features of the G3S SMARC Module

Board Features	Details
Processor	RTK9845S33S01000BE: RZ/G3S (P/N: R9A08G045S33GBG), 14 mm × 14 mm, 0.5-mm pitch, 359-pin PBGA RTK9845S37S01000BE: RZ/G3S (P/N: R9A08G045S37GBG), 14 mm × 14 mm, 0.5-mm pitch, 359-pin PBGA
Memory	1-GB 512Mx16 LPDDR4 SDRAM supporting data rate up to 1600MT/s
	microSD card slot supporting default, high-speed, and UHS-I transfer modes, including SDR50, SDR104, and DDR50
	64-GB eMMC flash with HS200 transfer mode support
	microSD card slot with default, high-speed transfer modes support
	128-Mbit Quad SPI flash memory
Supported interfaces and peripherals	Supports 10-pin JTAG connection from a debugger
	Supports ADC connection for 8 channels
	I3C interface
	5x ISL28025FRZ for current monitoring
	2x gigabit Ethernet transceiver
	9-channel PMIC (P/N: RAA215300A2GNP#HA3)
	6-channel clock generator (P/N: 5L35023B-615NLGI)
Board dimensions	82mm(W) × 80mm(L) × 1.2mm(H), 6-layer

The G3S SMARC Module may be used in any carrier board which follows the SMARC 2.1.1 Specification, however, Renesas recommends using the Renesas RZ SMARC Carrier II board.

The details of the RZ SMARC Carrier II board are to be found in the “RZ SMARC Series Carrier Board II User’s Manual”.

1.1 Kit Contents

If you have purchased the RZ/G3S SMARC Evaluation Board Kit, your contents will include:

- RZ/G3S SMARC Module Board
- RZ SMARC Series JTAG Adaptor Cable (hereinafter referred to as "SMARC JTAG Adaptor")
- RZ SMARC Series Carrier Board II
- USB Type-A to USB Micro B cable for serial debugging
- Accessories bag:
  - 2off M2.5 x6mm pan-head machine screws (for securing M.2 cards)
  - 1off 2.5mm spacer (for securing M.2 key B cards)

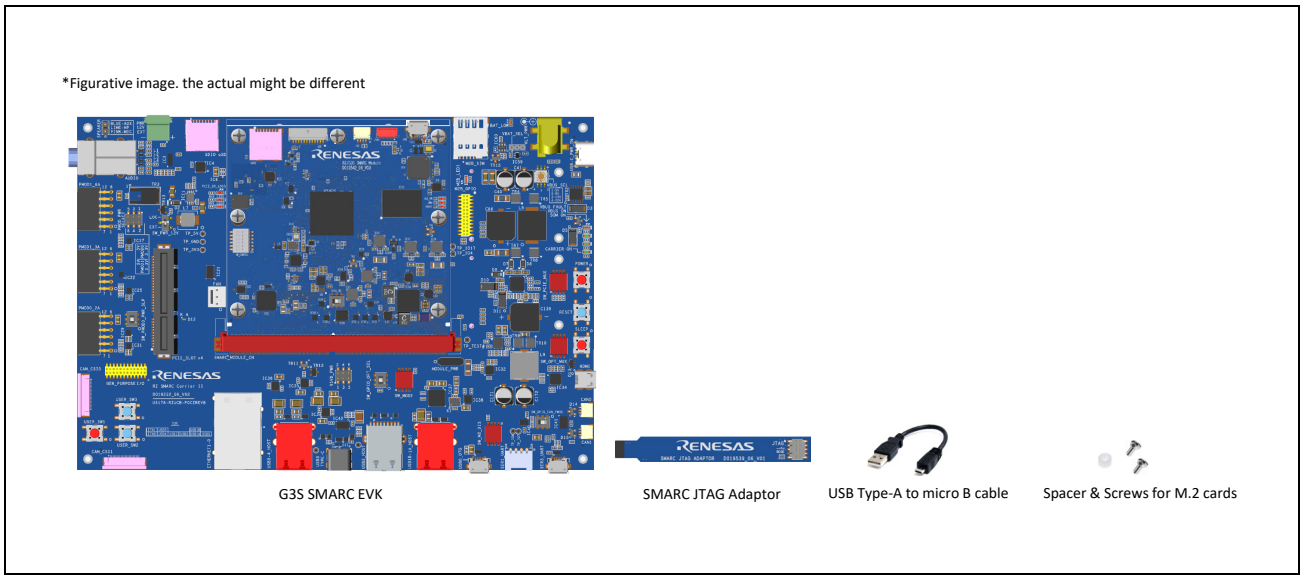


Figure 1.2 RZ/G3S SMARC Evaluation Board Kit Contents

1.2 Module Assembly and EVK Revisions

The G3S SMARC Module can only be used when fitted to a SMARC compliant Carrier board.

Secure the Module using 7off M2.5 x4mm pan-head machine screws (these are provided with the RZ SMARC Carrier II).

If connection to the JTAG interface is required, it may be necessary to connect the SMARC JTAG Adaptor. Refer to the section heading **JTAG**.

1.3 Ordering Information

- G3S SMARC EVK orderable part numbers:
  - RTK9845S33S01000BE
  - RTK9845S37S01000BE

There are two types of G3S SMARC EVK.

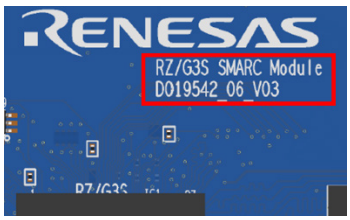
RTK9845S33S01000BE is equipped with R9A08G045S33GBG (for which the security is not supported) as the microprocessor.

RTK9845S37S01000BE is equipped with R9A08G045S37GBG (for which the security is supported). This kit is compatible with the security type.

The PCB design revisions of the G3S SMARC EVK are listed in **Table 1.2**. To distinguish them using the outer box, you can check the serial number (S.LOT#) on the label attached to the outer box. The serial number is also printed on the bottom surface of the board.

To distinguish them using the actual board, you can check the PCB revision number indicated on the silkscreen of the PCB. You can also check the device part number printed on the device itself.

Table 1.2 PCB Design Revisions of the G3S SMARC EVK

PCB Revision	Device Part Number	Silkscreen*1	S.LOT# on the Carrier Board (S.LOT# on the Outer Box Label)	Description
1.0	#AC0 #BC0		284608 – 284807 (0000284608 – 0000284807)	Initial release
3.0	#AC0 #BC0		293401 or later (0000293401 or later)	Several improvements have been made. The main changes are the pull-up voltage on the MODE terminals and the power control signal for the microSD0 card interface. For more details on the improvements, refer to the errata material included with the design data below. URL: RZ/G3S SMARC Module Board Design Data V3.00

Note 1. The board image may differ from the actual board.

2. System Description

Figure 2.1 and **Figure 2.2** show the pictures of the G3S SMARC Module and location of various blocks on the board.

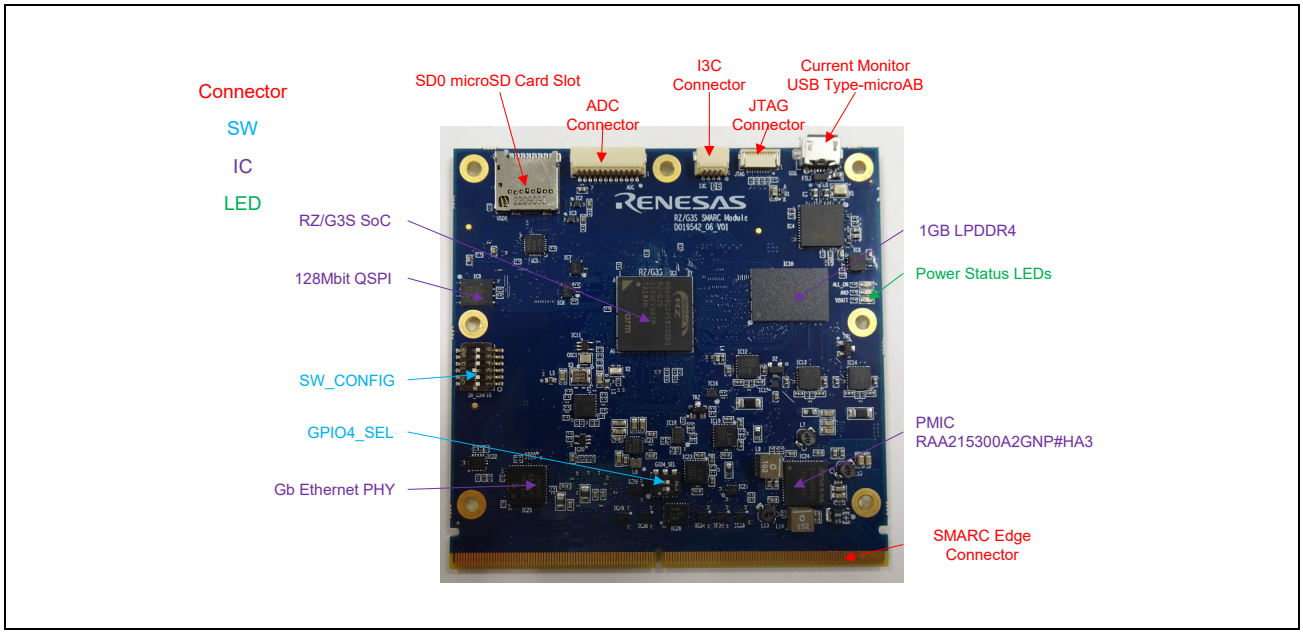


Figure 2.1 RZ/G3S SMARC Module Board Top View



Figure 2.2 RZ/G3S SMARC Module Board Bottom View

The G3S SMARC Module has several switched configuration options and on-board interfaces. These are detailed in the following sections.

The default settings are highlighted.

2.1 G3S SMARC EVK Functional Block

Figure 2.3 shows the functional block diagram of the G3S SMARC EVK. ICs, connectors and switches surrounded by red frame indicate functions used on the G3S SMARC Module.

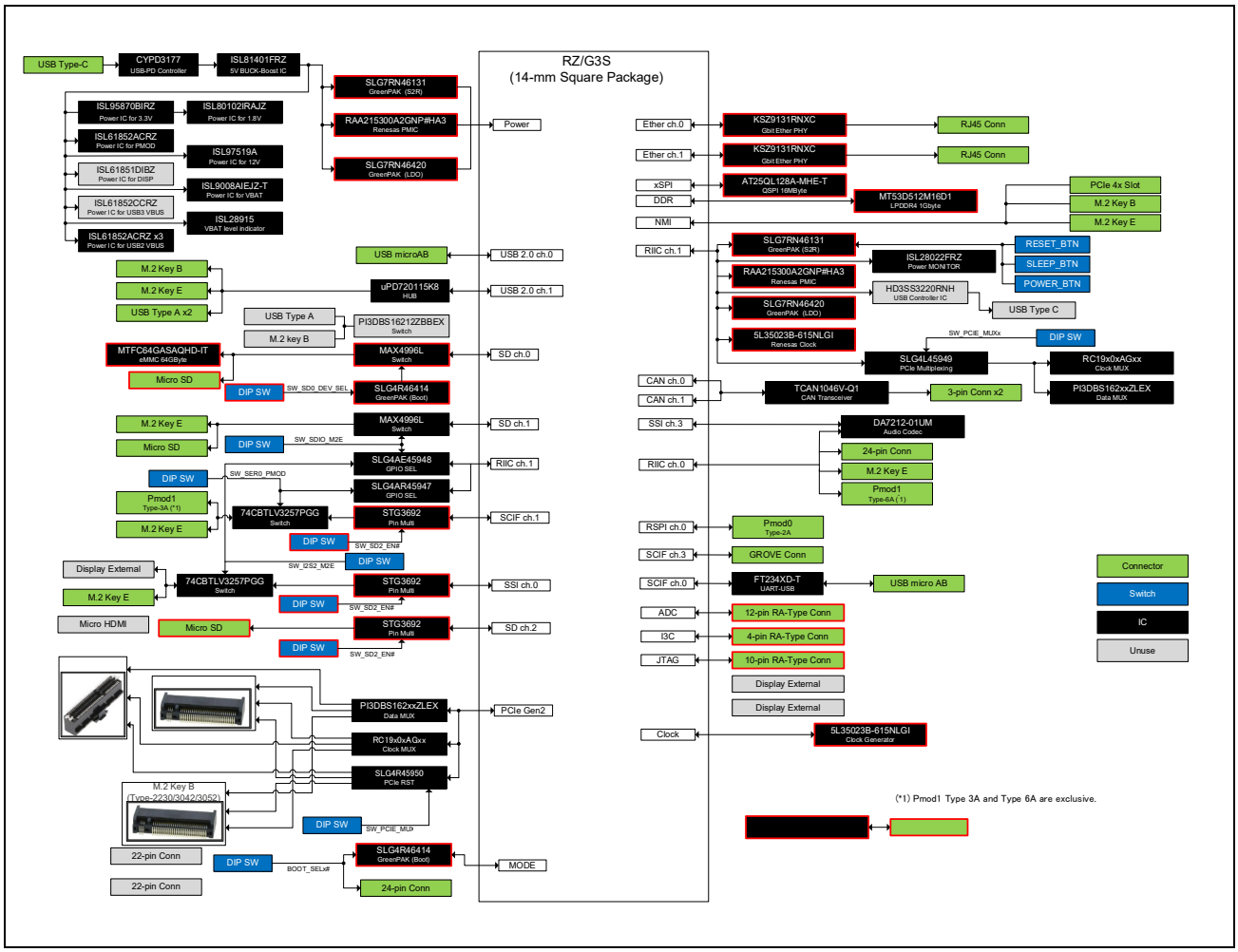


Figure 2.3 G3S SMARC EVK Block Diagram

2.2 G3S SMARC EVK Interface Mapping

Table 2.1 lists the device part numbers used on the G3S SMARC EVK, including ICs mounted on both the G3S SMARC Module and the RZ SMARC Carrier II. Renesas parts are highlighted.

The SMARC Interface Name column indicates the interface name on the RZ SMARC Carrier II, and the RZ/G3S I/F column indicates the corresponding interface on the RZ/G3S. For some interfaces, "—" is shown in the SMARC Interface Name column, indicating that the corresponding RZ port pins are not connected to the RZ SMARC Carrier II via the SMARC edge connector and that the interface is implemented entirely within the G3S SMARC Module. On the other hand, for some interfaces, "—" is shown in the RZ/G3S I/F column, indicating that the interface is implemented on the RZ SMARC Carrier II but is not connected to the RZ/G3S on the G3S SMARC Module. Such interfaces are therefore not available on the G3S SMARC EVK.

The rightmost two columns (G3S SMARC Module and RZ SMARC Carrier II) indicate the mounting location of each component. A check mark (√) indicates that the component is mounted on the corresponding board, while "—" indicates that it is not mounted. Some components are mounted on the adaptor board; in such cases, "—" is indicated in both columns. Refer to the notes in **Table 2.1** for details.

Table 2.1 Interface Mapping (1/3)

SMARC Interface Name	RZ/G3S I/F	Device Part Number	Description	G3S SMARC Module	RZ SMARC Carrier II
USB0	USB2.0 ch0	629105150921	USB2.0 Type-microAB receptacle	—	√
		SLG4E46290	GreenPAK (USB Logic)	√	—
USB1	USB2.0 ch1	uPD720115K8-711-BAK-A	USB2.0 Hub IC	—	√
		72309-8014BLF	USB2.0 Type-A receptacle	—	√
		SLG4E46290	GreenPAK (USB Logic)	√	—
USB2	—	692122030100	USB3.0 Type-A receptacle	—	√
USB3	—	1054500101	USB3.0 Type-C receptacle	—	√
USB4	—	72309-8014BLF	USB2.0 Type-A receptacle	—	√
USB5	—	72309-8014BLF	USB2.0 Type-A receptacle	—	√
CAN0	CAN ch0	TCAN1046VDMTRQ1	CAN transceiver	—	√
		SM03B-SRSS-TB(LF)(SN)	3-pin connector	—	√
CAN1	CAN ch1	TCAN1046VDMTRQ1	CAN transceiver	—	√
		SM03B-SRSS-TB(LF)(SN)	3-pin connector	—	√
I2S0	SSI ch3	DA7212-01UM	Audio Codec	—	√
		STX-4335-5BGP-S1	Connector for Stereo Headphone, Stereo Mic, Aux	—	√
		M20-9990246	Pin header for speaker	—	√
I2S2	SSI ch0	MDT420E01001	M.2 Key E for I2S interface	—	√
SPI0	—	GRPB122VWQS-RC	24-pin header	—	√
SPI1	RSPI ch0	SSW-106-02-T-D-RA	PMOD Type-2A connector	—	√
SER0	SCIF ch1	SSW-106-02-T-D-RA	PMOD Type-3A connector (*1)	—	√
		MDT420E01001	M.2 Key E (*1)	—	√
SER1	SCIF ch3	110990037	Grove connector	—	√
SER2	—	MDT420E01001	M.2 Key E (*1)	—	√
SER3	SCIF ch0	FT234XD-T	USB to UART conversion IC	—	√
		629105150921	USB2.0 Type-microAB receptacle for UART Debug	—	√

Table 2.1 Interface Mapping (2/3)

SMARC Interface Name	RZ/G3S I/F	Device Part Number	Description	G3S SMARC Module	RZ SMARC Carrier II
PCIE_A	PCIe Gen2	10061913-111PLF	PCIe 4x Slot	—	√
		MDT420B01001	M. 2 Key B	—	√
		MDT420E01001	M. 2 Key E	—	√
		78646-3001	SIM card for M. 2 Key B	—	√
		SLG4R45950	GreenPAK (PCIe Slot Reset, M.2 Key E Reset, M.2 Key B Reset)	—	√
SATA	—	GRPB122VWQS-RC	GPIO pin header	—	√
HDMI	—	46765-1301	Micro HDMI connector	—	√
DSI0/LVDS0	—	2041262-1	Mini PCI Express & mSATA connector	—	√
DSI1/LVDS1	—	2041262-1	Mini PCI Express & mSATA connector	—	√
CSI0	—	2-1734592-2	22-pin FPC connector	—	√
CSI1	—	2-1734592-2	22-pin FPC connector	—	√
GBE0	Ether ch0	KSZ9131RNXC	Ethernet PHY	√	—
		2301997-7	Stacked RJ45 connector	—	√
GBE1	Ether ch1	KSZ9131RNXC	Ethernet PHY	√	—
		2301997-7	Stacked RJ45 connector	—	√
I2C_GP	RIIC ch0	GRPB122VWQS-RC	GPIO pin header	—	√
		MDT420B01001	M. 2 Key E for I2C interface	—	√
		DA7212-01UM	Audio Codec for I2C interface	—	√
		SSW-106-02-T-D-RA	PMOD Type-6A connector	—	√
I2C_PM	RIIC ch1	ISL28022FRZ	Current monitor for measuring SMARC module	—	√
		SLG4L45949	GreenPAK (PCIe Data Multiplexing Control, PCIe Slot Enable, M.2 Key E Enable, M.2 Key B Enable)	—	√
		SLG4AR45947	GreenPAK (GPIO and SER0 Multiplexing Control, M.2 Key B Reset/Power off, M.2 Key E Disable)	—	√
		SLG4AE45948	GreenPAK (M.2 Key B Configuration Decoding, USB2, I2S2 and SDIO Multiplexing Control, USB1 Hub Enable)	—	√
		RAA215300A2GNP#HA3	PMIC	√	—
		SLG7RN46420	GreenPAK (Power Regulator)	√	—
		SLG7RN46131	GreenPAK (Power/Reset control)	√	—
		5L35023B-615NLGI	Clock generator	√	—
I2C_LCD	—	2041262-1	Mini PCI Express & mSATA connector	—	√
I2C_CAM0	—	2-1734592-2	22-pin FPC connector	—	√
I2C_CAM1	—	2-1734592-2	22-pin FPC connector	—	√
—	SD/MMC ch0	1040310811	microSD card slot	√	—
		MTFC64GASAQHD-IT	64-GB eMMC memory	√	—
SDIO	SD ch1	1040310811	microSD card slot	—	√
—	SD ch2	1040310811	microSD card slot	√	—
—	DDR	MT53E512M16D1FW-046WT	1-GB LPDDR4 SDRAM	√	—
—	xSPI	AT25QL128A_MHE	128-Mbit Quad SPI Flash memory	√	—
—	ADC	SM12B-SRSS-TB(LF)(SN)	12-pin connector	√	—
—	I3C	SM04B-SRSS-TB(LF)(SN)	4-pin connector	√	—

Table 2.1 Interface Mapping (3/3)

SMARC Interface Name	RZ/G3S I/F	Device Part Number	Description	G3S SMARC Module	RZ SMARC Carrier II
—	JTAG	10051922-1010EHLF	10-pin FPC connector	√	—
		FTSH-105-01-L-DV-007-K	10-pin connector (*2)	—	—
—	CPG	5L35023B-615NLGI	Clock generator	√	—
		830208214909	Oscillator for AUDIO_CLK2	√	—
—	(For current monitoring)	ISL28025FR12Z	Current monitor for measuring five power rails on SMARC module	√	—
		FT232HQ	USB to I2C conversion IC	√	—
		629105150921	USB2.0 Type-microAB receptacle	√	—
Boot	System	SLG4R46414	GreenPAK (Boot mode and device selection)	√	—

Note 1. Select whether to assign PMOD1 to SER0 or M.2 Key E to SER0. M.2 Key E cannot be assigned to SER2 since SER2 is not connected to the G3S SMARC Module.

Note 2. The SMARC JTAG Adaptor is required. It is bundled with the G3S SMARC EVK.

2.3 Board Configuration and Status

This section provides details of the G3S SMARC Module switch settings.

2.3.1 SW_CONFIG

A bank of 6-switches is used to configure operating modes of the Module. The default settings are highlighted.

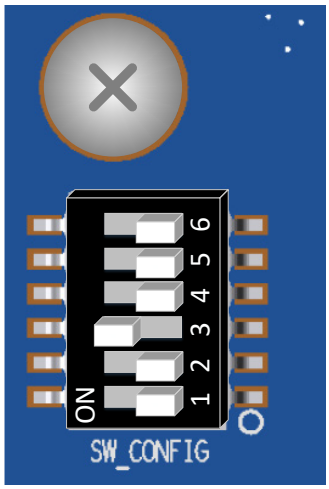


Figure 2.4 The Location and the Default Setting of the SW_CONFIG

Table 2.2 DIP Switch “SW_CONFIG” Settings

SW_CONFIG[x]	Signal	ON	OFF
6	RZ_BOOTCPUSEL	Cold boot from Cortex-M33(w/o FPU)	Cold boot from Cortex-A55
5	RZ_MD_CLKS	SSCG is disabled	SSCG is enabled
4	SW_I3C_VIO_SEL	I3C voltage is 1.2 V	I3C voltage is 1.8 V
3	SW_SD2_EN	SD2 is disabled.	SD2 is enabled
2	SW_SD0_DEV_SEL	SD0 connected to microSD0 card	SD0 connected to eMMC
1	RZ_DEBUGEN	JTAG Debug is disabled	JTAG Debug is enabled

2.3.2 GPIO4_SEL

The SMARC GPIO4 signal from/to the Carrier II may be used for RZ_TAMPIN as an alternative to the default port pin. The default settings are highlighted.

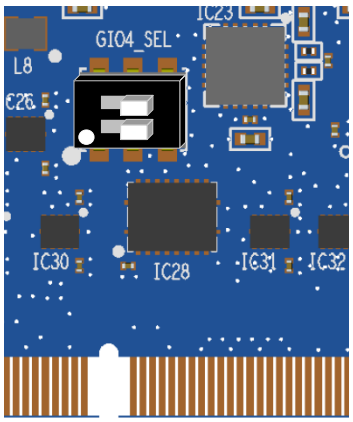


Figure 2.5 The Location and the Default Setting of the GPIO4_SEL

Table 2.3 DIP Switch “GPIO4_SEL” Settings (1/2)

GPIO4_SEL	GPIO4 Function
1 – 2	SMARC GPIO4 pin is connected to RZ_TAMPIN
2 – 3	SMARC GPIO4 pin is connected to RZ/G3S P18_0 *Note*: RZ_TAMPIN is pulled up to VBATT_VDD

Table 2.3 DIP Switch “GPIO4_SEL” Settings (2/2)

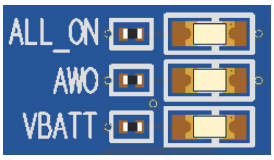
GPIO4_SEL	Function
4 – 5	Spare – unused
5 – 6	Spare – unused

2.4 List of Pin Functions

2.4.1 LED Indicators

The RZ/G3S has the following four power modes depending on the power on/off combination of the power domain. There are three Red LEDs on the G3S SMARC Module to provide indication of the RZ/G3S power modes.

Table 2.4 Indicator LEDs – Power Status

ALL_ON	Power Mode
	ALL_ON All CPUs and peripheral modules are active
	AWO Cortex-M33 and peripheral modules in PD_VCC and PD_VBATT domain are active
	VBATT Only RTC, tamper detection and backup registers are active
	ALL_OFF All CPUs and peripheral modules are disabled

2.5 Recommended Operating Condition

Table 2.5 lists operating conditions of the G3S SMARC Module.

Table 2.5 Operating Conditions of G3S SMARC Module

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage *1	3.0 V to 5.25 V	Reference: SMARC 2.1.1 Specification
—	Maximum power consumption	5 A	Reference: SMARC 2.1.1 Specification
Topr	Operating ambient temperature *2	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. Supplied from the connected RZ SMARC Carrier II.

Note 2. The ambient temperature is the air temperature at a point as close to the board as possible.

3. Functional Specifications

3.1 Processor

The RZ/G3S (P/N: R9A08G045S33GBG or R9A08G045S37GBG, 14 mm × 14 mm, 0.5-mm pitch, 359-pin) includes a single ARM Cortex-A55 core with speeds up to 1.2 GHz. Dual Arm Cortex-M33 cores with speeds up to 250 MHz is for real-time and low-power processing. One Arm Cortex-M33 has FPU function. Low power mode is supported and realized low power consumption of micro ampere class. Also, dual 1Gbit/s Ethernet controllers and PCI Express Gen2 drive gateway applications with low latency.

The RZ/G3S is useful for application such as:

- IoT gateway (i.e. smart home gateway, smart meter, and fleet tracker)

For details on the processor, see the “RZ/G3S Group User’s Manual: Hardware”.

3.2 Power Supply

Figure 3.1 shows a block diagram of power system of the G3S SMARC EVK.

This board has one USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected among 5 V, 9 V, 15 V, and 20 V.

The 5 V power supply is supplied to the PMIC (RAA215300A2GNP#HA3) installed in the G3S SMARC Module, and the PMIC generates the power supply voltage for each interface.

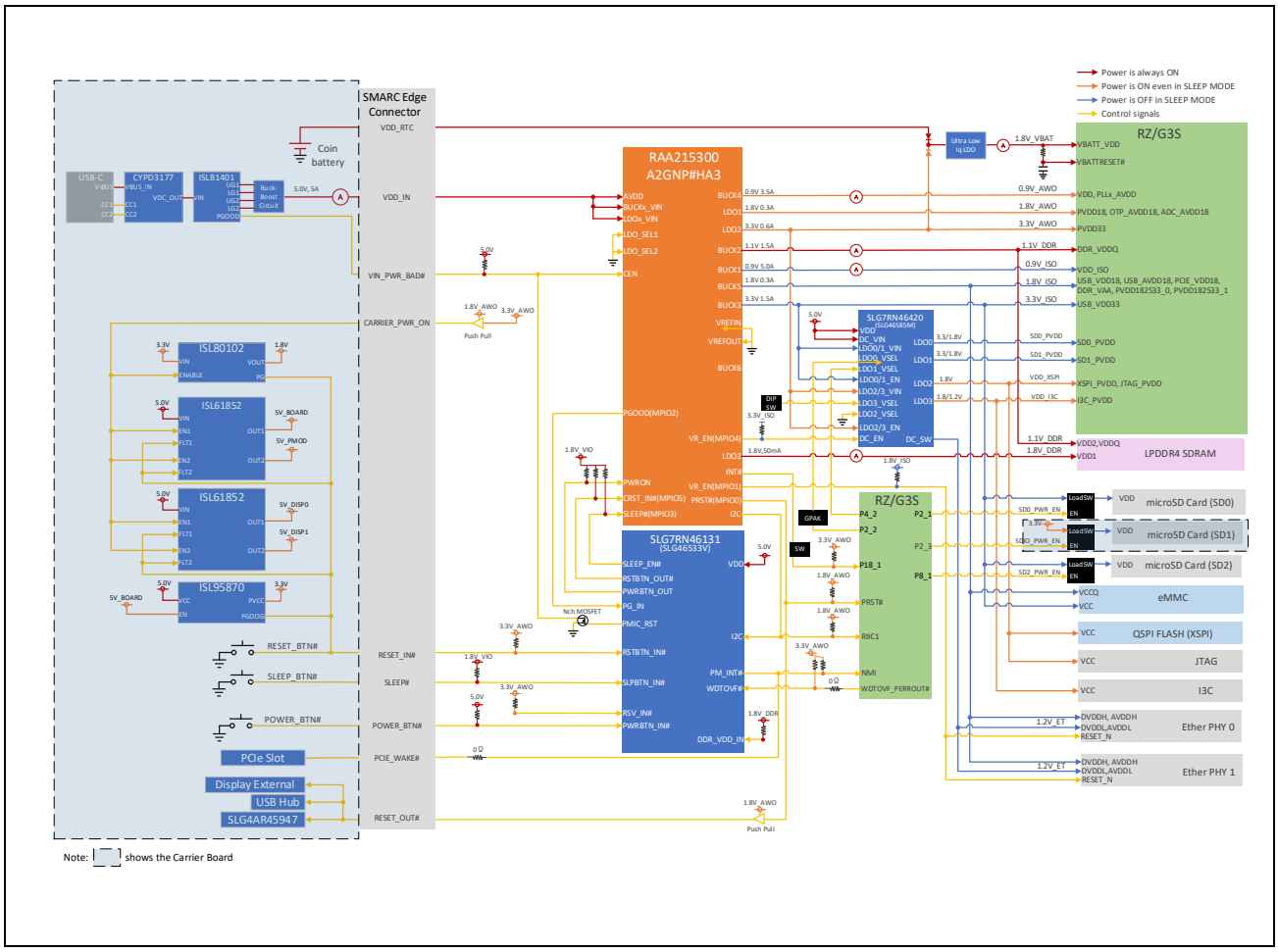


Figure 3.1 Power System Circuitry of G3S SMARC EVK

The G3S SMARC EVK supports two low-power modes: VBATT Retention mode and AWO + DDR Retention mode. **Figure 3.2** and **Figure 3.3** show the power sequence of the transition/return between ALL_ON mode and AWO + DDR Retention mode, and the transition/return between ALL_ON mode and VBATT Retention mode, respectively. The RZ/G3S SoC power rails are shown in red text. The control signals for PMIC or GreenPAKs are shown in blue. The control signals for the RZ/G3S SoC, JTAG, and Ethernet are shown in light green.

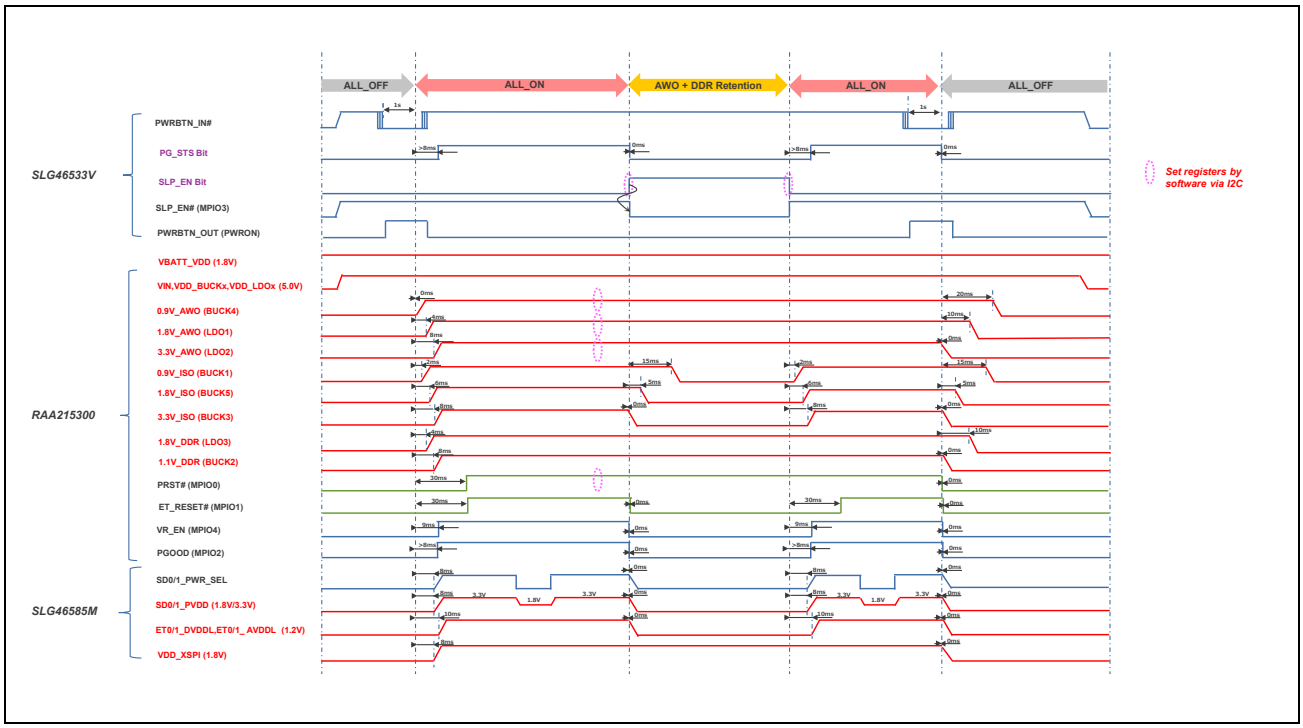


Figure 3.2 Power Sequence of G3S SMARC EVK when the Power Mode Changes from ALL_OFF to ALL_ON, ALL_ON to AWO + DDR Retention, AWO + DDR Retention to ALL_ON, and ALL_ON to ALL_OFF

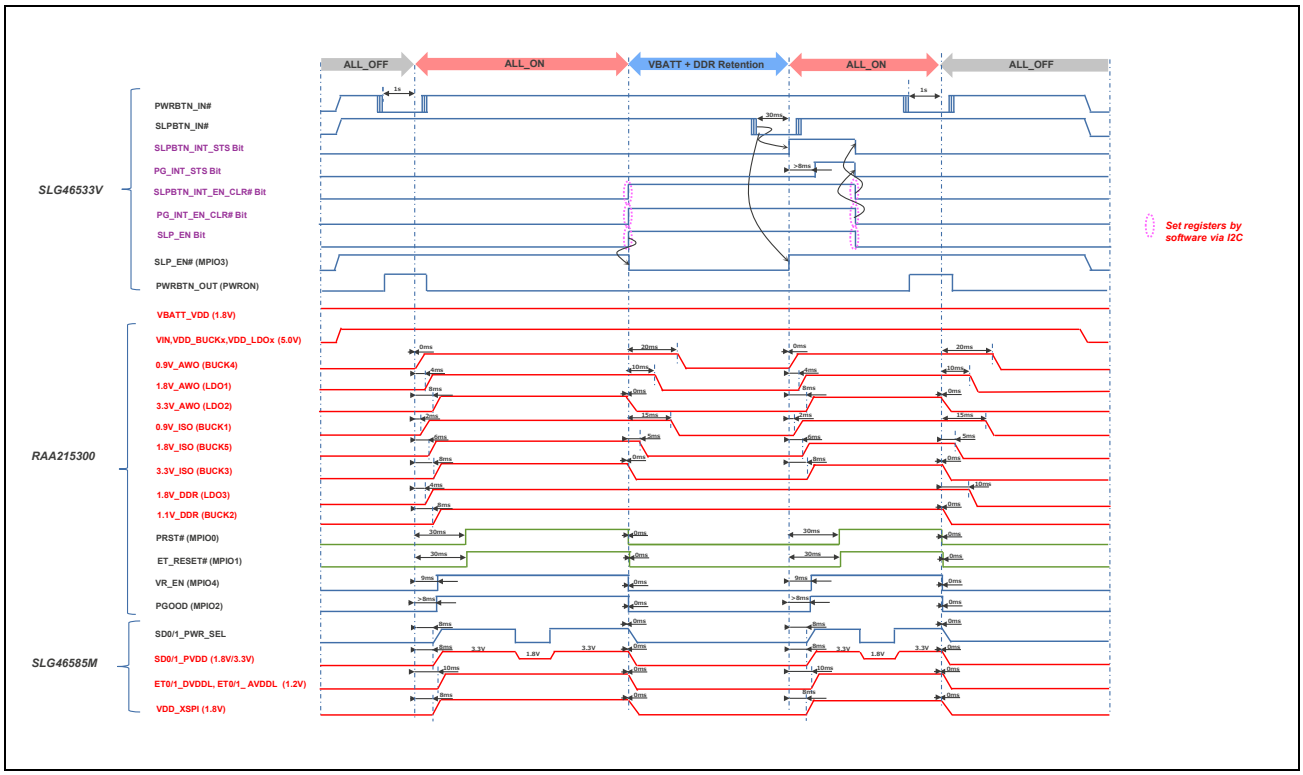


Figure 3.3 Power Sequence of G3S SMARC EVK when the Power Mode Changes from ALL_OFF to ALL_ON, ALL_ON to VBATT + DDR Retention, VBATT + DDR Retention to ALL_ON, and ALL_ON to ALL_OFF

3.3 Clock

The clock generator (part number 5L35023B-615NLGI) provides the clock required for the RZ/G3S SoC and peripheral interfaces.

The 5L35023B is Renesas VersaClock@ 3S programmable clock generator and supports 6 unique frequency outputs.

The 5L35023B-615NLGI takes the 24 MHz crystal as a reference input and provides a 24 MHz reference clock output for the RZ/G3S SoC, two 11.2896 MHz LVCMOS clock outputs for the RZ/G3S SoC and Audio Codec, one 125 MHz LVCMOS clock output for two Ethernet PHYs, and two 100 MHz LPHSCL clock outputs for the RZ/G3S SoC and a PCI Express Card Module. One oscillator provides 12.2880 MHz clock output for the RZ/G3S SoC.

An external crystal is attached to the RZ/G3S SoC to provide clock to the RTC domain of the SoC (32.768 kHz).

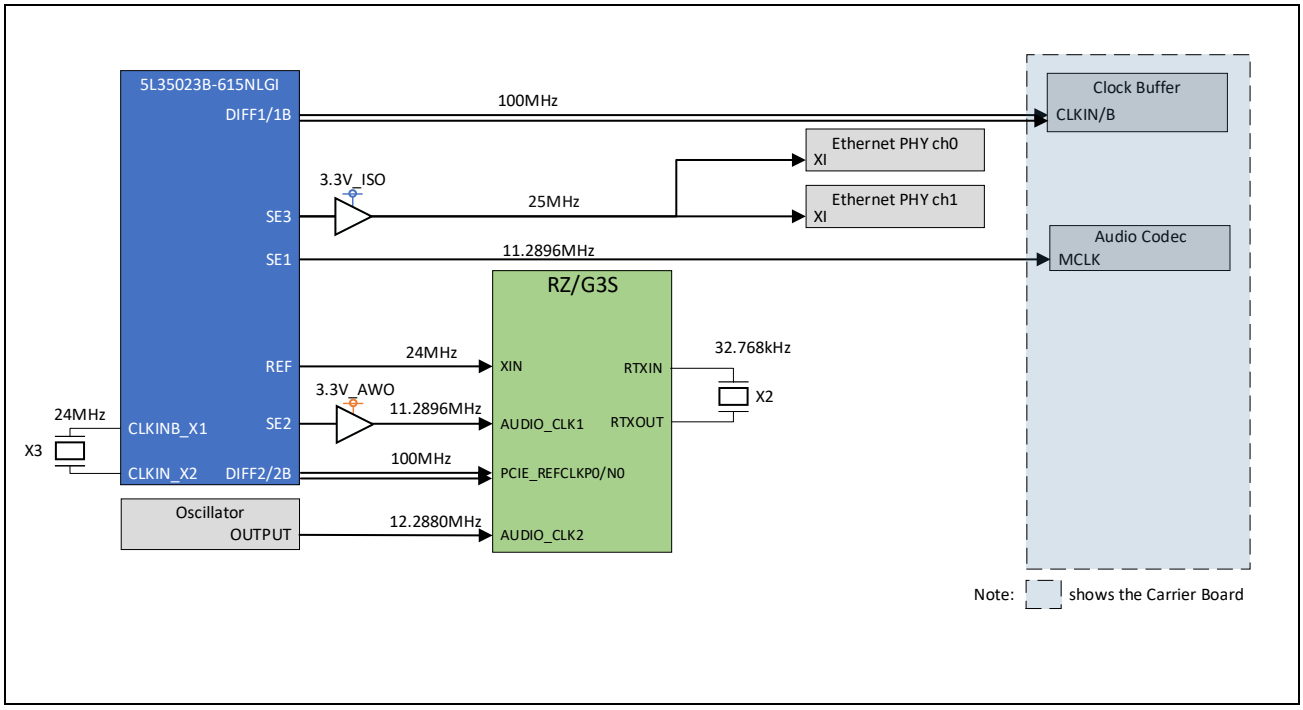


Figure 3.4 Clock Architecture of G3S SMARC EVK

Clock inputs required for peripherals such as FT232HQ, USB Hub, M.2 Key E Card Module, HDMI Transmitter are generated locally using separate crystals or oscillators. The crystals or oscillators used to provide the reference clocks for the G3S SMARC EVK peripherals are shown in the table below.

Table 3.1 Clock Table

Peripheral	Device Part Number	Frequency
FT232HQ Bridge	FL2400022	24.000 MHz
USB Hub*1	FL2400022	24.000 MHz
M.2 Key E*1	7XZ-32.768KBE	32.768 kHz
HDMI Transmitter*2	SIT1602AI-23-18E-12.000000D	12.000 MHz

Note 1. RZ SMARC Carrier II

Note 2. SMARC MIPI-DSI to HDMI Adaptor. However, the SMARC MIPI-DSI to HDMI adaptor is not bundled with the G3S SMARC EVK.

3.4 Reset

Figure 3.5 shows block diagrams of a reset control for the G3S SMARC EVK.

For the G3S SMARC EVK, the RZ/G3S SoC and Ethernet PHY on the G3S SMARC Module and some modules on the RZ SMARC Carrier II are controlled by the reset signal from the RAA215300.

There are two types of system resets.

- Cold reset by power-on reset
- Warm reset by the reset button switch

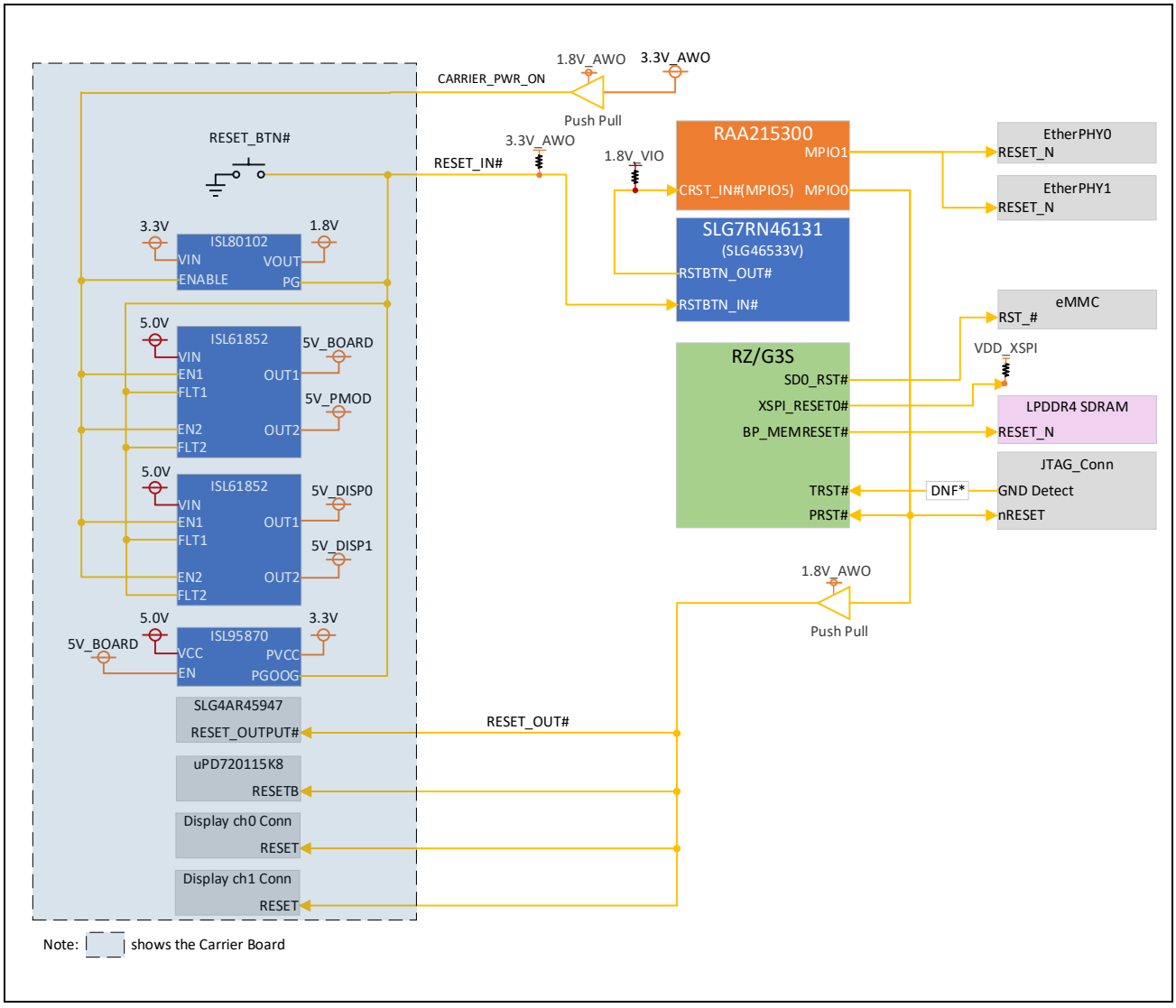


Figure 3.5 Reset Architecture of G3S SMARC EVK

3.5 LPDDR4 SDRAM

The G3S SMARC Module supports LPDDR4 SDRAM. A LPDDR4 SDRAM from Micron Technology (part number MT53E512M16D1FW-046WT) is provided for connection to the RZ/G3S DDR IO.

3.6 xSPI Interface

The G3S SMARC Module supports QSPI flash memory for xSPI interfaces. A QSPI flash memory from Renesas (part number AT25QL128A-MHE) is provided for connection to the RZ/G3S xSPI IO.

3.7 eMMC Memory

This eMMC is on the bottom side of the G3S SMARC Module. An eMMC from Micron Technology (part number MTFC64GASAQHD-IT) is provided for connection to the RZ/G3S MMC IO.

The RZ/G3S MMC IO may be used either for eMMC (SW_CONFIG[2] = OFF) or for the microSD0 Card interface (SW_CONFIG[2] = ON).

3.8 microSD0 Card Interface

This microSD card interface is on the top side of the G3S SMARC Module. Cards must be inserted with the contacts facing down.

The connector is a push-pull type.

The RZ/G3S SD0 IO may be used either for eMMC (SW_CONFIG[2] = OFF) or for the microSD0 Card interface (SW_CONFIG[2] = ON)*[1].

Additional control of the microSD0 card using the RZ/G3S port pins is shown below.

Note 1. The G3S SMARC EVK supports eSD boot mode. The GPIO signal (P2_1) is used to control the power supply for microSD ch.0. Therefore, a system reboot during an eSD boot is supported by the following method:
- Software reset using P2_1

However, (1) a reset caused by a watchdog timer underflow and (2) a hardware reset by pressing the blue reset button on the RZ SMARC Carrier II do not result in a proper reboot due to the circuit specifications. In such cases, switch the board's power off and then back on again through red power button on the RZ SMARC Carrier II.

Table 3.2 microSD0 Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD0 Card Detect	P0_0	Input	0: Card present 1: No card present
microSD0 Card Power Enable	P2_1	Output	0: Power disabled 1: Power enabled
microSD0 Card IO Power Select	P2_2	Output	0: 1.8 V 1: 3.3 V

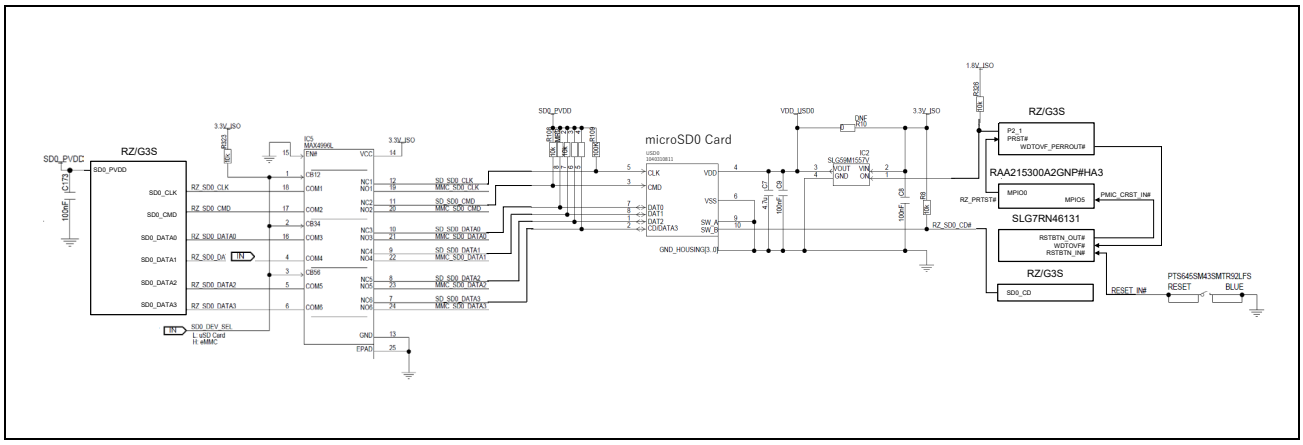


Figure 3.6 Proposed Block Diagram of microSD0 Card I/F

The following is an example of a circuit that enables system reboot even when both of the above events occur during an eSD boot.

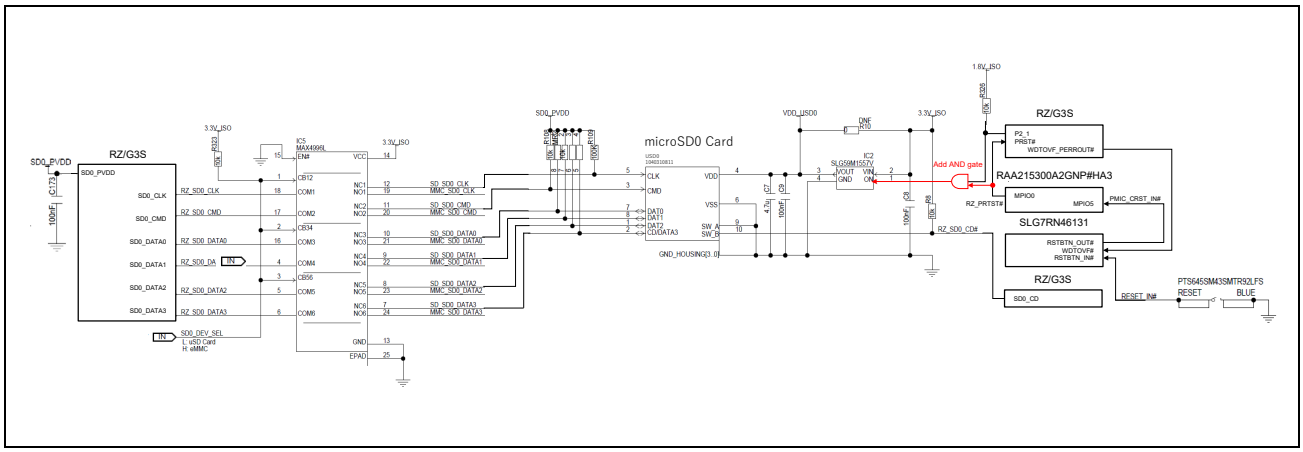


Figure 3.7 Proposed Block Diagram of microSD0 Card I/F

3.9 microSD1 Card Interface

This microSD card interface is on the RZ SMARC Carrier II through the SMARC Edge connector. Cards must be inserted with the contacts facing up.

The connector is a push-pull type.

The control signals of the microSD1 card using the RZG3S port pins, are shown below. For signals other than those listed in the table below, refer to **section 3.17.3, SDIO Card (4-Bit) Interface**.

Table 3.3 microSD1 card Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD1 Card Detect	P0_2/SD1_CD	Input	0: Card present 1: No card present
microSD1 Card Power Enable	P2_3_SDIO_PWR_EN	Output	0: Power disabled 1: Power enabled
microSD1 Card IO Power Select	P4_2_SD1_PWR_SEL	Output	0: 1.8 V 1: 3.3 V

3.10 microSD2 Card Interface

This microSD card interface is on the bottom side of the G3S SMARC Module. Cards must be inserted with the contacts facing up.

The connector is a push-pull type.

The RZ/G3S SD2 IO may be used either for SCIF1, SSI3, IRQ0, IRQ1 (SW_CONFIG[3] = ON) or for the microSD2 Card interface (SW_CONFIG[3] = OFF).

The microSD2 card signals, using the RZ/G3S port pins, are shown below.

NOTE

The microSD2 card interface supports only default and high-speed transfer modes.

Table 3.4 microSD2 card Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD2 Data0	P11_2	In/Out	microSD2 data
microSD2 Data1	P11_3	In/Out	microSD2 data
microSD2 Data2	P12_0	In/Out	microSD2 data
microSD2 Data3	P12_1	In/Out	microSD2 data
microSD2 Command	P11_1	In/Out	microSD2 CMD
microSD2 Clock	P11_0	Output	microSD2 clock
microSD2 Card Detect	P14_1	Input	0: Card present 1: No card present
microSD2 Card Power Enable	P8_1	Output	0: Power disabled 1: Power enabled
microSD2 Card IO Power Select	Not available	—	Fixed at 3.3 V

3.11 ADC

A right angle, 12-pin, 1.0mm pitch connector from JST (part number SM12B-SRSS-TB) is provided for connection to the RZ/G3S ADC IO.

The ADC interface voltage is 1.8 V.

Table 3.5 ADC Pin Assignment

Pin Number	Signal
1	RZ_ADC_CH0
2	RZ_ADC_CH1
3	RZ_ADC_CH2
4	RZ_ADC_CH3
5	RZ_ADC_CH4
6	RZ_ADC_CH5
7	RZ_ADC_CH6
8	RZ_ADC_CH7
9	RZ_ADC_TRG
10	ADC_AVDD (1.8 V)
11	3.3V_AWO (3.3 V)
12	Ground

3.12 I3C

A right angle, 4-pin, 1.0mm pitch connector from JST (part number SM04B-SRSS-TB) is provided for connection to the RZ/G3S I3C IO.

Table 3.6 I3C Pin Assignment

Pin Number	Signal
1	RZ_I3C_SCL
2	RZ_I3C_SDA
3 *1	VDD_I3C (1.2 V or 1.8 V)
4	Ground

Note 1. The I3C interface voltage is either 1.8 V (when SW_CONFIG[4] = OFF) or 1.2 V (when SW_CONFIG[4] = ON).

3.13 I2C

There are two I2C interfaces connected to the SMARC Edge connector.

RIIC ch0 is connected to the general purpose “I2C_GP” interface. RIIC ch1 is connected to the power management “I2C_PM” interface.

RIIC0 is not connected to any devices on the G3S SMARC Module.

Table 3.7 Address Mapping for RIIC1

RIIC1 Device	7-bit Address
Renesas RAA215300A2GNP#HA3 (PMIC)	0x12
Renesas GreenPAK SLG7RN46420 (Power Regulator)	0x28
Renesas GreenPAK SLG7RN46131 (Power/Reset control)	0x38
Renesas 5L35023B-615NLGI (clock generator)	0x68

3.14 JTAG

The G3S SMARC Module JTAG interface is implemented with a 10-pin, 0.5mm pitch, FPC connector from FCI (part number 10051922-1010EHLF). All JTAG IO are 1.8 V levels.

Table 3.8 JTAG Pin Assignment

JTAG Pin Number	SMARC Specification	Module Connection
1	VDD_JTAG	VDD_XSPI (1.8 V)
2	JTAG_TRST#	JTAG_TRST#_18 *1
3	JTAG_TMS	JTAG_TMS_18
4	JTAG_TDO	JTAG_TDO_18
5	JTAG_TDI	JTAG_TDI_18
6	JTAG_TCK	JTAG_TCK_18
7	JTAG_RTCK	Not connected
8	JTAG_RESET_IN#	RZ_PRST#
9	MFG_MODE#	Not connected
10	GND	Ground

Note 1. To use the JTAG interface, RZ_DEBUGEN must be high (SW_CONFIG[1] = OFF). If RZ_DEBUGEN is low (SW_CONFIG[1] = ON), the TRST# pin is held low and the JTAG interface will not function.

This connector and its pinout are part of the SMARC specification, but since most JTAG tools require a 9-pin header, the Renesas SMARC JTAG Adaptor is included in the kit.

3.14.1 JTAG Adaptor

The flexi SMARC JTAG Adaptor is required to convert the SMARC specified FPC connection to the 9-pin Cortex debug header.



Figure 3.8 SMARC JTAG Adaptor Top View

To insert the flexi SMARC JTAG Adaptor, first open the FPC connector by lifting the tab from behind. Then insert the flexi cable and close the tab to lock it in place. Ensure the connection is square and made with the flexi contacts facing down.

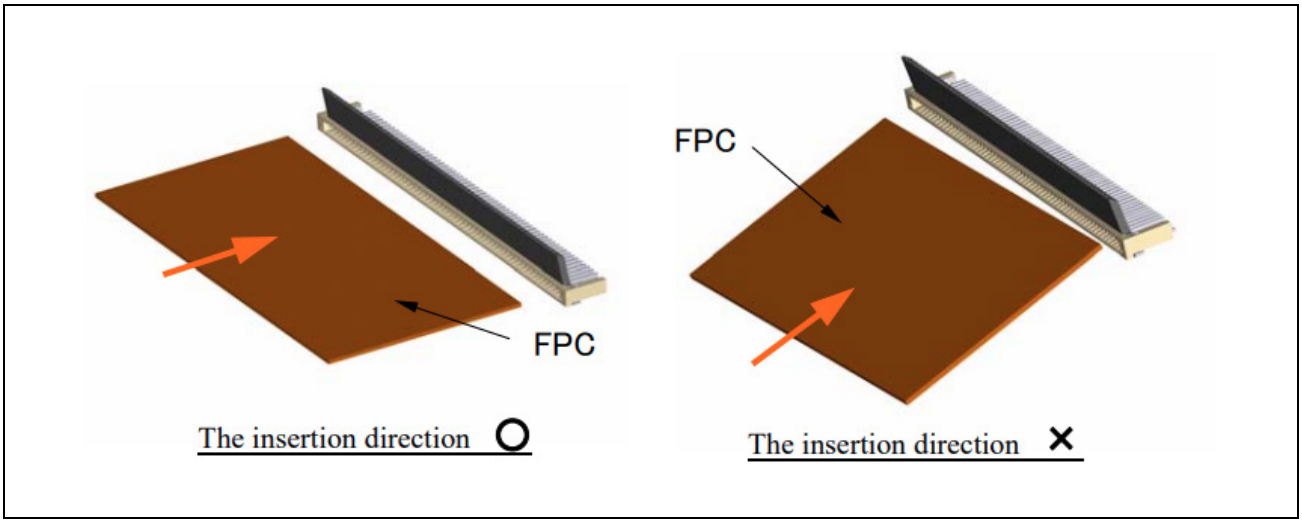


Figure 3.9 Caution When Connecting SMARC JTAG Adaptor to Connector

Table 3.9 JTAG Pin Assignment for SMARC JTAG Adaptor

Cortex 9-Pin Header Pin Number	Module Connection	Module Connection	Cortex 9-Pin Header Pin Number
1	VDD_XSPI (1.8 V)	JTAG_TMS_18	2
3	Ground	JTAG_TCK_18	4
5	Ground	JTAG_TDO_18	6
7	No pin (key)	JTAG_TDI_18	8
9 *1	Ground	RZ_PRST#	10

Note 1. By default, TRST# is not connected and pin 9 is ground. However, resistor options allow TRST# to be connected to pin 9.

3.15 Gigabit Ethernet Interface

Two gigabit Ethernet transceivers with RGMII support are mounted on the G3S SMARC Module.

There are RJ45 connectors to the SMARC Edge connector. Please refer to **Ethernet** for pin assignment.

3.16 Current Monitor

The G3S SMARC Module includes current monitoring circuitry that is accessed through the on-board micro-USB connector.

The current monitoring circuitry is powered from the USB and is completely independent of all other module and RZ/G3S functions.

A software application is required to execute on a host PC and provides current measurements for

- 0.9V_AWO
- 0.9V_ISO
- 1.1V_DDR
- 1.8V_DDR
- VBATT_VDD

Table 3.10 I2C Address Mapping for Current Monitoring

Device	7-bit Address
Renesas ISL28025FR12Z(0.9V_AWO)	0xa0
Renesas ISL28025FR12Z(0.9V_ISO)	0x84
Renesas ISL28025FR12Z(1.1V_DDR)	0x86
Renesas ISL28025FR12Z(1.8V_DDR)	0x9c
Renesas ISL28025FR12Z(VBATT_VDD)	0x9e

3.17 SMARC Edge Connector

In the G3S SMARC EVK, the G3S SMARC Module and the RZ SMARC Carrier II are electrically connected via the SMARC Edge connector. This section describes the RZ/G3S pins and signals on the G3S SMARC Module that can be connected to the SMARC edge connector.

How to read this section

This section provides tables, as shown in **Table 3.11**, which list the connections among “SMARC Signal Name”, “Pin #”, “RZ Port Pin”, and “Signal”. **Figure 3.10** shows these connections on the G3S SMARC Module.

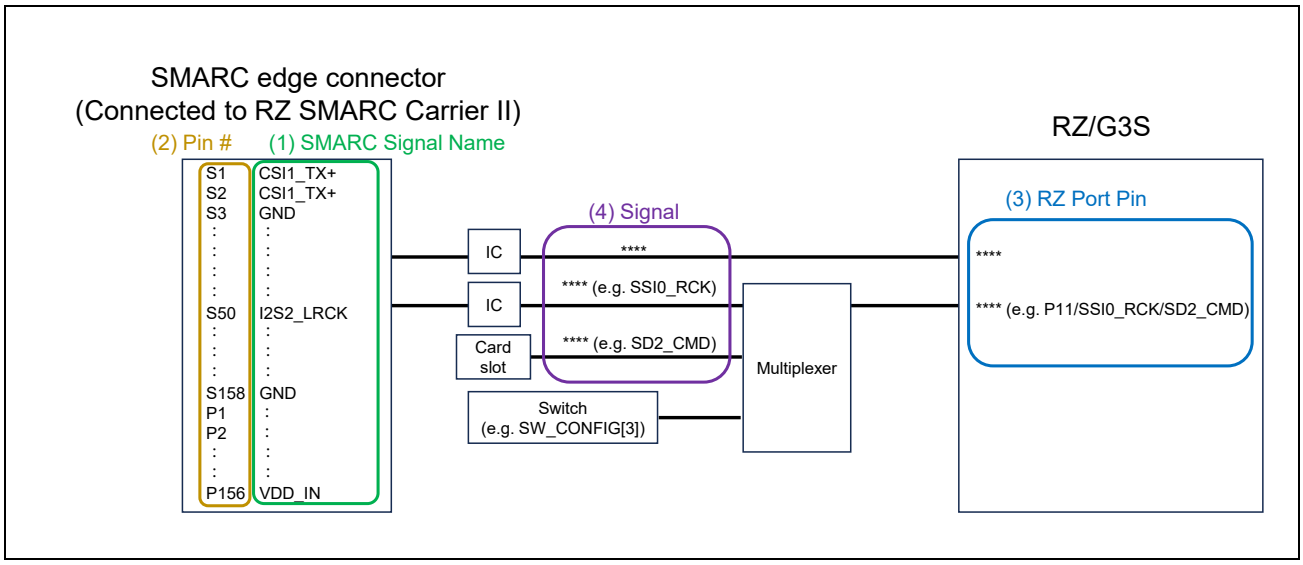


Figure 3.10 Signal Connections on the G3S SMARC Module among “SMARC Signal Name”, “Pin #”, “RZ Port Pin”, and “Signal”

Table 3.11 Examples of the Connections

(1) SMARC Signal Name	(2) Pin #	(3) RZ Port Pin	(4) Signal*1
I2S2_LRCK	S50	P11_1/SSI0_RCK/SD2_CMD	RZ_SSI0_RCK*2
			RZ_SD2_CMD*2
I2S2_SDOUT	S51	P11_2/SSI0_TXD/SD2_DATA0	RZ_SSI0_TXD*2
			RZ_SD2_DATA0*2
I2S2_SDIN	S52	P11_3/SSI0_RXD/SD2_DATA1	RZ_SSI0_RXD*2
			RZ_SD2_DATA1*2
I2S2_CK	S53	P11_0/SSI0_BCK/SD2_CK	RZ_SSI0_BCK*2
			RZ_SD2_CK*2

Note 1. Some RZ port pins are connected to a multiplexer, and the signal connected to the RZ port pin depends on the switch setting.

Note 2. The signal connected to the RZ port pin depends on the SW_CONFIG[3] switch setting on the G3S SMARC Module. The upper entry corresponds to SW_CONFIG[3] = ON, and the lower entry corresponds to SW_CONFIG[3] = OFF.

(1) SMARC Signal Name

"SMARC Signal Name" indicates the signals on the SMARC edge connector. They are described according to the definitions in the SMARC 2.1.1 Specification. Therefore, the signal names do not necessarily correspond to the channel numbers or functional names on the RZ/G3S SoC. For example, in **Table 3.11**, the SSI0_RCK function of the RZ/G3S is connected to I2S2_LRCK (S50) on the SMARC edge connector.

(2) Pin #

The SMARC edge connector consists of two sides: the Primary side and the Secondary side. Pin # refers to the pin numbers on the SMARC edge connector. Pin # on the Primary side are denoted as "Pxx", while those on the Secondary side are denoted as "Sxx". They are also described according to the definitions in the SMARC 2.1.1 Specification.

(3) RZ Port Pin

"RZ Port Pin" indicates the names of the pins on the RZ/G3S SoC that can be connected to the SMARC edge connector. These pin names correspond to those stated in the RZ/G3S User's Manual: Hardware. Appropriate switch settings may be required to enable the connections.

(4) Signal

"Signal" indicates the names of the signals that can be connected to the RZ port pins on the G3S SMARC Module. These signal names are selected to clearly indicate the functional purpose of each signal. Due to the multiplexing configuration, the schematic may be designed such that multiple types of signals can be configured for a single RZ/G3S port pin. In such cases, the configuration based on the default switch settings is highlighted.

3.17.1 Display Interfaces

The RZ/G3S does not support any display interfaces. None of the display signals are connected.

3.17.2 Camera Interfaces

The RZ/G3S does not support any camera interfaces. None of the camera signals are connected.

3.17.3 SDIO Card (4-Bit) Interface

The SDIO signal is routed to the SMARC Edge Connector.

Table 3.12 SDIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SDIO_D0	P39	SD1_DATA0	RZ_SD1_D0
SDIO_D1	P40	SD1_DATA1	RZ_SD1_D1
SDIO_D2	P41	SD1_DATA2	RZ_SD1_D2
SDIO_D3	P42	SD1_DATA3	RZ_SD1_D3
SDIO_WP	P33	—	Not connected
SDIO_CMD	P34	SD1_CMD	RZ_SD1_CMD
SDIO_CD#	P35	P0_2/SD1_CD	RZ_SD1_CD#
SDIO_CK	P36	SD1_CLK	RZ_SD1_CLK
SDIO_PWR_EN	P37	P2_3	RZ_SDIO_PWR_EN
—	—	P4_2	RZ_SD1_PWR_SEL

3.17.4 SPI Interfaces

The SPI1 signal is routed to the SMARC Edge Connector.

The SPI0 signal is not connected to the SMARC Edge Connector.

Table 3.13 SPI0 and SPI1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SPI0_CS0#	P43	—	Not connected
SPI0_CS1#	P31	—	Not connected
SPI0_CK	P44	—	Not connected
SPI0_DIN	P45	—	Not connected
SPI0_DO	P46	—	Not connected
SPI1_CS0#	P54	P15_3/RSPI0_SSL	RZ_RSPI0_SSL
SPI1_CS1#	P55	—	Not connected
SPI1_CK	P56	P15_0/RSPI0_CK	RZ_RSPI0_CK
SPI1_DIN	P57	P15_2/RSPI0_MISO	RZ_RSPI_MISO
SPI1_DO	P58	P15_1/RSPI0_MOSI	RZ_RSPI0_MOSI

3.17.5 Audio

These signals are routed to the SMARC Edge Connector.

Table 3.14 I2S0 and I2S2 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2S0_LRCK	S39	P18_3/SSI3_RCK	RZ_SSI3_RCK
I2S0_SDOUT	S40	P18_4/SSI3_TXD	RZ_SSI3_TXD
I2S0_SDIN	S41	P18_5/SSI3_RXD	RZ_SSI3_RXD
I2S0_CK	S42	P18_2/SSI3_BCK	RZ_SSI3_BCK
AUDIO_MCK	S38	N/A	AUDIO_MCK (clock generator)
I2S2_LRCK	S50	P11_1/SSI0_RCK/SD2_CMD	RZ_SSI0_RCK*1
			RZ_SD2_CMD*1
I2S2_SDOUT	S51	P11_2/SSI0_TXD/SD2_DATA0	RZ_SSI0_TXD*1
			RZ_SD2_DAT0*1
I2S2_SDIN	S52	P11_3/SSI0_RXD/SD2_DATA1	RZ_SSI0_RXD*1
			RZ_SD2_DATA1*1
I2S2_CK	S53	P11_0/SSI0_BCK/SD2_CK	RZ_SSI0_BCK*1
			RZ_SD2_CK*1
AUDIO_MCK	S38	N/A	AUDIO_MCK (clock generator)

Note 1. SW_CONFIG[3] switch option on the G3S SMARC Module

3.17.6 I2C Interfaces

The I2C_GP and I2C PM signals are routed to the SMARC Edge Connector.

The I2C_CAM0, I2C_CAM1, and I2C_LCD signals are not connected to the SMARC Edge Connector.

Table 3.15 I2C_GP and I2C_PM Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2C_GP_CK	S48	RIIC0_SCL	RZ_RIIC0_SCL
I2C_GP_DAT	S49	RIIC0_SDA	RZ_RIIC0_SDA
I2C_PM_CK	P121	RIIC1_SCL	RZ_RIIC1_SCL
I2C_PM_DAT	P122	RIIC1_SDA	RZ_RIIC1_SDA

NOTE

RZ_RIIC1 bus is also used on the G3S SMARC Module itself for:

- Power/Reset Control: SLG7RN46131
- PMIC: RAA215300A2GNP#HA3
- Power Regulator: SLG7RN46420
- Clock Generator: 5L35023B-615NLGI

3.17.7 Asynchronous Serial Ports

The SER0, SER1, and SER3 signals are routed to the SMARC Edge Connector.

The SER2 signal is not connected to the SMARC Edge Connector.

Table 3.16 SER0, SER1, SER2, and SER3 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SER0_TX	P129	P14_0/SCIF1_TXD	RZ_SCIF1_TXD
SER0_RX	P130	P14_1/SCIF1_RXD/SD2_CD	RZ_SCIF1_RXD*1
			RZ_SD2_CD*1
SER0_RTS#	P131	P16_1/SCIF1_RTS#	RZ_SCIF1_RTS#
SER0_CTS#	P132	P16_0/SCIF1_CTS#	RZ_SCIF1_CTS#
SER1_TX	P134	P17_3/SCIF3_TXD	RZ_SCIF3_TXD
SER1_RX	P135	P17_2/SCIF3_RXD	RZ_SCIF3_RXD
SER2_TX	P136	—	Not connected
SER2_RX	P137	—	Not connected
SER2_RTS#	P138	—	Not connected
SER2_CTS#	P139	—	Not connected
SER3_TX	P140	P6_4/SCIF0_TXD	RZ_SCIF0_TXD
SER3_RX	P141	P6_3/SCIF0_RXD	RZ_SCIF0_RXD

Note 1. SW_CONFIG[3] switch option on the G3S SMARC Module

3.17.8 CAN Bus

These signals are routed to the SMARC Edge Connector.

Table 3.17 CAN0 and CAN1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
CAN0_TX	P143	P6_1/CAN0_TX	RZ_CAN0_TX
CAN0_RX	P144	P6_2/CAN0_RX	RZ_CAN0_RX
CAN1_TX	P145	P17_0/CAN1_TX	RZ_CAN1_TX
CAN1_RX	P146	P17_1/CAN1_RX	RZ_CAN1_RX

3.17.9 USB Interfaces

The USB channel 0 and 1 signals are routed to the SMARC Edge Connector.

The USB channel 2, 3, 4, and 5 signals are not connected to the SMARC Edge connector.

Table 3.18 USB0 and USB1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
USB0+	P60	—	RZ_USB0_DP
USB0-	P61	—	RZ_USB0_DM
USB0_EN_OC# *	P62	P5_0/USB0_VBUSEN	RZ_USB0_VBUSEN
		P5_2/USB0_OVRCUR	RZ_USB0_OVRCUR#
USB0_VBUS_DET	P63	—	RZ_USB0_VBUSIN
USB0_OTG_ID	P64	P5_3/USB0_OTG_ID	RZ_USB0_OTG_ID
USB1+	P65	—	RZ_USB1_DP
USB1-	P66	—	RZ_USB1_DM
USB1_EN_OC# *1	P67	P6_0/USB1_VBUSEN	RZ_USB1_VBUSEN
		P5_4/USB1_OVRCUR	RZ_USB1_OVRCUR#

Note 1. Logic circuitry is used to provide independent enable and overcurrent IO.

3.17.10 PCI Express

The PCIE_A signal is routed to the SMARC Edge Connector.

The PCIE_B, PCIE_C, and PCIE_D signals are not connected to the SMARC Edge Connector.

Table 3.19 PCIE_A Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
PCIE_A_TX+	P89	PCIE_TX_DP	PCIE_A_TX+
PCIE_A_TX-	P90	PCIE_TX_DN	PCIE_A_TX-
PCIE_A_RX+	P86	PCIE_RX_DP	PCIE_A_RX+
PCIE_A_RX-	P87	PCIE_RX_DN	PCIE_A_RX-
PCIE_A_REFCK+	P83	PCIE_REFCLKP0	RZ_PCIE_REFCLK+
PCIE_A_REFCK-	P84	PCIE_REFCLKN0	RZ_PCIE_REFCLK-
PCIE_A_RST#	P75	P13_2/PCI_RST_OUT_B	PCIE_A_RST#
PCIE_A_CKREQ#	P78	P13_3/PCI_CLKREQ_B	PCIE_A_CKREQ#

3.17.11 SATA

The RZ/G3S does not support SATA interfaces. None of the SATA signals are connected.

3.17.12 Ethernet

These signals are routed to the SMARC Edge Connector.

Table 3.20 GBE0 and GBE1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET0_xxx
GBE0_LINK100#	P21	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK1000#	P22	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK_ACT#	P25	N/A	ET0_LED1 (ET0 PHY)
GBE0_CTREF	P28	—	Not connected
GBE0_SDP	P6	—	Not connected
Ethernet PHY0 Interrupt	n/a	P12_0/IRQ0/SD2_DATA2	ET0_INT# (RZ_IRQ0) *1
			RZ_SD2_DATA2*1
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET1_xxx
GBE1_LINK100#	S19	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK1000#	S22	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK_ACT#	S31	N/A	ET1_LED1 (ET1 PHY)
GBE1_CTREF	S28	—	Not connected
GBE1_SDP	P5	—	Not connected
Ethernet PHY1 Interrupt	n/a	P12_1/IRQ1/SD2_DATA3	ET1_INT# (RZ_IRQ1) *1
			RZ_SD2_DATA3*1

Note 1. SW_CONFIG[3] switch option on the G3S SMARC Module

3.17.13 GPIO

Table 3.21 GPIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GPIO0	P108	—	Not connected
GPIO1	P109	—	Not connected
GPIO2	P110	—	Not connected
GPIO3	P111	—	Not connected
GPIO4 *1	P112	P18_0/IRQ2	RZ_IRQ2_GPIO4
		TAMPIN	RZ_TAMPIN
GPIO5	P113	P13_4	RZ_P13_4_GPIO5
GPIO6	P114	P0_1	RZ_P0_1_GPIO6
GPIO7	P115	P0_3	RZ_P0_3_GPIO7
GPIO8	P116	P13_0	RZ_P13_0_GPIO8
GPIO9	P117	P13_1	RZ_P13_1_GPIO9
GPIO10	P118	P18_1/IRQ3	RZ_IRQ3_GPIO10
GPIO11	P119	P14_2	RZ_P14_2_GPIO11
GPIO12	S142	P8_2	RZ_P8_2_GPIO12
GPIO13	S123	P8_3	RZ_P8_3_GPIO13

Note 1. GPIO4_SEL switch option on the G3S SMARC Module

4. Certifications

The G3S SMARC Module comprising the G3S SMARC EVK meets the following certification/standards. See page 3 of this user's manual for the disclaimer and precautions.

4.1 EMC/EMI Standards

- FCC Notice (Class A)

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

[NOTE] — This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
  CAN ICES-3 (A)/NMB-3(A)
- CE Class A (EMC)

This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

[Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)

This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

[Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

4.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013



For customers in the UK & European Union the WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at;
https://www.renesas.com/en/support/regional-customer-support/weee

4.3 Safety Standards

- UL 94V-0

REVISION HISTORY	RZ/G3S SMARC Module Board User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 14, 2023	—	First edition issued
1.10	Nov. 20, 2024	All	As RZ/G3S SMARC EVK, RTK9845S37S01000BE which is equipped with R9A08G045S37GBG (for which the security is supported) was added.
		13	Figure 2.3 was modified.
		14, 15	Table 2.1 was modified.
		18	Table 2.4 was modified.
		20	Figure 3.1 was modified.
		21	Figure 3.2 was added.
		22	Figure 3.3 was added.
		23	Figure 3.4 was modified.
		24	Figure 3.5 was modified.
1.11	June 25, 2025	10	The information about the RZ/G3S SMARC Module PCB design revisions was added.
		13	Figure 2.3 was modified.
		18	Table 2.4 was modified.
		20	Figure 3.1 was modified.
		21	Figure 3.2 was modified.
		22	Figure 3.3 was modified.
1.20	Nov. 12, 2025	8	1. Introduction Table 1.1 was modified.
		9	1.1 Kit Contents Some descriptions and Figure 1.2 were modified.
		11	2. System Description Some descriptions, as well as Figure 2.1 and Figure 2.2, were modified.
		12	2.1 G3S SMARC EVK Functional Block Figure 2.3 was modified.
		13, 14	2.2 G3S SMARC EVK Interface Mapping Table 2.1 was modified.
		24	3.8 microSD0 Card Interface Section title and Table 3.2 were changed.
		25	3.9 microSD1 Card Interface Added
		25	3.10 microSD2 Card Interface Section title, some descriptions, and Table 3.4 were changed.
		38, 39	4. Certifications Added
2.00	July 08, 2026	11	1.3 Ordering Information Added. Table 1.2 was moved to this section and the information on how to distinguish the PCB design revisions was added.
		14 to 16	2.2 G3S SMARC EVK Interfaces Mapping Table 2.1 was modified.
		26, 27	3.8 microSD0 Card Interface A note on the specification restriction and countermeasure for eSD boot was added.
		34, 35	3.17 SMARC Edge Connector "How to read this section" was added.

RZ/G3S SMARC Module Board User's Manual: Hardware

Publication Date: Rev.1.00 Nov. 14, 2023
Rev.2.00 July 08, 2026

Published by: Renesas Electronics Corporation

RZ/G3S SMARC Module Board

Renesas Electronics Corporation

R01UH1076EJ0200