

APPLICATION NOTE

RZ/A2M Smart Configurator

User's Guide: e² studio

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Introduction

This application note describes the basic usage of the RZ/A2M Smart Configurator (hereafter called the Smart Configurator), which is an e^2 studio plug-in tool.

References to the e² studio integrated development environment in this application note apply to the following versions.

• e² studio 7.3.0 and later

Target Devices and Compilers

Refer to the following URL for the range of supported devices and compilers:

https://www.renesas.com/smart-configurator

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1. Overview

1.1 Purpose

This User's Guide describes the basic usage of the Smart Configurator and the e² studio integrated development environment, including the procedure for creating a project.

Refer to the User's Manual of the e² studio for how to use the e² studio.

1.2 Features

The Smart Configurator is a utility for combining software to meet your needs. It handles the following three functions to support the embedding of drivers, middleware and RTOS from Renesas in your systems: importing software package and making pin settings.

1.3 RZ/A2M Software Core Package

The RZ/A2M Software Core Package consists of driver, middleware and RTOS. By using this software package, you can easily use the functions in RZ/A2M



2. Creating a Project

The following describes the procedure for creating a C project using the Smart Configurator.

(1) Start e² studio and launch a workspace. Select [File] \rightarrow [New] \rightarrow [C/C++ Project] to activate the project creation wizard.

	e²	worksp	ace - e² s	tudio									
1)	File	Edit	Source	Refactor	Navigate	Search Proj	ct Re	enesas Views	Run	Window	Help		
2)		New				Alt+Shift+N	> 📬	RZ Linux C/0	C++ pro	ject			
		Open	File				Ť	Synergy C/C	C++ Proj	ject			
		Open	Projects	from File Sy	stem		C.	Makefile Pro	oject wit	h Existing	Code		
		Close				Ctrl+W	C	C/C++ Proje	ect)			
		Close	All			Ctrl+Shift+W	D	Project		(3)			
		Save				Ctrl+S	C++	Convert to a	C/C++	Project (Adds C/C+	+ Nature)	
		Save A	As			Curro .	63	Source Fold	er				
		Save A	AII			Ctrl+Shift+S	<u></u>	Folder					
	100	Rever	t				C	Source File					
		Move					ĥ	Header File					
		Renar				F2	Ľ	File from Te	mplate				
	8	Refres				F5	G	Class					
	Ф <u> </u>			elimiters To			, °	Code Genera	ator				
						Ctrl+P		Other					Ctrl+N
	ł	Print	•			Ctri+P	ia	uration se	tting	5			
	è	Impor	t					iercely conte			es		
	⊿	Export	t										
		Prope	rties			Alt+Enter							
		Switch	n Worksp	ace			> 1	ile					
		Restar	ť				file	system					
		Exit											
	_												

Figure 2-1 Creating a New Project

(2) In the project creation wizard, please operate until you see the [Select Coding Assistant Settings].



(3) In the [Select Coding Assistant settings] dialog box, select the [Smart Configurator] checkbox and click on the [Finish] button.

	e ²			\times
	New Renesas CC-RX Executable Project Select Coding Assistant settings			\$
(1)				
(1)	Smart Configurator Use Peripheral Code Generator			
	Use FIT Module Download FIT Modules			
	Smart Configurator is a single User Interface that combines the functionalities of Code Generator and FIT Cor imports, configures and generates different types of drivers and middleware modules. Smart Configurator encompasses unified clock configuration view, interrupt configuration view and pin conf Hardware resources conflict in peripheral modules, interrupts and pins occurred in different types of drivers a modules will be notified. (Smart Configurator is available only for the supported devices)	iguration	view.	
	User Application			
	User Application Driver and Middleware Driver Code Configured in GUI and Generated MCU Hardware			
	MCU Hardware			
	(2)			
	? < Back Next > Finish		Cancel	

Figure 2-2 Selecting the Coding Assistant Tool

(4) Wait for completion of project creation.

Progress Information	
Smart Configurator operation in progress	
Loading data for Smart Configurator editor	
	Cancel

Figure 2-3 Smart Configurator Starts File Generation



(5) After a new C Project is successfully created, the project will be opened in the Smart Configurator perspective.

File Edit Navigate Search Project RenesarViews Run Window Help				
🔨 🎓 🔳 ֆ Debug 🗸 🔽 Smart_Configurator_Example Hand V 🔅 🖸 * 📓 🔞 📎 * 🖏 🐇 New Connection 🔍 以 対 副 🛔 👔 🔍 💷 📾 📾 🕺 〇 毛 ズ 偽 * 物 🗈 💷 🖄 🖉 🍏 🥙 🍎 * 🗛 * 🎯 🏈 *				
N + (i) + U + V + V + U + U + U + V + U + U + U	ifigurator 20 Debug			
> 🖉 Smart, Configurator, Example	Default Board			
- General Information				
This effort allows you to modify the settings stored in configuration file (setg)				
Allow clock configuration Application under				
Corporation - Comparents - Comp				
Allow software component selection and configuration model ware				
driver RTOS RENESAS				
Pins Allow agreent join contrauration and join contrauration for stretced apfearse component + * Fins + * Fins + * *				
MMV Allow MUL configuration				
- Current Configuration	R4 R6 R6 r- -			
Soliced board/arcice: ET5521368 (AbM size 4M); Pin count: 244, CPU Conter 44; Mais: Freq 243MHz)				
deckid componentsi				
Composet Vesio Configuration International Configuration EXACTL				
Low concentration REALED				
				
Overview Clocks Components Plins MMU + Legend				
🖸 Conside 🔅 🕹 🚯 🕼 🖾 📰 🐘 🛃 💭 🔹 🖄 👘 💭 🕶 🖄	∌ ⊽ = □			
CDT Build Console (RZA2M) 0 tems				
Description Type				

Figure 2-4 Smart Configurator Perspective



3. Operating the Smart Configurator

3.1 Procedure for Operations

Figure 3-1 shows the procedure for using the Smart Configurator to set up peripheral modules and build the project with the e^2 studio. Refer to the related documents on the e^2 studio for the operation of the e^2 studio.



Figure 3-1 Procedure for Operations



3.2 Displaying the Smart Configurator Perspective

To fully utilize Smart Configurator features, ensure that the Smart Configurator perspective is opened. If it is not opened, select [Window] \rightarrow [Perspective] \rightarrow [Open perspective] \rightarrow [Other...] to open the [Open Perspective] dialog box.

In the [Open Perspective] dialog box, select [Smart Configurator] and click on the [Open] button, change to the Smart Configurator perspective.

	Quick Access	
e ² Open Perspective	— 🗆	Х
EC/C++ (default)		
Code Generator		
* Debug		
🐉 Java		
🕵 Java Browsing		
Java Type Hierarchy		
🐜 LTTng Kernel		
Remote System Explorer		
Resource		
Smart Configurator		
Synergy Configuration		
Target Explorer		
E ⁰ Team Synchronizing		
Er Tracing		
	_	
Oper	n Cancel	

Figure 3-2 Opening the Smart Configurator Perspective



3.3 Window

The configuration of the Smart Configurator perspective is shown in Figure 3-3, Smart Configurator Perspective.

figurato Example/Smart_Config						3), 4	- ø ×
	Run Window Help				A10 8		
	nart_Configurator_Example Hard 🗸 🧔	E : 🗖 • 🔟	🐘 🕤 👻 🐔 🐂 🔝 🚅 New Connection 🔍 🕅 👪 🖛 🔛 💷		* ゆ + も m m h む な 母 雪 		
○ ■ □ 適当		-				cess 🗄 😭 😨 C/C++ 🧔 Smar	rt Configurator 🎄 Debug
		R_r_startup_con	lig.h 💽 Smart_Configurator_Example_main.c	- 0			5
or_Example	erview information			1 di 🖞	🖺 🔺 🔎 🔎 🖻 🖻	Type pin function O Assign	ned 🔘 Default Board
	General Information			0			
т	his editor allows you to modify the setti	ings stored in cor	figuration file (.scfg)				
	iocks						
^	llow clock configuration		Application under development				
	omponents		+ Components				
A	llow software component selection and	l configuration	Device				
	ins.		driver RIOS			RENESAS	
	llow general pin configuration and pin-	configuration for	selected software component				
	IMU					· · · · · · · · · · · · · · · · · · ·	
	Ilow MMU configuration					540 MA MA 942 502	NO 163 163 163
	,					ten has has ten ten	
	Current Configuration					(m) (m) (m) (m)	
		size: 4MB, Pin co	unt: 324, CPU: Cortex+A9, Max. Freq: 528MHz)			Van No. No. Van	
	elected components:				• • • • • • • • •	NH NH NH NH NH	
	Component S r.ostm	Version	Configuration ostm.reserved(OSTM≥ used)				
	♥ r_ostm	1.01	ostm_reserved(OSTM2: used)				
					- 6 6 9 9 9 9 9 9		D 100 100 100 100 100 1
					14 (PL) (14 PL) PL PL PL PL PL PL PL		
L							
Ove	view Clocks Components Pins MM	U			▶ Legend		
		4	🗟 🗘 🔀 🖾 🗁 🗟 📑 🗳 🐨 🗂 📲 🚨 Configuration Problem	22			∌ ⊽ = □
0			Ditems	Туре			
			Description	type			
			> ¹				
							3
		\sim			\sim		
		~ ~	5)		(6)		

Figure 3-3 Smart Configurator Perspective

- 1) Project Explorer
- 2) Smart Configurator view
- 3) MCU Package view
- 4) MMU Layout view
- 5) Console view
- 6) Configuration Problems view



3.3.1 Project Explorer

The structure of the folders in the project is displayed in a tree form.



Figure 3-4 Project Explorer

When the Project Explorer is not opened, select [Window] \rightarrow [Show View] \rightarrow [Other] from the e² studio menu and select [General] \rightarrow [Project Explorer] on the opened [Show View] dialog box.



3.3.2 Smart Configurator view

The Smart Configurator view consists of six pages: [Overview], [Clocks], [Components], [Pins] and [MMU]. Select a page by clicking on a tab; the displayed page will be changed.

🔅 Smart_Configurator_Example.scfg 🔀	h r_startup_config	g.h 💽 Smart_Configurate	or_Example_main.c	
Overview information				🔁 🖻
← General Information				?
This editor allows you to modify the set	ttings stored in config	guration file (.scfg)		
Clocks				
Allow clock configuration			Application under development	
Components				-Compone
Allow software component selection ar	nd configuration		Device	
			driver RTOS	J
Pins				- Pins
Allow general pin configuration and pi	n configuration for se	elected software component		
MMU				
Allow MMU configuration				
Current Configuration				
Selected board/device: R7S921058 (RAI	Misize: 4MB. Pin cour	nt: 324 CPU: Cortex-A9 Max. F	reg: 528MHz)	
Selected components:			req: 525(11)(2)	
Component	Version	Configuration		
✓ r_ostm	1.01	ostm_reserved(OSTM2: use	ed)	
Overview Clocks Components Pins M	MU			~

Figure 3-5 Smart Configurator View

When this view is not opened, right-click on the project file (*.scfg) in the Project Explorer and select [Open] from the context menu.



3.3.3 MCU Package view

The states of pins are displayed on the figure of the MCU package. The settings of pins can be modified from here.





When this view is not opened, select [Renesas Views] \rightarrow [Smart Configurator] \rightarrow [MCU Package] from the e² studio menu.



3.3.4 MMU Layout view

The MMU Layout view displays memory map reflected from setting by MMU page.



Figure 3-7 MMU Layout View

When this view is not opened, select [Renesas Views] \rightarrow [Smart Configurator] \rightarrow [MMU Layout] from the e² studio menu.



3.3.5 Console view

The Console view displays details of changes to the configuration made in the Smart Configurator or MCU Package view.

📮 Console 🛛	🖹 📑 🖻 📑 🚍 🕶 🗖 🗖	j
Smart Configurator Output		
M05000001: Pin 24 is assigned to EXTAL		~
M05000001: Pin 22 is assigned to XTAL		
M00000001: Code generation is started		
M03000002: File generated:src\smc_gen\general\r_smc_cgc.c		
M03000002: File generated:src\smc_gen\general\r_smc_cgc.h		
M03000002: File generated:src\smc_gen\general\r_smc_cgc_user.c		
M04000001: File generated:src\smc_gen\r_bsp_v3.80.zip		
M04000001: File generated:src\smc_gen\general\r_cg_macrodriver.h		U
MOX000001. F31. [2	Ċ

Figure 3-8 Console View

When this view is not opened, select [Window] \rightarrow [Show View] \rightarrow [Other] from the e² studio menu and select [General] \rightarrow [Console] on the opened [Show View] dialog box.

3.3.6 Configuration Problems view

The Configuration Problems view displays the details of conflicts between pins.

Configuration Problems Configuration Config		† ₽	~ •	
0 items				
Description	Туре			

Figure 3-9 Configuration Problems View

When this view is not opened, select [Renesas Views] \rightarrow [Smart Configurator] \rightarrow [Configuration Problems] from the e² studio menu.



4. Setting of Peripheral Modules

You can select peripheral modules from the Smart Configurator view.

4.1 Clock Settings

You can set the system clock on the [Clocks] tabbed page. The settings made on the [Clocks] page are used for software package.

Follow the procedure below to update the device setting in the project properties.

- (1) Select the MD_CLK input level and set the input clock frequency.
- (2) Select the dividing ratio on divider 1.
- (3) Select the dividing ratio on divider 2.
- (4) Select the clock source for output clock by multiplexer switches.
- (5) Check the output clock frequency.



Figure 4-1 Clock settings



4.2 Component Settings

Drivers and middleware can be combined as software components on the [Components] page. Added components are displayed in the Components tree at the left of the page.

oftware component config	Julation		۱
omponents 🛛 🎝 🔁 🖽 🛟 🔻	Configure		
type filter text	Property	Value	
	# Mode	Interval	
V 🗁 Drivers	# Counter format	ms	
🗸 🗁 Timers	# Counter value	1	
💣 ostm_reserved	# Start interrupt	Unused	
	# Interrupt Setting	Used	
	# Interrupt priority level(0 ~ 31)	30	
	# Interrupt function	os_abstraction_isr	
	✓ I Resources		
	V 📵 OSTM		
	OSTM2		
	Components tree		^

Figure 4-2 [Components] Page

4.2.1 Downloading a Software Core Package

You need to download a desired Software Core Package from the Renesas Electronics website. The Software Core Package can be used as a software component after downloading.

(1) Click on the [* (Add component)] icon.

Components $\downarrow^{a}_{Z} \boxdot \boxdot \ddagger$	▶ ▼
(1) 💼	
type filter text	
 Communications 	^
scifa0	
 Timers ostm_reserved 	
🗸 🗁 Middleware	
✓	
•	
	~

Figure 4-3 Adding a Software Component



(2) Click the [Download more software components] link in the [Software Component Selection] page of the [New Component] dialog box to download a software core package

Figure 4-4 Downloading More Software Components

Note: This service requires login to "My Renesas". If you have not logged in, the following dialog box will prompt you to log in. To register as a new user, click on the [About My Renesas] button.

e ² My Renesas			×
My Renesas			
Enter the e-mail address They allow you to down	and password that you registered for My Renesas. load documents and software by using Smart Browser.		
_			
Email Address:			
Password:			
	isas account to use our tool download services, receive Newsletter / Update Notice, and take advantage of our other services. Renesas] to register it.		
	About	t My Renesas OK Cance	1

Figure 4-5 Login to My Renesas



- (3) Select the checkbox of the required module in the [Core Software Download] dialog box.
- (4) Click on [Browse...] to select the location where the downloaded module is to be stored.
- (5) Click on [Download] to start downloading the selected core software.

	e ²	Package Download					×
		ct the core packages for download				Ľ	5
		Title	Document No.	Rev.	Issue date	Sele	ct All
4) (RZ/A2M Group Software Core Package	R01AN4583JJ0200	Rev.2.00	2018/12/28	Desel	ect All
						(5)	
Γ		lule Folder Path:					
		C:¥Users¥a5090534¥.eclipse¥org.eclipse.platform_dow	nload¥RZ_Modules			Brow	se
				(6)	Download	Cance	I

Figure 4-6 Downloading a core software



4.2.2 Adding software component

- (1) Click on the [(Add component)] icon.
- (2) Select components from the list in the [Software Component Selection] page of the [New Component] dialog box (e.g. r_scifa). Two or more components can be selected by clicking with the Ctrl key pressed.
- (3) Click on [Next].

_				
Type A				
Function A				
Filter				
Componer	nts	Version		
tr_ether		1.00		
🌐 r_jcu		1.02		
🖶 r_mipi		1.00		
r_ostm		1.01		
⊞ r_png ⊞ r_rga		1.02		
⊞ r_riic		1.02		
⊕ r_rvapi		1.01		
r_scifa		1.01		
tr_vdc		1.01		
Description Dependent SCIFA Drive	ly latest version cy : r_cbuffer vers er nore software co			
	eneral settings	mponents		

Figure 4-7 Adding software component

- (4) Set a configuration name of adding software component and change a resource in the [Add new configuration for selected component] page of the [New Component] dialog box .
- (5) Click on [Finish].

			×
dd new configurat	ion for selected component		}
r_scifa (4	.)		
- Configuration name	scifa0		
Resource:	SCIFA0		~
r_cbuffer			
Configuration name	cbuffer0		
Resource:	r_cbuffer		~

Figure 4-8 Changing configuration name and resource for software component

The selected software component will be added to the components tree.

By code generating, the source files are added to the project.



4.2.3 Removing a software component

Follow the procedure below to remove a software component from a project.

- (1) Select a software component from the Components tree.
- (2) Click on the $\begin{bmatrix} 1 \\ 1 \end{bmatrix}$ (Remove component)] icon.

Components da Carta (2)	* *
type filter text	
	*

Figure 4-9 Removing a Software Component

The selected software component will be removed from the Components tree.

This operation will also remove the source files generated for this component from the Project Explorer.



4.2.4 Setting a Software Component

Follow the procedure below to set up a software component.

- (1) Select a software component from the Component tree (e.g. r_scifa).
- (2) Setting a software component and select a pin function on configure page.



Figure 4-10 Settings for scifa

The software component setting will be generated to configuration header files. (When r_scifa, generate to r_scifa_drv and sc_cfg,h)

The pin function setting will be generated to GPIO configuration header files. (Generate to $r_gpio_drv.h$ and $sc_cfg.h$)



4.2.5 Changing the name for a software component

Follow the procedure below to change the name for a software component.

- (1) Right-click on a software component.
- (2) Select [Rename] from the context menu.
- (3) Enter a new name in the [Rename Configuration] dialog box (e.g. change scifa0 to scifa1).
- (4) Click on [OK].

Components	
	ت ت
type filter text	
🗸 🗁 Drivers	
V 🗁 Commun	
(1) scifa1	Change resource Change version
v ⊖ Ge ×	Remove Duplicate
(2)	Rename
	Reset to default

Figure 4-11 Renaming the Configuration



Figure 4-12 Enter the component name

4.2.6 Changing the resource for a software component

The Smart Configurator enables you to change the resource for a software component (e.g. from SCIFA0 to SCIFA1). Compatible settings can be ported from the current resource to the new resource selected.

Follow the procedure below to change the resource for an existing software component.

- (1) Right-click on a software component (e.g. scifa0).
- (2) Select [Change resource] from the context menu.

Components	.ª₂ 🖻 🕀 📫 🕇 ▼
	ت ن
type filter text	
✓ ➢ Commun (1) ➢ scifa1	ications
	Change resource Change version
✓ 🧁 Middle ✓ 🗁 Ge 🗱	Remove
e 🖥	Duplicate Rename
	Reset to default

Figure 4-13 Changing the Resource

- (3) Select a new resource (e.g. SCIFA1) in the [Resource Selection] dialog box.
- (4) The [Next] button will be active; click on it.

e ² Change R	esource		_		×
Resource Se	lection				
Select resou	ce from those available in the list				
Resource:	SCIFA1				\sim
(3)	SCIFA1 SCIFA2 SCIFA3 SCIFA4				
?	< Back(4) Next >	Finish		Cancel	

Figure 4-14 Components Page – Selecting a New Resource



- (5) Configuration settings will be listed in the [Configuration setting selection] dialog box.
- (6) Check the portability of the settings.
- (7) Select whether to use the listed or default settings.
- (8) Click on [Finish].

Confirm setting for resource change	● Use current setting ○ l	Use default setting
Setting	Current Value	Default Value
SCIFA communication modes	Asynchronous mode	Asynchronous mode
SCIFA Bit Rate (bps)	115200	115200
Clock select	Internal clock input	Internal clock input
Asynchronous Base Clock Select	Use clock as 16x mode	Use clock as 16x mode
Data Bit Length	8 Bits	8 Bits
Parity Enable	Unused	Unused
Parity Mode	Even Parity	Even Parity
Stop Bit Lenght(s)	1 bit	1 bit
Noise Cancellation	Unused	Unused
Data Transfer Direction Select	LSB-first	LSB-first
I and back and	(Income of the second se	Universit

Figure 4-15 Checking the Settings of the New Resource



4.2.7 Changing the version of Software Component

Follow the procedure below to change the version for an existing software component.

- (1) Right-click on a software component (e.g. scifa0).
- (2) Select [Change version] from the context menu.

Components	
	te 😜
type filter text	
V 🗁 Drivers	ications
(1) scifat	
🗸 🗁 Tin	Change resource
	Change version
✓ → Ge	Remove
e 🗈	Duplicate
	Rename
	Reset to default

Figure 4-16 Changing the version

- (3) Select a new version (e.g. 1.01) in the [Version Selection] dialog box .
- (4) Click on [Next].

e ² Change Version						_		\times
Version Selection	1							
Select available ver	rsion							
Component name:	r ssifa							
	r_scila							
Current version:	1.00							
(3) Available versions:	1.01							\sim
	1.01							
		(4)		<u> </u>				
(?)	< Back		Next >	J	Finish		Cance	I

Figure 4-17 Selecting the available version



(5) Check the portability of the settings and click in [Finish].

e ² Change Version	_		×
Setting Overview			
The following settings will be added or removed			
Setting		Status	
There are no differences			
2			
(5)			
? < Back Next >	Finish	Cance	9

Figure 4-18 Information of changing items

(6) Click on [Yes].

e ² Cha	nge Version	\times
	Confirm to change version and proceed to generate code	
	(7) Yes No	

Figure 4-19 Confirm to change version

(7) Software component version is changing and code is generated automatically.



4.3 Pin Settings

The [Pins] page is used for assigning pin functions. You can switch the view by clicking on the [Pin Function] and [Pin Number] tabs. The [Pin Function] list shows the pin functions for each of the peripheral functions, and the [Pin Number] list shows all pins in order of pin number.

# *Smart_Configurator_Example.scfg ⊠	up_config.h	C Smart_C	Configurator_Example_main.c				
Hardware Resource 🗉 🗐 🛓 🖧	Pin Function					2 🗉 🖬	24
Type filter text	type filter t	ext				All	\sim
Type filter text Image: SciFA0 SCiFA1 SCiFA3 SCiFA4 SCiFA4 SCiFA4 SCiFA3 SCiFA4 SCiFA1 SCiFA3 SCiFA4 SCiFA1 SCiFA4 SciFA RilC0 RilC1 RilC2 SiF1 SSIF2 SSIF2 SSIF3 CANFD0 CANFD1 CANFD0 CANFD1 CANFD0 RSP10 CANFD1 RSP12 SSIF1 SSIF2 SSIF2 SSIF2 SSIF2 SSIF2 SSIF2 SSIF2 SSIF2 SSIF2 <th>Enabled</th> <th>ext Function CTS1# RTS1# RxD1 SCK1 TxD1</th> <th>Assignment PT_S/CKE/DRP08/DV0_DATA1/C Not assigned P_T_1/RD/WR#/DRP05/DV0_VS/ PJ_0/TRACECLK/SPDIF_OUT/SC PT_3/RAS#/DRP06/DV0_HSYNC</th> <th>Not assignedL19K4</th> <th>Direction IO None I O O</th> <th>All Remarks I</th> <th>×</th>	Enabled	ext Function CTS1# RTS1# RxD1 SCK1 TxD1	Assignment PT_S/CKE/DRP08/DV0_DATA1/C Not assigned P_T_1/RD/WR#/DRP05/DV0_VS/ PJ_0/TRACECLK/SPDIF_OUT/SC PT_3/RAS#/DRP06/DV0_HSYNC	Not assignedL19K4	Direction IO None I O O	All Remarks I	×
Pin Function Pin Number							

Figure 4-20 [Pins] Page ([Pin Function])

Number								a 🖂
/pe filter text							All	
Pin Number	Pin Name	Function	Direction	Output Level	Interrupt	Drive Control	Initialize	Remai
K12	Vss	Vss	-	-	-	-	-	Read o
K13	Vss	Vss	-	-	-	-	-	Read o
K14	Vcc	Vcc	-	-	-	-	-	Read of
K19	P9_7/A15/DRP09/DV0_DATA2/SD1_WP	Not assigned	None	None	None	None	None	
K20	PG_1/ET0_TXD2/VIO_D9/MOSI0/MTIOC3C/HM_INT#/	Not assigned	None	None	None	None	None	
K21	P7_5/CKE/DRP08/DV0_DATA1/CTS1#/OVRCUR1	/ CTS1#	ю	None	/ Disabled	4mA	By GPIO Init	
K22	PG_2/ET0_TXD3/VIO_D10/MISO0/MTIOC3B/GTIOC0A/	Not assigned	None	None	None	None	None	
L1	PVcc	PVcc	-	-	-	-	-	Read of
L2	P0_1/D1/DRP25/DV0_DATA18/MTIOC6C/GTIOC4A	Not assigned	None	None	None	None	None	
L3	P0_0/D0/DRP24/DV0_DATA17/MTIOC6B/GTIOC3B	Not assigned	None	None	None	None	None	
L4	PJ_7/GTETRGB/NFDATA0/LCD0_EXTCLK/MTCLKB	Not assigned	None	None	None	None	None	
L9	Vcc	Vcc	-	-	-	-	-	Read of
L10	Vss	Vss	-	-	-	-	-	Read of
L11	Vss	Vss	-	-	-	-	-	Read of
L12	Vss	Vss	-	-	-	-	-	Read of
L13	Vss	Vss	-	-	-	-	-	Read of
L14	Vcc	Vcc	-	-	-	-	-	Read of
L19	P7_1/RD/WR#/DRP05/DV0_VSYNC/RxD1/CC1_Ra1	/ RxD1	1	None	Disabled	None	By GPIO Init	
L20	P7_4/CAS#/DRP07/DV0_DATA0/RTS1#/CC2_Ra1	Not assigned	None	None	None	None	None	
L21	P7_3/RAS#/DRP06/DV0_HSYNC/TxD1/CC2_Rd1	/ TxD1	0	None	None	4mA	By GPIO Init	
L22	P7_2/CS4#/DV0_CLK/LCD0_TCON2/TEND0/CC2_Ra0	Not assigned	None	None	None	None	None	
M1	P0_2/D2/DRP26/DV0_DATA19/MTIOC6D/GTIOC4B	Not assigned	None	None	None	None	None	
M2	P0_5/D5/DRP29/DV0_DATA22/MTIOC7C/GTIOC7A	Not assigned	None	None	None	None	None	
M3	P0_4/D4/DRP28/DV0_DATA21/MTIOC7B/GTIOC6B	Not assigned	None	None	None	None	None	
M4	P0_3/D3/DRP27/DV0_DATA20/MTIOC7A/GTIOC6A	Not assigned	None	None	None	None	None	
M9	Vcc	Vcc	÷	-	-	-	-	Read of
M10	Vss	Vss	-	-	-	-	-	Read of
M11	Vss	Vss	-	-	-	-	-	Read (
M12	Vss	Vss	-	-	-	-	-	Read of
c								>

Figure 4-21 [Pins] Page ([Pin Number])



4.3.1 Changing the pin assignment of a software component

The Smart Configurator assigns pins to the software components added to the project. Assignment of the pins can be changed on the [Pins] page.

This page provides two lists: Pin Function and Pin Number.

Follow the procedure below to change the assignment of pins to a software component in the Pin Function list.

- (1) Click on [🚠 (Show by Hardware Resource or Software Components)] to switch to the component view.
- (2) Select the target software component (e.g. scifa1).
- (3) Click the [Enabled] header to sort by pins used.
- (4) In the [Assignment] column on the [Pin Function] list, change the pin assignment (e.g. change from P7_5 to PJ_4).
- (5) Assignment of a single pin or multiple pins that belong to the same peripheral channel can be changed by clicking on the [(Next group of pins for the selected resource)] button.

Software Components	€	Pin Function						-2 II II	è e
Type filter text		type filter t	ext					All	~
∽ 💑 r_ostm	(3)	Enabled	Function		Assignment	Pin Number	Direction	Remarks	
ostm_reserved			CTS0#	(4)	Not assigned	Not assigned	None		
✓ ▲ r_cbuffer i cbuffer0			CTS1#	()	P7_5/CKE/DRP08/DV0_DATA1/C	/ K21	Ю		
 couffer0 ✓ [™]/_∞ r_scifa 			CTS2#		Not assigned	Not assigned	None		
2 scifa1			RTSO#		Not assigned	Not assigned	None		
			RTS1#		Not assigned	Not assigned	None		
			RTS2#		Not assigned	Not assigned	None		
			RxD0		Not assigned	Not assigned	None		
			RxD1		P7_1/RD/WR#/DRP05/DV0_VSY	/ L19	1		
			RxD2		Not assigned	Not assigned	None		

Figure 4-22 Pin Settings – Assigning Pins on the [Pin Function] List

The [Pins] page can assign to pin not add a software component.



4.3.2 Resolving pin conflicts

If there is a pin conflict, an error mark \bigotimes will appear on the tree and [Pin Function] list.

rdware Resource 🕀 🖃 🖓 😹	Pin Functio	on				🤣 💷 🔚 🔤
ype filter text	type filter	r text				All
GPT5	Enabled	Function	Assignment	Pin Number	Direction	Remarks
GPT6		🐼 CTS1#	P7_5/CKE/DRP08/DV0_DATA1/C	/ K21	ю	Multiple pin functions on th
GPT7		KIST#	Not assigned	Not assigned	None	
🤹 Realtime clock		RxD1	P7_1/RD/WR#/DRP05/DV0_VSY		1	
V the serial communication interface with		SCK1	P7_0/WE1#/DQMU/DRP04/DV0		ю	
SCIFA0		TxD1	P7_3/RAS#/DRP06/DV0_HSYNC		0	
SCIFA1					-	
SCIFA2						
SCIFA3						
SCIFA4						
* Serial communication interface (SCI						
📲 I2C bus interface						
🗤 🐗 Serial sound interface						
* 🛱 CAN interface (CANFD)						
🐗 Renesas SPDIF interface						
* Renesas serial peripheral interface						
* SPI multi I/O bus controller						
HyperBusTM controller/Octa memo						
* Ethernet controller						
NAND flash memory interface						
₩ USB 2.0 host/function module						
Video display controller 6						
LVDS output interface						
Capture engine unit						
La MIPI CSI-2 interface						
5D/MMC host interface						
A/D converter						
General I/O ports						
Debugging interface						
5 Dynamic Reconfigurable Processor (
Dynamic Reconfigurable Processor (

Figure 4-23 Pin Conflicts

The detailed information regarding conflicts is displayed in the Configuration Problems view.

💁 Configuration Problems 🛛 🛞 Smart Browser		
error, 0 warnings, 0 others		
Description	Туре	
🗸 🙆 Pin (1 item)		
😣 E05000010: Pin K21 cannot be used multiple	nes. Pin K21 is assigned to P7_5 and (Pin	

Figure 4-24 Pin Conflict Messages



To resolve a conflict, right-click on the node with an error mark on the tree and select [Resolve conflict].

Hardware Resou	rce		↓ <mark>a</mark> 品
Type filter text			
📦 GP 📦 GP			^
€ GP 偽 Realtin	17 ne clock		
111	ommunication	interface	with
🙆 SCI	FA1		
	Assign all		1
	Unassign all		
> ## Sei	Resolve conf	lict	
> ₩ <mark>#</mark> I2C bus	; interface		
> 👘 Serial s	ound interface		

Figure 4-25 Resolving Pin Conflicts

The pins of the selected node will be re-assigned to other pins.



4.3.3 Assigning pins using the MCU Package view

The Smart Configurator visualizes the pin assignment in the MCU Package view. You can save the MCU Package view as an image file, rotate it, and zoom in to and out from it.

Follow the procedure below to assign pins in the MCU Package view.

- (1) Zoom in to the view by clicking the [$\not>$ (Zoom in)] button or scrolling the view with the mouse wheel.
- (2) Right-click on the target pin.
- (3) Select the signal to be assigned to the pin.
- (4) The color of the pins can be customized through [Preference Setting...].





Icon	Description
PK_5	Not assigned
RMI1	Assigned (Input)
ET1_W	Assigned (Output)
ET1_E	Assigned (Input/Output)

Table 4-1Pin icons



4.3.4 Exporting pin settings

The pin settings can be exported for later reference. Follow the procedure below to export the pin settings.

- (1) Save the {ProjName}.scfg file.
- (2) Click on the [12] (Export board setting)] button on the [Pins] page.
- (3) Select the output location and specify a name for the file to be exported.

The exported XML file can be imported to another project having the same device part number.

in configuration							(2) ⁵
lardware Resource $\mathbb{H} = \bigcup_{\mathbf{Z}}^{\mathbf{a}}$	Pin Functio	n					ଏ 🖪 ଧ
Type filter text	Type pin f	unction					
👗 All 🗖	Enabled	Function	Assignment	Pin Number	Direction	Remarks	,
Clock generator		P00	Not assigned	Not assigned	None		
Clock frequency accuracy measureme		P01	Not assigned	Not assigned	None		
* Buses		P02	Not assigned	Not assigned	None		
EXDMA controller		P03	Not assigned	Not assigned	None		
Interrupt controller unit		P05	Not assigned	Not assigned	None		
> Multi-function timer pulse unit 3		P07	Not assigned	Not assigned	None		
Ort output enable 3		P10	Not assigned	Not assigned	None		
> 🙆 General PWM timer		P11	Not assigned	Not assigned	None		
< >		P12	Not assigned	Not assigned	None		

Figure 4-27 Exporting Pin Settings to an XML File

The Smart Configurator can also export the pin settings to a CSV file. Click on the [III] (Save the list to .csv file)] button on the [Pins] page.

4.3.5 Importing pin settings

To import pin settings into the current project, click on the $[\stackrel{\text{less}}{=}$ (Import board setting)] button and select the XML file that contains the desired pin settings. After the settings specified in this file are imported to the project, the settings will be reflected in the [Pin configuration] page.

n configuration							5
ardware Resource 🕀 🕒 🛱	Pin Functio	n					2 🖬 🔛
Type filter text	Type pin	function					
📥 All 🛛 🔺	Enabled	Function	Assignment	Pin Number	Direction	Remarks	
Clock generator		P00	Not assigned	Not assigned	None		
Clock frequency accuracy measureme		P01	Not assigned	Not assigned	None		
* Buses		P02	Not assigned	Not assigned	None		
EXDMA controller		P03	Not assigned	Not assigned	None		
Interrupt controller unit		P05	Not assigned	Not assigned	None		
> 🥨 Multi-function timer pulse unit 3		P07	Not assigned	Not assigned	None		
Port output enable 3		P10	Not assigned	Not assigned	None		
> 🙆 General PWM timer		P11	Not assigned	Not assigned	None		
< >>		P12	Not assigned	Not assigned	None		

Figure 4-28 Importing Pin Settings from an XML File



4.4 MMU Settings

The [MMU] page is used for assigning memory maps. Memory map settings are displayed in the [Page Table] list in virtual address order.

MU configuratio	n							٢
Use MMU Configuratio	n							
age Table								
Name	Virtual Address	Physical Address	Size	Attributes	NS	AP[2:0]	XN	Add
CS0 space	0x00000000	0x0000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Remove
CS1 space	0x04000000	0x04000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Kentove
CS2 space	0x08000000	0x08000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Edit
CS3(SDRAM)	0x0C000000	0x0C000000	0x4000000	Normal (L1/L	Non-secure	Read/Write (Executable (
CS4 space	0x1000000	0x10000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	
CS5 space	0x14000000	0x14000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Import
Reserved	0x18000000	0x18000000	0x7000000	Reserved	Non-secure	Access inhib	Execute nev	Export
Peripheral I/O	0x1F000000	0x1F000000	0x1000000	Strongly-ord	Secure (NS=	Read/Write (Execute nev	
SPI multi I/O bus area	0x20000000	0x20000000	0x10000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Hyper Flash area	0x3000000	0x3000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Hyper RAM area	0x4000000	0x4000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Octa Flash area	0x5000000	0x5000000	0x10000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Octa RAM area	0x6000000	0x6000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
SPI multi I/O bus area	0x7000000	0x20000000	0x10000000	Strongly-ord	Non-secure	Read/Write (Executable (
Internal RAM area	0x8000000	0x8000000	0x400000	Normal (L1-c	Non-secure	Read/Write (Executable (

Figure 4-29 MMU page

4.4.1 Add the page table

To add the page table, click on the [Add] button and set it in the dialog box opened.



Figure 4-30 Add the page table



4.4.2 Remove the page table

To remove the page table, select the remove page line and click on the [Remove] button. Two or more page tables can be selected by clicking with the Ctrl key pressed.

MU configuratio	n							Ć	5
Use MMU Configuratio	'n								
age Table									
Name	Virtual Address	Physical Address	Size	Attributes	NS	AP[2:0]	XN	Add	
CS0 space	0x0000000	0x0000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Remove	ī
CS1 space	0x04000000	0x04000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Kelliove	
CS2 space	0x0800000	0x08000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Edit	
CS3(SDRAM)	0x0C000000	0x0C000000	0x4000000	Normal (L1/L	Non-secure	Read/Write (Executable (
CS4 space	0x1000000	0x10000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev		٦
CS5 space	0x14000000	0x14000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Import	
Reserved	0x18000000	0x18000000	0x7000000	Reserved	Non-secure	Access inhib	Execute nev	Export	
Peripheral I/O	0x1F000000	0x1F000000	0x1000000	Strongly-ord	Secure (NS=	Read/Write (Execute nev		_
SPI multi I/O bus area	0x20000000	0x20000000	0x10000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Hyper Flash area	0x3000000	0x3000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Hyper RAM area	0x4000000	0x40000000	0x10000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Octa Flash area	0x5000000	0x5000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Octa RAM area	0x6000000	0x6000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
SPI multi I/O bus area	0x7000000	0x20000000	0x10000000	Strongly-ord	Non-secure	Read/Write (Executable (
Internal RAM area	0x8000000	0x80000000	0x400000	Normal (L1-c	Non-secure	Read/Write (Executable (
Reserved	0x80400000	0x80400000	0x1C00000	Reserved	Non-secure	Access inhib	Execute nev		

Figure 4-31 Remove the page table

4.4.3 Edit the page table

To edit the page table, select the edit page line and click on the [Edit] button. Edit the memory map in the dialog box opened and click on the [OK] button. Setting is reflecting to the page tables.

MU configuratio	n							6	3
								-	
Use MMU Configuratio	n								
age Table									
Name	Virtual Address	Physical Address	Size	Attributes	NS	AP[2:0]	XN	Add]
CS0 space	0x0000000	0x0000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Remove	ī
CS1 space	0x04000000	0x04000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Remove	
CS2 space	0x08000000	0x08000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Edit	
CS3(SDRAM)	0x0C000000	0x0C000000	0x4000000	Normal (L1/L	Non-secure	Read/Write (Executable (
CS4 space	0x1000000	0x10000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev		٦
CS5 space	0x14000000	0x14000000	0x4000000	Strongly-ord	Non-secure	Read/Write (Execute nev	Import	
Reserved	0x18000000	0x18000000	0x7000000	Reserved	Non-secure	Access inhib	Execute nev	Export	1
Peripheral I/O	0x1F000000	0x1F000000	0x1000000	Strongly-ord	Secure (NS=	Read/Write (Execute nev		1
SPI multi I/O bus area	0x20000000	0x20000000	0x10000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Hyper Flash area	0x3000000	0x3000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Hyper RAM area	0x4000000	0x40000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Octa Flash area	0x5000000	0x5000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
Octa RAM area	0x6000000	0x6000000	0x1000000	Normal (L1/L	Non-secure	Read/Write (Executable (
SPI multi I/O bus area	0x7000000	0x20000000	0x1000000	Strongly-ord	Non-secure	Read/Write (Executable (
Internal RAM area	0x80000000	0x80000000	0x400000	Normal (L1-c	Non-secure	Read/Write (Executable (
Reserved	0x80400000	0x80400000	0x1C00000	Reserved	Non-secure	Access inhib	Execute nev		

Figure 4-32 Edit the page table



4.4.4 Import the memory maps

To import the memory map to current project, click on the [Import] button.

Select the memory map file in the dialog box opened.

You will be using default setting, check the [Use default template] and select a template.

You will be using custom memory map, check the [Use custom template] and select a template.

Click on the [OK] button, setting is reflecting to the page tables.

		e ² MMU		×
		Import Memory Map		
Add	Ν	O Use default template		
Remove	\square	Select template: Boot mode 3/4/5		~
Edit		O Use custom template Specify location:	Bro	wse
Import				
Export		OK	Cance	I

Figure 4-33 Import the memory maps

4.4.5 Export the memory maps

he memory maps can be exported for later reference. Follow the procedure below to export the memory mapss.

- (1) Save the {ProjName}.scfg file.
- (2) Click on the [Export] button on the [MMU] page.
- (3) Select the output location and specify a name for the file to be exported.

The exported XML file can be imported to another project having the same device part number.



Figure 4-34 Export the memory maps



5. Generating Source Code

5.1 Outputting Generated Source Code

Output a source file for the configured details by clicking on the [10 (Generate Code)] button in the Smart Configurator view.

🎄 *Smart_Configurator_Example.scfg 🛛 🗖 🗖								
Pin configuration								
Hardware Resou 庄 🕒 🖡	Pin Functio	on		2 📓 🖬 🕹				
Type filter text	Type pin	function						
🚣 All	^ Enabled	Function	Assignment	^				

Figure 5-1 Generating a Source File

The Smart Configurator generates a source file in <ProjectDir>¥generate¥drivers and <ProjectDir>¥generate¥sc_drivers folders and updates the source file list in the Project Explorer.



Figure 5-2 Source Files in the Project Explorer


5.2 Configuration of Generated Files and File Names

Figure 5-3, Configuration of Generated Files and File Names, shows the folders and files output by the Smart Configurator.



Figure 5-3 Configuration of Generated Files and File Names

Folder	File	Description
r_cpg		This folder is always generated.
		It contains header files and source files commonly used by clock pulse
		generator.
	r_cpg_drvs_sc_cfg.h	These files are always generated. It contains macro definitions for setting
		clock pulse generator.
		[Clock] page setting is reflecting to this file.
r_gpio		This folder is always generated.
		It contains header files and source files commonly set by pin assignment.
	r_gpio_drvs_sc_cfg.h	This file is always generated. It contains macro definitions for setting pin
		assignment.
		[Pins] page setting is reflecting to this file.
r_mmu		This folder is always generated.
		It contains header files and source files commonly used by memory
		management unit.
	r_mmu_drvs_sc_cfg.h	This file is always generated. It contains macro definitions for memory
		management unit.
		[MMU] page setting is reflecting to this file.
sc_drivers		This folder is always generated.
		It contains header files and source files commonly used by software
		components.
r_ostm		This folder is always generated.
		It contains header files and source files commonly used by OS timer.
	r_ostm_drvs_sc_cfg.h	This file is always generated. It contains macro definitions for OS timer.
		ostm_reserved setting in [Components] page is reflecting to this file.
r_xxx		This folder is always generated.
		It contains header files and source files commonly used by added
		software components.
	r_xxx_drvs_sc_cfg.h	This file is always generated. It contains macro definitions for added
		software components.
		software component setting in [Components] page is reflecting to this
		file.



6. Managing Conflicts

6.1 Resolving pin conflicts

If there is a pin conflict, an error mark 🔕 will appear on the tree and [Pin Function] list.

ardware Resource 🕀 🕒 🛱 🖧	Pin Functio	n				🤣 🔛 📑 🔛
Type filter text	type filter	text				All
GPT5	Enabled	Function	Assignment	Pin Number	Direction	Remarks
GPT6		🔇 CTS1#	P7_5/CKE/DRP08/DV0_DATA1/C	/ K21	10	Multiple pin functions on th
GPT7		RT31#	Not assigned	Not assigned		
🤹 Realtime clock		RxD1	<pre>/ P7_1/RD/WR#/DRP05/DV0_VSY</pre>		I	
 Serial communication interface with 		SCK1	P7_0/WE1#/DQMU/DRP04/DV0		10	
SCIEA0		TxD1	P7_3/RAS#/DRP06/DV0_HSYNC		0	
SCIFA1	\sim	IXD1	P7_3/RA3#/DRP06/DV0_H3TNC	# L21	0	
SCIFA2						
SCIFA3						
SCIFA4						
> 📲 Serial communication interface (SCk						
> ## I2C bus interface						
Serial sound interface						
*# CAN interface (CANFD)						
Renesas SPDIF interface						
> *# Renesas serial peripheral interface						
> * SPI multi I/O bus controller						
HyperBusTM controller/Octa memo						
* # Ethernet controller						
NAND flash memory interface						
> * USB 2.0 host/function module						
Video display controller 6						
🗱 LVDS output interface						
📭 Capture engine unit						
📥 MIPI CSI-2 interface						
> 🚣 SD/MMC host interface						
🖳 A/D converter						
> 🐲 General I/O ports						
Debugging interface						
👼 Dynamic Reconfigurable Processor (🗸						
	<					

Figure 6-1 Pin Conflicts

The detailed information regarding conflicts is displayed in the Configuration Problems view.

	⊉ ▽ - □
Туре	
I C Pin	
	Type

Figure 6-2 Pin Conflict Messages



To resolve a conflict, right-click on the node with an error mark on the tree and select [Resolve conflict].



Figure 6-3 Resolving Pin Conflicts

The pins of the selected node will be re-assigned to other pins.



6.2 Missing Dependencies

When user adds a component which is dependent on other components, the dependencies should also be added. For example, when a user adds the component r_scifa , an error message with the \bowtie mark will be displayed in the Configuration Problems view to inform the user that the dependent component $r_cbuffer$ is needed.

🏟 *Smart_Configurator_Example.scfg 🙁	h r_startup_config.h ြင်္လ Smart_Configurator_Examp	ole_main.c	
Software component configur	ation		🐻 🖨
Components $ _{Z}^{a} \boxdot \Rightarrow \checkmark$	Configure		
type filter text	Property	Value	^
	# SCIFA communication modes	Asynchronous mode	
🗸 🔂 Drivers	# SCIFA Bit Rate (bps)	115200	
Communications	# Clock select	Internal clock input	
scifa0	# Asynchronous Base Clock Select	Use clock as 16x mode	
V 🗁 Timers	# Data Bit Length	8 Bits	
💣 ostm_reserved	# Parity Enable	Unused	
	# Parity Mode	Even Parity	
	# Stop Bit Lenght(s)	1 bit	
	# Noise Cancellation	Unused	¥
			Ŷ
Oveniew Clocks Components Pins MMI			·

Figure 6-4 Error of Missing Dependency

🔝 Configuration Problems 🐹 🦇 Smart Browser	\$ ~ □ □
1 error, 0 warnings, 0 others	
Description	Туре
✓ Ø Dependency (1 item)	
8 E04020010: scifa0 module needs following module but not added: r_cbuffer[1.00]	Dependency
l.	

Figure 6-5 Missing Dependency Messages

To fix this error, add the dependent component into the project.



7. Generating Reports

The Smart Configurator generates a report on the configurations that the user works on. Follow the procedure below to generate a report.

7.1 Report on All Configurations

A report is output in response to clicking on the [👜 (Generate Report)] button in the Smart Configurator view.

Smart_Configurator_Example.scf	fg 🖾 🖪 r_startup_conf	fig.h 💽 Smart_Configu	urator_Example_main.c	- 8
Overview information				1
➡ General Information				?
This editor allows you to modify	the settings stored in con	figuration file (.scfg)		
Clocks				
Allow clock configuration			Application under development	
Components				- Compone
Allow software component select	tion and configuration		Device driver RTOS	
Pins				- Pins
Allow general pin configuration a	and pin configuration for	selected software compone		
MMU				
Allow MMU configuration				
 Current Configuration 				
Selected board/device: R7S92105	58 (RAM size: 4MB. Pin co	unt: 324. CPU: Cortex-A9. M	lax, Freq: 528MHz)	
Selected components:				
Component	Version	Configuration		
📀 r_ostm	1.01	ostm_reserved(OSTM2	2: used)	

Figure 7-1 Output of a Report on the Configuration

e ² Smart Report		×
Generate report of configurations		
Options		
Print all sections		
O Print specific sections		
Clocks		
Components		
> 🔳 Pins		
MMU		
Output as PDF	Select	Font
Output as text		
C:¥Workspace¥Smart_Configurator_Example¥output	Bro	wse
? ОК	Canc	el

Figure 7-2 Dialog Box for Output of a Report



7.2 Configuration of Pin Function List and Pin Number List (in csv Format)

A list of the configuration of pin functions and pin numbers (whichever is selected at the time) is output in response to clicking on the [🔛 (Save the list to .csv file)] button on the [Pins] page of the Smart Configurator view.

ardware Resource $$ \boxdot \downarrow^{a}_{z} $\overset{a}{\Longrightarrow}$	Pin Function	ı				ି 🕹 🖬 🖬 🖕
ype filter text	type filter	text				All
Image: Weak of the clock ▲ Image: Weak of the clock ▲ <	Enabled	Function CTS1# RTS1#	Assignment / P7_5/CKE/DRP08/DV0_DATA1/C / Not assigned	Not assigned	Direction IO None	Remarks
SCIFA1		RxD1	P7_1/RD/WR#/DRP05/DV0_VSY		1	
SCIFA2		SCK1	PJ_0/TRACECLK/SPDIF_OUT/SC		IO	
SCIFA4		TxD1	P7_3/RAS#/DRP06/DV0_HSYNC	/ L21	0	
♥ ♥						

Figure 7-3 Output of a List of Pin Functions or Numbers (in csv Format)

7.3 Image of MCU Package

An image of the MCU package is output in response to clicking on the [III] (Save Package View to external image file)] button of the [MCU Package] view.

MCU Package 없 볼 MMU Layout 드	
Type pin function 💿 Assigned 🔾 Default Boa	rd
4	
· · · · · · · · · · · · · · · · · · ·	
RENESAS BOTO	
e 443-446 448 4484 (Ra Ra Ra Ra Ra Ra Ra	
- 4/43-4/43-4/43-4/43-4/43-	
2 4000-4023-4023-4023-4023	
x (uu (gal (Hai (gal (ma (uu (uu (uu (uu (uu (uu (uu (uu (uu (u	
* R3 R3 R3 R3 · · · · · · · · · · · · · ·	
r find find find find and an	
· · · · · · · · · · · · · · · · · · ·	
* 51.5 51.5 W. FLE FLE FLE FLE FLE FLE FLE WELL W. 2017. 2017. 2017. W. FLE FLE FLE FLE W. *	
V BLE. BLE. V. R.C. R.S. R.S. R.S. R.S. R.S. M. V. DEV. DEV. DEV. DEV. DEV. DEV. DEV.	
1 1 4 4 4 7 8 8 11 11 11 11 11 11 11 11 11 11 11 11	
V Legend	
Highlighted pin In-used pin Warning pin Conflict pin	
System Timer Connectivity Analog Port	
Graphics Audio Others Preferences Setting	

Figure 7-4 Outputting a Figure of MCU Package



8. Help

8.1 Help

Refer to the help system from the e^2 studio menu for detailed information on the Smart Configurator.

e ² workspace - Smart_Configurator_Example/Smart_Configurator_Example.scfg - e ² studio				
File Edit Navigate Search Project Renesas Views Run Window	Help			
🐔 🐞 🔳 🔅 Debug 🗸 💽 Smart_Configurator	🚳 Welcome			
	Help Contents			
	💯 Search			
Project Explorer ⊠ 📄 🕏 ▽ 🗖 🗍 👹 Smart_	Show Contextual Help			

Figure 8-1 Help Menu

The help system can also be activated from the [Overview information] page.

🌼 Smart_Configurator_Example.scfg 🔀	h r_startup_cor	nfig.h 🛛 🔂 Smart_Configura	tor_Example_main.c	- 8
Overview information				🐻 🖨
➡ General Information				?
This editor allows you to modify the set	ings stored in co	nfiguration file (.scfg)		
Clocks				
Allow clock configuration			Application under development	
Components			Middleware	 Compone
Allow software component selection an	d configuration		Device driver RTOS	
Pins				- Pins
Allow general pin configuration and pin	configuration fo	r selected software component		
MMU				
Allow MMU configuration				
✓ Current Configuration				
-	A since 4MAR, Disc as	web 224 CBUb Center Ao Mar	From FOOL(11-)	
Selected board/device: R7S921058 (RAN Selected components:	i size: 4ivib, Pin co	ount: 324, CPU: Cortex-A9, Max.	. Freq: 528MHZ)	
Component	Version	Configuration		
🗢 r_ostm	1.01	ostm_reserved(OSTM2: us	sed)	
				×
Overview Clocks Components Pins MM	10			





9. Documents for Reference

User's Manual: Hardware

Obtain the latest version of the manual from the Renesas Electronics website.

Technical Update/Technical News

Obtain the latest information from the Renesas Electronics website.

User's Manual: Development Environment

e2 studio v7.0 Integrated Development Environment User's Manual: Getting Started Guide (R20UT4374)

RZ/A2M Group Software Core Package (R01AN4583)

(Obtain the latest version from the Renesas Electronics website.)



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Revision History

ILE VISIC	Jin mistory	Description		
Rev.	Date	Page	Summary	
1.00	Feb 1, 2019	-	First edition issued	
1.01	Sep 13, 2019	-	Modify the missing chapter number	
		4	Adjust the position of red box in Figure 2-1	
		8	Adjust the position of red box in Figure 3-2	
		21	Adjust the position of red box in Figure 4-10	

- 1. Handling of Unused Pins
 - Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
 - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

 The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
- The reserved addresses are provided for the possible future expansion of functions. Do not
 access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

 The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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