

RZ/A2M CPU Board

RTK7921053C00000BE

User's Manual

Renesas Microprocessor
RZ Family / RZ/A Series

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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Contact information

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1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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How to use this manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the functions and operating specifications of this CPU board. This manual is intended for all users of this CPU board. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product, functional specifications, and operating specifications.

Before using this CPU board, thoroughly understand the notes provided in the text of each section in this manual.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following document applies to the RZ/A2M CPU Board RTK7921053C00000BE.

Document Type	Description	Document Title	Document No.
User's manual	Description of functional specifications (mounted devices, memory map, electrical characteristics, etc.) and operating specifications (connectors, switches, etc.)	RZ/A2M CPU Board RTK7921053C00000BE User's Manual	This user's manual

The following documents apply to the RZ/A2M group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

document Type	Description	Document Title	Document No.
Application note	Application examples, reference programs, etc.	Available from Renesas Electronics Web site.	
RENESAS TECHNICAL UPDATE	Prompt reports on product specifications, documents, etc.		

2. Abbreviations

Abbreviation	Full Form
ACIA	Asynchronous Communications Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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1. Overview

1.1 Overview

RTK7921053C00000BE is a CPU board to evaluate the functions and performance of the Renesas Electronics microprocessor RZ/A2M “R7S921053VCBG” and to develop and evaluate application software programs

The RTK7921053C00000BE CPU board has the following features.

- This CPU board contains the following external memory.
 - Serial flash memory: 64 Mbytes x 1
 - HyperMCP (HyperFlash: 64 Mbytes and HyperRAM: 8 Mbytes) x 1
- One of serial flash memory, HyperMCP, and NAND flash memory with built-in SD controller is selectable as boot memory.
- A USB Type-C connector and a microSD card slot are mounted as standard as an RZ/A2M peripheral function interface.
- A Type-C receptacle is mounted as standard as a USB connector.
- A 15-pin FPC MIPI CSI-2 connector is mounted as a high-speed serial interface for camera devices.
- Pins that are not used in this board are connected to the SODIMM connector (J2) that can be used in connection with the RZ/A2M SUB board (model: RTK79210XXB00000BE). Furthermore, an expansion board can be developed in accordance with the development applications.
- This CPU board contains a CoreSight 20 connector for connection to the RZ/A2M user debug interface.

1.2 Configuration

Figure 1.1 shows an example of system configuration using RTK7921053C00000BE.

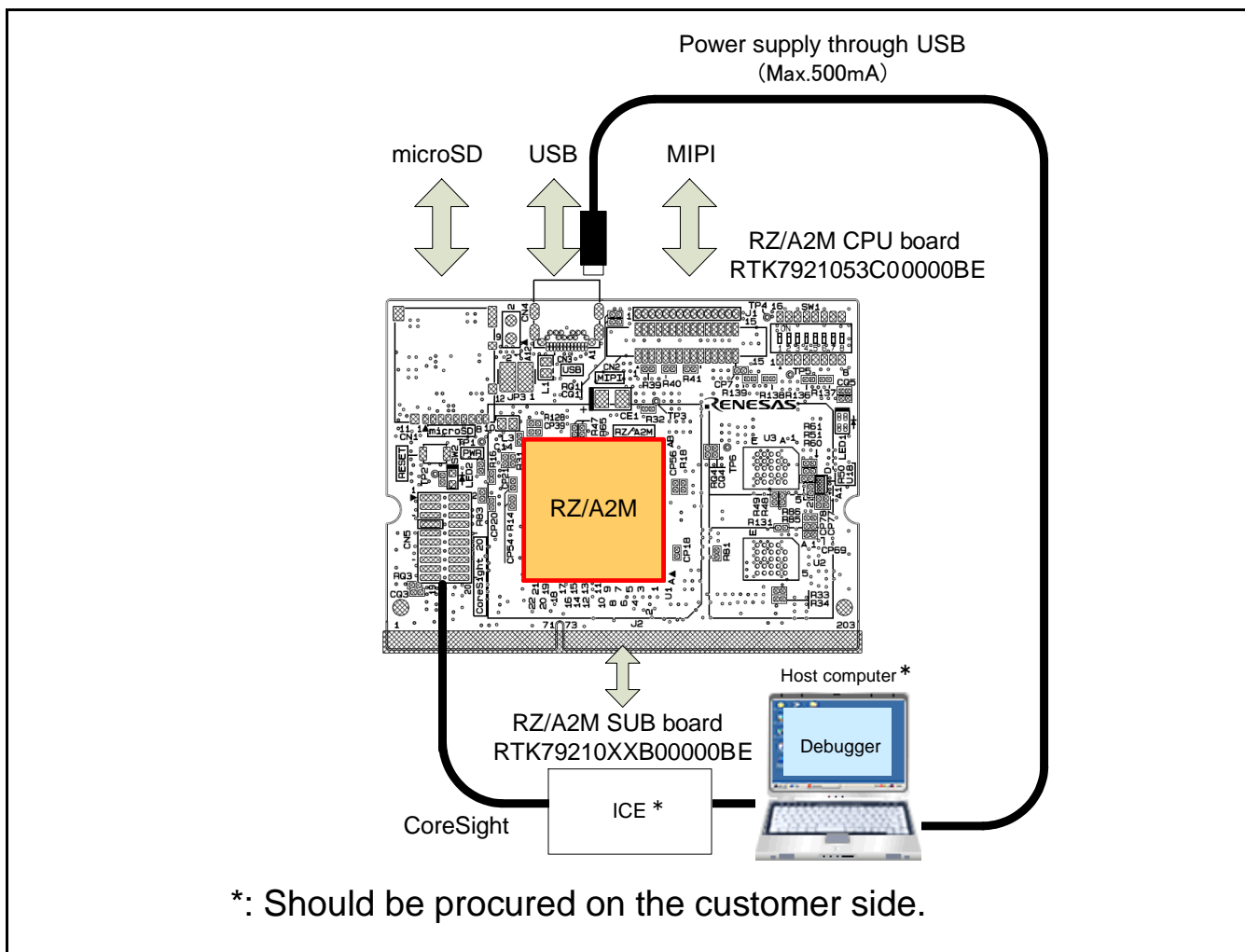


Figure 1.1 Example of System Configuration Using RTK7921053C00000BE

1.3 Features

Table 1.1 shows the features of RTK7921053C00000BE.

Table 1.1 Features of RTK7921053C00000BE

item	details
CPU	RZ/A2M <ul style="list-style-type: none"> • Input (XIN) clock: 24 MHz • CPU clock (Iϕ): max. 528 MHz • Image clock (Gϕ): max. 264 MHz • Internal bus clock (Bϕ): max. 132 MHz • External bus clock (CKIO): max. 132 MHz • Peripheral clock 1 (P1ϕ): max. 66 MHz • Peripheral clock 0 (P0ϕ): max. 33MHz • Internal memory <ul style="list-style-type: none"> large capacity internal RAM: 4 Mbytes Cache memory: 32 Kbytes Data cache: 32 Kbytes (write-back type) • Power voltage: internal: 1.2 V, I/O: 3.3 V, 1.8 V • 324-Pin BGA 0.8 mm pitch (package code: PRBG0324GA-A)
Memory	<ul style="list-style-type: none"> • Serial flash memory: 64 Mbytes x 1 <ul style="list-style-type: none"> - Macronix MX25L51245GXDI-08G • HyperMCP (HyperFlash: 64 Mbytes and HyperRAM: 8 Mbytes) x 1 <ul style="list-style-type: none"> - Cypress S71KS512SC0BHV000
Connector	<ul style="list-style-type: none"> • USB Type-C receptacle: 1 • microSD card slot (4 bits): 1 • MIPI CSI-2 connector (15 pins): 1 • User debug interface connector (CoreSight 20): 1 • SUB board connector (204 pins): 1
LED	<ul style="list-style-type: none"> • Power source LED: 1 • User LED: 1 (Dual)
Switch	<ul style="list-style-type: none"> • Reset switch: 1 • System setting DIP switch: 8 bits
Circuit board specifications	<ul style="list-style-type: none"> • Dimensions: 67.6 mm x 50 mm • Mount: Double-sided mounting (8 layers) • Configuration: Single board

1.4 Outside View

Figure 1.2 shows the outside view of RTK7921053C00000BE.

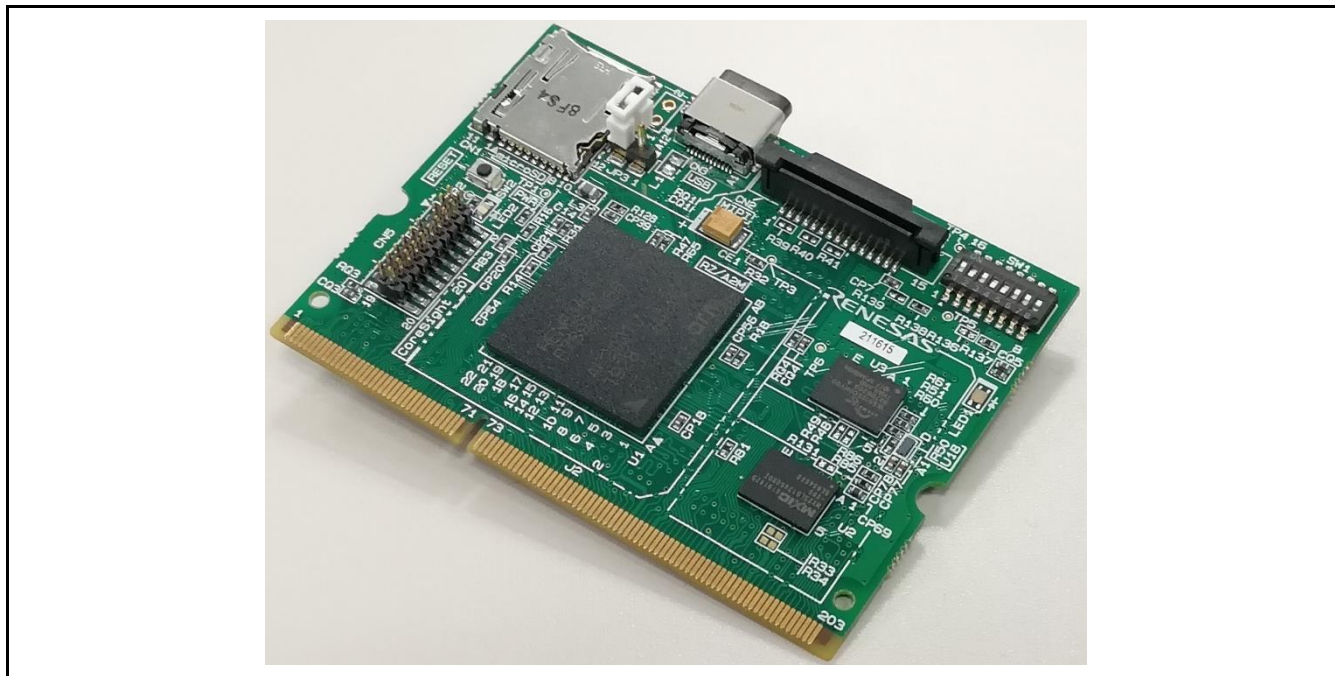


Figure 1.2 Outside View of RTK7921053C00000BE

1.5 Block Diagram

Figure 1.3 shows the block diagram of RTK7921053C00000BE.

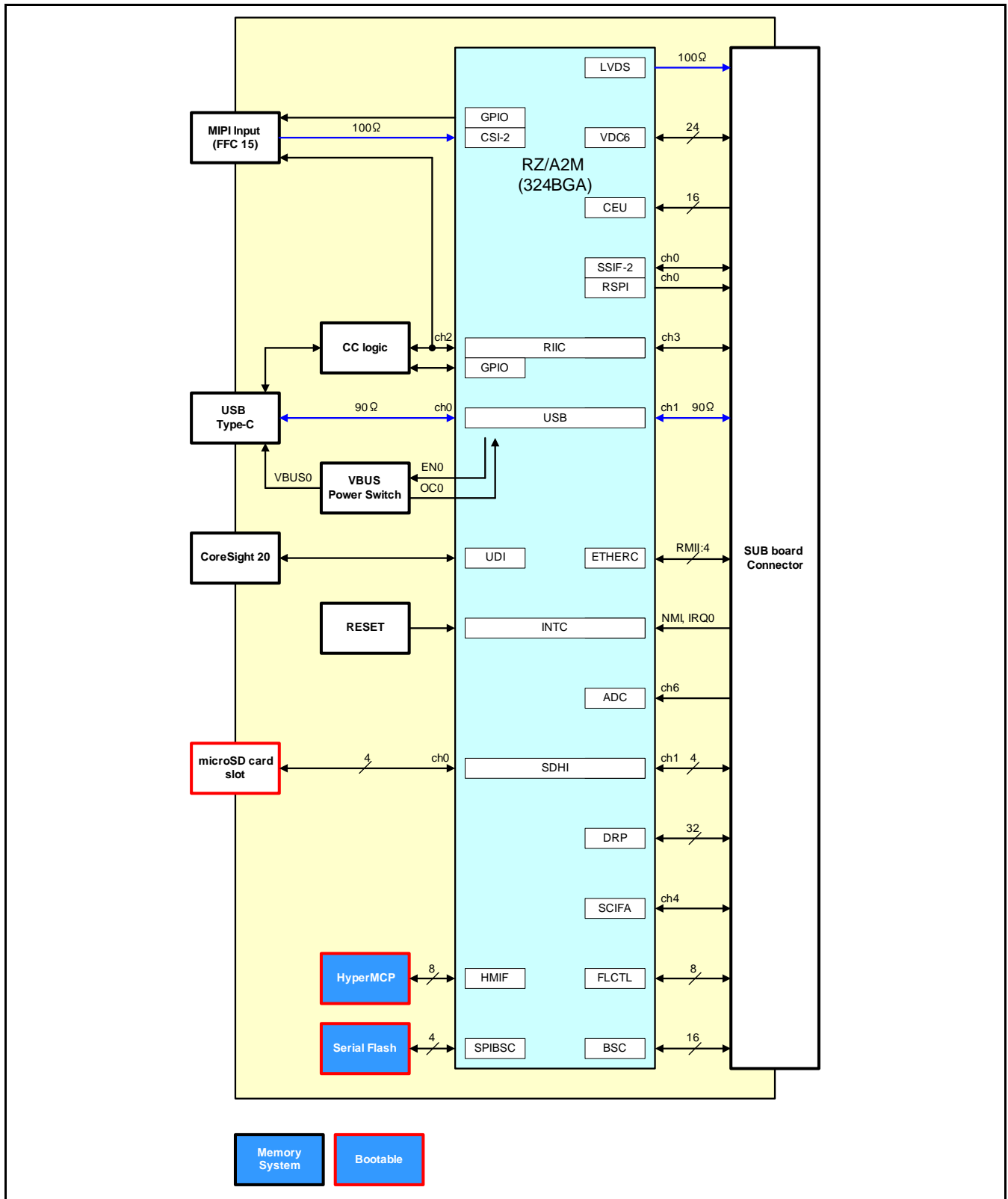


Figure 1.3 Block Diagram of RTK7921053C00000BE

1.6 Layout of Components

Figure 1.4 and Figure 1.5 show the layout of main components of RTK7921053C00000BE.

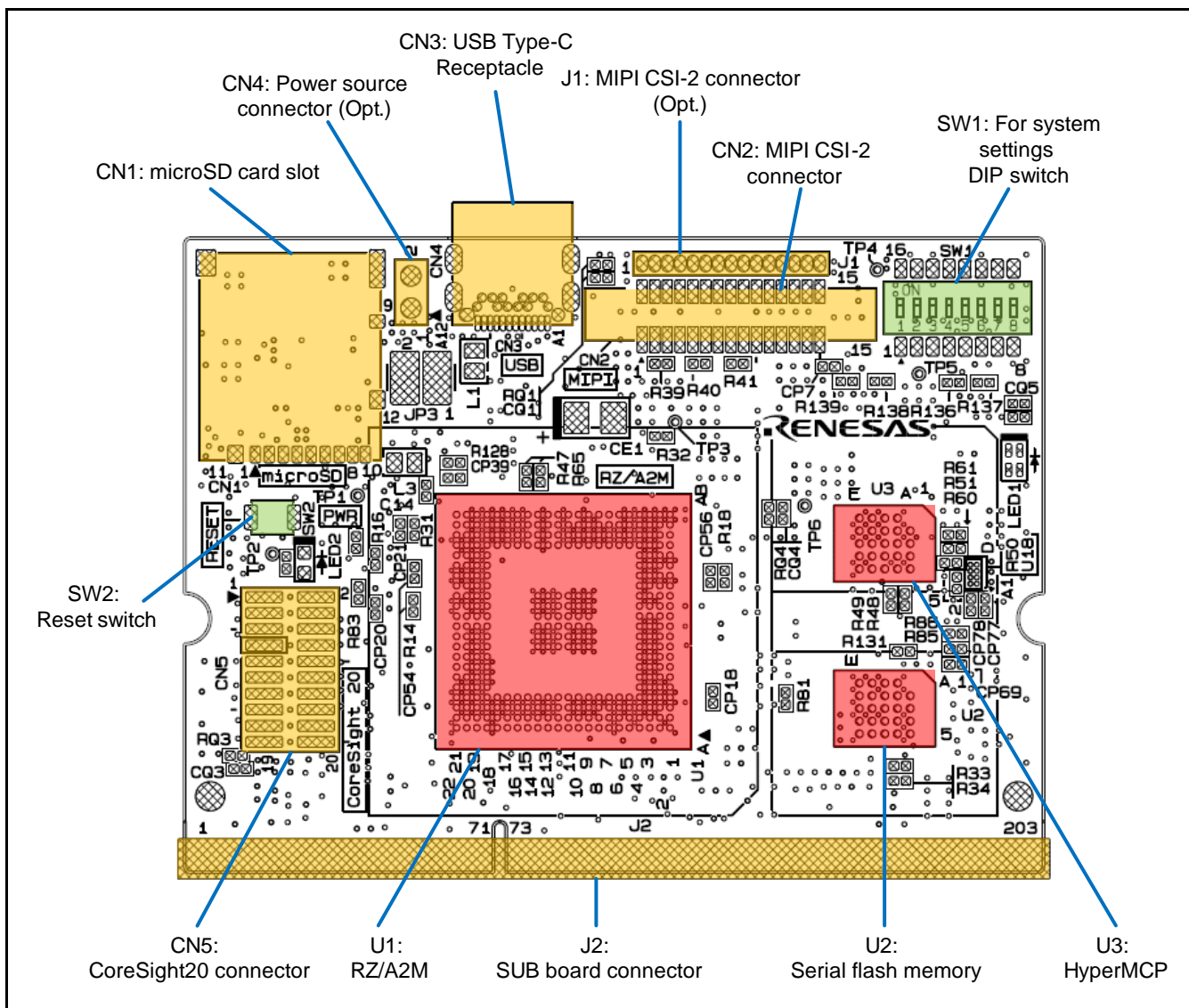


Figure 1.4 Layout of Components of RTK7921053C00000BE (C Side Top View)

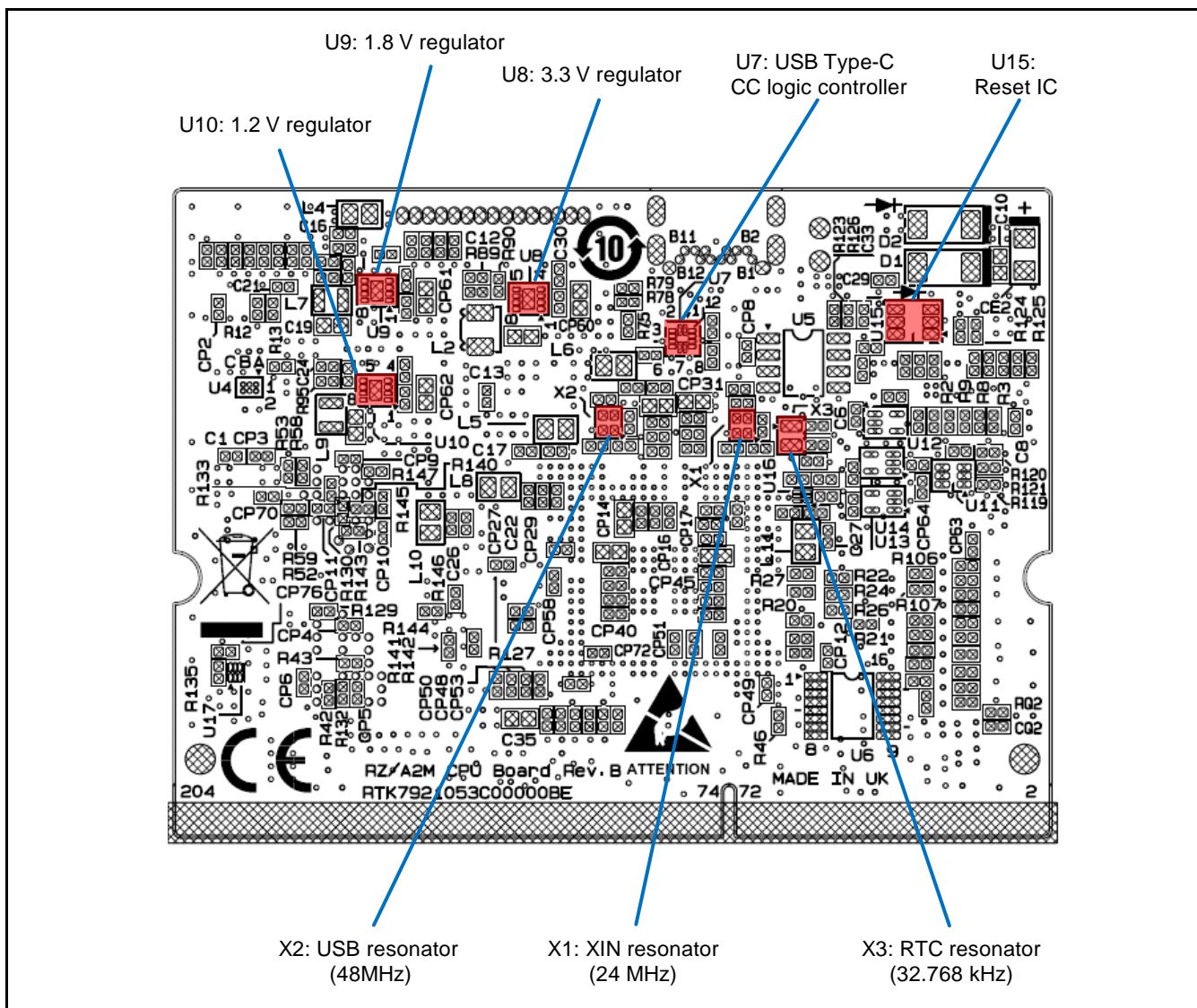


Figure 1.5 Layout of Components of RTK7921053C00000BE (S Side Top View)

Table 1.2 and Table 1.3 list main components mounted on RTK7921053C00000BE.

Table 1.2 Main Components on RTK7921053C00000BE (1) IC

Component Number	Component Name	Type (Manufacturer)	Recommended Optional Components
U1	CPU	R7S921053VCBG (Renesas)	
U2	Serial flash memory	MX25L51245GXDI-08G (Macronix)	
U3	HyperMCP	S71KS512SC0BHV000 (Cypress)	
U7	USB Type-C CC logic controller	TUSB320LIRWBR (TI)	
U8	3.3 V regulator	ISL80030AFRZ-T7A (Intersil)	5 V→3.3 V
U9	1.8 V regulator	ISL80020AIRZ-T7A (Intersil)	5 V→1.8 V
U10	1.2 V regulator	ISL80020AIRZ-T7A (Intersil)	5 V→1.2 V
U15	Reset IC	TPS3808G01DBV (TI)	
X1	Crystal resonator for XIN	CX1612DB24000D0PPSCC (Kyocera)	24 MHz
X2	Crystal resonator for USB	CX1612DB48000D0PPSC1 (Kyocera)	48 MHz
X3	Crystal resonator for RTC	ST2012SB32768H5HPWAA (Kyocera)	32.768 kHz

Table 1.3 Main Components on RTK7921053C00000BE (2) Connector

Component Number	Component Name	Type (Manufacturer)	Recommended Optional Parts
J1	MIPI CSI-2 connector (Optional) (15pins)	Not used	LL1013-04A-15 (LANL)
J2	SUB board connector (SODIMM 204 pins)		
CN1	microSD card slot	DM3AT-SF-PEJM5 (HRS)	
CN2	MIPI CSI-2 connector (15 pins)	1-1734248-5 (TE)	
CN3	USB Type-C receptacle	DX07S024XJ1 (JAE)	
CN4	Power source connector (Optional)	Not used	A2-2PA-2.54DSA(71) (HSR)
CN5	CoreSight20 connector (20 pins)	FTSH-110-01-L-DV (Samtec)	

1.7 Memory Mapping

Figure 1.6 shows the RZ/A2M memory mapping of RTK7921053C00000BE.

Logical address	RZ/A2M Logical space	RTK7921053C00000BE Memory mapping
H'0000 0000	CS0 space: 64 MB	-
H'0400 0000	CS1 space: 64 MB	-
H'0800 0000	CS2 space: 64 MB	-
H'0C00 0000	CS3 space: 64 MB	-
H'1000 0000	CS4 space: 64 MB	-
H'1400 0000	CS5 space: 64 MB	-
H'1800 0000	Others: 128 MB	Others: 128 MB
H'2000 0000	SPI multi I/O bus space: 256 MB	Serial flash memory (64 MB)
H'2400 0000		-
H'3000 0000	HyperFlash space: 256 MB	HyperFlash (64MB)
H'3400 0000		-
H'4000 0000	HyperRAM space: 256 MB	HyperRAM (8MB)
H'4080 0000		-
H'5000 0000	OctaFlash space: 256 MB	-
H'6000 0000	OctaRAM space: 256 MB	-
H'7000 0000	Reserved (cannot be used)	Reserved (cannot be used)
H'8000 0000	Large capacity internal RAM: 4 MB	Large capacity internal RAM: 4 MB
H'8040 0000	Others: 2044MB	Others: 2044MB
H'FFFF FFFF		

Figure 1.6 RZ/A2M Memory Mapping

1.8 Absolute Maximum Ratings

Table 1.4 lists absolute maximum ratings of RTK7921053C00000BE.

Table 1.4 Absolute Maximum Ratings of RTK7921053C00000BE

Symbol	Item	Rated Value	Note
D5V	5 V power voltage	-0.3 V to 6.25 V	Reference: Vss
T _{opr}	Operating ambient temperature *	0 °C to 50 °C	Do not expose to condensation or corrosive gases
T _{stg}	Storage temperature *	-10 °C to 60 °C	Do not expose to condensation or corrosive gases

[Note] * Ambient temperature is the air temperature at a position as close to the board as possible.

1.9 Operating Conditions

Table 1.5 lists operating conditions of RTK7921053C00000BE.

Table 1.5 Operating Conditions of RTK7921053C00000BE

Symbol	Item	Rated Value	Note
D5V	5 V power voltage	4.75 V to 5.25 V	Reference: Vss
—	Maximum power consumption	1 A	5 V, 3.3 V, 1.8 V, 1.2 V power source overall values
T _{opr}	Operating ambient temperature *	0 °C to 40 °C	Do not expose to condensation or corrosive gases

[Note] * Ambient temperature is the air temperature at a position as close to the board as possible.

2. Functional Specifications

2.1 Overview of Functions

Table 2.1.1 lists function modules of RTK7921053C00000BE.

Table 2.1.1 Function Modules of RTK7921053C00000BE

Section	Function	Description
2.2	CPU	<ul style="list-style-type: none"> ● RZ/A2M <ul style="list-style-type: none"> - Input (XIN) clock: 24 MHz - CPU clock: max. 528 MHz - Bus clock: max. 132 MHz
2.3	Memory	<ul style="list-style-type: none"> ● On-chip memory <ul style="list-style-type: none"> - Large capacity on-chip RAM: 4 Mbytes ● Serial flash memory: 64 Mbytes x 1 <ul style="list-style-type: none"> - Macronix MX25L51245GXDI-08G ● HyperMCP (HyperFlash: 64 Mbytes, HyperRAM: 8 Mbytes) x 1 <ul style="list-style-type: none"> - Cypress S71KS512SC0BHV000
2.4	USB Interface	Connection between RZ/A2M USB2.0 host/function module and USB connector
2.5	MIPI CSI-2 Interface	Connection between RZ/A2M MIPI CSI-2 interface and FPC connector
2.6	I/O Ports	Connection between RZ/A2M Input/output port and LEDs/DIP switches
2.7	Clock Configuration	System clock configuration
2.8	Reset Control	Reset control for devices mounted on RTK7921053C00000BE
2.9	Power Supply Configuration	System power supply configuration of RTK7921053C00000BE
2.10	Debug Interface	Connection between RZ/A2M user debug interface and CoreSight20 connector
2.11	SD/MMC Host Interface (4 bits)	Connection between RZ/A2M SD/MMC host interface (SDHI) channel 0 and microSD card slot
—	Operating specifications	Connectors, switches, and LEDs Details are described in Chapter 3

2.2 CPU

2.2.1 Overview of RZ/A2M

RTK7921053C00000BE contains a 32 bit RISC microcomputer RZ/A2M that runs in synchronization with the CPU clock (max. 528 MHz).

2.2.2 List of RZ/A2M Pin Functions

Table 2.2.1 to Table 2.2.14 list RZ/A2M pin functions used in RTK7921053C00000BE.

Table 2.2.1 List of Selections of RZ/A2M Pin Functions (1)

U1 Pin	Pin Name	Pin Function	Description	J2 Pin	Note
A1	Vcc				
A2	QSPI1_IO3		Connected to the serial flash memory (U2)	—	
A3	QSPI1_SPCLK		Connected to the serial flash memory (U2)	—	
A4	RPC_WP#		Open	—	
A5	QSPI0_IO3		Connected to the serial flash memory (U2)	—	
A6	PVcc_SPI				3.3V
A7	Vss				
A8	PVcc				
A9	PF_4 / RxD2 / DV0_DATA19 / LCD0_DATA4 / MTIOC6A / SSIBCK0 / IRQ1	DV0_DATA19	Used on the SUB board	113	
		LCD0_DATA4			
A10	PE_6 / ET0_MDIO / VIO_D2 / SSIRxD0 / MTIOC0D / CC2_RD1	ET0_MDIO	Used on the SUB board	107	
		VIO_D2			
A11	PL_2 / MD_BOOT2 / IRQ6	MD_BOOT2	Connected to the DIP switch (SW1)	—	PD_0: High
		IRQ6	Connected to the CC logic controller for USB (U7)		PD_0: Low
A12	PE_5 / ET0_MDC / VIO_D3 / SSITxD0 / MTIOC0C / CC1_RD1	ET0_MDC	Used on the SUB board	103	
		VIO_D3			
A13	P8_4 / A4 / DRP20 / DV0_DATA13 / SSL00 / SSIRxD3	A4	Used on the SUB board	101	
		DRP20			
		SSL00			
A14	P8_6 / A6 / DRP18 / DV0_DATA11 / MOSI0 / SSIFS3	A6	Used on the SUB board	95	
		DRP18			
		MOSI0			
A15	PE_4 / ET0_CRS/RMII0_CRSDV / VIO_D4 / SSIFS0 / MTIOC0B	ET0_CRS/RMII0_CRS	Used on the SUB board	91	
		DV VIO_D4			
A16	P9_1 / A9 / DRP15 / DV0_DATA8 / RxD4 / SSIFS2	A9	Used on the SUB board	83	
		DRP15			
		RxD4			
A17	PVcc				
A18	Vss				






[Note]  : 3.3V power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,  : GND displayed.

Table 2.2.2 List of Selections of RZ/A2M Pin Functions (2)

U1 Pin	Pin name	Pin Function	Description	J2 pin	Note
A19	PE_1 / ET0_RXD0/RMII0_RXD0 / VIO_D7 / RxD2 / POE8 / VBUSIN1 / IRQ1	ET0_RXD0/RMII0_RXD0	Used on the SUB board	73	
		VIO_D7			
A20	PA_4 / A20 / DV0_DATA9 / LCD0_DATA14 / SCI_TXD0 / MTIOC0C	DV0_DATA9	Used on the SUB board	69	
		LCD0_DATA14			
A21	CKIO		Used on the SUB board	54	
A22	Vss				
B1	PK_1 / ET1_TXD0/RMII1_TXD0 / NAF4 / CC1_RA0 / CAN_CLK / SSIDATA2	ET1_TXD0/RMII1_TXD0	Used on the SUB board	137	
		NAF4			
B2	Vcc				
B3	QSPI1_IO1		Connected to the serial flash memory (U2)	—	
B4	QSPI1_IO0		Connected to the serial flash memory (U2)	—	
B5	RPC_RESET#		Connected to the serial flash memory (U2)	—	
B6	QSPI0_IO1		Connected to the serial flash memory (U2)	—	
B7	QSPI0_SPCLK		Connected to the serial flash memory (U2)	—	
B8	PF_5 / TxD2 / DV0_DATA20 / LCD0_DATA3 / MTIOC6B / SSIFS0	DV0_DATA20	Used on the SUB board	115	
		LCD0_DATA3			
B9	P6_3 / ET0_TXD1/RMII0_TXD1 / VIO_HD / TxD3 / POE0	ET0_TXD1/RMII0_TXD1	Used on the SUB board	111	
		VIO_HD			
B10	PH_0 / AUDIO_CLK / VIO_D1 / GTIOC4A / MTIOC1A / CC1_RD0 / IRQ3	VIO_D1	Used on the SUB board	105	
B11	PL_3 / MD_BOOT1 / IRQ7	MD_BOOT1	Connected to the DIP switch (SW1)	—	PD_0: High SW1-4
		IRQ7	Connected to the USB CC logic controller (U7)		PD_0: Low
B12	PL_1 / MD_CLK / IRQ5	MD_CLK	Connected to the DIP switch (SW1)	48	PD_0: High SW1-2
		IRQ5	Used on the SUB board		PD_0: Low
B13	P8_3 / A3 / DRP21 / DV0_DATA14 / MTIOC6A / GTIOC3A	A3	Used on the SUB board	97	
		DRP21			
B14	PF_2 / TxD3 / DV0_DATA17 / LCD0_DATA6 / MTIOC7C / MISO1	DV0_DATA17	Used on the SUB board	93	
		LCD0_DATA6			
B15	P8_7 / A7 / DRP17 / DV0_DATA10 / RSPCK0 / SSIBCK3	A7	Used on the SUB board	87	
		DRP17			
		RSPCK0			

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND displayed.

Table 2.2.3 List of Selections of RZ/A2M Pin Functions (3)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
B16	PE_3 / ET0_RXER/RMII0_RXER / VIO_D5 / SSIBCK0 / MTIOC0A	ET0_RXER/RMII0_RXER	Used on the SUB board	79	
		VIO_D5			
B17	PA_0 / A16 / DV0_DATA13 / LCD0_DATA10 / SCI_TXD1 / MTIOC8C	DV0_DATA13	Used on the SUB board	77	
		LCD0_DATA10			
B18	PA_3 / A19 / DV0_DATA10 / LCD0_DATA13 / SCI_CTS0/RTS0 / MTIOC0D	DV0_DATA10	Used on the SUB board	68	
		LCD0_DATA13			
B19	PA_5 / A21 / DV0_DATA8 / LCD0_DATA15 / SCI_RXD0 / MTIOC0B / IRQ5	DV0_DATA8	Used on the SUB board	71	
		LCD0_DATA15			
B20	PA_6 / A22 / DV0_DATA7 / LCD0_DATA16 / SCI_SCK0 / MTIOC0A	DV0_DATA7	Used on the SUB board	67	
		LCD0_DATA16			
B21	Vss		Connected to the DIP switch (SW1)	—	SW1-8: ON
B22	PVcc				
C1	PH_2 / CTS2 / DV0_DATA22 / LCD0_DATA1 / MTIOC6D / SSIRxD0	DV0_DATA22	Used on the SUB board	143	
		LCD0_DATA1			
C2	P8_2 / A2 / DRP22 / DV0_DATA15 / GTIOC5A / IRQ2	A2	Used on the SUB board	141	
		DRP22			
C3	Vcc				
C4	QSPI1_SSL		Connected to a serial flash memory (U2)	—	
C5	RPC_INT#		Connect to the serial flash memory (U2)	—	
C6	QSPI0_SSL		Connected to the serial flash memory (U2)	—	
C7	QSPI0_IO0		Connected to the serial flash memory (U2)	—	
C8	P6_1 / ET0_TXEN/RMII0_TXDEN / VIO_CLK / SCK3 / MTIOC2A	ET0_TXEN/RMII0_TXDEN	Used on the SUB board	119	
		VIO_CLK			
C9	P6_2 / ET0_TXD0/RMII0_TXD0 / VIO_VD / RxD3 / MTIOC2B / OTG_EXICEN1 / IRQ0	ET0_TXD0/RMII0_TXD0	Used on the SUB board	106	
		VIO_VD			
C10	PH_1 / AUDIO_XOUT / VIO_D0 / GTIOC4B / MTIOC1B / CC2_RD0 / IRQ2	VIO_D0	Used on the SUB board	126	
C11	PL_4 / MD_BOOT0 / IRQ0	MD_BOOT0	Connect with DIP switch (SW1)	—	SW1-5
C12	PL_0 / MD_CLKS / IRQ4	IRQ4	Used on the SUB board	50	PD_0: Low
		MD_CLKS	Connected to the DIP switch (SW1)	—	PD_0: High SW1-1






[Note]  : 3.3V power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,  : GND displayed.

Table 2.2.4 List of Selections of RZ/A2M Pin Functions (4)

U1 Pin	Pin Name	Pin Function	Description	J2 Pin	Note
C13	P8_5 / A5 / DRP19 / DV0_DATA12 / MISO0 / SSITxD3	A5	Used on the SUB board	92	
		DRP19			
C14	PF_1 / RxD3 / DV0_DATA16 / LCD0_DATA7 / MTIOC7B / MOSI1 / IRQ4	DV0_DATA16	Used on the SUB board	88	
		LCD0_DATA7			
C15	P9_0 / A8 / DRP16 / DV0_DATA9 / TxD4 / SSIDATA2	A8	Used on the SUB board	84	
		DRP16			
		TxD4			
C16	PE_2 / ET0_RXD1/RMII0_RXD1 / VIO_D6 / TxD2 / POE10	ET0_RXD1/RMII0_RXD1	Used on the SUB board	78	
		VIO_D6			
C17	PA_2 / A18 / DV0_DATA11 / LCD0_DATA12 / SCI_SCK1 / MTIOC8A	DV0_DATA11	Used on the SUB board	74	
		LCD0_DATA12			
C18	PG_0 / ET0_TXCLK / VIO_D8 / RSPCK0 / MTIOC3A / HM_RSTO#	VIO_D8	Used on the SUB board	72	
C19	PB_0 / A24 / DV0_DATA5 / LCD0_DATA18 / SSITxD1 / POE8	DV0_DATA5	Used on the SUB board	64	
		LCD0_DATA18			
C20	Vss		Connected to the DIP switch (SW1)	—	SW1-7: ON
C21	PD_7 / RIIC3SDA / IRQ7	RIIC3SDA	Used on the SUB board	58	
C22	PD_3 / RIIC1SDA / IRQ3 / MTCLKD / GTETRGD	PD_3	Connected to the MIPI CSI-2 connector (CN2, J1)	—	
D1	PVcc				
D2	BSCANP		Connected to the DIP switch (SW1)	—	SW1-6
D3	P8_1 / A1 / DRP23 / DV0_DATA16 / GTIOC5B / IRQ3	A1	Used on the SUB board	128	
		DRP23			
D4	Vcc				
D5	QSPI1_IO2		Connected to the serial flash memory (U2)	—	
D6	Vss				
D7	QSPI0_IO2		Connected to the serial flash memory (U2)	—	
D8	PK_0 / ET1_TXEN/RMII1_TXDEN / NAF3 / CC1_RD0 / MTIOC1B / SSIBCK2	ET1_TXEN/RMII1_TXDEN	Used on the SUB board	110	
		NAF3			
D9	PF_6 / RTS2 / DV0_DATA21 / LCD0_DATA2 / MTIOC6C / SSITxD0	DV0_DATA21	Used on the SUB board	108	
		LCD0_DATA2			
D10	PE_0 / ET0_RXCLK/REF50CK0 / VIO_FLD / SCK2 / POE4	ET0_RXCLK/REF50CK0	Used on the SUB board	102	
		VIO_FLD			






[Note]  : 3.3V power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,  : GND displayed.

Table 2.2.5 List of Selections of RZ/A2M Pin Functions (5)

U1 Pin	Pin Name	Pin Function	Description	J2 Pin	Note
D11	PF_3 / SCK2 / DV0_DATA18 / LCD0_DATA5 / MTIOC7D / SSL10	DV0_DATA18 LCD0_DATA5	Used on the SUB board	124	
D12	PVcc				
D13	Vss				
D14	PF_0 / SCK3 / DV0_DATA15 / LCD0_DATA8 / MTIOC7A / RSPCK1	DV0_DATA15 LCD0_DATA8	Used on the SUB board	90	
D15	P8_0 / A0 / DV0_DATA14 / LCD0_DATA9 / SCI_CTS1/RTS1 / MTIOC8D	DV0_DATA14 LCD0_DATA9	Used on the SUB board	86	
D16	PA_1 / A17 / DV0_DATA12 / LCD0_DATA11 / SCI_RXD1 / MTIOC8B / IRQ6	DV0_DATA12 LCD0_DATA11	Used on the SUB board	80	
D17	PA_7 / A23 / DV0_DATA6 / LCD0_DATA17 / SSIRxD1 / POE10	DV0_DATA6 LCD0_DATA17	Used on the SUB board	76	
D18	PVcc				
D19	Vss				
D20	PD_6 / RIIC3SCL / IRQ6	RIIC3SCL	Used on the SUB board	60	
D21	PD_4 / RIIC2SCL / IRQ4	RIIC2SCL	Connected to the MIPI CSI-2 connector (CN2, J1) or USB CC logic controller (U7)	—	
D22	PD_1 / RIIC0SDA / IRQ1 / MTCLKB / GTETRGB	PD_1	Controlling power supply to PVcc_SD0	—	0 : 1.8V 1 : 3.3V
E1	Vss				
E2	PH_3 / HM_RSTO# / RTS2 / GTIOC6A / MTIOC2A / SD0_CD / IRQ3	HM_RSTO#	Connected to the HyperMCP (U3)	—	
E3	PK_3 / ET1_RXCLK/REF50CK1 / NAF6 / CC2_RD0 / CAN0RX_DATARATE_EN / MOSI0	ET1_RXCLK/REF50CK1 NAF6	Used on the SUB board	132	
E4	PK_2 / ET1_TXD1/RMII1_TXD1 / NAF5 / VBUSEN1 / CAN0RX / RSPCK0 / IRQ5	ET1_TXD1/RMII1_TXD1 NAF5	Used on the SUB board	133	
E19	PD_5 / RIIC2SDA / IRQ5	RIIC2SDA	Connected to the MIPI CSI-2 connector (CN2, J1) or USB CC logic controller (U7)	—	
E20	PD_2 / RIIC1SCL / IRQ2 / MTCLKC / GTETRGC	PD_2	Connected to the MIPI CSI-2 connector (CN2, J1)	—	
E21	JP0_3 / TCK	TCK	Connected to the UDI connector (CN5)	—	
E22	JP0_0 / TDI	TDI	Connected to the UDI connector (CN5)	—	
F1	PVcc_HO				1.8V
F2	HM_CS0#/OM_CS0#	HM_CS0#	Connected to the HyperMCP (U3)	—	
F3	HM_CK/OM_SCLK	HM_CK	Connected to the HyperMCP (U3)	—	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND displayed.

Table 2.2.6 List of Selections of RZ/A2M Pin Functions (6)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
F4	PF_7 / GTETRGD / DV0_DATA23 / LCD0_DATA0 / MTCLKD / IRQ1	DV0_DATA23	Used on the SUB board	136	
		LCD0_DATA0			
F19	PD_0 / RIIC0SCL / IRQ0 / MTCLKA / GTETRGA	PD_0	Controlling PL_[3:0] connection destination	—	0 : IRQ input 1 : SW1
F20	JP0_4 / TRST#	TRST#	Connected to the UDI connector (CN5)	—	
F21	JP_2 / TMS	TMS	Connected to the UDI connector (CN5)	—	
F22	PB_1 / A25 / DV0_DATA4 / LCD0_DATA19 / SSIFS1 / POE4	DV0_DATA4	Used on the SUB board	63	
		LCD0_DATA19			
G1	HM_DQ1/OM_SIO1	HM_DQ1	Connected to the HyperMCP (U3)	—	
G2	HM_RWDS/OM_DQS	HM_RWDS	Connected to the HyperMCP (U3)	—	
G3	HM_CS1#/OM_CS1#	HM_CS1#	Connected to the HyperMCP (U3)	—	
G4	HM_CK#		Connected to the HyperMCP (U3)	—	
G19	JP0_1 / TDO	TDO	Connected to the UDI connector (CN5)	—	
G20	PB_2 / BS / DV0_DATA3 / LCD0_DATA20 / SSIBCK1 / POE0	DV0_DATA3	Used on the SUB board	66	
		LCD0_DATA19			
G21	PB_3 / CS0 / DV0_DATA2 / LCD0_DATA21 / SSIDATA2 / CTS0	DV0_DATA2	Used on the SUB board	61	
		LCD0_DATA21			
G22	P9_2 / A10 / DRP14 / DV0_DATA7 / SCK4 / SSIBCK2	A10	Used on the SUB board	59	
		DRP14			
H1	HM_DQ4/OM_SIO4	HM_DQ4	Connected to the HyperMCP (U3)	—	
H2	HM_DQ2/OM_SIO2	HM_DQ2	Connected to the HyperMCP (U3)	—	
H3	HM_DQ3/OM_SIO3	HM_DQ3	Connected to the HyperMCP (U3)	—	
H4	HM_DQ0/OM_SIO0	HM_DQ0	Connected to the HyperMCP (U3)	—	
H19	PB_4 / CS1 / DV0_DATA1 / LCD0_DATA22 / SSIFS2 / RTS0	DV0_DATA1	Used on the SUB board	40	
		LCD0_DATA22			
H20	P9_3 / A11 / DRP13 / DV0_DATA6 / SSIRxD0	A11	Used on the SUB board	42	
		DRP13			
		SSIRxD0			
H21	PB_5 / WAIT / DV0_DATA0 / LCD0_DATA23 / SSIBCK2 / TxD0	DV0_DATA0	Used on the SUB board	57	
		LCD0_DATA23			
H22	P9_5 / A13 / DRP11 / DV0_DATA4 / SSIFS0	A13	Used on the SUB board	55	
		DRP11			
		SSIFS0			
J1	HM_RESET#/OM_RESET#	HM_RESET#	Connected to the HyperMCP (U3)	—	
J2	HM_DQ6/OM_SIO6	HM_DQ6	Connected to the HyperMCP (U3)	—	
J3	HM_DQ7/OM_SIO7	HM_DQ7	Connected to the HyperMCP (U3)	—	
J4	HM_DQ5/OM_SIO5	HM_DQ5	Connected to the HyperMCP (U3)	—	
J9	Vcc				
J10	Vss				
J11	Vss				
J12	Vss				
J13	Vss				
J14	Vcc				






[Note]  : 3.3V power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,
 : GND displayed.

Table 2.2.7 List of Selections of RZ/A2M Pin Functions (7)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
J19	P9_4 / A12 / DRP12 / DV0_DATA5 / SSITxD0	A12	Used on the SUB board	112	
		DRP12			
		SSITxD0			
J20	P7_7 / RD / DV0_HSYNC / LCD0_TCON0 / GTIOC3B / RxD0	DV0_HSYNC	Used on the SUB board	44	
		LCD0_TCON			
J21	P7_6 / AH / DV0_VSYNC / LCD0_TCON1 / GTIOC3A / SCK0	GTIOC3A	Used on the SUB board	53	
		DV0_VSYNC			
J22	P9_6 / A14 / DRP10 / DV0_DATA3 / SSIBCK0	A14	Used on the SUB board	49	
		DRP10			
		SSIBCK0			
K1	Vss				
K2	PJ_6 / GTETRGC / FCE / LCD0_CLK / MTCLKC / IRQ0	LCD0_CLK	Used on the SUB board	147	
		FCE			
K3	PH_4 / HM_INT# / CTS2 / GTIOC6B / MTIOC2B / SD0_WP / IRQ2	HM_INT#	Connected to the HyperMCP (U3)	—	
K4	PJ_0 / TRACECLK / SPDIF_OUT / VRAMMON0 / SCK1 / SSIRxD3	TRACECLK	Connected to the UDI connector (CN5)	—	
K9	Vcc				
K10	Vss				
K11	Vss				
K12	Vss				
K13	Vss				
K14	Vcc				
K19	P9_7 / A15 / DRP09 / DV0_DATA2 / SD1_WP	A15	Used on the SUB board	118	
		DRP09			
K20	PG_1 / ET0_TXD2 / VIO_D9 / MOSI0 / MTIOC3C / HM_INT#	VIO_D9	Used on the SUB board	116	
K21	P7_5 / CKE / DRP08 / DV0_DATA1 / CTS1 / OVRCUR1	CKE	Used on the SUB board	45	
		DRP08			
		CTS1			
		OVRCUR1			
K22	PG_2 / ET0_TXD3 / VIO_D10 / MISO0 / MTIOC3B / GTIOC0A / IRQ4	VIO_D10	Used on the SUB board	43	
L1	PVcc				
L2	P0_1 / D1 / DRP25 / DV0_DATA18 / MTIOC6C / GTIOC4A	D1	Used on the SUB board	151	
		DRP25			
L3	P0_0 / D0 / DRP24 / DV0_DATA17 / MTIOC6B / GTIOC3B	D0	Used on the SUB board	144	
		DRP24			
L4	PJ_7 / GTETRGB / NAF0 / LCD0_EXTCLK / MTCLKB	LCD0_EXTCLK	Used on the SUB board	140	
		NAF0			
L9	Vcc				
L10	Vss				

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND displayed.

Table 2.2.8 List of Selections of RZ/A2M Pin Functions (8)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
L11	Vss				
L12	Vss				
L13	Vss				
L14	Vcc				
L19	P7_1 / RD/WR / DRP05 / DV0_VSYNC / RxD1 / CC1_RA1	RD/WR	Used on the SUB board	123	
		DRP05			
		RxD1			
L20	P7_4 / CAS / DRP07 / DV0_DATA0 / RTS1 / CC2_RA1	CAS	Used on the SUB board	120	
		DRP07			
		RTS1			
L21	P7_3 / RAS / DRP06 / DV0_HSYNC / TxD1 / CC2_RD1	RAS	Used on the SUB board	41	
		DRP06			
		TxD1			
L22	P7_2 / CS4 / DV0_CLK / LCD0_TCON2 / TEND0 / CC2_RA0	DV0_CLK	Used on the SUB board	37	
M1	P0_2 / D2 / DRP26 / DV0_DATA19 / MTIOC6D / GTIOC4B	D2	Used on the SUB board	155	
		DRP26			
M2	P0_5 / D5 / DRP29 / DV0_DATA22 / MTIOC7C / GTIOC7A	D5	Used on the SUB board	153	
		DRP29			
M3	P0_4 / D4 / DRP28 / DV0_DATA21 / MTIOC7B / GTIOC6B	D4	Used on the SUB board	146	
		DRP28			
M4	P0_3 / D3 / DRP27 / DV0_DATA20 / MTIOC7A / GTIOC6A	D3	Used on the SUB board	148	
		DRP27			
M9	Vcc				
M10	Vss				
M11	Vss				
M12	Vss				
M13	Vss				
M14	Vcc				
M19	P6_6 / CS2 / DRP02 / LCD0_TCON4 / DREQ0 / CC1_RA0	DRP02	Used on the SUB board	127	
M20	P6_0 / ADTRG0	P6_0	Connected to the LED1 (red)	125	1 : Lit
M21	P7_0 / WE1/DQMU / DRP04 / DV0_CLK / SCK1 / CC1_RD1	WE1/DQML	Used on the SUB board	25	
		DRP04			
		SCK1			
M22	PVcc				
N1	PJ_3 / TRACEDATA1 / NAF0 / VRAMMON3 / RTS1 / SSIFS3	TRACEDATA1	Connected to the UDI connector (CN5)	—	
N2	PJ_1 / TRACECTL / SPDIF_IN / VRAMMON1 / RxD1 / VBUSIN0 / IRQ0	IRQ0	Used on the SUB board	159	
N3	P0_6 / D6 / DRP30 / DV0_DATA23 / MTIOC7D / GTIOC7B	D6	Used on the SUB board	150	
		DRP30			

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND displayed.

Table 2.2.9 List of Selections of RZ/A2M Pin Functions (9)

U1 Pin	Terminal name	Terminal function	Explanation	J2 pin	Notes
N4	PJ_2 / TRACEDATA0 / FCE / VRAMMON2 / TxD1 / SSITxD3	TRACEDATA0	Connected to the UDI connector (CN5)	—	
N9	Vcc				
N10	Vss				
N11	Vss				
N12	Vss				
N13	Vss				
N14	Vcc				
N19	P6_5 / CS3 / DRP01 / LCD0_TCON5 / AUDIO_XOUT / CC1_RD0	CS3	Used on the SUB board	135	
		DRP01			
N20	PG_3 / ET0_COL / VIO_D11 / SSL00 / MTIOC3D / GTIOC0B	VIO_D11	Used on the SUB board	129	
N21	P6_4 / CS5 / DRP00 / LCD0_TCON6 / AUDIO_CLK / SD1_CD	DRP00	Used on the SUB board	36	
		AUDIO_CLK			
N22	Vss				
P1	PH_6 / HM_INT# / NAF3 / ET1_WOL / MTIC5V / IRQ4	ET1_WOL	Used on the SUB board	163	
P2	PH_5 / HM_RSTO# / NAF2 / ET1_EXOUT / MTIC5U / IRQ5	ET1_EXOUT	Used on the SUB board	161	
		NAF2			
P3	PK_5 / GTETRGA / NAF1 / WDTOVF/PERROUT / MTCLKA	NAF1	Used on the SUB board	167	
P4	PVcc				
P9	Vcc				
P10	Vss				
P11	Vss				
P12	Vss				
P13	Vss				
P14	Vcc				
P19	SD0_DAT7		Connected to the SDVcc through a resistor	—	
P20	SD0_RST#		Connected to the test point (TP1)	—	
P21	P6_7 / WE0/DQML / DRP03 / LCD0_TCON3 / DACK0 / CC2_RD0	WE0/DQML	Used on the SUB board	23	
		DRP03	Used on the SUB board		
P22	PVcc_SD0				
R1	PVcc				
R2	PJ_4 / TRACEDATA2 / NAF1 / VRAMMON4 / CTS1 / SSIBCK3	TRACEDATA2	Connected to the UDI connector (CN5)	—	
R3	PJ_5 / TRACEDATA3 / NAF2 / OVRCUR0 / MTIOC1A / SSIFS2 / IRQ4	TRACEDATA3	Connected to the UDI connector (CN5)	—	
R4	Vss				
R19	SD0_DAT2		Connected to the microSD card slot (CN1)	—	
R20	SD0_DAT5		Connected to the SDVcc through a resistor	—	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND displayed.

Table 2.2.10 List of Selections of RZ/A2M Pin Functions (10)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
R21	SD0_DAT4		Connected to the SDVcc through a resistor	—	
R22	SD0_DAT6		Connected to the SDVcc through a resistor	—	
T1	AUDIO_X1		Connected to the GND through a resistor	—	
T2	AUDIO_X2		Open	—	
T3	P3_5 / ET1_RXD1/RMII1_RXD1 / FCLE / CC2_RA0 / CAN0TX_DATARATE_EN / SSL00	ET1_RXD1/RMII1_RXD1	Used on the SUB board	156	
		FCLE			
T4	P3_2 / ET1_CRSDV/RMII1_CRSDV / FRE / CC1_RA1 / CAN1RX_DATARATE_EN / MOSI2	ET1_CRSDV/RMII1_CRSDV	Used on the SUB board	154	
		FRE			
T19	SD0_DAT0		Connected to the microSD card slot (CN1)	—	
T20	SD0_DAT1		Connected to the microSD card slot (CN1)	—	
T21	SD0_DAT3		Connected to the microSD card slot (CN1)	—	
T22	Vss				
U1	Vss				
U2	PK_4 / ET1_RXD0/RMII1_RXD0 / NAF7 / OVRCUR1 / CAN0TX / MISO0 / IRQ6	ET1_RXD0/RMII1_RXD0	Used on the SUB board	164	
		NAF7			
U3	P3_1 / ET1_RXER/RMII1_RXER / FALE / VBUSEN0 / CAN1RX / RSPCK2 / IRQ6	ET1_RXER/RMII1_RXER	Used on the SUB board	166	
		FALE			
U4	MIPIAVcc18_1				
U19	SD1_DAT0		Used on the SUB board	33	
U20	SD1_DAT2		Used on the SUB board	31	
U21	SD0_CMD		Connected to the microSD card slot (CN1)	—	
U22	SD0_CLK		Connected to the microSD card slot (CN1)	—	
V1	CSI_CLKP		Connected to the MIPI CSI-2 connector (CN2, J1)	—	
V2	CSI_CLKN		Connected to the MIPI CSI-2 connector (CN2, J1)	—	
V3	PG_4 / ET0_TXER / VIO_D15 / RSPCK1 / MTIOC4A / GTIOC1A	VIO_D15	Used on the SUB board	169	
V4	Vss				
V19	P5_4 / AN004 / IRQ0 / SD1_CD	SD1_CD	Used on the SUB board	18	
V20	SD1_DAT1		Used on the SUB board	29	
V21	SD1_DAT3		Used on the SUB board	32	
V22	PVcc_SD1				3.3V






[Note]  : 3.3V power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,  : GND displayed.

Table 2.2.11 List of Selections of RZ/A2M Pin Functions (11)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
W1	CSI_DATA0P		Connected to the MIPI CSI-2 connector (CN2, J1)	—	
W2	CSI_DATA0N		Connected to the MIPI CSI-2 connector (CN2, J1)	—	
W3	Vss				
W4	PG_6 / ET0_RXD2 / VIO_D13 / MISO1 / MTIOC4C / GTIOC2A / IRQ5	VIO_D13	Used on the SUB board	171	
W5	P1_0 / D7 / DRP31 / IRQ0 / CAN_CLK / VBUSEN0	D7 DRP31	Used on the SUB board	160	
W6	P1_2 / D9 / MTIOC8B / IRQ2 / CAN0RX_DATARATE_EN / VBUSEN1	D9	Used on the SUB board	196	
W7	P2_0 / D12 / GTIOC6A / IRQ5 / CAN1RX / OTG_EXICEN0	D12	Used on the SUB board	200	
W8	PC_2 / OTG_EXICEN0 / NAF7 / ET1_TXD3 / MISO2 / LCD0_TCON5	PC_2	Used on the SUB board	202	
W9	P4_3 / RTS0 / TXOUT1M / SCI_CTS1/RTS1 / SSIFS1 / MTIOC8D / IRQ3	TXOUT1M	Used on the SUB board	184	
W10	LVDSAPVcc				
W11	Vss				
W12	LVDSPLLVcc				
W13	USBDPVcc0				
W14	USBVss				
W15	Vss				
W16	PVcc				
W17	Vss				
W18	PLLVcc				
W19	P5_2 / AN002 / IRQ6 / VBUSIN0	VBUSIN0	Connected to the USB connector (CN3)	—	JP3
W20	P5_6 / AN006 / IRQ2	AN006	Used on the SUB board	14	
W21	SD1_CMD		Used on the SUB board	28	
W22	Vss				
Y1	CSI_DATA1P		Connected to the MIPI CSI-2 connector (CN2, J1)	—	
Y2	CSI_DATA1N		Connected to the MIPI CSI-2 connector (CN2, J1)	—	
Y3	Vss				
Y4	P3_3 / ET1_MDC / FWE / OTG_EXICEN0 / CAN1TX / MISO2 / IRQ7	ET1_MDC FWE	Used on the SUB board	177	
Y5	P1_4 / D11 / MTIOC8D / IRQ4 / CAN0TX_DATARATE_EN / VBUSIN0	D11	Used on the SUB board	173	
Y6	PC_0 / VBUSIN1 / NAF5 / ET1_TXCLK / RSPCK2 / IRQ2	VBUSIN1	Used on the SUB board	194	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND displayed.

Table 2.2.12 List of Selections of RZ/A2M Pin Functions (12)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
Y7	P2_2 / D14 / GTIOC7A / IRQ7 / CAN1TX / VBUSIN1	D14	Used on the SUB board	198	
Y8	P4_2 / TxD0 / TXOUT1P / SCI_TXD1 / SSITxD1 / MTIOC8C / IRQ2	TXOUT1P	Used on the SUB board	182	
Y9	P4_6 / ET0_EXOUT / TXCLKOUTP / SCI_TXD0 / TxD4 / DACK0	TXCLKOUTP	Used on the SUB board	188	
Y10	NMI		Used on the SUB board	203	
Y11	Vss				
Y12	USBVss				
Y13	USBVss				
Y14	USBVss				
Y15	USBVss				
Y16	USBDPVcc1				
Y17	PC_7 / OVRCUR0 / FRB / ET1_RXD3 / SD1_WP / LCD0_TCON0 / IRQ6	OVRCUR0	Connected to the USB VBUS power supply control IC (U5)	—	
Y18	PC_6 / VBUSEN0 / FWE / ET1_RXD2 / SD1_CD / LCD0_TCON1 / IRQ7	VBUSEN0	Connected to the USB VBUS power supply control IC (U5)	—	
Y19	P5_0 / AN000 / IRQ4 / SD0_CD / SD1_CD	SD0_CD	Connected to the microSD card slot (CN1)	—	
Y20	P5_1 / AN001 / IRQ5 / SD0_WP / SD1_WP	SD0_WP	Connected to the D3.3V or GND through a resistor	—	
Y21	P5_7 / AN007 / IRQ3	IRQ3	Used on the SUB board	19	
Y22	SD1_CLK		Used on the SUB board	24	
AA1	MIPIAVcc18_2				
AA2	Vss				
AA3	P1_1 / D8 / MTIOC8A / IRQ1 / CAN0RX / OVRCUR0	D8	Used on the SUB board	179	
AA4	P3_4 / ET1_MDIO / FRB / CC2_RA1 / CAN1TX_DATARATE_EN / SSL20	ET1_MDIO FRB	Used on the SUB board	187	
AA5	P3_0 / OTG_EXICEN1 / NAF4 / ET1_LINKSTA / MTIC5W / IRQ3	ET1_LINKSTA	Used on the SUB board	191	
AA6	PC_1 / VBUSIN0 / NAF6 / ET1_TXD2 / MOSI2 / LCD0_TCON6	PC_1	Connected to the LED 1 (yellow green)	197	1 : illuminated
AA7	P4_0 / SCK0 / TXOUT0P / SCI_SCK1 / SSIBCK1 / MTIOC8A / IRQ0	TXOUT0P	Used on the SUB board	170	
AA8	P4_4 / CTS0 / TXOUT2P / SCI_CTS0/RTS0 / WDTOVF/PERROUT / OTG_EXICEN0	TXOUT2P	Used on the SUB board	176	
AA9	P4_7 / ET0_WOL / TXCLKOUTM / SCI_SCK0 / SCK4 / TEND0	TXCLKOUTM	Used on the SUB board	190	
AA10	USB_X2		Connected to the USB oscillator (X2)	—	48MHz






[Note]  : 3.3 power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,
 : GND displayed.

Table 2.2.13 List of Selections of RZ/A2M Pin Functions (13)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
AA11	DP0		Connected to the USB connector (CN3)	—	
AA12	USBAPVcc0				
AA13	RREF0		Connected to the GND through a resistor	—	2.2kΩ±1%
AA14	USBVss				
AA15	DP1		Used on the SUB board	96	
AA16	PVcc				
AA17	PC_5 / VBUSEN1 / FRE / ET1_RXDV / SPDIF_OUT / LCD0_TCON2 / IRQ0	VBUSEN1	Used on the SUB board	8	
AA18	XTAL		Connected to the system clock oscillator (X1)	—	24MHz
AA19	PC_4 / OTG_ID1 / FALE / ET1_TXER / SPDIF_IN / LCD0_TCON3 / IRQ1	LCD0_TCON3	Used on the SUB board	20	
AA20	RTC_X2		Connected to the RTC oscillator (X3)	—	32.768kHz
AA21	P5_3 / AN003 / IRQ7 / OTG_ID0	P5_3	Used on the SUB board	15	
AA22	P5_5 / AN005 / IRQ1 / SD1_WP	SD1_WP	Used on the SUB board	17	
AB1	Vss				
AB2	PG_5 / ET0_RXDV / VIO_D14 / MOSI1 / MTIOC4B / GTIOC1B	VIO_D14	Used on the SUB board	183	
AB3	PG_7 / ET0_RXD3 / VIO_D12 / SSL10 / MTIOC4D / GTIOC2B	VIO_D12	Used on the SUB board	181	
AB4	P1_3 / D10 / MTIOC8C / IRQ3 / CAN0TX / OTG_ID1	D10	Used on the SUB board	189	
AB5	P2_1 / D13 / GTIOC6B / IRQ6 / CAN1RX_DATARATE_EN / OTG_ID0	D13	Used on the SUB board	193	
AB6	P2_3 / D15 / GTIOC7B / WDTOVF/PERROUT / CAN1TX_DATARATE_EN / OTG_EXICEN1	D15	Used on the SUB board	199	
AB7	P4_1 / RxD0 / TXOUT0M / SCI_RXD1 / SSIRxD1 / MTIOC8B / IRQ1	TXOUT0M	Used on the SUB board	172	
AB8	P4_5 / ET0_LINKSTA / TXOUT2M / SCI_RXD0 / RxD4 / DREQ0	TXOUT2M	Used on the SUB board	178	
AB9	RES#		Connected to the reset input switch (SW2)	7	
AB10	USB_X1		Connected to the USB oscillator (X2)	—	48MHz
AB11	DM0		Connected to the USB connector (CN3)	—	
AB12	USBAPVcc1				
AB13	RREF1		Connected to the GND through a resistor	—	2.2kΩ±1%











[Note]  : 3.3 power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,  : GND displayed.

Table 2.2.14 List of Selections of RZ/A2M Pin Functions (14)

Pin	Pin Name	Pin Function	Description	J2 Pin	Note
AB14	USBVss				
AB15	DM1		Used on the SUB board	98	
AB16	PVcc				
AB17	PC_3 / OTG_ID0 / FCLE / ET1_COL / SSL20 / LCD0_TCON4	LCD0_TCON4	Used on the SUB board	10	
AB18	EXTAL		Connected to the system clock oscillator (X1)	—	24MHz
AB19	Vss				
AB20	RTC_X1		Connected to the RTC oscillator (X3)	—	32.768kHz
AB21	AVcc				
AB22	AVcc				

[Note]  : 3.3 power source,  : 1.8V power source,  : 1.2V power source,  : 3.3V or 1.8V power source,  : GND displayed.

2.3 Memory

In addition to the RZ/A2M on-chip RAM, serial flash memory and HyperMCP are mounted in RTK7921053C00000BE as external memory.

Refer to the following for details.

2.3.1 RZ/A2M On-Chip RAM

The microprocessor RZ/A2M contains a 4 Mbyte large capacity RAM (sharing an area of 128 kbytes with the data retention on-chip RAM).

2.3.2 Serial Flash Memory

RTK7921053C00000BE is equipped with standard serial flash memory x 1 shown in Table 2.3.1. Serial flash memory is controlled by RZ/A2M on-chip SPI multi-I/O bus controller (SPIBSC). During boot (boot mode 3), data (programs) can be read from the serial flash memory.

Figure 2.3.1 shows serial flash memory block diagram.

Table 2.3.1 Overview of Serial Flash Memory

Memory Device	Model	Operational Voltage	Capacity	Package
Serial flash memory	MX25L51245GXDI-08G	3.3V	64MB	24 ball BGA

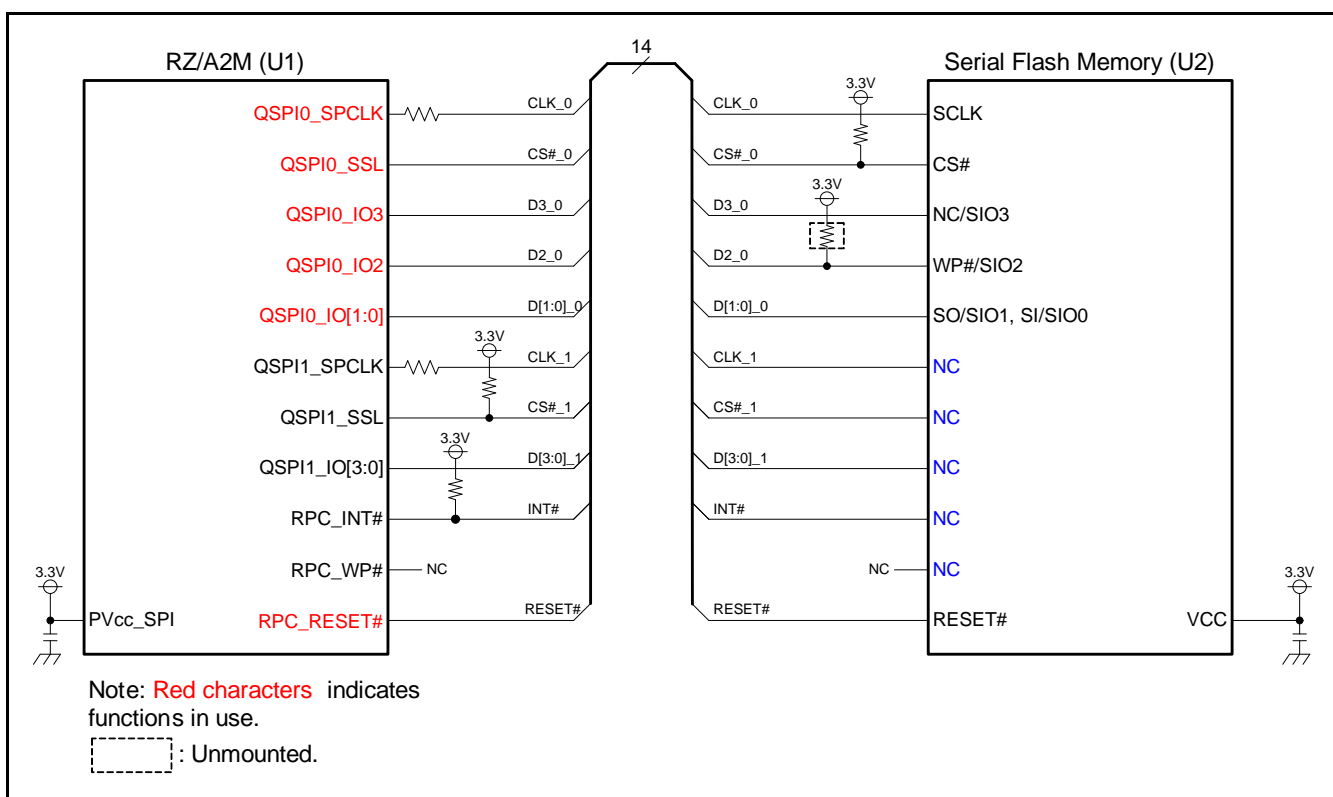


Figure 2.3.1 Serial Flash Memory Block Diagram

2.3.3 HyperMCP

RTK7921053C00000BE is equipped with HyperMCP x 1 shown in Table 2.3.2 as a default installation. HyperMCP is controlled by the HyperBus controller. During boot (boot mode 7), data (programs) can be read from the HyperFlash in HyperMCP.

Figure 2.3.2 shows HyperMCP block diagram.

Table 2.3.2 HyperMCP Overview

Memory types	Type name	RZ/A2M Connect with interface	Operational voltage	capacity	package
HyperMCP	S71KS512SC0BHV000	HyperBus controller	1.8V	HyperFlash: 64MB HyperRAM: 8MB	24 ball BGA

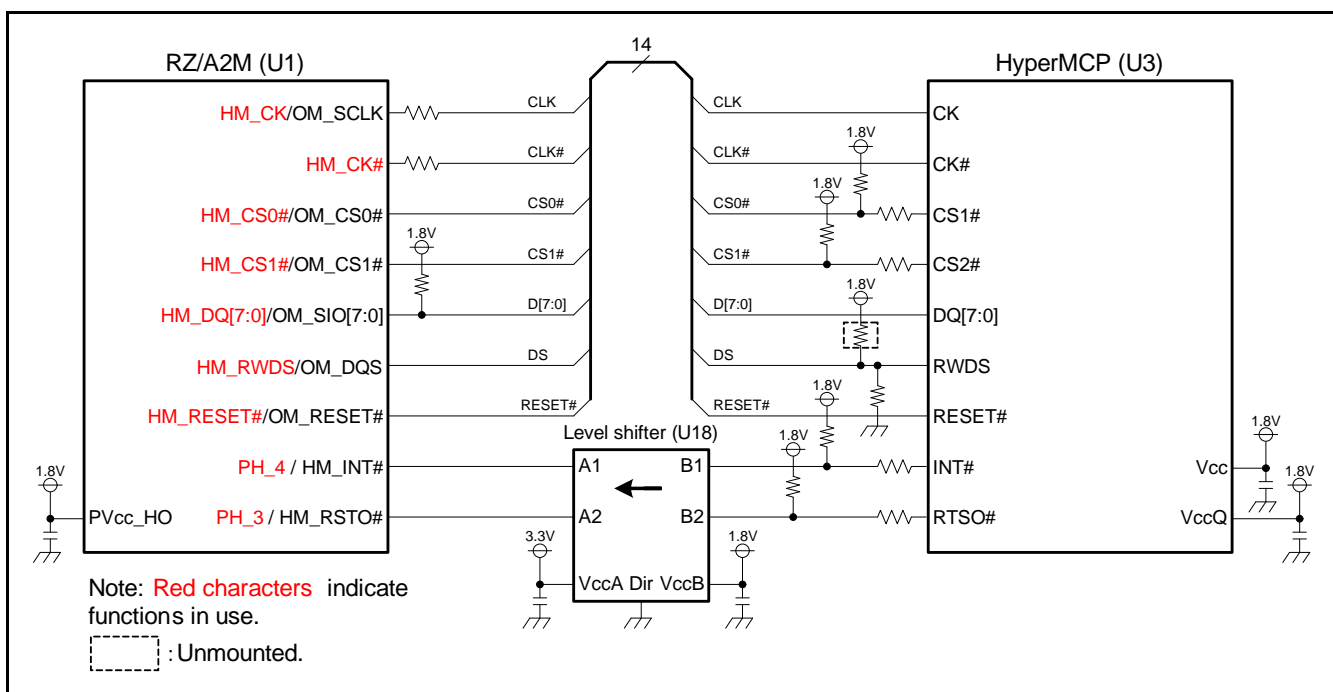


Figure 2.3.2 HyperMCP Block Diagram

2.4 USB Interface

USB Type-C receptacle x 1 is equipped with RTK7921053C00000BE as a default installation.

When using this receptacle as a USB host, attach JP3 because the VBUS voltage is supplied to the USB connector.

When using this receptacle as a USB function, detach JP3.

Moreover, USB port setting can be changed by the CC logic controller (U7) PORT terminal settings. Initial USB port settings are for DRP (Dual Role Port). If using as a USB host, mount R78 resistor and set USB port to DFP (Downstream Facing Port). If using for USB function, mount R79 resistor and set USB port to UFP (Upstream Facing Port).

Figure 2.4.1 shows USB interface block diagram, Table 2.4.1 shows jumper JP3 function setting table, Table 2.4.2 shows port L function switching table, and Table 2.4.3 shows USB port function switching table.

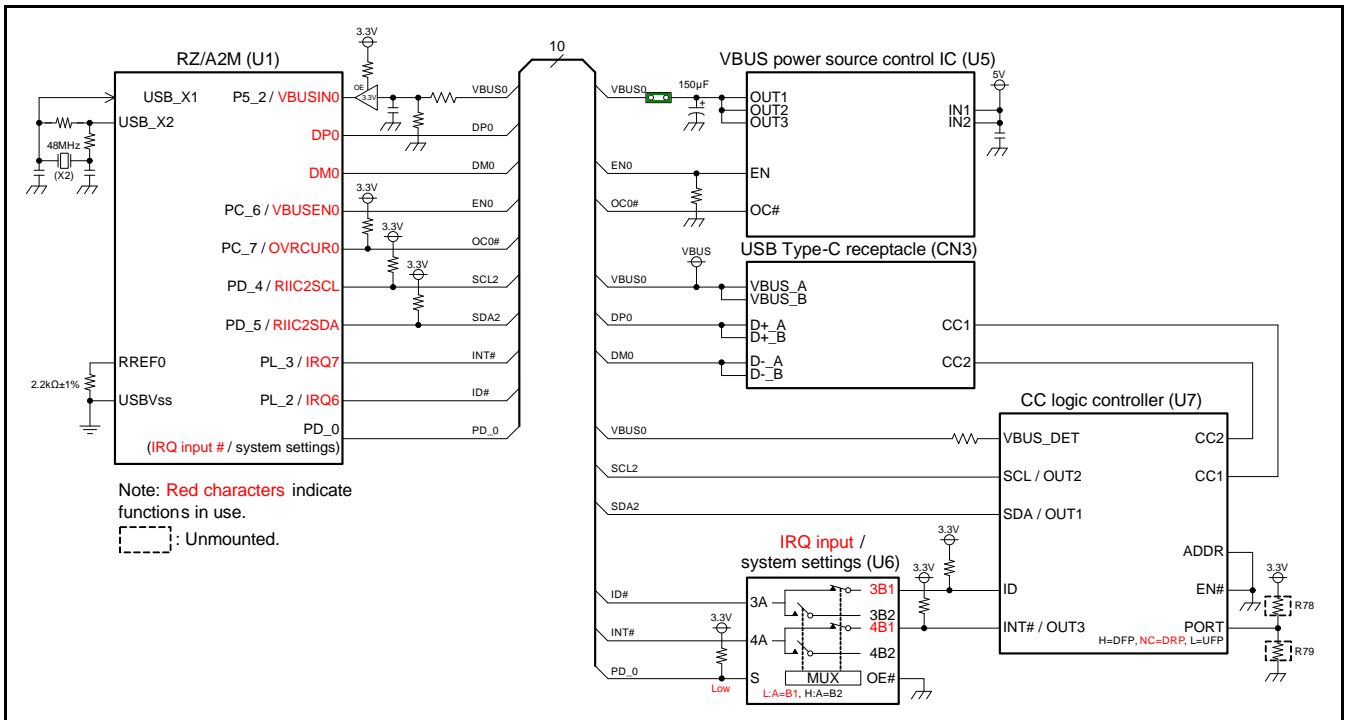


Figure 2.4.1 USB Interface Block Diagram

Table 2.4.1 Function Setting for Jumper JP3

Jumper	Short	Open
JP3	Supplies power to VBUS0.	Does not supply power to VBUS0. (Initial setting)

Table 2.4.2 Function Switching for Port L

Terminal	function	
	High	Low
PD_0	Uses PL_[3:0] as system setting pins. (Initial setting)	Uses PL_[3:0] as RQ input pins.


[Note]  shows the setting function to select.

Table 2.4.3 Function Switching for USB port

Terminal	function		
	High	NC	Low
PORT (U7)	Uses the USB port as DFP.	Uses the USB port as DRP. (Initial setting)	Uses the USB port as UFP.

2.5 MIPI CSI-2 Interface

The RZ/A2M contains MIPI CSI-2 interface that supports YCbCr422, RGB888, and RAW8 video. In RTK7921053C00000BE, the MIPI CSI-2 interface in RZ/A2M is connected to FPC connector. RTK7921053C00000BE also has board patterns that can mount a 1.0 mm pin header used as an expansion connector.

The MIPI CSI-2 pin is shared with the FPC connector and expansion connector. When the expansion connector is used, the FPC connector cannot be used.

Figure 2.5.1 shows the MIPI CSI-2 interface block diagram.

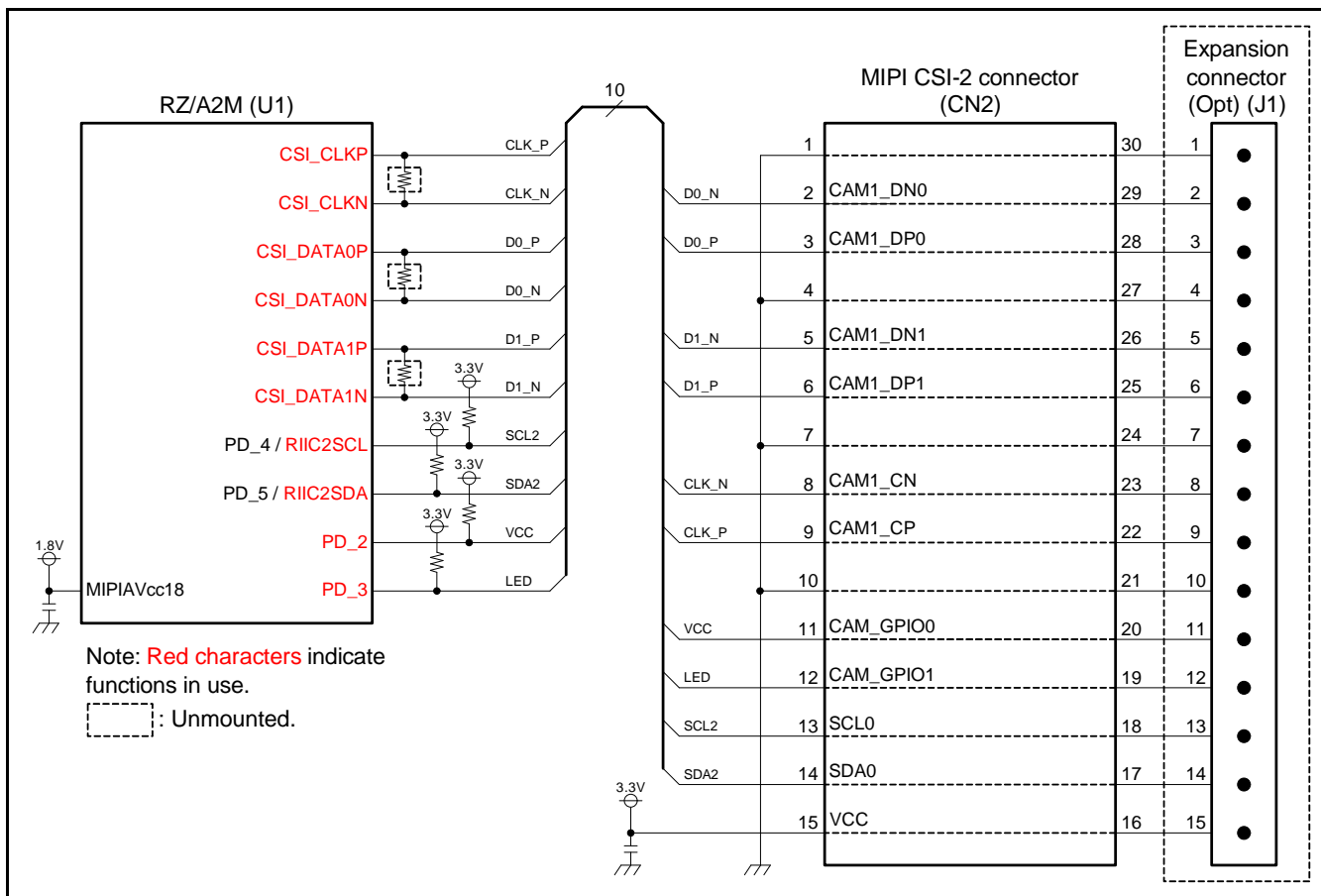


Figure 2.5.1 MIPI CSI-2 Interface Block Diagram

2.6 I/O Ports

In RTK7921053C00000BE, the I/O ports of the RZ/A2M are connected to switches and LEDs.

Figure 2.6.1 shows the I/O port block diagram. Table 2.6.1 shows the function switching for the port L.

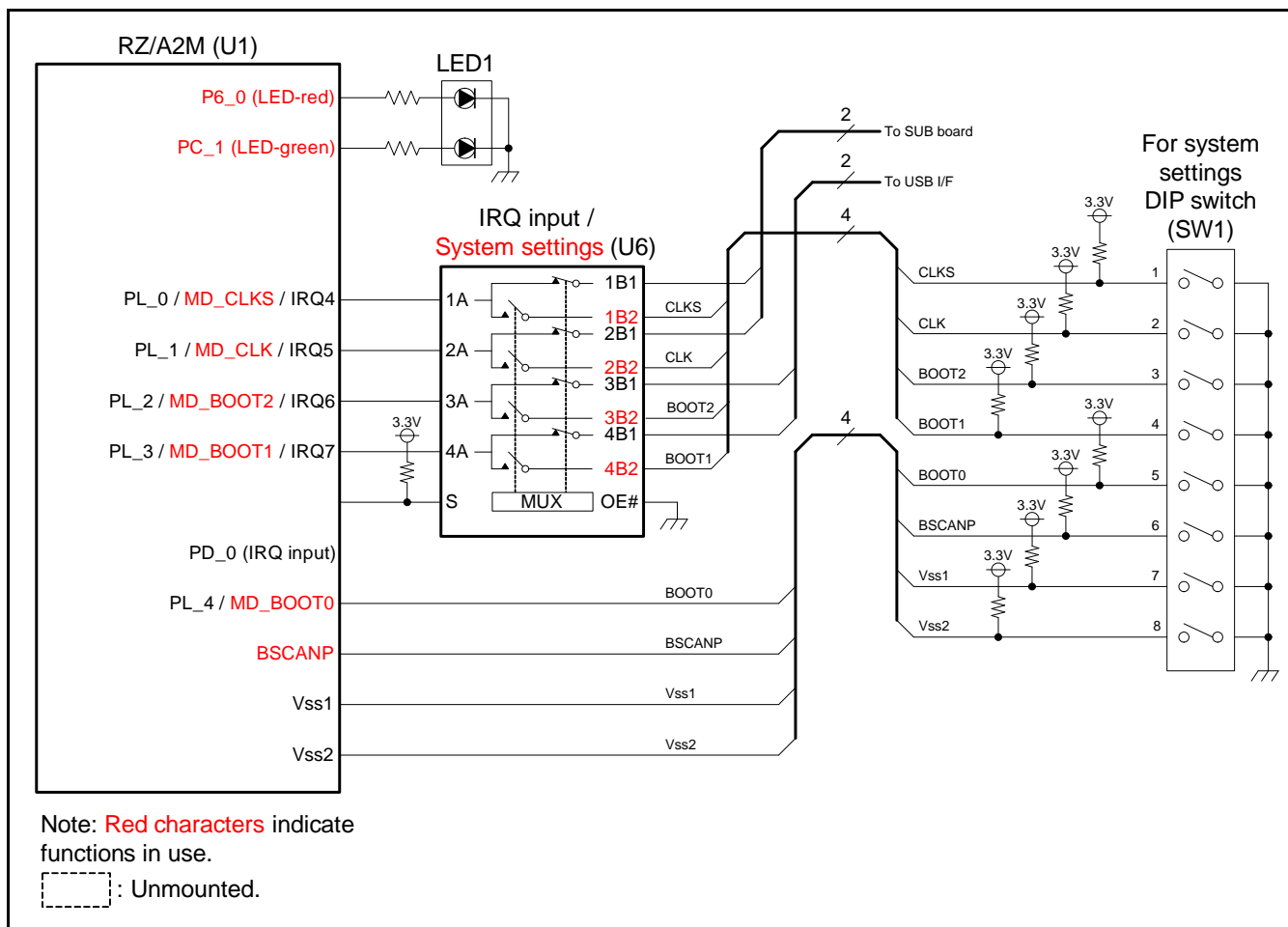


Figure 2.6.1 I/O Port Block Diagram

Table 2.6.1 Function Switching for Port L

Terminal	function	
	High	Low
PD_0	Uses PL_[3:0] as system setting pin. (Initial setting)	Uses PL_[3:0] as RQ input pin.

[Note] [] shows the setting function to select.

2.7 Clock Configuration

The following three types of clock are input to the RZ/A2M in RTK7921053C00000BE.

- RZ/A2M input clock : 24 MHz
- RZ/A2M USB clock : 48MHz
- RZ/A2M RTC clock : 32.768kHz

Figure 2.7.1 shows the clock configuration. Table 2.7.1 shows the function setting for the system settings DIP switches SW1-1 and SW1-2.

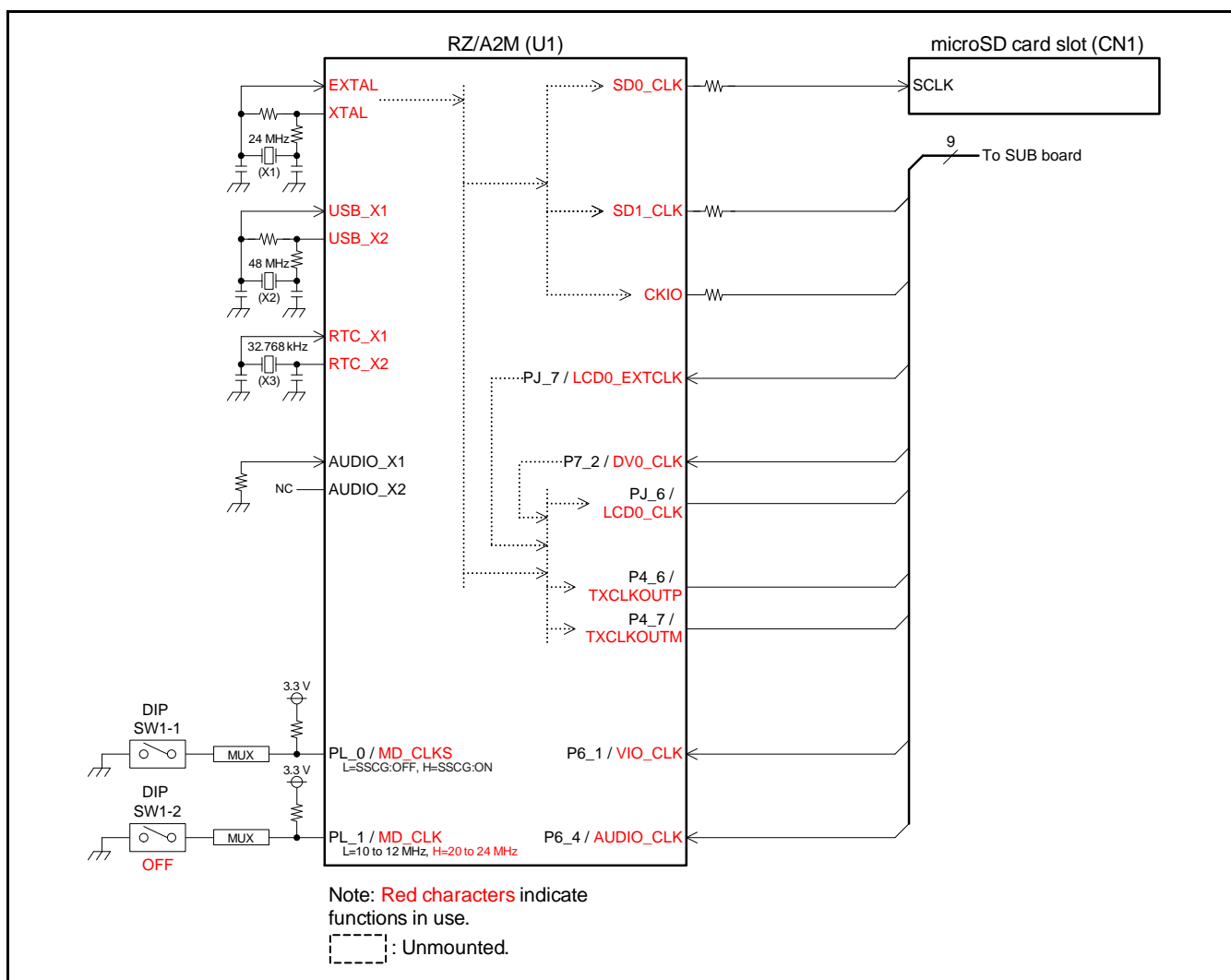


Figure 2.7.1 Clock Configuration

Table 2.7.1 Function Setting for System Settings DIP Switch SW1-1 and SW1-2

DIP switch	function	
	ON	OFF
SW1-1	SSCG function OFF (Initial setting)	SSCG function ON
SW1-2	Sets EXTAL input peripheral frequency range from 10 to 12MHz. (Setting prohibited)	Sets EXTAL input peripheral frequency range from 20 to 24MHz. (Initial setting)

[Note] shows the setting functions to select.

2.8 Reset Control

The reset IC in RTK7921053C00000BE controls the reset signal connected to the RZ/A2M, memory devices, and connectors.

There are two types of system reset: power-on reset and switch reset.

Figure 2.8.1 shows the reset control block diagram.

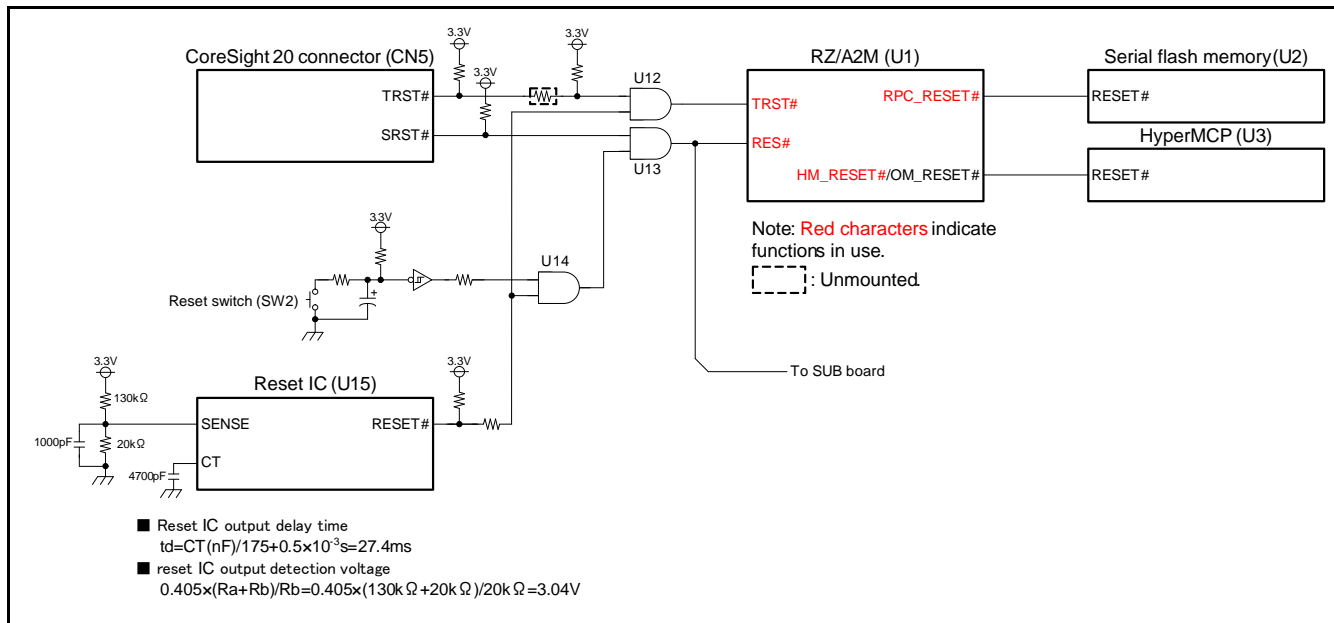


Figure 2.8.1 Reset Control Block Diagram

2.9 Power Supply Configuration

The regulators in RTK7921053C00000BE generate voltages 3.3 V, 1.8 V, and 1.2 V from 5 V.

Figure 2.9.1 shows the power supply configuration block diagram.

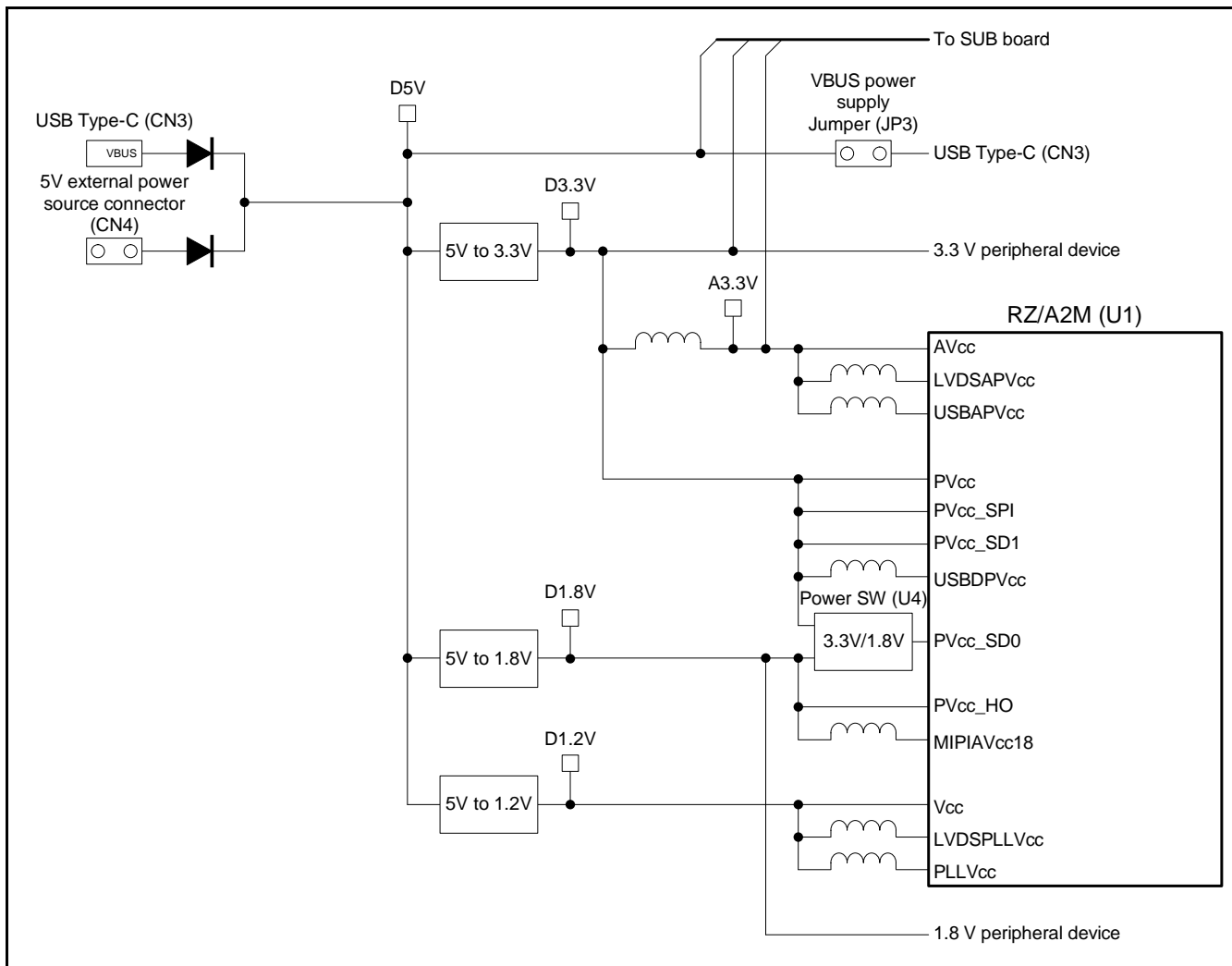


Figure 2.9.1 Power Supply Configuration Block Diagram

2.10 Debug Interface

RTK7921053C00000BE contains a CoreSight 20 connector (CN5) for connection to the RZ/A2M user debug interface. Figure 2.10.1 shows the debug interface block diagram.

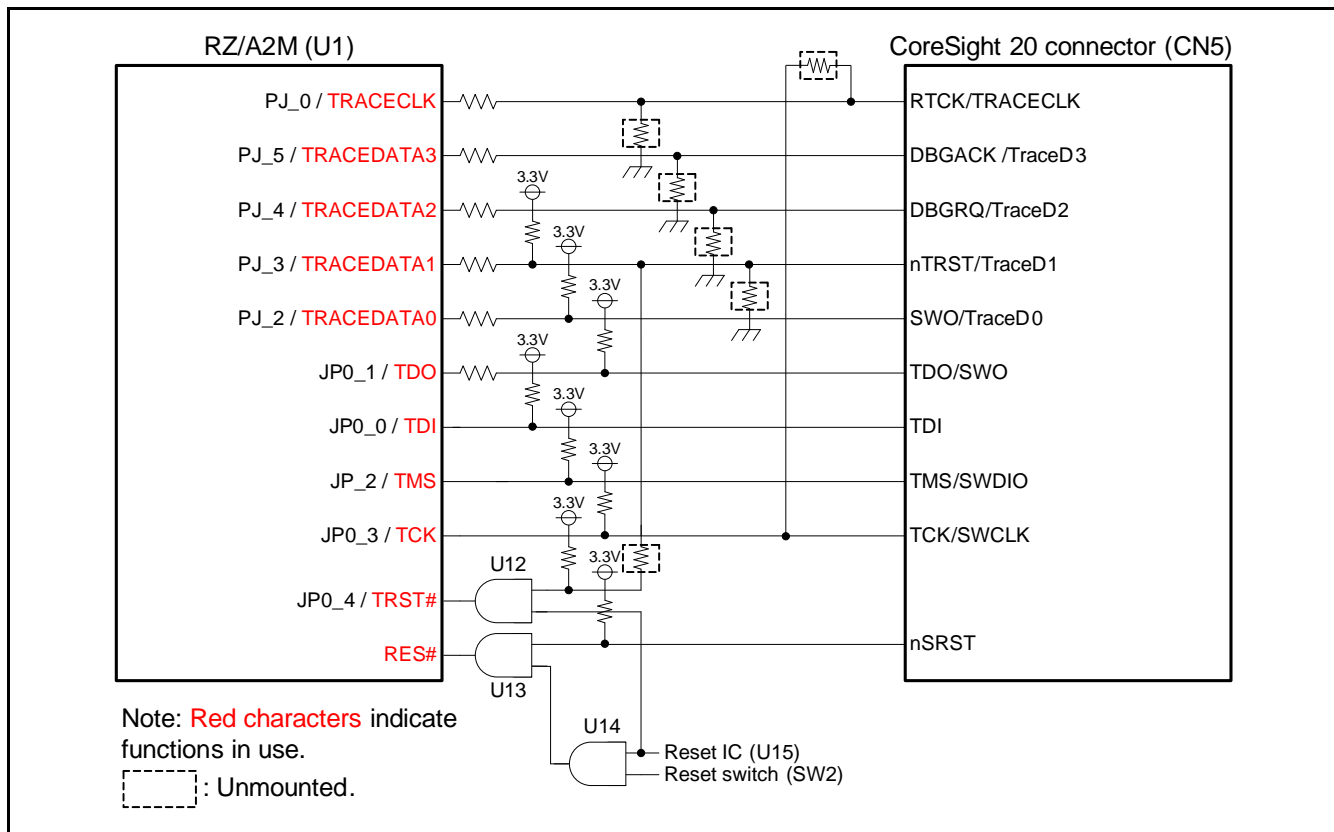


Figure 2.10.1 Debug Interface Block Diagram

2.11 SD/MMC Host Interface (4 bits)

RTK7921053C00000BE contains a 4 bit microSD slot connected to the SD/MMC host interface in the RZ/A2M.

SD/MMC host interface ch0 terminal operational voltage can be changed via the PD_1 terminal. Set PD_1 to High for 3.3V operation and to Low for 1.8V operation.

Figure 2.11.1 shows the SD/MMC host interface block diagram. Table 2.11.1 shows the PVcc_SD0 voltage switching table.

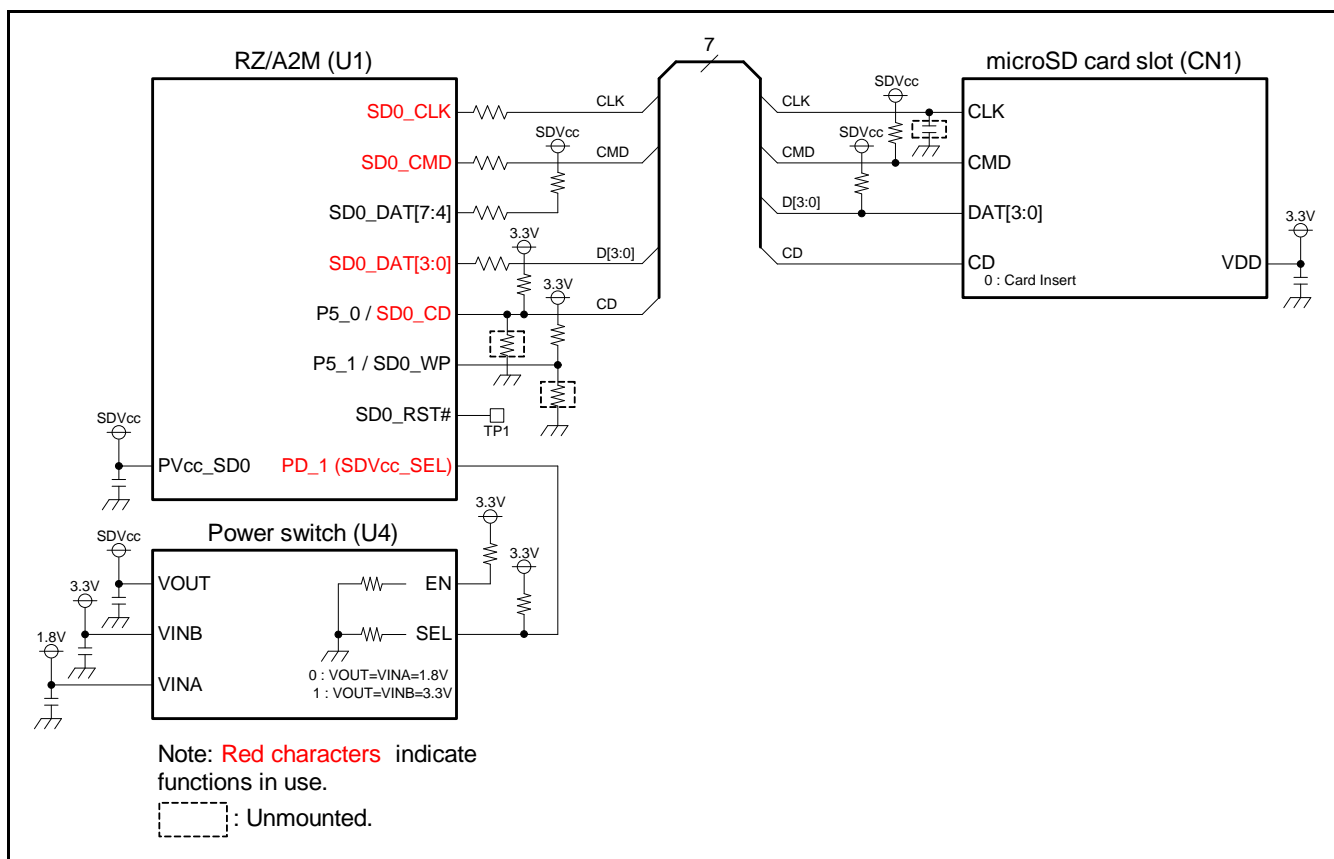


Figure 2.11.1 SD/MMC Host Interface Block Diagram

Table 2.11.1 PVcc_SD0 Voltage Switching Table

Terminal	function	
	High	Low
PD_1	Supplies 3.3V to PVcc_SD0. (Initial setting)	Supplies 1.8V to PVcc_SD0.

3. Operation Specifications

3.1 Overview of Connectors

Figure 3.1.1 illustrates the layout of connectors of RTK7921053C00000BE.

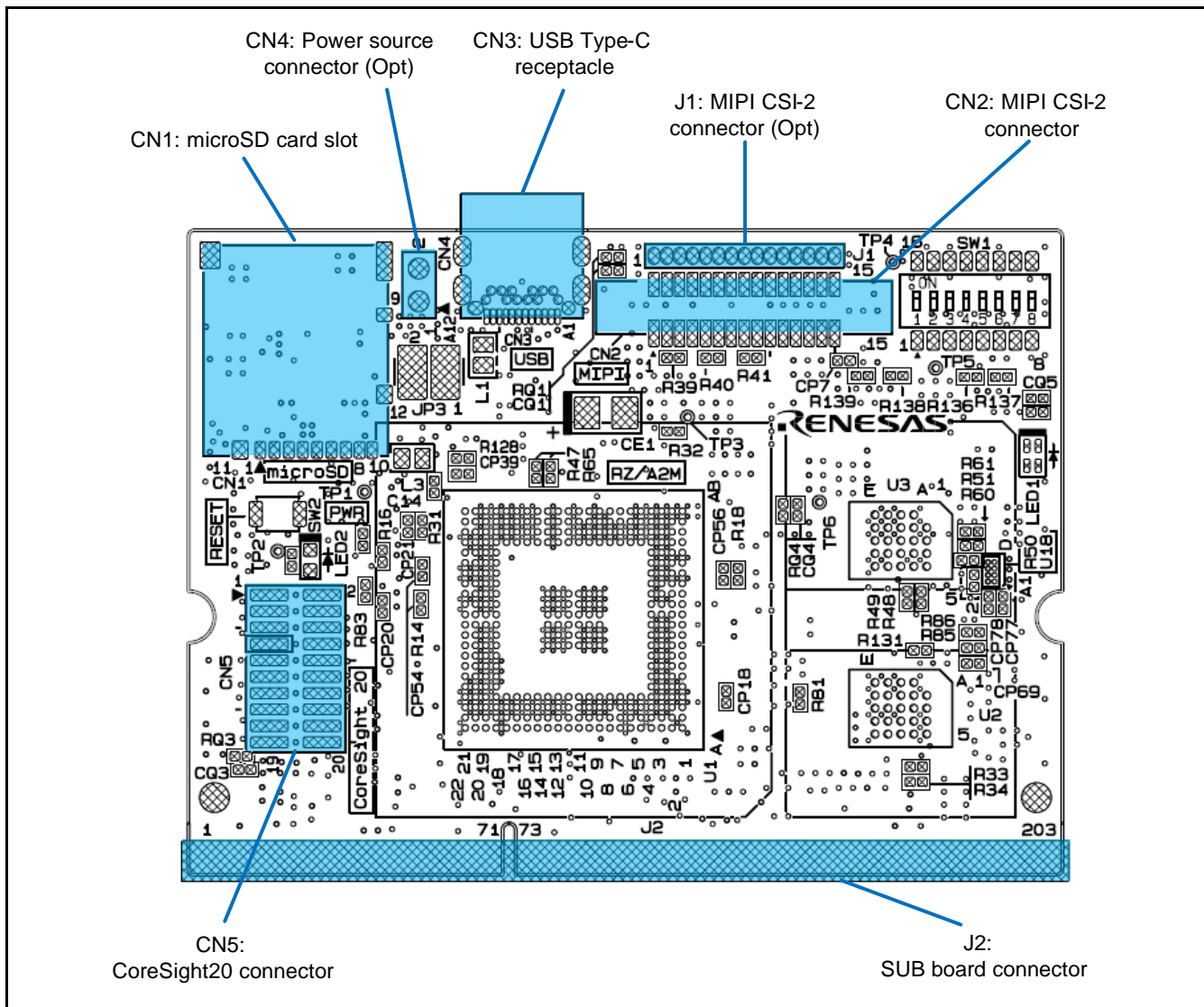


Figure 3.1.1 Layout of Connectors of RTK7921053C00000BE (C Side Top View)

3.1.1 microSD Card Slot (CN1)

RTK7921053C00000BE contains a microSD card slot (CN1).

Figure 3.1.2 illustrates the layout of microSD card slot pins. Table 3.1.1 shows the assignment of microSD card slot pins.

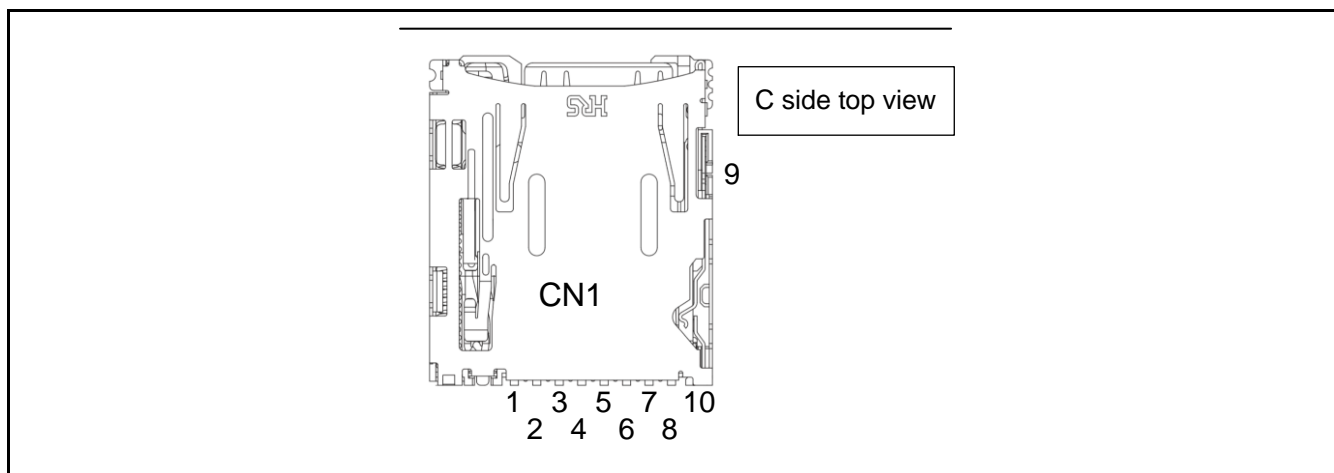


Figure 3.1.2 Layout of microSD Card Slot Pins

Table 3.1.1 Assignment of microSD Card Slot (CN1) Pins

Pin	Signal Name
1	DAT2 (SD0_DAT2)
2	CD/DAT3 (SD0_DAT3)
3	CMD (SD0_CMD)
4	+3.3V
5	CLK (SD0_CLK)
6	VSS (Vss)
7	DAT0 (SD0_DAT0)
8	DAT1 (SD0_DAT1)
9	COMMON (Vss)
10	Card_Detect (SD0_CD)

[Note] Red characters indicate functions in use.

3.1.2 MIPI CSI-2 Connector (CN2, J1)

RTK7921053C00000BE contains an MIPI CSI-2 connector (CN2). Moreover, this pattern allows to mount a connector (J1).

Pins 30 to 16 of the connector (CN2) are connected to pins 1 to 15 of the connector (J1). Pins 1 to 15 of the connector (J1) are connected to pins 30 to 16 of the connector (CN2).

When using a device that cannot be connected to the connector (CN2), it is possible to create a conversion connector via the connector (J1) to connect the device to the connector (CN2).

Figure 3.1.3 illustrates the layout of MIPI CSI-2 connector pins. Table 3.1.2 and Table 3.1.3 show the assignment of MIPI CSI-2 connector pins.

If connector (J1) is used, be careful for keeping the direction of the number 1 pin.

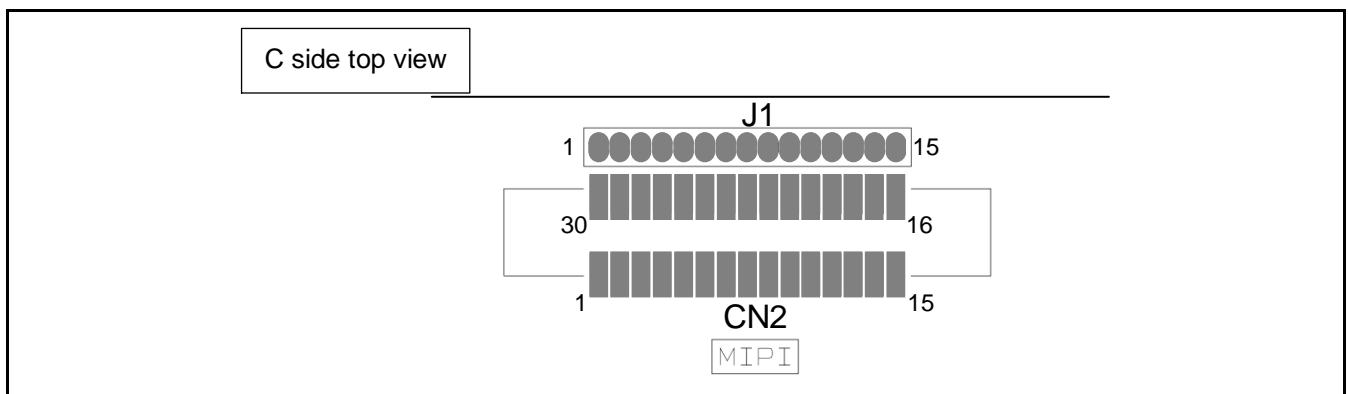


Figure 3.1.3 Layout of MIPI CSI-2 Connector Pins

Table 3.1.2 Assignment of MIPI CSI-2 Connector Pins (CN2)

Pin	Signal name
1, 30	GND (Vss)
2, 29	CAM1_DN0 (CSI_DATA0N)
3, 28	CAM1_DP0 (CSI_DATA0P)
4, 27	GND (Vss)
5, 26	CAM1_DN1 (CSI_DATA1N)
6, 25	CAM1_DP1 (CSI_DATA1P)
7, 24	GND (Vss)
8, 23	CAM1_CN (CSI_CLKN)
9, 22	CAM1_CP (CSI_CLKP)
10, 21	GND (Vss)
11, 20	CAM_GPIO0 (PD_2)
12, 19	CAM_GPIO1 (PD_3)
13, 18	SCL0 (PD_4 / RIIC2SCL)
14, 17	SDA0 (PD_5 / RIIC2SDA)
15, 16	+3.3V

[Note] Red characters indicate functions in use.

Table 3.1.3 Assignment of MIPI CSI-2 Connector Pins (J1)

Pin	Signal name	note
1	Vss	Connected to pin 30 of CN2
2	CSI_DATA0N	Connected to pin 29 of CN2
3	CSI_DATA0P	Connected to pin 28 of CN2
4	Vss	Connected to pin 27 of CN2
5	CSI_DATA1N	Connected to pin 26 of CN2
6	CSI_DATA1P	Connected to pin 25 of CN2
7	Vss	Connected to pin 24 of CN2
8	CSI_CLKN	Connected to pin 23 of CN2
9	CSI_CLKP	Connected to pin 22 of CN2
10	Vss	Connected to pin 21 of CN2
11	PD_2	Connected to pin 20 of CN2
12	PD_3	Connected to pin 19 of CN2
13	PD_4 / RIIC2SCL	Connected to pin 18 of CN2
14	PD_5 / RIIC2SDA	Connected to pin 17 of CN2
15	+3.3V	Connected to pin 16 of CN2

[Note] Red characters indicate functions in use.

3.1.3 USB Connector (CN3)

RTK7921053C00000BE contains a USB Type-C receptacle (CN3).

Figure 3.1.4 illustrates the layout of USB Type-C receptacle pins. Table 3.1.4 shows the assignment of USB Type-C receptacle pins.

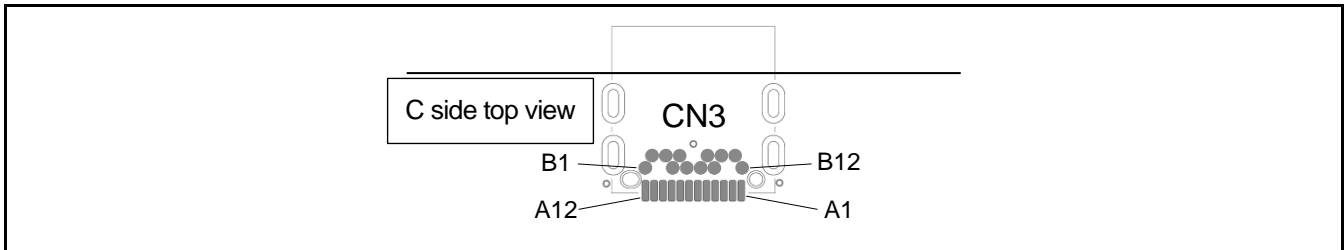


Figure 3.1.4 Layout of USB Type-C Receptacle Pins

Table 3.1.4 Assignment of USB Type-C Receptacle (CN3) Pins

Pin	Signal Name	Pin	Signal Name
A1	GND (Vss)	B12	GND (Vss)
A2	TX1+(NC)	B11	RX1+(NC)
A3	TX1-(NC)	B10	RX1-(NC)
A4	VBUS (P5_2 / VBUSIN0)	B9	VBUS (P5_2 / VBUSIN0)
A5	CC1 (CC1)	B8	SBU2 (NC)
A6	D+ (DP0)	B7	D- (DM0)
A7	D- (DM0)	B6	D+ (DP0)
A8	SBU1 (NC)	B5	CC2 (CC2)
A9	VBUS (P5_2 / VBUSIN0)	B4	VBUS (P5_2 / VBUSIN0)
A10	RX2-(NC)	B3	TX2-(NC)
A11	RX2+(NC)	B2	TX2+(NC)
A12	GND (Vss)	B1	GND (Vss)

[Note] Red characters indicate functions in use.

3.1.4 Power Source Connector (CN4)

RTK7921053C00000BE allows to mount the power source connector (CN4).

Figure 3.1.5 shows the layout of power source connector pins. Table 3.1.5 shows the assignment of power source connector pins.

If connector (CN4) is used, be careful for keeping the direction of number 1 pin.

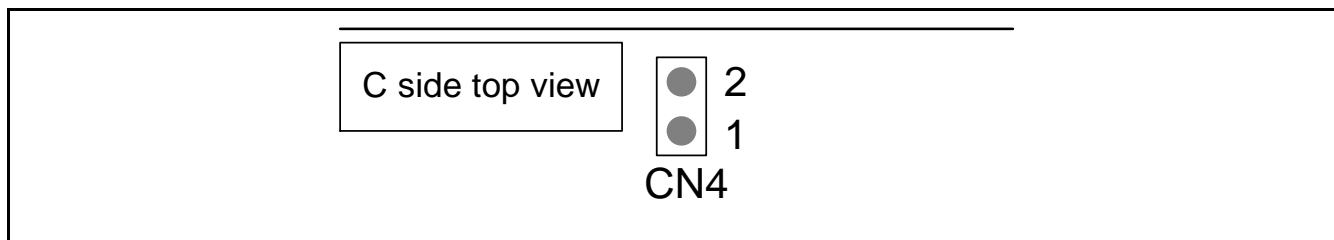


Figure 3.1.5 Layout of Power Source Connector Pins

Table 3.1.5 Assignment of Power Source Connector (CN4) Pins

Pin	Signal Name
1	+5V
2	GND (Vss)

3.1.5 UDI Connector (CN5)

RTK7921053C00000BE contains a 1.27 mm pitch CoreSight20 connector (CN5).

Figure 3.1.6 illustrates the layout of UDI connector pins. Table 3.1.6 shows the assignment of UDI connector pins.

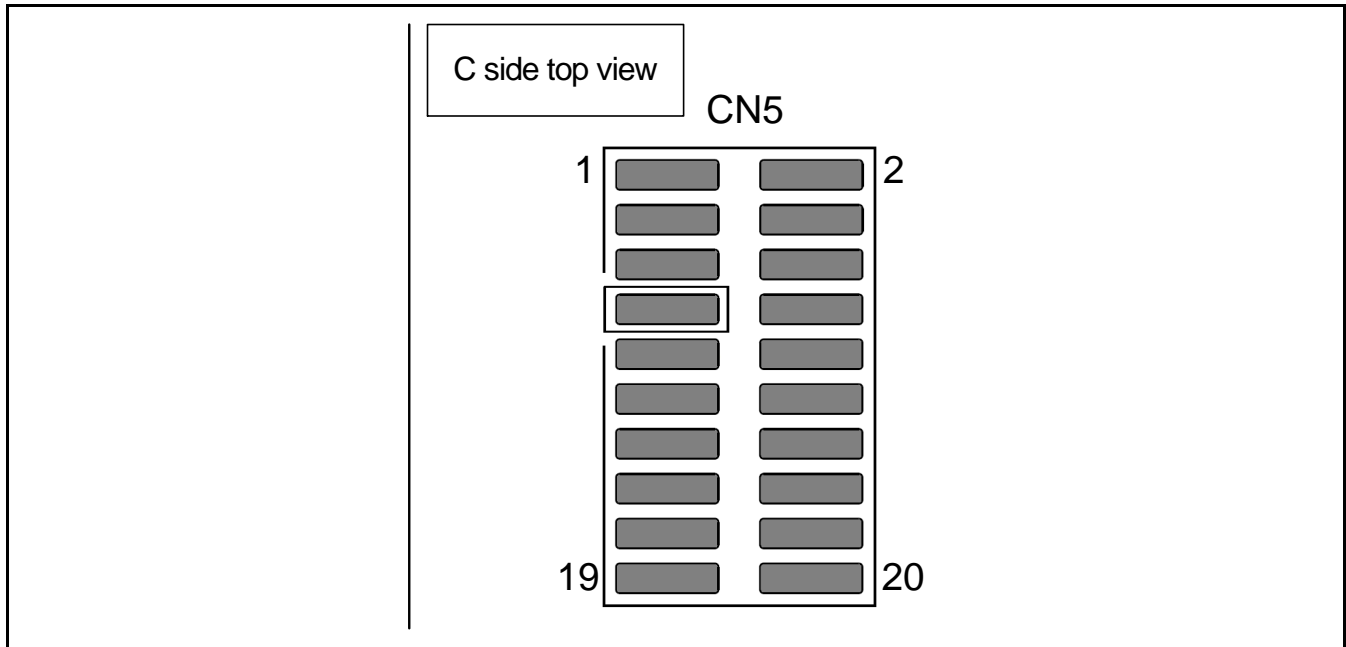


Figure 3.1.6 Layout of UDI Connector Pins

Table 3.1.6 Assignment of CoreSight 20 Connector (CN5) Pins

Pin	Signal name	Pin	Signal name
1	+3.3V	2	TMS/SWDIO (JP_2 / TMS)
3	GND (Vss)	4	TCK/SWCLK (JP0_3 / TCK)
5	GND (Vss)	6	TDO/SWO (JP0_1 / TDO)
7	KEY (NC)	8	TDI (JP0_0 / TDI)
9	GND (Vss)	10	nSRST
11	NC	12	RTCK/TraceCLK (PJ_0 / TRACECLK)
13	NC	14	SWO/TraceD0 (PJ_2 / TRACEDATA0)
15	GND (Vss)	16	nTRST/TraceD1 (PJ_3 / TRACEDATA1)
17	GND (Vss)	18	DBGRRQ/TraceD2 (PJ_4 / TRACEDATA2)
19	GND (Vss)	20	DBGACK/TraceD3 (PJ_5 / TRACEDATA3)

[Note] Red characters indicate functions in use.

3.1.6 SUB Board Connector (J2)

RTK7921053C00000BE can be connected to an external expansion board through the SUB board connecting connector (J2).

Figure 3.1.7 illustrates the layout of SUB board connecting connector pins. Table 3.1.7 to Table 3.1.9 show the assignment of SUB board connecting connector pins.

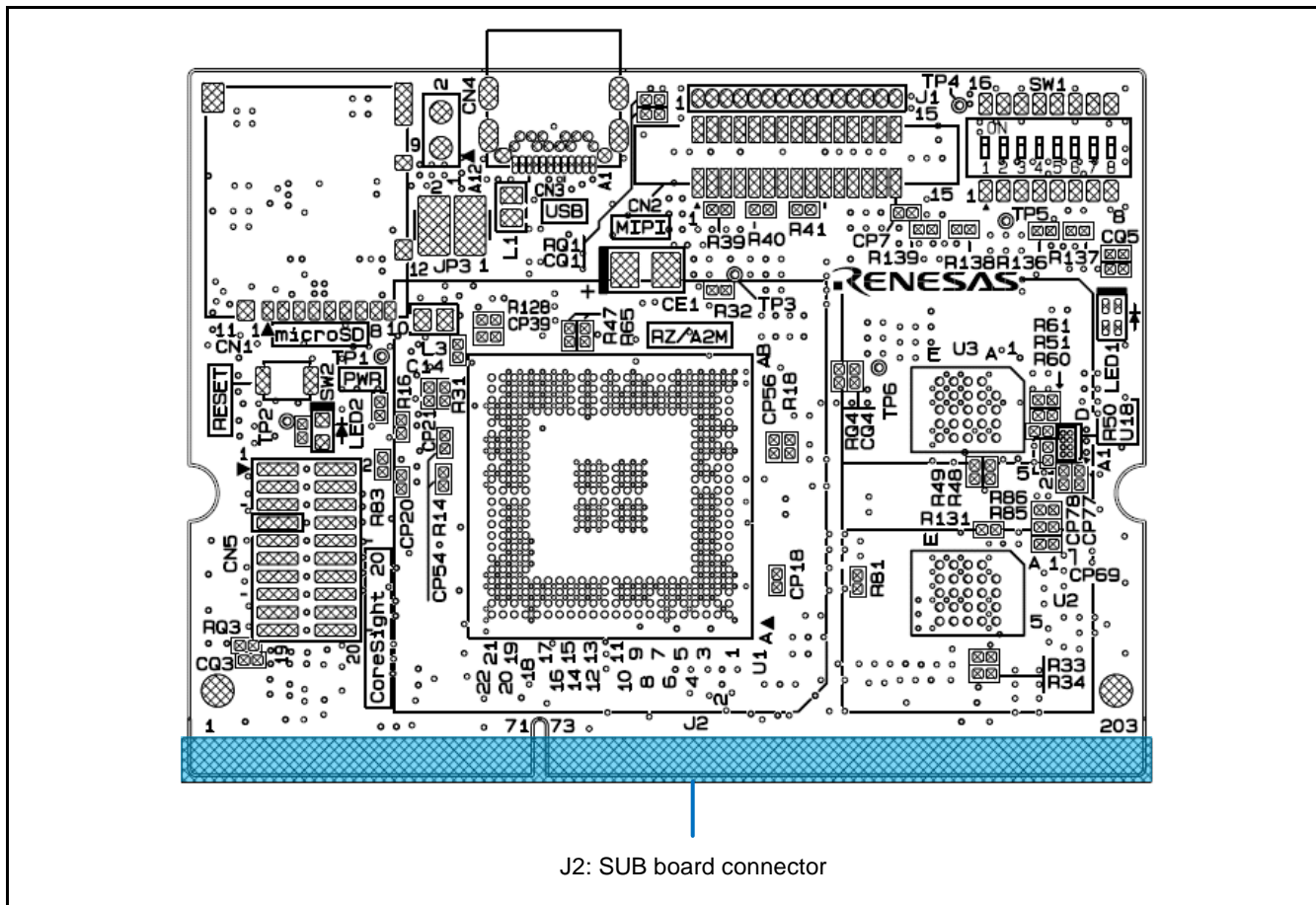


Figure 3.1.7 Layout of SUB Board Connecting Connector Pins

Table 3.1.7 Assignment of SUB Board Connecting Connector (J2) Pins (1)

Pin	Signal Name	Pin	Signal Name
1	D5V	2	D5V
3	D5V	4	D5V
5	D5V	6	D5V
7	RES#	8	PC_5 / VBUSEN1
9	D3.3V	10	PC_3 / LCD0_TCON4
11	D3.3V	12	AVcc
13	D3.3V	14	P5_6 / AN006
15	P5_3	16	AVss
17	P5_5 / SD1_WP	18	P5_4 / SD1_CD
19	P5_7 / IRQ3	20	PC_4 / LCD0_TCON3
21	D3.3V	22	Vss
23	P6_7 / WE0/DQML / DRP03	24	SD1_CLK
25	P7_0 / WE1/DQMU / DRP04 / SCK1	26	Vss
27	D3.3V	28	SD1_CMD
29	SD1_DAT1	30	Vss
31	SD1_DAT2	32	SD1_DAT3
33	SD1_DAT0	34	Vss
35	Vss	36	P6_4 / DRP00 / AUDIO_CLK
37	P7_2 / DV0_CLK	38	Vss
39	Vss	40	PB_4 / DV0_DATA1 / LCD0_DATA22
41	P7_3 / RAS / DRP06 / TxD1	42	P9_3 / A11 / DRP13 / SSIRxD0
43	PG_2 / VIO_D10	44	P7_7 / DV0_HSYNC / LCD0_TCON0
45	P7_5 / CKE / DRP08 / CTS1 / OVRCUR1	46	Vss
47	Vss	48	PL_1 / MD_CLK / IRQ5
49	P9_6 / A14 / DRP10 / SSIBCK0	50	PL_0 / MD_CLKS / IRQ4
51	Vss	52	Vss
53	P7_6 / DV0_VSYNC / GTIOC3A	54	CKIO
55	P9_5 / A13 / DRP11 / SSIFS0	56	Vss
57	PB_5 / DV0_DATA0 / LCD0_DATA23	58	PD_7 / RIIC3SDA
59	P9_2 / A10 / DRP14	60	PD_6 / RIIC3SCL
61	PB_3 / DV0_DATA2 / LCD0_DATA21	62	Vss
63	PB_1 / DV0_DATA4 / LCD0_DATA19	64	PB_0 / DV0_DATA5 / LCD0_DATA18
65	Vss	66	PB_2 / DV0_DATA3 / LCD0_DATA20
67	PA_6 / DV0_DATA7 / LCD0_DATA16	68	PA_3 / DV0_DATA10 / LCD0_DATA13
69	PA_4 / DV0_DATA9 / LCD0_DATA14	70	Vss
71	PA_5 / DV0_DATA8 / LCD0_DATA15	72	PG_0 / VIO_D8

[Note] : 5V power source, : 3.3V power source, : GND

Table 3.1.8 Assignment of SUB Board Connecting Connector (J2) Pins (2)

Pin	Signal Name	Pin	Signal Name
73	PE_1 / ET0_RXD0/RMII0_RXD0 / VIO_D7	74	PA_2 / DV0_DATA11 / LCD0_DATA12
75	Vss	76	PA_7 / DV0_DATA6 / LCD0_DATA17
77	PA_0 / DV0_DATA13 / LCD0_DATA10	78	PE_2 / ET0_RXD1/RMII0_RXD1 / VIO_D6
79	PE_3 / ET0_RXER/RMII0_RXER / VIO_D5	80	PA_1 / DV0_DATA12 / LCD0_DATA11
81	Vss	82	Vss
83	P9_1 / A9 / DRP15 / RxD4	84	P9_0 / A8 / DRP16 / TxD4
85	Vss	86	P8_0 / DV0_DATA14 / LCD0_DATA9
87	P8_7 / A7 / DRP17 / RSPCK0	88	PF_1 / DV0_DATA16 / LCD0_DATA7
89	Vss	90	PF_0 / DV0_DATA15 / LCD0_DATA8
91	PE_4 / ET0_CRS/RMII0_CRSDV / VIO_D4	92	P8_5 / A5 / DRP19 / MISO0
93	PF_2 / DV0_DATA17 / LCD0_DATA6	94	Vss
95	P8_6 / A6 / DRP18 / MOSI0	96	DP1
97	P8_3 / A3 / DRP21	98	DM1
99	Vss	100	Vss
101	P8_4 / A4 / DRP20 / SSL00	102	PE_0 / ET0_RXCLK/REF50CK0 / VIO_FLD
103	PE_5 / ET0_MDC / VIO_D3	104	Vss
105	PH_0 / VIO_D1	106	P6_2 / ET0_TXD0/RMII0_TXD0 / VIO_VD
107	PE_6 / ET0_MDIO / VIO_D2	108	PF_6 / DV0_DATA21 / LCD0_DATA2
109	Vss	110	PK_0 / ET1_TXEN/RMII1_TXDEN / NAF3
111	P6_3 / ET0_TXD1/RMII0_TXD1 / VIO_HD	112	P9_4 / A12 / DRP12 / SSITxD0
113	PF_4 / DV0_DATA19 / LCD0_DATA4	114	Vss
115	PF_5 / DV0_DATA20 / LCD0_DATA3	116	PG_1 / VIO_D9
117	Vss	118	P9_7 / A15 / DRP09
119	P6_1 / ET0_TXEN/RMII0_TXDEN / VIO_CLK	120	P7_4 / CAS / DRP07 / RTS1
121	Vss	122	Vss
123	P7_1 / RD/WR / DRP05 / RxD1	124	PF_3 / DV0_DATA18 / LCD0_DATA5
125	P6_0	126	PH_1 / VIO_D0
127	P6_6 / DRP02	128	P8_1 / A1 / DRP23
129	PG_3 / VIO_D11	130	Vss
131	Vss	132	PK_3 / ET1_RXCLK/REF50CK1 / NAF6
133	PK_2 / ET1_TXD1/RMII1_TXD1 / NAF5	134	Vss
135	P6_5 / CS3 / DRP01	136	PF_7 / DV0_DATA23 / LCD0_DATA0
137	PK_1 / ET1_TXD0/RMII1_TXD0 / NAF4	138	Vss
139	Vss	140	PJ_7 / NAF0 / LCD0_EXTCLK
141	P8_2 / A2 / DRP22	142	Vss
143	PH_2 / DV0_DATA22 / LCD0_DATA1	144	P0_0 / D0 / DRP24
145	Vss	146	P0_4 / D4 / DRP28
147	PJ_6 / FCE / LCD0_CLK	148	P0_3 / D3 / DRP27
149	Vss	150	P0_6 / D6 / DRP30
151	P0_1 / D1 / DRP25	152	Vss
153	P0_5 / D5 / DRP29	154	P3_2 / ET1_CRS/RMII1_CRSDV / FRE
155	P0_2 / D2 / DRP26	156	P3_5 / ET1_RXD1/RMII1_RXD1 / FCLE

[Note]  : 5V power source,  : 3.3V power source,  : GND

Table 3.1.9 Assignment of SUB Board Connecting Connector (J2) Pins (3)

Pin	Signal Name	Pin	Signal Name
157	Vss	158	Vss
159	PJ_1 / IRQ0	160	P1_0 / D7 / DRP31
161	PH_5 / NAF2 / ET1_EXOUT	162	Vss
163	PH_6 / ET1_WOL	164	PK_4 / ET1_RXD0/RMII1_RXD0 / NAF7
165	Vss	166	P3_1 / ET1_RXER/RMII1_RXER / FALE
167	PK_5 / NAF1	168	Vss
169	PG_4 / VIO_D15	170	P4_0 / TXOUT0P
171	PG_6 / VIO_D13	172	P4_1 / TXOUT0M
173	P1_4 / D11	174	Vss
175	Vss	176	P4_4 / TXOUT2P
177	P3_3 / ET1_MDC / FWE	178	P4_5 / TXOUT2M
179	P1_1 / D8	180	Vss
181	PG_7 / VIO_D12	182	P4_2 / TXOUT1P
183	PG_5 / VIO_D14	184	P4_3 / TXOUT1M
185	Vss	186	Vss
187	P3_4 / ET1_MDIO / FRB	188	P4_6 / TXCLKOUTP
189	P1_3 / D10	190	P4_7 / TXCLKOUTM
191	P3_0 / ET1_LINKSTA	192	Vss
193	P2_1 / D13	194	PC_0 / VBUSIN1
195	Vss	196	P1_2 / D9
197	PC_1	198	P2_2 / D14
199	P2_3 / D15	200	P2_0 / D12
201	Vss	202	PC_2
203	NMI	204	Vss

[Note] : 5V power source, : 3.3V power source, : GND

3.2 Layout of Operation Components

Figure 3.2.1 illustrates the layout of operation components of RTK7921053C00000BE.

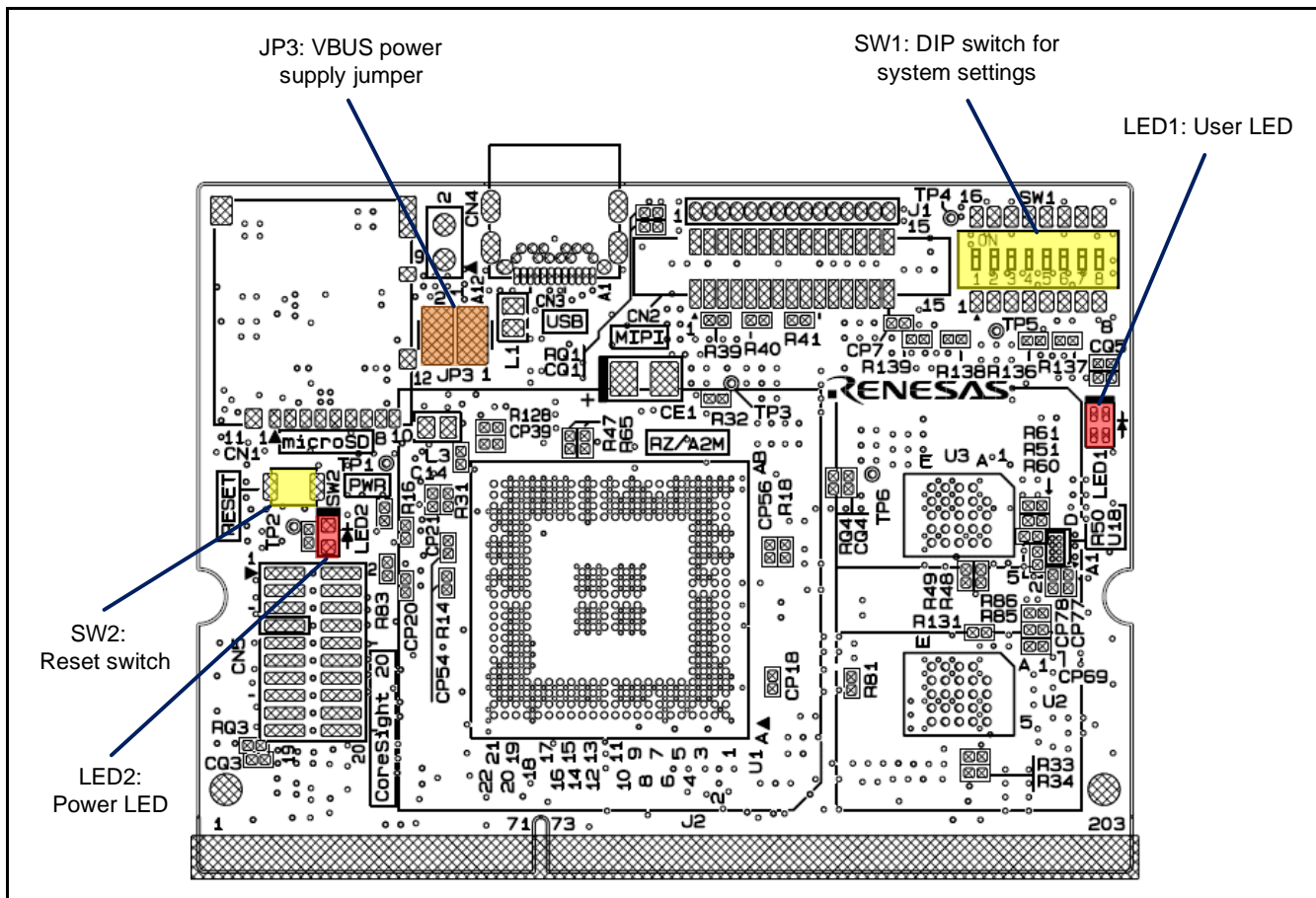


Figure 3.2.1 Layout of Operation Components of RTK7921053C00000BE

3.2.1 Jumper (JP1)

RTK7921053C00000BE contains one system setting jumper.

Figure 3.2.2 illustrates the layout of jumper. Table 3.2.1 lists jumper setting.

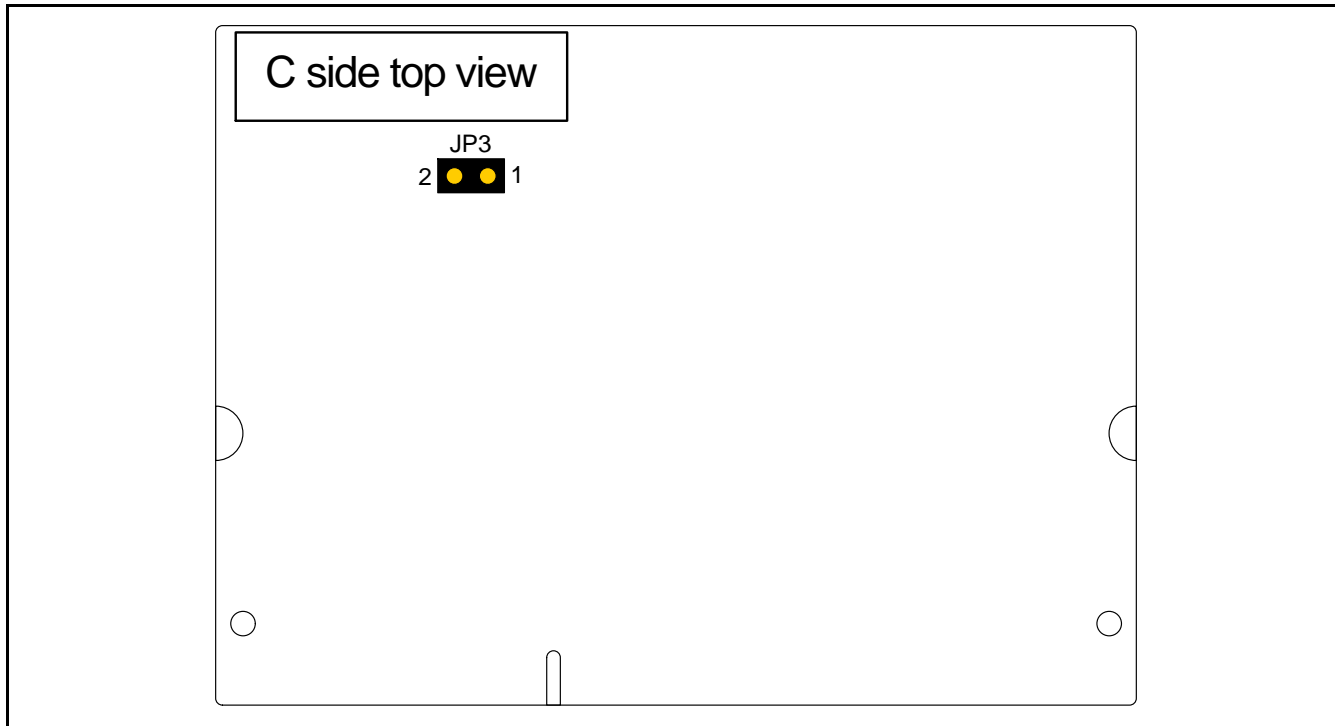


Figure 3.2.2 Layout of Jumper of RTK7921053C00000BE

Table 3.2.1 Setting for VBUS Power Supply Jumper (JP3)

Jumper	Setting	Function
JP3 For USB ch0	Short	Uses USB ch0 as host mode (with VBUS voltage supplied).
	Open	Uses USB ch0 as function mode (with no VBUS voltage supplied).

[Note] : Initial setting.

Before changing jumper settings, be sure to turn off the board.

3.2.2 Functions of Switches and LEDs

RTK7921053C00000BE contains two switches and two LEDs.

Figure 3.2.3 illustrates the layout of switches and LEDs. Table 3.2.2 lists mounted switches. Table 3.2.3 provides functions of the DIP switch. Table 3.2.4 lists mounted LEDs.

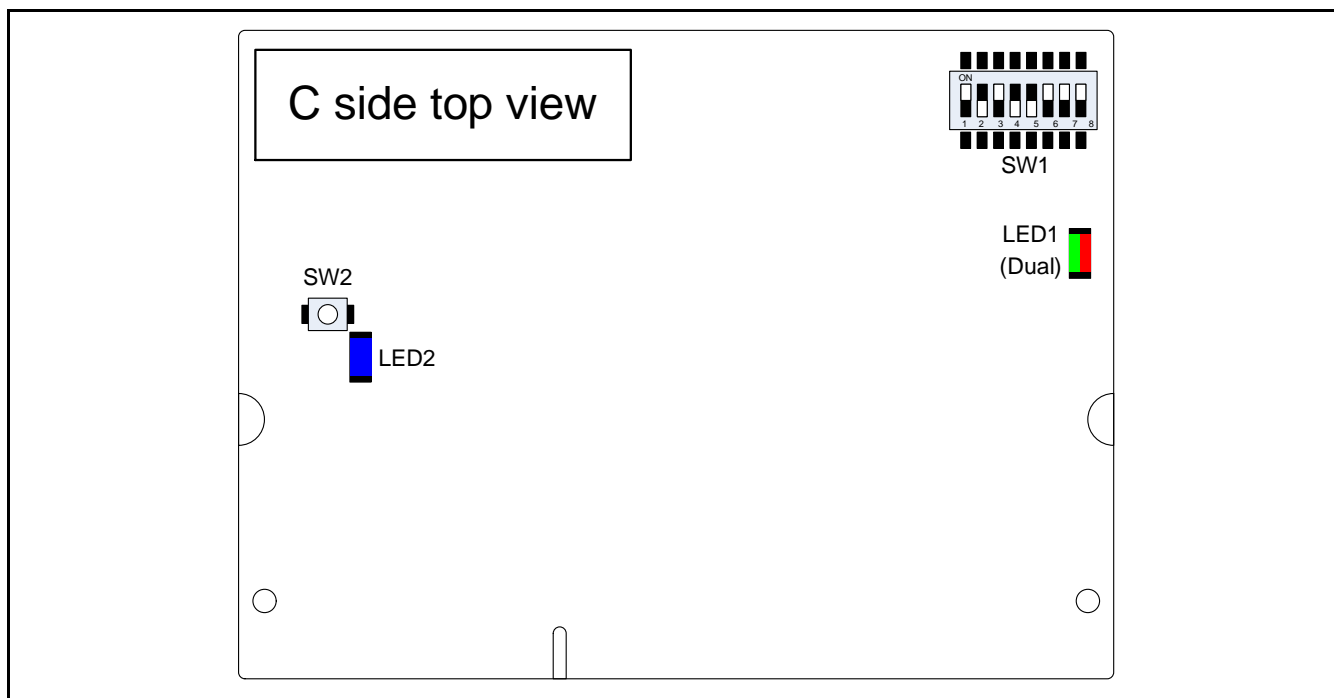


Figure 3.2.3 Layout of Switches and LEDs Mounted on RTK7921053C00000BE

Table 3.2.2 Switches Mounted on RTK7921053C00000BE

No.	Function	Note
SW1	System setting DIP switch	For details, see Table 3.2.3.
SW2	Reset switch	For details, see section 2.8.

Table 3.2.3 Functions of System Setting DIP Switch (SW1)

No.	Setting		Function																		
SW1-1 MD_CLKS	OFF	MD_CLKS="H"	Activates SSCG.																		
	ON	MD_CLKS="L"	Deactivates SSCG.																		
SW1-2 MD_CLK	OFF	MD_CLK="H"	Sets the EXTAL input frequency to 20 to 24 MHz.																		
	ON	MD_CLK="L"	Sets the EXTAL input frequency to 10 to 12 MHz (Setting prohibited).																		
SW1-3 MD_BOOT2	OFF	MD_BOOT2="H"	<table border="1"> <thead> <tr> <th>Boot Mode MD_BOOT[2:0]</th> <th>Boot Device</th> </tr> </thead> <tbody> <tr> <td>0 (B'000)</td> <td>Memory connected to the CS0 space (Bus width: 16 bits) (Setting prohibited)</td> </tr> <tr> <td>1 (B'001)</td> <td>eSD</td> </tr> <tr> <td>2 (B'010)</td> <td>eMMC (Setting prohibited)</td> </tr> <tr> <td>3 (B'011)</td> <td>Serial flash memory connected to the SPIBSC space (3.3V)</td> </tr> <tr> <td>4 (B'100)</td> <td>OctaFlash connected to the SPIBSC space (1.8V)</td> </tr> <tr> <td>5 (B'101)</td> <td>HyperFlash connected to the SPIBSC space (1.8V)</td> </tr> <tr> <td>6 (B'110)</td> <td>OctaFlash connected to the OctaFlash space (1.8V)</td> </tr> <tr> <td>7 (B'111)</td> <td>HyperFlash connected to the HyperFlash space (1.8V)</td> </tr> </tbody> </table>	Boot Mode MD_BOOT[2:0]	Boot Device	0 (B'000)	Memory connected to the CS0 space (Bus width: 16 bits) (Setting prohibited)	1 (B'001)	eSD	2 (B'010)	eMMC (Setting prohibited)	3 (B'011)	Serial flash memory connected to the SPIBSC space (3.3V)	4 (B'100)	OctaFlash connected to the SPIBSC space (1.8V)	5 (B'101)	HyperFlash connected to the SPIBSC space (1.8V)	6 (B'110)	OctaFlash connected to the OctaFlash space (1.8V)	7 (B'111)	HyperFlash connected to the HyperFlash space (1.8V)
	Boot Mode MD_BOOT[2:0]	Boot Device																			
0 (B'000)	Memory connected to the CS0 space (Bus width: 16 bits) (Setting prohibited)																				
1 (B'001)	eSD																				
2 (B'010)	eMMC (Setting prohibited)																				
3 (B'011)	Serial flash memory connected to the SPIBSC space (3.3V)																				
4 (B'100)	OctaFlash connected to the SPIBSC space (1.8V)																				
5 (B'101)	HyperFlash connected to the SPIBSC space (1.8V)																				
6 (B'110)	OctaFlash connected to the OctaFlash space (1.8V)																				
7 (B'111)	HyperFlash connected to the HyperFlash space (1.8V)																				
ON	MD_BOOT2="L"																				
SW1-4 MD_BOOT1	OFF	MD_BOOT1="H"																			
	ON	MD_BOOT1="L"																			
SW1-5 MD_BOOT0	OFF	MD_BOOT0="H"																			
	ON	MD_BOOT0="L"																			
SW1-6 BSCANP	OFF	BSCANP="H"	Boundary scan mode																		
	ON	BSCANP="L"	Normal operation (CoreSight debug mode)																		
SW1-7 Vss1	OFF	Vss1="H"	3.3V applied (Setting prohibited)																		
	ON	Vss1="L"	GND connection																		
SW1-8 Vss2	OFF	Vss2="H"	3.3V applied (Setting prohibited)																		
	ON	Vss2="L"	GND connection																		

[Note] : Initial setting

Before changing DIP switch settings, be sure to turn off the board.

Table 3.2.4 LEDs Mounted on RTK7921053C00000BE

No.	Color	Function
LED1	Red	User LED (Lit while P6_0 output is "H")
	Green	User LED (Lit while PC_1 output is "H")
LED2	Blue	Power LED (Lit while 5V is supplied)

3.3 Dimensions

Figure 3.3.1 shows the dimensions of RTK7921053C00000BE (C side top view).

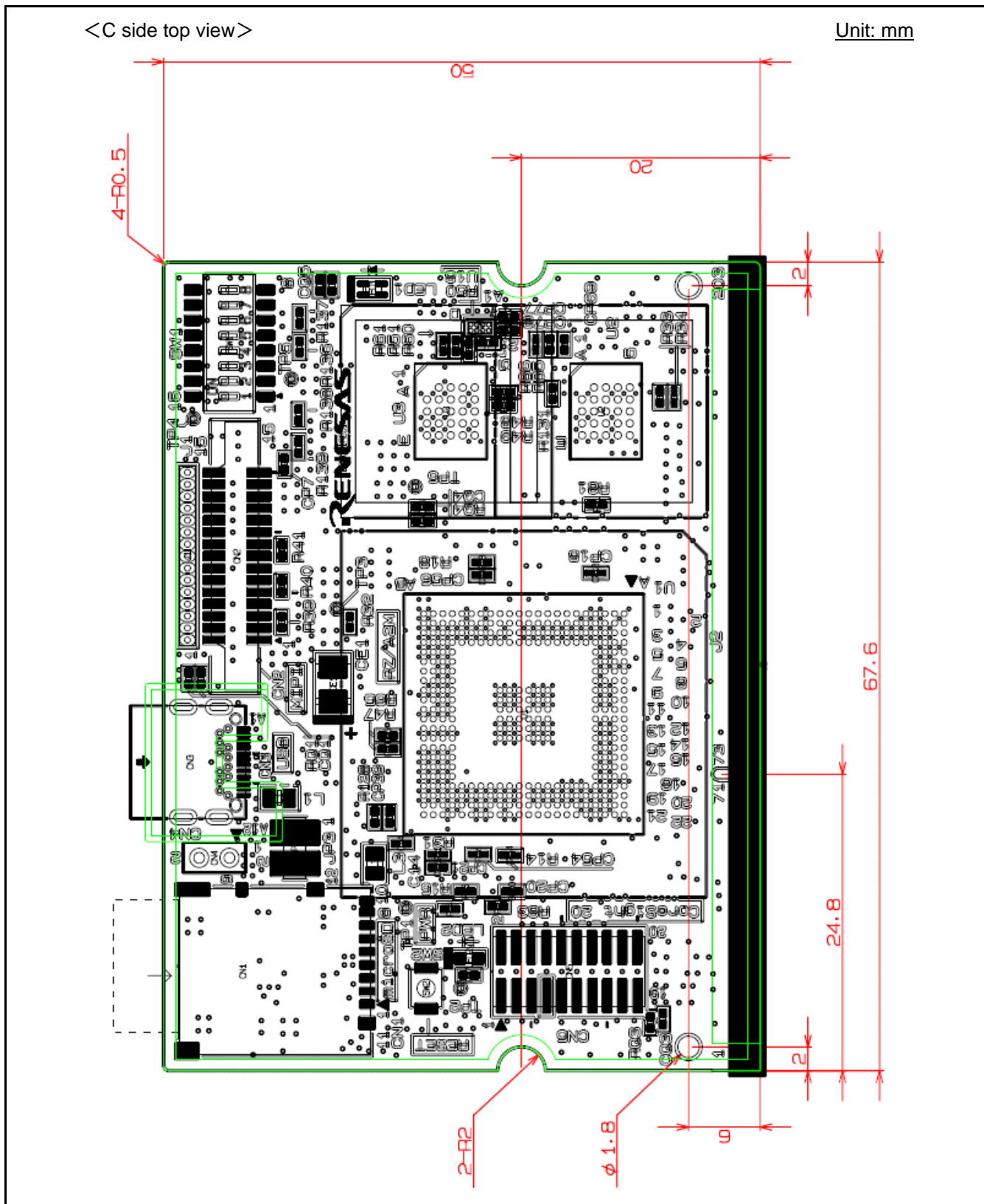



Figure 3.3.1 Dimensions of RTK7921053C00000BE (C Side Top View)

Appendix 1 RTK7921053C00000BE Connection Diagram

RZ/A2M CPU board RTK7921053C00000BE SCHEMATICS (BGA324)


TITLE	PAGE
Index	1
RZ/A2M(Dedicate), RAM, ROM, USB, MIPI, microSD, Clock, Dip-SW	2
RZ/A2M(Multi purpose, Power)	3
Mating	4
Power	5
POR, UDI	6

Note:

 Digital GND (GND)

 Analog GND (AVss)

 USB GND (UVss)

 Not mounted

D5V = Digital 5V (System Power)

D3.3V = Digital 3.3V

A3.3V = Analog 3.3V

PVcc = 3.3V for RZ/A2M I/O

Vcc = 1.2V for RZ/A2M Core

AVcc = Analog 3.3V for RZ/A2M

PLLVcc = Analog 1.2V for RZ/A2M PLL

USBAPVcc = Analog 3.3V for RZ/A2M USB

USBDPVcc = Digital 3.3V for RZ/A2M USB

LVDSAPVcc = Analog 3.3V for RZ/A2M LVDS

R = Fixed Resistors

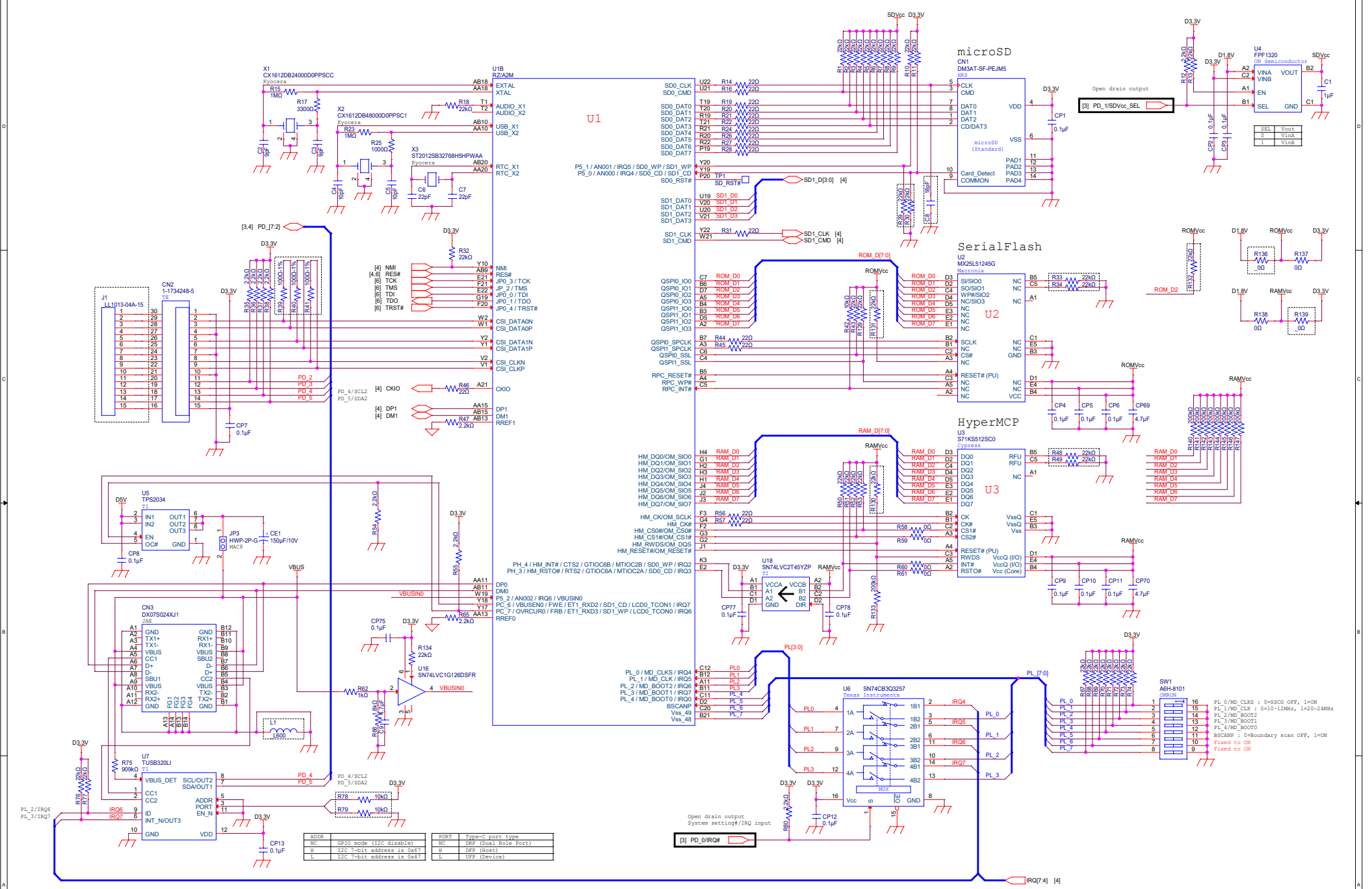
RA = Resistor Array

C = Ceramic Caps

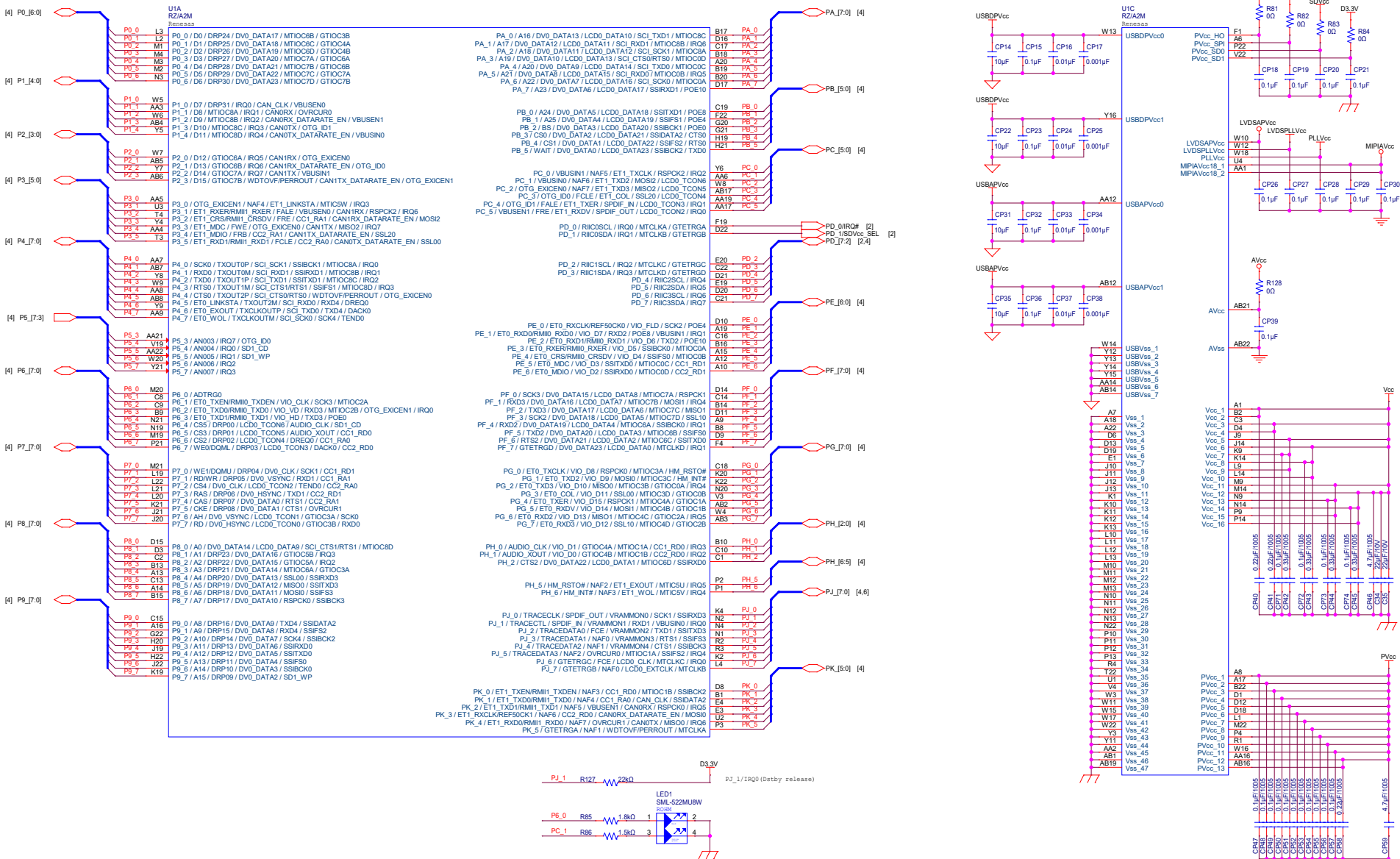
CE = Tantalum Electrolytic Caps

CP = Decoupling Caps

CHANGE			Renesas Electronics Corporation.				RZ/A2M CPU board
	SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	INDEX (1 / 6)
	DATE	19-09-10					R20UT4394EJ0400



CHANGE	Renesas Electronics Corporation.				RZ/A2M CPU board
	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED
	DATE	RZ/A2M(Dedicated)			
	19-09-10				R20UT4394EJ0400
					(2 / 6)



CHANGE

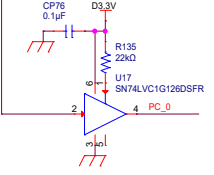
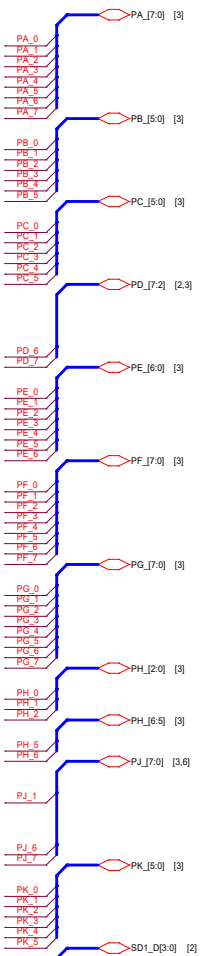
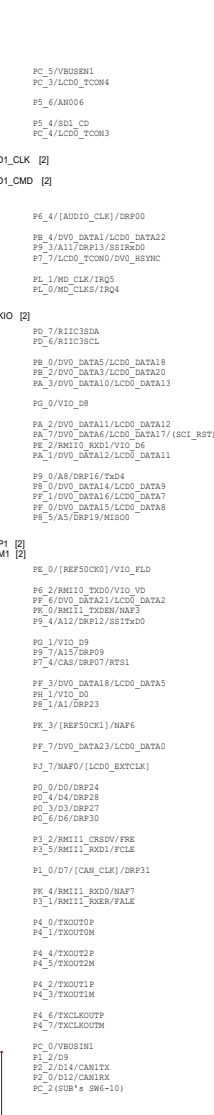
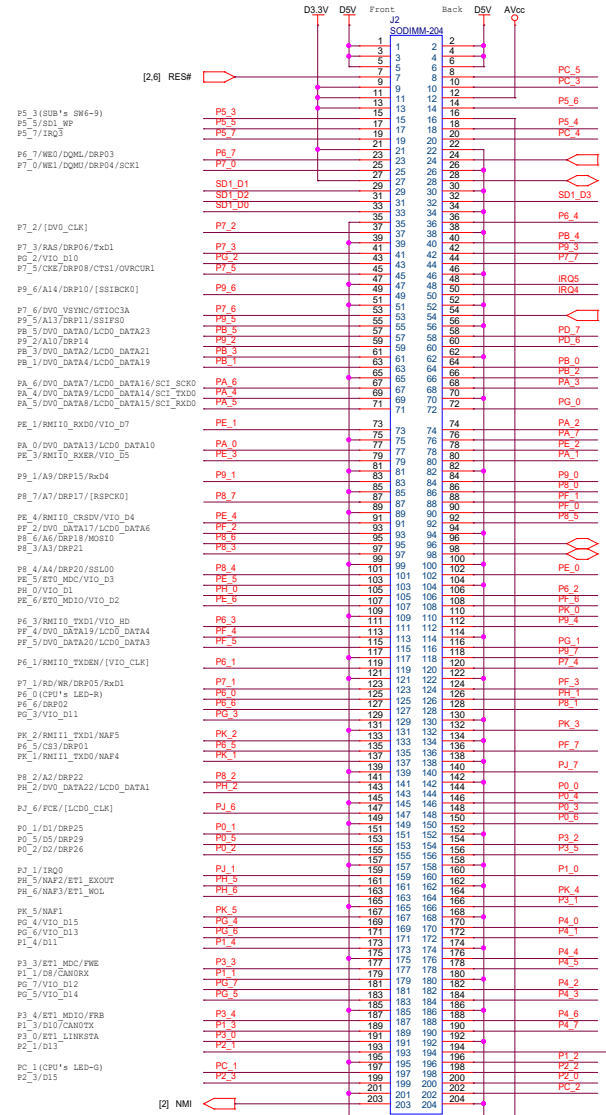
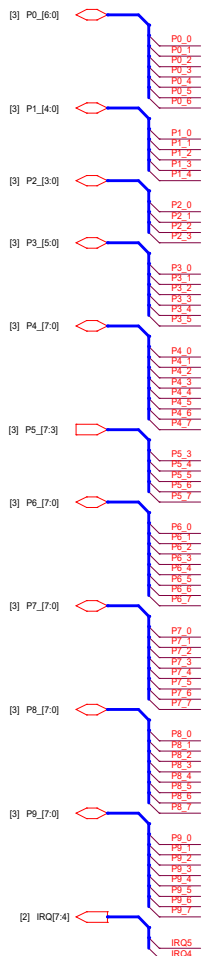
SCALE
DATE 19-09-10

Renesas Electronics Corporation.

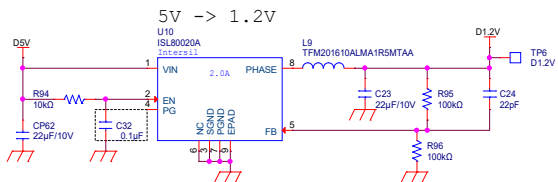
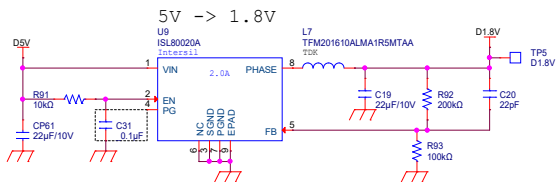
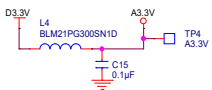
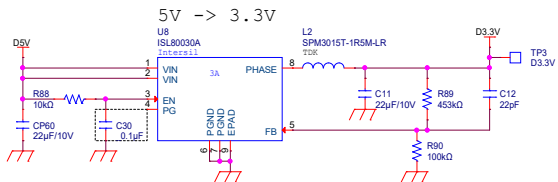
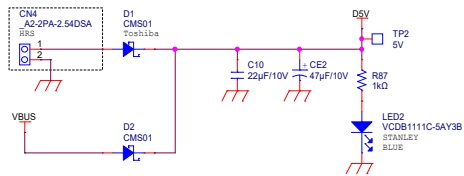
DRAWN CHECKED DESIGNED APPROVED

RZ/A2M CPU board
RZ/A2M(Multi purpose & Power)

R2OUT4394EJ0400



CHANGE	Renesas Electronics Corporation.				RZ/A2M CPU board	
	DRAWN				SODIMM Connector	
	CHECKED				DESIGNED	
	APPROVED				R20UT4394EJ0400	
SCALE						
DATE	19-09-10					(4 / 6)



/* PVcc=300mA */



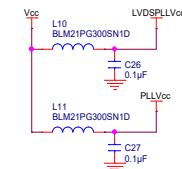
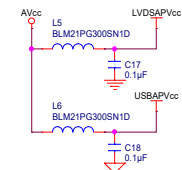
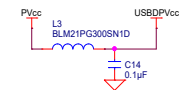
/* AVcc=44mA */



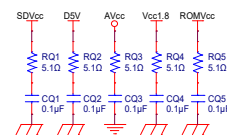
/* MIPIAVcc=6mA */



/* Vcc=1.6A */



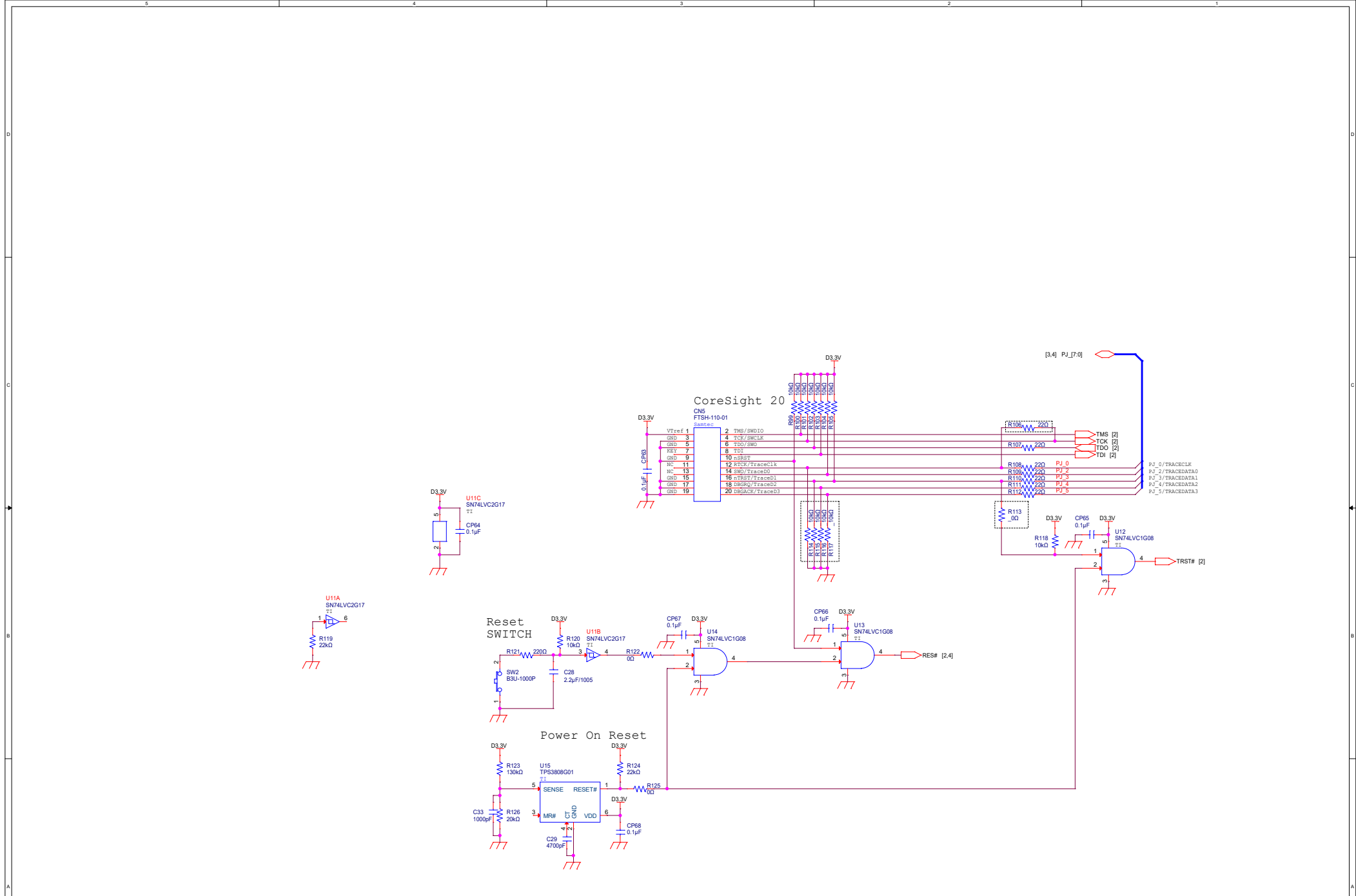
Anti-resonant circuit



GND Connection

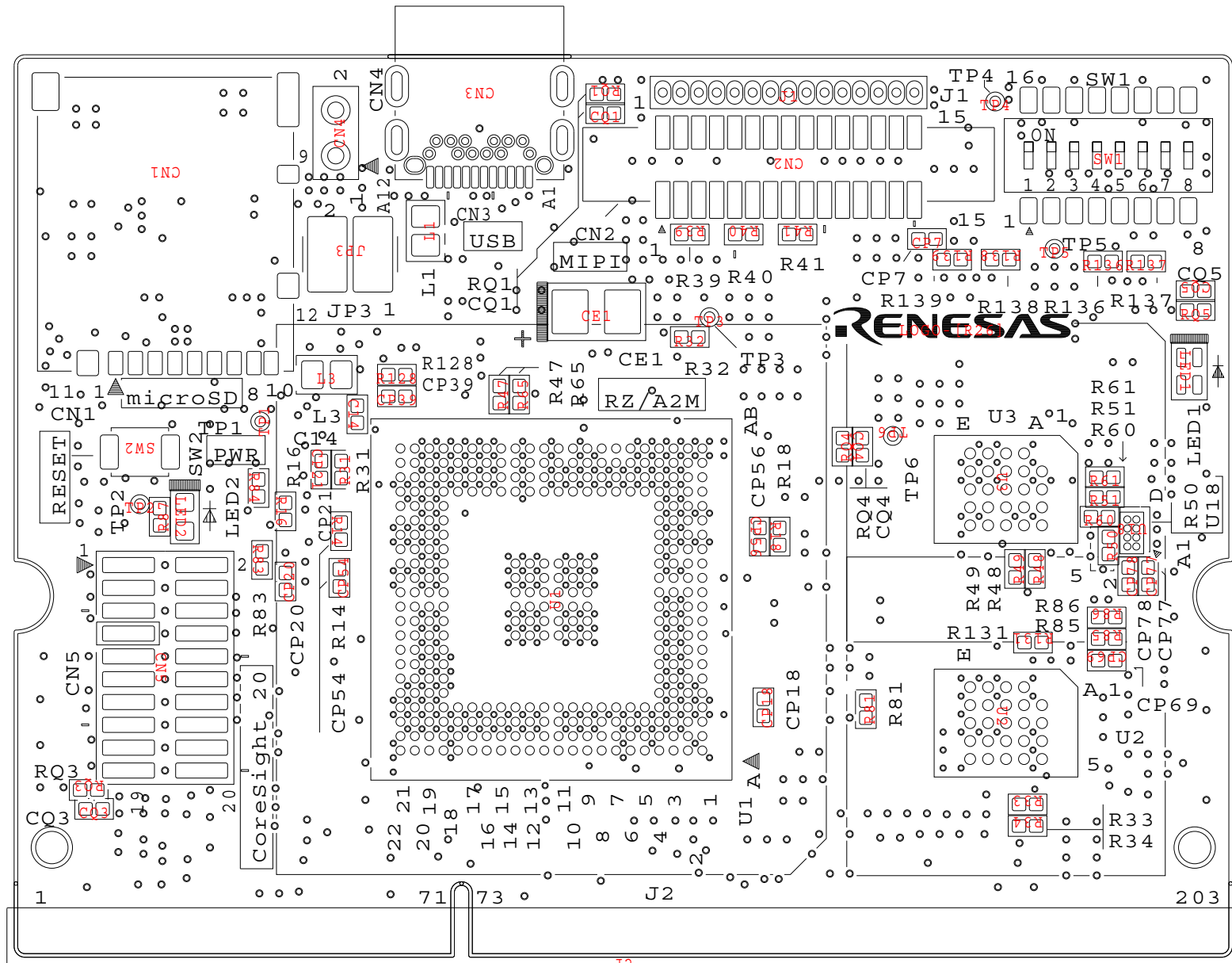


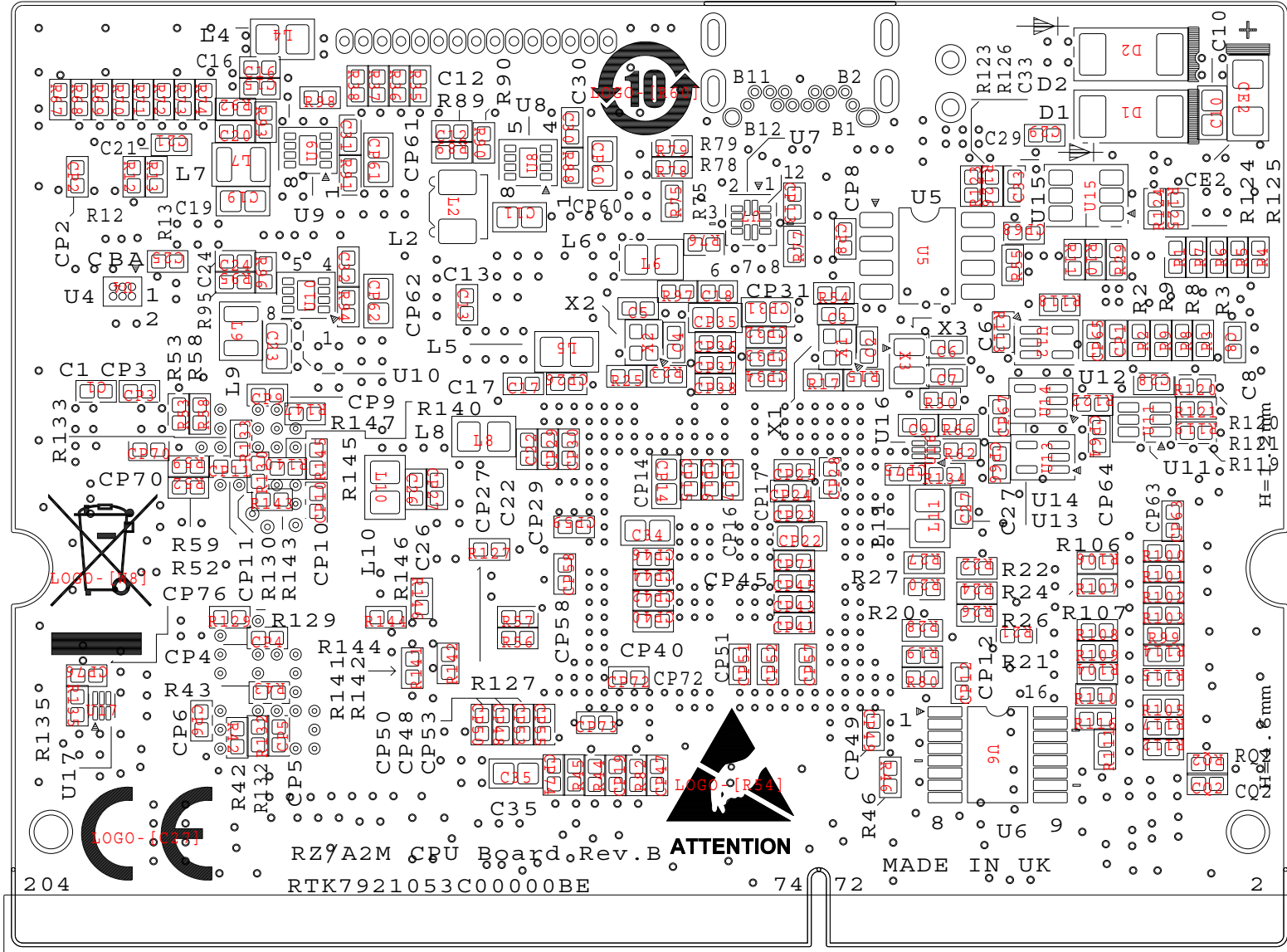
CHANGE	Renesas Electronics Corporation.			RZ/A2M CPU board	
	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED
	DATE	Power			
	19-09-10	R20UT4394EJ0400			
		(5 / 6)			



CHANGE	Renesas Electronics Corporation.				RZ/A2M CPU board	
	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED	POR, UDI
	DATE 19-09-10					R20UT4394EJ0400

Appendix 2 RTK7921053C00000BE Component Installation Diagram





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RZ9A2M CPU Board, Rev. B
RTK7921053C00000BE

ATTENTION

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MADE IN UK

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Revision History	RZ/A2M CPU Board RTK7921053C00000BE User's Manual
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Rev.	Date of Issue	Revised content	
		Page	Point
1.00	Oct. 11, 2018	—	First version issued
1.10	Apr. 08, 2019	Appendix 1	RTK7921053C00000BE Connection Diagram
		—	Updated RTK7921053C00000BE Connection Diagram
1.20	Jul. 17, 2019	—	Unused HM_INT# and HM_RSTO# terminals
		2-6	- Table 2.2.5 E2 pin
		2-8	- Table 2.2.7 K3 pin
		2-18	- Figure 2.3.2
		Appendix 1	- Connection Diagram
—	Correction of mistakes		
2.00	Jan. 31, 2020	Overall	Updated silk screen
		1-4	Figure 1.2: Update
		2-2	Table 2.2.1: Corrected comments of A6 pin
		2-6	Table 2.2.5: Corrected pin function and description of E2 pin
		2-6	Table 2.2.5: Corrected comments of F1 pin
		2-8	Table 2.2.7: Corrected pin function and description of K3 pin
		2-16	2.3.2: Deleted JP1 related sentence
		2-16	Figure 2.3.1: Deleted JP1, Changed ROMVcc to 3.3V
		2-16	Table 2.3.2: Deleted
		2-17	2.3.3: Deleted JP2 related sentence
		2-17	Figure 2.3.2: - Deleted JP2, Changed RAMVcc to 1.8V - Added pull-up resistor to HM_DQ[7:0] - Added pull-down resistor to HM_RWDS - Added level shifter to HM_INT# and HM_RSTO#
		2-17	Table 2.3.4: Deleted
		2-18	Figure 2.4.1: Added buffer to VBUSIN0
		2-24	Figure 2.9.1: Deleted JP1 and JP2
		2-26	Figure 2.11.1: Changed pull-down resistor of SD0_CD and SD0_WP to unmounted
		3-12	Figure 3.2.1: Deleted JP1 and JP2
		3-13	3.2.1: Deleted JP1 and JP2 related sentence
		3-13	Figure 3.2.2: Deleted JP1 and JP2
		3-13	Table 3.2.1: Deleted
Appendix 1	Updated RTK7921053C00000BE Connection Diagram		
Appendix 2	Updated RTK7921053C00000BE Component Installation Diagram		

RZ/A2M CPU Board RTK7921053C00000BE User's Manual

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