User Manual

32

RH850 Evaluation Platform

RH850/P1H-CE-404BGA PiggyBack board

Y-RH850-P1XC-404PIN-PB-T1-V2

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Chapter 1 Introduction

The RH850/P1H-CE Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/P1H-CE microcontroller. The PiggyBack board (Y-RH850-P1XC-404PIN-PB-T1-V2) can be used as a standalone board, or can be mated with a mainboard (e.g. Y-RH850-X1X-MB-Tx-Vx) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 3.3V and 1.25V)
- Device programming capability
- Device debugging capability
- Pin headers for direct access to each functional device pin
- Reset switch
- MainOSC circuitry
- Connectors to MainBoard
- Operating temperature from 0°C to +40°C

This document describes the functionality provided by the PiggyBack board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the RH850/P1H-CE User's Manual.

This manual describes the following board revision:

- Y-RH850-P1XC-404PIN-PB-T1-V2

For differences to the Y-RH850-P1XC-404PIN-PB-T1-V1 board see **Chapter 11 'Revision History'**.

Chapter 2 Overview

2.1 Overview

Figures 1 and 2 provide a schematic view of the PiggyBack board.

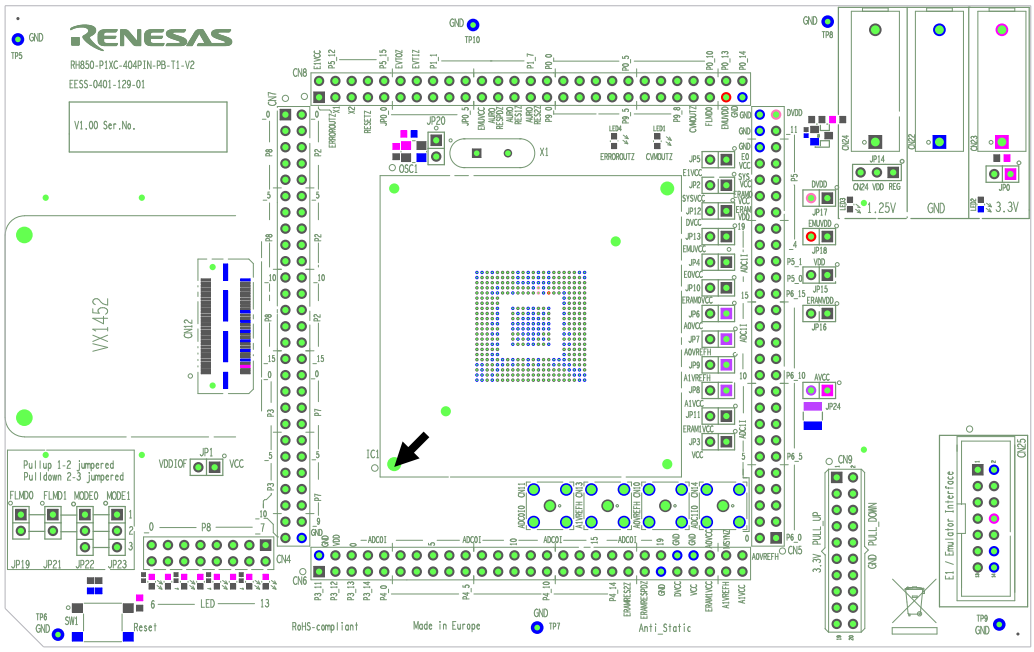

Figure 1 PiggyBack Board Schematic Top View

The black arrow denotes the position of socket pin #1.

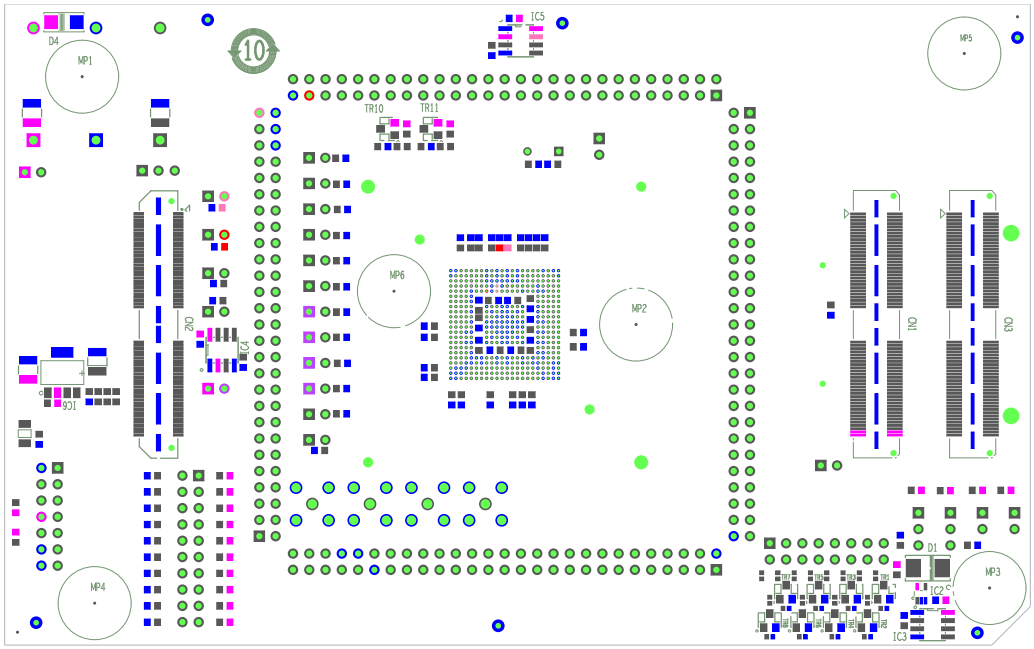

Figure 2 PiggyBack Board Schematic Bottom View

2.2 Mounting of the device

The board is designed for use with the following device:

RH850/P1H-CE in BGA404 package.

The device must be placed inside the socket IC1. To insert the device align the corner of the device package marked with a white triangle (see picture below) with the #1pin of the socket. The #1pin of the socket is marked with a circle near to the “IC1” label (see also black arrow in Figure 1).

Figure 3 Alignment Mark on Device Package

First insert the device into the socket with closed mount. Then press down the lid of the socket until the device slips into the socket and finally release the lid.

CAUTION: *Please follow the mounting instruction carefully as described. Otherwise the device might get damaged.*

Chapter 3 Power supply

3.1 Board power connection

For operation of the device, a supply voltage must be connected to the board. There are several possibilities to power the device.

Within this document the following voltages are considered as 'typical' connections:

Voltage1 = 3.3V

Voltage2 = 1.25V

Direct voltage supply

Two different voltages can be supplied to the board.

The following connectors are available to supply those voltages directly:

- Three 4mm 'banana-type' connectors:
  - Two red connectors for voltages Voltage1 (CN23) and Voltage2 (CN24).
  - A black connector for ground (GND) connection (CN22).
  Note: The three connectors are supplied with the board but not assembled.

For details about voltage distribution, refer to **Chapter 3.2 'Voltage distribution'**.

Supply by MainBoard

In case the PiggyBack board is mounted on a MainBoard, the voltage Voltage1 is supplied by the on-board regulator of the MainBoard.

CAUTION: *Do not supply Voltage1 directly to the PiggyBack board in case it is mounted on the MainBoard.*

For each of the voltages, Voltage1 and Voltage2 a green LED is available to signal that the related voltage is available on the PiggyBack board. The corresponding LEDs are placed directly beneath the connectors of the related voltage.

- Voltage1 is signalled by LED2
- Voltage2 is signalled by LED3

3.2 Voltage distribution

The table below shows the required device power supply pins. For detailed explanation of their function, please refer to the user documentation of the device.

Device Supply Pin
SYSVCC
VCC
EnVCC (n = 0, 1)
AnVCC (n = 0, 1)
AnVREFH (n = 0, 1)
ERAMnVCC (n = 0, 1)
DVCC
EMUVCC
VDD
DVDD
ERAMVDD
EMUVDD

Additional one power supply for the MainBoard can be selected:

Supply voltage	Function
VDDIOF	IO supply voltage for components located on a connected mainboard.

The following figure shows the configurable voltage distribution on the PiggyBack board.

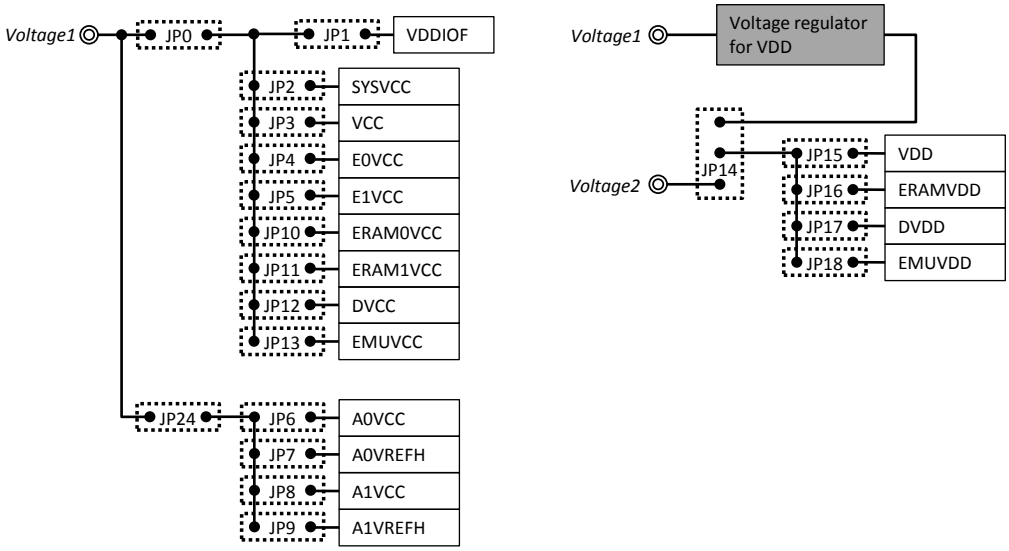

Figure 4 Voltage Distribution on the PiggyBack Board

- All power supply lines can be interrupted by jumpers. This provides the possibility to measure the current consumption of each individual power domain of the device (JP2 – 13 and JP15 – 18).
- The IO supply voltage for the Mainboard (VDDIOF) can be connected via jumper JP1 to Voltage1, if the PiggyBack board is mounted on a MainBoard.
- VDD can be powered either directly from the ‘banana-type’ connector (Voltage2 – CN24) or by an on-board voltage regulator. Thereby the DPS device can be operated with one single voltage supply (Voltage1*)*. The source for VDD is selectable by jumper JP14.

Chapter 4 Clock sources

One external crystal oscillator for the device clock supply is provided with the board.

4.1 MainOsc

A crystal or ceramic resonator can be mounted on socket X1.

A 16Mhz oscillator is supplied with the board.

4.2 Programmable Oscillator

It is possible to mount a programmable crystal oscillator on the PiggyBack board at OSC1. The available footprint and circuitry is designed for a SG-8002CE programmable crystal oscillator from Epson Toyocom. The output from this oscillator can be connected to port X1 of the device via jumper JP20. The SG-8002CE is neither mounted nor provided with the board. For details about the available circuitry refer to **Chapter 10 'Schematic'**. A resonator mounted on socket X1 must not be used in parallel to another clock source.

Chapter 5 Debug and Programming interface

For connection of the microcontroller debug and flash programming tools, the connector CN25 with fourteen pins is provided.

The signal connection of the connector CN25 is shown in the table below:

CN25 Pin	Device Port	Device Signal
1	JP0_2	TCK / LPDCLK / FLSCI3SCKI
2	GND	GND
3	JP0_4	TRSTZ
4	FLMD0	FLMD0
5	JP0_1	TDO / LPDO / FLSCI3TXD
6	-	-
7	JP0_0	TDI / LPDI / FLSCI3RXD / FLSCI3TXD
8	‘Dbg_Voltage’	Voltage1
9	JP0_3	TMS
10	-	-
11	JP0_5	RDYZ / LPDCLKOUT
12	GND	-
13	RESET	RESETZ
14	GND	-

Chapter 6 Connectors for ports of device

Connection to each functional pin of the device is possible via the connectors CN5 to CN8. For detailed explanation of their function, please refer to the user documentation of the device.

CAUTION: *The pin headers are directly connected to the pins of the device, therefore special care must be taken to avoid any electrostatic or other damage to the device.*

The following signals/device ports are not available at the connectors CN5 to CN8:

Device Port
TODP0
TODN0
TODP1
TODN1
CICREFP
CICREFN
AUDATA0
AUDATA1
AUDATA2
AUDATA3
AUDCK
AUDSYNCZ
AUDRSTZ

6.1 Connectors for ADC voltage supply

It is possible to apply the ADC related supply voltages via SMA connectors (CN10, CN11, CN13 and CN14). These are directly connected (JP7 and 9 are bypassed) to the following pins of the device

Device Port
ADC0I0
A0VREFH
ADC1I0
A1VREFH

The SMA connectors are not mounted on nor provided with the boards. SMA connectors that fit to the following mounting holes available on the board can be mounted on the board.

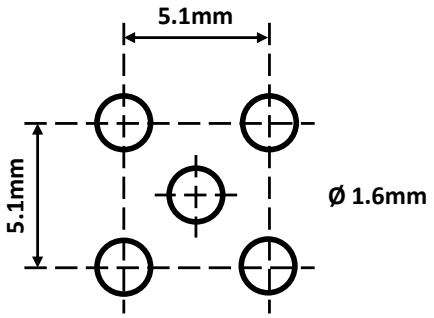

Figure 5 Mounting Holes for SMA Connectors

6.2 Connector for Trace I/F

One connector CN12 (Samtec QTH-030-01-L-D-A) is available with the following connections to the device

CN12 Pin #	Device Port	CN12 Pin #	Device Port
1	-	2	-
3	JP0_2	4	RESETZ
5	JP0_3	6	Voltage1[1)]
7	JP0_0	8	-
9	JP0_1	10	GND[1)]
11	JP0_4	12	TODP0
13	EVTOZ	14	TODN0
15	JP0_5	16	GND[1)]
17	EVTIZ	18	TODP1
19	P0_10	20	TODN1
21	ERAMRESPDZ	22	GND[1)]
23	FLMD0	24	-
25	-	26	-
27	-	28	GND[1)]
29	-	30	-
31	-	32	-
33	-	34	GND[1)]
35	-	36	CICREFP
37	-	38	CICREFN
39	-	40	GND[1)]
41	-	42	-
43	AUDATA3	44	-
45	AUDATA2	46	-
47	AUDATA1	48	-
49	AUDATA0	50	MSYNZ
51	-	52	AURORES2Z
53	AUDSYNCZ	54	AURORES1Z
55	AUDRSTZ	56	-
57	AUDCK	58	-
59	-	60	GND[1)]

1) These are not device pins but electrical signals on the PiggyBack board.

It is possible to mount a Vector VX1452 Generic POD to the PiggyBack board via CN12. Additionally, dedicated mounting holes are available on the board for mechanical assembly of the POD. It is recommended to use the ELPAC miniature PCB spacer (LPR 8233-4,8-MINI) delivered with the board.

6.3 Push button for RESET

In order to issue a reset to the device, the push-button SW1 is available.

6.4 Mode Selection

The PiggyBack Board gives the possibility to configure the following mode pins

- FLMD0 via jumper JP19
- FLMD1 via jumper JP21
- MODE0 via jumper JP22
- MODE1 via jumper JP23

To apply “High” or “Low” to the mode pins, the pins 1 and 2, or the pins 2 and 3 of the corresponding jumper must be shorted, respectively.

Note: Pin 1 is marked by a small circle.

CAUTION: *Be careful in configuration of mode related pins, as wrong configuration can cause irregular behaviour of the devices. Be sure to check the corresponding User Manual, for details, which modes can be selected for the device.*

6.5 Connectors to MainBoard

Three connectors (CN1, CN2 and CN3) are available to connect the PiggyBack board to a MainBoard. Regarding the function on the MainBoard, please refer to the UM of supported MainBoards.

6.5.1 Connector CN1

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	-	-		2	-	-
3	-	-		4	-	-
5	RESET	RESETZ		6	NMI	P5_7
7	-	-		8	-	-
9	INT0	P4_7		10	INT1	P4_12
11	INT2	P5_13		12	INT3	P0_5
13	-	-		14	-	-
15	UART0TX	P5_14		16	UART1TX	P5_5
17	UART0RX	P5_13		18	UART1RX	P5_4
19	LIN0TX	P5_14		20	LIN1TX	P5_5
21	LIN0RX	P5_13		22	LIN1RX	P5_4
23	-	-		24	-	-
25	-	-		26	-	-
27	CAN0TX	P5_1		28	CAN1TX	P5_9

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
29	CAN0RX	P5_0		30	CAN1RX	P5_10
31	SENT0IN	P0_0		32	SENT1IN	P0_1
33	SENT0OUT	P2_4		34	SENT1OUT	P3_9
35	-	-		36	-	-
37	-	-		38	-	-
39	-	-		40	-	-
41	FLX0TX	P3_7		42	FLX0EN	P3_5
43	FLX0RX	P3_2		44	-	-
45	FLX1TX	P7_5		46	FLX1EN	P7_6
47	FLX1RX	P7_7		48	-	-
49	-	-		50	-	-
51	ETH0MDIO	P3_3		52	ETH0MDC	P3_6
53	ETH0RXD0	P4_3		54	EH0TXD0	P3_9
55	ETH0RXD1	P4_4		56	EH0TXD1	P3_10
57	ETH0RXD2	P4_5		58	EH0TXD2	P3_12
59	ETH0RXD3	P4_6		60	EH0TXD3	P3_13
61	ETH0RXDCLK	P4_2		62	ETH0TXCLK	P4_1
63	ETH0RXER	P4_0		64	ETH0TXER	P3_8
65	ETH0CRSDV	P3_7		66	ETH0TXEN	P3_14
67	ETH0RXDV	P4_7		68	ETH0COL	P3_5
69	ETH0RESET	P3_0		70	ETH0LINK	P3_1
71	-	-		72	-	-
73	-	-		74	-	-
75	-	-		76	-	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	DIGIO_0	P8_0		86	DIGIO_1	P8_1
87	DIGIO_2	P8_2		88	DIGIO_3	P8_3
89	DIGIO_4	P8_4		90	DIGIO_5	P8_5
91	DIGIO_6	P8_6		92	DIGIO_7	P8_7
93	DIGIO_8	P8_8		94	DIGIO_9	P8_9
95	DIGIO_10	P8_10		96	DIGIO_11	P8_11
97	DIGIO_12	P8_12		98	DIGIO_13	P8_13
99	DIGIO_14	P8_14		100	DIGIO_15	P8_15
101	-	-		102	-	-
103	MUX0	P2_0		104	MUX1	P2_1
105	MUX2	P2_2		106	-	-
107	ADC0	ADC0I0		108	ADC1	ADC0I1
109	ADC2	ADC0I2		110	ADC3	ADC0I3
111	ADC4	ADC0I4		112	ADC5	ADC0I5
113	ADC6	ADC0I6		114	ADC7	ADC0I7

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
115	VDDIOF	-		116	VDDIOF	-
117	Voltage1	-		118	Voltage1	-
119	Voltage1	-		120	Voltage1	-

6.5.2 Connector CN2

The functions assigned to pins #99 to #118 are not available on any of the currently available Mainboards. They are only reserved for a potential future update.

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	CAN2TX	P5_14		2	CAN3TX	P9_7
3	CAN2RX	P5_15		4	CAN3RX	P9_8
5	-	-		6	-	-
7	-	-		8	-	-
9	LIN2TX	P7_5		10	LIN3TX	P9_1
11	LIN2RX	P7_4		12	LIN3RX	P9_2
13	-	-		14	-	-
15	-	-		16	-	-
17	-	-		18	-	-
19	-	-		20	-	-
21	-	-		22	-	-
23	-	-		24	-	-
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39	-	-		40	-	-
41	-	-		42	-	-
43	-	-		44	-	-
45	-	-		46	-	-
47	-	-		48	-	-
49	-	-		50	-	-
51	-	-		52	-	-
53	-	-		54	-	-
55	-	-		56	-	-
57	-	-		58	-	-
59	-	-		60	-	-
61	-	-		62	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
63	-	-		64	-	-
65	-	-		66	-	-
67	-	-		68	-	-
69	-	-		70	-	-
71	-	-		72	-	-
73	-	-		74	-	-
75	-	-		76	-	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
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85	-	-		86	-	-
87	-	-		88	-	-
89	-	-		90	-	-
91	-	-		92	-	-
93	-	-		94	-	-
95	-	-		96	-	-
97	-	-		98	-	-
99	ETH1MDIO	P8_15		100	ETH1MDC	P7_1
101	ETH1RXD0	P8_5		102	EH0TXD0	P8_9
103	ETH1RXD1	P8_4		104	EH0TXD1	P8_11
105	ETH1RXD2	P8_1		106	EH0TXD2	P8_12
107	ETH1RXD3	P8_0		108	EH0TXD3	P8_13
109	ETH1RXDCLK	P8_6		110	ETH1TXCLK	P8_7
111	ETH1RXER	P8_3		112	ETH1TXER	P8_14
113	ETH1CRSDV	P8_2		114	ETH1TXEN	P8_10
115	ETH1RXDV	P7_4		116	ETH1COL	P7_2
117	ETH1RESET	P7_0		118	ETH1LINK	P7_3
119	-	-		120	-	-

6.5.3 Connector CN3

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	-	-		2	-	-
3	-	-		4	-	-
5	-	-		6	-	-
7	-	-		8	-	-
9	-	-		10	CSIH1CSS0	P4_1
11	-	-		12	-	-
13	-	-		14	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
15	-	-		16	-	-
17	-	-		18	-	-
19	-	-		20	-	-
21	CSIH1CSS2	P3_12		22	CSIH1CSS7	P3_11
23	-	-		24	-	-
25	-	-		26	DIGIO	P2_2
27	-	-		28	CSIH1SO	P4_2
29	CSIH1SC	P4_3		30	CSIH1SI	P4_4
31	-	-		32	-	-
33	-	-		34	-	-
35	-	-		36	-	-
37	-	-		38	-	-
39	DIGIO	P2_3		40	-	-
41	-	-		42	-	-
43	-	-		44	-	-
45	-	-		46	-	-
47	-	-		48	-	-
49	-	-		50	-	-
51	-	-		52	-	-
53	-	-		54	-	-
55	-	-		56	-	-
57	-	-		58	-	-
59	-	-		60	-	-
61	-	-		62	-	-
63	-	-		64	-	-
65	-	-		66	-	-
67	-	-		68	-	-
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73	-	-		74	-	-
75	-	-		76	-	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	-	-		86	-	-
87	-	-		88	-	-
89	-	-		90	-	-
91	-	-		92	-	-
93	-	-		94	-	-
95	-	-		96	-	-
97	-	-		98	-	-
99	-	-		100	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
101	-	-		102	-	-
103	-	-		104	-	-
105	-	-		106	-	-
107	-	-		108	-	-
109	-	-		110	-	-
111	-	-		112	-	-
113	-	-		114	-	-
115	-	-		116	-	-
117	-	-		118	-	-
119	-	-		120	-	-

Chapter 7 Other circuitry

7.1 Signalling for CVMOUTZ and ERROROUTZ

Two red LEDs, LED1 and LED4 are available two indicate a “low” output signal from CVMOUTZ and ERROROUTZ, respectively.

7.2 Pin Headers for Pull-Down and Pull-Up

A connector CN9 is available to enable easy connection to Voltage1 (3.3V) or GND via pull-up or pull-down resistances, respectively.

Hereby uneven pins from 1 to 19 (in total ten) are configured as pull-up pin headers, while the even numbers from 2 to 20 (in total ten) can be used for pull-down.

By connecting device port pins from CN5 – 8 to CN9 it is therefore possible to pull a desired port pin to “Low” or “High”.

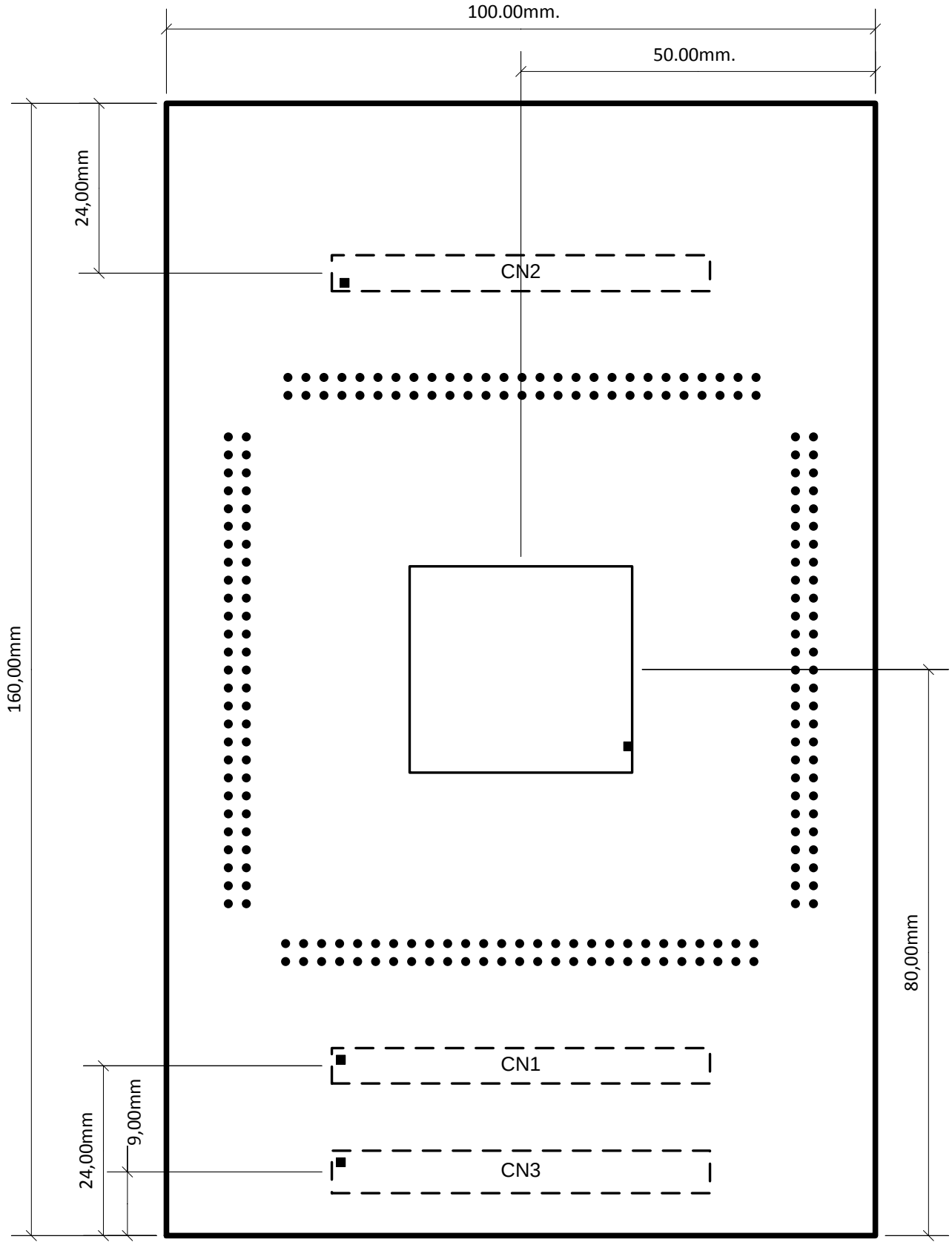
7.3 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins. Device pins P8_0 to P8_7 are connected to the uneven pins 15 to 1 of the pin header CN4, while the LEDs 6 to 13 are connected to the even pins 16 to 2, respectively. Thus the LEDs can be either connected to the device port pins P8_0 to P8_7 via jumper or any device port pin can be connected directly to the even pin headers.

Chapter 8 Precautions

No limitations are known at the release of this document.

Chapter 9 Mechanical dimensions



Chapter 10 Schematic

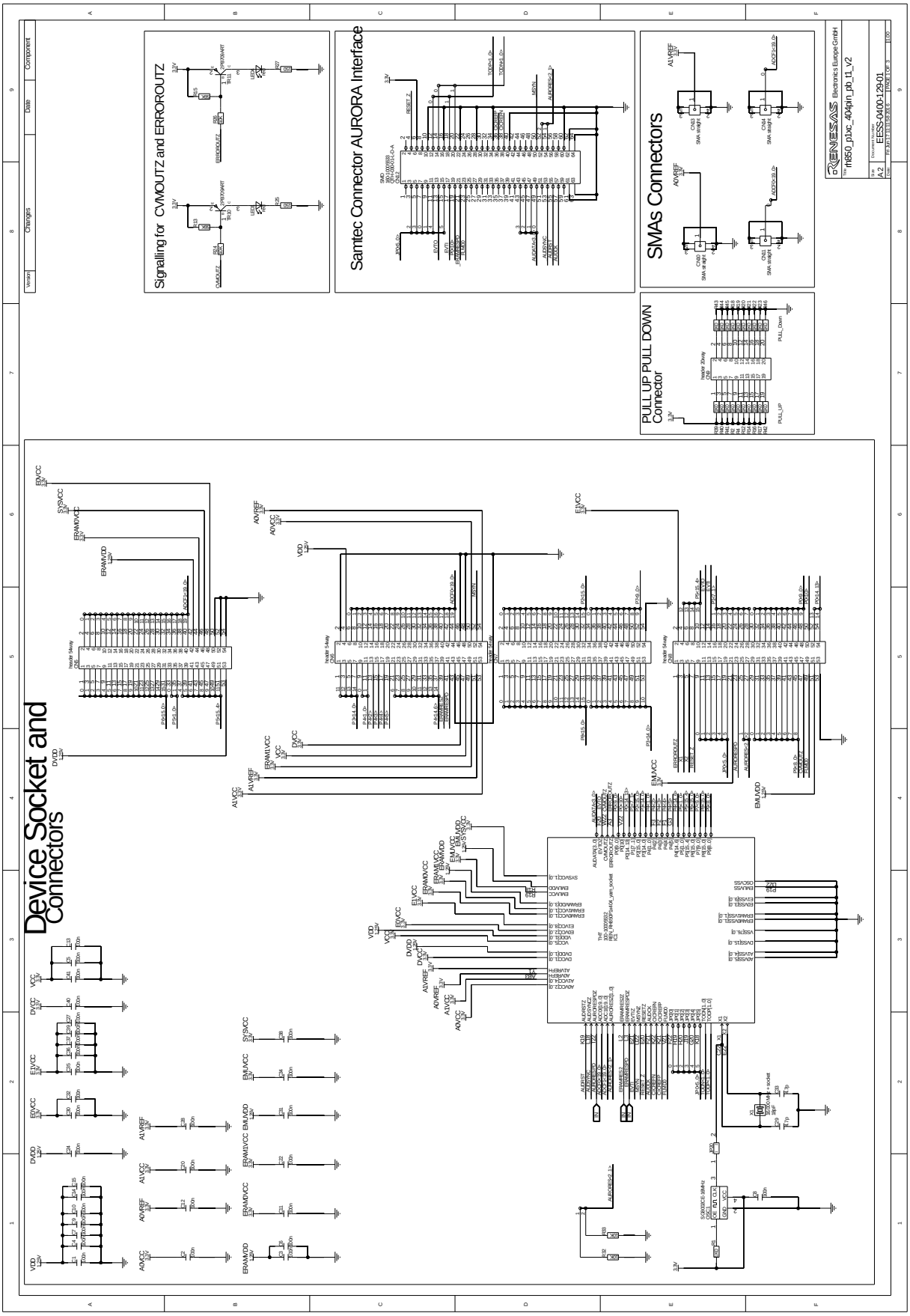
CAUTION: *The schematic shown in this document is not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.*

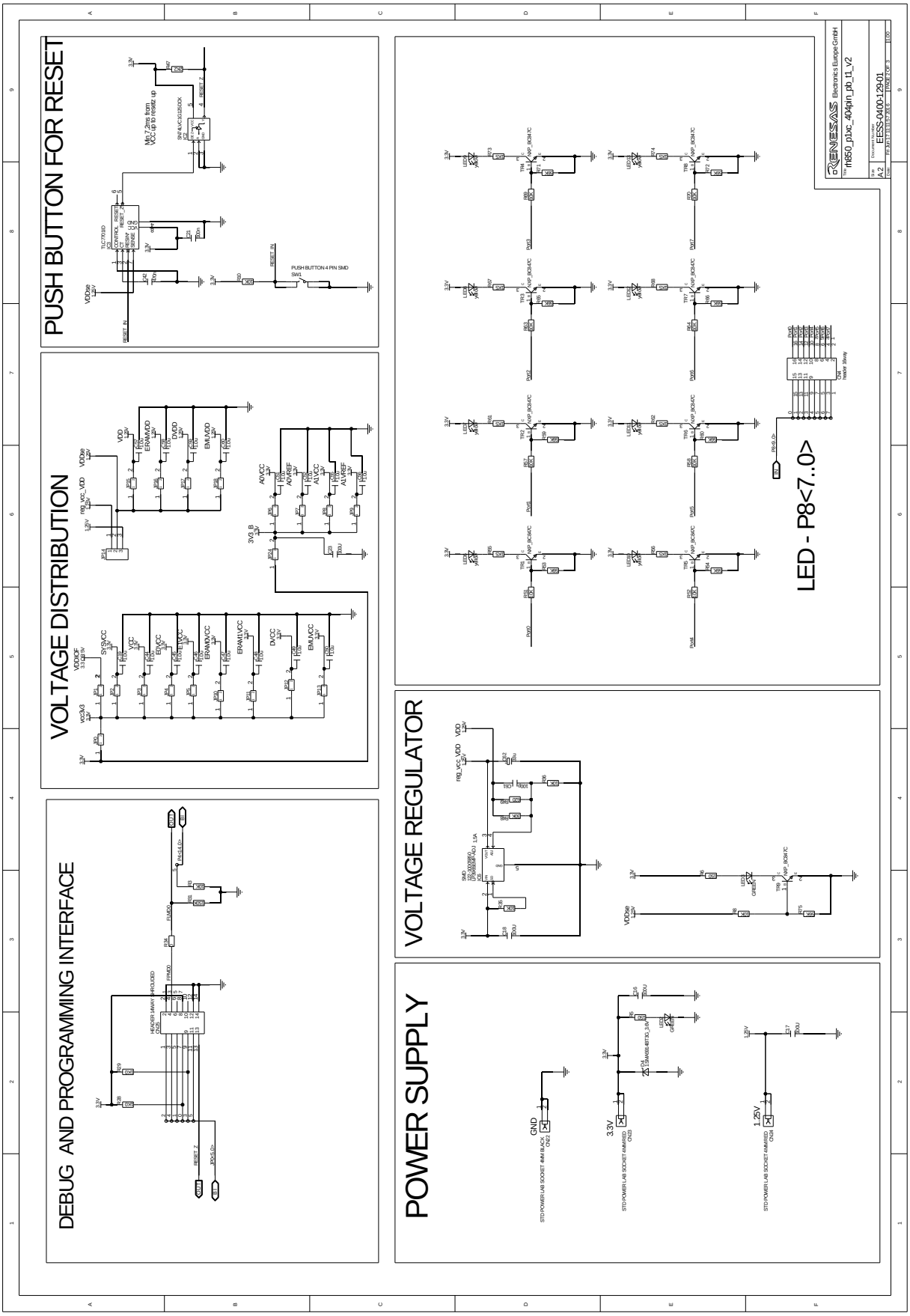
The following components described in the schematic are not provided with the board:

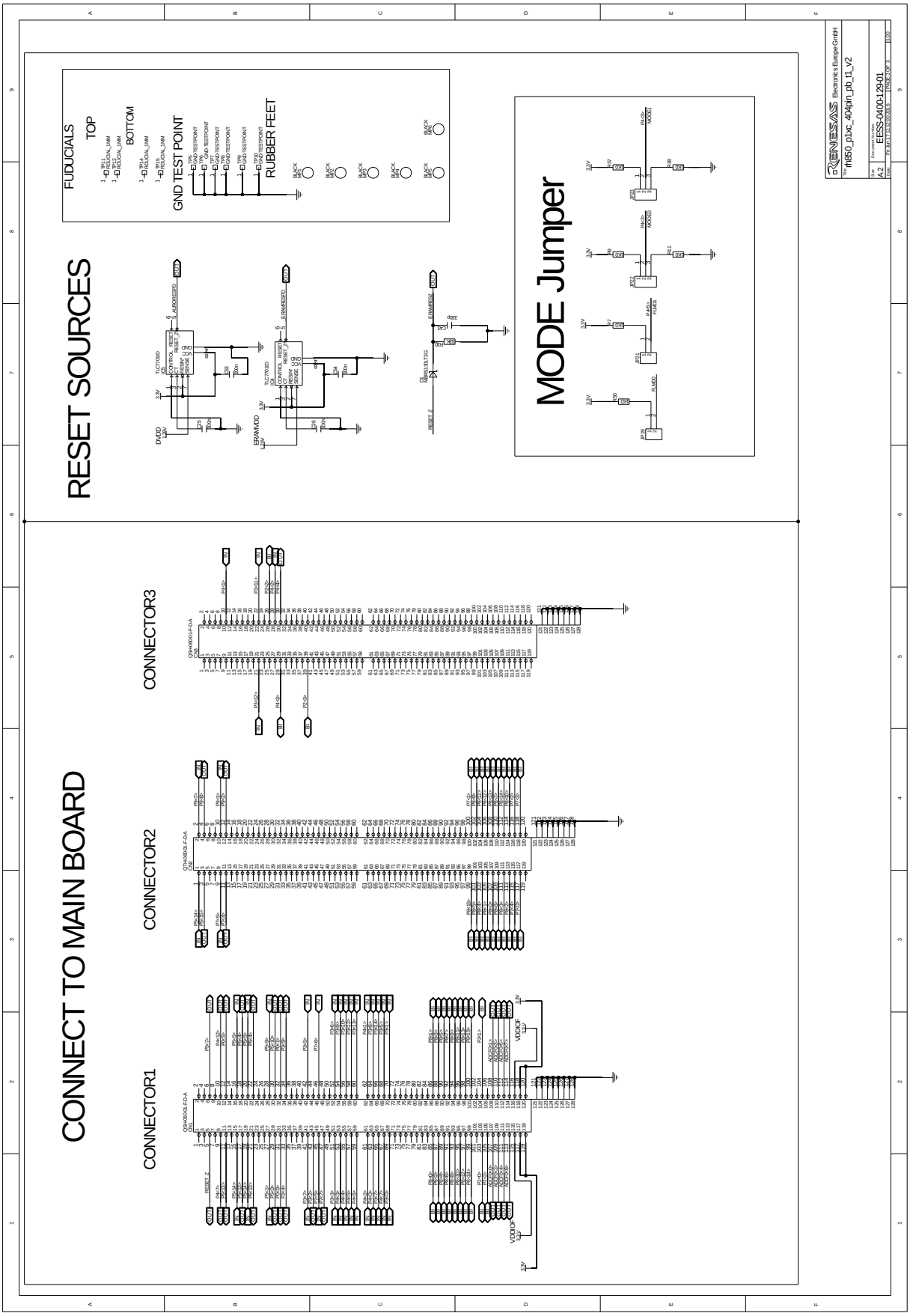
- SMA connectors
  - CN10
  - CN11
  - CN13
  - CN14
- Jumper JP20
- Oscillator OSC1
- Capacitors
  - C29
  - C33
- Resistances
  - R28
  - R29
  - R31

The following components described in the schematic are provided with but not mounted on the board:

- Standard 4mm power lab sockets
  - CN22
  - CN23
  - CN24


Signalling for CVMOUTZ and ERROROUTZ
Samtec Connector AURORA Interface
SMAs Connectors
PULL UP PULL DOWN Connector
Device Socket and Connectors
RENESAS Electronics Europe GmbH
rh850_p1xc_404pin_pb_t1_v2
EES-0400-129-01


PUSH BUTTON FOR RESET
VOLTAGE DISTRIBUTION
DEBUG AND PROGRAMMING INTERFACE
LED - P8<7..0>
VOLTAGE REGULATOR
POWER SUPPLY
RENESAS Electronics Europe GmbH
m850_p1xc_404pin_pb_t1_v2
EESS-0400-129-01


RESET SOURCES
FUDUCIALS
TOP
BOTTOM
GND TEST POINT
RUBBER FEET
MODE Jumper
CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RENESAS Electronics Europe GmbH
rh850_p1xc_404pin_pb_t1_v2
EESS-0400-129-01

Chapter 11 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2016-08-04	1.0	Initial release

Differences to the Y-RH850-P1XC-404PIN-PB-T1-V1

- Changed circuitry for signalling of Voltage2
- The connector for the Trace I/F CN12 has additional pin assignment. FLMD0 is connected to pin #23 and pin #40 is connected to GND
- GPIO signal LEDs (LED6 – 13) for P8_0 to P8_7 or other device port pins
- Changed value of R30
- Changed circuitry for signalling of CVMOUTZ and ERROROUTZ
- Support of functions on new mainboard (touchpad) by adding CN3
- Added signals on CN2 in order to support additional Ethernet I/F, if this is added on a possible future update of the mainboards
- Four ELPAC miniature PCB spacer (LPR 8233-4,8-MINI) are delivered with the board

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