RH850 Evaluation Platform

RH850/F1x 144-pin  
RH850/R1x 144-pin

User’s Manual: Piggyback board V3

Y-RH850-F1X-144PIN-PB-T1-V3

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable.
   When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal.
   Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   - The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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Chapter 1  Introduction

The RH850/F1x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/F1x microcontrollers. The piggyback board (Y-RH850-F1X-144PIN-PB-T1-V3) can be used as a standalone board, or can be mated with a mainboard (e.g. Y-RH850-X1X-MB-Tx-Vx) for extended functionality.

Main features:

• Socket for mounting of device
• Standalone operation of the board
• Direct supply of device voltage (typ. 3.3V-5.0V)
• Device programming capability
• Device debugging capability
• Pin headers for direct access to each device pin
• Reset switch
• MainOSC and SubOSC circuitry
• Signal LEDs
• Connectors to mainboard

This document describes the functionality provided by the piggyback board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the User’s Manual of the applicable devices:

• RH850/F1L
• RH850/R1L
• RH850/F1M
• RH850/F1K
• RH850/F1KM-S2
• RH850/F1KM-S4

This manual describes the following board revision:

• Y-RH850-F1X-144PIN-PB-T1-V3

For differences to the Y-RH850-F1X-144PIN-PB-T1-V2 see the Revision History.
### 1.1 Package Components

The Y-RH850-F1X-144PIN-PB-T1-V3 product package consists of the items included in below table. After you have unpacked the box, check if your Y-RH850-F1X-144PIN-PB-T1-V3 package contains all these items.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>D15371#01</td>
<td>RH850/F1x 144pin piggyback board</td>
<td>1</td>
</tr>
<tr>
<td>D15373</td>
<td>Documentation CD</td>
<td>1</td>
</tr>
<tr>
<td>D010816-24</td>
<td>China RoHS document</td>
<td>1</td>
</tr>
<tr>
<td>D15370-24</td>
<td>Product contents List</td>
<td>1</td>
</tr>
<tr>
<td>Jumpers (2-way, 0.1&quot;)</td>
<td>In the bag</td>
<td>37</td>
</tr>
<tr>
<td>Red Hirschmann 4 mm power lab sockets</td>
<td>In the bag</td>
<td>2</td>
</tr>
<tr>
<td>Black Hirschmann 4 mm power lab sockets</td>
<td>In the bag</td>
<td>1</td>
</tr>
<tr>
<td>Crystal, TC38, 32.768 kHz</td>
<td>In the bag</td>
<td>1</td>
</tr>
<tr>
<td>Crystal, HC49, 8 MHz</td>
<td>In the bag</td>
<td>1</td>
</tr>
<tr>
<td>Crystal, HC49, 20 MHz</td>
<td>In the bag</td>
<td>1</td>
</tr>
</tbody>
</table>

Note: Please keep the Y-RH850-F1X-144PIN-PB-T1-V3 packing box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original packing box when transporting the Y-RH850-F1X-144PIN-PB-T1-V3. If packing of your product is not complete, it may be damaged during transportation.
Chapter 2 Overview

2.1 Overview

Figures 1 and 2 provide the views of the piggyback board.

Device pin #1

Figure 1 – Piggyback board top view

Figure 2 – Piggyback board bottom view
2.2 Mounting of the device

The board is designed for use with the following devices, all in their 144 pin package:

- RH850/F1L
- RH850/F1M
- RH850/F1K
- RH850/F1KM-S2
- RH850/F1KM-S4
- RH850/R1L

The device must be placed inside the socket IC1. To insert the device, press down the lid, align the #1 pin of the device to the #1 pin of the socket, insert the device inside the socket and release the lid.
Chapter 3 Jumper Configuration

The function of the board can be configured via jumpers. This chapter describes the standard configuration, i.e., jumper setting for the intended devices. For the supported function of the used device, please refer to the corresponding HW user's manual.

The table has the following meaning:

- \( x-y \): Connect the pins \( x \) and \( y \); valid for 3-pin jumpers (e.g., JP19)

The pin #1 can be identified by a small circle in the vicinity of the jumper.

Depending on the used device, a configuration of several jumpers is required. The detailed configuration is shown below. The applicable setting for each device/jumper is highlighted in blue:

<table>
<thead>
<tr>
<th></th>
<th>F1L</th>
<th>F1M</th>
<th>F1H</th>
<th>F1K</th>
<th>F1KM-S2</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP7 1-2</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>open</td>
<td>Selection of Pin 61: P1_6 or ISOVCL</td>
</tr>
<tr>
<td>JP7 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td></td>
</tr>
<tr>
<td>JP20</td>
<td>closed</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>closed</td>
<td>Selection of pin 98: P9_6, VSS or REGVCC</td>
</tr>
<tr>
<td>JP22</td>
<td>open</td>
<td>closed</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td></td>
</tr>
<tr>
<td>JP23</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>closed</td>
<td></td>
</tr>
<tr>
<td>JP24</td>
<td>closed</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>closed</td>
<td>Selection of pin 97: P9_5, ISOVCL or VSS</td>
</tr>
<tr>
<td>JP25</td>
<td>open</td>
<td>closed</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td></td>
</tr>
<tr>
<td>JP26</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>closed</td>
<td></td>
</tr>
<tr>
<td>JP27 1-2</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>open</td>
<td>Selection of Pin 60: P1_7 or VSS</td>
</tr>
<tr>
<td>JP27 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td></td>
</tr>
<tr>
<td>JP28 1-2</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>open</td>
<td>Selection of Pin 14: P11_14 or VSS</td>
</tr>
<tr>
<td>JP28 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td></td>
</tr>
<tr>
<td>JP29 1-2</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>open</td>
<td>Selection of Pin 73: P11_13 or ISOVCL</td>
</tr>
<tr>
<td>JP29 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td></td>
</tr>
<tr>
<td>JP30 1-2</td>
<td>closed</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>Either</td>
<td>Selection of PWGA34: Either from P9_5 or P0_11</td>
</tr>
<tr>
<td>JP30 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>Or</td>
<td></td>
</tr>
<tr>
<td>JP31 1-2</td>
<td>closed</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>Either</td>
<td>Selection of PWGA35: Either P9_6 or P0_6</td>
</tr>
<tr>
<td>JP31 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>Or</td>
<td></td>
</tr>
<tr>
<td>JP32 1-2</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>open</td>
<td>Selection of PWGA53: Either P11_13 or P10_4</td>
</tr>
<tr>
<td>JP32 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>closed</td>
<td></td>
</tr>
<tr>
<td>JP33 1-2</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>closed</td>
<td>open</td>
<td>Selection of PWGA54: Either P11_14 or P10_5</td>
</tr>
<tr>
<td>JP33 2-3</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>open</td>
<td>closed</td>
<td></td>
</tr>
</tbody>
</table>
The jumper setting also are shown in this picture:

- The **green jumper** JP12 for FLMDO0 always must be closed for a ‘normal’ (user mode and debug) operation of the device.
- The **red jumpers** must be set for a single “Voltage 1” (typ +5.0V) operation of the device.
- The **blue jumper** must be set for a single “Voltage 2” (typ +3.3V) operation of the device.
- The **orange jumpers** must be selected depending on the used device. See the printing on the board for the applicable setting.

For jumper settings related to the device operation mode, refer to the chapter 8.2.
Chapter 4  Power supply

4.1  Board power connection

For operation of the device, a supply voltage must be connected to the board. Though a single supply voltage is sufficient for the operation of the device, two (different) voltages can be supplied to the board.

Within this document the following voltages are considered as ‘typical’ connections:

- Voltage1 = 5.0V
- Voltage2 = 3.3V

The following connectors are available to supply those voltages:

- Three 4mm ‘banana-type’ connectors:
  - Two red connectors for voltages Voltage1 (CN10) and Voltage2 (CN11).
  - A black connector for VSS connection (CN12).
  **Note:** The three connectors are supplied with the board but not assembled.
- The E1 emulator, that is used for debug purposes and flash programming, can also supply a single operating voltage (‘Dbg_Voltage’). The voltage is programmable via the E1 GUI as 3.3 or 5.0V (typ). See the documentation of the E1 and chapter 5 ‘Debug and Programming interface’ for details.
- In case the piggyback board is mounted on a mainboard, the voltages Voltage1 and Voltage2 are supplied by the on-board regulators of the mainboard.
  **NOTE:** Do not supply any voltage directly to the piggyback board in case it is mounted on the mainboard.

For each of the two voltages, ‘Voltage 1 ’ and ‘Voltage 2’, a green LED (LED1 and LED2) is available to signal that the related voltage is available on the piggyback board.
4.2 Voltage distribution

The table shows the required device power supply pins and their function:

<table>
<thead>
<tr>
<th>Device supply pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>REGVCC</td>
<td>Supply for the device internal regulators for the digital logic.</td>
</tr>
<tr>
<td>EVCC</td>
<td>Supply for ports of AWO and ISO area.</td>
</tr>
<tr>
<td>BVCC</td>
<td>Supply for ports of AWO and ISO area.</td>
</tr>
<tr>
<td>A0VREF</td>
<td>Supply for ports and analog functions of ADC0.</td>
</tr>
<tr>
<td>A1VREF</td>
<td>Supply for ports and analog functions of ADC1.</td>
</tr>
</tbody>
</table>

Additional one power supply for mainboard can be selected:

<table>
<thead>
<tr>
<th>Supply voltage</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIOF</td>
<td>IO supply voltage for components located on a connected mainboard.</td>
</tr>
</tbody>
</table>

- For each of the above voltages, the voltage source can be selected from Voltage1 (typ. 5.0V) or Voltage2 (typ. 3.3V) by the jumpers JP1 to JP6.

  Error! Not a valid link.
Chapter 5  Clock sources

Four external crystal oscillators for the device clock supply are provided with the board.

5.1.1  MainOsc

A crystal or ceramic resonator in the range of 8MHz to 24MHz can be mounted on socket X1.

A 8MHz, 16Mhz and 20MHz oscillator is supplied with the board.

5.1.2  SubOSC

An oscillator with a frequency of 32.768kHz is supplied with the board and can be soldered into the connector X2.
Chapter 6  Debug and Programming interface

For connection of the microcontroller debug and flash programming tools, the connector CN19 is provided.

The signal connection of the connector CN19 is shown in the picture below:

<table>
<thead>
<tr>
<th>CN19 pin</th>
<th>Device Port</th>
<th>Device signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>JP0_2</td>
<td>DCUTCK / LPDCLK</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>JP0_4</td>
<td>DCUTRST</td>
</tr>
<tr>
<td>4</td>
<td>FLMD0</td>
<td>FLMD0</td>
</tr>
<tr>
<td>5</td>
<td>JP0_1</td>
<td>DCUTDO / LPDO</td>
</tr>
<tr>
<td>6</td>
<td>P10_8*</td>
<td>FLMD1</td>
</tr>
<tr>
<td>7</td>
<td>JP0_0</td>
<td>DCUTDI / LPDI</td>
</tr>
<tr>
<td>8</td>
<td>‘Dbg_Voltage’</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>JP0_3</td>
<td>DCUTMS</td>
</tr>
<tr>
<td>10</td>
<td>JP0_6</td>
<td>EVTO</td>
</tr>
<tr>
<td>11</td>
<td>JP0_5</td>
<td>DCURDY / LPDCLKOUT</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>-</td>
</tr>
<tr>
<td>13</td>
<td>RESET</td>
<td>-</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>-</td>
</tr>
</tbody>
</table>

* In case of connecting a debug/programming tool to CN19, the pin header JP11 must be closed.

The ‘Dbg_Voltage’ (on CN19 pin 8) is monitored or supplied by the debug and flash programming tools. Therefore, it is necessary to select either Voltage1 (5V) or the Voltage2 (3.3V) by pin header JP10:

<table>
<thead>
<tr>
<th>JP10 pin</th>
<th>Selection for Dbg_Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>5V is selected</td>
</tr>
<tr>
<td>2-3</td>
<td>3.3V is selected</td>
</tr>
</tbody>
</table>

If the EVTO signal is used, a pull-up can be applied to that signal. To do so, close the JP11:

<table>
<thead>
<tr>
<th>JP11 pin</th>
<th>Pull-up for EVTO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>No pull-up is applied</td>
</tr>
<tr>
<td>Closed</td>
<td>Pull-up is selected</td>
</tr>
</tbody>
</table>
Chapter 7  Connectors for ports of device

Connection to each pin of the device is possible via the connectors CN5 to CN8.

Note : The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.1  Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

7.2  Connectors to Mainboard

Three connectors (CN1 to CN3) are available to connect the piggyback board to a mainboard.

The signal connection of each connector is described in the following tables:

7.2.1  Connector CN1

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When using this piggyback board in conjunction of R1L 144-pin device and the Y-RH850-X1X-MB-T1-Vx mainboard the following details must be noted:

On the Piggyback board the signals of P0_2 and P0_3 are connected the CN1 pins 30 and 28 for usage as CAN1Rx and CAN1Tx signals.

The ports P0_2 and P0_3 on the R1L 144-pin device do not carry those CAN1 signals, they are available (only) at ports P10_6 (CAN1RX) and P10_7 (CAN1TX).

**Applicable workaround / solutions:**

In order to use the CAN1 instance of the R1L device on the mainboard a manual wire connection must be made between the related pins of the device and pin headers on the mainboard. See the connection below for details:

<table>
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<th>CAN1 signals</th>
<th>Piggyback board</th>
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<td>CAN1Tx</td>
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</table>
Chapter 8 Other circuitry

8.1 Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

8.2 Mode Selection

The piggyback board gives the possibility to configure the following mode pins

- FLMD0 via jumper JP12
- FLMD1 via jumper JP13
- MODE0 via jumper JP14
- MODE1 via jumper JP15
- MODE2 via jumper JP16

To apply “High” or “Low” to the mode pins, the pins 1 and 2, or the pins 2 and 3 (if available) of the corresponding jumper must be closed, respectively.

Note: Pin 1 of all jumpers is marked by a small circle.

CAUTION: Be careful in configuration of mode related pins. Wrong configuration and operation of the device outside of its specification can cause irregular behaviour of the device and long term damage cannot be excluded. Be sure to check the corresponding User’s Manual for details, which modes are specified for the used device.

Note:
In the very most cases the ‘Normal operating mode’ of the device will be used. This mode is for execution of the user program. The on-chip debug functions also use this mode.
To select the ‘Normal operating mode’ of the device, the FLMD0 pin must be pulled low. To do so, close the pins 2-3 on the jumper JP25:

All other jumper related to the mode selection can be left open.

8.3 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins. Device pins P8_0 to P8_7 are connected to the even pins 2 to 16 of the pin header CN24, while the LEDs 1 to 8 are connected to the odd pins 1 to 15, respectively.

Thus the LEDs can be either connected to
- the device port pins P8_0 to P8_7 by closing the connection on CN24 using a jumper, or
- any device port pin by using the provided wire connections.
Chapter 9  Mechanical dimensions
Chapter 10 Schematic
Chapter 11 Revision History

The table provides information about the major changes of the document versions.

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<tr>
<th>Date</th>
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<td>1.00</td>
<td>Initial release</td>
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<tr>
<td>2018-05-17</td>
<td>1.10</td>
<td>Corrected table for the jumper configuration in chapter 3</td>
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<tr>
<td>2021-08-12</td>
<td>1.20</td>
<td>Added RH850/F1KM-S2 to the list of supported devices</td>
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Differences to the Y-RH850-F1X-144PIN-PB-T1-V2:

- Support for RH850/F1K, F1KM-S2 and F1KM-S4 devices.
- Added jumpers for mode selection.
- Added signal LEDs.
- EVTO signal added to the debug interface.
- Updated signal assignment of main board connectors CN1 to CN4.
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