User's Manual

32

RZ/T1 Group

Renesas Starter Kit+ User's Manual For e^2 studio

RENESAS MCU
Family / RZ/T1 Series

Renesas Electronics
www.renesas.com

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1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tool including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare hands.

EEDT-ST-004-10

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How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK+ hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK+ platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK+ and development environment can found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/T1H Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+ hardware.	RSK+RZT1 User's Manual	R20UT3242EG0100
Tutorial Manual	Provides a guide to setting up RSK environment, running sample code and debugging programs.	RSK+RZ/T1 Tutorial Manual	R20UT3243EG0100
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample, on a single A4 sheet.	RSK+RZT1 Quick Start Guide	R20UT3244EG0100
Schematics	Full detail circuit schematics of the RSK+.	RSK+RZT1 Schematics	R20UT3241EG0100
Hardware Manual	Provides technical details of the RZ/T1 microcontroller.	RZ/T1 Group User's Manual: Hardware	R01UH0483EJ0100

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	Bits per second
e^2 studio	Renesas Eclipse Embedded Studio Integrated Debugging Environment
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
I2C, IIC	Philips™ Inter-Integrated Circuit Connection Bus
IEBus	Inter Equipment Bus
IrDA	Infrared Data Association
I/O	Input/Output
IRQ	Interrupt Request
J-LINK	On-chip Debugger
KR	Key Return
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
MCU	Micro-controller Unit
MSB	Most Significant Bit
n/a	Not applicable
NC	Non-Connect
n/c	Not connected
PC	Personal Computer
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
QSPI	Quad Serial Programming Interface
RSK	Renesas Starter Kit
RSK+	Renesas Starter Kit + (denotes extra functionality over standard RSK)
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table of Contents

1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK+ hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialisation code

The RSK+ board contains all the circuitry required for microcontroller operation.

2. Power Supply

2.1 Requirements

This RSK+ is supplied with a SEGGER J-Link Lite debugger. This board is supplied with a 5V DC supply using a 5.0mm barrel power jack. The board can operate with a supply of up to 12V DC if required, with appropriate changes to jumper settings as detailed in Table 2.1.

Ensure to check the three pin JP2 jumper settings prior to connecting the power supply.

Details of the power supply requirements for the RSK+, and configuration are shown in Table 2.1 below. The default RSK+ power configuration is shown in **bold, blue text.**

JP2 Settings	
1-2	**7V - 12V**
2-3	5V
OPEN	No Power

Table 2.1: Main Power Supply Requirements

The main power supply connected to JP2 should supply a minimum of 5V to ensure full functionality.

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the 'Release' build of the example Tutorial software pre-programmed into the Renesas microcontroller. Please consult the 'Renesas Starter Kit Tutorial Manual' for further information of this example.

3. Board Layout

3.1 Component Layout

Figure 3.1 below shows the top component layout of the board.

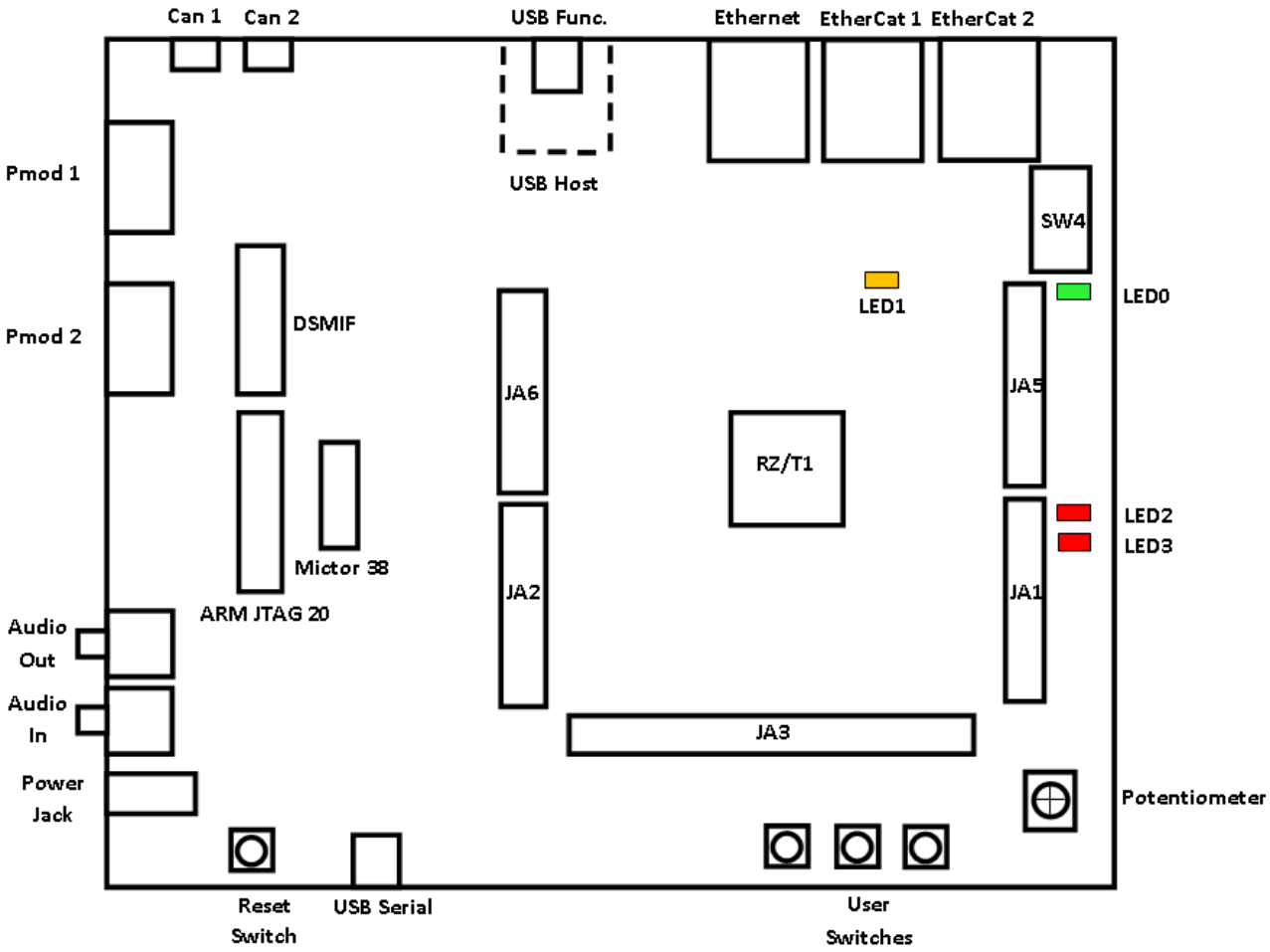


Figure 3.1: Board Layout

3.2 Board Dimensions

Figure 3.2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 0.1 inch grid for easy interfacing.

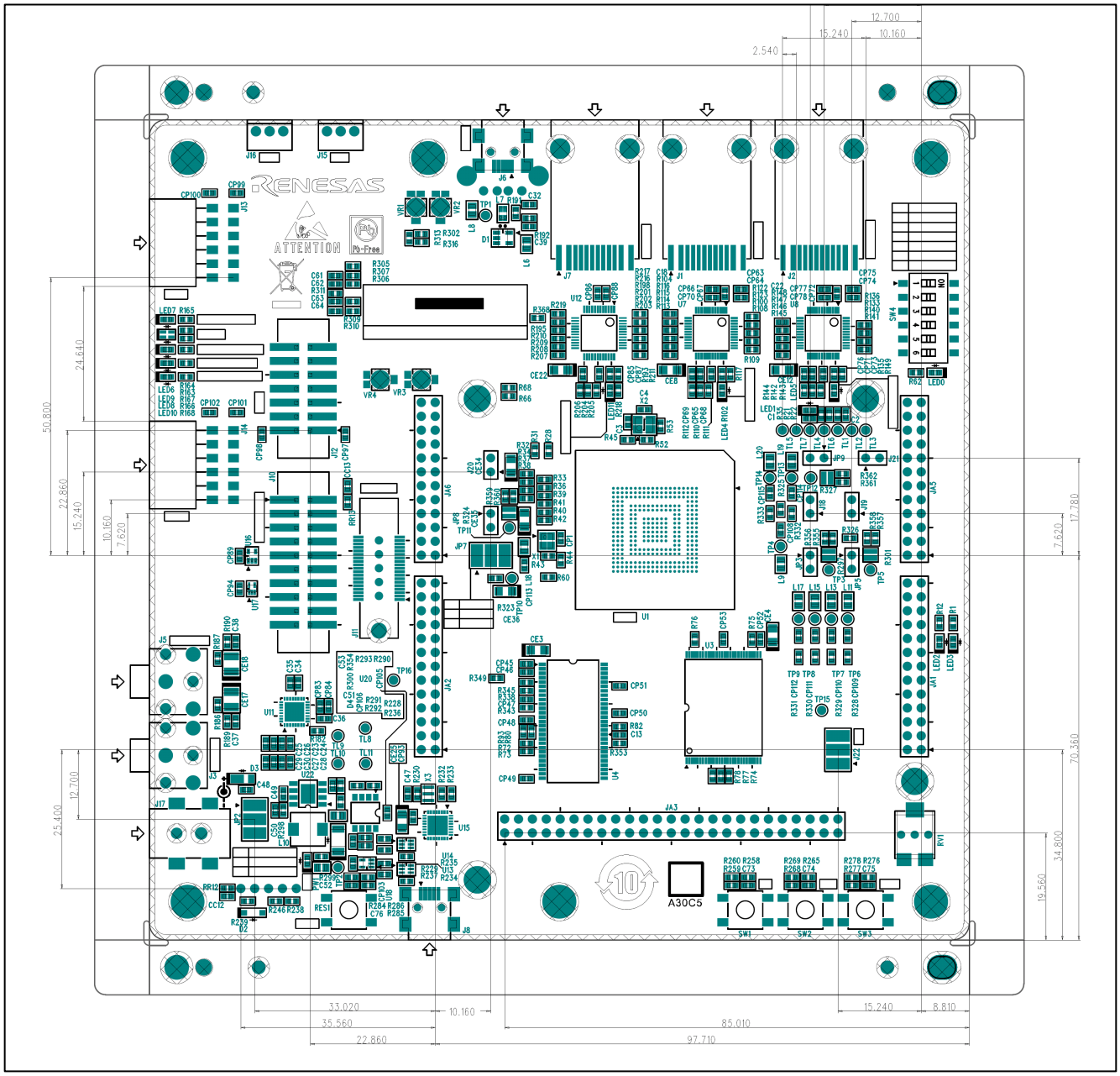


Figure 3.2: Board Dimensions

3.3 Component Placement

Figure 3.3 below shows placement of individual components on the top-side PCB. Figure 3.4 shows placement of individual components on the underside of the PCB. Component types and values can be looked up using the board schematics.

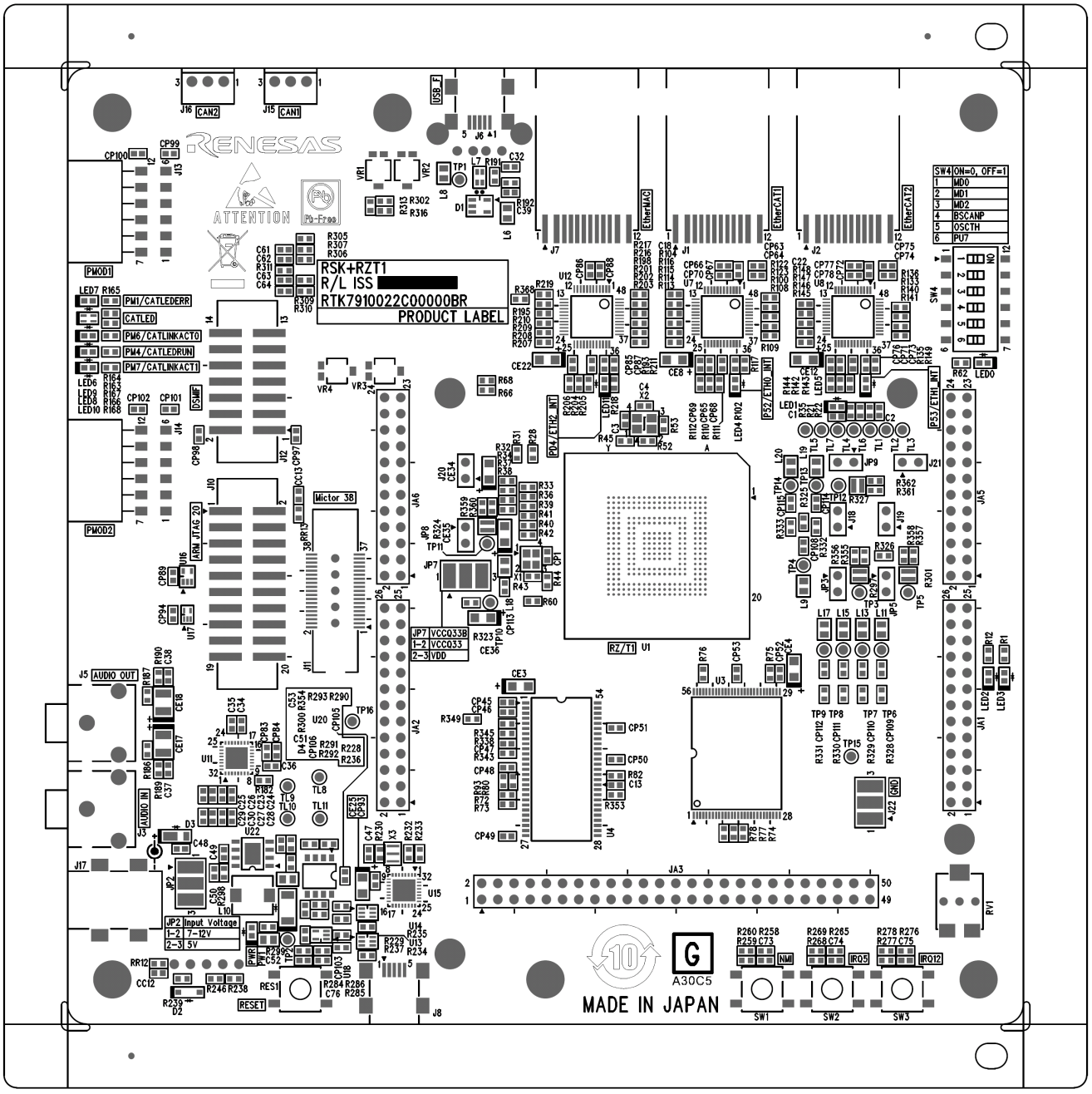


Figure 3.3: Top-Side Component Placement

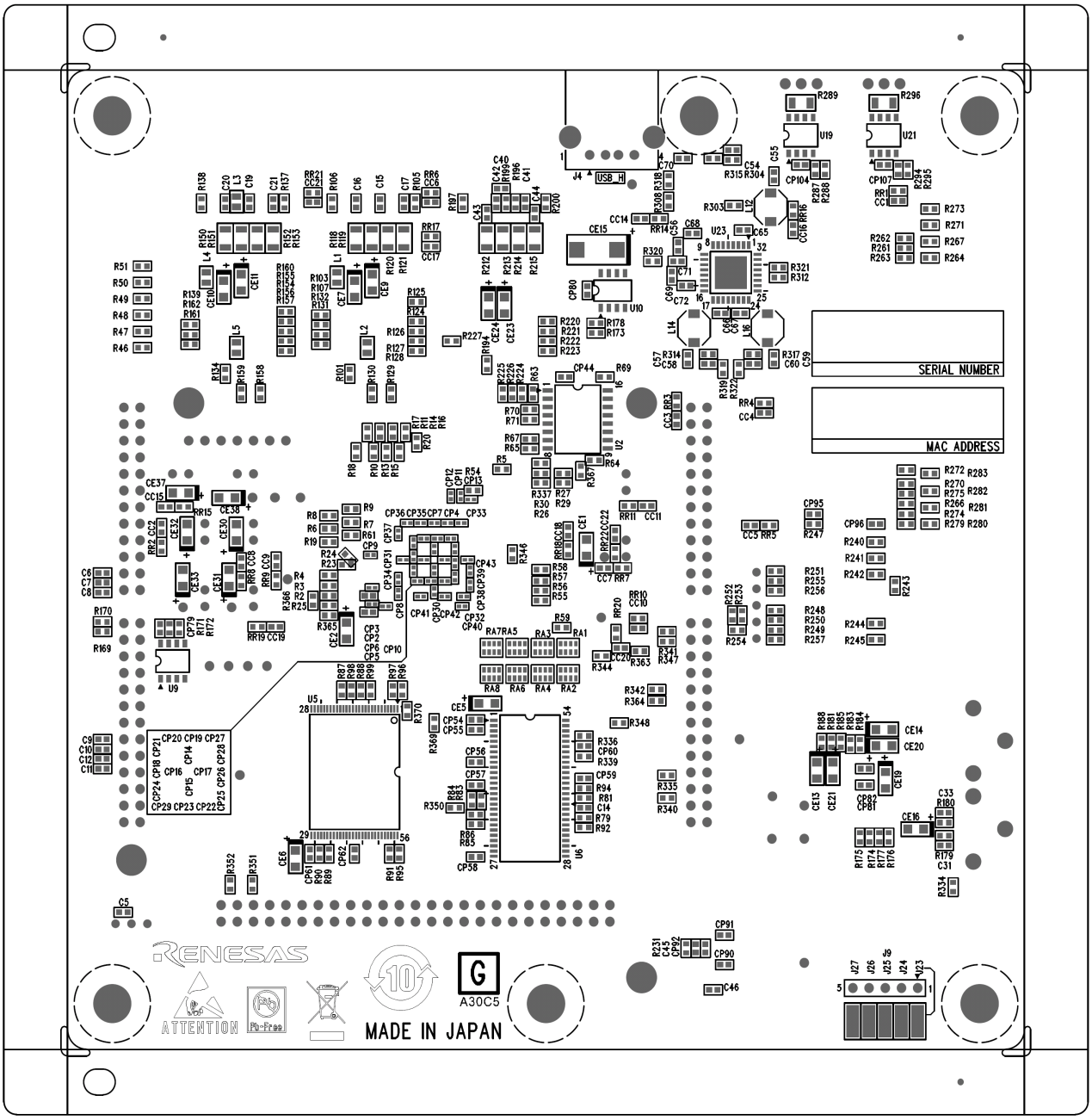


Figure 3.4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal RSK Connections

The diagram below shows the RSK board components and their connectivity to the MCU.

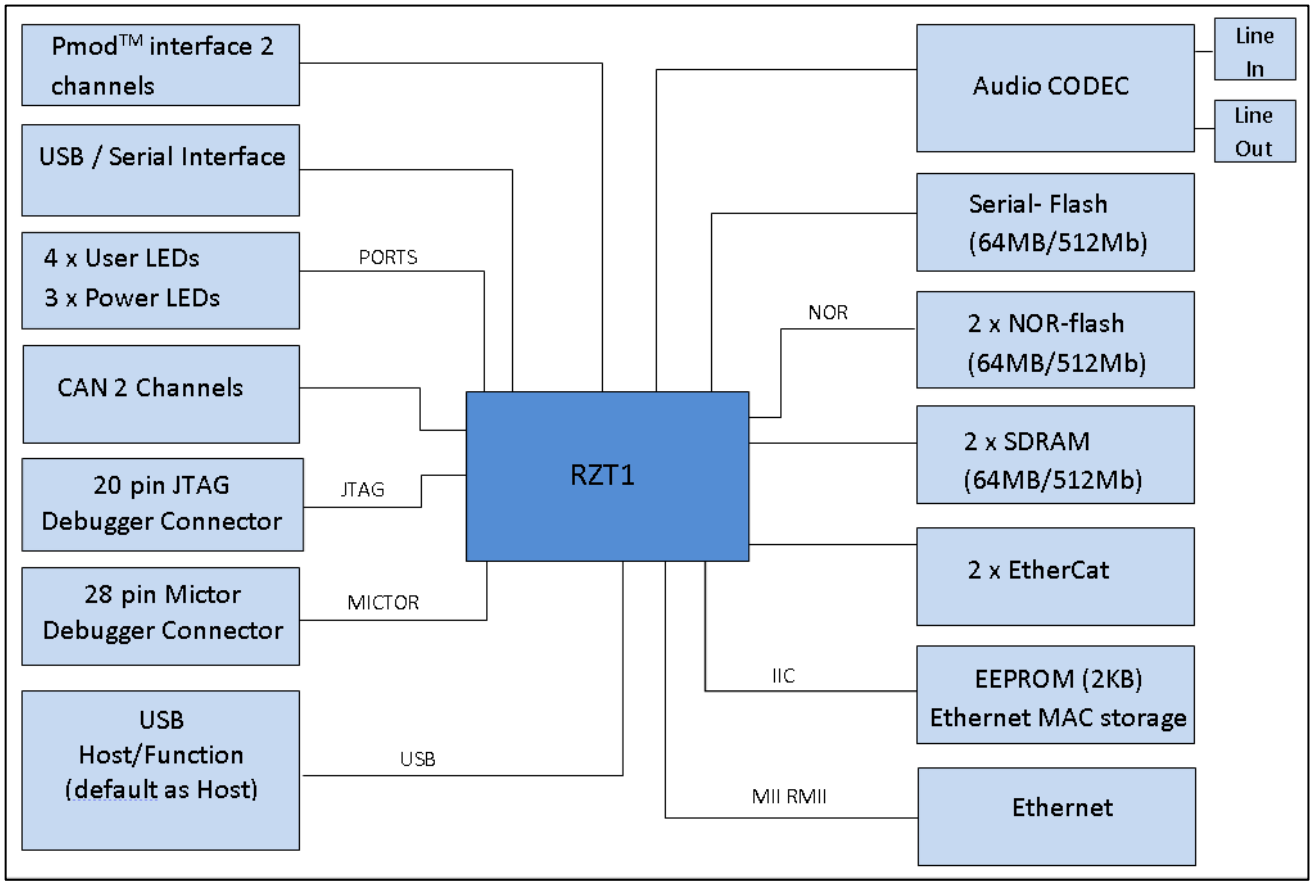


Figure 4.1: Internal RSK Block Diagram

4.2 Debugger Connections

The diagram below shows the connections between the RSK, SEGGER J-Link Lite debugger and the host PC.

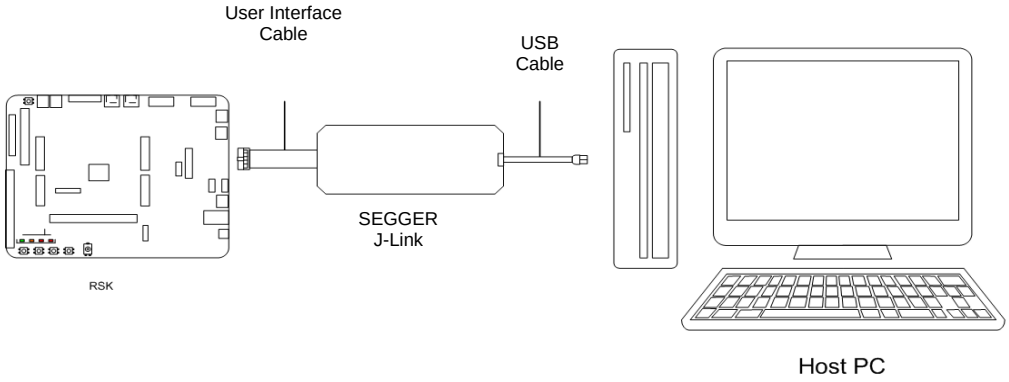


Figure 4.2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the RSK+ to generate a reset signal from the RES1 switch. Refer to the RZ/T1 hardware manual for details regarding the reset signal timing requirements, and the RSK+ schematics for information regarding the reset circuitry in use on the board.

5.2 Potentiometer

A single-turn potentiometer, RV1, is connected as a potential divider to analogue input pin number A13, Port AN007. The potentiometer can be used to create a voltage between AVCC0 and AVSS0.

The potentiometer is fitted to offer an easy method of supplying a variable analogue input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RZ/T1 Group Hardware Manual for further details.

5.3 Clock Circuit

Clock circuits are fitted to the RSK+ to generate the required clock signals to drive the MCU, and associated peripherals. Refer to the RZ/T1 Group Hardware Manual for details regarding the clock signal requirements, and the RSK+RZT1 board schematics for information regarding the clock circuitry in use on the RSK+. Details of the oscillators fitted to the board are listed in Table 5.1 below.

Crystal/Oscillator	Function	Default Placement	Frequency	Device Package
X1	Audio oscillator.	Fitted	11.2896MHz	NZ2520SD
X2	Main MCU oscillator.	Fitted	25.000MHz	NX3225GA
X3	USB oscillator	Fitted	12.000MHz	CSTCE12M0G52

Table 5.1: Oscillators

5.4 Switches

There are four switches located on the RSK+ board. The function of each switch and its connection is shown in Table 5.2. For further information regarding switch connectivity, refer to the RSK+RZT1 schematics.

Switch	Function	MCU	
		Port	Pin
RES1	Microcontroller reset.	RES#	N5
SW1	Connects to NMI.	P35	H3
SW2	Connects to IRQ5.	PN5	W3
SW3	Connects to IRQ12/ADTRG0#.	P44	W15

Table 5.2: Switch Connections

5.5 CAN

There are two CAN channels which are connected to the MCU as listed in Table 5.3: CAN Connection.

CAN Signal	Function	Port
CTXD0	CAN Channel 0 Transmit	P67/CTXD0
CRXD0	CAN Channel 0 Receive	PC6/CRXD0
CTXD1	CAN Channel 1 Transmit	P66/CTXD1
CRXD1	CAN Channel 1 Receive	PC7/CRXD1

Table 5.3: CAN Connection

5.6 Universal Serial Bus (USB)

This RSK+ board is fitted with one channel of USB. The channel can operate as either a host or as a function device. There is no default configuration, the user must only operate the channel as either a host or function device. Do **NOT** connect to both USB ports, J4 and J6, at the same time. The signal connections to the MCU for Host and function are detailed in Table 5.4 and Table 5.5 respectively.

Note: Default settings are shown in **bold**, **blue** text

USB Signal	Function	MCU	
		Port	Pin
D+	Positive differential data signal.	USB_DP	R1
D-	Negative differential data signal.	USB_DM	R2
USB_VBUSEN	Cable monitor pin.	USB_VBUSEN	12

Table 5.4: Host (J4) Module MCU Connections

USB Signal	Function	MCU	
		Port	Pin
D+	Positive differential data signal.	USB_DP	R1
D-	Negative differential data signal.	USB_DM	R2
P31/USB_VBUSIN	Cable monitor pin.	USB_VBUSEN	12

Table 5.5: Function (J6) Module MCU Connections

5.7 Ethernet, EtherCAT & EEPROM

This RSK+ board is fitted with an Ethernet connection. The connections from the Ethernet driver IC, U12, are detailed in Table 5.6. Refer to the RZ/T1 board schematics for further information.

Signal	MCU	
	Port	Pin
MII2_MDC	PU4	F5
MII2_MDIO	PU5	G5
ETH2_CRS	PU2	C3
ETH2_COL	PU3	D3
ETH2_RXC	PU1	E3
ETH2_RXER	PU0	E5
ETH2_RXDV	PL7	C4
RXD0/CONFIG2	PL3	F8
ETH2_RXD1	PL4	E7
ETH2_RXD2	PL5	C5
ETH2_RXD3	PL6	E6
ETH2_TXC	PL1	C4
ETH2_TXEN	PL2	E2
ETH2_TXD0	PL0	E9
ETH2_TXD1	PK5	F10
ETH2_TXD2	PK7	E10
ETH2_TXD3	PK6	E11
ETH2_TXER	PK4	F11
PHYRESETOUT2#	PD3	F14
CLKOUT25M2	PM0	G6

Table 5.6: Ethernet Connection

This RSK+ board is fitted with two EtherCAT drivers, EtherCAT1 and EtherCAT2, placed on U7 and U8 respectively, the connections are detailed in **Table 5.7** and **Table 5.8**. Refer to the RZ/T1 board schematics for further information.

Signal	MCU	
	Port	Pin
ETH_MDC	PB6	C6
ETH_MDIO	PB5	B6
ETH0_CRS	P83	F2
ETH0_COL	P84	E1
ETH0_RXC	PC3	B3
ETH0_RXER	P81	D1
ETH0_RXDV	P80	D2
ETH0_RXD0	PJ4	C10
ETH0_RXD1	PJ5	B7
ETH0_RXD2	PJ6	C2
ETH0_RXD3	PJ7	C1
ETH0_TXC	PC2	A2
ETH0_TXEN	P82	E2
ETH0_TXD0	PJ3	E12
ETH0_TXD1	PJ2	C11
ETH0_TXD2	PJ1	A4
ETH0_TXD3	PJ0	B5
PHYRESETOUT#	P17	A19
CLKOUT25M0	P85	F3

Table 5.7: EtherCAT1 Connection

Signal	MCU	
	Port	Pin
ETH_MDC	PB6	C6
ETH_MDIO	PB5	B6
ETH1_CRS	PB3	C7
ETH1_COL	PB4	A6
ETH1_RXC	PB2	B7
ETH1_RXER	PB1	C8
ETH1_RXDV	PB0	A7
ETH1_RXD0	PF6	A9
ETH1_RXD1	PB7	B9
ETH1_RXD2	PC0	A8
ETH1_RXD3	PC1	B8
ETH1_TXC	P87	C10
ETH1_TXEN	PF5	C9
ETH1_TXD0	P86	B10
ETH1_TXD1	PD7	B11
ETH1_TXD2	PD6	C11
ETH1_TXD3	PD5	E12
PHYRESETOUT#	P17	A19
CLKOUT25M1	P54	A11

Table 5.8: EtherCAT2 Connection

A 2KByte EEPROM is fitted in order to store the MAC address for the Ethernet connection. This can be accessed with address 0xA0. This EEPROM responds to all addresses starting with ‘0xA-’, where ‘-‘ is a value from 0-7. Therefore, do not connect another IIC device with an address starting with ‘0xA-’ to IIC channel 0. Connection details are described in Table 5.9 below.

I^2C Signal	Function	MCU	
		Port	Pin
SCL0	Serial Data Line	PC4	F1
SDA0	Clock Line	PC5	G2

Table 5.9: EEPROM Connection on I^2C Channel 0

5.8 LEDs

There are twelve LEDs on the RSK. The function of each LED, its colour and connection are shown in Table 5.10.

LED	Colour	Function	MCU	
			Port	Pin
PW1	Green	Indicates the status of the power connected to the board.	---	---
LED0	Green	User operated LED	PF7	A5
LED1	Orange	User operated LED	P56	E13
LED2	Red	User operated LED.	P77	K16
LED3	Red	User operated LED.	PA0	J18
LED4	Green	Input the Ethernet PHY interrupt request signal.	P52	B12
LED5	Green	Input the Ethernet PHY interrupt request signal.	P53	C12
LED6	Red	EtherCAT Error LED port	PM1	H2
LED6	Green	EtherCAT Dual-color State LED port	PM5	A4
LED7	Green	EtherCAT Error LED port	PM1	H2
LED8	Green	EtherCAT RUN LED port	PM4	K3
LED9	Green	EtherCAT link / Activity LED port (port 0)	PM6	F2
LED10	Green	EtherCAT link / Activity LED port (port 1)	PM7	E1
LED11	Green	Input the Ethernet PHY interrupt request signal.	PD4	E14

Table 5.10: LED Connections

5.9 Audio

The RSK+ board provides audio input via a 3.5mm Stereo jack (J3), and audio output via 3.5mm stereo jack (J5). It also incorporates an audio codec device, U11 which is linked to the MCU via the signals described in Table 5.11

Signal	Function	MCU	
		Port	Pin
MCLK	Clock Line	---	---
SSISCK0	SSISCK0 Digital Audio Bit Clock	PS1	L20
SSITXD0	Digital Audio Serial Data DAC Input	PS4	Y18
SSIWS0	Digital Audio Left-Right Clock IO	PS2	K18
SSIRXD0	Digital Audio Serial Data ADC Output	PS3	L19
RSPCK1	Clock line for the data line	PN3	R8
MOSI1	Data Line	PN2	PG4

Table 5.11: Audio Codec Connections

5.10 USB Serial Port

A USB serial port implemented in another Renesas low power microcontroller, RL78/G1C (U15), is fitted on the RSK+ to the microcontroller Serial Communications Interface with FIFO (SCIF) module. Multiple options are provided to allow re-use of the serial interface.

Connections between the USB to Serial converter and the microcontroller are listed in Table 5.12 below.

Signal Name	Function	MCU	
		Port	Pin
TXD2	External SCI Transmit Signal	P91	F19
RXD2	External SCI Receive Signal.	P92	F18
CTS2	Clear To Send	P95	D20
RTS2	Request to Send	P94	E19

Table 5.12: Serial Port Connections

When the RSK+ is first connected to a PC running Windows with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in Figure 5.1. The exact messages may vary depending upon operating system.

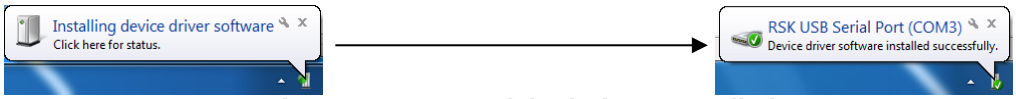


Figure 5.1 USB-Serial Windows Installation message

5.10.1 Reading the Virtual COM Port Number

In order for the PC to be able to communicate with the RSK+ board via the USB virtual COM port, the correct COM port number must be determined. If the COM port number is not known, follow this process:

1. Connect the PC to the serial/USB port.
2. On the PC, go to Start à Control Panel à Device Manager. Go to the “Ports (COM & LPT)” section and the COM port should be listed there. To verify the correct port, the USB cable can be disconnected and re-connected to show the COM port appearing and disappearing.

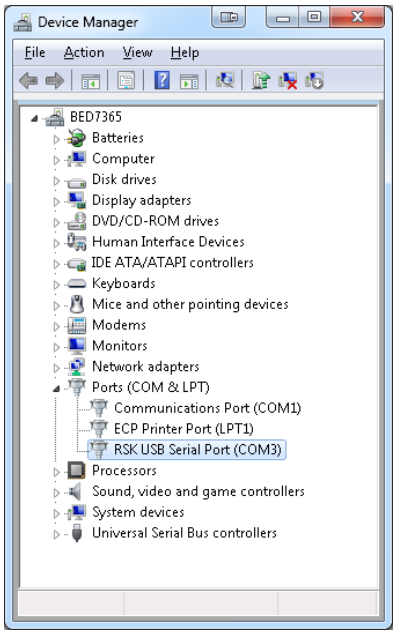


Figure 5.2 Device Manager Ports

5.10.2 Changing the Virtual COM Port Number

Some PC applications will only work with particular COM port numbers. COM port numbers for the RSK+ serial/USB are assigned automatically at the time of first connection to the PC. It is possible to assign a different value manually. The procedure to do this is as follows:

1. Right-click the USB-Serial port in device manager and select “Properties”

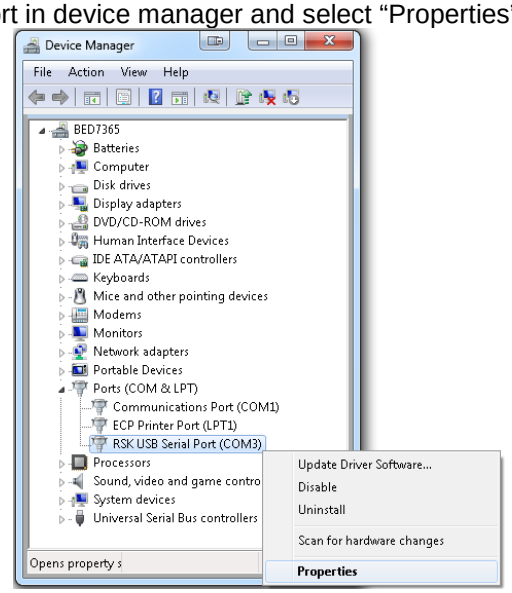


Figure 5.3 Device Manager Port Properties

2. Select the “Port Settings” tab and click “Advanced…”

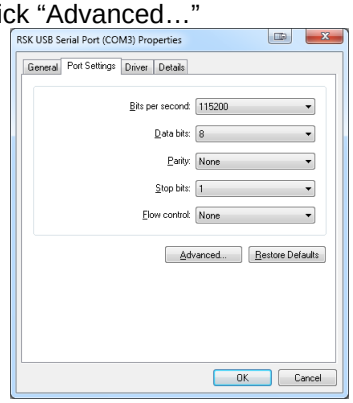


Figure 5.4 Device Manager Port Settings

3. Select the new COM port from the drop down list. Bear in mind that the “in use” label on various ports listed may not actually mean that that port is in use at this current point in time.

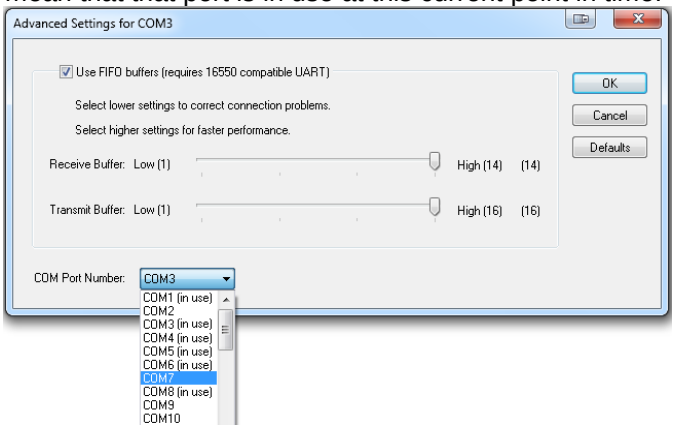


Figure 5.5 Device Manager Advanced Port Settings

4. Click OK to complete the process.

5.11 Pmod™ Module Connectors

A Pmod™ Compatible debug LCD module is supplied with the RSK+, and should be connected to the PMOD1 or PMOD2 header.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible header uses a SPI interface. Some RSKs will be provided with a monochrome display, others will have a colour display. Code for the appropriate display will be included in the product software support. Connection information for the Digilent Pmod™ Compatible header is provided in Table 5.13 for Pmod™ connector 1 and Table 5.14 for Pmod™ connector 2.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011.

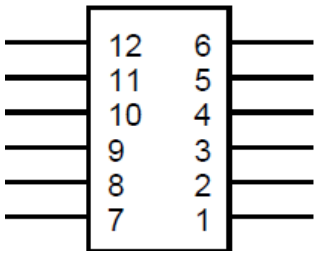


Figure 5.6: Digilent Pmod™ Compatible Header Pin Numbering

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SSL10	PN0	R5	7	P66	P66	Y3
2	MOSI1	PN2	R6	8	P67	P67	Y2
3	MISO1	PN1	U3	9	P76	P76	K18
4	RSPCK1	PN3	V3	10	P74	P74	L20
5	GROUND	-	-	11	GROUND	-	-
6	D3.3v	-	-	12	D3.3v	-	-

Table 5.13: PMOD1 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SSL11	PN4	V4	7	P50	P50	F13
2	MOSI1	PN2	R6	8	P51	P51	C13
3	MISO1	PN1	U3	9	PM2	PM2	J3
4	RSPCK1	PN3	V3	10	PM3	PM3	J2
5	GROUND	-	-	11	GROUND	-	-
6	D3.3V	-	-	12	D3.3v	-	-

Table 5.14: PMOD2 Header Connections

5.12 External Memory Buses

The RSK+ is fitted with external memories accessed using address and data buses.
The connections for the address and data buses are shown in Table 5.15 and Table 5.16, respectively.

Signal Name	Function	MCU	
		Port	Pin
A25	Address line 25	P97	E18
A24	Address line 24	PK3	G15
A23	Address line 23	PK2	F15
A22	Address line 22	PT7	J19
A21	Address line 21	PT6	J20
A20	Address line 20	P27	R14
A19	Address line 19	P26	T14
A18	Address line 18	P25	Y14
A17	Address line 17	P20	V12
A16	Address line 16	PH7	V11
A15	Address line 15	PH6	R12
A14	Address line 14	PH5	T12
A13	Address line 13	PH4	R11
A12	Address line 12	PH3	T10
A11	Address line 11	PH2	R10
A10	Address line 10	PH1	V10
A9	Address line 9	PH0	V9
A8	Address line 8	PG7	R9
A7	Address line 7	PG6	T9
A6	Address line 6	PG5	V8
A5	Address line 5	PG4	V7
A4	Address line 4	PG3	T8
A3	Address line 3	PG2	R8
A2	Address line 2	PG1	V6
A1	Address line 1	PG0	R7

Table 5.15: Address Bus

Signal Name	Function	MCU	
		Port	Pin
D15	Data line 15	PE7	L16
D14	Data line 14	PE6	M16
D13	Data line 13	PE5	N18
D12	Data line 12	PE4	N16
D11	Data line 11	PE3	P18
D10	Data line 10	PE2	N15
D9	Data line 9	PE1	T20
D8	Data line 8	PE0	T19
D7	Data line 7	P07	P16
D6	Data line 6	P06	P15
D5	Data line 5	P05	V18
D4	Data line 4	P04	U19
D3	Data line 3	P03	U20
D2	Data line 2	P02	V20
D1	Data line 1	P01	V19
D0	Data line 0	P00	U18

Table 5.16: Data Bus

5.13 NOR flash Memory

There are two NOR-flash (64MB) devices, U3 & U5. These device share the address and data buses, A1 - A25 and D0 - D15, listed in section 5.12.

U3 is controlled by chip select CS0 and U5 is controlled by chip select CS1. The connections for NOR application is shown in Table 5.17.

Signal Name	Function	MCU	
		Port	Pin
P21/CS0	Chip select for NOR-flash 1.	P21	V13
PD1/CS1	Chip select for NOR-flash 2.	PD1	E16
P22/RD	Read enable.	P22	W14
WE0/DQMLL	Write enable.	P36	T7
RES#	Reset*	RES#	RES#
RSTOUT	Reset*	RSTOUT#	RSTOUT#

Table 5.17: NOR Flash control signals

* RES# is connected by default. Do not connect both signals at the same time.

5.14 SDRAM

There are two SDRAM (64MB) devices, U4 & U6. These device share the address and data buses, A1 – A15 and D0 - D15, listed in section 5.12. U4 is controlled by chip select CS2 and U6 is controlled by chip select CS3.

Control signals for the SDRAMs are shown in Table 5.18.

Signal Name	Function	MCU	
		Port	Pin
P45 (CS2	Chip select for U4.	P45	V15
PT4/CS3	Chip select for U6.	PT4	M19
P90/RAS	Row access Strobe	P90	F16
PK0/CAS	Column access strobe	PK0	H19
P24/RDWR	Read/ Write operation	P24	W13
P37/DQMLU	Outputs the data mask enable signal to D7 to D0 when SDRAM is connected.	P37	T6
P36/WE0/DQMLL	Outputs the data mask enable signal to D15 to D8 when SDRAM is connected.	P36	T7
P46/CKE	Clock Enable	P46	V16
CKIO_SD1	Clock Line	CKIO	Y19

Table 5.18: SDRAM control signals

5.15 Quad Serial flash Memory

The RSK+ board provides one 64 MByte Serial Flash memory, U8, which connects to the RZ/T1 MCU via the SPI Multi I/O Bus Controller. Signal Connections are detailed in Table 5.19 below.

Signal Name	Function	MCU	
		Port	Pin
P62/SPBCLK	Clock Line.	P62	W1
P60/SPBSSL	Slave select for U2.	P60	U1
P63/SPBMO/SPIBO0	Master transmit data/data 0 I/O pins	P63	U2
P64/SPBMI/SPBIO1	Master input data/data 1 I/O pins	P64	V2
P65/SPBIO2	Data 2, data 3 I/O pins	P65	W2
P61/SPNIO3	Data 2, data 3 I/O pins	P61	V1
RES#	Reset.	RES#	N5

Table 5.19: QSPI control signals

6. Configuration

6.1 Modifying the RSK

This section lists the option links that are used to modify the way RSK+ operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers.

Please note that some signals are directly shared between different devices and connectors fitted on the RSK+ and are not selectable via option links. Ensure to correctly configure the MCU pins which these signals are connected to in the user application software.

When removing soldered components, always ensure that the RSK is not exposed to a soldering iron for intervals greater than **five** seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to RZ/T1 Group Hardware Manual and RSK+RZT1 schematics for further information.

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. Refer to the component placement diagram (Figure 3.3, Figure 3.4) to locate the option links and jumpers. **Bold, blue text** indicates the default configuration that the RSK is supplied with.

6.1.1 Switches, Potentiometer and LED

Table **6.1** details the option links associated with the user switches and pot.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
SW1	P35	H3	P35	**R260**	---	JA2 PIN 3	R340	---
SW2	PN5	W3	PN5	**R269**	---	JA2 Pin23	R348	R347 R349
SW3	P44	W15	P44	**R278**	---	JA2 PIN 7	R335	R336
POT	AN007	A13	AN007	**---**	---	JA5 PIN 4	---	---

Table 6.1: Option Link configuration for user switches, potentiometer and LEDs

Switch bank SW4 is used to control the boot options. Please refer to section 6.2 MCU Boot and Oscillator Configuration on page 34 for further information.

6.1.2 SDRAM

Table **6.2** details the option links associated with the SDRAM.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
SDRAM	P45	V15	P45/CS2	**R73**	R174	---	---	---
	M19	H1	PT4/ CS3	**R86**	R18	JA3 PIN 45	R350	**R352**

Table 6.2: Option Link configuration for SDRAM

6.1.3 NOR Flash

Table 6.3 details the option links associated with the NOR flash.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
Reset	RES#	N5	RES#	**R77**	R78	JA2 Pin 1	**---**	---
	RSTOUT#	N3	RSTOUT#	R78	**R77**	---	**---**	---

Table 6.3: Option Link configuration for NOR flash

6.1.4 Quad Serial Peripheral Flash

Table 6.4 details the option links associated with the Serial flash.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
Reset	RES#	N5	RES#	**R70**	R71	JA2 Pin 1	**---**	---
	RSTOUT#	N3	RSTOUT#	R71	**R70**	---	**---**	---

Table 6.4: Option Link configuration for QSPI flash

6.1.5 CAN

Table **6.5** details the option links associated with the CAN interface.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
	PC6	T5	PC6/CRXD0	**R288**	---	JA5 Pin6	---	---
	PC7	V5	PC7/CRXD1	**R295**	---	JA5 Pin8	---	---

Table 6.5: Option Link configuration for CAN

6.1.6 Ethernet

Table **6.6** details the option links associated with the Ethernet Functionality.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
Ethernet	PD3	F14	PD3/PHYRESET OUT2#	**R216**	R217	---	---	---
	RES#	N5	RES#	R217	**R16**	JA2 Pin1	---	---

Table 6.6: Option Link configuration for Ethernet

6.1.7 USB / Serial

Table **6.7** details the option links associated with the USB/Serial Interface.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
USB/Serial	P95	D20	P95/MTCLKA	R234	R235	JA2 Pin 25	---	---
	P94	E19	P94/MTCLKB	R235	R234	JA2 Pin26	---	---

Table 6.7: Option Link configuration for USB/Serial

6.1.8 Pmod™ Interfaces

Table **6.8** details the option links associated with the Pmod™ Interfaces.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
PMOD2	P50	F13	P50/IRQ8	R365	---	---	---	---
	P51	C13	P51	R366	---	---	---	---

Table 6.8: Option Link configuration for PMOD

6.2 Power Supply Configuration

Power to the RSK+RZT1 board should be applied to connector J17, from a 5mm diameter centre positive plug, at either 5V DC or 12V DC.
The header JP2 is used to select operation from a 12V or 5V supply.

It is essential that if a 12V supply is used that pins 2 and 3 of JP2 are ***NOT*** shorted otherwise an overvoltage will be applied to the MCU and associated devices, resulting in the likely destruction of the whole board.

Table 6.9 describes the jumper settings for the JP2 header

JP2 Pins	Input Voltage Setting
1 - 2	**7V - 12V**
2 - 3	**5V****
** **Do NOT connect a 12V input source to the RSK+ when the JP2 jumper is set to short pins 2-3**	

Table 6.9: JP2 Header Configuration

The RSK+ includes allows for power consumption measurements via jumpers JP8 and JP3. JP8 allows measurement for the MCU's core power and JP3 for the MCU's I/O port pin power.

In order to use these functions, it is necessary to power down the RSK+ and remove the option links listed in the Table 6.10.

JP8	MCU Core Current Measurement
Remove R324 and connect an ammeter to JP8 to measure MCU core current.	
JP3	**MCU Port Pins Current Measurement**
Remove R297 and connect an ammeter to JP3 to measure MCU port pin current.	

Table 6.10: MCU Current Measurement Headers

6.3 Jumper Link Configuration

Table 6.11 describes the jumper link option configurations available on the RSK+RZT1 board. These configurations should be carried out while the board is powered off.

JP2	**System Power Input Selector**
Jumper Position	
1 - 2	2 - 3
7V – 12V	5V**
** Do NOT connect a 12V input source to the RSK+ when JP2 pins 2-3 are shorted.	
JP3	**VCCQ33 (MCU I/O pins) Power Measurement**
Remove R297 and connect an ammeter across JP3 for MCU I/O pins power consumption measurements.	
R355	R356
D3.3V Connected to VCCQ33	ExD3.3V Connected to VCCQ33
Do Not fit R355 and R356 at the same time	
JP5	**AVCC (12-bit A/D Converters) Analog Power Measurement**
Remove R301 and connect an ammeter across JP5 for A/D converters' power consumption measurements.	
R357	R358
A3.3V Connected to AVCC	ExA3.3V Connected to AVCC
Do Not fit R357 and R358 at the same time	
JP7	**MCU I/O Pin Power Selector**
Jumper Position	
1-2	2-3
VDD connected to VCCQ33B	VCCQ33 connected to VCCQ33B
VDD = 1.2V and VCCQ33 = 3.3V	
JP8	**VDD (MCU Core) Power Measurement**
Remove R324, short JP7 pins 2-3 and connect an ammeter across JP8 for MCU Core power consumption measurements.	
R359	R360
D1.2V Connected to VDD	ExD1.2V Connected to VDD
Short JP7 pins 2 and 3 if MCU Core power measurement is required	
Do Not fit R359 and R360 at the same time	
JP9	**PLL Power Measurement**
Remove R327 and connect an ammeter across JP9 for PLL power consumption measurements.	
R361	R362
A1.2V Connected to AVDD	ExA1.2V Connected to AVDD
Do Not fit R361 and R362 at the same time	

Table 6.11: Jumper Option descriptions

6.4 MCU Boot and Oscillator Configuration

The six-way DIP switch, SW4 provides some configuration options for the RZ/T1 MCU. Switches SW4.1, SW4.2 and SW4.3 are used to set the boot mode of the RZ/T1. **Table 6.12** provides details of the available modes and the corresponding switch settings. Due to pull-up resistors in the circuit, a “1” is produced when the corresponding switch position is OFF, and a “0” is produced when it is ON

MD_BOOT0 SW4-1	MD_BOOT1 SW6-2	MD_BOOT2 SW6-3	Boot Mode
ON (0)	ON	ON	SPI boot mode (Serial flash) Boots a program from a serial flash memory connected to the SPI multi-I/O bus space.
ON	OFF	ON	16-bit bus boot mode (CS0-space 16-bit booting) Boots a program from a NOR flash memory (bus width: 16 bits) connected to the CS0 space.
ON	**OFF**	**OFF**	32-bit bus boot mode (CS0-space 32-bit booting) Boots a program from a NOR flash memory (bus width: 32 bits) connected to the CS0 space.
Other than above			Reserved (Setting Prohibited)

Table 6.12: MCU Boot Modes

SW4-4	Clock Signal Source
ON	CoreSight Debugger Boundary Scan Enabled
OFF	CoreSight Debugger Boundary Scan Disabled

Table 6.13: Clock Signal Source

SW4-5	Clock input mode select signal
ON	When a crystal resonator is connected, it should be driven low.
OFF	When an external clock is input, this pin should be driven high.

Table 6.14: Clock Input Mode Signal Select

Switch 4.6 this is used for test purposes only (default is OFF = HIGH due to pull-ups).

7. Headers

7.1 Application Headers

This RSK+ is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.
The following tables provide details of the pin connections of these headers. Some pins will require link resistors to be fitted in order to make the connection to the specified MCU pin. These resistors are also documented in the tables, highlighted in **bold, blue** if they are fitted by default, or normal text if they are not fitted as standard.

Table 7.1 below lists the connections of the application header, JA1.

Application Header JA1, JA1-B							
Pin	**Header Name**	**MCU Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Pin**	**Link Required**
1	D5V	---	---	2	0V	---	---
3	D3.3V	---	---	4	0V	---	---
5	A3.3V	---	---	6	AVSS	---	---
7	A3.3V	---	---	8	P17	P17	---
9	AN000	AN000	---	10	AN001	AN001	---
11	AN002	AN002	---	12	AN003	AN003	---
13	N/C	N/C		14	N/C	N/C	---
15	PT3	PT3	---	16	PT2	PT2	---
17	PT1	PT1	---	18	PT0	PT0	---
19	PS7	PS7	---	20	PS6	PS6	---
21	PA0	PA0	---	22	P77	P77	---
23	P75	P75	---	24	N/C	N/C	---
25	PC5	PC5	---	26	PC4	PC4	---

Table 7.1: Application Header JA1 Connections

Table 7.2 below lists the connections of the application header, JA2.

Application Header JA2, JA2-B							
Pin	**Header Name**	**MCU Port, Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Port, Pin**	**Link Required**
1	RES#	RES#	---	2	X1	X1	---
3	P35	P35	R340	4	0V	0V	---
5	ERROROUT	ERROROUT	---	6	P40	P40	---
7	P44	P44	R335				---
	D14	D14	R336	8	P42	P42	
9	P32	P32	R337				---
	D12	D12	R338	10	P41	P41	---
11	D4	D4	R339	12	TP16	---	---
13	P16	P16	---	14	P15	P15	---
15	P14	P14	---	16	P13	P13	---
17	P12	P12	---	18	P11	P11	---
19	PA2	PA2	---	20	PA6	PA6	---
21	PA1	PA1	---	22	PA7	PA7	---
23	P93	P93	**R347**	24	P96	P96	---
25	P95	P95	---	26	P94	P94	---

Table 7.2: Application Header JA2 Connections

Table 7.3 below lists the connections of the application header, JA3.

Application Header JA3, JA3-B							
Pin	**Header Name**	**MCU Port, Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Port, Pin**	**Link Required**
1	A0	A0	R378	2	A1	A1	---
3	A2	A2	---	4	A3	A3	---
5	A4	A4	---	6	A5	A5	---
7	A6	A6	---	8	A7	A7	---
9	A8	A8	---	10	A9	A9	---
11	A10	A10	---	12	A11	A11	---
13	A12	A12	---	14	A13	A13	---
15	A14	A14	---	16	A15	A15	---
17	D0	D0	---	18	D1	D1	---
19	D2	D2	---	20	D3	D3	---
21	D4	D4	---	22	D5	D5	---
23	D6	D6	---	24	D7	D7	---
25	P22	P22	---	26	P24	P24	---
27	PD0	PD0	---	28	PK1	PK1	---
29	D8	D8	---	30	D9	D9	---
31	D10	D10	---	32	D11	D11	---
33	D12	D12	---	34	D13	D13	---
35	D14	D14	---	36	D15	D15	---
37	A16	A16	---	38	A17	A17	---
39	A18	A18	---	40	A19	A19	---
41	A20	A20	---	42	A21	A21	---
43	A22	A22	---	44	CKIO_CN	CKIO_CN	---
45	PT4	PT4	R350		P47	P47	**R351**
	PD2	PD2	**R352**	46	P46	P46	R353
47	P37	P37	---	48	P36	P36	---
49	PK0	PK0	**R369**	50	P90	P90	**R370**

Table 7.3: Application Header JA3 Connections

Table 7.4 below lists the connections of the application header, JA5.

Application Header JA5, JA5-B							
Pin	**Header Name**	**MCU Port, Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Port, Pin**	**Link Required**
1	AN004	AN004	**---**	2	AN005	---	---
3	AN006	AN006	---	4	AN007	---	---
5	P67	P67	**R367**	6	PC6	---	---
7	P66	P66	**R368**	8	PC7	---	---
9	P73	P73	---	10	P70	---	---
11	N/C	---	---	12	N/C	---	---
13	N/C	---	---	14	N/C	---	---
15	N/C	---	---	16	N/C	---	---
17	N/C	---	---	18	N/C	---	---
19	N/C	---	---	20	N/C	---	---
21	N/C	---	---	22	N/C	---	---
23	N/C	---	---	24	N/C	---	---

Table 7.4: Application Header JA5 Connections

Table 7.5 below lists the connections of the application header, JA6.

Application Header JA6, JA6-B							
Pin	**Header Name**	**MCU Port, Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Port, Pin**	**Link Required**
1	PA2	PA2	---	2	PA3	PA3	---
3	PT5	PT5	---	4	N/C	---	---
5	P91	P91	---	6	P92	P92	R342
7	P73	P73	---	8	P72	P72	---
9	PA5	PA5	---	10	P71	P71	---
11	PA3	PA3	---	12	PA4	PA4	---
13	P05	P05	R343	14	PH7	PH7	R344
15	P02	P02	R345	16	P23	P23	R346
17	0v	---	---	18	N/C	---	---
19	N/C	---	---	20	N/C	---	---
21	N/C	---	---	22	N/C	---	---
23	N/C	---	---	24	N/C	---	---

Table 7.5: Application Header JA6 Connections

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via a Segger JLink-Lite debugger, which is supplied with this RSK+ product.

8.2 Mode Support

The RZ/T1 microcontroller supports 3 boot modes which includes booting from memory connected to the CS0 space and serial flash memory.

8.3 Compiler Restrictions

The version of the compiler provided with this RSK+ is a fully functional GNU compiler, used in RSK+RZT1 sample projects.

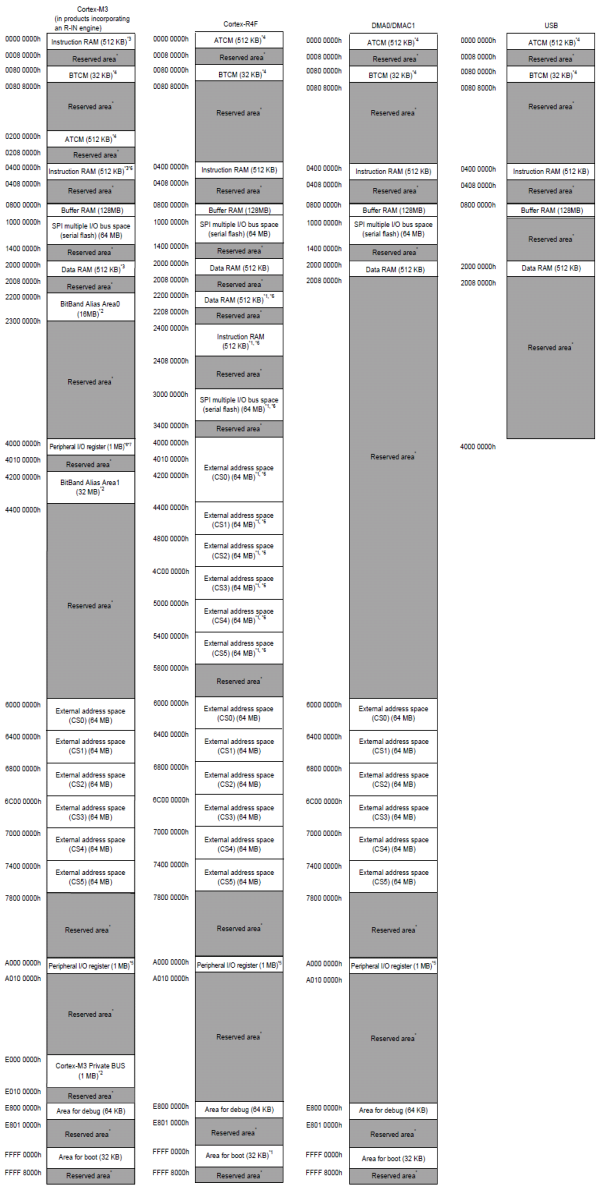
Support for the GNU NONE Compiler is available from http://www.kpitgnutools.com

8.4 Debugger Support

The RSK+ board is supplied with a Segger J-Link Lite Debugger. Please refer to the Segger website for further information www.segger.com.

8.5 Address Space

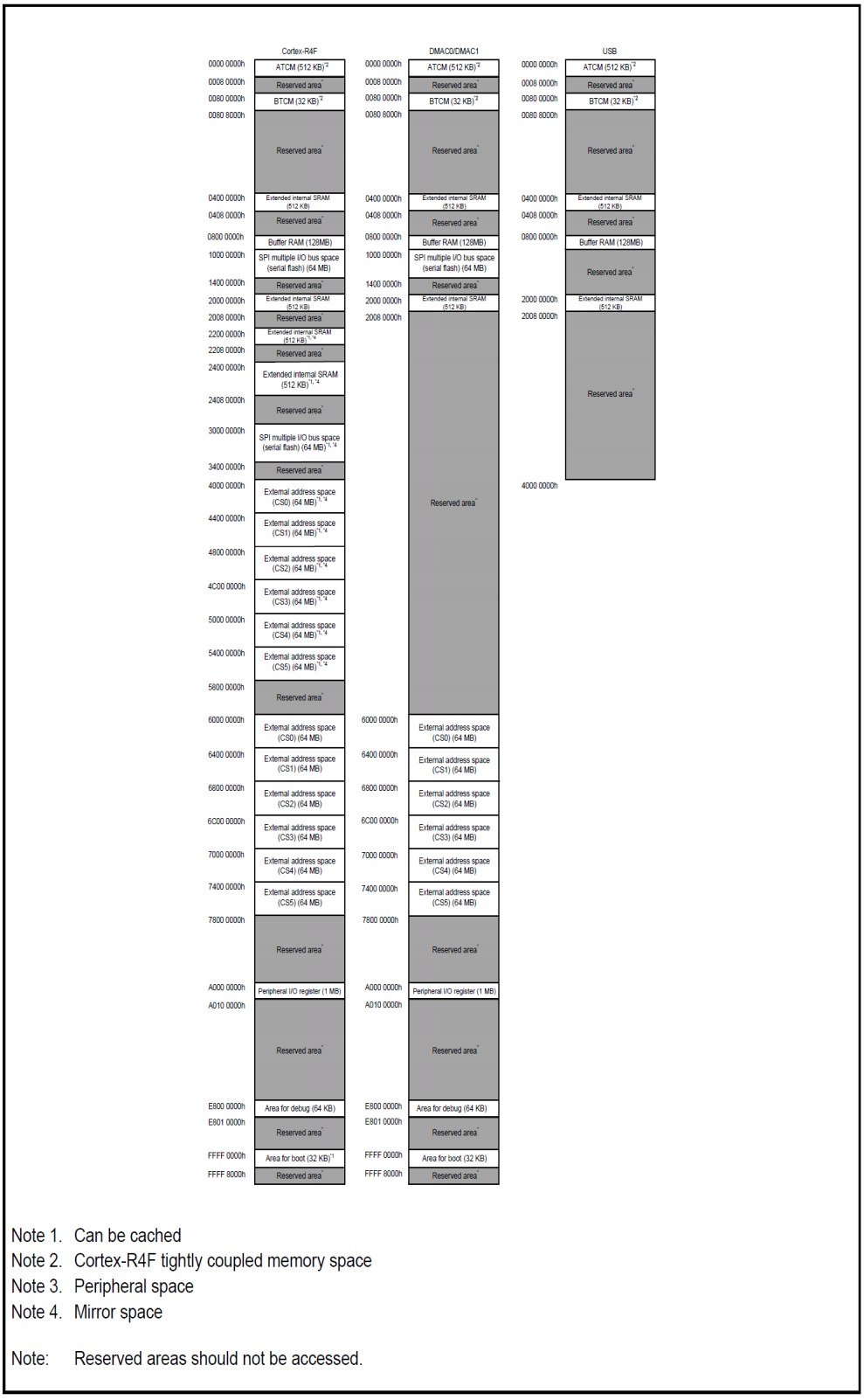
Figure 8.2 below details the address space of the MCU. This diagram is based on the Hardware Manual version 1.0. For further details, refer to the RZ/T1 Group Hardware Manual.



Note 1. Can be cached
(The MPU should not enable caching of other areas.)
Note 2. Accessible only from Cortex-M3.
Note 3. Cortex-M3 SRAM space (Extra-RAM)
Note 4. Cortex-R4F tightly coupled memory space
Note 5. Peripheral space
Note 6. Mirror space
Note 7. A00E0000 to A00FFFFF is a reserved area.

Note: Reserved areas should not be accessed.

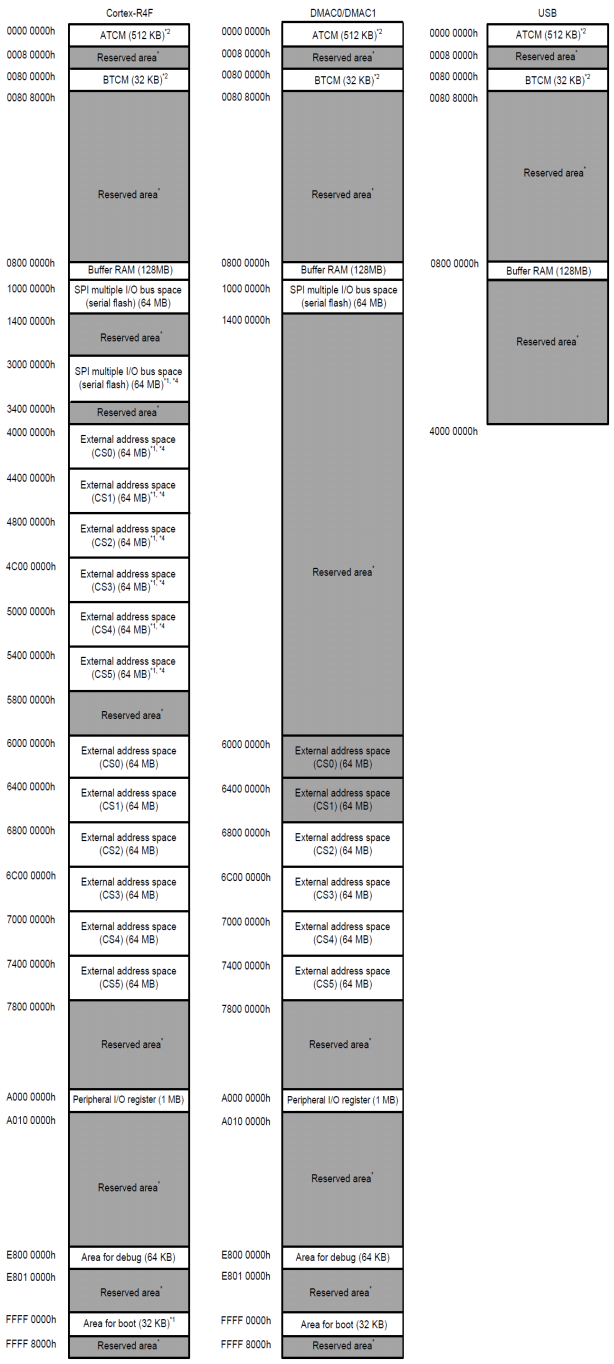
Figure 8.1: RZ/T1 Address Map On RSK+ Board



Note 1. Can be cached
Note 2. Cortex-R4F tightly coupled memory space
Note 3. Peripheral space
Note 4. Mirror space

Note: Reserved areas should not be accessed.

Figure 8.2: RSK+RZ/T1 Address Map (1-Mbyte Extended SRAM)



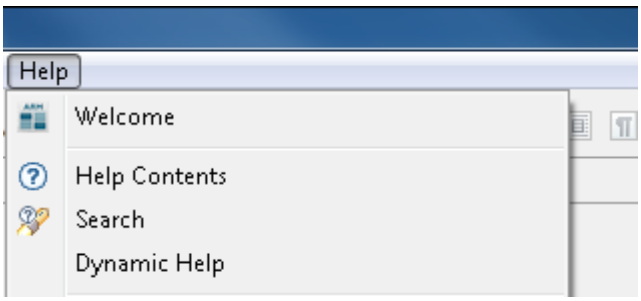
Note 1. Can be cached
Note 2. Cortex-R4F tightly coupled memory space
Note 3. Peripheral space
Note 4. Mirror space
Note 5. Debug APB area

Note: Reserved areas should not be accessed.

Figure 8.2: RSK+RZ/T1 Address Map (0-Kybte Extended Internal SRAM)

9. Additional Information

Technical Support
For details on how to use e^2 studio, refer to the help file by opening e^2 studio, then selecting Help > Help Contents from the menu bar.



For information about the RZ/T1 series microcontrollers refer to the RZ/T1 Group Hardware Manual.

For information about the RZ assembly language, refer to the RZ Series Software Manual.

Technical Contact Details

***Please refer to the contact details listed in section 11 of the* "Quick Start Guide"**

General information on Renesas Microcontrollers can be found on the Renesas website at:
http://www.renesas.com/

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