User's Manual

32

RX72T Group

Renesas Starter Kit for RX72T
User's Manual

RENESAS 32-Bit MCU
RX Family / RX700 Series

Renesas Electronics
www.renesas.com

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(Rev.4.0-1 November 2017)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit (RSK), the user accepts the following terms:

The RSK is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK is assumed by the User. The RSK is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK and development environment can be found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RSKRX72T. Please use the latest version of the document.
The latest version is posted on the Renesas Electronics website.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK hardware.	Renesas Starter Kit for RX72T User's Manual	R20UT4272EG (This manual)
Tutorial Manual	Provides a guide to setting up RSK environment, running sample code and debugging programs.	Renesas Starter Kit for RX72T Tutorial Manual	CS+: R20UT4273EG e^2 studio: R20UT4276EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample.	Renesas Starter Kit for RX72T Quick Start Guide	CS+: R20UT4274EG e^2 studio: R20UT4277EG
Smart Configurator Tutorial	Provides a guide to code generation and importing into the e^2 studio IDE.	Renesas Starter Kit for RX72T Smart Configurator Tutorial Manual	CS+: R20UT4275EG e^2 studio: R20UT4278EG
Schematics	Full detail circuit schematics of the RSK.	Renesas Starter Kit for RX72T Schematics	R20UT4271EG
Hardware Manual	Provides technical details of the RX72T microcontroller.	RX72T Group Hardware Manual	R01UH0803EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Do Not Fit
E1/E2 Lite	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GLCDC	Graphic LCD Controller
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK	Renesas Starter Kit
RTC	Real time Clock
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer

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1. Overview

1.1 Purpose

This RSK is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This RSK provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialisation code

The RSK board contains all the circuitry required for microcontroller operation.

1.3 Board specification

Board specification was shown in **Table 1-1** below.

Table 1-1: Board Specification

Item	Specification
Microcontroller	Part No: R5F572TKCDFB
	Package: 144-pin LFQFP
	On-Chip Memory: ROM 1MB+32KB, RAM 128KB+16KB
On-Board Memory	I^2C EEPROM: 2Kbit
Input Clock	RX72T Main: 8MHz
	RL78/G1C Main: 12MHz
Power Supply	DC Power Jack: 5 V Input
	Power Supply IC: 5V Input, 3.3V Output
Debug Interface	E1/E2 Lite 14-pin box header
DIP Switch	Mode Configuration: 2-pole x 1
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer (for ADC)	Single-turn, 10kΩ
LED	Power indicator: green x 1
	User: green x 1, orange x 1, red x 2
CAN	Connector: 2.54mm pitch, 3-pin x 1
	CAN Driver x 1
LIN	Connector: 2.54mm pitch, 3-pin x 1 *1
	LIN Driver x 1
USB	USB0 Function: USB-MiniB
	USB0 Host: USB-TypeA
USB to Serial Converter Interface	Connector: USB-MiniB
	Driver: RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1: Angle type, 12-pin Connector
	PMOD2 *1: Straight type, 12-pin Connector
Application Board Interface *1	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

*1: The connector is not included to a product.

2. Power Supply

2.1 Requirements

This RSK is supplied with an E1 debugger or E2 Lite debugger. The debugger is able to power the RSK board with up to 200mA. When the RSK is connected to another system then that system should supply power to the RSK. This board has an optional centre positive supply connector using a 2.0mm barrel power jack.

Details of the external power supply requirements for the RSK, and configuration are shown in **Table 2-1 and Table 2-2** below. The default RSK power configuration is shown in **bold, blue text.**

Table 2-1: PWR connector Requirements

Connector	Supply voltage
PWR	Input 5VDC

Table 2-2: Main Power Supply Requirements

J7 *1 Setting	J8 Setting	J9 Setting	J12 Setting	Supply Source	VCC_USB	Board_VCC UC_VCC	Board_5V
Open	**2-3 Shorted**	**2-3 Shorted**	**1-2 Shorted**	**E2-Lite / E1(3.3V)**	**3.3V *4, 5**	**3.3V *3**	**3.3V *7**
Open	2-3 Shorted	1-2 Shorted	2-3 Shorted	E1(5V)	3.3V *4, 5	5V *2	5V
Open	2-3 Shorted	2-3 Shorted	1-2 Shorted	E1(5V) / PWR / Unregulated_VCC / JA1-5V	5V *4, 5, 6	5V *2	5V
Open	1-2 Shorted	1-2 Shorted	1-2 or 2-3 Shorted	PWR / Unregulated_VCC / JA1-5V	3.3V *5	3.3V *3	5V
Open	2-3 Shorted	1-2 Shorted	2-3 Shorted	PWR / Unregulated_VCC / JA1-5V	3.3V *5	5V *2	5V
Shorted pin	1-2 Shorted	1-2 Shorted	1-2 or 2-3 Shorted	VBUS	3.3V *4, 6	3.3V *3	5V
Shorted pin	2-3 Shorted	1-2 Shorted	2-3 Shorted	VBUS	3.3V *4, 6	5V *2	5V

*1: The connector is not included to a product.

*2: 3.3V Pmod™ interface and Pmod™ LCD module cannot be used.

*3: 5V Pmod™ interface and CAN, LIN cannot be used.

*4: USB Host interface cannot be used.

*5: USB Function interface (Bus-powered) cannot be used.

*6: USB Function interface (Self-powered) cannot be used.

*7: When 3.3 V is supplied from the emulator, Board_5 V becomes 3.3 V voltage.

When using the function of 5 V, prepare an AC adapter. Suitable plugs are center plus, outer diameter 5.5 mm, inner diameter 2.1 mm.

The main power supply connected to PWR should supply a minimum of 5W to ensure full functionality.

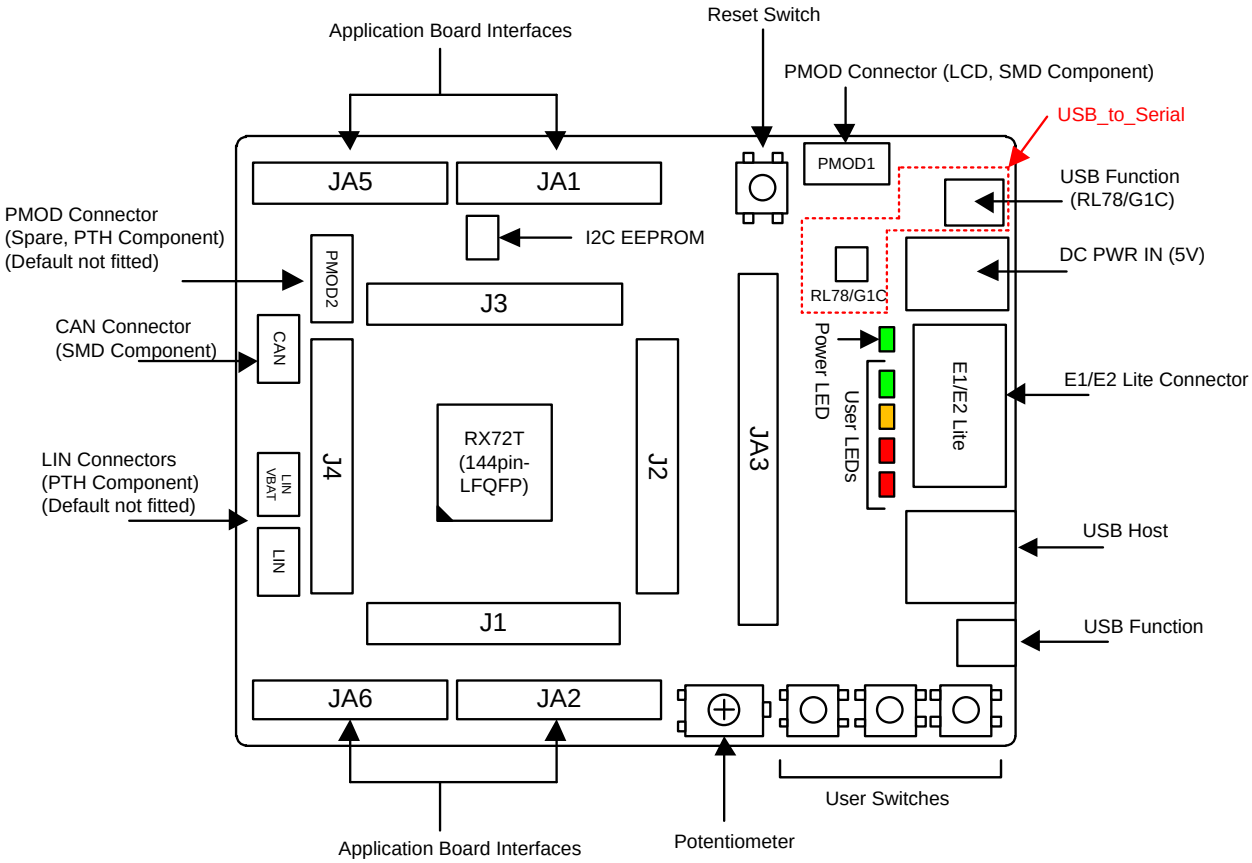
2.2 Power-Up Behaviour

When the RSK is purchased, the RSK board has the 'Release' build of the example tutorial software pre-programmed into the Renesas microcontroller. Please consult the 'Renesas Starter Kit Smart Configurator Tutorial Manual' for further information of this example.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.



* J1 to J4 : 36-pin Micon Pin Headers

Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.

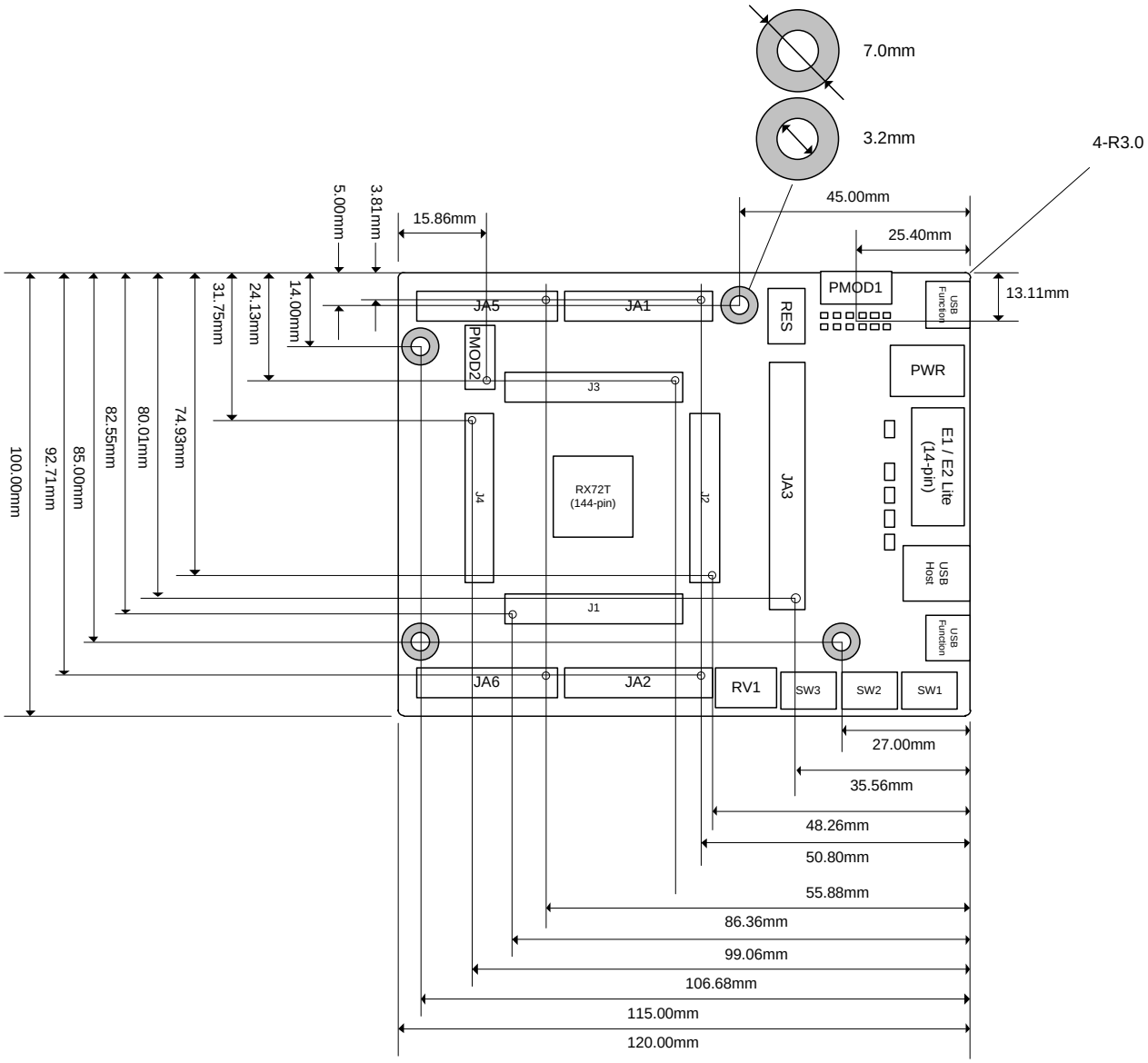


Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4**. Component types and values are shown on the board schematics.

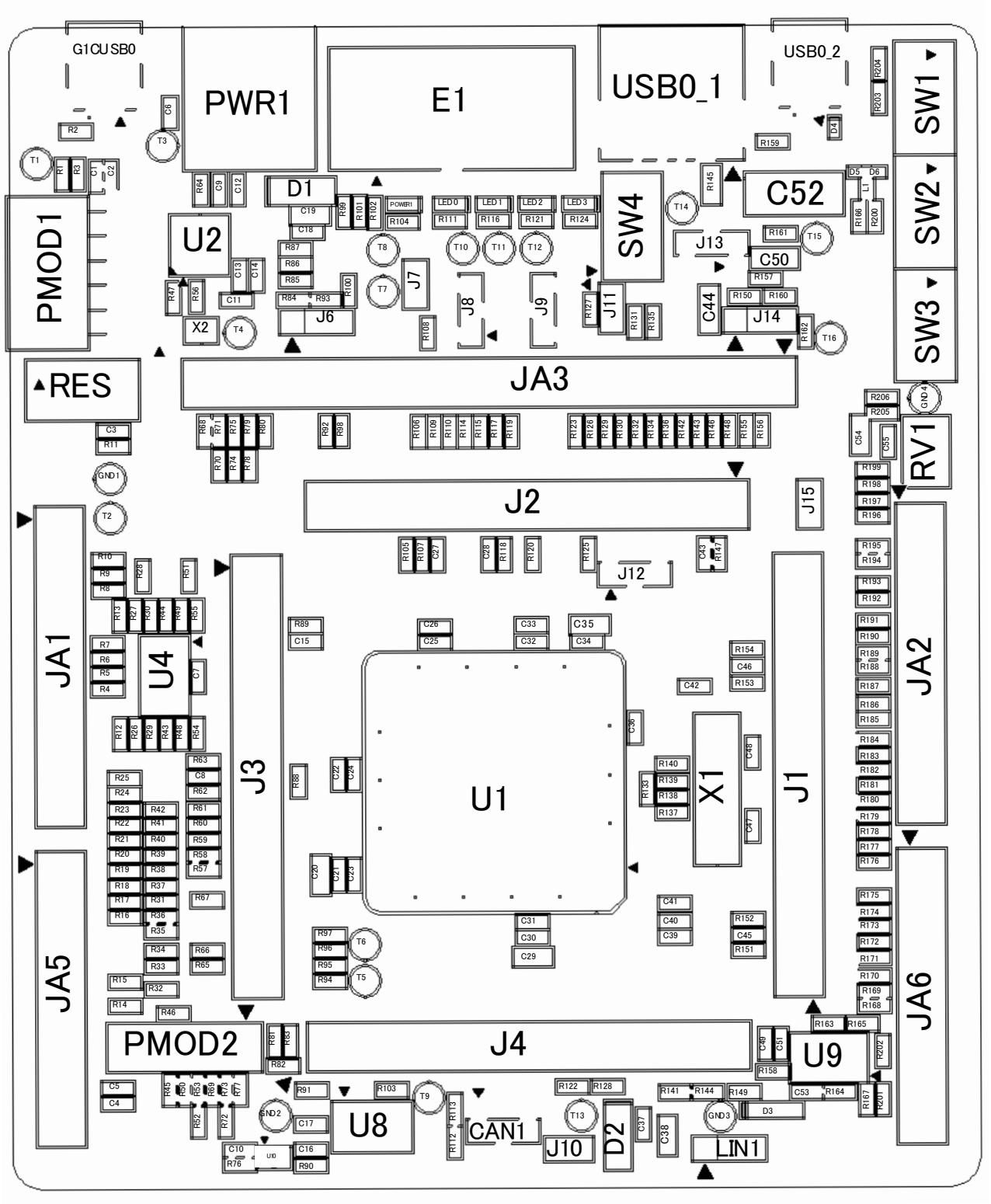


Figure 3-3: Top-Side Component Placement

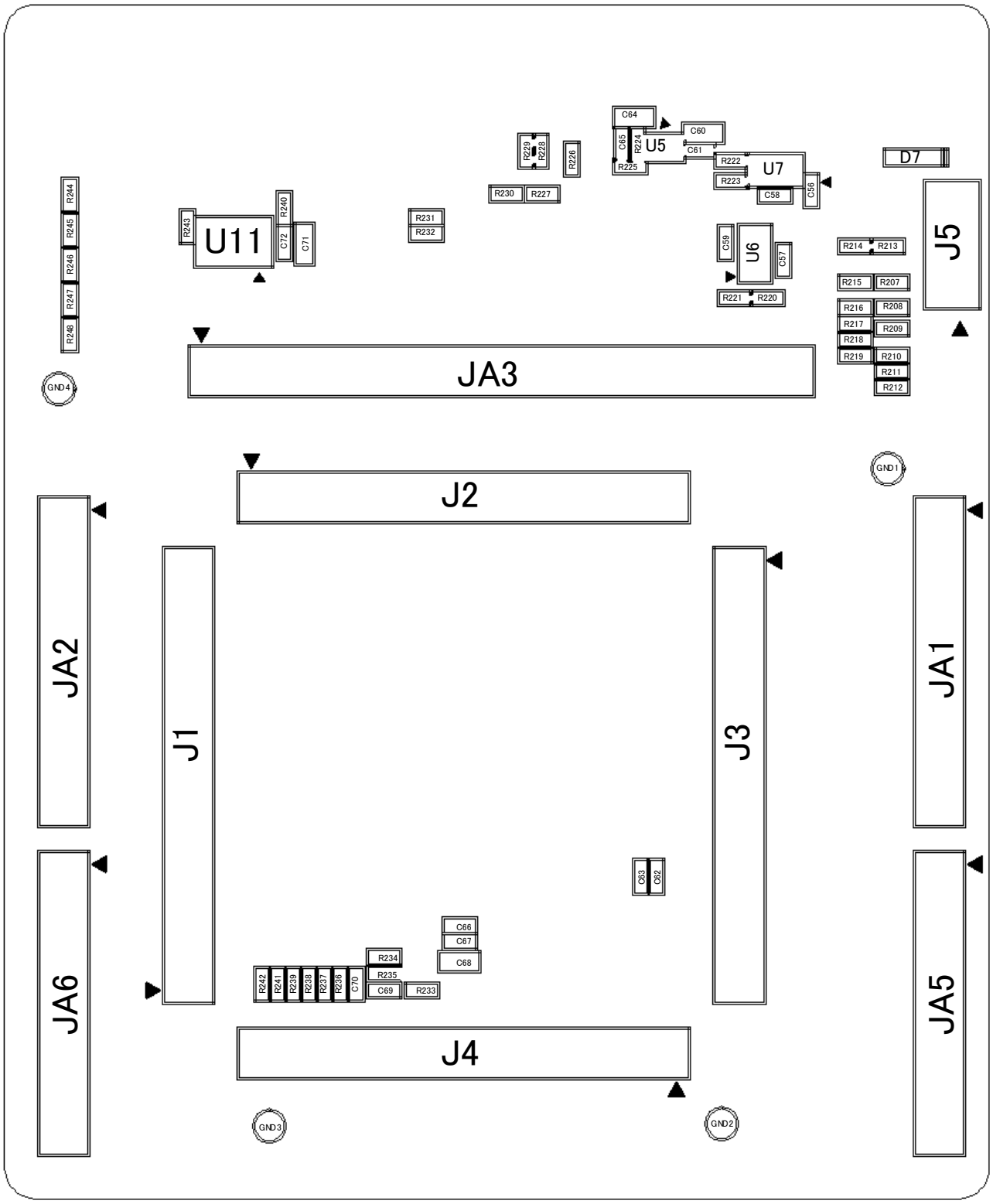


Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MCU.

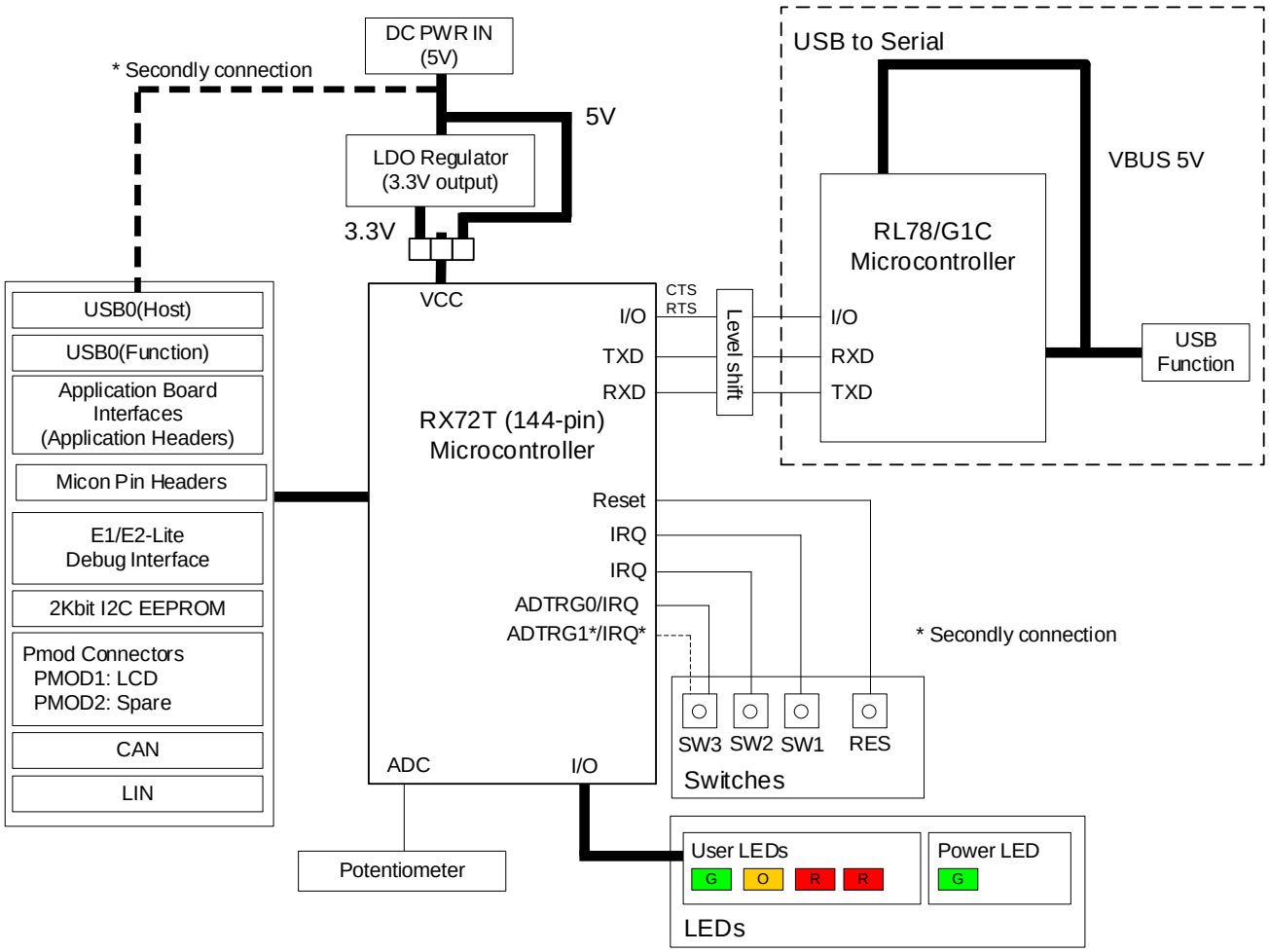


Figure 4-1: Internal Board Block Diagram

4.2 Debugger Connections

Figure 4-2 below shows the connections between the CPU board, E1/E2 Lite debugger and the host PC.

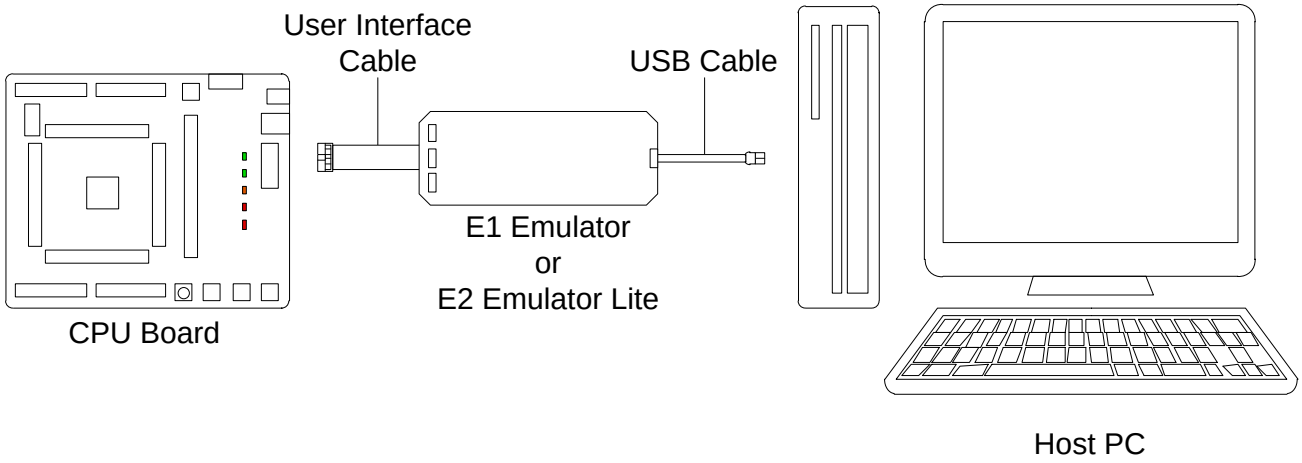


Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal, and is triggered from the RES switch. Refer to the RX72T Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX72T Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators fitted to the board are listed in Table 5-1 below.

Table 5-1: Crystal

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX72T	Fitted	8MHz	Encapsulated, SMT
X2	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT

5.3 Switches

There are four switches located on the CPU board. The function of each switch and its connection is shown in Table 5-2. For further information regarding switch connectivity, refer to the CPU board schematics.

Table 5-2: Switch Connections

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	15
SW1	Connects to an IRQ0_DS input for user controls.	P10	141
SW2	Connects to an IRQ9 input for user controls.	PB3	48
SW3	Connects to an IRQ7_DS input for user controls. Connects to an ADTRG0 input for ADC controls.	P20	101
	Connects to an IRQ6_DS input for user controls. Connects to an ADTRG1 input for ADC controls.	P21	100

5.4 LEDs

There are 5 LEDs on the CPU board. The function of each LED, its colour, and its connections are shown in **Table 5-3**.

Table 5-3: LED Connections

LED	Colour	Function	MCU	
			Port	Pin
POWER1	Green	Indicates the status of the Board_VCC power rail.	NC	NC
LED0	Green	User operated LED.	P54	112
LED1	Orange	User operated LED.	P55	111
LED2	Red	User operated LED.	P60	110
LED3	Red	User operated LED.	P61	109

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000, pin 131. The potentiometer can be used to create a voltage between Board_VCC and AVSS0.
Refer to the maker site for specification of the potentiometer (VISHAY with part number TS53 series).

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX72T Group User's Manual: Hardware for further details.

5.6 Pmod™

The CPU board are equipped with connectors for Digilent Pmod™ interface. Please connect the PMOD1 connector that is compatible with LCD module.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible headers use an SPI interface. **Figure 5-1** below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-4 and Table 5-5** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011.

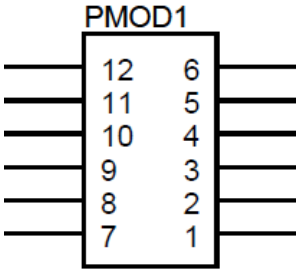


Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Table 5-4: Pmod™1 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD1-CS	PA2	57	7	PMOD1-IO0	PC6	62
2	PMOD1-MOSI	PB0	51	8	PMOD1-IO1	PC5	63
3	PMOD1-MISO	PA5	54	9	PMOD1-IO2	P25	94
4	PMOD1-SCK	PA4	55	10	PMOD1-IO3	P26	93
5	GROUND	-	-	11	GROUND	-	-
6	Board_VCC	-	-	12	Board_VCC	-	-

Table 5-5: Pmod™2 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD2-CS	P24	95	7	PMOD2-IO0	PF0	34
2	PMOD2-MOSI	P23	96	8	PMOD2-IO1	PK0	85
3	PMOD2-MISO	P22	97	9	PMOD2-IO2	P63	107
4	PMOD2-SCK	P30	91	10	PMOD2-IO3	P62	108
5	GROUND	-	-	11	GROUND	-	-
6	Board_VCC	-	-	12	Board_VCC	-	-

5.7 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RX72T Serial Communications Interface (SCI) module. Multiple options are provided to allow the selection of the connected SCI11 port. Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-6** below.

Table 5-6: Serial Port Connections

Signal Name	Function	MCU	
		Port	Pin
SERIAL-TXD	SCI1 Transmit Signal. *1	PD3	27
	SCI11 Transmit Signal.	PB5	41
	External RS232 Transmit Signal. *1	-	-
SERIAL-RXD	SCI1 Receive Signal. *1	PD5	25
	SCI11 Receive Signal.	PB6	40
	External RS232 Receive Signal. *1	-	-
SERIAL-CTS*2	Clear To Send.	PC3	99
SERIAL-RTS*2	Request To Send.	P31	89

*1: This connection is a not available in the default RSK configuration - refer to §6 for the required modifications.

*2: Flow control is a signal provided for expansion and is not currently supported. There is no schedule of function expansion at present.

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.

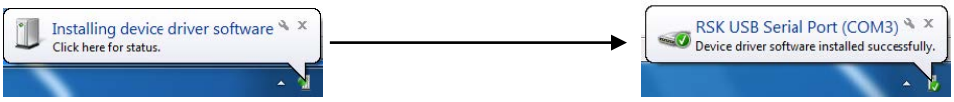


Figure 5-2: USB-Serial Windows™ Installation message

If you do not have the driver, please download the driver installer from the following URL.
https://www.renesas.com/en-eu/software/D6000699.html

5.8 Controller Area Network (CAN)

A CAN transceiver IC is fitted to the CPU board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX72T Group User's Manual: Hardware. The connections for the CAN microcontroller signals are listed in **Table 5-7** below.

Table 5-7: CAN Connections

CAN Signal	Function	MCU	
		Port	Pin
CAN1TX JA5-CAN1TX *1	CAN Data Transmission.	PA0	59
CAN1RX JA5-CAN1RX *1	CAN Data Reception.	PA1	58

*1: This connection is a not available in the default RSK configuration - refer to §6 for the required modifications.

5.9 External Bus

The RX72T features an external data bus, which is connected to various devices on the CPU board. Details of the devices connected to the external data bus are listed in **Table 5-8** below. Further details of the devices connected to the external bus can be found in the board schematics.

Table 5-8: External Bus Address Space

Chip Select	Device Name	Device Description	Address Space
CS0(JA3-CSa)	JA3	Application Header	FFE00000h – FFFFFFFFh (2MByte)
CS1	-	Unused	07E00000h – 07FFFFFFh (2MByte)
CS2(JA3-CSc)	JA3	Application Header	06E00000h – 06FFFFFFh (2MByte)
CS3(JA3-CSb)	JA3	Application Header	05E00000h – 05FFFFFFh (2MByte)

5.10 I²C Bus (Inter-IC Bus)

The RX72T features one I²C (Inter-IC Bus) interface modules. RIIC0 is connected to a 2Kbit EEPROM. Specific details of the EEPROM device and the connections can be found in the board schematics.

5.11 Local-Interconnect Network (LIN)

A LIN transceiver IC is fitted to the CPU board, and connected to the LIN MCU peripheral. For further details regarding the LIN protocol and supported modes of operation, please refer to the RX72T Group User's Manual: Hardware. The connections for the LIN microcontroller signals are listed in **Table 5-9** below.

Table 5-9: LIN Connections

CAN Signal	Function	MCU	
		Port	Pin
LINTXD	LIN Data Transmission.	P23	96
LINRXD	LIN Data Reception.	P22	97
LINNSLP	LIN Transceiver Device Sleep Control.	P24	95

5.12 Universal Serial Bus (USB)

This CPU board is fitted with a USB Host socket (type A) and a Function socket (type Mini B). USB module USB0 is connected to the Host and Function socket, and can operate as either a Host or Function device. The connection for the USB0 module is shown in **Table 5-10** below.

Table 5-10: USB0

USB Signal	Function	MCU	
		Port	Pin
USB0-DP	D+ I/O pin of the USB on-chip transceiver	USB0-DP	36
USB0-DM	D– I/O pin of the USB on-chip transceiver	USB0-DM	35
USB0-VBUS	USB cable connection monitor pin	PD2	28
USB0-VBUSEN	VBUS (5V) supply enable signal for external power supply chip	PC1	46
USB0-OVRCURA	External overcurrent detection signals	PC2	45

6. Configuration

6.1 Modifying the RSK

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX72T Group User's Manual: Hardware and CPU board schematics for further information.

6.2 MCU Operating Modes

Table 6-1 below details the option links associated with configuring the MCU Operating Modes.

Table 6-1: MCU Operating Modes Switch Settings (SW4)

Reference	Pin1	Pin2	Explanation	Related Ref.
SW4	**OFF**	**OFF(don't care)**	**Single Chip Mode**	
	ON	OFF	User Boot Mode	R126
	ON	ON	SCI Boot Mode	R126

6.3 E1/E2 Lite Debugger Configuration

Table 6-2 below details the function of the option links associated with E1/E2 Lite Debugger Configuration.

Table 6-2: E1/E2 Lite Debugger Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P00	9	P00	E1-UB	R126, R24	R129	E1/E2 Lite.10	-	-
			DSW-UB			SW4.2	-	-
			JA1-IRQd_M2HSIN0	R126, R24	R129	JA1.23	-	-
			JA3-A11	R129	R126, R24	JA3.12	-	-
PD7	23	PD7	E1-TRSTn	-	-	E1/E2 Lite.3	-	-
PD6	24	PD6	E1-TMS	-	-	E1/E2 Lite.9	-	-
PD5	25	PD5	E1-TDI_RXD	R231	R194, R172	E1/E2 Lite.11	-	-
			SERIAL-RXD	R194	R231, R172	U7.3	-	R195, R175
			JA6-RXDb	R172	R231, R194	JA6.7	-	
PD4	26	PD4	E1-TCK_FINEC	R101, R154	R99	E1/E2 Lite.1	-	-
			JA6-SCKb	R99, R154	R101	JA6.10	-	-
PD3	27	PD3	E1-TDO_TXD	R230	R142, R173	E1/E2 Lite.5		
			SERIAL-TXD	R142	R230, R173	U6.3	-	R143, R174
			JA6-TXDb	R173	R230, R142	JA6.8		
RESn	15	-	E1-RESn	-	-	E1/E2 Lite.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
EMLE	7	-	E1-EMLE	-	-	E1/E2 Lite.4	-	-
			JP-EMLE	-	-	J6.2	R93	-
MD_FINED	11	-	E1-MD_FINED	-	-	E1/E2 Lite.7	-	-
			DSW-MD_FINED	-	-	SW4.1	-	-

Table 6-3 below details the function of the jumpers associated with the E1/E2 Lite Debugger.

Table 6-3: E1/E2 Lite Debugger Configuration Jumper Settings

Reference	Jumper Position	Explanation	Related Ref.
J11(DNF) *1	Shorted Pin1-2	Enable E1/E2 Lite debugging with Hot plug-in function.	-
	Shorted Pin2-3	Enable E1/E2 Lite normal debugging and MCU single operation (without E1/E2 Lite).	R93
	All open	DO NOT SET.	-

*1: Jumper J11 is not fitted on the default CPU board. Same as Jumper Position “Shorted pin2-3” setting by resistor R93.

6.4 Power Supply Configuration

Table 6-4 below details the function of the jumpers associated with the Power Supply Configuration.

Table 6-4: Power Supply Configuration Jumper Settings

Reference	Jumper Position	Explanation	Related Ref.
J7(DNF) *1	Shorted	VBUS0 power rail to Board_5V.	U5
	Open	Disconnects VBUS0 power rail from Board_5V.	
J8 *2	Shorted Pin1-2	Board_3V3 power rail to Board_VCC.	J9
	Shorted Pin2-3 *4	Board_5V power rail to Board_VCC.	
	All Open	DO NOT SET.	
J9 *2	Shorted Pin1-2	Regulator output(3.3V) to Board_3V3.	
	Shorted Pin2-3 *3	Disconnects regulator output(3.3V) from Board_3V3.	
	All Open	Disconnects regulator output(3.3V) from Board_3V3.	
J11(DNF) *5	Shorted	Board_VCC power rail to UC_VCC.	R127
	Open	Enable current probe for measurement MCU current consumption.	
J12	Shorted Pin1-2	The operating voltage of VCC_USB is set to the same as the operating voltage of the MCU	
	Shorted Pin2-3	Operating voltage of VCC_USB is fixed at 3.3 V	
	All open	Please do not set	

*1: Jumper J7 is not fitted on the default CPU board.
*2: Same as Jumper Position “Shorted pin2-3” setting by jumper block.
*3: When the 3.3 V power supply source is the E1 / E2 Lite emulator or JA1-3V3, be sure to release it.
*4: When 5V power supply source is the E1 emulator, be sure to short Pin 2-3.
*5: Jumper J11 is not fitted on the default CPU board. Same as Jumper Position “Shorted” setting by resistor R127.

Table 6-5 below details the function of the option links associated with Power Supply Configuration.

Table 6-5: Power Supply Configuration Option Links

Reference	Explanation	Fit	DNF	Related Ref.
PWR	Connects PWR power rail to Board_5V.	-	-	U5, R141, J8, Simple IIC pull-up resistor
JA1-5V	Connects JA1-5V power rail to Board_5V.	R85	-	U5, R141, J8, Simple IIC pull-up resistor
	Disconnects JA1-5V power rail from Board_5V.	-	R85	
USB_5V	Connects USB_5V power rail to Board_5V.	R87	-	U5, R141, J8, Simple IIC pull-up resistor
	Disconnects USB_5Vpower rail from Board_5V.	-	R87	
Unregulated_VCC	Connects Unregulated_VCC power rail to Board_5V.	R86	-	U5, R141, J8, Simple IIC pull-up resistor
	Disconnects Unregulated_VCC power rail from Board_5V.	-	R86	
JA1-3V3	Connects JA1-3V3 power rail to Board_3V3.	R108	-	J9, J8
	Disconnects JA1-3V3 power rail from Board_3V3.	-	R108	
Board_VCC	Connects Board_VCC power rail to UC_VCC.	J11(Short) or R127	-	U1, R97, R95
	Enable current probe for measurement MCU current consumption.	-	J11(Open), R127	
U5.VOUT	Connects Regulator output to Board_3V3.	J9(1-2 Short)	-	J9
	Disconnects Regulator output from Board_3V3.	-	J9(1-2 Short), J9(Open)	
Board_5V	Connects Board_5V power rail to VBAT.	R141	-	J10
	Disconnects Board_5V power rail from VBAT.	-	R141	

6.5 Clock Configuration

Table 6-6 below details the function of the option links associated with Clock Configuration.

Table 6-6: Clock Configuration Option Links

Reference	Explanation	Fit	DNF	Related Ref.
XTAL, EXTAL	Connects 8MHz crystal (X1) to RX72T.	R138, R139	R137, R140	U1.16, U1.18
	Connects JA2-EXTAL to RX72T.	R140	R138, R139	U1.18

6.6 Analog Power & ADC & DAC Configuration

Table 6-7 below details the function of the option links associated with Analog Power & ADC & DAC Configuration.

Table 6-7: Analog Power & ADC & DAC Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P21	100	P21	SW3	R247	R248	SW3	-	-
			JA1-ADTRG	R8	R9	JA1.8	-	-
P20	101	P20	SW3	R248	R247	SW3	-	-
			JA1-ADTRG	R9	R8	JA1.8	-	-
JA5-ADC6	121	P46	JA5-ADC6	-	-	JA5.3	-	-
JA5-ADC5	122	P45	JA5-ADC5	-	-	JA5.2	-	-
JA5-ADC4	123	P44	JA5-ADC4	-	-	JA5.1	-	-
JA1-ADC2	129	P42	JA1-ADC2	-	-	JA1.11	-	-
JA1-ADC1	130	P41	JA1-ADC1	-	-	JA1.10	-	-
P40	131	P40	RV1-ADC	R235	R234	RV1(Board_VCC)	R206	R205
						RV1(AVCC0-2)	R205	R206
			JA1-ADC0	R234	R235	JA1.9		
P65	102	P65	JA1-DAC1	-	-	JA1.14	-	-
P64	103	P64	JA1-DAC0	-	-	JA1.13	-	-
JA5-ADC7	124	PH4	JA5-ADC7	-	-	JA5.4	-	-
JA1-ADC3	132	PH0	JA1-ADC3	-	-	JA1.12	-	-
AVCC0-2	134,133, 104,105	-	UC_VCC	R97	R96	-	-	-
			JA1-AVCC	R96	R97	JA1.5	-	-
AVSS0-2	135,136,106	-	GROUND	R95	R94	-	-	-
			JA1-AVSS	R94	R95	JA1.6	-	-

6.7 BUS Configuration

Table 6-8 and Table 6-9 below details the function of the option links associated with BUS Configuration.

Table 6-8: BUS Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P01	12	P01	JA5-M2HSIN2	R35	R123	JA5.10	-	-
			JA3-A10	R123	R35	JA3.11	-	-
P00	9	P00	E1-UB	R126, R24	R129	E1/E2 Lite.10	-	-
			DSW-UB			SW4.2	-	-
			JA1-IRQd_M2HSIN0	R126, R24	R129	JA1.23	-	-
			JA3-A11	R129	R126, R24	JA3.12	-	-
P27	92	P27	JA2-M1ENC	R60	R61	JA2.23	R183	R182
			JA3-CSb	R61	R60	JA3.28	-	-
JA3-A13	60	P35	JA3-A13	-	-	JA3.14	-	-
JA3-A12	61	P34	JA3-A12	-	-	JA3.13	-	-
P33	86	P33	JA2-M1TRCCLK	R178	R179	JA2.25	-	-
			JA3-D7	R179	R178	JA3.24	-	-
P32	87	P32	JA2-M1TRDCLK	R177	R176	JA2.26	-	-
			JA3-D8	R176	R177	JA3.29	-	-
P31	89	P31	JA3-D9	R109	R106	JA3.30	-	-
			SERIAL-RTS	R106	R109	U6.2	-	-
P30	91	P30	JA3-D10	R63, R88	R62	JA3.31	-	-
			PMOD2-SCK	R62, R88	R63	PMOD2.4	-	-
JA3-D0	73	P76	JA3-D0	-	-	JA3.17	-	-
JA3-D1	74	P75	JA3-D1	-	-	JA3.18	-	-
JA3-D2	75	P74	JA3-D2	-	-	JA3.19	-	-
JA3-D3	76	P73	JA3-D3	-	-	JA3.20	-	-
JA3-D4	77	P72	JA3-D4	-	-	JA3.21	-	-
JA3-D5	78	P71	JA3-D5	-	-	JA3.22	-	-
P70	79	P70	JA2-M1POE	R180, R89	R119	JA2.24	-	-
			JA3-D6	R119, R89	R180	JA3.23	-	-
P82	137	P82	JA5-M2UIN	R238, R236	R239, R241, R237, R242	JA5.12	-	-
			JA3-ALE	R239, R236	R238, R241, R237, R242	JA3.46	-	-
			JA3-WAIT	R241, R236	R238, R239, R237, R242	JA3.45	R75	R79
			JA6-M1UIN	R237, R236	R238, R239, R241, R242	JA6.14	-	-
			JA6-SCKc	R242, R236	R238, R239, R241, R237	JA6.11	-	-
P81	138	P81	JA5-M2VIN	R16	R80, R168	JA5.13	-	-
			JA3-CSc	R80	R16, R168	JA3.45	R79	R75
			JA6-M1VIN	R168	R16, R80	JA6.15	-	-
JA3-A15	52	PA7	JA3-A15	-	-	JA3.16	-	-
JA3-A14	53	PA6	JA3-A14	-	-	JA3.15	-	-
PA2	57	PA2	PMOD1-CS	R212	R155	PMOD1.1	-	-
			JA3-A0	R155	R212	JA3.1	-	-
PB7	39	PB7	JA2-SCKa	R192, R147	R193	JA2.10	-	-
			JA3-A4	R193, R147	R192	JA3.15	-	-
PB6	40	PB6	SERIAL-RXD	R195, R198	R148	U7.3		R194, R175
			JA2-RXDa	R195, R198	R148	JA2.8	-	-
			JA3-A3	R148	R195, R198	JA3.4	-	-
PB5	41	PB5	SERIAL-TXD	R143, R199	R146	U6.3	-	R142, R174
			JA2-TXDa	R199, R143	R146	JA2.6	-	-
			JA3-A2	R146	R143, R199	JA3.3	-	-
PB4	43	PB4	JA2-CTSaRTSa	R188	R156	JA2.12	-	-
			JA3-A1	R156	R188	JA3.2	-	-
JA3-A20		PC4	JA3-A20	-	-	JA3.41	-	-
PC1	46	PC1	USB0-VBUSEN	R98	R92	U11.4	-	-
			JA3-A16	R92	R98	JA3.37	-	-
JA3-CSa	47	PC0	JA3-CSa	-	-	JA3.27	-	-

Table 6-9: BUS Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PD2	28	PD2	USB0-VBUS	R132	R134	USB0_1.1, USB0_2.1	J14 (2-3 short) or R162	-
			JA3-A7	R134	R132	JA3.8	-	-
PD1	29	PD1	JA2-TIMOUT1	R186	R130	JA2.20	-	-
			JA3-A6	R130	R186	JA3.7	-	-
PD0	30	PD0	JA2-TIMIN1	R184	R136	JA2.22	-	-
			JA3-A5	R136	R184	JA3.6	-	-
JA3-RDn	4	PE6	JA3-RDn	-	-	JA3.25	-	-
JA3-BCLK	5	PE5	JA3-BCLK	-	-	JA3.44	-	-
PE4	13	PE4	JA5-M2TRCCLK	R34	R66	JA5.17	-	-
			JA3-A9	R66	R34	JA3.10	-	-
PE3	14	PE3	JA5-M2TRDCLK	R33	R65	JA5.18	-	-
			JA3-A8	R65	R33	JA3.9	-	-
PE1	21	PE1	JA3-WRLn	R68	R115	JA3.48	-	-
			JA3-WRn	R115	R68	JA3.26	-	-
JA3-WRHn	22	PE0	JA3-WRHn	-	-	JA3.47	-	-
JA3-A19	31	PF3	JA3-A19	-	-	JA3.40	-	-
JA3-A18	32	PF2	JA3-A18	-	-	JA3.39	-	-
JA3-A17	33	PF1	JA3-A17	-	-	JA3.38	-	-
JA3-D11	80	PG2	JA3-D11	-	-	JA3.32	-	-
JA3-D12	81	PG1	JA3-D12	-	-	JA3.33	-	-
JA3-D13	82	PG0	JA3-D13	-	-	JA3.34	-	-
JA3-D14	83	PK2	JA3-D14	-	-	JA3.35	-	-
JA3-D15	84	PK1	JA3-D15	-	-	JA3.36	-	-

6.8 CAN Configuration

Table 6-10 below details the function of the option links associated with CAN Configuration.

Table 6-10: CAN Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PA1	58	PA1	CAN1RX	R76	R19, R38	U10.3	-	-
			JA5-CAN1RX	R19	R76, R38	JA5.15	-	-
			JA5-M2TOGGLE	R38	R76, R19	JA5.6	-	-
PA0	59	PA0	CAN1TX	R91	R57	U8.1	-	-
			JA5-CAN1TX	R57	R91	JA5.5	-	-

6.9 General IO & LED Configuration

Table 6-11 below details the function of the option links associated with General IO & LED Configuration.

Table 6-11: General IO & LED Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
LED1	111	P55	LED1	-	-	LED1.K	R228	-
LED0	112	P54	LED0	-	-	LED0.K	R228	-
JA1-IO7	115	P51	JA1-IO7	-	-	-	-	-
JA1-IO6	116	P50	JA1-IO6	-	-	-	-	-
LED3	109	P61	LED3	-	-	LED3.K	R228	-
LED2	110	P60	LED2	-	-	LED2.K	R228	-
JA1-IO5	117	PH7	JA1-IO5	-	-	-	-	-
JA1-IO4	118	PH6	JA1-IO4	-	-	-	-	-
JA1-IO3	119	PH5	JA1-IO3	-	-	-	-	-
JA1-IO2	125	PH3	JA1-IO2	-	-	-	-	-
JA1-IO1	126	PH2	JA1-IO1	-	-	-	-	-
JA1-IO0	127	PH1	JA1-IO0	-	-	-	-	-

6.10 I2C & EEPROM Configuration

Table 6-12 and Table 6-13 below detail the function of the option links associated with I2C & EEPROM Configuration.

Table 6-12: I2C & EEPROM Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PB2	49	PB2	E2P-SDA	-	-	U4.5	-	-
			JA1-SDA	-	-	JA1.25	-	-
PB1	50	PB1	E2P-SCL	R189	R190	U4.6	-	-
			JA1-SCL	R189	R190	JA1.26	-	-
			JA2-IRQb_M1HSIN1	R190	R189	JA2.9	-	-

Table 6-13: I2C & EEPROM Configuration Option Links (2)

Reference	Explanation	Fit	DNF	Related Ref.
SDA, SCL	Connects pull-up resistor to Board_3V3.	R28	R51	U4
	Connects pull-up resistor to Board_5V.	R51	R28	U4
WP	EEPROM Write protect.	R48	-	U4
A0, A1, A2	Device address (0xA6).	R49, R44, R13	R27, R30, R55	U4
	Device address (0xA4).	R55, R44, R13	R27, R30, R49	U4

6.11 IRQ & Switch Configuration

Table 6-14 below details the function of the option links associated with IRQ & Switch Configuration.

Table 6-14: IRQ & Switch Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P00	9	P00	E1-UB	R126, R24	R129	E1/E2 Lite.10	-	-
			DSW-UB			SW4.2	-	-
			JA1-IRQd_M2HSIN0	R126, R24	R129	JA1.23	-	-
			JA3-A11	R129	R126, R24	JA3.12	-	-
P10	141	P10	SW1	R203, R67	-	SW1	-	-
			JA5-IRQe_M2HSIN1	R203, R67	-	JA5.9	R17	R18
P21	100	P21	SW3	R247	R248	SW3	-	-
			JA1-ADTRG	R8	R9	JA1.8	-	-
P20	101	P20	SW3	R248	R247	SW3	-	-
			JA1-ADTRG	R9	R8	JA1.8	-	-
PB3	48	PB3	SW2	R245	-	SW2	-	-
			JA2-IRQa_M1HSIN0	R197	-	JA2.7	-	-
PB1	50	PB1	E2P-SCL	R189	R190	U4.6	-	-
			JA1-SCL	R189	R190	JA1.26	-	-
			JA2-IRQb_M1HSIN1	R190	R189	JA2.9	-	-
PB0	51	PB0	PMOD1-MOSI	R217	R218	PMOD1.2	-	-
			JA2-IRQc_M1HSIN2	R218	R217	JA2.23	R182	R183
PMOD1-IO0	62	PC6	PMOD1-IO0	-	-	PMOD1.7	-	-
PMOD1-IO1	63	PC5	PMOD1-IO1	-	-	PMOD1.8	-	-
SERIAL-CTS	99	PC3	SERIAL-CTS	-	-	U7.2	-	-
PE2	20	PE2	JA2-NMIn	-	-	JA2.3	-	-
			JP-UPSEL	-	-	J15.2	-	-
PMOD2-IO0	34	PF0	PMOD2-IO0	-	-	PMOD2.7	-	-
PMOD2-IO1	85	PK0	PMOD2-IO1	-	-	PMOD2.8	-	-
RESn	10	-	E1-RESn	-	-	E1/E2 Lite.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
MD_FINED	11	-	E1-MD_FINED	-	-	E1/E2 Lite.7	-	-
			DSW-MD_FINED	-	-	SW4.1	-	-

6.12 LIN Configuration

Table 6-15 and Table 6-16 below details the function of the option links associated with LIN Configuration.

Table 6-15: LIN Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P24	95	P24	LINNSLP	R202	R83	U9.2	-	-
			PMOD2-CS	R83	R202	PMOD2.1	-	-
P23	96	P23	LINTXD	R165	R171, R72	U9.4	-	-
			JA6-TXDc	R171	R165, R72	JA6.9	-	-
			PMOD2-MOSI	R72	R165, R171	PMOD2.2	-	-
P22	97	P22	LINRXD	R167	R170, R52	U9.1	-	-
			JA6-RXDc	R170	R167, R52	JA6.12	-	-
			PMOD2-MISO	R52	R167, R170	PMOD2.3	-	-

Table 6-16: LIN Configuration Option Links (2)

Reference	Explanation	Fit	DNF	Related Ref.
U9.6	Master	R144, R149	-	U9
	Slave	-	R144, R149	U9

6.13 MTU & POE Configuration

Table 6-17 and Table 6-18 below details the function of the option links associated with MTU & POE Configuration.

Table 6-17: MTU & POE Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P01	12	P01	JA5-M2HSIN2	R35	R123	JA5.10	-	-
			JA3-A10	R123	R35	JA3.11	-	-
P00	9	P00	E1-UB	R126, R24	R129	E1/E2 Lite.10	-	-
			DSW-UB			SW4.2	-	-
			JA1-IRQd_M2HSIN0	R126, R24	R129	JA1.23	-	-
			JA3-A11	R129	R126, R24	JA3.12	-	-
P11	140	P11	JA6-M1TOGGLE	-	-	JA6.13	-	-
P10	141	P10	SW1	R203, R67	-	SW1	-	-
			JA5-IRQe_M2HSIN1	R203, R67	-	JA5.9	R17	R18
P12	3	P12	JA2-M1UP	-	-	JA2.13	-	-
P13	2	P13	JA2-M1VP	-	-	JA2.15	-	-
P14	1	P14	JA2-M1WP	-	-	JA2.17	-	-
P15	144	P15	JA2-M1UN	-	-	JA2.14	-	-
P16	143	P16	JA2-M1VN	-	-	JA2.16	-	-
P17	142	P17	JA2-M1WN	-	-	JA2.18	-	-
P27	92	P27	JA2-M1ENC	R60	R61	JA2.23	R183	R182
			JA3-CSb	R61	R60	JA3.28	-	-
P33	86	P33	JA2-M1TRCCLK	R178	R179	JA2.25	-	-
			JA3-D7	R179	R178	JA3.24	-	-
P32	87	P32	JA2-M1TRDCLK	R177	R176	JA2.26	-	-
			JA3-D8	R176	R177	JA3.29	-	-
P53	113	P53	JA2-M1UD	-	-	JA2.11	-	-
P52	114	P52	JA5-M2UD	-	-	JA5.11	-	-
P70	79	P70	JA2-M1POE	R180, R89	R119	JA2.24	-	-
			JA3-D6	R119, R89	R180	JA3.23	-	-
P82	137	P82	JA5-M2UIN	R238, R236	R239, R241, R237, R242	JA5.12		
			JA3-ALE	R239, R236	R238, R241, R237, R242	JA3.46		
			JA3-WAIT	R241, R236	R238, R239, R237, R242	JA3.45	R75	R79
			JA6-M1UIN	R237, R236	R238, R239, R241, R242	JA6.14		
			JA6-SCKc	R242, R236	R238, R239, R241, R237	JA6.11		

Table 6-18: MTU & POE Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P81	138	P81	JA5-M2VIN	R16	R80, R168	JA5.13	-	-
			JA3-CSc	R80	R16, R168	JA3.45	R79	R75
			JA6-M1VIN	R168	R16, R80	JA6.15	-	-
P80	139	P80	JA5-M2WIN	R15	R169	JA5.14	-	-
			JA6-M1WIN	R169	R15	JA6.16	-	-
P96	65	P96	JA5-M2POE	R107	-	JA5.16	-	-
P95	67	P95	JA5-M2UP	-	-	JA5.19	-	-
P94	68	P94	JA5-M2VP	-	-	JA5.21	-	-
P93	69	P93	JA5-M2WP	-	-	JA5.23	-	-
P92	70	P92	JA5-M2UN	R32	R187	JA5.20	-	-
			JA2-TIMOUT0	R187	R32	JA2.19	-	-
P91	71	P91	JA5-M2VN	R14	R185	JA5.22	-	-
			JA2-TIMIN0	R185	R14	JA2.21	-	-
JA5-M2WN	72	P90	JA5-M2WN	-	-	JA5.24	-	-
JA5-M2ENC	56	PA3	JA5-M2ENC	-	-	JA5.9	R18	R17
PA1	58	PA1	CAN1RX	R76	R19, R38	U10.3	-	-
			JA5-CAN1RX	R19	R76, R38	JA5.15	-	-
			JA5-M2TOGGLE	R38	R76, R19	JA5.6	-	-
PB3	48	PB3	SW2	R245	-	SW2	-	-
			JA2-IRQa_M1HSIN0	R197	-	JA2.7	-	-
PB1	50	PB1	E2P-SCL	R189	R190	U4.6	-	-
			JA1-SCL	R189	R190	JA1.26	-	-
			JA2-IRQb_M1HSIN1	R190	R189	JA2.9	-	-
PB0	51	PB0	PMOD1-MOSI	R217	R218	PMOD1.2	-	-
			JA2-IRQc_M1HSIN2	R218	R217	JA2.23	R182	R183
PD1	29	PD1	JA2-TIMOUT1	R186	R130	JA2.20	-	-
			JA3-A6	R130	R186	JA3.7	-	-
PD0	30	PD0	JA2-TIMIN1	R184	R136	JA2.22	-	-
			JA3-A5	R136	R184	JA3.6	-	-
PE4	13	PE4	JA5-M2TRCCLK	R34	R66	JA5.17	-	-
			JA3-A9	R66	R36	JA3.10	-	-
PE3	14	PE3	JA5-M2TRDCLK	R33	R65	JA5.18	-	-
			JA3-A8	R65	R33	JA3.9	-	-
RESn	10	-	E1-RESn	-	-	E1/E2 Lite.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-

6.14 PMOD1 Configuration

Table 6-19 below details the function of the option links associated with PMOD1 Configuration.

Table 6-19: PMOD1 Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PMOD1-IO3	93	P26	PMOD1-IO3	-	-	PMOD1.10	-	-
PMOD1-IO2	94	P25	PMOD1-IO2	-	-	PMOD1.9	-	-
PMOD1-MISO	54	PA5	PMOD1-MISO	-	-	PMOD1.3	-	-
PMOD1-SCK	55	PA4	PMOD1-SCK	R118	-	PMOD1.4	-	-
PMOD1-IO0	62	PC6	PMOD1-IO0	-	-	PMOD1.7	-	-
PMOD1-IO1	63	PC5	PMOD1-IO1	-	-	PMOD1.8	-	-
PA2	57	PA2	PMOD1-CS	R212	R155	PMOD1.1	-	-
			JA3-A0	R155	R212	JA3.1	-	-
PB0	51	PB0	PMOD1-MOSI	R217	R218	PMOD1.2	-	-
			JA2-IRQc_M1HSIN2	R218	R217	JA2.23	R182	R183

6.15 PMOD2 Configuration

Table 6-20 below details the function of the option links associated with PMOD2 Configuration.

Table 6-20: PMOD2 Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P24	95	P24	LINNSLP	R202	R83	U9.2	-	-
			PMOD2-CS	R83	R202	PMOD2.1	-	-
P23	96	P23	LINTXD	R165	R171, R72	U9.4	-	-
			JA6-TXDc	R171	R165, R72	JA6.9	-	-
			PMOD2-MOSI	R72	R165, R171	PMOD2.2	-	-
P22	97	P22	LINRXD	R167	R170, R52	U9.1	-	-
			JA6-RXDc	R170	R167, R52	JA6.12	-	-
			PMOD2-MISO	R52	R167, R170	PMOD2.3	-	-
P30	91	P30	JA3-D10	R63, R88	R62	JA3.31	-	-
			PMOD2-SCK	R62, R88	R63	PMOD2.4	-	-
PMOD2-IO2	107	P63	PMOD2-IO2	-	-	PMOD2.9	-	-
PMOD2-IO3	108	P62	PMOD2-IO3	-	-	PMOD2.10	-	-
PMOD2-IO0	34	PF0	PMOD2-IO0	-	-	PMOD2.7	-	-
PMOD2-IO1	85	PK0	PMOD2-IO1	-	-	PMOD2.8	-	-

6.16 Serial & USB to Serial Configuration

Table 6-21 below details the function of the option links associated with Serial & USB to Serial Configuration.

Table 6-21: Serial & USB to Serial Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P23	96	P23	LINTXD	R165	R171, R72	U9.4	-	-
			JA6-TXDc	R171	R165, R72	JA6.9	-	-
			PMOD2-MOSI	R72	R165, R171	PMOD2.2	-	-
P22	97	P22	LINRXD	R167	R170, R52	U9.1	-	-
			JA6-RXDc	R170	R167, R52	JA6.12	-	-
			PMOD2-MISO	R52	R167, R170	PMOD2.3	-	-
P32	87	P32	JA2-M1TRDCLK	R177	R176	JA2.26	-	-
			JA3-D8	R176	R177	JA3.29	-	-
P31	89	P31	JA3-D9	R109	R106	JA3.30	-	-
			SERIAL-RTS	R106	R109	U6.2	-	-
P82	137	P82	JA5-M2UIN	R238, R236	R239, R241, R237, R242	JA5.12		
			JA3-ALE	R239, R236	R238, R241, R237, R242	JA3.46		
			JA3-WAIT	R241, R236	R238, R239, R237, R242	JA3.45	R75	R79
			JA6-M1UIN	R237, R236	R238, R239, R241, R242	JA6.14		
			JA6-SCKc	R242, R236	R238, R239, R241, R237	JA6.11		
PB7	39	PB7	JA2-SCKa	R192, R147	R193	JA2.10	-	-
			JA3-A4	R193, R147	R192	JA3.15	-	-
PB6	40	PB6	SERIAL-RXD	R195, R198	R148	U7.3		R194, R175
			JA2-RXDa	R195, R198	R148	JA2.8	-	-
			JA3-A3	R148	R195, R198	JA3.4	-	-
PB5	41	PB5	SERIAL-TXD	R143, R199	R146	U6.3	-	R142, R174
			JA2-TXDa	R199, R143	R146	JA2.6	-	-
			JA3-A2	R146	R143, R199	JA3.3	-	-
PB4	43	PB4	JA2-CTSaRTSa	R188	R156	JA2.12	-	-
			JA3-A1	R156	R188	JA3.2	-	-
PD5	25	PD5	E1-TDI_RXD	R231	R194, R172	E1/E2 Lite.11	-	-
			SERIAL-RXD	R194	R231, R172	U7.3	-	R195, R175
			JA6-RXDb	R172	R231, R194	JA6.7	-	
PD4	26	PD4	E1-TCK_FINEC	R101, R154	R99	E1/E2 Lite.1	-	-
			JA6-SCKb	R99, R154	R101	JA6.10	-	-
PD3	27	PD3	E1-TDO_TXD	R230	R142, R173	E1/E2 Lite.5		
			SERIAL-TXD	R142	R230, R173	U6.3	-	R143, R174
			JA6-TXDb	R173	R230, R142	JA6.8		

6.17 USB Configuration

Table 6-22 below details the function of the option links associated with the USB Configuration.

Table 6-22: USB Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PC2	45	PC2	USB0-OVRCURA	-	-	U11.5	-	-
PC1	46	PC1	USB0-VBUSEN	R98	R92	U11.4	-	-
			JA3-A16	R92	R98	JA3.37	-	-
PD2	28	PD2	USB0-VBUS	R132	R134	USB0_1.1, USB0_2.1	J14 (2-3 short) or R162	-
			JA3-A7	R134	R132	JA3.8	-	-
PE2	20	PE2	JP-UPSEL	-	-	J15.2	-	-
			JA2-NMIn	-	-	JA2.3	-	-
USB0-DP	36	-	USB0-DP	-	-	USB0_1.3	-	-
						USB0_2.3	-	-
USB0-DM	35	-	USB0-DM	-	-	USB0_1.2	-	-
						USB0_2.2	-	-

Table 6-23 below details the function of the jumpers associated with the USB Configuration.

Table 6-23: USB Configuration Jumper Option Links

Reference	Jumper Position	Explanation	Related Ref.
J12	Shorted Pin1-2	The operating voltage of VCC_USB is set to the same as the operating voltage of the MCU.	-
	Shorted Pin2-3	Operating voltage of VCC_USB is fixed at 3.3V.	-
	All open	DO NOT SET.	-
J13	Shorted Pin1-2	USB0 Host mode	-
	Shorted Pin2-3	USB0 Function mode	J14
	All open	DO NOT SET.	-
J14(DNF) *1	Shorted Pin1-2	Bus-powered	J13, R162
	Shorted Pin2-3	Self-powered	J13, R162
	All open	Self-powered by R162	R162

*1: In case of fit J14, remove R162.

7. Headers

7.1 Application Headers

This CPU board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Table 7-1: Application Header JA1 Connections

Application Header JA1					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	5V JA1-5V	-	2	0V GROUND	-
3	3V3 JA1-3V3	-	4	0V GROUND	-
5	AVCC JA1-AVCC	134,133,104	6	AVSS JA1-AVSS	135,136,106
7	AVREF NC	NC	8	ADTRG JA1-ADTRG	101,100
9	ADC0 JA1-ADC0	131	10	ADC1 JA1-ADC1	130
11	ADC2 JA1-ADC2	129	12	ADC3 JA1-ADC3	132
13	DAC0 JA1-DAC0	103	14	DAC1 JA1-DAC1	102
15	IO_0 JA1-IO0	127	16	IO_1 JA1-IO1	126
17	IO_2 JA1-IO2	125	18	IO_3 JA1-IO3	119
19	IO_4 JA1-IO4	118	20	IO_5 JA1-IO5	117
21	IO_6 JA1-IO6	116	22	IO_7 JA1-IO7	115
23	IRQd / IRQAEC / M2_HSIN0 JA1-IRQd_M2HSIN0	9/ NC / 9	24	IIC_EX NC	NC
25	IIC_SDA JA1-SDA	49	26	IIC_SCL JA1-SCL	50

Table 7-2 below lists the connections of the application header, JA2.

Table 7-2: Application Header JA2 Connections

Application Header JA2					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	RESET JA2-RESn	15	2	EXTAL JA2-EXTAL	18
3	NMI JA2-NMIn	20	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX JA2-TXDa	41
7	IRQa / WKUP / M1_HSIN0 JA2-IRQa_M1HSIN0	48 / NC / 48	8	SCIaRX JA2-RXDa	40
9	IRQb / M1_HSIN1 JA2-IRQb_M1HSIN1	50	10	SCIaCK JA2-SCKa	39
11	M1_UD JA2-M1UD	113	12	CTSaRTSa JA2-CTSaRTSa	43
13	M1_UP JA2-M1UP	3	14	M1_UN JA2-M1UN	144
15	M1_VP JA2-M1VP	2	16	M1_VN JA2-M1VN	143
17	M1_WP JA2-M1WP	1	18	M1_WN JA2-M1WN	142
19	TimerOut0 JA2-TIMOUT0	70	20	TimerOut1 JA2-TIMOUT1	29
21	TimerIn0 JA2-TIMIN0	71	22	TimerIn1 JA2-TIMIN1	30
23	IRQc / M1_EncZ / M1_HSIN2 JA2-23PIN	51 / 92 / 51	24	M1_POE JA2-M1POE	79
25	M1_TRCCLK JA2-M1TRCCLK	86	26	M1_TRDCLK JA2-M1TRDCLK	87

Table 7-3 below lists the connections of the BUS application header, JA3.

Table 7-3: Application Header JA3 Connections

Application Header JA3					
Pin	Header Name Circuit Net Name	MCU Pin	Pin	Header Name Circuit Net Name	MCU Pin
1	A0 JA3-A0	57	2	A1 JA3-A1	43
3	A2 JA3-A2	41	4	A3 JA3-A3	40
5	A4 JA3-A4	39	6	A5 JA3-A5	30
7	A6 JA3-A6	29	8	A7 JA3-A7	28
9	A8 JA3-A8	14	10	A9 JA3-A9	13
11	A10 JA3-A10	12	12	A11 JA3-A11	9
13	A12 JA3-A12	61	14	A13 JA3-A13	60
15	A14 JA3-A14	53	16	A15 JA3-A15	52
17	D0 JA3-D0	73	18	D1 JA3-D1	74
19	D2 JA3-D2	75	20	D3 JA3-D3	76
21	D4 JA3-D4	77	22	D5 JA3-D5	78
23	D6 JA3-D6	79	24	D7 JA3-D7	86
25	RDn JA3-RDn	4	26	WR / SDWE JA3-WRn	21 / NC
27	CSa JA3-CSa	47	28	CSb JA3-CSb	92
29	D8 JA3-D8	87	30	D9 JA3-D9	89
31	D10 JA3-D10	91	32	D11 JA3-D11	80
33	D12 JA3-D12	81	34	D13 JA3-D13	82
35	D14 JA3-D14	83	36	D15 JA3-D15	84
37	A16 JA3-A16	46	38	A17 JA3-A17	33
39	A18 JA3-A18	32	40	A19 JA3-A19	31
41	A20 JA3-A20	98	42	A21 NC	NC
43	A22 NC	NC	44	SDCLK JA3-BCLK	5
45	CSc / Wait JA3-45PIN	138 / 137	46	ALE / SDCKE JA3-ALE	137 / NC
47	HWRn / DQMH JA3-WRHn	22 / NC	48	LWRn / DQML JA3-WRLn	21 / NC
49	CAS NC	NC	50	RAS NC	NC

Table 7-4 below lists the connections of the application header, JA5.

Table 7-4: Application Header JA5 Connections

Application Header JA5					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	ADC4 JA5-ADC4	123	2	ADC5 JA5-ADC5	122
3	ADC6 JA5-ADC6	121	4	ADC7 JA5-ADC7	124
5	CAN1TX JA5-CAN1TX	59	6	CAN1RX JA5-CAN1RX	58
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQe / M2_EncZ / M2HSIN1 JA5-9PIN	141 / 56 / 141	10	IRQf / M2_HSIN2 JA5-M2HSIN2	NC / 12
11	M2_UD JA5-M2UD	114	12	M2_Uin JA5-M2UIN	137
13	M2_Vin JA5-M2VIN	138	14	M2_Win JA5-M2WIN	139
15	M2_Toggle JA5-M2TOGGLE	58	16	M2_POE JA5-M2POE	65
17	M2_TRCCLK JA5-M2TRCCLK	13	18	M2_TRDCLK JA5-M2TRDCLK	14
19	M2_UP JA5-M2UP	67	20	M2_Un JA5-M2UN	70
21	M2_VP JA5-M2VP	68	22	M2_Vn JA5-M2VN	71
23	M2_WP JA5-M2WP	69	24	M2_Wn JA5-M2WN	72

Table 7-5 below lists the connections of the application header, JA6.

Table 7-5: Application Header JA6 Connections

Application Header JA6					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	DREQ NC	NC	2	DACK NC	NC
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX JA6-RS232TX	NC	6	RS232RX JA6-RS232RX	NC
7	SCIbRX JA6-RXDb	25	8	SCIbTX JA6-TXDb	27
9	SCIcTX JA6-TXDc	96	10	SCIbCK JA6-SCKb	26
11	SCIcCK JA6-SCKc	137	12	SCIcRX JA6-RXDc	97
13	M1_Toggle JA6-M1TOGGLE	140	14	M1_Uin JA6-M1UIN	137
15	M1_Vin JA6-M1VIN	138	16	M1_Win JA6-M1WIN	139
17	EXT_USB_VBUS NC	NC	18	Reserved NC	NC
19	EXT_USB_BATT NC	NC	20	Reserved NC	NC
21	EXT_USB_CHG NC	NC	22	Reserved NC	NC
23	Unregulated_VCC Unregulated_VCC	-	24	Vss GROUND	-

7.2 Microcontroller Pin Headers

This RSK is fitted with MCU pin headers, which are used to access all the MCU's pins.
Table 7-6 below lists the connections of the microcontroller pin header, J1.

Table 7-6: Microcontroller Pin Header, J1

Microcontroller Pin Header J1					
Pin	Circuit Net Name	**MCU Pin**	**Pin**	Circuit Net Name	**MCU Pin**
1	JA2-M1WP	1	2	JA2-M1VP	2
3	JA2-M1UP	3	4	JA3-RDN	4
5	JA3-BCLK	5	6	UC_VCC	-
7	EMLE	7	8	GROUND	-
9	P00	9	10	NC	NC
11	MD_FINED	11	12	P01	12
13	PE4	13	14	PE3	14
15	RESn	15	16	P37	16
17	GROUND	-	18	JA2-EXTAL	18
19	UC_VCC	-	20	PE2	20
21	PE1	21	22	JA3-WRHn	22
23	E1-TRSTn	23	24	E1-TMS	24
25	PD5	25	26	PD4	26
27	PD3	27	28	PD2	28
29	PD1	29	30	PD0	30
31	JA3-A19	31	32	JA3-A18	32
33	JA3-A17	33	34	PMOD2-IO0	34
35	NC	NC	36	NC	NC

Table 7-7 below lists the connections of the microcontroller pin header, J2.

Table 7-7: Microcontroller Pin Header, J2

Microcontroller Pin Header J2					
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	GROUND	-	2	VCC_USB	38
3	PB7	39	4	PB6	40
5	PB5	41	6	UC_VCC	-
7	PB4	43	8	GROUND	-
9	USB0-OVRCURA	45	10	PC1	46
11	JA3-CSa	47	12	PB3	48
13	PB2	49	14	PB1	50
15	PB0	51	16	JA3-A15	52
17	JA3-A14	53	18	PMOD1-MISO	54
19	PMOD1-SCK	55	20	JA5-M2ENC	56
21	PA2	57	22	PA1	58
23	PA0	59	24	JA3-A13	60
25	JA3-A12	61	26	PMOD1-IO0	62
27	MOD1-IO1	63	28	UC_VCC	-
29	JA5-M2POE	65	30	GROUND	-
31	JA5-M2UP	67	32	JA5-M2VP	68
33	JA5-M2WP	69	34	P92	70
35	P91	71	36	JA5-M2WN	72

Table 7-8 below lists the connections of the microcontroller pin header, J3.

Table 7-8: Microcontroller Pin Header, J3

Microcontroller Pin Header J3					
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	JA3-D0	73	2	JA3-D1	74
3	JA3-D2	75	4	JA3-D3	76
5	JA3-D4	77	6	JA3-D5	78
7	P70	79	8	JA3-D11	80
9	JA3-D12	81	10	JA3-D13	82
11	JA3-D14	83	12	JA3-D15	84
13	PMOD2-IO1	85	14	P33	86
15	P32	87	16	UC_VCC	-
17	P31	89	18	GROUND	-
19	P30	91	20	P27	92
21	PMOD1-IO3	93	22	PMOD1-IO2	94
23	P24	95	24	P23	96
25	P22	97	26	JA3-A20	98
27	SERIAL-CTS	99	28	P32	100
29	P20	101	30	JA1-DAC1	102
31	JA1-DAC0	103	32	AVCC0-2	-
33	AVCC0-2	-	34	AVSS0-2	-
35	PMOD2-IO2	107	36	PMOD2-IO3	108

Table 7-9 below lists the connections of the microcontroller pin header, J4.

Table 7-9: Microcontroller Pin Header, J4

Microcontroller Pin Header J4					
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	LED3	109	2	LED2	110
3	LED1	111	4	LED0	112
5	JA2-M1UD	113	6	JA5-M2UD	114
7	JA1-IO7	115	8	JA1-IO6	116
9	JA1-IO5	117	10	JA1-IO4	118
11	JA1-IO3	119	12	P47	120
13	P46	121	14	P45	122
15	P44	123	16	PH4	124
17	JA1-IO2	125	18	JA1-IO1	126
19	JA1-IO0	127	20	P43	128
21	P42	129	22	P41	130
23	P40	131	24	PH0	132
25	AVCC0-2	-	26	AVCC0-2	-
27	AVSS0-2	-	28	AVSS0-2	-
29	P82	137	30	P81	138
31	P80	139	32	JA6-M1TOGGLE	140
33	P10	141	34	JA2-M1WN	142
35	JA2-M1VN	143	36	JA2-M1UN	144

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK board must be connected to a PC via an E1/E20/E2 Lite debugger. An E1/E2 Lite debugger is supplied with this RSK product.

For further information regarding the debugging capabilities of the E1/E20/E2 Lite debuggers, refer to E1/E20 Emulator, E2 Emulator Lite Additional Document for User's Manual (R20UT0399EJ).

8.2 Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip and Boot Modes (SCI), which are configured on the RSK board. Details of the modifications required can be found in §6.2. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX72T Group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E1 Emulator or E2 Emulator Lite (as supplied with this RSK) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer RX Family E1/E20 Emulator User's Manual (R20UT0398EJ) or E2 Emulator Lite User's Manual (R20UT3240EJ).

8.5 Address Space

For the MCU address space details, refer to the 'Address Space' section of RX72T Group User's Manual: Hardware.

9. Additional Information

Technical Support

For information about the RX72T Group microcontrollers refer to the RX72T Group Hardware Manual.

For information about the RX assembly language, refer to the RX Family Software Manual.

Technical Contact Details

Please refer to the contact details listed in section 8 of the "Quick Start Guide"

General information on Renesas microcontrollers can be found on the Renesas website at:
https://www.renesas.com/

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