User's Manual

32

RX72N Group

Renesas Starter Kit+ for RX72N
User's Manual

RENESAS 32-Bit MCU
RX Family / RX700 Series

Renesas Electronics
www.renesas.com

Rev. 1.00 Nov 2019

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit+ (RSK+), the user accepts the following terms:

The RSK+ is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK+ is assumed by the User. The RSK+ is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK+. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK+, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK+ product:

This Renesas Starter Kit+ is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the CPU Board hardware functionality, and electrical characteristics. It is intended for users designing sample code on the CPU Board platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RX72N Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+ hardware.	Renesas Starter Kit+ for RX72N User's Manual	R20UT4443EG
Tutorial Manual	Provides a guide to setting up RSK+ environment, running sample code and debugging programs.	Renesas Starter Kit+ for RX72N Tutorial Manual	CS+: R20UT4437EG e^2 studio: R20UT4440EG
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample.	Renesas Starter Kit+ for RX72N Quick Start Guide	CS+: R20UT4438EG e^2 studio: R20UT4441EG
Smart Configurator Tutorial	Provides a guide to code generation and importing into the e^2 studio/CS+ IDE.	Renesas Starter Kit+ for RX72N Smart Configurator Tutorial Manual	CS+: R20UT4439EG e^2 studio: R20UT4442EG
Schematics	Full detail circuit schematics of the CPU Board.	Renesas Starter Kit+ for RX72N Schematics	R20UT4435EG
Hardware Manual	Provides technical details of the RX72N microcontroller.	RX72N Group Hardware Manual	R01UH0824EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Do Not Fit
E1 / E2 Lite	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GLCDC	Graphic LCD Controller
I2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MII	Media Independent Interface
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
RTC	Real Time Clock
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer

Table of Contents

1. Overview 9
1.1 Purpose 9
1.2 Features 9
1.3 Board specification 10

2. Power Supply 11
2.1 Requirements 11
2.2 Power-Up Behaviour 11

3. Board Layout 12
3.1 Component Layout 12
3.2 Board Dimensions 13
3.3 Component Placement 14

4. Connectivity 16
4.1 Internal Board Connections 16
4.2 Debugger Connections 17

5. User Circuitry 18
5.1 Reset Circuit 18
5.2 Clock Circuit 18
5.3 Switches 18
5.4 LEDs 19
5.5 Potentiometer 19
5.6 Pmod™ 20
5.7 USB Serial Port 21
5.8 Controller Area Network (CAN) 21
5.9 Ethernet 22
5.10 Universal Serial Bus (USB) 23
5.11 External Bus 23
5.12 SDRAM 24
5.13 Renesas Serial Peripheral Interface (RSPI) 25
5.14 Quad Serial Peripheral Interface (QSPI) 25
5.15 I^2C Bus (Inter-IC Bus) 25
5.16 SD Host Interface (SDHI) 26
5.17 Parallel Data Capture Unit Interface (PDC) 26
5.18 Serial Sound Interface Enhanced (SSIE) 26
5.19 Graphic LCD Controller (GLCDC) 27
5.20 Unused terminal 28

6. Configuration 29
6.1 Modifying the RSK+ 29
6.2 MCU Operating Modes 29
6.3 E1/E2 Lite Debugger Configuration 30
6.4 Power Supply Configuration 31
6.5 Clock Configuration 31
6.6 Analog Power, ADC and DAC Configuration 32
6.7 BUS & SDRAM Configuration 33
6.8 CAN Configuration 35
6.9 Ethernet Configuration 36
6.10 General IO & LED Configuration 37
6.11 GLCDC Configuration 37
6.12 I2C & EEPROM Configuration 39
6.13 IRQ & Switch Configuration 39
6.14 MTU & POE Configuration 40
6.15 PDC Configuration 41
6.16 PMOD1 Configuration 43

6.17 PMOD2 Configuration 43
6.18 QSPI Configuration 44
6.19 RSPI Configuration 44
6.20 SDHI Configuration 44
6.21 Serial & USB to Serial Configuration 45
6.22 SSIE Configuration 46
6.23 USB Configuration 46
6.24 Unused Terminal Configuration 47

7. Headers 48
7.1 Application Headers 48

8. Code Development 53
8.1 Overview 53
8.2 Compiler Restrictions 53
8.3 Mode Support 53
8.4 Debugging Support 53
8.5 Address Space 53
8.6 Note of Flash Access Window Setting Register 53

9. Additional Information 54

1. Overview

1.1 Purpose

This CPU Board is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the CPU Board hardware.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample applications
- Sample peripheral device initialisation code

The RSK+ board contains all the circuitry required for microcontroller operation.

1.3 Board specification

Board specification was shown in **Table 1-1** below.

Table 1-1: Board Specification

Item	Specification
Microcontroller	Part No : R5F572NNDDBD or R5F572NNHDBD *3
	Package : 224-pin LFBGA
	On-Chip Memory : ROM 4MB, RAM 1MB
On-Board Memory	SDRAM: 128Mbit (Data width 16bit)
	I2C EEPROM: 2Kbit
	SPI Serial Flash: 32Mbit x 2
Input Clock	RX72N Main : 24MHz
	RX72N Sub : 32.768kHz
	RL78/G1C Main: 12MHz
	Ethernet PHY (for RMII) : 50MHz
Power Supply	DC Power Jack : 5 V Input
	Power Supply IC : 5V Input, 3.3V Output
	Power Supply IC : 5V Input, Max.38V Output(For TFT Backlight)
	Power Supply IC : 3.3V Input, 3.3V Output(For SDHI)
	Power Supply IC : 5V Input, 5V Output(For USB Host)
Debug Interface	E1/E2 Lite 14-pin box header
DIP Switch	Mode Configuration : 2-pole x 1
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer(for ADC)	Single-turn, 10kΩ
LED	5V Power indicator: green x 1
	3.3V Power Indicator : green x 1
	User : green x 1, orange x 1, red x 2
	Ethernet Status: green x 1, yellow x 1
Ethernet	Connector : RJ45 x 1
	PHY : Single Channel PHY x 1
SDHI *1	SD Card Slot (4-bit) x 1
CAN	Connector : 2.54mm pitch, 3-pin x 1
	CAN Driver : R2A25416SP *4 x 1
USB	USB0-Function : USB-MiniB
	USB0-Host : USB-TypeA
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1 : Angle type, 12-pin Connector
	PMOD2 *2 : Straight type, 12-pin Connector
GLCDC Interface (Mounts On-Board TFT Panel)	FPC Connector : 40-pin x 1 (ONTFT1)
	FPC Connector : 6-pin x 1 (ONTFT2)
PDC Interface *2	2.54 mm pitch, 20-pin x 1 (J19)
SSI Interface *2	2.54 mm pitch, 12-pin x 1 (J18)
Application Board Interface *2	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

*1: The RX72N Group incorporate an SD Host Interface (SDHI) which is compliant with the SD Specifications. When developing host devices that are compliant with the SD Specifications, the user must enter into the SD Host/Ancillary Product License Agreement (SD HALA).

*2: The connector is not included in the product.

*3: R5F572NNDDBD does not have a built-in security function, but R5F572NNHDBD has a built-in security function.

*4: This CAN driver has Non-promotion status, so do not use this CAN driver on your system.

2. Power Supply

2.1 Requirements

This board has an optional centre-positive supply connector using a 2.0mm barrel power jack (PWR). The main power supply connected to PWR should supply a minimum of 10W to ensure full functionality. When the board is connected to another system then that system should supply power to the board.

This CPU board supports one external voltage input. Details of the external power supply connection are shown in **Table 2-1 and Table 2-2** below. The default power configuration is shown in **bold, blue text.**

Table 2-1: PWR connector Requirements

Connector	Supply voltage
PWR	Input 5VDC (4.75V to 5.25V)

There are RSK+ products which supports the 12V voltage input. Since this board is supporting the 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally.
Moreover, the main power supply connected to PWR should supply a minimum of 10W to ensure full functionality.

Table 2-2: Main Power Supply Requirements

J17[*1] Setting	Supply Source	Board_5V	UC_VCC
Open	**PWR connector**/JA1-5V/Unregulated_VCC	**5V**	**3.3V**
Shorted	VBUS0	5V	3.3V

[*1]: The connector is not fitted to the RSK+.

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the ‘Release’ build of the example tutorial software pre-programmed into the Renesas microcontroller. Please consult the ‘Renesas Starter Kit+ Smart Configurator Tutorial Manual’ for further information of this example.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

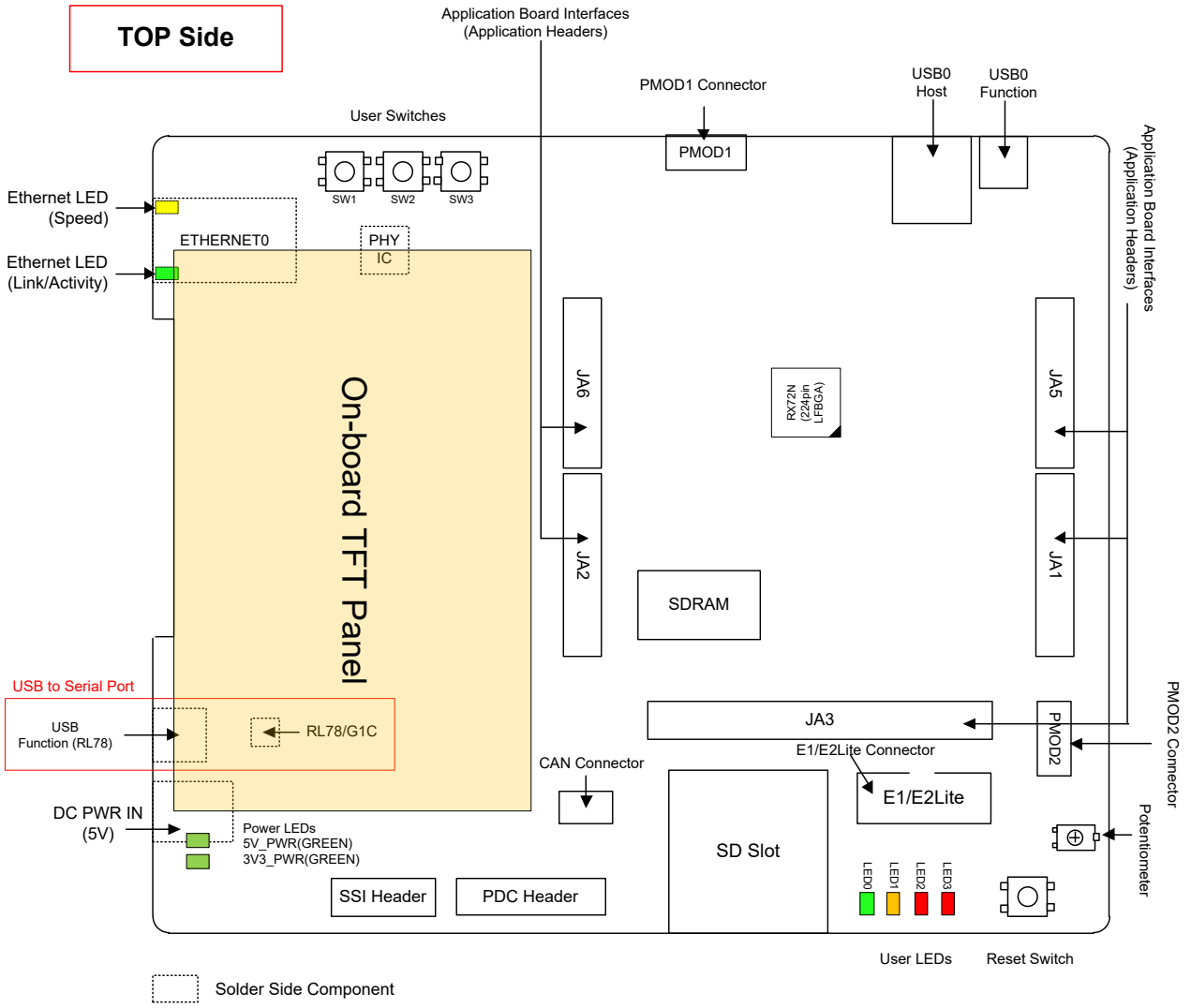

Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.

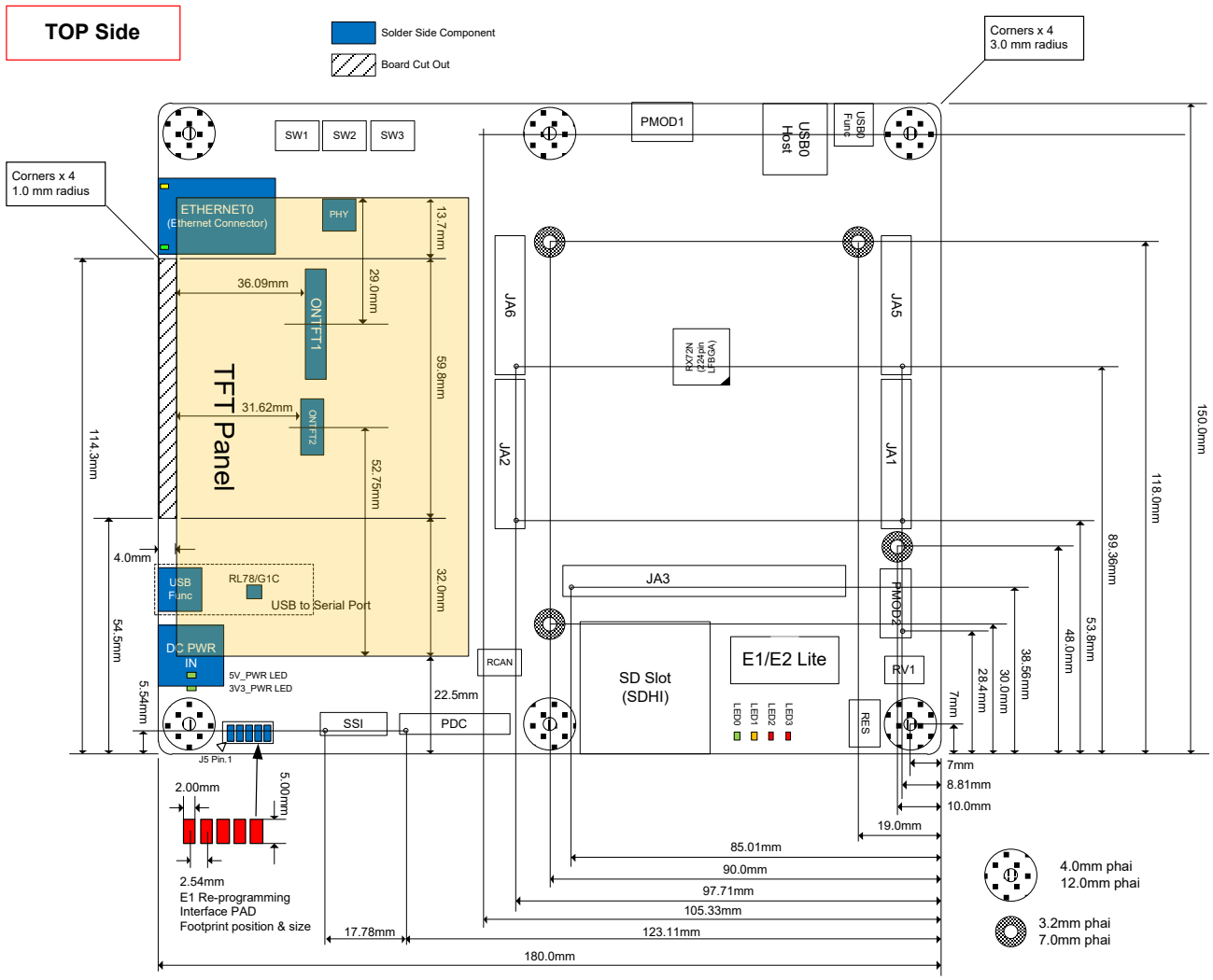

Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4**. Component types and values are shown on the board schematics.

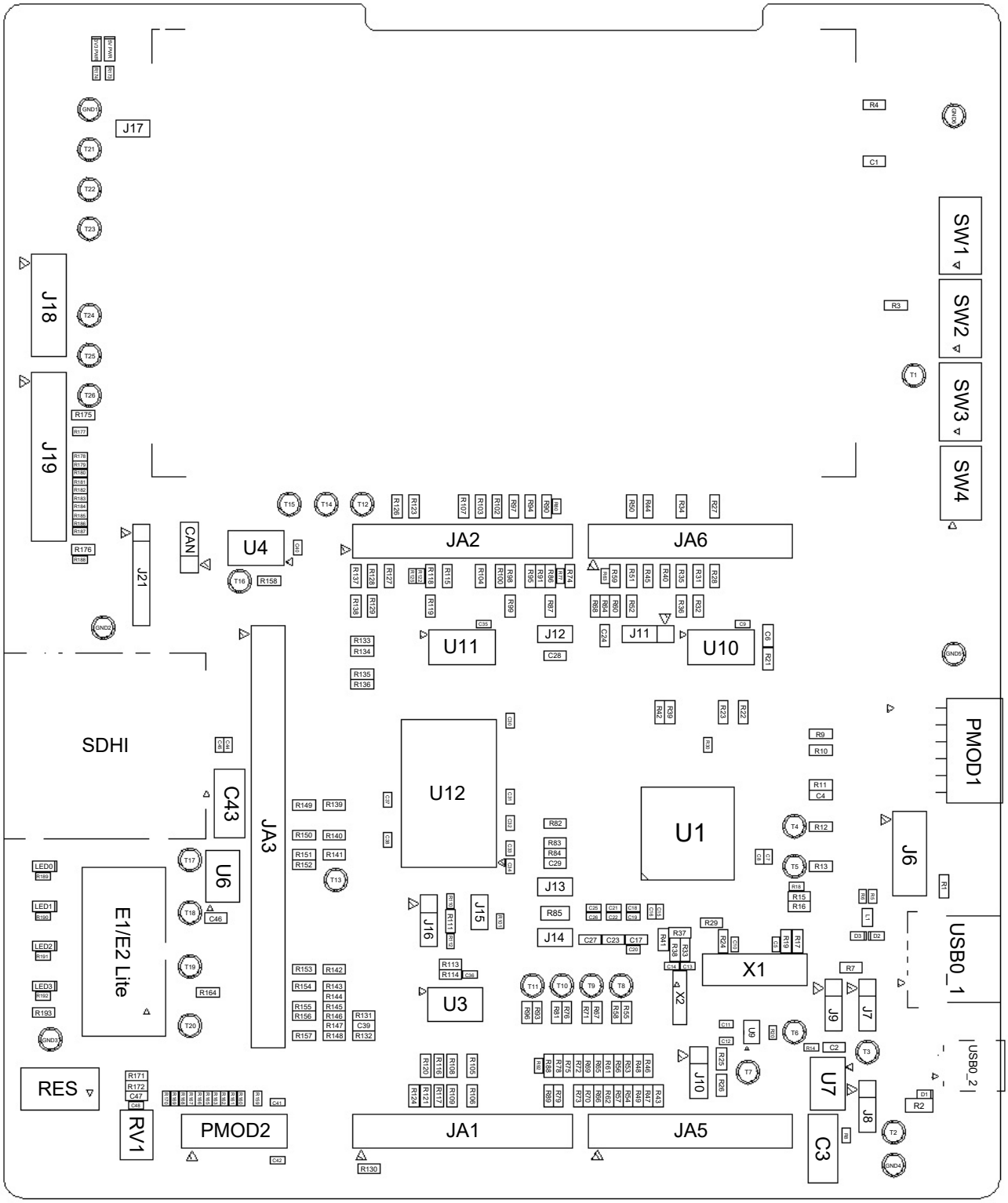

Figure 3-3: Top-Side Component Placement

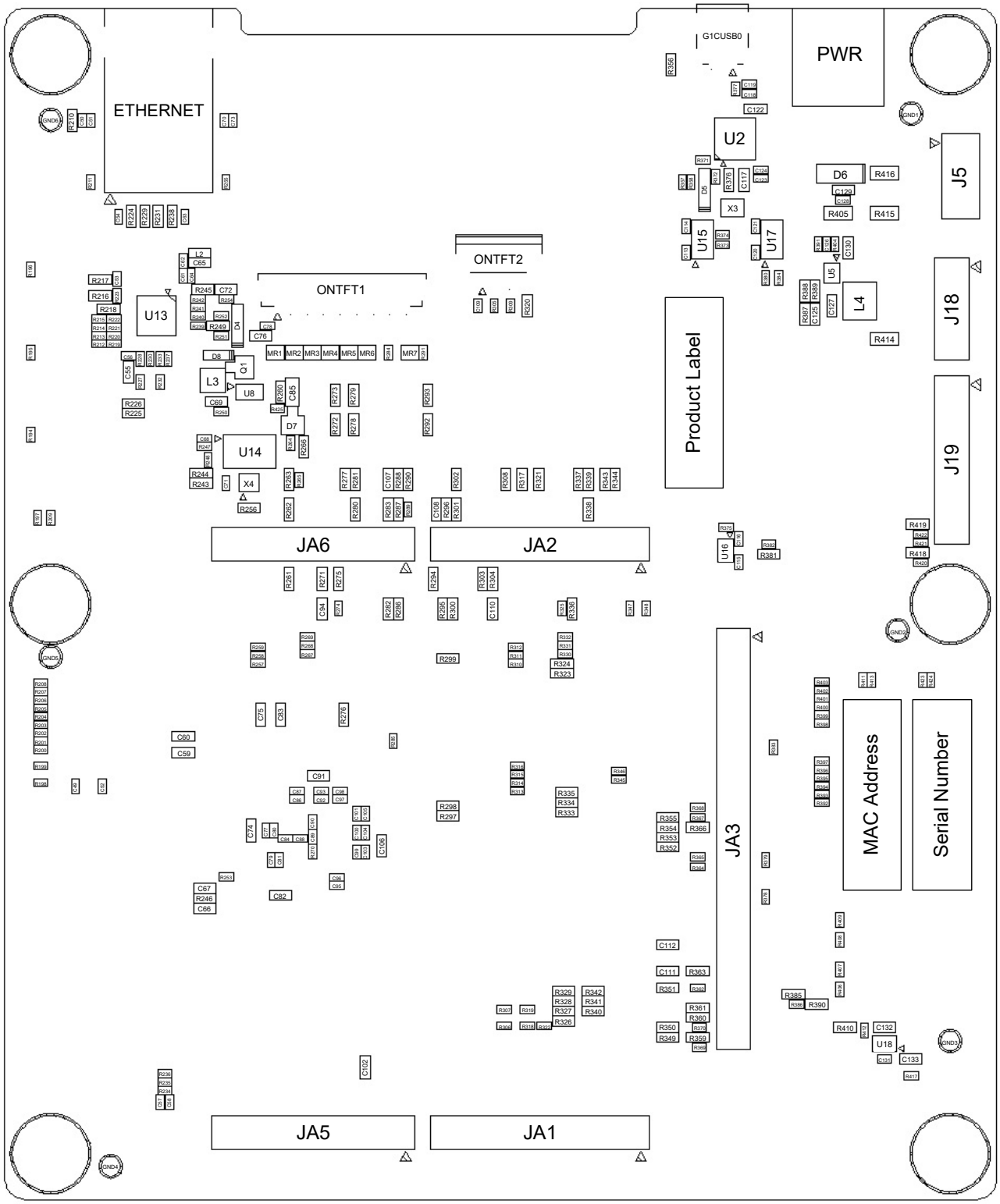

Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MCU.

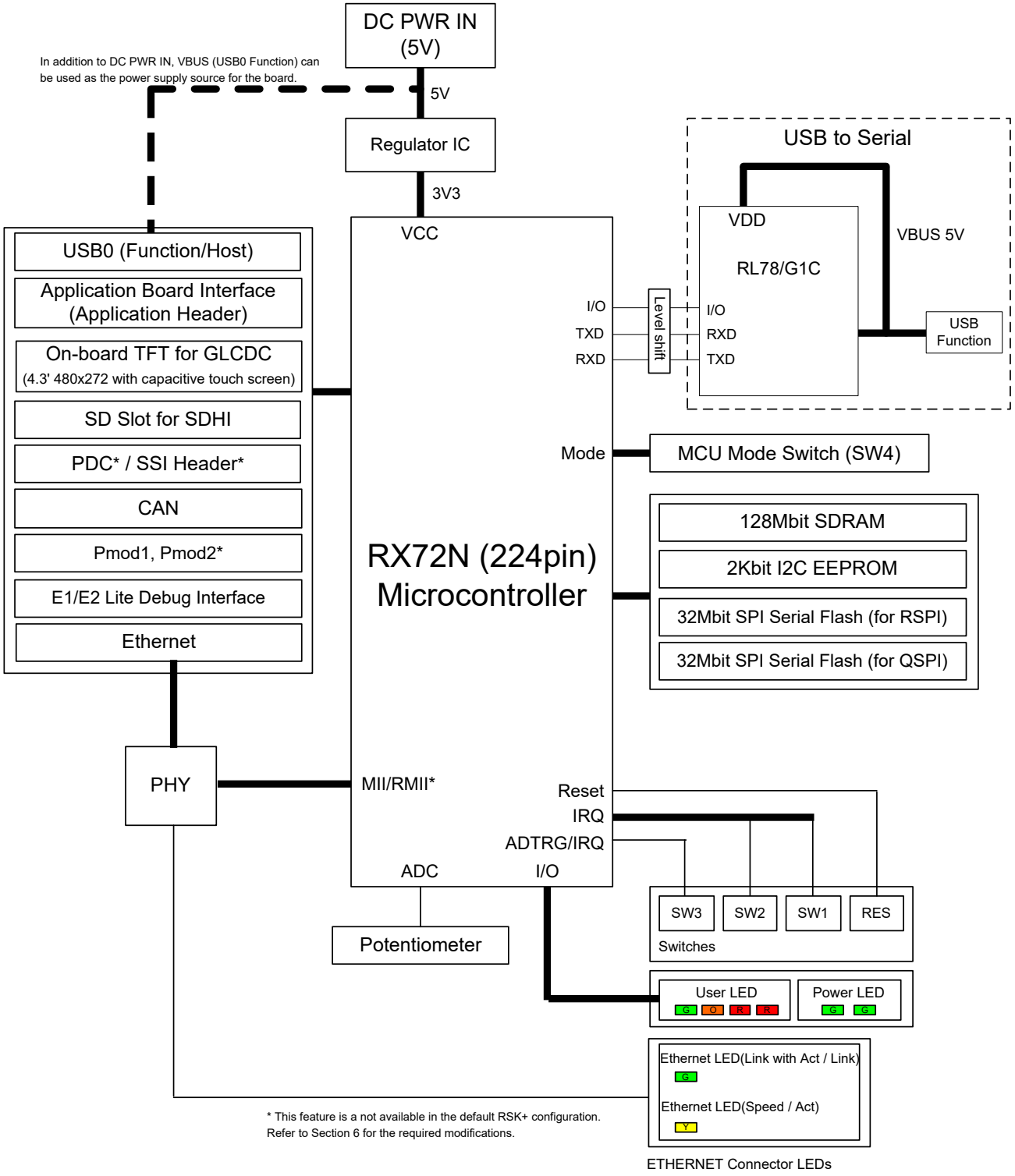

Figure 4-1: Internal Board Block Diagram

4.2 Debugger Connections

Figure 4-2 below shows the connections between the CPU board, E1/E2 Lite debugger and the host PC.

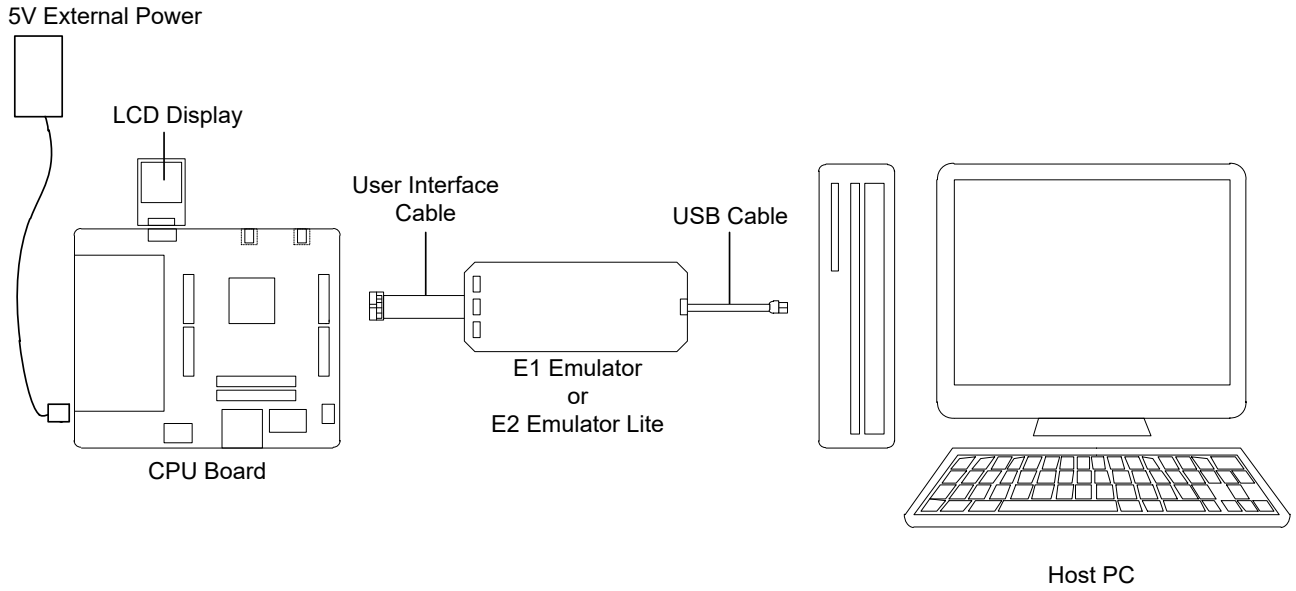

Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal, and is triggered from the RES switch. Refer to the RX72N Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX72N Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Table 5-1: Crystal

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX72N	Fitted	24MHz	Encapsulated, SMT
X2	Real time Clock for RX72N	Fitted	32.768kHz	Encapsulated, SMT
X3	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT
X4	Crystal for Ethernet (RMII)	Fitted	50MHz	Encapsulated, SMT

5.3 Switches

There are five switches located on the CPU board. The function of each switch and its connection is shown in **Table 5-2 and Table 5-3**. For further information regarding switch connectivity, refer to the CPU board schematics.

Table 5-2: Push Switch Connections

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	G7
SW1	Connects to an IRQ13-DS input for user controls.	P45	D1
SW2	Connects to an IRQ12-DS input for user controls.	P44	C4
SW3	Connects to an IRQ15 input for user controls. Connects to an ADTRG0 input for ADC controls.	P07	E5

Table 5-3: DIP Switch Connections

Switch		Function	MCU	
			Signal (Port)	Pin
SW4	Pin 1	Refer to section 6.2 for the setting contents.	MD/FINED	G4
SW4	Pin 2	Refer to section 6.2 for the setting contents.	PC7	N9

5.4 LEDs

There are 8 LEDs on the RSK+ board. The function of each LED, its colour, and its connections are shown in **Table 5-4**.

Table 5-4: LED Connections

LED	Colour	Function	MCU	
			Port	Pin
3V3 PWR	Green	Indicates the status of the Board_3V3 power rail.	NC	NC
5V PWR	Green	Indicates the status of the Board_5V power rail.	NC	NC
LED0	Green	User operated LED.	P71	J13
LED1	Orange	User operated LED.	PH6	K2
LED2	Red	User operated LED.	PL7	L10
LED3	Red	User operated LED.	PL6	M12
ETHERNET Connector	Green	Ethernet LED(Link with Activity*1 / Link)	P93	D7
ETHERNET Connector	Yellow	Ethernet LED(Speed*1 / Activity)	NC	NC

*1: Default setting of PHY.

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000, pin D4. The potentiometer can be used to create a voltage between Board_3V3 and AVSS0.
Refer to the maker site for specification of the potentiometer (VISHAY with part number TS53 series).

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX72N Group User's Manual: Hardware for further details.

5.6 Pmod™

The RSK+ board is equipped with connectors for the Digilent Pmod™ interface. Please connect an LCD module that is compatible with the PMOD1 connector.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible headers use an SPI interface. **Figure 5-1** below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-5 and Table 5-6** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011.

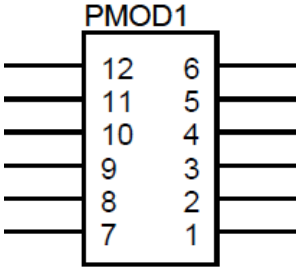

Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Table 5-5: PMOD1 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD1-CS	PH3	L1	7	PMOD1-IO0	P17	P2
2	PMOD1-MOSI	PH2	J6	8	PMOD1-IO1	P02	D6
3	PMOD1-MISO	PH1	K6	9	PMOD1-IO2	PK7	P1
4	PMOD1-SCK	PH0	N2	10	PMOD1-IO3	PL0	H11
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-6: PMOD2 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD2-CS *1	PJ5	G5	7	PMOD2-IO0	P46	B4
2	PMOD2-MOSI *1	P50	K8	8	PMOD2-IO1 *1	P00	E3
3	PMOD2-MISO *1	P52	L8	9	PMOD2-IO2	PQ3	E9
4	PMOD2-SCK *1	P51	M8	10	PMOD2-IO3	P47	D2
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.7 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RX72N Serial Communications Interface (SCI) module. Multiple options are provided to allow the selection of the connected SCI9 port. Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-7** below.

Table 5-7: Serial Port Connections

Signal Name	Function	MCU	
		Port	Pin
SERIAL-TXD	SCI1 Transmit Signal. *1	PF0	K5
	SCI9 Transmit Signal.	PL2	P12
	External RS232 Transmit Signal. *1	-	-
SERIAL-RXD	SCI1 Receive Signal. *1	PF2	J2
	SCI9 Receive Signal.	PL1	J10
	External RS232 Receive Signal. *1	-	-
SERIAL-CTS *2	Clear To Send.	P03	D3
SERIAL-RTS *2	Request To Send.	P43	E4

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

*2: Flow control is a signal provided for expansion and is not currently supported. There is no schedule of function expansion at present.

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.

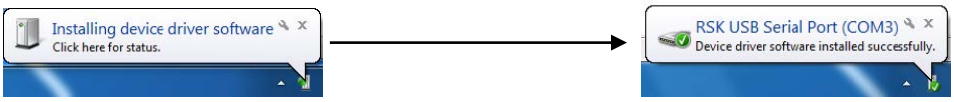

Figure 5-2: USB-Serial Windows™ Installation message

If you do not have the driver, please download the driver installer from the following URL.
https://www.renesas.com/en-eu/software/D6000699.html

5.8 Controller Area Network (CAN)

A CAN transceiver IC is fitted to the RSK+ board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX72N Group User's Manual: Hardware. The connections for the CAN microcontroller signals are listed in **Table 5-8** below.

Table 5-8: CAN Connections

CAN Signal	Function	MCU	
		Port	Pin
CAN1TX JA5-CAN1TX *1	CAN Data Transmission.	P32	H5
CAN1RX JA5-CAN1RX *1	CAN Data Reception.	P33	H4

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.9 Ethernet

When running any Ethernet software, a unique MAC address should be used. A unique Renesas allocated MAC address is attached to the PCB as a sticker, and should be always be used with this device ensured to ensure full compatibility when using other Renesas hardware on a common Ethernet connection.

An Ethernet controller IC is fitted to the CPU board, and is connected to the Ethernet MCU peripheral. The RX72N MCU supports full duplex 10Mb/s and 100Mb/s transmission and reception. Refer to §5.4 for information about the Ethernet LEDs. The connections for the Ethernet controller are listed in **Table 5-9, Table 5-10, Table 5-11** below.

Table 5-9: Ethernet Connections

Ethernet signal	Function	MCU	
		Port	Pin
ET1-TXCLK	MII: Transmit clock	PN2	G9
ET1-TXEN_RMII1TXDEN	MII/RMII: Transmit data valid	PQ7	H8
ET1-ETXD0_RMII1TXD0	MII/RMII: Transmit data 0	PQ5	E10
ET1-ETXD1_RMII1TXD1	MII/RMII: Transmit data 1	PQ6	F9
ET1-ETXD2	MII: Transmit data 2	PN0	E6
ET1-ETXD3	MII: Transmit data 3	PN1	F8
ET1-RXCLK	MII: Receive clock RMII: Reference clock *1	PQ4	E11
ET1-RXER_RMII1RXER	MII/RMII: Receive error	PN3	H9
ET1-ERXD0_RMII1RXD0	MII/RMII: Receive data 0	P94	B7
ET1-ERXD1_RMII1RXD1	MII/RMII: Receive data 1	P95	B8
ET1-ERXD2	MII: Receive data 2	P96	A8
ET1-ERXD3	MII: Receive data 3	P97	C9
ET1-COL	MII: Collision detect signal	P91	B5
ET1-CRS	MII: Carrier sense	PQ0	E7
ET1-LED0	MII/RMII: Link status input from the PHY-LSI	P93	D7
ET1-RXDV_RMII1CRSDV	MII: Receive data valid	P90	C6
	RMII: Carrier sense/receive data valid *1	PQ0	E7

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

Table 5-10: Ethernet Connections

Ethernet signal	Function	MCU	
		Port	Pin
CLKOUT25M	MII: For PHY clock 25MHz	PH7	K1
ET-MDIO	MII/RMII: Management data I/O	P30	J5
ET-MDC	MII/RMII: Management data clock	P31	J4
SW-PHYRESn *1	MII/RMII: PHY reset controlled by the reset switch on the board	-	-
ET-GPIORST *1	MII/RMII: PHY reset controlled by RX72N port PL4	PL4	R12
ET-INTn	MII/RMII: PHY Interrupt	P15	J7

*1: In the default RSK+ configuration, both the SW-PHYRESn and ET-GPIORST lines are connected to the reset pin of the Ethernet controller IC. Normally, reset is activated by SW-PHYRESn, so set port PL4 (ET-GPIORST) of the RX72N in the input direction. Refer to §6 for using ET-GPIORST as a reset.

Table 5-11: Default PHY setting

Default PHY setting items	Default PHY setting contents
PHY Address	ETHERNET (U13)=1
MII/RMII	MII
Isolate	Disable
Speed	100Mbps
Duplex	Full-Duplex
Auto negotiation	Enable

5.10 Universal Serial Bus (USB)

This CPU board is fitted with a USB Host socket (type A) and a Function socket (type Mini B). USB module USB0 is connected to the Host and Function socket, and can operate as either a Host or Function device. The connection for the USB0 module is shown in **Table 5-12** below.

Table 5-12: USB0 Module Connections

USB Signal	Function	MCU	
		Port	Pin
USB0-DP	D+ I/O pin of the USB on-chip transceiver	USB0_DP	R6
USB0-DM	D– I/O pin of the USB on-chip transceiver	USB0_DM	R5
USB0-VBUS	USB cable connection monitor pin	P16	R3
USB0-VBUSEN *1	VBUS (5V) supply enable signal for external power supply chip		
USB0-OVRCURA *1	External overcurrent detection signals A	P14	P4
USB0-OVRCURB	External overcurrent detection signals B	P22	N1

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.11 External Bus

The RX72N features an external data bus, which is connected to various devices on the CPU board. Details of the devices connected to the external data bus are listed in **Table 5-13** below. Further details of the devices connected to the external bus can be found in the board schematics.

Table 5-13: External Bus Address Space

Chip Select	Device Name	Device Description	Address Space
CS0	-	Unused	FF000000h – FFFFFFFFh (16Mbyte)
SDCS(SDRAM-SDCSn)	U12	128Mbit SDRAM	08000000h – 0FFFFFFFh (128Mbyte)
SDCS(JA3-CSb) *1	JA3	Application Header	08000000h – 0FFFFFFFh (128Mbyte)
CS1 – CS2	-	Unused	06000000h – 07FFFFFFh (2 x 16Mbyte)
CS3(JA3-CSa)	JA3	Application Header	05000000h – 05FFFFFFh (16Mbyte)
CS4 – CS5	-	Unused	03000000h – 04FFFFFFh (2 x 16Mbyte)
CS6(JA3-CSc)	JA3	Application Header	02000000h – 02FFFFFFh (16Mbyte)
CS7	-	Unused	01000000h – 01FFFFFFh (16Mbyte)

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.12 SDRAM

The RX72N features an SDRAM controller. It is connected to SDRAM on the CPU board with a 16-bit width. **Table 5-14** gives an Overview of the onboard SDRAM.

Table 5-14: Overview of the onboard SDRAM

Specification	Contents
Type name	MT48LC8M16A2P-6A
Constitution	2Meg x 16 x 4 bank
Capacity	128Mbit
Row address	12bit
Column address	9bit
Number of banks	4
Auto refresh period (tRFC)	Min. 60ns
Initialization auto refresh count	2
Precharge command period (tRP)	Min. 18ns
Auto refresh request interval	15.625us (64ms/4096)
CAS latency (CL)	2 @SDCLK:80MHz
Write recovery period (tWR)	Min. 12ns
ACTIVE-to-PRECHARGE command period (tRAS)	42ns - 120000ns
ACTIVE-to-READ or WRITE delay (tRCD)	Min. 18ns

When accessing SDRAM on the CPU board, make the following settings regardless of the operating frequency of the SDRAM clock. **Table 5-15** shows the On-board SDRAM settings.

Table 5-15: On-board SDRAM settings

Register name	Setting values	Setting details
External Bus Control Register 3 (PFBCR3.SDCLKDRV)	0b0	Use the pin with the SDCLK set for a frequency no higher than 60 MHz.
Drive Capacity Control Register (PORT6.DSCR)	0b0000000x	Normal drive output
Drive Capacity Control Register 2 (PORT6.DSCR2)		
Drive Capacity Control Register (PORT7.DSCR)	0bxxxxxxx0	
Drive Capacity Control Register 2 (PORT7.DSCR2)		
Drive Capacity Control Register (PORTA.DSCR)	0b0000000x	
Drive Capacity Control Register 2 (PORTA.DSCR2)		
Drive Capacity Control Register (PORTB.DSCR)	0bx0000000	
Drive Capacity Control Register 2 (PORTB.DSCR2)		
Drive Capacity Control Register (PORTD.DSCR)	0b00000000	
Drive Capacity Control Register 2 (PORTD.DSCR2)		
Drive Capacity Control Register (PORTE.DSCR)		
Drive Capacity Control Register 2 (PORTE.DSCR2)		

5.13 Renesas Serial Peripheral Interface (RSPI)

The RX72N features three Renesas Serial Peripheral Interface modules (Renesas SPI or RSPI). RSPI1 is connected to a 32Mbit Serial Flash. **Table 5-16** below details the connected devices, and their connections to the MCU.

Table 5-16: RSPI Connections

RSPI Signal	Function	MCU	
		Port	Pin
RSPI-CS	Chip Select	PK3	J9
RSPI-CLK	Clock	PK0	M10
RSPI-MOSI	Master out slave in data	PK1	K9
RSPI-MISO	Master in slave out data	PK2	N11

5.14 Quad Serial Peripheral Interface (QSPI)

The RX72N features one Quad Serial Peripheral Interface module (QSPI). **Table 5-17** below details the connected device, and its connection to the MCU.

Table 5-17: QSPI Connections

QSPI signal	Function	MCU	
		Port	Pin
QSPI-CS	Chip Select	PN5	J11
QSPI-CLK	Clock	PN4	L12
QSPI-IO0	I/O Data0	PJ3	H7
QSPI-IO1	I/O Data1	PJ5	G5
QSPI-IO2	I/O Data2	P00	E3
QSPI-IO3	I/O Data3	P01	D5

5.15 I²C Bus (Inter-IC Bus)

The RX72N features three I²C (Inter-IC Bus) interface modules. RIIC1 is connected to a 2Kbit EEPROM. **Table 5-18** below details the connected device, and their connection to the MCU.

Table 5-18: I²C Bus Connections

I²C Bus signal	Function	MCU	
		Port	Pin
E2P-SDA	Data	P20	P3
E2P-SCL	Clock	P21	R1

5.16 SD Host Interface (SDHI)

A SD Card Slot is fitted to the CPU board, and connected to the SD Host Interface (SDHI) MCU peripheral. For further details regarding the SDHI operation, please refer to the RX72N Group User's Manual: Hardware. The connections for the SDHI signals are listed in **Table 5-19** below.

Table 5-19: SDHI Connections

SD Card Slot (SD1)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SDHI-D3	PM5	R15	2	SDHI-CMD	PM1	F11
3	GROUND	-	-	4	SDHI-PE(SDHI-VCC)	PH4	K3
5	SDHI-CLK	PM0	G11	6	GROUND	-	-
7	SDHI-D0	PM2	K11	8	SDHI-D1	PM3	P15
9	SDHI-D2	PM4	P14	10	SDHI-CD	PM6	N13
11	GROUND	-	-	12	SDHI-WP	PM7	M13

5.17 Parallel Data Capture Unit Interface (PDC)

This CPU board is fitted with a Parallel Data Capture Unit (PDC) thru-hole pattern. The connections for the PDC signals are listed in **Table 5-20** below.

Table 5-20: PDC Connections

PDC Header (J19)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_5V	-	-	2	Board_3V3	-	-
3	GROUND	-	-	4	GROUND	-	-
5	PDC-PCKO *1	P33	H4	6	PDC-RESn	RESn	G7
						PL5 *1	M11
7	GROUND	-	-	8	PDC-PIXCLK	P24	L4
9	PDC-VSYNC *1	P32	H5	10	PDC-HSYNC	P25	M3
11	PDC-PIXD7	P23	M2	12	PDC-PIXD6 *1	P22	N1
13	PDC-PIXD5 *1	P21	R1	14	PDC-PIXD4 *1	P20	P3
15	PDC-PIXD3 *1	P17	P2	16	PDC-PIXD2	P87	R2
17	PDC-PIXD1	P86	N3	18	PDC-PIXD0 *1	P15	J7
19	PDC-SSDA *1	PM2	K11	20	PDC-SSCL *1	PM1	F11

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.18 Serial Sound Interface Enhanced (SSIE)

This CPU board is fitted with a Serial Sound Interface Enhanced Unit (SSIE) thru-hole pattern. The connections for the SSIE signals are listed in **Table 5-21** below.

Table 5-21: SSIE Connections

SSIE Header (J18)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_5V	-	-	2	Board_3V3	-	-
3	GROUND	-	-	4	GROUND	-	-
5	SSI-AUDIOCLK *1	P22	N1	6	GROUND	-	-
7	GROUND	-	-	8	NC	-	-
9	SSI-SCK *1	P23	M2	10	SSI-RXD *1	PJ5	G5
11	SSI-LRCK	PF5	G6	12	SSI-TXD *1	P17	P2

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.19 Graphic LCD Controller (GLCDC)

The RX72N features a graphic LCD controller (GLCDC) built in and is connected to via the FPC connector to NHD - 4.3 - 480272EF - ATXL - CTP manufactured by Newhaven Display International, Inc.
Table 5-22 and Table 5-23 show the connection relationship of the GLCDC interface.

Table 5-22: GLCDC Connections(1)

GLCDC (ONTFT1) *1							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	OnTFT-LEDK	-	-	2	OnTFT-LEDA	-	-
3	GROUND	-	-	4	Board_3V3	-	-
5	OnTFT-R5(R0) *2	P81	L9	6	OnTFT-R6(R1) *2	P80	N10
7	OnTFT-R7(R2) *2	PC4	P11	8	OnTFT-R3	PC5	R10
9	OnTFT-R4	P82	P10	10	OnTFT-R5	P81	L9
11	OnTFT-R6	P80	N10	12	OnTFT-R7	PC4	P11
13	OnTFT-G6(G0) *2	PC7	N9	14	OnTFT-G7(G1) *2	PC6	R9
15	OnTFT-G2	P55	R8	16	OnTFT-G3	P54	R7
17	OnTFT-G4	P11	P8	18	OnTFT-G5	P83	M9
19	OnTFT-G6	PC7	N9	20	OnTFT-G7	PC6	R9
21	OnTFT-B5(B0) *2	P84	M6	22	OnTFT-B6(B1) *2	P57	P7
23	OnTFT-B7(B2) *2	P56	N7	24	OnTFT-B3	PJ0	M5
25	OnTFT-B4	P85	N4	26	OnTFT-B5	P84	M6
27	OnTFT-B6	P57	P7	28	OnTFT-B7	P56	N7
29	GROUND	-	-	30	OnTFT-CLK	P14	P4
31	OnTFT-DISP	PK4	F4	32	OnTFT-HSYNC	PJ2	L6
33	OnTFT-VSYNC	P13	N5	34	OnTFT-DEN	PJ1	N6
35	NC	-	-	36	GROUND	-	-
37	NC	-	-	38	NC	-	-
39	NC	-	-	40	NC	-	-

*1: Connection driver: ST7282T2 manufactured by Sitronix Technology Corp.
*2: Normalization from RGB 565 to RGB 888.

Table 5-23: GLCDC Connections(2)

GLCDC (ONTFT2)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_3V3	-	-	2	GROUND	-	-
3	OnTFT-SCL*3	PQ1	E8	4	OnTFT-SDA*3	PQ2	G8
5	OnTFT-INT	P10	K7	6	OnTFT-RESn	RESn	G7
						PL3 *4	K10

*3: Simple I2C bus is used for TFT touch interface.
Connection touch controller: FT5426 manufactured by Focal Tech, Inc.
Slave address (A6-0): 0111000.
*4: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.20 Unused terminal

The pins of the RX72N microcontroller not used on this board are connected to the header J6. **Table 5-24** shows the connection of unused pins.

Table 5-24: Unused terminal

Unused terminal(J6)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	P60TERM	P60	C10	2	P72TERM	P72	K15
3	P74TERM	P74	R14	4	P75TERM	P75	R13
5	P76TERPM	P76	N12	6	P77TERM	P77	L11
7	P92TERM	P92	A5	8	PH5TERM	PH5	K4
9	PK5TERM	PK5	F5	10	PK6TERM	PK6	F7

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX72N Group User's Manual: Hardware and CPU board schematics for further information.

In the table in this section, "pin" expression is omitted, so please read as follows.
Example: U9.4 -> U9.4pin
J7(1-2 short) -> J7(1pin-2pin short)

6.2 MCU Operating Modes

Table 6-1 below details the option links associated with configuring the MCU Operating Modes.

Table 6-1: MCU Operating Modes Switch Settings

SW4 Pin1	SW4 Pin2	J15 *1	Configuration	Related Links
OFF	**OFF (don't care)**	**Open (don't care)**	**Single Chip Mode**	**R274**, R275, R40, **J11**
OFF	**OFF**	**Open (don't care)**	**Boot Mode(FINE Interface)** *2	**R274**, R275, R40, **J11**
ON	OFF	don't care	SCI Boot Mode	**R274**, R275, R40, **J11**
ON	ON	Open	USB Boot Mode (Bus-powered)	**R274**, R275, R40, **J11**
		Shorted	USB Boot Mode (Self-powered)	**R274**, R275, R40, **J11**

*1: Jumper J15 is not mounted on the board at the time of product shipment.

*2: To use the FINE interface, mode control by the E1 / E2 Lite debugger is required.

6.3 E1/E2 Lite Debugger Configuration

Table 6-2 below details the function of the option links associated with E1/E2 Lite Debugger Configuration.

Table 6-2: E1/E2 Lite Debugger Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PC7	N9	PC7	**OnTFT-G6**	**J11 (1-2pin short)**	**R275, R40**	**ONTFT1.13**	-	-
						ONTFT1.19	-	-
			EMU-UB	J11 (2-3pin short)	**R275, R40**	E1.10	-	-
			DSW-UB			SW4.2	-	-
			JA2-M1TRDCLK	R275	J11 (open), **R40**	JA2.26	-	-
			JA6-TXDc	R40	J11 (open), **R275**	JA6.9	-	-
EMU-TRSTn	F3	PF4	**EMU-TRSTn**	-	-	**E1.3**	-	-
EMU-TMS	J3	PF3	**EMU-TMS**	-	-	**E1.9**	-	-
PF2	J2	PF2	**EMU-TDI_RXD**	**R338**	**R339, R123**	**E1.11**	-	-
			SERIAL-RXD	R339	R338, **R123**	U15.3	-	**R50,** R337
			JA2-RXDa	R123	R338, **R339**	JA2.8	-	-
PF1	L3	PF1	**EMU-TCK**	**R385, R11**	**R164**	**E1.1**	-	-
			JA2-SCKa	R164, **R11**	R385	JA2.10	-	-
PF0	K5	PF0	**EMU-TDO_TXD**	**R344**	**R343, R126**	**E1.5**	-	-
			SERIAL-TXD	R343	R344, **R126**	U17.3	-	**R51,** R52
			JA2-TXDa	R126	R344, **R343**	JA2.6	-	-
RESn	G7	-	**EMU-RESn**	-	-	**E1.13**	-	-
			SW-RESn	-	-	**RES1(Switch)**	-	-
			JA2-RESn	-	-	**JA2.1**	-	-
			PDC-RESn	**R137**	**R138**	**J19.6**	**R175**	-
			OnTFT-RESn	**R128**	**R129**	**ONTFT2.6**	**R320**	-
EMLE	F6	-	**EMU-EMLE**	-	-	**E1.4**	-	-
			JP-EMLE	-	-	**J16.2**	**R111**	-
MD_FINED	G4	-	**EMU-MD_FINED**	-	-	**E1.7**	-	-
			DSW-MD_FINED	-	-	**SW4.1**	-	-

Table 6-3 below details the function of the jumpers associated with the E1/E2 Lite Debugger.

Table 6-3: E1/E2 Lite Debugger Configuration Jumper Settings

Reference	Jumper Position	Configuration	Related Links
J16(DNF) *1	**Shorted Pin1-2**	**Enable E1/E2 Lite normal debugging and MCU single operation (without E1/E2 Lite).**	**R111**
	Shorted Pin2-3	Enable E1/E2 Lite debugging with Hot plug-in function.	
	All open	DO NOT SET.	-

*1: Jumper J16 is not fitted on the default CPU board. Same as Jumper Position “shorted pin1-2” setting by resistor R111.

6.4 Power Supply Configuration

Table 6-4 below details the function of the option links associated with Power Supply Configuration.

Table 6-4: Power Supply Configuration Option Links

Reference	Configuration	Fit	DNF	Related Links
VBUS0	Connect 5V Power rail to VBUS0.	J17.shorted, **J8.Pin1-2**	-	**U5.1, U5.2**
Unregulated_VCC	**Connect 5V power rail to Unregulated_VCC.**	**R405**	-	**U5.1, U5.2**
JA1-5V	**Connect 5V power rail to JA1-5V.**	**R415**	-	**U5.1, U5.2**
USB_5V	**Connect 5V power rail to USB_5V.**	**R416**	-	**U7.2, U7.3, U9.6**
Board_5V	**Connect 5V power rail to Board_5V.**	-	-	**U5.1, U5.2**, U3.8
SD_3V3	**Connect 3.3V power rail to SD_3V3.**	**R414**	-	**U6.2, U6.3**
JA1-3V3	**Connect 3.3V power rail to JA1-3V3.**	**R130**	-	**JA1.3**
Board_3V3	**Connect 3.3V power rail to Board_3V3.**	-	-	**U3.8 and many devices**
UC_VCC	**Connect 3.3V power rail to UC_VCC.**	J14.Short or **R85**	-	**U1, R13, R71, R81**
	Enable current probe for measurement MCU current consumption.	-	**J14.Open** and R85	**U1, R13, R71, R81**
VBATT	**Connect UC_VCC power rail to VBATT.**	**R83**	**R84**	**U1**
	J13 connected to VBATT of MCU	R84	R83	**U1**

*1: J13 is a power connector for VBATT, not a jumper. Do not short-circuit J13 Pin 1 and Pin 2 because the power supply is directly connected to ground.

Table 6-5 below details the function of the jumpers associated with the Power Supply Configuration.

Table 6-5: Power Supply Configuration Jumper Settings

Reference	Jumper Position	Configuration	Related Links
J14(DNF) *1	**Shorted**	**Connect 3.3V power rail to UC_VCC.**	**R85**
	All open	Enable current probe for measurement MCU current consumption.	
J17(DNF) *2	Shorted	Enable VBUS0.	**J9**
	All open	**Disable VBUS0**	**J9**

*1: Jumper J14 is not fitted on the default CPU board. Fitting resistor R85 has the same effect as "shorting" jumper J14.

*2: Jumper J17 is not fitted on the default CPU board.

6.5 Clock Configuration

Table 6-6 below details the function of the option links associated with Clock Configuration.

Table 6-6: Clock Configuration Option Links

Reference	Configuration	Fit	DNF	Related Links
XTAL, EXTAL	**Connect 24MHz crystal (X1) to RX72N.**	**R19, R24**	**R17, R29**	**U1.H1, U1.J1**
	Connect JA2-EXTAL to RX72N.	R17	R19, R24, **R29**	U1.J1
XCIN, XCOUT	**Connect 32.768kHz crystal (X2) to RX72N.**	**R38, R33**	**R41, R37**	**U1.F1, U1.G1**
	Disconnect X2 from RX72N.	R41	R38, R33, **R37**	-

6.6 Analog Power, ADC and DAC Configuration

Table 6-7 below details the function of the option links associated with Analog Power, ADC and DAC Configuration.

Table 6-7: Analog Power, ADC and DAC Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07 *1	E5	P07	**SW3**	**R88**	**R124, R89**	**SW3**	-	-
			JA1-ADTRG	R124	R88, **R89**	JA1.8	R124	**R292**
			JA1-IRQd	R89	R88, **R124**	JA1.23	-	-
JA1-DAC1	C3	P05	**JA1-DAC1**	-	-	**JA1.14**	-	-
P03	D3	P03	**SERIAL-CTS**	**R105**	**R106**	**U15.2**	-	-
			JA1-DAC0	R106	R105	JA1.13	-	-
P13	N5	P13	**OnTFT-VSYNC**	**R293**	**R292**	**ONTFT1.33**	-	-
			JA1-ADTRG	R292	R293	JA1.8	R292	**R124**
P43	E4	P43	**SERIAL-RTS**	**R108**	**R109**	**U17.2**	-	-
			JA1-ADC3	R109	R108	JA1.12	-	-
JA1-ADC2	B3	P42	**JA1-ADC2**	-	-	**JA1.11**	-	-
P41	A4	P41	SDHI-POWFLT	R120	R121	U6.5	-	-
			JA1-ADC1	**R121**	**R120**	**JA1.10**	-	-
P40	D4	P40	**RV1-ADC**	**R116**	**R117**	**RV1**	-	-
			JA1-ADC0	R117	R116	JA1.9	-	-
PE5	C13	PE5	**SDRAM-D13**	**R56**	**R57**	**U12.50**	-	-
			JA3-D13			**JA3.34**	-	-
			JA5-ADC7	R57	R56	JA5.4	-	-
PE4	B14	PE4	**SDRAM-D12**	**R53**	**R54**	**U12.48**	-	-
			JA3-D12			**JA3.33**	-	-
			JA5-ADC6	R54	R53	JA5.3	-	-
PE3	D12	PE3	**SDRAM-D11**	**R65**	**R66**	**U12.47**	-	-
			JA3-D11			**JA3.32**	-	-
			JA5-ADC5	R66	R65	JA5.2	-	-
PE2	B13	PE2	**SDRAM-D10**	**R61**	**R62**	**U12.45**	-	-
			JA3-D10			**JA3.31**	-	-
			JA5-ADC4	R62	R61	JA5.1	-	-
VREFH0	A2	-	**UC_VCC**	**R81**	**R76**	-	-	-
			JA1-VREFH	R76	R81	JA1.7	-	-
VREFL0	A3	-	**GROUND**	**R96**	**R93**	-	-	-
			JA1-AVSS	R93	R96	JA1.6	-	-
AVCC0-1	B2, C2	-	**UC_VCC**	**R71**	**R171, R67** or R172, **R67**	-	-	-
			JA1-AVCC	R67	**R171,** R71 or R172, R71	JA1.5	-	-
			Board_3V3	**R171**, R172	R71, **R67**	-	-	-
AVSS0-1	B1, C1	-	**GROUND**	**R58**	**R55**	-	-	-
			JA1-AVSS	R55	R58	JA1.6	-	-

*1: When changing the option link of P07, pay attention to the presence or absence of a pull-up resistor. Leave the pull-up resistor for SW3 (R194) fitted, otherwise the internal pull-up in the MCU will need to be enabled.

6.7 BUS & SDRAM Configuration

Table 6-8, Table 6-9, Table 6-10 below details the function of the option links associated with BUS & SDRAM Configuration.

Table 6-8: BUS & SDRAM Configuration Option Links(1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P10	K7	P10	**OnTFT-INT**	**R263**	**R262, R27**	**ONTFT2.5**	-	-
			JA3-ALE	R262	R263, **R27**	JA3.46	**R361**	**R155**
			JA6-M1WIN	R27	R263, **R262**	JA6.16	-	-
JA3-CSc	M1	P26	**JA3-CSc**	-	-	**JA3.45**	**R15**	**R154**
JA3-BCLK	J8	P53	**JA3-BCLK**	**R142**	-	**JA3.44**	**R153**	**R363**
P52	L8	P52	**JA3-RDn**	**R149**	**R139**	**JA3.25**	-	-
			PMOD2-MISO	R139	R149	PMOD2.3	-	-
P51	M8	P51	**JA3-WRHn**	**R148, R131**	**R132**	**JA3.47**	**R157**	**R359**
			PMOD2-SCK	R132, **R131**	R148	PMOD2.4	-	-
P50	K8	P50	**JA3-WRn**	**R140**	**R352, R353**	**JA3.26**	**R150**	**R366**
			JA3-WRLn	R352	R140, **R353**	JA3.48	R156	**R360**
			PMOD2-MOSI	R353	R140, **R352**	PMOD2.2	-	-
P67	D15	P67	**SDRAM-DQMH**	**R350**	**R349**	**U12.39**	-	-
			JA3-DQMH	R349	R350	JA3.47	R359	R157
P66	C15	P66	**SDRAM-DQML**	**R146**	**R147**	**U12.15**	-	-
			JA3-DQML	R147	R146	JA3.48	R360	**R156**
P65	C14	P65	**SDRAM-CKE**	**R144**	**R145**	**U12.37**	-	-
			JA3-CKE	R145	R144	JA3.46	R155	R361
P64	C11	P64	**SDRAM-WEn**	**R355**	**R354**	**U12.16**	-	-
			JA3-WEn	R354	R355	JA3.26	R366	R150
P63	B12	P63	**SDRAM-CASn**	-	-	**U12.17**	-	-
			JA3-CAS	-	-	**JA3.49**	-	-
P62	A13	P62	**SDRAM-RASn**	-	-	**U12.18**	-	-
			JA3-RAS	-	-	**JA3.50**	-	-
P61	A12	P61	**SDRAM-SDCSn**	**R141**	**R151**	**U12.19**	-	-
			JA3-CSb	R151	R141	JA3.28	-	-
JA3-CSa	H10	P73	**JA3-CSa**	**R152**	-	**JA3.27**	-	-
P70	A15	P70	**SDRAM-SDCLK**	**R335, R334**	**R333**	**U12.38**	-	-
			JA3-SDCLK	R333, **R334**	R335	JA3.44	R363	R153
PA7	J15	PA7	**SDRAM-A7**	-	-	**U12.31**	-	-
			JA3-A7	-	-	**JA3.8**	-	-
PA6	H14	PA6	**SDRAM-A6**	-	-	**U12.30**	-	-
			JA3-A6	-	-	**JA3.7**	-	-
PA5	H15	PA5	**SDRAM-A5**	-	-	**U12.29**	-	-
			JA3-A5	-	-	**JA3.6**	-	-
PA4	G15	PA4	**SDRAM-A4**	-	-	**U12.26**	-	-
			JA3-A4	-	-	**JA3.5**	-	-
PA3	G14	PA3	**SDRAM-A3**	-	-	**U12.25**	-	-
			JA3-A3	-	-	**JA3.4**	-	-
PA2	G13	PA2	**SDRAM-A2**	-	-	**U12.24**	-	-
			JA3-A2	-	-	**JA3.3**	-	-
PA1	G12	PA1	**SDRAM-A1**	-	-	**U12.23**	-	-
			JA3-A1	-	-	**JA3.2**	-	-

Table 6-9: BUS & SDRAM Configuration Option Links(2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
JA3-A0	F12	PA0	**JA3-A0**	-	-	**JA3.1**	-	-
JA3-A15	N15	PB7	**JA3-A15**	-	-	**JA3.16**	-	-
PB6	M15	PB6	**SDRAM-A14**	-	-	**U12.21**	-	-
			JA3-A14	-	-	**JA3.15**	-	-
PB5	K13	PB5	**SDRAM-A13**	-	-	**U12.20**	-	-
			JA3-A13	-	-	**JA3.14**	-	-
PB4	L15	PB4	**SDRAM-A12**	-	-	**U12.35**	-	-
			JA3-A12	-	-	**JA3.13**	-	-
PB3	K14	PB3	**SDRAM-A11**	-	-	**U12.22**	-	-
			JA3-A11	-	-	**JA3.12**	-	-
PB2	L14	PB2	**SDRAM-A10**	-	-	**U12.34**	-	-
			JA3-A10	-	-	**JA3.11**	-	-
PB1	J12	PB1	**SDRAM-A9**	-	-	**U12.33**	-	-
			JA3-A9	-	-	**JA3.10**	-	-
PB0	J14	PB0	**SDRAM-A8**	-	-	**U12.32**	-	-
			JA3-A8	-	-	**JA3.9**	-	-
PC6	R9	PC6	JA3-A22	R278	R279	JA3.43	-	-
			OnTFT-G7	**R279**	**R278**	**ONTFT1.14**	-	-
						ONTFT1.20	-	-
PC5	R10	PC5	JA3-A21	R272	R273	JA3.42	-	-
			OnTFT-R3	**R273**	**R272**	**ONTFT1.8**	-	-
PC4	P11	PC4	**OnTFT-R7**	**R302, R296**	**R301, R90**	**ONTFT1.7**	-	-
						ONTFT1.12	-	-
			JA3-A20	R301, **R296**	R302, **R90**	JA3.41	-	-
			JA2-M1POE	R90, **R296**	R302, **R301**	JA2.24	-	-
JA3-A19	R11	PC3	**JA3-A19**	-	-	**JA3.40**	-	-
JA3-A18	P13	PC2	**JA3-A18**	-	-	**JA3.39**	-	-
PC1	N14	PC1	**JA3-A17**	**R32**	**R31**	**JA3.38**	-	-
			JA6-M1TOGGLE	R31	R32	JA6.13	-	-
JA3-A16	M14	PC0	**JA3-A16**	-	-	**JA3.37**	-	-
PD7	A11	PD7	**SDRAM-D7**	-	-	**U12.13**	-	-
			JA3-D7	-	-	**JA3.24**	-	-
PD6	B10	PD6	**SDRAM-D6**	-	-	**U12.11**	-	-
			JA3-D6	-	-	**JA3.23**	-	-
PD5	D9	PD5	**SDRAM-D5**	-	-	**U12.10**	-	-
			JA3-D5	-	-	**JA3.22**	-	-
PD4	B9	PD4	**SDRAM-D4**	-	-	**U12.8**	-	-
			JA3-D4	-	-	**JA3.21**	-	-
PD3	A9	PD3	**SDRAM-D3**	-	-	**U12.7**	-	-
			JA3-D3	-	-	**JA3.20**	-	-
PD2	A7	PD2	**SDRAM-D2**	-	-	**U12.5**	-	-
			JA3-D2	-	-	**JA3.19**	-	-
PD1	C7	PD1	**SDRAM-D1**	-	-	**U12.4**	-	-
			JA3-D1	-	-	**JA3.18**	-	-
PD0	A6	PD0	**SDRAM-D0**	-	-	**U12.2**	-	-
			JA3-D0	-	-	**JA3.17**	-	-

Table 6-10: BUS & SDRAM Configuration Option Links(3)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PE7	B15	PE7	**SDRAM-D15**	-	-	**U12.53**	-	-
			JA3-D15	-	-	**JA3.36**	-	-
PE6	E13	PE6	**SDRAM-D14**	-	-	**U12.51**	-	-
			JA3-D14	-	-	**JA3.35**	-	-
PE5	C13	PE5	**SDRAM-D13**	**R56**	**R57**	**U12.50**	-	-
			JA3-D13			**JA3.34**	-	-
			JA5-ADC7	R57	R56	JA5.4	-	-
PE4	B14	PE4	**SDRAM-D12**	**R53**	**R54**	**U12.48**	-	-
			JA3-D12			**JA3.33**	-	-
			JA5-ADC6	R54	R53	JA5.3	-	-
PE3	D12	PE3	**SDRAM-D11**	**R65**	**R66**	**U12.47**	-	-
			JA3-D11			**JA3.32**	-	-
			JA5-ADC5	R66	R65	JA5.2	-	-
PE2	B13	PE2	**SDRAM-D10**	**R61**	**R62**	**U12.45**	-	-
			JA3-D10			**JA3.31**	-	-
			JA5-ADC4	R62	R61	JA5.1	-	-
PE1	A14	PE1	**SDRAM-D9**	-	-	**U12.44**	-	-
			JA3-D9	-	-	**JA3.30**	-	-
PE0	D11	PE0	**SDRAM-D8**	-	-	**U12.42**	-	-
			JA3-D8	-	-	**JA3.29**	-	-
PF5	G6	PF5	**SSI-LRCK**	**R351**	**R143**	**J18.11**	-	-
			JA3-WAIT	R143	R351	JA3.45	R154	R15

6.8 CAN Configuration

Table 6-11 below details the function of the option links associated with CAN Configuration.

Table 6-11: CAN Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P33	H4	P33	**CAN1RX**	**R46, R48**	**R43, R49**	**U4.4**	-	-
			PDC-PCKO	R43, **R48**	R46, **R49**	J19.5	-	-
			JA5-CAN1RX	R49, **R48**	R46, **R43**	JA5.6	-	-
P32	H5	P32	**CAN1TX**	**R300**	**R87, R47, R295**	**U16.3**	-	-
			JA2-IRQc_M1HSIN2	R87	R300, **R47, R295**	JA2.23	**R86**	**R91**
			JA5-CAN1TX	R47	R300, **R87, R295**	JA5.5	-	-
			PDC-VSYNC	R295	R300, **R87, R47**	J19.9	-	-

6.9 Ethernet Configuration

Table 6-12, Table 6-13 below details the function of the option links associated with Ethernet Configuration.

Table 6-12: Ethernet Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ET1-ERXD3	C9	P97	**ET1-ERXD3**	-	-	**U13.13**	-	-
ET1-ERXD2	A8	P96	**ET1-ERXD2**	-	-	**U13.14**	-	-
ET1-ERXD1_RMII1RXD1	B8	P95	**ET1-ERXD1_RMII1RXD1**	-	-	**U13.15**	-	-
ET1-ERXD0_RMII1RXD0	B7	P94	**ET1-ERXD0_RMII1RXD0**	-	-	**U13.16**	-	-
ET1-LED0	D7	P93	**ET1-LED0**	-	-	**ETHERNET.11**	-	-
						U13.30	-	-
ET1-COL	B5	P91	**ET1-COL**	-	-	**U13.28**	-	-
ET1-RXDV	C6	P90	**ET1-RXDV_RMII1CRSDV**	**R39**	**R276**	**U13.18**	-	-
ET1-RXER_RMII1RXER	H9	PN3	**ET-ET1RXER_RMII1RXER**	-	-	**U13.20**	-	-
ET1-TXCLK	G9	PN2	**ET1-TXCLK**	**R10**	-	**U13.22**	-	-
ET1-ETXD3	F8	PN1	**ET1-ETXD3**	-	-	**U13.27**	-	-
ET1-ETXD2	E6	PN0	**ET1-ETXD2**	-	-	**U13.26**	-	-
ET1-TXEN_RMII1TXDEN	H8	PQ7	**ET1-TXEN_RMII1TXDEN**	-	-	**U13.23**	-	-
ET1-ETXD1_RMII1TXD1	F9	PQ6	**ET1-ETXD1_RMII1TXD1**	-	-	**U13.25**	-	-
ET1-ETXD0_RMII1TXD0	E10	PQ5	**ET1-ETXD0_RMII1TXD0**	-	-	**U13.24**	-	-
ET1-RXCLK	E11	PQ4	**ET1-RXCLK**	**R9**	-	**U13.19**	**R226**	**R225**
						U14.2	R225	R226
PQ0	E7	PQ0	ET1-RXDV_RMII1CRSDV	R276	R39, R42	U13.18	-	-
			ET1-CRS	**R42, R39**	**R276**	**U13.29**	-	-

Table 6-13: Ethernet Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P15	J7	P15	**ET-INTn**	**R336**	**R118, R119**	**U13.21**	-	-
			JA2-IRQb-M1HSIN1	R118	R336, **R119**	JA2.9	-	-
			PDC-PIXD0	R119	R336, **R118**	J19.18	-	-
P31	J4	P31	**ET-MDC**	**R218**	**R3**	**U13.12**	-	-
			JA2-CTSaRTSa	R3	R218	JA2.12	-	-
P30	J5	P30	**ET-MDIO**	**R216**	**R100, R95**	**U13.11**	-	-
			JA2-M1WP	R100	R216, **R95**	JA2.17	-	-
			JA2-TIMIN0	R95	R216, **R100**	JA2.21	-	-
CLKOUT25M	K1	PH7	**CLKOUT25M**	**R16**	-	**U13.9**	**R243**	**R244**
ET-GPIORST *1	R12	PL4	**ET-GPIORST**	**R245,** R254, C72	R410	**U13.32**	-	-
SW-PHYRESn *1	-	-	**SW-PHYRESn**	**R410**	-			

*1: In the default RSK+ configuration, ET-GPIORST signal and SW-PHYRESn signal are connected to the reset pin of the Ethernet controller IC (U13). Normally, reset is activated by SW-PHYRESn, so set port PL4 (ET-GPIORST) of the RX72N in the input direction. When using ET-GPIORST as a reset, configure as shown in **Table 6-13** above.

Table 6-14 below details the function of the jumpers associated with the Ethernet Configuration.

Table 6-14: Ethernet Configuration Option Links(PHY Mode)

PHY Mode	Config Placement	Reference	Related Links
MII Mode	**Fit**	**R266, R243, R226, R39, R42**	**U13, U14**
	DNF	**R225, R244, R249, R276**	
RMII Mode	DNF	R266, R243, R226, R39, R42	U13, U14
	Fit	R225, R244, R249, R276	

6.10 General IO & LED Configuration

Table 6-15 below details the function of the option links associated with General IO & LED Configuration.

Table 6-15: General IO & LED Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
LED0	J13	P71	LED0	-	-	LED0.K	R193	-
ET1-LED0	D7	P93	ET1-LED0	-	-	ETHERNET.11	-	-
						U13.30	-	-
JA1-IO7	F15	PG7	JA1-IO7	-	-	JA1.22	-	-
JA1-IO6	F14	PG6	JA1-IO6	-	-	JA1.21	-	-
JA1-IO5	E14	PG5	JA1-IO5	-	-	JA1.20	-	-
JA1-IO4	E15	PG4	JA1-IO4	-	-	JA1.19	-	-
JA1-IO3	F13	PG3	JA1-IO3	-	-	JA1.18	-	-
JA1-IO2	D14	PG2	JA1-IO2	-	-	JA1.17	-	-
JA1-IO1	D10	PG1	JA1-IO1	-	-	JA1.16	-	-
JA1-IO0	A10	PG0	JA1-IO0	-	-	JA1.15	-	-
LED1	K2	PH6	LED1	-	-	LED1.K	R193	-
LED2	L10	PL7	LED2	-	-	LED2.K	R193	-
LED3	M12	PL6	LED3	-	-	LED3.K	R193	-

6.11 GLCDC Configuration

Table 6-16 and Table 6-17 below details the function of the option links associated with GLCDC Configuration.

Table 6-16: GLCDC Configuration Option Links(1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P14	P4	P14	OnTFT-CLK	R294, R299	R74, J12(open)	ONTFT1.30	-	-
			JA2-M1TRCCLK	R74, R299	R294, J12(open)	JA2.25	-	-
			USB0-OVRCURA	J12(short) , R299	R294, R74, R282	U9.3	J10 (2-3pin short) or R26	J10 (1-2pin open) and R25
P13	N5	P13	OnTFT-VSYNC	R293	R292	ONTFT1.33	-	-
			JA1-ADTRG	R292	R293	JA1.8	R292	R124
P11	P8	P11	OnTFT-G4	R261	R28	ONTFT1.17	-	-
			JA6-M1VIN	R28	R261	JA6.15	-	-
P10	K7	P10	OnTFT-INT	R263	R262, R27	ONTFT2.5	-	-
			JA3-ALE	R262	R263, R27	JA3.46	R361	R155
			JA6-M1WIN	R27	R263, R262	JA6.16	-	-
OnTFT-BACKLIGHT	L2	P27	OnTFT-BACKLIGHT	-	-	U8.3	-	-
OnTFT-B6	P7	P57	OnTFT-B6	-	-	ONTFT1.22	-	-
						ONTFT1.27	-	-
OnTFT-B7	N7	P56	OnTFT-B7	-	-	ONTFT1.23	-	-
						ONTFT1.28	-	-
OnTFT-G2	R8	P55	OnTFT-G2	-	-	ONTFT1.15	-	-
OnTFT-G3	R7	P54	OnTFT-G3	-	-	ONTFT1.16	-	-
OnTFT-B4	N4	P85	OnTFT-B4	-	-	ONTFT1.25	-	-
OnTFT-B5	M6	P84	OnTFT-B5	-	-	ONTFT1.21	-	-
						ONTFT1.26	-	-
P83	M9	P83	OnTFT-G5	R271, R36	R35	ONTFT1.18	-	-
			JA6-SCKc	R35, R36	R271	JA6.11	-	-
OnTFT-R4	P10	P82	OnTFT-R4	-	-	ONTFT1.9	-	-

Table 6-17: GLCDC Configuration Option Links(2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P81	L9	P81	**OnTFT-R5**	**R321**	**R107**	**ONTFT1.5**	-	-
						ONTFT1.10	-	-
			JA2-M1UN	R107	R321	JA2.14	-	-
OnTFT-R6	N10	P80	**OnTFT-R6**	-	-	**ONTFT1.6**	-	-
						ONTFT1.11	-	-
PC7	N9	PC7	**OnTFT-G6**	**J11 (1-2pin short)**	**R275, R40**	**ONTFT1.13**	-	-
						ONTFT1.19	-	-
			EMU-UB	J11 (2-3pin short)	**R275, R40**	E1.10	-	-
			DSW-UB			SW4.2	-	-
			JA2-M1TRDCLK	R275	J11 (open), **R40**	JA2.26	-	-
			JA6-TXDc	R40	J11 (open), **R275**	JA6.9	-	-
PC6	R9	PC6	JA3-A22	R278	R279	JA3.43	-	-
			OnTFT-G7	**R279**	**R278**	**ONTFT1.14**	-	-
						ONTFT1.20	-	-
PC5	R10	PC5	JA3-A21	R272	R273	JA3.42	-	-
			OnTFT-R3	**R273**	**R272**	**ONTFT1.8**	-	-
PC4	P11	PC4	**OnTFT-R7**	**R302, R296**	**R301, R90**	**ONTFT1.7**	-	-
						ONTFT1.12	-	-
			JA3-A20	R301, **R296**	R302, **R90**	JA3.41	-	-
			JA2-M1POE	R90, **R296**	R302, **R301**	JA2.24	-	-
OnTFT-HSYNC	L6	PJ2	**OnTFT-HSYNC**	-	-	**ONTFT1.32**	-	-
OnTFT-DEN	N6	PJ1	**OnTFT-DEN**	-	-	**ONTFT1.34**	-	-
OnTFT-B3	M5	PJ0	**OnTFT-B3**	-	-	**ONTFT1.24**	-	-
OnTFT-DISP	F4	PK4	**OnTFT-DISP**	-	-	**ONTFT1.31**	-	-
OnTFT-RESn	K10	PL3	OnTFT-RESn	R129	R128	ONTFT2.6	**R320**	-
OnTFT-SDA	G8	PQ2	**OnTFT-SDA**	-	-	**ONTFT2.4**	-	-
OnTFT-SCL	E8	PQ1	**OnTFT-SCL**	-	-	**ONTFT2.3**	-	-
RESn	G7	-	**EMU-RESn**	-	-	**E1.13**	-	-
			SW-RESn	-	-	**RES1(Switch)**	-	-
			JA2-RESn	-	-	**JA2.1**	-	-
			PDC-RESn	**R137**	**R138**	**J19.6**	**R175**	-
			OnTFT-RESn	**R128**	**R129**	**ONTFT2.6**	**R320**	-

6.12 I2C & EEPROM Configuration

Table 6-18 and **Table 6-19** below detail the function of the option links associated with I2C & EEPROM Configuration.

Table 6-18: I2C & EEPROM Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P21	R1	P21	**E2P-SCL**	**R75, R79**	**R78**	**U3.6**	-	-
			JA1-SCL			**JA1.26**	-	-
			PDC-PIXD5	R78	R75, R79	J19.13	-	-
P20	P3	P20	**E2P-SDA**	**R72, R73**	**R69, R70**	**U3.5**	-	-
			JA1-SDA			**JA1.25**	-	-
			PDC-PIXD4	R69	R72, R73, **R70**	J19.14	-	-
			JA2-M1ENC	R70	R72, R73, **R69**	JA2.23	R91	R86

Table 6-19: I2C & EEPROM Configuration Option Links (2)

Reference	Configuration	Fit	DNF	Related Links
SDA1, SCL1	**Connect pull-up resistor to Board_3V3.**	**R113**	**R114**	**U3**
	Connect pull-up resistor to Board_5V.	R114	R113	**U3**
WP	EEPROM Write protect.	R326	-	**U3**
A0, A1, A2	**Device address (0xA6).**	**R329, R328, R340**	**R342, R341, R327**	**U3**
	Device address (0xA4).	R342, **R328, R340**	R329, **R341, R327**	**U3**

6.13 IRQ & Switch Configuration

Table 6-20 and **Table 6-21** below details the function of the option links associated with IRQ & Switch Configuration.

Table 6-20: IRQ & Switch Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07 *1	E5	P07	**SW3**	**R88**	**R124, R89**	**SW3**	-	-
			JA1-ADTRG	R124	R88, **R89**	JA1.8	R124	**R292**
			JA1-IRQd	R89	R88, **R124**	JA1.23	-	-
P03	D3	P03	**SERIAL-CTS**	**R105**	**R106**	**U15.2**	-	-
			JA1-DAC0	R106	R105	JA1.13	-	-
PMOD1-IO1	D6	P02	**PMOD1-IO1**	-	-	**PMOD1.8**	-	-
P00	E3	P00	**QSPI-IO2**	**R324**	**R323**	**U11.3**	-	-
			PMOD2-IO1	R323	R324	PMOD2.8	-	-
P17	P2	P17	**PMOD1-IO0**	**R280**	**R44, R281, R277**	**PMOD1.7**	-	-
			JA6-TXDb	R44	R280, **R281, R277**	JA6.8	-	-
			PDC-PIXD3	R281	R280, **R44, R277**	J19.15	-	-
			SSI-TXD	R277	R280, **R44, R281**	J18.12	-	-
P15	J7	P15	**ET-INTn**	**R336**	**R118, R119**	**U13.21**	-	-
			JA2-IRQb-M1HSIN1	R118	R336, **R119**	JA2.9	-	-
			PDC-PIXD0	R119	R336, **R118**	J19.18	-	-
P10	K7	P10	**OnTFT-INT**	**R263**	**R262, R27**	**ONTFT2.5**	-	-
			JA3-ALE	R262	R263, **R27**	JA3.46	**R361**	**R155**
			JA6-M1WIN	R27	R263, **R262**	JA6.16	-	-
P35	H3	P35	**JP-UPSEL**	-	-	**J15.2**	-	-
			JA2-NMIn	**R127**	-	**JA2.3**	-	-
JA2-IRQa-M1HSIN0	H2	P34	**JA2-IRQa-M1HSIN0**	-	-	**JA2.7**	-	-
P32	H5	P32	**CAN1TX**	**R300**	**R87, R47, R295**	**U16.3**	-	-
			JA2-IRQc_M1HSIN2	R87	R300, **R47, R295**	JA2.23	**R86**	**R91**
			JA5-CAN1TX	R47	R300, **R87, R295**	JA5.5	-	-
			PDC-VSYNC	R295	R300, **R87, R47**	J19.9	-	-

*1: When changing the option link of P07, pay attention to the presence or absence of a pull-up resistor. Leave the pull-up resistor for SW3 (R194) fitted, otherwise the internal pull-up in the MCU will need to be enabled.

Table 6-21: IRQ & Switch Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P30	J5	P30	**ET-MDIO**	**R216**	**R100, R95**	**U13.11**	-	-
			JA2-M1WP	R100	R216, **R95**	JA2.17	-	-
			JA2-TIMIN0	R95	R216, **R100**	JA2.21	-	-
PMOD2-IO0	B4	P46	**PMOD2-IO0**	-	-	**PMOD2.7**	-	-
SW1	D1	P45	**SW1**	-	-	**SW1**	-	-
SW2	C4	P44	**SW2**	-	-	**SW2**	-	-
P41	A4	P41	SDHI-POWFLT	R120	R121	U6.5	-	-
			JA1-ADC1	**R121**	**R120**	**JA1.10**	-	-
PC7	N9	PC7	**OnTFT-G6**	**J11 (1-2pin short)**	**R275, R40**	**ONTFT1.13**	-	-
						ONTFT1.19	-	-
			EMU-UB	J11 (2-3pin short)	**R275, R40**	E1.10	-	-
			DSW-UB			SW4.2	-	-
			JA2-M1TRDCLK	R275	J11 (open), **R40**	JA2.26	-	-
			JA6-TXDc	R40	J11 (open), **R275**	JA6.9	-	-
MD_FINED	G4	-	**EMU-MD_FINED**	-	-	**E1.7**	-	-
			DSW-MD_FINED	-	-	**SW4.1**	-	-
RESn	G7	-	**EMU-RESn**	-	-	**E1.13**	-	-
			SW-RESn	-	-	**RES1(Switch)**	-	-
			JA2-RESn	-	-	**JA2.1**	-	-
			PDC-RESn	**R137**	**R138**	**J19.6**	**R175**	-
			OnTFT-RESn	**R128**	**R129**	**ONTFT2.6**	**R320**	-

6.14 MTU & POE Configuration

Table 6-22 and **Table 6-23** below details the function of the option links associated with MTU & POE Configuration.

Table 6-22: MTU & POE Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P16	R3	P16	**USB0-VBUS**	**J7(1-2 short),** J9(1-2 short) or **R7**	**R115**	**USB0_2.1**	**J8(1-2 short), R2**	-
			USB0-VBUSEN	J7(2-3 short)	**R115**	U7.4	-	-
			JA2-M1UD	R115	J7(Open)	JA2.11	-	-
P15	J7	P15	**ET-INTn**	**R336**	**R118, R119**	**U13.21**	-	-
			JA2-IRQb-M1HSIN1	R118	R336, **R119**	JA2.9	-	-
			PDC-PIXD0	R119	R336, **R118**	J19.18	-	-
P14	P4	P14	**OnTFT-CLK**	**R294, R299**	**R74, J12(open)**	**ONTFT1.30**	-	-
			JA2-M1TRCCLK	R74, **R299**	R294, **J12(open)**	JA2.25	-	-
			USB0-OVRCURA	J12(short) , **R299**	R294, **R74**, R282	U9.3	**J10 (2-3pin short)** or R26	**J10 (1-2pin open) and R25**
P11	P8	P11	**OnTFT-G4**	**R261**	**R28**	**ONTFT1.17**	-	-
			JA6-M1VIN	R28	R261	JA6.15	-	-
P10	K7	P10	**OnTFT-INT**	**R263**	**R262, R27**	**ONTFT2.5**	-	-
			JA3-ALE	R262	R263, **R27**	JA3.46	**R361**	**R155**
			JA6-M1WIN	R27	R263, **R262**	JA6.16	-	-
P25	M3	P25	**PDC-HSYNC**	**R317**	**R103, R97, R45**	**J19.10**	-	-
			JA2-M1VN	R103	R317, **R97, R45**	JA2.16	-	-
			JA2-TIMOUT1	R97	R317, **R103, R45**	JA2.20	-	-
			JA6-RXDb	R45	R317, **R103, R97**	JA6.7	-	-
P24	L4	P24	**PDC-PIXCLK**	**R304, R99**	**R104, R303, R98**	**J19.8**	-	-
			JA2-M1VP	R104, **R99**	R304, **R303, R98**	JA2.15	-	-
			JA6-SCKb	R303, **R99**	R304, **R104, R98**	JA6.10	-	-
			JA2-TIMOUT0	R98, **R99**	R304, **R104, R303**	JA2.19	-	-

Table 6-23: MTU & POE Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P22	N1	P22	**USB0-OVRCURB**	**R282, R60**	**R64, R286, R68, R59**	**U9.3**	**J10 (1-2pin short)** or R25	**J10 (2-3pin short) and R26**
			PDC-PIXD6	R64, **R60**	R282, **R286, R68, R59**	J19.12	-	-
			SSI-AUDIOCLK	R286, **R60**	R282, **R64, R68, R59**	J18.5	-	-
			JA2-M1UP	R68, **R60**	R282, **R64, R286, R59**	JA2.13	-	-
			JA6-DREQ	R59, **R60**	R282, **R64, R286, R68**	JA6.1	-	-
P20	P3	P20	**E2P-SDA**	**R72, R73**	**R69, R70**	**U3.5**	-	-
			JA1-SDA			**JA1.25**	-	-
			PDC-PIXD4	R69	R72, R73, **R70**	J19.14	-	-
			JA2-M1ENC	R70	R72, R73, **R69**	JA2.23	R91	R86
JA2-IRQa-M1HSIN0	H2	P34	**JA2-IRQa-M1HSIN0**	-	-	**JA2.7**	-	-
P32	H5	P32	**CAN1TX**	**R300**	**R87, R47, R295**	**U16.3**	-	-
			JA2-IRQc_M1HSIN2	R87	R300, **R47, R295**	JA2.23	**R86**	**R91**
			JA5-CAN1TX	R47	R300, **R87, R295**	JA5.5	-	-
			PDC-VSYNC	R295	R300, **R87, R47**	J19.9	-	-
P30	J5	P30	**ET-MDIO**	**R216**	**R100, R95**	**U13.11**	-	-
			JA2-M1WP	R100	R216, **R95**	JA2.17	-	-
			JA2-TIMIN0	R95	R216, **R100**	JA2.21	-	-
P86	N3	P86	**PDC-PIXD1**	**R308**	**R34, R102, R94**	**J19.17**	-	-
			JA6-RXDc	R34	R308, **R102, R94**	JA6.12	-	-
			JA2-M1WN	R102	R308, **R34, R94**	JA2.18	-	-
			JA2-TIMIN1	R94	R308, **R34, R102**	JA2.22	-	-
P81	L9	P81	**OnTFT-R5**	**R321**	**R107**	**ONTFT1.5**	-	-
						ONTFT1.10	-	-
			JA2-M1UN	R107	R321	JA2.14	-	-
PC7	N9	PC7	**OnTFT-G6**	**J11 (1-2pin short)**	**R275, R40**	**ONTFT1.13**	-	-
						ONTFT1.19	-	-
			EMU-UB	J11 (2-3pin short)	**R275, R40**	E1.10	-	-
			DSW-UB			SW4.2	-	-
			JA2-M1TRDCLK	R275	J11 (open), **R40**	JA2.26	-	-
			JA6-TXDc	R40	J11 (open), **R275**	JA6.9	-	-
PC4	P11	PC4	**OnTFT-R7**	**R302, R296**	**R301, R90**	**ONTFT1.7**	-	-
						ONTFT1.12	-	-
			JA3-A20	R301, **R296**	R302, **R90**	JA3.41	-	-
			JA2-M1POE	R90, **R296**	R302, **R301**	JA2.24	-	-
PC1	N14	PC1	**JA3-A17**	**R32**	**R31**	**JA3.38**	-	-
			JA6-M1TOGGLE	R31	R32	JA6.13	-	-

6.15 PDC Configuration

Table 6-24 and Table 6-25 below details the function of the option links associated with PDC Configuration.

Table 6-24: PDC Configuration Option Links(1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17	P2	P17	**PMOD1-IO0**	**R280**	**R44, R281, R277**	**PMOD1.7**	-	-
			JA6-TXDb	R44	R280, **R281, R277**	JA6.8	-	-
			PDC-PIXD3	R281	R280, **R44, R277**	J19.15	-	-
			SSI-TXD	R277	R280, **R44, R281**	J18.12	-	-
P15	J7	P15	**ET-INTn**	**R336**	**R118, R119**	**U13.21**	-	-
			JA2-IRQb-M1HSIN1	R118	R336, **R119**	JA2.9	-	-
			PDC-PIXD0	R119	R336, **R118**	J19.18	-	-

Table 6-25: PDC Configuration Option Links(2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P25	M3	P25	**PDC-HSYNC**	**R317**	**R103, R97, R45**	**J19.10**	-	-
			JA2-M1VN	R103	R317, **R97, R45**	JA2.16	-	-
			JA2-TIMOUT1	R97	R317, **R103, R45**	JA2.20	-	-
			JA6-RXDb	R45	R317, **R103, R97**	JA6.7	-	-
P24	L4	P24	**PDC-PIXCLK**	**R304, R99**	**R104, R303, R98**	**J19.8**	-	-
			JA2-M1VP	R104, **R99**	R304, **R303, R98**	JA2.15	-	-
			JA6-SCKb	R303, **R99**	R304, **R104, R98**	JA6.10	-	-
			JA2-TIMOUT0	R98, **R99**	R304, **R104, R303**	JA2.19	-	-
P23	M2	P23	**PDC-PIXD7**	**R290, R283**	**R288, R287**	**J19.11**	-	-
			SSI-SCK	R288, **R283**	R290, **R287**	J18.9	-	-
			JA6-DACK	R287, **R283**	R290, **R288**	JA6.2	-	-
P22	N1	P22	**USB0-OVRCURB**	**R282, R60**	**R64, R286, R68, R59**	**U9.3**	**J10 (1-2pin short)** or R25	**J10 (2-3pin short) and R26**
			PDC-PIXD6	R64, **R60**	R282, **R286, R68, R59**	J19.12	-	-
			SSI-AUDIOCLK	R286, **R60**	R282, **R64, R68, R59**	J18.5	-	-
			JA2-M1UP	R68, **R60**	R282, **R64, R286, R59**	JA2.13	-	-
			JA6-DREQ	R59, **R60**	R282, **R64, R286, R68**	JA6.1	-	-
P21	R1	P21	**E2P-SCL**	**R75, R79**	**R78**	**U3.6**	-	-
			JA1-SCL			**JA1.26**	-	-
			PDC-PIXD5	R78	R75, R79	J19.13	-	-
P20	P3	P20	**E2P-SDA**	**R72, R73**	**R69, R70**	**U3.5**	-	-
			JA1-SDA			**JA1.25**	-	-
			PDC-PIXD4	R69	R72, R73, **R70**	J19.14	-	-
			JA2-M1ENC	R70	R72, R73, **R69**	JA2.23	R91	R86
P33	H4	P33	**CAN1RX**	**R46, R48**	**R43, R49**	**U4.4**	-	-
			PDC-PCKO	R43, **R48**	R46, **R49**	J19.5	-	-
			JA5-CAN1RX	R49, **R48**	R46, **R43**	JA5.6	-	-
P32	H5	P32	**CAN1TX**	**R300**	**R87, R47, R295**	**U16.3**	-	-
			JA2-IRQc_M1HSIN2	R87	R300, **R47, R295**	JA2.23	**R86**	**R91**
			JA5-CAN1TX	R47	R300, **R87, R295**	JA5.5	-	-
			PDC-VSYNC	R295	R300, **R87, R47**	J19.9	-	-
P87	R2	P87	**PDC-PIXD2**	-	-	**J19.16**	**R12**	-
						T4	-	-
P86	N3	P86	**PDC-PIXD1**	**R308**	**R34, R102, R94**	**J19.17**	-	-
			JA6-RXDc	R34	R308, **R102, R94**	JA6.12	-	-
			JA2-M1WN	R102	R308, **R34, R94**	JA2.18	-	-
			JA2-TIMIN1	R94	R308, **R34, R102**	JA2.22	-	-
PDC-RESn	M11	PL5	PDC-RESn	R138	R137	J19.6	**R175**	-
PM2	K11	PM2	**SDHI-D0**	**R134**	**R133**	**SDHI1.7**	-	-
			PDC-SSDA	R133	R134	J19.19	**R176**	-
PM1	F11	PM1	**SDHI-CMD**	**R136**	**R135**	**SDHI1.2**	-	-
			PDC-SSCL	R135	R136	J19.20	**R419**	-
RESn	G7	-	**EMU-RESn**	-	-	**E1.13**	-	-
			SW-RESn	-	-	**RES1(Switch)**	-	-
			JA2-RESn	-	-	**JA2.1**	-	-
			PDC-RESn	**R137**	**R138**	**J19.6**	**R175**	-
			OnTFT-RESn	**R128**	**R129**	**ONTFT2.6**	**R320**	-

6.16 PMOD1 Configuration

Table 6-26 below details the function of the option links associated with PMOD1 Configuration.

Table 6-26: PMOD1 Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PMOD1-IO1	D6	P02	**PMOD1-IO1**	-	-	**PMOD1.8**	-	-
P17	P2	P17	**PMOD1-IO0**	**R280**	**R44, R281, R277**	**PMOD1.7**	-	-
			JA6-TXDb	R44	R280, **R281, R277**	JA6.8	-	-
			PDC-PIXD3	R281	R280, **R44, R277**	J19.15	-	-
			SSI-TXD	R277	R280, **R44, R281**	J18.12	-	-
PMOD1-CS	L1	PH3	**PMOD1-CS**	-	-	**PMOD1.1**	-	-
PMOD1-MOSI	J6	PH2	**PMOD1-MOSI**	-	-	**PMOD1.2**	-	-
PMOD1-MISO	K6	PH1	**PMOD1-MISO**	-	-	**PMOD1.3**	-	-
PMOD1-SCK	N2	PH0	**PMOD1-SCK**	**R246**	-	**PMOD1.4**	-	-
PMOD1-IO2	P1	PK7	**PMOD1-IO2**	-	-	**PMOD1.9**	-	-
PMOD1-IO3	H11	PL0	**PMOD1-IO3**	-	-	**PMOD1.10**	-	-

6.17 PMOD2 Configuration

Table 6-27 below details the function of the option links associated with PMOD2 Configuration.

Table 6-27: PMOD2 Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P00	E3	P00	**QSPI-IO2**	**R324**	**R323**	**U11.3**	-	-
			PMOD2-IO1	R323	R324	PMOD2.8	-	-
PMOD2-IO3	D2	P47	**PMOD2-IO3**	-	-	**PMOD2.10**	-	-
PMOD2-IO0	B4	P46	**PMOD2-IO0**	-	-	**PMOD2.7**	-	-
P52	L8	P52	**JA3-RDn**	**R149**	**R139**	**JA3.25**	-	-
			PMOD2-MISO	R139	R149	PMOD2.3	-	-
P51	M8	P51	**JA3-WRHn**	**R148, R131**	**R132**	**JA3.47**	**R157**	**R359**
			PMOD2-SCK	R132, **R131**	R148	PMOD2.4	-	-
P50	K8	P50	**JA3-WRn**	**R140**	**R352, R353**	**JA3.26**	**R150**	**R366**
			JA3-WRLn	R352	R140, **R353**	JA3.48	R156	**R360**
			PMOD2-MOSI	R353	R140, **R352**	PMOD2.2	-	-
PJ5	G5	PJ5	**QSPI-IO1**	**R298**	**R82, R297**	**U11.2**	-	-
			PMOD2-CS	R82	R298, **R297**	PMOD2.1	-	-
			SSI-RXD	R297	R298, **R82**	J18.10	-	-
PMOD2-IO2	E9	PQ3	**PMOD2-IO2**	-	-	**PMOD2.9**	-	-

6.18 QSPI Configuration

Table 6-28 below details the function of the option links associated with QSPI Configuration.

Table 6-28: QSPI Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
QSPI-IO3	D5	P01	**QSPI-IO3**	-	-	**U11.7**	-	-
P00	E3	P00	**QSPI-IO2**	**R324**	**R323**	**U11.3**	-	-
			PMOD2-IO1	R323	R324	PMOD2.8	-	-
PJ5	G5	PJ5	**QSPI-IO1**	**R298**	**R82, R297**	**U11.2**	-	-
			PMOD2-CS	R82	R298, **R297**	PMOD2.1	-	-
			SSI-RXD	R297	R298, **R82**	J18.10	-	-
QSPI-IO0	H7	PJ3	**QSPI-IO0**	-	-	**U11.5**	-	-
QSPI-CS	J11	PN5	**QSPI-CS**	-	-	**U11.1**	-	-
QSPI-CLK	L12	PN4	**QSPI-CLK**	**R22**	-	**U11.6**	-	-

6.19 RSPI Configuration

Table 6-29 below details the function of the option links associated with RSPI Configuration.

Table 6-29: RSPI Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
RSPI-CS	J9	PK3	**RSPI-CS**	-	-	**U10.1**	-	-
RSPI-MISO	N11	PK2	**RSPI-MISO**	-	-	**U10.2**	-	-
RSPI-MOSI	K9	PK1	**RSPI-MOSI**	-	-	**U10.5**	-	-
RSPI-CLK	M10	PK0	**RSPI-CLK**	**R21**	-	**U10.6**	-	-

6.20 SDHI Configuration

Table 6-30 below details the function of the option links associated with SDHI Configuration.

Table 6-30: SDHI Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P41	A4	P41	SDHI-POWFLT	R120	R121	U6.5	-	-
			JA1-ADC1	**R121**	**R120**	**JA1.10**	-	-
SDHI-PE	K3	PH4	**SDHI-PE**	-	-	**U6.4**	-	-
SDHI-WP	M13	PM7	**SDHI-WP**	-	-	**SDHI1.12**	-	-
SDHI-CD	N13	PM6	**SDHI-CD**	-	-	**SDHI1.10**	-	-
SDHI-D3	R15	PM5	**SDHI-D3**	-	-	**SDHI1.1**	-	-
SDHI-D2	P14	PM4	**SDHI-D2**	-	-	**SDHI1.9**	-	-
SDHI-D1	P15	PM3	**SDHI-D1**	-	-	**SDHI1.8**	-	-
PM2	K11	PM2	**SDHI-D0**	**R134**	**R133**	**SDHI1.7**	-	-
			PDC-SSDA	R133	R134	J19.19	**R176**	-
PM1	F11	PM1	**SDHI-CMD**	**R136**	**R135**	**SDHI1.2**	-	-
			PDC-SSCL	R135	R136	J19.20	**R419**	-
SDHI-CLK	G11	PM0	**SDHI-CLK**	**R23**	-	**SDHI1.5**	-	-

6.21 Serial & USB to Serial Configuration

Table 6-31 below details the function of the option links associated with Serial & USB to Serial Configuration.

Table 6-31: Serial & USB to Serial Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P03	D3	P03	**SERIAL-CTS**	**R105**	**R106**	**U15.2**	-	-
			JA1-DAC0	R106	R105	JA1.13	-	-
P17	P2	P17	**PMOD1-IO0**	**R280**	**R44, R281, R277**	**PMOD1.7**	-	-
			JA6-TXDb	R44	R280, **R281, R277**	JA6.8	-	-
			PDC-PIXD3	R281	R280, **R44, R277**	J19.15	-	-
			SSI-TXD	R277	R280, **R44, R281**	J18.12	-	-
P12	R4	P12	**JA6-M1UIN**	-	-	**JA6.14**	-	-
P25	M3	P25	**PDC-HSYNC**	**R317**	**R103, R97, R45**	**J19.10**	-	-
			JA2-M1VN	R103	R317, **R97, R45**	JA2.16	-	-
			JA2-TIMOUT1	R97	R317, **R103, R45**	JA2.20	-	-
			JA6-RXDb	R45	R317, **R103, R97**	JA6.7	-	-
P24	L4	P24	**PDC-PIXCLK**	**R304, R99**	**R104, R303, R98**	**J19.8**	-	-
			JA2-M1VP	R104, **R99**	R304, **R303, R98**	JA2.15	-	-
			JA6-SCKb	R303, **R99**	R304, **R104, R98**	JA6.10	-	-
			JA2-TIMOUT0	R98, **R99**	R304, **R104, R303**	JA2.19	-	-
P31	J4	P31	**ET-MDC**	**R218**	**R3**	**U13.12**	-	-
			JA2-CTSaRTSa	R3	R218	JA2.12	-	-
P43	E4	P43	**SERIAL-RTS**	**R108**	**R109**	**U17.2**	-	-
			JA1-ADC3	R109	R108	JA1.12	-	-
P86	N3	P86	**PDC-PIXD1**	**R308**	**R34, R102, R94**	**J19.17**	-	-
			JA6-RXDc	R34	R308, **R102, R94**	JA6.12	-	-
			JA2-M1WN	R102	R308, **R34, R94**	JA2.18	-	-
			JA2-TIMIN1	R94	R308, **R34, R102**	JA2.22	-	-
P83	M9	P83	**OnTFT-G5**	**R271, R36**	**R35**	**ONTFT1.18**	-	-
			JA6-SCKc	R35, **R36**	R271	JA6.11	-	-
PC7	N9	PC7	**OnTFT-G6**	**J11 (1-2pin short)**	**R275, R40**	**ONTFT1.13**	-	-
						ONTFT1.19	-	-
			EMU-UB	J11 (2-3pin short)	**R275, R40**	E1.10	-	-
			DSW-UB			SW4.2	-	-
			JA2-M1TRDCLK	R275	J11 (open), **R40**	JA2.26	-	-
			JA6-TXDc	R40	J11 (open), **R275**	JA6.9	-	-
PF2	J2	PF2	**EMU-TDI_RXD**	**R338**	**R339, R123**	**E1.11**	-	-
			SERIAL-RXD	R339	R338, **R123**	U15.3	-	**R50,** R337
			JA2-RXDa	R123	R338, **R339**	JA2.8	-	-
PF1	L3	PF1	**EMU-TCK**	**R385, R11**	**R164**	**E1.1**	-	-
			JA2-SCKa	R164, **R11**	R385	JA2.10	-	-
PF0	K5	PF0	**EMU-TDO_TXD**	**R344**	**R343, R126**	**E1.5**	-	-
			SERIAL-TXD	R343	R344, **R126**	U17.3	-	**R51,** R52
			JA2-TXDa	R126	R344, **R343**	JA2.6	-	-
PL2	P12	PL2	**SERIAL-TXD**	**R52**	**R51, R343**	**U17.3**	-	-
PL1	J10	PL1	**SERIAL-RXD**	**R377**	**R50, R339**	**U15.3**	-	-

6.22 SSIE Configuration

Table 6-32 below details the function of the option links associated with SSIE Configuration.

Table 6-32: SSIE Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17	P2	P17	**PMOD1-IO0**	**R280**	**R44, R281, R277**	**PMOD1.7**	-	-
			JA6-TXDb	R44	R280, **R281, R277**	JA6.8	-	-
			PDC-PIXD3	R281	R280, **R44, R277**	J19.15	-	-
			SSI-TXD	R277	R280, **R44, R281**	J18.12	-	-
P23	M2	P23	**PDC-PIXD7**	**R290, R283**	**R288, R287**	**J19.11**	-	-
			SSI-SCK	R288, **R283**	R290, **R287**	J18.9	-	-
			JA6-DACK	R287, **R283**	R290, **R288**	JA6.2	-	-
P22	N1	P22	**USB0-OVRCURB**	**R282, R60**	**R64, R286, R68, R59**	**U9.3**	**J10 (1-2pin short)** or R25	**J10 (2-3pin short) and R26**
			PDC-PIXD6	R64, **R60**	R282, **R286, R68, R59**	J19.12	-	-
			SSI-AUDIOCLK	R286, **R60**	R282, **R64, R68, R59**	J18.5	-	-
			JA2-M1UP	R68, **R60**	R282, **R64, R286, R59**	JA2.13	-	-
			JA6-DREQ	R59, **R60**	R282, **R64, R286, R68**	JA6.1	-	-
PF5	G6	PF5	**SSI-LRCK**	**R351**	**R143**	**J18.11**	-	-
			JA3-WAIT	R143	R351	JA3.45	R154	R15
PJ5	G5	PJ5	**QSPI-IO1**	**R298**	**R82, R297**	**U11.2**	-	-
			PMOD2-CS	R82	R298, **R297**	PMOD2.1	-	-
			SSI-RXD	R297	R298, **R82**	J18.10	-	-

6.23 USB Configuration

Table 6-33 below details the function of the option links associated with the USB Configuration.

Table 6-33: USB Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P16	R3	P16	**USB0-VBUS**	**J7(1-2 short),** J9(1-2 short) or **R7**	**R115**	**USB0_2.1**	**J8(1-2 short), R2**	-
			USB0-VBUSEN	J7(2-3 short)	**R115**	U7.4	-	-
			JA2-M1UD	R115	J7(Open)	JA2.11	-	-
P14	P4	P14	**OnTFT-CLK**	**R294, R299**	**R74, J12(open)**	**ONTFT1.30**	-	-
			JA2-M1TRCCLK	R74, **R299**	R294, **J12(open)**	JA2.25	-	-
			USB0-OVRCURA	J12(short) **, R299**	R294, **R74**, R282	U9.3	**J10 (2-3pin short)** or R26	**J10 (1-2pin open) and R25**
P22	N1	P22	**USB0-OVRCURB**	**R282, R60**	**R64, R286, R68, R59**	**U9.3**	**J10 (1-2pin short)** or R25	**J10 (2-3pin short) and R26**
			PDC-PIXD6	R64, **R60**	R282, **R286, R68, R59**	J19.12	-	-
			SSI-AUDIOCLK	R286, **R60**	R282, **R64, R68, R59**	J18.5	-	-
			JA2-M1UP	R68, **R60**	R282, **R64, R286, R59**	JA2.13	-	-
			JA6-DREQ	R59, **R60**	R282, **R64, R286, R68**	JA6.1	-	-
P35	H3	P35	**JP-UPSEL**	-	-	**J15.2**	-	-
			JA2-NMIn	**R127**	-	**JA2.3**	-	-
USB0-DP	R6	-	**USB0-DP**	-	-	**USB0_1.3**	-	-
						USB0_2.3	-	-
USB0-DM	R5	-	**USB0-DM**	-	-	**USB0_1.2**	-	-
						USB0_2.2	-	-

Table 6-34 below details the function of the jumpers associated with the USB Configuration.

Table 6-34: USB Configuration Jumper Option Links

Reference	Jumper Position	Configuration	Related Links
J9(DNF) *1	Shorted Pin1-2	Self-powered	**J8, R7**
	Shorted Pin2-3	Bus-powered	**J8,** J17, **R7**
	All open	**Self-powered by R7**	**J8**
J8	**Shorted Pin1-2**	**USB0 Function mode**	J9, **R7**
	Shorted Pin2-3	USB0 Host mode	-
	All open	DO NOT SET.	-

*1: If J9 is fitted, remove R7.

When using USB in function mode, be sure to set J8 to 1-2 Short. Also, do not plug in both USB0_1 and USB0_2 cables at the same time.

6.24 Unused Terminal Configuration

Table 6-35 below details the function of the option links associated with the Unused Terminal Configuration.

Table 6-35: Unused Terminal Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P60TERM	C10	P60	**P60TERM**	-	-	**J6.1**	-	-
P77TERM	L11	P77	**P77TERM**			**J6.6**		
P76TERM	N12	P76	**P76TERM**	-	-	**J6.5**	-	-
P75TERM	R13	P75	**P75TERM**			**J6.4**		
P74TERM	R14	P74	**P74TERM**	-	-	**J6.3**	-	-
P72TERM	K15	P72	**P72TERM**			**J6.2**		
P92TERM	A5	P92	**P92TERM**	-	-	**J6.7**	-	-
PH5TERM	K4	PH5	**PH5TERM**			**J6.8**		
PK6TERM	F7	PK6	**PK6TERM**	-	-	**J6.10**	-	-
PK5TERM	F5	PK5	**PK5TERM**			**J6.9**		

7. Headers

7.1 Application Headers

This RSK+ board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Table 7-1: Application Header JA1 Connections

Application Header JA1					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	5V JA1-5V	-	2	0V GROUND	-
3	3V3 JA1-3V3	-	4	0V GROUND	-
5	AVCC JA1-AVCC	B2, C2	6	AVSS JA1-AVSS	B1, C1, A3
7	AVREF JA1-VREFH	A2	8	ADTRG JA1-ADTRG	E5, N5
9	ADC0 JA1-ADC0	D4	10	ADC1 JA1-ADC1	A4
11	ADC2 JA1-ADC2	B3	12	ADC3 JA1-ADC3	E4
13	DAC0 JA1-DAC0	D3	14	DAC1 JA1-DAC1	C3
15	IO_0 JA1-IO0	A10	16	IO_1 JA1-IO1	D10
17	IO_2 JA1-IO2	D14	18	IO_3 JA1-IO3	F13
19	IO_4 JA1-IO4	E15	20	IO_5 JA1-IO5	E14
21	IO_6 JA1-IO6	F14	22	IO_7 JA1-IO7	F15
23	IRQd / IRQAEC / M2_HSIN0 JA1-IRQd	E5 / NC / NC	24	IIC_EX NC	NC
25	IIC_SDA JA1-SDA	P3	26	IIC_SCL JA1-SCL	R1

Table 7-2 below lists the connections of the application header, JA2.

Table 7-2: Application Header JA2 Connections

Application Header JA2					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	RESET JA2-RESn	G7	2	EXTAL JA2-EXTAL	J1
3	NMI JA2-NMIn	H3	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX JA2-TXDa	K5
7	IRQa / WKUP / M1_HSIN0 JA2-IRQa_M1HSIN0	H2	8	SCIaRX JA2-RXDa	J2
9	IRQb / M1_HSIN1 JA2-IRQb_M1HSIN1	J7	10	SCIaCK JA2-SCKa	L3
11	M1_UD JA2-M1UD	R3	12	CTSaRTSa JA2-CTSaRTSa	J4
13	M1_UP JA2-M1UP	N1	14	M1_UN JA2-M1UN	L9
15	M1_VP JA2-M1VP	L4	16	M1_VN JA2-M1VN	M3
17	M1_WP JA2-M1WP	J5	18	M1_WN JA2-M1WN	N3
19	TimerOut0 JA2-TIMOUT0	L4	20	TimerOut1 JA2-TIMOUT1	M3
21	TimerIn0 JA2-TIMIN0	J5	22	TimerIn1 JA2-TIMIN1	N3
23	IRQc / M1_EncZ / M1_HSIN2 JA2-23PIN	H5 / P3 / H5	24	M1_POE JA2-M1POE	P11
25	M1_TRCCLK JA2-M1TRCCLK	P4	26	M1_TRDCLK JA2-M1TRDCLK	N9

Table 7-3 below lists the connections of the BUS application header, JA3.

Table 7-3: Application Header JA3 Connections

Application Header JA3 (Bus)					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	A0 JA3-A0	F12	2	A1 JA3-A1	G12
3	A2 JA3-A2	G13	4	A3 JA3-A3	G14
5	A4 JA3-A4	G15	6	A5 JA3-A5	H15
7	A6 JA3-A6	H14	8	A7 JA3-A7	J15
9	A8 JA3-A8	J14	10	A9 JA3-A9	J12
11	A10 JA3-A10	L14	12	A11 JA3-A11	K14
13	A12 JA3-A12	L15	14	A13 JA3-A13	K13
15	A14 JA3-A14	M15	16	A15 JA3-A15	N15
17	D0 JA3-D0	A6	18	D1 JA3-D1	C7
19	D2 JA3-D2	A7	20	D3 JA3-D3	A9
21	D4 JA3-D4	B9	22	D5 JA3-D5	D9
23	D6 JA3-D6	B10	24	D7 JA3-D7	A11
25	RDn JA3-RDn	L8	26	WR / SDWE JA3-26PIN	K8 / C11
27	CSa JA3-CSa	H10	28	CSb *1 JA3-CSb	A12
29	D8 JA3-D8	D11	30	D9 JA3-D9	A14
31	D10 JA3-D10	B13	32	D11 JA3-D11	D12
33	D12 JA3-D12	B14	34	D13 JA3-D13	C13
35	D14 JA3-D14	E13	36	D15 JA3-D15	B15
37	A16 JA3-A16	M14	38	A17 JA3-A17	N14
39	A18 JA3-A18	P13	40	A19 JA3-A19	R11
41	A20 JA3-A20	P11	42	A21 JA3-A21	R10
43	A22 JA3-A22	R9	44	SDCLK *2 JA3-44PIN	A15 / J8
45	CSc / Wait JA3-45PIN	M1 / G6	46	ALE / SDCKE JA3-46PIN	K7 / C14
47	HWRn / DQMH JA3-47PIN	M8 / D15	48	LWRn / DQML JA3-48PIN	K8 / C15
49	CAS JA3-CAS	B12	50	RAS JA3-RAS	A13

*1: The chip select signal assigned on this board can also be used as a SDRAM chip select.
*2: This board can also output BCLK signal to JA3 header.

Table 7-4 below lists the connections of the application header, JA5.

Table 7-4: Application Header JA5 Connections

Application Header JA5					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	ADC4 JA5-ADC4	B13	2	ADC5 JA5-ADC5	D12
3	ADC6 JA5-ADC6	B14	4	ADC7 JA5-ADC7	C13
5	CAN1TX JA5-CAN1TX	H5	6	CAN1RX JA5-CAN1RX	H4
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQe / M2_EncZ / M2HSIN1 NC	NC / NC / NC	10	IRQf / M2_HSIN2 NC	NC / NC
11	M2_UD NC	NC	12	M2_Uin NC	NC
13	M2_Vin NC	NC	14	M2_Win NC	NC
15	M2_Toggle NC	NC	16	M2_POE NC	NC
17	M2_TRCCLK NC	NC	18	M2_TRDCLK NC	NC
19	M2_UP NC	NC	20	M2_Un NC	NC
21	M2_VP NC	NC	22	M2_Vn NC	NC
23	M2_WP NC	NC	24	M2_Wn NC	NC

Table 7-5 below lists the connections of the application header, JA6.

Table 7-5: Application Header JA6 Connections

Application Header JA6					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	DREQ JA6-DREQ	N1	2	DACK JA6-DACK	M2
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX JA6-RS232TX	NC	6	RS232RX JA6-RS232RX	NC
7	SCIbRX JA6-RXDb	M3	8	SCIbTX JA6-TXDb	P2
9	SCIcTX JA6-TXDc	N9	10	SCIbCK JA6-SCKb	L4
11	SCIcCK JA6-SCKc	M9	12	SCIcRX JA6-RXDc	N3
13	M1_Toggle JA6-M1TOGGLE	N14	14	M1_Uin JA6-M1UIN	R4
15	M1_Vin JA6-M1VIN	P8	16	M1_Win JA6-M1WIN	K7
17	EXT_USB_VBUS NC	NC	18	Reserved NC	NC
19	EXT_USB_BATT NC	NC	20	Reserved NC	NC
21	EXT_USB_CHG NC	NC	22	Reserved NC	NC
23	Unregulated_VCC Unregulated_VCC	-	24	Vss GROUND	-

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via an E1/E20/E2 Lite debugger. An E1/E2 Lite debugger is supplied with this RSK+ product.

For further information regarding the debugging capabilities of the E1/E20/E2 Lite debuggers, refer to E1/E20 Emulator, E2 Emulator Lite Additional Document for User's Manual (R20UT0399EJ).

8.2 Compiler Restrictions

The compiler supplied with this RSK+ is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip and Boot Modes (SCI and USB and FINE), which are configured on the RSK+ board. Details of the modifications required can be found in §6.2. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX72N Group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK+ is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E1 Emulator or E2 Emulator Lite (as supplied with this RSK+) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer E1/E20 Emulator User's Manual (R20UT0398EJ) or E2 Emulator Lite User's Manual (R20UT3240EJ).

8.5 Address Space

For the MCU address space details, refer to the 'Address Space' section of RX72N Group User's Manual: Hardware.

8.6 Note of Flash Access Window Setting Register

This register is used to set the write protection flag and start-up area select flag for setting the flash access window start address, flash access window end address, and access window.

Once 0 is written to this bit, the bit can never be restored to 1.
Therefore, the access window and the BTFLG bit will never be set again. If set the TM function will never be disabled, once enabled. Exercise extra caution when handling the FSPR bit.

For details, refer to Section 7.2.9 in the RX72N Group User's Manual: Hardware.

9. Additional Information

Technical Support

For information about the RX72N group microcontrollers refer to the ‘RX72N Group User’s Manual: Hardware’.

For information about the RX assembly language, refer to the ‘RX Family User’s Manual: Software’.

Technical Contact Details

Please refer to the contact details listed in section 8 of the “*Quick Start Guide*”

General information on Renesas microcontrollers can be found on the Renesas website at:
https://www.renesas.com/

Trademarks

All brand or product names used in this manual are trademarks or registered trademarks of their respective companies or organisations.

Copyright

REVISION HISTORY	RX72N Group Renesas Starter Kit+ for RX72N User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Nov 30, 2019	—	First Edition issued

RX72N Group

Renesas Starter Kit+ for RX72N User's Manual

Publication Date: Rev.1.00 Nov 30, 2019

Published by: Renesas Electronics Corporation

RX72N Group

Renesas Electronics Corporation

R20UT4443EG0100