Renesas Starter Kit+ for RX71M
CPU Board Schematics

REV	REF	DATE	DRAWN BY
1.00	Release	05.03.2015	YOI

Note:

C : Capacitor
D : Diode
R : Fixed Resistor
RV : Potentiometer
L : Inductor
U : Integrated Circuit
X : Crystal, Oscillator
RES : Reset Switch
SW : Switch
LED : Light Emitting Diode
PWR : Power Jack
J : Connector, Jumper

*** "DNF" marking means that component is not fitted by default.**

Board Code:

R0K50571MC000BE: MP Board

REEL Drawing No. D013292_04

Renesas System Design Co., Ltd.		
Title: RSK+RX71M [Index]		
Size	Document Number R20UT3216EG0100	Rev 1.00
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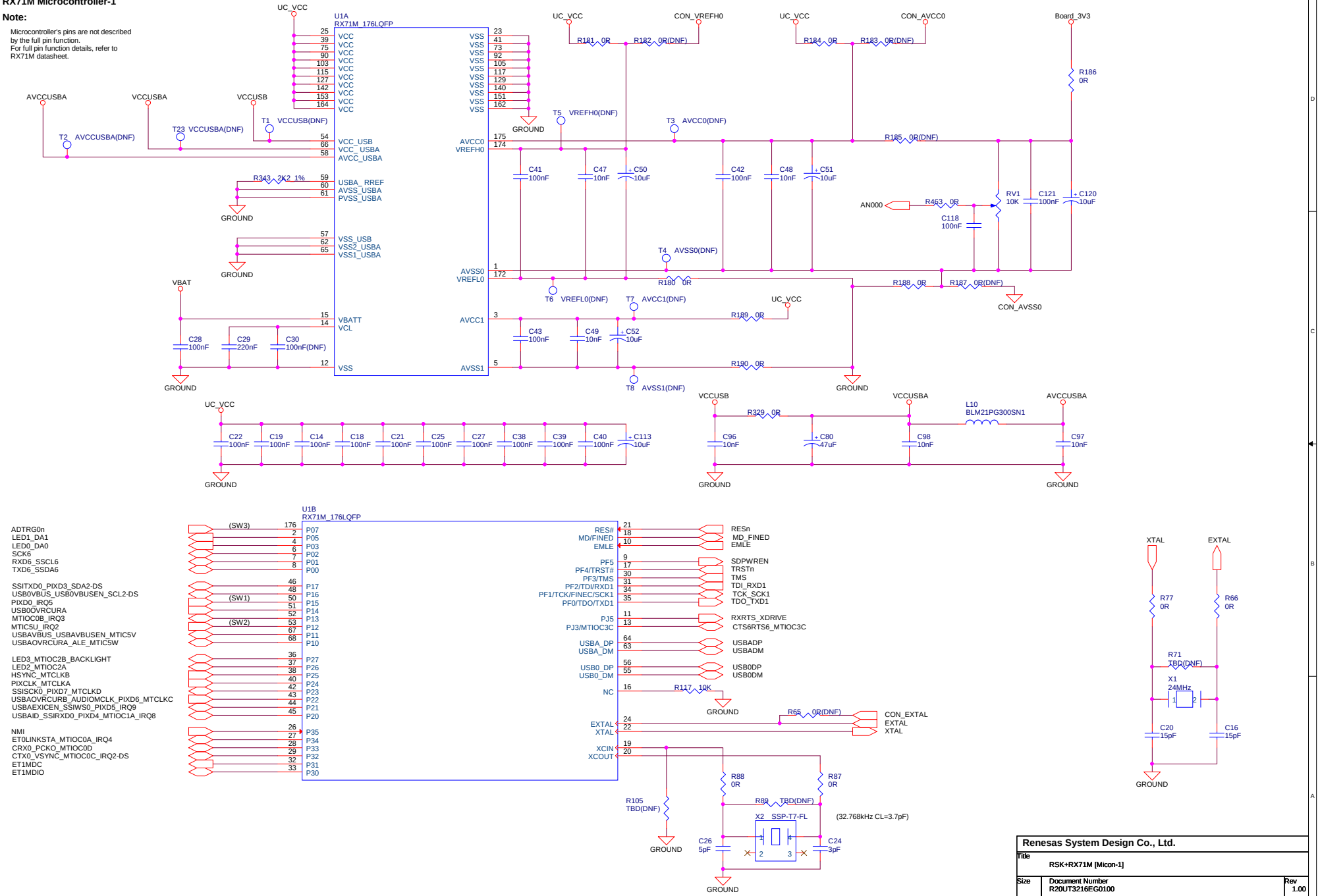
RX71M Microcontroller-1

Note:

Microcontroller's pins are not described by the full pin function.
For full pin function details, refer to RX71M datasheet.



Renesas System Design Co., Ltd.		
Title: RSK+RX71M [Micon-1]		
Size	Document Number: R20UT3216EG0100	Rev: 1.00
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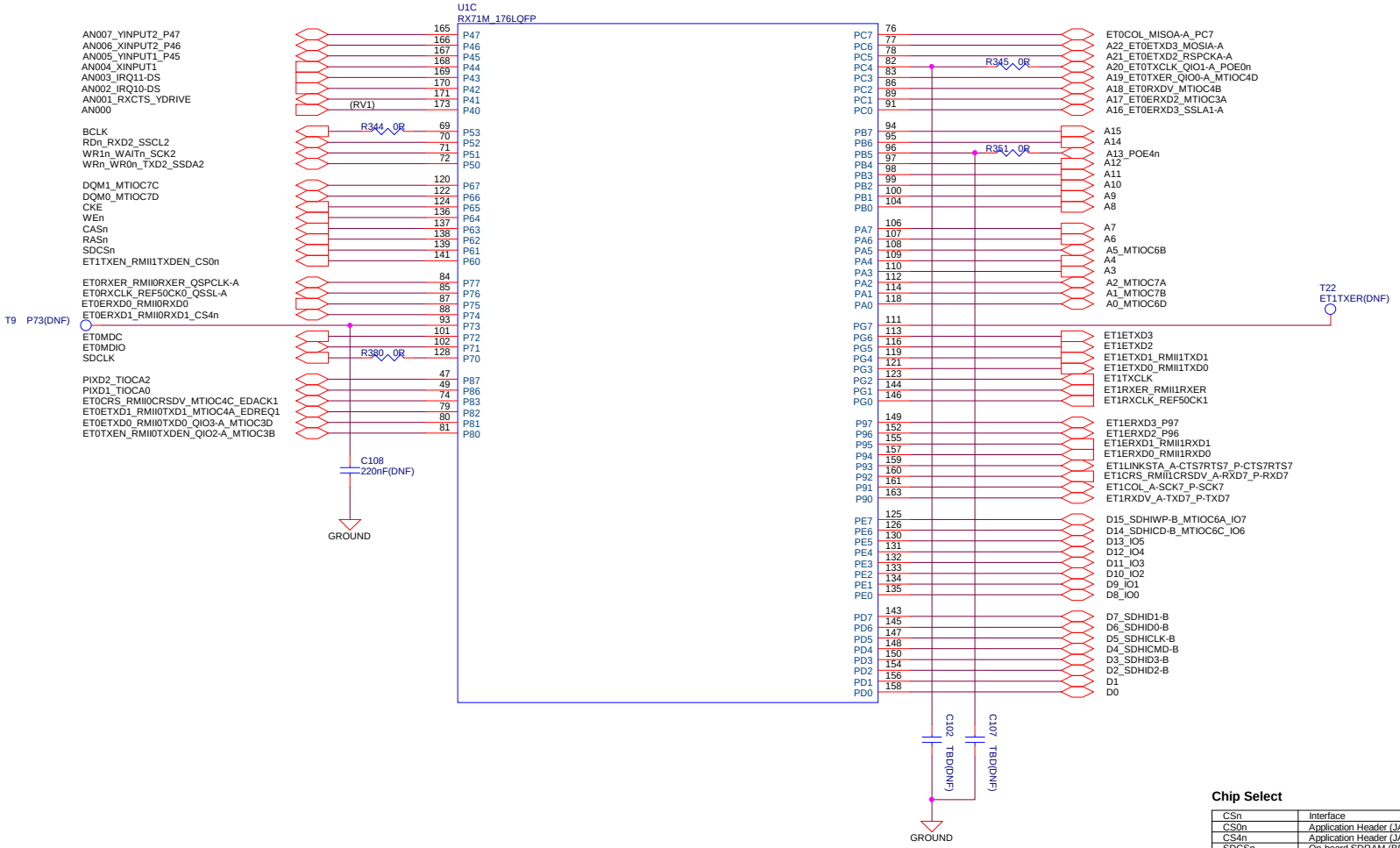
RX71M Microcontroller-2

Note:

Microcontroller's pins are not described
by the full pin function.
For full pin function details, refer to
RX71M datasheet.



Chip Select

CSn	Interface
CS0n	Application Header (JA3)
CS4n	Application Header (JA3)
SDCSn (CS1n)	On-board SDRAM (BD_SDCSn) / Application Header JA3 (CON_SDCSn)

RSPI Slave Select

SSL	Interface
SSLA1-A	On-board SPI Serial Flash

QSPI Slave Select

QSSL	Interface
QSSL-A	On-board QSPI Serial Flash (BD_QSSL-A) / TFT Header (TFT_QSSL-A)

Renesas System Design Co., Ltd.		
Title	**RSK+RX71M [Micon-2]**	
Size	**Document Number** R20UT3216EG0100	**Rev** 1.00
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MCU Pin Function Select-1

Default setting of DIP Switches.

SW5	Default
Pin1	ON
Pin2	ON
Pin3	OFF
Pin4	ON
Pin5	OFF
Pin6	ON
Pin7	OFF
Pin8	OFF
Pin9	ON
Pin10	OFF

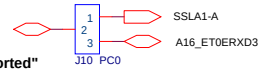
SW6	Default
Pin1	ON
Pin2	ON
Pin3	ON
Pin4	OFF
Pin5	ON
Pin6	OFF
Pin7	ON
Pin8	OFF
Pin9	ON
Pin10	OFF

SW7	Default
Pin1	ON
Pin2	OFF
Pin3	OFF
Pin4	ON
Pin5	OFF
Pin6	OFF
Pin7	ON
Pin8	OFF
Pin9	ON
Pin10	OFF

SW8	Default
Pin1	ON
Pin2	OFF
Pin3	ON
Pin4	OFF
Pin5	ON
Pin6	OFF
Pin7	ON
Pin8	OFF
Pin9	ON
Pin10	OFF

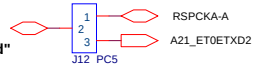
SW9	Default
Pin1	ON
Pin2	OFF
Pin3	ON
Pin4	OFF
Pin5	OFF
Pin6	OFF
Pin7	ON
Pin8	OFF
Pin9	OFF
Pin10	OFF

PC0(Pin91)
A16_ET0ERXD3_SSLA1-A



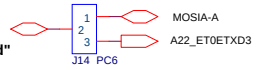
Default setting "Pin2-3 shorted"

PC5(Pin78)
A21_ET0ETXD2_RSPCKA-A



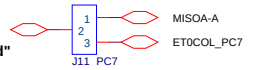
Default setting "Pin2-3 shorted"

PC6(Pin77)
A22_ET0ETXD3_MOSIA-A



Default setting "Pin2-3 shorted"

PC7(Pin76)
ET0COL_MISOA-A_PC7



Default setting "Pin2-3 shorted"

T26
ET0TXER(DNF)

SW5
SW DIP-10/SM

PC0(Pin91)	A16_ET0ERXD3	1 / 20	ET0ERXD3
PC1(Pin89)	A17_ET0ERXD2_MTIOC3A	2 / 19	ET0ERXD2
		3 / 18	MTIOC3A
PC2(Pin86)	A18_ET0RXDV_MTIOC4B	4 / 17	ET0RXDV
		5 / 16	MTIOC4B
PC3(Pin83)	A19_ET0TXER_QIO0-A_MTIOC4D	6 / 15	
		7 / 14	QIO0-A
		8 / 13	MTIOC4D
PC4(Pin82)	A20_ET0TXCLK_QIO1-A_POE0n	9 / 12	ET0TXCLK
		10 / 11	QIO1-A_POE0n

PC3(Pin83)
QIO0-A

PC4(Pin82)
QIO1-A_POE0n

R375 0R
R374 0R(DNF)
BD_QIO0-A
TFT_QIO0-A

R371 0R
R370 0R(DNF)
R372 0R(DNF)
BD_QIO1-A
TFT_QIO1-A
POE0n

SW6
SW DIP-10/SM

PC5(Pin78)	A21_ET0ETXD2	1 / 20	ET0ETXD2
PC6(Pin77)	A22_ET0ETXD3	2 / 19	ET0ETXD3
PC7(Pin76)	ET0COL_PC7	3 / 18	ET0COL
		4 / 17	PC7
P34(Pin27)	ET0LINKSTA_MTIOC0A_IRQ4	5 / 16	ET0LINKSTA
		6 / 15	MTIOC0A_IRQ4
P74(Pin88)	ET0ERXD1_RMII0RXD1_CS4n	7 / 14	ET0ERXD1_RMII0RXD1
		8 / 13	CS4n
P77(Pin84)	ET0RXER_RMII0RXER_QSPCLK-A	9 / 12	ET0RXER_RMII0RXER
		10 / 11	QSPCLK-A

P77(Pin84)
QSPCLK-A

R382 0R
R381 0R(DNF)
BD_QSPCLK-A
TFT_QSPCLK-A

SW7
SW DIP-10/SM

P80(Pin81)	ET0TXEN_RMII0TXDEN_QIO2-A_MTIOC3B	1 / 20	ET0TXEN_RMII0TXDEN
		2 / 19	QIO2-A
		3 / 18	MTIOC3B
P81(Pin80)	ET0ETXD0_RMII0TXD0_QIO3-A_MTIOC3D	4 / 17	ET0ETXD0_RMII0TXD0
		5 / 16	QIO3-A
		6 / 15	MTIOC3D
P82(Pin79)	ET0ETXD1_RMII0TXD1_MTIOC4A_EDREQ1	7 / 14	ET0ETXD1_RMII0TXD1
		8 / 13	MTIOC4A_EDREQ1
P83(Pin74)	ET0CRS_RMII0CRSDV_MTIOC4C_EDACK1	9 / 12	ET0CRS_RMII0CRSDV
		10 / 11	MTIOC4C_EDACK1

P82(Pin79)
MTIOC4A_EDREQ1

P83(Pin74)
MTIOC4C_EDACK1

R231 0R
R455 0R(DNF)
EDREQ1
MTIOC4A

R229 0R
R456 0R(DNF)
EDACK1
MTIOC4C

SW8
SW DIP-10/SM

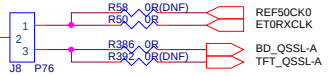
PD2(Pin154)	D2_SDHID2-B	1 / 20	D2
PD3(Pin150)	D3_SDHID3-B	2 / 19	SDHID2-B
PD4(Pin148)	D4_SDHICMD-B	3 / 18	D3
PD5(Pin147)	D5_SDHICLK-B	4 / 17	SDHID3-B
PD6(Pin145)	D6_SDHID0-B	5 / 16	D4
		6 / 15	SDHICMD-B
		7 / 14	D5
		8 / 13	SDHICLK-B
		9 / 12	D6
		10 / 11	SDHID0-B

SW9
SW DIP-10/SM

PD7(Pin143)	D7_SDHID1-B	1 / 20	D7
PE6(Pin126)	D14_SDHICD-B_MTIOC6C_IO6	2 / 19	SDHID1-B
		3 / 18	D14
PE7(Pin125)	D15_SDHIWP-B_MTIOC6A_IO7	4 / 17	SDHICD-B
		5 / 16	MTIOC6C
		6 / 15	IO6
		7 / 14	D15
		8 / 13	SDHIWP-B
		9 / 12	MTIOC6A
		10 / 11	IO7

P76(Pin85)
ET0RXCLK_REF50CK0_QSSL-A

Default setting "Pin1-2 shorted"



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Title	RSK+RX71M [MCU Pin Function Select-1]		
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MCU Pin Function Select-2

P00(Pin8)
TXD6_SSDA6
R119 0R
R118 0R
TXD6
SSDA6

P01(Pin7)
RXD6_SSCL6
R128 0R
R127 0R
RXD6
SSCL6

P03(Pin4)
LED0_DA0
R281 0R
R195 0R(DNF)
LED0
DA0

P05(Pin2)
LED1_DA1
R284 0R
R194 0R(DNF)
LED1
DA1

P10(Pin68)
USBAOVRCURA_ALE_MTIC5W
R362 0R
R480 0R(DNF)
R76 0R(DNF)
USBAOVRCURA
ALE
MTIC5W

P11(Pin67)
USBAVBUS_USBAVBUSEN_MTIC5V
Default setting "Pin1-2 shorted"
R55 0R(DNF)
J7 P11
MTIC5V
USBAVBUS
USBAVBUSEN

P12(Pin53)
MTIC5U_IRQ2
R83 0R(DNF)
R367 0R
MTIC5U
IRQ2

P15(Pin50)
PIXD0_IRQ5
R488 0R
R276 0R(DNF)
IRQ5
PIXD0

P16(Pin48)
USB0VBUS_USB0VBUSEN_SCL2-DS
Default setting of J21 "Open"
Default setting of J3 "Pin1-2 shorted"
SCL2-DS
J21 P16_SCL
J3 P16_USB
USB0VBUS
USB0VBUSEN

P17(Pin46)
SSITXD0_PIXD3_SDA2-DS
R292 0R(DNF)
R225 0R(DNF)
R192 0R
SSITXD0
PIXD3
SDA2-DS

P20(Pin45)
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8
R322 0R
R51 0R(DNF)
R290 0R(DNF)
R272 0R(DNF)
R143 0R(DNF)
IRQ8
USBAID
SSIRXD0
PIXD4
MTIOC1A

P21(Pin44)
USBAEXICEN_SSIWS0_PIXD5_IRQ9
R334 0R
R323 0R(DNF)
R293 0R(DNF)
R273 0R(DNF)
IRQ9
USBAEXICEN
SSIWS0
PIXD5

P22(Pin43)
USBAOVRCURB_AUDIOMCLK_PIXD6_MTCLKC
R289 0R(DNF)
R32 0R(DNF)
R270 0R
R72 0R(DNF)
AUDIOMCLK
USBAOVRCURB
PIXD6
MTCLKC

P23(Pin42)
SSISCK0_PIXD7_MTCLKD
R291 0R(DNF)
R271 0R
R342 0R(DNF)
SSISCK0
PIXD7
MTCLKD

P24(Pin40)
PIXCLK_MTCLKA
R267 0R
R142 0R(DNF)
PIXCLK
MTCLKA

P25(Pin38)
HSYNC_MTCLKB
R268 0R
R126 0R(DNF)
HSYNC
MTCLKB

P26(Pin37)
LED2_MTIOC2A
R285 0R
R121 0R(DNF)
LED2
MTIOC2A

P27(Pin36)
LED3_MTIOC2B_BACKLIGHT
Default setting "Pin1-2 shorted"
J24 P27
R177 0R(DNF)
R225 0R
LED3
MTIOC2B
BACKLIGHT

P32(Pin29)
CTX0_VSYNC_MTIOC0C_IRQ2-DS
Default setting "Pin1-2 shorted"
R269 0R(DNF)
J15 P32
VSYNC
CTX0
MTIOC0C_IRQ2-DS

P33(Pin28)
CRX0_PCKO_MTIOC0D
Default setting "Pin1-2 shorted"
R294 0R(DNF)
J17 P33
PCKO
CRX0
MTIOC0D

P41(Pin171)
AN001_RXCTS_YDRIVE
R207 0R(DNF)
R419 0R(DNF)
R237 0R
AN001
RXCTS
YDRIVE

P42(Pin170)
AN002_IRQ10-DS
R203 0R
R178 0R(DNF)
AN002
IRQ10-DS

P43(Pin169)
AN003_IRQ11-DS
R202 0R
R176 0R(DNF)
AN003
IRQ11-DS

P44(Pin168)
AN004_XINPUT1
R238 0R
R124 0R(DNF)
XINPUT1
AN004

P45(Pin167)
AN005_YINPUT1_P45
R239 0R
R133 0R(DNF)
R427 0R
YINPUT1
AN005
P45

P46(Pin166)
AN006_XINPUT2_P46
R240 0R
R130 0R(DNF)
R315 0R
XINPUT2
AN006
P46

P47(Pin165)
AN007_YINPUT2_P47
R241 0R
R127 0R(DNF)
R313 0R
YINPUT2
AN007
P47

P50(Pin72)
WRn_WR0n_TXD2_SSDA2
R116 0R
R124 0R(DNF)
R104 0R(DNF)
R125 0R(DNF)
WRn
WR0n
TXD2
SSDA2

P51(Pin71)
WR1n_WAITn_SCK2
R483 0R
R478 0R(DNF)
R484 0R(DNF)
WAITn
WR1n
SCK2

P52(Pin70)
RDn_RXD2_SSCL2
R86 0R
R85 0R(DNF)
R84 0R(DNF)
RDn
RXD2
SSCL2

P60(Pin141)
ET1TXEN_RMII1TXDEN_CS0n
R111 0R
R397 0R(DNF)
ET1TXEN_RMII1TXDEN
CS0n

P61(Pin139)
SDCSn
R435 0R
R398 0R(DNF)
BD_SDCSn
CON_SDCSn

P66(Pin122)
DQM0_MTIOC7D
R430 0R
R59 0R(DNF)
DQM0
MTIOC7D

P67(Pin120)
DQM1_MTIOC7C
R443 0R
R67 0R(DNF)
DQM1
MTIOC7C

P86(Pin49)
PIXD1_TIOCA0
R277 0R
R168 0R(DNF)
PIXD1
TIOCA0

P87(Pin47)
PIXD2_TIOCA2
R274 0R
R169 0R(DNF)
PIXD2
TIOCA2

P90(Pin163)
ET1RXDV_A-TXD7_P-TXD7
Default setting "Pin2-3 shorted"
J16 P90
R152 0R
R411 0R(DNF)
ET1RXDV
A-TXD7
P-TXD7

P91(Pin161)
ET1COL_A-SCK7_P-SCK7
Default setting "Pin1-2 shorted"
J20 P91
R198 0R
R417 0R(DNF)
ET1COL
A-SCK7
P-SCK7

P92(Pin160)
ET1CRS_RMII1CRSDV_A-RXD7_P-RXD7
Default setting "Pin2-3 shorted"
J18 P92
R172 0R
R415 0R(DNF)
ET1CRS_RMII1CRSDV
A-RXD7
P-RXD7

P93(Pin159)
ET1LINKSTA_A-CTS7RTS7_P-CTS7RTS7
R407 0R
R191 0R(DNF)
R408 0R(DNF)
ET1LINKSTA
A-CTS7RTS7
P-CTS7RTS7

P96(Pin152)
ET1ERXD2_P96
R388 0R
R175 0R(DNF)
ET1ERXD2
P96

P97(Pin149)
ET1ERXD3_P97
R389 0R
R167 0R(DNF)
ET1ERXD3
P97

PA0(Pin118)
A0_MTIOC6D
R247 0R
R340 0R(DNF)
A0
MTIOC6D

PA1(Pin114)
A1_MTIOC7B
R421 0R
R317 0R(DNF)
A1
MTIOC7B

PA2(Pin112)
A2_MTIOC7A
R422 0R
R309 0R(DNF)
A2
MTIOC7A

PA5(Pin108)
A5_MTIOC6B
R450 0R
R368 0R(DNF)
A5
MTIOC6B

PB5(Pin96)
A13_POE4n
R420 0R
R359 0R(DNF)
A13
POE4n

PE0(Pin135)
D8_IO0
R442 0R
R405 0R(DNF)
D8
IO0

PE1(Pin134)
D9_IO1
R441 0R
R401 0R(DNF)
D9
IO1

PE2(Pin133)
D10_IO2
R440 0R
R400 0R(DNF)
D10
IO2

PE3(Pin132)
D11_IO3
R226 0R
R394 0R(DNF)
D11
IO3

PE4(Pin131)
D12_IO4
R227 0R
R393 0R(DNF)
D12
IO4

PE5(Pin130)
D13_IO5
R228 0R
R390 0R(DNF)
D13
IO5

PF0(Pin35)
TDO_TXD1
T30
TDO_TXD1(DNF)
R253 0R
R151 0R(DNF)
TDO
TXD1

PF1(Pin34)
TCK_SCK1
R261 0R
R378 0R(DNF)
TCK
SCK1

PF2(Pin31)
TDI_RXD1
T31
TDI_RXD1(DNF)
R243 0R
R165 0R(DNF)
TDI
RXD1

PG0(Pin146)
ET1RXCLK_REF50CK1
R396 0R
R144 0R(DNF)
ET1RXCLK
REF50CK1

PJ3(Pin13)
CTS6RTS6_MTIOC3C
R323 0R(DNF)
R240 0R
CTS6RTS6
MTIOC3C

PJ5(Pin11)
RXRTS_XDRIVE
R409 0R(DNF)
R236 0R
RXRTS
XDRIVE

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Title: RSK+RX71M [MCU Pin Function Select-2]		
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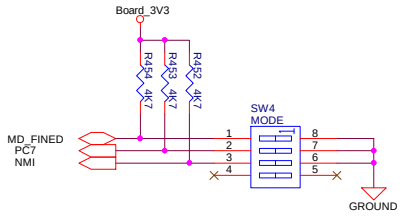
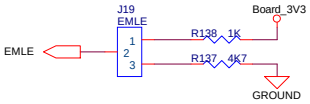
MCU & Emulator Mode Setting





MCU Operating Mode Configuration

SW4 Pin1	SW4 Pin2	Operating Mode
OFF	Don't care	Single Chip Mode
ON	ON	Boot Mode (SCI)
ON	OFF	User Boot Mode USB Boot Mode

Power Configuration for USB Boot Mode

SW4 Pin3	Power Configuration
OFF	Bus Powered
ON	Self Powered

Default setting of SW4.

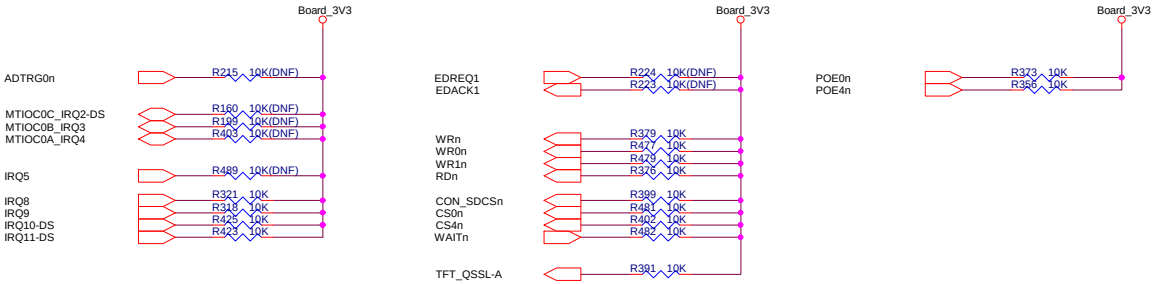
SW4	Default
Pin1	OFF
Pin2	OFF
Pin3	OFF
Pin4	OFF

Emulator Configuration

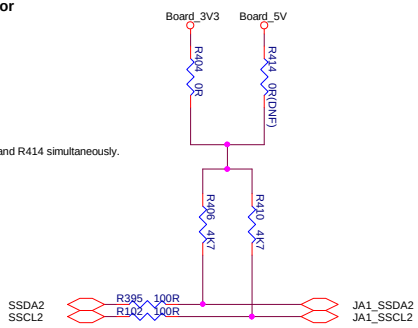
J19	Emulator Configuration
Shorted Pin1-2	E1 debugging with Hot plug-in
Shorted Pin2-3	E1 normal debugging Microcontroller single operation (without E1/E20)
all open	DO NOT SET

Default setting of J19 "Pin2-3 shorted"

Option pull-up resistor

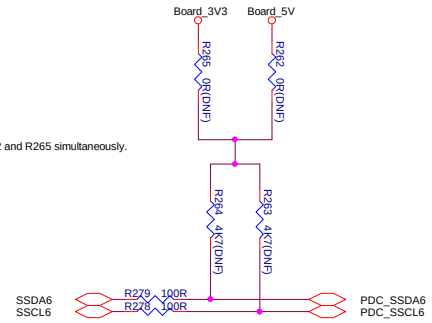


Simple IIC pull-up resistor



Warning:

NEVER FIT R404 and R414 simultaneously.



Warning:

NEVER FIT R262 and R265 simultaneously.

Renesas System Design Co., Ltd.		
Title: RSK+RX71M [MCU & Emulator Mode Setting]		
Size	Document Number: R20UT3216EG0100	Rev: 1.00
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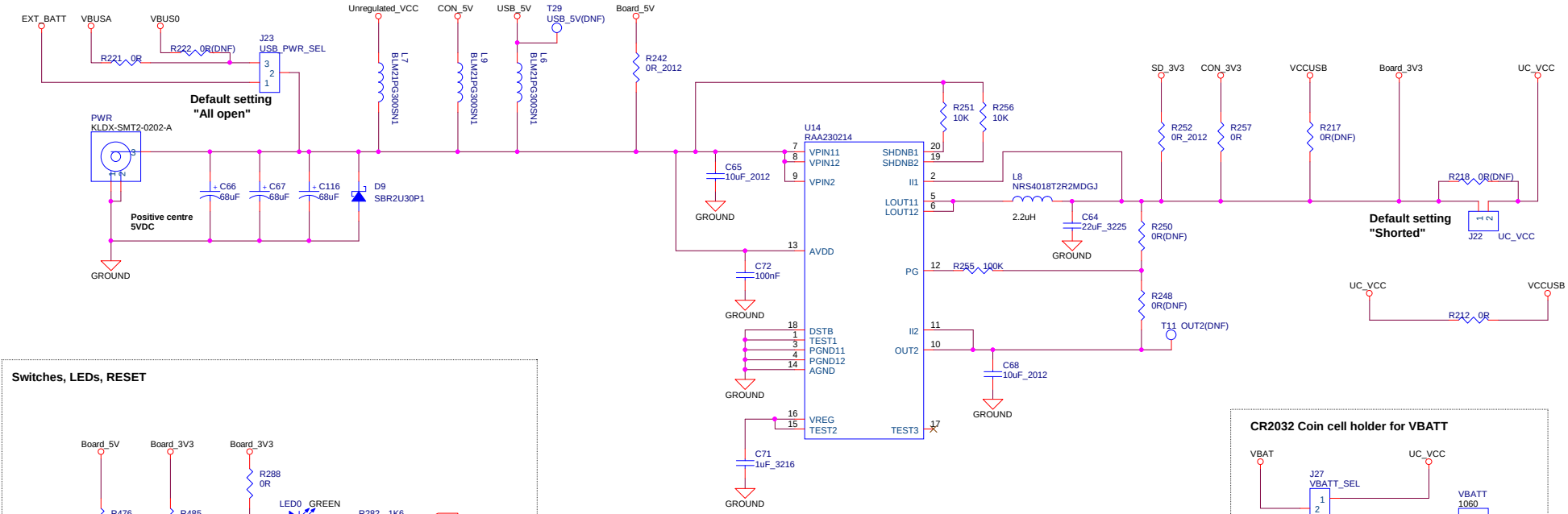
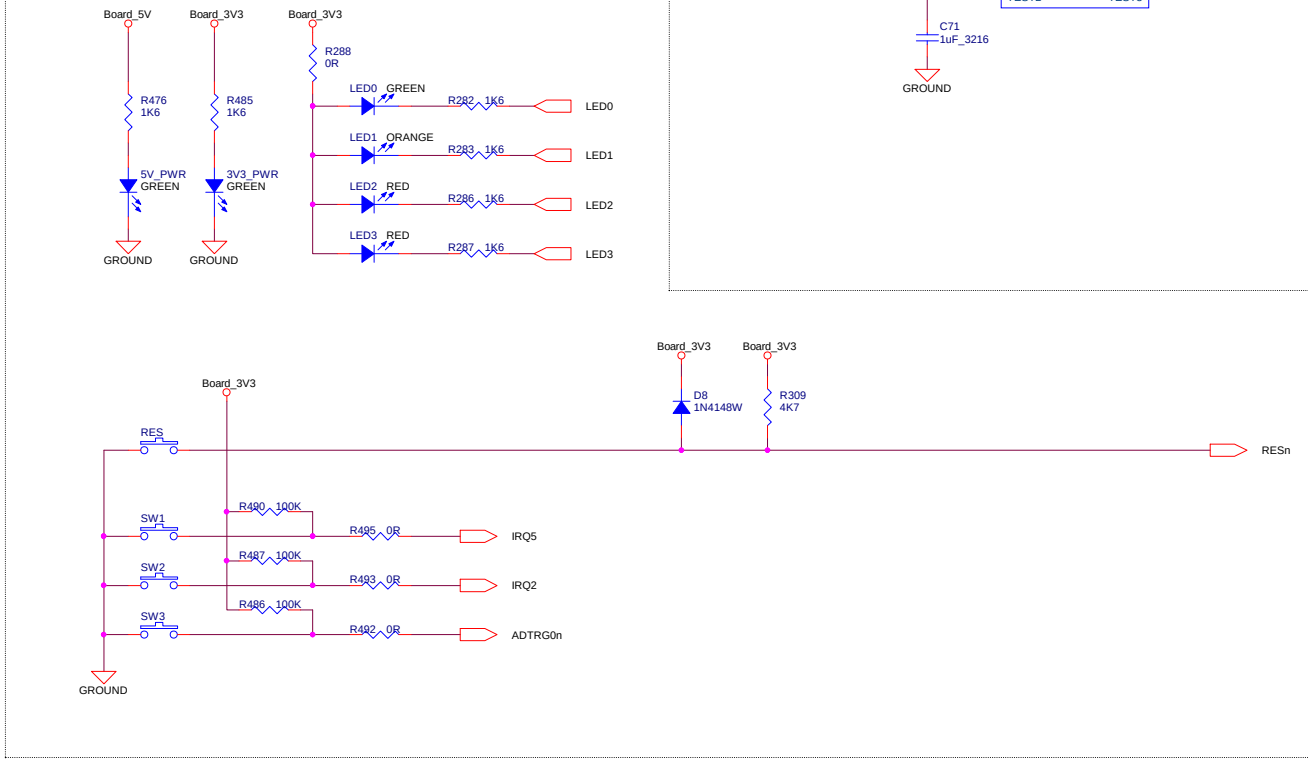
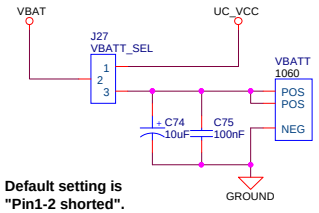
Power Supply Unit



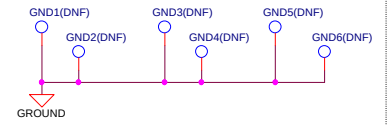
Switches, LEDs, RESET



CR2032 Coin cell holder for VBATT



Ground Test Point



Renesas System Design Co., Ltd.		
Title: RSK+RX71M [PSU, Reset, Switches, LEDs]		
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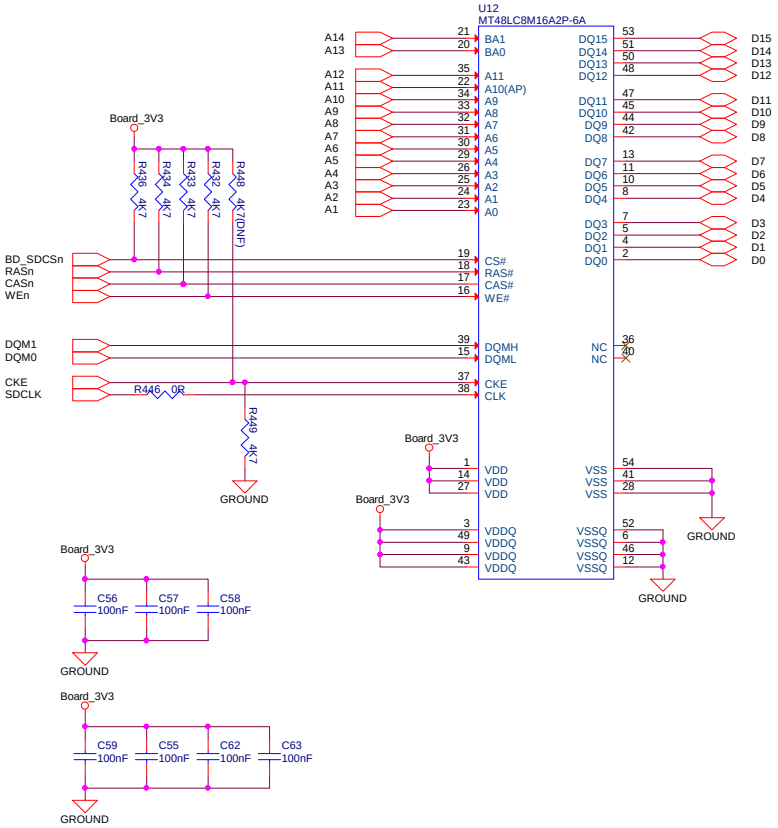
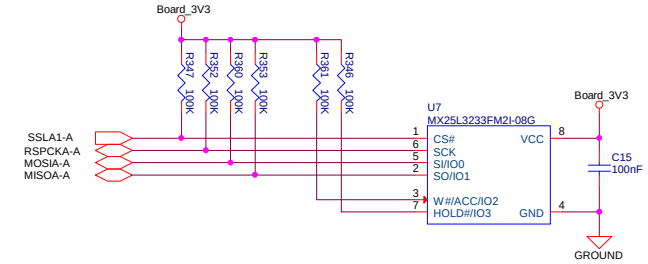
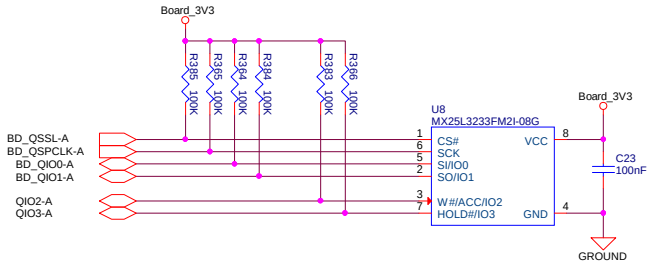
SDRAM(128Mbits)



RSPI- SPI Serial Flash(32Mbits)



QSPI- SPI Serial Flash(32Mbits)

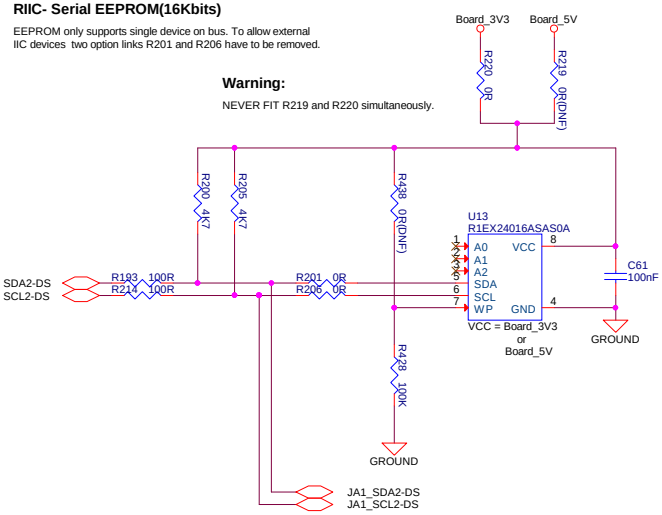


RIIC- Serial EEPROM(16Kbits)

EEPROM only supports single device on bus. To allow external IIC devices two option links R201 and R206 have to be removed.

Warning:

NEVER FIT R219 and R220 simultaneously.



Renesas System Design Co., Ltd.		
Title: **RSK+RX71M [On-board Memory]**		
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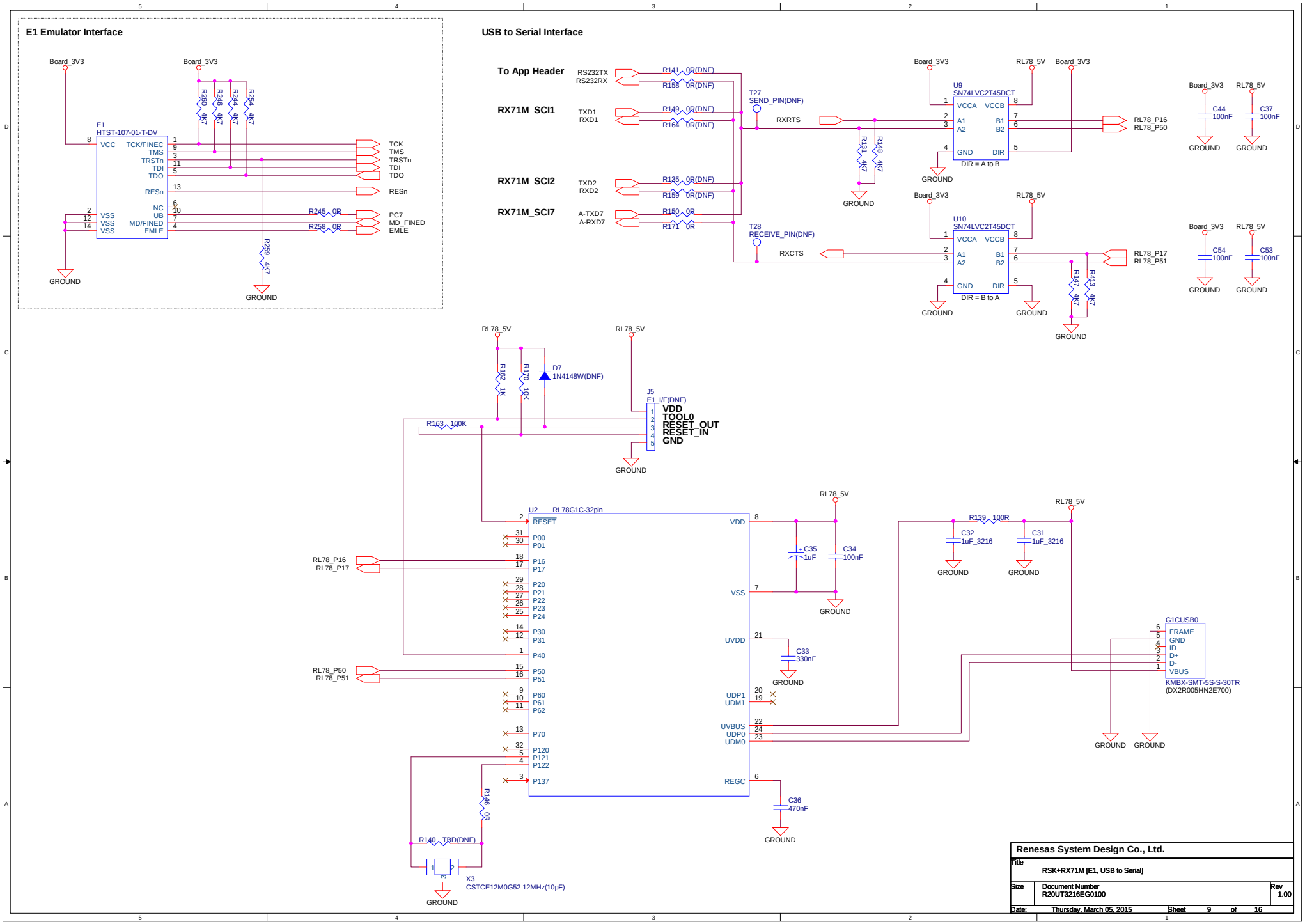
E1 Emulator Interface
USB to Serial Interface
To App Header
RX71M_SCI1
RX71M_SCI2
RX71M_SCI7
E1
HTST-107-01-T-DV
U2 RL78G1C-32pin
U9
SN74LVC2T45DCT
U10
SN74LVC2T45DCT
DIR = A to B
DIR = B to A
J5
E1_I/F(DNF)
VDD
TOOL0
RESET_OUT
RESET_IN
GND
D7
1N4148W(DNF)
G1CUSB0
KMBX-SMT-5S-S-30TR
(DX2R005HN2E700)
X3
CSTCE12M0G52 12MHz(10pF)
Board_3V3
RL78_5V
GROUND
Renesas System Design Co., Ltd.
RSK+RX71M [E1, USB to Serial]
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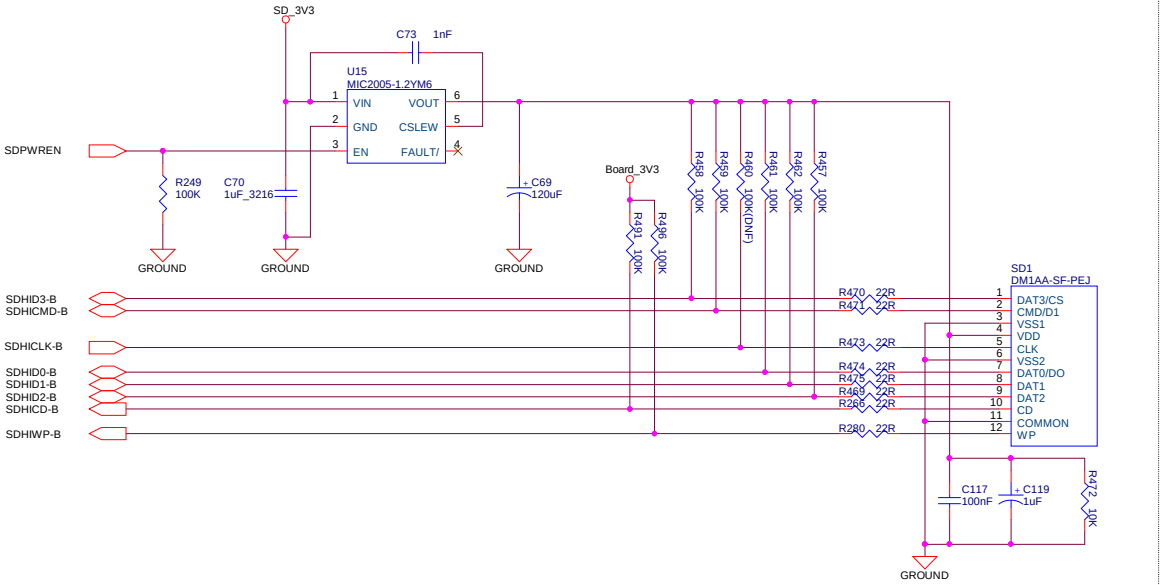
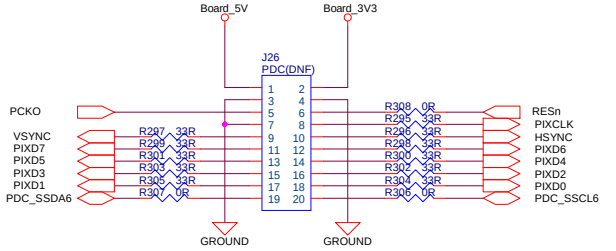
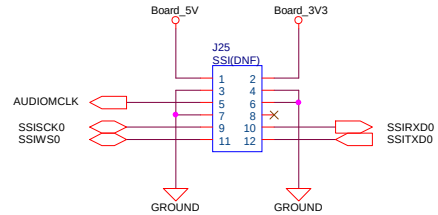
SD Slot



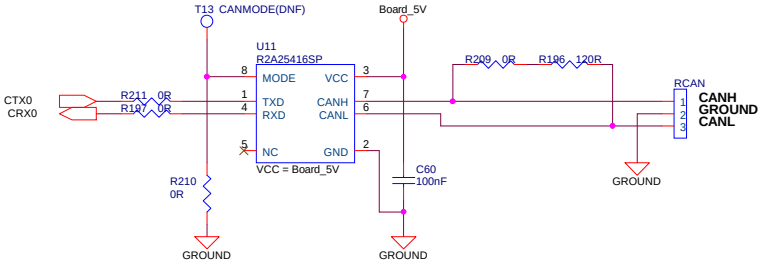
PDC



SSI



RCAN



Renesas System Design Co., Ltd.		
Title: RSK+RX71M [SD Slot, RCAN, PDC & SSI Interface]		
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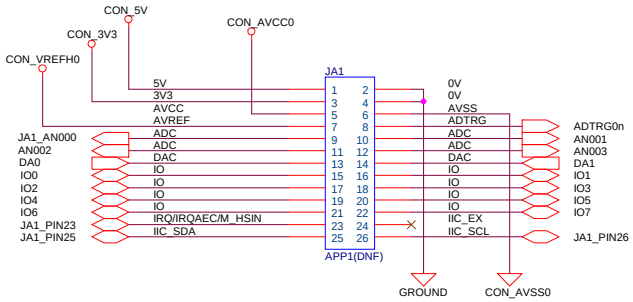
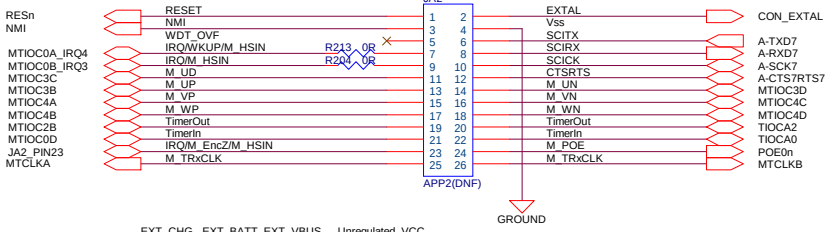
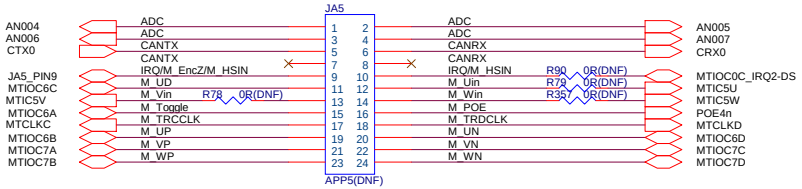
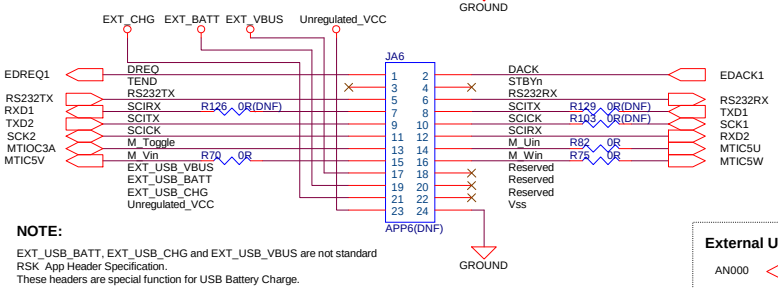
Application Headers





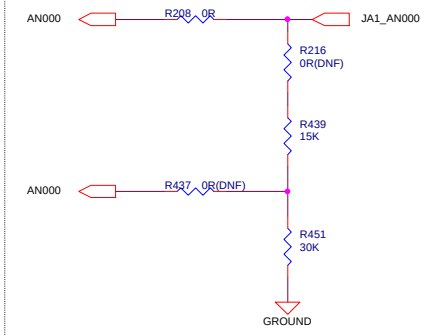


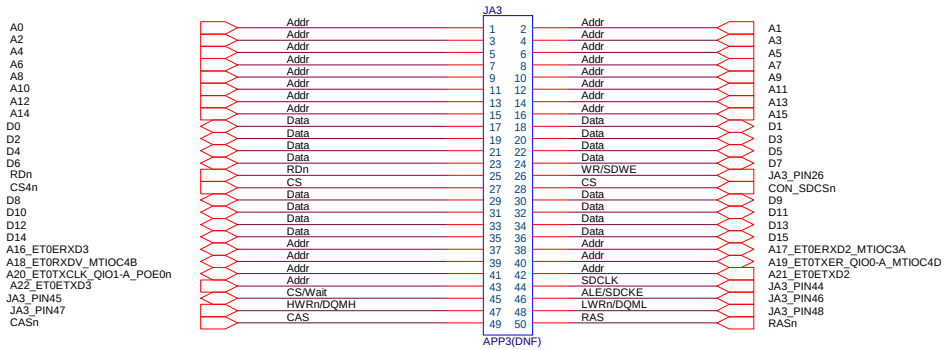


NOTE:

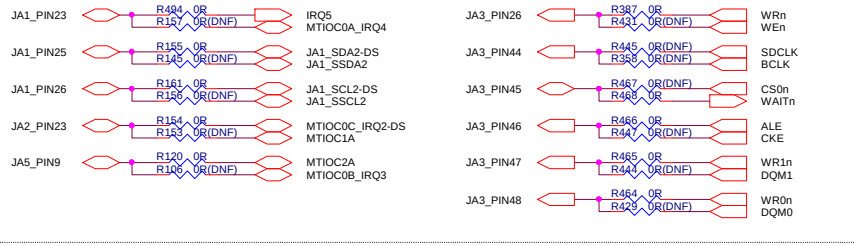
EXT_USB_BATT, EXT_USB_CHG and EXT_USB_VBUS are not standard RSK App Header Specification.
These headers are special function for USB Battery Charge.

External USB Battery Charge IC Monitor





Application Header Function Select



Renesas System Design Co., Ltd.		
Title: RSK+RX71M [Application Headers]		
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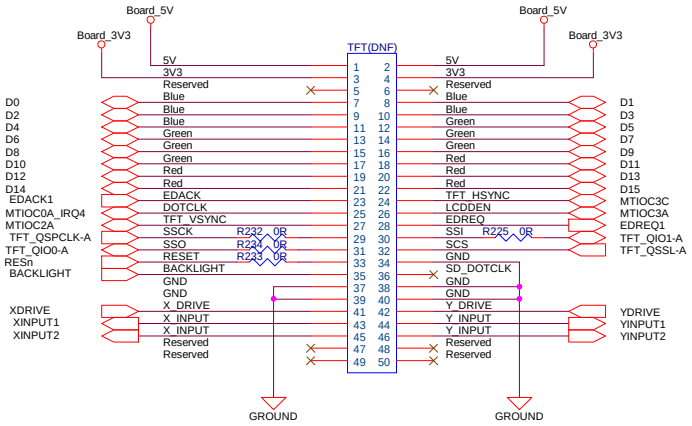
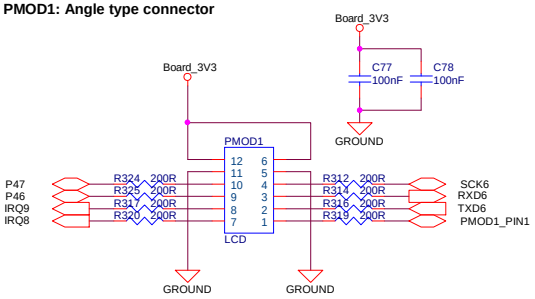
LCD Direct Drive Header (TFT)

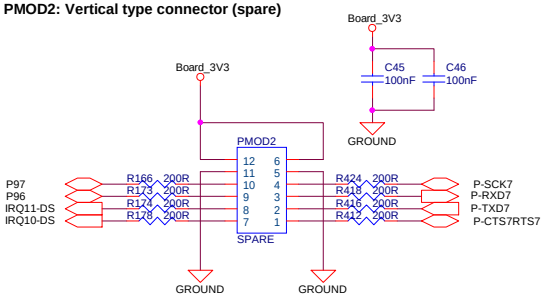


Pmod connectors

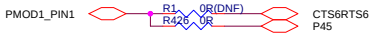
PMOD1: Angle type connector



PMOD2: Vertical type connector (spare)



Pmod Function Select



Renesas System Design Co., Ltd.		
Title: RSK+RX71M [TFT, Pmod]		
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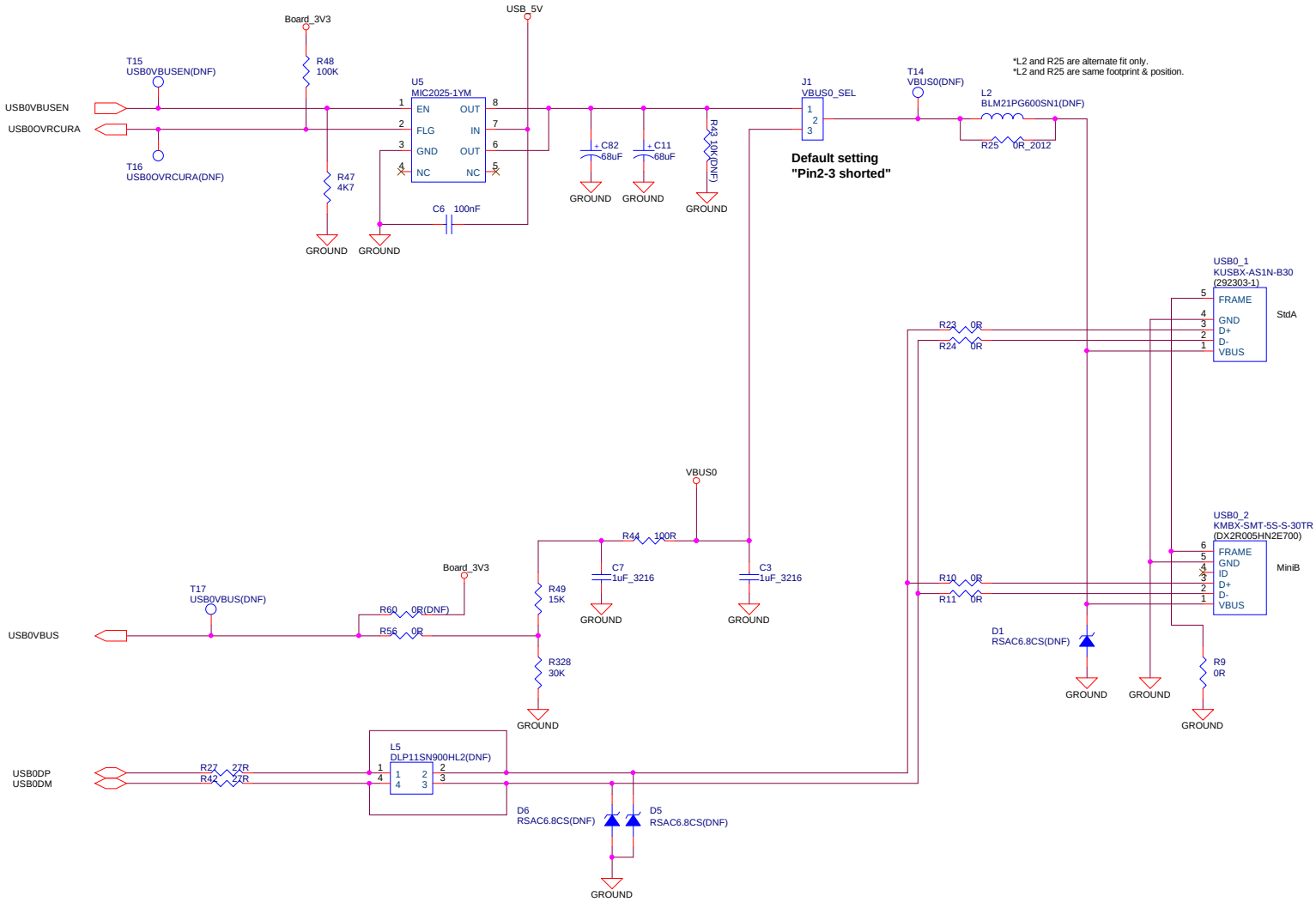
USB0 Host/Function

Self-powered/Bus-powered Configuration for Function Mode

R56	R60	
Fit	Remove	Self-powered
Remove	Fit	Bus-powered

USB0 Host/Function Select

J1	
1-2 shorted	Host Mode
2-3 shorted	Function Mode



Renesas System Design Co., Ltd.		
Title: RSK+RX71M [USB0]		
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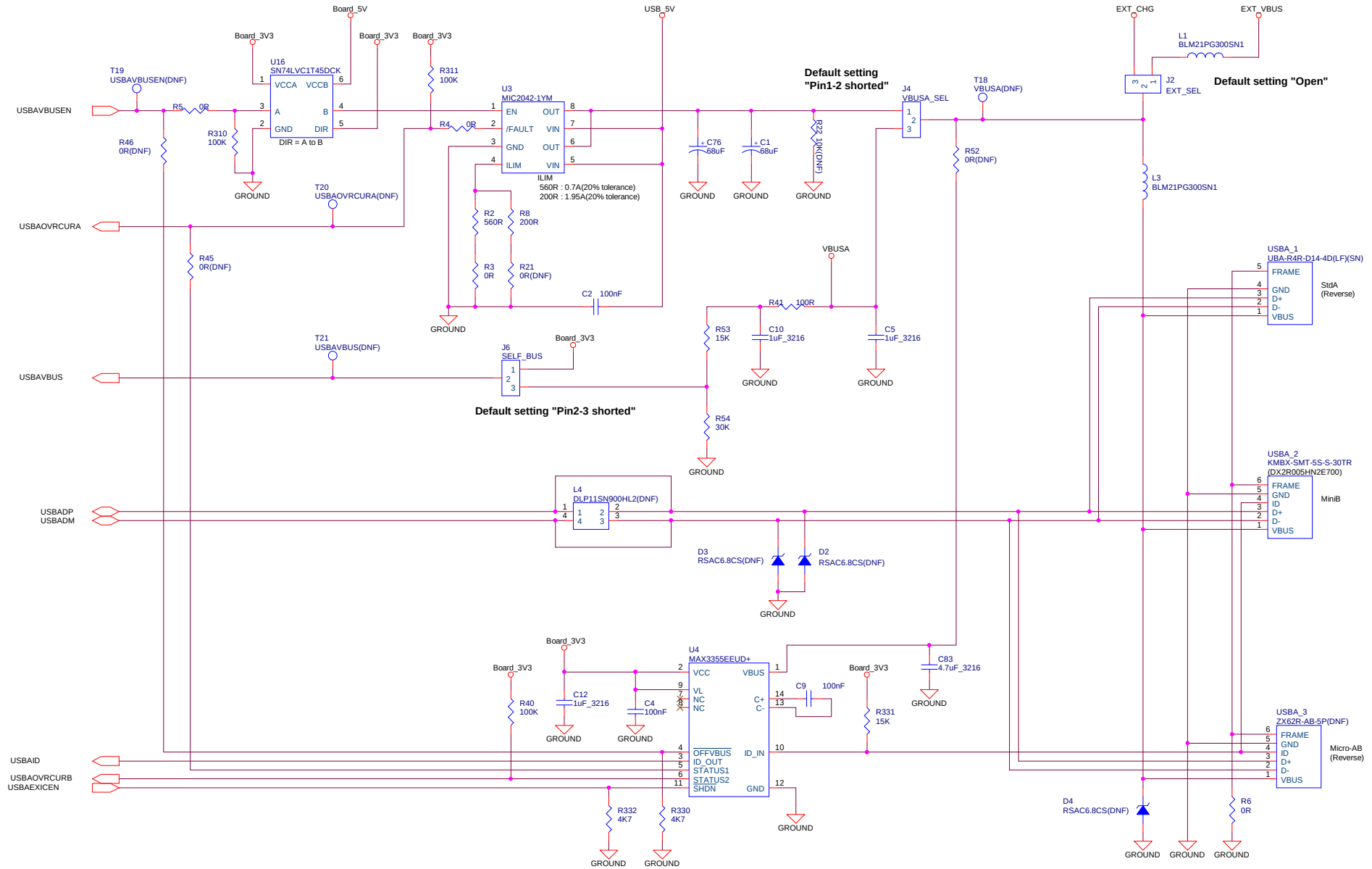
USBA Host/Function/OTG



USBA Host/Function/OTG Select

J4	R52	
1-2 shorted	Remove	Host Mode
2-3 shorted	Remove	Function Mode
All open	Fit	OTG Mode

Self/Bus Power Configuration for Function Mode

J6	
1-2 shorted	Bus-powered
2-3 shorted	Self-powered

USBAOVRCURA Select

R4	R45	
Fit	Remove	Host Mode
Remove	Fit	OTG Mode

USBAVBUSEN Select

R5	R46	
Fit	Remove	Host Mode
Remove	Fit	OTG Mode

Renesas System Design Co., Ltd.

Title	RSK+RX71M [USBA]	
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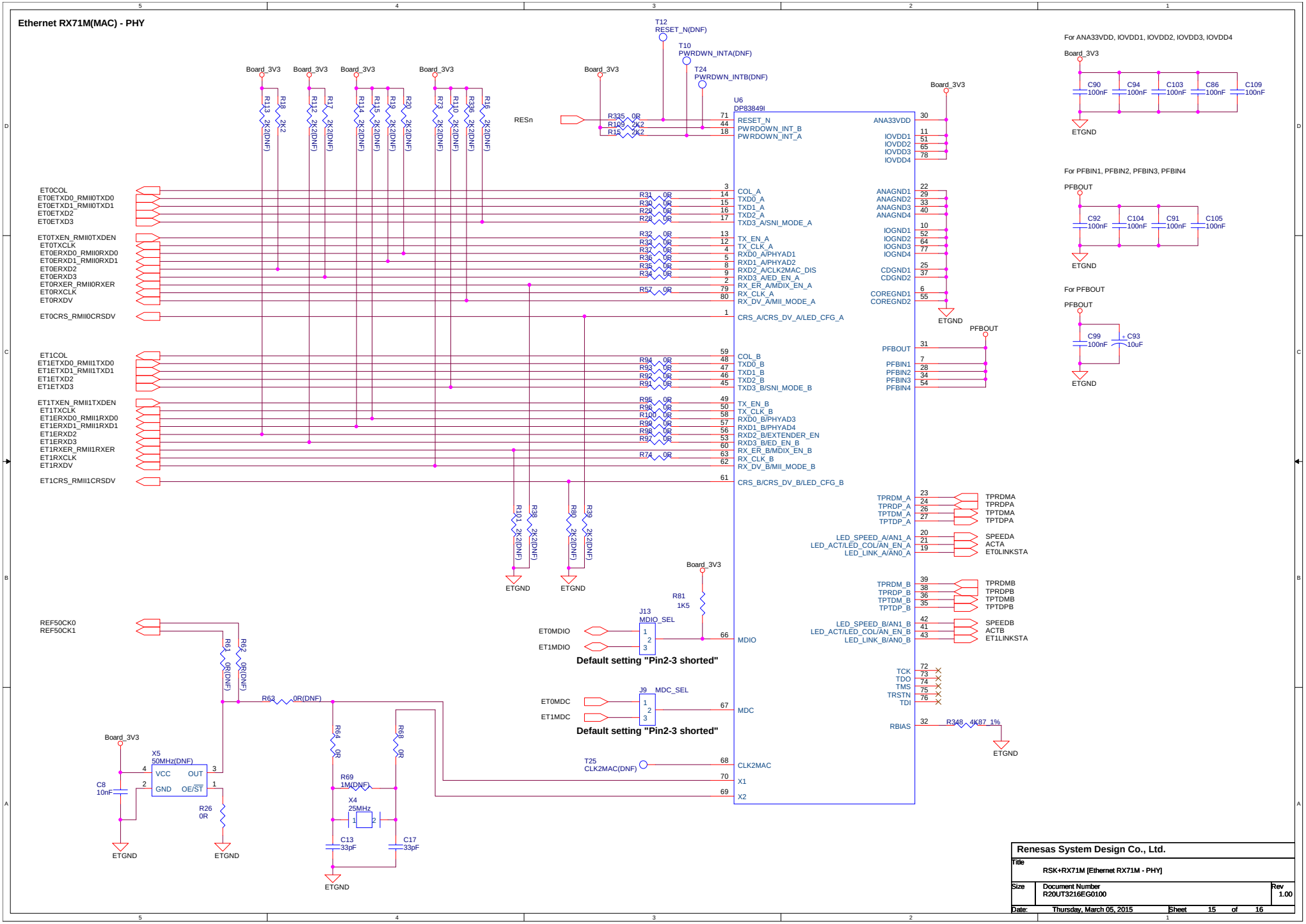
Ethernet RX71M(MAC) - PHY



Renesas System Design Co., Ltd.	
Title	RSK+RX71M [Ethernet RX71M - PHY]
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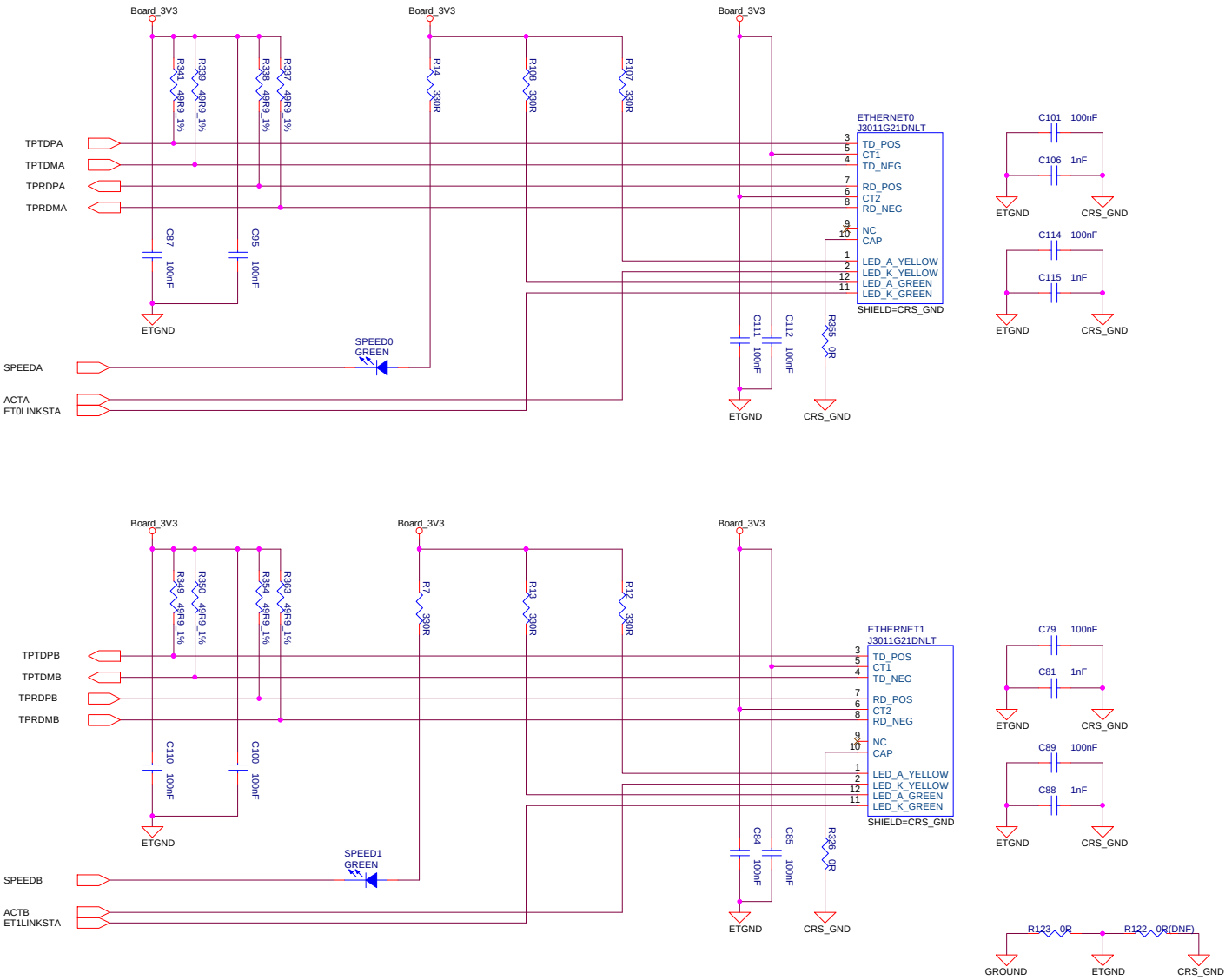
Ethernet RJ45



Renesas System Design Co., Ltd.		
Title: RSK+RX71M [Ethernet RJ45]		
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Revision History

REV	DATE	PAGE	DESCRIPTION
1.00	05.03.2015	---	1st release edition.

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