Renesas Starter Kit+ for RX65N-2MB
CPU Board Schematics

REV	REF	DATE	DRAWN BY
1.00	Release	11.05.2017	KOS
2.00	Release (TRAC #1479)	10.11.2017	YOI

Note:

C : Capacitor
D : Diode
R : Fixed Resistor
RV : Potentiometer
MR : Resistor Array
L : Inductor
U : Integrated Circuit
X : Crystal, Oscillator
RES : Reset Switch
SW : Switch
LED : Light Emitting Diode
PWR : Power Jack
J : Connector, Jumper

*** "DNF" marking means that component is not fitted by default.**

Board Code:

RTK50565N2C00000BE : RSK+RX65N-2MB MP Board

REEL Drawing No. D014902_04

Renesas Electronics Corporation		
Title: RSK+RX65N-2MB [Index]		
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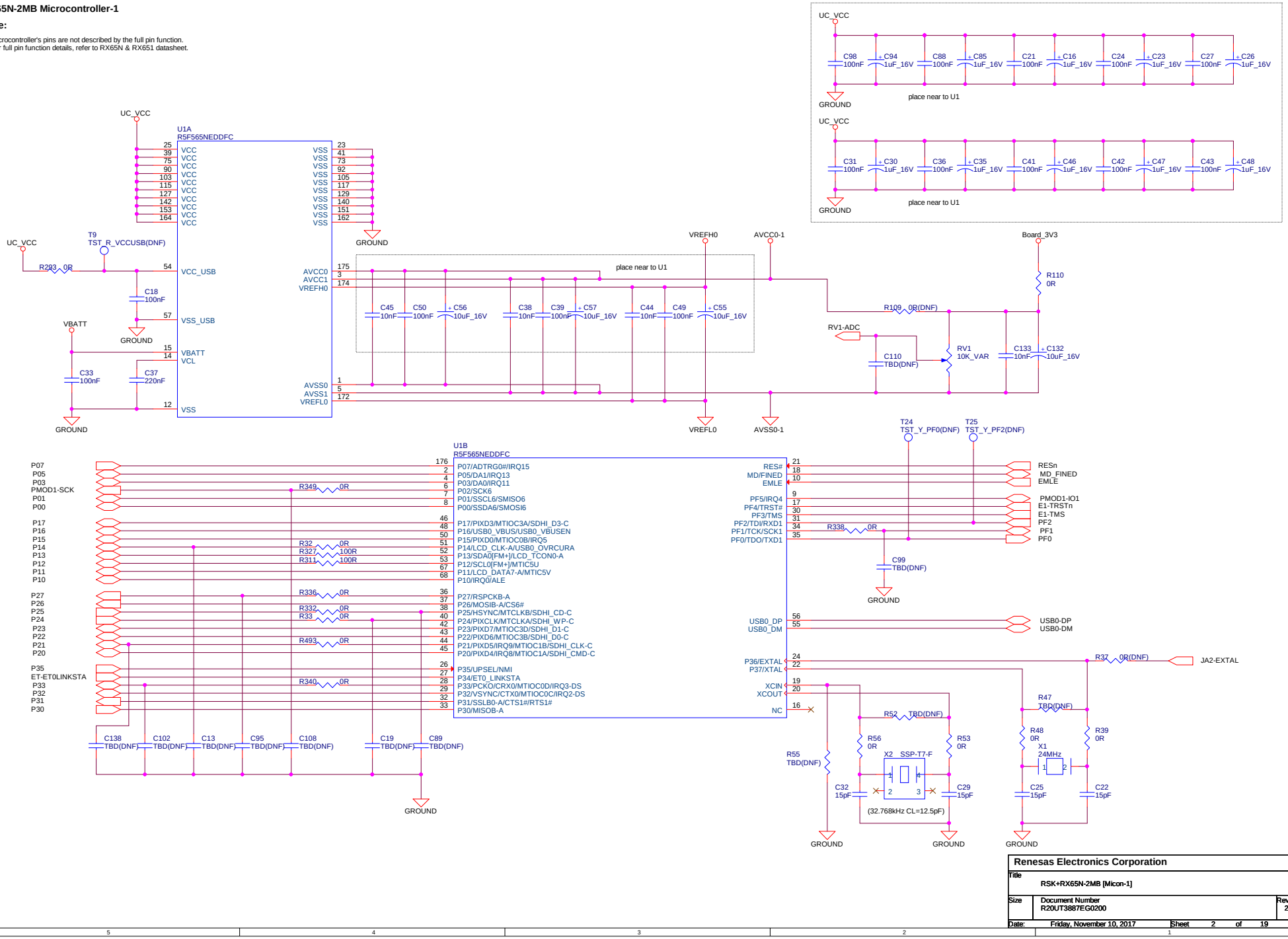
RX65N-2MB Microcontroller-1

Note:

Microcontroller's pins are not described by the full pin function.
For full pin function details, refer to RX65N & RX651 datasheet.



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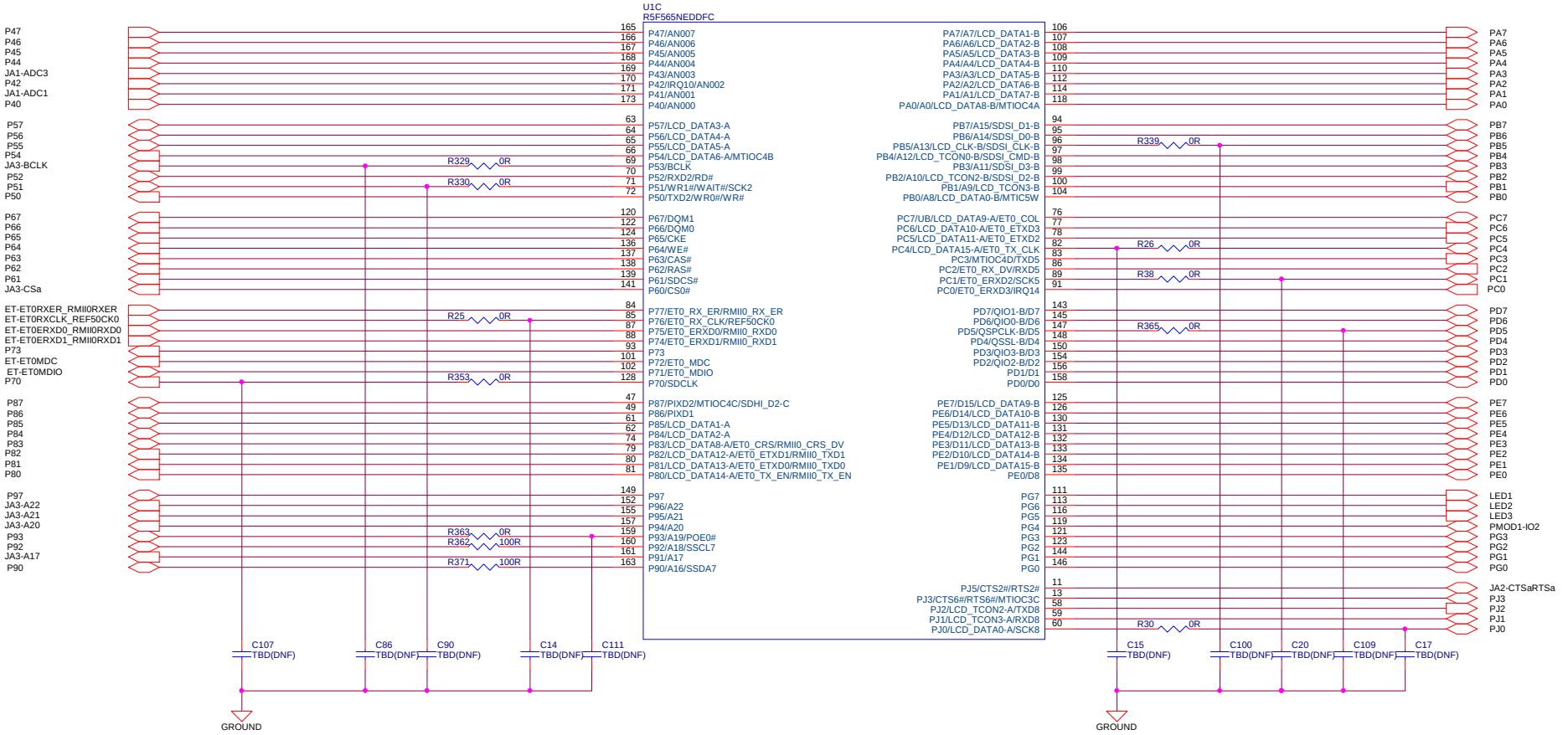
RX65N-2MB Microcontroller-2

Note:

Microcontroller's pins are not described by the full pin function.
For full pin function details, refer to RX65N & RX651 datasheet.



Chip Select

CSn	Interface
CS0n	Application Header (JA3-CSa)
CS6n	Application Header (JA3-CSc)
SDCSn (CS1n)	On-board SDRAM (SDRAM-SDCSn) / Application Header (JA3-CSb)

RSPI Slave Select

SSL	Interface
SSLB0-A	On-board Serial Flash (RSPI-CS) / TFT Header (TFT-CS)

QSPI Slave Select

QSSL	Interface
QSSL-B	On-board Serial Flash (QSPI-CS)

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MCU Pin Function Select-1

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MCU Pin Function Select-2

P67(Pin120) P67 — R132 0R, R413 0R(DNF) — SDRAM-DQMH, JA3-DQMH

P66(Pin122) P66 — R388 0R, R387 0R(DNF) — SDRAM-DQML, JA3-DQML

P65(Pin124) P65 — R130 0R, R121 0R(DNF) — SDRAM-CKE, JA3-CKE

P64(Pin136) P64 — R390 0R, R389 0R(DNF) — SDRAM-WEn, JA3-WEn

P63(Pin137) P63 — SDRAM-CASn, JA3-CAS

P62(Pin138) P62 — SDRAM-RASn, JA3-RAS

P61(Pin139) P61 — R393 0R, R394 0R(DNF) — SDRAM-SDCSn, JA3-CSb

P73(Pin93) P73 — R223 0R — LED0

T32 place near to R223
TST_Y_TFTEXTCLK(DNF)

P70(Pin128) P70 — R352 0R, R346 0R(DNF) — SDRAM-SDCLK, JA3-SDCLK

P87(Pin47) P87 — R201 0R(DNF), R102 0R(DNF), R91 0R(DNF), R491 0R — PDC-PIXD2, JA2-M1VN, JA2-TIMIN1, SDHI-D2

P86(Pin49) P86 — R204 0R(DNF), R186 0R(DNF), R481 0R — PDC-PIXD1, PMOD2-IO3, SDHI-PE

P85(Pin61) P85 — R128 0R, R100 0R(DNF) — TFT-B2, JA1-IO4

P84(Pin62) P84 — R139 0R, R97 0R(DNF) — TFT-B3, JA1-IO5

P83(Pin74) P83 — R269 0R, R268 0R(DNF) — ET-ET0CRS_RMII0CRSDV, TFT-G3

P82(Pin79) P82 — R321 0R, R320 0R(DNF) — ET-ET0ETXD1_RMII0TXD1, TFT-R2

P81(Pin80) P81 — R305 0R, R319 0R(DNF) — ET-ET0ETXD0_RMII0TXD0, TFT-R3

P80(Pin81) P80 — R304 0R, R318 0R(DNF) — ET-ET0TXEN_RMII0TXDEN, TFT-R4

P97(Pin149) P97 — R360 0R, R101 0R(DNF), R41 0R(DNF) — OnTFT-DISP, JA1-IO3, JA5-LCDDISP

P93(Pin159) P93 — R427 0R(DNF), R89 0R — JA3-A19, JA2-M1POE

P92(Pin160) P92 — R428 0R(DNF), R385 0R — JA3-A18, OnTFT-SCL, TFT-SCL

P90(Pin163) P90 — R429 0R(DNF), R397 0R — JA3-A16, OnTFT-SDA, TFT-SDA

PB0(Pin104), PA7(Pin106), PA6(Pin107), PA5(Pin108)

Board_3V3 — U7 SN74CB3Q3257PW

PB0, PA7, PA6, PA5 → 1A, 2A, 3A, 4A; DSW-SEL0 → S; VCC = 16; OE = 15; GND = 8

1B1 — OnTFT-R3
1B2 — SDRAM-A8, JA3-A8
2B1 — OnTFT-R4
2B2 — SDRAM-A7, JA3-A7
3B1 — OnTFT-R5
3B2 — SDRAM-A6, JA3-A6
4B1 — OnTFT-R6
4B2 — SDRAM-A5, JA3-A5
OE — DSW-OE

For configuration details, refer to Bus Switch configuration table on page8.

For configuration details, refer to Bus Switchi configuration table on page8.

GROUND

R44 0R(DNF) — JA6-M1WIN

PA4(Pin109), PA3(Pin110), PA2(Pin112), PA1(Pin114)

Board_3V3 — U15 SN74CB3Q3257PW

PA4, PA3, PA2, PA1 → 1A, 2A, 3A, 4A; DSW-SEL0 → S; VCC = 16; OE = 15; GND = 8

1B1 — OnTFT-R7
1B2 — SDRAM-A4, JA3-A4
2B1 — OnTFT-G2
2B2 — SDRAM-A3, JA3-A3
3B1 — OnTFT-G3
3B2 — SDRAM-A2, JA3-A2
4B1 — OnTFT-G4
4B2 — SDRAM-A1, JA3-A1

For configuration details, refer to Bus Switch configuration table on page8.

GROUND

PA0(Pin118) PA0 — R427 0R(DNF), R343 0R, R395 0R(DNF), R96 0R(DNF) — JA3-A0, OnTFT-G5, JA2-M1VP, JA2-TIMOUT1

PB7(Pin94) PB7 — R260 0R(DNF), R258 0R, R255 0R(DNF), R257 0R(DNF) — JA3-A15, OnTFT-BACKLIGHT, TFT-BACKLIGHT, SDSI-D1

PB6(Pin95) PB6 — R253 0R, R254 0R(DNF) — SDRAM-A14, JA3-A14, SDSI-D0

PB5(Pin96), PB4(Pin97), PB2(Pin99), PB1(Pin100)

Board_3V3 — U9 SN74CB3Q3257PW

PB5, PB4, PB2, PB1 → 1A, 2A, 3A, 4A; DSW-SEL0 → S; VCC = 16; OE = 15; GND = 8

1B1 — OnTFT-CLK
1B2 — SDRAM-A13, JA3-A13
2B1 — OnTFT-VSYNC
2B2 — SDRAM-A12, JA3-A12
3B1 — OnTFT-HSYNC
3B2 — SDRAM-A10, JA3-A10
4B1 — OnTFT-DEN
4B2 — SDRAM-A9, JA3-A9
OE — DSW-OE

For configuration details, refer to Bus Switch configuration table on page8.

For configuration details, refer to Bus Switchi configuration table on page8.

GROUND

R75 0R(DNF) — SDSI-CLK
R325 0R(DNF) — SDSI-CMD
R61 0R(DNF) — SDSI-D2

PB3(Pin98) PB3 — R248 0R, R249 0R(DNF) — SDRAM-A11, JA3-A11, SDSI-D3

PC7(Pin76) PC7 — R409 0R; J12 (3PIN_PTH(DNF)) — ET-ET0COL, E1-UB, DSW-UB; R402 0R(DNF) — TFT-G4

PC6(Pin77) PC6 — R324 0R, R325 0R(DNF) — ET-ET0ETXD3, TFT-G5

PC5(Pin78) PC5 — R17 0R, R27 0R(DNF) — ET-ET0ETXD2, TFT-R1

PC4(Pin82) PC4 — R16 0R, R294 0R(DNF) — ET-ET0TXCLK, TFT-R5

PC3(Pin83) PC3 — R98 0R, R50 0R(DNF) — JA2-M1WN, JA6-TXDc

PC2(Pin86) PC2 — R267 0R, R265 0R(DNF) — ET-ET0RXDV, JA6-RXDc

PC1(Pin89) PC1 — R288 0R, R287 0R(DNF) — ET-ET0ERXD2, JA6-SCKc

PC0(Pin91) PC0 — R315 0R, R316 0R(DNF) — ET-ET0ERXD3, JA1-IRQd

Board_3V3 — C34 100nF, C91 100nF, C28 100nF — GROUND

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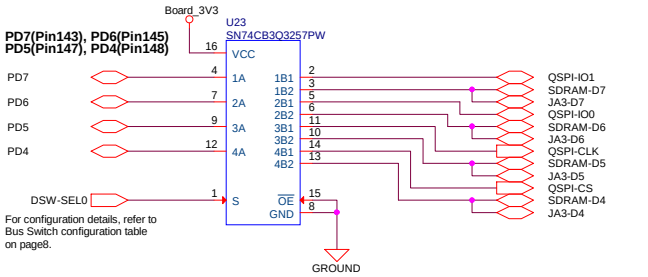
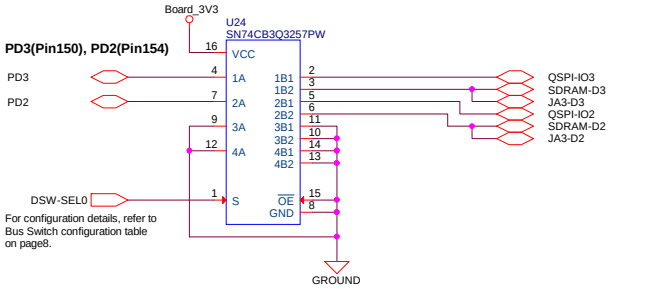
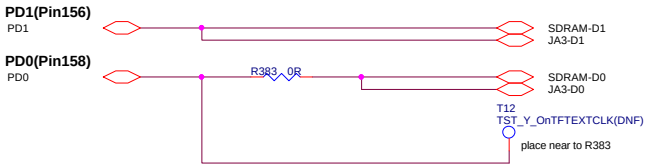
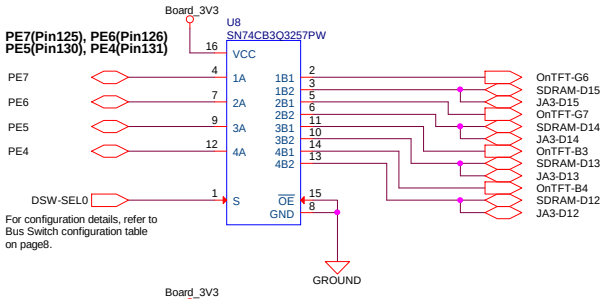
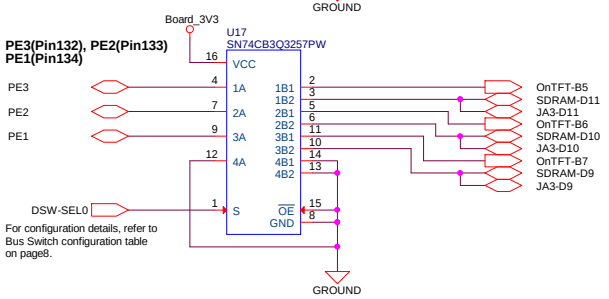
MCU Pin Function Select-3

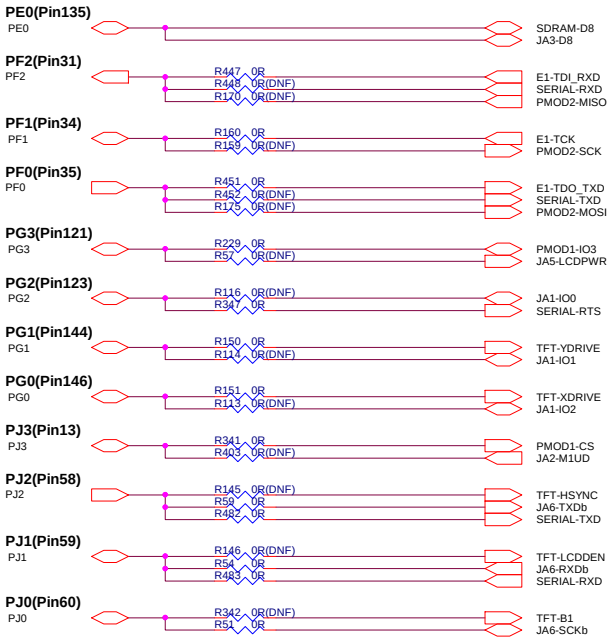




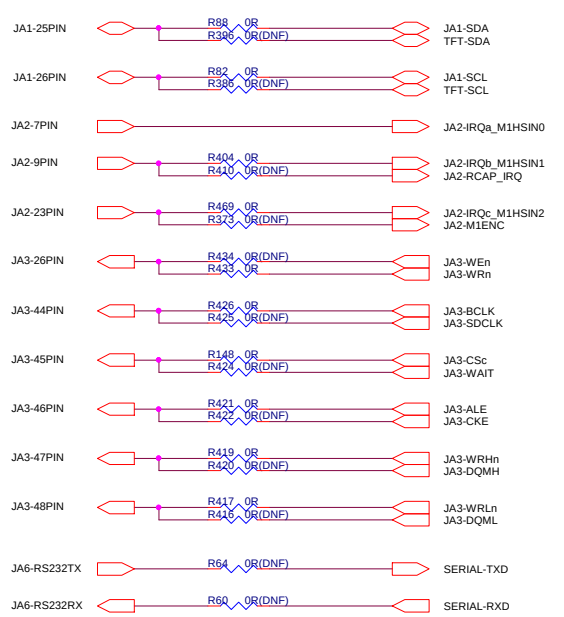


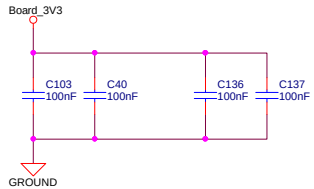






Application Header Function Select





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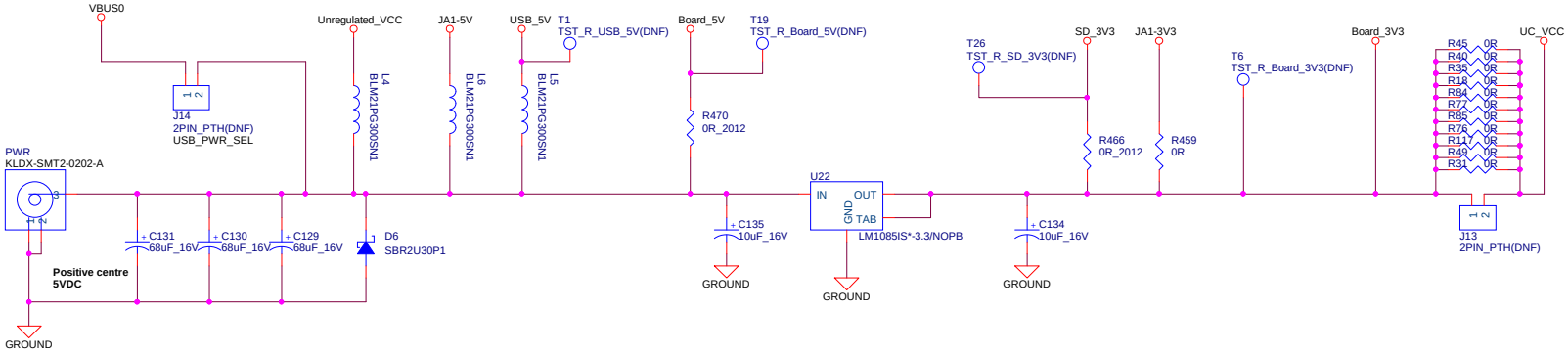
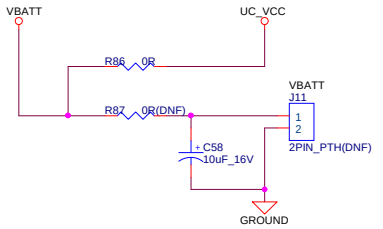
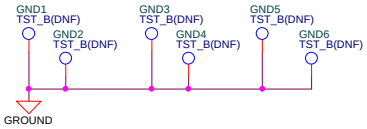
Power Supply Unit



VBATT Supply



Ground Test Point



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Title: RSK+RX65N-2MB [PSU]		
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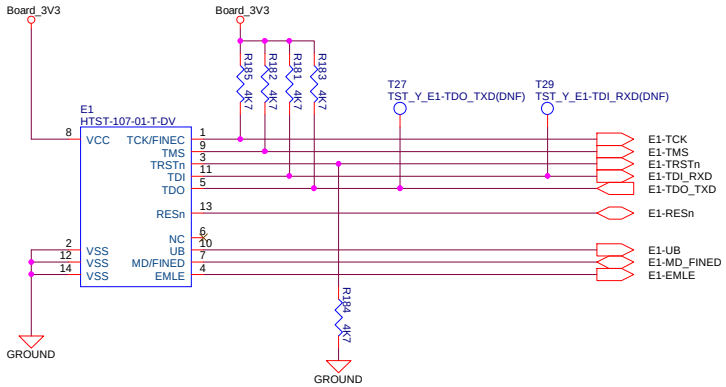
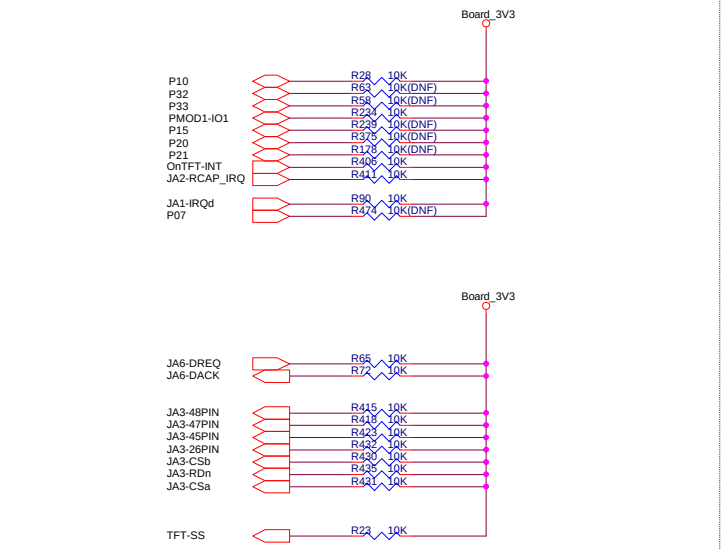
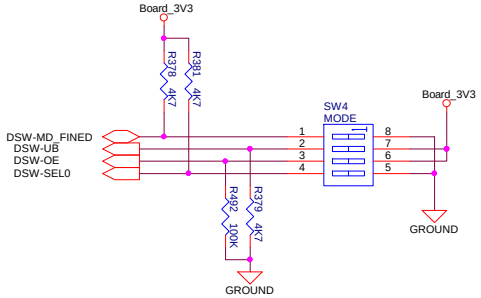
E1/E2 Lite Emulator Interface



Option pull-up resistor



MCU & Emulator Mode and Bus Switch Setting



MCU Operating Mode Configuration

SW4 Pin1	SW4 Pin2	J9	Operating Mode
OFF	Don't care	Don't care	Single Chip Mode
ON	OFF	Don't care	SCI Boot Mode
ON	ON	Open	USB Boot Mode (Bus Powered)
ON	ON	Shorted Pin	USB Boot Mode (Self Powered)

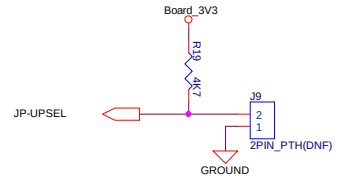
Default setting of SW4.

SW4	Default
Pin1	OFF
Pin2	OFF
Pin3	OFF
Pin4	ON

Bus Switch Select Configuration

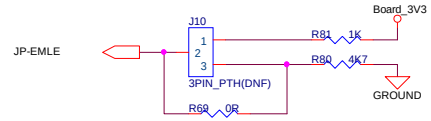
SW4 Pin3	SW4 Pin4	Available Feature	Unavailable Feature
OFF	OFF	SDRAM, JA3	On Board TFT, QSPI, SDSI, App header(JA6-M1WIN)
OFF	ON	On Board TFT, QSPI	SDRAM, JA3, SDSI, App header(JA6-M1WIN)
ON	OFF	DO NOT SET	DO NOT SET
ON	ON	QSPI, SDSI*, App header(JA6-M1WIN)*	On Board TFT, SDRAM, JA3

* In addition to this setting, it is necessary to change option link resistor in order to enable SDSI and JA6-M1WIN.
For configuration details, refer to option links on page5.



Power Configuration for USB Boot Mode

J9	Power Configuration
Open	Bus Powered
Shorted	Self Powered



Emulator Configuration

J10	Emulator Configuration
Shorted Pin1-2	E1/E2 Lite debugging with Hot plug-in
Shorted Pin2-3	E1/E2 Lite normal debugging Microcontroller single operation (without emulator)
All open	DO NOT SET

Renesas Electronics Corporation		
Title: RSK+RX65N-2MB [E1/E2 Lite, MCU & Emulator Mode Setting]		
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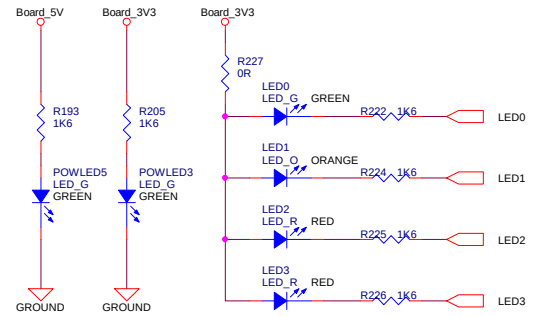
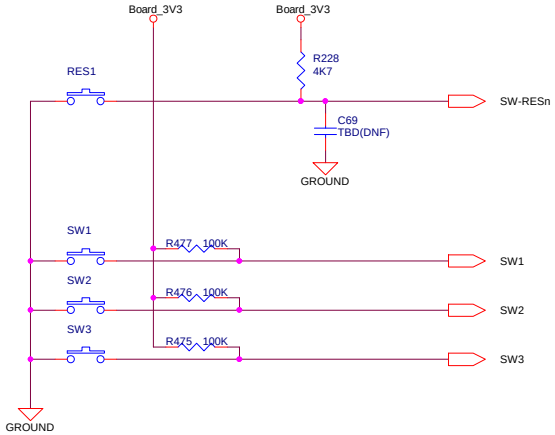
Switches, LEDs, RESET





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Title: RSK+RX65N-2MB [RESET, Switches, LEDs]		
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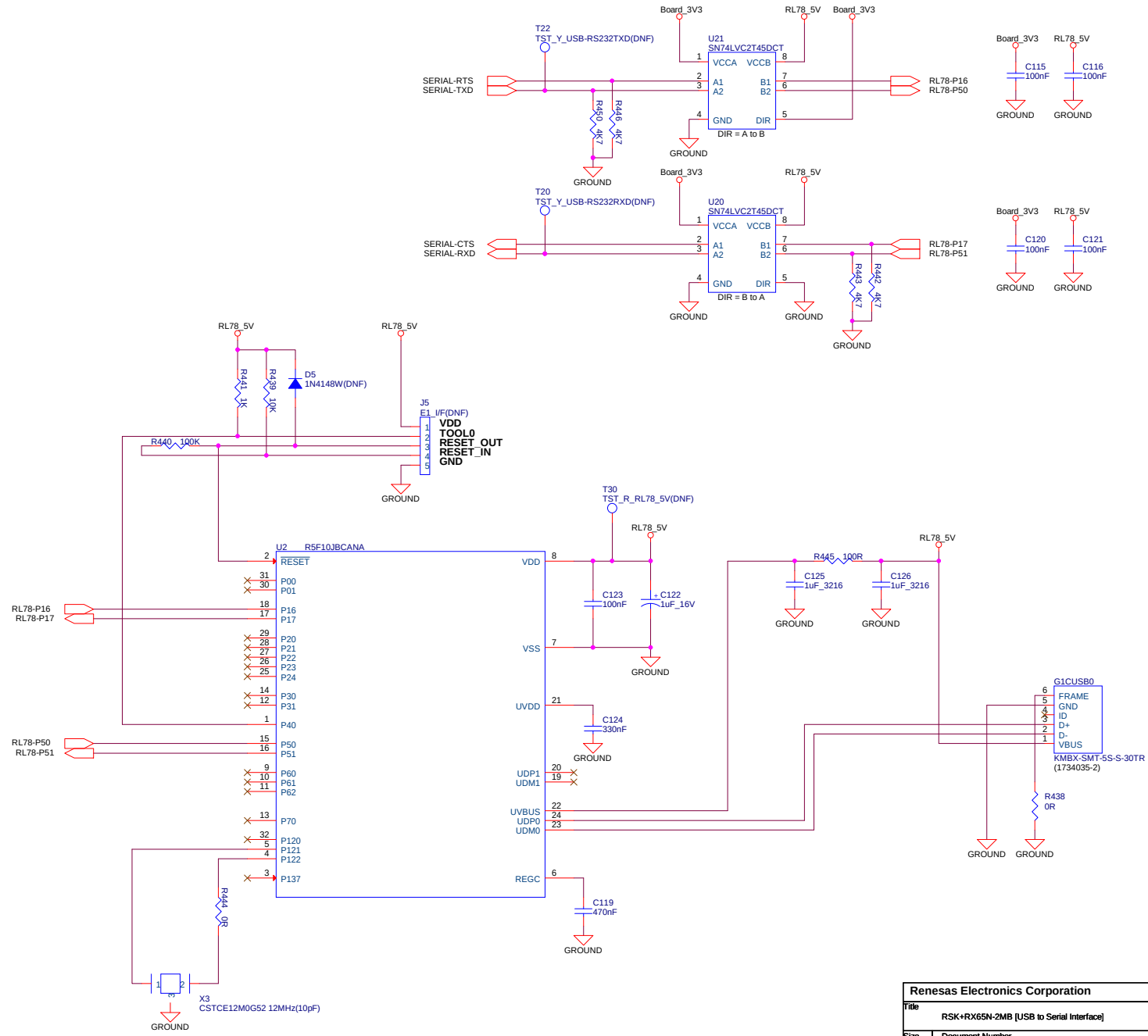
USB to Serial Interface



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Title: RSK+RX65N-2MB [USB to Serial Interface]		
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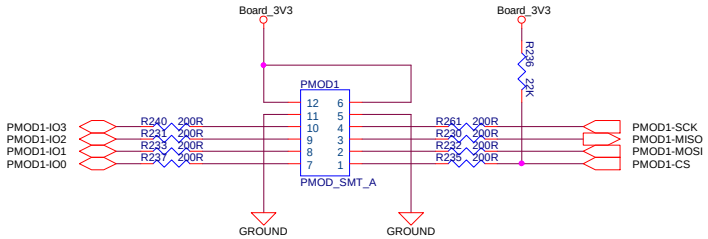
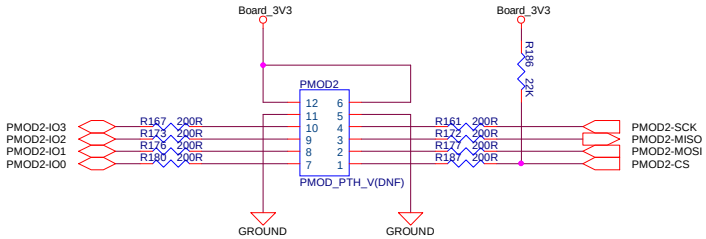
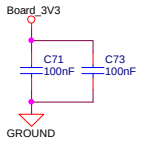
Pmod connectors

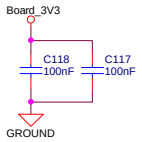
PMOD1: Angle type connector

PMOD2: Vertical type connector (spare)





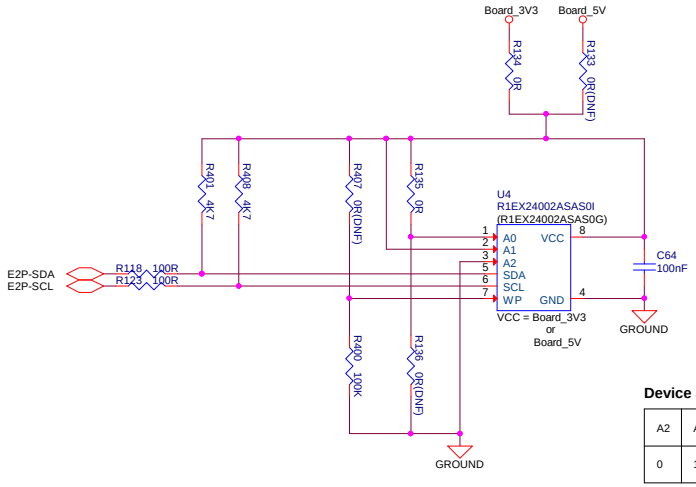




RIIC- Serial EEPROM(2Kbits)

Warning:

NEVER FIT R133 and R134 simultaneously.



Device address

A2	A1	A0
0	1	1

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Title: RSK+RX65N-2MB [Pmod, IIC EEPROM]		
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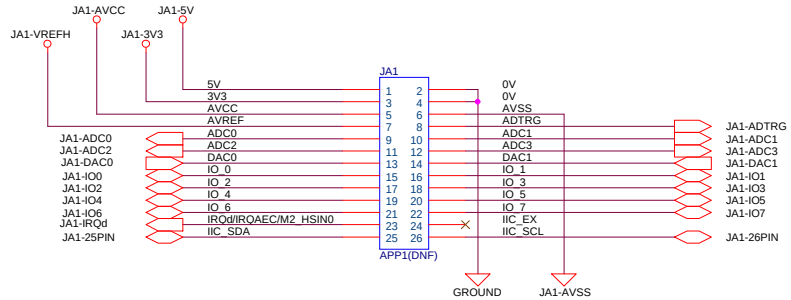
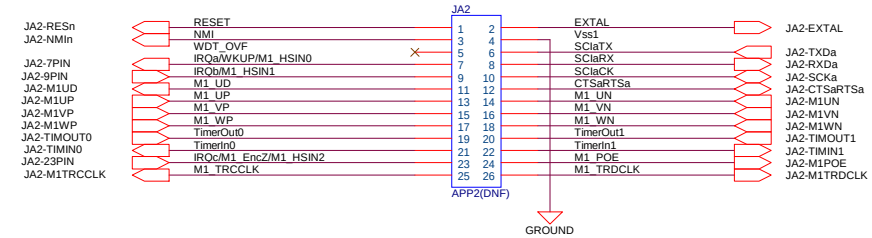
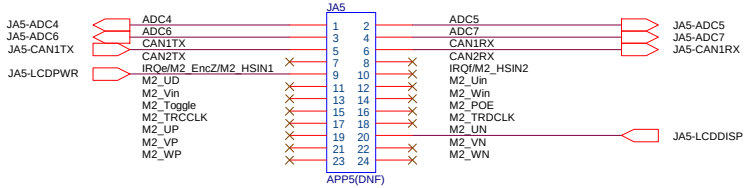
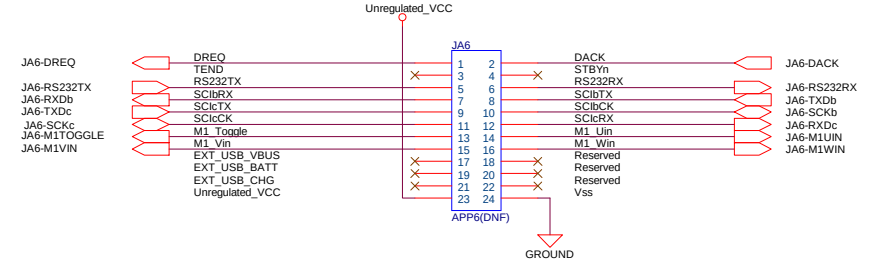
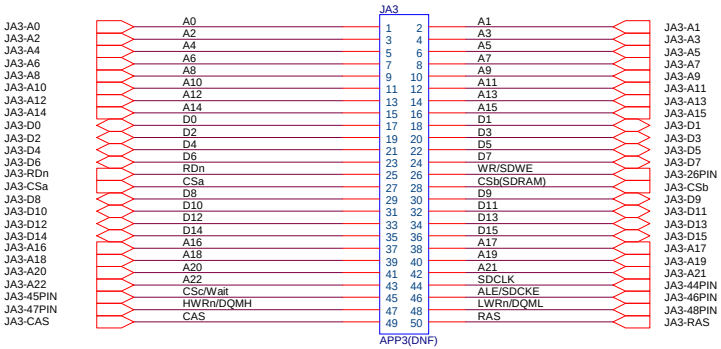
Application Headers











Note:

JA5-LCDPWR, JA5-LCDDISP, JA2-RCAP_IRQ(via JA2-9PIN) are not standard RSK App Header Specification.
These signals are special function for YGUI-ADDON TFT Board contained in the RX71M Display it! product.

YGUI-ADDON TFT Board requires the signals on TFT header, and the following signals.

App Header	YGUI-ADDON TFT Board
JA1.Pin11	IRQ/GPIO for user SW1
JA1.Pin12	IRQ/GPIO for user SW2 (Not Applicable)
JA1.Pin25	IIC for capacitive touch control
JA1.Pin26	IIC for capacitive touch control
JA2.Pin9	IRQ for capacitive touch control
JA2.Pin21	IRQ/GPIO for user SW3
JA5.Pin9	GPIO for TFT power enable
JA5.Pin20	GPIO for TFT Display enable

Note:

When connecting the HMI Expansion Board (R0K50564MB001BR), Test points TP1 and TP2 on the expansion board and Ethernet connector on the RSK board interfere physically.
Please remove the test points TP1 and TP2, when you connect the expansion board.

Renesas Electronics Corporation		
Title: **RSK+RX65N-2MB [Application Headers]**		
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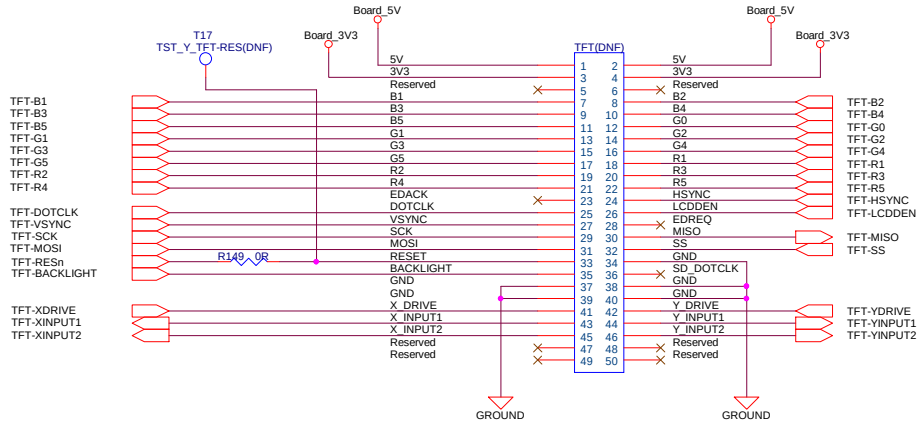
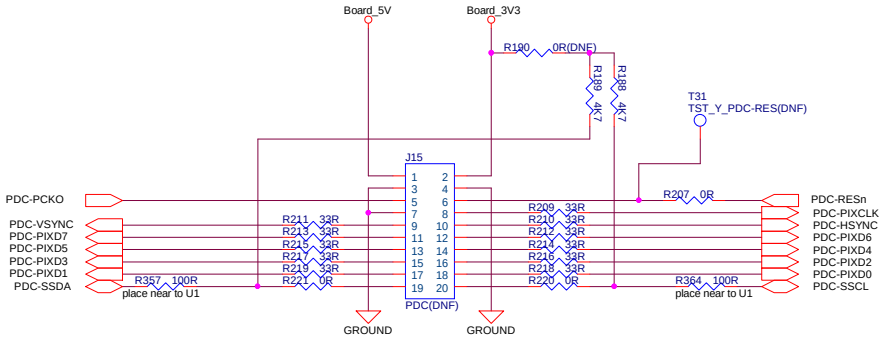
TFT Header for Graphic LCD Controller (TFT)



PDC

Warning:

When the voltage of your PDC target system differs from this board,
please do not supply a board power to your system directly.
When the voltage of your PDC target system differs from this board, please do not fit resistor R190.
Please fix pull-up resistor on your PDC target system.



Renesas Electronics Corporation		
Title: **RSK+RX65N-2MB [PDC Header, TFT Header]**		
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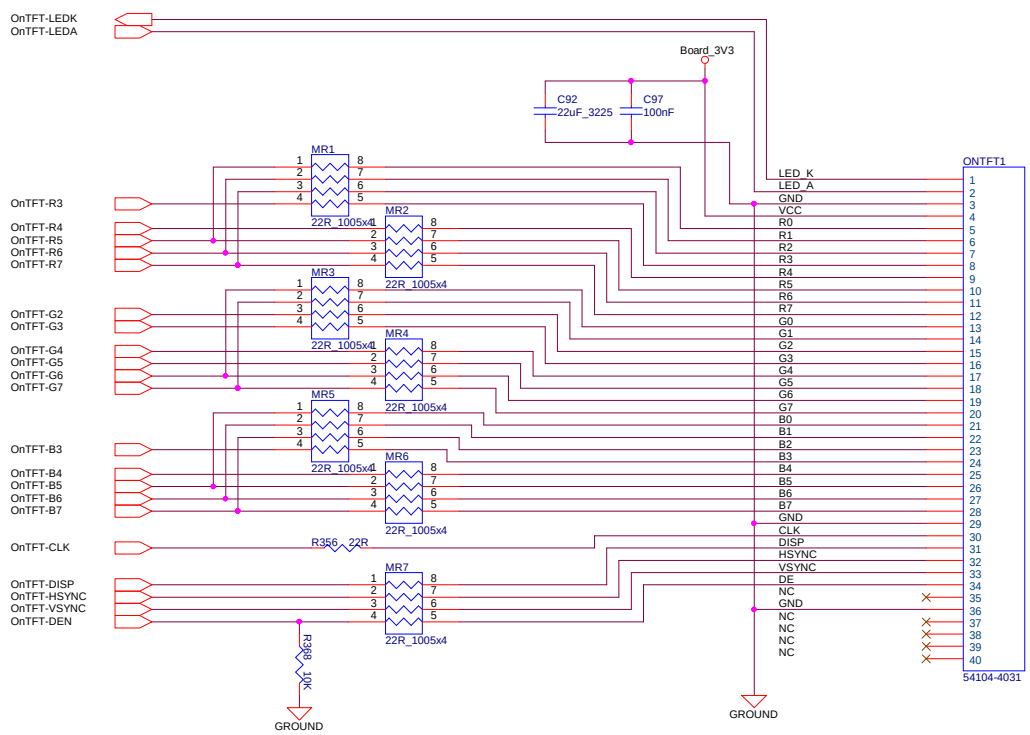
On-board TFT

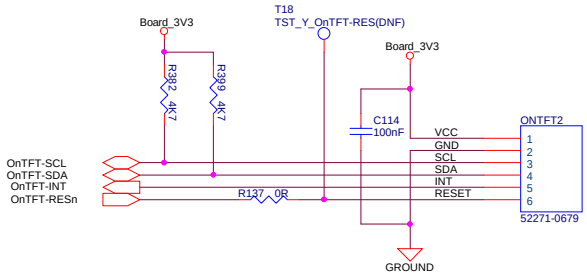
Note:

On-board TFT circuit is the design based on NHD-4.3-480272EF-ATXL#-CTP (4.3' 480x272 with Capacitive Touch).

Display Interface (Driver IC: HX8257-A)



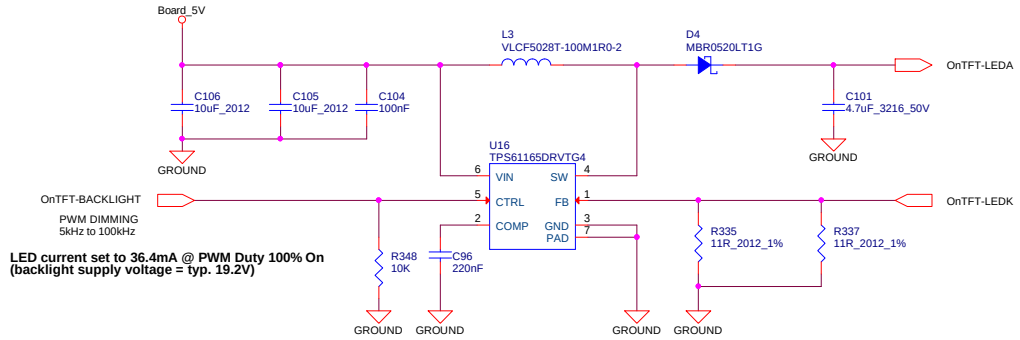
Capacitive Touch Interface (Driver IC: FT5306)



Device address for touch panel driver

A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0

LED Backlight



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Title: RSK+RX65N-2MB [On-board TFT]		
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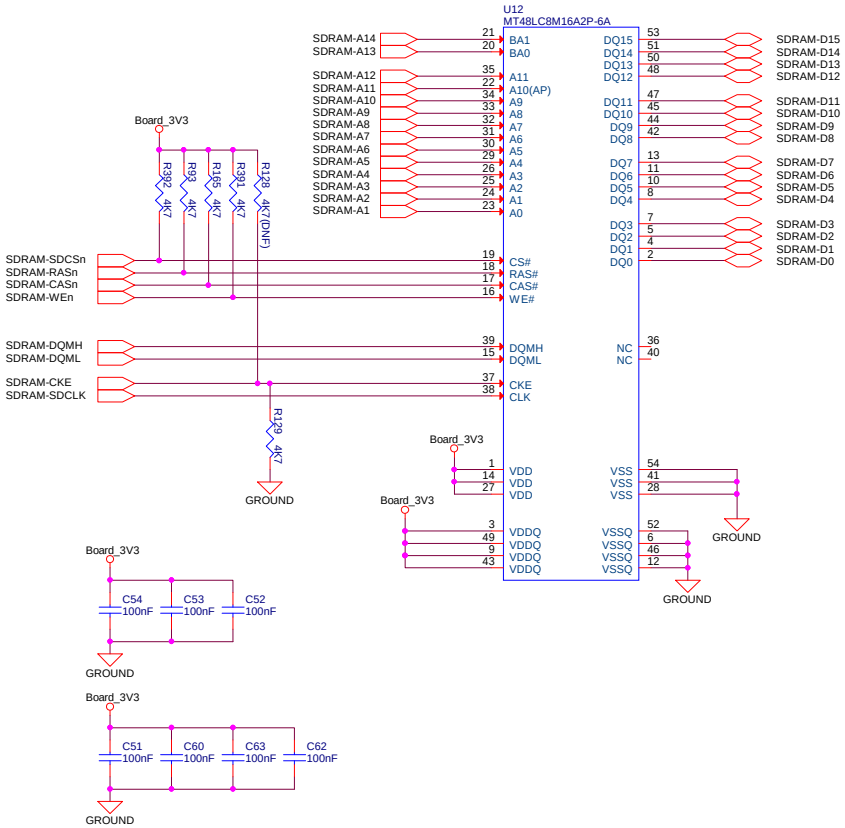
SDRAM(128Mbits)



Renesas Electronics Corporation		
Title: RSK+RX65N-2MB [On-board SDRAM]		
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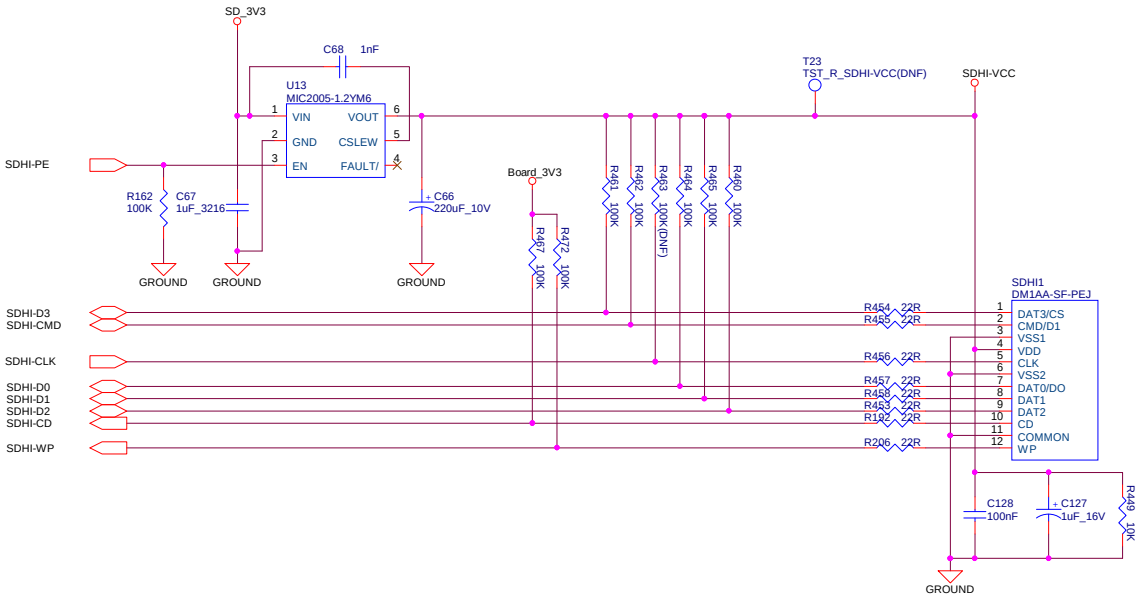
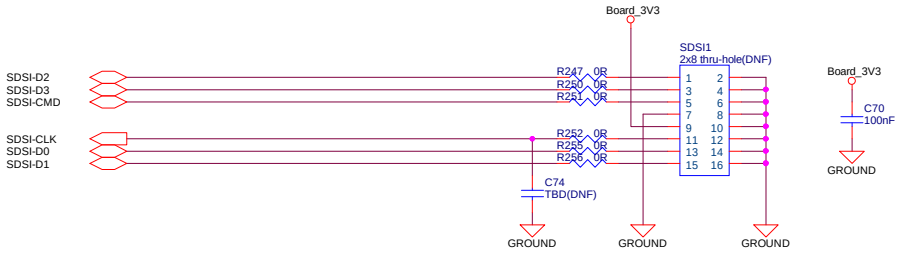
SDHI



SDSI



Renesas Electronics Corporation		
Title: RSK+RX65N-2MB [SDHI, SDSI]		
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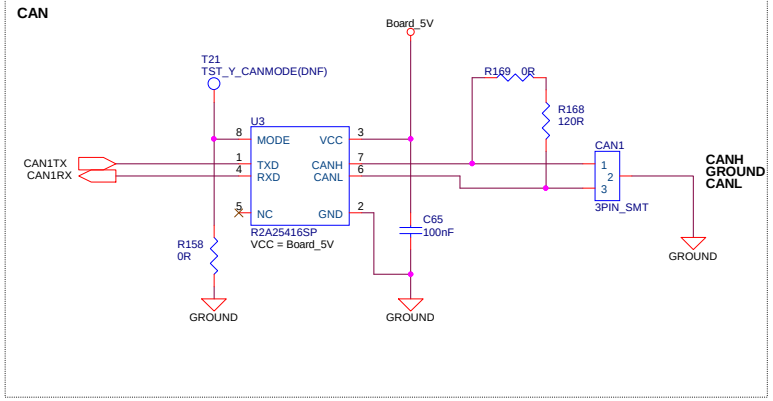
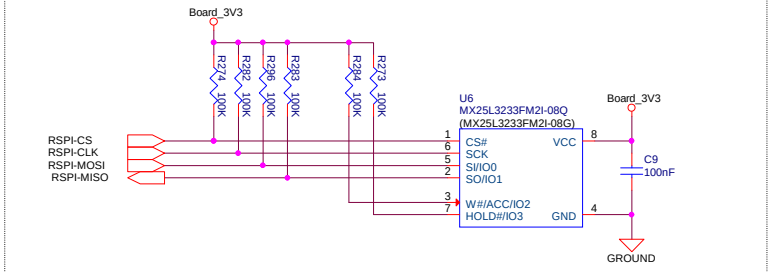
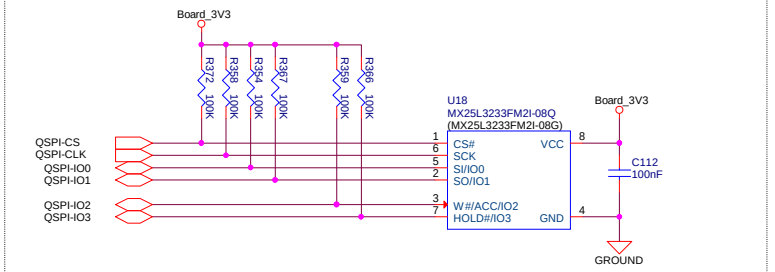
CAN



RSPI- SPI Serial Flash(32Mbits)



QSPI- SPI Serial Flash(32Mbits)



Renesas Electronics Corporation		
Title	**RSK+RX65N-2MB [CAN, RSPI, QSPI]**	
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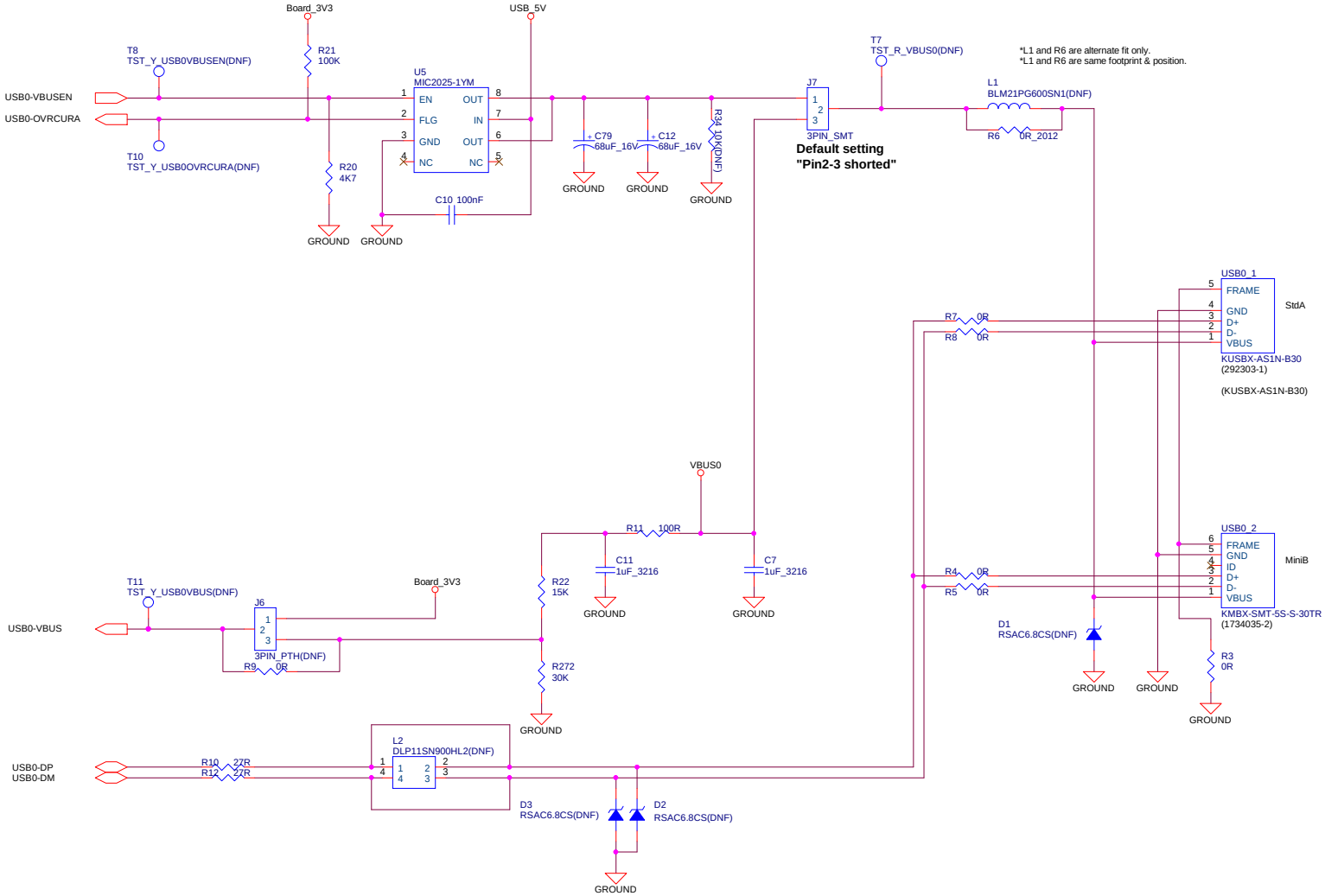
USB0 Host/Function

USB0 Host/Function Select

J7	
1-2 shorted	Host Mode
2-3 shorted	Function Mode

Self-powered/Bus-powered Configuration for Function Mode

J6	R9	
1-2 shorted	Remove	Bus-powered
2-3 shorted	Remove	Self-powered
Open	Fit	Self-powered



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Title: RSK+RX65N-2MB [USB0]		
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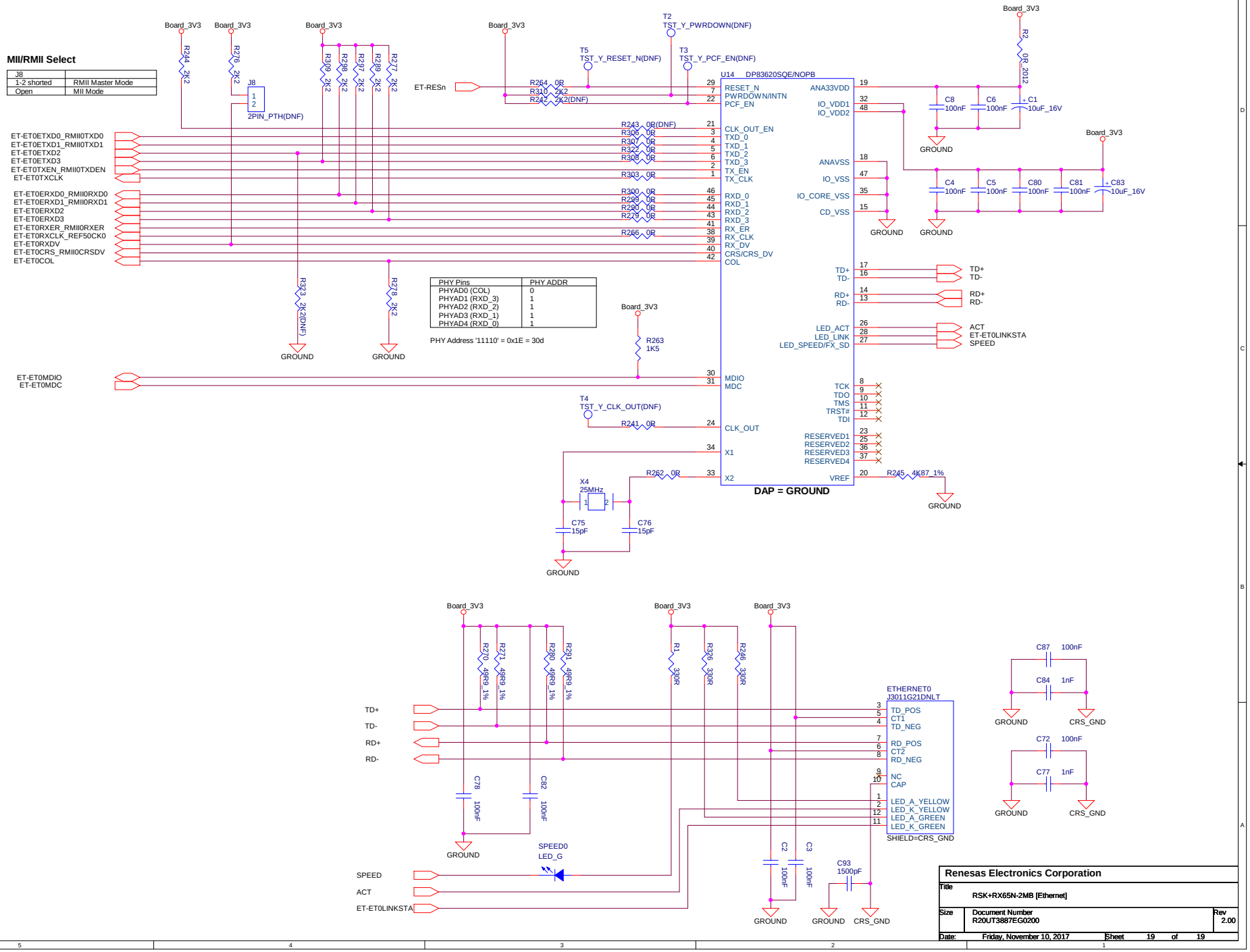
Ethernet


MII/RMII Select
J8
1-2 shorted RMII Master Mode
Open MII Mode
2PIN_PTH(DNF)
U14 DP83620SQE/NOPB
RESET_N
PWRDOWN/INTN
PCF_EN
CLK_OUT_EN
TXD_0
TXD_1
TXD_2
TXD_3
TX_EN
TX_CLK
RXD_0
RXD_1
RXD_2
RXD_3
RX_ER
RX_CLK
RX_DV
CRS/CRS_DV
COL
MDIO
MDC
CLK_OUT
X1
X2
ANA33VDD
IO_VDD1
IO_VDD2
ANAVSS
IO_VSS
IO_CORE_VSS
CD_VSS
TD+
TD-
RD+
RD-
LED_ACT
LED_LINK
LED_SPEED/FX_SD
TCK
TDO
TMS
TRST#
TDI
RESERVED1
RESERVED2
RESERVED3
RESERVED4
VREF
DAP = GROUND
PHY Pins PHY ADDR
PHYAD0 (COL) 0
PHYAD1 (RXD_3) 1
PHYAD2 (RXD_2) 1
PHYAD3 (RXD_1) 1
PHYAD4 (RXD_0) 1
PHY Address '11110' = 0x1E = 30d
ET-RESn
ET-ET0ETXD0_RMII0TXD0
ET-ET0ETXD1_RMII0TXD1
ET-ET0ETXD2
ET-ET0ETXD3
ET-ET0TXEN_RMII0TXDEN
ET-ET0TXCLK
ET-ET0ERXD0_RMII0RXD0
ET-ET0ERXD1_RMII0RXD1
ET-ET0ERXD2
ET-ET0ERXD3
ET-ET0RXER_RMII0RXER
ET-ET0RXCLK_REF50CK0
ET-ET0RXDV
ET-ET0CRS_RMII0CRSDV
ET-ET0COL
ET-ET0MDIO
ET-ET0MDC
ACT
ET-ET0LINKSTA
SPEED
X4 25MHz
GROUND
CRS_GND
Board_3V3
T2 TST_Y_PWRDOWN(DNF)
T3 TST_Y_PCF_EN(DNF)
T4 TST_Y_CLK_OUT(DNF)
T5 TST_Y_RESET_N(DNF)
ETHERNET0
J3011G21DNLT
TD_POS
CT1
TD_NEG
RD_POS
CT2
RD_NEG
NC
CAP
LED_A_YELLOW
LED_K_YELLOW
LED_A_GREEN
LED_K_GREEN
SHIELD=CRS_GND
SPEED0
LED_G
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RSK+RX65N-2MB [Ethernet]
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Revision History

REV	DATE	PAGE	DESCRIPTION
1.00	11.05.2017	---	1st release edition.
2.00	10.11.2017	---	Changes company name.
		8	Changes DIP switch (SW4) setting. (SW4.4=OFF -> SW4.4=ON)

Renesas Electronics Corporation		
Title: RSK+RX65N-2MB [Revision History]		
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