ISL81805EVAL1Z

The ISL81805EVAL1Z dual-phase evaluation board (shown in Figure 4) features the ISL81805, an 80V high voltage dual synchronous boost controller that offers external soft-start, independent enable functions, and integrates UV/OV/OC/OT protection. A programmable switching frequency ranging from 100kHz to 1MHz helps to optimize inductor size while the strong gate driver delivers up to 5A for the boost output.

Specifications

The ISL81805EVAL1Z dual-phase evaluation board is designed for high output voltage applications. The current rating of the ISL81805EVAL1Z is limited by the FETs and inductor selected. The ISL81805EVAL1Z electrical ratings are shown in Table 1.

Table 1. ISL81805EVAL1Z Electrical Ratings

Parameter	Rating
Input Voltage	9V to 36V
Switching Frequency	200kHz
Output Voltage	48V
Output Current	5A
OCP Set Point (input average)	Minimum 17.6A at ambient room temperature

Features

- Wide input range: 9V to 36V
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/PWM operation
- Optional CC/HICCUP OCP protection
- Supports pre-bias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection
- Back biased from external to improve efficiency
- Optional input/output average OCP

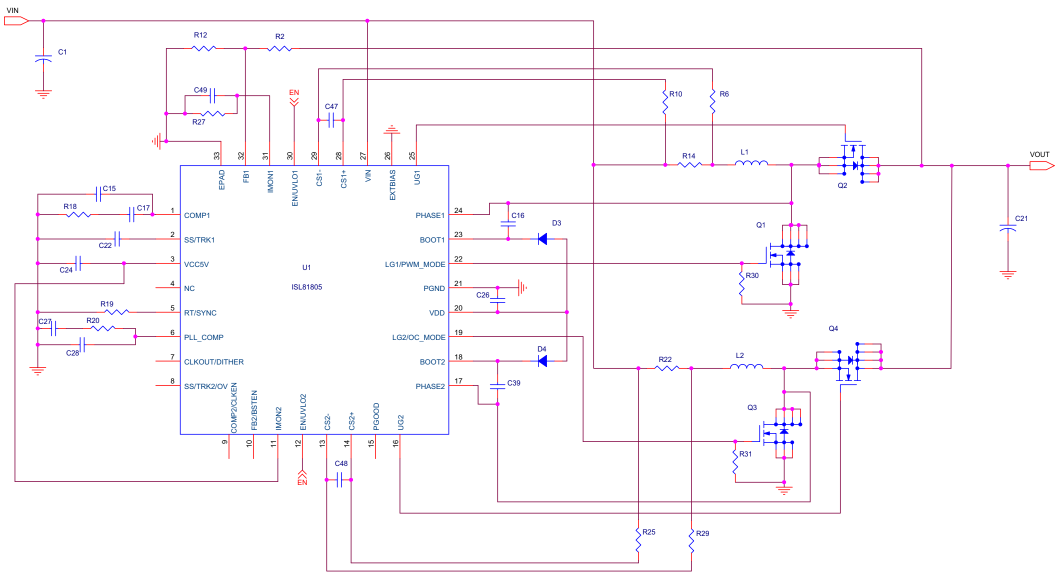

Figure 1. ISL81805EVAL1Z Block Diagram

Contents

1. Functional Description

The ISL81805EVAL1Z is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81805 TQFN IC. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in Figure 3, 9V to 36V V_{IN} is supplied to J1 (+) and J2 (-). The regulated 48V output on J4 (+) and J5 (-) can supply up to 5A to the load. Because of the high-power efficiency, the evaluation board can run at 5A continuously without airflow at ambient room temperature conditions.

Test points TP1 through TP24 provide easy access to the IC pin and external signal injection terminals.

As shown in Table 2, connector J6 provides a selection of either Forced PWM mode (shorting Pin 1 and Pin 2) or DEM mode (shorting Pin 2 and Pin 3). Connector J7 provides a selection of either constant current limit (shorting Pin 1 and Pin 2) or HICCUP OCP (shorting Pin 2 and Pin 3). Connector J3 provides an option to disable the converter by shorting its Pin 1 and Pin 2.

1.1 Recommended Testing Equipment

The following materials are recommended for testing:

- 0V to 40V power supply with at least 20A source current capability
- Electronic loads capable of sinking current up to 7A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

1.2 Operating Range

The input voltage range is from 9V to 36V for an output voltage of 48V. If the output voltage is set to a lower value, the minimum V_{IN} can be reset to a lower value by changing the ratio of R_1 and R_5. The minimum EN threshold that V_{IN} can be set to is 4.5V.

The rated load current is 5A with the input average OCP point set at a minimum 17.6A at ambient room temperature conditions. The operating temperature range of this board is -40°C to +85°C.

Note: Airflow is needed for higher temperature ambient conditions.

1.3 Quick Test Guide

1. Jumper J6 provides the option to select PWM or DEM. Jumper J7 provides the option to select a constant current limit or HICCUP. See Table 2 for the operating options. Ensure that the circuit is correctly connected to the supply and electronic loads before applying any power. See Figure 3 for the proper setup.
2. Turn on the power supply.
3. Adjust the input voltage (V_{IN}) within the specified range and observe the output voltage. The output voltage variation should be within 3%.
4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see Figure 2 for the proper test setup.

Note: Renesas recommends adding a minimum 0.1A load current if configured as DEM.

Table 2. Operating Options

Jumper	Position	Function
3	EN-GND	Disable output
	EN Floating	Enable output
6	Pin 1-2	PWM
	Pin 2-3	DEM
7	Pin 1-2	Constant current limit
	Pin 2-3	HICCUP

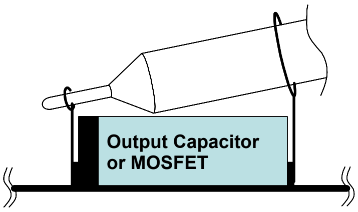

Figure 2. Proper Probe Setup to Measure Output Ripple and Phase Node Ringing

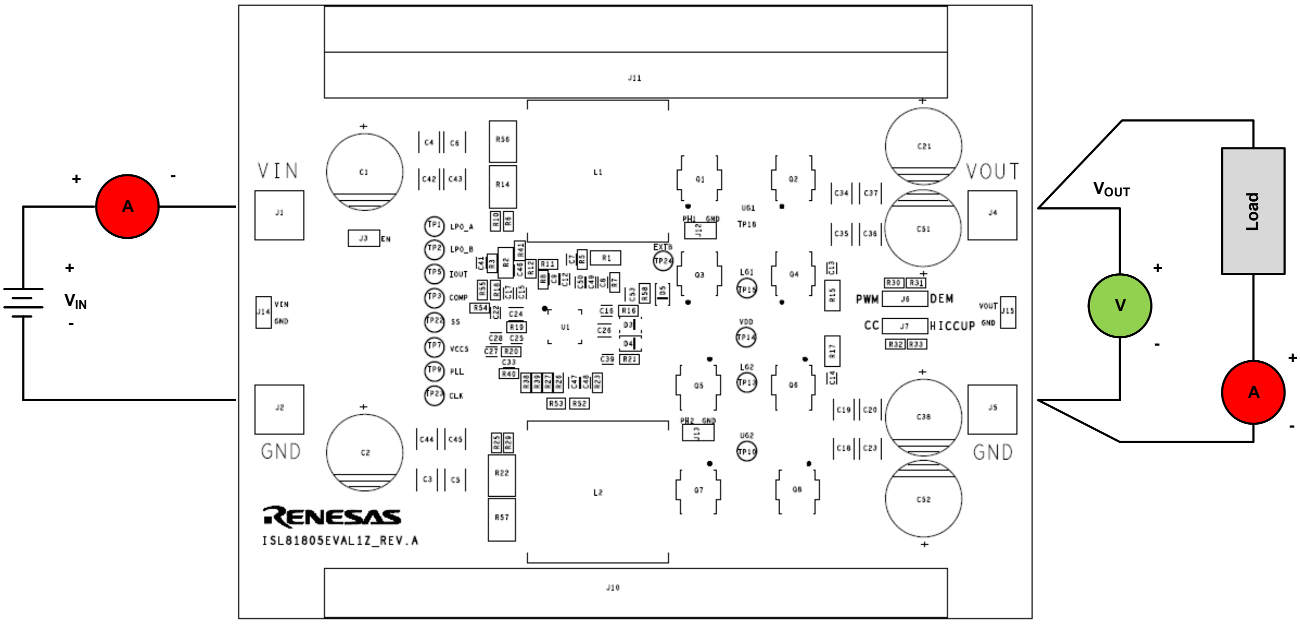

Figure 3. Proper Test Setup

2. Board Design

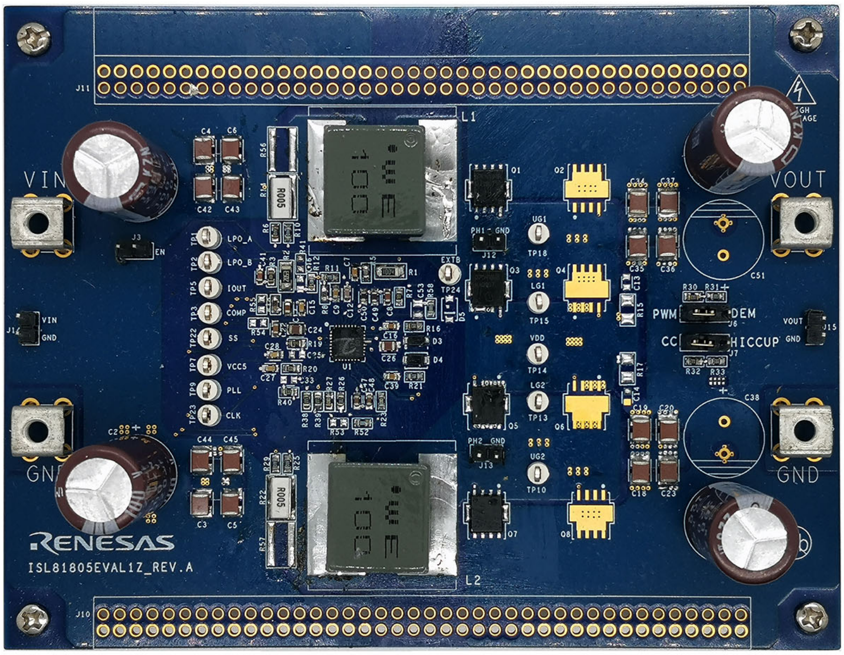

Figure 4. ISL81805EVAL1Z Evaluation Board, Top View

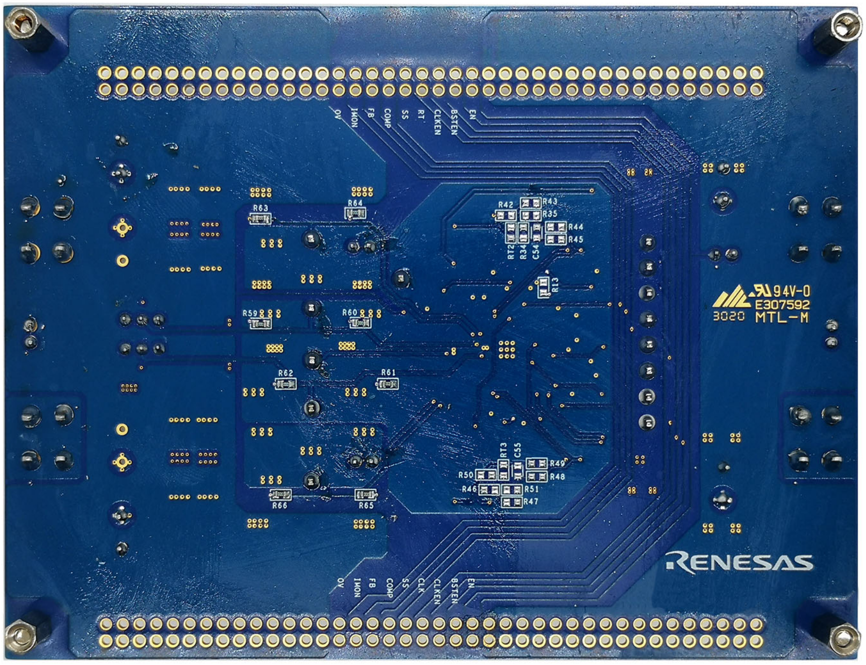

Figure 5. ISL81805EVAL1Z Evaluation Board, Bottom View

2.1 PCB Layout Guidelines

Careful attention to Printed Circuit Board (PCB) layout requirements is necessary for the successful implementation of an ISL81805 based DC/DC converter. The ISL81805 switches at a high frequency; therefore, the switching times are short. At these switching frequencies, even the shortest trace has significant impedance and the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes.

Three sets of components are critical when using the ISL81805 DC/DC converter:

- Controller
- Switching power components
- Small-signal components

The switching power components are the most critical to the layout because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small-signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

Complete the following steps to optimize the PCB layout.

- Place the input capacitors, inductor, boost FETs, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors close to the MOSFETs.
- If signal components and the IC are placed in a separate area to the power train, use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small-signal ground. Connect the SGND and PGND close to the IC. DO NOT connect them anywhere else.
- Keep the loop formed by the output capacitor, the boost top FET, and the boost bottom FET as small as possible.
- Keep the current paths from the input capacitor to the power inductor, the boost FETs, and the output capacitor as short as possible with maximum allowable trace widths.
- Place the PWM controller IC close to the lower FETs. The low-side FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane using a via. DO NOT directly connect the PGND pin to the SGND EPAD.
- Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
- Use copper filled polygons or wide short traces to connect the junction of the upper FET, lower FET, and output inductor. Also, keep the PHASE nodes connection to the IC short. DO NOT oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
- Route all high-speed switching nodes away from the control circuitry.
- Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
- Use a pair of traces with minimum loop for the input or output current sensing connection.
- Ensure the feedback connection to the output capacitor is short and direct.

2.2 Schematic Drawing

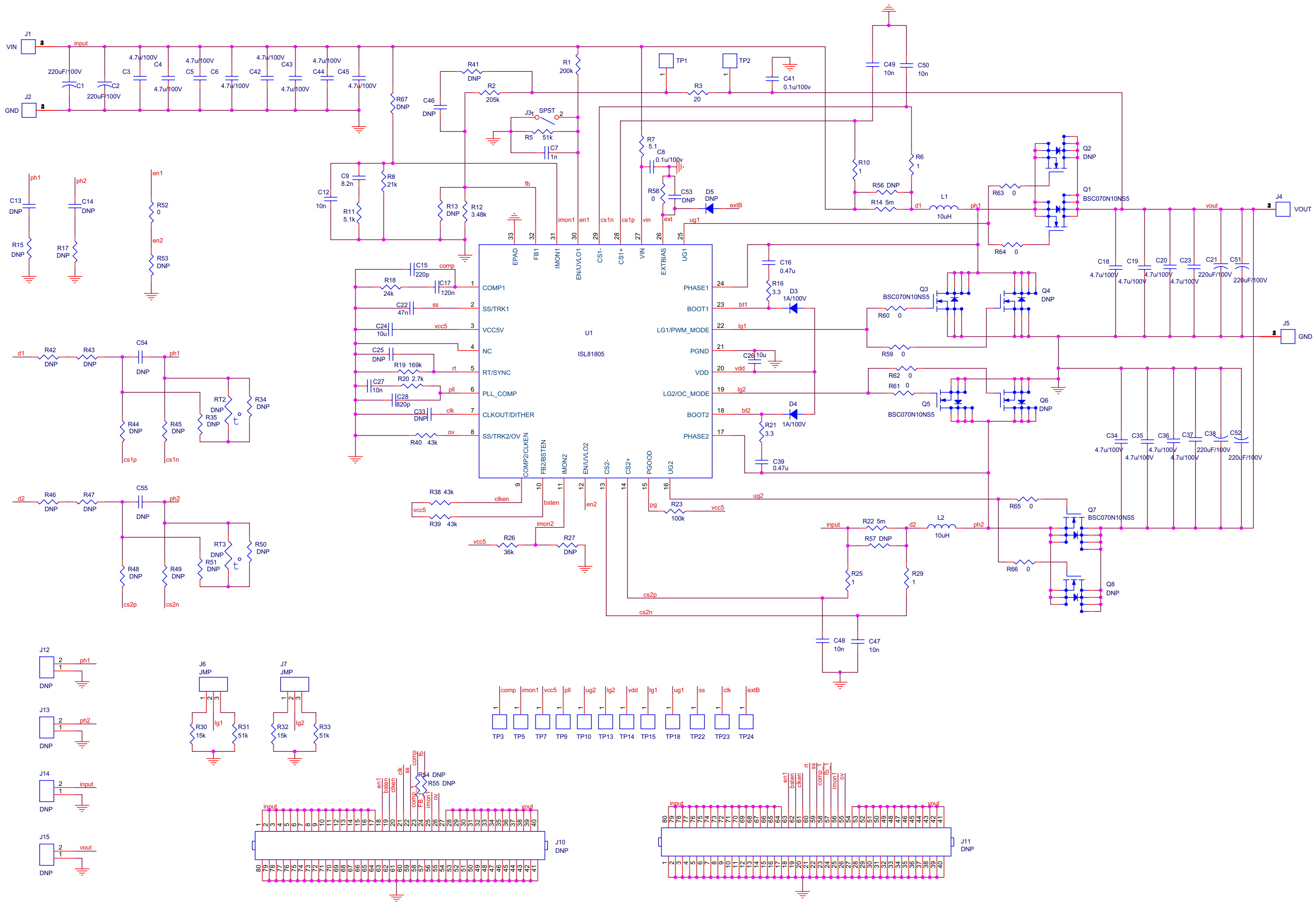

Figure 6. Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL81805EVAL1Z, REVA, ROHS	Multilayer PCB Technology	ISL81805EVAL1ZREVAPCB
6	C1, C2, C21, C38, C51, C52	CAP, RADIAL, 12.5x26.5, 220µF, 100V, 20%, ALUM.ELEC., 5mm, ROHS	United Chemi-Con	EKZN101ELL221MK25S
16	C3, C4, C5, C6, C18, C19, C20, C23, C34, C35, C36, C37, C42, C43, C44, C45	CAP-AEC-Q200, SMD, 1210, 4.7µF, 100V, 10%, X7S, ROHS	TDK	CGA6M3X7S2A475K200AB
1	C7	CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS	TDK	C1608X7R1H102K080AE
1	C8	CAP, SMD, 0603, 0.1µF, 100V, 10%, X7R, ROHS	Vishay	GRJ188R72A104KE11D
1	C9	CAP, SMD, 0603, 2200pF, 100V, 5%, X7R, ROHS	Kemet	C0603C222J1RACTU
5	C27, C47, C48, C49, C50	CAP, SMD, 0603, 0.01µF, 100V, 5%, X7R, ROHS	Kemet	C0603C103J1RACTU
1	C12	CAP, SMD, 0603, 100PF, 50V, X7R, 10%, ROHS	Kemet	C0603C101K5RACTU
1	C15	CAP, SMD, 0603, 220pF, 50V, 10%, X7R, ROHS	Murata	GRM188R71H221KA01D
2	C16, C39	CAP, SMD, 0603, 0.47µF, 25V, 10%, X7R, ROHS	Murata	GRM188R71E474KA12D
1	C17	CAP, SMD, 0603, 0.12µF, 25V, 10%, X7R, ROHS	Murata	GRM188R71E124KA01D
8	C18, C19, C20, C23, C34, C35, C36, C37	CAP, SMD, 1210, 22µF, 25V, X7R, ROHS	Murata	GRM32ER71E226KE15L
2	C21, C38	CAP-OSCON, SMD, 10mm, 1000µF, 16V, 20%, 12mΩ, ROHS	Panasonic	16SVPF1000M
1	C22	CAP, SMD, 0603, 0.047µF 25V X7R, ROHS	Kemet	C0603C473K3RACTU
2	C24, C26	CAP, SMD, 0805, 10µF, 16V, 10%, X7S, ROHS	Murata	GRM21BC71C106KE11L
1	C28	CAP, SMD, 0603, 820pF, 50V, 10%, X7R, ROHS	Kemet	C0603C821K5RACTU
1	C41	CAP, SMD, 0603, 0.1µF, 100V, 10%, X7R, ROHS	Vishay	GRJ188R72A104KE11D
0	C53	CAP, SMD, 0805, DNP-PLACE HOLDER, ROHS		
0	C13, C14, C25, C33, C46, C54, C55	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
2	D3, D4	DIODE-RECTIFIER, SMD, 2P, S0D-123FL, 100V, 1A, ROHS	ON Semiconductor	MBR1H100SFT3G
4	J1, J2, J4, J5	HDWARE, TERMINAL, M4 METRIC SCREW, TH, 4P, SNAP-FIT, ROHS	Keystone	7795

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	J3	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	69190-202HLF
2	J6, J7	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
0	J10, J11, J12, J13, J14, J15	2.54mm Headers, DNP-PLACE HOLDER, ROHS		
2	L1, L2	COIL-PWR INDUCTOR, SMD, 10µH, 20%, 11.5A, 6.5mΩ, ROHS	Wurth	74439370100
1	U1	80V DUAL-BOOST PWM CONTROLLER, 32P TQFN 5x5, ROHS	Renesas Electronics America	ISL81805FRTZ
4	Q1, Q3, Q5, Q7	TRANSISTOR-MOS, N-CHANNEL, SMD, 8P, PPK SO-8, 100V, 80A, ROHS	Infineon	BSC070N10NS5ATMA1
0	Q2, Q4, Q6, Q8	DO NOT POPULATE OR PURCHASE		
1	R1	RES SMD 200kΩ 1% 1/4W 1206	Yageo	RC1206FR-07200KL
1	R2	RES SMD 205kΩ 1% 1/10W 0603	Yageo	RC1206FR-07205KL
1	R3	RES SMD 20Ω 1% 1/10W 0603	Yageo	RC0603FR-0720RL
3	R5, R31, R33	RES SMD 51kΩ 1% 1/10W 0603	Yageo	RC0603FR-0751KL
4	R6, R10, R25, R29	RES SMD 1Ω 1% 1/10W 0603	Panasonic	ERJ-3RQF1R0V
1	R7	RES SMD 5.1Ω 1% 1/10W 0603	Yageo	RC0603FR-075R1L
1	R8	RES SMD 21kΩ 1% 1/10W 0603	Yageo	RC0603FR-0721KL
1	R11	RES SMD 5.1kΩ 1% 1/10W 0603	Yageo	RC0603FR-075K1L
1	R12	RES SMD 3.48kΩ 1% 1/10W 0603	Yageo	RC0603FR-073K48L
2	R14, R22	RES SMD 0.005Ω 3W 2512 WIDE	Susumu	KRL6432E-M-R005-F-T1
2	R16, R21	RES SMD 3.3Ω 1% 1/10W 0603	Yageo	RC0603FR-073R3L
1	R18	RES SMD 24kΩ 1% 1/10W 0603	Yageo	RC0603FR-0724KL
1	R19	RES SMD 169kΩ 1% 1/10W 0603	Venkel	CR0603-10W-1693FT
1	R20	RES SMD 2.7kΩ 1% 1/10W 0603	Yageo	RC0603FR-072K7L
1	R23	RES SMD 100kΩ 1% 1/10W 0603	Yageo	RC0603FR-07100KL
1	R26	RES SMD 36kΩ 1% 1/10W 0603	Yageo	RC0603FR-0736KL
2	R30, R32	RES SMD 15kΩ 1% 1/10W 0603	Yageo	RC0603FR-0715KL
3	R38, R39, R40	RES SMD 43kΩ 1% 1/10W 0603	Yageo	RC0603FR-0743KL
10	R52, R58, R59, R60, R61, R62, R63, R64, R65, R66	RES SMD 0Ω 1% 1/10W 0603	Yageo	RC0603FR-070RL

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
0	RT2, RT3, R13, R27, R34, R35, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R53, R54, R55, R67	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
0	R15, R17	RES, SMD, 1206, DNP-PLACE HOLDER, ROHS		
0	R56, R57	RES, SMD, 2512, DNP-PLACE HOLDER, ROHS		
14	TP1, TP2, TP3, TP5, TP7, TP9, TP10, TP13, TP14, TP15, TP18, TP22, TP23, TP24	CONN-COMPACT TEST PT, VERTICAL, WHT, ROHS	Keystone	5007
2	J6, J7	CONN-JUMPER,SHORTING,2PIN,BLACK,GOLD,ROHS	Sullins	SPC02SYAN
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Keystone	2204
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	7795

2.4 Board Layout

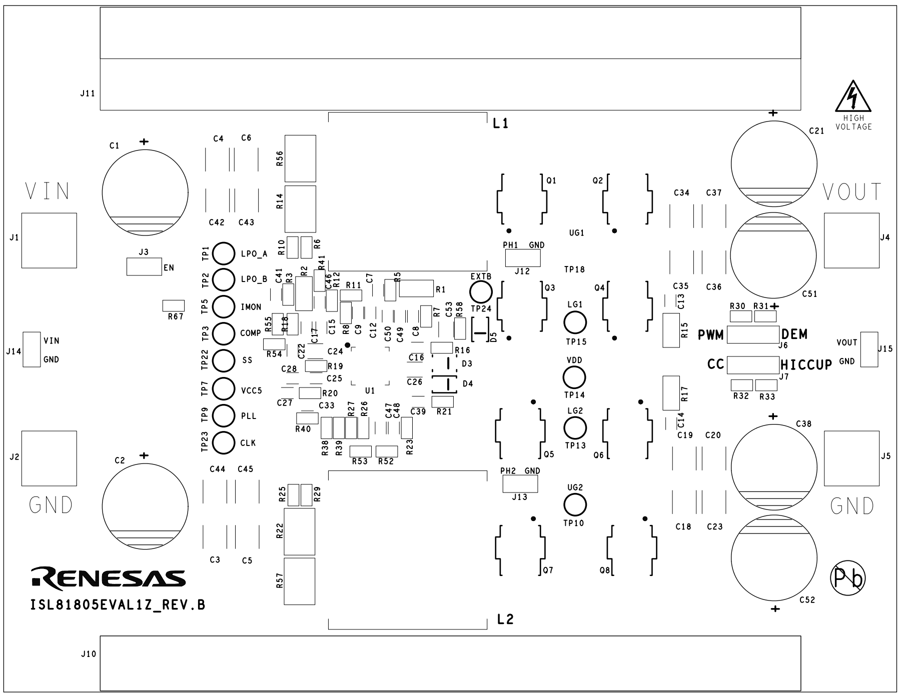

Figure 7. Silkscreen Top

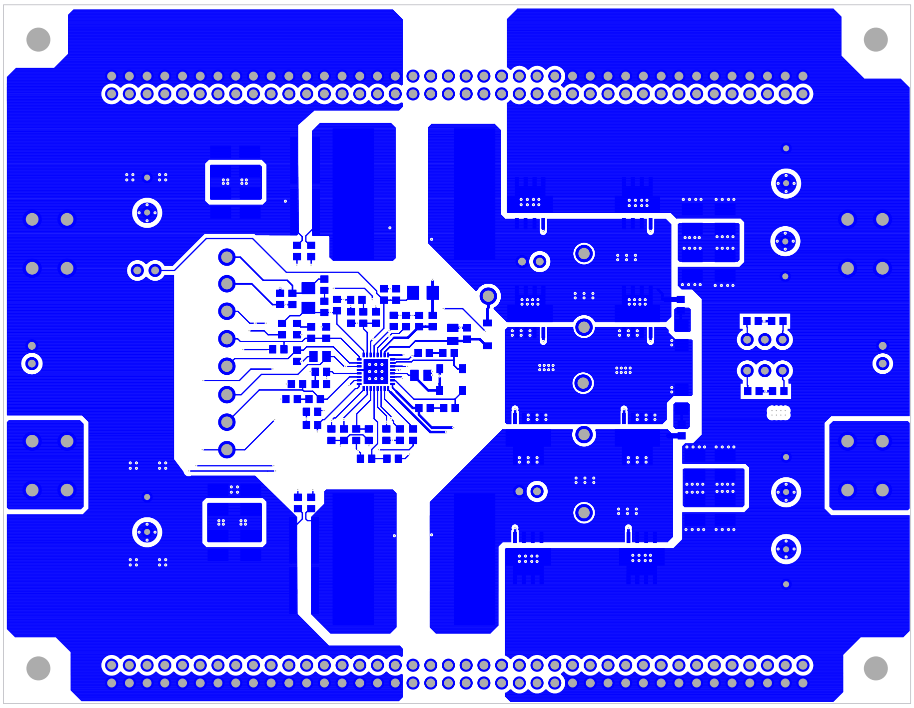

Figure 8. Top Layer

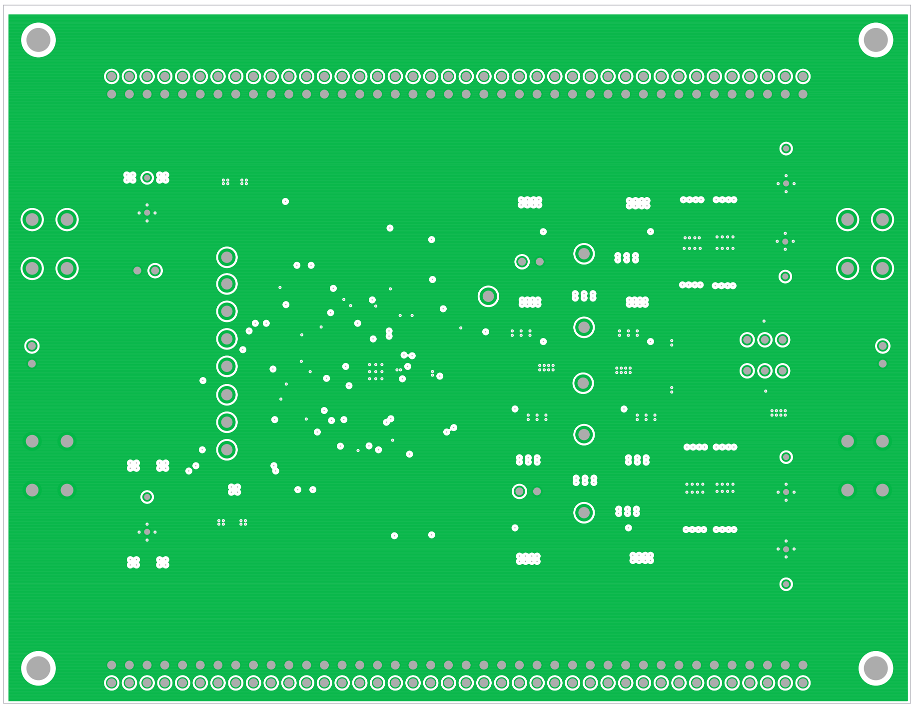

Figure 9. Second Layer (Solid Ground)

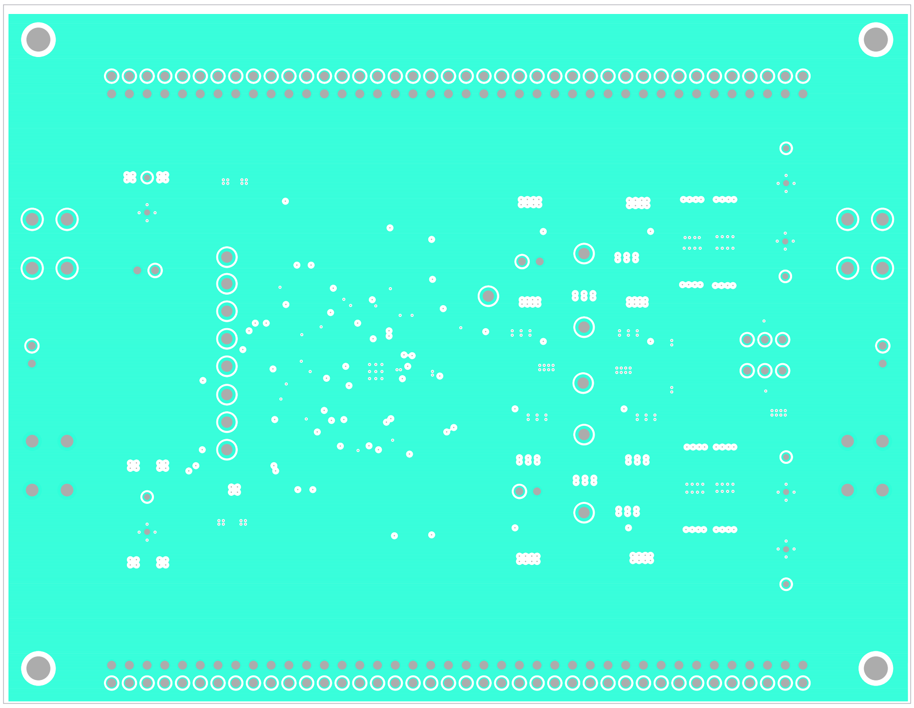

Figure 10. Third Layer

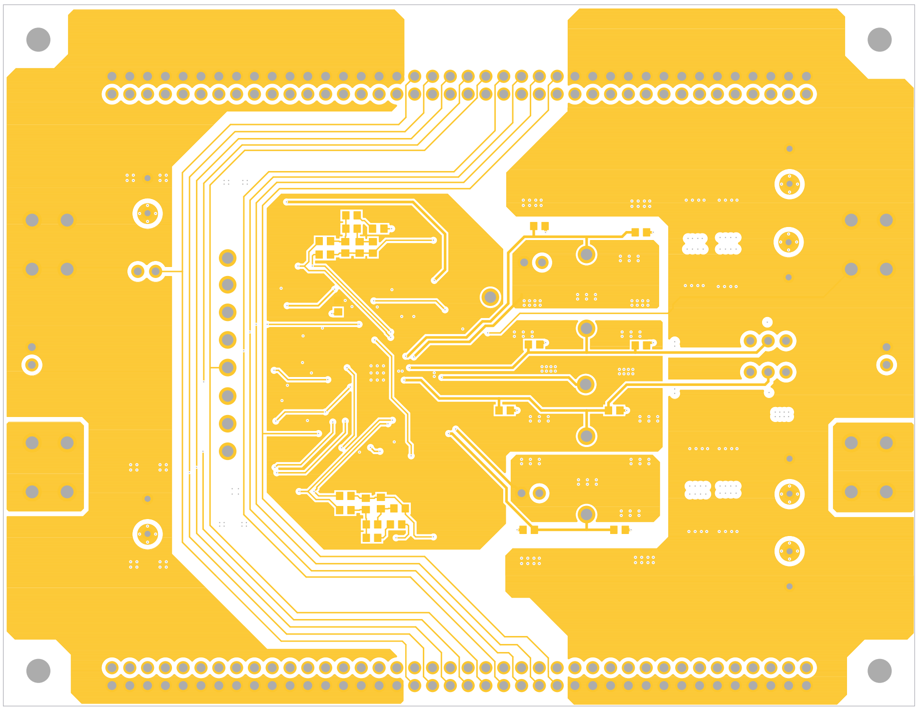

Figure 11. Bottom Layer

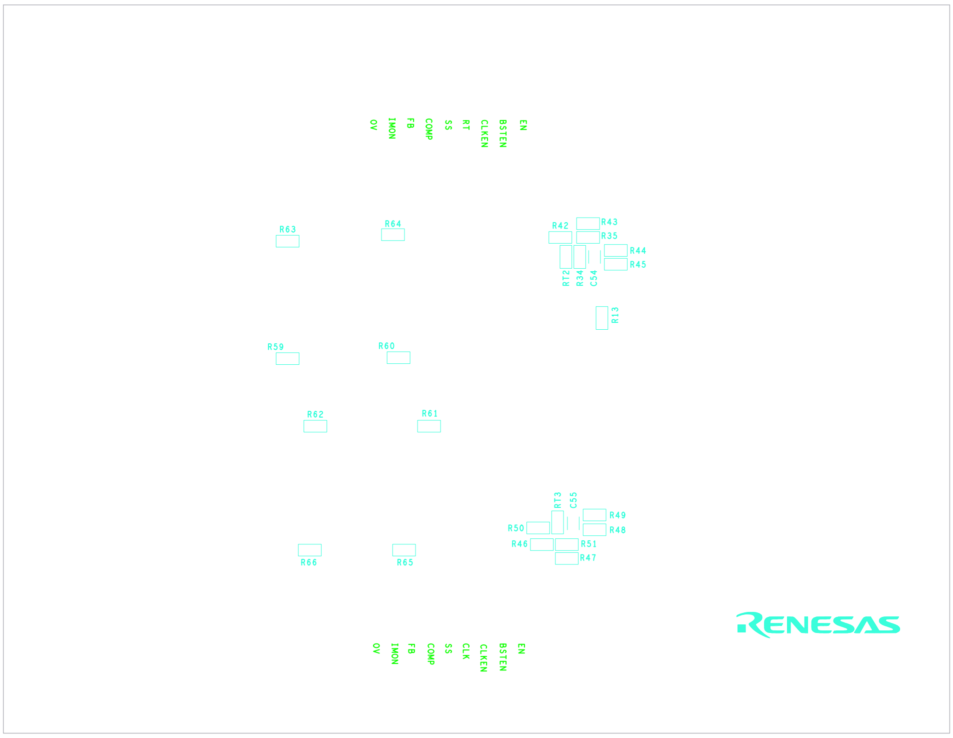

Figure 12. Silkscreen Bottom

2.5 Design Procedure

2.5.1 Design Requirements

Parameter	Rating
Input Voltage	9V to 36V
Switching Frequency	200kHz
Output Voltage	48V
Output Current	5A
OCP Set Point (input average)	17.6A
Output Mode	Dual phase
PWM Mode	Forced PWM
OCP Mode	Constant current

2.5.2 Frequency Setting

The default switching frequency of the PWM controller is determined by the resistor R_T (R19). It adjusts the default switching frequency from 100kHz to 1MHz. The R_T value for f_{SW} = 200kHz is calculated using Equation 1.

(EQ. 1) $$R_T = \left(\frac{34.7}{f_{SW}} - 4.78\right) = \frac{34.7}{0.2} - 4.78 = 168.72\text{k}\Omega$$

where f_{SW} is the switching frequency in MHz. Select a standard value resistor R_T = 169kΩ.

2.5.3 Output Voltage Setting

The output voltage can be set from 0.8V up to a level determined by the feedback voltage divider. A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB1 pin. With V_{OUT} = 48V and R_{FBO1} (R2) = 205k, the R_{FBO2} (R12) value is calculated using Equation 2.

(EQ. 2)
$$R_{FBO2} = \frac{0.8V \times R_{FBO1}}{V_{OUT} - 0.8V} = \frac{0.8V \times 205k\Omega}{48V - 0.8V} = 3.474k\Omega$$

where R_{FBO1} (R2) is the top resistor of the feedback divider network and R_{FBO2} (R12) is the bottom resistor connected from FB1 to ground. Select a standard value resistor R_{FBO2} = 3.48kΩ.

2.5.4 UVLO Setting

The ISL81805 has input UVLO protection. When the voltage on the EN/UVLO pin reaches 1.8V, the PWM modulator is enabled. Accurate UVLO feature can be implemented by feeding the V_{IN} into the EN/UVLO pin using a voltage divider, R_{UV1} (R1) and R_{UV2} (R5). The V_{IN} UVP rising threshold is calculated using Equation 3.

(EQ. 3)
$$V_{UVRISE} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - I_{LEAK}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(200k\Omega + 51k\Omega) - 2.8\mu A(200k\Omega)(51k\Omega)}{51k\Omega} = 8.3V$$

The V_{IN} UVP falling threshold is calculated using Equation 4.

(EQ. 4)
$$V_{UVFALL} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - I_{UVLO\_HYST}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(200k\Omega + 51k\Omega) - 6.8\mu A(200k\Omega)(51k\Omega)}{51k\Omega} = 7.5V$$

where V_{UVLO_THR} is the 1.8V UVLO rising threshold and I_{UVLO_HYST} is the 6.8µA UVLO hysteresis current.

2.5.5 Soft-Start Capacitor

The soft-start time for dual-phase is set by the value of the soft-start capacitor C_{SS} (C22) connected from SS/TRK1 to GND. The soft-start time with C_{SS} = 47nF is calculated using Equation 5.

(EQ. 5)
$$t_{SS} = 0.8V\left(\frac{C_{SS}}{4\mu A}\right) = 0.8V \times \left(\frac{47nF}{4\mu A}\right) = 9.4ms$$

When the soft-start time set by external C_{SS} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

2.5.6 MOSFET Considerations

The MOSFETs are selected based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power loss of the upper and lower MOSFETs for each phase is calculated using Equation 6 and Equation 7. The equations assume linear voltage current transitions and ignore the power loss caused by the reverse recovery of the body diode of the lower MOSFET.

(EQ. 6)
$$P_{LOWERMAX} = \left[\frac{(I_{OUT})^2(V_{OUT})^2}{(V_{INMIN}^{\ 2})}\right]\frac{(V_{OUT} - V_{INMIN})(r_{DS(ON)})}{V_{OUT}} + \frac{(I_{OUT})(V_{OUT})^2(t_{SW})(f_{SW})}{2(V_{INMIN})}$$
$$= \left[\frac{\left(\frac{3A}{2}\right)^2(48V)^2}{(12V)^2}\right]\frac{(48V - 12V)(6m\Omega)}{48V} + \frac{\left(\frac{3A}{2}\right)(48V)^2\left(\frac{6nC}{\left(\frac{8V - 4.9V}{1\Omega}\right)} + \frac{6nC}{\left(\frac{4.9V}{1\Omega}\right)}\right)(200kHz)}{2(12V)} = 0.162W + 0.09W = 0.252W$$

(EQ. 7)
$$P_{UPPERMAX} = \frac{(I_{OUT}^{2})(r_{DS(ON)})(V_{OUT})}{V_{INMIN}} = \frac{\left(\frac{3A}{2}\right)^{2}(6m\Omega)(48V)}{12V} = 0.054W$$

Ensure that all MOSFETs are within their maximum junction temperature with enough margin at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

2.5.7 Inductor Selection

The inductor value determines the ripple current of the converter. To limit the inductor core loss, the inductor ripple current is usually 40-80% of the rated output current. Assume the ripple current ratio is 80% of the inductor average current at the minimum input voltage and the full output load condition. The inductor value for each phase is calculated using Equation 8.

(EQ. 8)
$$L_{INMIN} = \frac{(V_{OUT} - V_{INMIN})(V_{INMIN})}{(f_{SW})(0.8 \times I_{INMAX})(V_{OUT})} = \frac{(48V - 12V)(12V)}{(200kHz)\left(0.8 \times \frac{48Vx3A}{12Vx2}\right)(48V)} = 9.375\mu H$$

The recommended inductor value is 10µH. Then the ripple current and peak current are calculated using Equation 9, Equation 10, and Equation 11.

(EQ. 9)
$$\Delta I_{LMAX} = \frac{(V_{OUT} - V_{IN})(V_{IN})}{(f_{SW})(L)(V_{OUT})} = \frac{(48V - 12V)(12V)}{(200kHz)(10\mu H)(48V)} = 4.5A$$

(EQ. 10)
$$I_{LRMS} = \sqrt{(I_{INMAX})^{2} + \frac{(\Delta I_{LMAX})^{2}}{12}} = \sqrt{\left(\frac{48Vx3A}{12Vx2}\right)^{2} + \frac{(4.5A)^{2}}{12}} = 6.14A$$

(EQ. 11)
$$I_{LPEAKMAX} = \frac{I_{INOCP}}{2} + \frac{\Delta I_{LMAX}}{2} = \frac{17.6A}{2} + \frac{4.5A}{2} = 11.05A$$

The saturation current of the inductor should be larger than 11.05A. The heat rating current of the inductor should be larger than 6.14A.

With inductor 74439370100 from Wurth Electronics, the maximum DC power dissipation in the inductor is approximately calculated using Equation 12.

(EQ. 12)
$$P_{LMAX} = (I_{LRMS})^{2}(DCR) = (6.14A)^{2} \times (6.4m\Omega) = 0.241W$$

2.5.8 Output Capacitor Selection

The minimum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 13.

(EQ. 13)
$$C_{OUTMIN} = \frac{L(V_{OUT})(I_{TRAN})^{2}}{2(V_{INMIN})^{2}(\Delta V_{OUT})} = \frac{10\mu H \times (48V) \times \left(\frac{3A}{2} - 0A\right)^{2}}{2(12V)^{2}\left(48V \times \frac{1}{100}\right)} = 7.8\mu F$$

where C_{OUTMIN} is the minimum output capacitor(s) required, I_{TRAN} is the transient load current step, and ΔV_{OUT} is the drop-in output voltage allowed during the load transient. Choose a capacitor no less than 7.8µF for each phase. 440µF electrolytic capacitor and 18.8µF MLCC in total are used for each phase on this board.

The output voltage ripple is because of the discontinuous ripple current to the output capacitor and the ESR of the output capacitors as defined by Equation 14.

(EQ. 14)
$$V_{RIPPLE} = \left(\frac{(I_{OUT})(V_{OUT})}{V_{INMIN}} + \frac{\Delta I_{L}}{2}\right) \times ESR = \left(\frac{\left(\frac{3A}{2}\right)(48V)}{12V} + \frac{4.5A}{2}\right) \times 5m\Omega = 41.25mV$$

2.5.9 Input Capacitor Selection

The important parameters for the input capacitors are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline.

In Boost mode, the input current is continuous. The RMS current supplied by the input capacitance is noticeably small.

Renesas recommends using a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Two 220µF electrolytic capacitors with 2.2A rating current and eight 4.7µF ceramic capacitors are used to share the input RMS current on this board.

2.5.10 First Level Peak Current Limit and Sense Resistor Selection

The inductor peak current is sensed by the sense resistor R_S (R14). When the voltage drop on R_S reaches the set point $V_{OCSET\text{-}CS}$ typical 82mV, it triggers the pulse-by-pulse peak current limit. With the current limit set point I_{OCPP1} = 2xI_{INMAX} = 16A for each phase, the value of the sense resistor is calculated using Equation 15.

(EQ. 15) $$R_S = \frac{V_{OCSET-CS}}{I_{OCPP1}} = \frac{82mV}{16A} = 5.125m\Omega$$

Select a standard value resistor R_S = 5mΩ. Then the actual peak current limit is calculated using Equation 16.

(EQ. 16) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_S} = \frac{82mV}{5m\Omega} = 16.4A$$

The maximum power dissipation in R_S is calculated by Equation 17.

(EQ. 17) $$P_{RSMAX} = (I_{IN})^2R_S = (6.14A)^2(5m\Omega) = 0.188W$$

Therefore, a sense resistor with 1W power rating is sufficient for this application.

2.5.11 Second Level Hiccup Peak Current Protection

In this condition, V_{IN} is so close to V_{OUT} that the inductor current runs away with the minimum on PWM duty. The ISL81805 integrates a second level hiccup type of peak current protection. The second level peak current protection set point I_{OCPP2} is calculated using Equation 18.

(EQ. 18) $$I_{OCPP2} = \frac{V_{OCSET\text{-}CS\text{-}HIC}}{R_S} = \frac{98mV}{5m\Omega} = 19.6A$$

2.5.12 Input Average Overcurrent Protection and R_{IM} Selection

The ISL81805 provides either constant current or hiccup type of overcurrent protection for input average current. The OCP mode is set by a resistor connected between the LG2/OC_MODE pin and ground. With input constant current/hiccup set point I_{INOCP} = 17.6A for two phases in total, the current monitoring resistor R_{IM} (R8) is calculated using Equation 19.

(EQ. 19) $$R_{IM} = \frac{1.2}{I_{INOCP} \times R_S \times Gm_{CS} + 2 \times I_{CSOFFSET}} = \frac{1.2V}{17.6A x 5m\Omega x 195\mu S + 2 \times 20\mu A} = 20.99k\Omega$$

where $I_{CSOFFSET}$ is the output current sense op amp internal offset current, typical 20µA. Select a standard value resistor R_{IM} = 21kΩ.

The board can also be configured to be output average overcurrent protection by injecting into the IMON pin an additional signal which changes with V_{IN}. This can be implemented by the resister R67, which is between the VIN terminal and the IMON1 pin.

2.5.13 Output Mode Selection

When the IMON2 pin voltage is higher than 3V, the IC is set for one output dual-phase application, and the original IMON2 current monitor function pin is disconnected from the IMON2 pin and internally connected to the IMON1 pin. The IMON2 pin is connected to VCC5 using R26 for dual-phase setting on this board.

2.5.14 PWM Mode Selection

You can set the ISL81805 to either forced PWM mode or DE mode. The mode is set by a resistor $R_{PWMMODE}$ (R30 or R31) connected between the LG1/PWM_MODE pin and GND. The boundary resistor value for $R_{PWMMODE}$ is calculated using Equation 20.

(EQ. 20) $$R_{PWMMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to forced PWM mode, while a resistor higher than 30kΩ sets the converter to DE mode. Considering the tolerance in all temperature ranges, Renesas recommends using 22kΩ to set Forced PWM mode and 39kΩ to set DE mode.

2.5.15 Overcurrent Protection Mode Selection

The ISL81805 is set to either a constant current or hiccup type of overcurrent protection for input average current by selecting a different value of the resistor R_{OCMODE} (R32 or R33) connected between LG2/OC_MODE and GND. The boundary resistor value for R_{OCMODE} is calculated using Equation 21.

(EQ. 21) $$R_{OCMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to constant current mode, while a resistor higher than 30kΩ sets the converter to Hiccup mode. Considering the tolerance in all temperature ranges, Renesas recommends using 22kΩ to set constant current and 39kΩ to set the Hiccup mode.

2.5.16 Phase Lock Loop (PLL)

The PLL of the ISL81805 ensures the wide range of accurate clock frequency and phase setting. It also makes the internal clock easily synchronized to an external clock with the frequency either lower or higher than the internal setting. The external compensation network of R_{PLL} (R20), C_{PLL1} (C27), and C_{PLL2} (C28) is needed to connect to the PLL_COMP pin to ensure PLL stable operation. Renesas recommends choosing 2.7kΩ for R_{PLL}, 10nF for C_{PLL1}, and 820pF for C_{PLL2}.

2.5.17 Feedback Loop Compensation

To adapt the different applications, the controller is designed with an externally compensation network. Figure 13 shows the peak current mode boost converter circuit.

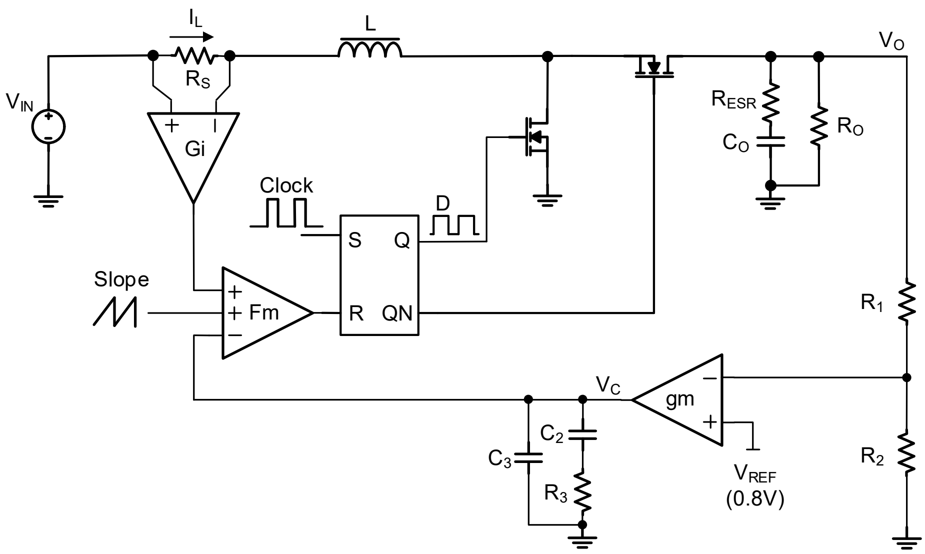

Figure 13. Peak Current Mode Boost Converter Circuit

In the current loop, the control to output simplified transfer function is shown in Equation 22.

(EQ. 22) $$\frac{\hat{V}_O}{\hat{V}_C} = \frac{R_O \times (1-D)}{R_I \times K_d} \times \frac{\left(1 - \frac{s}{\omega_{RHPZ}}\right)\left(1 + \frac{s}{\omega_{z(esr)}}\right)}{\left(1 + \frac{s}{\omega_{po}}\right)\left(1 + \frac{s}{\omega_{pi}}\right)}$$

where:

(EQ. 23) $$K_d = 2 + \frac{R_O \cdot (1-D)^2}{R_I} \cdot \left(\frac{1}{K_m} + \frac{K}{1-D}\right)$$

(EQ. 24) $$K_m = \frac{1}{(D-0.5)R_I \times \frac{T_s}{L} + \frac{V_{SL}}{V_O}}$$

(EQ. 25) $$K = 0.5R_I \times \frac{T_s}{L} \times D \times (1-D)$$

(EQ. 26) $$R_I = G_I \times R_S$$

- R_O is the load resistor
- C_O is the output capacitor
- L is the inductor
- R_S is the current sense resistor
- V_O is the output voltage
- T_S is the period of one switching cycle
- D is the duty cycle of lower MOSFET

- V_{SL} = 0.843V, is the slope compensation voltage
- V_{IN} is the input voltage of the boost
- V_C is the output of the error amplifier
- G_I = 5.472, is the gain of the current sensor

The low frequency pole frequency is shown in Equation 27.

(EQ. 27) $$\omega_{p0} = 2\pi f_{p0} = \frac{K_d}{C_o \times R_o}$$

The high frequency pole frequency is shown in Equation 28.

(EQ. 28) $$\omega_{pi} = 2\pi f_{pi} = \frac{K_m \times R_I}{L}$$

The output capacitor ESR (R_{ESR}) zero frequency is shown in Equation 29.

(EQ. 29) $$\omega_{z(esr)} = 2\pi f_{z(esr)} = \frac{1}{C_o \times R_{ESR}}$$

The output voltage is regulated by an error amplifier EA. The EA compensation network parameters can be determined by compensating the current loop poles and zero so as to implement an ideal -20dB/decade close-loop gain with crossover frequency around 1/50~1/20 of f_{sw} crossover frequency.

For boost topology, the maximum crossover frequency is also limited by the RHPZ. Estimate the RHPZ at the minimum input voltage by Equation 30.

(EQ. 30) $$\omega_{RHPZ} = 2\pi f_{RHPZ} = \frac{R}{L} \times (1 - D_{max})^2$$

If the crossover frequency $f_c << f_{pi}$, a type-2 compensation network is enough to achieve the goal.

(EQ. 31) $$\frac{\hat{V}_c}{\hat{V}_o} = -\frac{R_2}{R_1 + R_2} \cdot g_m \cdot \frac{1 + sR_3C_2}{s(C_2 + C_3) + s^2R_3C_2C_3} = -\frac{R_2}{R_1 + R_2} \cdot \frac{g_m}{C_2 + C_3} \cdot \frac{1 + sR_3C_2}{s\left(1 + \frac{sR_3C_2C_3}{C_2 + C_3}\right)}$$

To simplify the model, assuming $C_3 << C_2$, the type-2 EA amplifier transfer function is simplified to Equation 32.

(EQ. 32) $$\frac{\hat{V}_c}{\hat{V}_o} = -\frac{R_2}{R_1 + R_2} \cdot \frac{g_m}{C_2 + C_3} \cdot \frac{1 + sR_3C_2}{s(1 + sR_3C_3)}$$

Where g_m is the gain of error amplifier, typical 1.75mS.

The transfer function has one pole and one zero.

- The pole is at the frequency of $f_{p1} = 1/2\pi R_3C_3$. This is the frequency where the impedance of R_3 is equal to C_3.
- The zero is at the frequency of $f_{z1} = 1/2\pi R_3C_2$. This is the frequency where the impedance of R_3 is equal to C_2.

To achieve ideal compensation, Renesas recommends making $f_{z1} = f_{p0}$ and $f_{p1} = f_{z(esr)}$ as shown in Figure 14.

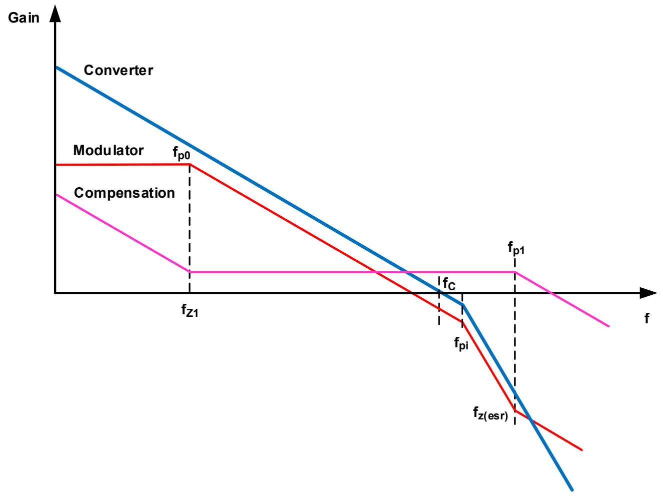

Figure 14. Feedback Loop Compensation

The close-loop transfer function is then simplified to Equation 33.

(EQ. 33) $$G_{loop}(s) = \frac{R_O \times (1-D)}{R_I \times K_d} \times \frac{\left(1 - \frac{s}{\omega_{RHPZ}}\right)\left(1 + \frac{s}{\omega_{z(esr)}}\right)}{\left(1 + \frac{s}{\omega_{p0}}\right)\left(1 + \frac{s}{\omega_{pi}}\right)} \times \left(-\frac{R_2}{R_1 + R_2} \cdot \frac{g_m}{C_2 + C_3}\right) \cdot \frac{1 + sR_3C_2}{s(1 + sR_3C_3)}$$

The Loop design example for the 48V output under 20V input voltage is shown in the following:

V_{IN} = 20V, V_{OUT} = 48V, I_{OUT} = 5A, f_{sw} = 200kHz, T_s = 5µs, D = 1-V_{IN} / V_{OUT} = 0.588, L = 10µH, C_O = 458.8µF (220µFx2+4.7µFx4), R_O = V_{OUT} /I_{OUT} = 9.6Ω, R_s = 5mΩ, R_{esr} = 5mΩ.

(EQ. 34) $$K_m = \frac{1}{(D-0.5)R_I \times \frac{T_s}{L} + \frac{V_{SL}}{V_O}} = \frac{1}{(0.588 - 0.5)(5m\Omega \times 5.472) \times \frac{5\mu s}{10\mu H} + \frac{0.843V}{48V}} = 53.29$$

(EQ. 35) $$K_d = 2 + \frac{R_O \cdot (1-D)^2}{R_I} \cdot \left(\frac{1}{K_m} + \frac{K}{1-D}\right) = 2 + \frac{9.6 \cdot (1 - 0.588)^2}{5m\Omega \times 5.472} \cdot \left(\frac{1}{53.29} + 0.5 \times 5m\Omega \times 5.472 \times \frac{5\mu s}{10\mu H} \times 0.588\right) = 3.343$$

(EQ. 36) $$\omega_{p0} = \frac{K_d}{C_O \times R_O} = \frac{3.343}{458.8\mu F \times 9.6\Omega} = 0.759kHz$$

(EQ. 37) $$f_{p0} = \frac{\omega_{p0}}{2\pi} = 0.121kHz$$

(EQ. 38) $$\omega_{pi} = \frac{K_m \times R_I}{L} = \frac{53.29 \times 0.027\Omega}{10\mu H} = 143.9kHz$$

(EQ. 39) $$f_{pi} = \frac{\omega_{pi}}{2\pi} = 22.9kHz$$

(EQ. 40) $$\omega_{z(esr)} = \frac{1}{C_O \times R_{ESR}} = \frac{1}{458.8\mu F \times 5m\Omega} = 435.9kHz$$

(EQ. 41) $$f_{z(esr)} = \frac{\omega_{z(esr)}}{2\pi} = 69.4\text{kHz}$$

The minimum value of RHPZ could be calculate by Equation 42.

(EQ. 42) $$f_{RHPZ} = \frac{R_O}{2\pi \times L} \times (1 - D_{max})^2 = \frac{9.6\Omega}{2\pi \times 10\mu H} \times \left(\frac{12V}{48V}\right)^2 = 9.55\text{kHz}$$

Therefore make 0.1 x f_{RHPZ} as crossover frequency and make the gain -20dB/decade:

(EQ. 43) $$f_c = 0.1 \times f_{RHPZ} = 0.955\text{kHz}$$

If R_3 (R18) = 24k, set the frequency of this zero f_{z1}= f_{p0}, then C_2 (C17) is calculated using Equation 44.

(EQ. 44) $$C_2 = \frac{1}{2\pi R_3 f_{p0}} = \frac{1}{2\pi \times 24k\Omega \times 0.121\text{kHz}} = 54.8\text{nF}$$

Select a standard value capacitor C_2 (C17) = 68nF.

Set the frequency of this pole f_{p1} = $f_{z(esr)}$, and should make sure f_c<< f_{p1} << f_{sw}. Then C_3 (C15) is calculated using Equation 45.

(EQ. 45) $$C_3 = \frac{1}{2\pi R_3 f_{z(esr)}} = \frac{1}{2\pi \times 24k\Omega \times 69.4\text{kHz}} = 95.5\text{pF}$$

Select a standard value capacitor C_3 (C15) = 100pF.

2.5.18 Parallel Connection

The ISL81805EVAL1Z evaluation board can operate in parallel, in a daisy chain setup. Figure 15 shows the wiring of two units in parallel and Figure 16 shows three units in parallel.

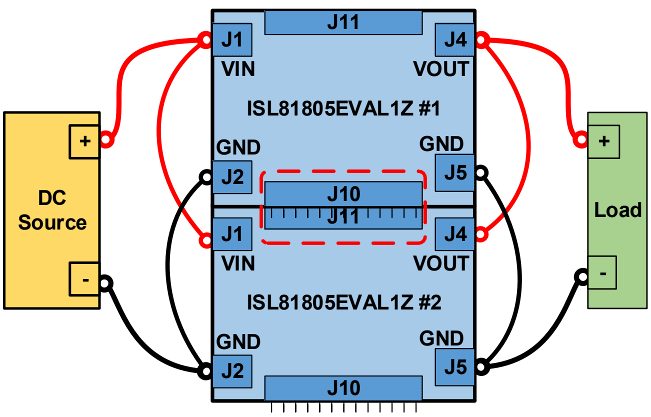

Figure 15. Setup for Two Units in Parallel

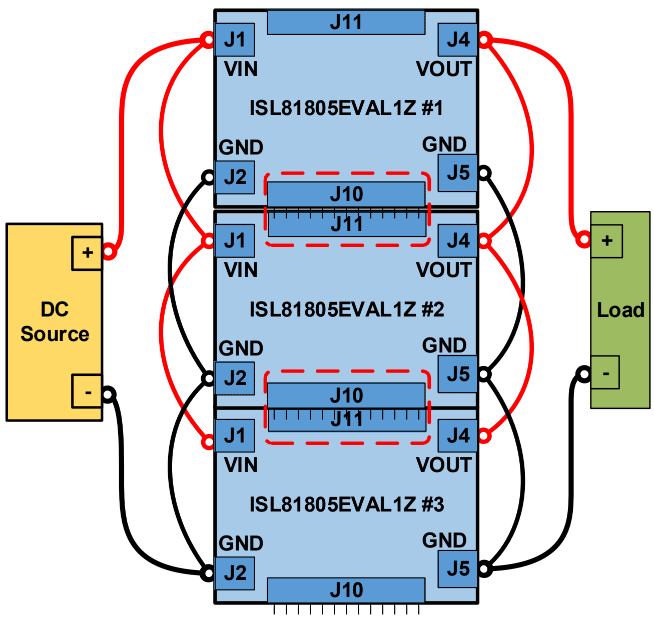

Figure 16. Setup for Three Units in Parallel

Table 3 shows the CLKOUT/DITHER phase settings with a different EN/UVLO2 pin connection and IMON2 pin voltage.

Table 3. CLKOUT and Channel 2 Phase Shift vs EN/UVLO2 and IMON2 Voltage

CLKOUT Phase Shift (°)[1]	Channel 2 Phase Shift (°)[2]	IMON2 Voltage (V)	EN/UVLO2
90	180	0 to 4.3	Tie to EN/UVLO1
60	180	4.7 to 5	Tie to EN/UVLO1
240	120	3 to 5	Tie to SGND

1. CLKOUT Phase Shift: CLKOUT rising edge delay after LG1 rising edge.
2. Channel 2 Phase Shift: LG2 rising edge delay after LG1 rising edge.

On the ISL81805EVAL1Z board, the IMON2 pin is tied to 5V and EN/UVLO2 is tied to EN/UVLO1, which leads to a default 60° CLKOUT Phase Shift.

3. Typical Performance Graphs

V_{IN} = 24V, V_{OUT} = 48V,T_A = 25°C, unless otherwise noted.

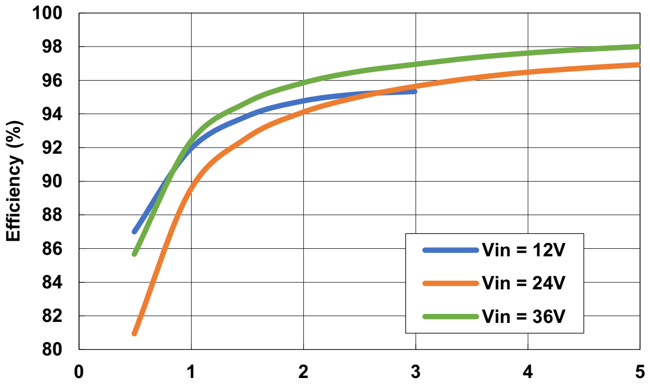

Figure 17. Efficiency, CCM

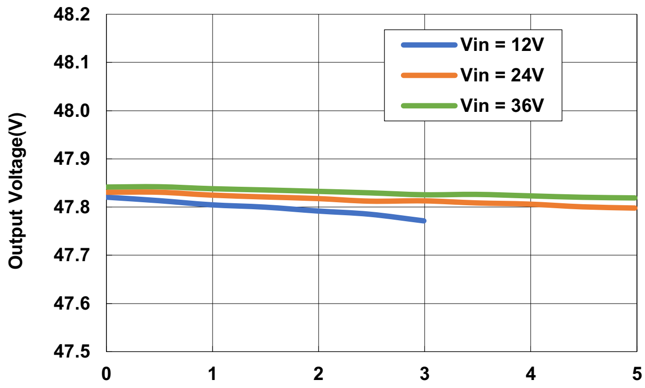

Figure 18. Load Regulation, CCM

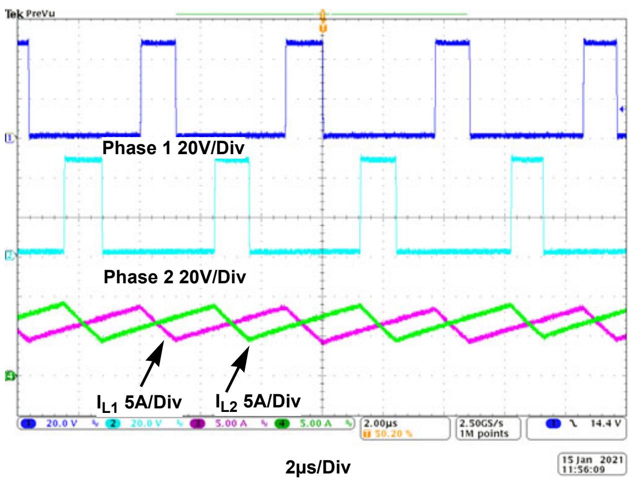

Figure 19. Phase 1, Phase 2, I_{L1}, I_{L2}, V_{IN} = 12V, I_{OUT} = 3A

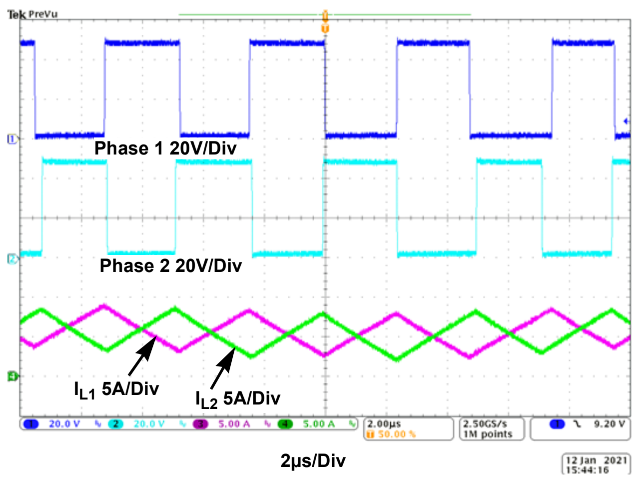

Figure 20. Phase 1, Phase 2, I_{L1}, I_{L2}, V_{IN} = 24V, I_{OUT} = 5A

V_{IN} = 24V, V_{OUT} = 48V,T_A = 25°C, unless otherwise noted. (Cont.)

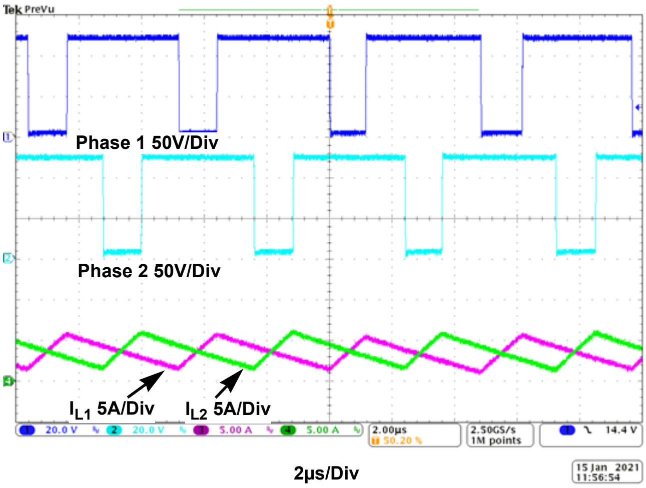

Figure 21. Phase 1, Phase 2, I_{L1}, I_{L2}, V_{IN} = 36V, I_{OUT} = 5A

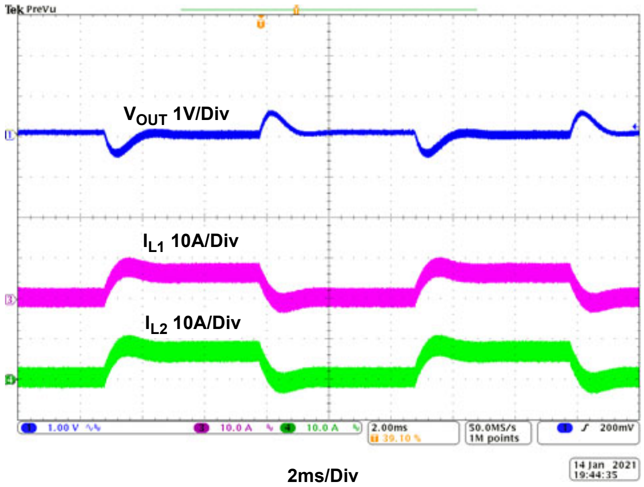

Figure 22. Load Transient, V_{IN} = 12V, I_{OUT} = 0A to 3A, 2.5A/µs, CCM

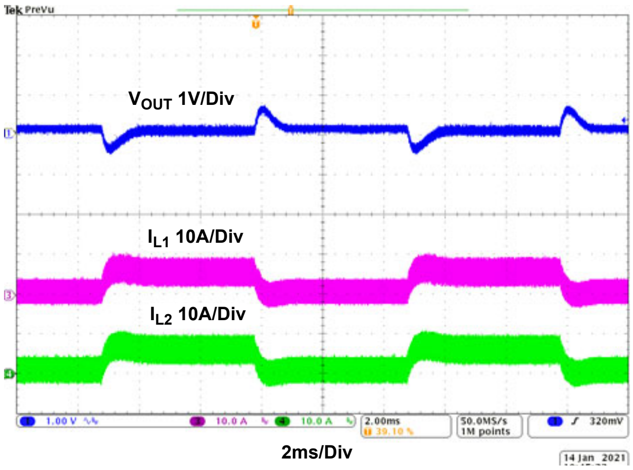

Figure 23. Load Transient, V_{IN} = 24V, I_{OUT} = 0A to 5A, 2.5A/µs, CCM

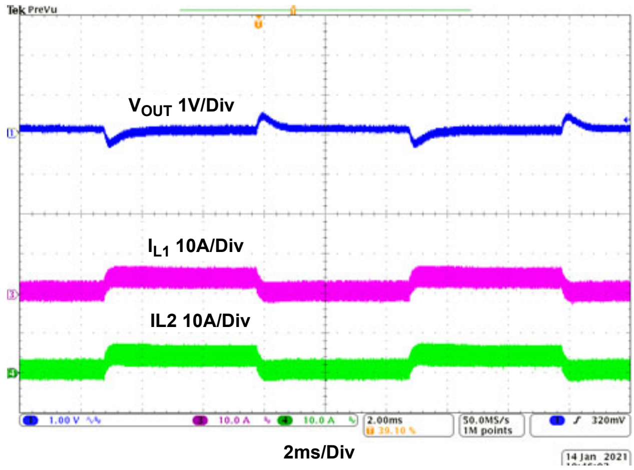

Figure 24. Load Transient, V_{IN} = 36V, I_{OUT} = 0A to 5A, 2.5A/µs, CCM

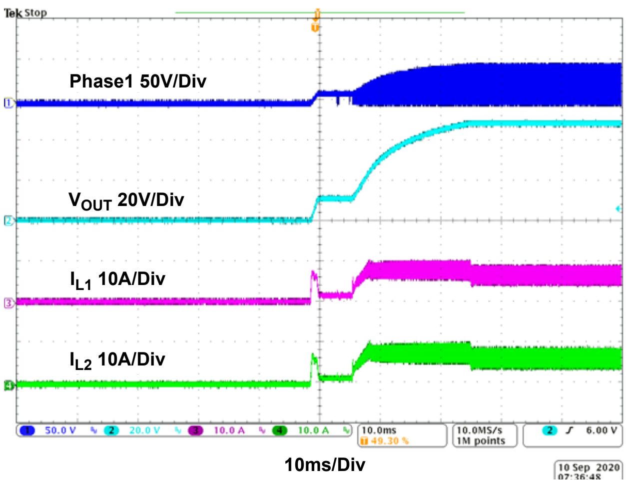

Figure 25. Start-Up Waveform, V_{IN} = 12V, I_{OUT} = 3A, CCM

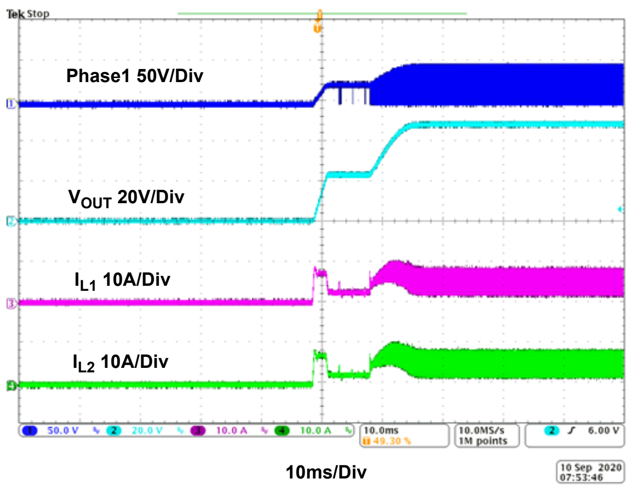

Figure 26. Start-Up Waveform, V_{IN} = 24V, I_{OUT} = 5A, CCM

V_{IN} = 24V, V_{OUT} = 48V,T_A = 25°C, unless otherwise noted. (Cont.)

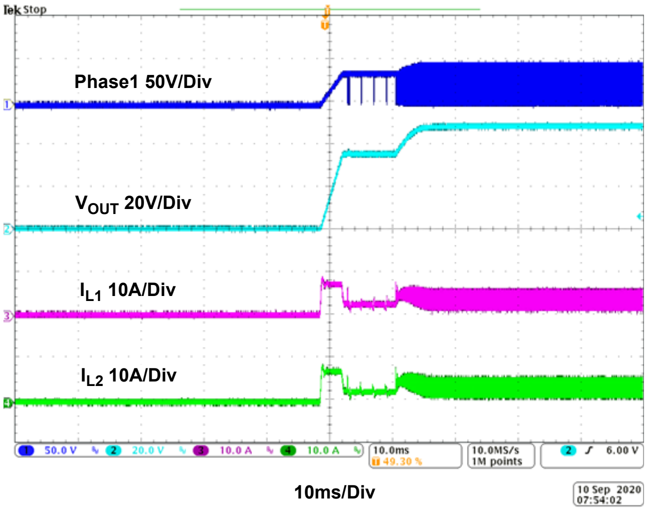

Figure 27. Start-Up Waveform, V_{IN} = 36V, I_{OUT} = 5A, CCM

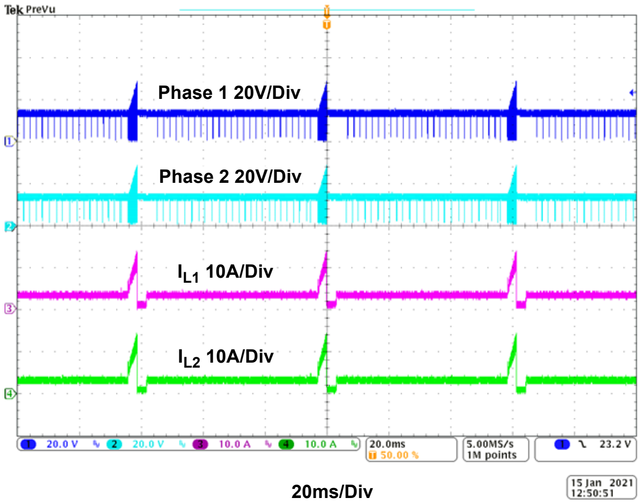

Figure 28. Hiccup OCP Waveform, V_{IN} = 12V

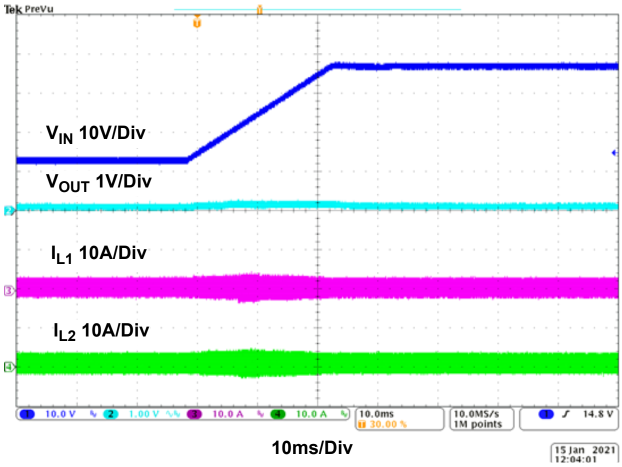

Figure 29. Line Transient, V_{IN} = 12V to 36V, 1V/ms, I_{OUT} = 0A

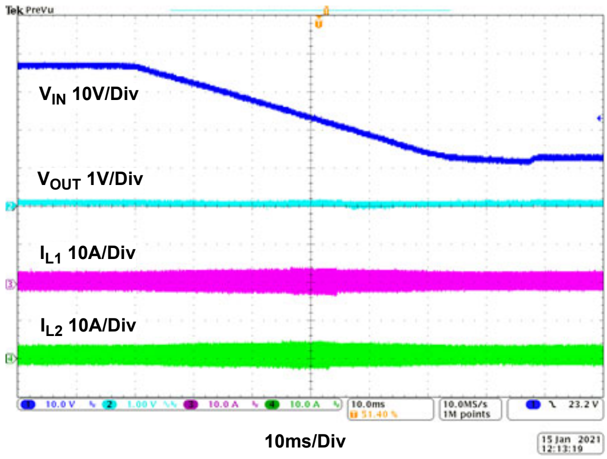

Figure 30. Line Transient, V_{IN} = 36V to 12V, 1V/ms, I_{OUT} = 0A

4. Ordering Information

Part Number	Description
ISL81805EVAL1Z	High Voltage Dual-phase Boost Controller Evaluation Board

5. Revision History

Rev.	Date	Description
1.00	Sep 14, 2021	Initial release

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