User's Manual

ISL75051ASEHEV1Z

User's Manual: Evaluation Board

High Reliability

Rev 0.00 Nov 2017

ISL75051ASEHEV1Z

Evaluation Board

UG148
Rev.0.00
Nov 29, 2017

1. Overview

ISL75051ASEH is a high-performance, adjustable, low-voltage, high-current, low-dropout linear regulator specified at 3A rated output current for input voltages from 2.2V to 6V. The LDO outputs can be adjusted from 0.8V to 5V using two preset resistors.

The ISL75051ASEHEV1Z evaluation board provides a simple platform to evaluate performance of the ISL75051ASEH. The device output voltage is adjustable, and jumpers are provided to easily set popular output voltages.

1.1 Key Features

- TID, ELDRS, and SEE Rated
- Very fast load transient response
- ±2.0% guaranteed V_{OUT} accuracy over line, load, and temperature
- Typical dropout of 287mV at 3A
- EN, PG, and OCP features
- Short-circuit and over-temperature protection

1.2 Specifications

- V_{IN} = 2.2V to 6.0V
- Temperature range: -55°C to 125°C

1.3 Ordering Information

Part Number	Description
ISL75051ASEHEV1Z	ISL75051ASEH evaluation board

1.4 Related Literature

- For a full list of related documents, visit our website
  - ISL75051ASEH product page

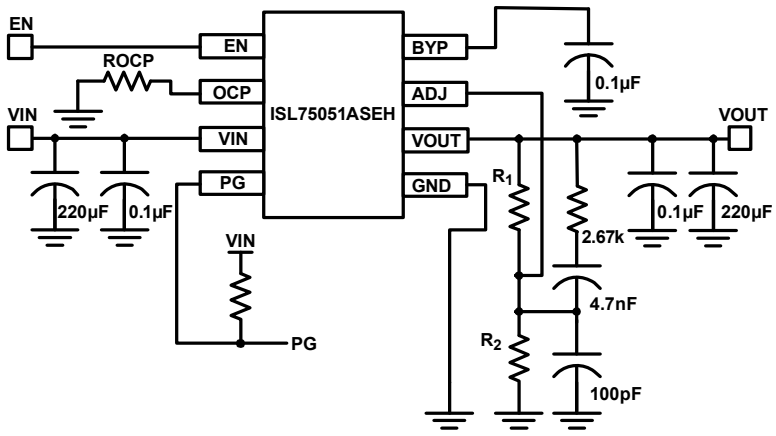

Figure 1. ISL75051ASEHEV1Z Simplified Schematic

1.5 What's Inside

The evaluation kit contains the following:

- ISL75051ASEHEV1Z evaluation board
- ISL75051ASEH datasheet
- This user manual

1.6 Test Steps

(1) Select the desired output voltage by shorting one of the jumpers from J2 through J6. The option of JP7 provides for continuous adjustment of V_{OUT} using potentiometer R_{13}.

(2) Set the OCP limit by using jumpers JP8 and JP9. JP9 = 0.8A min and JP8 = 4A min.

(3) Close JP10. Also closing jumper JP1 (2 and 3) selects R_2 = 5.49k as pull-up for PGOOD.

(4) Ensure that the output capacitor and C_P are set according to recommended values shown in Table 1 on page 5.

(5) Connect the input supply to VIN/GND and the load to VOUT/GND. Select the VIN to VOUT ratio to keep dissipation within the thermal limits of the device.

- Use JP11 to enable/disable the IC; Open = Enable, and Close = Disable.
(Note: For REVB boards, Close = Enable and Open = Disable.)

2. Functional Description

Use the following information to optimize the performance of the ISL75051ASEH.

2.1 Operating Range

- V_{IN} = 2.2V to 6.0V

2.2 Quick Start Guide

(1) Configure the EN pin. Shorting JP11 disables the part, while leaving it open enables the LDO.

(2) Set the OCP level.

(a) Use the 2 resistor locations provided on the board to configure the OCP trip point. R_3 and R_{14}, which are connected to JP8 and JP9, respectively.

(b) JP9 is set to provide an OCP trip point of 6.7A, JP8 is set for a trip point of 1.2A.

(3) Ensure that JP10 is shorted.

(a) R_4 (100Ω) is connected across the terminals of JP10. This is used for measuring the loop stability. Apply the AC signal across R_4 using JP10 and use TP7 (VOUT) and TP12 (VOUT') for the measurement.

(4) Short pins 2 and 3 of JP1.

(5) Set the VOUT level by shorting JP2 – JP7.

- JP2 – 0.8V
- JP3 – 1.5V
- JP4 – 1.8V
- JP5 – 2.5V
- JP6 – 4.0V
- JP7 – Adjustable, use R_{13} (potentiometer) to set your desired voltage.

(6) Apply 5.0V between VIN and GND (J1 – J2)

(7) Monitor VOUT using J3 – J4.

(8) SP1 is a scope probe jack on VOUT for evaluating load step transients on VOUT.

2.3 Input and Output Capacitor Selection

RH operation requires a combination of tantalum and ceramic capacitors to achieve a good volume-to-capacitance ratio. The recommended combination is a 220µF, 25mΩ, 10V DSSC 04051-032 rated tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 CDR04 ceramic capacitor. This is to be connected between VIN to GND pins and VOUT to GND pins of the LDO, with PCB traces no longer than 0.5cm. The stability of the device depends on the capacitance and ESR of the output capacitor. The usable ESR range for the device is 6mΩ to 100mΩ. At the lower limit of ESR = 6mΩ, the phase margin is about 51°C. On the high side, an ESR of 100mΩ is found to limit the gain margin at around 10dB. The typical GM/PM seen on the ISL75051ASEHEV1Z evaluation board for V_{IN} = 3.3V, V_{OUT} = 1.8V, and I_{OUT} = 3A, with a 220µF, 10V, 25mΩ capacitor, is GM = 16.3dB and PM = 69.16°C.

2.4 Pole Capacitor (C_P)

A small capacitor (C_P) can be placed on the ADJ pin of the ISL75051ASEH, as shown in Figure 2 on page 5, across the bottom resistor in the feedback resistor divider. This is effectively a pole. The value of the capacitor can be calculated using (EQ. 1):

$$F_P = 1/(2 \bullet pi \bullet R_{BOTTOM} \bullet C_P) \quad \text{(EQ. 1)}$$

The pole should be set to have the break frequency at 1MHz.

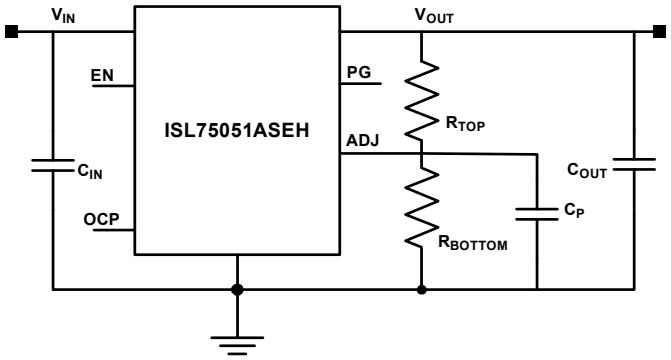

Figure 2. ISL75051ASEH Typical Application

Table 1 gives the recommended values for output capacitors (MLCC X5R/X7R) and C_P for different voltage rails. Correct selection of the output capacitor and C_P also helps increase PSRR at high frequencies. The board, however, uses a 100pF capacitor as a typical value most suited for the application range.

Table 1. Recommended Output Capacitor Values

V_{OUT} (V)	R_{TOP} (kΩ)	R_{BOTTOM} (Ω)	C_P (pF)	C_{OUT} (µF)
5.0	4.32	499	120	220
4.0	4.32	634	120	220
2.5	4.32	1.13k	120	220
1.8	4.32	1.74k	100	220
1.5 (Note 1)	4.32	2.26k	100	47
1.5	4.32	2.26k	100	220
0.8	4.32	7.87k	68	220

Note:

1. Either option can be used depending on cost/performance requirements.

3. PCB Layout Guidelines

Good PCB layout is important for achieving expected performance. When placing components and routing traces, minimize ground impedance and keep parasitic inductance low. Give the input and output capacitors a good ground connection, and place them as close to the IC as possible. Route the traces connecting the ADJ pin away from noisy planes and traces, and keep the board capacitance of the ADJ net to GND as low as possible.

3.1 Thermal Guidelines

If the die temperature exceeds +175°C typical, then the LDO output shuts down to zero until the die temperature cools to +155°C typical. The level of power combined with the thermal impedance of the package ($R\theta_{JC}$ of 4°C/W for the 18 Ld CDFP package) determines whether the junction temperature exceeds the thermal shutdown temperature specified in the “Electrical Specifications” table of the ISL75051ASEH datasheet. Mount the device on a high-effective thermal conductivity PCB with thermal vias, per JESD51-7 and JESD51-5. Place a silpad between the package base and PCB copper plane. Select the V_{IN} and V_{OUT} ratios to ensure that dissipation for the selected V_{IN} range keeps T_J within the recommended operating level of 150°C for normal operation.

3.2 ISL75051ASEHEV1Z Evaluation Board

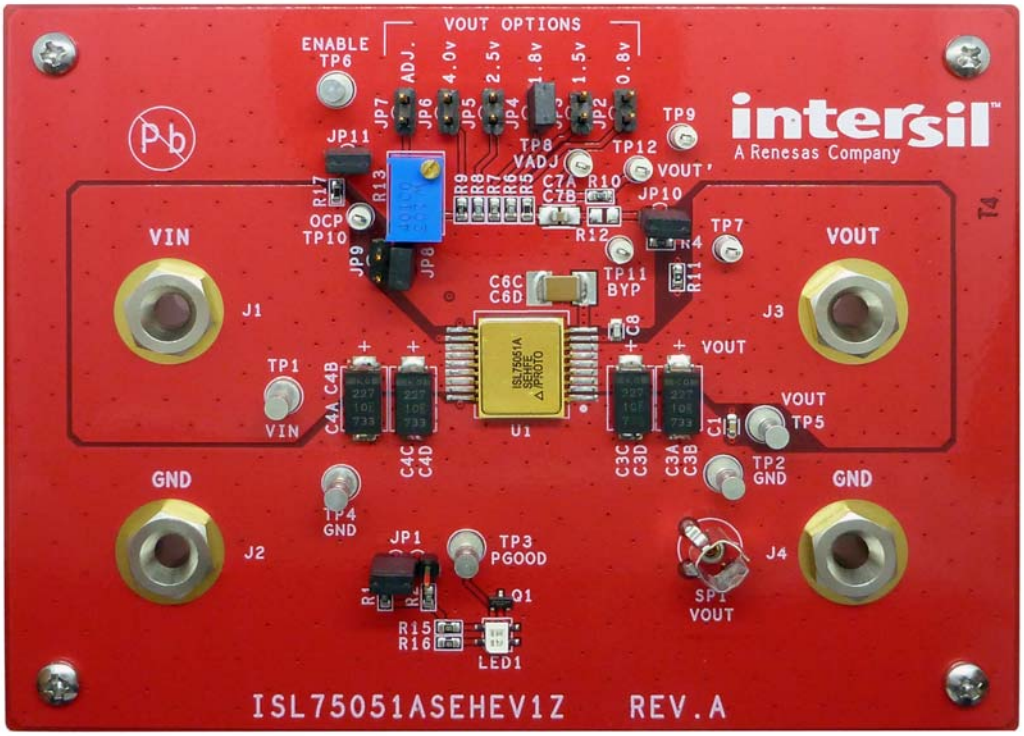

Figure 3. ISL75051ASEHEV1Z Evaluation Board, Top

Figure 4. ISL75051ASEHEV1Z Evaluation Board, Bottom

3.3 ISL75051ASEHEV1Z Schematic

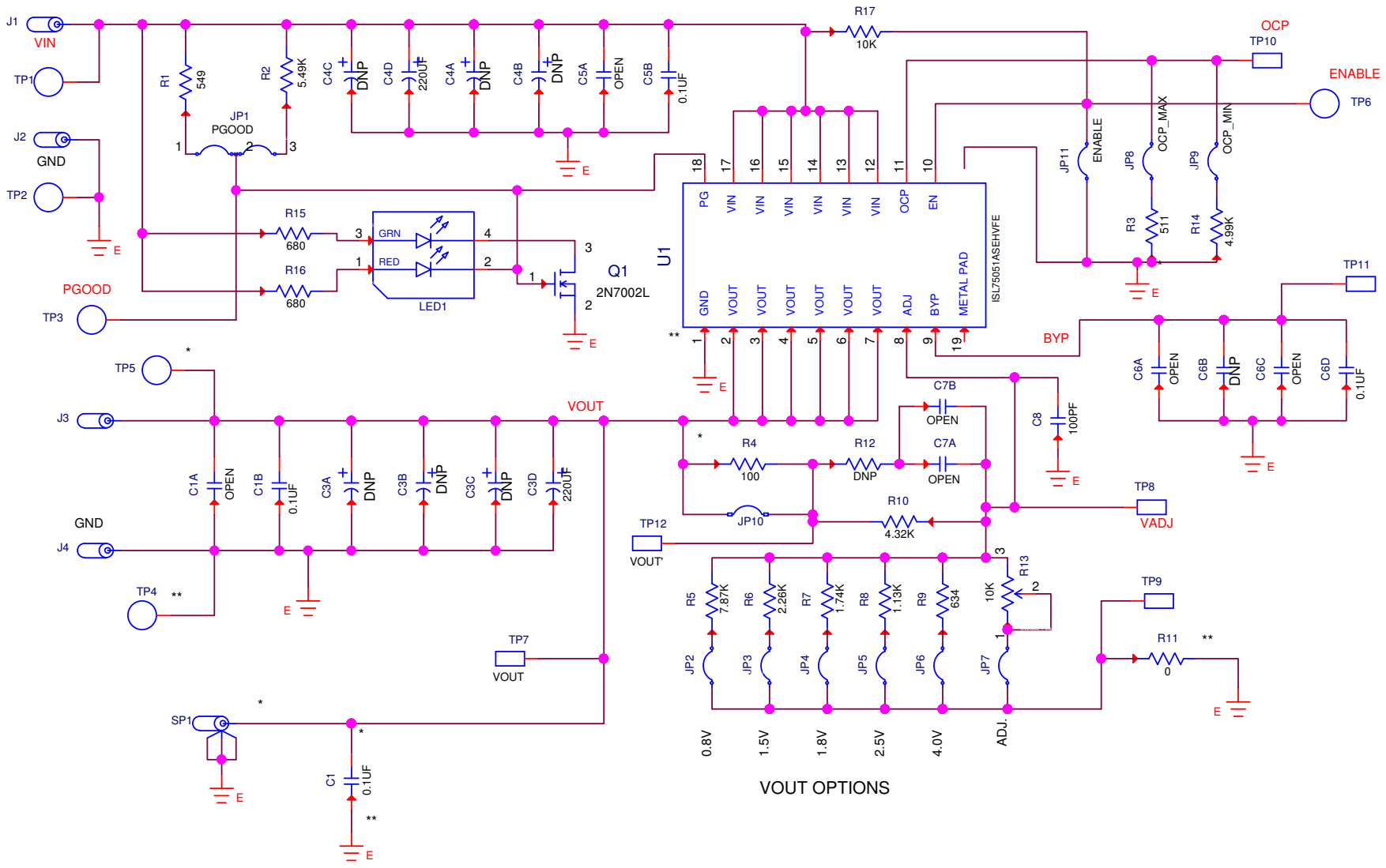

Figure 5. Schematic

3.4 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL75051ASEHEV1Z, REVA, ROHS	IMAGINEERING INC	ISL75051ASEHEV1ZREVAPCB
1	C7B	CAP-MILQUAL, SMD, 0805, 4700pF, 50V, 10%, BX, ROHS	VISHAY/VITRAMON	CDR01BX472AKMR
4	C1B, C5B, C6B, C6D	CAP-MILQUAL, SMD, 1812, 0.1µF, 50V, 10%, BX, ROHS	AVX	CDR04BX104AKMR
1	C8	CAP, SMD, 0603, 100pF, 50V, 10%, X7R, ROHS	KEMET	C0603C101K5RACTU
1	C1	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	MURATA	GRM39X7R104K016AD
0	C1A, C5A, C6A, C6C	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
0	C7A	CAP, SMD, 0805, DNP-PLACE HOLDER, ROHS		
4	C3B, C3D, C4B, C4D	CAP-TANT, SMD, 7.3x4.3, 220µF, 10V, 20%, 25mΩ, DF:10, ROHS	KEMET	T525D227M010ATE025
4	J1-J4	CONN-JACK, BANANA-SS-SDRLESS, VERTICAL, 0.53 Length, ROHS	JOHNSON COMPONENTS	108-0740-001
1	SP1	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	TEKTRONIX	131-4353-00
6	TP1-TP6	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
6	TP7-TP12	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
10	JP2-JP11	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	JP1	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
11	JP1-Pins 1-2, JP2-JP11	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	SULLINS	SPC02SYAN
1	LED1	LED, SMD, 3x2.5mm, 4P, RED/GREEN, 12/20MCD, 2V	LUMEX	SSL-LXA3025IGC-TR
1	U1	IC-RADHARD, CMOS 3A LDO REGULATOR, 18P, CFP, ROHS	INTERSIL	ISL75051ASEHFE/PROTO
1	Q1	TRANSISTOR-MOS, N-CHANNEL, SMD, SOT23, 60V, 115mA, ROHS	ON SEMICONDUCTOR	2N7002LT1G

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R13	POT-TRIM, TH, 3P, 10k, 1/2W, 10%, 3/8SQ, 25TURN, TOPADJ, ROHS	BOURNS	3299W-1-103LF
0	R12	RESISTOR, SMD, 0805, DNP, DNP, DNP, TF		
1	R11	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
1	R4	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1000FT
1	R17	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1002FT
1	R8	RES, SMD, 0603, 1.13k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-071K13L
1	R7	RES, SMD, 0603, 1.74k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1741V
1	R6	RES, SMD, 0603, 2.26k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-072K26L
1	R10	RES, SMD, 0603, 4.32k, 1/10W, 1%, TF, ROHS		
1	R14	RES, SMD, 0603, 4.99k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF4991V
1	R3	RES, SMD, 0603, 511Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5110FT
1	R1	RES, SMD, 0603, 549Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5490FT
1	R2	RES, SMD, 0603, 5.49k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5491FT
1	R9	RES, SMD, 0603, 634Ω, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-07634RL
2	R15, R16	RES, SMD, 0603, 680Ω, 1/10W, 1%, TF, ROHS	ROHM	MCR03EZPFX6800
1	R5	RES, SMD, 0603, 7.87k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-077K87L
4	Four corners	SCREW, 4-40X1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	BUILDING FASTENERS	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40X3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	KEYSTONE	2204
1	Place assy in bag	BAG, STATIC, 6X8, ZIPLOC, ROHS	ULINE	S-2262
1	AFFIX TO BACK OF PCB	LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME	INTERSIL	LABEL-DATE CODE

3.5 Board Layout

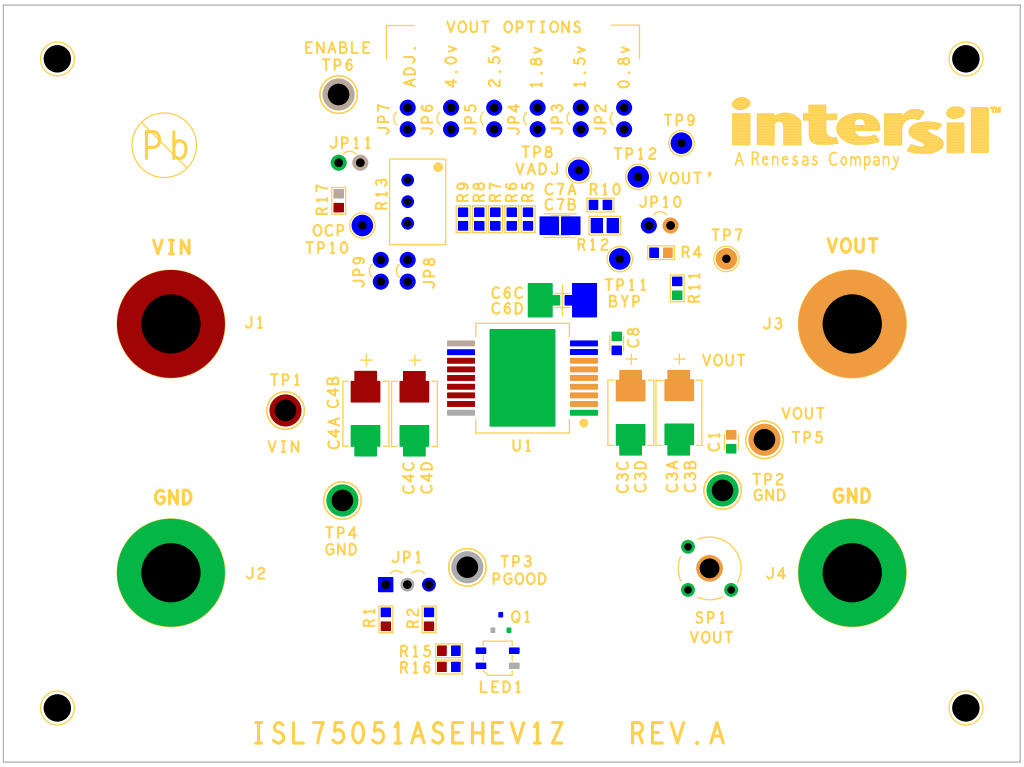

Figure 6. Silk Screen Top

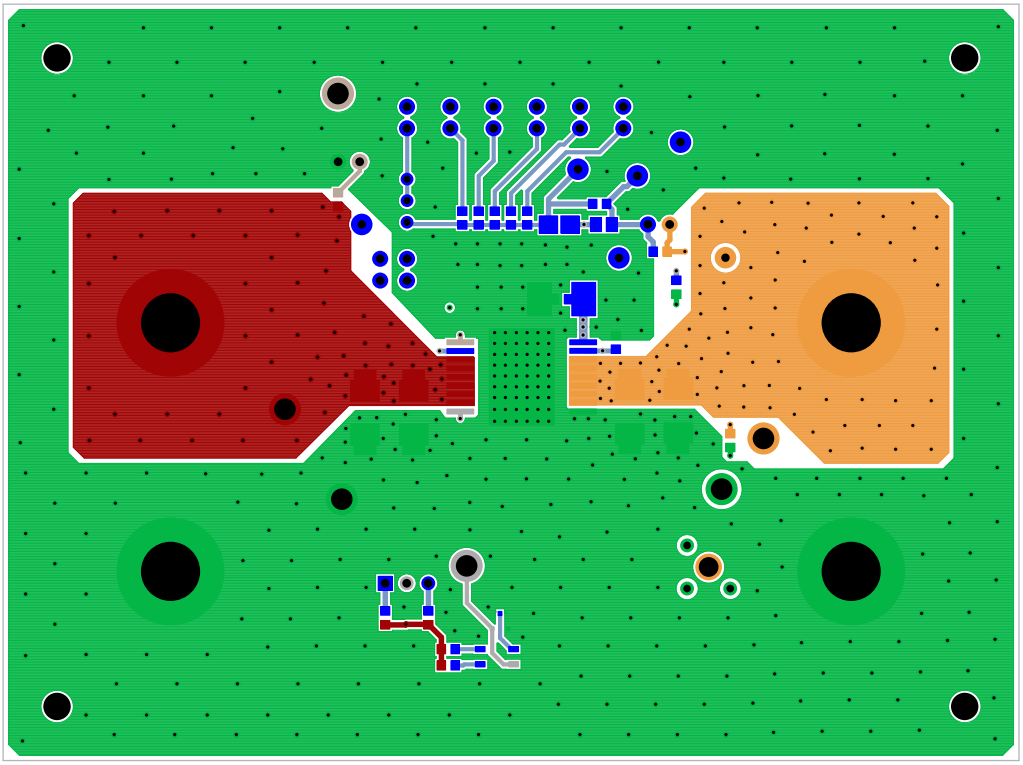

Figure 7. Top Layer Component Side

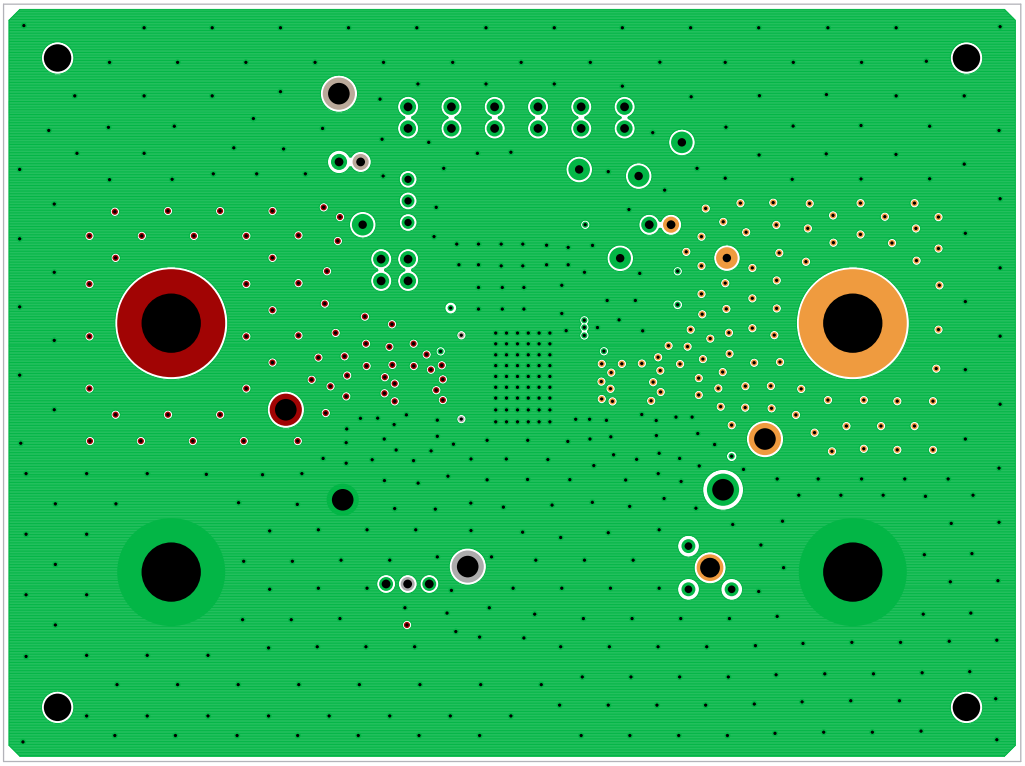

Figure 8. Layer 2

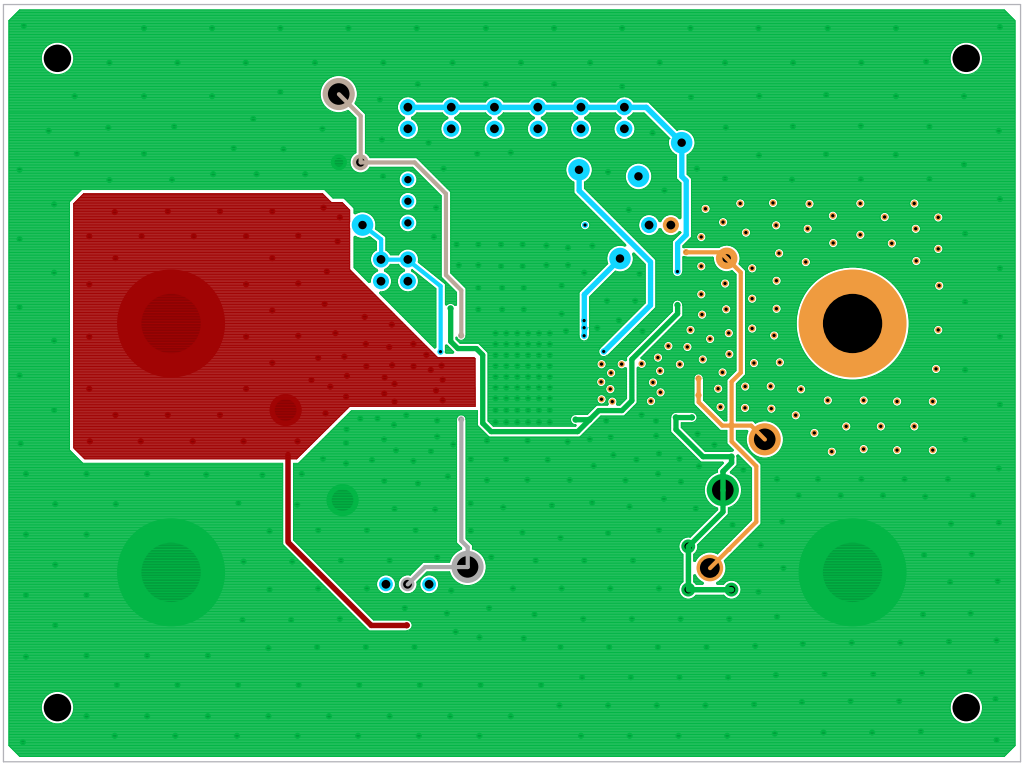

Figure 9. Layer 3

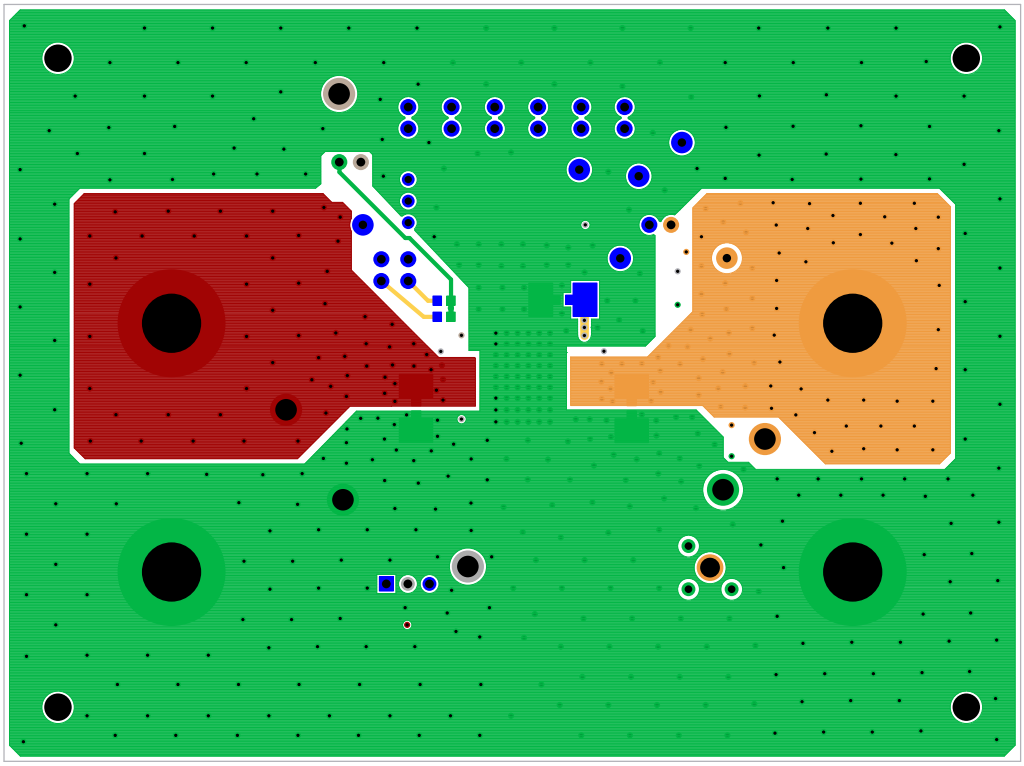

Figure 10. Bottom Layer Solder Side

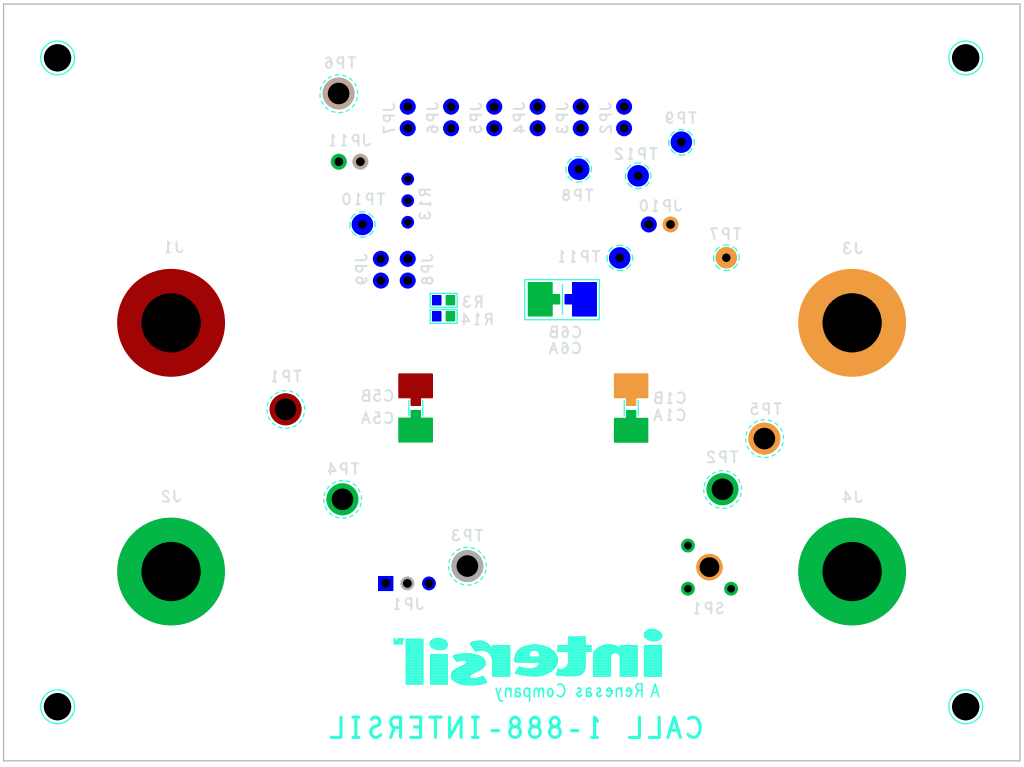

Figure 11. Silk Screen Bottom

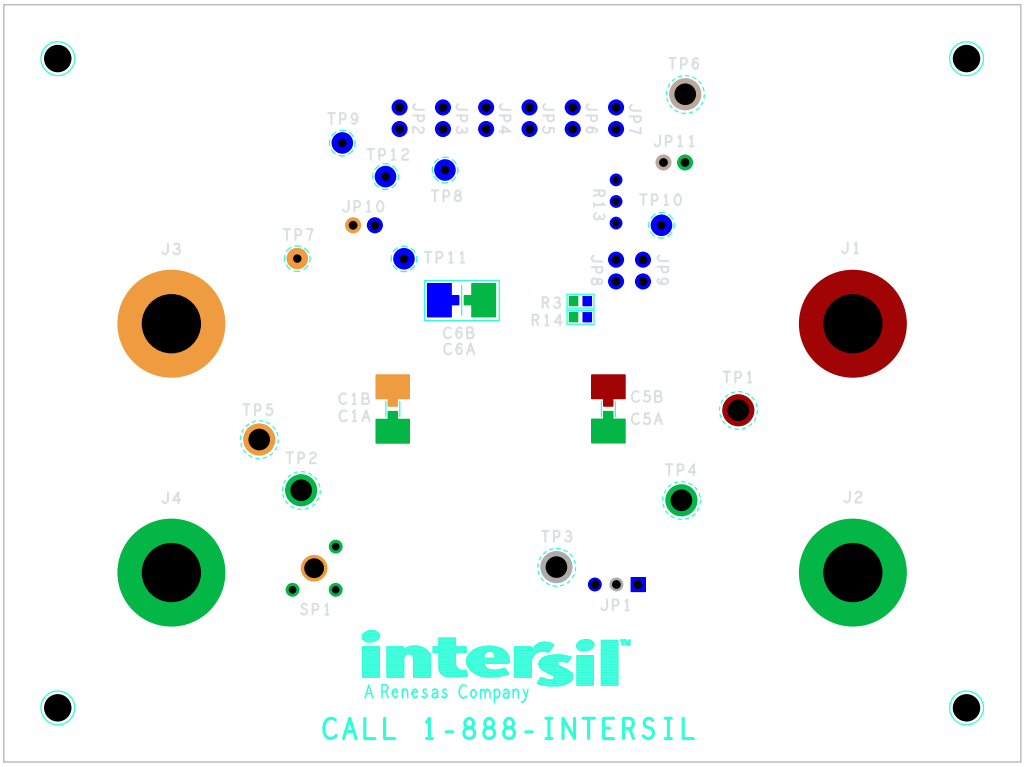

Figure 12. Silk Screen Bottom Mirror

4. Typical Performance Curves

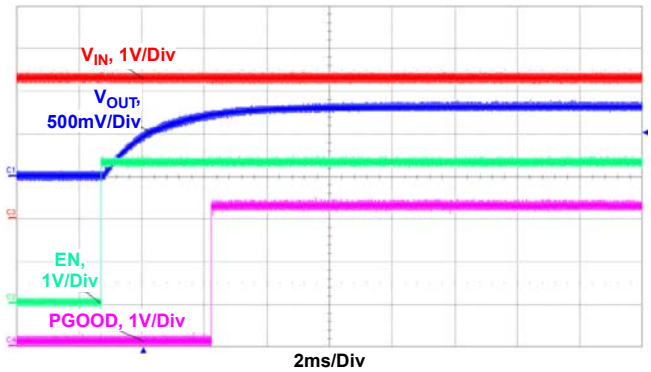

Figure 13. Start-Up Waveforms: V_{IN} = 6.0V, V_{OUT} = 0.8V, EN Low to High

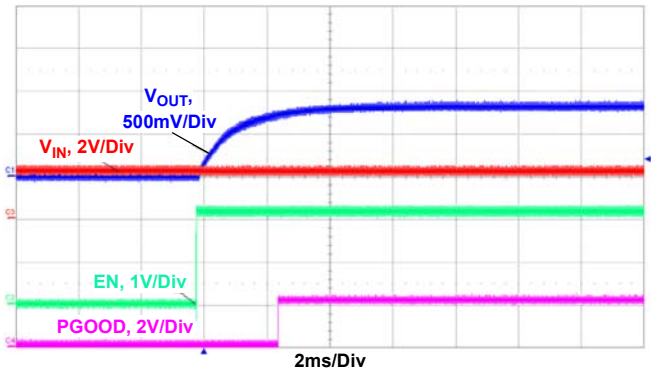

Figure 14. Start-Up Waveforms: V_{IN} = 2.2V, V_{OUT} = 0.8V, EN Low to High

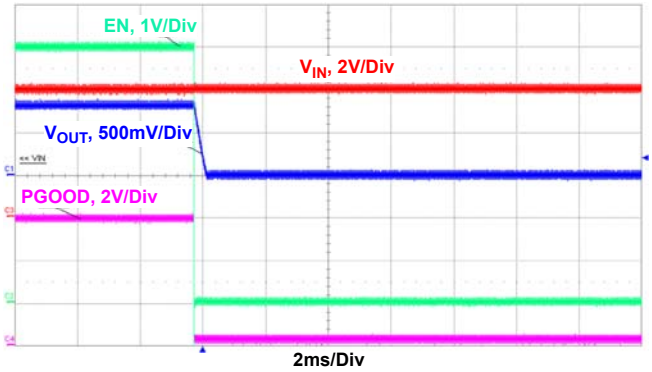

Figure 15. Shutdown Waveform: V_{IN} = 6.0V, V_{OUT} = 0.8V, EN High to Low

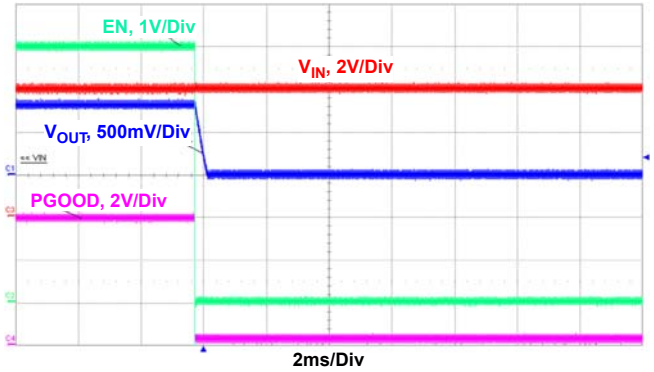

Figure 16. Shutdown Waveform: V_{IN} = 2.2V, V_{OUT} = 0.8V, EN High to Low

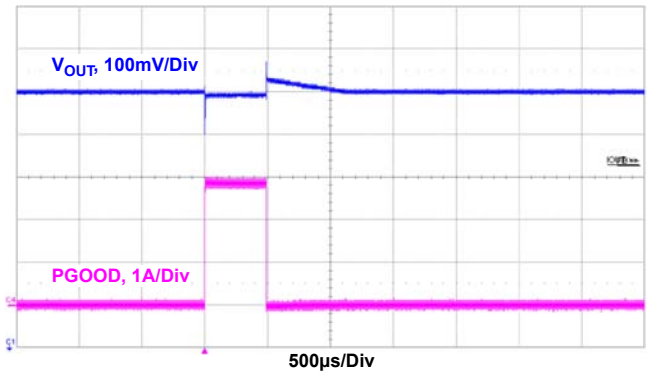

Figure 17. Load Transient, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 47µF 35mΩ

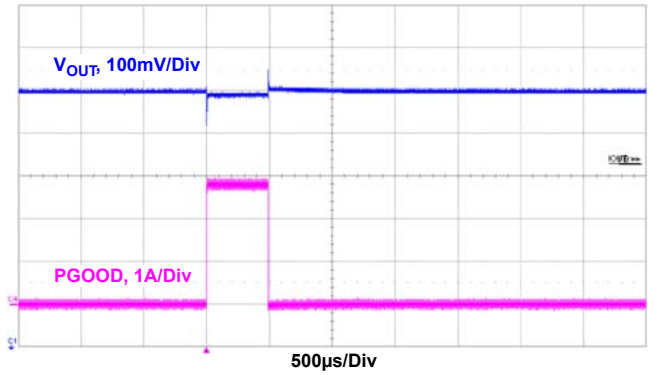

Figure 18. Load Transient, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 220µF 25mΩ

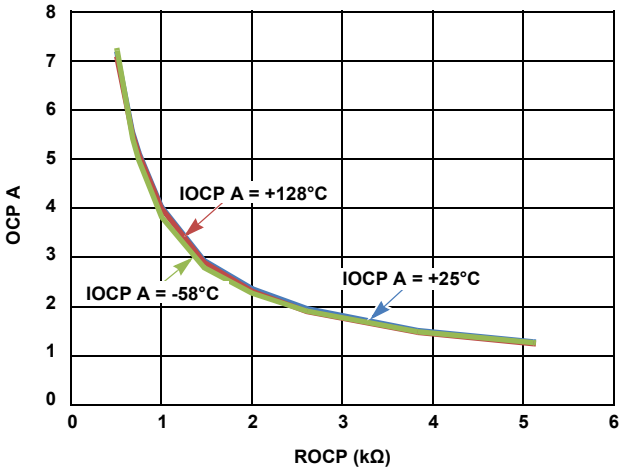

Figure 19. ROCP (kΩ) vs OCP A Over Temperature

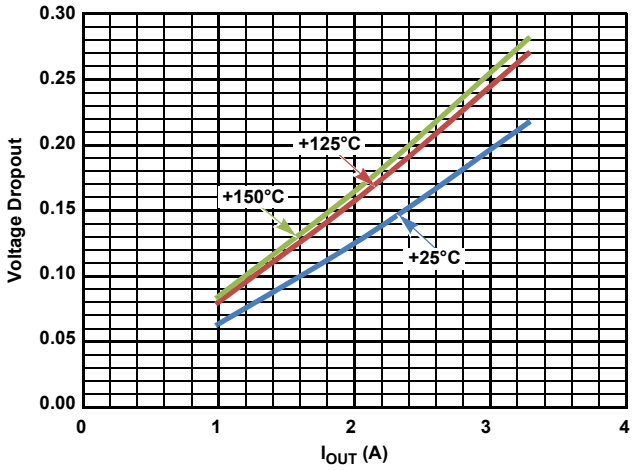

Figure 20. Dropout vs I_{OUT}

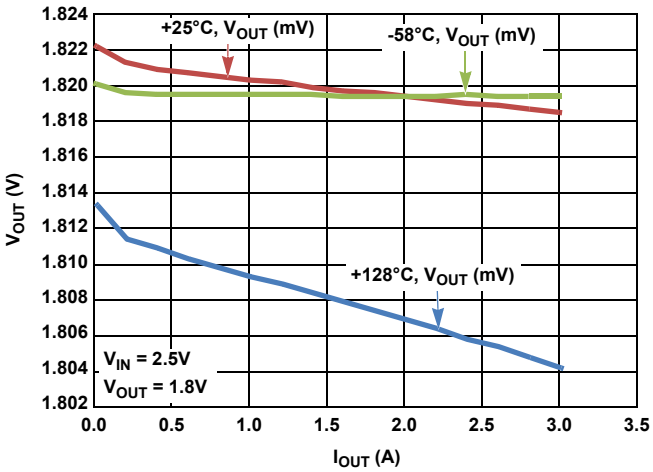

Figure 21. Load Regulation V_{OUT} vs I_{OUT}

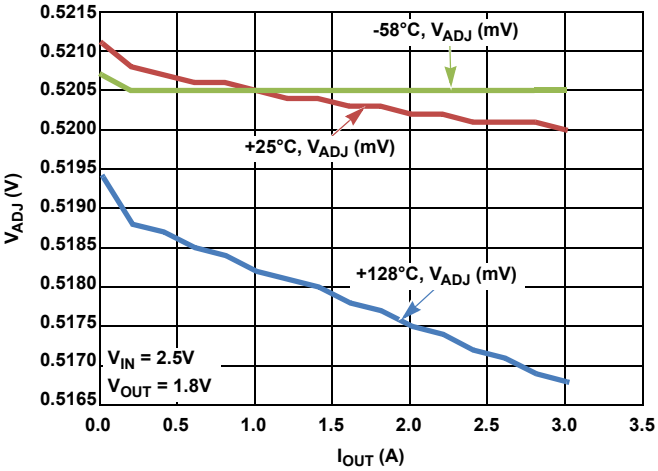

Figure 22. Load Regulation V_{ADJ} vs I_{OUT}

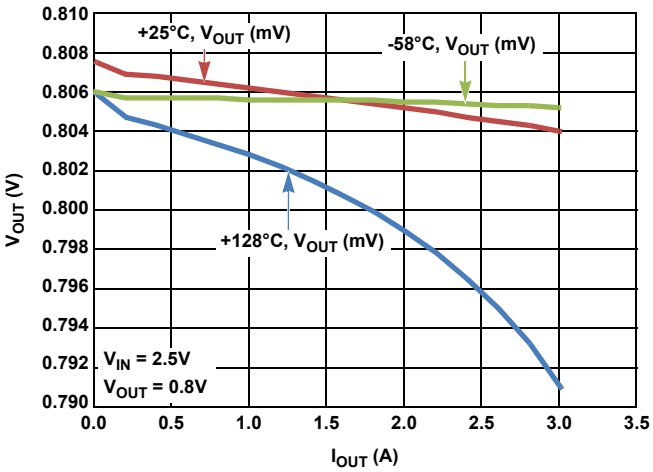

Figure 23. Load Regulation V_{OUT} vs I_{OUT}

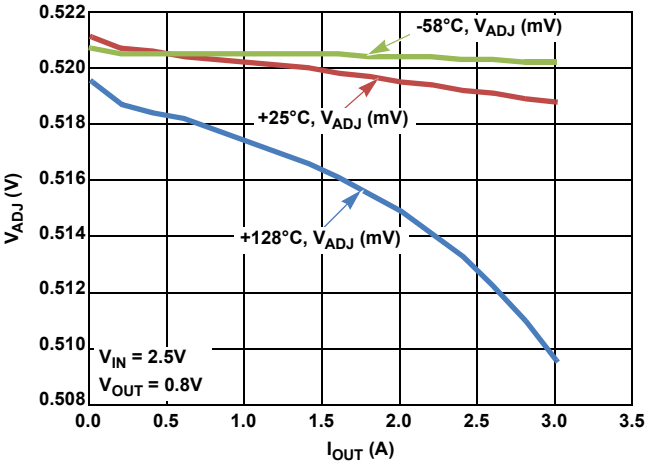

Figure 24. Load Regulation V_{ADJ} vs I_{OUT}

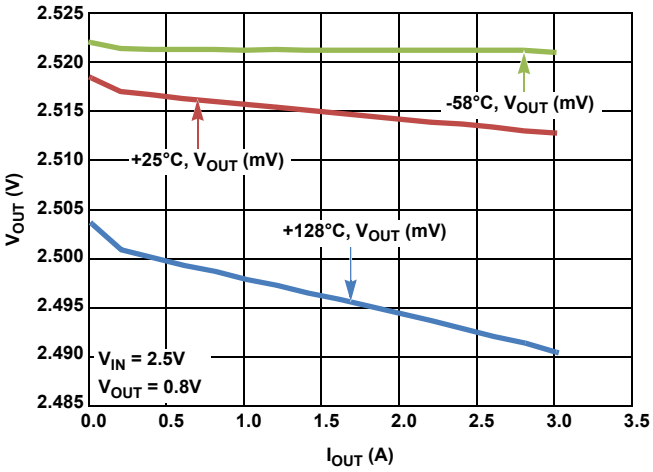

Figure 25. Load Regulation V_{OUT} vs I_{OUT}

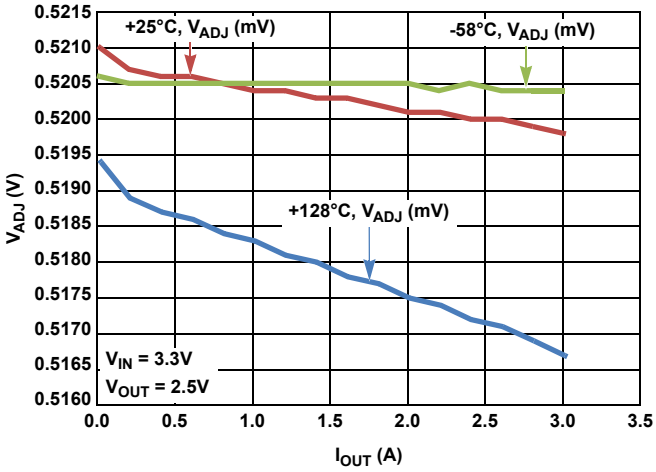

Figure 26. Load Regulation V_{ADJ} vs I_{OUT}

5. Revision History

Rev.	Date	Description
0.00	Nov 29, 2017	Initial release

ISL75051ASEHEV1Z

intersil™

UG148