ISL71040MEV1Z

Evaluation Board

The ISL71040MEV1Z evaluation platform is designed to evaluate the ISL71040M. The ISL71040M is designed to drive enhancement mode Gallium Nitride (GaN) FETs in isolated topologies and boost type configurations. It operates across a supply range of 4.5V to 13.2V and offers both non-inverting and inverting inputs to satisfy non-inverting and inverting gates drive within a single device. The ISL71040M has a 4.5V gate drive voltage (V_{DRV}) that is generated using an internal regulator that prevents the gate voltage from exceeding the maximum gate-to-source rating of enhancement mode GaN FETs. The gate drive voltage also features an Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB) and keeps OUTL turned on to ensure the GaN FET is in an OFF state whenever VDRV is below the UVLO threshold. The ISL71040M inputs can withstand voltages up to 14.7V regardless of the V_{DD} voltage. This allows the ISL71040M inputs to be connected directly to most PWM controllers. The split outputs of the ISL71040M offer the flexibility to adjust the turn-on and turn-off speed independently by adding additional impedance to the turn-on/off paths.

Key Features

- Wide V_{DD} range single
  - 4.5V to 13.2V
- Location provided for load resistors to switch the GaN FET with a load
- SMA connector on the gate drive voltage to analyze the gate waveforms
- Drain/source sense test points to analyze the drain to source waveforms
- Banana jack connectors for power supplies and drain/source connections

Specifications

- V_{DD} range: 4.5V to 13.2V

Ordering Information

Part Number	Description
ISL71040MEV1Z	ISL71040MEV1Z evaluation board

Related Literature

For a full list of related documents, visit our website:

- ISL71040M device page

1. Functional Description

The ISL71040M is a single channel, high speed enhanced mode GaN FET low-side driver for isolated power supplies and Synchronous Rectifier (SR) applications.

The inputs stage can handle inputs to the 14.7V independent of V_{DD} and offers both inverting and non-inverting inputs. The split output stage is capable of sourcing and sinking high currents and allows for independent tuning of the turn-on and turn-off times. A typical propagation delay of 36ns enables high switching frequency operation.

1.1 Operating Range

The ISL71040M offers a wide operating supply range of 4.5V to 13.2V. The gate drive voltage is generated from an internal linear regulator to keep the gate-source voltage below the absolute maximum level of 6V for the ISL7002xSEH GaN FET devices.

1.2 Quick Start Guide

1. Apply 5.0V to VDD.
2. Drive the IN or INB driver inputs.
    a. To drive INB, populate R_1 with a 0Ω resistor and remove the 0Ω resister on R_2.
3. Monitor the gate transition waveforms using SP_3.
    a. Use a low capacitance SMA cable to reduce the rise and fall times.
    b. Use a scope probe with a short ground loop soldered to the outside of the SMA connector.
4. Monitor the V_{DS} voltage using TP_{10} and TP_{11} with a short ground loop connection on a scope probe.
5. Switch the FET with a load using R_5, R_6, and R_7.
    a. C_3:C_8 counter any cable inductance leading up the J_3 and prevent drain-to-source voltage spikes that can damage the GaN FET.
6. Use SP_1 and SP_2 to sense the current traveling through the FET.

1.3 Gate Drive for N-Channel GaN FETs

New technologies based on wide bandgap semiconductors produce High Electron Mobility Transistors (HEMT). An example of a HEMT is the GaN based power transistors such as the ISL73023SEH, which offer very low $r_{DS(ON)}$ and gate charge (Q_g). These attributes make the devices capable of supporting very high switching frequency operation while avoiding significant efficiency loss. However, GaN power FETs have special requirements in terms of gate drive that the ISL71040M is designed to specifically address.

Key properties of a gate driver for GaN FETs are:

- Gate drive signals need to be sufficiently higher than the V_{GS} threshold specified in GaN FET datasheets for proper operation
- A well regulated gate drive voltage to keep the V_{GS} lower than specified absolute maximum level of 6V
- Split pull-up and pull-down gate connections to add series gate resistors that independently adjust turn-on and turn-off speed. This eliminates the need of a series diode whose voltage drop can cause an insufficient gate drive voltage
- Driver pull-down resistance < 0.5Ω that eliminates undesired Miller turn-on
- High current source/sink capability and low propagation delay achieve high switching frequency operation

1.4 Undervoltage Lockout

The VDD pin accepts a recommended supply voltage range of 4.5V to 13.2V and is the input to the internal linear regulator. VDRV is the output of the regulator and is equal to 4.5V. VDRV provides the bias for all internal circuitry and the gate drive voltage for the output stage.

UVLO circuitry monitors the voltage on VDRV and is designed to prevent unexpected glitches when VDD is being turned on or turned off. When VDRV < ~1V, an internal 500Ω resistor connected between OUTL and ground helps keep the gate voltage close to ground. When ~1.2V < VDRV < UV, OUTL is driven low while ignoring the logic inputs and OUTH is in a high impedance state. This low state has the same current sinking capacity as during normal operation. This ensures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates from the Miller capacitance.

When VDRV > UVLO, the outputs now respond to the logic inputs. In the non-inverting operation (PWM signal applied to IN pin) the output is in-phase with the input. In the inverting operation (PWM signal applied to INB pin) the output is out-phase with the input.

For the negative transition of VDD through the UV lockout voltage, the OUTL is active low and OUTH is high impedance when VDRV < ~3.7VDC regardless of the input logic states.

1.5 Input Stage

The input threshold of the ISL71040M is based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage. With typical high threshold = 1.7V and typical low threshold = 1.4V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V and 5V power controllers.

The ISL71040M offers both inverting and non-inverting inputs. The state of the output pin is dependent on the bias on both input pins. Table 1 summarizes the inputs to output relation.

Table 1. Truth Table

IN	INB	OUT	OUTH	OUTL
0	0	0	Hi-Z	0
0	1	0	Hi-Z	0
1	0	1	1	Hi-Z
1	1	0	Hi-Z	0

Note: OUT is the combination of OUTH and OUTL connected together. Hi-Z represents a high impedance state.

As a protection mechanism, if any of the input pins are left in a floating condition, OUTL is held in the low state and OUTH is high impedance. This is achieved using a 300kΩ pull-up resistor from INB to VDD and a 300kΩ pull-down resistor from the IN pin to VSS. For proper operation in non-inverting applications, INB should be connected to VSS. For inverting applications, IN should be connected to VDD for proper operation.

1.6 Enable Function

An enable or disable function can be easily implemented in ISL71040M using the unused input pin. The following tips describe how to implement an enable/disable function:

- In a non-inverting configuration, the INB pin can be used to implement the enable/disable function. OUT is enabled when INB is biased low, acting as an active low enable pin
- In an inverting configuration, the IN pin can be used to implement the enable and disable function. OUT is enabled when IN is biased high, acting as an active high enable pin

1.7 Driver Power Dissipation

The ISL71040M power dissipation is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation but is usually not significant compared to the gate charge losses.

For example, the ISL73023SEH has a total gate charge of 13nC when V_{DS} = 50V and V_{GS} = 4.5V. This is the charge that a driver must source to turn on the GaN FET and must sink to turn off the GaN FET.

Equation 1 calculates the power dissipation of the driver:

(EQ. 1) $$P_D = 2 \bullet Q_c \bullet freq \bullet V_{GS} \bullet \frac{R_{gate}}{R_{gate} + r_{DS(ON)}} + I_{DD}(freq) \bullet V_{DD}$$

where:

freq = Switching frequency

V_{GS} = V_{DRV} bias of the ISL71040M

Q_c = Gate charge for V_{GS}

I_{DD}(freq) = Bias current at the switching frequency

$r_{DS(ON)}$ = ON-resistance of the driver

R_{gate} = External gate resistance (if any)

Note that the gate power dissipation is proportionally shared with the external gate resistor. Do not overlook the power dissipated by the external gate resistor.

2. General PCB Layout Guidelines

The AC performance of the ISL71040M depends significantly on the design of the Printed Circuit Board (PCB). The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET induces significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt induces currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. The noise, magnetically induced on a 10kΩ resistor, is 10 times larger than the noise on a 1kΩ resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the V_{DRV}, V_{DD}, and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits, especially on OUTH. If an external gate resistor is unacceptable, then the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL71040M.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. This injects di/dt currents into the signal ground paths.
- Calculate power dissipation and voltage drop for the power traces. Many PCB/CAD programs have built in tools for trace resistance calculation.
- Large power components (such as power FETs, electrolytic caps, and power resistors) have internal parasitic inductance which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components, especially parasitic inductance.
- The GaN FETs have a separate substrate connection that is internally tied to the source pin. Source and substrate should be at the same potential. Limit the inductance in the OUTH/L to Gate trace by keeping it as short and thick as possible.

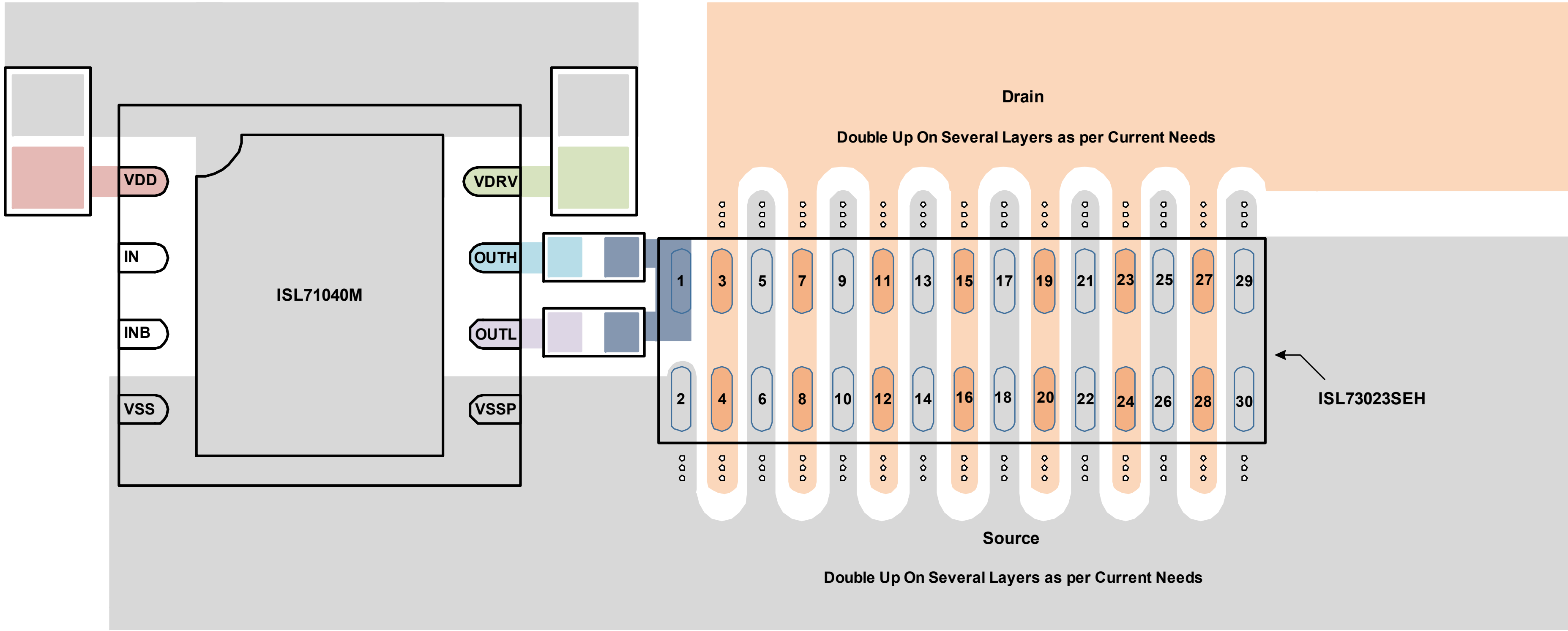

Figure 1. PCB Layout Recommendation

2.1 ISL71040MEV1Z Evaluation Board

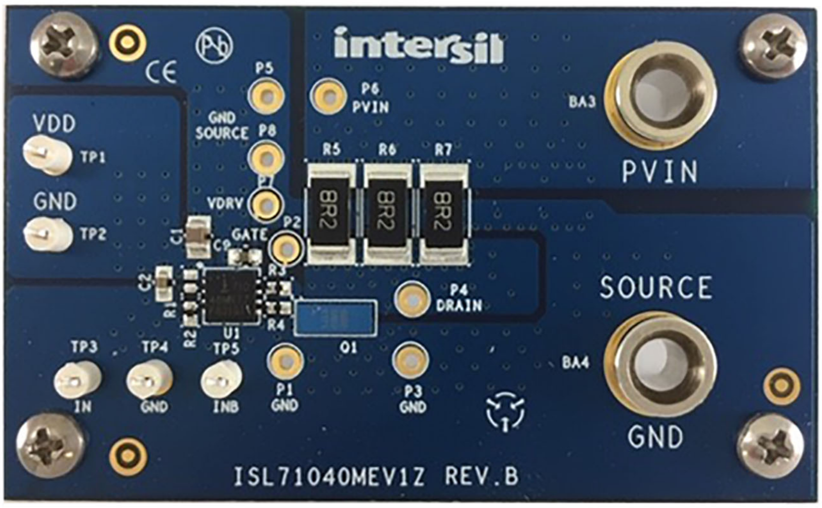

Figure 2. ISL71040MEV1Z Evaluation Board, Top View

Figure 3. ISL71040MEV1Z Evaluation Board, Bottom View

2.2 ISL71040MEV1Z Schematic Diagram

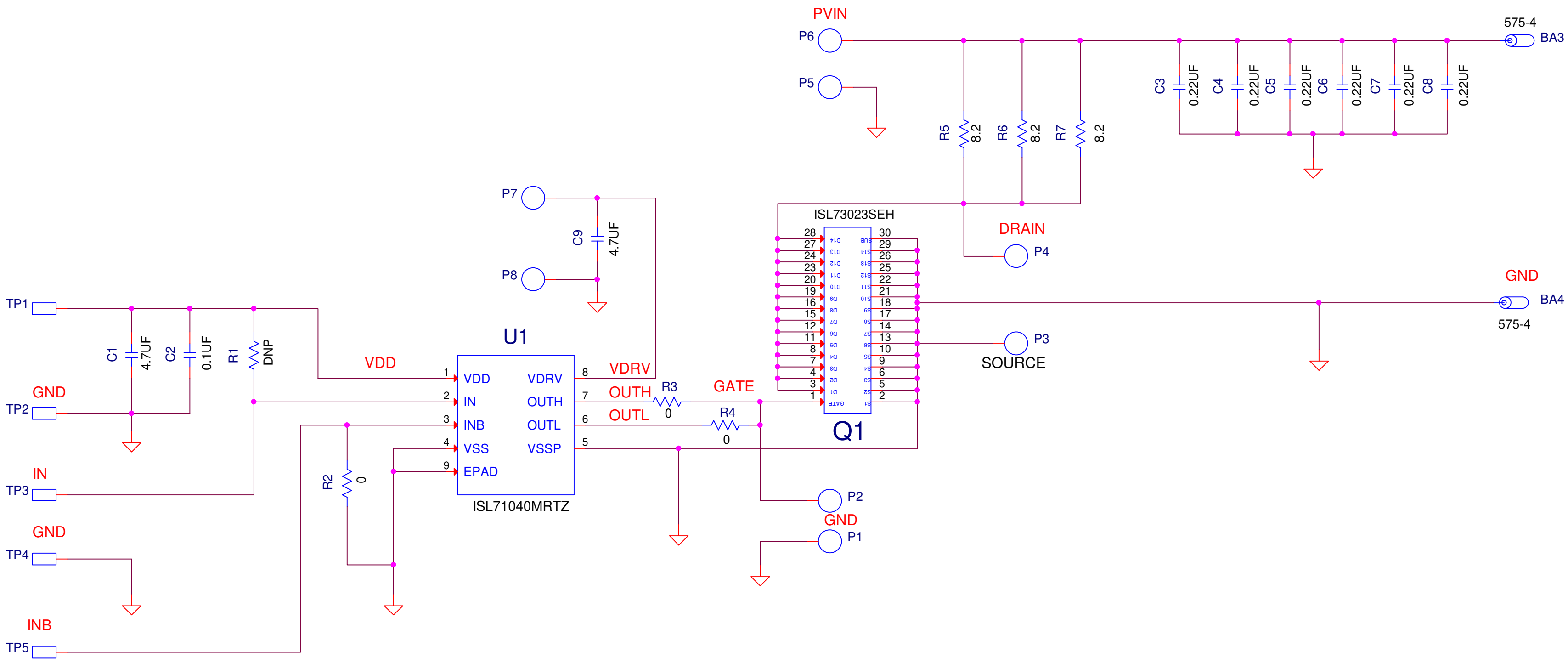

Figure 4. ISL71040MEV1Z Schematic

2.3 Bill of Materials

Table 2. Components Parts List

Qty	Reference Designator	Description	Manufacturer	Part Number
3	R5, R6, R7	Surface Mount Power Resistor	TE Connectivity	35228R2JT
5	TP1, TP2, TP3, TP4, TP5	Miniature White Test Point 100 Pad 0.040 Thole	KEYSTONE	5002
2	BA3, BA4	Solder Mount Banana Plug	KEYSTONE	575-4
1	C1	Ceramic Chip Capacitor	TDK	CGA4J1X7R1E475K125AC
1	Q1	IC-DIE SAMPLE,RAD HARD 100V GAN FET	Renesas	ISL73023SEHX/SAMPLE
6	C3, C4, C5, C6, C7, C8	Ceramic Chip Cap	MURATA	GRM32DR72E224KW01L
1	C2	Multilayer Cap	GENERIC	H1045-00104-25V10
1	C9	Multilayer Cap	GENERIC	H1045-00475-10V10-T
3	R2, R3, R4	Thick Film Chip Resistor	GENERIC	H2510-00R00-1/16W
1	R1	Thick Film Chip Resistor (Do Not Populate)	GENERIC	H2510-DNP-DNP-1
1	U1	Radiation Tolerant Low-Side GaN FET Driver	Renesas	ISL71040MRTZ

2.4 Board Layout

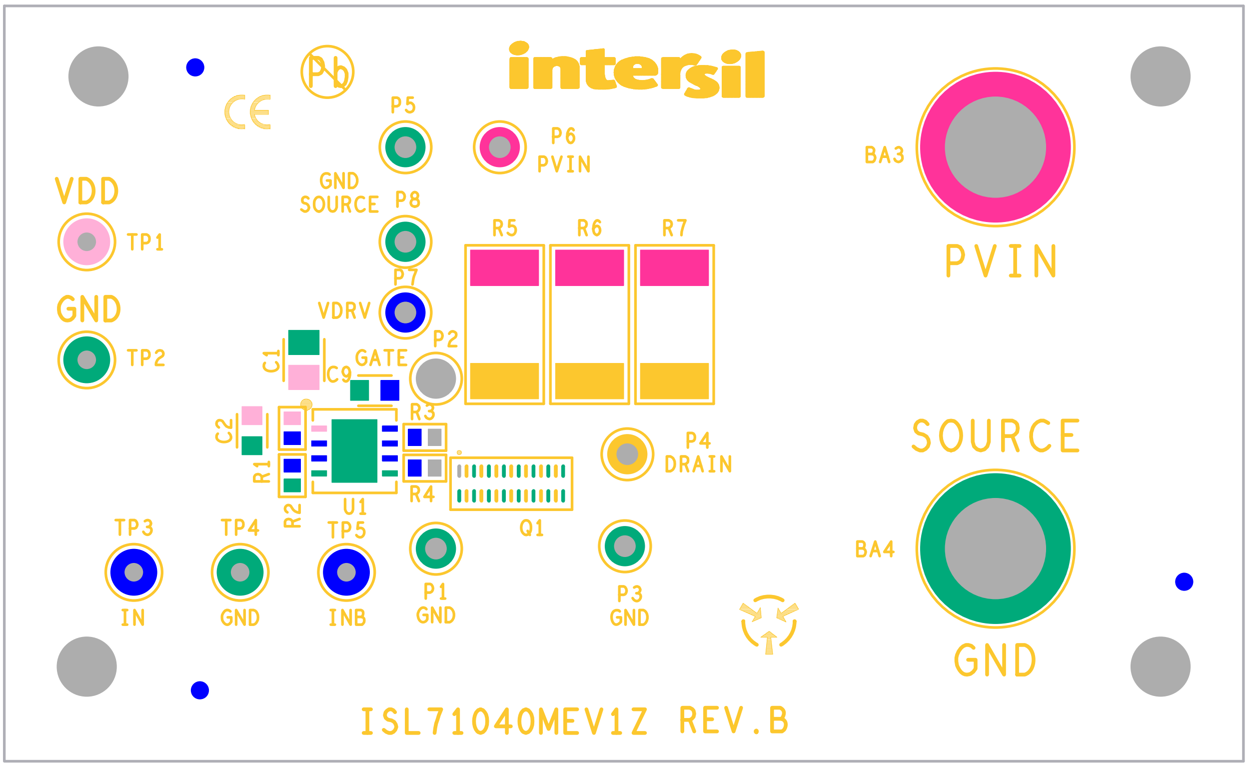

Figure 5. Top Silkscreen

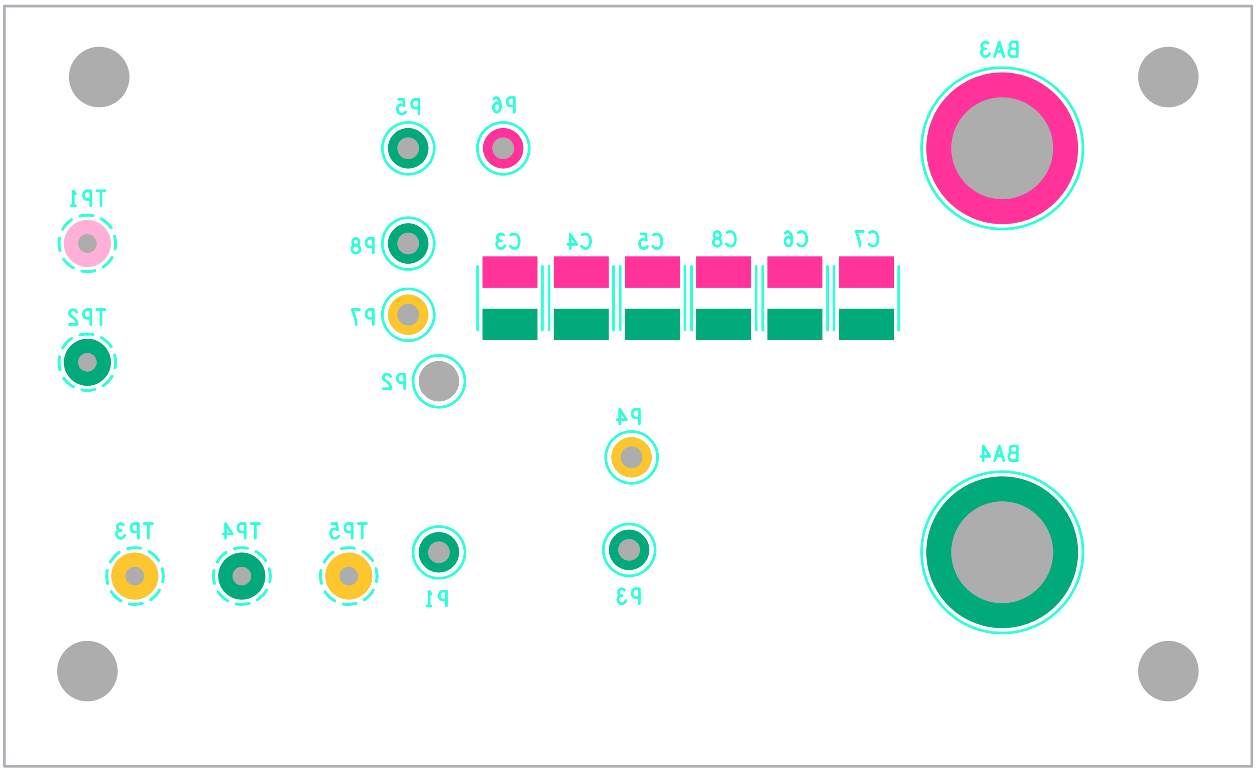

Figure 6. Bottom Silkscreen

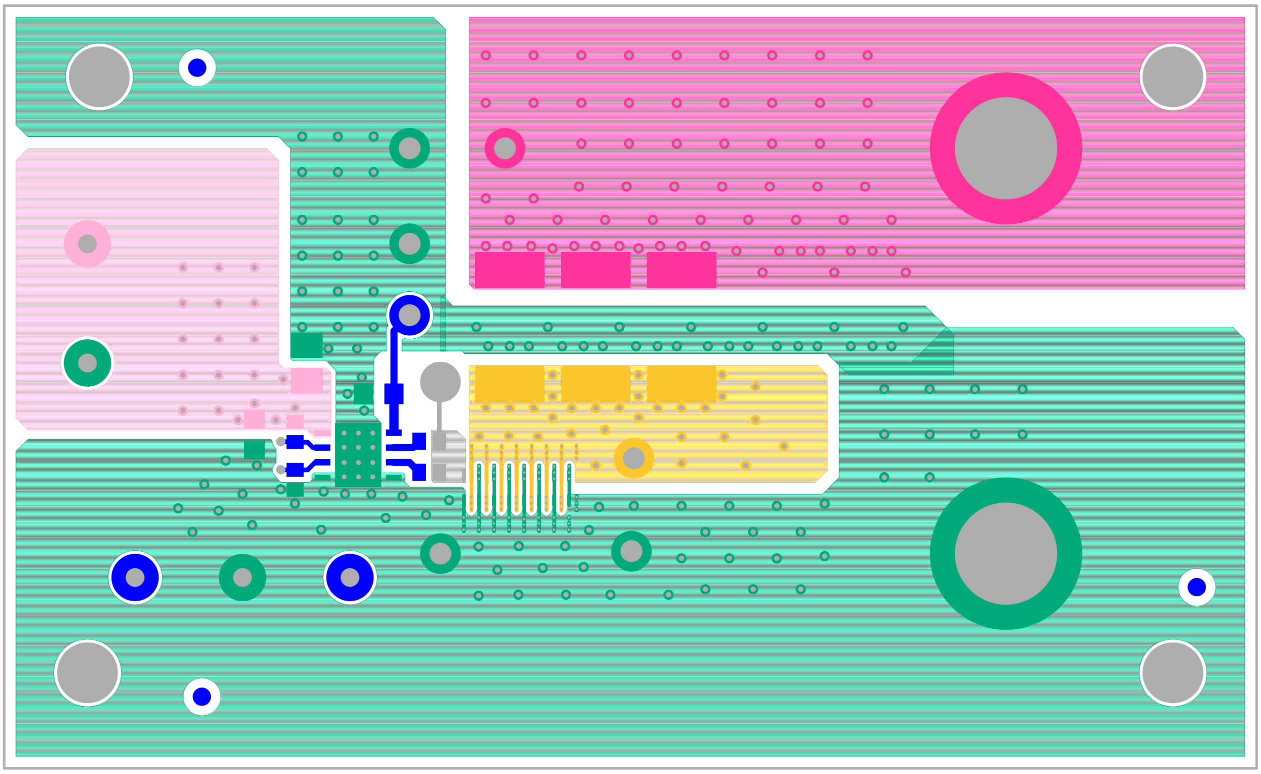

Figure 7. Top Layer

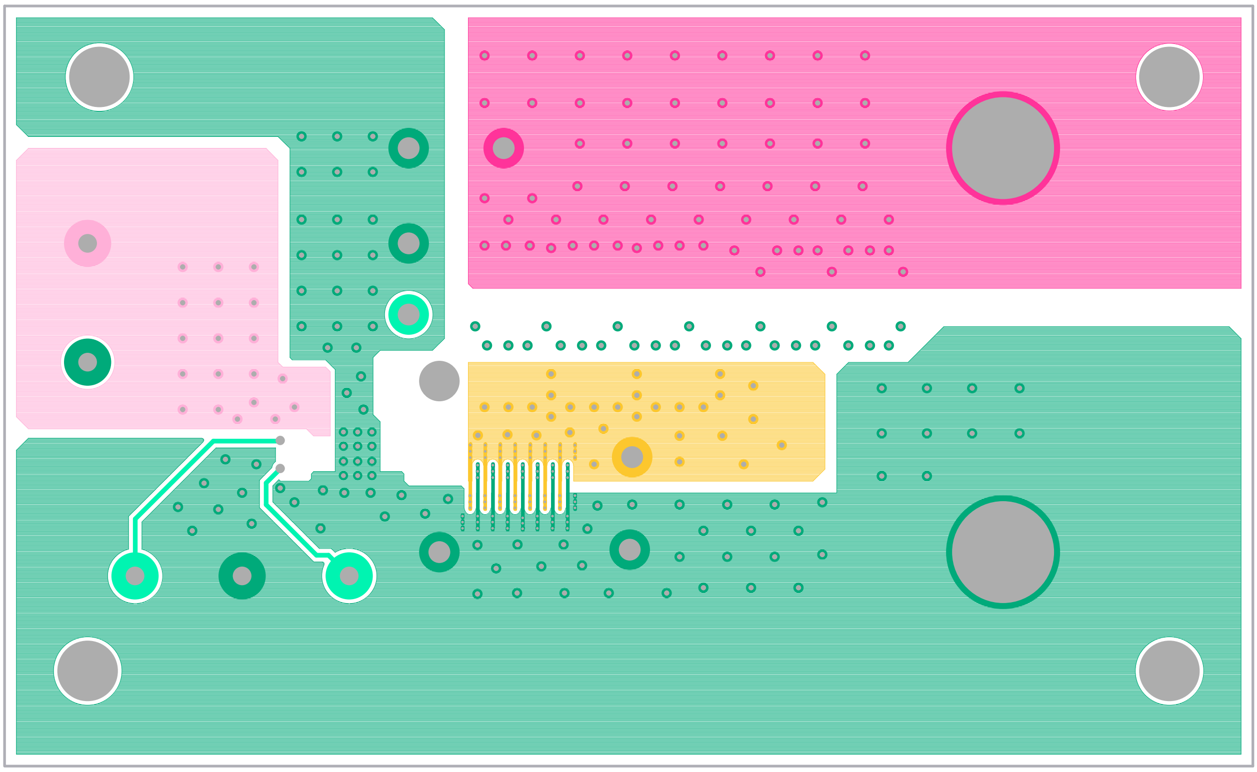

Figure 8. Second Layer

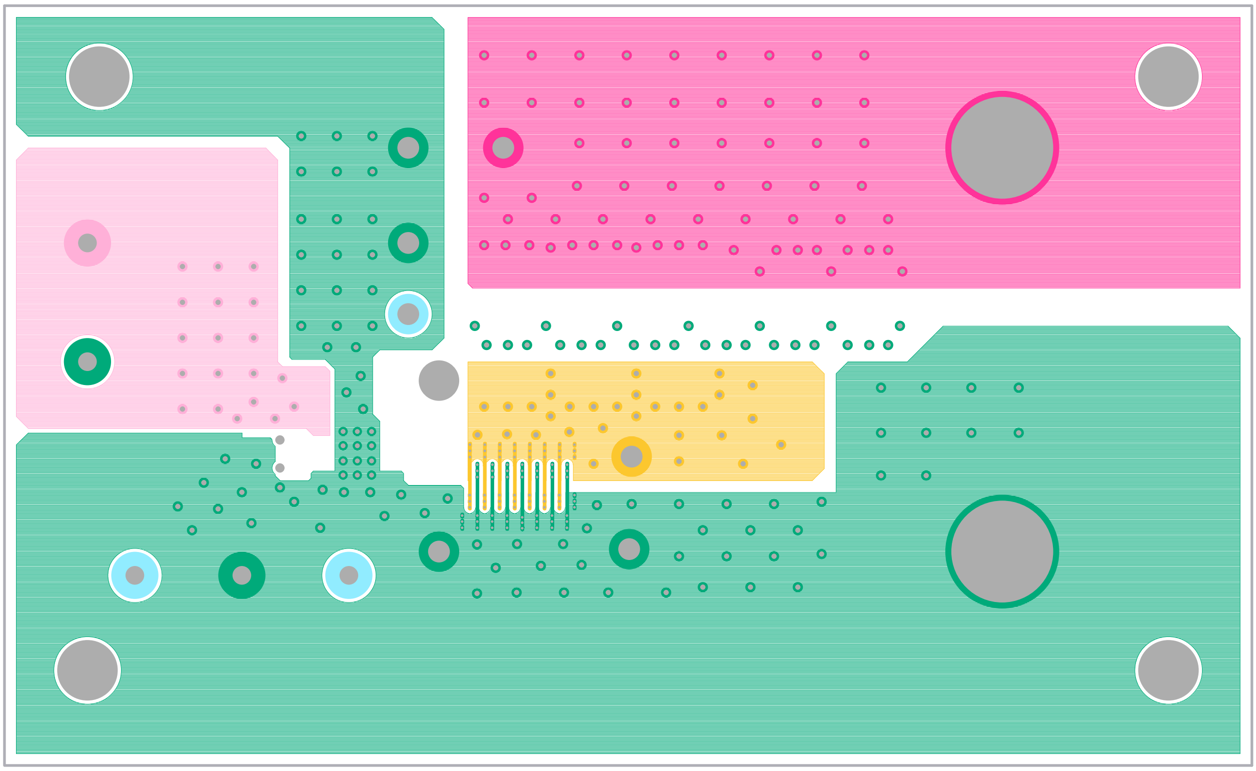

Figure 9. Third Layer

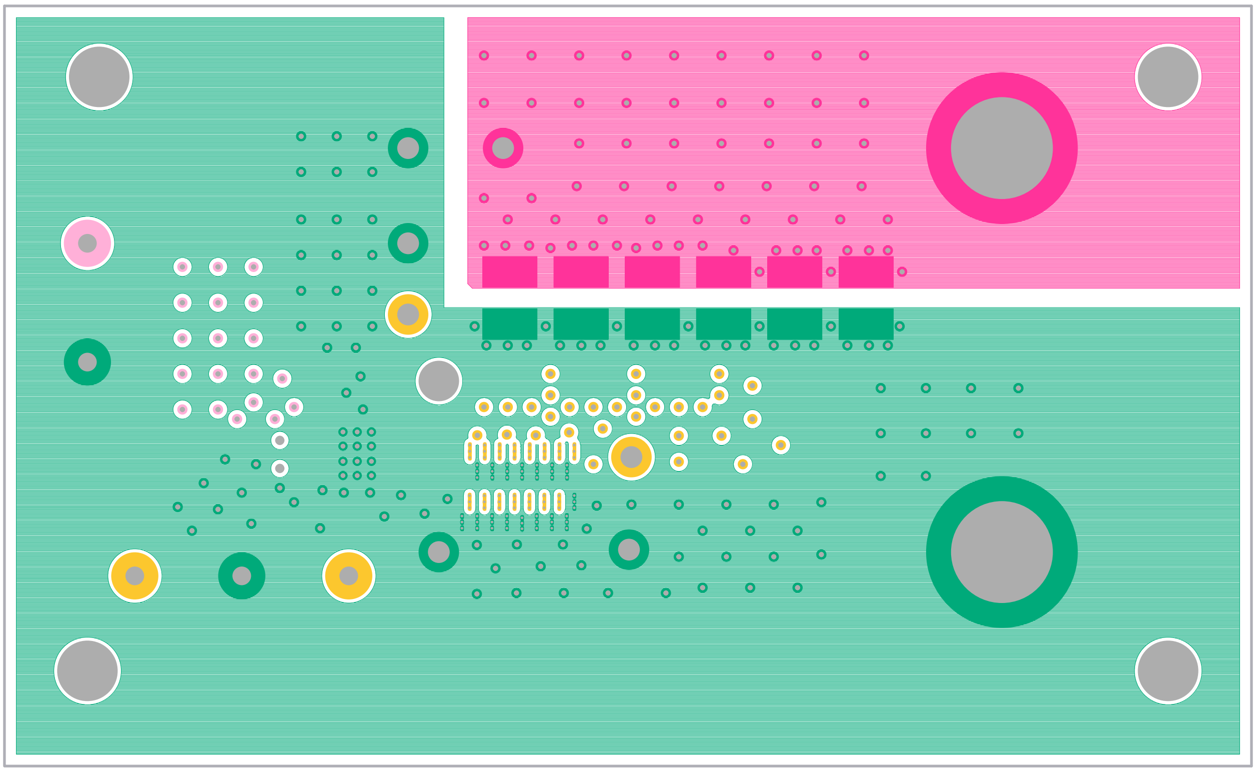

Figure 10. Bottom Layer

3. Typical Performance Curves

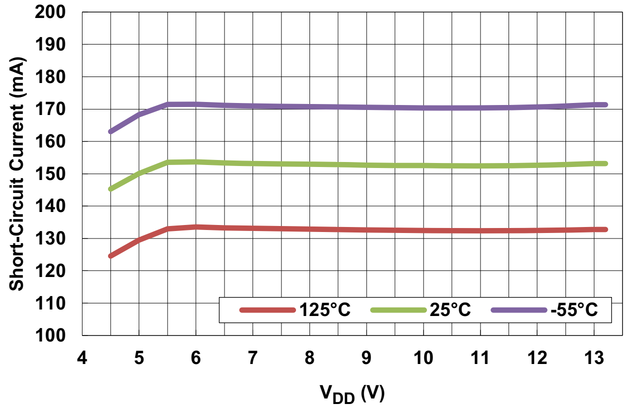

Figure 11. V_{DRV} Short-Circuit Current vs Temperature

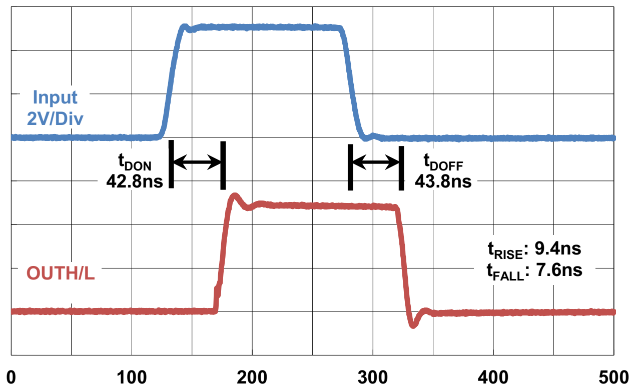

Figure 12. Input Propagation Delay

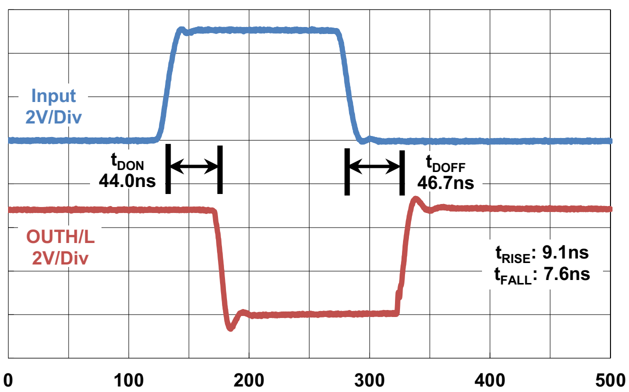

Figure 13. Input Bar Propagation Delay

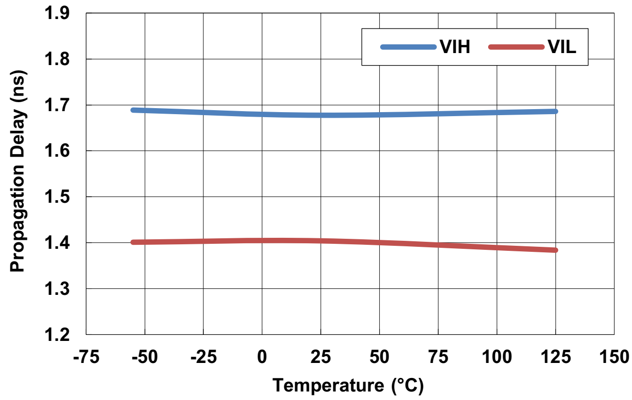

Figure 14. Input Logic Threshold vs Temperature

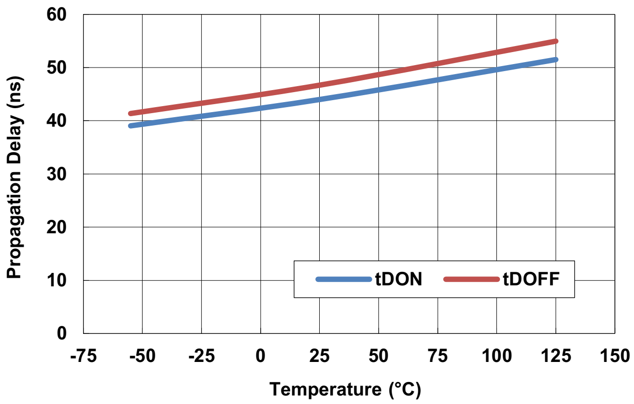

Figure 15. Input Bar Propagation Delay vs Temperature

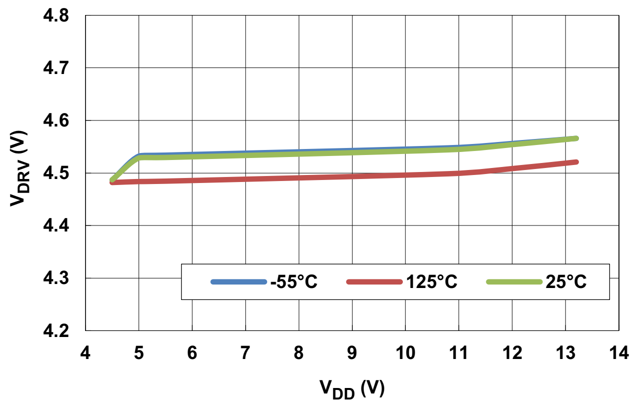

Figure 16. V_{DRV} Line Regulation vs Temperature

4. Revision History

Rev.	Date	Description
2.0	Feb.9.21	Updated BOM, schematic, layout files, and photos to reflect Rev B build.
1.0	Feb.21.19	Initial release

IMPORTANT NOTICE AND DISCLAIMER

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks