

ISL70040SEHEV3Z

User's Manual: Evaluation Board

High Reliability

ISL70040SEHEV3Z

Evaluation Board for the ISL70040SEH and ISL70024SEH

UG146
Rev.0.00
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1. Overview

The ISL70040SEHEV3Z evaluation platform is designed to evaluate the [ISL70040SEH](#) alongside the [ISL70024SEH](#). The ISL70040SEH is designed to drive enhancement mode Gallium Nitride (GaN) FETs in isolated topologies and boost-type configurations. It operates across a supply range of 4.5V to 13.2V and offers both non-inverting and inverting inputs to satisfy non-inverting and inverting gate drives within a single device. The ISL70040SEH has a 4.5V gate drive voltage (V_{DRV}) that is generated using an internal regulator which prevents the gate voltage from exceeding the maximum gate-source rating of enhancement mode GaN FETs. The gate drive voltage also features an Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB), and keeps OUTL turned on to ensure the GaN FET is in an OFF state whenever V_{DRV} is below the UVLO threshold. The inputs of the ISL70040SEH can withstand voltages up to 14.7V regardless of the VDD voltage. This allows the inputs of the ISL70040SEH to be connected directly to most PWM controllers. The split outputs of the ISL70040SEH offer the flexibility to adjust the turn-on and turn-off speed independently by adding additional impedance the turn-on/off paths.

The ISL70024SEH is a 200V N-channel enhancement mode GaN power transistor. GaN's exceptionally high electron mobility and low temperature coefficient allows for very low $r_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can operate at a higher switching frequency with more efficiency while reducing the overall solution size.

1.1 Key Features

- Wide V_{DD} range single
 - 4.5V to 13.2V
- Location provided for load resistors to switch the GaN FET with a load
- SMA connector on the gate drive voltage to analyze the gate waveforms
- Drain/Source sense test points to analyze the drain to source waveforms
- Banana jack connectors for power supplies and drain/source connections

1.2 Specifications

- V_{DD} range: 4.5V to 13.2V

1.3 Ordering Information

Part Number	Description
ISL70040SEHEV3Z	ISL70040SEHEV3Z evaluation board

1.4 Related Literature

- For a full list of related documents, visit our website
 - [ISL70040SEH](#) and [ISL70024SEH](#) product pages

2. Functional Description

The ISL70040SEH is a single channel high speed enhanced mode GaN FET low side driver for isolated power supplies and Synchronous Rectifier (SR) applications.

The inputs stage can handle inputs to the 14.7V independent of V_{DD} and offers both inverting and non-inverting inputs. The split output stage is capable of sourcing and sinking high currents and allows for independent tuning of the turn-on and turn-off times. A propagation delay of 36ns, typical, enables high switching frequency operation.

2.1 Operating Range

The ISL70040SEH offers a wide operating supply range of 4.5V to 13.2V. The gate drive voltage is generated from an internal linear regulator to keep the gate-source voltage below the absolute maximum level of 6V for the ISL7002xSEH GaN FET devices.

2.2 Quick Start Guide

- (1) Apply 5.0V to V_{DD} .
- (2) Drive the IN or INB inputs of the driver.
 - (a) To drive INB you'll need to populate R_1 with a 0Ω resistor and remove the 0Ω resistor on R_2 .
- (3) Monitor the gate transition waveforms using SP3.
 - (b) Make sure to use a low capacitance SMA cable because this can reduce the rise/fall times.
 - (c) You can also use a scope probe with a short ground loop soldered to the outside of the SMA connector.
- (4) Monitor the VDS voltage using TP10 and TP11 with a short ground loop connection on a scope probe.
- (5) R_5 , R_6 , and R_7 are provided so that you can switch the FET with a load.
 - (d) $C_3 - C_8$ are provided to counter any cable inductance leading up to J3 and prevent drain-source voltage spikes that can damage the GaN FET.
- (6) SP1 and SP2 are provided to sense the current going through the FET.

2.3 Gate Drive for N-Channel GaN FETs

New technologies based on wide bandgap semiconductors produce High Electron Mobility Transistors (HEMT). Examples of HEMT are the GaN-based power transistors such as the ISL70023SEH and ISL70024SEH, which offer very low $r_{DS(ON)}$ and gate charge (Q_G). These attributes make the devices capable of supporting very high switching frequency operation without suffering significant efficiency loss. However, GaN power FETs have special requirements in terms of gate drive, which the ISL70040SEH was designed to specifically address.

Key properties of a gate driver for GaN FETs are:

- (1) Gate drive signals needs to be sufficiently higher than the V_{GS} threshold specified in GaN FET datasheets for proper operation.
- (2) A well regulated gate drive voltage to keep the V_{GS} lower than specified absolute maximum level of 6V.
- (3) Split pull-up and pull-down gate connections to add series gate resistors to independently adjust turn-on and turn-off speed, without the need of a series diode whose voltage drop may cause an insufficient gate drive voltage.
- (4) Driver pull-down resistance $<0.5\Omega$ to eliminate undesired Miller turn-on.
- (5) High current source/sink capability and low propagation delay to achieve high switching frequency operation.

2.4 Undervoltage Lockout

The V_{DD} pin accepts a recommended supply voltage range of 4.5V to 13.2V and is the input to the internal linear regulator. V_{DRV} is the output of the regulator and is equal to 4.5V. V_{DRV} provides the bias for all internal circuitry and the gate drive voltage for the output stage.

UVLO circuitry monitors the voltage on VDRV and is designed to prevent unexpected glitches when VDD is being turned on or turned off. When $VDRV < \sim 1V$, an internal 500Ω resistor connected between OUTL and ground helps to keep the gate voltage close to ground. When $\sim 1.2V < VDRV < UV$, OUTL is driven low while ignoring the logic inputs, OUTH is in a high impedance state. This low state has the same current sinking capacity as during normal operation. This ensures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates through Miller capacitance.

When $VDRV > UVLO$, the outputs now respond to the logic inputs. In the non-inverting operation (PWM signal applied to IN pin) the output is in phase with the input. In the inverting operation (PWM signal applied to INB pin) the output is out of phase with the input.

For the negative transition of VDD through the UV lockout voltage, the OUTL is active low and OUTH is high impedance when $VDRV < \sim 3.7VDC$, regardless of the input logic states.

2.5 Input Stage

The input thresholds of the ISL70040SEH are based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage. With a typical high threshold of 1.7V and typical low threshold of 1.4V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V and 5V power controllers.

The ISL70040SEH offers both inverting and non-inverting inputs. The state of the output pin is dependent on the bias on both input pins. [Table 1](#) summarizes the inputs to output relation.

Table 1. Truth Table

IN	INB	OUT	OUTH	OUTL
0	0	0	Hi-Z	0
0	1	0	Hi-Z	0
1	0	1	1	Hi-Z
1	1	0	Hi-Z	0

Note: OUT is the combination of OUTH and OUTL connected together. Hi-Z represents a high impedance state.

As a protection mechanism, if any of the input pins are left in a floating condition, OUTL is held in the low state and OUTH is high impedance. This is achieved using a $300k\Omega$ pull-up resistor on the INB to VDD and a $300k\Omega$ pull-down resistor on the IN pin to VSS. For proper operation in non-inverting applications, INB should be connected to VSS. Inversely, for inverting applications, IN should be connected to VDD for proper operation.

2.6 Enable Function

An enable or disable function can be easily implemented in ISL70040SEH using the unused input pin. Follow the recommendations below to implement an enable/disable function:

- In a non-inverting configuration, the INB pin can be used to implement the enable/disable function. OUT is enabled when INB is biased low, acting as an active low enable pin.
- In an inverting configuration, the IN pin can be used to implement the enable and disable function. OUT is enabled when IN is biased high, acting as an active high enable pin.

2.7 Driver Power Dissipation

The power dissipation of the ISL70040SEH is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation but is usually not significant as compared to the gate charge losses.

For example, the ISL70024SEH has a total gate charge of 5nC when $V_{DS} = 100V$ and $V_{GS} = 4.5V$. This is the charge that a driver must source to turn on the GaN FET and must sink to turn off the GaN FET.

[Equation 1](#) shows calculating the power dissipation of the driver:

$$(EQ. 1) \quad P_D = 2 \cdot Q_c \cdot \text{freq} \cdot V_{GS} \cdot \frac{R_{gate}}{R_{gate} + r_{DS(ON)}} + I_{DD}(\text{freq}) \cdot V_{DD}$$

where:

freq = Switching frequency

$V_{GS} = V_{DRV}$ bias of the ISL70040SEH

Q_c = Gate charge for V_{GS}

$I_{DD}(\text{freq})$ = Bias current at the switching frequency

$r_{DS(ON)}$ = ON-resistance of the driver

R_{gate} = External gate resistance (if any).

Note that the gate power dissipation is proportionally shared with the external gate resistor. Do not overlook the power dissipated by the external gate resistor.

3. General PCB Layout Guidelines

The AC performance of the ISL70040SEH depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt will induce currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. The noise, magnetically induced on a 10k Ω resistor, is 10x larger than the noise on a 1k Ω resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the V_{DRV} , V_{DD} , and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits especially on OUTH. If an external gate resistor is unacceptable, then the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL70040SEH.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. This will inject di/dt currents into the signal ground paths.
- Do the power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built-in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic caps, power resistors, etc.) will have internal parasitic inductance which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components especially parasitic inductance.
- The GaN FETs have a separate substrate connection which is internally tied to the source pin. Source and substrate should be at the same potential. Limit the inductance in the OUTH/L to Gate trace by keeping it as short and thick as possible.

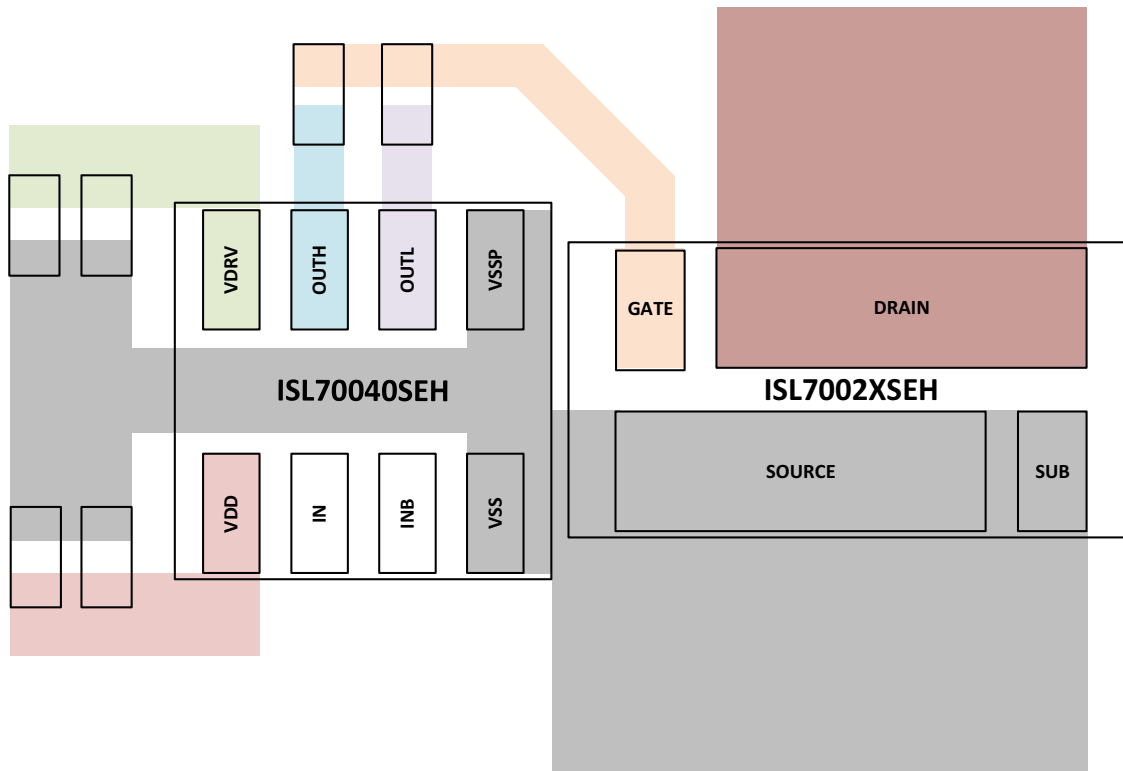


Figure 1. PCB Layout Recommendation

4. ISL70040SEHEV3Z Evaluation Board



Figure 2. ISL70040SEHEV3Z Evaluation Board, Top View



Figure 3. ISL70040SEHEV3Z Evaluation Board, Bottom View

4.1 ISL70040SEHEV3Z Schematic Diagram

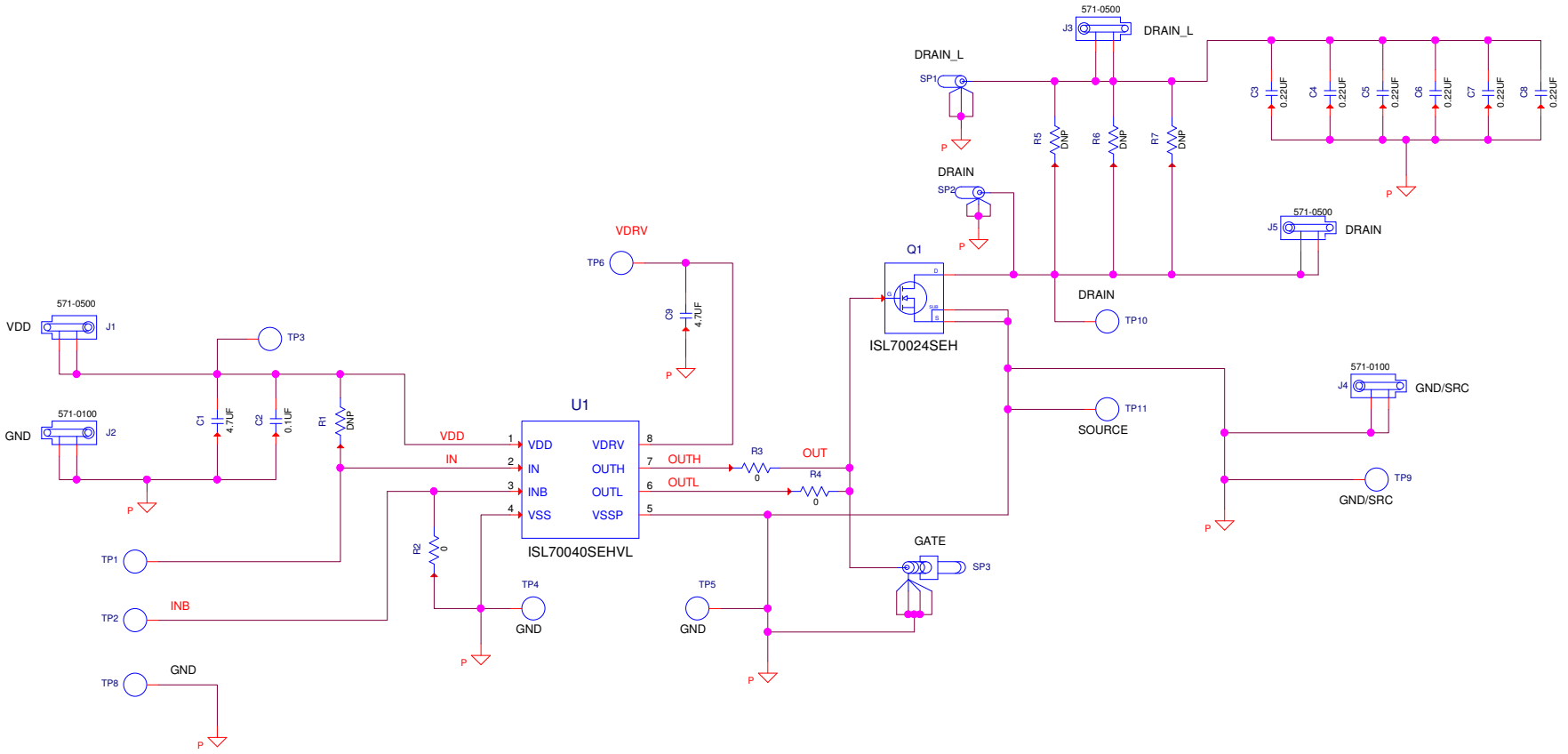


Figure 4. ISL70040SEHEV3Z Schematic

4.2 Bill of Materials

Qty	Reference Designator	Description	Mfr.	Manufacturer Part Number
2	SP1, SP2	Scope Probe Test Point PCB Mount	TEKTRONIX	131-4353-00
8	TP1-TP6, TP8, TP9	Miniature White Test Point 0.100 Pad 0.040 Thole	KEYSTONE	5002
2	J2, J4	10A BLACK Banana Jack Socket Terminal - Female - Horizontal - 4mm Plug	Deltron	571-0100
3	J1, J3, J5	10A BLACK Banana Jack Socket Terminal - Female - Horizontal - 4mm Plug	Deltron	571-0500
1	SP3	Straight SMA PCB Mount Jack	Amphenol	901-144-8RFX
6	C3-C8	Ceramic Chip Cap	Kemet	C1210C224J3GACTU
1	C1	Ceramic Chip Capacitor	TDK	CGA4J1X7R1E475K125AC
1	C2	Multilayer Cap	GENERIC	H1045-00104-25V10
1	C9	Multilayer Cap	GENERIC	H1045-00475-10V10-T
1	R1	Metal Film Chip Resistor (Do Not Populate)	GENERIC	H2505-DNP-DNP-R1
3	R2-R4	Thick Film Chip Resistor	GENERIC	H2511-00R00-1/10W1
3	R5-R7	Thick Film Chip Resistor (Do Not Populate)	GENERIC	H2515-DNP-DNP-1
1	Q1	200V 8.5A Enhancement Mode GaN Power Transistor	INTERSIL	ISL70024SEH
1	U1	Radiation Tolerant Single Low Side GaN FET Driver	INTERSIL	ISL70040SEHVL
2	TP10, TP11	0.086 Pad with 0.046 Plated Thru Hole	GENERIC	PAD_86C_46P-DNP

4.3 Board Layout

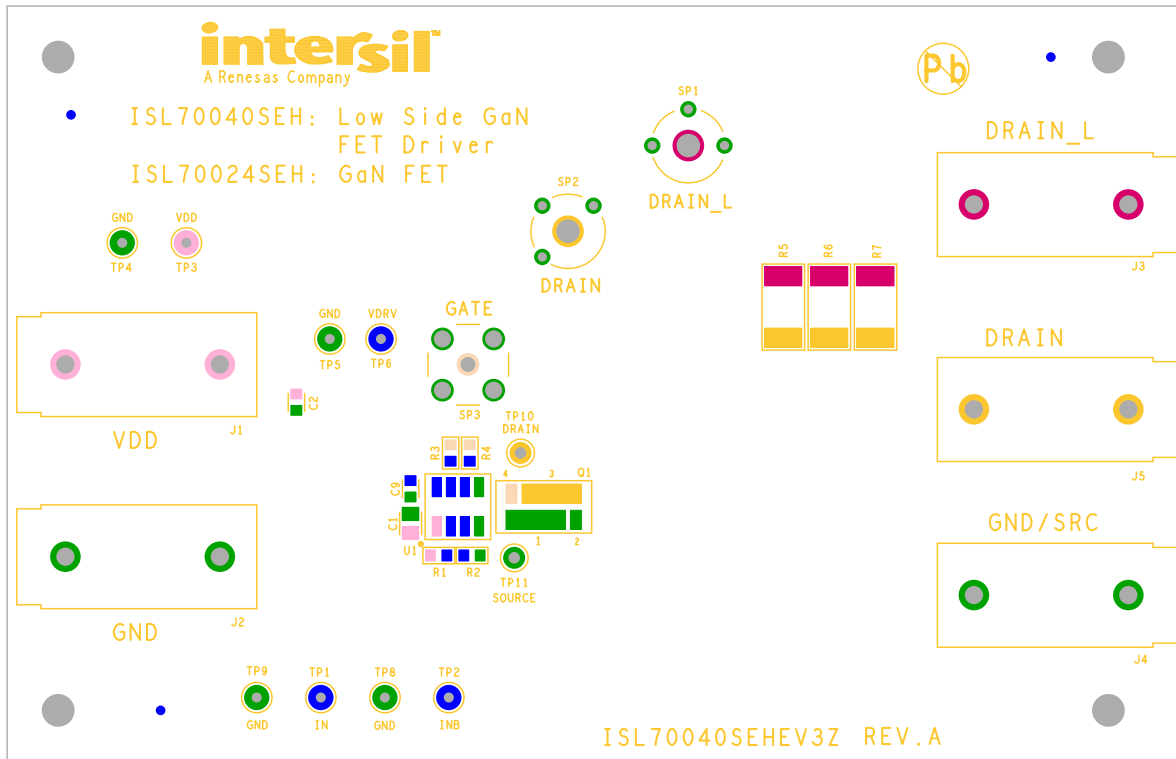


Figure 5. Top Silkscreen

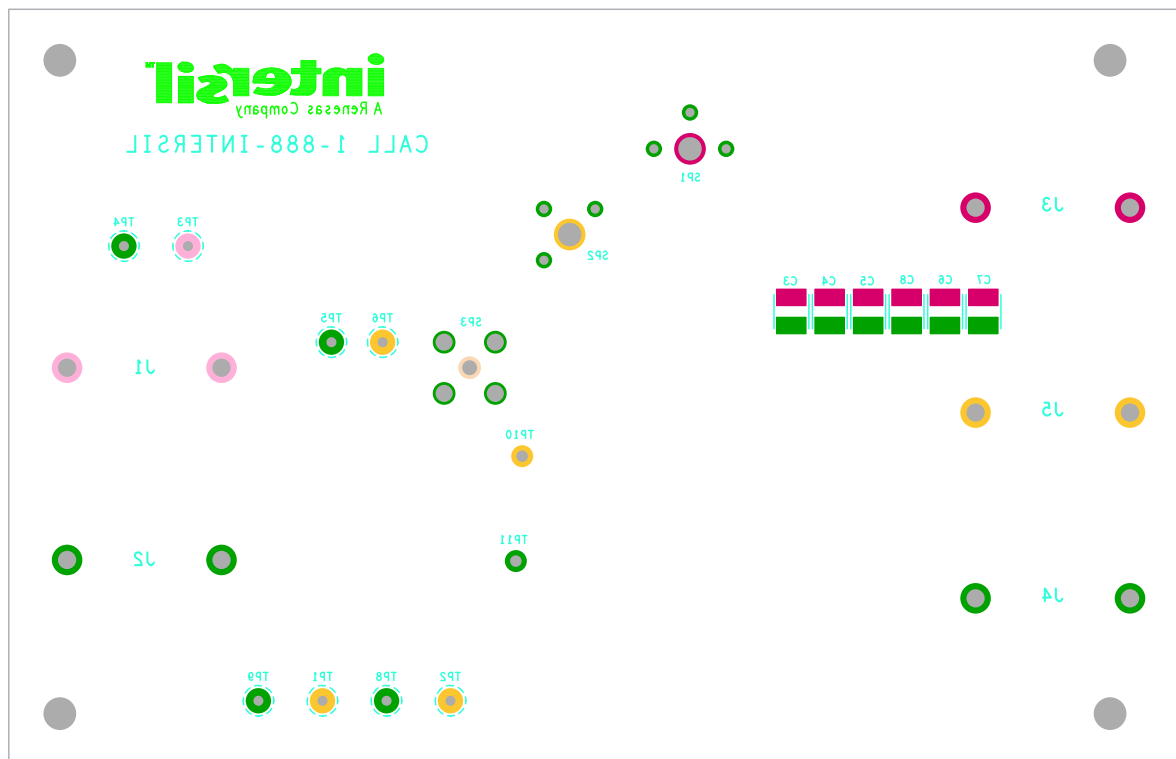


Figure 6. Bottom Silk Screen

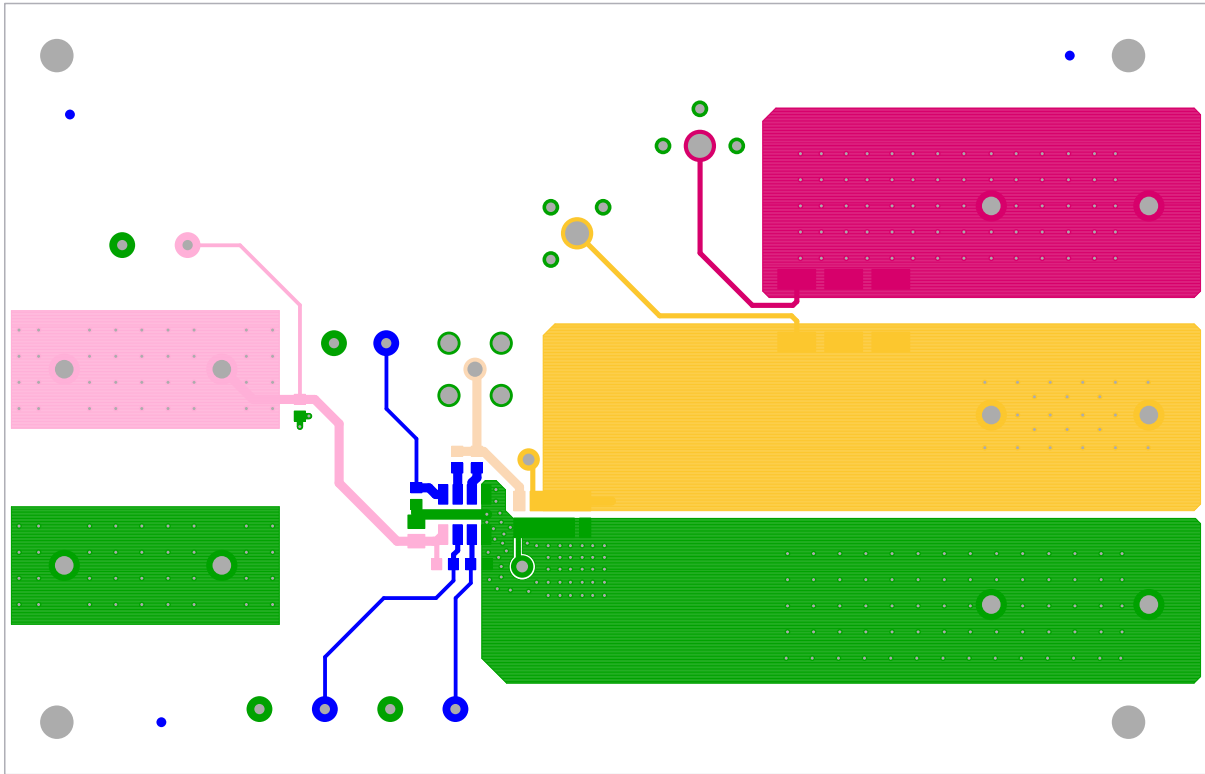


Figure 7. Top Layer

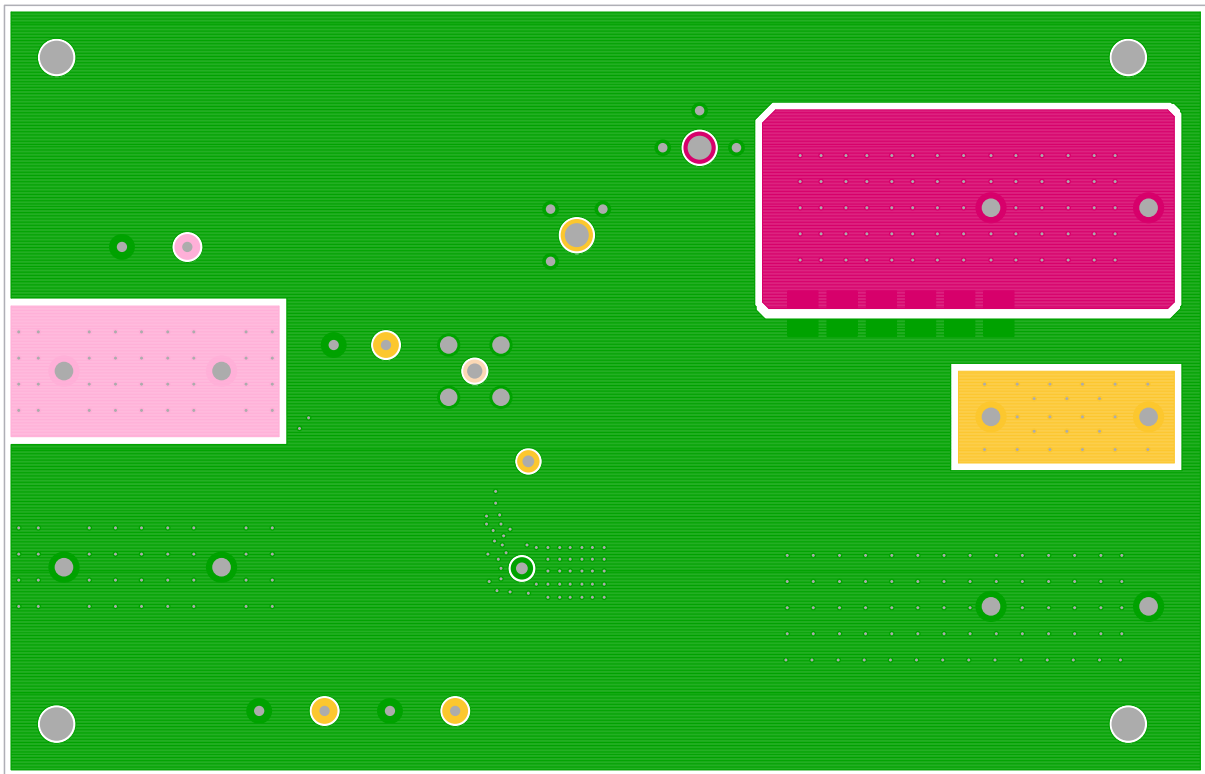


Figure 8. Bottom Layer

5. Typical Performance Curves

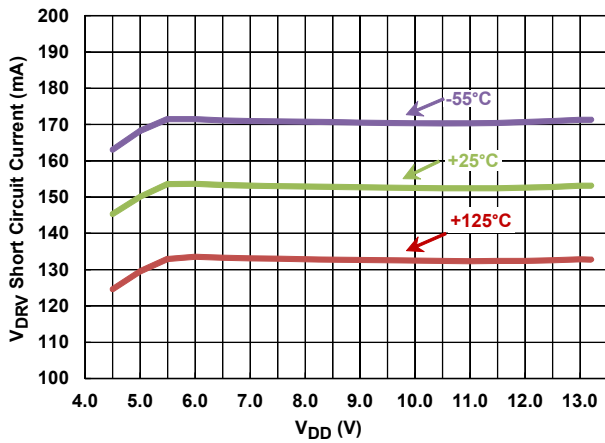


Figure 9. V_{DRV} Short-Circuit Current vs Temperature

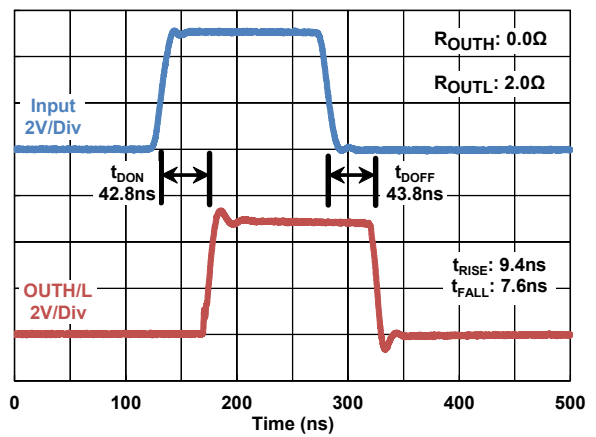


Figure 10. Input Propagation Delay

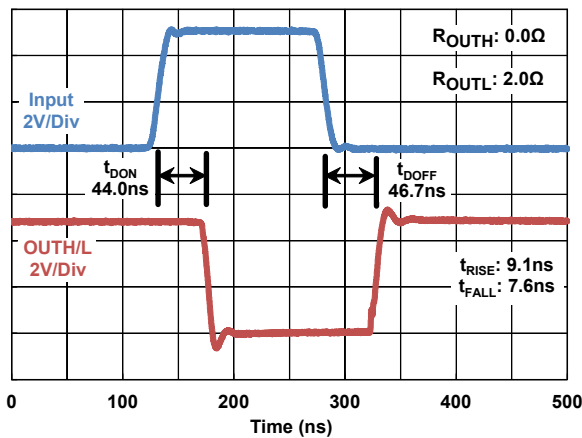


Figure 11. Input Bar Propagation Delay

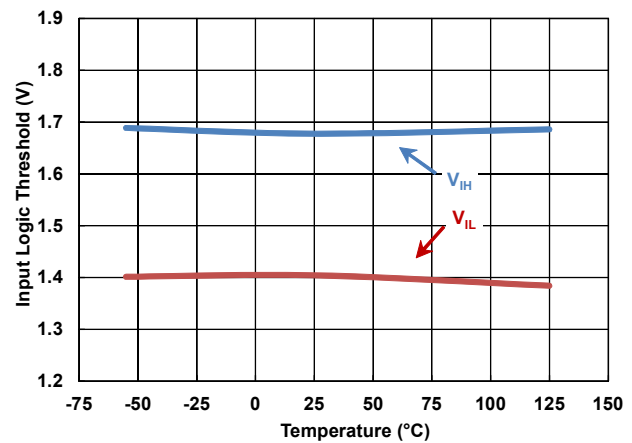


Figure 12. Input Logic Threshold vs Temperature

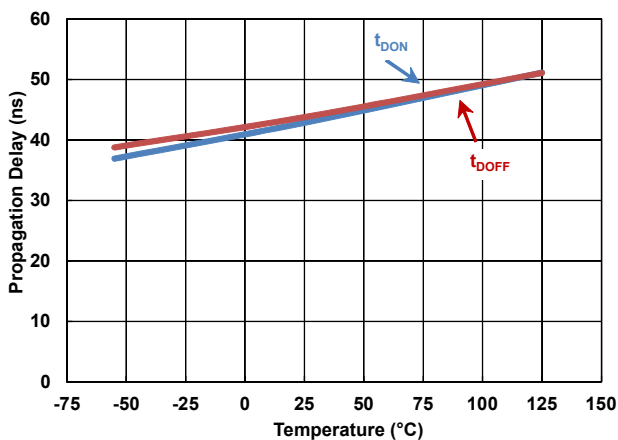


Figure 13. Input Propagation Delay vs Temperature

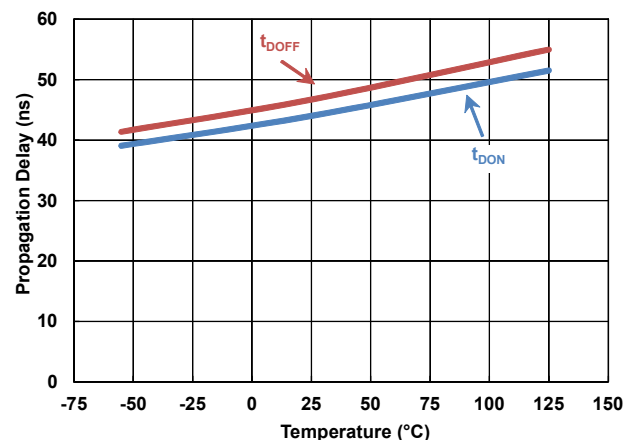


Figure 14. Input Bar Propagation Delay vs Temperature

6. Revision History

Rev.	Date	Description
0.00	Nov 29, 2017	Initial release

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