High Reliability
1. Overview

The ISL70002SEHDEMO1Z demonstration board shows the ISL70002SEH in a dual current sharing configuration to 38A of output current.

1.1 Key Features

- Ease of use
- Critical monitor points
- Commercial version of NASA outgassing compliant power inductor

1.2 Specifications

- $V_{IN} = 3V$ to $5.5V$
- $V_{OUT} = 0.95V$
- Minimum current limit = 43A
- Switching frequency = $500kHz$

1.3 Ordering Information

<table>
<thead>
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<th>Part Number</th>
<th>Description</th>
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<tr>
<td>ISL70002SEHDEMO1Z</td>
<td>ISL70002SEH dual high current demonstration board</td>
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1.4 Related Literature

For a full list of related documents, visit our website

- ISL70002SEH product page

Figure 1. ISL70002SEHDEMO1Z Block Diagram
2. Functional Description

The ISL70002SEHDEMO1Z provides a 0.95V output from a 3V to 5.5V input with an output current load up to 38A. The two ISL70002SEH devices on board are in a current sharing configuration. They are set to enable upon VIN being applied and PORSEL pulled low. Switching typically starts at a VIN of 2.8V.

2.1 Operating Range

Although rated across the full military ambient temperature range, factors that influence the operational envelope include input and output voltages, switching frequency, output current, and die temperature.

The ISL70002SEHDEMO1Z is default configured to provide an output voltage of 0.95V, with a 500kHz switching frequency. To change the output voltage, R20 in the output voltage divider has to be changed. As guidance, the output voltage range is adjustable from ~0.65V to ~80% of the input voltage. These are not hard stops on the operating envelope as the constraint is set by the minimum on and off time and influenced by temperature and current loading.

2.2 Quick Start Guide

The ISL70002SEHDEMO1Z is simple to use with a minimum of steps listed below to observe operation:

1. Connect a suitable power supply to the VIN connector, set the supply between 3V and 5.5V. Account for voltage drop to ensure adequate bias is applied at full load. Test points are provided to measure closer to the IC PVIN, inductor output and ground pins.

2. Connect an electronic or resistive load to the output. Configure the output current loading to not exceed 40A.

3. Turn-on the input voltage, confirm the output voltage is 0.95V.

4. Three probe jacks are provided to observe the two LX nodes switching out of sync with each other, and for the output voltage.

The information displayed in the Typical Performance Curves starting on page 11 was gathered on the ISL70002SEHDEMO1Z. Modifications were made for some of the testing and thus cannot be replicated without additional effort. Modifications were limited to the addition of circuit access points and or component changes.

The case temperature efficiency data in Figures 15, 16, and 31 through 43 was taken with the board immersed in a turbulent liquid environment to control the package temperature. Efficiency curves are at the noted case temperatures (T_C).

The inductors used are the Coilcraft XAL1580-102MEB, a commercial version of the AE619PYA102MSZ (1µH, 1mΩ, 73A), a NASA outgassing compliant power inductor. Oversized current is advisable for this application and it is a readily available standard product.
3. PCB Layout Guidelines

Printed Circuit Board (PCB) layout is very important in high frequency switching converter design. The resulting current transitions from one power device to another can cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and PCB design minimizes these voltage spikes. The following guidelines can mitigate those effects:

- Use an eight layer PCB with 2oz (70µm) copper on all layers.

- Two layers should be dedicated for ground plane.

- Top and bottom layers should be used primarily for signals, but can also be used to increase the V\text{IN}, V\text{OUT}, and ground planes as required.

- Connect all AGND, DGND, and PGND\text{x} pins directly to the ground plane. Connect all PVIN\text{x} pins directly to the VIN portion of the power plane.

- Locate ceramic bypass capacitors as close as possible to the switcher. Prioritize the placement of the bypass capacitors on the pins of in the order shown: PVIN\text{x}, REF, AVDD, DVDD, SS, EN, PGOOD.

- Locate the output voltage resistive divider and the compensation as close as possible to the FB and VERR pins of the IC. The top leg of the divider should connect directly to the load and the bottom leg of the resistive divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.

- Use a small island of copper to connect the LX\text{x} pins of U1 to the inductor, L1, to minimize the routing capacitance that degrades efficiency. Separate the island from ground and power planes as much as is reasonably possible with inner layer voiding and shape spacing.

- Keep all signal traces as short as possible.

- Optimize load regulation by reducing noise from the power and digital grounds into the analog ground by splitting ground into three planes; analog, digital, and power. Bypass or ground pins accordingly to their design preferred ground plane. Independently tie each of the analog and digital grounds to power ground through a single trace in a low noise area of the layout.

3.1 Heatsink Mounting Guidelines

The R64.C package has a heatsink mounted on the underside of the package and is the recommended package for the high current (>12A per IC) application. Follow these JESD-51x series guidelines to mount the package:

- Place a thermal land on the PCB under the heatsink.

- The land should be approximately 1mm larger per side than the 10.16x10.16mm heatsink.

- Place an array of thermal vias below the thermal land.

- Via array size: 7x4 = 49 thermal vias placed under each device.

- Vias should drop to and contact as much metal area on other layers as feasible to provide the best thermal path.

3.2 Schottky Diode Clamp and RC Snubber

Place a Schottky diode clamp at the LX node to GND as close as possible to the IC when the output current is 18A or greater per IC. A diode rated for an average forward current of 3A at the maximum operating temperature is adequate.

The diode, by shunting current at the switching transient edges, reduces the Si die temperature approximately 22% at an output current level of 18A.

It is imperative that adequate thermal relief in the hardware design is implemented, because at an output current level of 22A the Si temperature is >135°C with the diode clamp in place at ambient room temperature.

A small series R-C snubber connected from the LX\text{x} pins to the PGND\text{x} pins may be used to damp high-frequency ringing on the LX\text{x} pins.
3.3 ISL70002SEHDEMO1Z Demonstration Board

Figure 2. ISL70002SEHDEMO1Z Demonstration Board (Top)

Figure 3. ISL70002SEHDEMO1Z Demonstration Board (Bottom)
3.4 ISL70002SEHDEMO1Z Circuit Schematic

Figure 4. ISL70002SEHDEMO1Z Schematic
## 3.5 Bill of Materials

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<th>Description</th>
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<td>2</td>
<td>U1, U2</td>
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<td>Renesas</td>
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<td>IHI Connectors</td>
<td>B2C-PCB-HEX</td>
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3.6 Board Layout

Figure 5. Top Layer

Figure 6. Layer 2

Figure 7. Layer 3

Figure 8. Layer 4
Figure 13. Top Silkscreen

Figure 14. Bottom Silkscreen
4. Typical Performance Curves

Unless noted: VIN = 3.3V, VOUT = 0.95V, fSW = 500kHz, TA = +25°C. Efficiency curves are at the noted case temperatures (TC).

**Figure 15.** VIN = 3.3V Over-Temperature Efficiency

**Figure 16.** V_IN = 5V Over-Temperature Efficiency

**Figure 17.** Load Regulation

**Figure 18.** DC Line Regulation

**Figure 19.** 3.3VIN Gain/Phase Bode Plot

**Figure 20.** 5VIN Gain/Phase Bode Plot
Unless noted: $V_{IN} = 3.3V$, $V_{OUT} = 0.95V$, $f_{SW} = 500kHz$, $T_A = +25^\circ C$. Efficiency curves are at the noted case temperatures ($T_C$) (Continued)
Unless noted: \( V_{IN} = 3.3V, V_{OUT} = 0.95V, f_{SW} = 500kHz, T_A = +25^\circ C \). Efficiency curves are at the noted case temperatures (\( T_C \)).

**Figure 27.** Current Share During Turn-On into 38A

**Figure 28.** Current Share During Turn-off

**Figure 29.** Turn-On Soft-Start Detail

**Figure 30.** Case Temperature at 20A

**Figure 31.** 3.3V to 0.8V Over-Temperature Efficiency

**Figure 32.** 5V to 0.8V Over-Temperature Efficiency
Unless noted: $V_{IN} = 3.3V$, $V_{OUT} = 0.95V$, $f_{SW} = 500kHz$, $T_A = +25^\circ C$. Efficiency curves are at the noted case temperatures ($T_C$)

Figure 33. 3.3V to 1V Over-Temperature Efficiency

Figure 34. 5V to 1V Over-Temperature Efficiency

Figure 35. 3.3V to 1.2V Over-Temperature Efficiency

Figure 36. 5V to 1.2V Over-Temperature Efficiency

Figure 37. 3.3V to 1.5V Over-Temperature Efficiency

Figure 38. 5V to 1.5V Over-Temperature Efficiency
Unless noted: $V_{\text{IN}} = 3.3\text{V}, V_{\text{OUT}} = 0.95\text{V}, f_{\text{SW}} = 500\text{kHz}, T_{\text{A}} = +25^\circ\text{C}$. Efficiency curves are at the noted case temperatures ($T_C$). (Continued)
## 5. Revision History

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<td>May 24, 2018</td>
<td>Initial release</td>
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