ISL6334EVAL1Z User Guide

Board Specifications
1. Intel VR11.1 compliant.
2. 4-Phase, 130W, 400kHz, Load Line = 0.8mΩ.
3. Socket: LGA1366, die sensing, can be configured for motherboard sensing.
4. 6 Layer Board: Top/Bottom - 0.5oz plated, 1.5oz finished; Internal Layer – 1oz.
5. Dual footprint for Intersil 12V (ISL6612A, ISL6622) and 5V drivers (ISL6596/ISL6620) for cost or efficiency optimization. With minor re-work, the board can also operate 12V drive for high-side MOSFET and 5V drive for low-side MOSFET.
6. Dual footprint for PowerPak and DPAK MOSFET for cost or efficiency optimization.

ISL6334EVAL1Z Board Brief

Description
Control Power Supply
There are two ways to provide 5VDC to this evaluation board: through ATX power connectors (J21) or Banana connectors (J5 and J0). SW1 is used to control the ATX silver box power supply.

Input Power Supply and External Load Connector
12VDC input power supply can be connected to the board through the 4-pin ATX connector J4. Two test points, TPV1N and TPGND, are provided for input voltage measurement. Two connectors (J1 and J2) are provided for external load.

VR Enable Switch
One switch (SW2) is provided for EN_VTT signal control. In “OFF” position, EN_VTT signal is shorted to ground and ISL6334 is disabled. Place SW2 in the “ON” position to enable operation.

PGOOD Indicator and Test Points
CR2 is used to indicate the status of VR_RDY (PGOOD) signal. When VR_RDY is high, the LED in CR2 will be OFF (no light); otherwise the red LED in CR2 will be on once 5V is applied.

Test points are provided for VR_RDY, IMON, VR_HOT and VR_FAN signals.
VID (Figure 7)
VID code can be generated from Demo board (JP9 = DEMO) or VTT tool (JP9 = VTT).

PSI
Dynamic PSI signal can be generated from LGA1366 VTT or external function generator. Static, fixed PSI operation can be set through SW5. Placing the 0 switch in the "N" position, leads to the circuit operating in PSI mode.

Phase Count Control
R1P, R2P, R3P, RW2, RW3, and RW4 are used to set the phase count, as shown in Table 1. If phase count is different than 4, R1 and R5 must be adjusted accordingly for stability and correct load line.

<table>
<thead>
<tr>
<th></th>
<th>R3P</th>
<th>R2P</th>
<th>R1P</th>
<th>RW4</th>
<th>RW3</th>
<th>RW2</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-Phase</td>
<td>DNP</td>
<td>DNP</td>
<td>DNP</td>
<td>0Ω</td>
<td>0Ω</td>
<td>0Ω</td>
</tr>
<tr>
<td>3-Phase</td>
<td>0Ω</td>
<td>DNP</td>
<td>DNP</td>
<td>0Ω</td>
<td>0Ω</td>
<td>0Ω</td>
</tr>
<tr>
<td>2-Phase</td>
<td>X</td>
<td>0Ω</td>
<td>DNP</td>
<td>DNP</td>
<td>DNP</td>
<td>0Ω</td>
</tr>
<tr>
<td>1-Phase</td>
<td>X</td>
<td>X</td>
<td>0Ω</td>
<td>DNP</td>
<td>DNP</td>
<td>DNP</td>
</tr>
</tbody>
</table>

NOTE: X = Don’t care.

Available Design Assist Tools
1. Layout Check list.
2. VR Design Worksheet.
3. \(V_{\text{CORE}}\) and IMON TOB Calculator.
4. Schematic is available in OrCAD format.
5. Layout is available in Allegro format.

Contact Intersil’s local office or field support for the latest available information.
FIGURE 8. ISL6334 BURNSIDE - 130W REV C BOARD, CONTROLLER CIRCUIT

**Controller circuit**

- **Phase Dropping Decoding**: CI or SI connection
- **Number of Operating Phases Configuration**: 4-PHASE, 3-PHASE, 2-PHASE
- **Placement needs correction**: Placement needs correction
- **Exposure**: Expose these traces on external layers
- **Place this close to the socket**: Place this close to the socket
- ** conexión**: Connection needs correction
- **Close to any current sensing network**: Closeness to current sensing network

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**NOTE**: Droop (R1+R5) and compensation network must be adjusted accordingly.
Follow Intel Burside ATX Layout Guideline for Power Stage and LGA1366 Socket as well as Input Bus Line (1080 pre-preg stackup, 6 layers)

Dual footprint for Si and Ci - Expose Output Inductor Copper

Dual footprint - LPF/ADP for High-side (T1B) and Low-Side (B1T)

Cl: Phase1 (Thermistor) + Phase3; Phase2 + Phase4

Default - 12VUG, LDO+LG. Hardware Options: 12VUG5VLG; LDO=UGLG; 5V DRIVER

Place these hoods on different positions for scope probe ground

FIGURE 9. ISL6334 BURNSIDE - 130W REV C BOARD, POWER STAGE
FIGURE 10. ISL6334 BURNSIDE - 130W REV C BOARD
FIGURE 11. LGA1366 SOCKET PINOUT
ISL6334EVAL1Z Board Layout

FIGURE 12. TOP SILKSCREEN
ISL6334EVAL1Z Board Layout (Continued)

FIGURE 13. TOP COMPONENT SIDE
FIGURE 14. INTERNAL PLANE L2
ISL6334EVAL1Z Board Layout (Continued)

FIGURE 15. INTERNAL ETCH L3
FIGURE 16. INTERNAL ETCH L4
FIGURE 17. INTERNAL PLANE L5
ISL6334EVAL1Z Board Layout (Continued)

FIGURE 18. SOLDER SIDE BOTTOM
ISL6334EVAL1Z Board Layout (Continued)

FIGURE 19. SILKSCREEN BOTTOM

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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