

# Voltage Reference Evaluation Board User's Guide

## Introduction

This evaluation board is designed to evaluate the performance of various precision voltage reference devices. This evaluation board includes pads for 2 different voltage reference ( $V_{REF}$ ) package types: 8 lead SOIC, and 3 lead SOT-23. Only one device type is mounted on the board for evaluation purposes (reference schematic on page 3).

The evaluation board includes voltage input test points ( $V_{IN}$  and GND1) for a power supply input. There are a pair of test points for the output as well ( $V_{OUT}$  and GND2). The common circuitry for each reference includes a jumperable R-C damper network on the  $V_{OUT}$  (LINK6), and the Link4 and Link5 sockets, which accept through-hole style resistors and capacitors for output load testing.

## ISL21090-EVALZ Board

The evaluation board contains the ISL21090 ultra low noise voltage reference (U2), a 10 $\mu$ F input decoupling capacitor (C2), a 1nF compensation capacitor (LINK3), and a 0.1 $\mu$ F load capacitor on the output (LINK4).

The power supply leads attach to the  $V_{IN}$  and GND1 inputs. The input voltage range is from 4.7V to 36V. The ISL21090 has an initial accuracy of 0.02% and a 7 ppm/ $^{\circ}$ C output voltage temperature coefficient. The output is measured at test points TP3 and TP4 ( $V_{OUT}$ , GND2).

The board is capable of accommodating an RC damper network to improve stability by reducing transient load ringing. The damper network is added by populating R1 with a 2.2k $\Omega$  resistor, C3 with a 10 $\mu$ F capacitor, and LINK6 with a shunt.

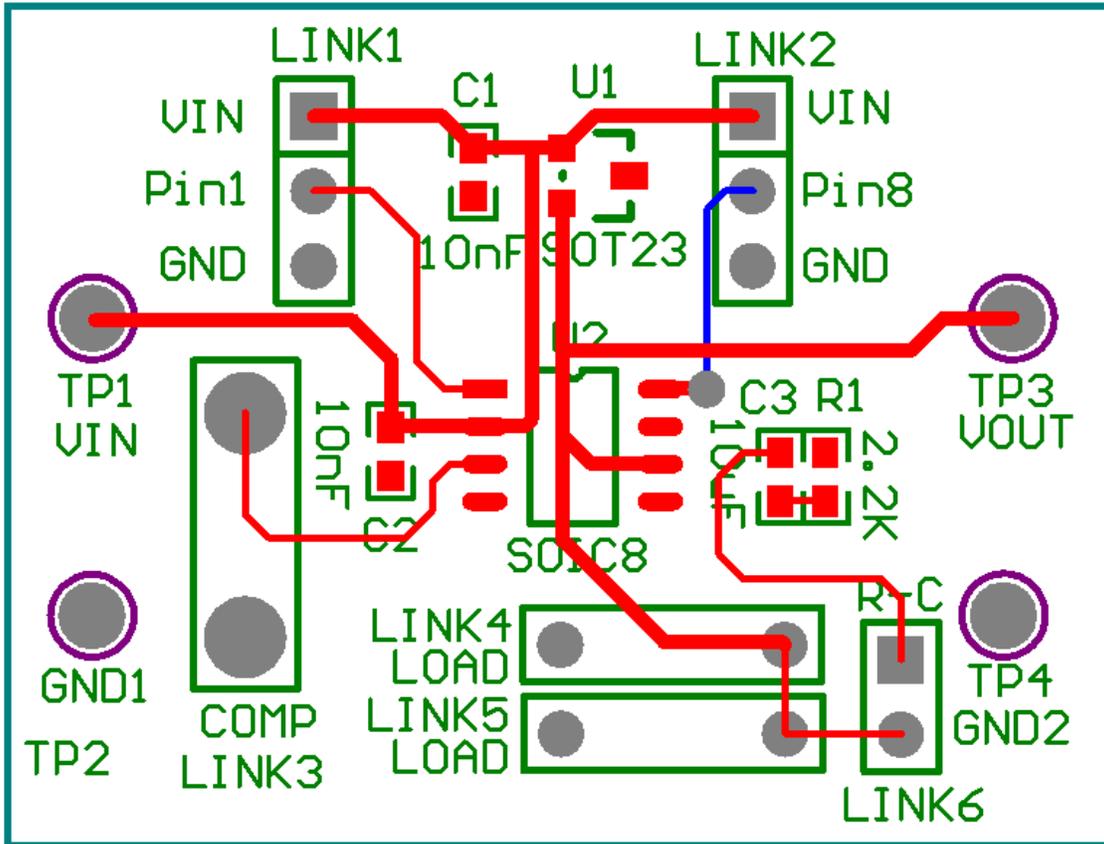


FIGURE 1. VOLTAGE REFERENCE EVALUATION BOARD

## Components on the Board

TABLE 1. COMPONENTS PARTS LIST

DEVICE #	VALUE	DESCRIPTION
<b>VOLTAGE REFERENCE SECTION</b>		
C1	DNP	Bypass Capacitor
C2	10 $\mu$ F	Bypass Capacitor
C3	Open	Optional Damper Capacitor
R1	DNP	Optional Damper Resistor
U1	DNP	SOT-23 3-Pin Package
U2	ISL21090	SOIC 8-Pin Package

TABLE 2. JUMPER LIST

DEVICE #	VALUE	DESCRIPTION
<b>VOLTAGE REFERENCE SECTION</b>		
Link1	DNP	Pin1 state jumper
Link2	DNP	Pin8 state jumper
Link3	1nF	Pin3 compensation capacitor
Link4	0.1 $\mu$ F	Pin6 Load
Link5	Open	Pin6 Load
Link6	Open	R-C Jumper
TP3, TP1, TP2, TP4	VOUT, VIN, GND1, GND2	Test Point

## Voltage Reference Evaluation Board Layout

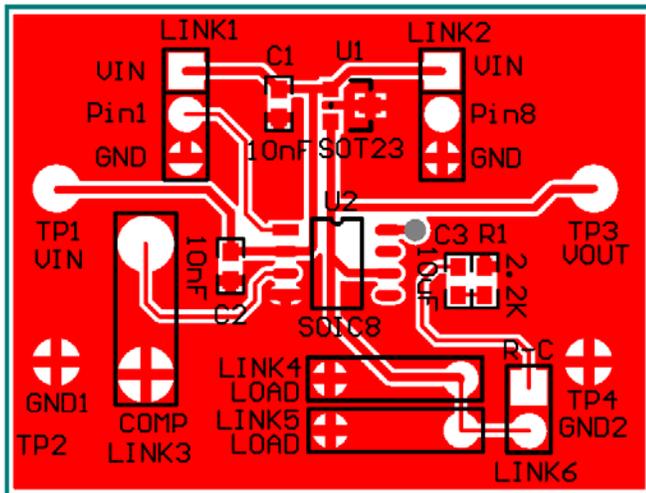


FIGURE 2. TOP COMPONENTS

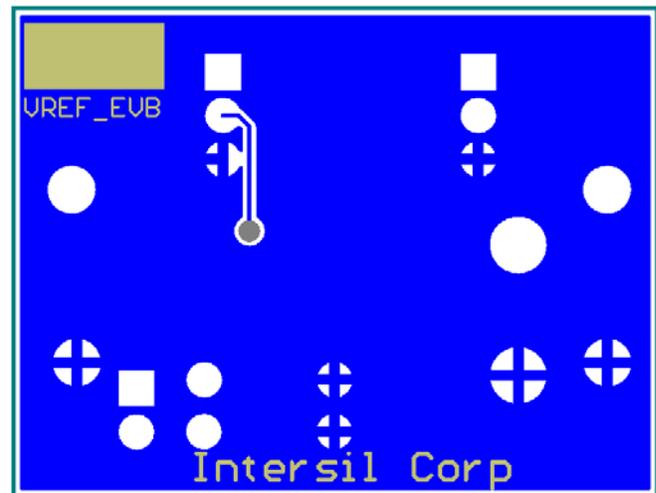


FIGURE 3. BOTTOM LAYER

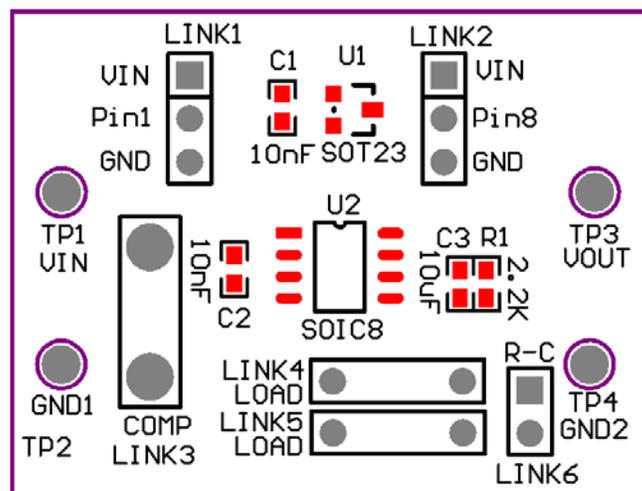


FIGURE 4. ASSEMBLY DRAWING

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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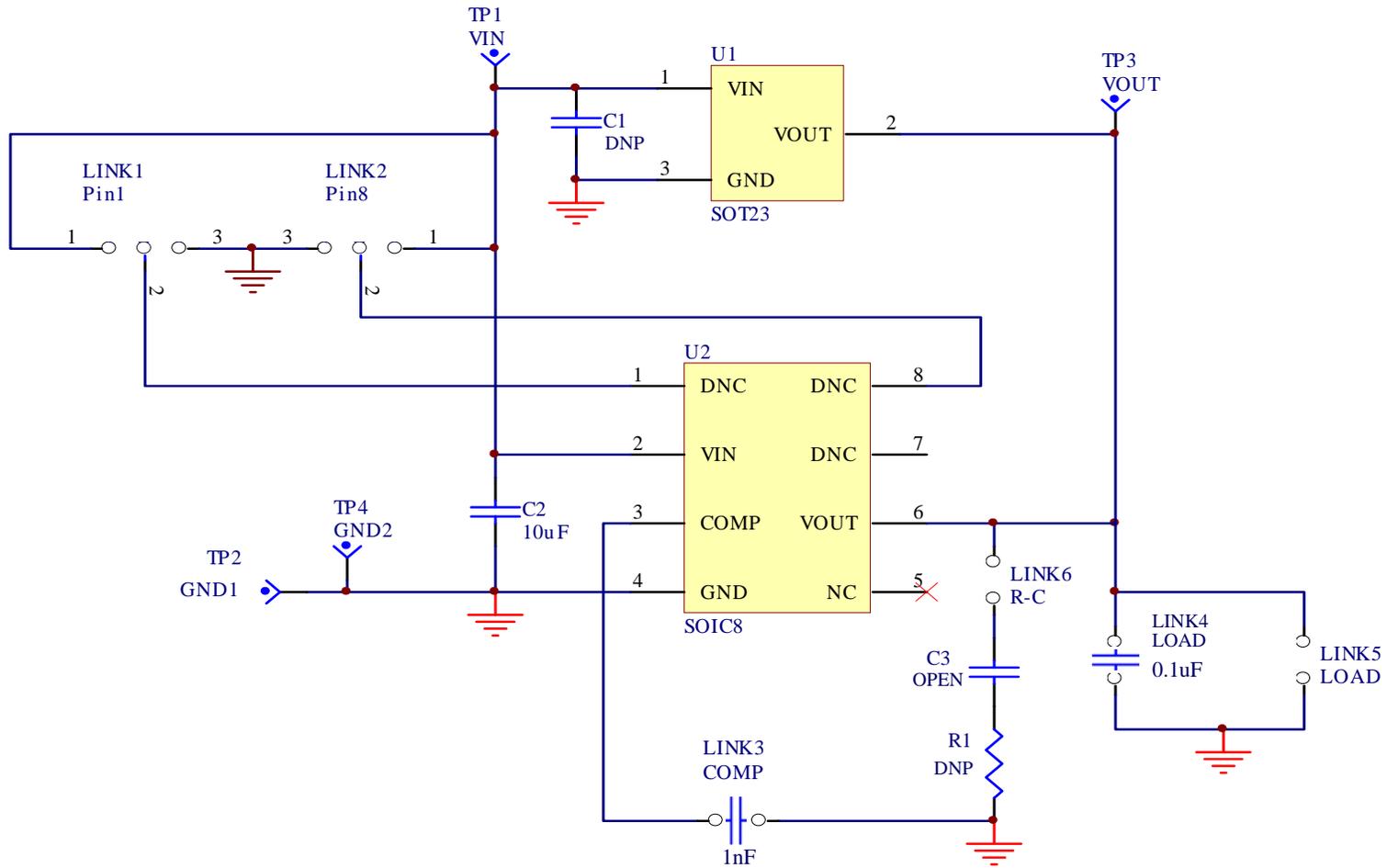


FIGURE 5. SCHEMATIC