NEC

Preliminary User's Manual

IE-78K0-NS-P04
IE-780948-NS-EM4

Emulation Board and Probe Board

for IE-78K0-NS-A

Target device
µPD780948 Subseries

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CE

This equipment complies with the EMC protection requirements.

Warning

This is a ´Class A´ (EN 55022: 1994) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

Caution

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tools including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The In-Circuit Emulator probe target connector plug and/or its adapter pins should not be touched with bare hands.

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- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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Introduction

Product Overview

The IE-78K0-NS-P04 and the IE-780948-NS-EM4, when combined with the IE-78K0-NS-A, is used to debug the following target devices that belong to the 78K/0 Series of 8-bit single-chip microcontrollers.

- µPD780948 Subseries : µPD780948, 78F0948

Target Readers

This manual is intended for engineers who will use the IE-78K0-NS-P04 and the IE-780948-NS-EM4 with the IE-78K0-NS-A to perform system debugging.
Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization

When using the IE-78K0-NS-P04 and the IE-780948-NS-EM4, refer to not only this manual (supplied with the IE-780948-NS-EM4) but also the manual that is supplied with the IE-78K0-NS-A.

IE-78K0-NS-A User's Manual	**IE-78K0-NS-P04 IE-780948-NS-EM4 User's Manual**
· Basic specifications · System configuration · Part names · External interface functions	· General · Parts names · Installation · Differences between target devices and target interface circuits

Purpose

This manual's purpose is to explain various debugging functions that can be performed when using the IE-78K0-NS-P04 and the IE-780948-NS-EM4.

Terminology

The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is a device (a PD780948 Subseries chip) that is the target for emulation.
Target system	This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K0-NS-A, the IE-78K0-NS-P04 and the IE-780948-NS-EM4.

Conventions Data significance weight : Higher digits on the left and lower digits on the right

Note : Footnote for item marked with **Note** in the text.

Caution : Information requiring particular attention

Remark : Supplementary information

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name	Document Number	
	English	Japanese
IE-78K0-NS-A	To be prepared	To be prepared
IE-78K0-NS-P04, IE-780948-NS-EM4.	This manual	To be prepared
ID78K0-NS Integrated Debugger Reference Windows Based	U12900E	U12900J

Caution: The documents listed above are subject to change without notice. Be sure to use the latest documents when designing.

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[MEMO]

Chapter 1 General

The IE-78K0-NS-P04 and the IE-780948-NS-EM4 are development tools for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K/0 Series of 8-bit single-chip microcontrollers.

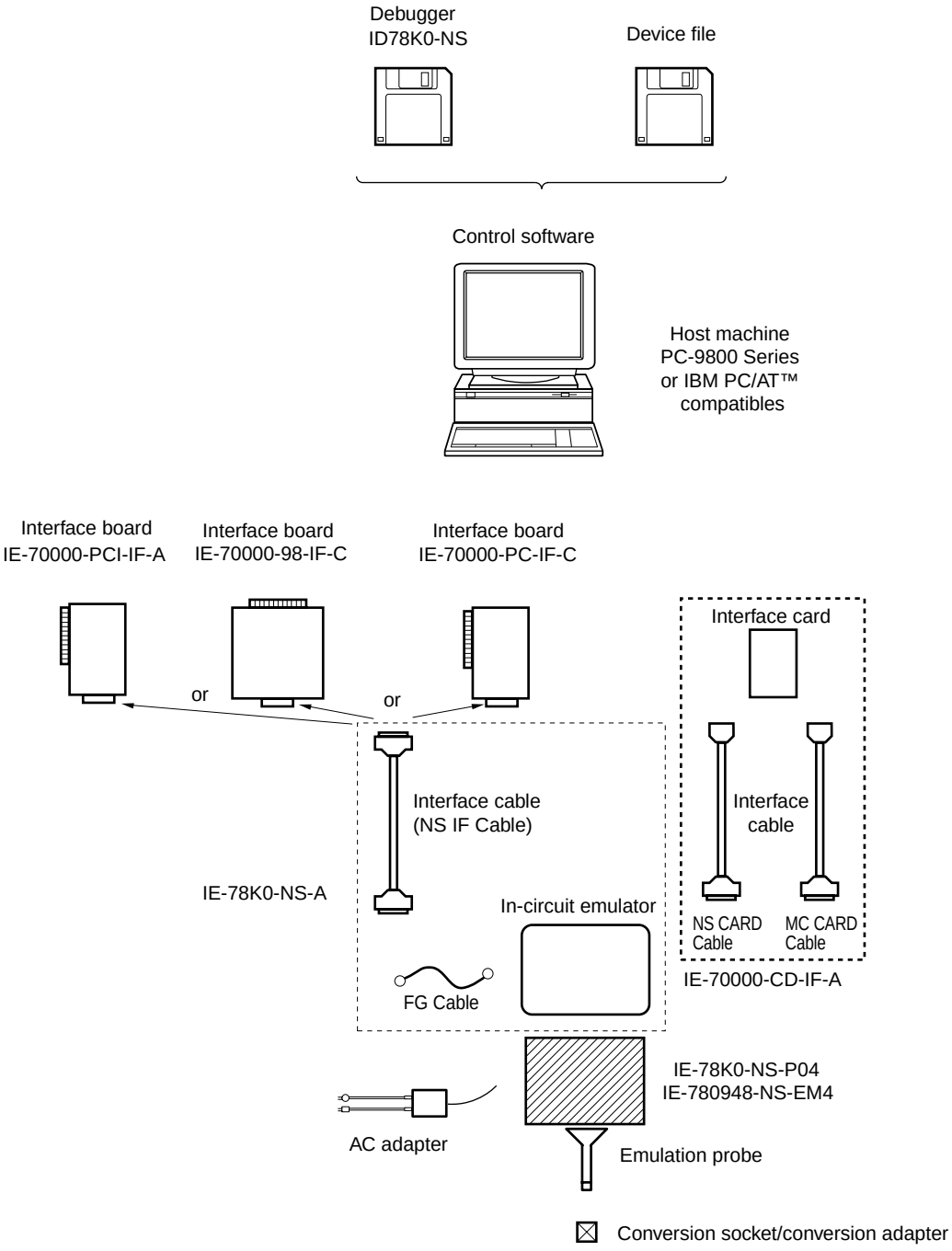
This chapter describes the emulation board’s and probe board's system configuration and basic specifications.

- Target device
  - µPD780948 Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-78K0-NS-P04/IE-780948-NS-EM4's system configuration.

Figure 1-1: System Configuration



Note: The packages, emulation probes, and conversion sockets/conversion adapters are listed below.

Package	Emulation Probe	Conversion Socket/ Conversion Adapter
100-pin plastic QFP (GF - type)	NP-100 GF-TQ	NQPACK100RB YQPACK100RB HQPACK100RB YQSOCKET100RBF

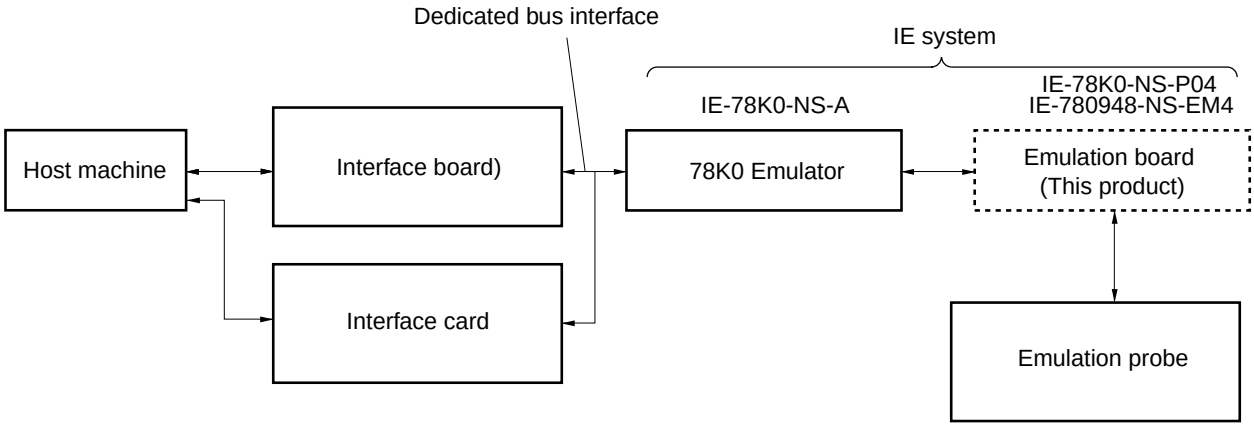
The NP-100GF-TQ is a product of Naito Densei Machidaseisakusho Co., Ltd.

The sockets are products of TOKYO ELETECH CORPORATION.

1.2 Hardware Configuration

Figure 1-2 shows the IE-78K0-NS-P04/IE-780948-NS-EM4's position in the basic hardware configuration.

Figure 1-2: Basic Hardware Configuration



1.3 Basic Specifications

The IE-78K0-NS-P04/IE-780948-NS-EM4's basic specifications are listed in Table 1-1.

Table 1-1: Basic Specifications

Parameter	Description
Target device	PD780948 Subseries
System clock	Main system clock: 8,38 MHz Subsystem clock: typically 32.768 KHz
Clock supply	External: Pulse input Internal: Mounted on emulation board
Voltage support	4.0 to 5.5 V (same as target device)

1.4 Notes on Use of IE-78K0-NS-P04 and IE-780948-NS-EM4

(1) Ensure that the power supply for the IE-78K0-NS-A and the target system is OFF before connecting or disconnecting to/from the IE-78K0-NS-A and the target device, or changing switch settings, etc.

(2) When carrying out target device emulation using the IE-78K0-NS-P04 and IE-780948-NS-EM4 in conjunction with the IE-78K0-NS-A, there are certain differences from the operation of the actual device (see **Differences from Target Device**).

(3) The target system V_{DD} must be between 4.0 V and 5.5 V.

(4) **Power on sequence:**
   1. Power on IE-78K0-NS-A
   2. Power on target hardware
   3. Start debugger ID78K0-NS

(5) **Power off sequence:**
   1. Exit from debugger ID78K0-NS
   2. Power off target hardware
   3. Power off IE-78K0-NS-A.

[Memo]

Chapter 2 Part Names

This chapter introduces the parts of the IE-78K0-NS-P04 and the IE-780948-NS-EM4.
The packaging boxes of the IE-78K0-NS-P04 and the IE-780948-NS-EM4 contain the following items:

2.1 Package Components

IE-78K0-NS-P04 Components

The IE-78K0-NS-P04 comprises the following components. Please check that all these items are included in the package.

(1)	IE-78K0-NS-P04	x 1
(2)	Parts holder (with cover)	x 2
(3)	Registration Card	x 1
(4)	Readme First	x 1
(5)	List of Contents	x 1

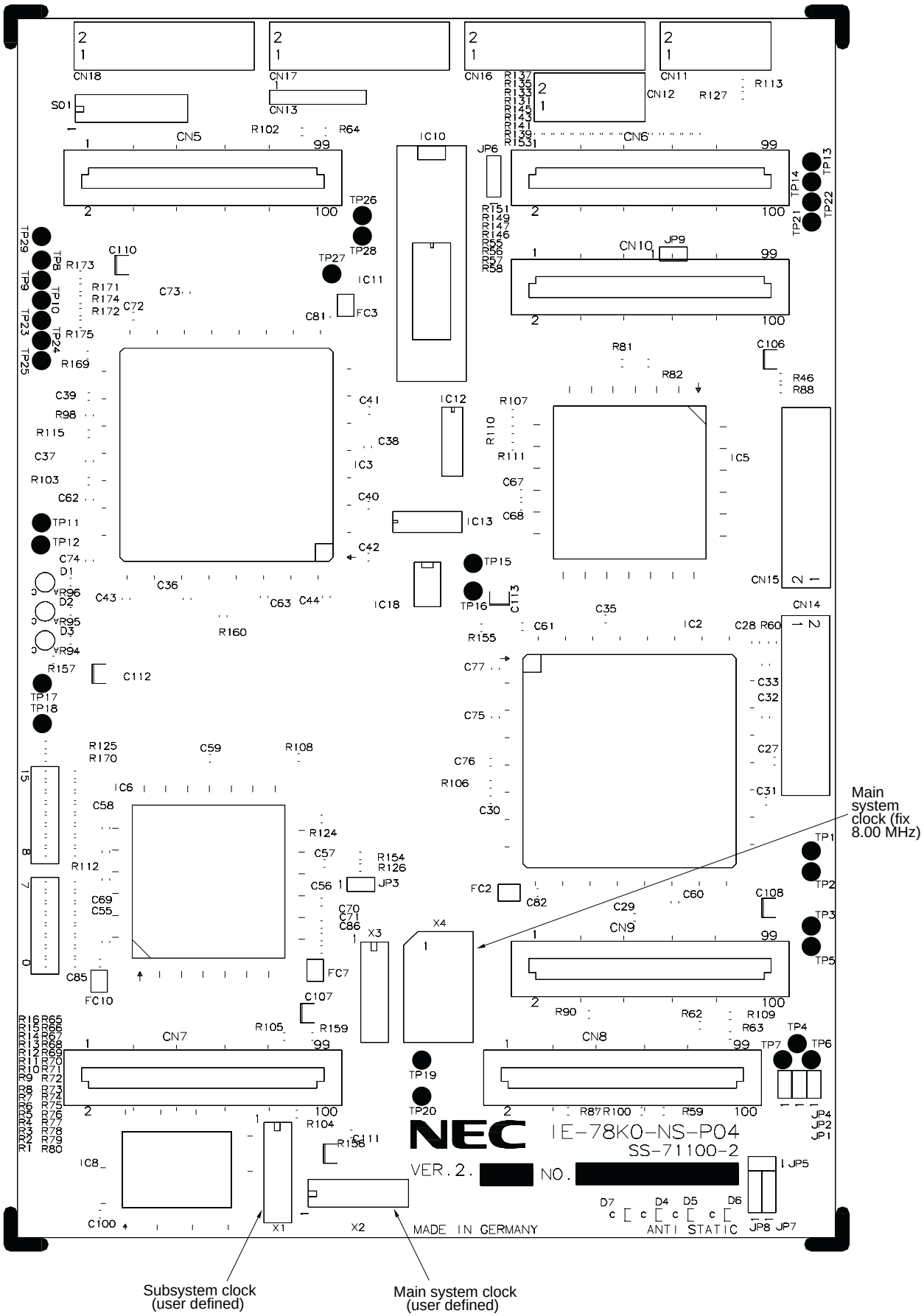
IE-780948-NS-EM4 Components

The IE-780948-NS-EM4 comprises the following components. Please check that all these items are included in the package.

(1)	IE-780948-NS-EM4	x 1
(2)	Screws Set	x 1
(3)	Registration Card	x 1
(4)	Readme First	x 1
(5)	List of Contents	x 1
(6)	Floppy Disk with Device File and FPGA Data	x 1
(7)	Socket for LCD-C/D resistor network	x 1
(8)	User's Manual (this manual)	x 1

2.2 Parts of the IE-78K0-NS-P04

Figure 2-1: IE-78K0-NS-P04 External View and Part Names



2.3 Parts of the IE-780948-NS-EM4

Figure 2-2: IE-780948-NS-EM4 External View and Part Names

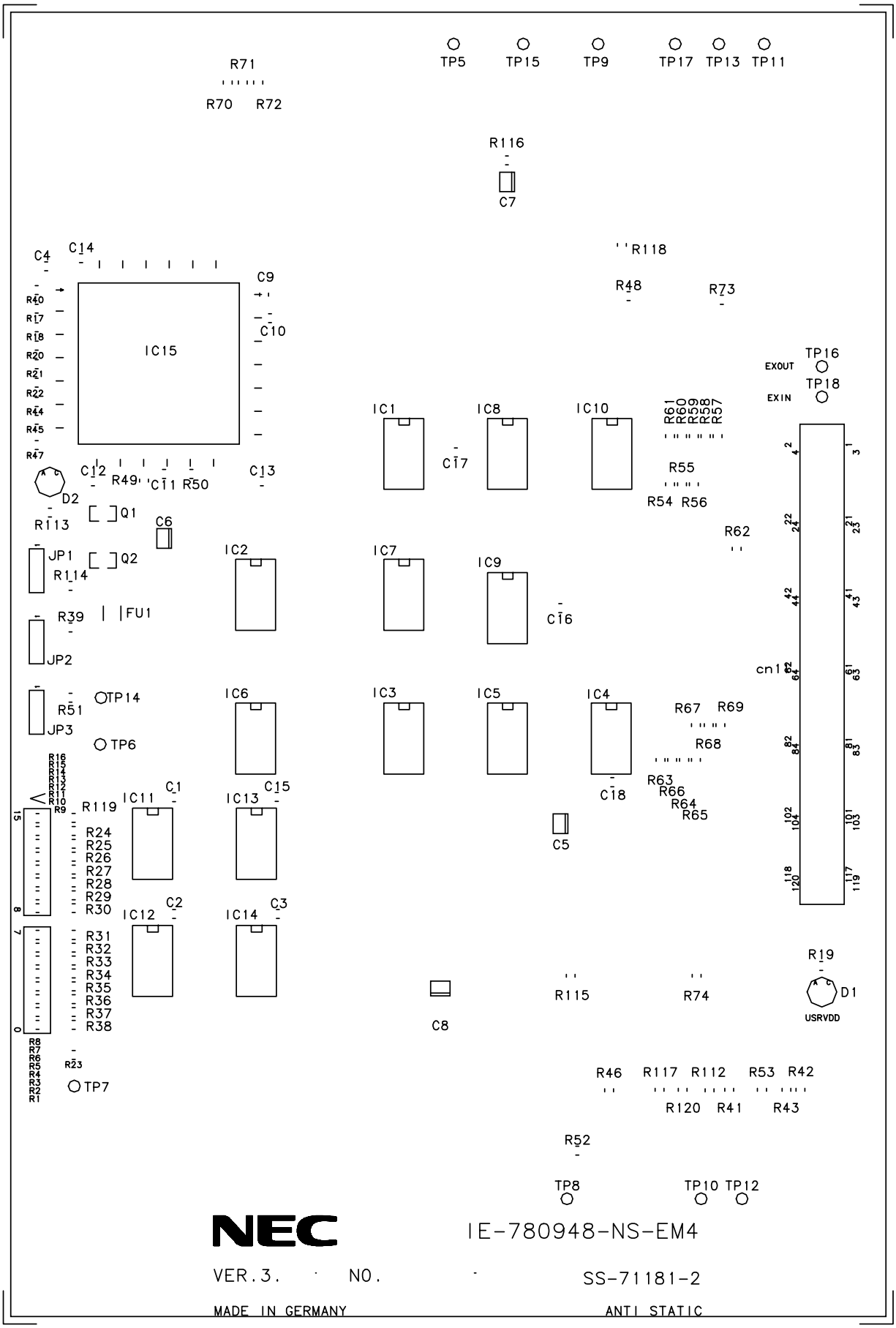


Table 2-1: Names of IE-78K0-NS-P04 and IE-780948-NS-EM4 Parts

Name	Description (IE-78K0-NS-P04)	Name	Description (IE-780948-NS-EM4)
CN1	Emulator connections	CN5	Emulation board connectors (IE-78K0-NS-P04)
CN2		CN6	
CN3		CN7	
CN4		CN8	
CN5	Probe board connectors (IE-78K0-NS-P04)	CN9	
CN6		CN10	
CN7		CN11	Probe connector
CN8		JP1	Disconnect USER-Reset
CN9		JP2	CAN TxD driver buffer type
CN10		JP3	CAN RxD receive buffer type
CN11	Test connector (only for internal use by NEC)		
CN12			
CN13			
CN14			
CN15			
CN16			
CN17			
CN18			
JP1	Analog reference voltage		
JP2	GND-pin of A/D Converter		
JP3	Reseved (only for internal use by NEC)		
JP4	JTAG mode selection (only for internal use by NEC)		
JP5	FPGA mode selection		
JP6	JTAG mode selection (only for internal use by NEC)		
JP7	LV_{REF1}		
JP8	LV_{REF0}		

[Memo]

Chapter 3 Installation

This chapter describes the method for the connection of the IE-78K0-NS-P04, the IE-780948-NS-EM4 and the emulation probe.

- Installation of the IE-78K0-NS-P04
- Installation of the IE-780948-NS-EM4
- Installation of the emulation probe
- Setting of the jumpers for the clock selection

The power supply of the IE-78K0-NS-A and the target system must be switched off when connecting or disconnecting any item.

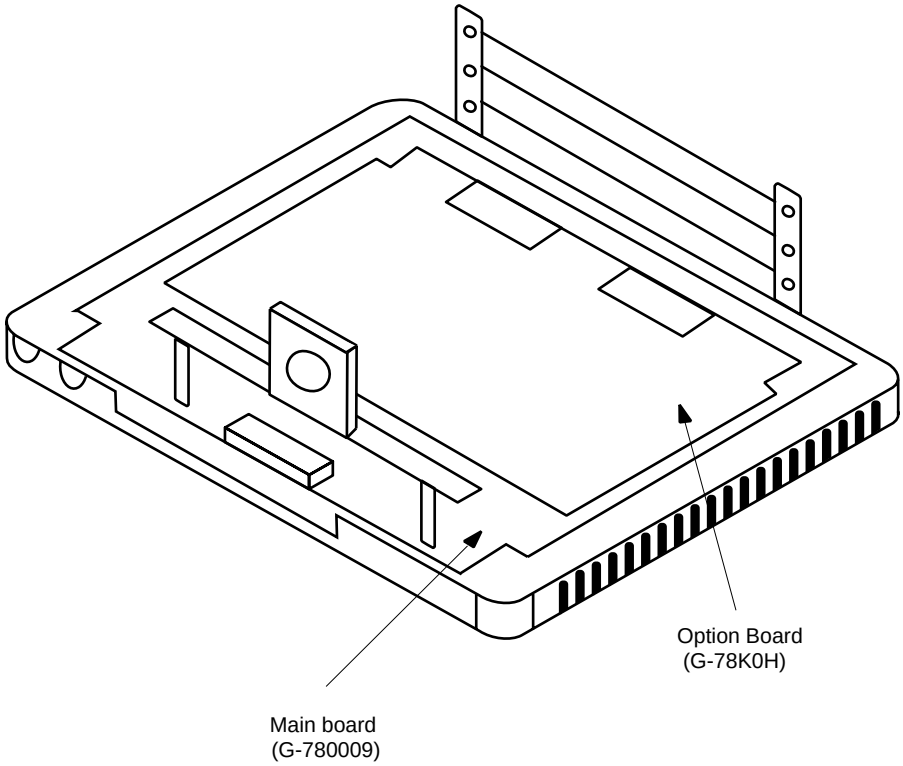
Caution: Usage of incorrect connection methods may damage the IE system.

3.1 Installation Procedure

<1> Remove the 4 screws at the sides of the IE-78K0-NS-A and open the top of the cover.

<2> Remove the screws on the option board (G-78K0H) and remove the option board.

Figure 3-1: IE-78K0-NS-A inside



<3> Setup the jumper's on the **main board** (G-780009).

It is necessary to set some jumpers on the main board for the clock selection. An example for the jumper setting will be given in the chapter clock setting.

Jumper JP2

Table 3-1: Flash ROM Mode

Jumper Position	Function
(1-2)	Internal use
(2-3)	Internal use **(default)**

Jumper JP3

Table 3-2: Internal Mode 1

Jumper Position	Function
(1-2)	Internal use **(default)**
(2-3)	Internal use

Jumper JP4

Table 3-3: Internal Mode 2

Jumper Position	Function
(1-2)	Internal use **(default)**
(2-3)	Internal use

Jumper JP6

Table 3-4: Main Clock Selection

Jumper Position	Function
(1-2)	Not selectable
(3-4)	EM1/P04 board selection **(default)**
(5-6)	EM4 board selection

Jumper JP7

Table 3-5: Main Clock Doubler Selection

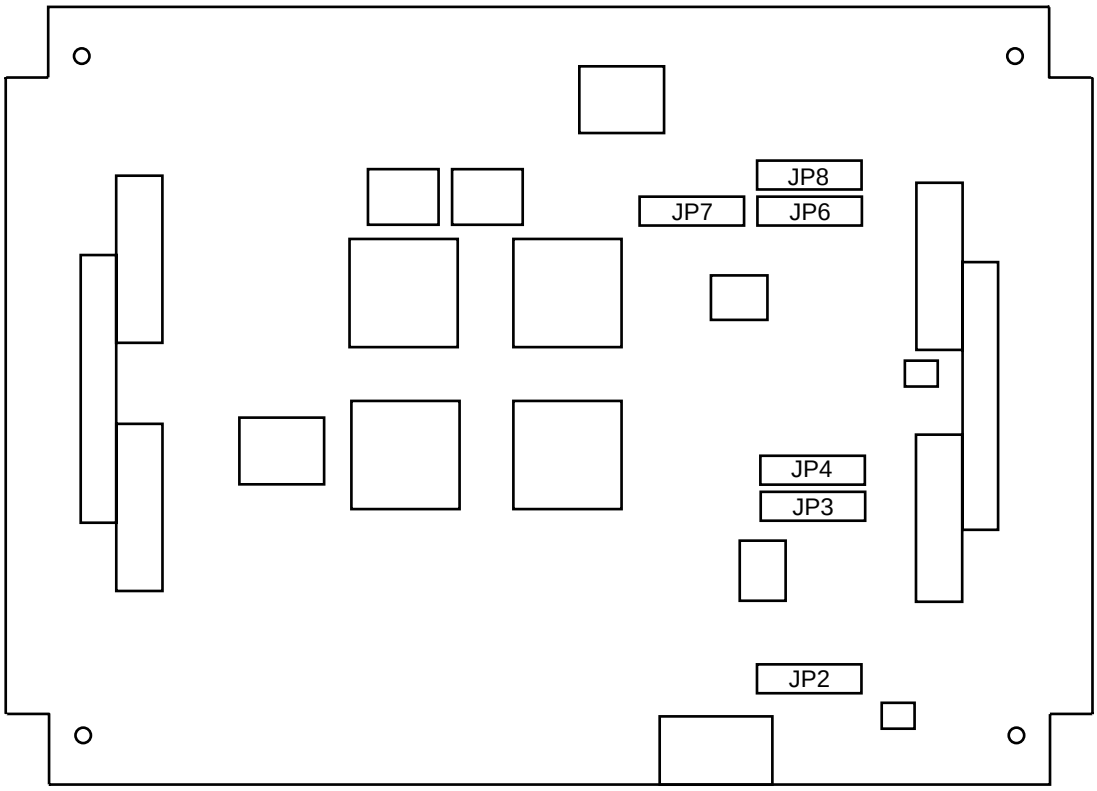
Jumper Position	Function
(1-2)	Main board selection **(default)**
(3-4)	EM board selection 1
(5-6)	EM board selection 2

Jumper JP8

Table 3-6: Sub Clock Selection

Jumper Position	Function
(1-2)	On EM board **(default)**
(3-4)	On target system
(5-6)	On main board

Figure 3-2: Main Board (G-780009) Jumper Positioning



<4> Connect the option board (G-78K0H) to the main board (G-780009).

<5> Setup of the **emulation board (IE-78K0-NS-P04)**

LCD - C/D resistor network

The 780948 Series has the possibility to use the LCD-C/D with the external resistor network or with resistor as mask option.

A socket is delivered with the IE-780948-NS-EM4 for the mounting of the LCD-C/D resistor network. This socket has to be plugged in the socket SO1 of the IE-78K0-NS-P04.

Jumper JP5

Table 3-7: FPGA Mode Selection (for internal tests only)

Jumper Position	ESN	Function
Closed	GND	Reserved
Open	Pull-up	Asynchronous Peripheral Mode (FPGA s are loaded by IE) (**default**)

Jumper JP2

Table 3-8: Ground Voltage Pin of AD-Converter

Jumper Position	AAVSS	Function
Open	Target	Connected to target selected ground base **(default**)
Closed	GND	Internal digital ground

Jumper JP1

Table 3-9: V_{CC} Voltage Pin of AD-Converter

Jumper Position	AA_{REF0}	Function
Open	Target	Connected to target selection voltage **(default)**
Closed	V_{CC}	Internal digital V_{CC}

Jumper JP8

Table 3-10: Voltage Setting

Jumper Position	LV_{REF1}	Function
(1 - 2)	V_{CC}	For internal testing
(2 - 3)	LV_{DD}	For internal testing (**default**)

Jumper JP7

Table 3-11: Voltage Setting

Jumper Position	LV_{REF0}	Function
(1 - 2)	V_{CC}	For internal testing
(2 - 3)	LV_{DD}	For internal testing (**default**)

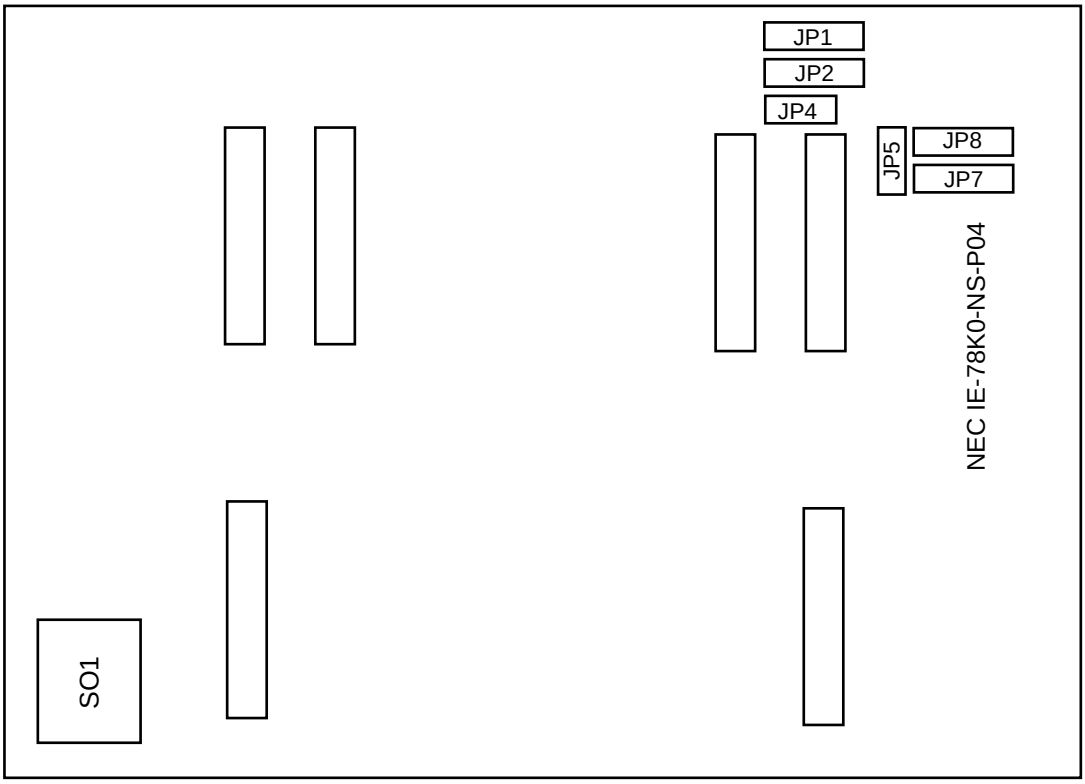
LED indicator

Table 3-12: LED Indicator D1, D2, D3

LED	Condition	Function
LED1 green	Blinking	FPGA downloading ongoing
LED1 green	On	FPGA download complete
LED1 green	Off	FPGA not programmed
LED2 yellow	Blinking	Not used
LED2 yellow	On	V_{CC} on
LED2 yellow	Off	V_{CC} off
LED3 red	Blinking	Not used
LED3 red	On	Not used
LED3 red	Off	Not used

Remark: Not used conditions reserved for future functions.

Figure 3-3: Emulation Board (IE-78K0-NS-P04) Jumper Positioning



<6> Connect the emulation board (IE-78K0-NS-P04) to the option board (G-78K0H).

<7> When user clock as main clock is used, the main system clock can be mounted by using a parts holder or a crystal oscillator (see chapter clock setting).

<8> Setup of the **probe board (IE-780948-NS-EM4)**

Jumper JP1

Table 3-13: User $\overline{\text{RESET}}$ mode

Jumper Position	User $\overline{\text{RESET}}$	Function
(1 - 2)	To probe	User Reset (IE) connected to the probe (**default**)
(2 - 3)	Pull-up	User Reset (IE) pull-up by resistor (10K)

Jumper JP2

Table 3-14: DCAN Transmit Buffer Selection

Jumper Position	DCAN out	Function
(1 - 2)	Pin emulator	Reserved
(2 - 3)	FPGA	DCAN transmit line from FPGA via transistor to probe (**default**)

Jumper JP3

Table 3-15: DCAN Receive Buffer Type Selection

Jumper Position	DCAN in	Function
(1 - 2)	Pin emulator	Original buffer (**default**)
(2 - 3)	FPGA	Buffer type different /timing optimized (limitation $USRV_{DD} \geq 4.5$ V)

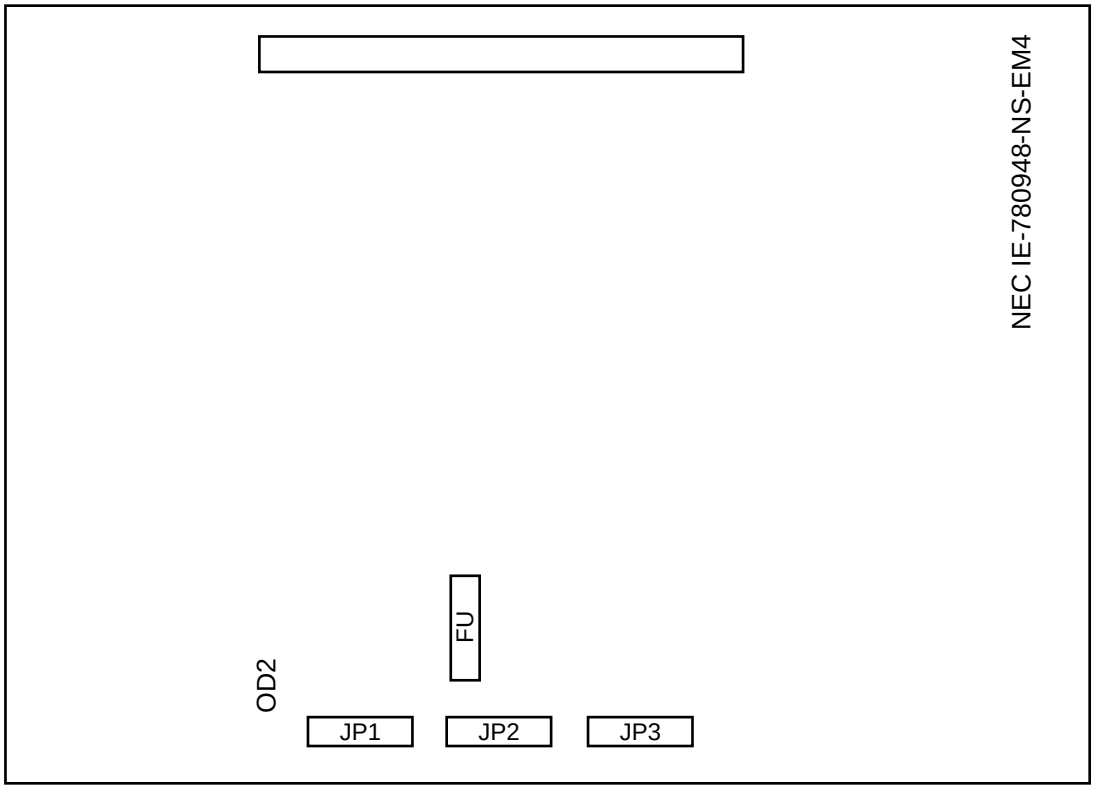
LED Indicator

Table 3-16: LED Indicator D2

LED	Condition	Function
LED2	On	Correct connection of CTxD
LED2	Off	Shortcut at CTxD

Remark: This is a fuse on the CTxD included to avoid a short cut at a wrong connection. After a power down/off the CTxD function will work again.

Figure 3-4: Probe Board (IE-780948-NS-EM4) Jumper Positioning



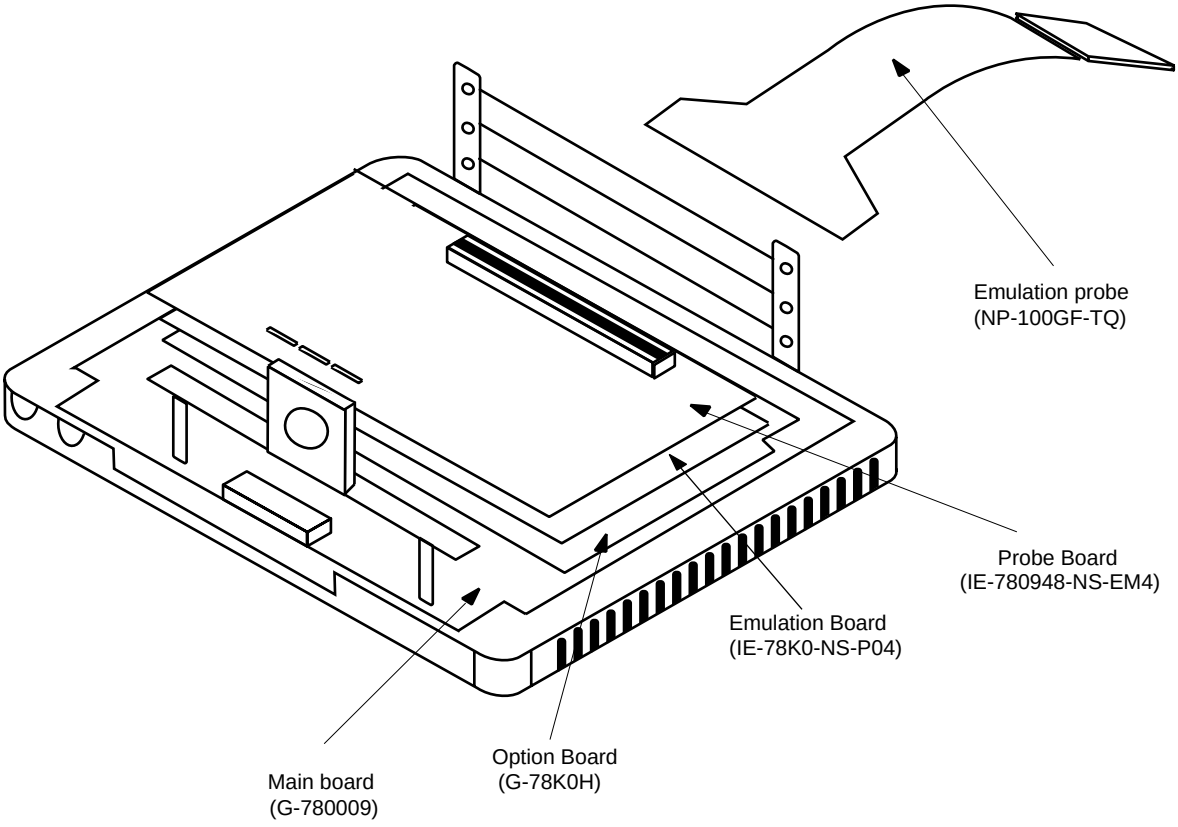
<9> Connect the probe board (IE-780948-NS-EM4) to the emulation board (IE-78K0-NS-P04)

<10> Remove the top and the bottom plate by removing the screws)

<11> Connect the probe (NP-100GF-TQ) to CN11 of the probe board (IE-780948-NS-EM4).

<12> Connect the cover and tighten the 4 screws.

Figure 3-5: Connection of Boards



3.2 Clock Settings

3.2.1 Overview of clock settings

Main system clock

Select from (1) to (3) below as the main system clock and subsystem clock to be used during debugging.

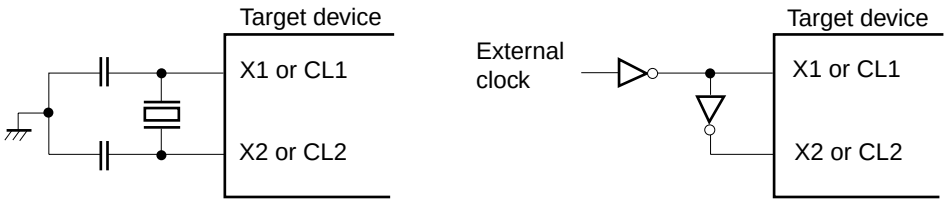
(1) Clock that is already mounted on emulation board
(2) Clock that is mounted by user
(3) External clock

If the target system includes an internal clock, select either “(1) Clock that is already mounted on emulation board” or “(2) Clock that is mounted by user”. An internal clock connects the target device to an oscillator and uses the target device’s internal oscillation circuit. An example of an external circuit is shown in part (a) of Figure 3-2. During emulation, the oscillator that is mounted on the target system is not used. Instead, it uses the clock that is mounted on the emulation board which is installed for the IE-78K0-NS-A.

If the target system includes an external clock, select “(3) External clock”.

An external clock supplies a clock signal from outside of the target device and does not use the target device’s internal oscillation circuit. An example of an external circuit is shown in part (b) of Figure 3-2.

Figure 3-6: External Circuits Used as System Clock Oscillation Circuit

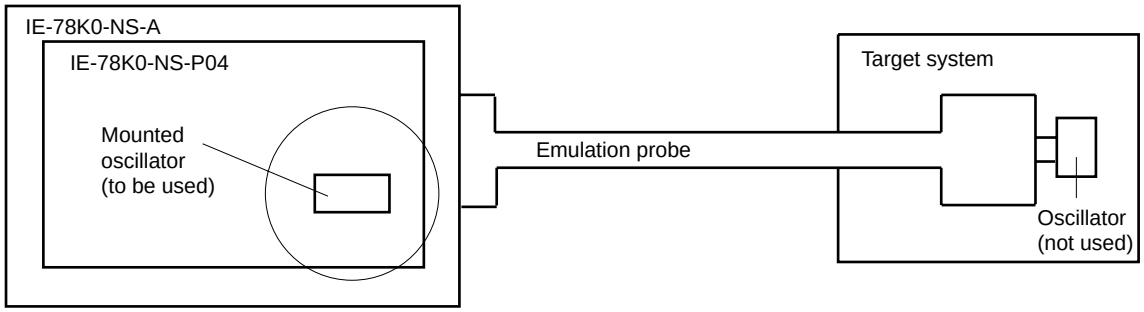


3.2.2 Main System Clock Selections

(1) Clock that is already mounted on emulation board

A crystal resonator is already mounted on the emulation board. Its frequency is 8.0000 MHz.

Figure 3-7: When Using Clock That Is Already Mounted on Emulation Board

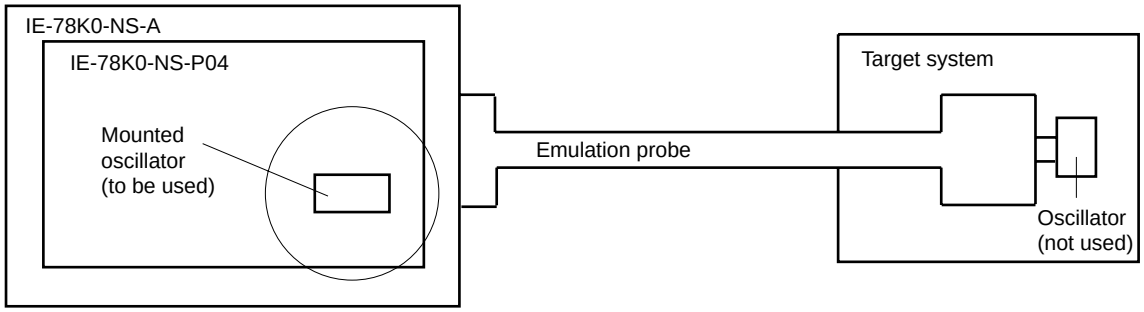


Remark: The clock that is supplied by the IE-78K0-NS-P04 oscillator (encircled in the figure) is used.

(2) Clock that is mounted by user

The user is able to mount any clock supported by the set specifications on the IE-78K0-NS-P04. First mount the oscillator on the parts holder, then attach the parts board to the IE-78K0-NS-P04. This method is useful when using a different frequency from that of the pre-mounted clock.

Figure 3-8: When Using User-mounted Clock

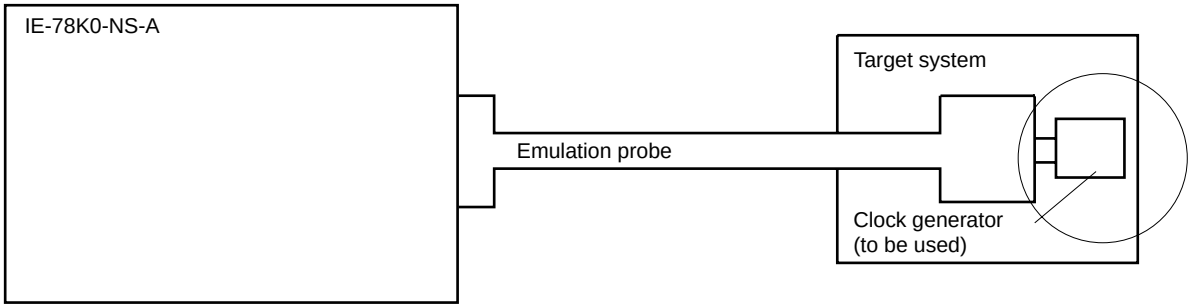


Remark: The clock that is supplied by the IE-78K0-NS-P04 oscillator (encircled in the figure) is used.

(3) External clock

An external clock connected to the target system can be used via the emulation probe.

Figure 3-9: When Using an External Clock



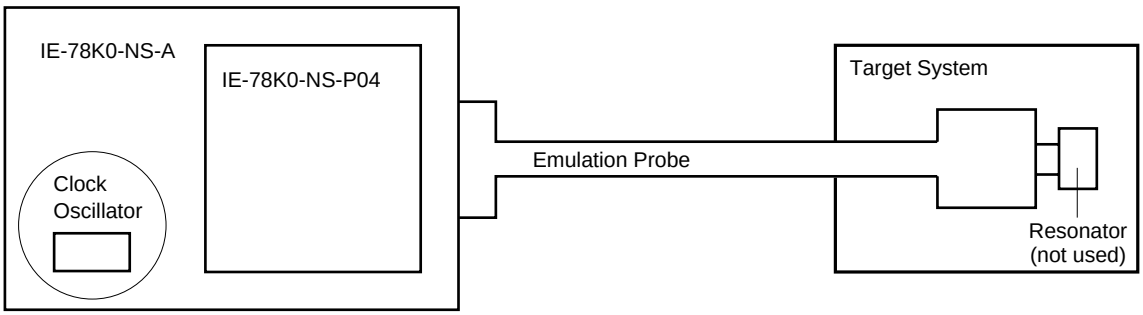
Remark: The clock supplied by the target system's clock generator (encircled in the figure) is used.

3.2.3 Subsystem Clock

(1) Standard clock offered by the main board

A crystal oscillator is already mounted on the main board. The frequency is 32.768 kHz.

Figure 3-10: When Using Standard Clock Mounted on Main Board

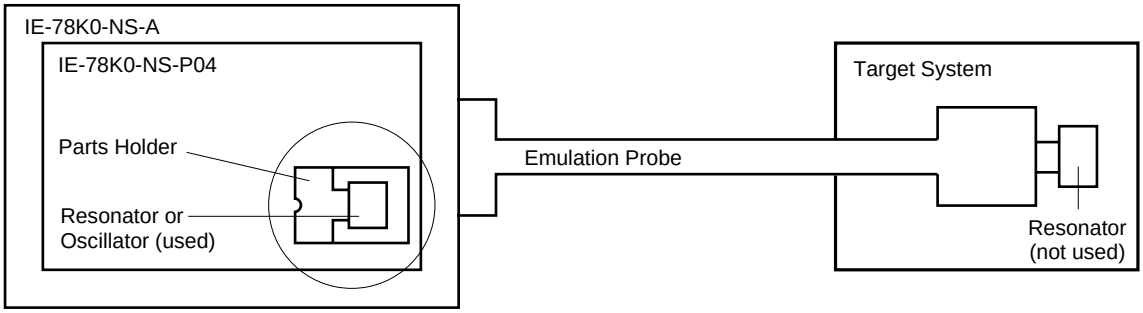


Remark: The clock supplied from the oscillator on the Main Board (G-78009) (circled) is used.

(2) Clock mounted by user on the emulation board

A clock that matches the specifications set by the user can be mounted on the IE-78K0-NS-P04. The resonator or oscillator to be used is mounted on a parts holder and that parts holder is installed on the IE-78K0-NS-P04. This is useful if you want to perform debugging at a different frequency from that of the clock mounted beforehand.

Figure 3-11: When Using Clock Mounted on the Emulation Board

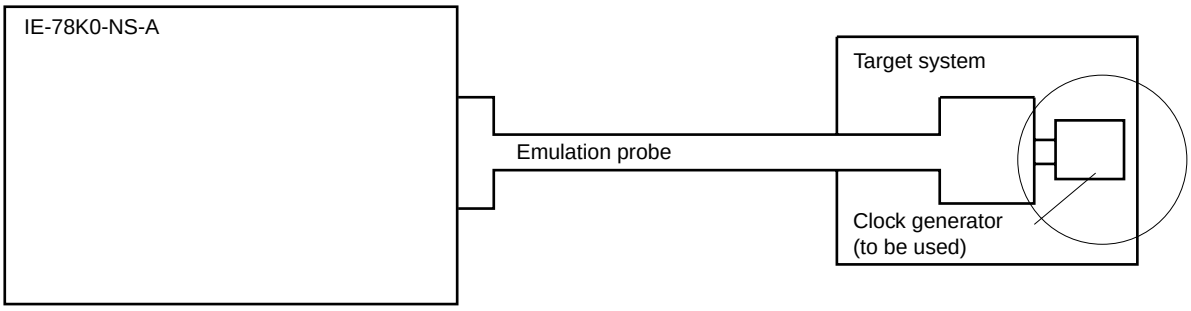


Remark: The clock supplied from the resonator or oscillator on the IE-78K0-NS-P04 (circled) is used.

(3) External clock on the target hardware

The external clock on the target system can be used via an emulation probe.

Figure 3-12: Using an External Clock mounted on the Target Hardware



Remark: The clock supplied by the clock generator circuit (circled in the above figure) is used.

3.2.4 Main system clock settings

Table 3-17: Main System Clock Settings

Frequency of Main System Clock		IE-78K0-NS-P04	CPU Clock Source Selection (ID)
When using clock that is already mounted on emulation board	8.0000 MHz	Shortcut 6-8	Internal
When using clock mounted by user	Other than 8.0000 MHz	Includes oscillator circuit	External
When using external clock		Shortcut 6-8	

Caution: When using an user defined clock or external clock, open the configuration dialog when starting the integrated debugger (ID78K0-NS) and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).

Remark: The IE-78K0-NS-P04 factory settings are those listed above under "when using clock that is already mounted on emulation board".

(1) When using clock that is already mounted on emulation board

When the IE-78K0-NS-P04 is shipped, an 8.0000-MHz crystal resonator is already mounted in the IE-78K0-NS-P04 X4 socket. When using the factory-set mode settings, there is no need to make any other hardware settings.

When starting the integrated debugger (ID78K0-NS), open the configuration dialog and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).

(2) When using clock mounted by user

The settings described under either (a) or (b) are required, depending on the type of clock to be used. When starting the integrated debugger (ID78K0-NS), open the configuration dialog and select “Internal” in the area (Clock) for selecting the CPU’s clock source (this selects the emulator’s internal clock).

(a) When using a ceramic oscillator or crystal resonator

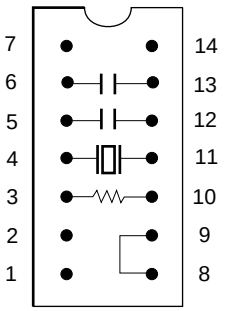
- Items to be prepared
  - Parts holder (supplied with IE-78K0-NS-P04)
  - Ceramic oscillator or crystal resonator
  - Resistor Rx
  - · Capacitor CA
  - · Capacitor CB
  - · Solder kit

<Steps>

<1> Solder onto the supplied parts board (as shown below) the target ceramic oscillator or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequency).

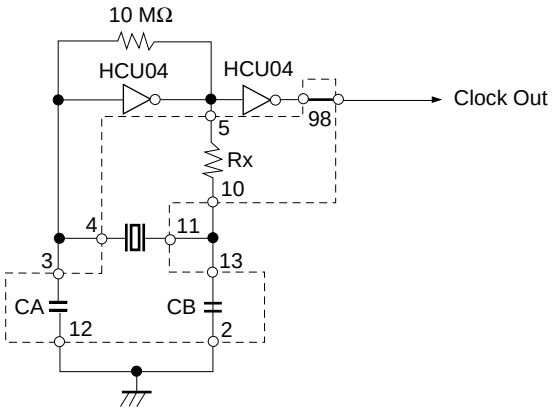
Figure 3-13: Connections on Parts Board (When Using Main System Clock or User-Mounted Clock)

Parts board (MAINCLK)



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic oscillator or crystal resonator
5-10	Resistor Rx
8-9	Short

Circuit diagram

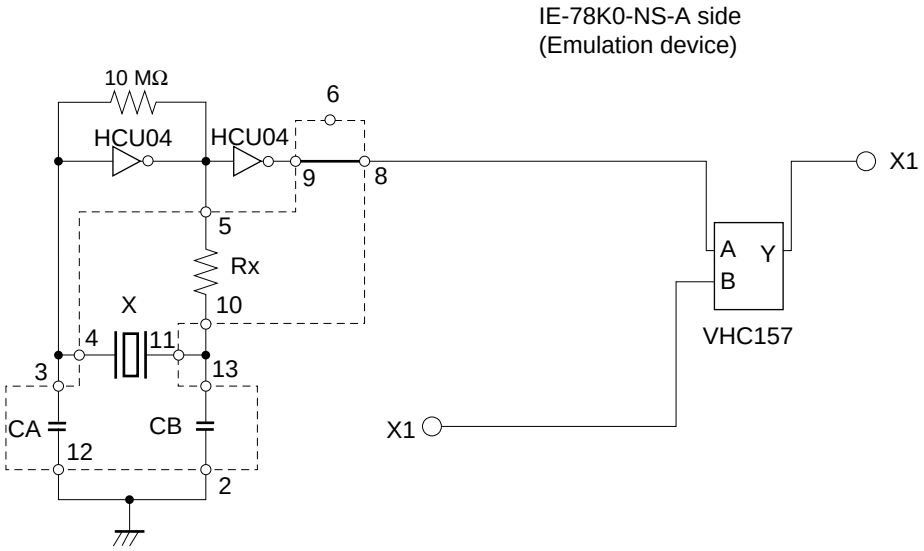


Remark: The sections enclosed in broken lines indicate parts that are attached to the parts board.

<2> Prepare the IE-78K0-NS-P04.
<3> Remove the parts holder inserted in the socket (marked "X2") on the IE-78K0-NS-P04.
<4> Connect the parts holder (from <1> above) to the socket (X2) from which the part holder was removed. Check the pin 1 mark to make sure the board is mounted in the correct direction.
<5> Make sure that the parts board mounted in the X2 socket on the emulation board is wired as shown in Figure 3-10 above.
<6> Install the IE-78K0-NS-P04 and the IE-780948-NS-EM4 in the IE-78K0-NS-A.

The above steps configure a circuit and enable clock output to be supplied from the mounted oscillator to the emulation device.

Figure 3-14: IE-78K0-NS-A side (Emulation Device)

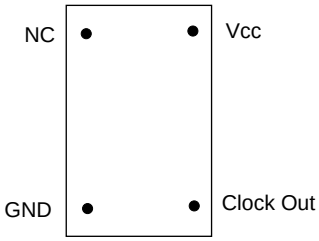


Remark: The sections enclosed in broken lines indicate parts that are attached to the parts holder.

(b) When using a crystal oscillator

- Items to be prepared
  - Crystal oscillator (see pinouts shown in Figure 3-7)

Figure 3-15: Crystal Oscillator (When Using Main System Clock or User-mounted Clock)



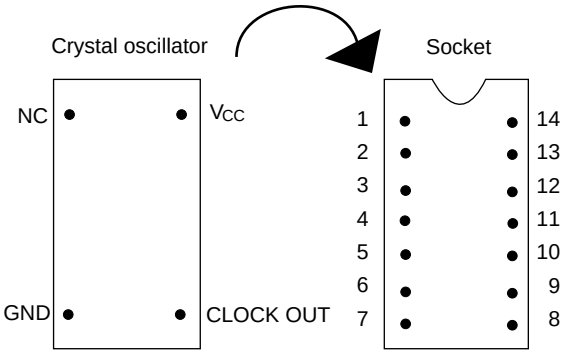
<Steps>

<1> Prepare the IE-78K0-NS-P04.

<2> Remove the parts holder inserted in the socket (marked “X2”) on the IE-78K0-NS-P04.

<3> Connect the parts board (from <2> above) to the socket (X2) from which the parts holder was removed. Insert the crystal oscillator into the socket so as to align the pins as shown in the figure below.

Figure 3-16: Pin Alignment of Crystal Oscillator and Socket

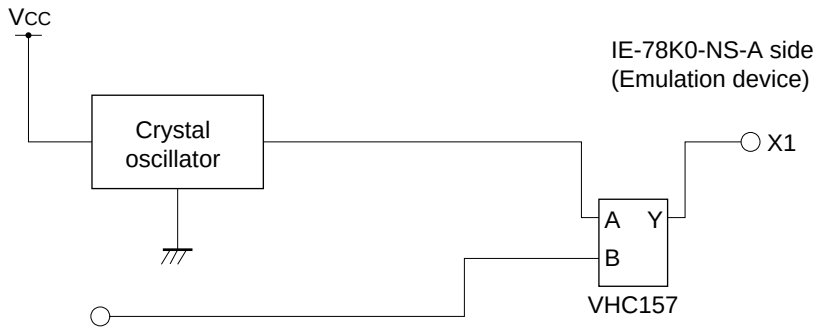


Crystal Oscillator Pin Name	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
V_{CC}	14

<4> Install the IE-78K0-NS-P04 and the IE-780948-NS-EM4 in the IE-78K0-NS-A.

The above steps configure a circuit and enable clock output to be supplied from the mounted oscillator to the emulation device.

Figure 3-17: IE-78K0-NS-A side (Emulation Device)



(3) When using an external clock

No hardware settings are required for this situation.

Make sure that the parts holder with a shortcut between 6 and 8 is in the socket (marked "X2").

When starting the integrated debugger (ID78K0-NS), open the configuration dialog and select “External” in the area (Clock) for selecting the CPU’s clock source (this selects the user’s clock).

3.2.5 Examples of Main System Clock Setting

(1) Standard Clock 8.0000 MHz offered by the Emulation Board (IE-78K0-NS-P04)

Main Board:	JP6 - (3-4)
	JP7 - (1-2)
Emulation Board:	X2 with shortcut between 6 - 8
ID78K0-NS:	Internal

(2) Clock mounted by the User on the Emulation Board

- User related Clock

Main Board:	JP6 - (3-4)
	JP7 - (1-2)
Emulation Board:	X2 with parts holder and crystal resonator, ceramic resonator or crystal oscillator
ID78K0-NS:	External

(3) External Clock on the Target Hardware

Main Board:	JP6 - (3-4)
	JP7 - (1-2)
Emulation Board:	X2 with shortcut between 6 - 8
ID78K0-NS:	External

3.3 Subsystem Clock

3.3.1 Subsystem Clock Setting

Table 3-18: Subsystem Clock Settings

Subsystem Clock Frequency to be Used		IE-78K0-NS-P04	IE-78K0-NS-A
		Parts holder (X1)	JP8
When using clock that is already mounted on main board	32.768 KHz	Short 6 - 8	Short 5 - 6
When using user-mounted clock	Other than 32.768 KHz	Includes oscillator	Short 1 - 2
When using external clock		Not used	Short 3 - 4

Caution: Jumper JP8, which is used to select the board's clock or an external clock, should be set only after turning off the IE-78K0-NS-A's power.

(1) When using clock that is already mounted on main board

When the IE-78K0-NS-P04 / IE-780948-NA-EM4 are shipped, there is no 32.768 KHz crystal on the board. The parts holder on X1 is shortened between 6 and 8. Short pins 5 and 6 of JP8 of the IE-78K0-NS-A's main board to use the 32.768 KHz crystal of the emulator. There is no additional settings of the integrated debugger ID78K0-NS necessary.

(2) When using the user-mounted clock on the IE-78K0-NS-P04

The settings described under either (a) or (b) are required, depending on the type of clock to be used.
Short pins 1 and 2 on the IE-78K0-NS-A's jumper (JP8).
There is no need to make any other settings via the integrated debugger (ID78K0-NS).

(a) When using a ceramic oscillator or crystal resonator

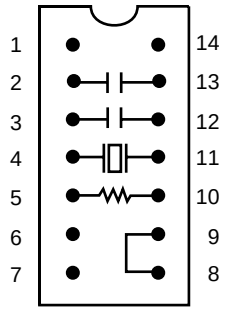
- Items to be prepared
  - Parts board (supplied with IE-78K0-NS)
  - Ceramic oscillator or crystal resonator
  - Resistor Rx
  - Capacitor CA
  - Capacitor CB
  - Solder kit

<Steps>

<1> Solder onto the supplied parts board (as shown below) the target ceramic oscillator or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequency).

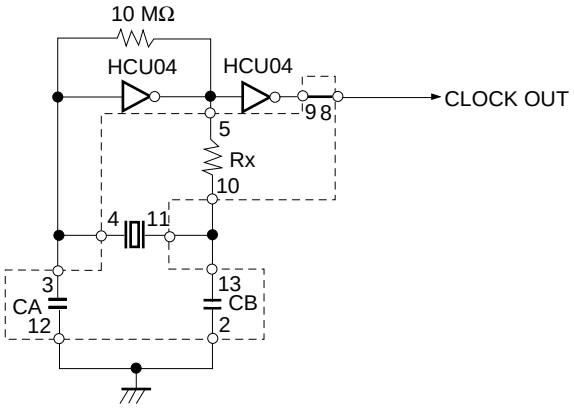
Figure 3-18:Connections on Parts Board (When Using Subsystem Clock or User-Mounted Clock)

Parts holder (X1 of IE-78K0-NS-P04)



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic oscillator or crystal resonator
5-10	Resistor Rx
8-9	Short

Circuit diagram

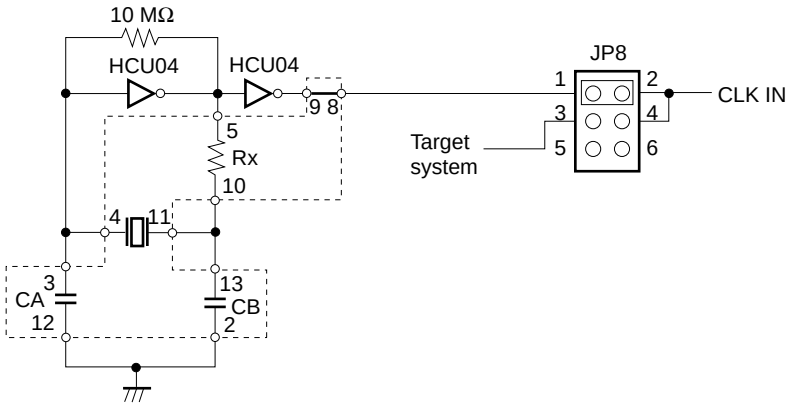


Remark: The sections enclosed in broken lines indicate parts that are attached to the parts board.

<2> Prepare the IE-78K0-NS-P04.
<3> Remove the crystal oscillator that is mounted in the IE-78K0-NS-P04's socket (the socket marked as "X1").
<4> Connect the parts board (from <1> above) to the socket (X1) from which the crystal oscillator was removed (see <3> above). Check the pin 1 mark to make sure the board is mounted in the correct direction.
<5> Install the IE-78K0-NS-P04 and the IE-780948-NS-EM4 in the IE-78K0-NS-A.

The above steps configure a circuit and enable clock output to be supplied from the mounted oscillator to the emulation device.

Figure 3-19: IE-78K0-NS-A side

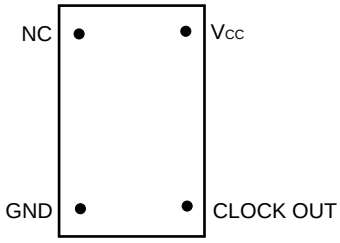


Remark: The section enclosed in broken lines indicates parts that are attached to the parts board.

(b) When using a crystal oscillator

- Items to be prepared
  - Crystal oscillator (see pinouts shown in Figure 3-20)

Figure 3-20: Crystal Oscillator (When Using Subsystem Clock or User-mounted Clock)

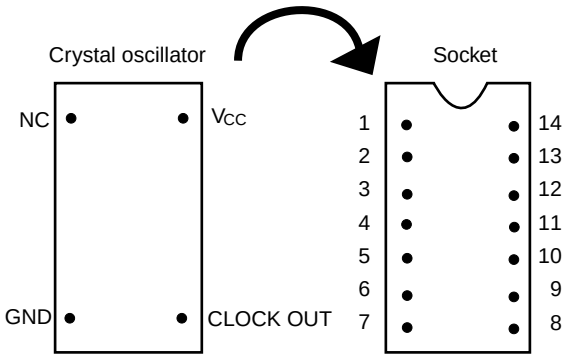


<Steps>

<1> Prepare the IE-78K0-NS-P04.

<2> Remove the crystal oscillator that is mounted in the IE-78K0-NS-P04's socket (the socket marked as "X1").

<3> Connect the parts board (from <2> above) to the socket (X1) from which the crystal oscillator was removed. Insert the crystal oscillator into the socket so as to align the pins as shown below.

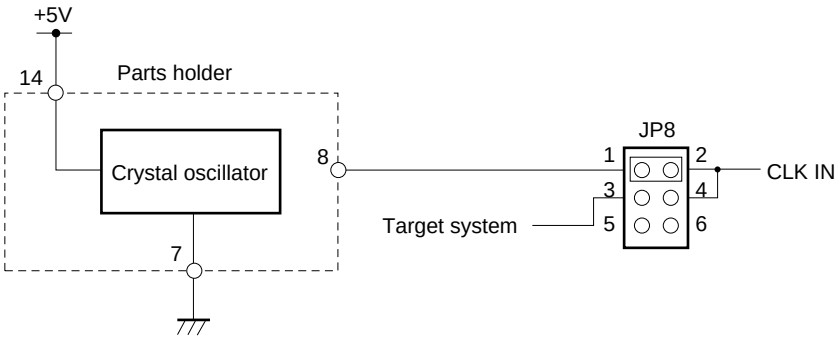


Crystal Oscillator Pin Name	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
VCC	14

<4> Install the IE-78K0-NS-P04 and the IE-780948-NS-EM4 in the IE-78K0-NS-A.

The above steps configure a circuit and enable clock output to be supplied from the mounted oscillator to the emulation device.

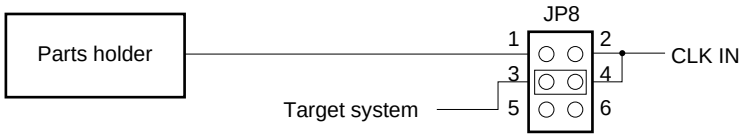
Figure 3-21: IE-78K0-NS-A side



(3) When using an external clock

Short pins 3 and 4 on the IE-78K0-NS-A's jumper (JP8). There is no need to make any settings via the integrated debugger (ID78K0-NS).

Figure 3-22: IE-78K0-NS-A side



3.3.2 Examples of Subsystem Clock Setting

(1) Standard Clock 32.768 KHz offered by the Main Board (G-78009)

Main Board:	JP8 - (5-6)
Emulation Board (IE-78K0-NS-P04):	X1 with shortcut between 6 - 8
ID78K0-NS:	don't care

(2) Clock mounted by the User on the Emulation Board

Main Board:	JP8 - (1-2)
Emulation Board (IE-78K0-NS-P04):	X1 with oscillation circuit
ID78K0-NS:	don't care

(3) External Clock on the Target Hardware

Main Board:	JP8 - (3-4)
Emulation Board (IE-78K0-NS-P04):	X1 with shortcut between 6 - 8
ID78K0-NS:	don't care

3.4 LCD-C/D Resistor Network

In order to use the LCD during the emulation with internal resistors it is necessary to connect the soldered socket (as given in the UM of the 780948 Series) to the socket SO1 on the IE-78K0-NS-P04.

3.5 Jumper Settings on IE-78K0-NS-A

When using the IE-78K0-NS-P04 and the IE-780948-NS-EM4, set the jumpers on the IE-78K0-NS-A as shown below.

Table 3-19: Jumper Settings on IE-78K0-NS-A

	JP2	JP3	JP4	JP6	JP7	JP8
Short	2-3	1-2	1-2	3-4	1-2	5-6

Table 3-20: Jumper Settings on IE-78K0-NS-P04

JP1	JP2	JP6	JP7	JP8	JP9
Open	Open	2-3	1-2	2-3	Open

Table 3-21: Jumper Settings on IE-780948-NS-EM4

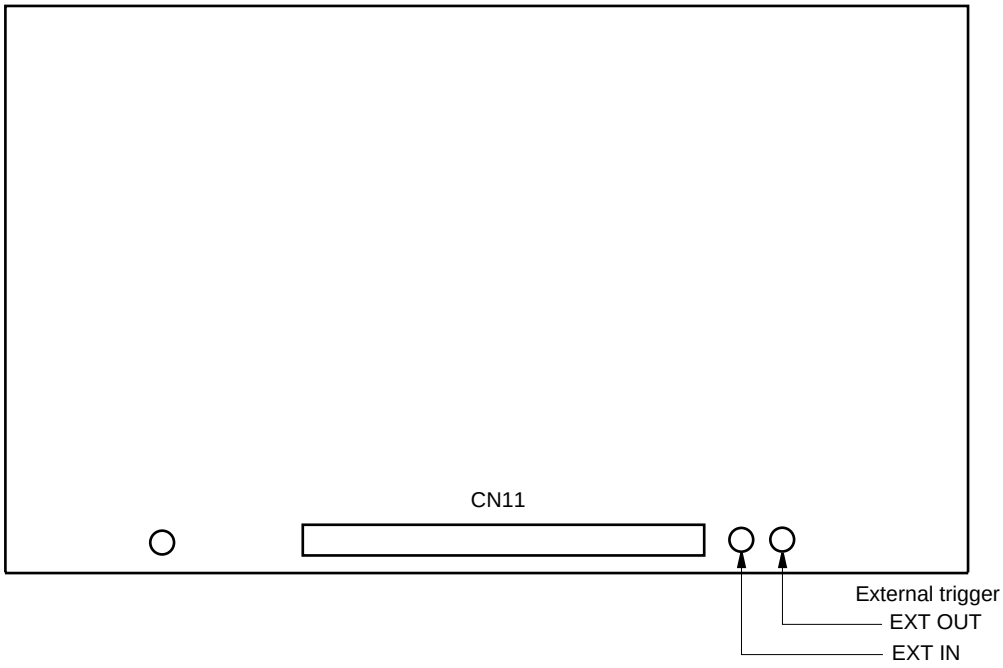
JP1	JP2	JP3
1-2	3-4	1-2

3.6 External Trigger

To set up an external trigger, connect the IE-780948-NS-EM4's check pin, EXTOUT, and EXTIN as shown below.

See the in-circuit emulator (IE-78K0-NS-A) User's Manual for description of related use methods and pin characteristics.

Figure 3-23: External Trigger Input Position



[Memo]

Chapter 4 Differences among Target Devices and Target Interface Circuits

This chapter describes differences between the target device and the IE-78K0-NS-P04 / IE-780948-NS-EM4 target interface circuit.

Although the target device is a CMOS circuit, the IE-78K0-NS-P04/IE-780948-NS-EM4's target interface circuit consists of an emulation chip, TTL, CMOS-IC, and other components.

When connected the IE system with the target system for debugging, the IE system performs emulation so as to operate as the actual target device would operate on the target system.

However, some minor differences exist since the operations are performed via the IE system's emulation.

4.1 Input/Output Signals

<1> Signals which are input or output from the gate array.

<2> Signals which are input or output from the µPD78P0308.

<3> Signals wich are input or output from the µPD780009 emulation CPU

<4> Other signals

The IE system circuit is used as follows for above mentioned signals.

(1) Signals which are input or output from the gate array

P00 to P07
P10/ANI0 to P17/ANI7
P20 to P26
P30 to P33
P40 to P47
P50 to P57
P64, P65, P67
P70 to P77
P120 to P127
P130 to P137
P140 to P147
AV_{DD}/AV_{REF}
AV_{SS}
CRxD

(2) Signals which are input or output from the µPD78P0308

S0 to S39
COM0 to COM4
V_{LC0} to V_{LC2}

(3) Signals which are input or output from the µPD780009 emulation CPU

X1
CL1
$\overline{\text{RESET}}$

(4) Other signals

P34
$V_{DD}0$, $V_{DD}1$
$V_{SS}0$, $V_{SS}1$
X2
CL2
CTxD
V_{PP}/Test

Figure 4-1: Equivalent Circuit 1 from Emulation Circuit

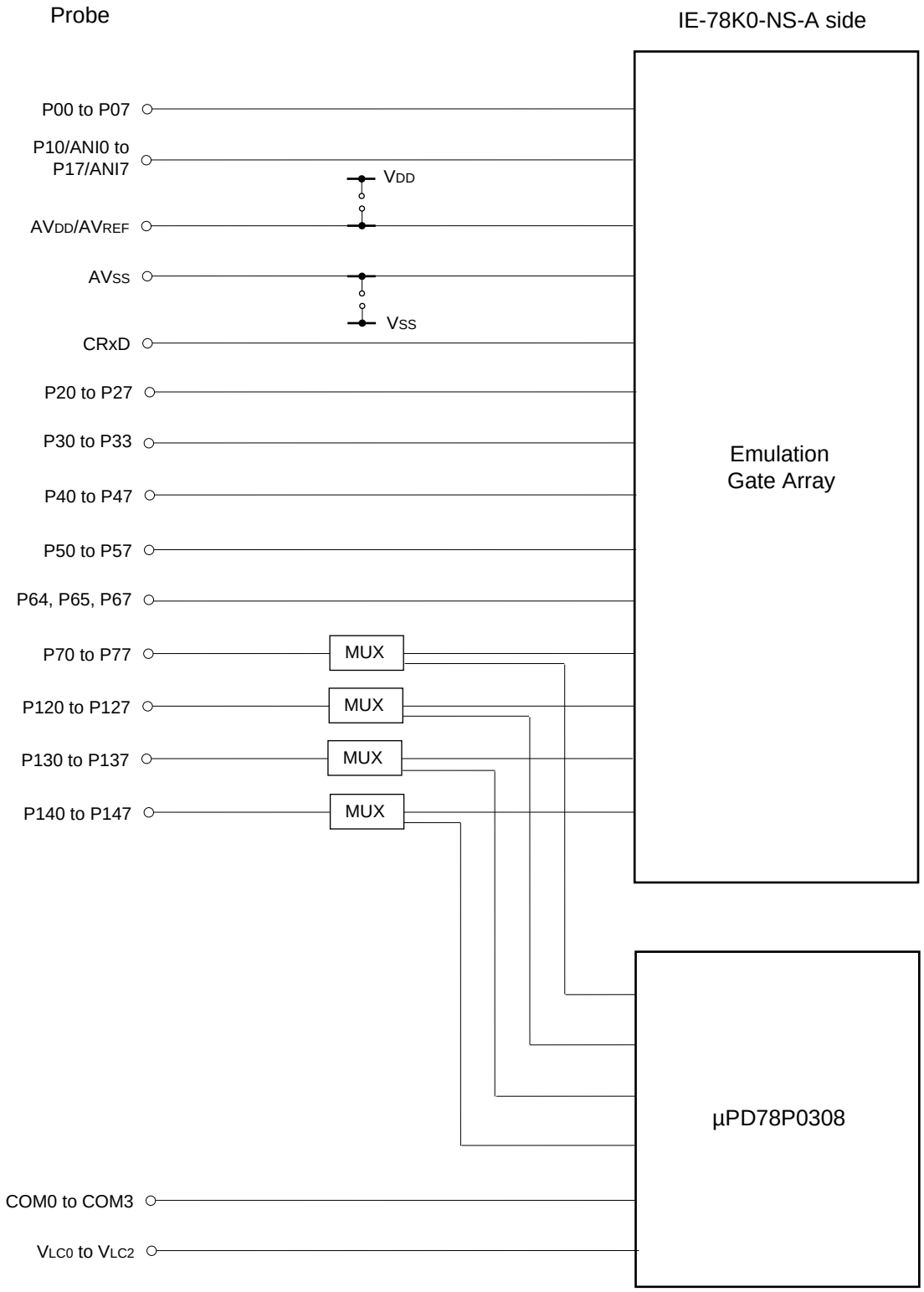


Figure 4-2: Equivalent Circuit 2 from Emulation Circuit

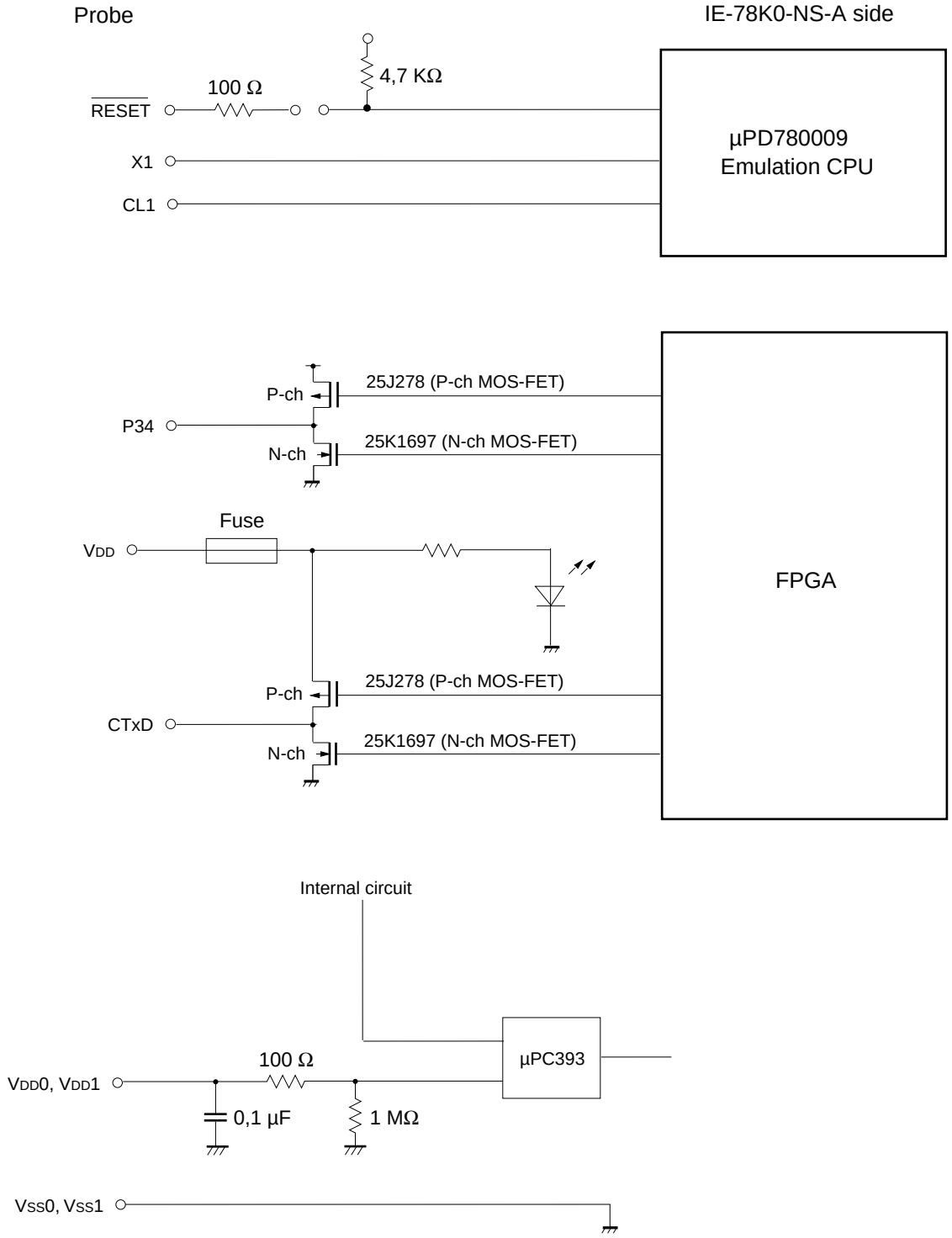
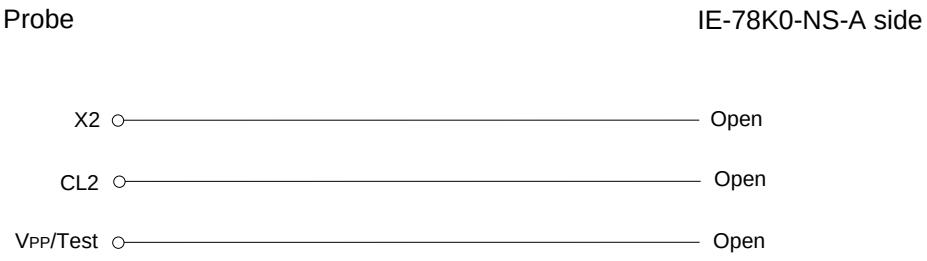


Figure 4-3: Equivalent Circuit 3 from Emulation Circuit



4.2 Differences in Port Functions

(1) Port 13 and 14 of the device are normal CMOS inputs with no hysteresis. The emulator has pins with hysteresis.

(2) The LCD-segment signals S0-S39 are input/output ports of type 17A/17B at the device. The emulator drives these signals by an analog switch.

4.3 Differences in SFR-Registers

Caution: 1. The emulator has a register to emulate the powerfail detection which is not existing at the real chip. The name of the register is DAM0 (SFR-Adr: 0xFF9C). This register has to be set to the value 0x01 by the user program.

2. The emulator has a register for the emulation of the LCD-function. The name of the register is LCDTM (SFR-Adr: 0xFF4A). This register has to be set to the value 0x02 by the user program.

4.4 Target Interface Circuit

The purpose of the target interface circuit is to have the same operations as the target device performed in the IE-78K0-NS-A. It comprises the emulation device and various dates (CMOS, TTL and othes ICs).

When debugging is performed with the target system connected to the IE-78K0-NS-A, the IE-78K0-NS-A target interface circuit performes emulation as though the actual target device were operating in the target system.

The target device has a CMOS LSI configuration. The target interface circuit emulator device also has a CMOS LSI configuration, and is virtually identical to the target device in terms of DC characteristics and AC characteristics (when operating on V_{DD} = 4.0 to 5.5 V).

However, where emulation device signal input/output is performed via gates in the target interface circuit, DC and AC characteristics differ from those of the target device.

In particular, regarding AC characteristics, there is a date delay time (which differs from date to date) each time a gate is passed through.

The above points must be taken into consideration when designing the target system.

Caution: When the IE-78K0-NS-A and IE-78K0-NS-P04 and IE-780948-NS-EM4 are connected to the target system, 4.0 to 5.5 V must be supplied as the target system power supply (V_{DD}).

[Memo]

Chapter 5 Restrictions

1. Starting up the IE system without target board connected makes initial values for ports-indefinite.

2. The RESET value of the CANES register is not correct. As workaround the CANES register has to be reset by software.

[Memo]

Appendix A IE-78K0-NS-P04, IE-780948-NS-EM4 Product Specifications

Product name : IE-78K0-NS-P04, IE-780948-NS-EM4
Operating temperature : 0 to 50 °C
Humidity : 10 to 80% RH (no condensation)
Storage temperature : –15 to +60 °C
Power supply : Power supply capacity : DC 200mA (MAX.) 1.0 W +5 V

Table A-1: Connectors on IE-78K0-NS-P04 Board and IE-780948-NS-EM4 Board

Name	Description (IE-78K0-NS-P04)	Name	Description (IE-780948-NS-EM4)
CN1	Emulator connections	CN5	Emulation board connectors (IE-78K0-NS-P04)
CN2		CN6	
CN3		CN7	
CN4		CN8	
CN5	Probe board connectors (IE-78K0-NS-P04)	CN9	
CN6		CN10	
CN7		CN11	Probe connector
CN8		JP1	Disconnect USER-Reset
CN9		JP2	CAN TxD driver buffer type
CN10		JP3	CAN RxD receive buffer type
CN13			
CN14			
CN15			
CN16			
CN17			
CN18			
JP1	Analog reference voltage		
JP2	GND-pin of A/D Converter		
JP3	Reseved (only for internal use by NEC)		
JP4	JTAG mode selection (only for internal use by NEC)		
JP5	FPGA mode selection		
JP6	JTAG mode selection (only for internal use by NEC)		
JP7	LV_{REF1}		
JP8	LV_{REF0}		

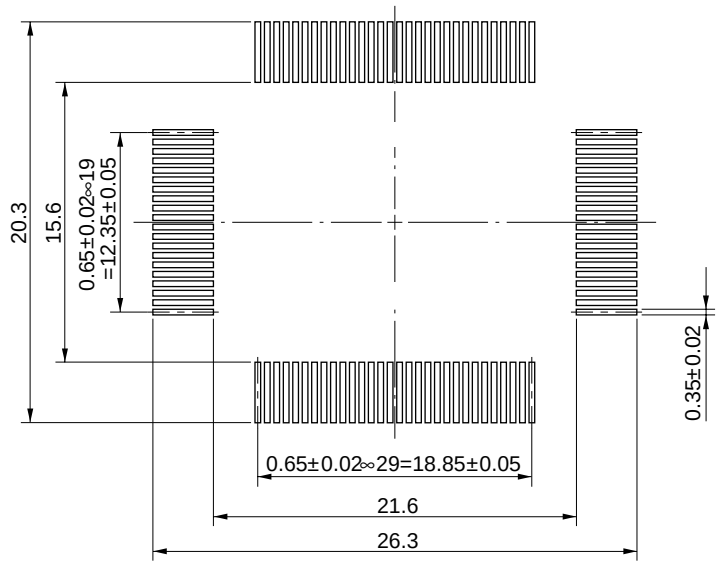
[Memo]

Appendix B Conversion Socket Adapter Package Drawings and recommended Board Mounting Pattern

The following sockets and socket adapters are available for the connection of the probe or device:

- Soldering socket : NQPACK100RB
- Probe adapter : YQPACK100RB
- High adapter : YQSOCKET100RBF
- Device Lid : HQPACK100RB

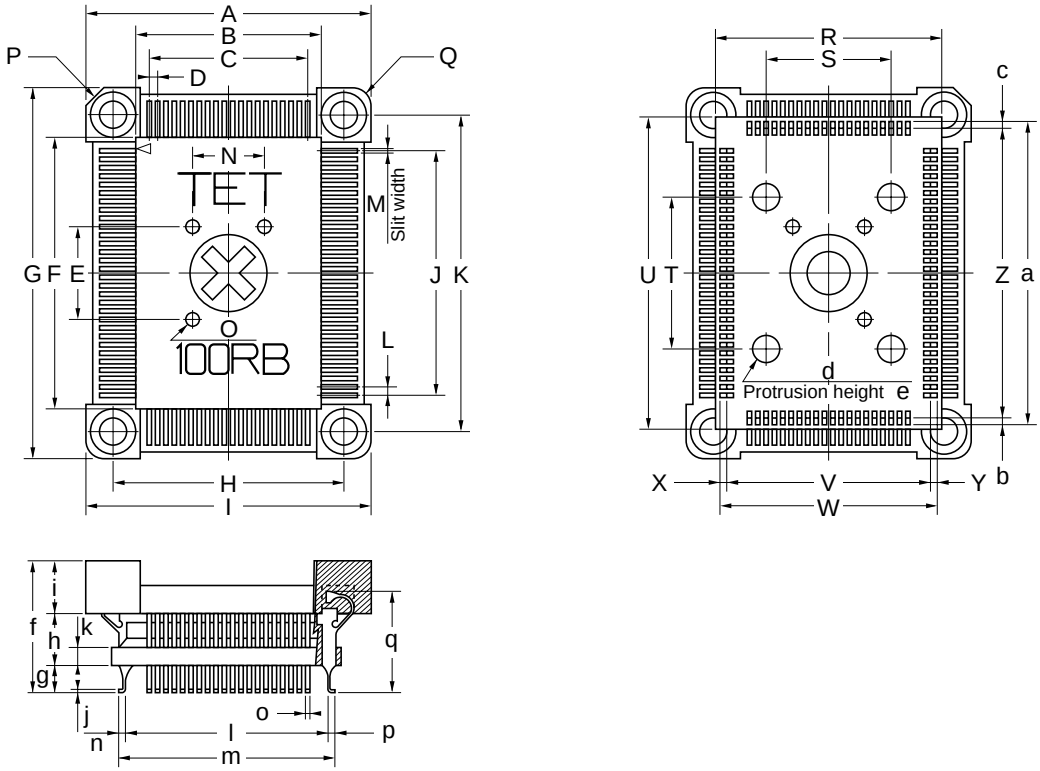
Figure B-1: 100GF Package Drawings (Reference)



NQPACK100RB

Remark: Manufactured by Tokyo Eletech.Corp.

Figure B-2: NQPACK100RB (Target Side) Package Drawings (Reference)



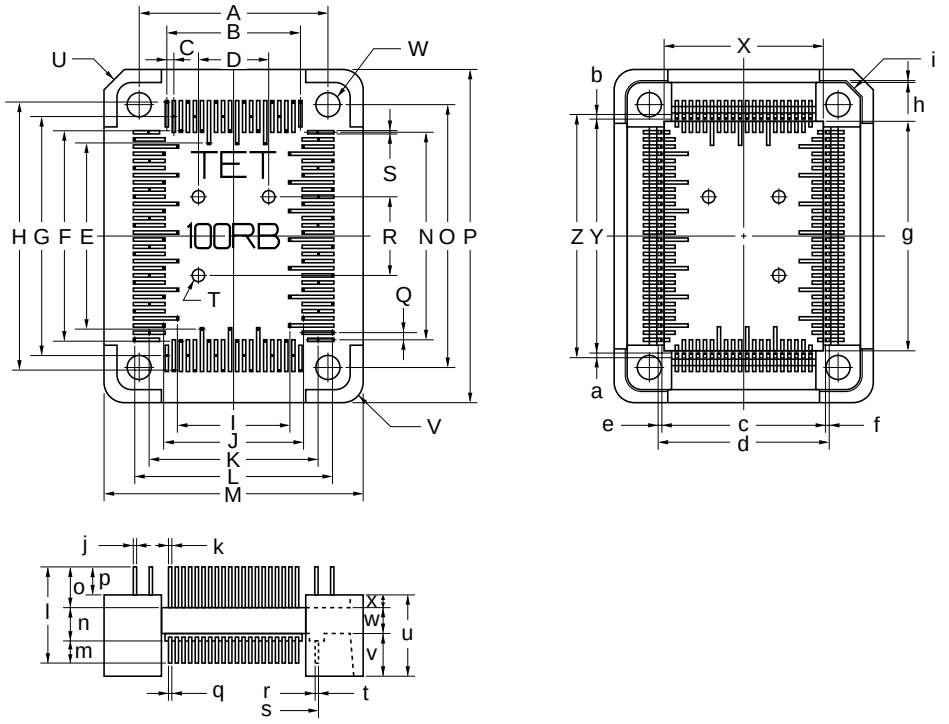
Item	Millimeters	Inches
A	21.75	0.856
B	14.25	0.561
C	0.65x19=12.35	0.026x0.748=0.486
D	0.65	0.026
E	7.0	0.276
F	20.75	0.817
G	28.25	1.112
H	17.4	0.685
I	21.75	0.856
J	0.65x29=18.85	0.026x1.142=0.742
K	23.9	0.941
L	0.65	0.026
M	0.4	0.016
N	6.0	0.236
O	3-ϕ1.0	3-ϕ0.039
P	C 1.5	C 0.059
Q	3-R 1.5	3-R 0.059
R	17.15	0.675
S	10.0	0.394
T	12.0	0.472
U	23.65	0.931
V	15.25	0.600
W	16.25	0.640
X	0.5	0.020
Y	0.5	0.020
Z	21.75	0.856

Item	Millimeters	Inches
a	22.75	0.896
b	0.5	0.020
c	0.5	0.020
d	4-ϕ2.0	4-ϕ0.079
e	1.8	0.071
f	9.45	0.372
g	1.85	0.073
h	3.7	0.146
i	3.9	0.154
j	0.2	0.008
k	1.2	0.047
l	15.25	0.600
m	16.25	0.640
n	0.5	0.020
o	0.25	0.010
p	0.5	0.020
q	6.95	0.274

NQPACK100RB-G1E

Remark: Manufactured by Tokyo Eletech.Corp.

Figure B-3: YQPACK100RB (Probe Side) Package Drawings (Reference)



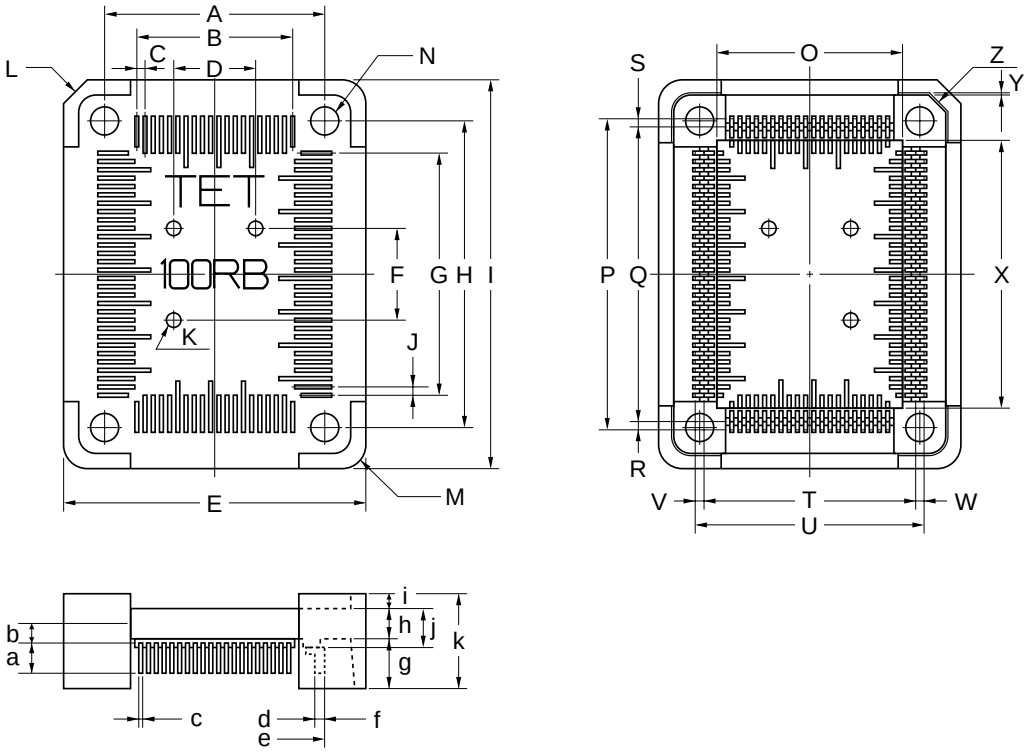
Item	Millimeters	Inches
A	17.4	0.685
B	0.65x19=12.35	0.026x0.748=0.486
C	0.65	0.026
D	6.0	0.236
E	16.85	0.663
F	19.25	0.758
G	21.65	0.852
H	24.05	0.947
I	10.35	0.407
J	12.75	0.502
K	15.15	0.596
L	17.55	0.691
M	23.75	0.935
N	0.65x29=18.85	0.026x1.142=0.742
O	23.9	0.941
P	30.25	1.191
Q	0.65	0.026
R	7.0	0.276
S	0.25	0.010
T	3-ϕ1.0	3-ϕ0.039
U	C 2.0	C 0.079
V	3-R 2.5	3-R 0.098
W	4-ϕ2.2	4-ϕ0.087
X	14.1	0.555
Y	21.25	0.837
Z	22.05	0.868

Item	Millimeters	Inches
a	0.4	0.685
b	0.4	0.026
c	14.75	0.748
d	15.55	0.486
e	0.4	0.016
f	0.4	0.016
g	20.1	0.791
h	0.2	0.008
i	C 1.5	C 0.059
j	0.3	0.012
k	0.25x0.3	0.010x0.012
l	9.0	0.354
m	2.2	0.087
n	3.1	0.122
o	3.7	0.146
p	2.5	0.098
q	0.25	0.010
r	14.75	0.581
s	15.55	0.612
t	0.4	0.016
u	7.4	0.291
v	3.9	0.154
w	2.3	0.091
x	1.2	0.047

YQPACK100RB-G0E

Remark: Manufactured by Tokyo Eletech.Corp.

Figure B-4: HQPACK100RB (TLid for device Mounted) Package Drawings (Reference)



Item	Millimeters	Inches
A	17.4	0.685
B	0.65x19=12.35	0.026x0.748=0.486
C	0.65	0.026
D	6.0	0.236
E	23.75	0.935
F	7.0	0.276
G	0.65x29=18.85	0.026x1.142=0.742
H	23.9	0.941
I	30.25	1.191
J	0.65	0.026
K	3-ϕ1.0	3-ϕ0.039
L	C 2.0	C 0.079
M	3-R 2.5	3-R 0.098
N	4-ϕ2.2	4-ϕ0.087
O	14.1	0.555
P	24.07	0.948
Q	23.07	0.908
R	0.5	0.020
S	0.5	0.020
T	16.57	0.652
U	17.57	0.692
V	0.5	0.020
W	0.5	0.020
X	20.1	0.791
Y	0.2	0.008
Z	C 1.5	C 0.059

Item	Millimeters	Inches
a	2.25	0.089
b	1.6	0.063
c	0.25	0.010
d	16.57	0.652
e	17.57	0.692
f	0.5	0.020
g	3.9	0.154
h	2.3	0.091
i	1.2	0.047
j	3.1	0.122
k	7.4	0.291

HQPACK100RB-G0E

Remark: Manufactured by Tokyo Eletech.Corp.

[Memo]

Appendix C Pin Correspondence Tables of Emulation Probe

Table C-1: Connector CN11 to Emulation Probe (1/2)

No.	Signal Name	Function	No.	Signal Name	Function
1	GND01		2	GND02	
3	ACHSP2(0)	P70/S31	4	ACHSP2(1)	P71/S30
5	BCHSP3(4)	P144/S3	6	BCHSP3(5)	P145/S2
7	EXP1(6)	P56/A14/S33	8	EXP1(7)	P57/A15/S32
9	BCHSP3(6)	P146/S1	10	BCHSP3(7)	P147/S0
11	GND03		12	GND04	
13	EXP1(4)	P54/A12/S35	14	EXP1(5)	P55/A13/S34
15	COM(3)	COM3	16	COM(2)	COM2
17	EXP1(2)	P52/A10/S37	18	EXP1(3)	P53/A11/S36
19	COM(1)	COM1	20	COM(0)	COM0
21	EXP1(0)	P50/A8/S39	22	EXP1(1)	P51/A9/S38
23	VLC(2)	VLC2	24	VLC(1)	VLC1
25	GND05		26	GND06	
27	EXP0(6)	P46/AD6	28	EXP0(7)	P47/AD7
29	VLC(0)	VLC0	30	VCC	VDD1
31	ACHSP2(3)	P73/S28	32	ACHSP2(2)	P72/S29
33	BCHSP3(3)	P143/S4	34	BCHSP3(2)	P142/S5
35	ACHSP2(5)	P75/S26	36	ACHSP2(4)	P74/S27
37	BCHSP3(1)	P141/S6	38	BCHSP3(0)	P140/S7
39	GND07		40	GND08	
41	ACHSP2(7)	P77/S24	42	ACHSP2(6)	P76/S25
43	BCHSP1(7)	P137/S8	44	BCHSP1(6)	P136/S9
45	BCHSP0(1)	P121/S22	46	BCHSP0(0)	P120/S23
47	BCHSP1(5)	P135/S10	48	BCHSP1(4)	P134/S11
49	BCHSP0(3)	P123/S20	50	BCHSP0(2)	P122/S21
51	BCHSP1(3)	P133/S12	52	BCHSP1(2)	P132/S13
53	GND09		54	GND10	
55	BCHSP0(5)	P125/S18	56	BCHSP0(4)	P124/S19
57	BCHSP1(1)	P131/S14	58	BCHSP1(0)	P130/S15
59	BCHSP0(7)	P127/S16	60	BCHSP0(6)	P126/S17
61	ACHSP4(5)	P25/RxD	62	ACHSP4(6)	P26/TxD
63	ACHSP4(3)	P23/SI1/SO1	64	ACHSP4(4)	P24/SCK1
65	URESETH_B	RESET	66	X1LI	X1
67	GND11		68	GND12	
69	ACHSP4(1)	P21/SO0	70	ACHSP4(2)	P22/SCK0
71	NC	X2	72	NC	VPP(/IC)
73	ACHSP1(7)	P07/TI51/TO51	74	ACHSP4(0)	P20/SI0
75	XT1LI	CL1/CCLK	76	NC	CL2
77	ACHSP1(5)	P05/TI00/TO0	78	ACHSP1(6)	P06/TI50/TO50
79	GND	VSS2	80	VCC	VDD2

Table C-1: Connector CN11 to Emulation Probe (2/2)

No.	Signal Name	Function	No.	Signal Name	Function
81	GND13		82	GND14	
83	ACHSP1(3)	P03/INTP3/T2P0	84	ACHSP1(4)	P04/INTP4/TI01
85	AAVREF0	AVREF	86	AANI(0)	P10/ANI0
87	ACHSP1(1)	P01/INTP1	88	ACHSP1(2)	P02/INTP2
89	AANI(1)	P11/AANI1	90	AANI(2)	P12/ANI2
91	EXP0(4)	P44/AD4	92	EXP0(5)	P45/AD5
93	GND	VSS1	94	BCHSP2(4)	P34/SGO/SGOF
95	GND15		96	GND16	
97	EXP0(2)	P42/AD2	98	EXP0(3)	P43/AD3
99	BCHSP2(3)	P33/PCL/SGOA	100	BCHSP2(2)	P32/TI22
101	EXP0(0)	P40/AD0	102	EXP0(1)	P41/AD1
103	BCHSP2(1)	P31/TI21	104	BCHSP2(0)	P30/TI20
105	EXP2(6)	P65/WR	106	EXP2(7)	P67/ASTB
107	AAVSS	AVSS	108	AANI(7)	P17/ANI7
109	GND17		110	GND18	
111	CRXD	CRxD	112	EXP2(4)	P64/RD
113	AANI(6)	P16/ANI6	114	AANI(5)	P15/ANI5
115	ACHSP1(0)	P00/INTP0	116	CTXD	CTxD
117	AANI(4)	P14/ANI4	118	AANI(3)	P13/ANI3
119	GND19		120	GND20	

Remark: The meaning of the symbols and figures in the Emulation Probe column is as follows:
GND: Ground clip
NC: Not connected
1–120: Emulation probe tip pin numbers

[Memo]

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