User Guide

DA7219 Ultra Low Power Codec with advanced accessory detect

UG-DA7219 Performance Evaluation Board

Contents

1 Terms and definitions

BCLK	Bit Clock
GND	Ground reference
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Circuit Sound
MCLK	Master Clock
MCU	Micro-controller Unit
MIC	Microphone
PCB	Printed Circuit Board
TRS	Tip-Ring-Sleeve (refers to the connector arrangement of the three-pin audio jack)
TRRS	Tip-Ring-Ring- Sleeve (refers to the connector arrangement of the four-pin audio jack)
WCLK	Word Clock

2 References

1. DA7219 datasheet
2. DA7219 schematics, layout & SmartCanvas™ GUI software
3. DA7219 - Advanced Accessory Detection widget and configuration

3 Introduction

The DA7219 Evaluation Board (284-02-C) has been designed to allow measurement and functional testing of the DA7219 device.

All analogue and digital audio functionalities are contained within the DA7219 Evaluation Board (EVB) as well as the control interface.

The EVB can be controlled via a PC using the on-board USB microcontroller or from a host system via the provided headers.

The EVB is supplied with a USB memory stick containing supporting documentation and the Windows based control GUI to allow the user to configure the DA7219.

The GUI is called SmartCanvas™. It uses a simple graphical interface, allowing the DA7219 to be controlled via a PC. A SmartCanvas user guide is available upon installation.

The EVB has a number of jumper links to allow the user to change the system configuration enabling them to make required measurements. Configuration options are described in detail in this document.

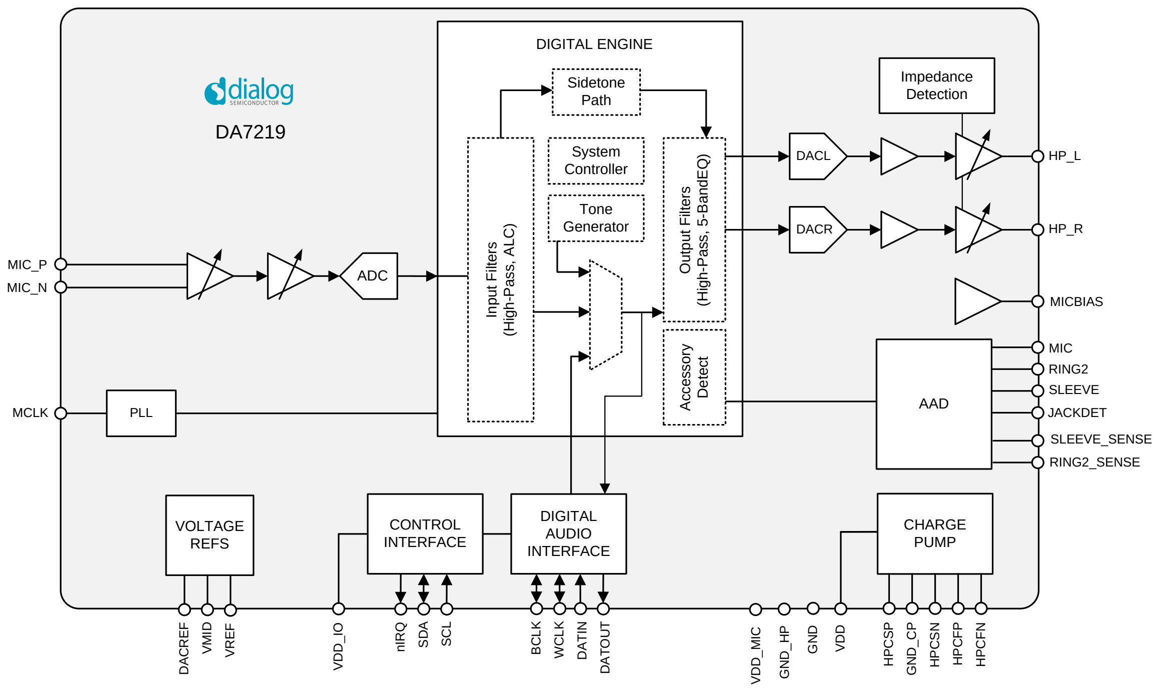


Figure 1: DA7219 block diagram

4 Summary

This document provides information about the DA7219 Ultra Low Power Codec Performance EVB that will enable you to use it in a number of ways to carry out performance measurements and functional checks.

The hardware version referenced throughout this document is:

- DA7219 Performance Board 284-02-C

This document is limited to detailing the hardware of the DA7219 Performance Board 284-02-C only. It should be used in conjunction with the DA7219 datasheet and SmartCanvas™ GUI User Guide.

5 DA7219 Performance Board Hardware Description

The DA7219 Evaluation Board consists of the DA7219 device, the essential external components, analogue interconnects and a USB interface for digital interconnects as shown in Figure 2.

This board can be used standalone or as a module for interface to a customer development platform.

The EVB is configured by default to work 'out-of –the–box' from the USB and powered from the on-board regulators.

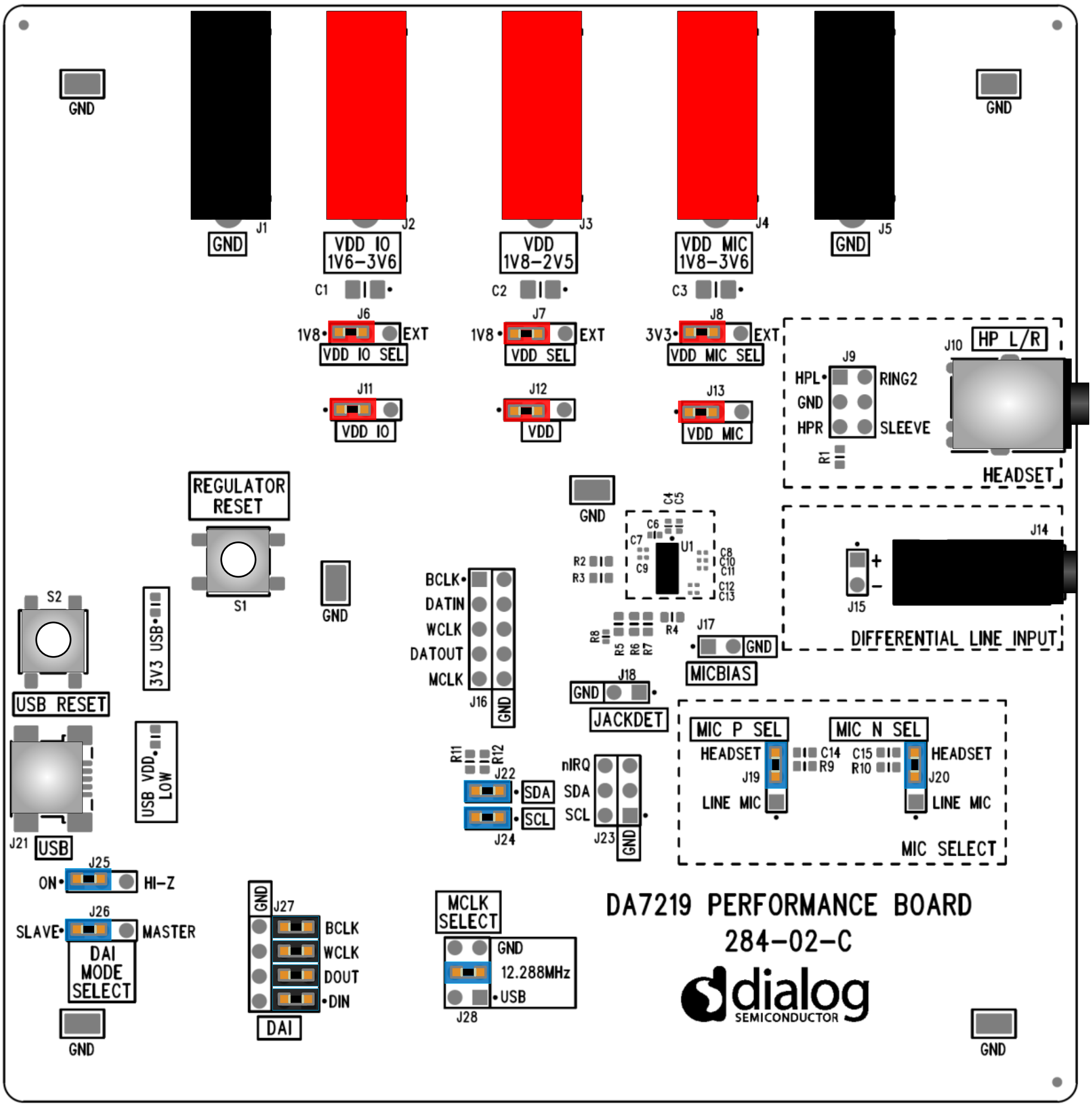


Figure 2: DA7219 default jumper positions (Red = Power; Blue = Signal)

5.1 Power Supply

The DA7219 EVB can be powered from the on-board regulators via the USB port or externally via the connectors J1 to J5. The on-board regulators can be reset by de-pressing switch S1 on the evaluation board. Selection of the supply from the on-board regulators or the external source is determined by the position of jumpers on J6, J7 and J8.

An external current monitor can be placed across each of the supplies by removing the appropriate jumper (pins 1&2) on J11, J12 and J13, also the voltage level of each supply can be monitored on pin 3 of the same connetors.

An example is shown in Figure 3 where an external power supply has been connected to J4 and J5 to supply VDD_MIC, this is configured via J8 which is set to external. VDD and VDD_IO have been selected to be powered from on-board regulators via the jumper settings on J6 and J7.

The voltage on VDD being measured via pin 3 of J12.

The current to VDD_IO being measured by replacing the jumper on pins 1 and 2 of J11 with an ammeter.

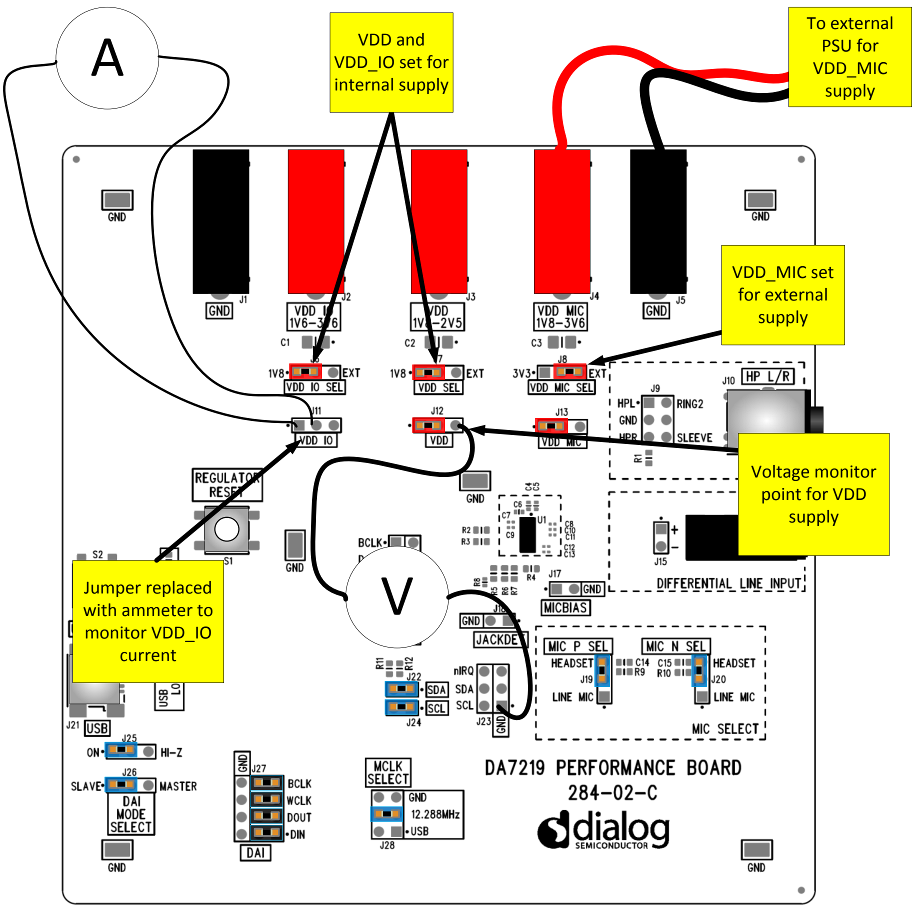


Figure 3: DA7219 current and voltage measurement example

5.2 MCLK Source

The Master Clock (MCLK) for the device can be provided in three ways via J28. It is important to note that only one connection should be made at any time on J28.

The default configuration is via an on-board 12.288MHz oscillator which is selected by populating a jumper link on pins 3 and 4 of J28 as shown in Figure 4.

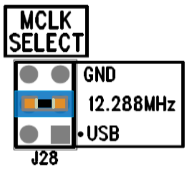


Figure 4: On-board oscillator selected as MCLK source

To select MCLK from the USB interface, populate a jumper link on pins 1 and 2 of J28 as shown in Figure 5.

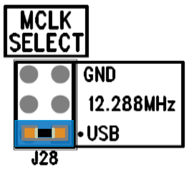


Figure 5: USB selected as MCLK source

To use an external clock, remove all jumper links from J28 and provide the external clock to pin 6 of J28 and an associated GND to pin 5 of J28 as shown in Figure 6.

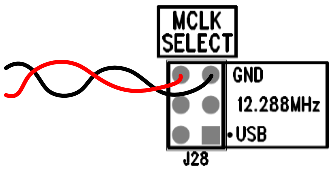


Figure 6: External clock as MCLK source

The MCLK connections on J28 are buffered via a level shifter to allow level translation to occur if required. By default the level shifter acts only as a buffer (both sides are at VDD_IO level).

MCLK can also be provided directly to the device by removing R11 and supplying MCLK directly to pin 9 of J16.

It is recommended that a twisted pair with GND approach is used when applying external clocks to maintain signal externally.

5.3 Interfaces

5.3.1 USB Interface

The DA7219 EVB uses an ATMEL SAM3U micro-controller as the USB transceiver, programmed to deliver the following functionality:

1. I2C/SPI control interfaces
2. I2S Audio Interface for audio streaming over USB

The USB transceiver is powered by an on-board regulator U8. Pressing the USB RESET switch S2 shuts down regulator U8, disconnecting the 3v3 supply from the SAM3U and the other on-board regulators during the push phase.

The I2S audio streaming sample rates supported by the SAM3U USB transceiver are 8 KHz – 96 KHz at 16-bit word long.

5.3.2 Digital Audio Interface (DAI)

The DAI interface is used to receive and transmit the audio data between the DA7219 and external development platform.

The DAI interface consists of a Word Clock (WCLK), a data clock (BCLK), a serial data input (DIN) and a serial data output (DOUT).

The DAI is routed to the device via J27. In the default configuration a jumper is fitted between rows A and B to connect the DAI interface to the SAM3U micro-controller for USB playback and record as shown in Figure 7.

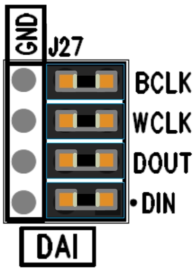


Figure 7: USB used as the DAI signal source

Removing the jumper on J27 allows an external DAI interface to be connected via row B (centre pins).

It is recommended that a twisted pair with GND approach is used for each separate signal when applying external DAI signals to maintain signal externally as shown in Figure 8.

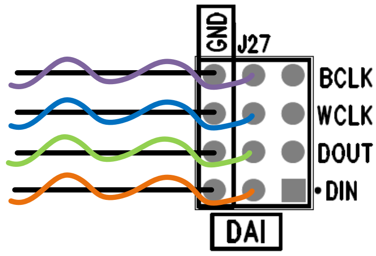


Figure 8: External signals used as the DAI signal source

The DAI connections on J27 are buffered via level shifters to allow level translation to occur if required. By default the level shifters act only as a buffer (both sides are at VDD_IO level). The direction of the DAI level shifters is determined by jumper J26 and should be set depending on whether the device is in Master or Slave mode.

The DAI connections can also be provided directly to the device via J16 as shown in Figure 9. When using J16, the level shifters are bypassed so voltage levels applied must match the VDD_IO of the DA7219.

When providing signals directly to the DAI interface of the device, ensure that pins 2 and 3 of J25 are shorted setting the output of the level-shifter to Hi-Z.

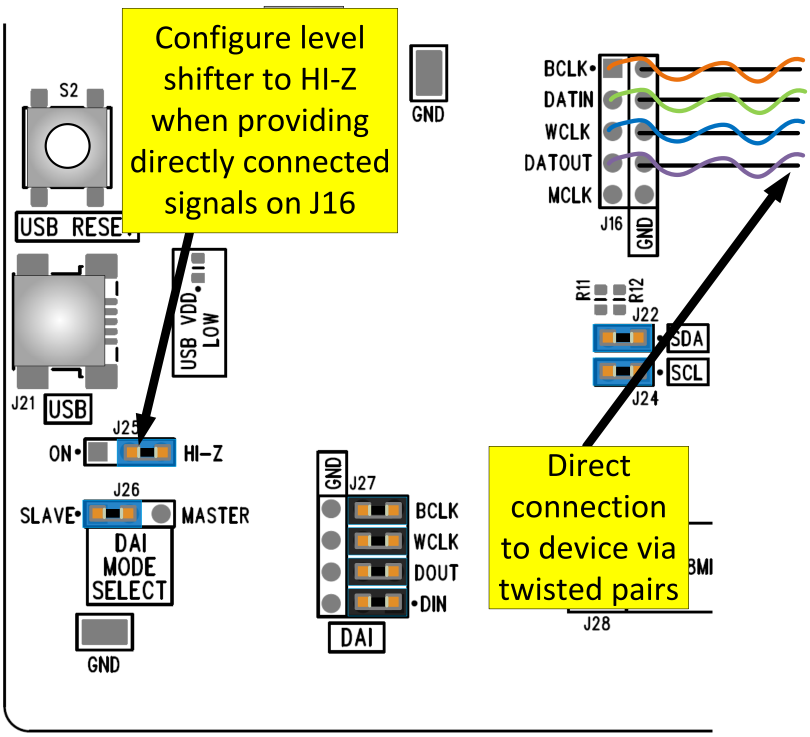


Figure 9: Configuration for directly connected DAI or MCLK signals

5.3.3 I2C Interface

Command and configuration data to and from the device is sent via the I2C interface on the SAM3U micro-controller using the SmartCanvas™ GUI via the USB interface.

The I2C interface consists of a data clock (SCL) and a serial data input/output (SDA).

When external I2C connectivity is required, this can be provided via pin 2 (SCL) and pin 4 (SDA) on J23.

To disconnect any I2C activity from the SAM3U when external I2C connectivity is needed, remove the jumpers on J22 and J24.

Pull-up resistors are provided for the I2C interface on the evaluation board. If they are not required due to support elsewhere in the connecting system, resistors in sites R5 and R6 should be removed.

It is recommended that a twisted pair with GND approach is used for each separate signal when applying external SDA and SCL signals to maintain signal externally.

5.4 Quick Reference

The board component placement is shown in Figure 10. A summary of the connection options is listed in Table 1.

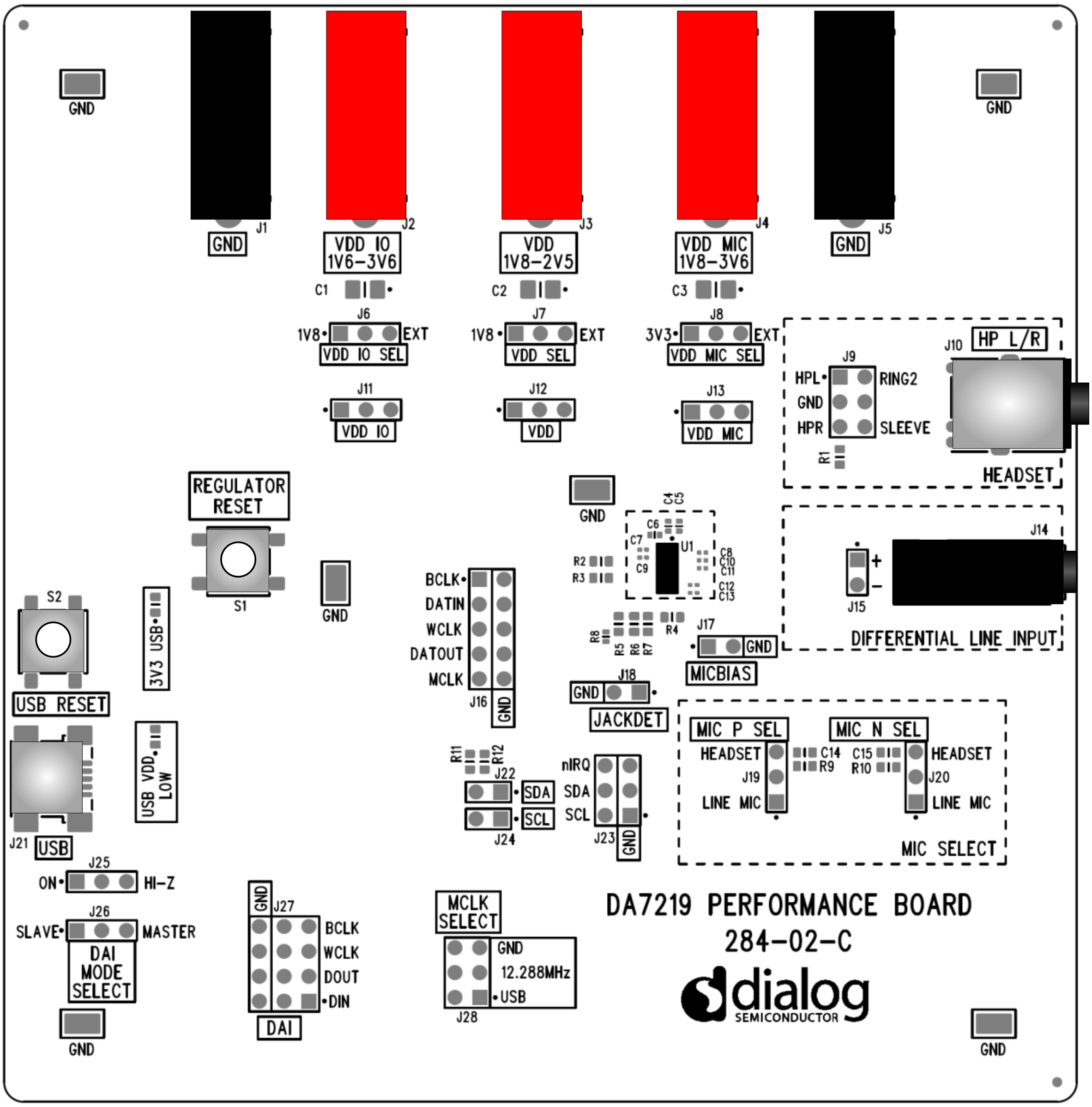


Figure 10 DA7219 performance board connector summary

Table 1 Connector Summary

Connector	Functionality	Description
J1-J5	External power supply connections	J1 = GND (0V) J2 = VDD_IO (+1.6V to +3.6V) J3 = VDD (+1.8V to +2.5V) J4 = VDD_MIC (+1.8V to +3.6V) J5 = GND [1]*Refer to footnote*
J6	VDD_IO power source select	VDD_IO SEL **1-2 = on-board 1.8V regulator (Default)** 2-3 = external supply via J2
J7	VDD power source select	VDD SEL **1-2 = on-board 1.8V regulator (Default)** 2-3 = external supply via J3
J8	VDD_MIC power source select	VDD_MIC SEL **1-2 = on-board 3.3V regulator (Default)** 2-3 = external supply via J4
J9	Headset connection monitor and connection points	Pin 1 = HPL; Pin 2 = RING2; Pin 3 = GND, Pin 4 = GND; Pin 5 = HPR, Pin 6 = SLEEVE
J10	4-pole headset jack socket	Tip = Headphone Left; Ring1 = Headphone Right; Ring2 = GND/MIC; Sleeve = MIC/GND
J11	VDD_IO monitoring point	VDD IO **1-2 = VDD_IO supply. Replace jumper with ammeter for current measurement. (Default)** 3: VDD_IO voltage monitoring pin
J12	VDD monitoring point	VDD **1-2 = VDD supply. Replace jumper with ammeter for current measurement. (Default)** 3: VDD voltage monitoring pin
J13	VDD_MIC monitoring point	VDD MIC **1-2 = VDD_MIC supply. Replace jumper with ammeter for current measurement. (Default)** 3: VDD_MIC voltage monitoring pin
J14	Differential input jack socket	Tip = Mic P; Ring = Mic N; Sleeve = GND
J15	Differential input connection points	Pin 1 = Positive; Pin 2 = Negative

[1] Note that when supplying power to these sockets and monitoring the current to these supplies, the reading will have an additional current offset (current=supply voltage at socket/4000 Ohms) due to on board current monitoring devices on each supply. To measure the current to the device without an offset, use an ammeter to monitor the supplies at J11, J12 and J13.

J16	Digital audio interface – direct connection to DA7219	Pin 1 = BCLK; Pin 3 = DATIN; Pin 5 = WCLK; Pin 7 = DATOUT; Pin 9 = MCLK Pins 2, 4, 6, 8 = GND
J17	MICBIAS monitoring point	Pin 1 = MICBIAS; Pin 2 = GND
J18	JACKDET monitor point	Pin 1 = JACKDET; Pin 2 = GND
J19	Positive microphone input source select	MIC P SEL 1-2 = Differential line input jack (J15/J14) **2-3 = Headset (J10) (Default)**
J20	Negative microphone input source select	MIC N SEL 1-2 = Differential line input jack (J15/J14) **2-3 = Headset (J10) (Default)**
J21	Mini USB connector	Provides power and communication to device via a PC
J22	SCL source	SCL **1-2 = I2C SCL comes from USB interface (Default)** Open = External source (via J23)
J23	SDA source	SDA **1-2 = I2C SDA comes from USB interface (Default)** Open = External source (via J23)
J24	I2C and nIRQ monitoring and connection points	Pin 2 = SCL; Pin 4 = SDA; Pin 6 = nIRQ Pins 1, 3, 5 = GND
J25	Buffer output state for external signal connection	**1-2 = DAI inputs connect to J27 (Default)** 2-3 = Buffer in Hi-Z (J27 disconnected)
J26	Digital audio interface Master/Slave select	DAI MODE SELECT **1-2 = DA7219 is a DAI Slave (Default)** 2-3 = DA7219 is the DAI Master
J27	Digital audio interface – connection to DA7219 via a level-shift	DAI **1-2 = Connect USB DIN to DIN (Default)** **4-5 = Connect USB DOUT to DOUT (Default)** **7-8 = Connect USB WCLK to WCLK (Default)** **10-11 = Connect USB BCLK to BCLK (Default)** Pins 3, 4, 9, 12 = GND for connecting external DAI connections
J28	MCLK source selection	MCLK SELECT 1-2 = USB MCLK **3-4 = 12.288MHz on-board oscillator (Default)** Pin 5: GND Pin 6: Connection for external MCLK

6 Example scripts

An example of a typical setup file is shown in this section which sets up the device to stream 48 KHz, 16-bit audio, over USB from a PC using the evaluation board and GUI software.

The scripts also handle accessory detection and in the case of a 4 pole headset, the audio from the microphone is sent over the DAI to the PC via USB where it can be recorded.

The scripts are split into a number of sections to explain how the device should be typically setup.

The first section is shown in Figure 11, this script takes the device out of standby and sets up the references, PLL and digital audio interface.

```
//
// Take device out of standby mode, setup PLL and DAI interface //
//
WRITE  DA7219 0xFD   0x01   //Enable ACTIVE mode to take device out of standby
WRITE  DA7219 0x13   0x01   //Set I2C repeat mode-address+data is sent for each write
WRITE  DA7219 0x91   0x01   //Set IO Level 1.5-2.5V
WRITE  DA7219 0x32   0x08   //Enable references - Master BIAS + VMID
WRITE  DA7219 0x22   0x18   //Set PLL divider value, FRAC_TOP for 12MHz MCLK
WRITE  DA7219 0x23   0x93   //Set PLL divider value , FRAC_BOT for 12MHz MCLK
WRITE  DA7219 0x24   0x20   //Set PLL divider value, INTEGER for 12MHz MCLK
WRITE  DA7219 0x20   0x88   //Enabled PLL in SRM mode, PLL INDIV= 10-20MHz
WRITE  DA7219 0x17   0x0B   //Set 48kHz sample rate
WRITE  DA7219 0x2C   0xA0   //DAI Enabled, DAI Channel 1L and 1R enabled, 16bit, I2S
```

Figure 11: Configuration script for active mod, PLL and DAI setup

The second part shown in Figure 12, enables the ADC and accessory detection.

At this point when the user plugs in a jack, the device detects if a 3 pole or 4 pole jack is inserted. In the case of a 4 pole jack, the mic and ground pin wiring is automatically detected by the device. Mic bias is then only then turned on for the 4 pole detection case, this ensures that power not wasted by turning on the mic bias supply when it is not needed.

```
//
// Setup ADC, MIC bias@2V2 (enabled when 4 pole jack inserted) and accessory detect
//
WRITE  DA7219 0x33   0x01   //Enable L_MIXIN
WRITE  DA7219 0x2A   0x00   //Left and Right DAI channels contain ADC data
WRITE  DA7219 0x50   0x55   //Enable MIC, MIXIN and ADC
WRITE  DA7219 0x62   0x0B   //Set MIC_BIAS-Output on only when 4 pole jack detected
WRITE  DA7219 0xC6   0xD7   //Turn on accesory detect
WRITE  DA7219 0xC7   0x00   //configure accessory detect
```

Figure 12: Configuration script for ADC, MIC bias and accessory detect

An interrupt request is then set at this stage so that the host controlling the device can then be woken up to send scripts to enable the headphone outputs. This is done to ensure that the headphone outputs are turned on in a controlled way so that no pops or clicks are heard when inserting the jack into the socket and is shown in Figure 13.

```
//
// After the accessory has been detected, the host sends the following code to enable
// the headphone outputs to ensure there are no pops and clicks
//
WRITE  DA7219 0x47   0xE0   //Enable Charge Pump DAC VOL mode
WRITE  DA7219 0x4B   0x01   //MIXOUTL enabled
WRITE  DA7219 0x4C   0x01   //MIXOUTR enabled
WRITE  DA7219 0x6E   0x80   //MIXOUTL_CTRL enabled
WRITE  DA7219 0x6F   0x80   //MIXOUTR_CTRL enabled
WRITE  DA7219 0x69   0x88   //DAC_L_CTRL enabled
WRITE  DA7219 0x6A   0x80   //DAC_R_CTRL enabled
WRITE  DA7219 0x6B   0xC8   //HP_L_CTRL enabled
WRITE  DA7219 0x6C   0xC8   //HP_R_CTRL enabled
WRITE  DA7219 0x51   0xF1   //Enable stereo DAC, MIXOUT and HP
```

Figure 13: Configuration script to enable the headphone outputs

The accessory detection sequence for enabling/disabling the headphone outputs and mic bias is automatically handled in a Linux driver which is available from Dialog.

The device has a similar sequence for handling jack removal, the host is signalled that the jack is being removed and the host signals to the system controller in the device that the audio outputs should be turned off. The device initiates a sequence internally where the mic bias can be turned off, I2S is disabled, the DAC is muted and the headphone outputs are disabled. The sequence is done in this way to ensure no pops or clicks are heard when inserting or removing the jack,

A full demo of the capabilities of the accessory detection, performance for pop-free insertion/removal, button detection (4 button Android specification) and impedance measurement is available in the GUI under the Plugins pull-down menu – Advanced Accessory Detect.

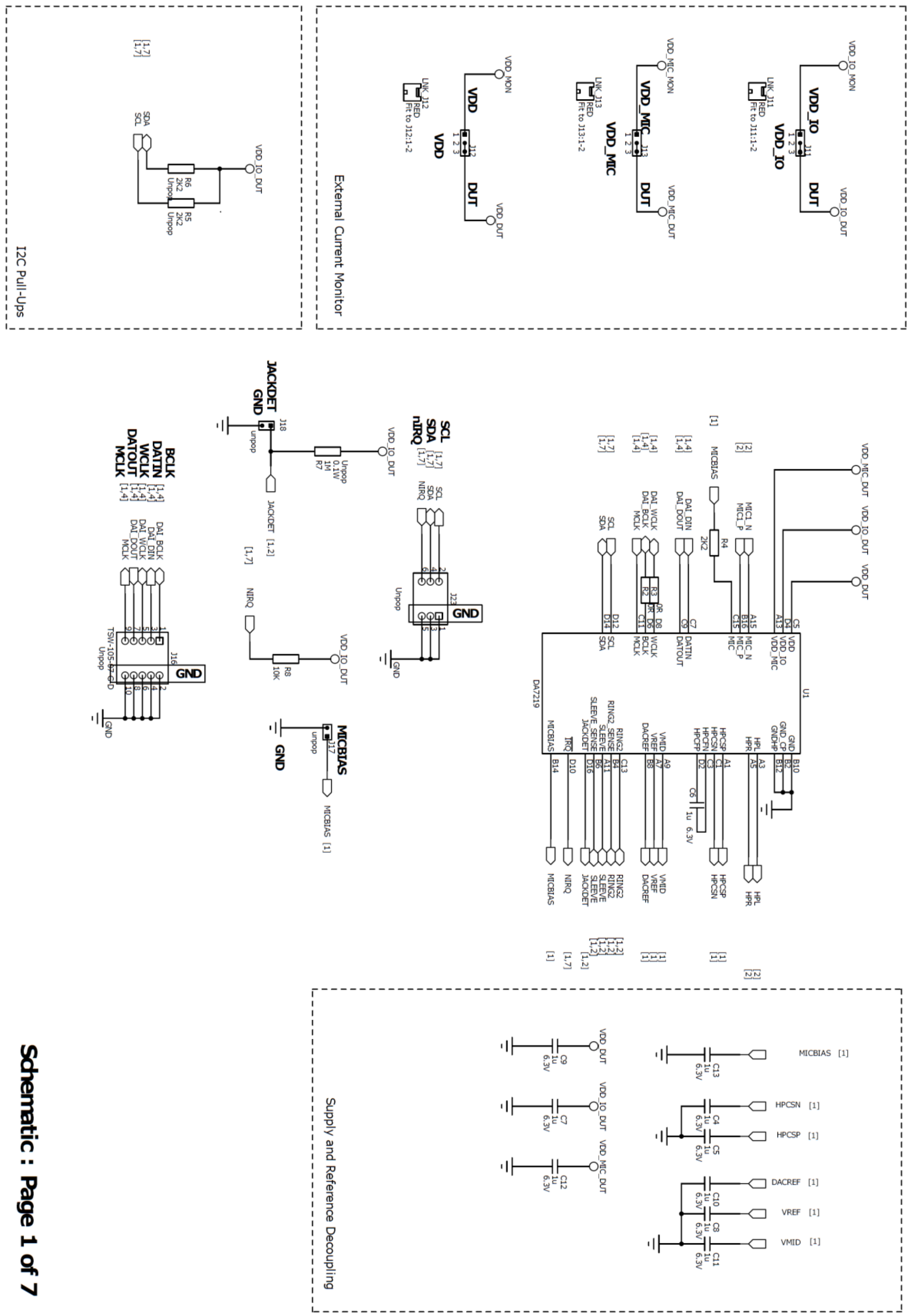
Please ensure windows sound driver is set for 48 KHz 16-bit audio when using the demo, please refer to the advanced accessory detection widget and configuration document.

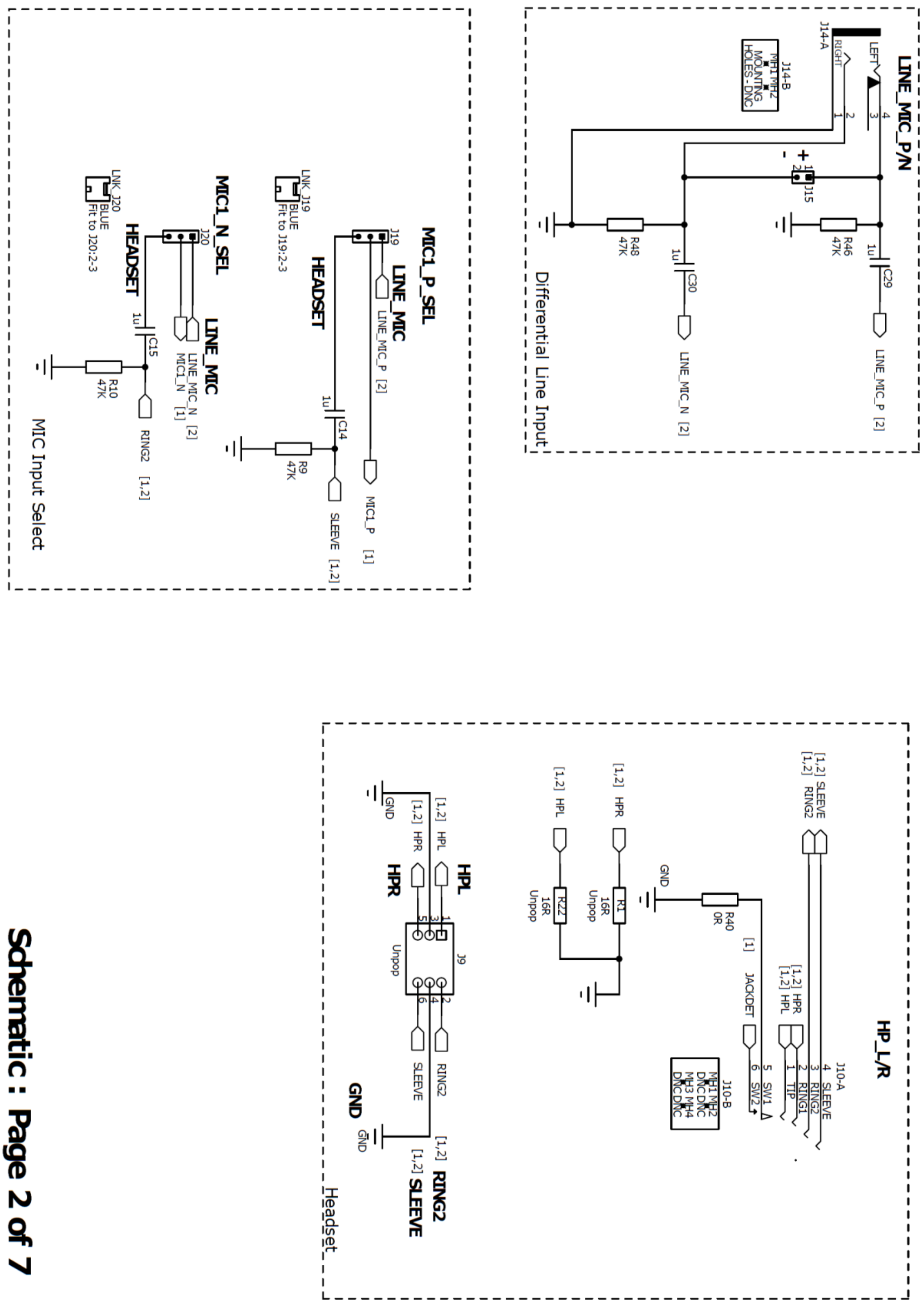
A quick overview of the sequence for pop-free operation using the GUI is shown below.

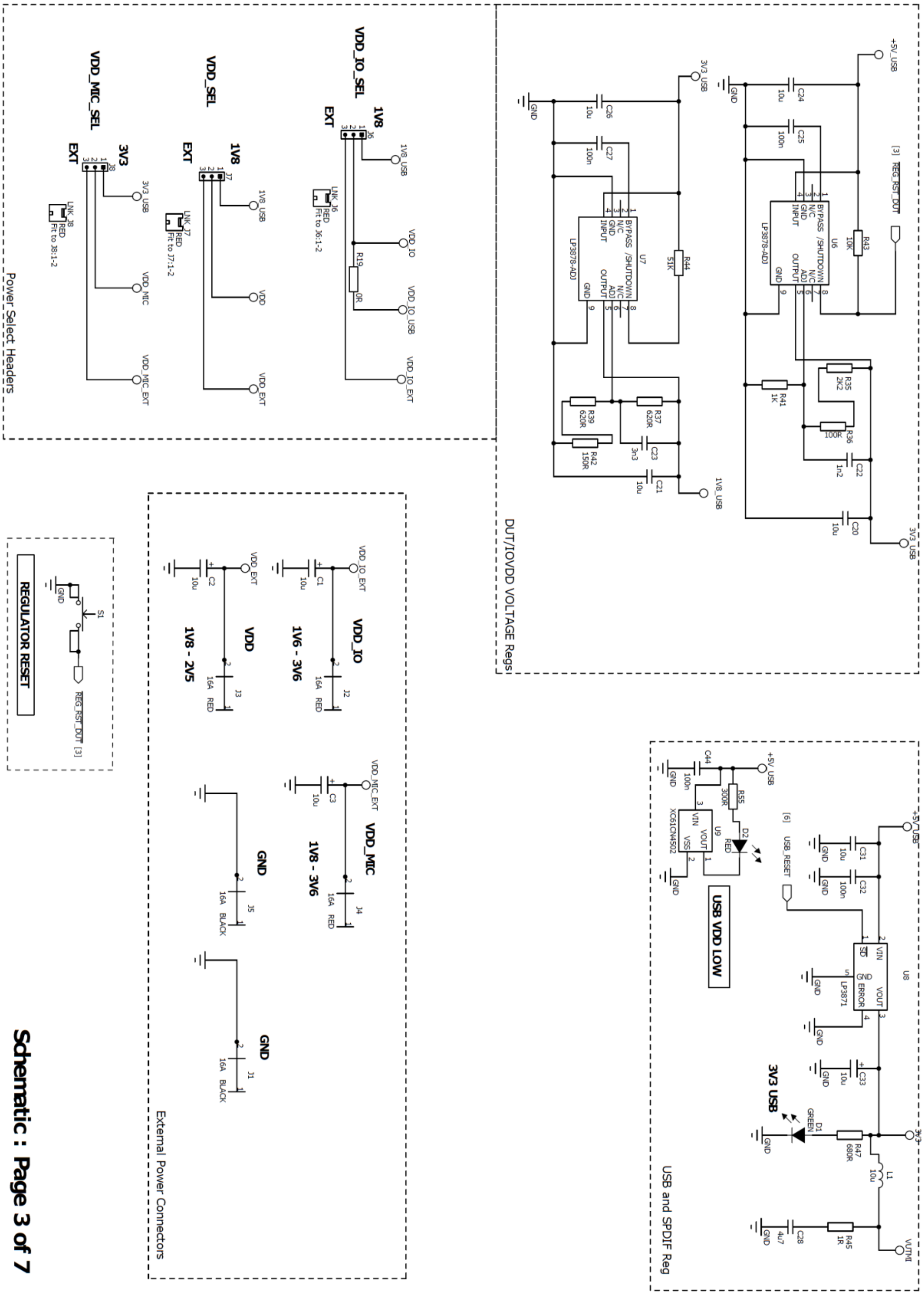
1. On insertion of the jack, the nIRQ line from the DA7219 is pulled low. This line is connected to a GPIO on the SAM3U (MCU).
2. The software polls this register in the SAM3U to see if an interrupt occurs.
3. If an interrupt occurs we determine what type of interrupt it is:
    a. Jack insertion has begun
        - The jack is been inserted but has not been fully inserted
        - In this instance we keep polling until the jack has been fully inserted
    b. Jack is fully inserted
        - We now run the impedance detection routine as we need to determine if the jack is a headphone (<1000 Ohms) or line (>1000 Ohms)
        - Switch the tone generator to drive the DAC and headphone path
        - Drive out a slow SRAMP tone at -15dB
        - The DA7219 now measures the current taken by the headphone amp and determines the load dependant on the trigger level threshold in our case 1000 Ohms
        - The software now unmutes the headphones and DAC and you should hear the I2S audio been played. This transition is pop free, however you can hear low level switching of the DAC/HP path.

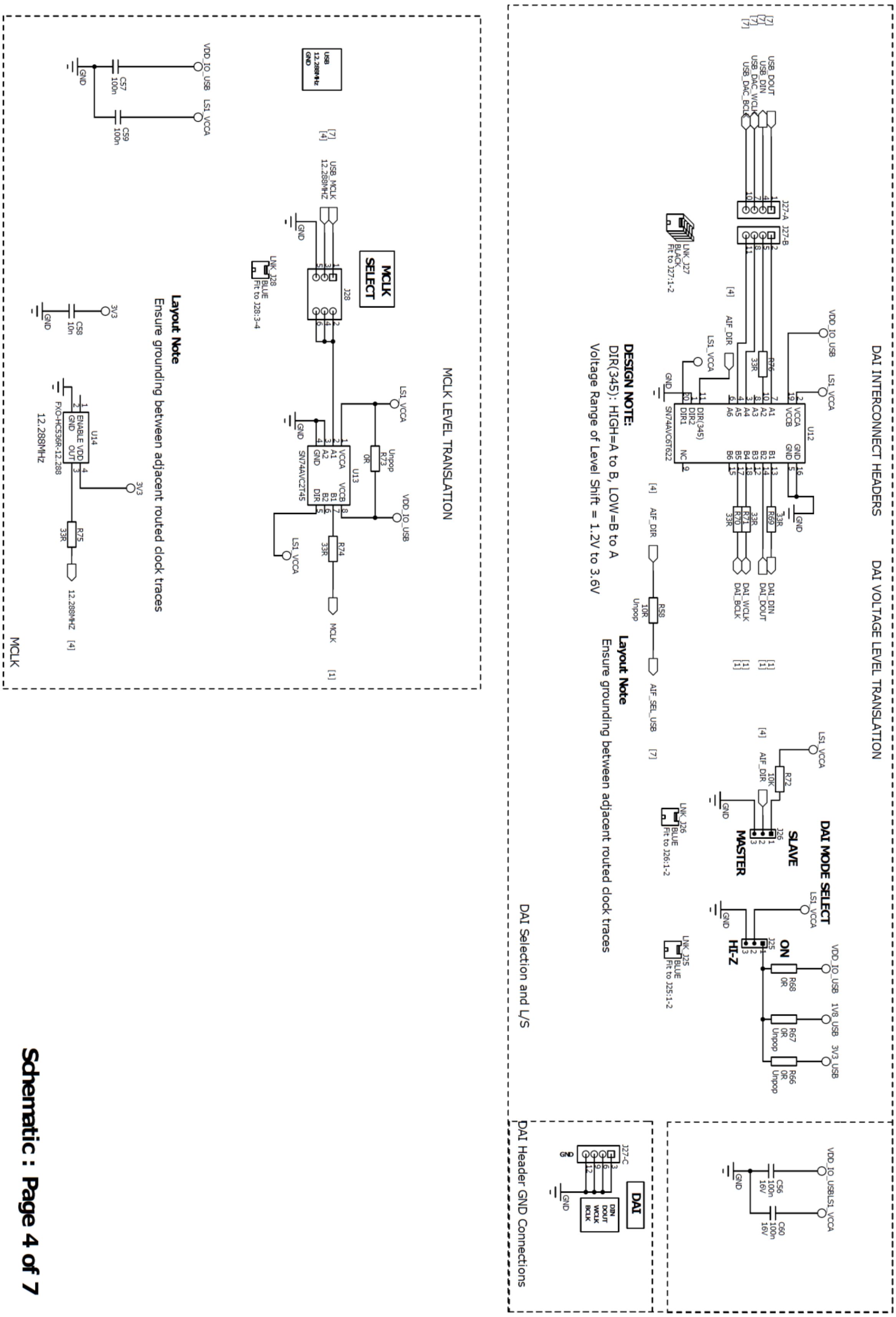
    c. Jack removal
    The system controller inside the DA7219 is signalled to turn off the outputs, this initiates a sequence which turns off the following blocks to ensure a pop free sequence on the headphone outputs
        - Disables I2S out
        - Mutes DAC
        - Turns off MICBIAS
        - Mutes Headphone

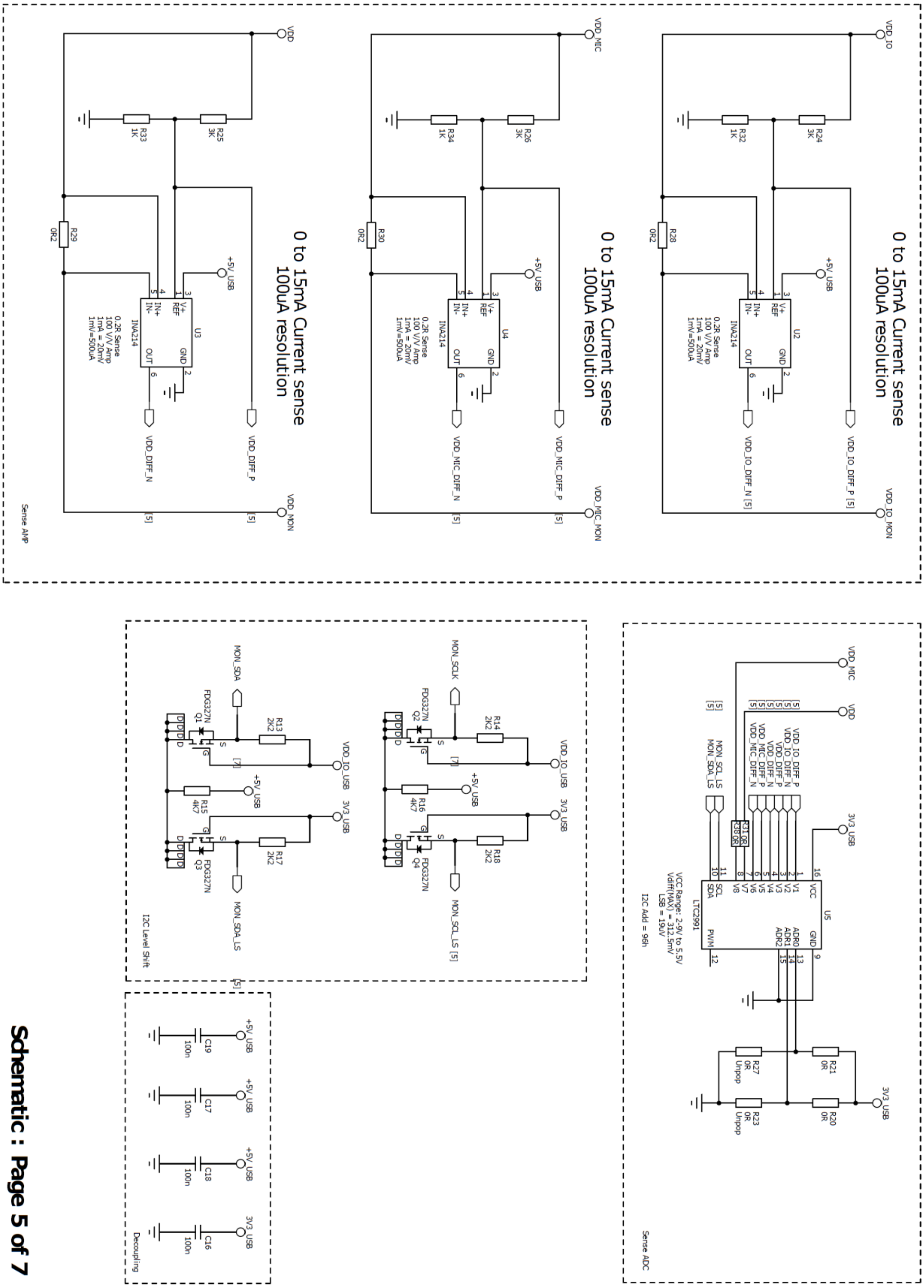
7 Schematic diagrams

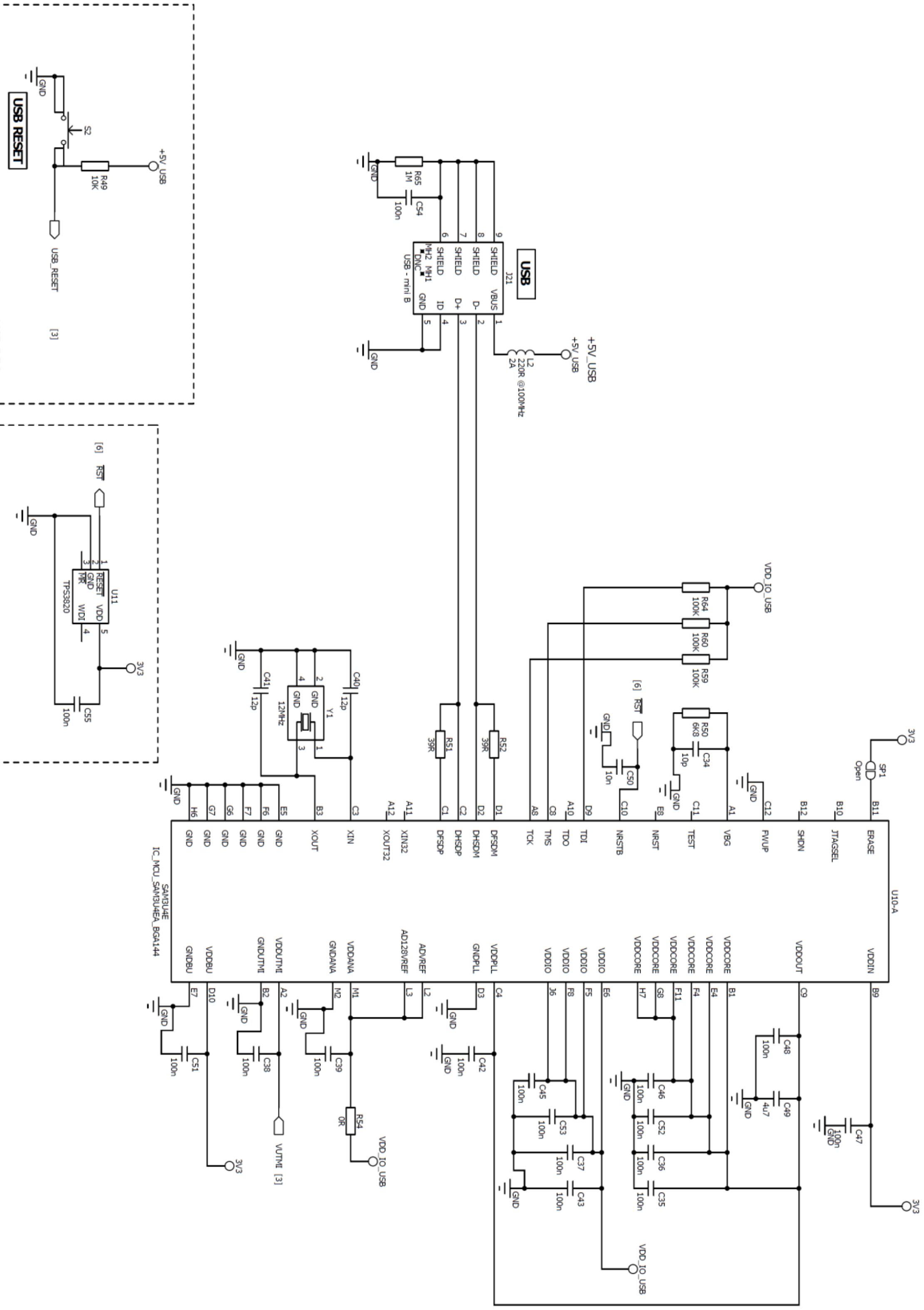



MIC Input Select
MIC1_N_SEL
MIC1_P_SEL
LINE_MIC
HEADSET
Differential Line Input
LINE_MIC_P/N
HP_L/R
HPL
HPR
RING2
SLEEVE
GND
Headset
Schematic : Page 2 of 7

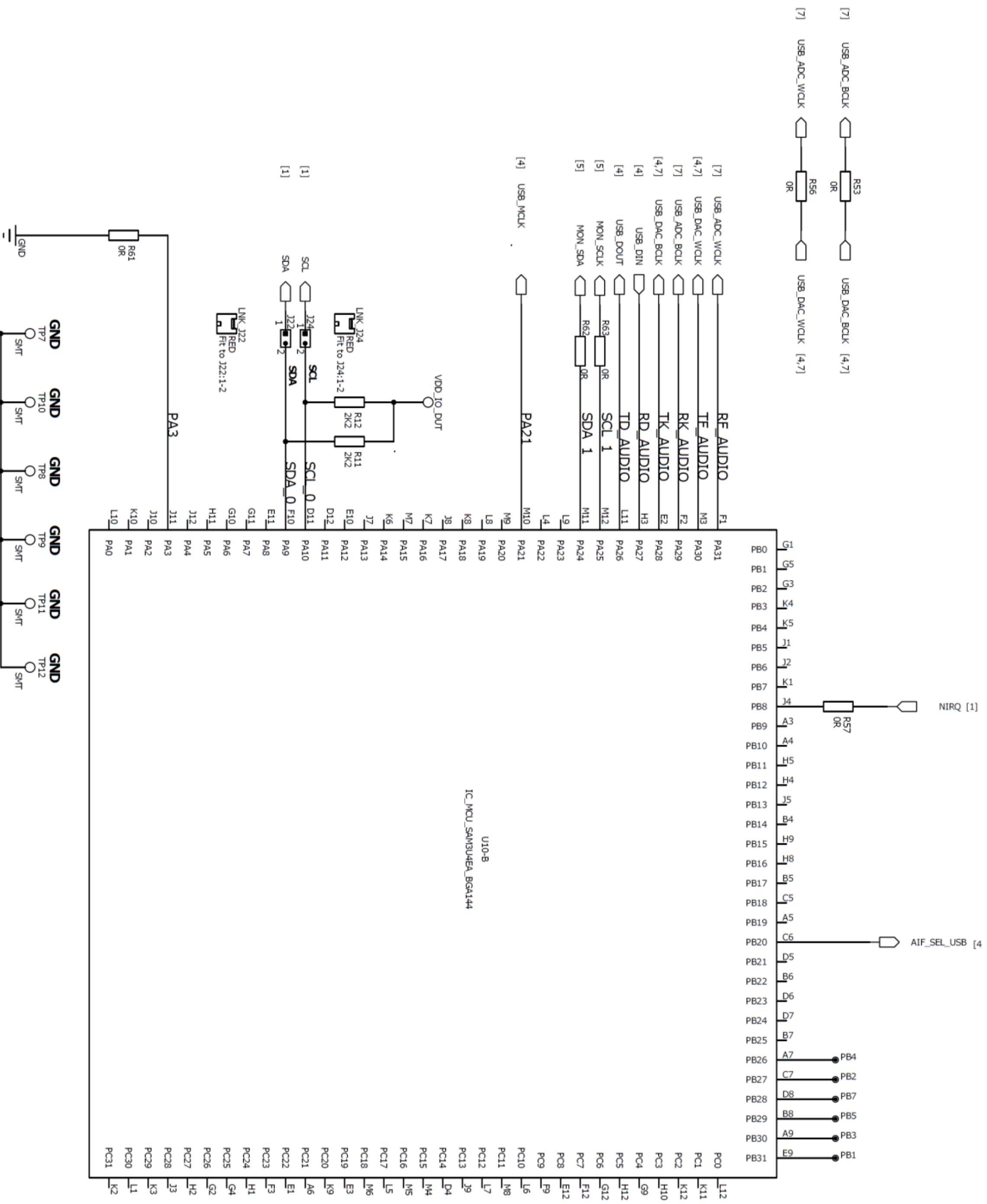

Schematic : Page 3 of 7
Power Select Headers
VDD_IO_SEL
VDD_SEL
VDD_MIC_SEL
DUT/IOVDD VOLTAGE Regs
LP3878-ADJ
REGULATOR RESET
External Power Connectors
VDD_IO
1V6 - 3V6
VDD
1V8 - 2V5
VDD_MIC
1V8 - 3V6
GND
USB and SPDIF Reg
USB VDD LOW
3V3 USB
LP3871


DAI INTERCONNECT HEADERS
DAI VOLTAGE LEVEL TRANSLATION
DESIGN NOTE:
DIR(345): HIGH=A to B, LOW=B to A
Voltage Range of Level Shift = 1.2V to 3.6V
Layout Note
Ensure grounding between adjacent routed clock traces
DAI MODE SELECT
SLAVE
MASTER
ON
HI-Z
DAI Selection and L/S
DAI
DAI Header GND Connections
MCLK LEVEL TRANSLATION
MCLK SELECT
Layout Note
Ensure grounding between adjacent routed clock traces
MCLK
Schematic : Page 4 of 7


0 to 15mA Current sense
100uA resolution
0 to 15mA Current sense
100uA resolution
0 to 15mA Current sense
100uA resolution
Sense AMP
I2C Level Shift
Decoupling
Sense ADC
Schematic : Page 5 of 7



Schematic : Page 6 of 7



Schematic : Page 7 of 7

8 Revision history

Revision	Date	Originator	Change
1	18-Nov-2015	JM	Initial Release
1.1	27-Jan-2022		Updated logo, disclaimer, copyright.

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

RoHS Compliance

Dialog Semiconductor complies to European Directive 2001/95/EC and from 2 January 2013 onwards to European Directive 2011/65/EU concerning Restriction of Hazardous Substances (RoHS/RoHS2).
Dialog Semiconductor's statement on RoHS can be found on the customer portal https://support.diasemi.com/. RoHS certificates from our suppliers are available on request.