Restrictions:
IDTs ZSPM4011/12/13 Evaluation Kit is designed for evaluation of the ZSPM4011/ZSPM4012/ZSMP4013, laboratory setup, and module development only. This kit must not be used for module production and production test setups. IDT shall not be liable for any damages arising out of defects resulting from (i) delivered hardware (ii) non-observance of instructions contained in this manual, or (iii) misuse, abuse, use under abnormal conditions or alteration by anyone other than IDT. To the extent permitted by law, IDT hereby expressly disclaims and User expressly waives any and all warranties, whether express, implied, or statutory, including, without limitation, implied warranties of merchantability and of fitness for a particular purpose, statutory warranty of non-infringement and any other warranty that may arise by reason of usage of trade, custom or course of dealing.

Contents

1 Kit Contents

- ZSPM4011/12/13 Evaluation Board
- Kit User Guide

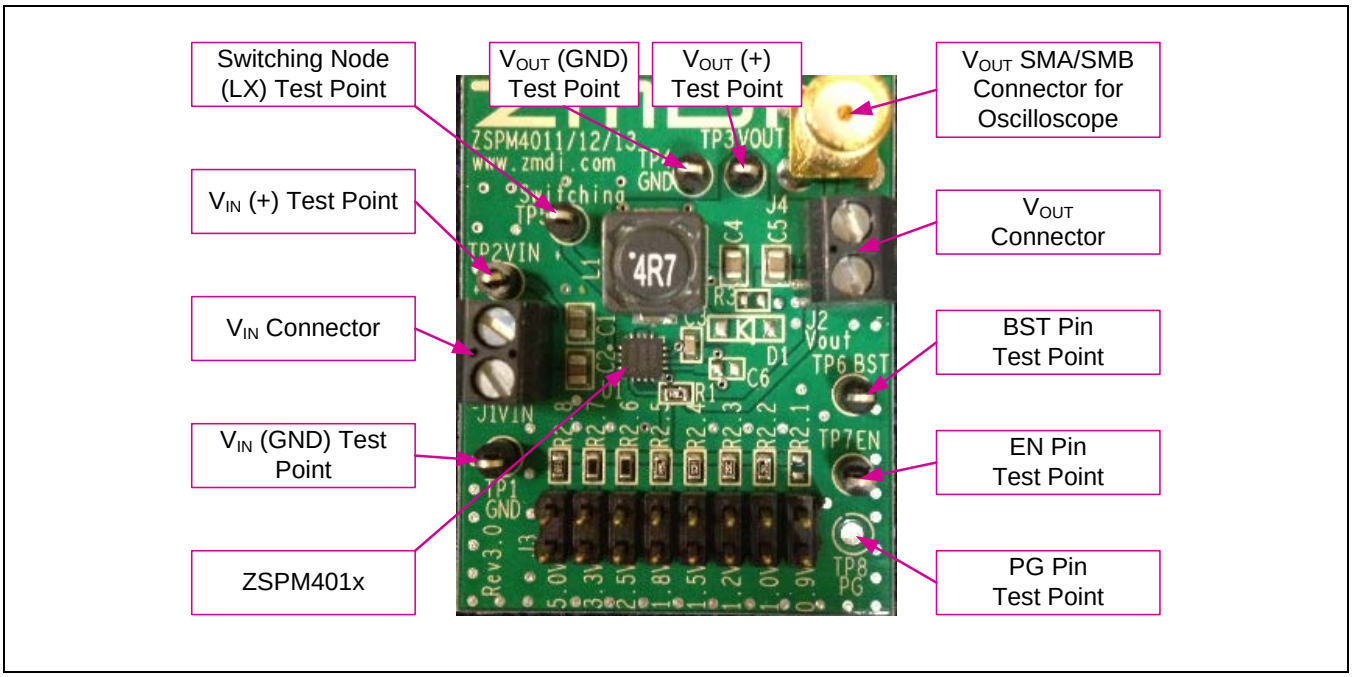
2 Introduction

The ZSPM4011/12/13 Evaluation Board is a complete, self-contained system to measure the performance and operating characteristics of the ZSPM4011, ZSPM4012, and ZSPM4013 switch mode regulators. The board contains various test points and jumpers to evaluate all functions of the devices.

3 General Overview

The input voltage for the board is supplied via J1 connector as shown in the picture below, Vin(+) is on the top pin and Vin (GND) is on the bottom pin of this connector. The output of the power supply is set via jumpers on J3, and J2 can be used to connect any appropriate load to this power supply.

Figure 3.1 Overview of ZSPM4011/12/13 Evaluation Board



4 Setup

The setup for the ZSPM4011/12/13 Demonstration Board is very simple. An input voltage is applied at J1 and the output voltage is supplied at J2. The board is enabled by floating the TP7EN test point, or applying a voltage above 2V. If TP7EN is pulled to GND, the device is disabled and input current should drop below 10uA.

The output voltage is adjusted by sizing R2 and R3 feedback resistors.

The equation for the output voltage is

$$Vout = 0.9 * \left(1 + \left(\frac{R1}{R2.x}\right)\right)$$

For example, values of R2.x=3.3kΩ and R3=1.1kΩ provide a 1.2V output at J2. A jumper set, J3, allows selection of discrete resistor values for R2.x to program the output voltage to 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V.

4.1. Board Connectors

The board contains the following banana jack connectors for external signals and supplies:

J1: The input supply voltage for the board.

J2: Output voltage from the regulator.

J4: SMA, SMB, or Johnson Jack connection to Vout for connecting to oscilloscope to measure Vout ripple and transient response.

4.2. Test and Probe Points

The board contains the following test/probe points:

TP2VIN+: Input supply voltage to the board.

TP3VOUT: Output voltage from the regulator.

TP1&4GND: Ground connections for the board. All of the GND test points are shorted together and the GND pin of the IC.

TP5 Switching: Connects to the VSW pin and is used to evaluate the switching node of the regulator.

TP6BST: Connects to the BST pin and is used to evaluate the bootstrap switching node of the regulator.

TP7EN: Connects directly to the Enable pin. The input range on the EN pin is 0-5V typical. If this pin is pulled to GND, the IC will turn off, and if it is pulled to above 2V , the IC will remain on.

TP8PG: Connects directly to PG pin. If R1 is installed, there is a pull-up to VOUT. The voltage range on the PG pin is 0-5V typical.

5 Board Options

5.1. Input Capacitor Selection

There are locations for five different types and sizes of input capacitors on the board to evaluate different ESR and capacitances for the application. One capacitor should be low ESR ceramic type, with a minimum of 10uF recommended. The input capacitor locations are: C1, and C2.

5.2. Output Capacitor Selection

There are locations for four different types and sizes of output capacitors. Low ESR single or parallel ceramic capacitors are recommended to keep the output ripple low. However, other capacitors can be evaluated. One capacitor should be of low ESR ceramic type. Locations are C4 and C5.

5.3. Schottky Diode

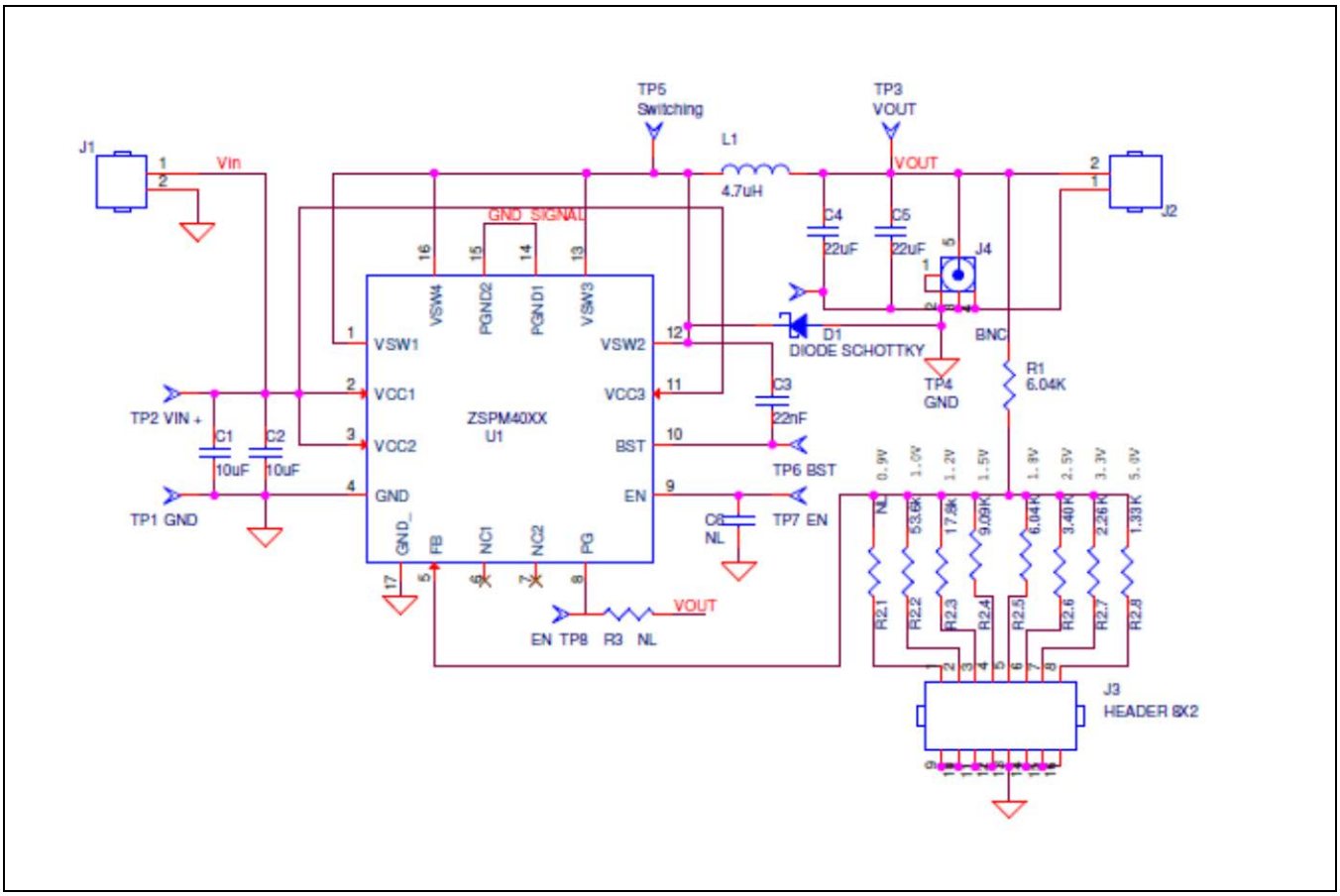
While D1 is not required, it can be populated to increase efficiency and provide a better load regulation. Care should be taken to select a diode that is able to handle the output current supplied by the regulator.

5.4. PG Pull-up

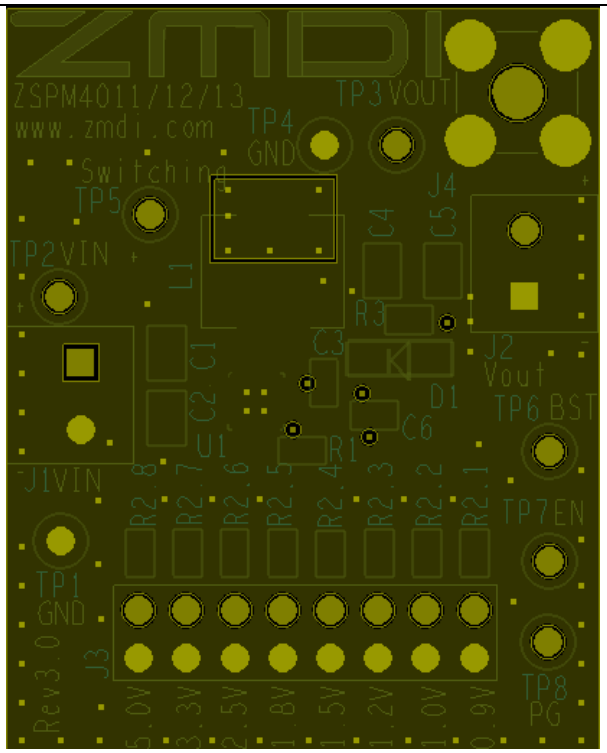
The PG output is an open drain output. R3 can be populated to provide a pull-up to the VOUT supply.

6 Evaluation Board Schematic

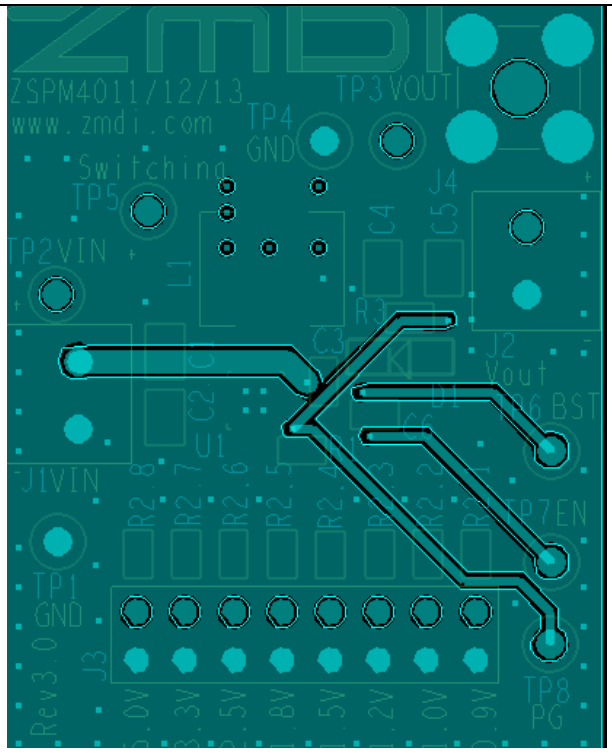
Figure 6.1Schematic for the ZSPM4011/12/13 Evaluation Board Revision 3.0



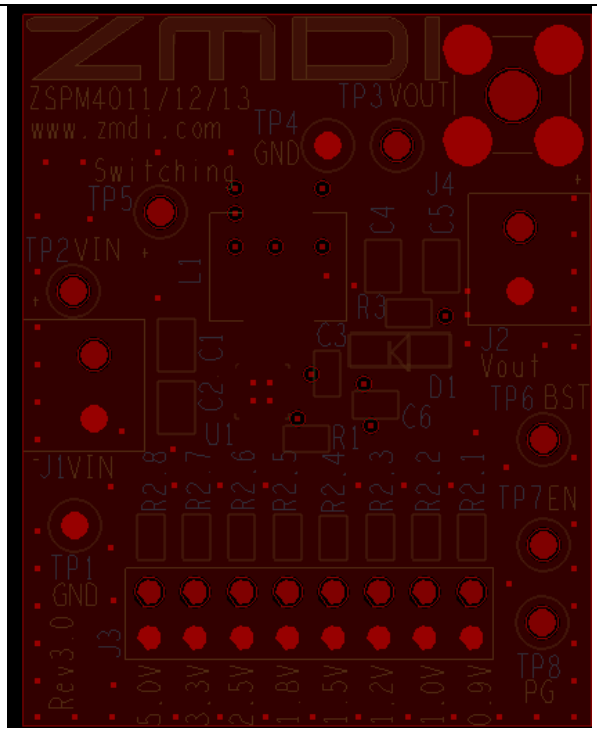
6.1. Evaluation Board Layout



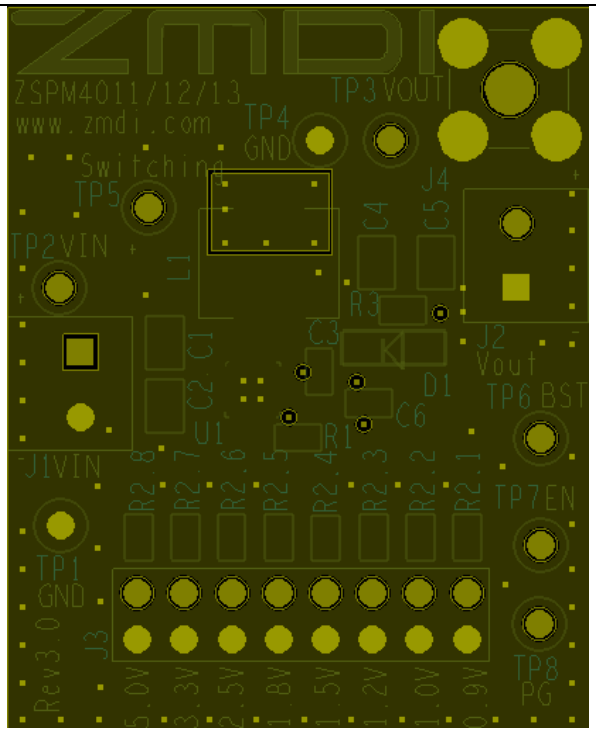
Top Layer



2nd Layer



3rd Layer



Bottom Layer

6.2. ZSPM4011/12/13 Evaluation Board Bill of Materials

Table 6.1 ZSPM4011/12/13 Evaluation Board Bill of Materials

Reference	Part	Footprint	Manufacturer	Manufacturer P/N
C1	10uF	805	TDK	C2012X5R1E106M
C2	10uF	805	TDK	C2012X5R1E106M
C3	22nF	603	TDK	C2012C0G1E223J
C4	22uF	805	Murata	GRM21BR60J226ME39L
C5	22uF	805	Murata	GRM21BR60J226ME39L
R3	NL	603		
C6	NL	603		
R2.1	NL	603		
J1	ED1514-ND	OSTVQ021150	On-Shore	ED555/2DS
J2	ED1514-ND	OSTVQ021150	On-Shore	ED555/2DS
J3	HEADER 8X2	jumper16	Omron	XG8T-0631

J4	BNC	SMB	Tektronix	
L1	4.7uH	ind	Wurth	7447779004
R1	6.04K	603	Susumu	RR0816P-6041-D-76H
R2.5	6.04K	603	Susumu	RR0816P-6041-D-76H
R2.2	53.6k	603	Susumu	RR0816P-5362-D-71C
R2.3	17.8k	603	Susumu	RR0816P-1782-D-25C
R2.4	9.09K	603	Susumu	RR0816P-9091-D-93H
R2.6	3.40K	603	Susumu	RG1608P-3401-B-T5
R2.7	2.26K	603	Susumu	RG1608P-2261-B-T5
R2.8	1.33K	603	Welwyn	PCF0603R-1K33BT1
TP1	GND	TP	Keystone	5001
TP4	GND	TP	Keystone	5001
TP2	VIN +	TP	Keystone	5001
TP3	VOUT	TP	Keystone	5001
TP5	Switching	TP	Keystone	5001
TP6	BST	TP	Keystone	5001
TP7	EN	TP	Keystone	5001
TP8	PG	TP	Keystone	5001
U1	ZSPM401X	QFN 300 x300 x100 – 17N	IDT	ZSPM4013AA1W00

7 Ordering Information

Product Sales Code	Description
ZSPM4011KIT	ZSPM4011KIT: Evaluation kit for 0.9 to 5V, 1A synchronous buck converter
ZSPM4012KIT	ZSPM4012KIT: Evaluation kit for 0.9 to 5V, 2A synchronous buck converter
ZSPM4013KIT	ZSPM4013KIT: Evaluation kit for 0.9 to 5V, 3A synchronous buck converter

8 Related Documents

File Name
ZSPM4011 Datasheet
ZSPM4012 Datasheet
ZSPM4013 Datasheet

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

9 Glossary

Term	Description
Buck converter	Step-down converter; converts a higher DC input voltage to a lower DC output voltage with high efficiency
Synchronous rectification	is a technique for improving the efficiency of rectification by replacing diodes with actively-controlled switches such as transistors
PWM	Pulse Width Modulation (fixed frequency)
PFM	Pulse Frequency Modulation (fixed pulse width)
ESR	Equivalent Series Resistance
Bootstrap control	When using an N-Channel Power MOSFET transistor as a high-side switch for the converter switching output, a gate voltage higher than the supply voltage is necessary to turn the transistor fully on. For this purpose, a charge pump circuit, called bootstrap control is implemented to provide this high supply voltage for the high-side power MOSFET driver block.

10 Document Revision History

Revision	Date	Description
1.00	October 10, 2012	First release.
	April 12, 2016	Changed to IDT branding.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.