User's Manual

32

SH7269 CPU Board

R0K572690C000BR

User's Manual

Renesas 32-Bit RISC Microcomputer
SuperH™ RISC engine Family / SH7260 Series

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About This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the functions and operating specifications of this CPU board. It is intended for users of this CPU board. A basic knowledge of electrical circuits, logical circuits, and microcomputers (MCUs) is necessary in order to use this manual.

This manual comprises an overview of the CPU board; its function, and operating specifications.

Carefully read all notes in the manual. These notes occur within the body of the text.

The Revision History summarizes primary modifications and additions to the previous versions. Refer to the text of the manual for details.

The following documents apply to the SH7269 CPU board R0K572690C000BR.

Document Type	Description	Document Title	Document No.
User's Manual	Describes functions (devices, memory maps, electrical characteristics), and operating specifications (connectors, and switches)	SH7269 CPU Board R0K572690C000BR User's Manual	This publication
Installation Manual	Describes how to set up hardware and software	SH7269 CPU Board R0K572690C000BR Installation Manual	R20UT0160EJ

The following documents apply to the SH7269 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics website.

Document Type	Description	Document Title	Document No.
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to application notes for details on using peripheral functions	SH7269 Group User's manual: Hardware	R01UH0048EJ
Software manual	Description of CPU instruction set	SH-2A, SH2A-FPU Software manual	REJ09B0051
Application note	Applications, sample programs	Available from the Renesas Electronics website.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Frequently Used Abbreviations and Acronyms

ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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1. Overview

1.1 Introduction

The SH7269 CPU Board and optional boards are designed for evaluating the features and performance of the SH7269 Group of Renesas Electronics single-chip RISC microcomputers (MCUs). It is also used for developing and evaluating application software for these MCUs. This section describes features of the SH7269 CPU Board and its optional boards.

1.1.1 SH7269 CPU Board (Part Number: SH7269 CPU Board)

The SH7269 CPU Board comes standard with a 32MB NOR flash memory (16-bit bus), a 16MB SDRAM (16-bit bus), two serial flash memories of 4MB, and a 16KB EEPROM. The SH7269 CPU Board has five boot options; boot from NOR flash memory, NAND flash memory (note), serial flash memory, NAND flash memory with the SD controller, and NAND flash memory with the MMC controller.

Note: To boot from the NAND flash memory, the user must install it. Refer to Table 1.6.1 for the component that can be installed.

The SH7269 CPU Board comes standard with an RS-232C connector, a USB connector, an SD card slot, and an RCA connector as the SH7269 peripheral interfaces.

The USB connector on the SH7269 CPU Board is a Series-A receptacle. The wiring pattern on the SH7269 CPU Board allows the user to connect a Mini-B receptacle to evaluate the USB host and function modules.

The SH7269 MCU's data bus, address bus, and internal peripheral pins are connected to expansion connectors on the SH7269 CPU Board to allow for timing evaluation with peripherals using measurements instruments, and the development of the expansion board according to its application.

The Renesas Electronics E10A-USB on-chip emulator (AUT trace enabled: 36-pin, AUB trace disabled: 14-pin) can be connected to the SH7269 CPU Board.

1.1.2 Optional Board for Audio (Part Number: M3A-HS64G01)

The M3A-HS64G01 is an evaluation board suitable for advance development of the audio system, which comes standard with an audio interface, CD deck interface and a character LCD module connector.

Also, it comes with two channels of a D/A Converter for audio output, and one channel of a D/A Converter and an A/D Converter for audio input and output as its audio interfaces. It also comes standard with an LCD module interface connector, a UART interface connector, a CAN (Controller Area Network) connector, an IEBus™ connector, an IIC connector, and an SD card connector.

Note: Some of the functions cannot be used with the SH7269 CPU Board.

1.1.3 Optional Board for Graphic Display (Part Number: M3A-HS64G02)

The M3A-HS64G02 is an evaluation board, which comes standard with a video input interface, an audio interface and an LCD module interface for developing the video processing or music-playing applications. All PWM output pins and time output pins are inserted into connectors to allow for developing the automotive meter or brightness-control applications. It comes standard with a CAN connector, an IEBus™ connector, an IIC connector and an SD card connector.

Note: Some of the functions cannot be used with the SH7269 CPU Board.

1.2 SH7269 CPU Board Configuration

Figure 1.2.1 shows an example of a system configuration using the SH7269 CPU Board.

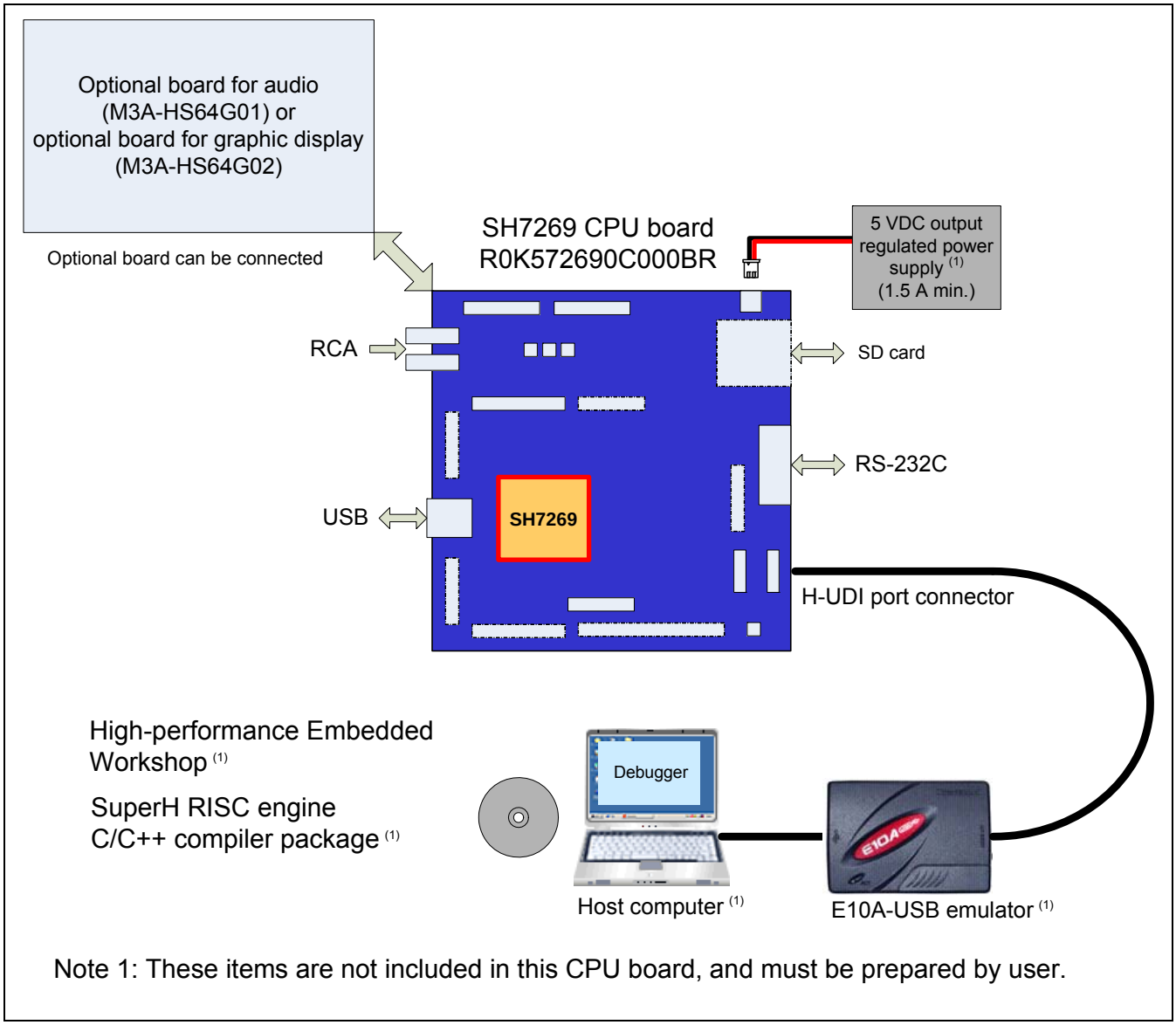

Figure 1.2.1 Configuration Using the SH7269 CPU Board

1.3 SH7269 CPU Board Specifications

Table 1.3.1 and Table 1.3.2 describe the specifications of the SH7269 CPU Board.

Table 1.3.1 SH7269 CPU Board Specifications

Item	Description
CPU	SH7269 • Input (XIN) clock: 13.33MHz • Bus clock: Up to 133.33MHz • CPU clock: Up to 266.67MHz • Internal memory High-speed internal RAM: 64KB Large-capacity internal RAM: 2.5MB Instruction cache: 8KB Operand cache: 8KB • Power supply voltage: internal: 1.25V, I/O: 3.3V • 256-pin QFP, 0.4mm pitch (package code: PLQP0256LB-A)
External memory	• SDRAM: 16MB — EDS1216AATA-75E: 1 (Elpida) • NOR flash memory: 32MB — S29GL256P90TFIR1: 1 (Spansion) • NAND flash memory: Optional — Board pattern is designed to install the K9F2G08U0B-PCB0: 1 (Samsung) • Serial flash memory: 4MB — S25FL032P0XMFI01: 2 (Spansion) • EEPROM: 16KB — R1EX24128ASAS0A: 1 (Renesas)
USB	• USB Series-A receptacle (Mini-B receptacle is optional)
SD card interface	• Accesses the SD card by the SH7269 on-chip SD Host Interface (SDHI) • Accesses the MMC by the SH7269 on-chip MMC Host Interface (MMC) — SD card slot: 1 — Includes a card power control IC (Software control NOT allowed)
Composite video input	• Inputs the analog video signal to the SH7269 on-chip video decoder directly
Connectors and through-holes	• 14-pin or 38-pin H-UDI port connector • RS-232C connector (D-sub, 9-pin) • 20-pin MIL-spec connectors — SH7269 expansion connectors: 5 (Ports A, C, D, F, and H) • 30-pin MIL-spec connectors — SH7269 expansion connectors: 2 (Ports B and G) • 40-pin MIL-spec connector — SH7269 expansion connector: 1 (Ports E and F) • 40-pin half pitch connectors — LCD output connector: 1 — DV input and PWM output connector: 1

Table 1.3.2 SH7269 CPU Board Specifications (2/2)

Item	Description
LEDs	• Power supply LED: 1 • User LEDs: 2 (Connected to the SH7269 I/O port pins)
Switches, jumpers	• Reset switch: 1 • NMI switch: 1 • IRQ1 switch: 1 • Test switch: 1 • System setting DIP switches: 1 (4/package) • User DIP switches: 1 (6/package)
Board specifications	• Dimensions: 148mm × 148mm • Mounting form: 6-layer, double-sided • Board thickness: 1.6mm • Number of boards: 1

1.4 SH7269 CPU Board Exterior

Figure 1.4.1 shows the exterior of the SH7269 CPU Board.

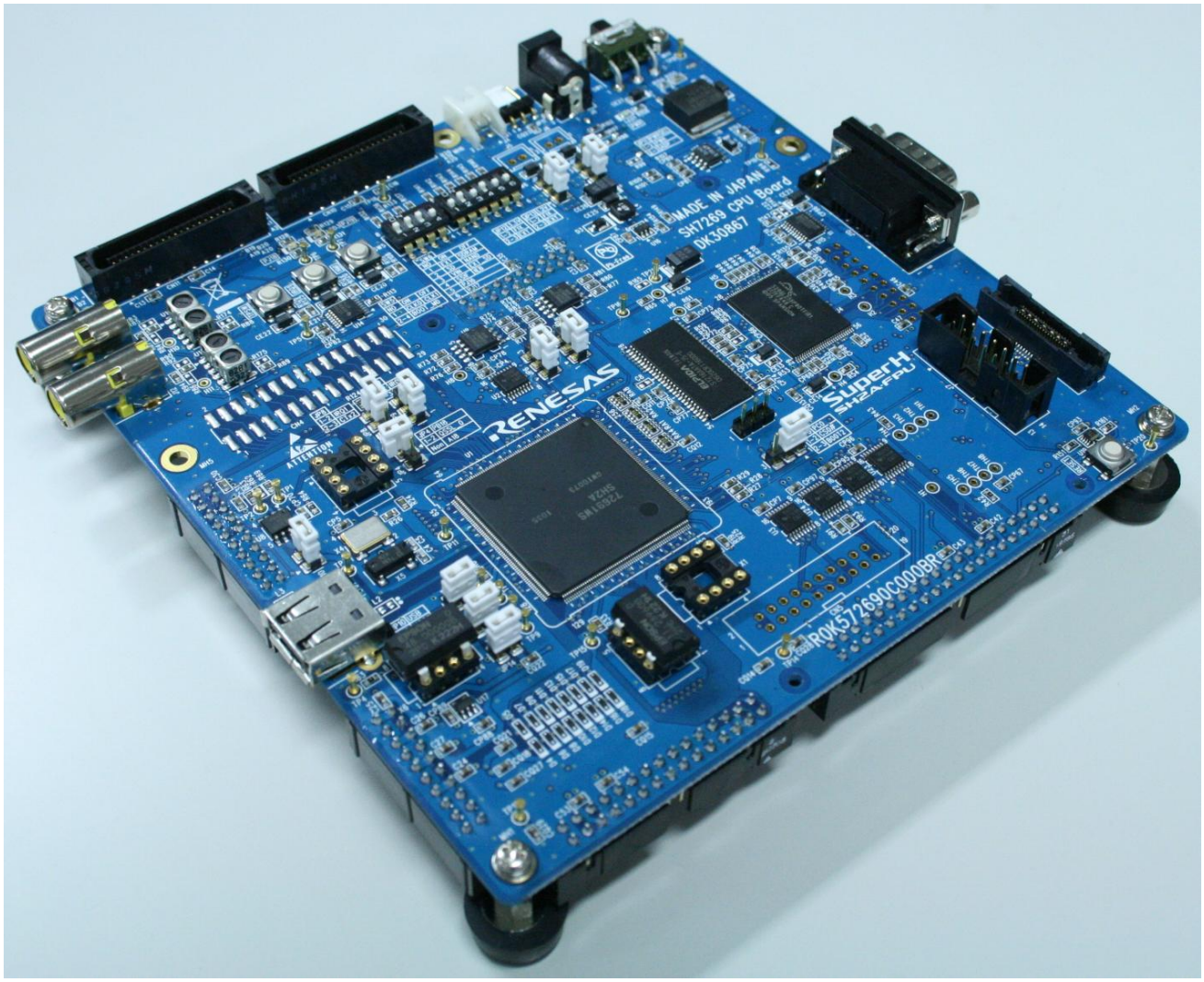

Figure 1.4.1 SH7269 CPU Board Exterior

1.5 SH7269 CPU Board Block Diagram

Figure 1.5.1 shows the block diagram of the SH7269 CPU Board.

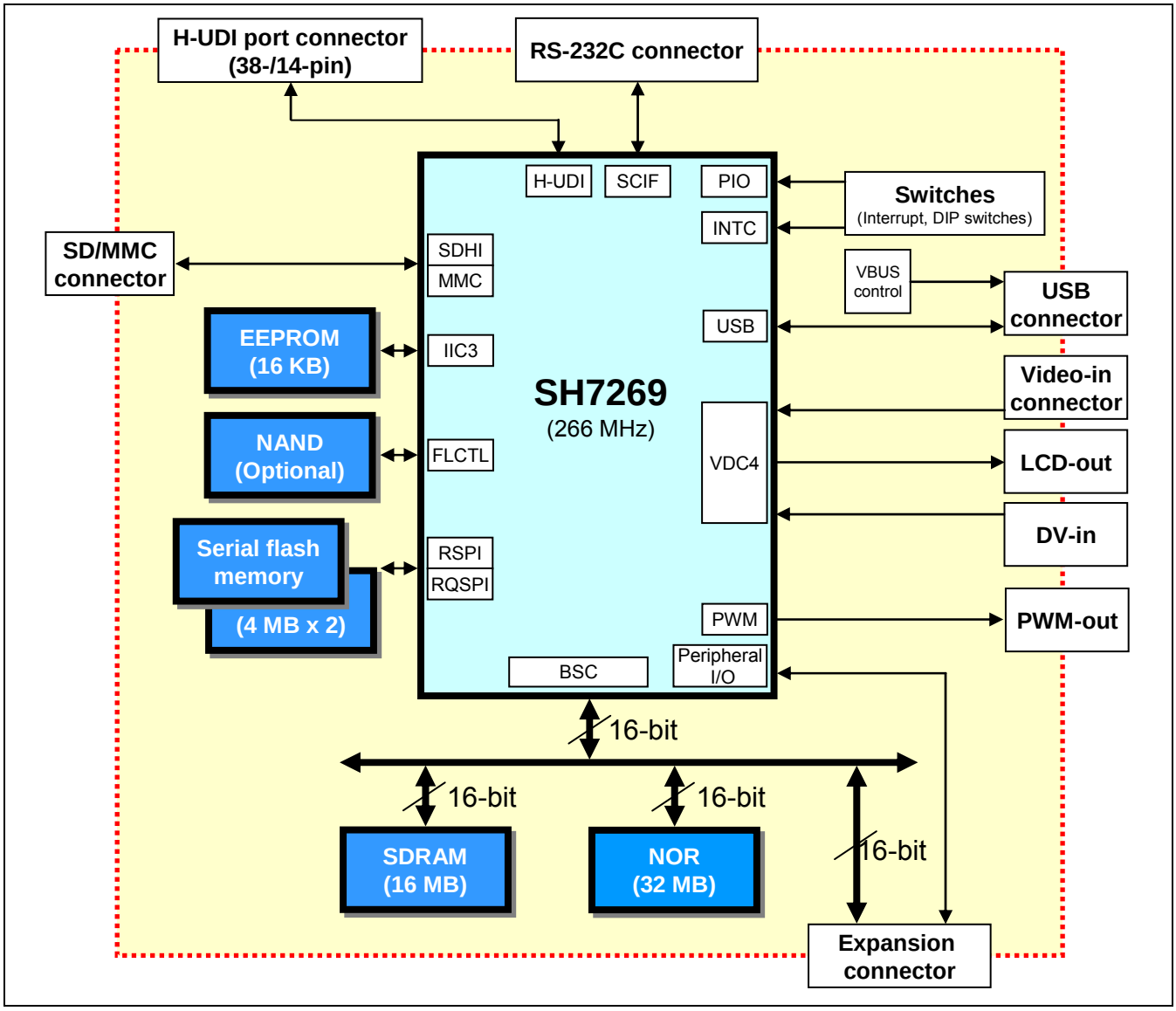

Figure 1.5.1 SH7269 CPU Board Block Diagram

1.6 SH7269 CPU Board Major Components

Figure 1.6.1 and Figure 1.6.2 show the layouts of the major components on the SH7269 CPU Board (PCB drawing).

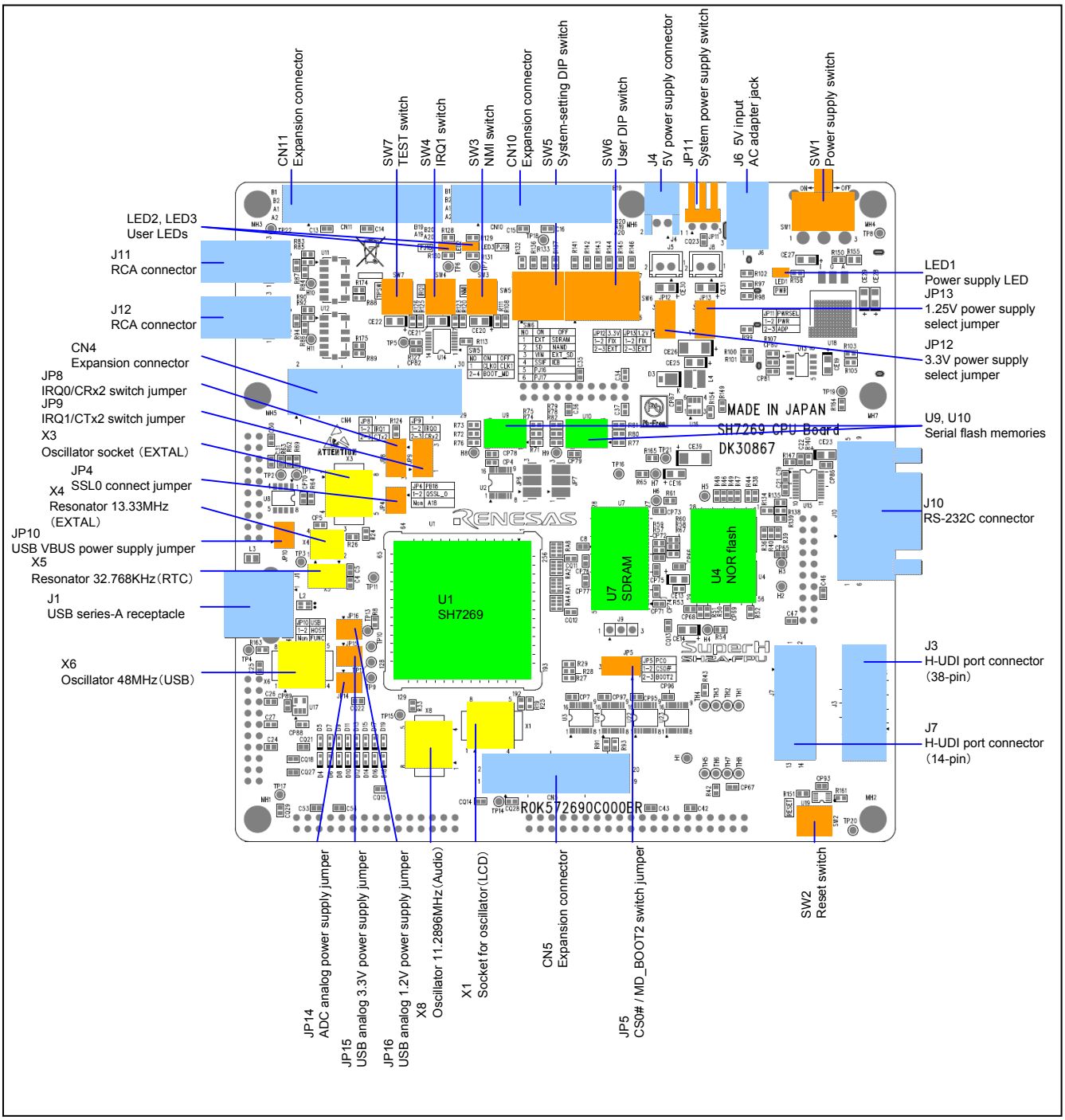

Figure 1.6.1 SH7269 CPU Board Layout and Component Placement (Top View of the Component Side)

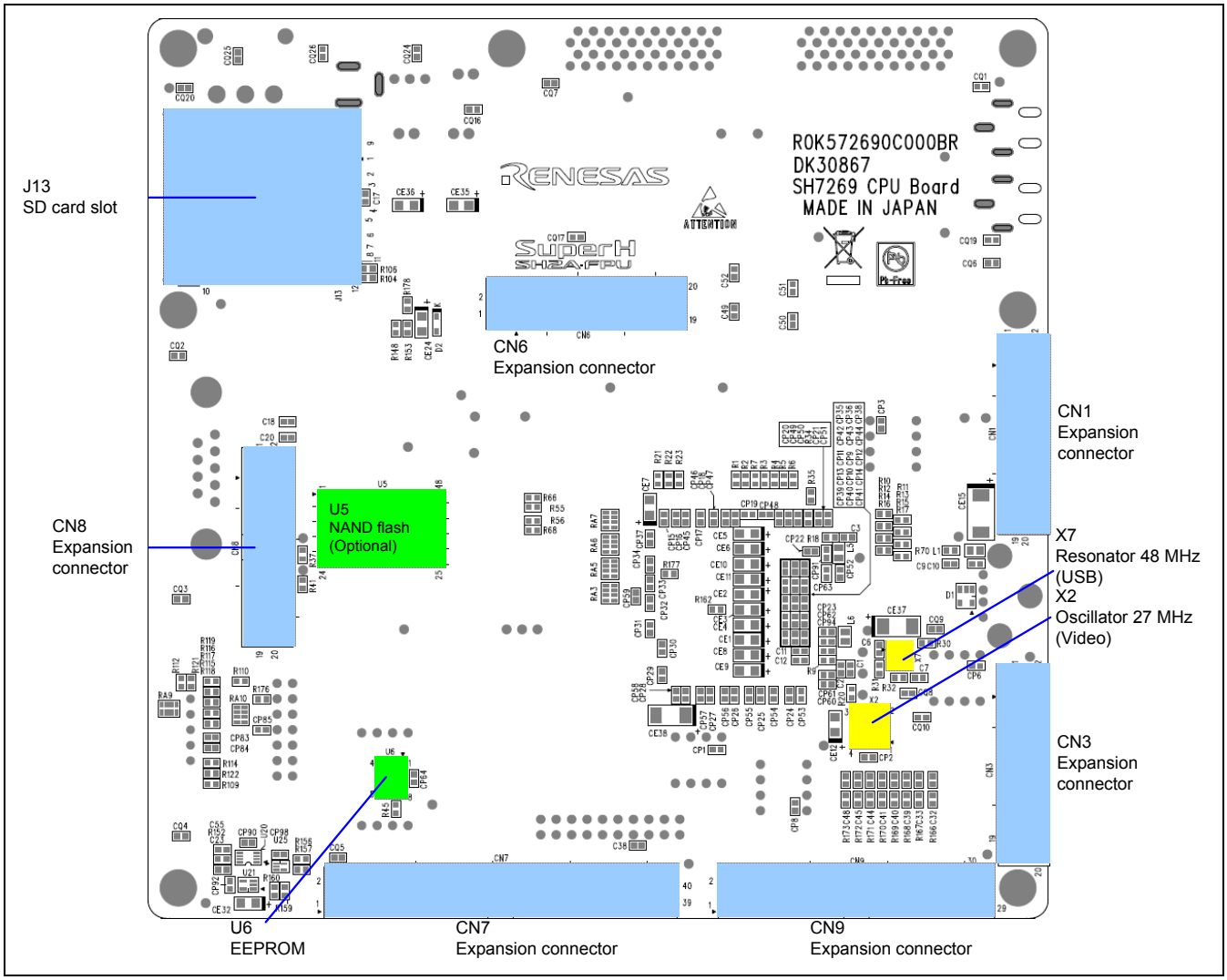

Figure 1.6.2 SH7269 CPU Board Layout and Component Placement (Top View of the Solder Side)

Table 1.6.1 to Table 1.6.3 list the major components on the SH7269 CPU Board.

Table 1.6.1 Major Components on the SH7269 CPU Board – ICs (1/3)

No.	Name	Part Number	Manufacturer	Remarks	Quantity per Board
1	CPU	R5S72691P266FP	Renesas		1
2	SDRAM	EDS1216AATA-75E	Elpida	16-bit bus 16MB	1
3	NOR flash memory	S29GL256P90TFIR1	Spansion	16-bit bus 32MB	1
4	NAND flash memory	K9F2G08U0B-PCB0	Samsung	Optional	0
5	Serial flash memories	S25FL032P0XMFI01	Spansion	4-wire serial 4MB	2
6	EEPROM	R1EX24128ASAS0A	Renesas	2-wire serial 16KB	1
7	Reset IC	RNA50C27AUS	Renesas		1
8	RS-22C driver	MAX3222ECUP	Maxim		1
9	Adjustable regulator	LMS1587CSX-ADJ	NS	3.3V	1
10	Adjustable regulator	LM2734X	NS	1.25V	1
11	Voltage reference	LM4132AMF-3.3	NS	ADC reference power supply	1
12	Multiplexers	SN74CB3Q3257PWR	TI	Analog switches	5

Table 1.6.2 Major Components on the SH7269 CPU Board – Connectors (2/3)

No.	Name	Part Number	Manufacturer	Remarks	Quantity per Board
1	38-pin H-UDI port connector	2-5767004-2	Tyco		1
2	14-pin H-UDI port connector	2514-6002	3M		1
3	RS-232C connector	XM2C-0942-132L	Omron	D-sub 9-pin	1
4	20-pin expansion connectors	XG4C-2031	Omron	20-pin MIL-spec	3
5	30-pin expansion connector	XG4C-2031	Omron	30-pin MIL-spec	1
6	30-pin expansion connector	961230-6300	3M	Optional	0
7	40-pin expansion connector	XG4C-4031	Omron	40-pin MIL-spec	1
8	40-pin expansion connectors	FX2C-40P-1.27DSA	Hirose	40-pin half pitch	2
9	DIP switches (4/package)	A6S-4104-H	Omron	System setting	1
10	DIP switches (6/package)	A6S-6104-H	Omron	User	1
11	USB Series-A receptacle	UBA-4R-D14T-4D	J.S.T. Manufacturing	DIP type	1
12	USB Mini-B receptacle	54819-0572	Molex	Optional	0
13	SD card slot	DM1B-DSF-PEJ	Hirose	Reverse type	1
14	RCA connectors	JPJ2545-01-540	Hosiden	Composite video input pin	2

Table 1.6.3 Major Components on the SH7269 CPU Board – USB (3/3)

No.	Name	Part Number	Manufacturer	Remarks	Quantity per Board
1	USB power distribution switch	MIC-2025-2YM	Micrel	VBUS power control	1
2	Zener diode	HZN6.2Z4MFA	Renesas	Optional	0
3	Ferrite beads	BLM21PG600SN1	Murata	Optional	0
4	Common mode choke	DLW21HN900SQ2	Rohm	Optional	0

1.7 M3A-HS64G01 Configuration

Figure 1.7.1 shows an example of a system configuration using the M3A-HS64G01 (optional board for audio).

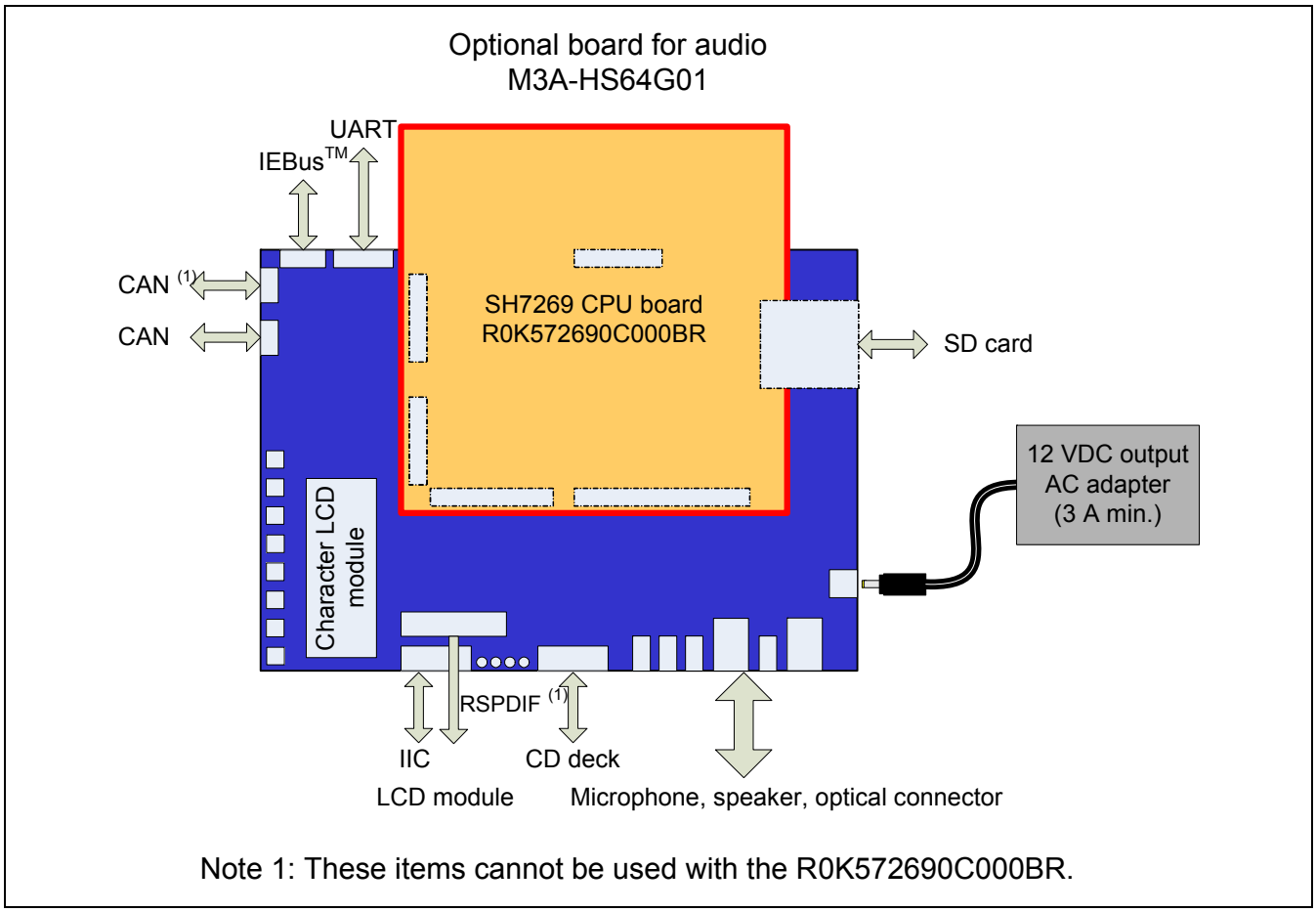

Figure 1.7.1 Configuration Using the M3A-HS64G01

1.8 M3A-HS64G01 Board Specifications

Table 1.8.1 describes the board specifications of the M3A-HS64G01.

Table 1.8.1 M3A-HS64G01 Board Specifications

No.	Item	Description
1	LCD	Comes with following connectors to control an LCD module by the SH7269 on-chip Video Display Controller 4 (VDC4) • Flexible connectors for LCD module: 2 • MIL-spec connector for LCD module: 1 (30-pin)
2	Character LCD	Controls the character LCD module by the SH7269 on-chip general-purpose I/O ports • 16 × 2 semi-transmissive character LCD module with LED backlight: 1
3	Audio	Comes with audio codecs for audio input (AK4353) and audio input/output (AK4524) by the SH7269 on-chip Serial Sound Interface with FIFO (SSIF) • AK4353 (Asahi Kasei Microdevices Corporation): 2 — 96 kHz 24-bit DAC, on-chip digital audio transmitter — Sampling frequency: 16 to 96 kHz — Stereo pin jacks: 2 — Optical connectors: 2 • AK4524 (Asahi Kasei Microdevices Corporation): 1 — 24-bit stereo codec with microphone AMP — Sampling frequency: 32 to 48kHz
4	CD deck	Inputs PCM data using the SH7269 on-chip SSIF and controls the CD deck by the Renesas Serial Peripheral Interface (RSPI) • Flexible connector for connecting a CD deck: 1
5	SD card interface	Accesses the SD card by the SH7269 on-chip SD Host Interface (SDHI) • SD card slot: 1 • Includes a card power control IC (Software control NOT allowed)
6	CAN	CAN (Controller Area Network) communication by the SH7269 on-chip CAN (RCAN-TL1) • HA13721FP (Renesas CAN driver IC), includes a voltage level shifter
7	IEBus ™	IEBus ™ communication by the SH7263 on-chip IEBus Controller (IEB) • HA12187FP (Renesas IEBus driver IC), includes a voltage level shifter
8	UART interface	Connected to the SH7269 on-chip Serial Communication Interface with FIFO (SCIF) pin
9	IIC	Connected to the SH7269 on-chip IIC bus interface (IIC3) pin • MIL-spec connector for connecting an external IIC interface: 1 (20-pin)
10	Switches	Key input by the SH7269 on-chip A/D converter • Key input switches: 16 (4 switches × 4 inputs)
11	Board specifications	• Dimensions: 210mm × 148mm • Mounting form: 4 layers, double-sided • Board thickness: 1.6mm • Number of boards: 1

1.9 M3A-HS64G01 Exterior

Figure 1.9.1 shows the exterior of the M3A-HS64G01.

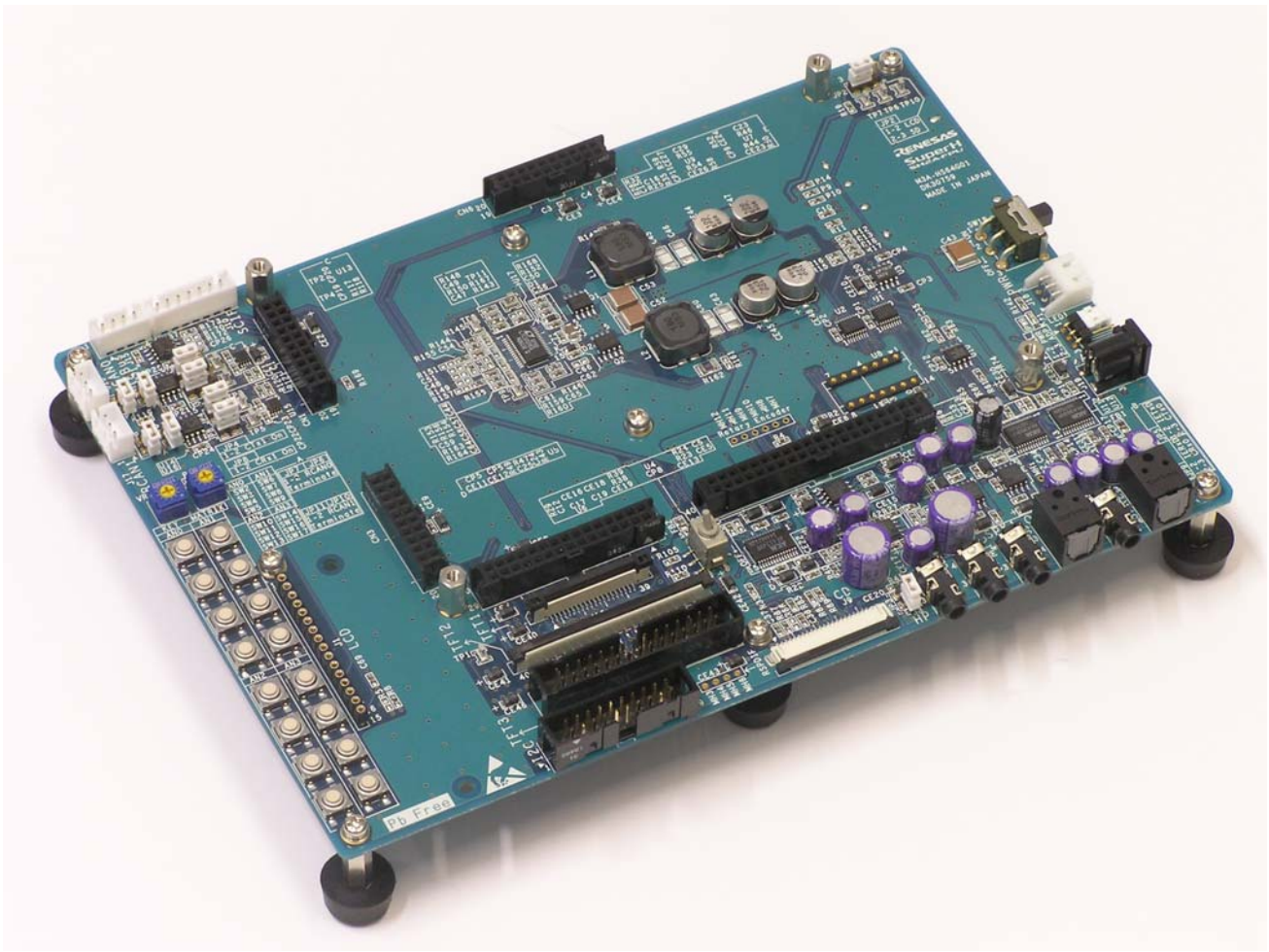

Figure 1.9.1 M3A-HS64G01 Exterior

1.10 M3A-HS64G01 Block Diagram

Figure 1.10.1 shows the block diagram of the M3A-HS64G01.

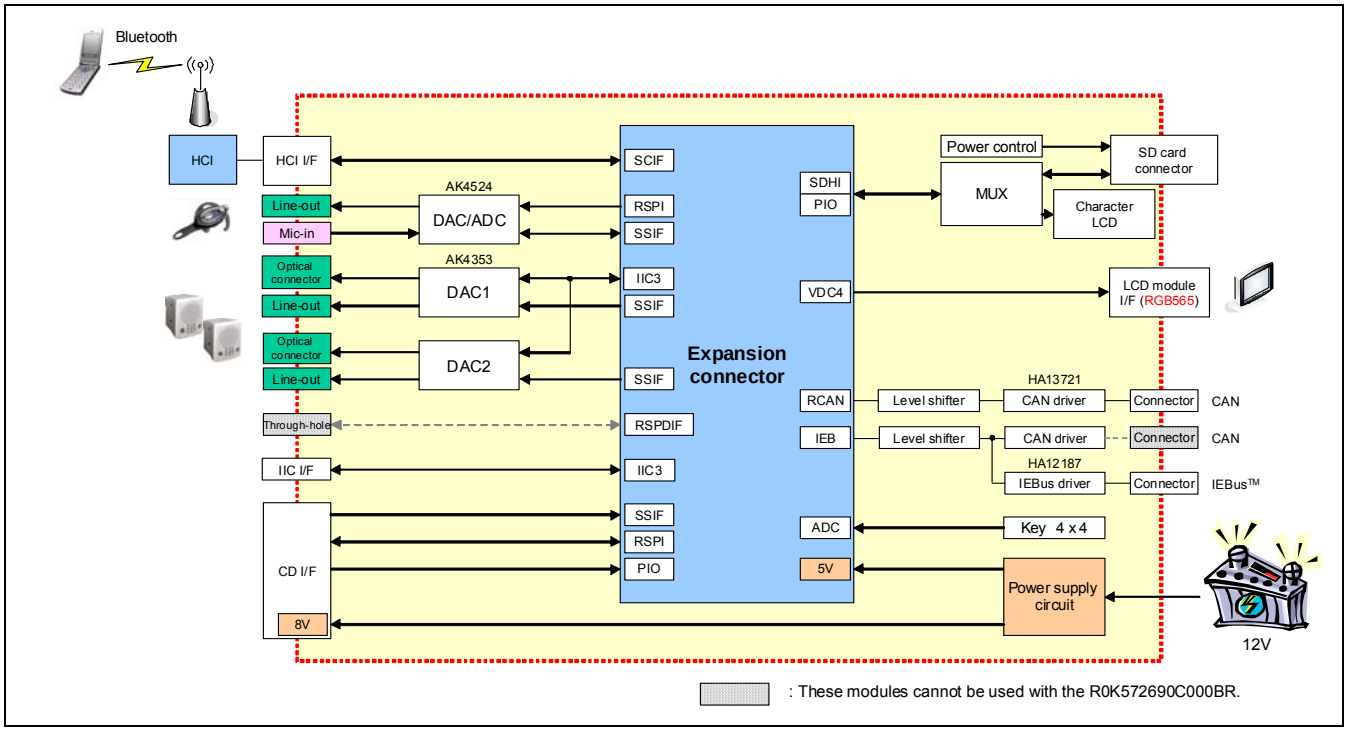

Figure 1.10.1 M3A-HS64G01 Block Diagram

1.11 M3A-HS64G01 Major Components

Figure 1.11.1 shows the M3A-HS64G01 layout and locations of the major components (PCB drawing).

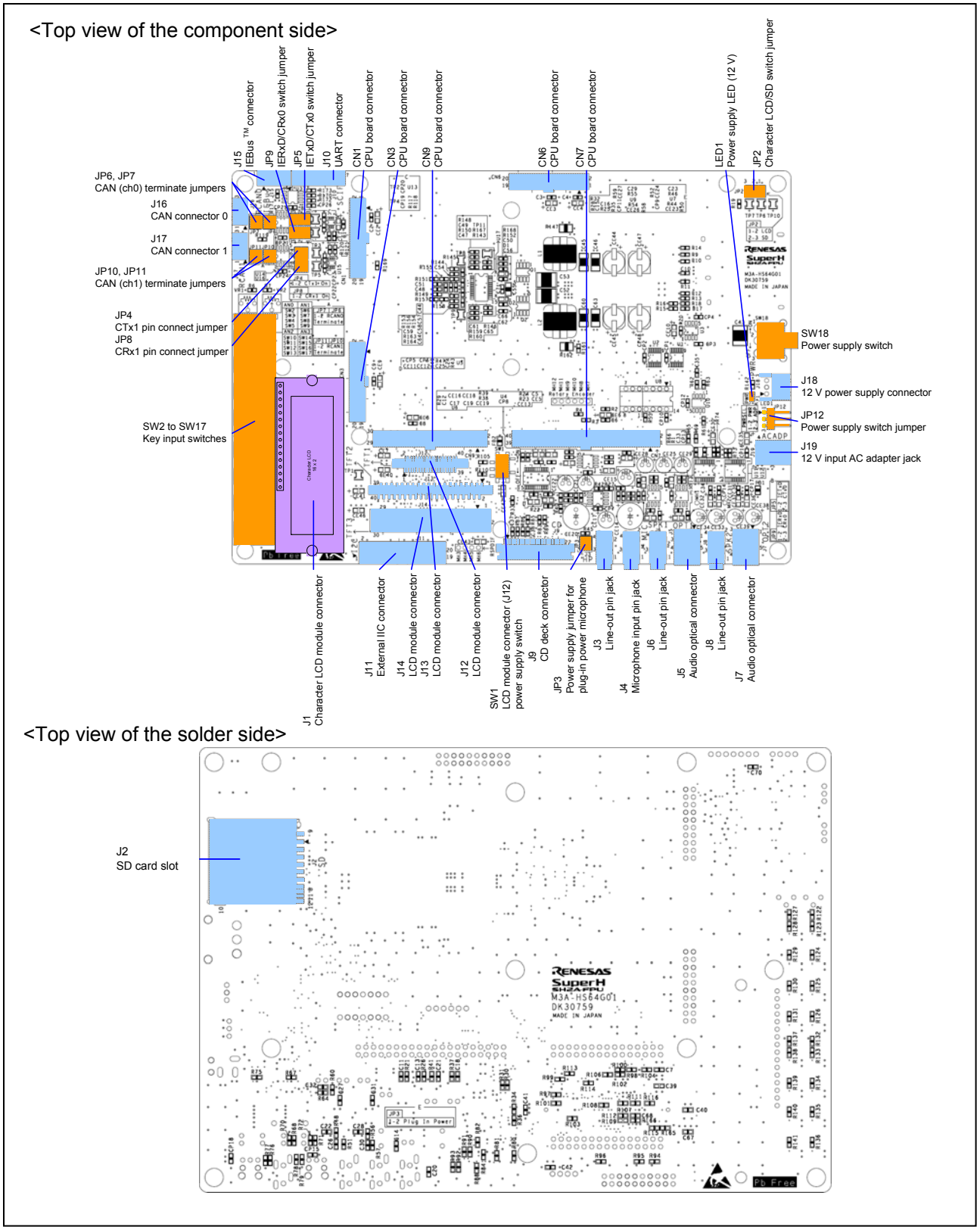

Figure 1.11.1 M3A-HS64G01 Layout and Component Placement

Table 1.11.1 and Table 1.11.2 list the major components on the M3A-HS64G01.

Table 1.11.1 Major Components – ICs (1/2)

No.	Name	Part Number	Manufacturer	Remarks	Quantity per Board
1	Character LCD module	SD1602H	Sunlike	16 characters × 2 lines	1
2	Audio CODEC	AK4524VF	Asahi Kasei	24-bit 96 kHz audio codec	1
3	D/A Converters	AK4353VF	Asahi Kasei	96kHz 24-bit D/A converter	2
4	CAN drivers	HA13721FP	Renesas		2
5	IEBus™ driver	HA12187FP	Renesas		1
6	Adjustable regulator	LTC3727EG	LT	8V/5V	1
7	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	2

Table 1.11.2 Major Components – Connectors (2/2)

No.	Name	Part Number	Manufacturer	Remarks	Quantity per Board
1	20-pin expansion connectors	XG4C-2031	Omron	20-pin MIL-spec	3
2	30-pin expansion connector	XG4C-3031	Omron	30-pin MIL-spec	1
3	40-pin expansion connector	XG4C-4031	Omron	40-pin MIL-spec	1
4	SD card slot	DM1B-DSF-PEJ	Hirose	Reverse type	1
5	Audio optical connectors	TOTX147PL	Toshiba		2
6	CD deck connector	IMSA-9617S-22	Iriso	1 mm pitch FFC	1
7	UART connector	B7B-XH-A	J.S.T. Manufacturing	TTL level	1
8	External IIC connector	XG4C-2031	Omron	20-pin MIL-spec	1
9	LCD module connector 1 (J12)	IMSA-9639S-40D	Iriso	0.5mm pitch FFC, for TX09D55VM1CDA only	1
10	LCD module connector 2 (J13)	IMSA-9619S-40B	Iriso	1 mm pitch FFC, for TX09D14VM3CCA only	1
11	LCD module connector 3 (J14)	XG4C-3031	Omron	30-pin MIL-spec, multi-purpose	1
12	IEBus™ connector	B3B-XH-A	J.S.T. Manufacturing	2.5mm pitch	1
13	CAN connectors	B3B-XH-A	J.S.T Manufacturing	2.5mm pitch	2

1.12 M3A-HS64G02 Configuration

Figure 1.12.1 shows an example of the system configuration using the M3A-HS64G02 (optional board for graphic display).

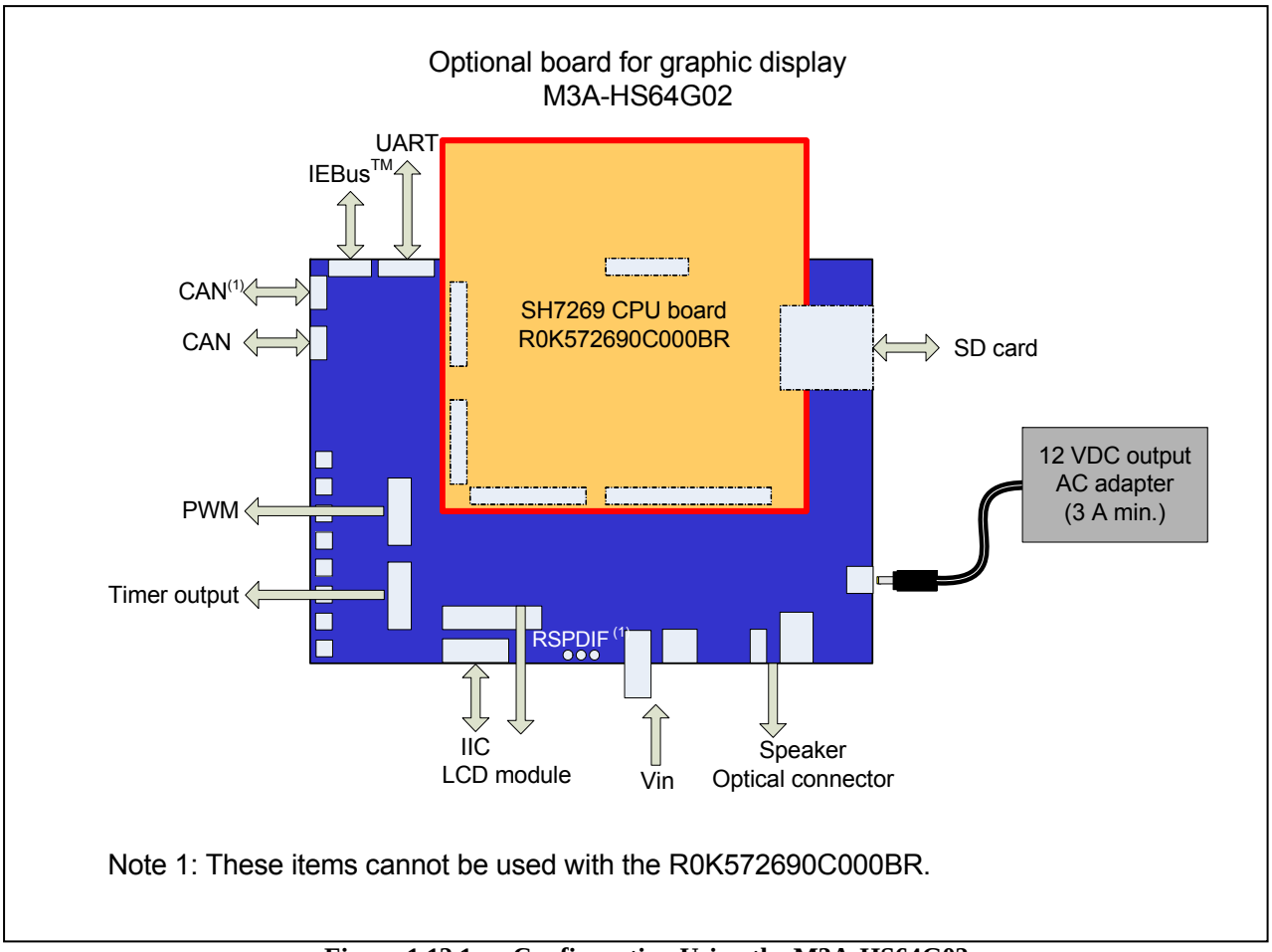

Figure 1.12.1 Configuration Using the M3A-HS64G02

1.13 M3A-HS64G02 Board Specifications

Table 1.13.1 describes the M3A-HS64G02 board specifications.

Table 1.13.1 M3A-HS64G02 Board Specifications

No.	Item	Description
1	LCD	Comes with following connectors to control an LCD module by the SH7269 on-chip Video Display Controller 4 (VDC4) • Flexible connectors for LCD module: 2 • MIL-spec connector for LCD module: 1 (30-pin)
2	Video signal input	Inputs the video signal in the SH7269 on-chip VDC4 • AK8851 (Asahi Kasei Microdevices Corporation): 1 — Decodes NTSC or PAL composite video signal and S-video signal digitally — Includes two channels of a 10-bit ADC (Operates at 27MHz) — Composite video pin (RCA connector) — S-video connector
3	Audio	Comes with audio codec for audio output by the SH7269 on-chip Serial Sound Interface with FIFO (SSIF) • AK4353 (Asahi Kasei Microdevices Corporation): 1 — 96 kHz 24-bit D/A Converter, on-chip digital audio transmitter — Sampling frequency: 16 to 96 kHz — Stereo pin jacks: 2 — Optical connectors: 2
4	PWM	Connected to the SH7269 on-chip Motor Control PWM timer pin • MIL-spec connector for PWM timer output: 1 (20-pin)
5	Timer output	Controls the LED brightness by PWM mode in the SH7269 on-chip MTU2 • MIL-spec connector for time output: 1 (20-pin)
6	SD card interface	Accesses the SD card by the SH7269 on-chip SD Host Interface • SD card slot: 1 • Includes a card power control IC (Software control NOT allowed)
7	CAN	CAN communication by the SH7269 on-chip CAN (RCAN-TL1) • HA13721FP (Renesas CAN driver IC), includes a voltage level shifter
8	IEBus ™	IEBus ™ communication by the SH7263 on-chip IEBus Controller (IEB) • HA12187FP (Renesas IEBus driver IC), includes a voltage level shifter
9	IIC	Connected to the SH7269 on-chip IIC bus interface (IIC3) pin • MIL-spec connector for connecting an external IIC interface: 1 (20-pin)
10	Switches	Key input by the SH7269 on-chip A/D Converter • Key input switches: 16 (4 switches × 4 inputs)
11	Board specifications	• Dimensions: 210mm × 148mm • Mounting form: 4 layers, double-sided • Board thickness: 1.6mm • Number of boards: 1

1.14 M3A-HS64G02 Exterior

Figure 1.14.1 shows the exterior of the M3A-HS64G02.

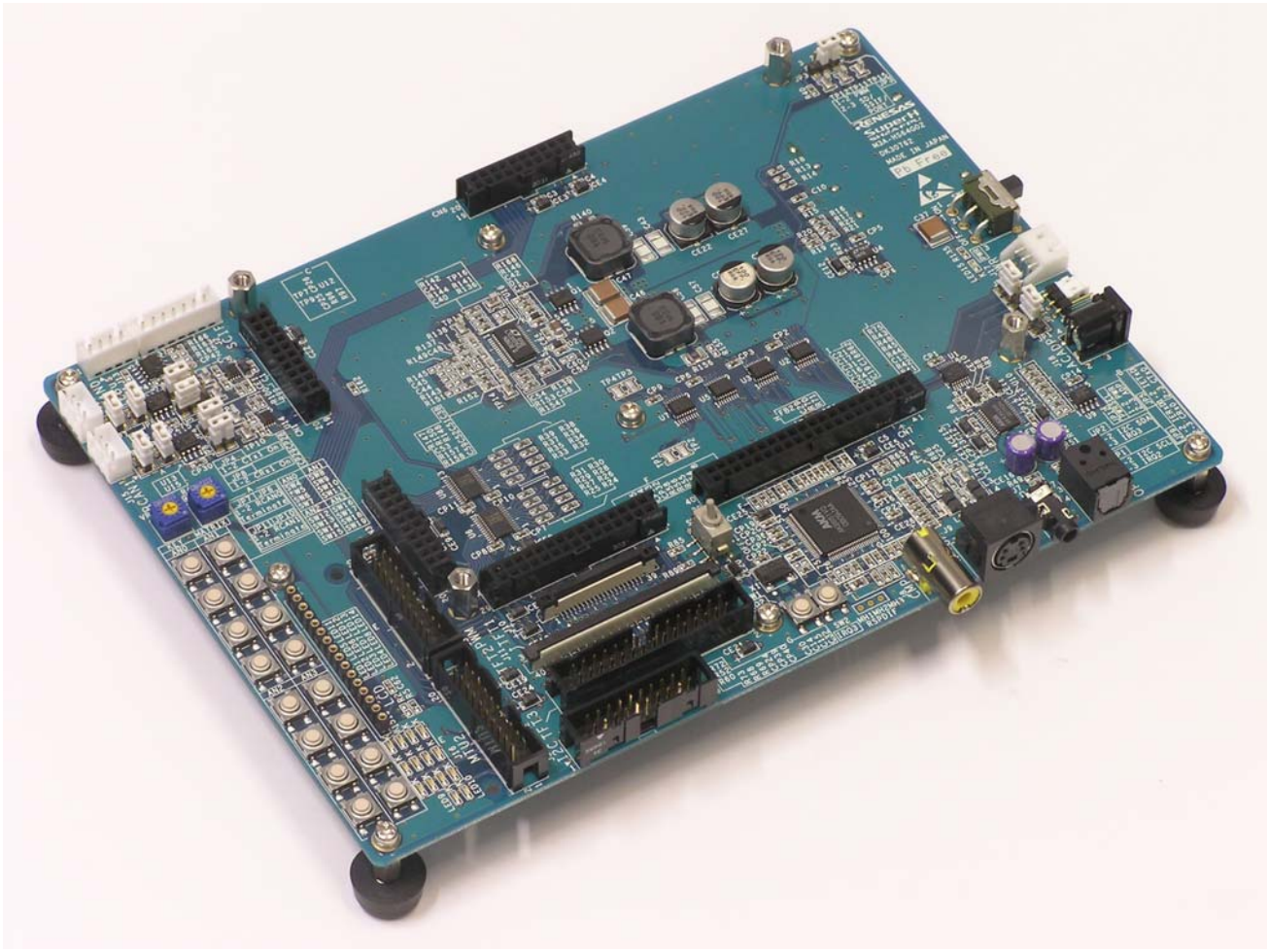

Figure 1.14.1 M3A-HS64G02 Exterior

1.15 M3A-HS64G02 Block Diagram

Figure 1.15.1 shows the block diagram of the M3A-HS64G02.

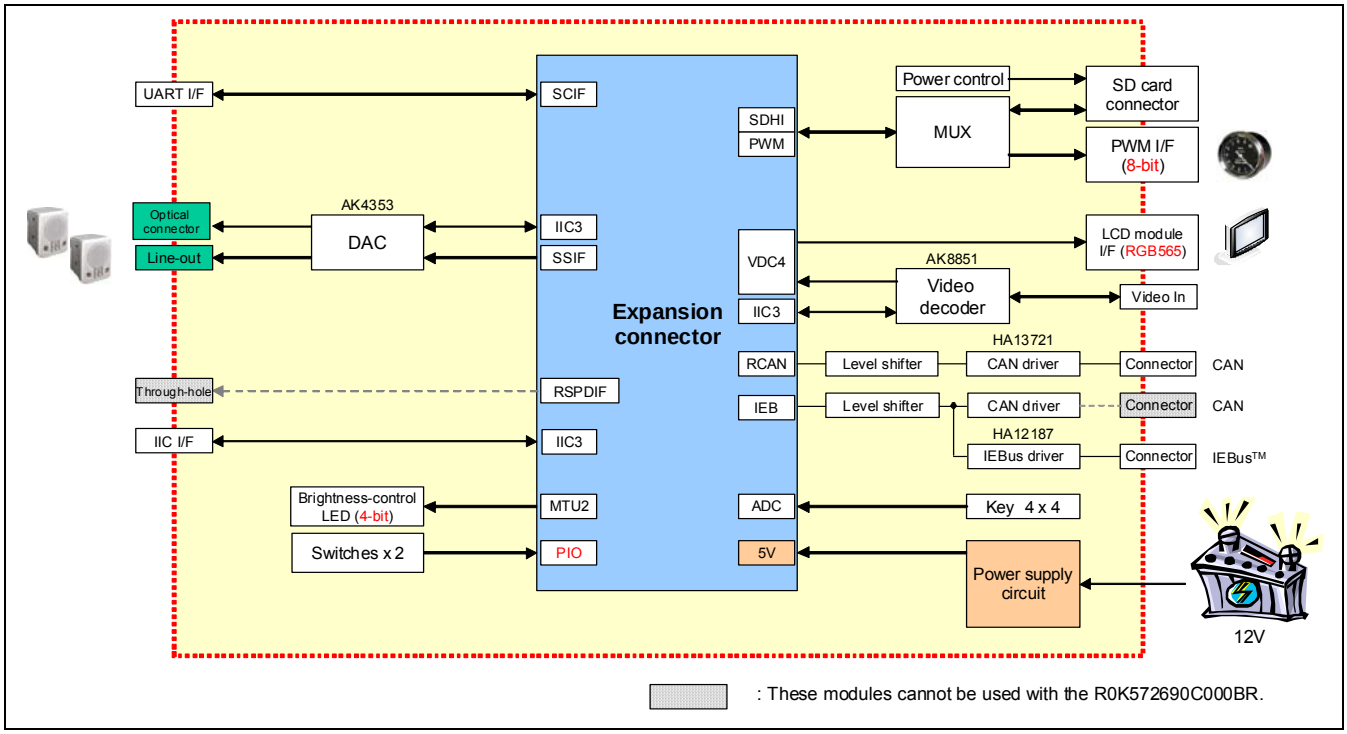

Figure 1.15.1 M3A-HS64G02 Block Diagram

1.16 M3A-HS64G02 Major Components

Figure 1.16.1 shows the M3A-HS64G02 layout and locations of the major components (PCB drawing).

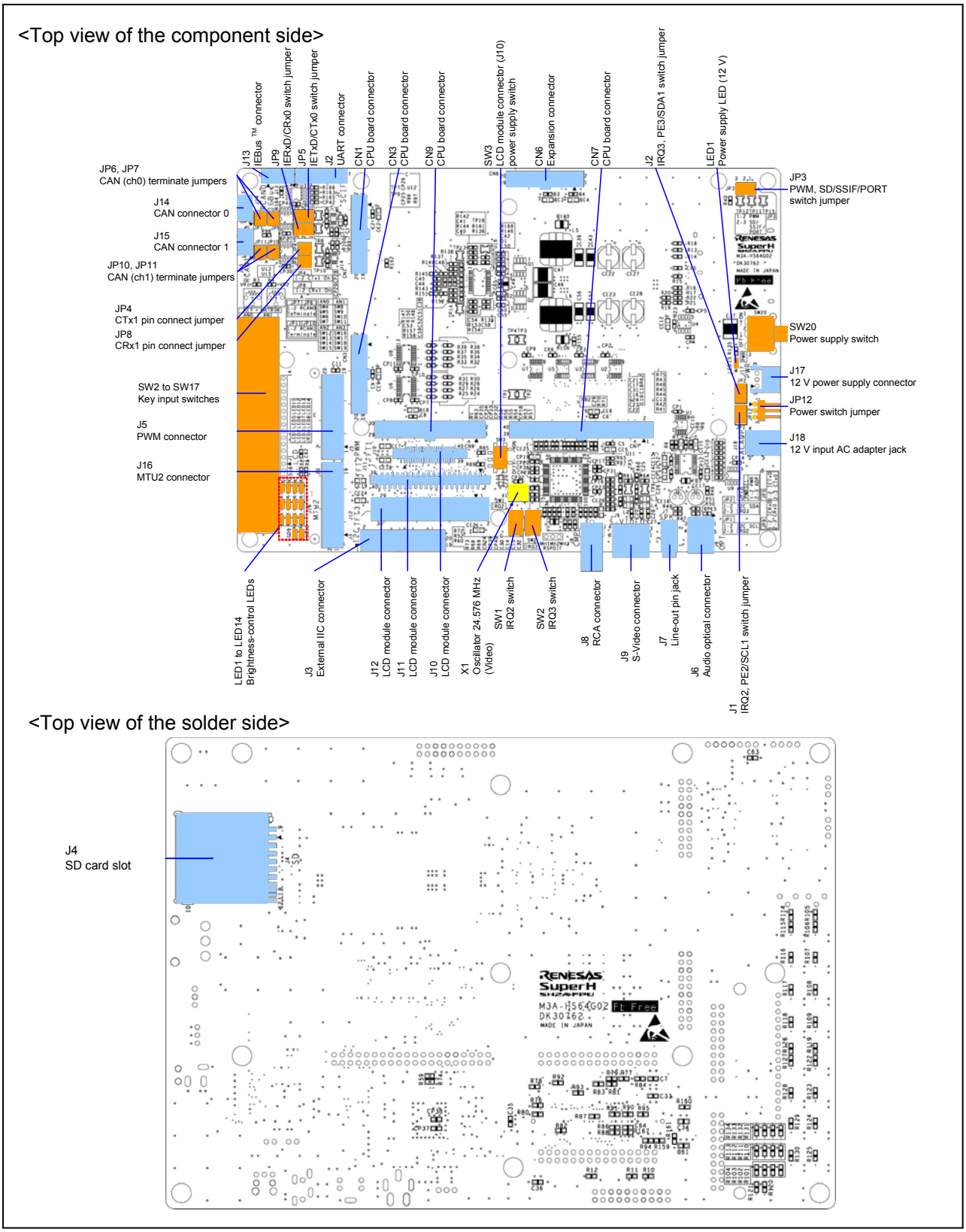

Figure 1.16.1 M3A-HS64G02 Layout and Component Placement

Table 1.16.1 and Table 1.16.2 list the major components on the M3A-HS64G02.

Table 1.16.1 Major Components – ICs (1/2)

No.	Name	Part Number	Manufacturer	Remarks	Quantity per Board
1	Character LCD module	SD1602H	Sunlike	16 characters × 2 lines	1
2	Audio codec	AK4524VF	Asahi Kasei	24-bit 96kHz audio codec	1
3	D/A Converters	AK4353VF	Asahi Kasei	96kHz 24-bit D/A converter	1
4	CAN drivers	HA13721FP	Renesas		2
5	IEBus™ driver	HA12187FP	Renesas		1
6	Adjustable regulator	LTC3727EG	LT	8V/5V	1
7	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	4

Table 1.16.2 Major Components – Connectors (2/2)

No.	Name	Part Number	Manufacturer	Remarks	Quantity per Board
1	20-pin expansion connectors	XG4C-2031	Omron	20-pin MIL-spec	3
2	30-pin expansion connector	XG4C-3031	Omron	30-pin MIL-spec	1
3	40-pin expansion connector	XG4C-4031	Omron	40-pin MIL-spec	1
4	SD card slot	DM1B-DSF-PEJ	Hirose	Reverse type	1
5	Audio optical connectors	TOTX147PL	Toshiba		1
6	UART connector	B7B-XH-A	J.S.T. Manufacturing	TTL level	1
7	External IIC connector	XG4C-2031	Omron	20-pin MIL-spec	1
8	LCD module connector 1 (J10)	IMSA-9639S-40D	Iriso	0.5mm pitch FFC, for TX09D55VM1CDA only	1
9	LCD module connector 2 (J11)	IMSA-9619S-40B	Iriso	1 mm pitch FFC, for TX09D14VM3CCA only	1
10	LCD module connector 3 (J12)	XG4C-3031	Omron	30-pin MIL-spec, multi-purpose	1
11	IEBus™ connector	B4B-XH-A	J.S.T. Manufacturing	2.5mm pitch	1
12	CAN connectors	B3B-XH-A	J.S.T Manufacturing	2.5mm pitch	2
13	PWM connector	XG4C-2031	Omron	20-pin MIL-spec	1
14	MTU2 connector	XG4C-2031	Omron	20-pin MIL-spec	1

1.17 Memory Maps

Figure 1.17.1 shows the memory map example of the SH7269 on the SH7269 CPU Board.

Figure 1.17.1 SH7269 Memory Map Example

1.18 Absolute Maximum Ratings

Table 1.18.1 and Table 1.18.2 list the absolute maximum ratings of the SH7269 CPU Board and its optional boards.

Table 1.18.1 SH7269 CPU Board Absolute Maximum Ratings

Symbol	Item	Value	Remarks
VCC	5V system power supply voltage	−0.3V to 6.0V	Reference voltage: VSS
3VCC	3.3V system power supply voltage	−0.3V to 4.6V	Reference voltage: VSS
1.2VCC	1.25V system power supply voltage	−0.3V to 1.7V	Reference voltage: VSS
T_{opr}	Operating ambient temperature	−10°C to 55°C	Do not expose to condensation or corrosive gas
T_{stg}	Storage ambient temperature	−20°C to 60°C	Do not expose to condensation or corrosive gas

Note: Ambient temperature refers to the air temperature in the vicinity of the board.

Table 1.18.2 Absolute Maximum Ratings on the SH7269 Optional Boards

Symbol	Item	Value	Remarks
12VCC	12V system power supply voltage	−0.3V to 15.0V	Reference voltage: VSS
8VCC	8V system power supply voltage	−0.3V to 10.0V	Reference voltage: VSS
5VCC	5V system power supply voltage	−0.3V to 6.0V	Reference voltage: VSS
3VCC	3.3V system power supply voltage	−0.3V to 4.6V	Reference voltage: VSS
T_{opr}	Operating ambient temperature	−10°C to 55°C	Do not expose to condensation or corrosive gas
T_{stg}	Storage ambient temperature	−20°C to 60°C	Do not expose to condensation or corrosive gas

Note: Ambient temperature refers to the air temperature in the vicinity of the board.

1.19 Operating Conditions

Table 1.19.1 and Table 1.19.2 list the operating conditions of the SH7269 CPU Board and its optional boards.

Table 1.19.1 SH7269 CPU Board Operating Conditions

Symbol	Item	Value	Remarks
VCC	5V system power supply voltage	4.75V to 5.25V	Reference voltage: VSS
–	Maximum current consumption	1.5A max.	
T_{opr}	Operating ambient temperature	0°C to 40°C	Do not expose to condensation or corrosive gas

Table 1.19.2 SH7269 Optional Boards Operating Conditions

Symbol	Item	Value	Remarks
12VCC	12V system power supply voltage	11.4V to 12.6V	Reference voltage: VSS
–	Maximum current consumption	3A max.	Includes the SH7269 CPU BoardC000BR
T_{opr}	Operating ambient temperature	0°C to 40°C	Do not expose to condensation or corrosive gas

1.20 Usage Note

This section describes the usage note of the SH7269 CPU board and its optional boards.

1.20.1 Configuring Unused Pins

Set the SH7269 unused (unconnected) multiplexed pin to output when the optional board is not connected with the SH7269 CPU board. Port H requires external resistors or must be set to an analog input.

2. Functions

2.1 Overview of Functions

The R0K572690C000BR includes the function modules listed in the following table.

Table 2.1.1 R0K572690C000BR Function Modules

Section	Function	Description
2.2	CPU	• SH7269 — Input (XIN) clock: 13.33MHz — Bus clock: Up to 133.33MHz — CPU clock: Up to 266.67MHz
2.3	Memory	• Internal memory — High-speed internal RAM: 64KB, Large-capacity internal RAM: 2.5MB • SDRAM: 16MB — EDS1216AATA-75E: 1 (Elpida) • NOR flash memory: 32MB — S29GL256P90TFIR1: 1 (Spansion) • NAND flash memory: Optional — Board pattern is designed to install the K9F2G08U0B-PCB0: 1 (Samsung) • Serial flash memory: 4MB — S25FL032P0XMFI01: 2 (Spansion) • EEPROM: 16KB — R1EX24128ASAS0A: 1 (Renesas)
2.4	USB interface	Connects the SH7269 USB 2.0 host/function module and a USB connector
2.5	RS-232C interface	Connects the SH7269 Serial Communication Interface with FIFO (SCIF) and an RS-232C connector
2.6	I/O ports	Connects the SH7269 I/O ports, LEDs, and DIP switches
2.7	Interrupt switches	Connects the SH7269 NMI pin, IRQ1 pin, and push-button switches
2.8	Clock modules	• Controls the system clock • Controls the peripheral I/O clock
2.9	Reset module	• Resets devices on the R0K572690C000BR
2.10	Power supply module	• Controls the R0K572690C000BR system power supply
2.11	H-UDI	• Connects the SH7269 user debug interface to the H-UDI port connector
2.12	SD//MMC card interface	• Connects the SH7269 SD Host Interface (SDHI) and an SD card slot • Connects the SH7269 MMC Host Interface (MMC) and an MMC card slot
2.13	VDC4 interface	• Connects the SH7269 Video Display Controller 4 (VDC4) and the LCD module connector • Connects the SH7269 Video Display Controller 4 (VDC4) and the digital video input connector
2.14	Video input interface	• Connects the SH7269 digital video decoder and the composite video input pin
2.15	PWM interface	• Connects the SH7269 Motor Control PWM Timer (PWM) and a 40-pin half pitch connector
–	Operating Specifications	Refer to chapter 5 for details on connectors, switches, and LEDs

2.2 CPU

2.2.1 SH7269 Overview

The R0K572690C000BR includes the SH7269, the 32-bit RISC MCU that operates with a maximum frequency of 266.67 MHz.

2.2.2 SH7269 Pin Functions Used on the R0K572690C000BR

Table 2.2.1 to Table 2.2.10 list the SH7269 pin functions used on the R0K572690C000BR

Table 2.2.1 R0K572690C000BR Function Modules

No.	Name	Symbol	Description	Expansion Connector	Remarks
1	PC1/RD#	RD#	Connected to NOR flash memory OE# pin	CN6, pin 6	
2	PVcc				
3	PC2/RD/WR#/SCK6	RD/WR#	Connected to SDRAM WE# pin	CN6, pin 7	
4	PC3/WE0#/DQMLL/RxD6	WE0#	Connected to NOR flash memory WE# pin	CN6, pin 8	
		DQMLL	Connected to SDRAM DQML pin		
5	PC4/WE1#/WE#/DQMLU/TxD6	DQMLU	Connected to SDRAM DQMU pin	CN6, pin 9	
6	PC5/RAS#/CRx0 / CRx0/CRx1/CRx2/IRQ0	RAS#	Connected to SDRAM RAS# pin	–	SW6-1: OFF
		–	–	CN6, pin 14	SW6-1: ON
7	PVcc				
8	PC6/CAS#/SCK7/CTx0/ CTx0&CTx1&CTx2	CAS#	Connected to SDRAM CAS# pin	–	SW6-1: OFF
		–	–	CN6, pin 15	SW6-1: ON
9	Vss				
10	PC7/CKE/RxD7/CRx1/ CRx0/CRx1/IRQ1	CKE	Connected to SDRAM CKE pin	–	SW6-1: OFF
		–	–	CN6, pin 16	SW6-1: ON
11	Vcc				
12	PC8/CS3#/TxD7/ CTx1/CTx0&CTx1	CS3#	Connected to SDRAM CS# pin	–	SW6-1: OFF
		–	–	CN6, pin 17	SW6-1: ON
13	PB1/A1/TIOC0A	A1	Address bus	CN4, pin 28	
14	PB2/A2/TIOC0B	A2	Address bus	CN4, pin 27	
15	PB3/A3/TIOC0C	A3	Address bus	CN4, pin 26	
16	PJ14/DV_DATA14 / LCD_DATA14/PINT6/ PWM2G/TxD6	PWM2G	PWM output	CN11, pin A1	TTL level
		DV_DATA14	DV input		
		–	–	CN1, pin 4	
17	PVcc				
18	PJ15/DV_DATA15/ LCD_DATA15/PINT7/ PWM2H/TxD7	PWM2H	PWM output	CN11, pin B1	TTL level
		DV_DATA15	DV input		
		–	–		
19	Vss				
20	PB4/A4/TIOC0D	A4	Address bus	CN4, pin 25	
21	Vcc				
22	PJ16/DV_DATA16/ LCD_DATA16/RSPCK0/ TIOC0A/SIOFSCK	PJ16	Connected to SW6-5 as user input port 1	CN11, pin B13	
		DV_DATA16	DV input		
23	PJ17/DV_DATA17/ LCD_DATA17/SSL00/ TIOC0B/SIOFSYNC	PJ17	Connected to SW6-6 as user input port 2	CN11, pin B12	
		DV_DATA17	DV input		

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.2 SH7269 Pin Functions (2/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
24	PJ18/DV_DATA18/ LCD_DATA18/MOSI0/ TIOC0C/SIOFTxD	PJ18	Connected to LED2 as user output port 1	CN11, pin B8	
		DV_DATA18	DV input		
25	PB5/A5/TIOC1A	A5	Address bus	CN4, pin 22	
26	PB6/A6/TIOC1B	A6	Address bus	CN4, pin 21	
27	PVcc				
28	PB7/A7/TIOC2A	A7	Address bus	CN4, pin 20	
29	Vss				
30	PB8/A8/TIOC2B	A8	Address bus	CN4, pin 19	
31	Vcc				
32	PB9/A9/TIOC3A	A9	Address bus	CN4, pin 18	
33	PB10/A10/TIOC3B	A10	Address bus	CN4, pin 17	
34	PB11/A11/TIOC3C	A11	Address bus	CN4, pin 14	
35	PB12/A12/TIOC3D	A12	Address bus	CN4, pin 13	
36	PJ19/DV_DATA19/ LCD_DATA19/MISO0/TIOC0D/ SIOFRxD/AUDIO_XOUT	PJ19	Connected to LED3 as user output port 2	CN11, pin A12	
		DV_DATA19	DV input		
		–	–	CN7, pin 40	
37	PVcc				
38	PJ20/DV_DATA20/ LCD_DATA20/LCD_TCON3/ IRQ0/CRx2/CRx0/CRx1/CRx2	–	–	CN7, pin 8	JP9: 1-2
		DV_DATA20	DV input	CN11, pin B4	JP9: 2-3
		–	–	CN1, pin 17	
39	Vss				
40	PB13/A13/QIO2_1 / SPBIO2_1	A13	Address bus	CN4, pin 12	
		QIO2_1 / SPBIO2_1	Connected to serial flash memory 2 IO2 pin		
41	Vcc				
42	PJ21/DV_DATA21 LCD_DATA21/LCD_TCON4/ IRQ1/CTx2/CTx0&CTx1&CTx2	IRQ1	IRQ1 switch	–	JP8: 1-2
		DV_DATA21	DV input	CN11, pin A14	JP8: 2-3
		–	–	CN1, pin 18	
43	PJ22/DV_DATA22/ LCD_DATA22/LCD_TCON5/ IRQ2/CRx1/CRx0/CRx1	DV_DATA22	DV input	CN11, pin B14	
		LCD_TCON5	Connected to LCD module DE pin	CN1, pin 24 CN10, pin B17	
44	PJ23/DV_DATA23/ LCD_DATA23/LCD_TCON6/ IRQ3/CTx1/CTx0&CTx1	DV_DATA23	DV input	CN11, pin A15	
		LCD_TCON6	Connected to the LCD module M_DISP pin	CN1, pin 18 CN10, pin B18	
45	PB14/A14/QIO3_1 / SPBIO3_1	A14	Address bus	CN4, pin 11	
		QUI3_1 / SPBIO3_1	Connected to serial flash memory 2 IO3 pin		
46	PB15/A15/QIO2_0 / SPBIO2_0	A15	Address bus	CN4, pin 10	
		QIO2_0 / SPBIO2_0	Connected to serial flash memory 1 IO2 pin		
47	PVcc				
48	PB16/A16/QIO3_0 / SPBIO3_0	A16	Address bus	CN4, pin 9	
		QIO3_0 / SPBIO3_0	Connected to serial flash memory 1 IO3 pin		
49	Vss				

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.3 SH7269 Pin Functions (3/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
50	PB17/A17/QSPCLK_0/ RSPCK0 / SPBCLK	A17	Address bus	CN4, pin 6	
51	VCC				
52	PB18/A18/QSSL_0/SSL00 / SPBSSL	A18	Address bus	CN4, pin 5	JP4: Open
		QSSL_0/ SSL00/ SPBSSL	Connected to serial flash memory 1 CS pin	–	JP4: 1-2
53	PB19/A19/QMO_0/QIO0_0/ MOSI0 / SPBMO_0/SPBIO0_0	A19	Address bus	CN4, pin 4	
		QMO_0/QIO0_0/ MOSI0 / SPBMO_0/SPBIO0_0	Connected to serial flash memory 1 SI pin		
54	PB20/A20/QMI_0/QIO1_0/ MISO0 / SPBMI_0/SPBIO1_0	A20	Address bus	CN4, pin 3	
		QMI_0/QIO1_0/ MISO0 / SPBMI_0/SPBIO1_0	Connected to serial flash memory 1 SO pin		
55	Vss				
56	PB21/A21/CRx2/IERxD	A21	Address bus	CN4, pin 2	
57	Vcc				
58	PB22/A22/CTx2/IETxD/CS4#	A22	Address bus	CN4, pin 1	
59	PC0/CS0#/MD_BOOT2	CS0#	Connected to NOR flash memory CE# pin	CN6, pin 5	JP5: 1-2
		MD_BOOT2	Connected to SW5-4 as boot mode input 2		JP5: 2-3
60	PVcc				
61	CKIO	CKIO	Connected to SDRAM CLK pin	CN6, pin 20	
62	Vss				
63	PA0/MD_BOOT0	MD_BOOT0	Connected to SW5-2 as boot mode input 0	CN1, pin 10	RES#: low
64	Vcc				
65	PA1/MD_BOOT1	MD_BOOT1	Connected to SW5-3 as boot mode input 1	CN1, pin 9	RES#: low
66	PJ28/SSISCK5/TIOC1B/ RTS7#	–	–	CN7, pin 22	
67	PJ29/SSIWS5/TIOC2A/ IERxD	–	–	CN7, pin 24	SW6-4: ON
				CN1, pin 19	SW6-4: OFF
68	PJ30/SSIDATA5/TIOC2B/ IETxD	–	–	CN7, pin 23	SW6-4: ON
				CN1, pin 20	SW6-4: OFF
69	PJ31/DV_CLK	DV_CLK	DV input	CN11, pin B16	
		–	–	CN7, pin 27	
70	PE0/SCL0/TCLKA/ LCD_EXTCLK	–	–	CN7, pin 5	
71	PE1/SDA0/TCLKB/ AUDIO_CLK/DV_CLK	–	–	CN7, pin 8	
72	PE2/SCL1/TCLKC/IOIS16#/ DV_VSYNC	SCL1	Connected to EEPROM SCL pin	CN7,, pin 7	
		–	–		
73	PE3/SDA1/TCLKD/ADTRG#/ DV_HSYNC	SDA1	Connected to EEPROM SDA pin	CN7, pin 10	
		–	–		
		–	–	CN7, pin 12	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.4 SH7269 Pin Functions (4/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
74	PE4/SCL2/RxD4/DV_VSYNC	DV_VSYNC	DV input	CN11, pin A17	
75	PE5/SDA2/RxD5/DV_HSYNC	DV_HSYNC	DV input	CN11, pin B17	
76	PE6/SCL3/RxD6	–	–	CN6, pin 12	
77	PE7/SDA3/RxD7	–	–	CN6, pin 13	
78	PVcc				
79	NMI	NMI	Non-maskable interrupt	–	
80	Vss				
81	ASEMD#	ASEMD#	ASE mode select	–	H-UDI
82	Vcc				
83	PLLVcc				
84	EXTAL			CN7, pin 9	
85	XTAL	XTAL	Open	–	
86	PLLVss				
87	PLLVss				
88	RES#	RES#	Reset input	CN7, pin 6	
89	RTC_X1	RTC_X1	Connects the real time clock resonator to MCU	–	32.768kHz
90	RTC_X2	RTC_X2		–	
91	USBDPVcc				
92	USBDPVss				
93	DM	DM	USB differential D− data	–	
94	DP	DP	USB differential D+ data	–	
95	VBUS	VBUS	VBUS input	–	
96	USBDVcc				
97	USBDVss				
98	REFRIN	REFRIN	Reference input	–	Connects a 5.6 kΩ±1% resistor
99	USBAVss				
100	USBAPVcc				
101	USBAVcc				
102	USBAVss				
103	USBUVcc				
104	USBUVss				
105	USB_X1	USB_X1	Connects the USB external clock to MCU	–	48MHz
106	USB_X2	USB_X2	Open	–	
107	PVcc				
108	VIDEO_X1	VIDEO_X1	Connects the digital video decoder external clock to MCU	–	27MHz
109	VIDEO_X2	VIDEO_X2	Open	–	
110	Vss				
111	DVAVcc				
112	DVAVss				
113	VIN1	VIN1	Analog video signal input	CN10, pin A19	
114	VIN2	VIN2	Analog video signal input	CN10, pin B20	
115	VRT	VRT	Top reference voltage	–	
116	VRB	VRB	Bottom reference voltage	–	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.5 SH7269 Pin Functions (5/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
117	BIAS	BIAS	Reference voltage	–	Connects a 24 kΩ±1% resistor
118	PH0/AN0/PINT0	–	–	CN3, pin 4	
119	PH1/AN1/PINT1	–	–	CN3, pin 3	
120	PH2/AN2/PINT2	–	–	CN3, pin 8	
121	PH3/AN3/PINT3	–	–	CN3, pin 7	
122	PH4/AN4/PINT4	–	–	CN3, pin 12	
				CN11, pin B18	
123	PH5/AN5/PINT5/ LCD_EXTCLK	–	–	CN3, pin 11	
				CN11, pin A19	
124	AVss				
125	PH6/AN6/PINT6	–	–	CN3, pin 16	
				CN11, pin B19	
126	AVcc				
127	PH7/AN7/PINT7	–	–	CN3, pin 15	
				CN11, pin A20	
128	AVref				
129	TRST#	TRST#	Initialization signal input pin	–	H-UDI
130	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Break mode acknowledge	–	H-UDI
		ASEBRK#	Break request		
131	TDO	TDO	Test data output	–	H-UDI
132	TDI	TDI	Test data input	–	H-UDI
133	TMS	TMS	Test mode select	–	H-UDI
134	TCK	TCK	Test clock	–	H-UDI
135	Vss				
136	PG0/D16/LCD_DATA0/ IRQ0/TIOC0A	LCD_DATA0	Connected to LCD module D0 pin	CN9, pin 2 CN10, pin A1	B0
137	Vcc				
138	PG1/D17/LCD_DATA1/ IRQ1/TIOC0B	LDC_DATA1	Connected to LCD module D1 pin	CN9, pin 1 CN10, pin B1	B1
139	Vss				
140	PG2/D18/LCD_DATA2/ IRQ2/TIOC0C	LCD_DATA2	Connected to LCD module D2 pin	CN9, pin 4 CN10, pin A2	B2
141	PVcc				
142	AUDIO_X2	AUDIO_X2	Open	–	
143	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	–	11.2896 MHz
144	Vss				
145	PG3/D19/LCD_DATA3/ IRQ3/TIOC0D	LCD_DATA3	Connected to LCD module D3 pin	CN9, pin 3 CN10, pin B2	B3
146	Vcc				
147	PG4/D20/LCD_DATA4/ IRQ4/TIOC1A	LCD_DATA4	Connected to LCD module D4 pin	CN9, pin 6 CN10, pin B3	B4
148	PG5/D21/LCD_DATA5/ IRQ5/TIOC1B	LCD_DATA5	Connected to LCD module D5 pin	CN9, pin 8 CN10, pin A4	B5
149	PG6/D22/LCD_DATA6/ IRQ6/TIOC2A	LCD_DATA6	Connected to LCD module D6 pin	CN9, pin 7 CN10, pin B4	B6
150	PG7/D23/LCD_DATA7/ IRQ7/TIOC2B	LCD_DATA7	Connected to LCD module D7 pin	CN9, pin 9 CN10, pin B4	B7

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.6 SH7269 Pin Functions (6/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
151	PJ0/DV_DATA0/LCD_DATA0 /SD_CD_1/PWM1A	DV_DATA0	DV input	CN11, pin A6	
		–	–	CN7, pin 15	SW6-3: OFF
		–	–	CN7, pin 17	SW6-3: ON
152	PVcc				
153	PJ1/DV_DATA1/LCD_DATA1 /SD_WP_1/PWM1B	DV_DATA1	DV input	CN11, pin B6	
		–	–	CN7, pin 16	SW6-3: OFF
		–	–	CN7, pin 20	SW6-3: ON
154	Vss				
155	PG8/D24/LCD_DATA8/ PINT0/TIOC3A	LCD_DATA8	Connected to LCD module D8 pin	CN 9, pin 12 CN 10, pin A6	G0
156	Vcc				
157	PJ2/DV_DATA2/LCD_DATA2 /SD_D1_1/PWM1C	DV_DATA 2	DV input	CN11, pin A10	
		–	–	CN7, pin 13	SW6-3: OFF
		–	–	CN7, pin 19	SW6-3: ON
158	PJ3/DV_DATA3/LCD_DATA3 /SD_D0_1/PWM1D	DV_DATA3	DV input	CN11, pin B9	
		–	–	CN7, pin 14	SW6-3: OFF
		–	–	CN7, pin 22	SW6-3: ON
159	PJ4/DV_DATA4/LCD_DATA4 /SD_CLK_1/PWM1E	DV_DATA4	DV input	CN11, pin A9	
		–	–	CN7, pin 3	SW6-3: OFF
		–	–	CN7, pin 24	SW6-3: ON
160	PG9/D25/LCD_DATA9/ PINT1/TIOC3B	LCD_DATA9	Connected to LCD module D9 pin	CN9, pin 11 CN10, pin B6	G1
161	PG10/D26/LCD_DATA10/ PINT2/TIOC3C	LCD_DATA10	Connected to LCD module D10 pin	CN9, pin 14 CN10, pin A7	G2
162	PVcc				
163	PG11/D27/LCD_DATA11/ PINT3/TIOC3D	LCD_DATA11	Connected to LCD module D11 pin	CN9, pin 13 CN10, pin B7	G3
164	Vss				
165	PG12/D28/LCD_DATA12/ PINT4	LCD_DATA12	Connected to LCD module D12 pin	CN9, pin 16 CN10, pin B8	G4
166	Vcc				
167	PG13/D29/LCD_DATA13/ PINT5	LCD_DATA13	Connected to LCD module D13 pin	CN9, pin 18 CN10, pin A9	G5
168	PG14/D30/LCD_DATA14/ PINT6	LCD_DATA14	Connected to LCD module D14 pin	CN9, pin 17 CN10, pin B9	G6
169	PG15/D31/LCD_DATA15/ PINT7	LCD_DATA15	Connected to LCD module D15 pin	CN9, pin 20 CN10, pin A10	G7
170	PG16/WE2#/ICIORD#/DQMUL /LCD_DATA16/AUDATA0	LCD_DATA16	Connected to LCD module D16 pin	CN10, pin A11	R0
		AUDATA0	Connected to the H-UDI port connector (J3)		AUD
171	PJ5/DV_DATA5/LCD_DATA5 /SD_CMD_1/PWM1F	DV_DATA5	DV input	CN11, pin A7	
		–	–	CN7, pin 4	SW6-3: OFF
		–	–	CN7, pin 23	SW6-3: ON
172	PVcc				
173	PJ6/DV_DATA6/LCD_DATA6 /SD_D3_1/PWM1G	DV_DATA6	DV input	CN11, pin B7	
		–	–	CN7, pin 1	SW6-3: OFF
		–	–	CN7, pin 25	SW6-3: ON
174	Vss				

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.7 SH7269 Pin Functions (7/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
175	PG17/WE3#/ICIOWR#/AH#/ DQMUU/LCD_DATA17/ AUDATA1	LCD_DATA17	Connected to LCD module D17 pin	CN10, pin B11	R1
		AUDATA1	Connected to the H-UDI port connector (J3)		AUD
176	Vcc				
177	PJ7/DV_DATA7/LCD_DATA7/ SD_D2_1/PWM1H	DV_DATA7	DV input	CN11, pin A5	
		–	–	CN7, pin 2	SW6-3: OFF
		–	–	CN7, pin 28	SW6-3: ON
178	PJ8/DV_DATA8/LCD_DATA8/ PINT0/PWM2A/CTS5#	PWM2A	PWM output	CN11, pin A4	TTL level
		DV_DATA8	DV input		
		–	–	CN1, pin 12	
179	PJ9/DV_DATA9/LCD_DATA9/ PINT1/PWM2B/RTS5#	PWM2B	PWM output	CN11, pin B3	TTL level
		DV_DATA9	DV input		
		–	–	CN1, pin 5	
180	PG18/DV_DATA4/ LCD_DATA18/SPDIF_IN/SCK4	LCD_DATA18	Connected to LCD module D18 pin	CN10, pin A12	R2
181	PG19/DV_DATA5/ LCD_DATA19/SPDIF_OUT/ SCK5	LCD_DATA19	Connected to LCD module D19 pin	CN10, pin B12	R3
182	PVcc				
183	PG20/DV_DATA6/ LCD_DATA20/LCD_TCON3/ RxD4	LCD_DATA20	Connected to LCD module D20 pin	CN10, pin B13	R4
184	Vss				
185	PG21/DV_DATA7/ LCD_DATA21/LCD_TCON4/ TxD4/AUDATA2	LCD_DATA21	Connected to LCD module D21 pin	CN10, pin A14	R5
		AUDATA2	Connected to the H-UDI port connector (J3)		AUD
186	Vcc				
187	PG22/LCD_DATA22/ LCD_TCON5/RxD5/ AUDSYNC#	LCD_DATA22	Connected to LCD module D22 pin	CN10, pin B14	R6
		AUDSYNC#	Connected to the H-UDI port connector (J3)		AUD
		–	–	CN1, pin 15	
188	PG23//LCD_DATA23/ LCD_TCON6/TxD5/AUDATA3	LCD_DATA23	Connected to LCD module D23 pin	CN10, pin A15	R7
		AUDATA3	Connected to the H-UDI port connector (J3)		AUD
		–	–	CN1, pin 14	
189	PG24/LCD_CLK	LCD_CLK	Connected to LCD module CLK pin	CN9, pin 23 CN10, pin A16	
190	PG25/LCD_TCON0	LCD_TCON0	Connected to LCD module VSYNC pin	CN9, pin 19 CN10, pin B16	
191	PG26/LCD_TCON1	LCD_TCON1	Connected to LCD module HSYNC pin	CN9, pin 21 CN10, pin A17	
192	PG27/LCD_TCON2/ LCD_EXTCLK	LCD_EXTCLK	Connects LCD module external clock to MCU	CN9, pin 26	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.8 SH7269 Pin Functions (8/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
193	PF0/BREQ#0/QSPCLK_1/ RSPCK1/TIOC4A/DREQ0/ AUDCK	QSPCLK_1/ RSPCK1	Connected to serial flash memory 2 SCK pin	CN7, pin 30	
		AUDCK	Connected to the H-UDI port connector (J3)		AUD
		–	–		
				CN9, pin 28	
194	PVcc				
195	PF1/BACK#/QSSL_1/SSL10/ TIOC4B/DACK0	QSSL_1/ SSL10	Connected to serial flash memory 2 CS# pin	CN5, pin 20	
196	Vss				
197	PF2/WAIT#/QMO_1/QIO0_1/ MOSI1/TIOC4C/TEND0 / SPBMO_1/SPBIO0_1	QMO_1/ QIO0_1/MOSI1 / SPBMO_1/SPBI O0_1	Connected to serial flash memory 2 SI pin	CN7, pin 31	
		–	–	CN9, pin 30	
198	PF3/CS2#/QMI_1/QIO1_1/ MISO1/TIOC4D/AUDIO_XOUT / SPBMI_1/SPBIO1_1	QMI_1/QIO1_1/M ISO1 / SPBMI_1/SPBIO 1_1	Connected to serial flash memory 2 SO pin	CN7, pin 33	
		–	–		
199	PF4/CS5#/CE1A#/SSISCK0/ SGOUT_0	SGOUT_0		CN7, pin 36	0 Ω resistor
		–	–		
200	PF5/SSIWS0/SGOUT_1	SGOUT_1		CN7, pin 35	0 Ω resistor
		–	–		
201	PF6/CE2A#/SSITxD0/ SGOUT_2	SGOUT_2		CN7, pin 37	0 Ω resistor
		–	–		
202	PF7/SSIRxD0/RxD0/ SGOUT_3/CTS1#	SGOUT_3		CN7, pin 38	0 Ω resistor
		–	–		
203	PF8/A23/TxD0	A23	Address bus	CN5, pin 19	
204	PF9/BS#/DV_DATA0/SCK0/ MMC_D4/RTS1#	PF9		CN5, pin 18	
205	PVcc				
206	PF10/CS1#/SSISCK1/ DV_DATA1/SCK1/MMC_D5	–	–	CN7, pin 17	
207	Vss				
208	PF11/SSIWS1/DV_DATA2/ RxD1/MMC_D6	–	–	CN7, pin 20	
209	PF12/SSIDATA1/DV_DATA3/ TxD1/MMC_D7	–	–	CN7, pin 19	
210	PF13/A24/SSISCK2/SCK2	A24	Address bus	CN5, pin 17	
211	PF14/A25/SSIWS2/RxD2	RxD2	Connected to the RS-232C connector (J10)	CN5, pin 16	
212	PF15/A0/SSIDATA2/ WDTOVF#/TxD2/UBCTRG#	TxD2	Connected to the RS-232C connector (J10)	CN5, pin 15	
213	PVcc				
214	PJ10/DV_DATA10/ LCD_DATA10/PINT2/PWM2C/ SCK5#	PWM2C	PWM output	CN11, pin A2	TTL level
		DV_DATA10	DV input		
		–	–	CN1, pin 13	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.9 SH7269 Pin Functions (9/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
215	Vss				
216	PF16/SD_CD_0/FCE#/ IRQ4/MMC_CD	SD_CD_0 MMC_CD	Connected to SD/MMC card slot CD pin	CN5, pin 13	SW6-2: ON
		FCE#	Connected to NAND flash memory CE# pin	CN5, pin 12	SW6-2: OFF
217	PF17/SD_WP_0/FRB/IRQ5	SD_WP_0	Connected to SD/MMC card slot WP pin	CN5, pin 11	SW6-2: ON
		FRB	Connected to NAND flash memory R/B# pin	CN5, pin 10	SW6-2: OFF
218	PF18/SD_D1_0/SSISCK3/ IRQ6/MMC_D1	SD_D1_0/ MMC_D1	Connected to SD/MMC card slot DAT1 pin	CN5, pin 8	
219	PJ11/DV_DATA11/ LCD_DATA11/PINT3/PWM2D/ SCK6	PWM2D	PWM output	CN1, pin B2	TTL level
		DV_DATA11	DV input		
		–	–	CN1, pin 1	
220	PJ12/DV_DATA12/ LCD_DATA12/PINT4/PWM2E/ SCK7	PWM2E	PWM output	CN11, pin B11	TTL level
		DV_DATA12	DV input		
		–	–	CN9, pin 27	
221	PJ13/DV_DATA13/ LCD_DATA13/PINT5/PWM2F/ TxD5	PWM2F	PWM output	CN11, pin A11	TTL level
		DV_DATA13	DV input		
		–	–	CN7, pin 32	
222	PVcc				
223	PF19/SD_D0_0/SSIWS3/ IRQ7/MMC_D0	SD_D0_0 MMC_D0	Connected to SD/MMC card slot DAT0 pin	CN5, pin 7	
224	Vss				
225	PF20/SD_CLK_0/SSIDATA3/ MMC_CLK	SD_CLK_0/ MMC_CLK	Connected to SD/MMC card slot CLK pin	CN5, pin 5	
226	Vcc				
227	PF21/SD_CMD_0/SCK3/ MMC_CMD	SD_CMD_0/ MMC_CMD	Connected to SD/MMC card slot CMD pin	CN5, pin 4	
228	PF22/SD_3_0/RxD3/ MMC_D3	SD_D3_0/ MMC_D3	Connected to SD/MMC card slot DAT3 pin	CN5, pin 3	
229	PF23/SD_D2_0/TxD3/ MMC_D2	SD_D2_0/ MMC_D2	Connected to SD/MMC card slot DAT2 pin	CN5, pin 2	
230	PD0/D0/PWM1A	D0	Data bus	CN8, pin 1	
231	PVcc				
232	PJ24/SGOUT_0/SSISCK4/ LCD_TCON3/SPDIF_IN/SCK7	–	–	CN7, pin 25	
233	Vss				
234	PD1/D1/PWM1B	D1	Data bus	CN8, pin 3	
235	PD2/D2/PWM1C	D2	Data bus	CN8, pin 6	
236	PD3/D3/PWM1D	D3	Data bus	CN8, pin 8	
237	PJ25/SGOUT_1/SSIWS4/ LCD_TCON4/SPDIF_OUT/ RxD7	–	–	CN7, pin 28	
238	PJ26/SGOUT_2/SSIDATA4/ LCD_TCON5/TxD7	–	–	CN7, pin 27	
239	PJ27/SGOUT_3/TIOC1A/ CTS7#	–	–	CN9, pin 29	
240	PVcc				
241	Vss				
242	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and NAND flash memory RE# pin	CN8, pin 11	Auto-switch

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 2.2.10 SH7269 Pin Functions (10/10)

No.	Name	Symbol	Description	Expansion Connector	Remarks
243	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and NAND flash memory CLE pin	CN8, pin 13	Auto-switch
244	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and NAND flash memory ALE pin	CN8, pin 16	Auto-switch
245	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and NAND flash memory WE# pin	CN8, pin 18	Auto-switch
246	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 2	
247	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 4	
248	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 7	
249	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 9	
250	PVcc				
251	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 12	
252	Vss				
253	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 14	
254	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 17	
255	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 19	
256	MD_CLK0	MD_CLK0	Connected to SW5-1 as the clock mode input	–	RES#: low

Legend: : 3.3V power supply, : 1.25V power supply, : GND

2.2.3 R0K572690C000BR Module Availability

The following table shows which combination of modules can/cannot be used.

Table 2.2.11 R0K572690C000BR Module Availability

				R0K572690C000BR																
	SH7269 Peripherals	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory 1	Serial flash memory 2	USB	SD/MMC card	H-UDI (14-pin)	H-UDI (38-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C	LCD	DV	PWM
R0K572690C000BR	BSC	U6	NOR flash memory		Y	Y	Y	N	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	BSC	U9	SDRAM	Y		Y	Y	Y	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	FLCTL	U7	NAND flash memory	Y	Y		Y	Y	Y	Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	RSPI	U10	Serial flash memory 1	N	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	RSPI	U10	Serial flash memory 2	(1)	(1)	Y	Y	Y		Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y
	USB	J1, J2	USB	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	SDHI/MMC	J11	SD/MMC card	Y	Y	(2)	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y	Y	Y		(3)	Y	Y	Y	Y	Y	Y	Y	Y
	H-UDI, AUD	J3	H-UDI (38-pin)	Y	Y	Y	Y	Y	N	Y	Y	(3)		Y	Y	Y	Y	Y	N	Y	Y
	I/O ports	LED2, LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	(6)	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	(5)	Y
	I/O ports	SW5, SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	(7)	Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y
	VDC4	CN10	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y		(4)	Y
	VDC4	CN11	DV	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(6)	Y	(5)	(7)	Y	(4)		(8)
	PWM	CN11	PWM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(8)	

Y: Yes, N: No

Notes:
1. When using a serial flash memory with NOR flash memory or SDRAM, quad mode cannot be used.
2. PF16 and PF17 are multiplexed pins. When setting SW6-2, ether SD/MMC card or NAND flash memory can be used.
3. Either 14-pin or 38-pin H-UDI port connector can be used.
4. PJ22 and PJ23 are multiplexed pins. Either LCD or DV can be used.
5. PJ21 is a multiplexed pin. Either IRQ1 switch or DV can be used.
6. PJ19 and PJ18 are multiplexed pins. Either LED or DV can be used.
7. PJ17 and PJ16 are multiplexed pins. Either DIP switches or DV can be used.
8. PJ15 to PJ8 are multiplexed pins. Either DV or PWM can be used.

2.2.4 SH7269 Multiplexed Pins Used on the R0K572690C000BR

Table 2.2.12 to Table 2.2.25 list the SH7269 multiplexed pin functions used on the R0K572690C000BR.

These multiplexed pins are set as port input pins by default. Set the MD bit in the Port control register to use the SH7269 peripheral functions (except I/O ports).

Table 2.2.12 SH7269 Multiplexed Pin Functions (BSC1)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
BSC	CS0#	PCCR0	PC0MD = B'1 (1)	PC0/**CS0#**/MD_BOOT2
	CS3#	PCCR2	PC8MD[2:0] = B'001	PC8/**CS3#**/TxD7/CTx1/CTx0&CTx1
	RD#	PCCR0	PC1MD = B'1 (1)	PC1/**RD#**
	WE0#/DQMLL	PCCR0	PC3MD[1:0] = B'01	PC3/**WE0#**/**DQMLL**/RxD6
	WE1#/WE#/DQMLU	PCCR1	PC4MD[1:0] = B'01	PC4/**WE1#**/**DQMLU**/TxD6
	RAS#	PCCR1	PC5MD[2:0] = B'001	PC5/**RAS#**/CRx0/CRx0/CRx1/CRx2/IRQ0
	CAS#	PCCR1	PC6MD[2:0] = B'001	PC6/**CAS#**/SCK7/CTx0/CTx0&CTx1&CTx2
	CKE	PCCR1	PC7MD[2:0] = B'001	PC7/**CKE**/RxD7/CRx1/CRx0/CRx1/IRQ1
	RD/WR#	PCCR0	PC2MD[1:0] = B'01	PC2/**RD/WR#**/SCK6
	A24	PFCR3	PF13MD[2:0] = B'001	PF13/**A24**/SSISCK2/SCK2
	A23	PFCR2	PF8MD[2:0] = B'001	PF8/**A23**/TxD0
	A22	PBCR5	PB22MD[2:0] = B'001	PB22/**A22**/CTx2/IETxD/CS4#
	A21	PBCR5	PB21MD[1:0] = B'01	PB21/**A21**/CRx2/IERxD
	A20	PBCR5	PB20MD[1:0] = B'001 (1)	PB20/**A20**/QMISO0&QIO10/MISO0 / SPBMI_0/SPBIO1_0
	A19	PBCR4	PB19MD[1:0] = B'001 (1)	PB19/**A19**/QMO_0&QIO0_0/MOSI0 / SPBMO_0/SPBIO0_0
	A18	PBCR4	PB18MD[1:0] = B'001 (1)	PB18/**A18**/QSSL_0/SSL00 / SPBSSL
	A17	PBCR4	PB17MD[1:0] = B'001 (1)	PB17/**A17**/QSPCLK_0/RSPCK0 / SPBCLK
	A16	PBCR4	PB16MD[1:0] = B'001 (1)	PB16/**A16**/QIO3_0 / SPBIO3_0
	A15	PBCR3	PB15MD[1:0] = B'001 (1)	PB15/**A15**/QIO2_0 / SPBIO2_0
	A14	PBCR3	PB14MD[1:0] = B'001 (1)	PB14/**A14**/QIO3_1 / SPBIO3_1
	A13	PBCR3	PB13MD[1:0] = B'001 (1)	PB13/**A13**/QIO2_1 / SPBIO2_1
	A12	PBCR3	PB12MD[1:0] = B'01 (1)	PB12/**A12**/TIOC3D
	A11	PBCR2	PB11MD[1:0] = B'01 (1)	PB11/**A11**/TIOC3C
	A10	PBCR2	PB10MD[1:0] = B'01 (1)	PB10/**A10**/TIOC3B
	A9	PBCR2	PB9MD[1:0] = B'01 (1)	PB9/**A9**/TIOC3A
	A8	PBCR2	PB8MD[1:0] = B'01 (1)	PB8/**A8**/TIOC2B
	A7	PBCR1	PB7MD[1:0] = B'01 (1)	PB7/**A7**/TIOC2A
	A6	PBCR1	PB6MD[1:0] = B'01 (1)	PB6/**A6**/TIOC1B
	A5	PBCR1	PB5MD[1:0] = B'01 (1)	PB5/**A5**/TIOC1A
	A4	PBCR1	PB4MD[1:0] = B'01 (1)	PB4/**A4**/TIOC0D
	A3	PBCR0	PB3MD[1:0] = B'01 (1)	PB3/**A3**/TIOC0C
	A2	PBCR0	PB2MD[1:0] = B'01 (1)	PB2/**A2**/TIOC0B
	A1	PBCR0	PB1MD[1:0] = B'01 (1)	PB1/**A1**/TIOC0A
	D15	PDCR3	PD15MD[1:0] = B'01 (1)	PD15/**D15**/**NAF7**/PWM2H
	D14	PDCR3	PD14MD[1:0] = B'01 (1)	PD14/**D14**/**NAF6**/PWM2G
	D13	PDCR3	PD13MD[1:0] = B'01 (1)	PD13/**D13**/**NAF5**/PWM2F
	D12	PDCR3	PD12MD[1:0] = B'01 (1)	PD12/**D12**/**NAF4**/PWM2E
	D11	PDCR2	PD11MD[1:0] = B'01 (1)	PD11/**D11**/**NAF3**/PWM2D
	D10	PDCR2	PD10MD[1:0] = B'01 (1)	PD10/**D10**/**NAF2**/PWM2C
	D9	PDCR2	PD9MD[1:0] = B'01 (1)	PD9/**D9**/**NAF1**/PWM2B
	D8	PDCR2	PD8MD[1:0] = B'01 (1)	PD8/**D8**/**NAF0**/PWM2A
	D7	PDCR1	PD7MD[1:0] = B'01 (1)	PD7/**D7**/**FWE#**/PWM1H
	D6	PDCR1	PD6MD[1:0] = B'01 (1)	PD6/**D6**/**FALE**/PWM1G

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 2.2.13 SH7269 Multiplexed Pin Functions (BSC2)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
BSC	D5	PDCR1	PD5MD[1:0] = B'01 (1)	PD5 / **D5**/**FCLE** / PWM1F
	D4	PDCR1	PD4MD[1:0] = B'01 (1)	PD4/**D4**/**FRE**#/PWM1E
	D3	PDCR0	PD3MD[1:0] = B'01 (1)	PD3/**D3**/PWM1D
	D2	PDCR0	PD2MD[1:0] = B'01 (1)	PD2/**D2**/PWM1C
	D1	PDCR0	PD1MD[1:0] = B'01 (1)	PD1/**D1**/ PWM1B
	D0	PDCR0	PD0MD[1:0] = B'01 (1)	PD0/**D0**/PWM1A

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 2.2.14 SH7269 Multiplexed Pin Functions (INTC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
INTC	IRQ1	PJCR5	PJ21MD[2:0] = B'100	PJ21/DV_DATA21/LCD_DATA21/LCD_TCON4/ /**IRQ1**/CTx2/CTx0&CTx1&CTx2

Note: Bold text indicates the function used.

Table 2.2.15 SH7269 Multiplexed Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SCIF	RxD2	PFCR3	PF14MD[2:0] = B'100	PF14/A25/SSIWS2//**RxD2**
	TxD2	PFCR4	PF15MD[2:0] = B'100	PF15/A0/SSIDATA2/WDTOVF#/**TxD2**/UBCTRG#

Note: Bold text indicates the function used.

Table 2.2.16 SH7269 Multiplexed Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
IIC3	SDA1	PECR0	PE3MD[2:0] = B'001	PE3/**SDA1**/TCLKD/ADTRG#/DV_HSYNC
	LDA1	PECR0	PE2MD[2:0] = B'001	PE2/**SCL1**/TCLKC/IOIS16#/DV_VSYNC

Note: Bold text indicates the function used.

Table 2.2.17 SH7269 Multiplexed Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01 (1)	PD15/**D15**/**NAF7**/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01 (1)	PD14/**D14**/**NAF6**/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01 (1)	PD13/**D13**/**NAF5**/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01 (1)	PD12/**D12**/**NAF4**/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01 (1)	PD11/**D11**/**NAF3**/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01 (1)	PD10/**D10**/**NAF2**/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01 (1)	PD9/**D9**/**NAF1**/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01 (1)	PD8/**D8**/**NAF0**/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01 (1)	PD7/**D7**/**FWE#**/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01 (1)	PD6/**D6**/**FALE**/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01 (1)	PD5/**D5**/**FCLE**/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01 (1)	PD4/**D4**/**FRE#**/PWM1E
	FCE#	PFCR5	PF16MD[2:0] = B'011	PF16/SD_CD_0/**FCE#**/IRQ4/MMC_CD
	FRB	PFCR5	PF17MD[2:0] = B'011	PF17/SD_WP_0/**FRB**/IRQ5

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 2.2.18 SH7269 Multiplexed Pin Functions (RSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RSPI	MISO0	PBCR5	PB20MD[2:0] = B'011 (1)	PB20/A20/QMI_0/QIO1_0/**MISO0** / SPBMI_0/SPBIO1_0
	MOSI0	PBCR4	PB19MD[2:0] = B'011 (1)	PB19/A19/QMO_0/QIO_0/**MOSI0** / SPBMO_0/SPBIO0_0
	SSL00	PBCR4	PB18MD[2:0] = B'011 (1)	PB18/A18/QSSL_0/**SSL00** / SPBSSL
	RSPCK0	PBCR4	PB17MD[2:0] = B'011 (1)	PB17/A17/QSPCLK_0/**RSPCK0** / SPBCLK
	MISO1	PFCR0	PF3MD[2:0] = B'011	PF3/CS2#/QMI_1/QIO1_1/**MISO1**/TIOC4D/ AUDIO_XOUT / SPBMI_1/SPBIO1_1
	MOSI1	PFCR0	PF2MD[2:0] = B'011	PF2/WAIT#/QMO_1/QIO0_1/**MOSI1**/TIOC4C TEND0 / SPBMO_1/SPBIO0_1
	SSL10	PFCR0	PF1MD[2:0] = B'011	PF1/BACK#/QSSL_1/**SSL10**/TIOC4B/DACK0
	RSPCK1	PFCR0	PF0MD[2:0] = B'011	PF0/BREQ#/QSPCLK_1/**RSPCK1**/TIOC4A/ DREQ0/AUDCK

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 2.2.19 SH7269 Multiplexed Pin Functions (RQSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RQSPI	QIO3_0	PBCR4	PB16MD[2:0] = B'010 (1)	PB16/A16/**QIO3_0** / SPBIO3_0
	QIO2_0	PBCR3	PB15MD[2:0] = B'010 (1)	PB15/A15/**QIO2_0** / SPBIO2_0
	QIO1_0	PBCR5	PB20MD[2:0] = B'010 (1)	PB20/A20/**QMI_0**/**QIO1_0**/MISO0 / SPBMI_0/SPBIO1_0
	QIO0_0	PBCR4	PB19MD[1:0] = B'010 (1)	PB19/A19/**QMO_0**/**QIO0_0**/MOSI0 / SPBMO_0/SPBIO0_0
	QSSL_0	PBCR4	PB18MD[2:0] = B'010 (1)	PB18/A18/**QSSL_0**/SSL00 / SPBSSL
	QSPCLK_0	PBCR4	PB17MD[2:0] = B'010 (1)	PB17/A17/**QSPCLK_0**/RSPCK0/ SPBCLK
	QIO3_1	PBCR3	PB14MD[2:0] = B'010 (1)	PB14/A14/**QIO3_1** / SPBIO3_1
	QIO2_1	PBCR3	PB13MD[2:0] = B'010 (1)	PB13/A13/**QIO2_1** / SPBIO2_1
	QIO1_1	PFCR0	PF3MD[2:0] = B'010	PF3/CS2#/**QMI_1**/**QIO1_1**/MISO1/TIOC4D/ AUDIO_XOUT / SPBMI_1/SPBIO1_1
	QIO0_1	PFCR0	PF2MD[2:0] = B'010	PF2/WAIT#/**QMO_1**/**QIO0_1**/MOSI1/TIOC4C/ TEND0 / SPBMO_1/SPBIO0_1
	QSSL_1	PFCR0	PF1MD[2:0] = B'010	PF1/BACK#/**QSSL_1**/SSL10/TIOC4B/DACK0
	QSPCLK_1	PFCR0	PF0MD[2:0] = B'010	PF0/BREQ#/**QSPCLK_1**/RSPCK1/TIOC4A/DREQ0/ AUDCK

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 2.2.20 SH7269 Multiplexed Pin Functions (SPIBSC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SPIBSC	SPBCLK	PBCR4	PB17MD[2:0] = B'110 (1)	PB17 / A17 / QSPCLK_0 / RSPCK0 / **SPBCLK**
	SPBSSL	PBCR4	PB18MD[2:0] = B'110 (1)	PB18 / A18 / QSSL_0 / SSL00 / **SPBSSL**
	SPBMO_0/ SPBIO0_0	PBCR4	PB19MD[2:0] = B'110 (1)	PB19 / A19 / QMO_0/QIO0_0 / MOSI0 / **SPBMO_0/SPBIO0_0**
	SPBMI_0/ SPBIO1_0	PBCR5	PB20MD[2:0] = B'110 (1)	PB20 / A20 / QMI_0/QIO1_0 / MISO0 / **SPBMI_0/SPBIO1_0**
	SPBIO2_0	PBCR3	PB15MD[2:0] = B'110 (1)	PB15 / A15 / QIO2_0 / **SPBIO2_0**
	SPBIO3_0	PBCR4	PB16MD[2:0] = B'110 (1)	PB16 / A16 / QIO3_0 / **SPBIO3_0**
	SPBMO_1/ SPBIO0_1	PFCR0	PF2MD[2:0] = B'110	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / **SPBMO_1/SPBIO0_1**
	SPBMI_1/ SPBIO1_1	PFCR0	PF3MD[2:0] = B'110	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / **SPBMI_1/SPBIO1_1**
	SPBIO2_1	PBCR3	PB13MD[2:0] = B'110 (1)	PB13 / A13 / QIO2_1 / **SPBIO2_1**
	SPBIO3_1	PBCR3	PB14MD[2:0] = B'110 (1)	PB14 / A14 / QIO3_1 / **SPBIO3_1**

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 2.2.21 SH7269 Multiplexed Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SDHI	SD_CD_0	PFCR5	PF16MD[2:0] = B'001	PF16/**SD_CD_0**/FCE#/IRQ4/MMC_CD
	SD_WP_0	PFCR5	PF17MD[2:0] = B'001	PF17/**SD_WP_0**/FRB/IRQ5
	SD_D1_0	PFCR5	PF18MD[2:0] = B'001	PF18/**SD_D1_0**/SSISCK3/IRQ6/MMC_D1
	SD_D0_0	PFCR5	PF19MD[2:0] = B'001	PF19/**SD_D0_0**/SSIWS3/IRQ7/MMC_D0
	SD_CLK_0	PFCR6	PF20MD[2:0] = B'001	PF20/**SD_CLK_0**/SSIDATA3/MMC_CLK
	SD_CMD_0	PFCR6	PF21MD[2:0] = B'001	PF21/**SD_CMD_0**/SCK3/ MMC_CMD
	SD_D3_0	PFCR6	PF22MD[2:0] = B'001	PF22/**SD_D3_0**/RxD3/MMC_D3
	SD_D2_0	PFCR6	PF23MD[2:0] = B'001	PF23/**SD_D2_0**/TxD3/MMC_D2

Note: Bold text indicates the function used.

Table 2.2.22 SH7269 Multiplexed Pin Functions (MMC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
MMC	MMC_CD	PFCR5	PF16MD[2:0] = B'101	PF16/SD_CD_0/FCE#/IRQ4/**MMC_CD**
	MMC_D1	PFCR5	PF18MD[2:0] = B'101	PF18/SD_D1_0/SSISCK3/IRQ6/**MMC_D1**
	MMC_D0	PFCR5	PF19MD[2:0] = B'101	PF19/SD_D0_0/SSIWS3/IRQ7/**MMC_D0**
	MMC_CLK	PFCR6	PF20MD[2:0] = B'101	PF20/SD_CLK_0/SSIDATA3/**MMC_CLK**
	MMC_CMD	PFCR6	PF21MD[2:0] = B'101	PF21/SD_CMD_0/SCK3/**MMC_CMD**
	MMC_D3	PFCR6	PF22MD[2:0] = B'101	PF22/SD_D3_0/RxD3/**MMC_D3**
	MMC_D2	PFCR6	PF23MD[2:0] = B'101	PF23/SD_D2_0/TxD3/**MMC_D2**

Note: Bold text indicates the function used.

Table 2.2.23 SH7269 Multiplexed Pin Functions (VDC4)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
VDC4	LCD_EXTCLK	PGCR6	PG27MD[1:0] = B'11	PG27/LCD_TCON2/**LCD_EXTCLK**
	LCD_CLK	PGCR6	PG24MD[1:0] = B'10	PG24/**LCD_CLK**
	LCD_TCON6	PJCR5	PJ23MD[2:0] = B'011	PJ23/DV_DATA23/LCD_DATA23/**LCD_TCON6**/ IRQ3/CTx1/CTx0&CTx1
	LCD_TCON5	PJCR5	PJ22MD[2:0] = B'011	PJ22/DV_DATA22/LCD_DATA22/**LCD_TCON5**/ IRQ2/CRx1/CRx0/CRx1
	LCD_TCON1	PGCR6	PG26MD[1:0] = B'10	PG26/**LCD_TCON1**
	LCD_TCON0	PGCR6	PG25MD[1:0] = B'10	PG25/**LCD_TCON0**
	LCD_DATA23	PGCR5	PG23MD[2:0] = B'010	PG23/**LCD_DATA23**/LCD_TCON6/TxD5/AUDATA3
	LCD_DATA22	PGCR5	PG22MD[2:0] = B'010	PG22/**LCD_DATA22**/LCD_TCON5/RxD5/AUDSYNC#
	LCD_DATA21	PGCR5	PG21MD[2:0] = B'010	PG21/DV_DATA7/**LCD_DATA21**/LCD_TCON4/TxD4
	LCD_DATA20	PGCR5	PG20MD[2:0] = B'010	PG20/DV_DATA6/**LCD_DATA20**/LCD_TCON3/RxD4
	LCD_DATA19	PGCR4	PG19MD[2:0] = B'010	PG19/DV_DATA5/**LCD_DATA19**/SPDIF_OUT/SCK5
	LCD_DATA18	PGCR4	PG18MD[2:0] = B'010	PG18/DV_DATA4/**LCD_DATA18**/SPDIF_IN/SCK4
	LCD_DATA17	PGCR4	PG17MD[1:0] = B'10	PG17/WE3#/ICIOWR#/AH/DQMUU/**LCD_DATA17**/ AUDATA1
	LCD_DATA16	PGCR4	PG16MD[1:0] = B'10	PG16/WE2#/ICIORD#/DQMUL/**LCD_DATA16**/ AUDATA0
	LCD_DATA15	PGCR3	PG15MD[1:0] = B'10 (1)	PG15/D31/**LCD_DATA15**/PINT7
	LCD_DATA14	PGCR3	PG14MD[1:0] = B'10 (1)	PG14/D30/**LCD_DATA14**/PINT6
	LCD_DATA13	PGCR3	PG13MD[1:0] = B'10 (1)	PG13/D29/**LCD_DATA13**/PINT5
	LCD_DATA12	PGCR3	PG12MD[1:0] = B'10 (1)	PG12/D28/**LCD_DATA12**/PINT4
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'010 (1)	PG11/D27/**LCD_DATA11**/PINT3/TIOC3D
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'010 (1)	PG10/D26/**LCD_DATA10**/PINT2/TIOC3C
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'010 (1)	PG9/D25/**LCD_DATA9**/PINT1/TIOC3B
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'010 (1)	PG8/D24/**LCD_DATA8**/PINT0/TIOC3A
	LCD_DATA7	PGCR1	PG7MD[2:0] = B'010 (1)	PG7/D23/**LCD_DATA7**/IRQ7/TIOC2B
	LCD_DATA6	PGCR1	PG6MD[2:0] = B'010 (1)	PG6/D22/**LCD_DATA6**/IRQ6/TIOC2A
	LCD_DATA5	PGCR1	PG5MD[2:0] = B'010 (1)	PG5/D21/**LCD_DATA5**/IRQ5/TIOC1B
	LCD_DATA4	PGCR1	PG4MD[2:0] = B'010 (1)	PG4/D20/**LCD_DATA4**/IRQ4/TIOC1A
	LCD_DATA3	PGCR0	PG3MD[2:0] = B'010 (1)	PG3/D19/**LCD_DATA3**/IRQ3/TIOC0D
	LCD_DATA2	PGCR0	PG2MD[2:0] = B'010 (1)	PG2/D18/**LCD_DATA2**/IRQ2/TIOC0C
	LCD_DATA1	PGCR0	PG1MD[2:0] = B'010 (1)	PG1/D17/**LCD_DATA1**/IRQ1/TIOC0B
	LCD_DATA0	PGCR0	PG0MD[2:0] = B'010 (1)	PG0/D16/**LCD_DATA0**/IRQ0/TIOC0A

Notes: 1. These values must not be set in boot mode 1.
2. Bold text indicates the function used.

Table 2.2.24 SH7269 Multiplexed Pin Functions (PWM)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
PWM	PWM2H	PJCR3	PJ15MD[2:0] = B'100	PJ15/DV_DATA15/LCD_DATA15/PINT7/**PWM2H**/TxD7
	PWM2G	PJCR3	PJ14MD[2:0] = B'100	PJ14/DV_DATA14/LCD_DATA14/PINT6/**PWM2G**/TxD6
	PWM2F	PJCR3	PJ13MD[2:0] = B'100	PJ13/DV_DATA13/LCD_DATA13/PINT5/**PWM2F**/TxD5
	PWM2E	PJCR3	PJ12MD[2:0] = B'100	PJ12/DV_DATA12/LCD_DATA12/PINT4/**PWM2E**/SCK7
	PWM2D	PJCR2	PJ11MD[2:0] = B'100	PJ11/DV_DATA11/LCD_DATA11/PINT3/**PWM2D**/SCK6
	PWM2C	PJCR2	PJ10MD[2:0] = B'100	PJ10/DV_DATA10/LCD_DATA10/PINT2/**PWM2C**/SCK5
	PWM2B	PJCR2	PJ9MD[2:0] = B'100	PJ9/DV_DATA9/LCD_DATA9/PINT1/**PWM2B**/RTS5#
	PWM2A	PJCR2	PJ8MD[2:0] = B'100	PJ8/DV_DATA8/LCD_DATA8/PINT0/**PWM2A**/CTS5#

Note: Bold text indicates the function used.

Table 2.2.25 SH7269 Multiplexed Pin Functions (PORT)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
PORT	PJ16	PJCR4	PJ16MD[2:0] = B'000	**PJ16**/DV_DATA16/LCD_DATA16/RSPCK0/TIOC0A/ SIOFSCK
	PJ17	PJCR4	PJ17MD[2:0] = B'000	**PJ17**/DV_DATA17/LCD_DATA17/SSL00/TIOC0B/ SIOFSYNC
	PJ18	PJCR4	PJ18MD[2:0] = B'000	**PJ18**/DV_DATA18/LCD_DATA18/MOSI0/TIOC0C/ SIOFTxD
	PJ19	PJCR4	PJ19MD[2:0] = B'000	**PJ19**/DV_DATA19/LCD_DATA19/MISO0/TIOC0D/ SIOFRxD/AUDIO_XOUT

Note: Bold text indicates the function used.

2.3 Memory

The R0K572690C000BR includes the SH7269 internal RAM, external flash memories, an external SDRAM, and an external EEPROM.

2.3.1 SH7269 Internal RAM

The SH7269 includes 64-KB high-speed internal RAM that allows high-speed access to MCU, and 2.5 MB large-capacity internal RAM of which 128 KB is used for data retention.

2.3.2 NOR Flash Memory Interface

The R0K572690C000BR comes standard with an NOR flash memory listed in the table below to store the user program. The NOR flash memory works at 16-bit mode, and 3.3 V-only single power supply. The SH7269 address pins (A20 to A13) are multiplexed with Renesas Serial Peripheral Interface (RSPI) pins. Set JP4 and JP5 to connect these pins to NOR flash memory. Figure 2.3.1 shows the NOR flash memory block diagram. Table 2.3.2 lists the jumper setting (JP4). Table 2.3.3 lists the jumper setting (JP5).

Table 2.3.1 NOR Flash Memory Specifications

Part Number	Bus Size	Capacity	Access Time
S29GL256P90TFIR1	16-bit mode	32MB (16-bit × 16-Mword × 1)	90ns

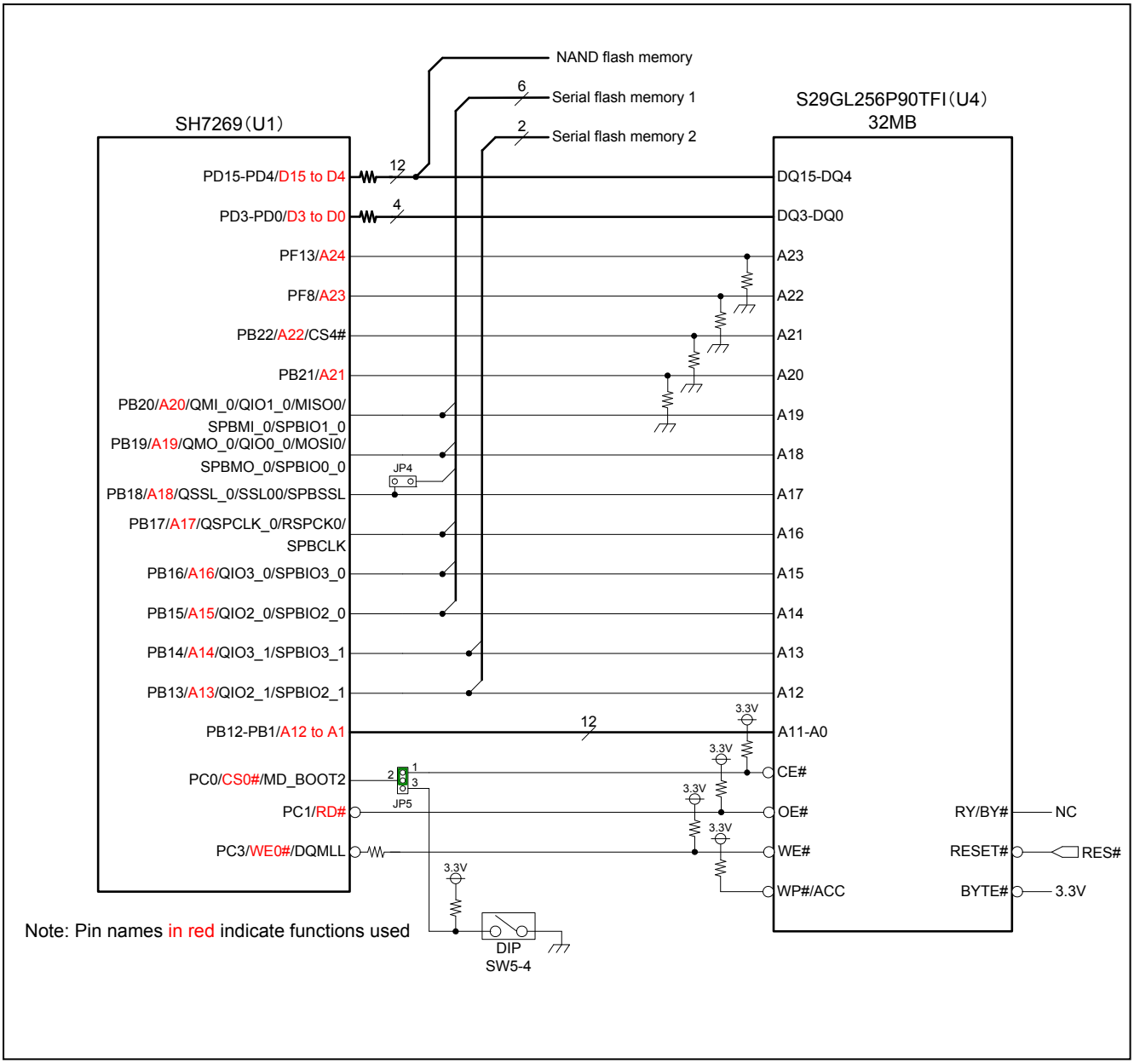

Figure 2.3.1 NOR Flash Memory Block Diagram

Table 2.3.2 Jumper Setting (JP4)

Number	1-2	None (Open)
JP4	Uses PB18 as QSSL_0/SSL00 output pin	Uses PB18 as A18 output pin (default)

Note: Shading indicates the function to be set.

Table 2.3.3 Jumper Setting (JP5)

Number	1-2	2-3
JP5	Uses PC0 as CS0# output pin (default)	Uses PC0 as MD_BOOT2 input pin

Note: Shading indicates the function to be set.

Figure 2.3.2 shows NOR flash memory write and read access timing example. Table 2.3.4 lists the Bus State Controller settings (write/read) when the SH7269 bus clock is at 66.67MHz.

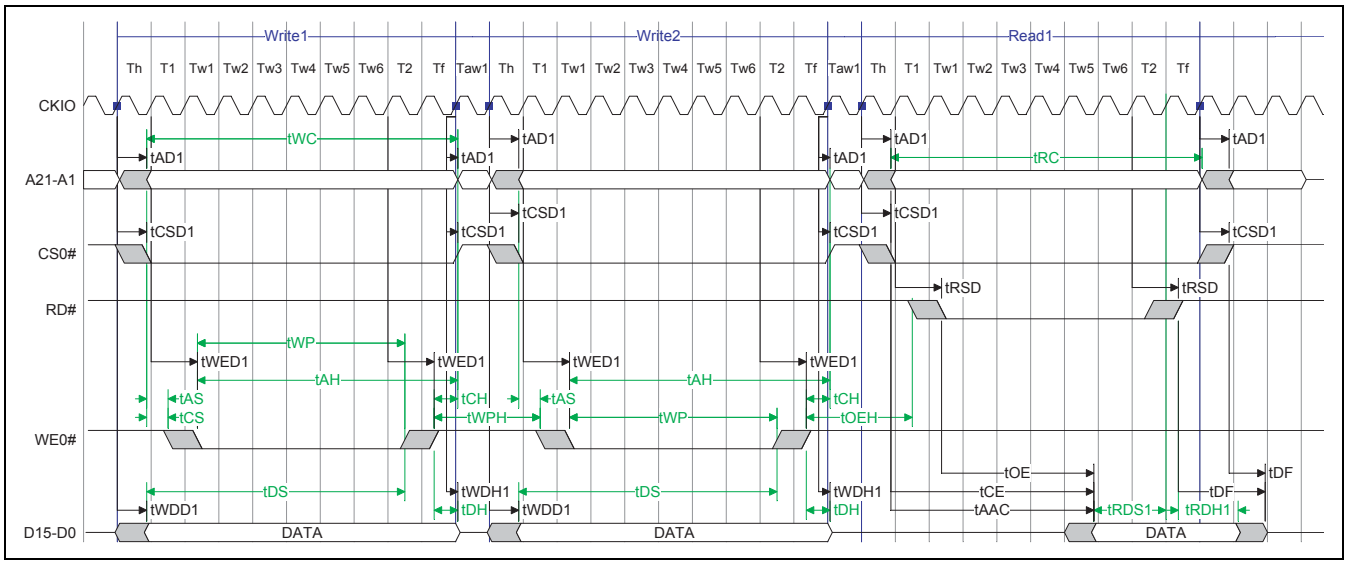

Figure 2.3.2 NOR Flash Memory Write/Read Access Timing Example

Table 2.3.4 Bus State Controller Settings (Write and Read NOR Flash Memory)

User Area	Target Device	Setting
CS0	S29GL256P90TFIR1	CS0 space bus control register (CS0BCR): Initial value: H'36DB 0400 (When the SH7269 is in boot mode 0) Recommended value: H'1000 0400 • Number of idles between Write-Read cycles and Write-Write cycles: IWW [2:0] = B'001; 1 idle cycle inserted • Number of idle cycles for another space Read-Write: IWRWD [2:0] = B'000; No idle cycles • Number of idles between Read-Write cycles in the same space: IWRWS [2:0] = B'000; No idle cycles • Data bus: BSZ [1:0] = B'10; 16-bit bus CS0 space wait control register (CS0WCR): Initial value: H'0000 0500 Recommended value: H'0000 0AC0 • Number of delay cycles from address, CS0# assertion to RD#, WEn# assertion: SW [1:0] = B'01; 1.5 cycles • Number of access wait cycles: WR [3:0] = B'0101; 5 cycles • External wait mask specification: WM = B'1; Ignore external wait input • Number of delay cycles from RD#, WEn# negation to address, CS0# negation: HW [1:0] = B'00; 0.5 cycles

2.3.3 SDRAM Interface

The R0K572690C000BRC000BR comes standard with an SDRAM listed in Table 2.3.5. The SDRAM is controlled by the SH7269 on-chip Bus State Controller (BSC). The R0K572690C000BR allows 16-bit bus access only.

Figure 2.3.3 shows the SDRAM block diagram. Table 2.3.6 lists the system setting DIP switches setting(SW6-1).

Table 2.3.5 SDRAM Specifications

Item	Description
Part Number	EDS1216AATA-75E
Configuration	16MB (16-bit bus) × 1
Capacity	16MB
Access Time	7.5ns
CAS Latency	2 (When the system clock is 66.67MHz)
Refresh	4096 cycles every 64ms
Row Address	A11 to A0
Column Address	A8 to A0
Number of Banks	4 (controlled by BA0 and BA1)

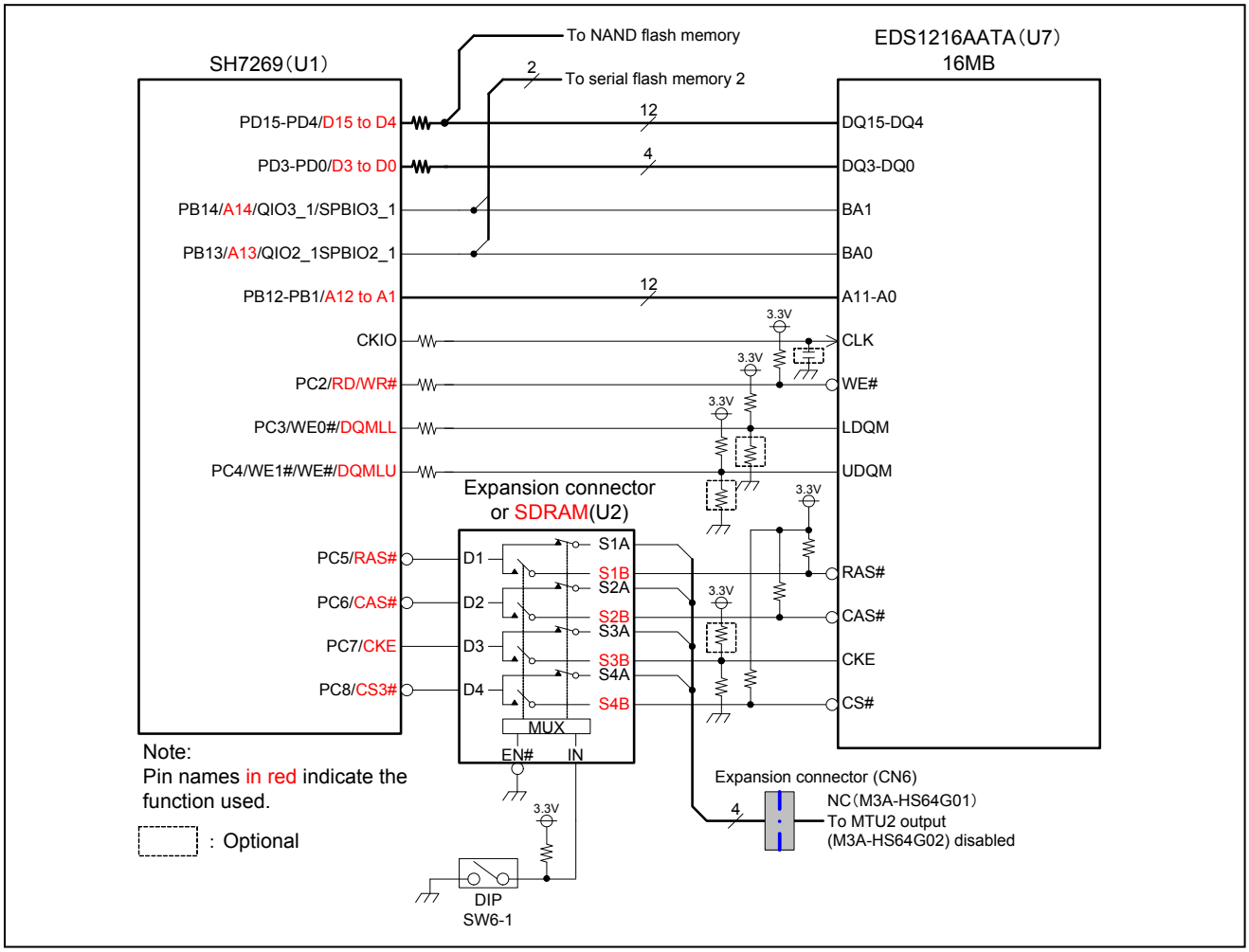

Figure 2.3.3 SDRAM Block Diagram

Table 2.3.6 DIP Switches Setting (SW6-1)

Number	Function	
	OFF (High)	ON (Low)
SW6-1	Connected to the SDRAM (default)	Connected to the expansion connector

Note: Shading indicates the function to be set.

Figure 2.3.4 shows the single read and write timing example of the SDRAM. Table 2.3.7 lists the Bus State Controller setting when the SH7269 bus clock is at 66.67MHz.

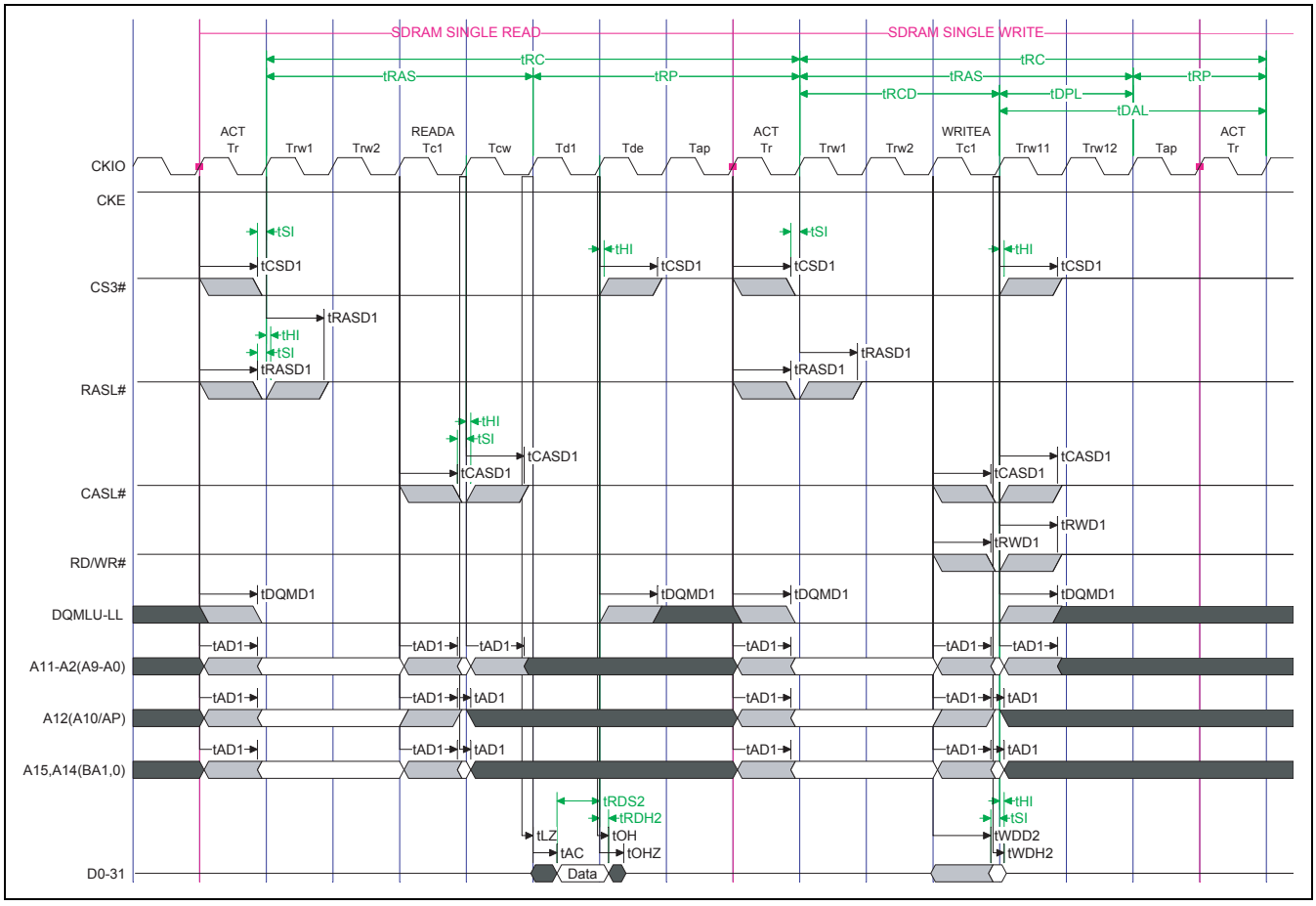

Figure 2.3.4 SDRAM Single Read and Write Timing Example

Table 2.3.7 Bus State Controller Setting (Read and Write SDRAM)

User Area	Target Device	Setting
CS3	EDS1216AATA-75E	CS3 space bus control register (CS3BCR): Initial value: H'36DB 0400, Recommended value: H'0000 4400 • Memory: TYPE [2:0] = B'100; SDRAM • Data bus: BSZ [1:0] = B'10; 16-bit bus CS3 space wait control register (CS3WCR): Initial value: H'0000 0500, Recommended value: H'0000 2492 • Number of auto-precharge completion wait cycles: WTRP [1:0] = B'01; 1 cycle • Number of wait cycles between ACTV command and READ (A)/WRIT(A) command: WTRCD [1:0] = B'01; 1 cycle • CAS latency for area 3 A3CL [1:0] = B'01; 2 cycles • Number of auto-precharge startup wait cycles: TRWL [1:0] = B'10; 2 cycles • Number of idle cycles from REF command/Self-refresh release to ACTV/REF/MRS command: WTRC [1:0] = B'10; 0.5 cycles SDRAM control register (SDCR): Initial value: H'0000 0000, Recommended value: H'0000 0809 • Refresh control RFSH = B'1; SDRAM is refreshed • Refresh control RMODE = B0; Auto-refreshed • Bank active mode BACTV = B'0; Auto-precharge mode • Number of bits of row address for area 3 A3ROW [1:0] = B'01; 12 bits • Number of bits of column address for area 3 A3COL [2:0] = B'01; 9 bits Refresh timer control/status register (RTCSR): Initial value: H'0000 0000, Recommended value: H'A55A 0010 • Clock select CKS [2:0] = B'010, Bφ/16 • Number of refresh RRC [2:0] = B'000; 1 Refresh time constant register (RTCOR): Initial value: H'0000 0000, Recommended value: H'A55A 0041 The refresh request interval when the clock select is set to Bφ/16 is as follows: 1 cycle: 240nsec (66.67MHz/16 = 4.167MHz) Refresh request interval in this SDRAM: 15.625 µsec/time 15.625µsec/240nsec = 65 (0×41) cycles/number of refresh

2.3.4 NAND Flash Memory Interface

The R0K572690C000BR is designed to allow the user to install an NAND flash memory listed in the table below. Refer to Table 1.6.1 for the component that can be installed. NAND flash memory works at 8-bit mode, and 3.3 V-only single power supply. The SH7269 NAND flash memory controller pins (FLCTL) are multiplexed with the data bus (D15 to D4) pins and SD Host Interface (SDHI) channel 0 pin. Set SW6-2 to OFF to connect these pins to NAND flash memory. Figure 2.3.5 shows the NAND flash memory block diagram. Table 2.3.9 lists the DIP switches setting (SW6-2).

Table 2.3.8 NAND Flash Memory Specifications

Part Number	Bus Size	Capacity	Access Time
K9F2G08U0B-PCB0	8-bit	256 MB (8-bit × 256-Mword × 1)	Random: 25 µs (max.) Page: 25 ns (max.)

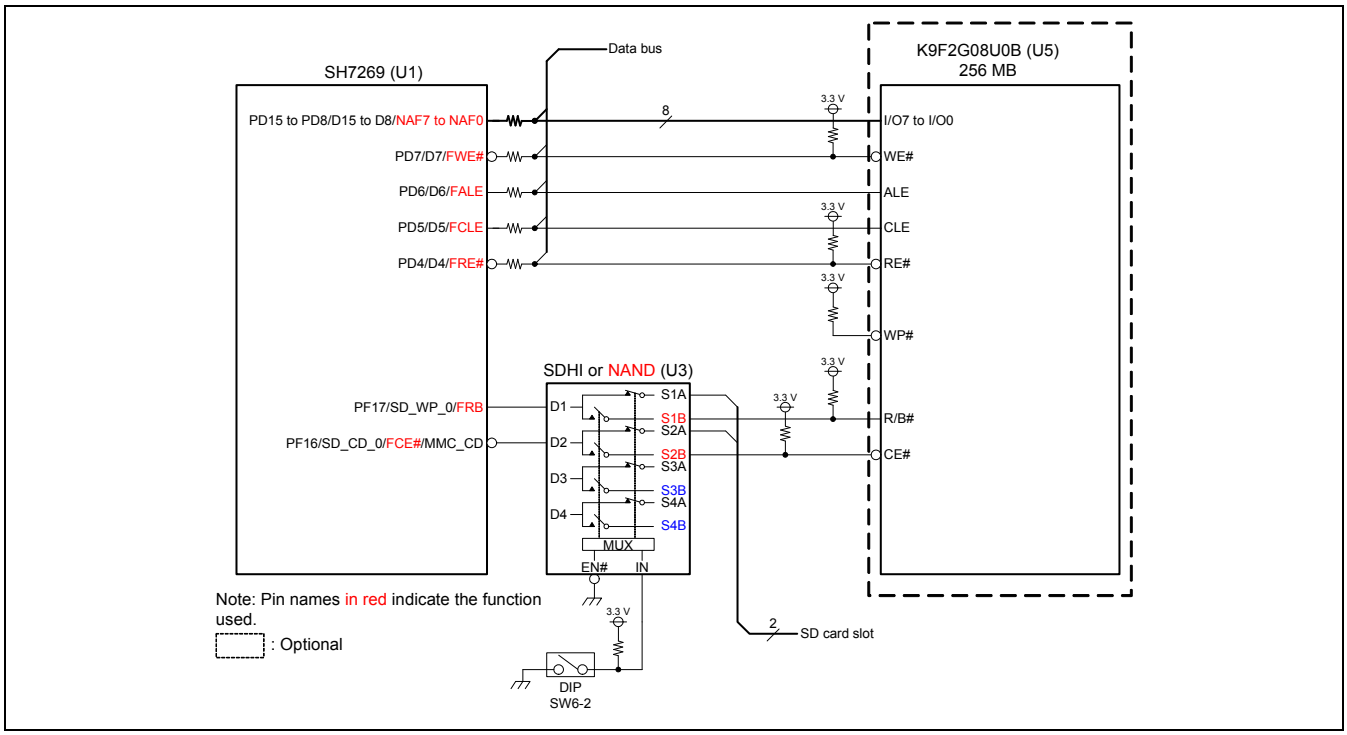

Figure 2.3.5 NAND Flash Memory Block Diagram

Table 2.3.9 DIP Switches Setting (SW6-2)

Number	Function	
	OFF (High)	ON (Low)
SW6-2	Connected to the NAND flash memory	Connected to the SD/MMC card slot (default)

Note: Shading indicates the function to be set.

2.3.5 Serial Flash Memory Interface

The R0K572690C000BR includes two serial flash memories listed in the table below. Serial flash memory is controlled by the SH7269 Renesas Serial Peripheral Interface (RSPI) or Renesas Quad Serial Peripheral Interface (RQSPI).

SH7269 SPI pins are multiplexed with address bus (A13 to A20) pins. Set JP4 to connect these pins to serial flash memory. O control two serial flash memories at one time using SPI multi I/O bus controller, JP6 and JP7 should be set. Figure 2.3.6 shows the serial flash memory block diagram. Table 2.3.11 lists the jumper JP4 setting. Table 2.3.12 describes about JP6 and JP7 settings.

Table 2.3.10 Serial Flash Memory Specifications

Part Number	Interface	Capacity	Package
S25FL032P0XMFI01	6-wire serial (QSPI)	4MB	8-pin SOP

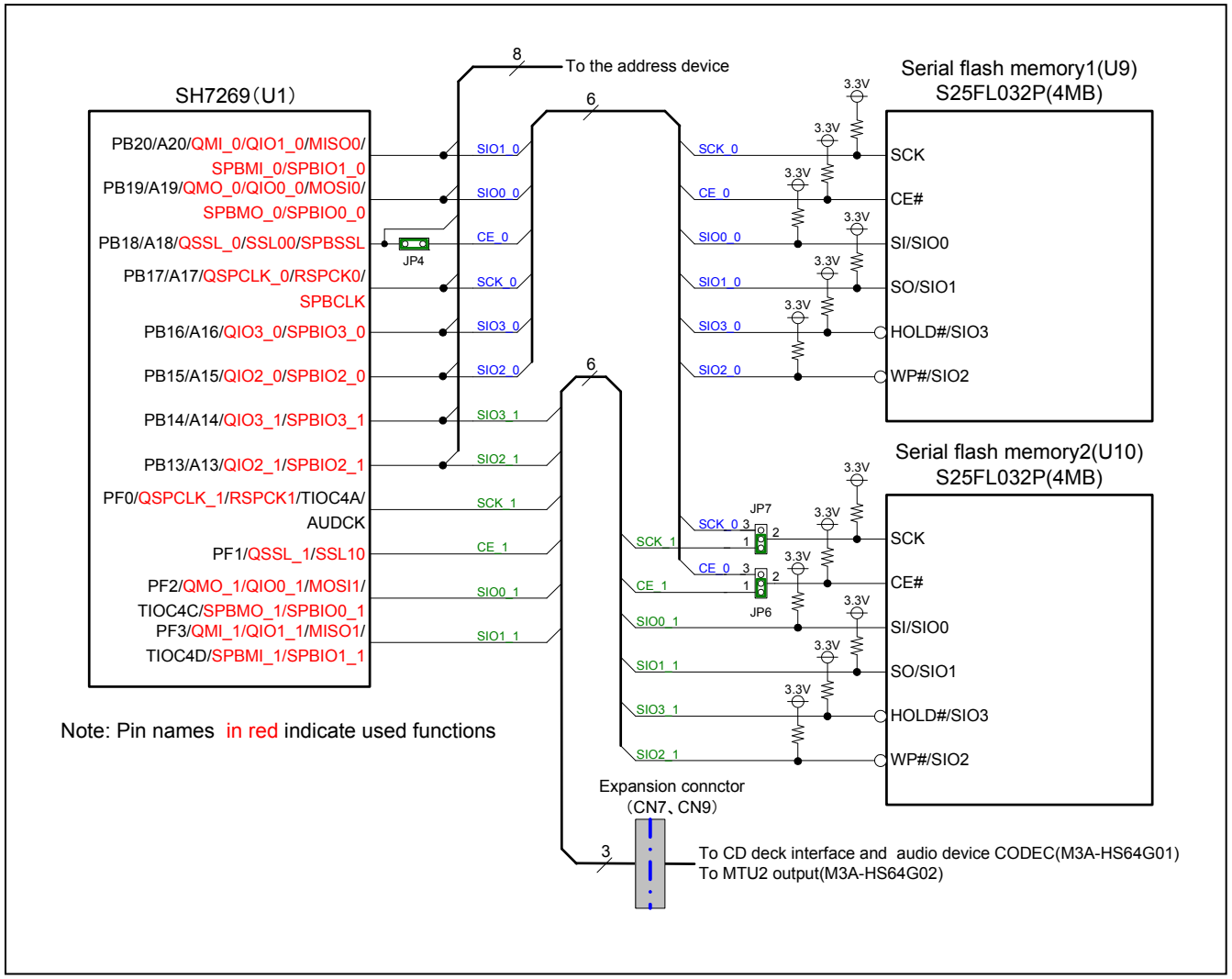

Figure 2.3.6 Serial Flash Memory Block Diagram

Table 2.3.11 Jumper Setting (JP4)

Number	1-2	None (Open)
JP4	Uses PB18 as QSSL_0/SSL00 output pin	Uses PB18 as A18 output pin (default)

Note: Shading indicates the function to be set.

Table 2.3.12 Jumper Setting (JP6, JP7)

Number	1-2	2-3
JP6	Uses PF1 as QSSL_1/SSL10 output pin (by default)	Uses PB18 as SPBSS output pin
JP7	Use PF0 as QSPCLK_1/RSPCK1 output pin (by default)	Use PB17 as SPBCLK output pin

Note: When controlling two serial flash memories at one time using SPIBSC, set as 2-3.

2.3.6 EEPROM Interface

The R0K572690C000BR comes standard with an EEPROM listed in the table below. The EEPROM is controlled by the SH7269 IIC bus interface 3 (IIC3).

Figure 2.3.7 shows the EEPROM interface block diagram.

Table 2.3.13 EEPROM Specifications

Part Number	Interface	Capacity	Package
R1EX24128ASAS0A	2-wire serial (IIC)	16KB (16-Kword × 8-bit)	8-pin SOP

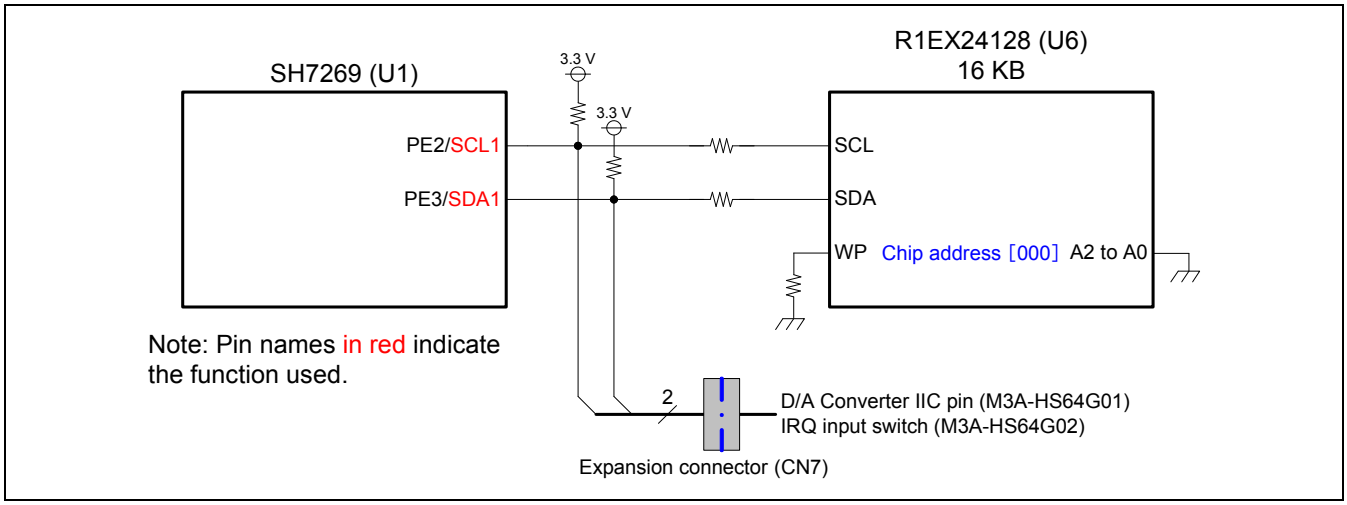

Figure 2.3.7 EEPROM Block Diagram

2.4 USB Interface

The R0K572690C000BR comes standard with a USB Series-A receptacle. Mini-B receptacle can be installed on the R0K572690C000BR to evaluate the USB host or function modules. Remove Series-A receptacle to install Mini-B receptacle. Figure 2.4.1 shows the USB interface block diagram. Table 2.4.1 lists the jumper setting (JP10).

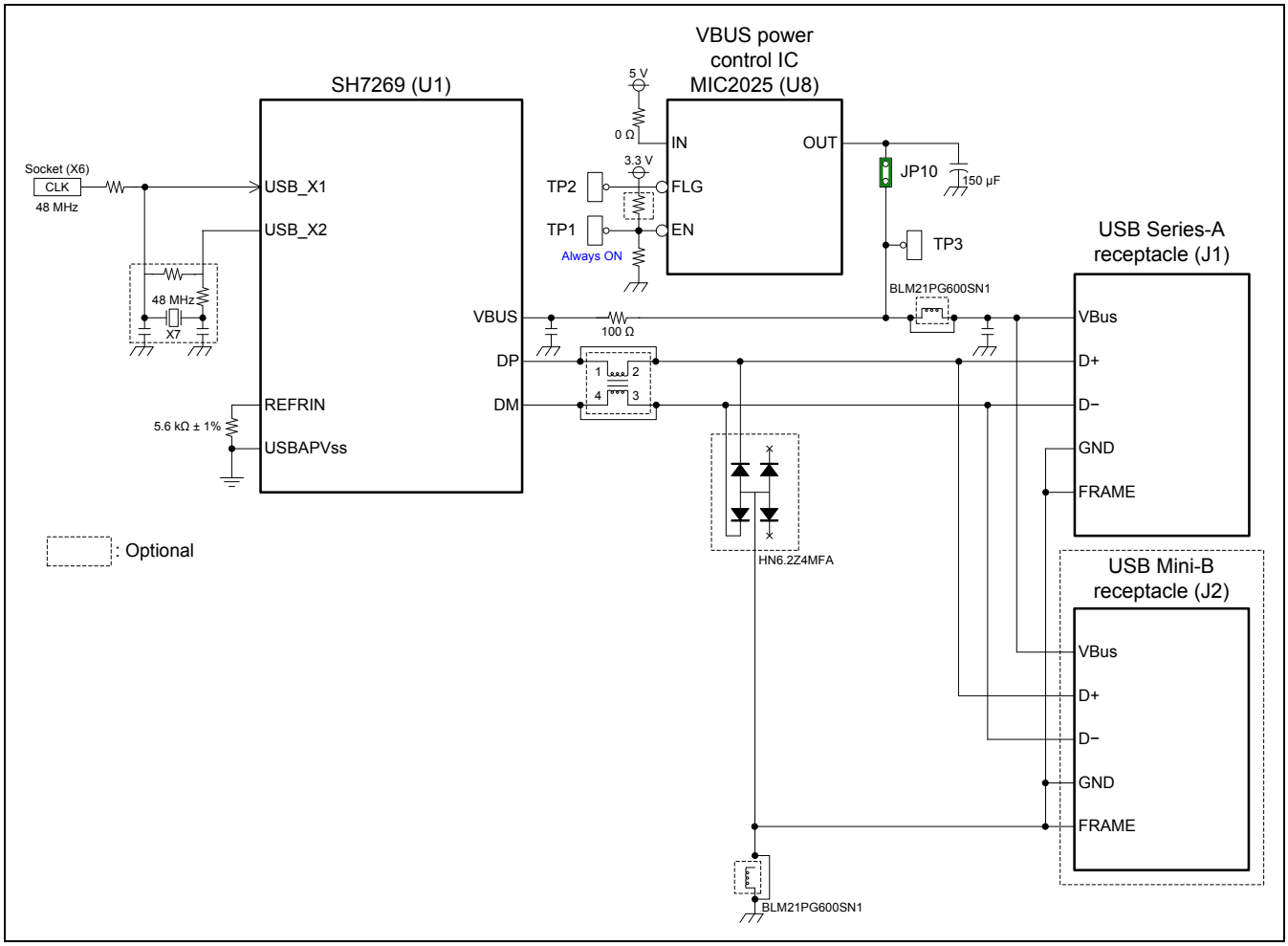

Figure 2.4.1 USB Interface Block Diagram

Table 2.4.1 Jumper Setting (JP10)

Number	1-2	None (Open)
JP10	USB host mode (VBUS power is supplied, default)	USB function mode (VBUS power is not supplied)

2.5 RS-232C Interface

The SH7269 includes the Serial Communication Interface with FIFO (SCIF). On the R0K572690C000BR, SH7269 SCIF channel 2 is connected to D-sub 9-pin connector via the RS-232C driver IC.

Figure 2.5.1 shows the RS-232C interface block diagram.

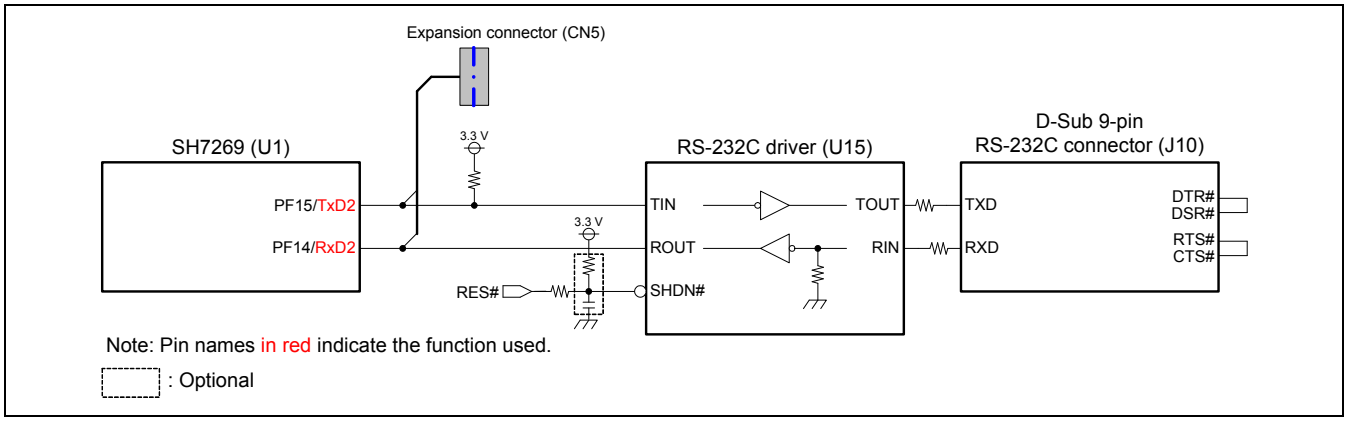

Figure 2.5.1 RS-232C Interface Block Diagram

2.6 I/O Ports

SH7269 I/O ports are connected to switches and LEDs on the R0K572690C000BR. Ports PH0 to PH7 can be used as analog input pins (AN0 to AN7). Figure 2.6.1 shows the I/O ports block diagram.

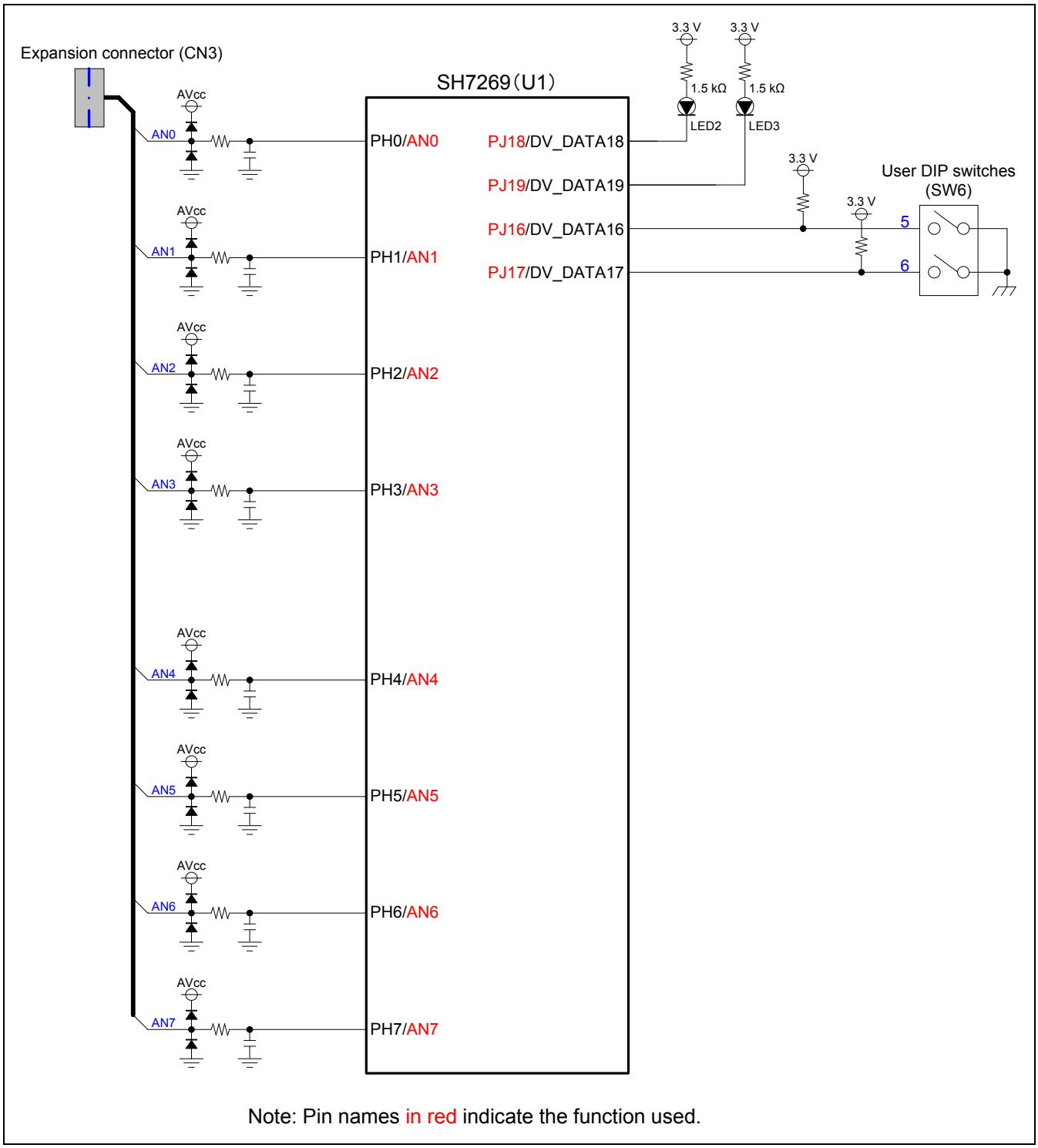

Figure 2.6.1 I/O Ports Block Diagram

2.7 Interrupt Switches

The R0K572690C000BR includes two push-button switches (NMI switch and IRQ1 switch) for the NRM and IRQ1 interrupt signals input from the SH7269, and a push-button switch (Test switch) for test signals. The Test switch is open to allow for connecting a desired pin. Set JP8 to use IRQ1 switch.

Figure 2.7.1 shows the interrupt switches block diagram. Table 2.7.1 lists the jumper setting (JP8).

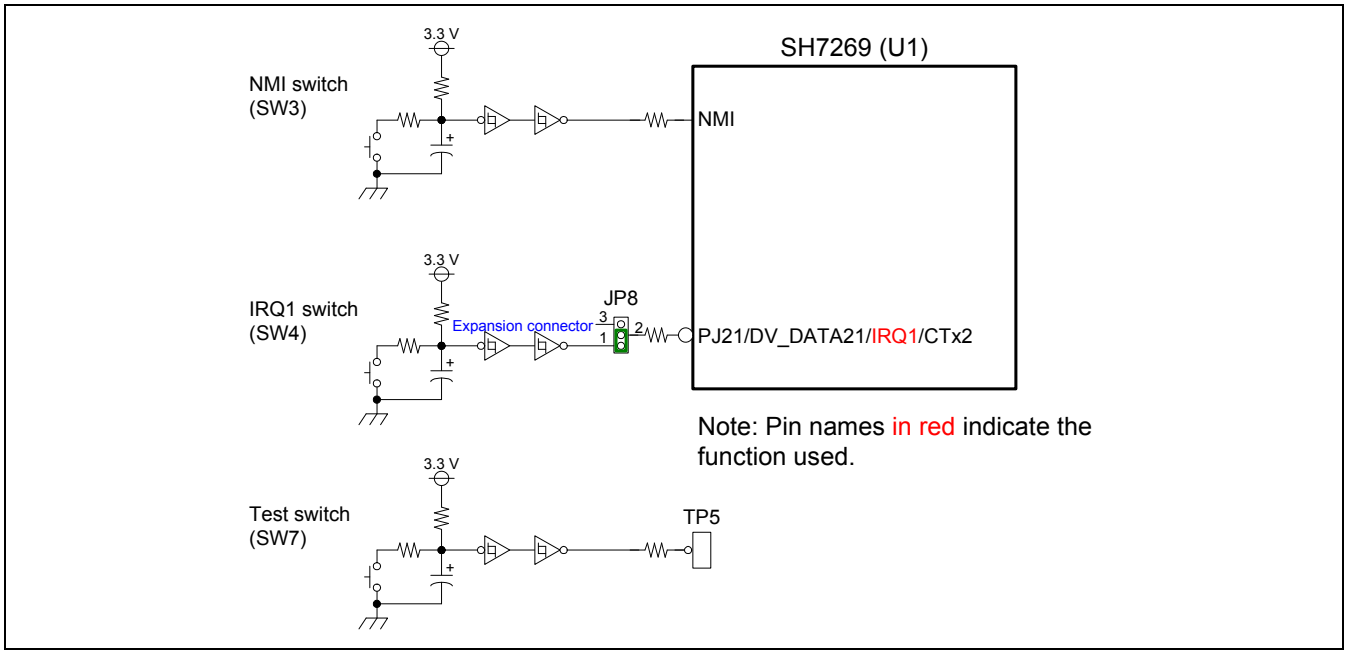

Figure 2.7.1 Interrupt Switches Block Diagram

Table 2.7.1 Jumper Setting (JP8)

Number	1-2	None (Open)
JP8	Uses PJ21 as IRQ1 input pin (default)	Uses PJ21 as CTx2 output/DV_DATA21 input pin

Note: Shading indicates the function to be set.

2.8 Clock Modules

Provide following clocks with the SH7269 on the R0K572690C000BR.

- SH7269 input clock (X4): 13.33MHz
- SH7269 RTC clock (X5): 32.768kHz
- SH7269 audio clock (X8): 11.2896MHz
- SH7269 USB clock (X6): 48.00MHz
- SH7269 LCD clock (X1): Optional
- SH7269 digital video decoder clock (X2): 27.00MHz

Figure 2.8.1 shows the clock module block diagram.

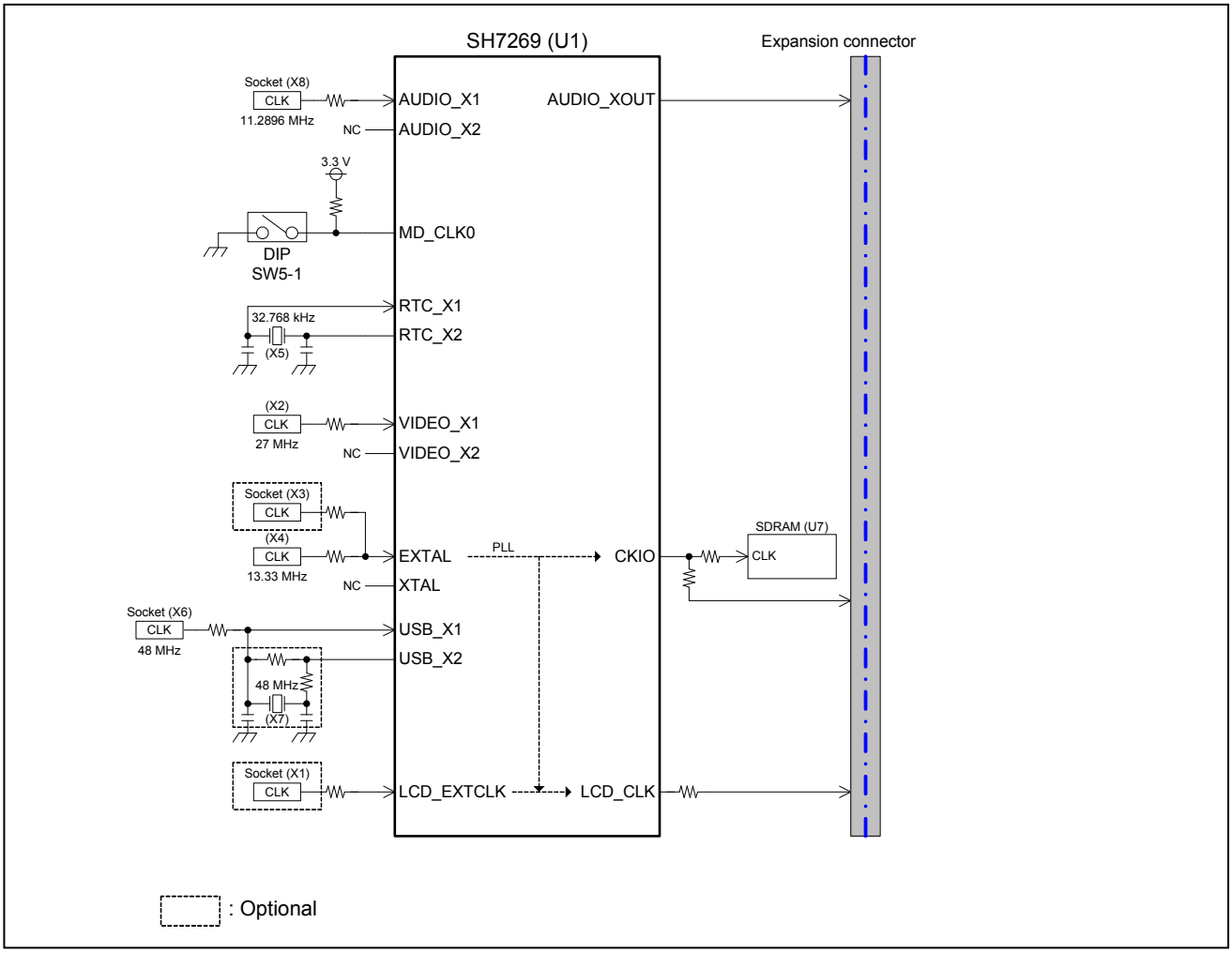

Figure 2.8.1 Clock Module Block Diagram

2.9 Reset Module

A reset IC controls reset signals connected to the SH7269, flash memory and peripheral I/Os on the R0K572690C000BR. There are two system reset options; power-on reset and reset by switch.

Figure 2.9.1 shows the reset module block diagram.

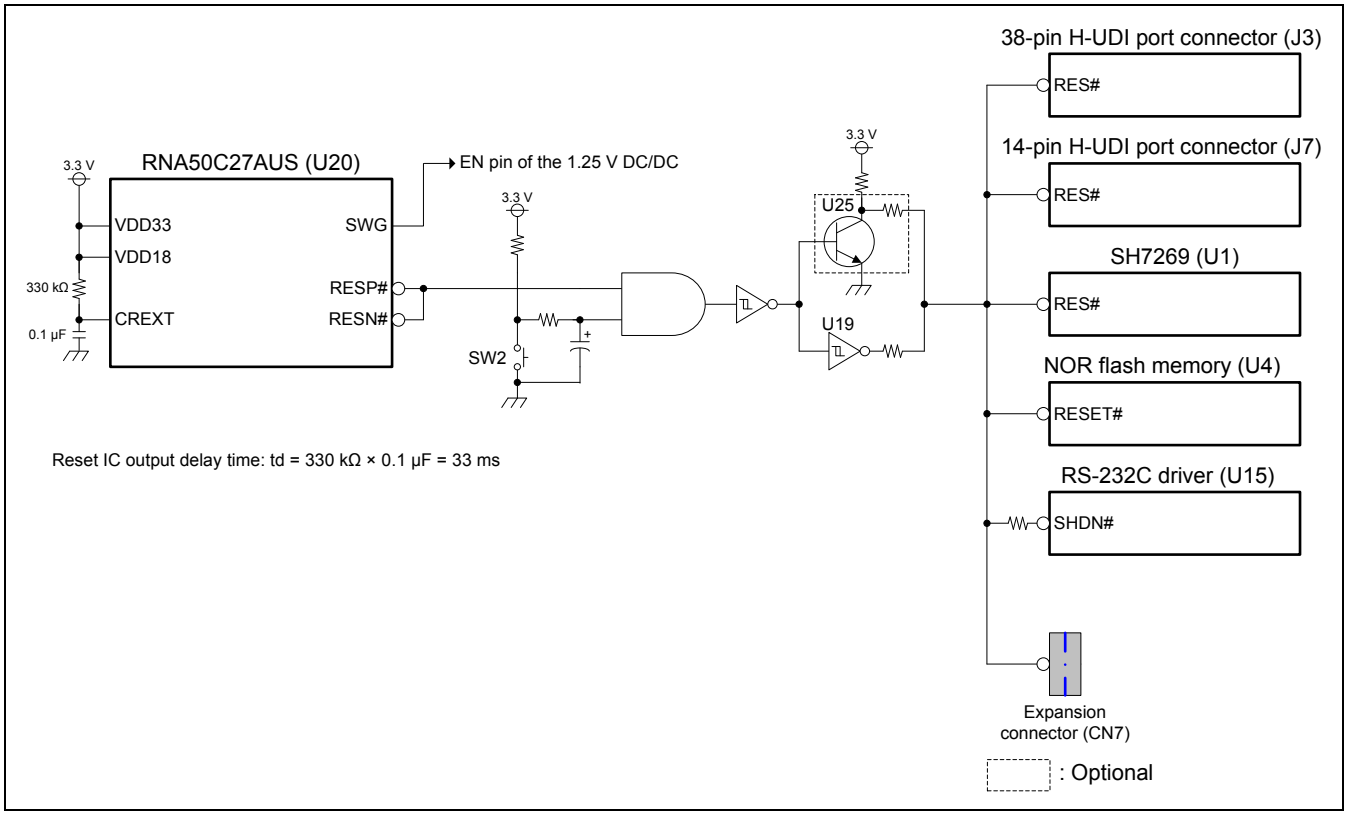

Figure 2.9.1 Reset Module Block Diagram

2.10 Power Supply Module

A 5 V power supply is input to the R0K572690C000BR, and the regulator on the R0K572690C000BR generates 3.3 V voltage, the reference voltage for the A/D Converter (3.3 V), and 1.25 V. CPU 3.3 V and 1.25 V power can be externally-supplied. Figure 2.10.1 shows the power supply module block diagram.

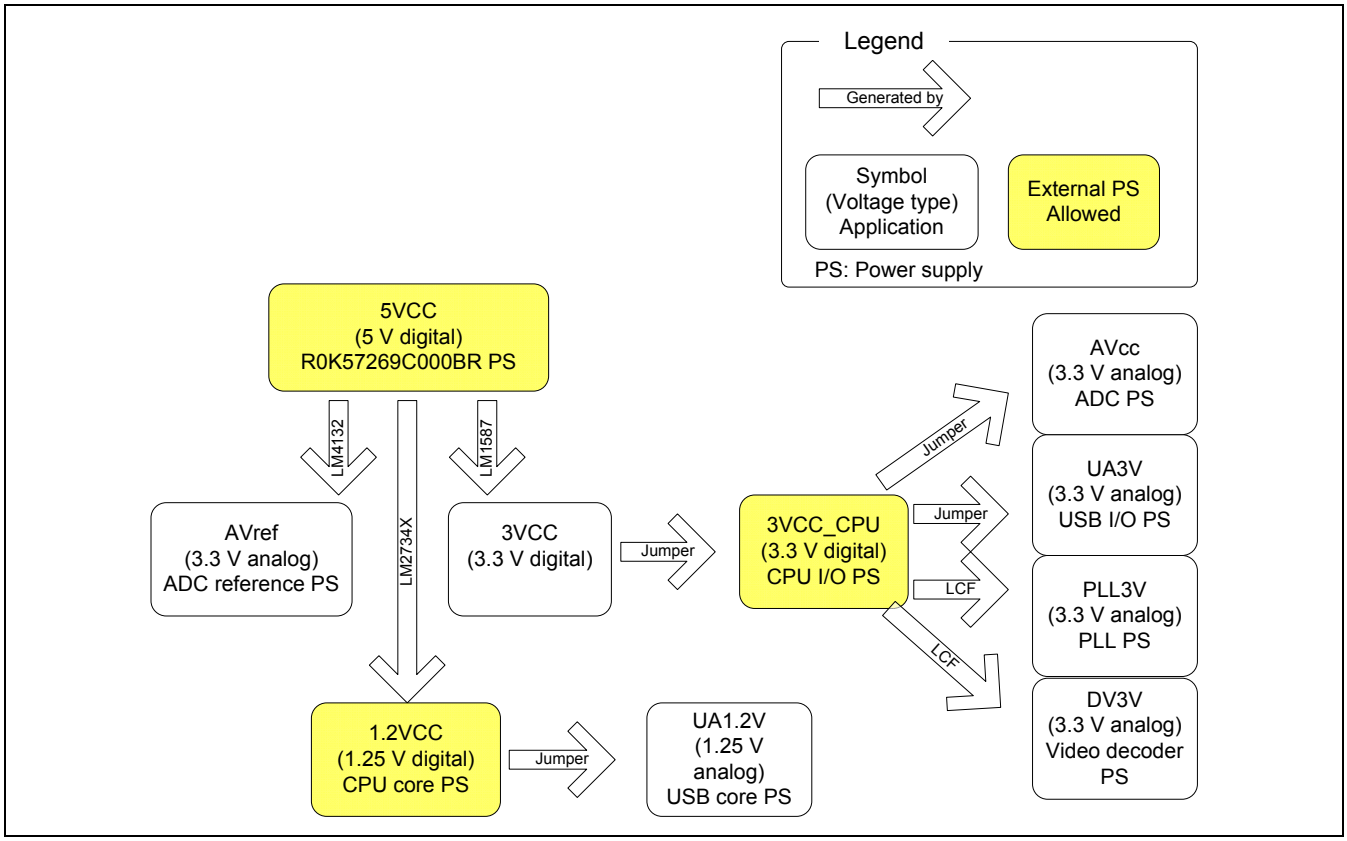

Figure 2.10.1 Power Supply Module

2.11 H-UDI

The R0K572690C000BR includes two H-UDI port connectors (14-pin and 38-pin) to connect to the E10A-USB emulator. AUD pins are multiplexed with the Renesas Serial Peripheral Interface (RSPI) pins, Serial Sound Interface with FIFO (SSIF) pins, and VDC4 (Video Display Controller 4) pins. AUD function can be used when the R0K572690C000BR is used alone (Do not use the AUD function when connecting optional boards). Note that serial flash memory 2 cannot be used when using the AUD function.

Figure 2.11.1 shows H-UDI block diagram.

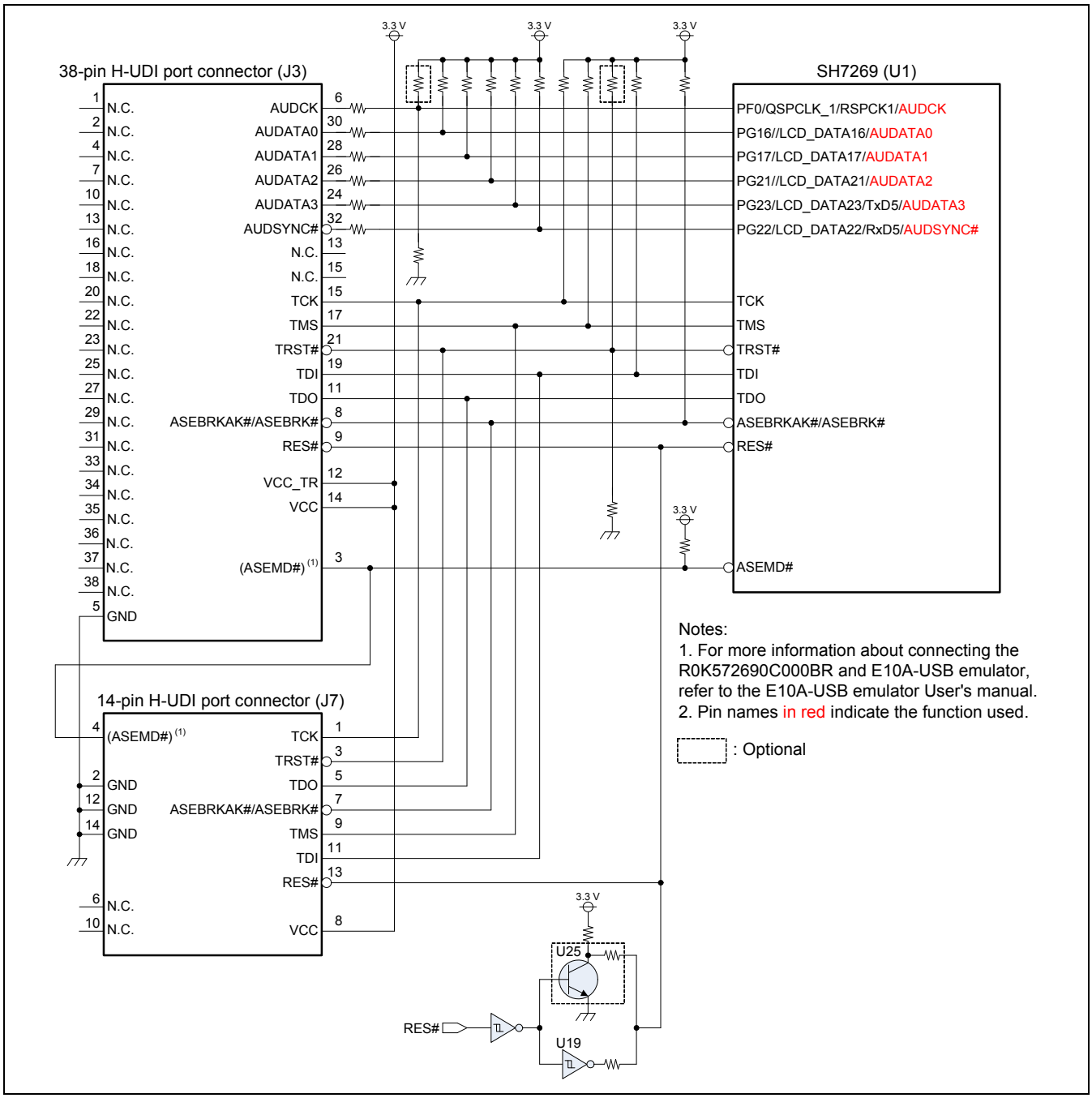

Figure 2.11.1 H-UDI Block Diagram

2.12 SD/MMC Card Interface

The R0K572690C000BR includes an SD/MMC card slot. The SD/MMC card slot is connected to the SH7269 SD Host Interface (SDHI) and the MMC Host Interface (MMC). SDHI channel 0 pin and MMC host interface (MMC) pin are multiplexed with the NAND flash memory controller (FLCTL) pins.

Figure 2.12.1 shows the SD/MMC card interface block diagram. Table 2.12.1 lists the DIP switches setting (SW6-2).

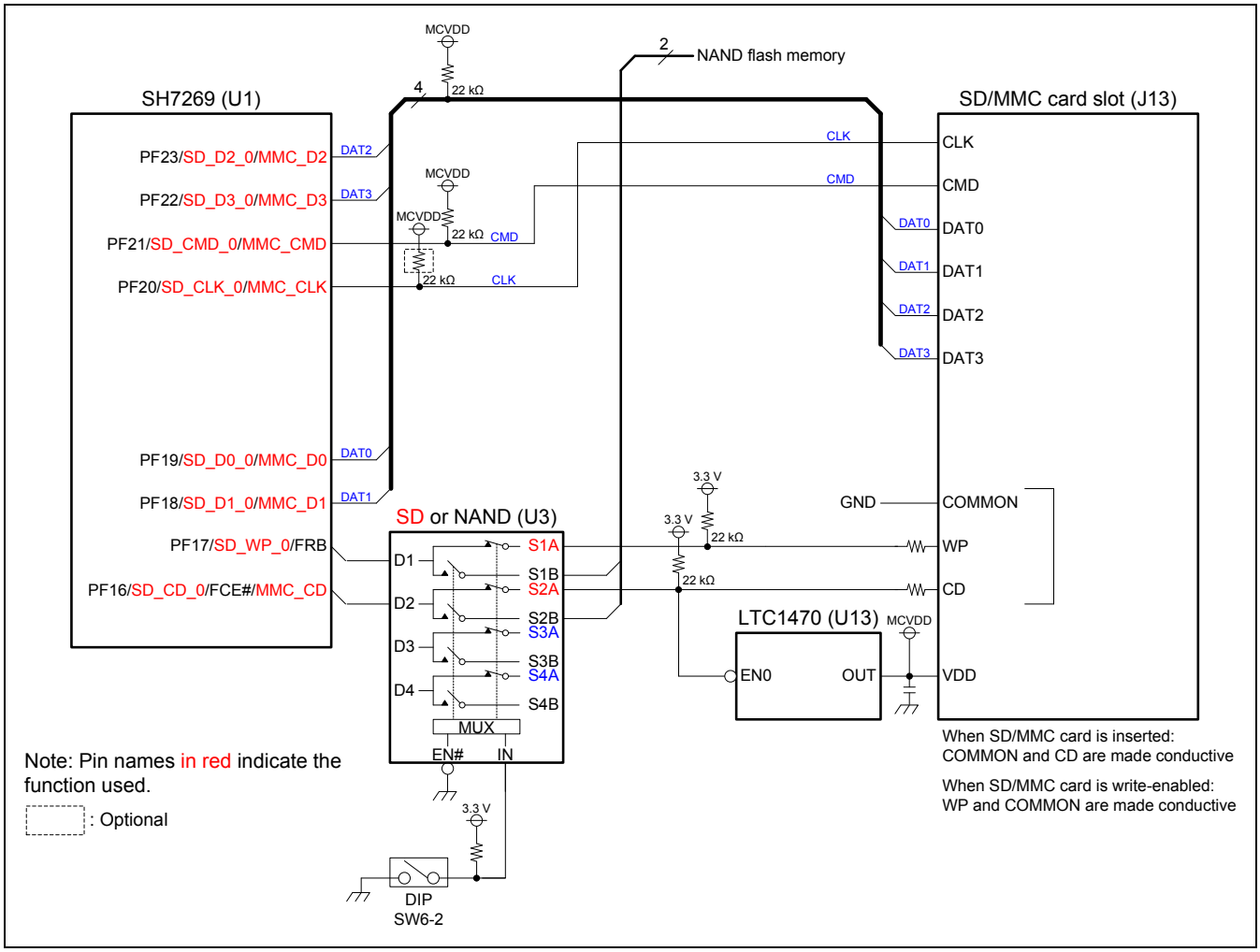

Figure 2.12.1 SD/MMC Card Interface Block Diagram

Table 2.12.1 DIP Switch Setting (SW6-2)

Number	Function	
	OFF (High)	ON (Low)
SW6-2	Connected to the NAND flash memory	Connected to the SD/MMC card slot (default)

Note: Shading indicates the function to be set.

2.13 VDC4 Interface

The SH7269 Video Display Controller 4 (VDC4) includes the features to output signals to control the LCD module and to input digital video (digital video IN). The R0K572690C000BR includes a 40-pin half pitch connector to connect the LCD module and digital video IN.

LCD module VDC4 pins are multiplexed with Serial Communication Interface (SCIF) channel 5 pins. When specifying LCD_DATA22 and LCD_DATA23, the UART connector on the optional board cannot be used.

Digital video IN VDC4 pins are multiplexed with Motor Control PWM Timer (PWM) channel 1 pins and Control Area Network (RCAN) channel 2 pins.

Figure 2.13.1 shows the LCD module interface block diagram. Figure 2.13.2 shows the digital video IN interface block diagram. Table 2.13.1 lists the jumper settings (JP8 ad JP9).

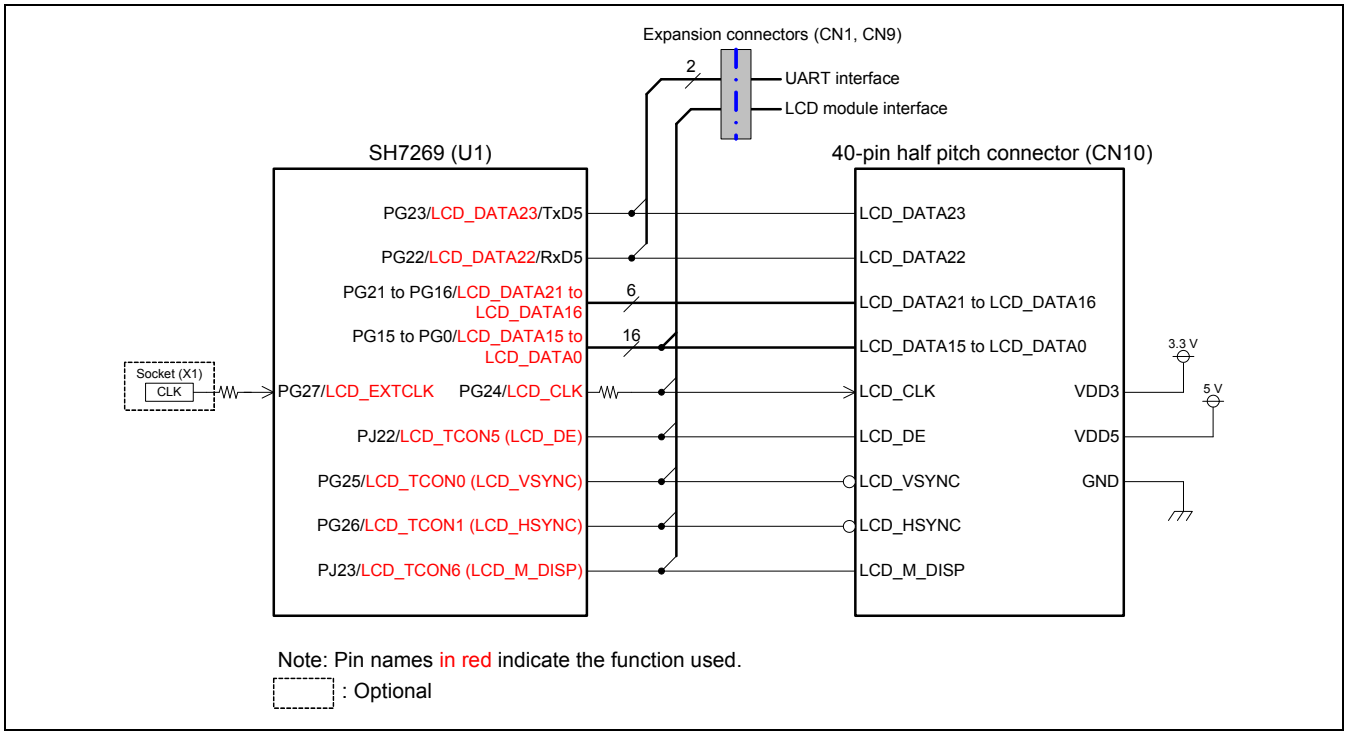

Figure 2.13.1 LCD Module Interface Block Diagram

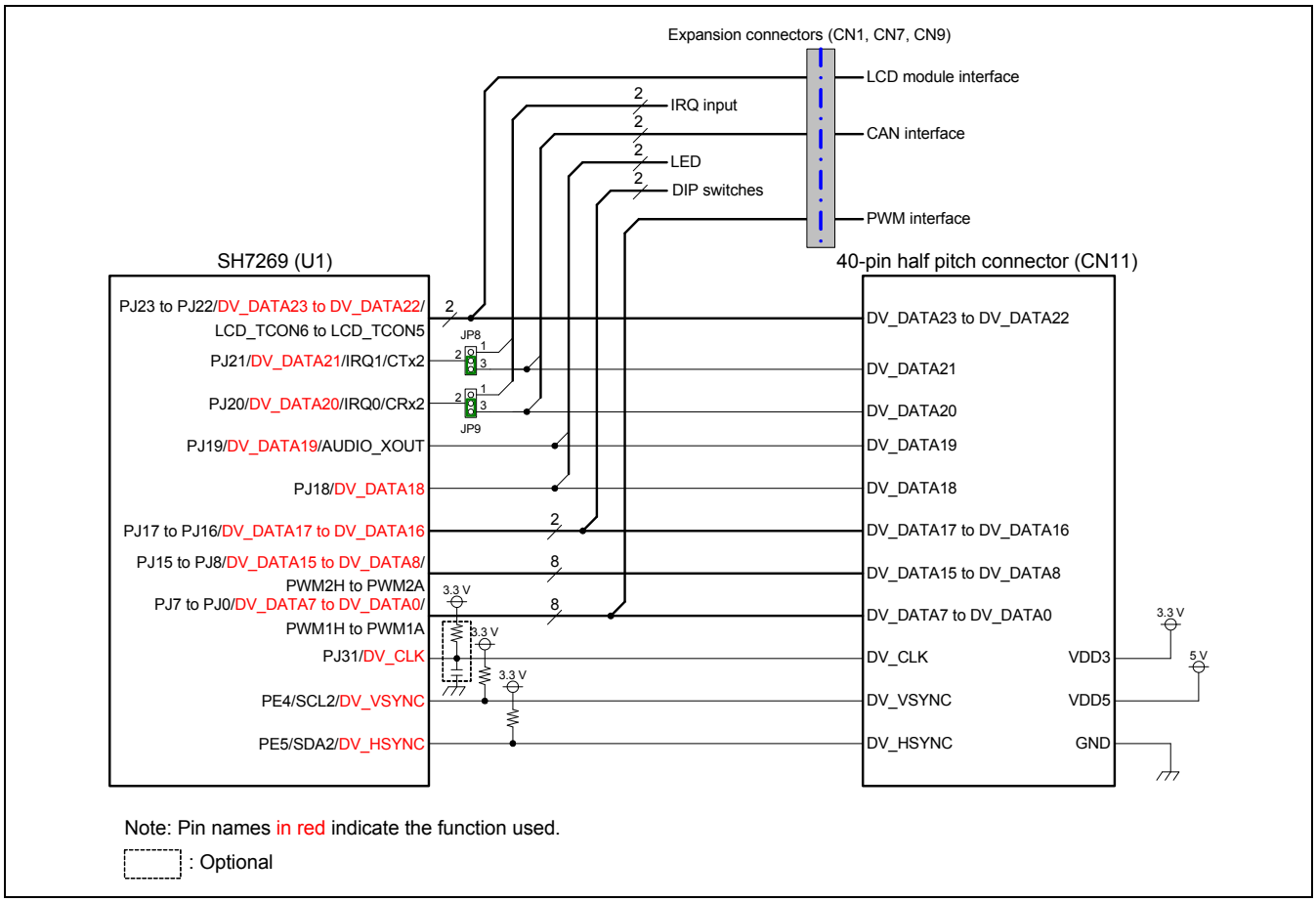

Figure 2.13.2 Digital Video-IN Interface Block Diagram

Table 2.13.1 Jumper Settings (JP8, JP9)

Number	1-2	None (Open)
JP8	Uses PJ21 as IRQ1 input pin (default)	Uses PJ21 as CTx2 output/DV_DATA21 input pin
JP9	Uses PJ20 as IRQ0 input pin (default)	Uses PJ20 as CRx2 input/DV_DATA20 input pin

Note: Shading indicates the function to be set.

2.14 Video-IN Interface

The SH7269 includes the digital video decoder, which allows the user to input the composite video (CVBS) signal directly. The R0K572690C000BR includes an RCA connector to input the CVBS signal.

Figure 2.14.1 shows the video IN interface block diagram.

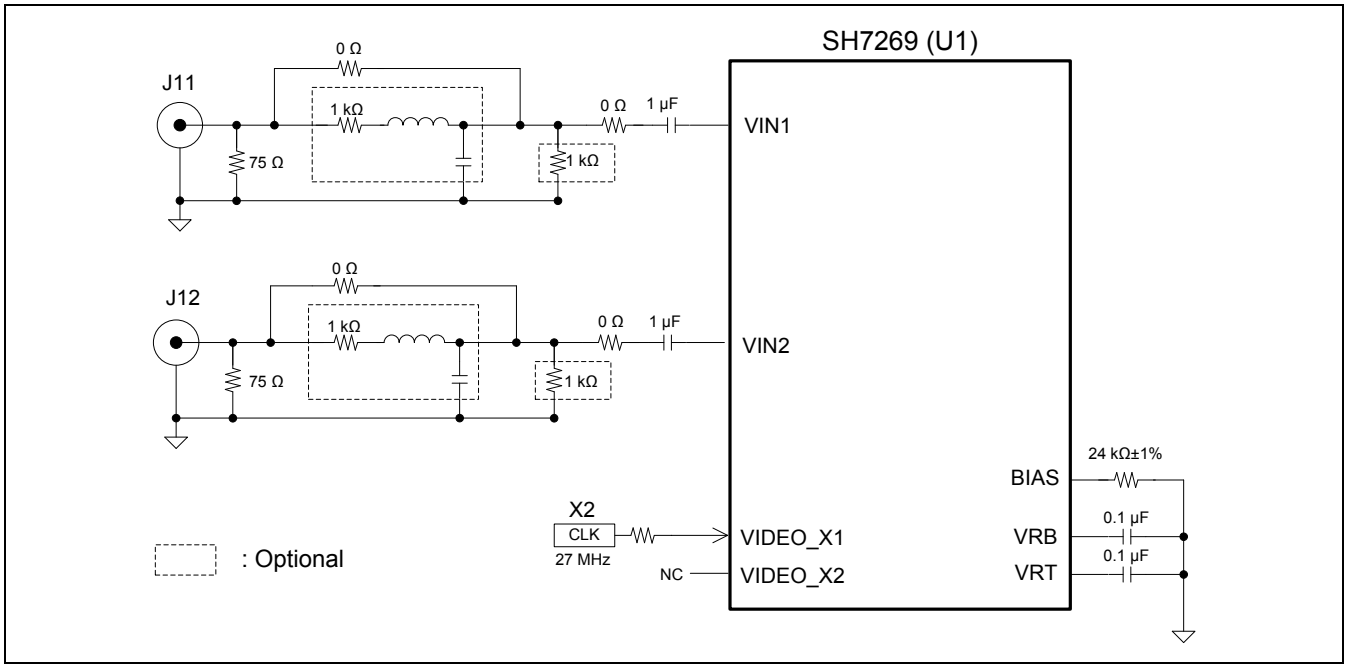

Figure 2.14.1 Video-IN Interface Block Diagram

2.15 PWM Interface

The SH7269 includes two channels of Motor Control Pulse Width Modulator (PWM) Timer with a maximum of eight pulse outputs per channel. On the R0K572690C000BR, SH7269 PWM channel 2 pins are connected to the 40-pin half pitch connector at TTL level. 40-pin half pitch connector is multiplexed with the digital video IN interface connector. PWM output pins are multiplexed with Video Display Controller 4 (VDC4) pins.

Figure 2.15.1 shows the PWM interface block diagram.

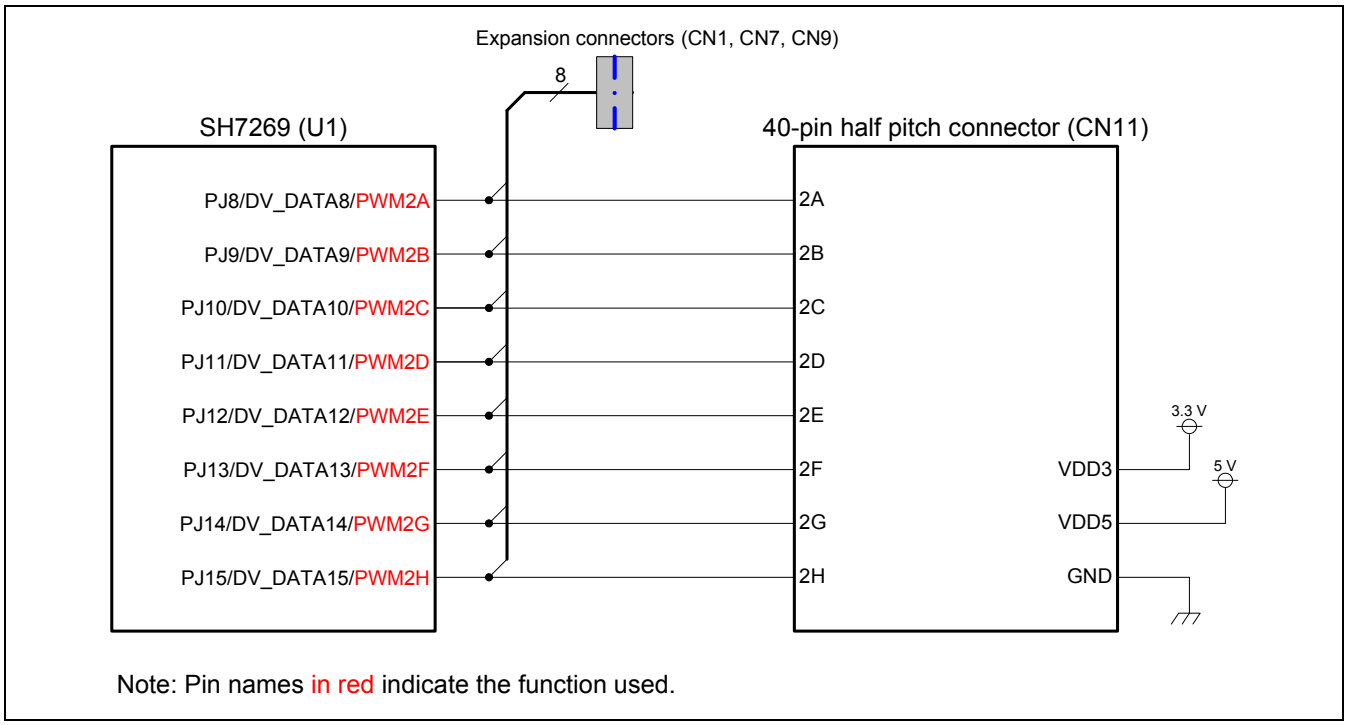

Figure 2.15.1 PWM Interface Block Diagram

3. M3A-HS64G01 Functions

3.1 Overview of Functions

The M3A-HS64G01 includes the function modules listed in the following table.

Table 3.1.1 M3A-HS64G01 Function Modules

Section	Function	Description
3.2	CPU	SH7269
3.3	LCD Module Interface	• LCD module interface — Connects the SH7269 Video Display Controller 4 (VDC4) and LCD module connectors — Includes flexible connectors for LCD module • Character LCD module with LED backlight
3.4	Audio Modules	• Connects the SH7269, D/A Converters and an audio codec — 96kHz 24-bit D/A Converters: 2 — 24-bit stereo codec with microphone AMP: 1
3.5	CD Deck Interface	• Connects the SH7269 Renesas Serial Peripheral Interface (RSPI), Serial Sound Interface (SSIF) and a CD deck
3.6	SD Card Interface	• Connects the SH7269 SD Host Interface (SDHI) and an SD card slot
3.7	UART Interface	• Connects the SH7269 Serial Communication Interface with FIFO (SCIF) and a UART connector
3.8	CAN Interface	• Connects the SH7269 Controller Area Network (RCAN-TL1) and a CAN connector Note: One CAN channel can be used on the R0K572690C000BR.
3.9	IEBus™ Interface	• Connects the SH7269 IEBus™ controller (IEB) and IEBus™ connector
3.10	I/O Ports	• Connect the SH7269 I/O ports, LEDs and DIP switches
3.11	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
3.12	Reset Module	• Resets devices on the M3A-HS64G01
3.13	Power Supply Module	• Controls the M3A-HS64G01 system power supply
–	Operating Specifications	• Connectors, switches and LEDs Refer to Chapter 6 for details.

3.2 CPU

3.2.1 SH7269 Overview

The R0K572690C000BR includes the SH7269, the 32-bit RISC MCU that operates with a maximum frequency of 266.67MHz.

3.2.2 SH7269 Pin Functions Used on the M3A-HS64G01

Table 3.2.1 to Table 3.2.11 list the SH7269 pin functions used on the M3A-HS64G01.

Table 3.2.1 SH7269 Pin Functions (1/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
1	PC1/RD#	RD#	Connected to NOR flash memory OE# pin	CN6, pin 6	
2	PVcc				
3	PC2/RD/WR#/SCK6	RD/WR#	Connected to SDRAM WE# pin	CN6, pin 7	
4	PC3/WE0#/DQMLL/RxD6	WE0#	Connected to NOR flash memory WE# pin	CN6, pin 8	
		DQMLL	Connected to SDRAM DQML pin		
5	PC4/WE1#/WE#/DQMLU/TxD6	DQMLU	Connected to SDRAM DQMU pin	CN6, pin 9	
6	PC5/RAS#/CRx0 / CRx0/CRx1/CRx2/IRQ0	RAS#	Connected to SDRAM RAS# pin	–	SW6-1: OFF
		–	NC	CN6, pin 14	SW6-1: ON
7	PVcc				
8	PC6/CAS#/SCK7/CTx0/ CTx0&CTx1&CTx2	CAS#	Connected to SDRAM CAS# pin	–	SW6-1: OFF
		–	NC	CN6, pin 15	SW6-1: ON
9	Vss				
10	PC7/CKE/RxD7/CRx1/ CRx0/CRx1/IRQ1	CKE	Connected to SDRAM CKE pin	–	SW6-1: OFF
		–	NC	CN6, pin 16	SW6-1: ON
11	Vcc				
12	PC8/CS3#/TxD7/CTx1/ CTx0&CTx1	CS3#	Connected to SDRAM CS# pin	–	SW6-1: OFF
		–	N.C.	CN6, pin 17	SW6-1: ON
13	PB1/A1/TIOC0A	A1	Address bus	CN4, pin 28	
14	PB2/A2/TIOC0B	A2	Address bus	CN4, pin 27	
15	PB3/A3/TIOC0C	A3	Address bus	CN4, pin 26	
16	PJ14/DV_DATA14 / LCD_DATA14/PINT6/ PWM2G/TxD6	PWM2G	PWM output	CN11, pin A1	TTL level
		DV_DATA14	DV input		
		PJ14	Connected to CD deck FLAG6 pin	CN1, pin 4	
17	PVcc				
18	PJ15/DV_DATA15/ LCD_DATA15/PINT7/ PWM2H/TxD7	PWM2H	PWM output	CN11, pin B1	TTL level
		DV_DATA15	DV input		
		PJ15	Connected to CD deck TRANS pin	CN1, pin 2	
19	Vss				
20	PB4/A4/TIOC0D	A4	Address bus	CN4, pin 25	
21	Vcc				
22	PJ16/DV_DATA16/ LCD_DATA16/RSPCK0/ TIOC0A/SIOFSCK	PJ16	Connected to SW6-5 as user input port 1	CN11, pin B13	
		DV_DATA16	DV input		
23	PJ17/DV_DATA17/ LCD_DATA17/SSL/00/ TIOC0B/SIOFSYNC	PJ17	Connected to SW6-6 as user input port 2	CN11, pin B12	
		DV_DATA17	DV input		
24	PJ18/DV_DATA18/ LCD_DATA18/MOSI0/ TIOC0C/SIOFTxD	PJ18	Connected to LED2 as user output port 1	CN11, pin B8	
		DV_DATA18	DV input		

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.2 SH7269 Pin Functions (2/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
25	PB5/A5/TIOC1A	A5	Address bus	CN4, pin 22	
26	PB6/A6/TIOC1B	A6	Address bus	CN4, pin 21	
27	PVcc				
28	PB7/A7/TIOC2A	A7	Address bus	CN4, pin 20	
29	Vss				
30	PB8/A8/TIOC2B	A8	Address bus	CN4, pin 19	
31	Vcc				
32	PB9/A9/TIOC3A	A9	Address bus	CN4, pin 18	
33	PB10/A10/TIOC3B	A10	Address bus	CN4, pin 17	
34	PB11/A11/TIOC3C	A11	Address bus	CN4, pin 14	
35	PB12/A12/TIOC3D	A12	Address bus	CN4, pin 13	
36	PJ19/DV_DATA19/ LCD_DATA19/MISO0/ TIOC0D/SIOFRxD/ AUDIO_XOUT	PJ19	Connected to LED3 as user output port 2	CN11, pin A12	
		DV_DATA19	DV input		
		AUDIO_XOUT	Connected to DAC (U11, U12) MCKI pins	CN7, pin 40	
37	PVcc				
38	PJ20/DV_DATA20/ LCD_DATA20/LCD_TCON3/ IRQ0/CRx2/CRx0/CRx1/CRx2	IRQ0	Connected to CD deck BLKCK pin	CN7, pin 8	JP9: 1-2
		DV_DATA20	DV input	CN11, pin B4	JP9: 2-3
		CRx2	Connected to the CAN driver IC (U16)	CN1, pin 17	
39	Vss				
40	PB13/A13/QIO2_1/ SPBIO2_1	A13	Address bus	CN4, pin 12	
		QIO2_1 SPBIO2_1	Connected to serial flash memory 2 IO2 pin		
41	Vcc				
42	PJ21/DV_DATA21 LCD_DATA21/LCD_TCON4/ IRQ1/CTx2/CTx0&CTx1&CTx2	IRQ1	IRQ1 switch	–	JP8: 1-2
		DV_DATA21	DV input	CN11, pin A14	JP8: 2-3
		CTx2	Connected to the CAN driver IC (U16)	CN1, pin 18	
43	PJ22/DV_DATA22/ LCD_DATA22/LCD_TCON5/ IRQ2/CRx1/CRx0/CRx1	DV_DATA22	DV input	CN11, pin B14	
		LCD_TCON5	Connected to LCD module DE pin	CN9, pin 24 CN10, pin B17	
44	PJ23/DV_DATA23/ LCD_DATA23/LCD_TCON6/ IRQ3/CTx1/CTx0&CTx1	DV_DATA23	DV input	CN11, pin A15	
		LCD_TCON6	Connected to the LCD module M_DISP pin	CN1, pin 18 CN10, pin B18	
45	PB14/A14/QIO3_1 / SPBIO3_1	A14	Address bus	CN4, pin 11	
		QIO3_1 / SPBIO3_1	Connected to serial flash memory 2 IO3 pin		
46	PB15/A15/QIO2_0/ SPBIO2_0	A15	Address bus	CN4, pin 10	
		QIO2_0 / SPBIO2_0	Connected to serial flash memory 1 IO2 pin		
47	PVcc				
48	PB16/A16/QIO3_0 / SPBIO3_0	A16	Address bus	CN4, pin 9	
		QIO3_0 / SPBIO3_0	Connected to serial flash memory 1 IO3 pin		
49	Vss				

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.3 SH7269 Pin Functions (3/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
50	PB17/A17/QSPCLK_0/ RSPCK0 / SPBCLK	A17	Address bus	CN4, pin 6	
		QSPCLK_0/ RSPCK0 / SPBCLK	Connected to serial flash memory 1 SCK pin		
51	Vcc				
52	PB18/A18/QSSL_0/SSL00 / SPBSSL	A18	Address bus	CN4, pin 5	JP4: Open
		QSSL_0/ SSL00/ SPBSSL	Connected to serial flash memory 1 CS pin	–	JP4: 1-2
53	PB19/A19/QMO_0/QIO0_0/ MOSI0 / SPBMO_0/SPBIO0_0	A19	Address bus	CN4, pin 4	
		QMO_0/QIO0_0/ MOSI0 / SPBMO_0/SPBIO0_0	Connected to serial flash memory 1 SI pin		
54	PB20/A20/QMI_0/QIO1_0/ MISO0 / SPBMI_0/SPBIO1_0	A20	Address bus	CN4, pin 3	
		QMI_0/QIO1_0/ MISO0 / SPBMI_0/SPBIO1_0	Connected to serial flash memory 1 SO pin		
55	Vss				
56	PB21/A21/CRx2/IERxD	A21	Address bus	CN4, pin 2	
57	Vcc				
58	PB22/A22/CTx2/IETxD/CS4#	A22	Address bus	CN4, pin 1	
59	PC0/CS0#/MD_BOOT2	CS0#	Connected to NOR flash memory CE# pin	CN6, pin 5	JP5: 1-2
		MD_BOOT2	Connected to SW5-4 as boot mode input 2		JP5: 2-3
60	PVcc				
61	CKIO	CKIO	Connected to SDRAM CLK pin	CN6, pin 20	
62	Vss				
63	PA0/MD_BOOT0	MD_BOOT0	Connected to SW5-2 as boot mode input 0	CN1, pin 10	RES#: low
64	Vcc				
65	PA1/MD_BOOT1	MD_BOOT1	Connected to SW5-3 as boot mode input 1	CN1, pin 9	RES#: low
66	PJ28/SSISCK5/TIOC1B/ RTS7#	SSISCK5	Connected to DAC 2 (U12) BICKI pin	CN7, pin 22	SW6-3: OFF
67	PJ29/SSIWS5/TIOC2A/ IERxD	SSIWS5	Connected to DAC 2 (U12) LRCKI pin	CN7, pin 24	SW6-3: OFF SW6-4: ON
		IERxD	Connected to the IEBus driver IC	CN1, pin 19	SW6-4: OFF
68	PJ30/SSIDATA5/TIOC2B/ IETxD	SSIDATA5	Connected to DAC 2 (U12) SDTI pin	CN7, pin 23	SW6-3: OFF SW6-4: ON
		IETxD	Connected to the IEBus driver IC	CN1, pin 20	SW6-4: OFF

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.4 SH7269 Pin Functions (4/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
69	PJ31/DV_CLK	DV_CLK	DV input	CN11, pin B16	
		–	Connected to the CD deck IIS_DATA pin	CN7, pin 27	
70	PE0/SCL0/TCLKA/ LCD_EXTCLK	–	–	CN7, pin 5	
71	PE1/SDA0/TCLKB/ AUDIO_CLK/DV_CLK	–	–	CN7, pin 8	
72	PE2/SCL1/TCLKC/IOIS16#/ DV_VSYNC	SCL1	Connected to EEPROM SCL pin	CN7, pin 7	
			Connected to DAC (U11, U12) SCL pins		
73	PE3/SDA1/TCLKD/ADTRG#/ DV_HSYNC	SDA1	Connected to EEPROM SDA pin	CN7, pin 10	
			Connected to DAC (U11, U12) SDA pins		
74	PE4/SCL2/RxD4/ DV_VSYNC	DV_VSYNC	DV input	CN11, pin A17	
		SCL2	Connected to the external IIC connector (J11)	CN7, pin 9	
75	PE5/SDA2/RxD5/ DV_HSYNC	DV_HSYNC	DV input	CN11, pin B17	
		SDA2	Connected to the external IIC connector (J11)	CN7, pin 12	
76	PE6/SCL3/RxD6	PE6	Connected to the character LCD RS pin	CN6, pin 12	
77	PE7/SDA3/RxD7	–	–	CN6, pin 13	
78	PVcc				
79	NMI	NMI	Non-maskable interrupt	–	
80	Vss				
81	ASEMD#	ASEMD#	ASE mode select	–	H-UDI
82	Vcc				
83	PLLVcc				
84	EXTAL	EXTAL	Connects the system external clock to MCU	–	13.33MHz
85	XTAL	XTAL	Open	–	
86	PLLVss				
87	PLLVss				
88	RES#	RES#	Reset input	CN7, pin 6	
89	RTC_X1	RTC_X1	Connects the realtime clock resonator to MCU	–	32.768kHz
90	RTC_X2	RTC_X2		–	
91	USBDPVcc				
92	USBDPVss				
93	DM	DM	USB differential D− data	–	
94	DP	DP	USB differential D+ data	–	
95	VBUS	VBUS	VBUS input	–	
96	USBDVcc				
97	USBDVss				
98	REFRIN	REFRIN	Reference input	–	Connects a 5.6 kΩ±1% resistor

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.5 SH7269 Pin Functions (5/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
99	USBAVss				
100	USBAPVcc				
101	USBAVcc				
102	USBAVss				
103	USBUVcc				
104	USBUVss				
105	USB_X1	USB_X1	Connects the USB external clock to MCU	–	48MHz
106	USB_X2	USB_X2	Open	–	
107	PVcc				
108	VIDEO_X1	VIDEO_X1	Connects the digital video decoder external clock to MCU	–	27MHz
109	VIDEO_X2	VIDEO_X2	Open	–	
110	Vss				
111	DVAVcc				
112	DVAVss				
113	VIN1	VIN1	Analog video signal input	CN10, pin A19	
114	VIN2	VIN2	Analog video signal input	CN10, pin B20	
115	VRT	VRT	Top reference voltage	–	
116	VRB	VRB	Bottom reference voltage	–	
117	BIAS	BIAS	Reference voltage	–	Connects a 24 kΩ±1% resistor
118	PH0/AN0/PINT0	–	–	CN3, pin 4	
119	PH1/AN1/PINT1	–	–	CN3, pin 3	
120	PH2/AN2/PINT2	–	–	CN3, pin 8	
121	PH3/AN3/PINT3	–	–	CN3, pin 7	
122	PH4/AN4/PINT4	–	–	CN3, pin 12 CN11, pin B18	
123	PH5/AN5/PINT5/ LCD_EXTCLK	–	–	CN3, pin 11 CN11, pin A19	
124	AVss				
125	PH6/AN6/PINT6	–	–	CN3, pin 16 CN11, pin B19	
126	AVcc				
127	PH7/AN7/PINT7	–	–	CN3, pin 15 CN11, pin A20	
128	AVref				
129	TRST#	TRST#	Initialization signal input pin	–	H-UDI
130	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Break mode acknowledge	–	H-UDI
		ASEBRK#	Break request		
131	TDO	TDO	Test data output	–	H-UDI
132	TDI	TDI	Test data input	–	H-UDI
133	TMS	TMS	Test mode select	–	H-UDI
134	TCK	TCK	Test clock	–	H-UDI
135	Vss				
136	PG0/D16/LCD_DATA0/ IRQ0/TIOC0A	LCD_DATA0	Connected to LCD module D0 pin	CN9, pin 2 CN10, pin A1	B0

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.6 SH7269 Pin Functions (6/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
137	Vcc				
138	PG1/D17/LCD_DATA1/ IRQ1/TIOC0B	LDC_DATA1	Connected to LCD module D1 pin	CN9, pin 1 CN10, pin B1	B1
139	Vss				
140	PG2/D18/LCD_DATA2/ IRQ2/TIOC0C	LCD_DATA2	Connected to LCD module D2 pin	CN9, pin 4 CN10, pin A2	B2
141	PVcc				
142	AUDIO_X2	AUDIO_X2	Open	–	
143	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	–	11.2896MHz
144	Vss				
145	PG3/D19/LCD_DATA3/ IRQ3/TIOC0D	LCD_DATA3	Connected to LCD module D3 pin	CN9, pin 3 CN10, pin B2	B3
146	Vcc				
147	PG4/D20/LCD_DATA4/ IRQ4/TIOC1A	LCD_DATA4	Connected to LCD module D4 pin	CN9, pin 6 CN10, pin B3	B4
148	PG5/D21/LCD_DATA5/ IRQ5/TIOC1B	LCD_DATA5	Connected to LCD module D5 pin	CN9, pin 8 CN10, pin A4	B5
149	PG6/D22/LCD_DATA6/ IRQ6/TIOC2A	LCD_DATA6	Connected to LCD module D6 pin	CN9, pin 7 CN10, pin B4	B6
150	PG7/D23/LCD_DATA7/ IRQ7/TIOC2B	LCD_DATA7	Connected to LCD module D7 pin	CN9, pin 9 CN10, pin B4	B7
151	PJ0/DV_DATA0/ LCD_DATA0/SD_CD_1/ PWM1A	DV_DATA0	DV input	CN11, pin A6	
		PJ0	Connected to the character LCD DB7 pin	CN7, pin 15	SW6-3: OFF
		SD_CD_1	Connected to the SD card slot CD pin		
		–	Connected to DAC1 (U11)BICKI pin	CN7, pin 17	SW6-3: ON
152	PVcc				
153	PJ1/DV_DATA1/ LCD_DATA1/SD_WP_1/ PWM1B	DV_DATA1	DV input	CN11, pin B6	
		PJ1	Connected to the character LCD DB6 pin	CN7, pin 16	SW6-3: OFF
		SD_WP_1	Connected to the SD card slot WP pin		
		–	Connected to DAC1 (U11) LRCKI pin	CN7, pin 20	SW6-3: ON
154	Vss				
155	PG8/D24/LCD_DATA8/ PINT0/TIOC3A	LCD_DATA8	Connected to LCD module D8 pin	CN 9, pin 12 CN 10, pin A6	G0
156	Vcc				
157	PJ2/DV_DATA2/ LCD_DATA2/SD_D1_1/ PWM1C	DV_DATA 2	DV input	CN11, pin A10	
		PJ2	Connected to the character LCD DB5 pin	CN7, pin 13	SW6-3: OFF
		SD_D1_1	Connected to the SD card slot DAT1 pin		
		–	Connected to DAC1 (U11) SDTI pin	CN7, pin 19	SW6-3: ON

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.7 SH7269 Pin Functions (7/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
158	PJ3/DV_DATA3/ LCD_DATA3/SD_D0_1/ PWM1D	DV_DATA3	DV input	CN11, pin B9	
		PJ3	Connected to the character LCD DB4 pin	CN7, pin 14	SW6-3: OFF
		SD_D0_1	Connected to the SD card slot DAT0 pin		
		–	Connected to DAC2 (U12) BICKI pin	CN7, pin 22	SW6-3: ON
159	PJ4/DV_DATA4/ LCD_DATA4/SD_CLK_1/ PWM1E	DV_DATA4	DV input	CN11, pin A9	
		PJ4	Connected to the character LCD DB3 pin	CN7, pin 3	SW6-3: OFF
		SD_CLK_1	Connected to the SD card slot CLK pin		
		–	Connected to DAC2 (U12) LRCKI pin	CN7, pin 24	SW6-3: ON
160	PG9/D25/LCD_DATA9/ PINT1/TIOC3B	LCD_DATA9	Connected to LCD module D9 pin	CN9, pin 11 CN10, pin B6	G1
161	PG10/D26/LCD_DATA10/ PINT2/TIOC3C	LCD_DATA10	Connected to LCD module D10 pin	CN9, pin 14 CN10, pin A7	G2
162	PVcc				
163	PG11/D27/LCD_DATA11/ PINT3/TIOC3D	LCD_DATA11	Connected to LCD module D11 pin	CN9, pin 13 CN10, pin B7	G3
164	Vss				
165	PG12/D28/LCD_DATA12/ PINT4	LCD_DATA12	Connected to LCD module D12 pin	CN9, pin 16 CN10, pin B8	G4
166	Vcc				
167	PG13/D29/LCD_DATA13/ PINT5	LCD_DATA13	Connected to LCD module D13 pin	CN9, pin 18 CN10, pin A9	G5
168	PG14/D30/LCD_DATA14/ PINT6	LCD_DATA14	Connected to LCD module D14 pin	CN9, pin 17 CN10, pin B9	G6
169	PG15/D31/LCD_DATA15/ PINT7	LCD_DATA15	Connected to LCD module D15 pin	CN9, pin 20 CN10, pin A10	G7
170	PG16/WE2#/ICIORD#/ DQMUL/LCD_DATA16/ AUDATA0	LCD_DATA16	Connected to LCD module D16 pin	CN10, pin A11	R0
		AUDATA0	Connected to the H-UDI port connector (J3)		AUD
171	PJ5/DV_DATA5/ LCD_DATA5/SD_CMD_1/ PWM1F	DV_DATA5	DV input	CN11, pin A7	
		PJ5	Connected to the character LCD DB2 pin	CN7, pin 4	SW6-3: OFF
		SD_CMD_1	Connected to the SD card slot CMD pin		
		–	Connected to DAC2 (U12) SDTI pin	CN7,pin 23	SW6-3: ON
172	PVcc				
173	PJ6/DV_DATA6/ LCD_DATA6/SD_D3_1/ PWM1G	DV_DATA6	DV input	CN11, pin B7	
		PJ6	Connected to the character LCD DB1 pin	CN7, pin 1	SW6-3: OFF
		SD_D3_1	Connected to the SD card slot DAT3 pin		
		–	Connected to the CD deck IIS_BCK pin	CN7, pin 25	SW6-3: ON
174	Vss				
175	PG17/WE3#/ICIOWR#/ AH#/DQMUU/ LCD_DATA17/AUDATA1	LCD_DATA17	Connected to LCD module D17 pin	CN10, pin B11	R1
		AUDATA1	Connected to the H-UDI port connector (J3)		AUD

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.8 SH7269 Pin Functions (8/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
176	Vcc				
177	PJ7/DV_DATA7/ LCD_DATA7/SD_D2_1/ PWM1H	DV_DATA7	DV input	CN11, pin A5	
		PJ7	Connected to the character LCD DB0 pin	CN7, pin 2	SW6-3: OFF
		SD_D2_1	Connected to the SD card slot DAT2 pin		
		–	Connected to the CD deck IIS_LRCK pin	CN7, pin 28	SW6-3: ON
178	PJ8/DV_DATA8/ LCD_DATA8/PINT0/ PWM2A/CTS5#	PWM2A	PWM output	CN11, pin A4	TTL level
		DV_DATA8	DV input		
		CTS5#	Connected to the UART connector (J10)	CN1, pin 12	TTL level
179	PJ9/DV_DATA9/ LCD_DATA9/PINT1/ PWM2B/RTS5#	PWM2B	PWM output	CN11, pin B3	TTL level
		DV_DATA9	DV input		
		RTS5#	Connected to the UART connector (J10)	CN1, pin 5	TTL level
180	PG18/DV_DATA4/ LCD_DATA18/SPDIF_IN/ SCK4	LCD_DATA18	Connected to LCD module D18 pin	CN10, pin A12	R2
181	PG19/DV_DATA5/ LCD_DATA19/SPDIF_OUT/ SCK5	LCD_DATA19	Connected to LCD module D19 pin	CN10, pin B12	R3
182	PVcc				
183	PG20/DV_DATA6/ LCD_DATA20/LCD_TCON3/ RxD4	LCD_DATA20	Connected to LCD module D20 pin	CN10, pin B13	R4
184	Vss				
185	PG21/DV_DATA7/ LCD_DATA21/LCD_TCON4/ TxD4/AUDATA2	LCD_DATA21	Connected to LCD module D21 pin	CN10, pin A14	R5
		AUDATA2	Connected to the H-UDI port connector (J3)		AUD
186	Vcc				
187	PG22/LCD_DATA22/ LCD_TCON5/RxD5/ AUDSYNC#	LCD_DATA22	Connected to LCD module D22 pin	CN10, pin B14	R6
		AUDSYNC#	Connected to the H-UDI port connector (J3)		AUD
		RxD5	Connected to the UART connector (J10)	CN1, pin 15	TTL level
188	PG23//LCD_DATA23/ LCD_TCON6/TxD5/ AUDATA3	LCD_DATA23	Connected to LCD module D23 pin	CN10, pin A15	R7
		AUDATA3	Connected to the H-UDI port connector (J3)		AUD
		TxD5	Connected to the UART connector (J10)	CN1, pin 14	TTL level
189	PG24/LCD_CLK	LCD_CLK	Connected to LCD module CLK pin	CN9, pin 23 CN10, pin A16	
190	PG25/LCD_TCON0	LCD_TCON0	Connected to LCD module VSYNC pin	CN9, pin 19 CN10, pin B16	
191	PG26/LCD_TCON1	LCD_TCON1	Connected to LCD module HSYNC pin	CN9, pin 21 CN10, pin A17	
192	PG27/LCD_TCON2/ LCD_EXTCLK	LCD_EXTCLK	Connects LCD module external clock to MCU	CN9, pin 26	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.9 SH7269 Pin Functions (9/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
193	PF0/BREQ#0/ QSPCLK_1/RSPCK1/ TIOC4A/DREQ0/ AUDCK	QSPCLK_1/ RSPCK1	Connected to serial flash memory 2 SCK pin	CN7, pin 30	
		AUDCK	Connected to the H-UDI port connector (J3)		AUD
		RSPCK1	Connected to the CD deck CDCK pin		
			Connected to the audio codec (U6) CCLK pin	CN9, pin 28	
194	PVcc				
195	PF1/BACK#/QSSL_1/ SSL10/TIOC4B/DACK0	QSSL_1/ SSL10	Connected to serial flash memory 2 CS# pin	CN5, pin 20	
196	Vss				
197	PF2/WAIT#/QMO_1/ QIO0_1/MOSI1/TIOC4C/ TEND0/ SPBMO_1/SPBIO0_1	QMO_1/QIO0_1 /MOSI1	Connected to serial flash memory 2 SI pin	CN7, pin 31	
		MOSI1 / SPBMO_1/SPBIO0_ 1	Connected to the CD deck CDSI pin		
			Connected to the audio codec (U6) CDTI pin	CN9, pin 30	
198	PF3/CS2#/QMI_1/ QIO1_1/MISO1/ TIOC4D/AUDIO_XOUT/ SPBMI_1/SPBIO1_1	QMI_1/QIO1_1 /MISO1	Connected to serial flash memory 2 SO pin	CN7, pin 33	
		MISO1/ SPBMI_1/SPBIO1_1	Connected to the CD deck CDSO pin		
199	PF4/CS5#/CE1A#/ SSISCK0/SGOUT_0	SGOUT_0		CN7, pin 36	0 Ω resistor
		SSISCK0	Connected to the audio codec (U6) BICK pin		
200	PF5/SSIWS0/SGOUT_1	SGOUT_1		CN7, pin 35	0 Ω resistor
		SSIWS0	Connected to the audio codec (U6) LRCK pin		
201	PF6/CE2A#/SSITxD0/ SGOUT_2	SGOUT_2		CN7, pin 37	0 Ω resistor
		SSITxD0	Connected to the audio codec (U6) SDTI pin		
202	PF7/SSIRxD0/RxD0/ SGOUT_3/CTS1#	SGOUT_3		CN7, pin 38	0 Ω resistor
		–	Connected to the audio codec (U6) SDTO pin		
203	PF8/A23/TxD0	A23	Address bus	CN5, pin 19	
204	PF9/BS#/DV_DATA0/ SCK0/MMC_D4/RTS1#	PF9		CN5, pin 18	
205	PVcc				
206	PF10/CS1#/SSISCK1/ DV_DATA1/SCK1/MMC_D 5	SSISCK1	Connected to DAC 1 (U11) BICKI pin	CN7, pin 17	SW6-3: OFF
207	Vss				
208	PF11/SSIWS1/DV_DATA2 / RxD1/MMC_D6	SSIWS1	Connected to DAC1 (U11) LRCKI pin	CN7, pin 20	SW6-3: OFF
209	PF12/SSIDATA1/ DV_DATA3/TxD1/MMC_D 7	SSIDATA1	Connected to DAC1 (U11) SDTI pin	CN7, pin 19	SW6-3: OFF
210	PF13/A24/SSISCK2/SCK2	A24	Address bus	CN5, pin 17	
211	PF14/A25/SSIWS2/RxD2	RxD2	Connected to the RS-232C connector (J10)	CN5, pin 16	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.10 SH7269 Pin Functions (10/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
212	PF15/A0/SSIDATA2/ WDTOVF#/TxD2/UBCTRG#	TxD2	Connected to the RS-232C connector (J10)	CN5, pin 15	
213	PVcc				
214	PJ10/DV_DATA10/ LCD_DATA10/PINT2/ PWM2C/SCK5#	PWM2C	PWM output	CN11, pin A2	TTL level
		DV_DATA10	DV input		
		SCK5#	Connected to the UART connector (J10)	CN1, pin 13	TTL level
215	Vss				
216	PF16/SD_CD_0/FCE#/ IRQ4/MMC_CD	SD_CD_0 MMC_CD	Connected to SD/MMC card slot CD pin	CN5, pin 13	SW6-2: ON
		FCE#	Connected to NAND flash memory CE# pin	CN5, pin 12	SW6-2: OFF
217	PF17/SD_WP_0/FRB/IRQ5	SD_WP_0	Connected to SD/MMC card slot WP pin	CN5, pin 11	SW6-2: ON
		FRB	Connected to NAND flash memory R/B# pin	CN5, pin 10	SW6-2: OFF
218	PF18/SD_D1_0/SSISCK3/ IRQ6/MMC_D1	SD_D1_0/ MMC_D1	Connected to SD/MMC card slot DAT1 pin	CN5, pin 8	
219	PJ11/DV_DATA11/ LCD_DATA11/PINT3/ PWM2D/SCK6	PWM2D	PWM output	CN1, pin B2	TTL level
		DV_DATA11	DV input		
		–	NC	CN1, pin 1	
220	PJ12/DV_DATA12/ LCD_DATA12/PINT4/ PWM2E/SCK7	PWM2E	PWM output	CN11, pin B11	TTL level
		DV_DATA12	DV input		
		PJ12	Connected to the audio codec (U6) CS pin	CN9, pin 27	
221	PJ13/DV_DATA13/ LCD_DATA13/PINT5/ PWM2F/TxD5	PWM2F	PWM output	CN11, pin A11	TTL level
		DV_DATA13	DV input		
		PJ13	Connected to the CD deck CDFS pin	CN7, pin 32	
222	PVcc				
223	PF19/SD_D0_0/SSIWS3/ IRQ7/MMC_D0	SD_D0_0 MMC_D0	Connected to SD/MMC card slot DAT0 pin	CN5, pin 7	
224	Vss				
225	PF20/SD_CLK_0/ SSIDATA3/MMC_CLK	SD_CLK_0/ MMC_CLK	Connected to SD/MMC card slot CLK pin	CN5, pin 5	
226	Vcc				
227	PF21/SD_CMD_0/SCK3/ MMC_CMD	SD_CMD_0/ MMC_CMD	Connected to SD/MMC card slot CMD pin	CN5, pin 4	
228	PF22/SD_3_0/RxD3/ MMC_D3	SD_D3_0/ MMC_D3	Connected to SD/MMC card slot DAT3 pin	CN5, pin 3	
229	PF23/SD_D2_0/TxD3/ MMC_D2	SD_D2_0/ MMC_D2	Connected to SD/MMC card slot DAT2 pin	CN5, pin 2	
230	PD0/D0/PWM1A	D0	Data bus	CN8, pin 1	
231	PVcc				
232	PJ24/SGOUT_0/SSISCK4/ LCD_TCON3/SPDIF_IN/SCK7	SSISCK4	Connected to the CD deck IIS_BCK pin	CN7, pin 25	SW6-3: OFF
233	Vss				
234	PD1/D1/PWM1B	D1	Data bus	CN8, pin 3	
235	PD2/D2/PWM1C	D2	Data bus	CN8, pin 6	
236	PD3/D3/PWM1D	D3	Data bus	CN8, pin 8	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 3.2.11 SH7269 Pin Functions (11/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
237	PJ25/SGOUT_1/SSIWS4/ LCD_TCON4/SPDIF_OUT/ RxD7	SSIWS4	Connected to the CD deck IIS_LRCK pin	CN7, pin 28	SW6-3: OFF
238	PJ26/SGOUT_2/SSIDATA4/ LCD_TCON5/TxD7	SSIDATA4	Connected to the CD deck IIS_DATA pin	CN7, pin 27	
239	PJ27/SGOUT_3/TIOC1A/ CTS7#	PJ27	Connected to DAC (U11, U12) and the audio codec (U6) PDN# pins	CN9, pin 29	
240	PVcc				
241	Vss				
242	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and NAND flash memory RE# pin	CN8, pin 11	Auto-switch
243	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and NAND flash memory CLE pin	CN8, pin 13	Auto-switch
244	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and NAND flash memory ALE pin	CN8, pin 16	Auto-switch
245	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and NAND flash memory WE# pin	CN8, pin 18	Auto-switch
246	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 2	
247	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 4	
248	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 7	
249	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 9	
250	PVcc				
251	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 12	
252	Vss				
253	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 14	
254	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 17	
255	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 19	
256	MD_CLK0	MD_CLK0	Connected to SW5-1 as the clock mode input	–	RES#: low

Legend: : 3.3V power supply, : 1.25V power supply, : GND

3.2.3 M3A-HS64G01 Module Availability

Table 3.2.12 shows which combination of modules can/cannot be used.

Table 3.2.12 M3A-HS64G01 Module Availability

				R0K572690C000BR																R0K572690C000BR+M3A-HS64G01											
	SH7269 Peripherals	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory 1	Serial flash memory 2	USB	SD/MMC card	H-UDI (14-pin)	H-UDI (38-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C	LCD	DV	PWM	Character LCD	SD card	Audio codec	D/A Converter 1	D/A Converter 2	CD deck	UART	IIC	LCD	IEBus™	CAN 0	CAN 1	Key input switches
R0K572690C000BR	BSC	U6	NOR flash memory		Y	Y	Y	N	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	BSC	U9	SDRAM	Y		Y	Y	Y	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	FLCTL	U7	NAND flash memory	Y	Y		Y	Y	Y	Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	RSPI	U10	Serial flash memory 1	N	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	RSPI	U10	Serial flash memory 2	(1)	(1)	Y	Y	Y		Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(11)	Y	Y	(11)	Y	Y	Y	–	Y	Y
	USB	J1,2	USB	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	SDHI/MMC	J11	SD/MMC card	Y	Y	(2)	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y	Y	Y		(3)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	H-UDI, AUD	J3	H-UDI (38-pin)	Y	Y	Y	Y	Y	N	Y	Y	(3)		Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	–	Y	Y
	I/O ports	LED2, LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	(6)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	(5)	Y	Y	Y	Y	Y	Y	Y	Y	Y	(13)	Y	–	(13)	Y
	I/O ports	SW5, SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	(7)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	VDC4	CN10	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y		(4)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	VDC4	CN11	DV	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(6)	Y	(5)	(7)	Y	(4)		(8)	N	N	N	N	N	N	N	Y	N	Y	–	(12)	Y
	PWM	CN11	PWM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(8)		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
R0K572690C000BR+M3A-HS64G01	I/O ports	J1	Character LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y		(9)	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	SDHI	J2	SD card	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	(9)		Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	SSIF, RSPI	U6	Audio codec	Y	Y	Y	Y	Y	(11)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y		Y	Y	(11)	Y	Y	Y	–	Y	Y
	SSIF, IIC3	U11	D/A Converter 1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y		Y	Y	Y	Y	Y	–	Y	Y
	SSIF, IIC3	U12	D/A Converter 2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y		Y	Y	Y	Y	(10)	–	Y	Y
	ROMDEC	J9	CD deck	Y	Y	Y	Y	Y	(11)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	(11)	Y	Y		Y	Y	Y	Y	–	Y	Y
	SCIF	J10	UART	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	–	Y	Y
	IIC3	J11	IIC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	–	Y	Y
	VDC4	J12 to J14	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(13)	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	–	Y	Y
	IEB	J15	IEBus™	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(10)	Y	Y	Y		–	Y	Y
	RCAN	J16	CAN 0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–
	RCAN	J17	CAN 1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(13)	Y	Y	Y	(12)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–		Y
	I/O ports	SW2 to SW17	Key input switches	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	

Y: Yes, N: No, –: N/A

Notes:
1. When using a serial flash memory with NOR flash memory or SDRAM, quad mode cannot be used.
2. PF16 and PF17 are multiplexed pins. When setting SW6-2 on the R0K572690C000BR, ether SD/MMC card or NAND flash memory can be used.
3. Either 14-pin or 38-pin H-UDI port connector can be used.
4. PJ22 and PJ23 are multiplexed pins. Either LCD or DV can be used.
5. PJ21 is a multiplexed pin. Either IRQ1 switch or DV can be used.
6. PJ19 and PJ18 are multiplexed pins. Either LED or DV can be used.
7. PJ17 and PJ16 are multiplexed pins. Either DIP switches or DV can be used.
8. PJ15 to PJ8 are multiplexed pins/ Either DV or PWM can be used.
9. Change the JP2 setting on the M3A-HS64G01 to use either the character LCD or the SD card.
10. PJ29 and PJ30 are multiplexed pins. When setting SW6-4 on the R0K572690C000BR, either IEBus or D/A Converter 2 can be used.
11. CD deck and audio codec cannot be accessed at the same time, because these modules use RSPI1 pin.
12. PJ20 and PJ21 are multiplexed pins. Either DV or CAN1 can be used.
13. Change the JP8 setting on the R0K572690C000BR to use either LCD or CAN1.

3.2.4 SH7269 Multiplexed Pins Used on the M3A-HS64G01

Table 3.2.13 to Table 3.2.30 list the SH7269 multiplexed pin functions used on the M3A-HS64G01.

These multiplexed pins are set as port input pins by default. Set the MD bit in the Port control register to use the SH7269 peripheral functions (except I/O ports).

Table 3.2.13 SH7269 Multiplexed Pin Functions (BSC1)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
BSC	CS0#	PCCR0	PC0MD = B'1 (1)	PC0/**CS0#**/MD_BOOT2
	CS3#	PCCR2	PC8MD[2:0] = B'001	PC8/**CS3#**/TxD7/CTx1/CTx0&CTx1
	RD#	PCCR0	PC1MD = B'1 (1)	PC1/**RD#**
	WE0#/DQMLL	PCCR0	PC3MD[1:0] = B'01	PC3/**WE0#**/**DQMLL**/RxD6
	WE1#/WE#/DQMLU	PCCR1	PC4MD[1:0] = B'01	PC4/**WE1#**/**DQMLU**/TxD6
	RAS#	PCCR1	PC5MD[2:0] = B'001	PC5/**RAS#**/CRx0/CRx0/CRx1/CRx2/IRQ0
	CAS#	PCCR1	PC6MD[2:0] = B'001	PC6/**CAS#**/SCK7/CTx0/CTx0&CTx1&CTx2
	CKE	PCCR1	PC7MD[2:0] = B'001	PC7/**CKE**/RxD7/CRx1/CRx0/CRx1/IRQ1
	RD/WR#	PCCR0	PC2MD[1:0] = B'01	PC2/**RD**/**WR#**/SCK6
	A24	PFCR3	PF13MD[2:0] = B'001	PF13/**A24**/SSISCK2/SCK2
	A23	PFCR2	PF8MD[2:0] = B'001	PF8/**A23**/TxD0
	A22	PBCR5	PB22MD[2:0] = B'001	PB22/**A22**/CTx2/IETxD/CS4#
	A21	PBCR5	PB21MD[1:0] = B'01	PB21/**A21**/CRx2/IERxD
	A20	PBCR5	PB20MD[2:0] = B'001 (1)	PB20/**A20**/QMISO0&QIO10/MISO0/SPBMI_0/ SPBIO1_0
	A19	PBCR4	PB19MD[2:0] = B'001 (1)	PB19/**A19**/QMO_0&QIO0_0/MOSI0 / SPBMO_0/SPBIO0_0
	A18	PBCR4	PB18MD[2:0] = B'001 (1)	PB18/**A18**/QSSL_0/SSL00/ SPBSSL
	A17	PBCR4	PB17MD[2:0] = B'001 (1)	PB17/**A17**/QSPCLK_0/RSPCK0 / SPBCLK
	A16	PBCR4	PB16MD[2:0] = B'001 (1)	PB16/**A16**/QIO3_0 / SPBIO3_0
	A15	PBCR3	PB15MD[2:0] = B'001 (1)	PB15/**A15**/QIO2_0 / SPBIO2_0
	A14	PBCR3	PB14MD[2:0] = B'001 (1)	PB14/**A14**/QIO3_1 / SPBIO3_1
	A13	PBCR3	PB13MD[2:0] = B'001 (1)	PB13/**A13**/QIO2_1 / SPBIO2_1
	A12	PBCR3	PB12MD[1:0] = B'01 (1)	PB12/**A12**/TIOC3D
	A11	PBCR2	PB11MD[1:0] = B'01 (1)	PB11/**A11**/TIOC3C
	A10	PBCR2	PB10MD[1:0] = B'01 (1)	PB10/**A10**/TIOC3B
	A9	PBCR2	PB9MD[1:0] = B'01 (1)	PB9/**A9**/TIOC3A
	A8	PBCR2	PB8MD[1:0] = B'01 (1)	PB8/**A8**/TIOC2B
	A7	PBCR1	PB7MD[1:0] = B'01 (1)	PB7/**A7**/TIOC2A
	A6	PBCR1	PB6MD[1:0] = B'01 (1)	PB6/**A6**/TIOC1B
	A5	PBCR1	PB5MD[1:0] = B'01 (1)	PB5/**A5**/TIOC1A
	A4	PBCR1	PB4MD[1:0] = B'01 (1)	PB4/**A4**/TIOC0D
	A3	PBCR0	PB3MD[1:0] = B'01 (1)	PB3/**A3**/TIOC0C
	A2	PBCR0	PB2MD[1:0] = B'01 (1)	PB2/**A2**/TIOC0B
	A1	PBCR0	PB1MD[1:0] = B'01 (1)	PB1/**A1**/TIOC0A
	D15	PDCR3	PD15MD[1:0] = B'01 (1)	PD15/**D15**/**NAF7**/PWM2H
	D14	PDCR3	PD14MD[1:0] = B'01 (1)	PD14/**D14**/**NAF6**/PWM2G
	D13	PDCR3	PD13MD[1:0] = B'01 (1)	PD13/**D13**/**NAF5**/PWM2F
	D12	PDCR3	PD12MD[1:0] = B'01 (1)	PD12/**D12**/**NAF4**/PWM2E
	D11	PDCR2	PD11MD[1:0] = B'01 (1)	PD11/**D11**/**NAF3**/PWM2D
	D10	PDCR2	PD10MD[1:0] = B'01 (1)	PD10/**D10**/**NAF2**/PWM2C
	D9	PDCR2	PD9MD[1:0] = B'01 (1)	PD9/**D9**/**NAF1**/PWM2B
	D8	PDCR2	PD8MD[1:0] = B'01 (1)	PD8/**D8**/**NAF0**/PWM2A
	D7	PDCR1	PD7MD[1:0] = B'01 (1)	PD7/**D7**/**FWE#**/PWM1H
	D6	PDCR1	PD6MD[1:0] = B'01 (1)	PD6/**D6**/**FALE**/PWM1G

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 3.2.14 SH7269 Multiplexed Pin Functions (BSC2)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
BSC	D5	PDCR1	PD5MD[1:0] = B'01(1)	PD5/**D5/FCLE**/PWM1F
	D4	PDCR1	PD4MD[1:0] = B'01 (1)	PD4/**D4/FRE#**/PWM1E
	D3	PDCR0	PD3MD[1:0] = B'01 (1)	PD3/**D3**/PWM1D
	D2	PDCR0	PD2MD[1:0] = B'01 (1)	PD2/**D2**/PWM1C
	D1	PDCR0	PD1MD[1:0] = B'01 (1)	PD1/**D1**/ PWM1B
	D0	PDCR0	PD0MD[1:0] = B'01 (1)	PD0/**D0**/PWM1A

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 3.2.15 SH7269 Multiplexed Pin Functions (INTC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
INTC	IRQ1	PJCR5	PJ21MD[2:0] = B'100	PJ21/DV_DATA21/LCD_DATA21/LCD_TCON4/ **IRQ1**/CTx2/CTx0&CTx1&CTx2
	IRQ2	PJCR5	PJ20MD[2:0] = B'100	PJ20/DV_DATA20/LCD_DATA20/LCD_TCON3/ **IRQ0**/CRx2/CRx0&CRx1&CRx2

Note: Bold text indicates the function used.

Table 3.2.16 SH7269 Multiplexed Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SCIF	RxD2	PFCR3	PF14MD[2:0] = B'100	PF14/A25/SSIWS2//**RxD2**
	TxD2	PFCR4	PF15MD[2:0] = B'100	PF15/A0/SSIDATA2/WDTOVF#/**TxD2**/UBCTRG#
	TxD5	PGCR5	PG23MD[2:0] = B'100	PG23/LCD_DATA23/LCD_TCON6/**TxD5**
	RxD5	PGCR5	PG22MD[2:0] = B'100	PG22/LCD_DATA22/LCD_TCON5/**RxD5**
	SCK5	PJCR2	PJ10MD[2:0] = B'101	PJ10/DV_DATA10/LCD_DATA10/PINT2/PWM2C/ **SCK5**
	RTS5#	PJCR2	PJ9MD[2:0] = B'101	PJ9/DV_DATA9/LCD_DATA9/PINT1/PWM2B/ **RTS5#**
	CTS5#	PJCR2	PJ8MD[2:0] = B'101	PJ8/DV_DATA8/PINT0/PWM2A/**CTS5#**

Note: Bold text indicates the function used.

Table 3.2.17 SH7269 Multiplexed Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
IIC3	SDA1	PECR0	PE3MD[2:0] = B'001	PE3/**SDA1**/TCLKD/ADTRG#/DV_HSYNC
	SCL1	PECR0	PE2MD[2:0] = B'001	PE2/**SCL1**/TCLKC/IOIS16#/DV_VSYNC
	SDA2	PECR1	PE5MD[2:0] = B'01	PE5/**SDA2**/RxD5/DV_HSYNC
	SCL2	PECR1	PE4MD[2:0] = B'01	PE4/**SCL2**/RxD4/DV_VSYNC

Note: Bold test indicates the function used.

Table 3.2.18 SH7269 Multiplexed Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01 (1)	PD15/**D15**/**NAF7**/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01 (1)	PD14/**D14**/**NAF6**/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01 (1)	PD13/**D13**/**NAF5**/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01 (1)	PD12/**D12**/**NAF4**/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01 (1)	PD11/**D11**/**NAF3**/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01 (1)	PD10/**D10**/**NAF2**/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01 (1)	PD9/**D9**/**NAF1**/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01 (1)	PD8/**D8**/**NAF0**/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01 (1)	PD7/**D7**/**FWE#**/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01 (1)	PD6/**D6**/**FALE**/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01 (1)	PD5/**D5**/**FCLE**/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01 (1)	PD4/**D4**/**FRE#**/PWM1E
	FCE#	PFCR5	PF16MD[2:0] = B'011	PF16/SD_CD_0/**FCE#**/IRQ4/MMC_CD
	FRB	PFCR5	PF17MD[2:0] = B'011	PF17/SD_WP_0/**FRB**/IRQ5

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 3.2.19 SH7269 Multiplexed Pin Functions (RSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RSPI	MISO0	PBCR5	PB20MD[1:0] = B'11 (1)	PB20/A20/QMI_0/QIO1_0/**MISO0**
	MOSI0	PBCR4	PB19MD[1:0] = B'11 (1)	PB19/A19/QMO_0/QIO_0/**MOSI0**
	SSL00	PBCR4	PB18MD[1:0] = B'11 (1)	PB18/A18/QSSL_0/**SSL00**
	RSPCK0	PBCR4	PB17MD[1:0] = B'11 (1)	PB17/A17/QSPCLK_0/**RSPCK0**
	MISO1	PFCR0	PF3MD[2:0] = B'011	PF3/CS2#/QMI_1/QIO1_1/**MISO1**/TIOC4D/ AUDIO_XOUT
	MOSI1	PFCR0	PF2MD[2:0] = B'011	PF2/WAIT#/QMO_1/QIO0_1/**MOSI1**/TIOC4C TEND0
	SSL10	PFCR0	PF1MD[2:0] = B'011	PF1/BACK#/QSSL_1/**SSL10**/TIOC4B/DACK0
	RSPCK1	PFCR0	PF0MD[2:0] = B'011	PF0/BREQ#/QSPCLK_1/**RSPCK1**/TIOC4A/ DREQ0/AUDCK

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 3.2.20 SH7269 Multiplexed Pin Functions (RQSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RQSPI	QIO3_0	PBCR4	PB16MD[2:0] = B'010 (1)	PB16/A16/**QIO3_0** / SPBIO3_0
	QIO2_0	PBCR3	PB15MD[2:0] = B'010 (1)	PB15/A15/**QIO2_0** / SPBIO2_0
	QIO1_0	PBCR5	PB20MD[2:0] = B'010 (1)	PB20/A20/**QMI_0**/**QIO1_0**/MISO0 / SPBMI_0/SPBIO1_0
	QIO0_0	PBCR4	PB19MD[2:0] = B'010 (1)	PB19/A19/**QMO_0**/**QIO0_0**/MOSI0 / SPBMO_0/SPBIO0_0
	QSSL_0	PBCR4	PB18MD[2:0] = B'010 (1)	PB18/A18/**QSSL_0**/SSL00 / SPBSSL
	QSPCLK_0	PBCR4	PB17MD[2:0] = B'010 (1)	PB17/A17/**QSPCLK_0**/RSPCK0 / SPBCLK
	QIO3_1	PBCR3	PB14MD[2:0] = B'010 (1)	PB14/A14/**QIO3_1** / SPBIO3_1
	QIO2_1	PBCR3	PB13MD[2:0] = B'010 (1)	PB13/A13/**QIO2_1** / SPBIO2_1
	QIO1_1	PFCR0	PF3MD[2:0] = B'010	PF3/CS2#/**QMI_1**/**QIO1_1**/MISO1/TIOC4D/ AUDIO_XOUT / SPBMI_1/SPBIO1_1
	QIO0_1	PFCR0	PF2MD[2:0] = B'010	PF2/WAIT#/**QMO_1**/**QIO0_1**/MOSI1/TIOC4C/TEND0/ SPBMO_1/SPBIO0_1
	QSSL_1	PFCR0	PF1MD[2:0] = B'010	PF1/BACK#/**QSSL_1**/SSL10/TIOC4B/DACK0
	QSPCLK_1	PFCR0	PF0MD[2:0] = B'010	PF0/BREQ#/**QSPCLK_1**/RSPCK1/TIOC4A/DREQ0/ AUDCK

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 3.2.21 SH7269 Multiplexed Pin Functions (SPIBSC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SPIBSC	SPBCLK	PBCR4	PB17MD[2:0] = B'110 (1)	PB17 / A17 / QSPCLK_0 / RSPCK0 / **SPBCLK**
	SPBSSL	PBCR4	PB18MD[2:0] = B'110 (1)	PB18 / A18 / QSSL_0 / SSL00 / **SPBSSL**
	SPBMO_0/ SPBIO0_0	PBCR4	PB19MD[2:0] = B'110 (1)	PB19 / A19 / QMO_0/QIO0_0 / MOSI0 / **SPBMO_0/SPBIO0_0**
	SPBMI_0/ SPBIO1_0	PBCR5	PB20MD[2:0] = B'110 (1)	PB20 / A20 / QMI_0/QIO1_0 / MISO0 / **SPBMI_0/SPBIO1_0**
	SPBIO2_0	PBCR3	PB15MD[2:0] = B'110 (1)	PB15 / A15 / QIO2_0 / **SPBIO2_0**
	SPBIO3_0	PBCR4	PB16MD[2:0] = B'110 (1)	PB16 / A16 / QIO3_0 / **SPBIO3_0**
	SPBMO_1/ SPBIO0_1	PFCR0	PF2MD[2:0] = B'110	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / **SPBMO_1/SPBIO0_1**
	SPBMI_1/ SPBIO1_1	PFCR0	PF3MD[2:0] = B'110	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / **SPBMI_1/SPBIO1_1**
	SPBIO2_1	PBCR3	PB13MD[2:0] = B'110 (1)	PB13 / A13 / QIO2_1 / **SPBIO2_1**
	SPBIO3_1	PBCR3	PB14MD[2:0] = B'110 (1)	PB14 / A14 / QIO3_1 / **SPBIO3_1**

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 3.2.22 SH7269 Multiplexed Pin Functions (RCAN-TL1)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RCAN-TL1	CRx2	PJCR5	PJ20MD[2:0] = B'101	PJ20/DV_DATA20/LCD_DATA20/LCD_TCON3/ IRQ0/**CRx2**/CRx0/CRx1/CRx2
	CTx2	PJCR5	PJ21MD[2:0] = B'101	PJ21/DV_DATA21/LCD_DATA21/LCD_TCON4/ IRQ1/**CTx2**/CTx0&CTx1&CTx2

Note: Bold text indicates the function used.

Table 3.2.23 SH7269 Multiplexed Pin Functions (IEB)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
IEB	IERxD	PJCR7	PJ29MD[2:0] = B'101	PJ29/SSIWS5/TIOC2A/**IERxD**
	IETxD	PJCR7	PJ30MD[2:0] = B'101	PJ30/SSIDATA5/TIOC2B/**IETxD**

Note: Bold text indicates the function used.

Table 3.2.24 SH7269 Multiplexed Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SDHI	SD_CD_0	PFCR5	PF16MD[2:0] = B'001	PF16/**SD_CD_0**/FCE#/IRQ4/MMC_CD
	SD_WP_0	PFCR5	PF17MD[2:0] = B'001	PF17/**SD_WP_0**/FRB/IRQ5
	SD_D1_0	PFCR5	PF18MD[2:0] = B'001	PF18/**SD_D1_0**/SSISCK3/IRQ6/MMC_D1
	SD_D0_0	PFCR5	PF19MD[2:0] = B'001	PF19/**SD_D0_0**/SSIWS3/IRQ7/MMC_D0
	SD_CLK_0	PFCR6	PF20MD[2:0] = B'001	PF20/**SD_CLK_0**/SSIDATA3/MMC_CLK
	SD_CMD_0	PFCR6	PF21MD[2:0] = B'001	PF21/**SD_CMD_0**/SCK3/ MMC_CMD
	SD_D3_0	PFCR6	PF22MD[2:0] = B'001	PF22/**SD_D3_0**/RxD3/MMC_D3
	SD_D2_0	PFCR6	PF23MD[2:0] = B'001	PF23/**SD_D2_0**/TxD3/MMC_D2
	SD_CD_1	PJCR0	PJ0MD[2:0] = B'011	PJ0/DV_DATA0/LCD_DATA0/**SD_CD_1**/PWM1A
	SD_WP_1	PJCR0	PJ1MD[2:0] = B'011	PJ1/DV_DATA1/LCD_DATA1/**SD_WP_1**/PWM1B
	SD_D1_1	PJCR0	PJ2MD[2:0] = B'011	PJ2/DV_DATA2/LCD_DATA2/**SD_D1_1**/PWM1C
	SD_D0_1	PJCR0	PJ3MD[2:0] = B'011	PJ3/DV_DATA3/LCD_DATA3/**SD_D0_1**/PWM1D
	SD_CLK_1	PJCR1	PJ4MD[2:0] = B'011	PJ4/DV_DATA4/LCD_DATA4/**SD_CLK_1**/PWM1E
	SD_CMD_1	PJCR1	PJ5MD[2:0] = B'011	PJ5/DV_DATA5/LCD_DATA5/**SD_CMD_1**/PWM1F
	SD_D3_1	PJCR1	PJ6MD[2:0] = B'011	PJ6/DV_DATA6/LCD_DATA6/**SD_D3_1**/PWM1G
	SD_D2_1	PJCR1	PJ7MD[2:0] = B'011	PJ7/DV_DATA7/LCD_DATA7/**SD_D2_1**/PWM1H

Note: Bold text indicates the function used,

Table 3.2.25 SH7269 Multiplexed Pin Functions (MMC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
MMC	MMC_CD	PFCR5	PF16MD[2:0] = B'101	PF16/SD_CD_0/FCE#/IRQ4/**MMC_CD**
	MMC_D1	PFCR5	PF18MD[2:0] = B'101	PF18/SD_D1_0/SSISCK3/IRQ6/**MMC_D1**
	MMC_D0	PFCR5	PF19MD[2:0] = B'101	PF19/SD_D0_0/SSIWS3/IRQ7/**MMC_D0**
	MMC_CLK	PFCR6	PF20MD[2:0] = B'101	PF20/SD_CLK_0/SSIDATA3/**MMC_CLK**
	MMC_CMD	PFCR6	PF21MD[2:0] = B'101	PF21/SD_CMD_0/SCK3/**MMC_CMD**
	MMC_D3	PFCR6	PF22MD[2:0] = B'101	PF22/SD_D3_0/RxD3/**MMC_D3**
	MMC_D2	PFCR6	PF23MD[2:0] = B'101	PF23/SD_D2_0/TxD3/**MMC_D2**

Note: Bold text indicates the function used.

Table 3.2.26 SH7269 Multiplexed Pin Functions (SSIF)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SSIF	SSISCK5	PJCR7	PJ28MD[2:0] = B'010	PJ28/**SSISCK5**/TIOC1B/RTS7#
	SSIWS5	PJCR7	PJ29MD[2:0] = B'010	PJ29/**SSIWS5**/TIOC2A/IERxD
	SSIDATA5	PJCR7	PJ30MD[2:0] = B'010	PJ30/**SSIDATA5**/TIOC2B/IETxD
	SSIDATA4	PJCR6	PJ26MD[2:0] = B'010	PJ26/SGOUT_2/**SSIDATA4**/LCD_TCON5/TxD7
	SSIWS4	PJCR6	PJ25MD[2:0] = B'010	PJ25/SGOUT_1/**SSIWS4**/LCD_TCON4/ SPDIF_OUT/RxD7
	SSISCK4	PJCR6	PJ24MD[2:0] = B'010	PJ24/SGOUT_0/**SSISCK4**/LCD_TCON3/SPDIF_IN/ SCK7
	SSIDATA1	PFCR3	PF12MD[2:0] = B'010	PF12 / **SSIDATA1** / DV_DATA3 / TxD1 / MMC_D7
	SSIWS1	PFCR2	PF11MD[2:0] = B'010	PF11/**SSIWS1**/DV_DATA2/RxD1/MMC_D6
	SSISCK1	PFCR2	PF10MD[2:0] = B'010	PF10/CS1#/**SSISCK1**/DV_DATA1/SCK1/MMC_D5
	SSIRxD0	PFCR1	PF7MD[2:0] = B'010	PF7/**SSIRxD0**/RxD0/SGOUT_3/CTS1#
	SSITxD0	PFCR1	PF6MD[2:0] = B'010	PF6/CE2A#/**SSITxD0**/SGOUT_2
	SSIWS0	PFCR1	PF5MD[2:0] = B'010	PF5/**SSIWS0**/SGOUT_1
	SSISCK0	PFCR1	PF4MD[2:0] = B'010	PF4/CS5#/CE1A#/**SSIWS0**/SGOUT_0

Note: Bold text indicates the function used.

Table 3.2.27 SH7269 Multiplexed Pin Functions (ADC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
ADC	AN7	PHCR1	PH7MD[1:0] = B'01	PH7/**AN7**/PINT7
	AN6	PHCR1	PH6MD[1:0] = B'01	PH6/**AN6**/PINT6
	AN5	PHCR1	PH5MD[1:0] = B'01	PH5/**AN5**/PINT5/LCD_EXTCLK
	AN4	PHCR1	PH4MD[1:0] = B'01	PH4/**AN4**/PINT4
	AN3	PHCR0	PH3MD[1:0] = B'01	PH3/**AN3**/PINT3
	AN2	PHCR0	PH2MD[1:0] = B'01	PH2/**AN2**/PINT2
	AN1	PHCR0	PH1MD[1:0] = B'01	PH1/**AN1**/PINT1
	AN0	PHCR0	PH0MD[1:0] = B'01	PH0/**AN0**/PINT0

Note: Bold text indicates the function used.

Table 3.2.28 SH7269 Multiplexed Pin Functions (VDC4)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
VDC4	LCD_EXTCLK	PGCR6	PG27MD[1:0] = B'11	PG27/LCD_TCON2/**LCD_EXTCLK**
	LCD_CLK	PGCR6	PG24MD[1:0] = B'10	PG24/**LCD_CLK**
	LCD_TCON6	PJCR5	PJ23MD[2:0] = B'011	PJ23/DV_DATA23/LCD_DATA23/**LCD_TCON6**/ IRQ3/CTx1/CTx0&CTx1
	LCD_TCON5	PJCR5	PJ22MD[2:0] = B'011	PJ22/DV_DATA22/LCD_DATA22/**LCD_TCON5**/ IRQ2/CRx1/CRx0/CRx1
	LCD_TCON1	PGCR6	PG26MD[1:0] = B'10	PG26/**LCD_TCON1**
	LCD_TCON0	PGCR6	PG25MD[1:0] = B'10	PG25/**LCD_TCON0**
	LCD_DATA23	PGCR5	PG23MD[2:0] = B'010	PG23/**LCD_DATA23**/LCD_TCON6/TxD5/AUDATA3
	LCD_DATA22	PGCR5	PG22MD[2:0] = B'010	PG22/**LCD_DATA22**/LCD_TCON5/RxD5/AUDSYNC#
	LCD_DATA21	PGCR5	PG21MD[2:0] = B'010	PG21/DV_DATA7/**LCD_DATA21**/LCD_TCON4/TxD4
	LCD_DATA20	PGCR5	PG20MD[2:0] = B'010	PG20/DV_DATA6/**LCD_DATA20**/LCD_TCON3/RxD4
	LCD_DATA19	PGCR4	PG19MD[2:0] = B'010	PG19/DV_DATA5/**LCD_DATA19**/SPDIF_OUT/SCK5
	LCD_DATA18	PGCR4	PG18MD[2:0] = B'010	PG18/DV_DATA4/**LCD_DATA18**/SPDIF_IN/SCK4
	LCD_DATA17	PGCR4	PG17MD[1:0] = B'10	PG17/WE3#/ICIOWR#/AH/DQMUU/**LCD_DATA17**/ AUDATA1
	LCD_DATA16	PGCR4	PG16MD[1:0] = B'10	PG16/WE2#/ICIORD#/DQMUL/**LCD_DATA16**/ AUDATA0
	LCD_DATA15	PGCR3	PG15MD[1:0] = B'10 (1)	PG15/D31/**LCD_DATA15**/PINT7
	LCD_DATA14	PGCR3	PG14MD[1:0] = B'10 (1)	PG14/D30/**LCD_DATA14**/PINT6
	LCD_DATA13	PGCR3	PG13MD[1:0] = B'10 (1)	PG13/D29/**LCD_DATA13**/PINT5
	LCD_DATA12	PGCR3	PG12MD[1:0] = B'10 (1)	PG12/D28/**LCD_DATA12**/PINT4
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'010 1)	PG11/D27/**LCD_DATA11**/PINT3/TIOC3D
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'010 1)	PG10/D26/**LCD_DATA10**/PINT2/TIOC3C
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'010 (1)	PG9/D25/**LCD_DATA9**/PINT1/TIOC3B
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'010 (1)	PG8/D24/**LCD_DATA8**/PINT0/TIOC3A
	LCD_DATA7	PGCR1	PG7MD[2:0] = B'010 (1)	PG7/D23/**LCD_DATA7**/IRQ7/TIOC2B
	LCD_DATA6	PGCR1	PG6MD[2:0] = B'010 (1)	PG6/D22/**LCD_DATA6**/IRQ6/TIOC2A
	LCD_DATA5	PGCR1	PG5MD[2:0] = B'010 (1)	PG5/D21/**LCD_DATA5**/IRQ5/TIOC1B
	LCD_DATA4	PGCR1	PG4MD[2:0] = B'010 (1)	PG4/D20/**LCD_DATA4**/IRQ4/TIOC1A
	LCD_DATA3	PGCR0	PG3MD[2:0] = B'010 (1)	PG3/D19/**LCD_DATA3**/IRQ3/TIOC0D
	LCD_DATA2	PGCR0	PG2MD[2:0] = B'010 (1)	PG2/D18/**LCD_DATA2**/IRQ2/TIOC0C
	LCD_DATA1	PGCR0	PG1MD[2:0] = B'010 (1)	PG1/D17/**LCD_DATA1**/IRQ1/TIOC0B
	LCD_DATA0	PGCR0	PG0MD[2:0] = B'010 (1)	PG0/D16/**LCD_DATA0**/IRQ0/TIOC0A

Notes: 1. These values must not be set in boot mode 1.
2. Bold text indicates the function used.

Table 3.2.29 SH7269 Multiplexed Pin Functions (PWM)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
PWM	PWM2H	PJCR3	PJ15MD[2:0] = B'100	PJ15/DV_DATA15/LCD_DATA15/PINT7/**PWM2H**/TxD7
	PWM2G	PJCR3	PJ14MD[2:0] = B'100	PJ14/DV_DATA14/LCD_DATA14/PINT6/**PWM2G**/TxD6
	PWM2F	PJCR3	PJ13MD[2:0] = B'100	PJ13/DV_DATA13/LCD_DATA13/PINT5/**PWM2F**/TxD5
	PWM2E	PJCR3	PJ12MD[2:0] = B'100	PJ12/DV_DATA12/LCD_DATA12/PINT4/**PWM2E**/SCK7
	PWM2D	PJCR2	PJ11MD[2:0] = B'100	PJ11/DV_DATA11/LCD_DATA11/PINT3/**PWM2D**/SCK6
	PWM2C	PJCR2	PJ10MD[2:0] = B'100	PJ10/DV_DATA10/LCD_DATA10/PINT2/**PWM2C**/SCK5
	PWM2B	PJCR2	PJ9MD[2:0] = B'100	PJ9/DV_DATA9/LCD_DATA9/PINT1/**PWM2B**/RTS5#
	PWM2A	PJCR2	PJ8MD[2:0] = B'100	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / **PWM2A** / CTS5#

Note: Bold text indicates the function used.

Table 3.2.30 SH7269 Multiplexed Pin Functions (PORT)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
PORT	PJ16	PJCR4	PJ16MD[2:0] = B'000	**PJ16**/DV_DATA16/LCD_DATA16/RSPCK0/TIOC0A/ SIOFSCK
	PJ17	PJCR4	PJ17MD[2:0] = B'000	**PJ17**/DV_DATA17/LCD_DATA17/SSL00/TIOC0B/ SIOFSYNC
	PJ18	PJCR4	PJ18MD[2:0] = B'000	**PJ18**/DV_DATA18/LCD_DATA18/MOSI0/TIOC0C/ SIOFTxD
	PJ19	PJCR4	PJ19MD[2:0] = B'000	**PJ19**/DV_DATA19/LCD_DATA19/MISO0/TIOC0D/ SIOFRxD/AUDIO_XOUT
	PJ0	PJCR0	PJ0MD[2:0] = B'000	**PJ0**/DV_DATA0/LCD_DATA0/SD_CD_1/PWM1A
	PJ1	PJCR0	PJ1MD[2:0] = B'000	**PJ1**/DV_DATA1/LCD_DATA1/SD_WP_1/PWM1B
	PJ2	PJCR0	PJ2MD[2:0] = B'000	**PJ2**/DV_DATA2/LCD_DATA2/SD_D1_1/PWM1C
	PJ3	PJCR0	PJ3MD[2:0] = B'000	**PJ3**/DV_DATA3/LCD_DATA3/SD_D0_1/PWM1D
	PJ4	PJCR1	PJ4MD[2:0] = B'000	**PJ4**/DV_DATA4/LCD_DATA4/SD_CLK_1/PWM1E
	PJ5	PJCR1	PJ5MD[2:0] = B'000	**PJ5**/DV_DATA5/LCD_DATA5/SD_CMD_1/PWM1F
	PJ6	PJCR1	PJ6MD[2:0] = B'000	**PJ6**/DV_DATA6/LCD_DATA6/SD_D3_1/PWM1G
	PJ7	PJCR1	PJ7MD[2:0] = B'000	**PJ7**/DV_DATA7/LCD_DATA7/SD_D2_1/PWM1H
	PJ12	PJCR3	PJ12MD[2:0] = B'000	**PJ12**/DV_DATA12/LCD_DATA12/PINT4/PWM2E/SCK7
	PJ13	PJCR3	PJ13MD[2:0] = B'000	**PJ13**/DV_DATA13/LCD_DATA13/PINT5/PWM2F/TxD5
	PJ14	PJCR3	PJ14MD[2:0] = B'000	**PJ14**/DV_DATA14/LCD_DATA14/PINT6/PWM2G/TxD6
	PJ15	PJCR3	PJ15MD[2:0] = B'000	**PJ15**/DV_DATA15/LCD_DATA15/PINT7/PWM2H/TxD7
	PJ27	PJCR6	PJ27MD[2:0] = B'000	**PJ27**/SGOUT_3/TIOC1A/CTS7#
	PE6	PECR1	PE6MD[1:0] = B'00	**PE6**/SCL3/RxD6
	PE7	PECR1	PE7MD[1:0] = B'00	**PE7**/SDA3/RxD7
	PE9	PECR2	PE8MD[2:0] = B'000	**PF9**/BS#/DV_DATA0/SCK0/MMC_D4/RTS1#

Note: Bold text indicates the function used.

3.3 LCD Module Interface

3.3.1 LCD Module Interface

The M3A-HS64G01 includes two flexible connectors and one MIL-spec connector for connecting LCD modules. The SH7269 on-chip Video Display Controller (VDC4) controls the LCD modules.

Figure 3.3.1 shows the LCD module interface block diagram.

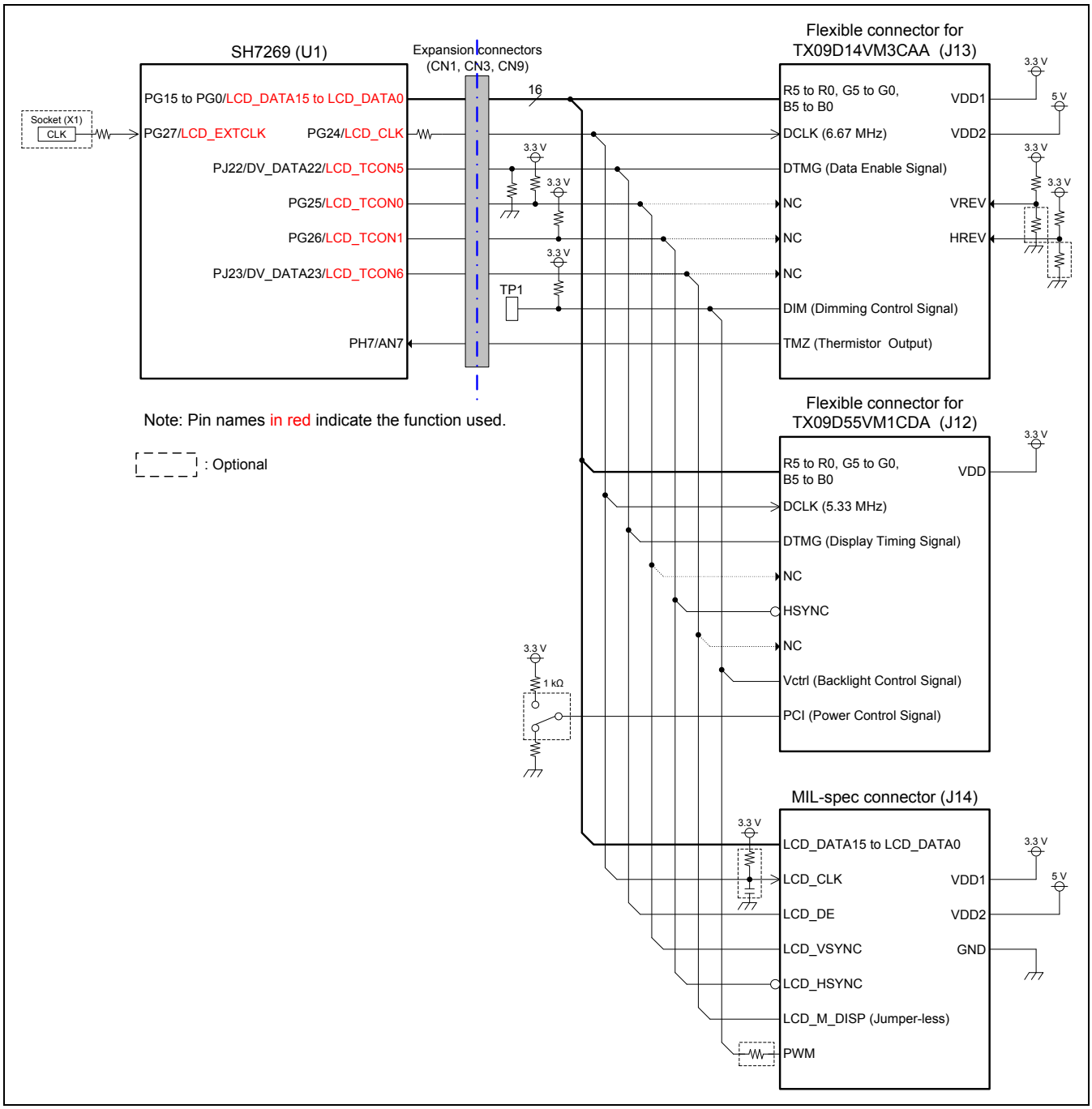

Figure 3.3.1 LCD Module Interface Block Diagram

3.3.2 Character LCD Module with LED Backlight

The M3A-HS64G01 includes a connector for 16 × 2 semi-transmissive character LCD module (SD1602H, Sunlike). The SH7269 general-purpose port output controls the character LCD modules. The M3A-HS64G01 is intended only for writing from the SH7269 to the character LCD modules. Therefore, the character LCD module R/W signal is fixed low.

The M3A-HS64G01 also includes a variable resistor (VR1) for the LCD driver voltage adjustment to control the LCD contrast and a variable resistor (VR2) for LCD backlight adjustment.

SH7269 PJ7 to PJ0 pins are multiplexed with VDC4 pins on the R0K572690C000BR, and the module to use is specified by SW6-3 on the R0K572690C000BR. On the M3A-HS64G01, PJ7 to PJ0 pins are multiplexed with the SDHI pins. Figure 3.3.2 shows the character LCD module block diagram. Table 3.3.1 lists the DIP switches setting (SW6-3). Table 3.3.2 lists the jumper setting (JP2).

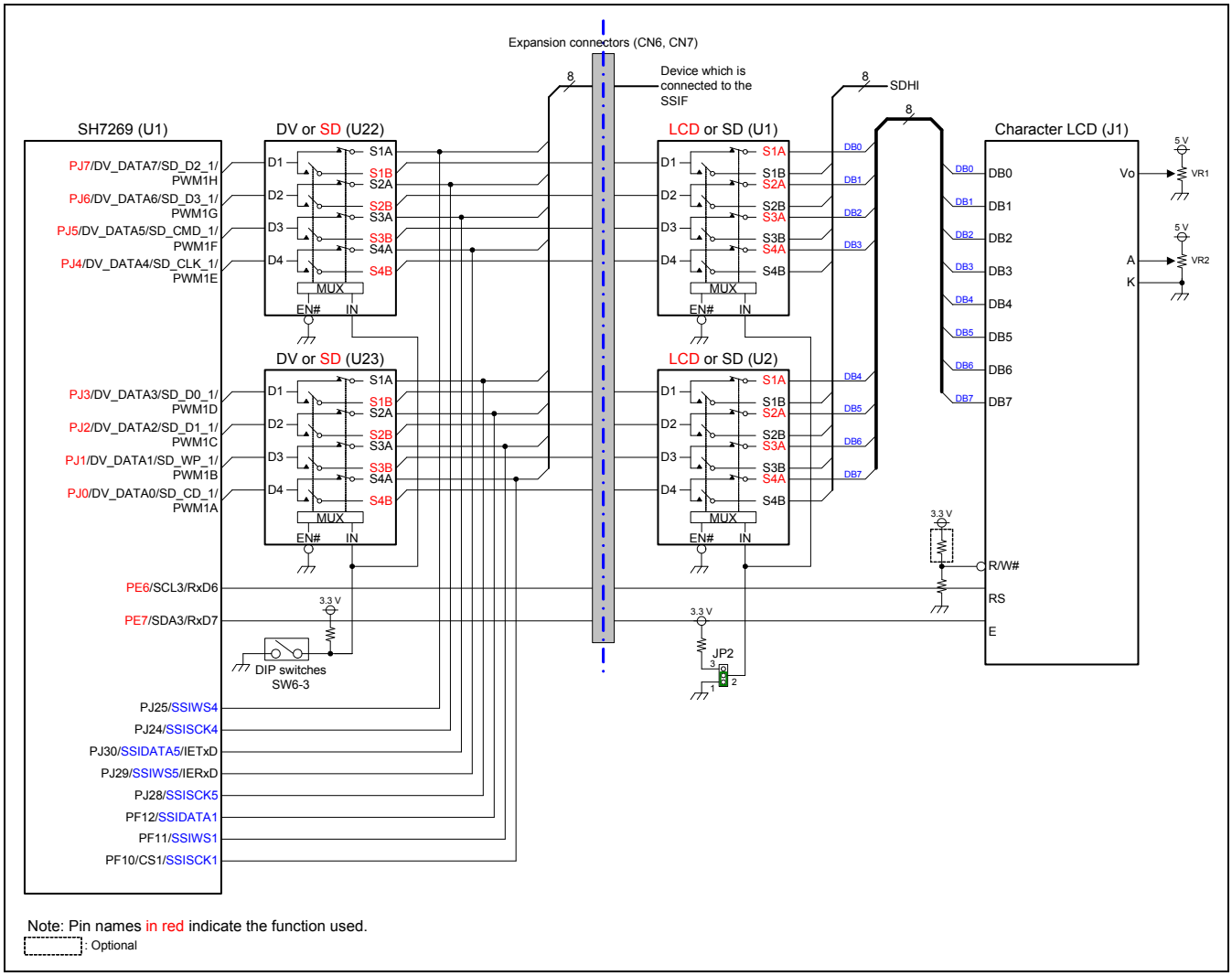

Figure 3.3.2 Character LCD Module Block Diagram

Table 3.3.1 R0K572690C000BR DIP Switches (SW6-3)

Number	Function	
	OFF (High)	ON (Low)
SW6-3	Connected to the SDHI/character LCD interface (default)	Connected to VDC4 (M3A-HS64G02)

Note: Shading indicates the function to be set.

Table 3.3.2 Jumper Setting (JP2)

Number	1-2 (Low)	2-3 (High)
JP2	Connected to the character LCD interface (default)	Connected to the SDHI

Note: Shading indicates the function to be set.

3.4 Audio Modules

The M3A-HS64G01 includes two 96 kHz 25-bit D/A Converters with DIT (AK4353, Asahi Kasei Microdevices Corporation), and a 24-bit stereo codec with IPGA (AK4524, Asahi Kasei Microdevices Corporation).

- AK4353 D/A Converter
  SH7269 IIC3, SSIF, and I/O ports control the AK4353.
  - SH7269 IIC3 (channel 1): Accesses the AK4353 registers to initialize AK4353, format data, and configure the attenuator
  - SH7269 SSIF (channels 1 and 5): Outputs the audio data
  - SH7269 I/O ports (PJ27): Powers down the AK4353 at low, powers up the AK4353 at high

Serial Sound Interface with FIFO (SSIF) channel 5 pins are multiplexed with IEBus™ Controller (IEB) pins. Figure 3.4.1 shows the D/A Converter block diagram. Table 3.4.1 lists the DIP switches setting (SW6-4).

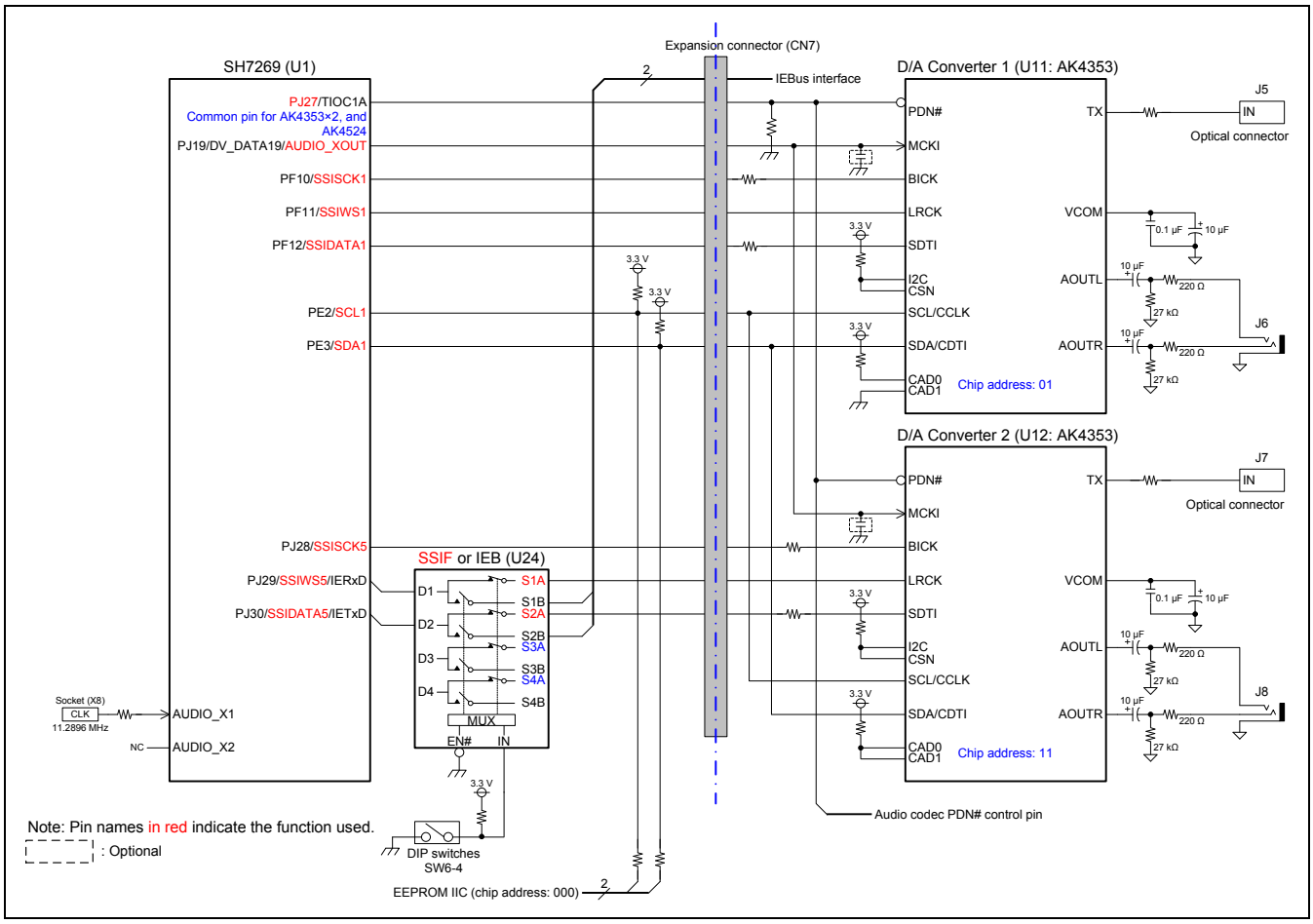

Figure 3.4.1 D/A Converter Block Diagram

Table 3.4.1 R0K572690C000BR DIP Switches Setting (SW6-4)

Number	Function	
	OFF (High)	ON (Low)
SW6-4	Connected to the IEBus™ interface	Connected to D/A Converter 2 (default)

Note: Shading indicates the function to be set.

- AK4524 Audio codec
  SH7269 RSPI, SSIF, and I/O ports control the AK4524.
  — SH7269 RSPI (channel 1): Accesses the AK4524 registers to initialize AK4524, and format data
  — SH7269 SSIF (channel 0): Inputs and outputs the audio data
  — SH7269 I/O ports (PJ27): Powers down the AK4524 at low, powers up the AK4524 at high

Renesas Serial Peripheral Interface (RSPI) channel 1 RSPCK 1 pin is multiplexed with the AUD AUDCK pin. Figure 3.4.2 shows the audio codec block diagram. Short the jumper (JP3) to use a plug-in power microphone.

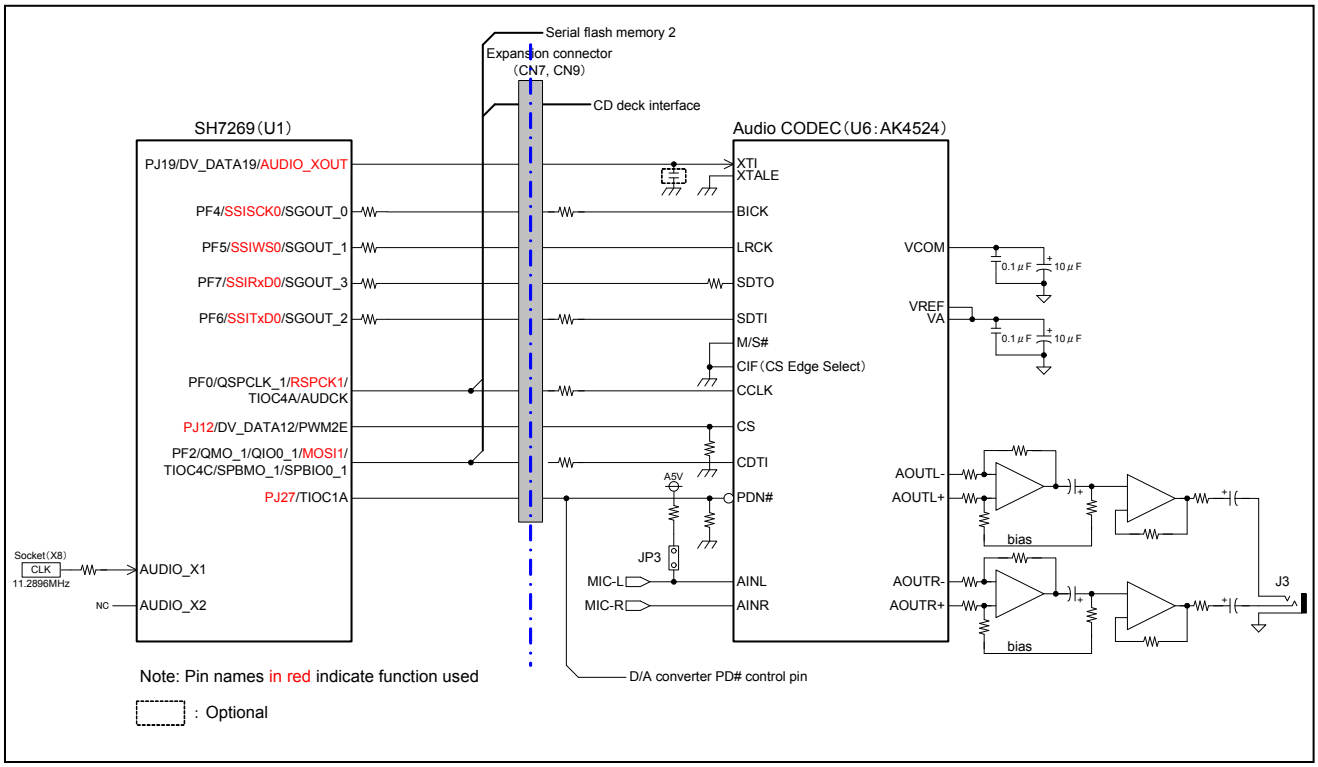

Figure 3.4.2 Audio CODEC Block Diagram

Table 3.4.2 Jumper Setting (JP3)

Number	1-2	None (Open)
JP3	Uses a plug-in power microphone	Uses a conventional microphone (default)

3.5 CD Deck Interface

The M3A-HS64G01 includes a CD deck interface connector. The SH7269 on-chip SSIF (Serial Sound Interface with FIFO) and RSPI (Renesas Peripheral Interface) control the CD deck.

RSPI channel 1 pins are multiplexed with serial flash memory 2 and audio codec pins, these devices cannot be controlled at the same time. RSPCK 1 pin is multiplexed with AUD AUDCK pin.

Figure 3.5.1 shows the CD deck interface block diagram. Table 3.5.1 lists the jumper setting (JP9).

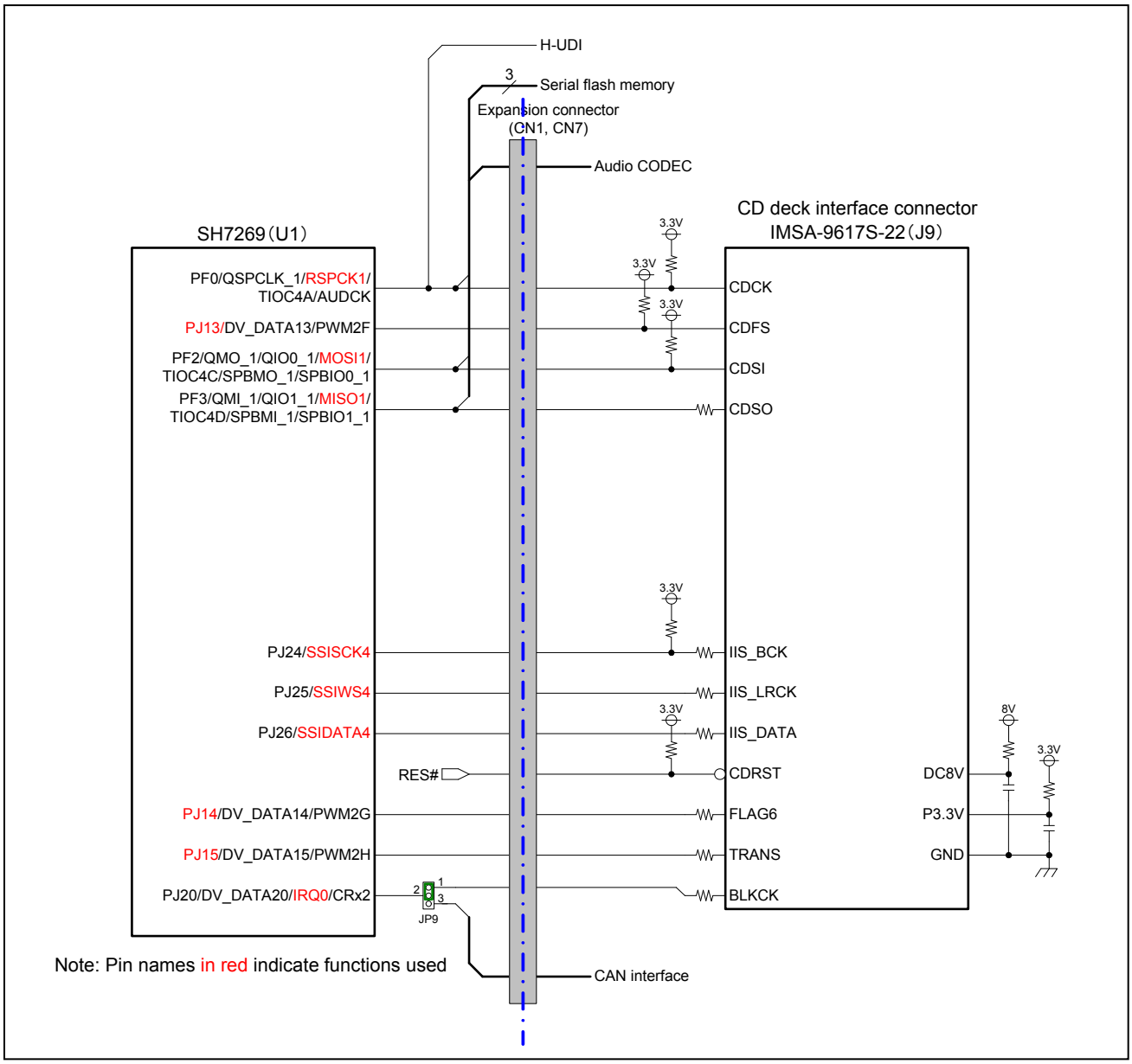

Figure 3.5.1 Serial Port Block Diagram

Table 3.5.1 R0K572690C000BR Jumper Setting (JP9)

Number	1-2	2-3
JP9	Uses PJ20 as IRQ0 input pin (default)	Uses PJ20 as CRx2 input/DV_DATA20 input pin

Note: Shading indicates the function to be set.

3.6 SD Card Interface

The M3A-HS64G01 includes an SD card slot. The SD card slot is connected to the SD Host Interface (SDHI) and the SH7269 SD card slot.

SDHI channel 1 pins are multiplexed with PJ7 to PJ0 pins to control the character LCD module. When using the SDHI, do not use the character LCD module.

Figure 3.6.1 shows the SD card interface block diagram. Table 3.6.1 lists the DIP switches setting (SW6-3). Table 3.6.2 lists the jumper setting (JP2)

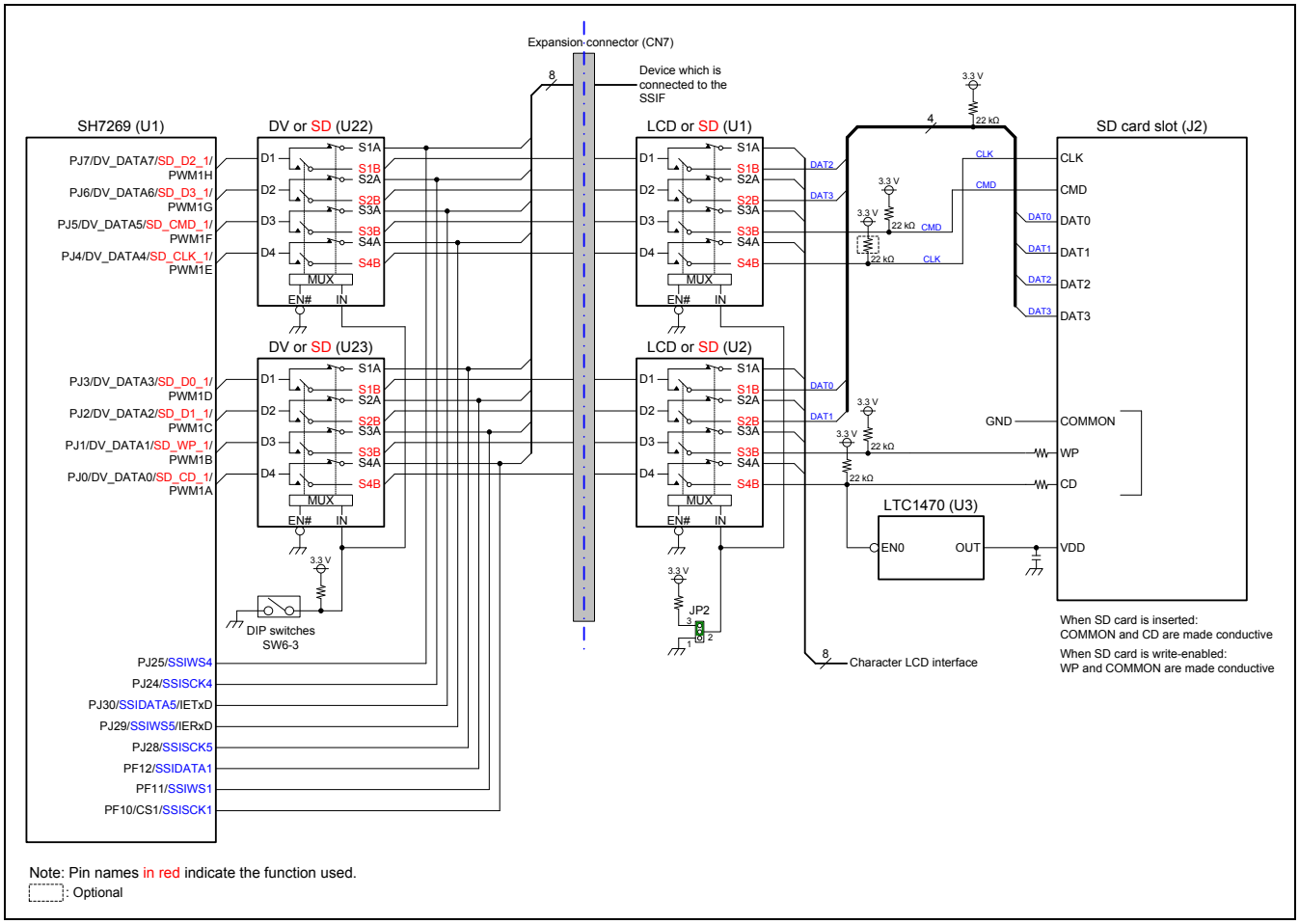

Figure 3.6.1 SD Card Interface Block Diagram

Table 3.6.1 DIP Switches Setting (SW6-3)

Number	Function	
	OFF (High)	ON (Low)
SW6-3	Connected to the SDHI/character LCD interface (default)	Connected to VDC4 (M3A-HS64G02)

Note: Shading indicates the function to be set.

Table 3.6.2 Jumper Setting (JP2)

Number	1-2 (Low)	2-3 (High)
JP2	Connected to the character LCD interface (default)	Connected to the SDHI

Note: Shading indicates the function to be set.

3.7 UART Interface

The SH7269 includes a Serial Communication Interface with FIFO (SCIF). SCIF channel 5 pin is connected to the UART connector (7-pin, 2.5 mm pitch) on the M3A-HS64G01 at TTL level.

SCIF channel 5 RxD5 pin is multiplexed with VDC4 LCD_DATA22 pin and AUD AUDSYNC# pin. SCIF channel TxD5 pin is multiplexed with VDC4 LCD_DATA23 pin and AUD AUDATA3 pin.

Figure 3.7.1 shows the UART interface block diagram.

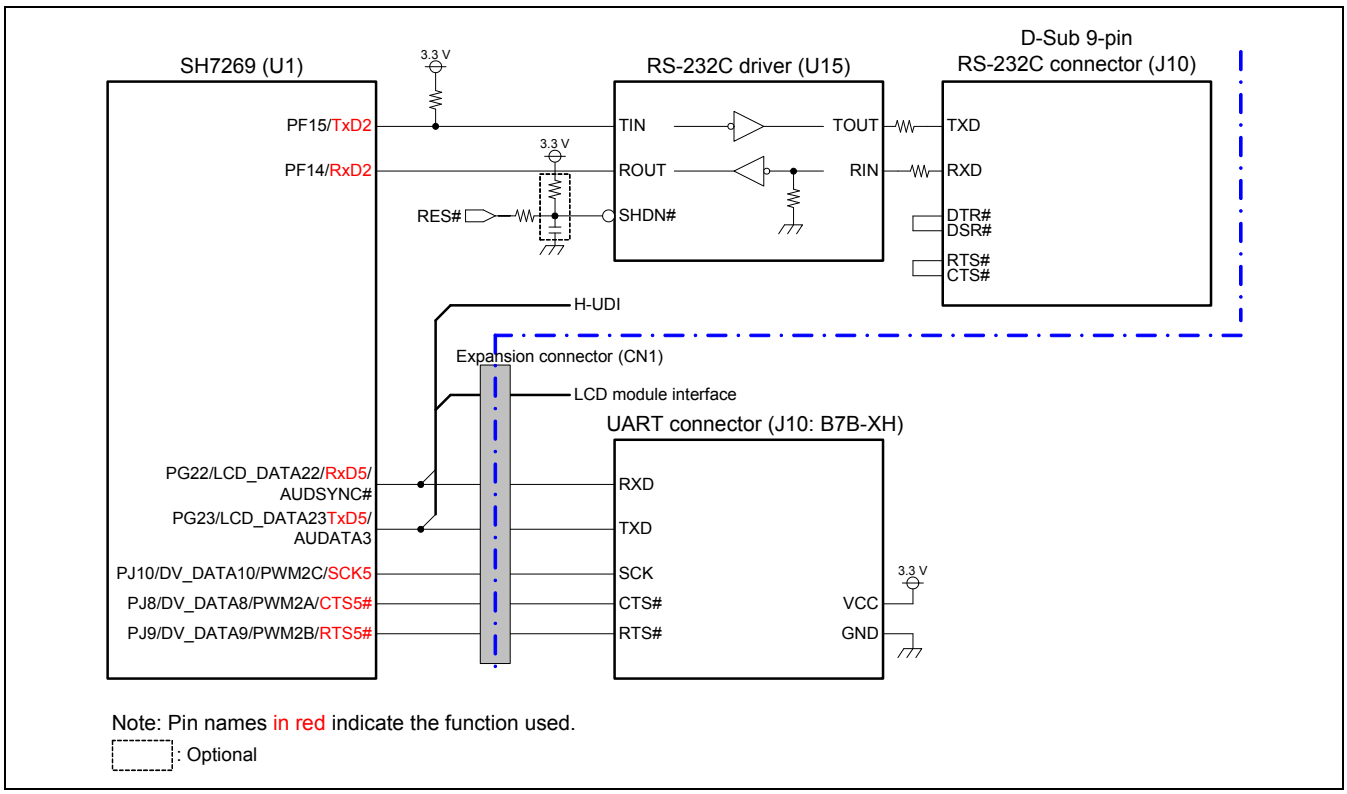

Figure 3.7.1 UART Interface Block Diagram

3.8 CAN Interface

The SH7269 includes RCAN-TL1 (Renesas CAN Time Trigger Level 1), the Controller Area Network. Two channels of the SH7269 RCAN-TL1 are connected to the CAN connector (3-pin, 2.5 mm pitch) on the M3A-HS64G01 via the voltage level shifter and the CAN driver IC. Note that only RCAN-TL1 channel 2 can be used on the R0K572690C000BR.

RCAN-TL1 channel 2 pins are multiplexed with IRQ input pins and Video Display Controller 4 (VDC4) pins.

Figure 3.8.1 shows the CAN interface block diagram. Table 3.8.1 lists jumper settings (JP8 and JP9). Table 3.8.2 and Table 3.8.3 list jumper settings (JP4, JP5, JP8, and JP9).

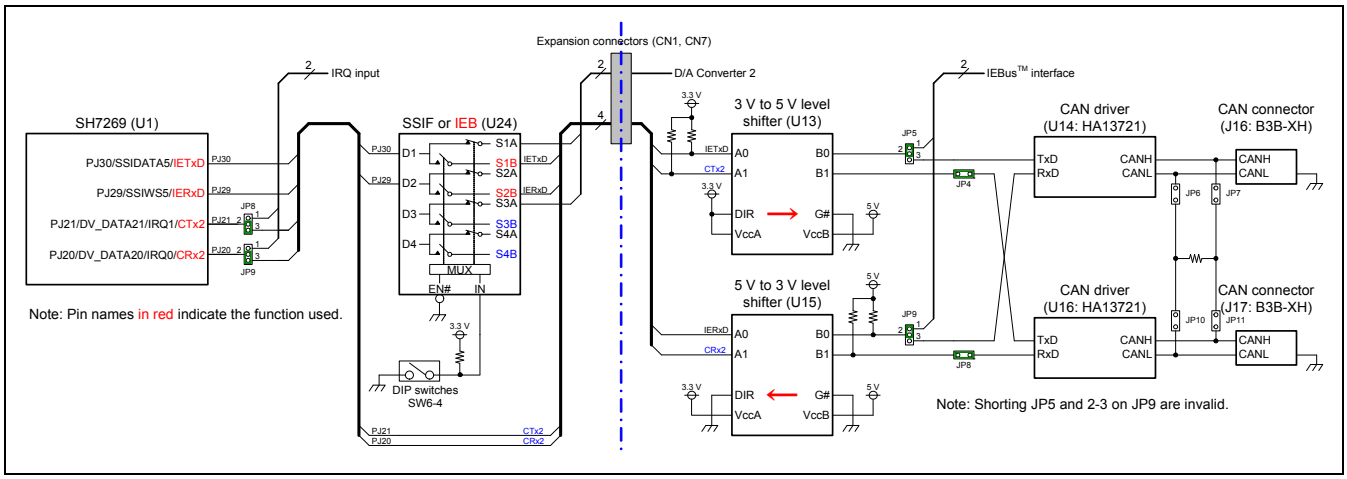

Figure 3.8.1 CAN Interface Block Diagram

Table 3.8.1 R0K572690C000BR Jumper Settings (JP8, JP9)

Number	1-2	2-3
JP8	Uses PJ21 as IRQ1 input pin (default)	Uses PJ21 as CTx2 output/DV_DATA21 input pin
JP9	Uses PJ20 as IRQ0 input pin (default)	Uses PJ20 as CRx2 input/DV_DATA20 input pin

Note: Shading indicates the function to be set.

Table 3.8.2 Jumper Settings (JP5, JP9)

Number	1-2	2-3
JP5	Selects IETxD (IEB)	Selects PJ30 (RCAN-TL1) pin (default) (1)
JP9	Selects IERxD (IEB)	Selects PJ29 (RCAN-TL1) pin (default) (1)

Notes: 1. This setting is invalid on the R0K572690C000BR.
2. Shading indicates the function to be set.

Table 3.8.3 Jumper Settings (JP4, JP8)

Number	1-2	None (Open)
JP4	Normal mode (Connects CTx1 pin) (default)	Debug mode (Leaves CTx1 pin disconnected)
JP8	Normal mode (Connects CRx1 pin) (default)	Debug mode (Leaves CRx1 pin disconnected)

Note: Shading indicates the function to be set.

3.9 IEBus™ Interface

The SH7269 includes and IEBus™ Controller (IEB). The IEBus™ (Inter Equipment Bus™) is the bus for digital data transfer system on a small scale. The SH7269 IEB pin is connected to the IEBus connector (4-pin, 2.5 mm pitch) via the voltage level shifter and the IEBus™ driver IC on the M3A-HS64G01.

The IEB pin is multiplexed with SCIF channel 0 pin and RCAN-TL1 channel 0 pin.

Figure 3.9.1 shows the IEBus™ interface block diagram. Table 3.9.1 lists the DIP switches settings (SW6-4). Table 3.9.2 lists jumper settings (JP5 and JP9).

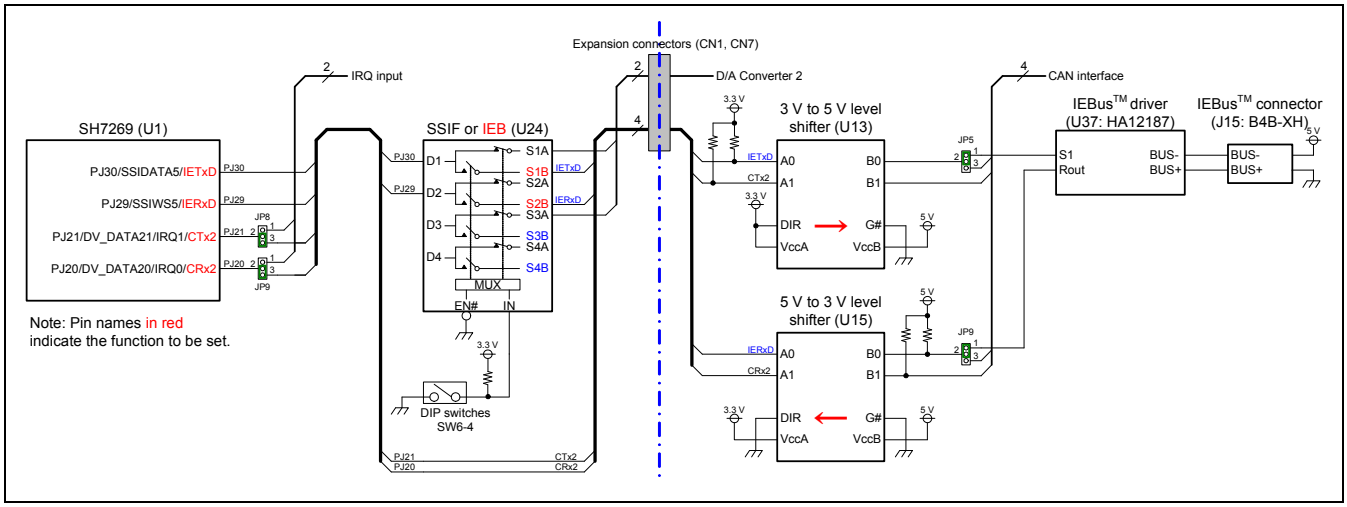

Figure 3.9.1 IEBus™ Interface Block Diagram

Table 3.9.1 R0K572690C000BR DIP Switches Setting (SW6-4)

Number	Function	
	OFF (High)	ON (Low)
SW6-4	Connected to the IEBus™ Interface	Connected to D/A Converter 2 (default)

Note: Shading indicates the function to be set.

Table 3.9.2 Jumper Settings (JP5, JP9)

Number	1-2	2-3
JP5	Selects IETxD (IEB)	Selects PJ30 (RCAN-TL1) pin (default) (1)
JP9	Selects IERxD (IEB)	Selects PJ29 (RCAN-TL1) pin (default) (1)

Notes: 1. This setting is invalid on the R0K572690C000BR.
2. Shading indicates the function to be set.

3.10 I/O Ports

The SH7269 I/O ports are connected to switches and LEDs on the M3A-HS64G01.

To use ports PH0 to PH3 as key input switches (4 switches × 4 inputs) via an A/D Converter (ADC), set the ports as analog input pins (AN0 to AN3).

PJ16 and PJ17 can be used as the user setting switches input. PJ18 and PJ19 can be used as the user LED control output.

Figure 3.10.1 shows the I/O ports block diagram.

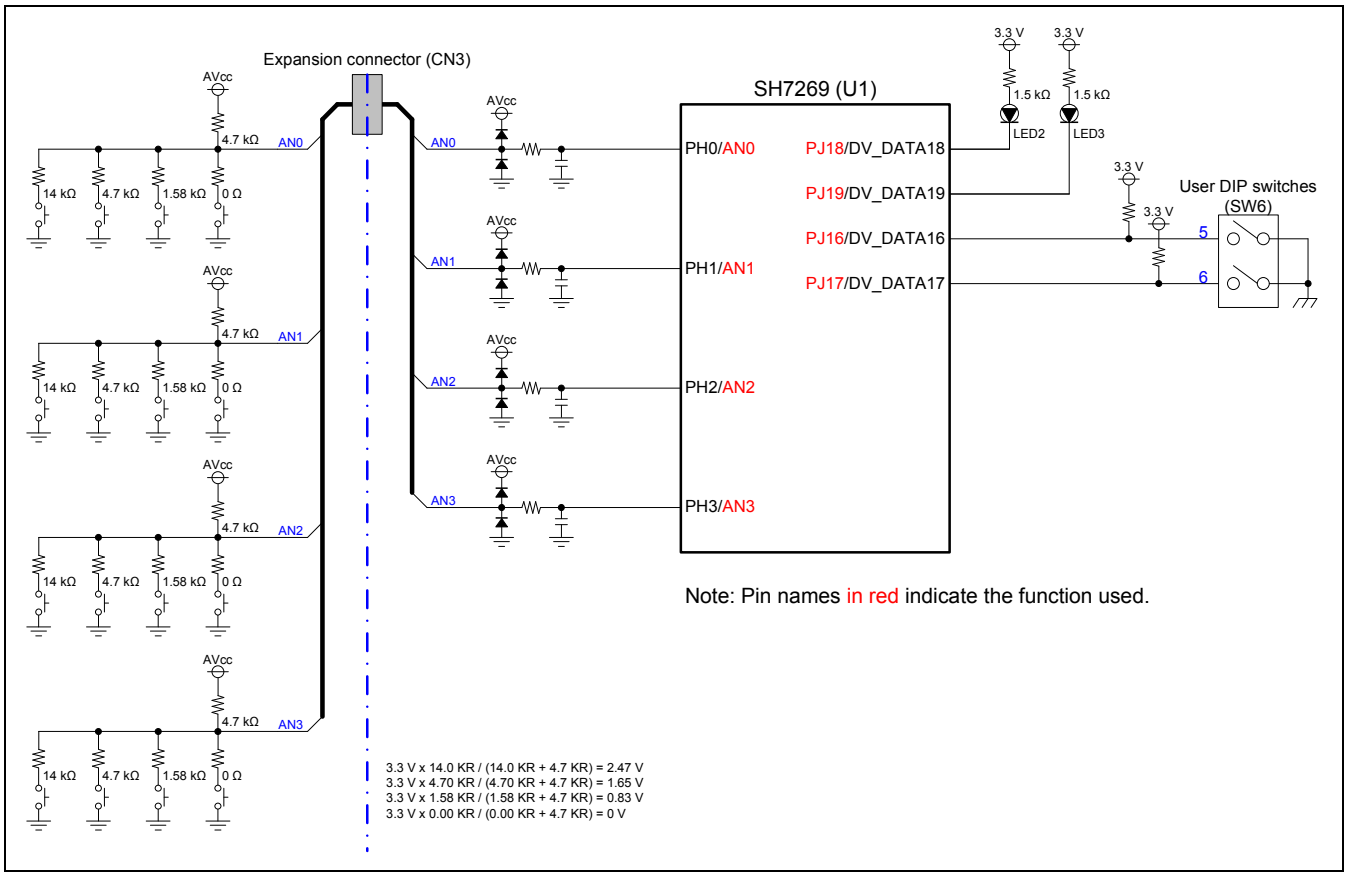

Figure 3.10.1 I/O Ports Block Diagram

3.11 Clock Modules

Provide following clocks with the SH7269 on the R0K572690C000BR.

- SH7269 input clock (X4): 13.33MHz
- SH7269 RTC clock (X5): 32.768kHz
- SH7269 audio clock (X8): 11.2896MHz
- SH7269 USB clock (X6): 48.00MHz
- SH7269 LCD clock (X1): Optional
- SH7269 digital video decoder clock (X2): 27.00MHz

Figure 3.11.1 shows the clock module block diagram of the R0K572690C000BR and M3A-HS64G01.

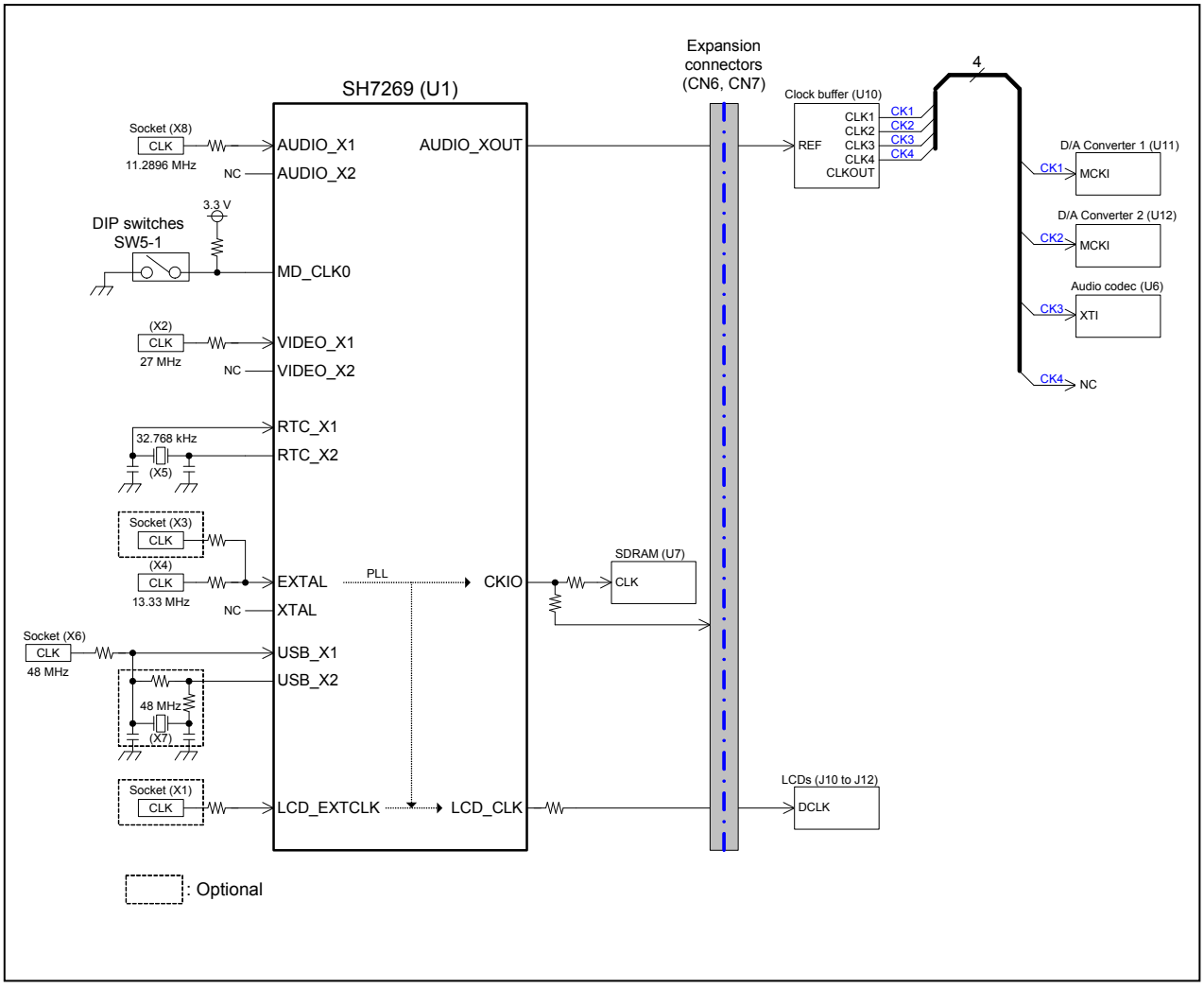

Figure 3.11.1 R0K572690C000BR and M3A-HS64G01 Clock Module Block Diagram

3.12 Reset Module

A reset IC controls reset signals connected to the SH7269, flash memory and peripheral I/Os on the R0K572690C000BR and M3A-HS64G01. There are two system reset options; power-on reset, and reset by switch.

Figure 3.12.1 shows the reset module block diagram.

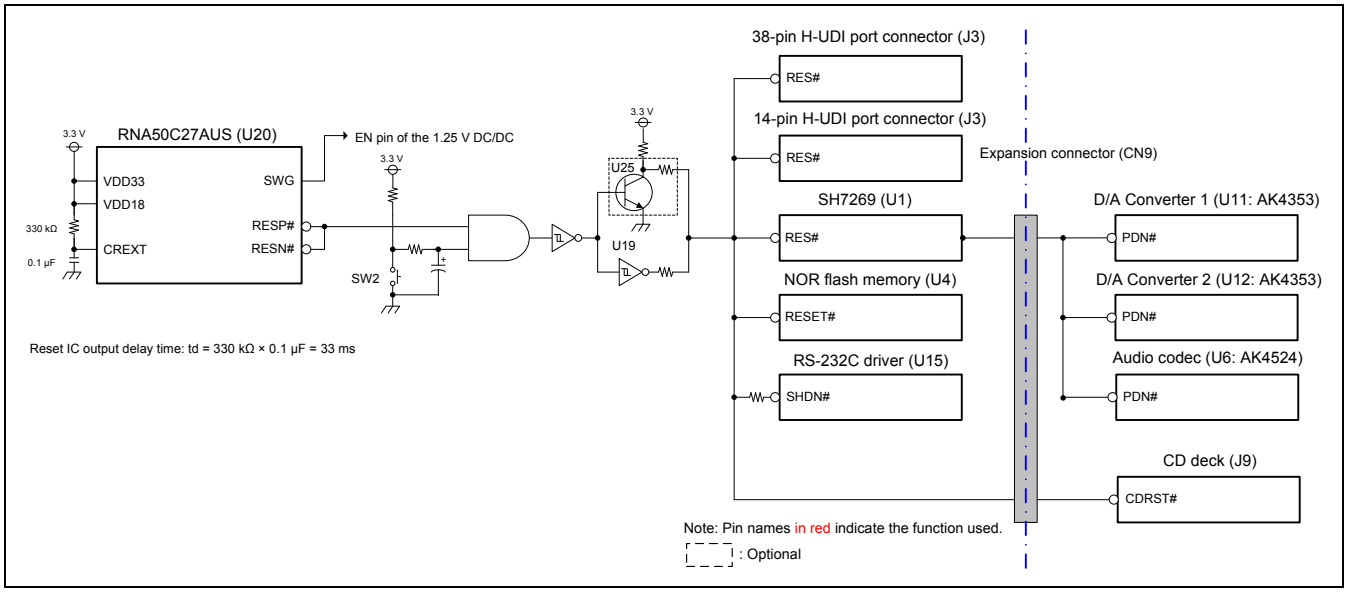

Figure 3.12.1 Reset Module Block Diagram

3.13 Power Supply Module

A 12V power supply is input to the M3A-HS64G01, and the voltage regulator on the M3A-HS64G01 generates 8V voltage, and 5V voltage. 5V voltage is provided to the R0K572690C000BR, and the voltage regulator on the R0K572690C000BR generates 3.3 V and 1.25V.

Figure 3.13.1 shows the power supply module block diagram.

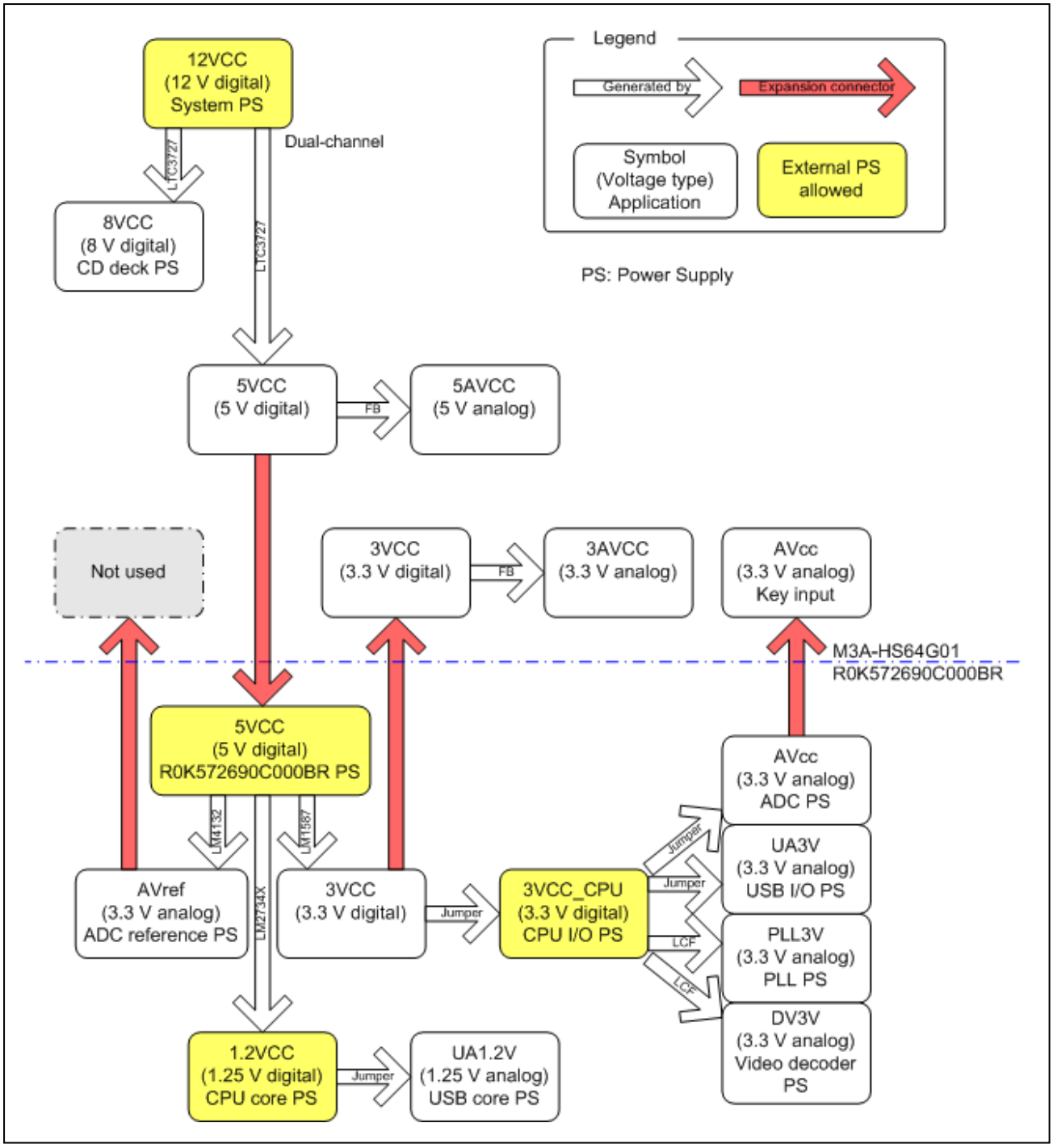

Figure 3.13.1 Power Supply Module Block Diagram

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4. M3A-HS64G02 Functions

4.1 Overview of Functions

The M3A-HS64G02 includes the function modules listed in the following table.

Table 4.1.1 M3A-HS64G02 Function Modules

Section	Function	Description
4.2	CPU	SH7269
4.3	LCD Module Interface	• LCD module interface — Connects the SH7269 Video Display Controller 4 (VDC4) and LCD module connectors — Includes flexible connectors for LCD module • Character LCD module with LED backlight
4.4	Audio Module	• Connects the SH7269 and D/A Converter — 96kHz 24-bit D/A Converter: 1
4.5	Video Signal Input Module	• Connects the SH7269 Video Display Controller (VDC3) and a video decoder IC
4.6	SD Card Interface	• Connects the SH7269 SD Host Interface (SDHI) and an SD card slot
4.7	UART Interface	• Connects the SH7269 Serial Communication Interface with FIFO (SCIF) and a UART connector
4.8	CAN Interface	• Connects the SH7269 Controller Area Network (RCAN-TL1) and a CAN connector Note: One CAN channel can be used on the R0K572690C000BR.
4.9	IEBus™ Interface	• Connects the SH7269 IEBus™ controller (IEB) and IEBus™ connector
4.10	PWM Interface	• Connects the SH7269 Motor Control PWM Timer (PWM) and a 20-pin MIL spec connector Note: One PWM channel can be used on the R0K572690C000BR
4.11	MTU2 Interface	• Connects the SH7269 Multi Function Timer Pulse Unit 2 (MTU2) and a 20-pin MIL-spec connector
4.12	I/O Ports	• Connect the SH7269 I/O ports, LEDs and DIP switches
4.13	Interrupt Switches	• Connects the SH7269 IRQ2 pin, IRQ3 pin, and push-button switches
4.14	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
4.15	Reset Module	• Resets devices on the M3A-HS64G02
4.16	Power Supply Module	• Controls the M3A-HS64G02 system power supply
–	Operating Specifications	• Connectors, switches and LEDs Refer to Chapter 7 for details.

4.2 CPU

4.2.1 SH7269 Overview

The R0K572690C000BR includes the SH7269, the 32-bit RISC MCU that operates with a maximum frequency of 266.67 MHz.

4.2.2 SH7269 Pin Functions Used on the M3A-HS64G02

Table 4.2.1 to Table 4.2.11 list the SH7269 pin functions used on the M3A-HS64G02.

Table 4.2.1 SH7269 Pin Functions (1/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
1	PC1/RD#	RD#	Connected to NOR flash memory OE# pin	CN6, pin 6	
2	PVcc				
3	PC2/RD/WR#/SCK6	RD/WR#	Connected to SDRAM WE# pin	CN6, pin 7	
4	PC3/WE0#/DQMLL/RxD6	WE0#	Connected to NOR flash memory WE# pin	CN6, pin 8	
		DQMLL	Connected to SDRAM DQML pin		
5	PC4/WE1#/WE#/DQMLU/TxD6	DQMLU	Connected to SDRAM DQMU pin	CN6, pin 9	
6	PC5/RAS#/CRx0 / CRx0/CRx1/CRx2/IRQ0	RAS#	Connected to SDRAM RAS# pin	–	SW6-1: OFF
		–	–	CN6, pin 14	SW6-1: ON
7	PVcc				
8	PC6/CAS#/SCK7/CTx0/ CTx0&CTx1&CTx2	CAS#	Connected to SDRAM CAS# pin	–	SW6-1: OFF
		–	–	CN6, pin 15	SW6-1: ON
9	Vss				
10	PC7/CKE/RxD7/CRx1/ CRx0/CRx1/IRQ1	CKE	Connected to SDRAM CKE pin	–	SW6-1: OFF
		–	–	CN6, pin 16	SW6-1: ON
11	Vcc				
12	PC8/CS3#/TxD7/CTx1/ CTx0&CTx1	CS3#	Connected to SDRAM CS# pin	–	SW6-1: OFF
		–	–	CN6, pin 17	SW6-1: ON
13	PB1/A1/TIOC0A	A1	Address bus	CN4, pin 28	
14	PB2/A2/TIOC0B	A2	Address bus	CN4, pin 27	
15	PB3/A3/TIOC0C	A3	Address bus	CN4, pin 26	
16	PJ14/DV_DATA14 / LCD_DATA14/PINT6/ PWM2G/TxD6	PWM2G	PWM output	CN11, pin A1	TTL level
		DV_DATA14	DV input		
		–	–	CN1, pin 4	
17	PVcc				
18	PJ15/DV_DATA15/ LCD_DATA15/PINT7/ PWM2H/TxD7	PWM2H	PWM output	CN11, pin B1	TTL level
		DV_DATA15	DV input		
		–	Connected to the PWM connector (J5)	CN1, pin 2	
19	Vss				
20	PB4/A4/TIOC0D	A4	Address bus	CN4, pin 25	
21	Vcc				
22	PJ16/DV_DATA16/ LCD_DATA16/RSPCK0/ TIOC0A/SIOFSCK	PJ16	Connected to SW6-5 as user input port 1	CN11, pin B13	
		DV_DATA16	DV input		
23	PJ17/DV_DATA17/ LCD_DATA17/SSL/00/ TIOC0B/SIOFSYNC	PJ17	Connected to SW6-6 as user input port 2	CN11, pin B12	
		DV_DATA17	DV input		
24	PJ18/DV_DATA18/ LCD_DATA18/MOSI0/ TIOC0C/SIOFTxD	PJ18	Connected to LED2 as user output port 1	CN11, pin B8	
		DV_DATA18	DV input		

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.2 SH7 269 Pin Functions (2/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
25	PB5/A5/TIOC1A	A5	Address bus	CN4, pin 22	
26	PB6/A6/TIOC1B	A6	Address bus	CN4, pin 21	
27	PVcc				
28	PB7/A7/TIOC2A	A7	Address bus	CN4, pin 20	
29	Vss				
30	PB8/A8/TIOC2B	A8	Address bus	CN4, pin 19	
31	Vcc				
32	PB9/A9/TIOC3A	A9	Address bus	CN4, pin 18	
33	PB10/A10/TIOC3B	A10	Address bus	CN4, pin 17	
34	PB11/A11/TIOC3C	A11	Address bus	CN4, pin 14	
35	PB12/A12/TIOC3D	A12	Address bus	CN4, pin 13	
36	PJ19/DV_DATA19/ LCD_DATA19/MISO0/ TIOC0D/SIOFRxD/ AUDIO_XOUT	PJ19	Connected to LED3 as user output port 2	CN11, pin A12	
		DV_DATA19	DV input		
		AUDIO_XOUT	Connected to DAC (U10) MCKI pin	CN7, pin 40	
37	PVcc				
38	PJ20/DV_DATA20/ LCD_DATA20/LCD_TCON3/ IRQ0/CRx2/CRx0/CRx1/CRx2	–	–	CN7, pin 8	JP9: 1-2
		DV_DATA20	DV input	CN11, pin B4	JP9: 2-3
		CRx2	Connected to the CAN driver IC (U15)	CN1, pin 17	
39	Vss				
40	PB13/A13/QIO2_1 / SPBIO2_1	A13	Address bus	CN4, pin 12	
		QIO2_1 / SPBIO2_1	Connected to serial flash memory 2 IO2 pin		
41	Vcc				
42	PJ21/DV_DATA21 LCD_DATA21/LCD_TCON4/ IRQ1/CTx2/CTx0&CTx1&CTx2	IRQ1	IRQ1 switch	–	JP8: 1-2
		DV_DATA21	DV input	CN11, pin A14	JP8: 2-3
		CTx2	Connected to the CAN driver IC (U15)	CN1, pin 18	
43	PJ22/DV_DATA22/ LCD_DATA22/LCD_TCON5/ IRQ2/CRx1/CRx0/CRx1	DV_DATA22	DV input	CN11, pin B14	
		LCD_TCON5	Connected to LCD module DE pin	CN9, pin 24 CN10, pin B17	
44	PJ23/DV_DATA23/ LCD_DATA23/LCD_TCON6/ IRQ3/CTx1/CTx0&CTx1	DV_DATA23	DV input	CN11, pin A15	
		LCD_TCON6	Connected to the LCD module M_DISP pin	CN1, pin 18 CN10, pin B18	
45	PB14/A14/QIO3_1 / SPBIO3_1	A14	Address bus	CN4, pin 11	
		QIO3_1 / SPBIO3_1	Connected to serial flash memory 2 IO3 pin		
46	PB15/A15/QIO2_0 / SPBIO2_0	A15	Address bus	CN4, pin 10	
		QIO2_0 / SPBIO2_0	Connected to serial flash memory 1 IO2 pin		
47	PVcc				
48	PB16/A16/QIO3_0 / SPBIO3_0	A16	Address bus	CN4, pin 9	
		QIO3_0 / SPBIO3_0	Connected to serial flash memory 1 IO3 pin		
49	Vss				

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.3 SH7269 Pin Functions (3/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
50	PB17/A17/QSPCLK_0/ RSPCK0 / SPBCLK	A17	Address bus	CN4, pin 6	
		QSPCLK_0/ RSPCK0 / SPBCLK	Connected to serial flash memory 1 SCK pin		
51	Vcc				
52	PB18/A18/QSSL_0/SSL00 / SPBSSL	A18	Address bus	CN4, pin 5	JP4: Open
		QSSL_0/ SSL00 / SPBSSL	Connected to serial flash memory 1 CS pin	–	JP4: 1-2
53	PB19/A19/QMO_0/QIO0_0/ MOSI0 / SPBMO_0/SPBIO0_0	A19	Address bus	CN4, pin 4	
		QMO_0/QIO0_0/ MOSI0 / SPBMO_0/SPBIO0_0	Connected to serial flash memory 1 SI pin		
54	PB20/A20/QMI_0/QIO1_0/ MISO0 / SPBMI_0/SPBIO1_	A20	Address bus	CN4, pin 3	
		QMI_0/QIO1_0/ MISO0 / SPBMI_0/SPBIO1_	Connected to serial flash memory 1 SO pin		
55	Vss				
56	PB21/A21/CRx2/IERxD	A21	Address bus	CN4, pin 2	
57	Vcc				
58	PB22/A22/CTx2/IETxD/CS4#	A22	Address bus	CN4, pin 1	
59	PC0/CS0#/MD_BOOT2	CS0#	Connected to NOR flash memory CE# pin	CN6, pin 5	JP5: 1-2
		MD_BOOT2	Connected to SW5-4 as boot mode input 2		JP5: 2-3
60	PVcc				
61	CKIO	CKIO	Connected to SDRAM CLK pin	CN6, pin 20	
62	Vss				
63	PA0/MD_BOOT0	MD_BOOT0	Connected to SW5-2 as boot mode input 0	CN1, pin 10	RES#: low
64	Vcc				
65	PA1/MD_BOOT1	MD_BOOT1	Connected to SW5-3 as boot mode input 1	CN1, pin 9	RES#: low
66	PJ28/SSISCK5/TIOC1B/ RTS7#	–	–	CN7, pin 22	
67	PJ29/SSIWS5/TIOC2A/ IERxD	–	–	CN7, pin 24	SW6-4: ON
		IERxD	Connected to the IEBus driver IC	CN1, pin 19	SW6-4: OFF
68	PJ30/SSIDATA5/TIOC2B/ IETxD	–	–	CN7, pin 23	SW6-4: ON
		IETxD	Connected to the IEBus driver IC	CN1, pin 20	SW6-4: OFF
69	PJ31/DV_CLK	DV_CLK	DV input	CN11, pin B16	
			Connected to the Video decoder IC CLK_27MO pin	CN7, pin 27	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.4 SH7269 Pin Functions (4/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
70	PE0/SCL0/TCLKA/ LCD_EXTCLK	SCL0	Connected to the External IIC connector (J3)	CN7, pin 5	
			Connected to the Video decoder IC SCL pin		
71	PE1/SDA0/TCLKB/ AUDIO_CLK/DV_CLK	SDA0	Connected to the External IIC connector (J3)	CN7, pin 8	
			Connected to the Video decoder IC SDA pin		
72	PE2/SCL1/TCLKC/IOIS16#/ DV_VSYNC	SCL1	Connected to EEPROM SCL pin	CN7, pin 7	
			Connected to DAC SCL/CCLK pin		JP1: 1-2
		PE2	Connected to IRQ2 switch		JP2: 2-3
73	PE3/SDA1/TCLKD/ADTRG#/DV_HSYNC	SDA1	Connected to EEPROM SDA pin	CN7, pin 10	
			Connected to DAC SDA/CDTI pin		JP2: 1-2
		PE3	Connected to IRQ3 switch		JP2: 2-3
74	PE4/SCL2/RxD4/ DV_VSYNC	DV_VSYNC	DV input	CN11, pin A17	
			Connected to the Video decoder IC VSYNC pin	CN7, pin 9	
75	PE5/SDA2/RxD5/ DV_HSYNC	DV_HSYNC	DV input	CN11, pin B17	
			Connected to the Video decoder IC HSYNC pin	CN7, pin 12	
76	PE6/SCL3/RxD6	PE6	Connected to the character LCD RS pin	CN6, pin 12	
77	PE7/SDA3/RxD7	PE7	Connected to the character LCD E pin	CN6, pin 13	
78	PVcc				
79	NMI	NMI	Non-maskable interrupt	–	
80	Vss				
81	ASEMD#	ASEMD#	ASE mode select	–	H-UDI
82	Vcc				
83	PLLVcc				
84	EXTAL	EXTAL	Connects the system external clock to MCU	–	13.33MHz
85	XTAL	XTAL	Open	–	
86	PLLVss				
87	PLLVss				
88	RES#	RES#	Reset input	CN7, pin 6	
89	RTC_X1	RTC_X1	Connects the real time clock resonator to MCU	–	32.768 kHz
90	RTC_X2	RTC_X2		–	
91	USBDPVcc				
92	USBDPVss				
93	DM	DM	USB differential D− data	–	
94	DP	DP	USB differential D+ data	–	
95	VBUS	VBUS	VBUS input	–	
96	USBDVcc				
97	USBDVss				
98	REFRIN	REFRIN	Reference input	–	Connects a 5.6 kΩ±1% resistor
99	USBAVss				
100	USBAPVcc				
101	USBAVcc				
102	USBAVss				
103	USBUVcc				

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.5 SH7269 Pin Functions (5/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
104	USBUVss				
105	USB_X1	USB_X1	Connects the USB external clock to MCU	–	48 MHz
106	USB_X2	USB_X2	Open	–	
107	PVcc				
108	VIDEO_X1	VIDEO_X1	Connects the digital video decoder external clock to MCU	–	27 MHz
109	VIDEO_X2	VIDEO_X2	Open	–	
110	Vss				
111	DVAVcc				
112	DVAVss				
113	VIN1	VIN1	Analog video signal input	CN10, pin A19	
114	VIN2	VIN2	Analog video signal input	CN10, pin B20	
115	VRT	VRT	Top reference voltage	–	
116	VRB	VRB	Bottom reference voltage	–	
117	BIAS	BIAS	Reference voltage	–	Connects a 24 kΩ±1% resistor
118	PH0/AN0/PINT0	–	–	CN3, pin 4	
119	PH1/AN1/PINT1	–	–	CN3, pin 3	
120	PH2/AN2/PINT2	–	–	CN3, pin 8	
121	PH3/AN3/PINT3	–	–	CN3, pin 7	
122	PH4/AN4/PINT4	–	–	CN3, pin 12 CN11, pin B18	
123	PH5/AN5/PINT5/ LCD_EXTCLK	–	–	CN3, pin 11 CN11, pin A19	
124	AVss				
125	PH6/AN6/PINT6	–	–	CN3, pin 16 CN11, pin B19	
126	AVcc				
127	PH7/AN7/PINT7	–	–	CN3, pin 15 CN11, pin A20	
128	AVref				
129	TRST#	TRST#	Initialization signal input pin	–	H-UDI
130	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Break mode acknowledge	–	H-UDI
		ASEBRK#	Break request		
131	TDO	TDO	Test data output	–	H-UDI
132	TDI	TDI	Test data input	–	H-UDI
133	TMS	TMS	Test mode select	–	H-UDI
134	TCK	TCK	Test clock	–	H-UDI
135	Vss				
136	PG0/D16/LCD_DATA0/ IRQ0/TIOC0A	LCD_DATA 0	Connected to LCD module D0 pin	CN9, pin 2 CN10, pin A1	B0
137	Vcc				
138	PG1/D17/LCD_DATA1/ IRQ1/TIOC0B	LDC_DATA 1	Connected to LCD module D1 pin	CN9, pin 1 CN10, pin B1	B1
139	Vss				
140	PG2/D18/LCD_DATA2/ IRQ2/TIOC0C	LCD_DATA 2	Connected to LCD module D2 pin	CN9, pin 4 CN10, pin A2	B2

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.6 SH7269 Pin Functions (6/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
141	PVcc				
142	AUDIO_X2	AUDIO_X2	Open	–	
143	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	–	11.2896 MHz
144	Vss				
145	PG3/D19/LCD_DATA3/ IRQ3/TIOC0D	LCD_DATA3	Connected to LCD module D3 pin	CN9, pin 3 CN10, pin B2	B3
146	Vcc				
147	PG4/D20/LCD_DATA4/ IRQ4/TIOC1A	LCD_DATA4	Connected to LCD module D4 pin	CN9, pin 6 CN10, pin B3	B4
148	PG5/D21/LCD_DATA5/ IRQ5/TIOC1B	LCD_DATA5	Connected to LCD module D5 pin	CN9, pin 8 CN10, pin A4	B5
149	PG6/D22/LCD_DATA6/ IRQ6/TIOC2A	LCD_DATA6	Connected to LCD module D6 pin	CN9, pin 7 CN10, pin B4	B6
150	PG7/D23/LCD_DATA7/ IRQ7/TIOC2B	LCD_DATA7	Connected to LCD module D7 pin	CN9, pin 9 CN10, pin B4	B7
151	PJ0/DV_DATA0/ LCD_DATA0/SD_CD_1/ PWM1A	PJ0	Connected to the character LCD DB7 pin	CN7, pin 15	SW6-3: OFF
		SD_CD_1	Connected to the SD card slot CD pin		
		DV_DATA0	DV input	CN11, pin A6	
			Connected to the Video decoder IC D0 pin	CN7, pin 17	SW6-3: ON
152	PVcc				
153	PJ1/DV_DATA1/ LCD_DATA1/SD_WP_1/ PWM1B	PJ1	Connected to the character LCD DB6 pin	CN7, pin 16	SW6-3: OFF
		SD_WP_1	Connected to the SD card slot WP pin		
		DV_DATA1	DV input	CN11, pin B6	
			Connected to the Video decoder IC D1 pin	CN7, pin 20	SW6-3: ON
154	Vss				
155	PG8/D24/LCD_DATA8/ PINT0/TIOC3A	LCD_DATA8	Connected to LCD module D8 pin	CN 9, pin 12 CN 10, pin A6	G0
156	Vcc				
157	PJ2/DV_DATA2/ LCD_DATA2/SD_D1_1/ PWM1C	PJ2	Connected to the character LCD DB5 pin	CN7, pin 13	SW6-3: OFF
		SD_D1_1	Connected to the SD card slot DAT1 pin		
		DV_DATA 2	DV input	CN11, pin A10	
			Connected to the Video decoder IC D2 pin	CN7, pin 19	SW6-3: ON
158	PJ3/DV_DATA3/ LCD_DATA3/SD_D0_1 PWM1D	PJ3	Connected to the character LCD DB4 pin	CN7, pin 14	SW6-3: OFF
		SD_D0_1	Connected to the SD card slot DAT0 pin		
		DV_DATA3	DV input	CN11, pin B9	
			Connected to the Video decoder IC D3 pin	CN7, pin 22	SW6-3: ON

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.7 SH7269 Pin Functions (7/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
159	PJ4/DV_DATA4/ LCD_DATA4/SD_CLK_1/ PWM1E	PJ4	Connected to the character LCD DB3 pin	CN7, pin 3	SW6-3: OFF
		SD_CLK_1	Connected to the SD card slot CLK pin		
		DV_DATA4	DV input	CN11, pin A9	
			Connected to the Video decoder IC D4 pin	CN7, pin 24	SW6-3: ON
160	PG9/D25/LCD_DATA9/ PINT1/TIOC3B	LCD_DATA9	Connected to LCD module D9 pin	CN9, pin 11 CN10, pin B6	G1
161	PG10/D26/LCD_DATA10/ PINT2/TIOC3C	LCD_DATA10	Connected to LCD module D10 pin	CN9, pin 14 CN10, pin A7	G2
162	PVcc				
163	PG11/D27/LCD_DATA11/ PINT3/TIOC3D	LCD_DATA11	Connected to LCD module D11 pin	CN9, pin 13 CN10, pin B7	G3
164	Vss				
165	PG12/D28/LCD_DATA12/ PINT4	LCD_DATA12	Connected to LCD module D12 pin	CN9, pin 16 CN10, pin B8	G4
166	Vcc				
167	PG13/D29/LCD_DATA13/ PINT5	LCD_DATA13	Connected to LCD module D13 pin	CN9, pin 18 CN10, pin A9	G5
168	PG14/D30/LCD_DATA14/ PINT6	LCD_DATA14	Connected to LCD module D14 pin	CN9, pin 17 CN10, pin B9	G6
169	PG15/D31/LCD_DATA15/ PINT7	LCD_DATA15	Connected to LCD module D15 pin	CN9, pin 20 CN10, pin A10	G7
170	PG16/WE2#/ICIORD#/ DQMUL/LCD_DATA16/ AUDATA0	AUDATA0	Connected to the H-UDI port connector (J3)	CN10, pin A11	AUD
		LCD_DATA16	Connected to LCD module D16 pin		R0
171	PJ5/DV_DATA5/ LCD_DATA5/SD_CMD_1/ PWM1F	PJ5	Connected to the character LCD DB2 pin	CN7, pin 4	SW6-3: OFF
		SD_CMD_1	Connected to the SD card slot CMD pin		
		DV_DATA5	DV input	CN11, pin A7	
			Connected to the Video decoder IC D5 pin	CN7,pin 23	SW6-3: ON
172	PVcc				
173	PJ6/DV_DATA6/ LCD_DATA6/SD_D3_1/ PWM1G	PJ6	Connected to the character LCD DB1 pin	CN7, pin 1	SW6-3: OFF
		SD_D3_1	Connected to the SD card slot DAT3 pin		
		DV_DATA6	DV input	CN11, pin B7	
			Connected to the Video decoder IC D6 pin	CN7, pin 25	SW6-3: ON
174	Vss				
175	PG17/WE3#/ICIOWR#/ AH#/DQMUU/ LCD_DATA17/AUDATA1	AUDATA1	Connected to the H-UDI port connector (J3)	CN10, pin B11	AUD
		LCD_DATA17	Connected to LCD module D17 pin		R1
176	Vcc				

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.8 SH7269 Pin Functions (8/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
177	PJ7/DV_DATA7/ LCD_DATA7/SD_D2_1/ PWM1H	PJ7	Connected to the character LCD DB0 pin	CN7, pin 2	SW6-3: OFF
		SD_D2_1	Connected to the SD card slot DAT2 pin		
		DV_DATA7	DV input	CN11, pin A5	
			Connected to the Video decoder IC D7 pin	CN7, pin 28	SW6-3: ON
178	PJ8/DV_DATA8/ LCD_DATA8/PINT0/ PWM2A/CTS5#	PWM2A	PWM output	CN11, pin A4	TTL level
		DV_DATA8	DV input		
		–	–	CN1, pin 12	
179	PJ9/DV_DATA9/ LCD_DATA9/PINT1/ PWM2B/RTS5#	PWM2B	PWM output	CN11, pin B3	TTL level
		DV_DATA9	DV input		
		–	–	CN1, pin 5	
180	PG18/DV_DATA4/ LCD_DATA18/SPDIF_IN/ SCK4	LCD_DATA18	Connected to LCD module D18 pin	CN10, pin A12	R2
181	PG19/DV_DATA5/ LCD_DATA19/SPDIF_OUT/ SCK5	LCD_DATA19	Connected to LCD module D19 pin	CN10, pin B12	R3
182	PVcc				
183	PG20/DV_DATA6/ LCD_DATA20/LCD_TCON3/ RxD4	LCD_DATA20	Connected to LCD module D20 pin	CN10, pin B13	R4
184	Vss				
185	PG21/DV_DATA7/ LCD_DATA21/LCD_TCON4/TxD4/AUDATA2	AUDATA2	Connected to the H-UDI port connector (J3)	CN10, pin A14	AUD
		LCD_DATA21	Connected to LCD module D21 pin		R5
186	Vcc				
187	PG22/LCD_DATA22/ LCD_TCON5/RxD5/ AUDSYNC#	AUDSYNC#	Connected to the H-UDI port connector (J3)	CN10, pin B14	AUD
		LCD_DATA22	Connected to LCD module D22 pin		R6
		RxD5	Connected to the UART connector (J10)	CN1, pin 15	TTL level
188	PG23//LCD_DATA23/ LCD_TCON6/TxD5/ AUDATA3	AUDATA3	Connected to the H-UDI port connector (J3)	CN10, pin A15	AUD
		LCD_DATA23	Connected to LCD module D23 pin		R7
		TxD5	Connected to the UART connector (J10)	CN1, pin 14	TTL level
189	PG24/LCD_CLK	LCD_CLK	Connected to LCD module CLK pin	CN9, pin 23 CN10, pin A16	
190	PG25/LCD_TCON0	LCD_TCON0	Connected to LCD module VSYNC pin	CN9, pin 19 CN10, pin B16	
191	PG26/LCD_TCON1	LCD_TCON1	Connected to LCD module HSYNC pin	CN9, pin 21 CN10, pin A17	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.9 SH7269 Pin Functions (9/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
192	PG27/LCD_TCON2/ LCD_EXTCLK	LCD_EXTCLK	Connects LCD module external clock to MCU	CN9, pin 26	
193	PF0/BREQ#0/ QSPCLK_1/RSPCK1/ TIOC4A/DREQ0/ AUDCK	AUDCK	Connected to the H-UDI port connector (J3)	CN7, pin 30	AUD
		QSPCLK_1/ RSPCK1	Connected to serial flash memory 2 SCK pin		
		TIOC4A	Connected to the MTU2 connector (J16)	CN9, pin 28	
194	PVcc				
195	PF1/BACK#/QSSL_1/ SSL10/TIOC4B/DACK0	QSSL_1/ SSL10	Connected to serial flash memory 2 CS# pin	CN5, pin 20	
196	Vss				
197	PF2/WAIT#/QMO_1/ QIO0_1/MOSI1/TIOC4C/ TEND0/SPBIO0_1	QMO_1/QIO0_1 /MOSI1/ SPBMO_1SPBIO0_1	Connected to serial flash memory 2 SI pin	CN7, pin 31	
		–	–		
		TIOC4C	Connected to the MTU2 connector (J16)	CN9, pin 30	
198	PF3/CS2#/QMI_1/ QIO1_1/MISO1/ TIOC4D/AUDIO_XOUT / SPBMI_1/SPBIO1_1	QMI_1/QIO1_1 /MISO1/ SPBMI_1SPBIO1_1	Connected to serial flash memory 2 SO pin	CN7, pin 33	
		TIOC4D	Connected to the MTU2 connector (J16)		
199	PF4/CS5#/CE1A#/ SSISCK0/SGOUT_0	SGOUT_0		CN7, pin 36	0 Ω resistor
		SSISCK0	Connected to the DAC BICK pin		
200	PF5/SSIWS0/SGOUT_1	SGOUT_1		CN7, pin 35	0 Ω resistor
		SSIWS0	Connected to the DAC LRCK pin		
201	PF6/CE2A#/SSITxD0/ SGOUT_2	SGOUT_2		CN7, pin 37	0 Ω resistor
		SSITxD0	Connected to the DAC SDTI pin		
202	PF7/SSIRxD0/RxD0/ SGOUT_3/CTS1#	SGOUT_3		CN7, pin 38	0 Ω resistor
		PF7	Connected to the DAC PDN# pin		
203	PF8/A23/TxD0	A23	Address bus	CN5, pin 19	
204	PF9/BS#/DV_DATA0/ SCK0/MMC_D4/RTS1#	PF9		CN5, pin 18	
205	PVcc				
206	PF10/CS1#/SSISCK1/ DV_DATA1/SCK1/MMC_D5	–	–	CN7, pin 17	SW6-3: OFF
207	Vss				
208	PF11/SSIWS1/DV_DATA2/ RxD1/MMC_D6	–	–	CN7, pin 20	SW6-3: OFF
209	PF12/SSIDATA1/ DV_DATA3/TxD1/MMC_D7	–	–	CN7, pin 19	SW6-3: OFF
210	PF13/A24/SSISCK2/SCK2	A24	Address bus	CN5, pin 17	
211	PF14/A25/SSIWS2/RxD2	RxD2	Connected to the RS-232C connector (J10)	CN5, pin 16	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.10 SH7269 Pin Functions (10/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
212	PF15/A0/SSIDATA2/ WDTOVF#/TxD2/UBCTRG #	TxD2	Connected to the RS-232C connector (J10)	CN5, pin 15	
213	PVcc				
214	PJ10/DV_DATA10/ LCD_DATA10/PINT2/ PWM2C/SCK5#	PWM2C	PWM output	CN11, pin A2	TTL level
		DV_DATA10	DV input		
		–	–	CN1, pin 13	
215	Vss				
216	PF16/SD_CD_0/FCE#/ IRQ4/MMC_CD	SD_CD_0 MMC_CD	Connected to SD/MMC card slot CD pin	CN5, pin 13	SW6-2: ON
		FCE#	Connected to NAND flash memory CE# pin	CN5, pin 12	SW6-2: OFF
217	PF17/SD_WP_0/FRB/IRQ5	SD_WP_0	Connected to SD/MMC card slot WP pin	CN5, pin 11	SW6-2: ON
		FRB	Connected to NAND flash memory R/B# pin	CN5, pin 10	SW6-2: OFF
218	PF18/SD_D1_0/SSISCK3/ IRQ6/MMC_D1	SD_D1_0/ MMC_D1	Connected to SD/MMC card slot DAT1 pin	CN5, pin 8	
219	PJ11/DV_DATA11/ LCD_DATA11/PINT3/ PWM2D/SCK6	PWM2D	PWM output	CN1, pin B2	TTL level
		DV_DATA11	DV input		
		–	–	CN1, pin 1	
220	PJ12/DV_DATA12/ LCD_DATA12/PINT4/ PWM2E/SCK7	PWM2E	PWM output	CN11, pin B11	TTL level
		DV_DATA12	DV input		
		–	–	CN9, pin 27	
221	PJ13/DV_DATA13/ LCD_DATA13/PINT5/ PWM2F/TxD5	PWM2F	PWM output	CN11, pin A11	TTL level
		DV_DATA13	DV input		
		–	–	CN7, pin 32	
222	PVcc				
223	PF19/SD_D0_0/SSIWS3/ IRQ7/MMC_D0	SD_D0_0 MMC_D0	Connected to SD/MMC card slot DAT0 pin	CN5, pin 7	
224	Vss				
225	PF20/SD_CLK_0/ SSIDATA3/MMC_CLK	SD_CLK_0/ MMC_CLK	Connected to SD/MMC card slot CLK pin	CN5, pin 5	
226	Vcc				
227	PF21/SD_CMD_0/SCK3/ MMC_CMD	SD_CMD_0/ MMC_CMD	Connected to SD/MMC card slot CMD pin	CN5, pin 4	
228	PF22/SD_3_0/RxD3/ MMC_D3	SD_D3_0/ MMC_D3	Connected to SD/MMC card slot DAT3 pin	CN5, pin 3	
229	PF23/SD_D2_0/TxD3/ MMC_D2	SD_D2_0/ MMC_D2	Connected to SD/MMC card slot DAT2 pin	CN5, pin 2	
230	PD0/D0/PWM1A	D0	Data bus	CN8, pin 1	
231	PVcc				
232	PJ24/SGOUT_0/SSISCK4/ LCD_TCON3/SPDIF_IN/SC K7	–	–	CN7, pin 25	SW6-3: OFF
233	Vss				
234	PD1/D1/PWM1B	D1	Data bus	CN8, pin 3	
235	PD2/D2/PWM1C	D2	Data bus	CN8, pin 6	
236	PD3/D3/PWM1D	D3	Data bus	CN8, pin 8	

Legend: : 3.3V power supply, : 1.25V power supply, : GND

Table 4.2.11 SH7269 Pin Functions (11/11)

No.	Name	Symbol	Description	Expansion Connector	Remarks
237	PJ25/SGOUT_1/SSIWS4/ LCD_TCON4/SPDIF_OUT/ RxD7	–	–	CN7, pin 28	SW6-3: OFF
238	PJ26/SGOUT_2/SSIDATA4/ LCD_TCON5/TxD7	–	–	CN7, pin 27	
239	PJ27/SGOUT_3/TIOC1A/ CTS7#	TIOC1A	Connected to the MCU2 connector (J16)	CN9, pin 29	
240	PVcc				
241	Vss				
242	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and NAND flash memory RE# pin	CN8, pin 11	Auto-switch
243	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and NAND flash memory CLE pin	CN8, pin 13	Auto-switch
244	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and NAND flash memory ALE pin	CN8, pin 16	Auto-switch
245	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and NAND flash memory WE# pin	CN8, pin 18	Auto-switch
246	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 2	
247	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 4	
248	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 7	
249	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 9	
250	PVcc				
251	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 12	
252	Vss				
253	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 14	
254	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 17	
255	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 19	
256	MD_CLK0	MD_CLK0	Connected to SW5-1 as the clock mode input	–	RES#: low

Legend: : 3.3V power supply, : 1.25V power supply, : GND

4.2.3 M3A-HS64G02 Module Availability

The following table shows which combination of modules can/cannot be used.

Table 4.2.12 M3A-HS64G02 Module Availability

				R0K572690C000BR																R0K572690C000BR+M3A-HS64G02																			
	SH7269 Peripherals	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory 1	Serial flash memory 2	USB	SD/MMC card	H-UDI (14-pin)	H-UDI (38-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C	LCD	DV	PWM	Character LCD	SD card	D/A Converter	UART	IIC	LCD	IEBus™	CAN0	CAN1	Key input switches	IRQ2 switch	IRQ3 switch	PWM	Video decoder	MTU2
R0K572690C000BR	BSC	U6	NOR flash memory		Y	Y	Y	N	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	BSC	U9	SDRAM	Y		Y	Y	Y	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	FLCTL	U7	NAND flash memory	Y	Y		Y	Y	Y	Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	RSPI	U10	Serial flash memory 1	N	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	RSPI	U10	Serial flash memory 2	(1)	(1)	Y	Y	Y		Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	(10)
	USB	J1, J2	USB	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	SDHI/MMC	J11	SD/MMC card	Y	Y	(2)	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y	Y	Y		(3)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	H-UDI, AUD	J3	H-UDI (38-pin)	Y	Y	Y	Y	Y	N	Y	Y	(3)		Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	N	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	N
	I/O ports	LED2, LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	(6)	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	(5)	Y	Y	Y	Y	Y	Y	Y	Y	–	(16)	Y	Y	Y	Y	Y	Y
	I/O ports	SW5, SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	(7)	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	VDC4	CN10	LCD	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y		(4)	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	VDC4	CN11	DV	Y	Y	Y	Y	Y	Y	Y	Y	Y	(6)	Y	(5)	(7)	Y	(4)		(8)	N	N	N	Y	Y	N	Y	–	(13)	Y	Y	Y	Y	N	Y
	PWM	CN11	PWM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(8)		Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
R0K572690C000BR+M3A-HS64G02	I/O ports	J1	Character LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y		(9)	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	(12)	(11)	Y
	SDHI	J4	SD card	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	(9)		Y	Y	Y	Y	Y	Y	–	Y	Y	Y	(9)	(11)	Y
	SSIF, IIC3	U10	D/A Converter	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y		Y	Y	Y	Y	Y	–	Y	Y	(14)	(14)	(9)	Y	Y
	SCIF	J2	UART	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	IIC3	J3	IIC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	VDC4	J10 to J12	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	(15)
	IEBus	J13	IEBus™	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y
	RCAN	J14	CAN0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–
	RCAN	J15	CAN1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(16)	Y	Y	Y	(13)	Y	Y	Y	Y	Y	Y	Y	Y	–		Y	Y	Y	Y	Y	Y
	I/O ports	SW4 to SW19	Key input switches	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y		Y	Y	Y	Y	Y
	INTC	SW1	IRQ2 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(14)	Y	Y	Y	Y	–	Y	Y		Y	Y	Y	Y
	INTC	SW2	IRQ3 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(14)	Y	Y	Y	Y	–	Y	Y	Y		Y	Y	Y
	PWM	J5	PWM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(12)	(9)	(9)	Y	Y	Y	Y	–	Y	Y	Y	Y		(11)	Y
	VDC4	U11	Video decoder	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	(11)	(11)	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	(11)		Y
	MTU2	LED1 to LED14	MTU2	Y	Y	Y	Y	Y	(10)	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(15)	Y	–	Y	Y	Y	Y	Y	Y	

Y: Yes, N: No, –: N/A

Notes:
1. When using a serial flash memory with NOR flash memory or SDRAM, quad mode cannot be used.
2. PF16 and PF17 are multiplexed pins. When setting SW6-2 on the R0K572690C000BR, either SD/MMC card or NAND flash memory can be used.
3. Either 14-pin or 38-pin H-UDI port connector can be used.
4. PJ22 and PJ23 are multiplexed pins. Either LCD or DV can be used.
5. PJ21 is a multiplexed pin. Either IRQ1 switch or DV can be used.
6. PJ19 and PJ18 are multiplexed pins. Either LED or DV can be used.
7. PJ17 and PJ16 are multiplexed pins. Either DIP switches or DV can be used.
8. PJ15 to PJ8 are multiplexed pins. Either DV or PWM can be used.
9. Change JP3 setting on the M3A-HS64G02 to use either the characet LCD or SD card.
10. PF0, PF2, PF3 are multiplexed pins. Either MTU2 or serial flash memory 2 can be used.
11. PJ0 to PJ7 are multiplexed pins. When setting SW6-3 on the R0K572690C000BR, either one of modules can be used.
12. PJ0 to PJ7 are multiplexed pins. Either Characer LCD or PWM can be used.
13. PJ20 and PJ21are multiplexed pins. Either CAN1 or DV can be used.
14. Change JP1, JP2 settings on the M3A-HS64G02 to use either IRQ2 or IRQ3 switch.
15. PF0 pin is connected to MTU2 and LCD.
16. Change JP8 setting on the R0K572690C000BR to use either CAN1 or IRQ1 switch.

4.2.4 SH7269 Multiplexed Pins Used on the M3A-HS64G02

Table 4.2.13 to Table 4.2.31 list the SH7269 multiplexed pin functions used on the M3A-HS64G02.

These multiplexed pins are set as port input pins by default. Set the MD bit in the Port control register to use the SH7269 peripheral functions (except I/O ports).

Table 4.2.13 SH7269 Multiplexed Pin Functions (BSC1)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
BSC	CS0#	PCCR0	PC0MD = B'1 (1)	PC0/**CS0#**/MD_BOOT2
	CS3#	PCCR2	PC8MD[2:0] = B'001	PC8/**CS3#**/TxD7/CTx1/CTx0&CTx1
	RD#	PCCR0	PC1MD = B'1 (1)	PC1/**RD#**
	WE0#/DQMLL	PCCR0	PC3MD[1:0] = B'01	PC3/**WE0#**/**DQMLL**/RxD6
	WE1#/WE#/DQMLU	PCCR1	PC4MD[1:0] = B'01	PC4/**WE1#**/**DQMLU**/TxD6
	RAS#	PCCR1	PC5MD[2:0] = B'001	PC5/**RAS#**/CRx0/CRx0/CRx1/CRx2/IRQ0
	CAS#	PCCR1	PC6MD[2:0] = B'001	PC6/**CAS#**/SCK7/CTx0/CTx0&CTx1&CTx2
	CKE	PCCR1	PC7MD[2:0] = B'001	PC7/**CKE**/RxD7/CRx1/CRx0/CRx1/IRQ1
	RD/WR#	PCCR0	PC2MD[1:0] = B'01	PC2/**RD**/**WR#**/SCK6
	A24	PFCR3	PF13MD[2:0] = B'001	PF13/**A24**/SSISCK2/SCK2
	A23	PFCR2	PF8MD[2:0] = B'001	PF8/**A23**/TxD0
	A22	PBCR5	PB22MD[2:0] = B'001	PB22/**A22**/CTx2/IETxD/CS4#
	A21	PBCR5	PB21MD[1:0] = B'01	PB21/**A21**/CRx2/IERxD
	A20	PBCR5	PB20MD[2:0] = B'001 (1)	PB20/**A20**/QMISO0&QIO10/MISO0 / SPBMI_0/SPBIO1_0
	A19	PBCR4	PB19MD[2:0] = B'001 (1)	PB19/**A19**/QMO_0&QIO0_0/MOSI0 / SPBMO_0/SPBIO0_0
	A18	PBCR4	PB18MD[2:0] = B'001 (1)	PB18/**A18**/QSSL_0/SSL00 / SPBSSL
	A17	PBCR4	PB17MD[2:0] = B'001 (1)	PB17/**A17**/QSPCLK_0/RSPCK0 / SPBCLK
	A16	PBCR4	PB16MD[2:0] = B'001 (1)	PB16/**A16**/QIO3_0 / SPBIO3_0
	A15	PBCR3	PB15MD[2:0] = B'001 (1)	PB15/**A15**/QIO2_0 / SPBIO2_0
	A14	PBCR3	PB14MD[2:0] = B'001 (1)	PB14/**A14**/QIO3_1 / SPBIO3_1
	A13	PBCR3	PB13MD[2:0] = B'001 (1)	PB13/**A13**/QIO2_1 / SPBIO2_1
	A12	PBCR3	PB12MD[1:0] = B'01 (1)	PB12/**A12**/TIOC3D
	A11	PBCR2	PB11MD[1:0] = B'01 (1)	PB11/**A11**/TIOC3C
	A10	PBCR2	PB10MD[1:0] = B'01 (1)	PB10/**A10**/TIOC3B
	A9	PBCR2	PB9MD[1:0] = B'01 (1)	PB9/**A9**/TIOC3A
	A8	PBCR2	PB8MD[1:0] = B'01 (1)	PB8/**A8**/TIOC2B
	A7	PBCR1	PB7MD[1:0] = B'01 (1)	PB7/**A7**/TIOC2A
	A6	PBCR1	PB6MD[1:0] = B'01 (1)	PB6/**A6**/TIOC1B
	A5	PBCR1	PB5MD[1:0] = B'01 (1)	PB5/**A5**/TIOC1A
	A4	PBCR1	PB4MD[1:0] = B'01 (1)	PB4/**A4**/TIOC0D
	A3	PBCR0	PB3MD[1:0] = B'01 (1)	PB3/**A3**/TIOC0C
	A2	PBCR0	PB2MD[1:0] = B'01 (1)	PB2/**A2**/TIOC0B
	A1	PBCR0	PB1MD[1:0] = B'01 (1)	PB1/**A1**/TIOC0A
	D15	PDCR3	PD15MD[1:0] = B'01 (1)	PD15/**D15**/**NAF7**/PWM2H
	D14	PDCR3	PD14MD[1:0] = B'01 (1)	PD14/**D14**/**NAF6**/PWM2G
	D13	PDCR3	PD13MD[1:0] = B'01 (1)	PD13/**D13**/**NAF5**/PWM2F
	D12	PDCR3	PD12MD[1:0] = B'01 (1)	PD12/**D12**/**NAF4**/PWM2E
	D11	PDCR2	PD11MD[1:0] = B'01 (1)	PD11/**D11**/**NAF3**/PWM2D
	D10	PDCR2	PD10MD[1:0] = B'01 (1)	PD10/**D10**/**NAF2**/PWM2C
	D9	PDCR2	PD9MD[1:0] = B'01 (1)	PD9/**D9**/**NAF1**/PWM2B
	D8	PDCR2	PD8MD[1:0] = B'01 (1)	PD8/**D8**/**NAF0**/PWM2A
	D7	PDCR1	PD7MD[1:0] = B'01 (1)	PD7/**D7**/**FWE#**/PWM1H
	D6	PDCR1	PD6MD[1:0] = B'01 (1)	PD6/**D6**/**FALE**/PWM1G

Notes 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 4.2.14 SH7269 Multiplexed Pin Functions (BSC2)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
BSC	D5	PDCR1	PD5MD[1:0] = B'01 (1)	PD5/**D5**/**FCLE**/PWM1F
	D4	PDCR1	PD4MD[1:0] = B'01 (1)	PD4/**D4**/**FRE**#/PWM1E
	D3	PDCR0	PD3MD[1:0] = B'01 (1)	PD3/**D3**/PWM1D
	D2	PDCR0	PD2MD[1:0] = B'01 (1)	PD2/**D2**/PWM1C
	D1	PDCR0	PD1MD[1:0] = B'01 (1)	PD1/**D1**/ PWM1B
	D0	PDCR0	PD0MD[1:0] = B'01 (1)	PD0/**D0**/PWM1A

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 4.2.15 SH7269 Multiplexed Pin Functions (INTC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
INTC	IRQ1	PJCR5	PJ21MD[2:0] = B'100	PJ21/DV_DATA21/LCD_DATA21/LCD_TCON4/ **IRQ1**/CTx2/CTx0&CTx1&CTx2

Note: Bold text indicates the function used.

Table 4.2.16 SH7269 Multiplexed Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bbit Setting	
SCIF	RxD2	PFCR3	PF14MD[2:0] = B'100	PF14/A25/SSIWS2//**RxD2**
	TxD2	PFCR4	PF15MD[2:0] = B'100	PF15/A0/SSIDATA2/WDTOVF#/**TxD2**/UBCTRG#
	TxD5	PGCR5	PG23MD[2:0] = B'100	PG23/LCD_DATA23/LCD_TCON6/**TxD5**
	RxD5	PGCR5	PG22MD[2:0] = B'100	PG22/LCD_DATA22/LCD_TCON5/**RxD5**

Note: Bold text indicates the function used.

Table 4.2.17 SH7269 Multiplexed Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
IIC3	SDA1	PECR0	PE3MD[2:0] = B'001	PE3/**SDA1**/TCLKD/ADTRG#/DV_HSYNC
	SCL1	PECR0	PE2MD[2:0] = B'001	PE2/**SCL1**/TCLKC/IOIS16#/DV_VSYNC
	SDA0	PECR0	PE1MD[2:0] = B'01	PE1 / **SDA0** / TCLKB / AUDIO_CLK / DV_CLK
	SCL0	PECR0	PE0MD[2:0] = B'01	PE0 / **SCL0** / TCLKA / LCD_EXTCLK

Note: Bold test indicates the function used.

Table 4.2.18 SH7269 Multiplexed Pin Functions (RCAN-TL1)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RCAN-TL1	CRx2	PJCR5	PJ20MD[2:0] = B'101	PJ20/DV_DATA20/LCD_DATA20/LCD_TCON3/ IRQ0/**CRx2**/CRx0/CRx1/CRx2
	CTx2	PJCR5	PJ21MD[2:0] = B'101	PJ21/DV_DATA21/LCD_DATA21/LCD_TCON4/ IRQ1/**CTx2**/CTx0&CTx1&CTx2

Note: Bold text indicates the function used.

Table 4.2.19 SH7269 Multiplexed Pin Functions (IEB)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD bit setting	
IEB	IERxD	PJCR7	PJ29MD[2:0] = B'101	PJ29/SSIWS5/TIOC2A/**IERxD**
	IETxD	PJCR7	PJ30MD[2:0] = B'101	PJ30/SSIDATA5/TIOC2B/**IETxD**

Note: Bold text indicates the function used.

Table 4.2.20 SH7269 Multiplexed Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD bit setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01 (1)	PD15/**D15**/**NAF7**/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01 (1)	PD14/**D14**/**NAF6**/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01 (1)	PD13/**D13**/**NAF5**/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01 (1)	PD12/**D12**/**NAF4**/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01 (1)	PD11/**D11**/**NAF3**/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01 (1)	PD10/**D10**/**NAF2**/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01 (1)	PD9/**D9**/**NAF1**/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01 (1)	PD8/**D8**/**NAF0**/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01 (1)	PD7/**D7**/**FWE#**/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01 (1)	PD6/**D6**/**FALE**/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01 (1)	PD5/**D5**/**FCLE**/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01 (1)	PD4/**D4**/**FRE#**/PWM1E
	FCE#	PFCR5	PF16MD[2:0] = B'011	PF16/SD_CD_0/**FCE#**/IRQ4/MMC_CD
	FRB	PFCR5	PF17MD[2:0] = B'011	PF17/SD_WP_0/**FRB**/IRQ5

Notes: 1. These values must be set in boot modes 2 to 5.
2. Bold text indicates the function used.

Table 4.2.21 SH7269 Multiplexed Pin Functions (RSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RSPI	MISO0	PBCR5	PB20MD[1:0] = B'11 (1)	PB20/A20/QMI_0/QIO1_0/**MISO0** / SPBMI_0/SPBIO1_0
	MOSI0	PBCR4	PB19MD[1:0] = B'11 (1)	PB19/A19/QMO_0/QIO_0/**MOSI0**/ SPBMO_0/SPBIO0_0
	SSL00	PBCR4	PB18MD[1:0] = B'11 (1)	PB18/A18/QSSL_0/**SSL00**/ SPBSSL
	RSPCK0	PBCR4	PB17MD[1:0] = B'11 (1)	PB17/A17/QSPCLK_0/**RSPCK0** / SPBCLK
	MISO1	PFCR0	PF3MD[2:0] = B'011	PF3/CS2#/QMI_1/QIO1_1/**MISO1**/TIOC4D/ AUDIO_XOUT / SPBMI_1/SPBIO1_1
	MOSI1	PFCR0	PF2MD[2:0] = B'011	PF2/WAIT#/QMO_1/QIO0_1/**MOSI1**/TIOC4C TEND0/ SPBMO_1/SPBIO0_1
	SSL10	PFCR0	PF1MD[2:0] = B'011	PF1/BACK#/QSSL_1/**SSL10**/TIOC4B/DACK0
	RSPCK1	PFCR0	PF0MD[2:0] = B'011	PF0/BREQ#/QSPCLK_1/**RSPCK1**/TIOC4A/ DREQ0/AUDCK

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 4.2.22 SH7269 Multiplexed Pin Functions (RQSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
RQSPI	QIO3_0	PBCR4	PB16MD[2:0] = B'010 (1)	PB16/A16/**QIO3_0** / SPBIO3_0
	QIO2_0	PBCR3	PB15MD[2:0] = B'010 (1)	PB15/A15/**QIO2_0** / SPBIO2_0
	QIO1_0	PBCR5	PB20MD[2:0] = B'010 (1)	PB20/A20/**QMI_0**/**QIO1_0**/MISO0/ SPBMI_0/SPBIO1_0
	QIO0_0	PBCR4	PB19MD[2:0] = B'010 (1)	PB19/A19/**QMO_0**/**QIO0_0**/MOSI0/ SPBMO_0/SPBIO0_0
	QSSL_0	PBCR4	PB18MD[2:0] = B'010 (1)	PB18/A18/**QSSL_0**/SSL00 / SPBSSL
	QSPCLK_0	PBCR4	PB17MD[2:0] = B'010 (1)	PB17/A17/**QSPCLK_0**/RSPCK0 / SPBCLK
	QIO3_1	PBCR3	PB14MD[2:0] = B'010 (1)	PB14/A14/**QIO3_1** / SPBIO3_1
	QIO2_1	PBCR3	PB13MD[2:0] = B'010 (1)	PB13/A13/**QIO2_1** / SPBIO2_1
	QIO1_1	PFCR0	PF3MD[2:0] = B'010	PF3/CS2#/**QMI_1**/**QIO1_1**/MISO1/TIOC4D/ AUDIO_XOUT / SPBMI_1/SPBIO1_1
	QIO0_1	PFCR0	PF2MD[2:0] = B'010	PF2/WAIT#/**QMO_1**/**QIO0_1**/MOSI1/TIOC4C/TEND0/ SPBMO_1/SPBIO0_1
	QSSL_1	PFCR0	PF1MD[2:0] = B'010	PF1/BACK#/**QSSL_1**/SSL10/TIOC4B/DACK0
	QSPCLK_1	PFCR0	PF0MD[2:0] = B'010	PF0/BREQ#/**QSPCLK_1**/RSPCK1/TIOC4A/DREQ0/A UDCK

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 4.2.23 SH7269 Multiplexed Pin Functions (SPIBSC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SPIBSC	SPBCLK	PBCR4	PB17MD[2:0] = B'110*1	PB17 / A17 / QSPCLK_0 / RSPCK0 / **SPBCLK**
	SPBSSL	PBCR4	PB18MD[2:0] = B'110*1	PB18 / A18 / QSSL_0 / SSL00 / **SPBSSL**
	SPBMO_0/ SPBIO0_0	PBCR4	PB19MD[2:0] = B'110*1	PB19 / A19 / QMO_0/QIO0_0 / MOSI0 / **SPBMO_0/SPBIO0_0**
	SPBMI_0/ SPBIO1_0	PBCR5	PB20MD[2:0] = B'110*1	PB20 / A20 / QMI_0/QIO1_0 / MISO0 / **SPBMI_0/SPBIO1_0**
	SPBIO2_0	PBCR3	PB15MD[2:0] = B'110*1	PB15 / A15 / QIO2_0 / **SPBIO2_0**
	SPBIO3_0	PBCR4	PB16MD[2:0] = B'110*1	PB16 / A16 / QIO3_0 / **SPBIO3_0**
	SPBMO_1/ SPBIO0_1	PFCR0	PF2MD[2:0] = B'110	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / **SPBMO_1/SPBIO0_1**
	SPBMI_1/ SPBIO1_1	PFCR0	PF3MD[2:0] = B'110	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / **SPBMI_1/SPBIO1_1**
	SPBIO2_1	PBCR3	PB13MD[2:0] = B'110*1	PB13 / A13 / QIO2_1 / **SPBIO2_1**
	SPBIO3_1	PBCR3	PB14MD[2:0] = B'110*1	PB14 / A14 / QIO3_1 / **SPBIO3_1**

Notes: 1. These values must not be set in boot modes 0 and 1.
2. Bold text indicates the function used.

Table 4.2.24 SH7269 Multiplexed Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SDHI	SD_CD_0	PFCR5	PF16MD[2:0] = B'001	PF16/**SD_CD_0**/FCE#/IRQ4/MMC_CD
	SD_WP_0	PFCR5	PF17MD[2:0] = B'001	PF17/**SD_WP_0**/FRB/IRQ5
	SD_D1_0	PFCR5	PF18MD[2:0] = B'001	PF18/**SD_D1_0**/SSISCK3/IRQ6/MMC_D1
	SD_D0_0	PFCR5	PF19MD[2:0] = B'001	PF19/**SD_D0_0**/SSIWS3/IRQ7/MMC_D0
	SD_CLK_0	PFCR6	PF20MD[2:0] = B'001	PF20/**SD_CLK_0**/SSIDATA3/MMC_CLK
	SD_CMD_0	PFCR6	PF21MD[2:0] = B'001	PF21/**SD_CMD_0**/SCK3/ MMC_CMD
	SD_D3_0	PFCR6	PF22MD[2:0] = B'001	PF22/**SD_D3_0**/RxD3/MMC_D3
	SD_D2_0	PFCR6	PF23MD[2:0] = B'001	PF23/**SD_D2_0**/TxD3/MMC_D2
	SD_CD_1	PJCR0	PJ0MD[2:0] = B'011	PJ0/DV_DATA0/LCD_DATA0/**SD_CD_1**/PWM1A
	SD_WP_1	PJCR0	PJ1MD[2:0] = B'011	PJ1/DV_DATA1/LCD_DATA1/**SD_WP_1**/PWM1B
	SD_D1_1	PJCR0	PJ2MD[2:0] = B'011	PJ2/DV_DATA2/LCD_DATA2/**SD_D1_1**/PWM1C
	SD_D0_1	PJCR0	PJ3MD[2:0] = B'011	PJ3/DV_DATA3/LCD_DATA3/**SD_D0_1**/PWM1D
	SD_CLK_1	PJCR1	PJ4MD[2:0] = B'011	PJ4/DV_DATA4/LCD_DATA4/**SD_CLK_1**/PWM1E
	SD_CMD_1	PJCR1	PJ5MD[2:0] = B'011	PJ5/DV_DATA5/LCD_DATA5/**SD_CMD_1**/PWM1F
	SD_D3_1	PJCR1	PJ6MD[2:0] = B'011	PJ6/DV_DATA6/LCD_DATA6/**SD_D3_1**/PWM1G
	SD_D2_1	PJCR1	PJ7MD[2:0] = B'011	PJ7/DV_DATA7/LCD_DATA7/**SD_D2_1**/PWM1H

Note: Bold text indicates the function used.

Table 4.2.25 SH7269 Multiplexed Pin Functions (MMC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
MMC	MMC_CD	PFCR5	PF16MD[2:0] = B'101	PF16/SD_CD_0/FCE#/IRQ4/**MMC_CD**
	MMC_D1	PFCR5	PF18MD[2:0] = B'101	PF18/SD_D1_0/SSISCK3/IRQ6/**MMC_D1**
	MMC_D0	PFCR5	PF19MD[2:0] = B'101	PF19/SD_D0_0/SSIWS3/IRQ7/**MMC_D0**
	MMC_CLK	PFCR6	PF20MD[2:0] = B'101	PF20/SD_CLK_0/SSIDATA3/**MMC_CLK**
	MMC_CMD	PFCR6	PF21MD[2:0] = B'101	PF21/SD_CMD_0/SCK3/**MMC_CMD**
	MMC_D3	PFCR6	PF22MD[2:0] = B'101	PF22/SD_D3_0/RxD3/**MMC_D3**
	MMC_D2	PFCR6	PF23MD[2:0] = B'101	PF23/SD_D2_0/TxD3/**MMC_D2**

Note: Bold text indicates the function used.

Table 4.2.26 SH7269 Multiplexed Pin Functions (MTU2)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
MTU2	TIOC4A	PFCR0	PF0MD [2:0] = B'100	PF0/BREQ#/QSPCLK_1/RSPCK1/**TIOC4A**/DREQ0
	TIOC4C	PFCR0	PF2MD [2:0] = B'100	PF2/WAIT#/QMO_1&QIO0_1/MOSI1/**TIOC4C**/ TEND0
	TIOC4D	PFCR0	PF3MD [2:0] = B'100	PF3/CS2#/QMI_1&QIO1_1/MISO1/**TIOC4D**/ AUDIO_XOUT
	TIOC1A	PJCR6	PJ27MD [2:0] = B'100	PJ27/SGOUT_3/**TIOC1A**/CTS7#

Note: Bold text indicates the function used.

Table 4.2.27 SH7269 Multiplexed Pin Functions (SSIF)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
SSIF	SSITxD0	PFCR1	PF6MD[2:0] = B'010	PF6/CE2A#/**SSITxD0**/SGOUT_2
	SSIWS0	PFCR1	PF5MD[2:0] = B'010	PF5/**SSIWS0**/SGOUT_1
	SSISCK0	PFCR1	PF4MD[2:0] = B'010	PF4/CS5#/CE1A#/**SSIWS0**/SGOUT_0

Note: Bold text indicates the function used.

Table 4.2.28 SH7269 Multiplexed Pin Functions (ADC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
ADC	AN7	PHCR1	PH7MD[1:0] = B'01	PH7/**AN7**/PINT7
	AN6	PHCR1	PH6MD[1:0] = B'01	PH6/**AN6**/PINT6
	AN5	PHCR1	PH5MD[1:0] = B'01	PH5/**AN5**/PINT5/LCD_EXTCLK
	AN4	PHCR1	PH4MD[1:0] = B'01	PH4/**AN4**/PINT4
	AN3	PHCR0	PH3MD[1:0] = B'01	PH3/**AN3**/PINT3
	AN2	PHCR0	PH2MD[1:0] = B'01	PH2/**AN2**/PINT2
	AN1	PHCR0	PH1MD[1:0] = B'01	PH1/**AN1**/PINT1
	AN0	PHCR0	PH0MD[1:0] = B'01	PH0/**AN0**/PINT0

Note: Bold text indicates the function used.

Table 4.2.29 SH7269 Multiplexed Pin Functions (VDC4)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
VDC4	DV_HSYNC	PECR1	PE5MD [1:0] = B'11	PE5/SDA2/RxD5/**DV_HSYNC**
	DV_VSYNC	PECR1	PE4MD [1:0] = B'11	PE4/SCL2/RxD4/**DV_VSYNC**
	DV_CLK	PJCR7	PJ31MD = B'1	PJ31/**DV_CLK**
	DV_DATA7	PJCR1	PJ7MD [2:0] = B'001	PJ7/**DV_DATA7**/LCD_DATA7/SD_D2_1/PWM1H
	DV_DATA6	PJCR1	PJ6MD [2:0] = B'001	PJ6/**DV_DATA6**/LCD_DATA6/SD_D3_1/PWM1G
	DV_DATA5	PJCR1	PJ5MD [2:0] = B'001	PJ5/**DV_DATA5**/LCD_DATA5/SD_CMD_1/PWM1F
	DV_DATA4	PJCR1	PJ4MD [2:0] = B'001	PJ4/**DV_DATA4**/LCD_DATA4/SD_CLK_1/PWM1E
	DV_DATA3	PJCR0	PJ3MD [2:0] = B'001	PJ3/**DV_DATA3**/LCD_DATA3/SD_D0_1/PWM1D
	DV_DATA2	PJCR0	PJ2MD [2:0] = B'001	PJ2/**DV_DATA2**/LCD_DATA2/SD_D1_1/PWM1C
	DV_DATA1	PJCR0	PJ1MD [2:0] = B'001	PJ1/**DV_DATA1**/LCD_DATA1/SD_WP_1/PWM1B
	DV_DATA0	PJCR0	PJ0MD [2:0] = B'001	PJ0/**DV_DATA0**/LCD_DATA0/SD_CD_1/PWM1A
	LCD_EXTCLK	PGCR6	PG27MD[1:0] = B'11	PG27/LCD_TCON2/**LCD_EXTCLK**
	LCD_CLK	PGCR6	PG24MD[1:0] = B'10	PG24/**LCD_CLK**
	LCD_TCON6	PJCR5	PJ23MD[2:0] = B'011	PJ23/DV_DATA23/LCD_DATA23/**LCD_TCON6**/ IRQ3/CTx1/CTx0&CTx1
	LCD_TCON5	PJCR5	PJ22MD[2:0] = B'011	PJ22/DV_DATA22/LCD_DATA22/**LCD_TCON5**/ IRQ2/CRx1/CRx0/CRx1
	LCD_TCON1	PGCR6	PG26MD[1:0] = B'10	PG26/**LCD_TCON1**
	LCD_TCON0	PGCR6	PG25MD[1:0] = B'10	PG25/**LCD_TCON0**
	LCD_DATA23	PGCR5	PG23MD[2:0] = B'010	PG23/**LCD_DATA23**/LCD_TCON6/TxD5/AUDATA3
	LCD_DATA22	PGCR5	PG22MD[2:0] = B'010	PG22/**LCD_DATA22**/LCD_TCON5/RxD5/AUDSYNC#
	LCD_DATA21	PGCR5	PG21MD[2:0] = B'010	PG21/DV_DATA7/**LCD_DATA21**/LCD_TCON4/TxD4/ AUDATA2
	LCD_DATA20	PGCR5	PG20MD[2:0] = B'010	PG20/DV_DATA6/**LCD_DATA20**/LCD_TCON3/RxD4
	LCD_DATA19	PGCR4	PG19MD[2:0] = B'010	PG19/DV_DATA5/**LCD_DATA19**/SPDIF_OUT/SCK5
	LCD_DATA18	PGCR4	PG18MD[2:0] = B'010	PG18/DV_DATA4/**LCD_DATA18**/SPDIF_IN/SCK4
	LCD_DATA17	PGCR4	PG17MD[1:0] = B'10	PG17/WE3#/ICIOWR#/AH/DQMUU/**LCD_DATA17**/ AUDATA1
	LCD_DATA16	PGCR4	PG16MD[1:0] = B'10	PG16/WE2#/ICIORD#/DQMUL/**LCD_DATA16**/ AUDATA0
	LCD_DATA15	PGCR3	PG15MD[1:0] = B'10 (1)	PG15/D31/**LCD_DATA15**/PINT7
	LCD_DATA14	PGCR3	PG14MD[1:0] = B'10 (1)	PG14/D30/**LCD_DATA14**/PINT6
	LCD_DATA13	PGCR3	PG13MD[1:0] = B'10 (1)	PG13/D29/**LCD_DATA13**/PINT5
	LCD_DATA12	PGCR3	PG12MD[1:0] = B'10 (1)	PG12/D28/**LCD_DATA12**/PINT4
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'010(1)	PG11/D27/**LCD_DATA11**/PINT3/TIOC3D
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'010 1)	PG10/D26/**LCD_DATA10**/PINT2/TIOC3C
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'010 (1)	PG9/D25/**LCD_DATA9**/PINT1/TIOC3B
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'010 (1)	PG8/D24/**LCD_DATA8**/PINT0/TIOC3A
	LCD_DATA7	PGCR1	PG7MD[2:0] = B'010 (1)	PG7/D23/**LCD_DATA7**/IRQ7/TIOC2B
	LCD_DATA6	PGCR1	PG6MD[2:0] = B'010 (1)	PG6/D22/**LCD_DATA6**/IRQ6/TIOC2A
	LCD_DATA5	PGCR1	PG5MD[2:0] = B'010 (1)	PG5/D21/**LCD_DATA5**/IRQ5/TIOC1B
	LCD_DATA4	PGCR1	PG4MD[2:0] = B'010 (1)	PG4/D20/**LCD_DATA4**/IRQ4/TIOC1A
	LCD_DATA3	PGCR0	PG3MD[2:0] = B'010 (1)	PG3/D19/**LCD_DATA3**/IRQ3/TIOC0D
	LCD_DATA2	PGCR0	PG2MD[2:0] = B'010 (1)	PG2/D18/**LCD_DATA2**/IRQ2/TIOC0C
	LCD_DATA1	PGCR0	PG1MD[2:0] = B'010 (1)	PG1/D17/**LCD_DATA1**/IRQ1/TIOC0B
	LCD_DATA0	PGCR0	PG0MD[2:0] = B'010 (1)	PG0/D16/**LCD_DATA0**/IRQ0/TIOC0A

Notes: 1. These values must not be set in boot mode 1.

2. Bold text indicates the function used.

Table 4.2.30 SH7269 Multiplexed Pin Functions (PWM)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
PWM	PWM2H	PJCR3	PJ15MD[2:0] = B'100	PJ15/DV_DATA15/LCD_DATA15/PINT7/**PWM2H**/TxD7
	PWM2G	PJCR3	PJ14MD[2:0] = B'100	PJ14/DV_DATA14/LCD_DATA14/PINT6/**PWM2G**/TxD6
	PWM2F	PJCR3	PJ13MD[2:0] = B'100	PJ13/DV_DATA13/LCD_DATA13/PINT5/**PWM2F**/TxD5
	PWM2E	PJCR3	PJ12MD[2:0] = B'100	PJ12/DV_DATA12/LCD_DATA12/PINT4/**PWM2E**/SCK7
	PWM2D	PJCR2	PJ11MD[2:0] = B'100	PJ11/DV_DATA11/LCD_DATA11/PINT3/**PWM2D**/SCK6
	PWM2C	PJCR2	PJ10MD[2:0] = B'100	PJ10/DV_DATA10/LCD_DATA10/PINT2/**PWM2C**/SCK5
	PWM2B	PJCR2	PJ9MD[2:0] = B'100	PJ9/DV_DATA9/LCD_DATA9/PINT1/**PWM2B**/RTS5#
	PWM2A	PJCR2	PJ8MD[2:0] = B'100	PJ8/DV_DATA8/LCD_DATA8/PINT0/**PWM2A**/CTS5#
	PWM1H	PJCR1	PJ7MD[2:0] = B'100	PJ7/DV_DATA7/LCD_DATA7/SD_D2_1/**PWM1H**
	PWM1G	PJCR1	PJ6MD[2:0] = B'100	PJ6/DV_DATA6/LCD_DATA6/SD_D3_1/**PWM1G**
	PWM1F	PJCR1	PJ5MD[2:0] = B'100	PJ5/DV_DATA5/LCD_DATA5/SD_CMD_1/**PWM1F**
	PWM1E	PJCR1	PJ4MD[2:0] = B'100	PJ4/DV_DATA4/LCD_DATA4/SD_CLK_1/**PWM1E**
	PWM1D	PJCR0	PJ3MD[2:0] = B'100	PJ3/DV_DATA3/LCD_DATA3/SD_D0_1/**PWM1D**
	PWM1C	PJCR0	PJ2MD[2:0] = B'100	PJ2/DV_DATA2/LCD_DATA2/SD_D1_1/**PWM1C**
	PWM1B	PJCR0	PJ1MD[2:0] = B'100	PJ1/DV_DATA1/LCD_DATA1/SD_WP_1/**PWM1B**
	PWM1A	PJCR0	PJ0MD[2:0] = B'100	PJ0/DV_DATA0/LCD_DATA0/SD_CD_1/**PWM1A**

Note: Bold text indicates the function used.

Table 4.2.31 SH7269 Multiplexed Pin Functions (PORT)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Register Name	MD Bit Setting	
PORT	PJ16	PJCR4	PJ16MD[2:0] = B'000	**PJ16**/DV_DATA16/LCD_DATA16/RSPCK0/TIOC0A/ SIOFSCK
	PJ17	PJCR4	PJ17MD[2:0] = B'000	**PJ17**/DV_DATA17/LCD_DATA17/SSL00/TIOC0B/ SIOFSYNC
	PJ18	PJCR4	PJ18MD[2:0] = B'000	**PJ18**/DV_DATA18/LCD_DATA18/MOSI0/TIOC0C/ SIOFTxD
	PJ19	PJCR4	PJ19MD[2:0] = B'000	**PJ19**/DV_DATA19/LCD_DATA19/MISO0/TIOC0D/ SIOFRxD/AUDIO_XOUT
	PJ0	PJCR0	PJ0MD[2:0] = B'000	**PJ0**/DV_DATA0/LCD_DATA0/SD_CD_1/PWM1A
	PJ1	PJCR0	PJ1MD[2:0] = B'000	**PJ1**/DV_DATA1/LCD_DATA1/SD_WP_1/PWM1B
	PJ2	PJCR0	PJ2MD[2:0] = B'000	**PJ2**/DV_DATA2/LCD_DATA2/SD_D1_1/PWM1C
	PJ3	PJCR0	PJ3MD[2:0] = B'000	**PJ3**/DV_DATA3/LCD_DATA3/SD_D0_1/PWM1D
	PJ4	PJCR1	PJ4MD[2:0] = B'000	**PJ4**/DV_DATA4/LCD_DATA4/SD_CLK_1/PWM1E
	PJ5	PJCR1	PJ5MD[2:0] = B'000	**PJ5**/DV_DATA5/LCD_DATA5/SD_CMD_1/PWM1F
	PJ6	PJCR1	PJ6MD[2:0] = B'000	**PJ6**/DV_DATA6/LCD_DATA6/SD_D3_1/PWM1G
	PJ7	PJCR1	PJ7MD[2:0] = B'000	**PJ7**/DV_DATA7/LCD_DATA7/SD_D2_1/PWM1H
	PE2	PECR0	PE2MD [2:0] = B'000	**PE2**/SCL1/TCLKD/IOIS16#/DV_VSYNC
	PE3	PECR0	PE3MD [1:0] = B'000	**PE3**/SDA1/TCLKD/ADTRG#/DV_VSYNC
	PE6	PECR1	PE6MD [1:0] = B'00	**PE6**/ SCL3/RxD6
	PE7	PECR1	PE7MD [1:0] = B'00	**PE7**/SDA3/RxD7
	PF7	PFCR1	PF7MD [2:0] = B'000	**PF7**/CE2B/SSIRxD0/RxD0/SGOUT_3/CTS1#
	PF9	PFCR2	PF9MD [2:0] = B'000	**PF9**/BS#/DV_DATA0/SCK0/MMC_D4/RTS1#

Note: Bold text indicates the function used.

4.3 LCD Module Interface

4.3.1 LCD Module Interface

The M3A-HS64G02 includes two flexible connectors and one MIL-spec connector for connecting LCD modules. The SH7269 on-chip Video Display Controller (VDC4) controls the LCD modules.

Figure 4.3.1 shows the LCD module interface block diagram.

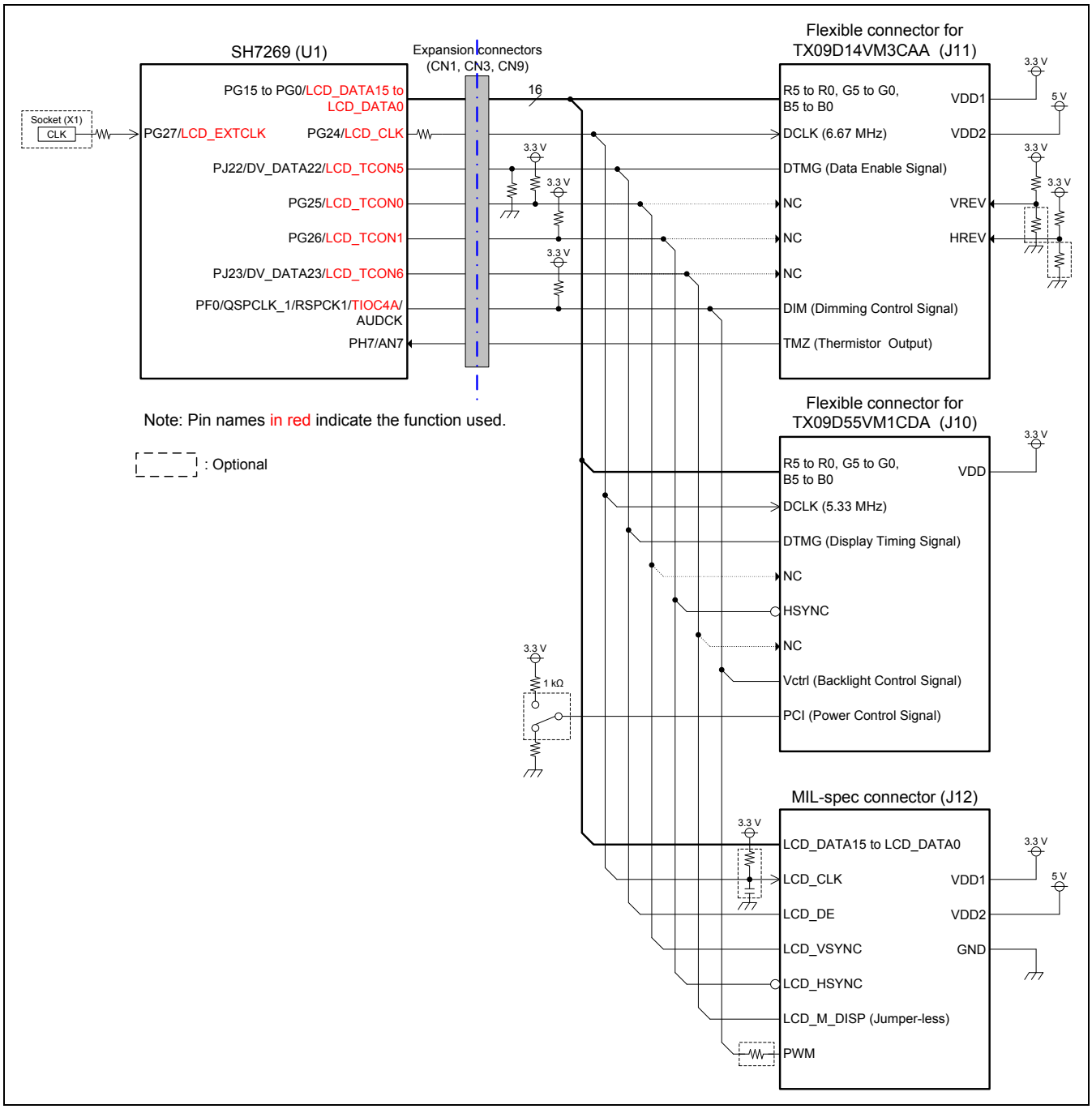

Figure 4.3.1 LCD Module Interface Block Diagram

4.3.2 Character LCD Module with LED Backlight

The M3A-HS64G02 includes a connector for 16 × 2 semi-transmissive character LCD module (SD1602H, Sunlike). The SH7269 general-purpose port output controls the character LCD modules. The M3A-HS64G02 is intended only for writing from the SH7269 to the character LCD modules. Therefore, the character LCD module R/W signal is fixed low.

The M3A-HS64G02 also includes a variable resistor (VR1) for the LCD driver voltage adjustment to control the LCD contrast and a variable resistor (VR2) for LCD backlight adjustment.

SH7269 PJ7 to PJ0 pins are multiplexed with VDC4 pins on the R0K572690C000BR, and the module to use is specified by SW6-3 on the R0K572690C000BR. On the M3A-HS64G02, PJ7 to PJ0 pins are multiplexed with the SDHI pins and PWM output pins. SDHI and PWM output cannot be used when using the character LCD module on the M3A-HS64G02. Figure 4.3.2 shows the character LCD module block diagram. Table 4.3.1 lists the DIP switches setting (SW6-3). Table 4.3.2 lists the M3A-HS64G02 jumper setting (JP3).

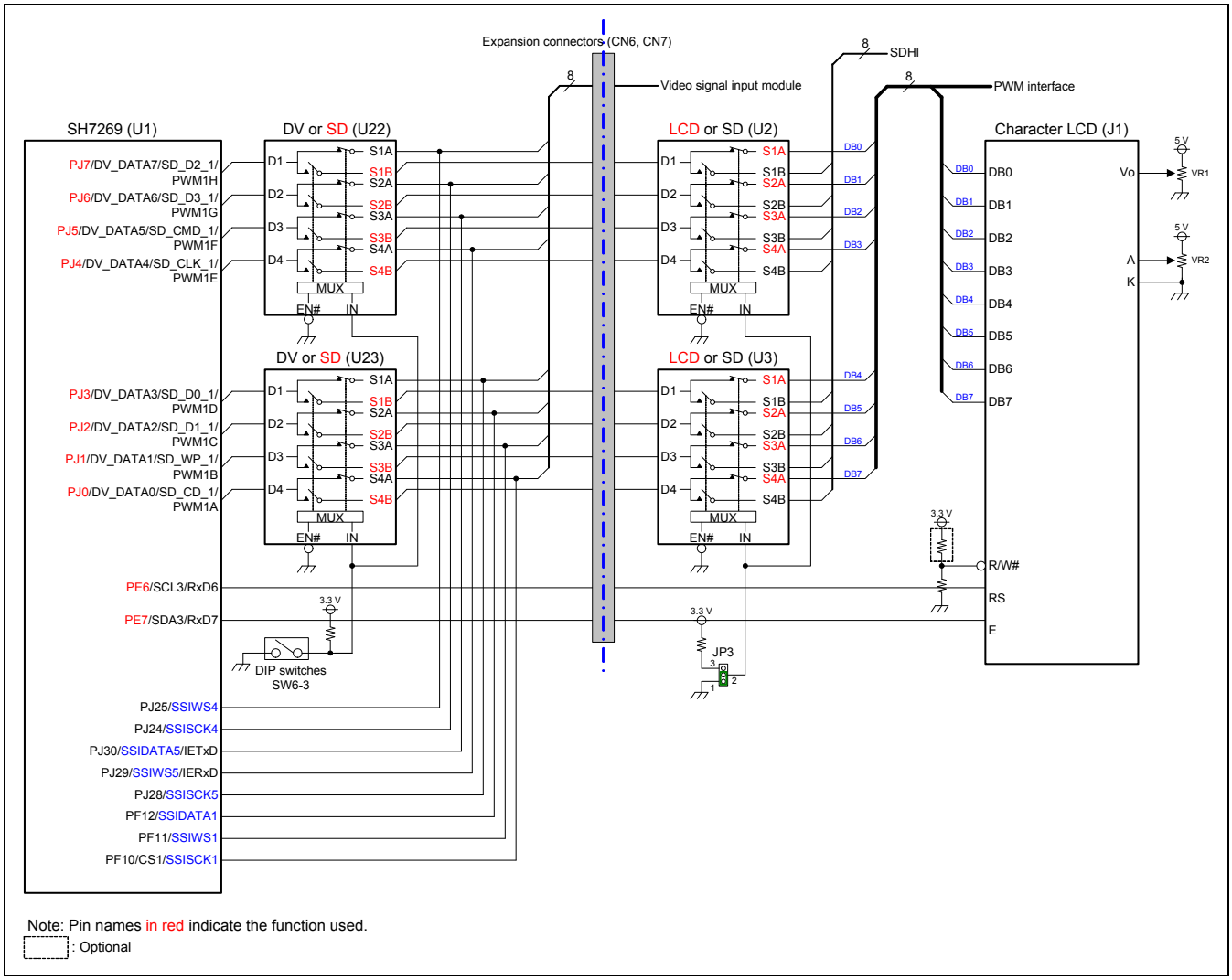

Figure 4.3.2 Character LCD Module Block Diagram

Table 4.3.1 R0K572690C000BR DIP Switches (SW6-3)

Number	Function	
	OFF (High)	ON (Low)
SW6-3	Connected to the SDHI/character LCD interface (default)	Connected to VDC4

Note: Shading indicates the function to be set.

Table 4.3.2 M3A-HS64G02 Jumper Setting (JP3)

Number	1-2 (Low)	2-3 (High)
JP3	Connected to the PWM/character LCD interface (default)	Connected to the SDHI

Note: Shading indicates the function to be set.

4.4 Audio Modules

The M3A-HS64G02 includes a 96 kHz 25-bit D/A Converter with DIT (AK4353, Asahi Kasei Microdevices Corporation).

- AK4353 D/A Converter
  SH7269 IIC3, SSIF, and I/O ports control the AK4353.
  - SH7269 IIC3 (channel 1): Accesses the AK4353 registers to initialize AK4353, format data, and configure the attenuator
  - SH7269 SSIF (channel 0): Outputs the audio data
  - SH7269 I/O ports (PF7): Powers down the AK4353 at low, powers up the AK4353 at high

Figure 4.4.1 shows the D/A Converter block diagram. Table 4.4.1 lists jumper settings (JP1 to JP3) on the M3A-HS64G02.

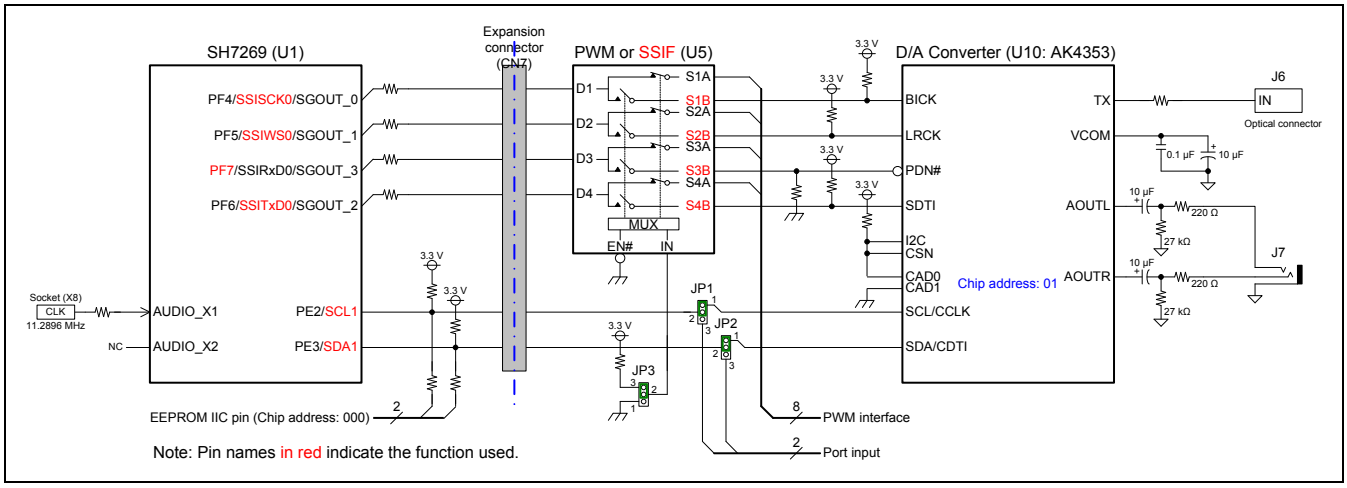

Figure 4.4.1 D/A Converter Block Diagram

Table 4.4.1 M3A-HS64G02 Jumper Settings (JP1 to JP3)

Number	1-2	2-3
JP1	IIC3 mode (Set PE2 as SCL1 output pin)	IRQ mode (Set PE2 as IRQ2 input pin, default)
JP2	IIC3 mode (Set PE3 as SDA1 I/O pin)	IRQ2 mode (SET PE3 as IRQ3 input pin, default)
JP3	Connected to the PWM interface (low level, default) Note: Only one channel can be used on the R0K572690C000BR	Connected to the SSIF (high level)

Note: Shading indicates the function to be set.

4.5 Video Signal Input Module

M3A-HS64G02 includes a video decoder IC (AK8851, Asahi Kasei Microdevices Corporation). M3A-HS64G02 also includes an RCA connector and an S-Video connector to input NTSC and PAL video signal, and inputs the digital signals to the SH7269 VDC4 module via the video decoder IC. VDC4 pins are also used as the SDHI and PWM pins. The SH7269 on-chip IIC3 controls the video decoder.

Figure 4.5.1 shows the video signal input module block diagram.

Table 4.5.1 lists the system-setting DIP switches setting (SW6-3 on the M3A-HS64G02).

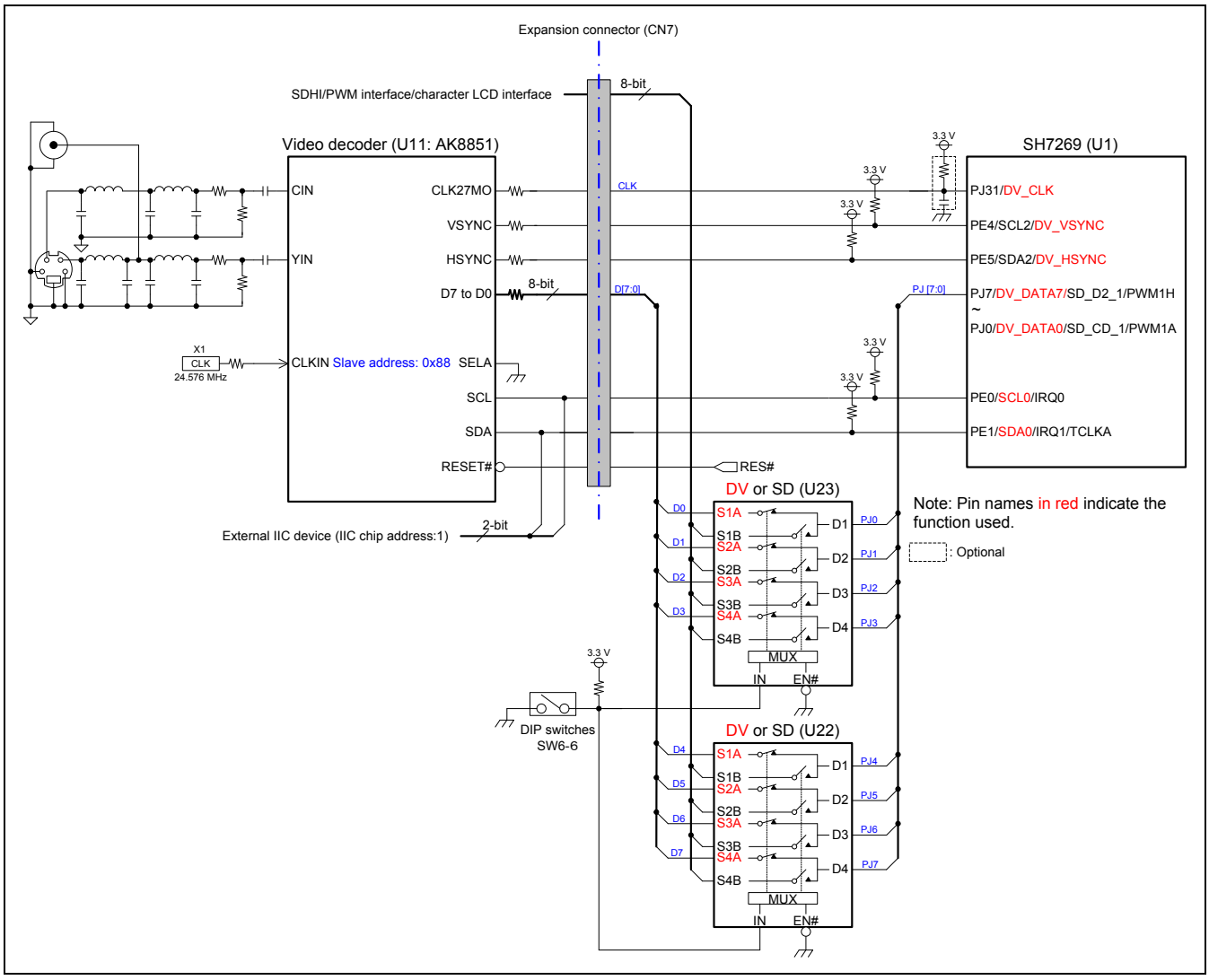

Figure 4.5.1 Video Signal Input Module Block Diagram

Table 4.5.1 R0K572690C000BR System Setting DIP Switches Setting (SW6-3)

Number	Function	
	OFF (High)	ON (Low)
SW6-3	Connected to the SDHI/PWM/character LCD interface (default)	Connected to VDC4

Note: Shading indicates the function to be set.

4.6 SD Card Interface

The M3A-HS64G02 includes an SD card slot. The SD card slot is connected to the SD Host Interface (SDHI) and the SH7269 SD card slot.

SDHI pins are multiplexed with VDC4, character LCD module, and PWM. When using the SDHI, do not use the video signal input module, character LCD module, and PWM interface.

Figure 4.6.1 shows the SD card interface block diagram. Table 4.6.1 lists the DIP switches setting (SW6-3). Table 4.6.2 lists the M3A-HS64G02 jumper setting (JP3).

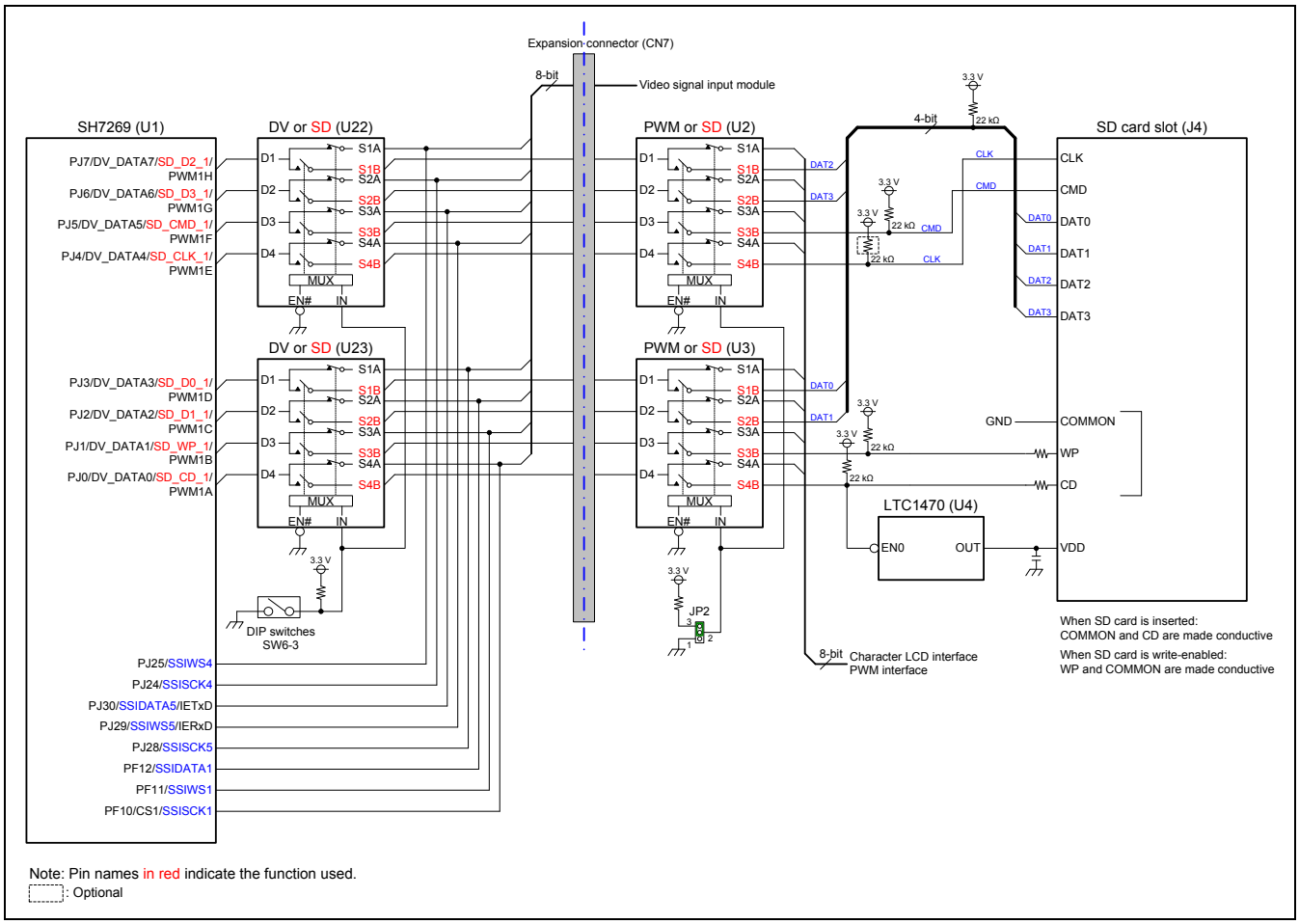

Figure 4.6.1 SD Card Interface Block Diagram

Table 4.6.1 DIP Switches Setting (SW6-3)

Number	Function	
	OFF (High)	ON (Low)
SW6-3	Connected to the SDHI/PWM/character LCD interface (default)	Connected to VDC4

Note: Shading indicates the function to be set.

Table 4.6.2 M3A-HS64G02 Jumper Setting (JP3)

Number	1-2	2-3
JP3	Connected to the character LCD interface (default)	Connected to the SDHI

Note: Shading indicates the function to be set.

4.7 UART Interface

The SH7269 includes a Serial Communication Interface with FIFO (SCIF). SCIF channel 5 RxD5 pin and TxD5 pin are connected to the UART connector (7-pin, 2.5 mm pitch) on the M3A-HS64G02 at TTL level.

SCIF channel 5 RxD5 pin is multiplexed with VDC4 LCD_DATA22 pin and AUD AUDSYNC# pin. SCIF channel TxD5 pin is multiplexed with VDC4 LCD_DATA23 pin and AUD AUDATA3 pin.

Figure 4.7.1 shows the UART interface block diagram.

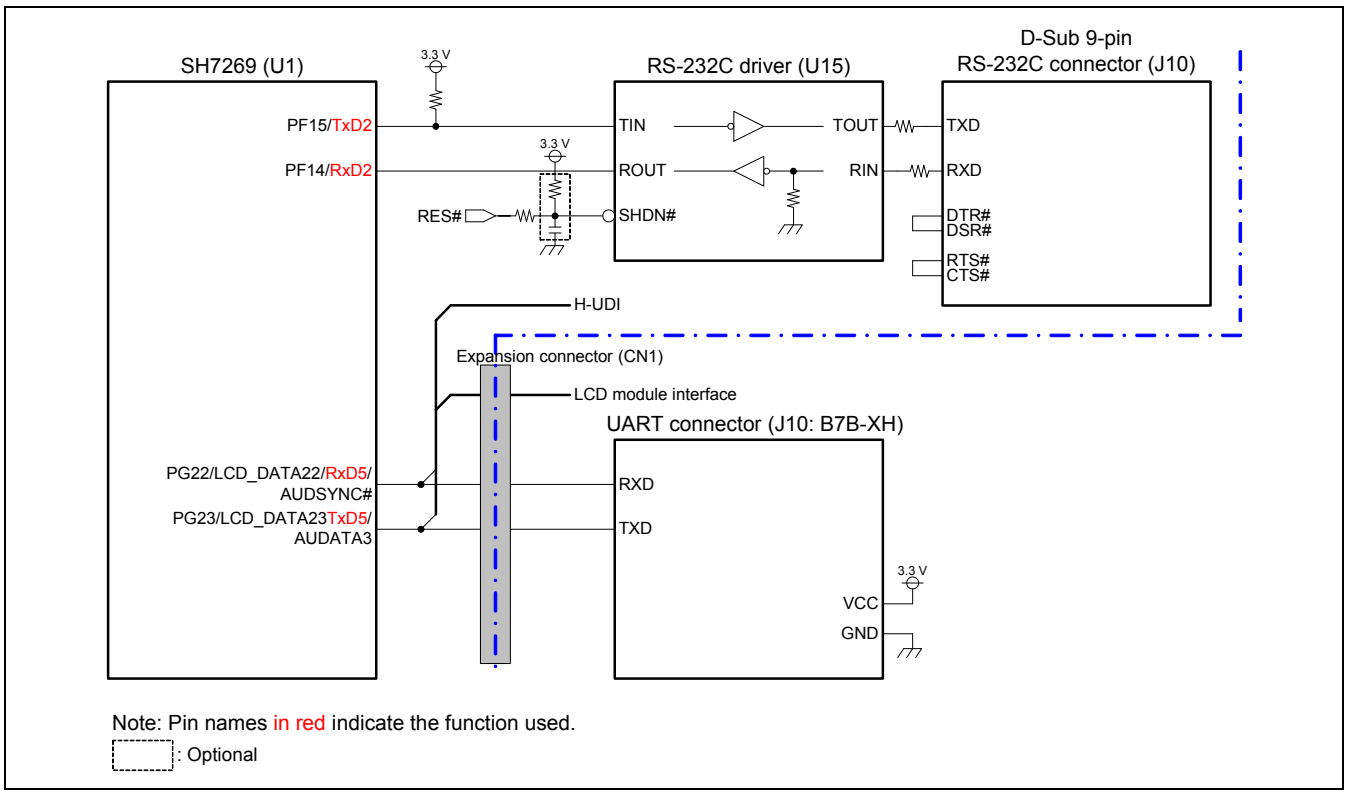

Figure 4.7.1 UART Interface Block Diagram

4.8 CAN Interface

The SH7269 includes RCAN-TL1 (Renesas CAN Time Trigger Level 1), the Controller Area Network. Two channels of the SH7269 RCAN-TL1 are connected to the CAN connector (3-pin, 2.5 mm pitch) on the M3A-HS64G02 via the voltage level shifter and the CAN driver IC. Note that only RCAN-TL1 channel 2 can be used on the R0K572690C000BR.

RCAN-TL1 channel 2 pins are multiplexed with IRQ input pins and Video Display Controller 4 (VDC4) pins.

Figure 4.8.1 shows the CAN interface block diagram. Table 4.8.1 lists jumper settings (JP8 and JP9). Table 4.8.2 and Table 4.8.3 list M3A-HS64G02 jumper settings (JP4, JP5, JP8, and JP9).

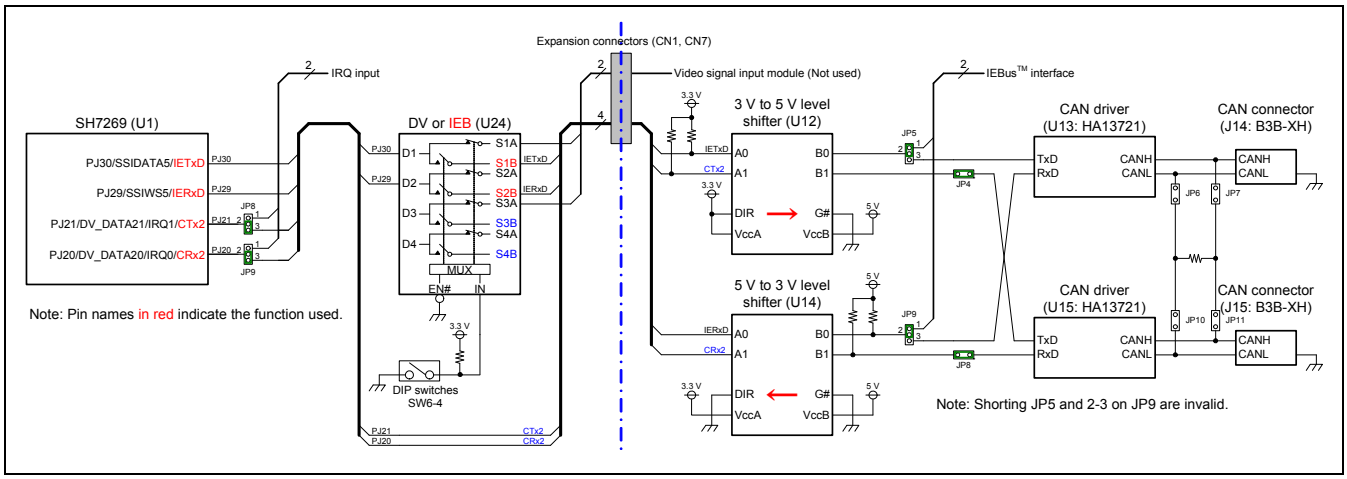

Figure 4.8.1 CAN Interface Block Diagram

Table 4.8.1 R0K572690C000BR Jumper Settings (JP8, JP9)

Number	1-2	2-3
JP8	Uses PJ21 as IRQ1 input pin (default)	Uses PJ21 as CTx2 output/DV_DATA21 input pin
JP9	Uses PJ20 as IRQ0 input pin (default)	Uses PJ20 as CRx2 input/DV_DATA20 input pin

Note: Shading indicates the function to be set.

Table 4.8.2 M3A-HS64G02 Jumper Settings (JP5, JP9)

Number	1-2	2-3
JP5	Selects IETxD (IEB)	Selects PJ30 (RCAN-TL1) pin (default) (1)
JP9	Selects IERxD (IEB)	Selects PJ29 (RCAN-TL1) pin (default) (1)

Notes: 1. This setting is invalid on the R0K572690C000BR.
2. Shading indicates the function to be set.

Table 4.8.3 M3A-HS64G02 Jumper Settings (JP4, JP8)

Number	1-2	2-3
JP4	Normal mode (Connects CTx1 pin) (default)	Debug mode (Leaves CTx1 pin disconnected)
JP8	Normal mode (Connects CRx1 pin) (default)	Debug mode (Leaves CRx1 pin disconnected)

Note: Shading indicates the function to be set.

4.9 IEBus™ Interface

The SH7269 includes and IEBus™ Controller (IEB). The IEBus™ (Inter Equipment Bus™) is the bus for digital data transfer system on a small scale. The SH7269 IEB pin is connected to the IEBus connector (4-pin, 2.5 mm pitch) via the voltage level shifter and the IEBus™ driver IC on the M3A-HS64G02.

The IEB pin is multiplexed with SSIF channel 5 pin.

Figure 4.9.1 shows the IEBus™ interface block diagram. Table 4.9.1 lists the DIP switches settings (SW6-4). Table 4.9.2 lists jumper settings (JP5 and JP9).

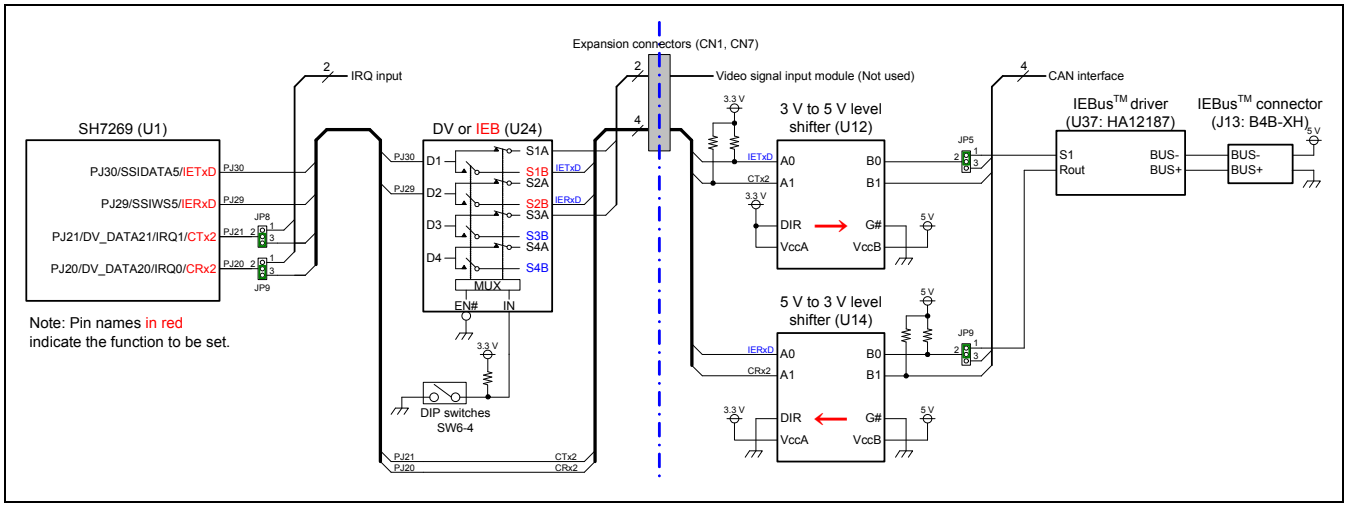

Figure 4.9.1 IEBus™ Interface Block Diagram

Table 4.9.1 R0K572690C000BR DIP Switches Setting (SW6-4)

Number	Function	
	OFF (High)	ON (Low)
SW6-4	Connected to the IEBus™ Interface	Connected to the Video signal input module (Not used, default)

Note: Shading indicates the function to be set.

Table 4.9.2 M3A-HS64G02 Jumper Settings (JP5, JP9)

Number	1-2	2-3
JP5	Selects IETxD (IEB)	Selects PJ30 (RCAN-TL1) pin (default) (1)
JP9	Selects IERxD (IEB)	Selects PJ29 (RCAN-TL1) pin (default) (1)

Notes: 1. This setting is invalid on the R0K572690C000BR.
2. Shading indicates the function to be set.

4.10 PWM Interface

The SH7269 includes two channels of on-chip Motor Control Pulse Width Modulator (PWM) timer with a maximum of eight pulse outputs per channel. The SH7269 PWM channel 1 pin is connected to a 20-pin MIL-spec connector on the M3A-HS64G02 via the voltage level shifter. As PWM channel 2 pin is connected to the PWM output connector (CN11) on the R0K572690C000BR, it cannot be used on the M3A-HS64G02. PWM channel 1 pin is multiplexed with the VDC4, SDHI, and character LCD module.

Figure 4.10.1 shows the PWM interface block diagram. Table 4.10.1 lists the R0K572690C000BR system setting DIP switches (SW6-4). Table 4.10.2 lists the M3A-HS64G02 jumper setting (JP3).

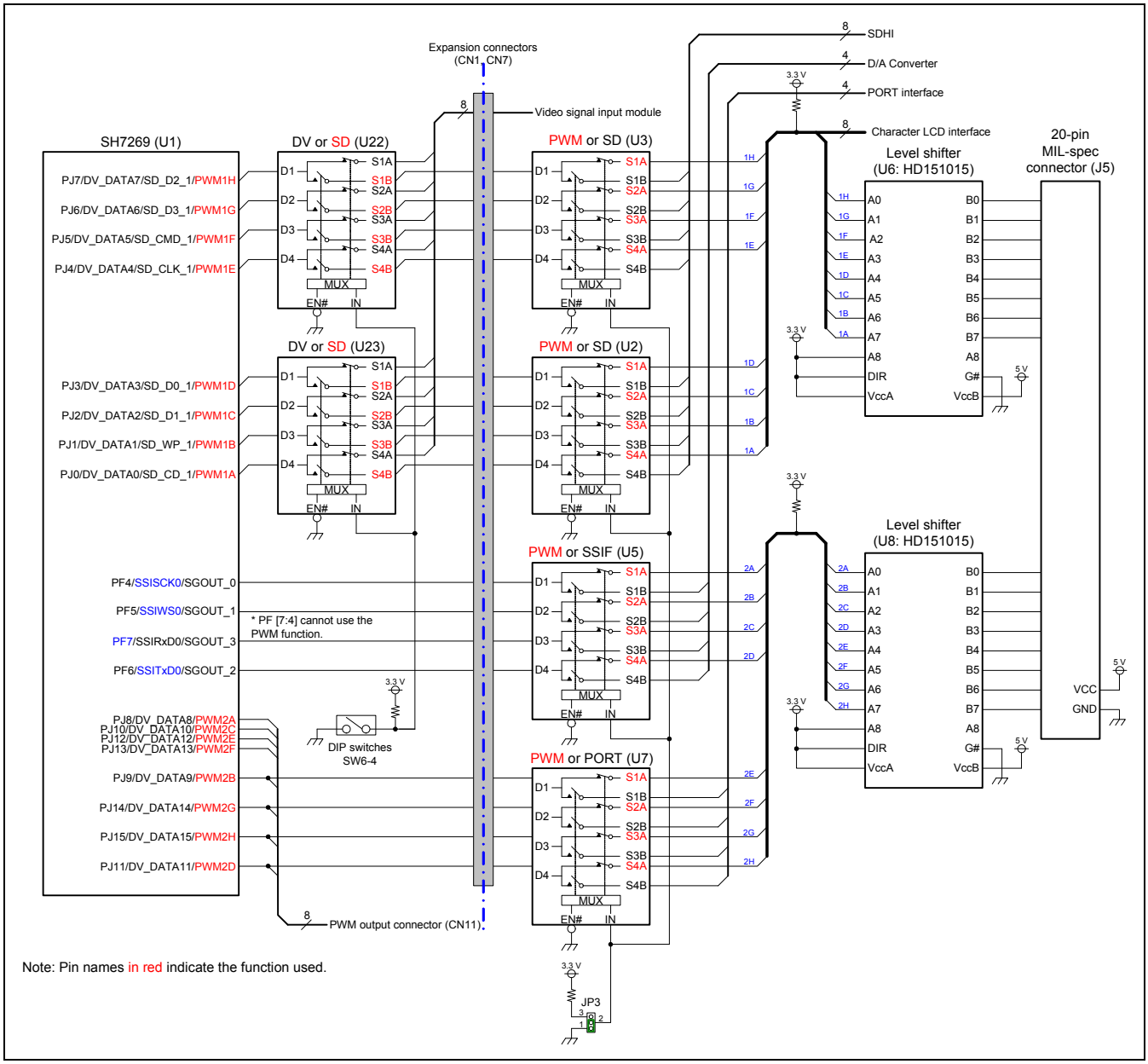

Figure 4.10.1 PWM Interface Block Diagram

Table 4.10.1 R0K572690C000BR System Setting DIP Switches (SW6-4)

Number	Function	
	OFF (High)	ON (Low)
SW6-4	Connected to the SDHI/PWM/character LCD Interface	Connected to the VDC4 (default)

Note: Shading indicates the function to be set.

Table 4.10.2 M3A-HS64G02 Jumper Setting (JP3)

Number	1-2	2-3
JP3	Connected to the PWM interface (default)	Connected to the SDHI/SSIF/PORT interface

Note: Shading indicates the function to be set.

4.11 MTU2 Interface

The SH7269 includes a Multi Function Timer Pulse Unit 2 (MTU2) consists of five channels of 16-bit timer counter. LEDs are connected to MTU2 pins to control LED brightness on the M3A-HS64G02. PF0/TIOC4A, PF2/TIOC4C, PF3/TIOC4D, and PJ27/TIOC1A pins are available on the R0K572690C000BR. These pins are multiplexed with the RSPI channel 1 pins. When using serial flash memory 2 by the RSPI, MTU2 cannot be used. Figure 4.11.1 shows the MTU2 interface block diagram.

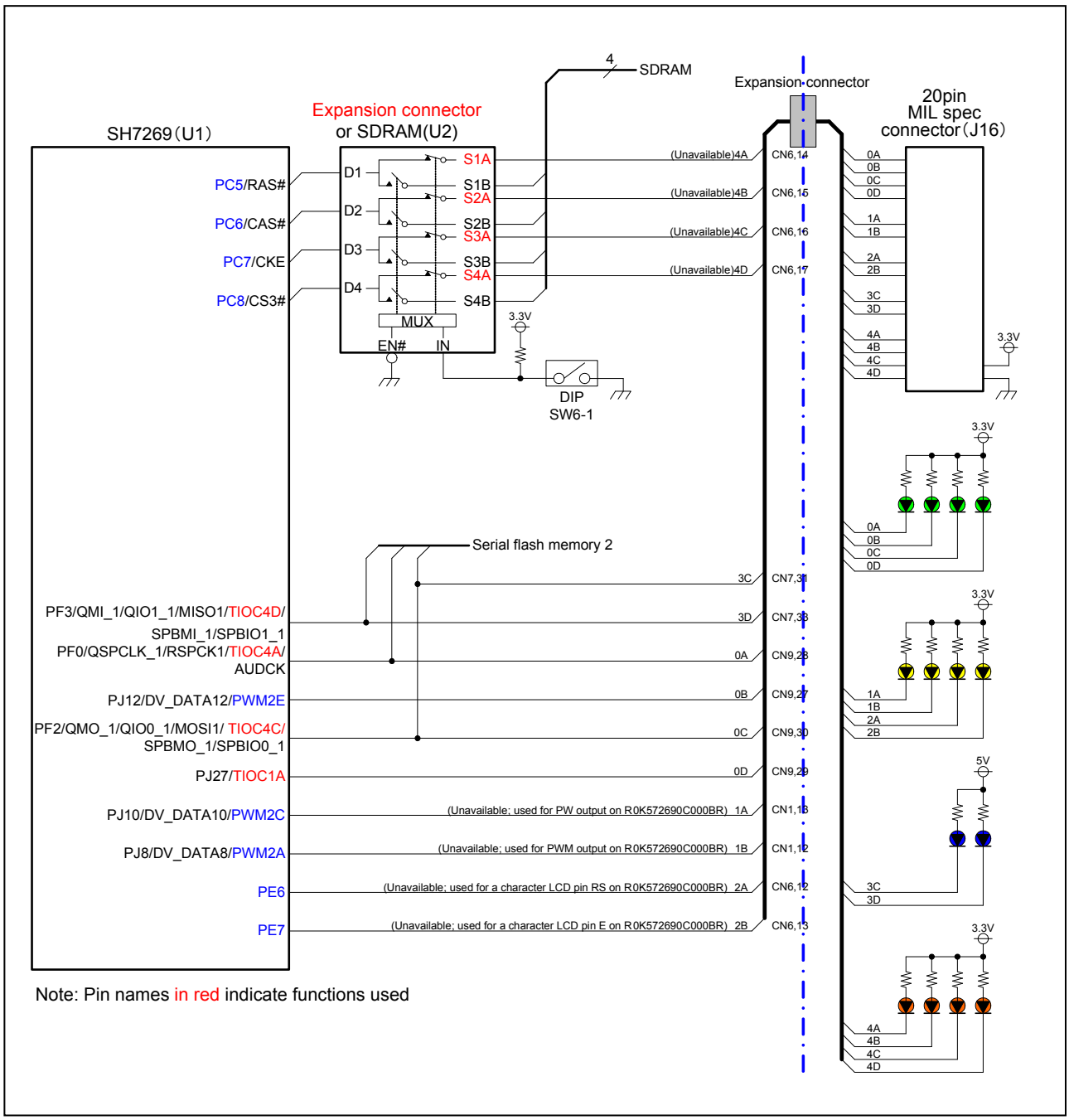

Figure 4.11.1 MTU2 Interface Block Diagram

4.12 I/O Ports

The SH7269 I/O ports are connected to switches and LEDs on the M3A-HS64G02.

To use ports PH0 to PH3 as key input switches (4 switches × 4 inputs) via an A/D Converter (ADC), set the ports as analog input pins (AN0 to AN3).

PJ16 and PJ17 can be used as the user setting switches input. PJ18 and PJ19 can be used as the user LED control output.

Figure 4.12.1 shows the I/O ports block diagram.

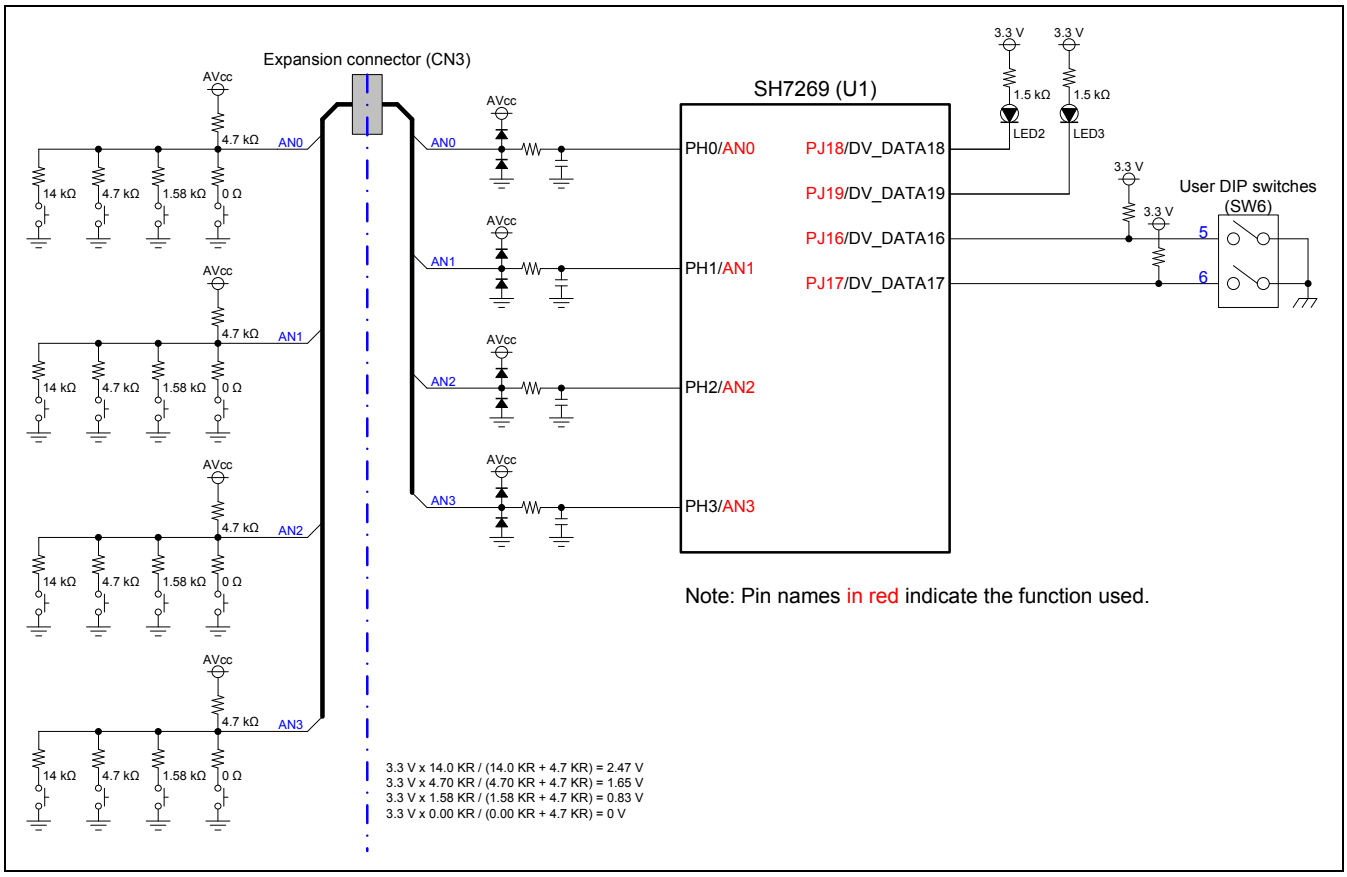

Figure 4.12.1 I/O Ports Block Diagram

4.13 Interrupt Switches

The M3A-HS64G02 includes two push-button switches (SW2 and SW3) for the interrupt signals input, however these switches are connected to general-purpose input port. Use the push-button switch SW4 (IRQ1 switch) on the R0K572690C000BR to input the interrupt signal from the SH7269.

Set jumpers (JP1 and JP2) on the M3A-HS64G02 to use SW2 and SW3 on the M3A-HS64G02 and remove resistors (R42 and R43) on the R0K572690C000BR to avoid the EEPROM malfunction.

Figure 4.13.1 shows the interrupt switches block diagram. Table 4.13.1 lists the M3A-HS64G02 jumper settings (JP1 and JP2).

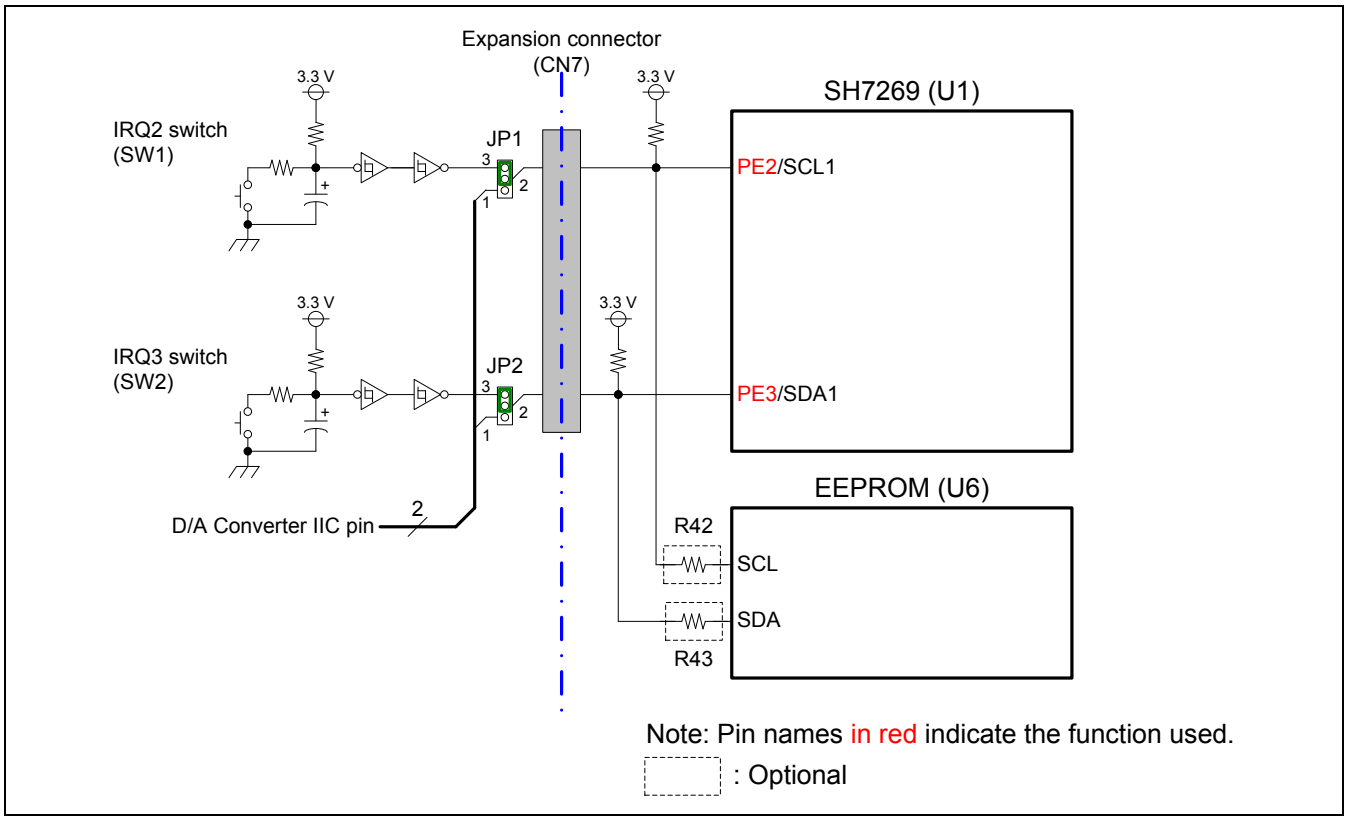

Figure 4.13.1 Interrupt Switches Block Diagram

Table 4.13.1 M3A-HS64G02 Jumper Settings (JP1, JP2)

Number	1-2	2-3
JP1	IIC3 mode [Set PE2 as SCL1 output pin]	IRQ mode [Set PE2 as the general-purpose input pin] (default)
JP2	IIC3 mode [Set PE3 as SDA1 I/O pin]	IRQ mode [Set PE3 as the general-purpose input pin] (default)

Note: Shading indicates the function to be set.

4.14 Clock Modules

Provide following clocks with the SH7269 on the R0K572690C000BR.

- SH7269 input clock (X4): 13.33MHz
- SH7269 RTC clock (X5): 32.768kHz
- SH7269 audio clock (X8): 11.2896MHz
- SH7269 USB clock (X6): 48.00MHz
- SH7269 LCD clock (X1): Optional
- SH7269 digital video decoder clock (X2): 27.00MHz

Figure 4.14.1 shows the clock module block diagram of the R0K572690C000BR and M3A-HS64G02.

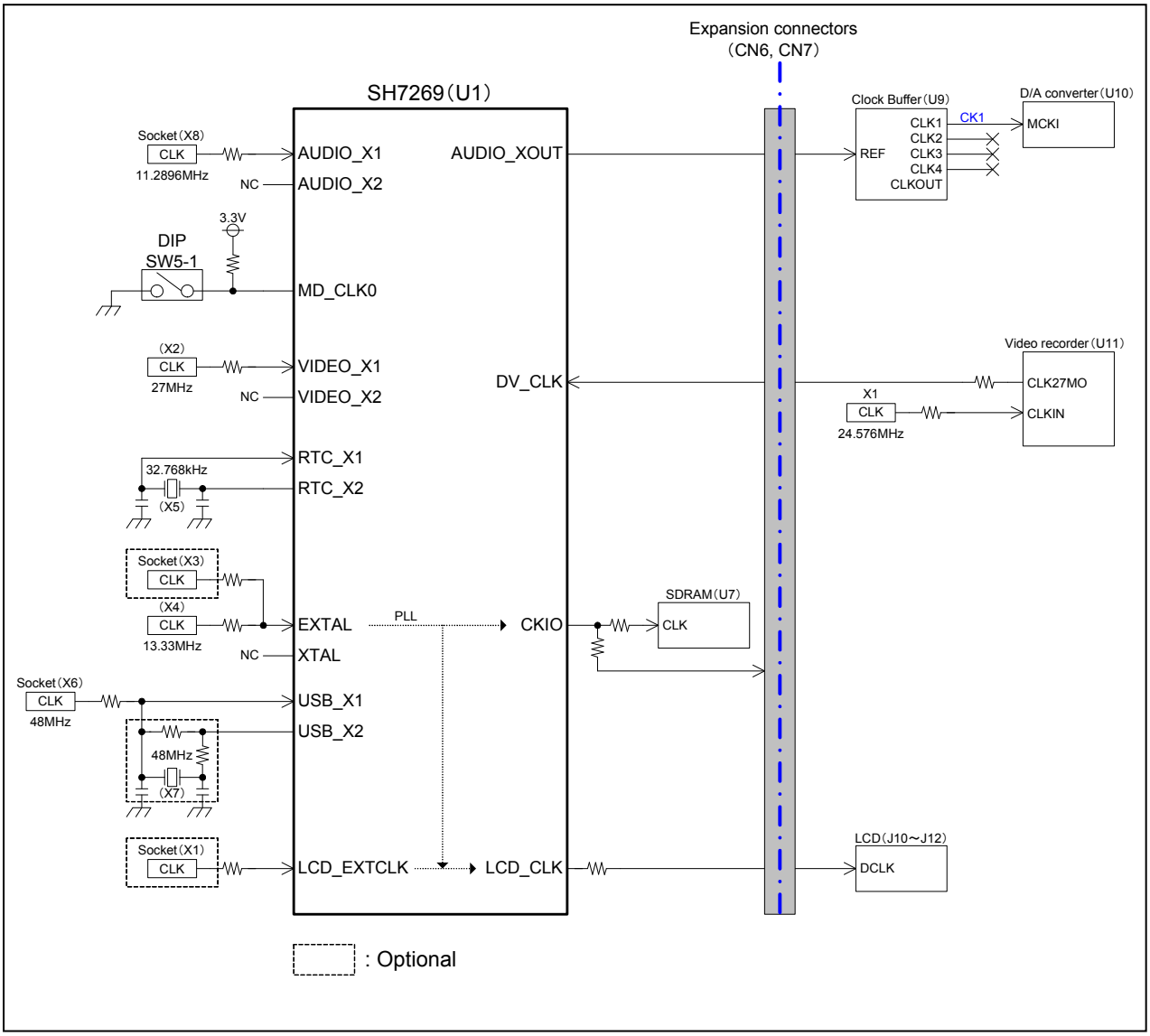

Figure 4.14.1 R0K572690C000BR and M3A-HS64G02 Clock Module Block Diagram

4.15 Reset Module

A reset IC controls reset signals connected to the SH7269, flash memory and peripheral I/Os on the R0K572690C000BR and M3A-HS64G02. There are two system reset options; power-on reset, and reset by switch.

Figure 4.15.1 shows the reset module block diagram.

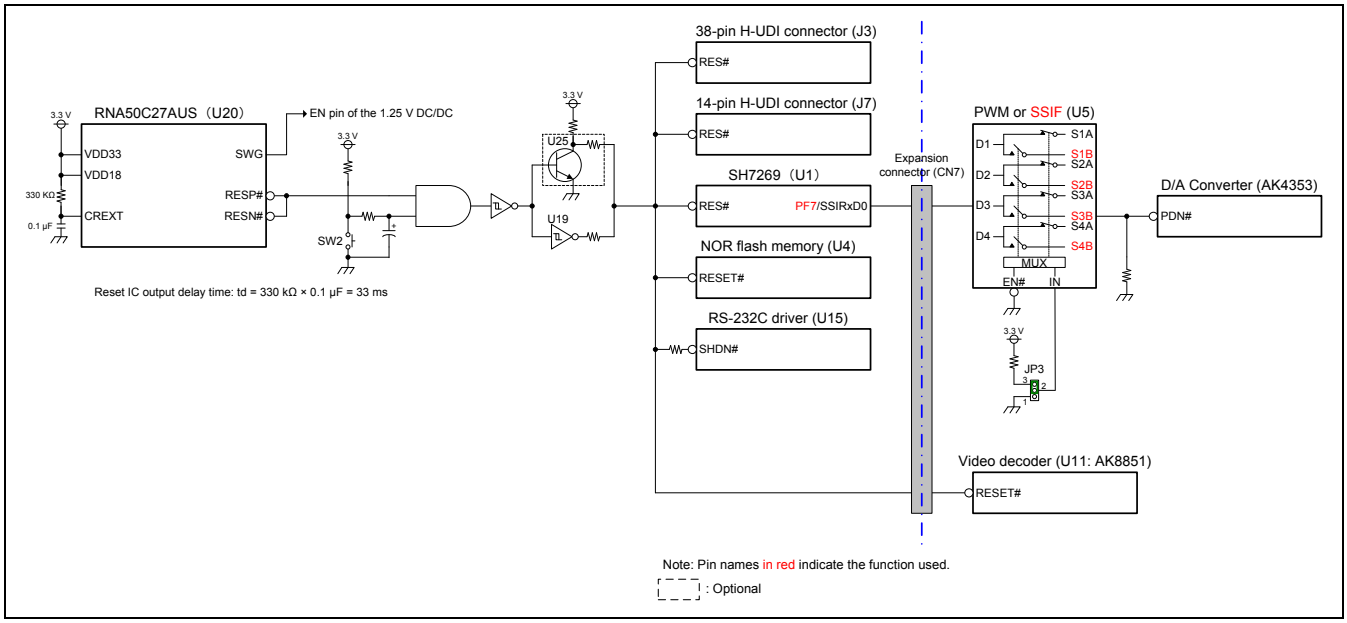

Figure 4.15.1 Reset Module Block Diagram

4.16 Power Supply Module

12 V power supply is input to the M3A-HS64G02, and the voltage regulator on theM3A-HS64G02 generates 8 V voltage, and 5 V voltage. 5 V voltage is provided to the R0K572690C000BR, and the voltage regulator on the R0K572690C000BR generates 3.3 V digital (3VCC) and 3.3 V analog (AVcc).

Figure 4.16.1 shows the power supply module block diagram.

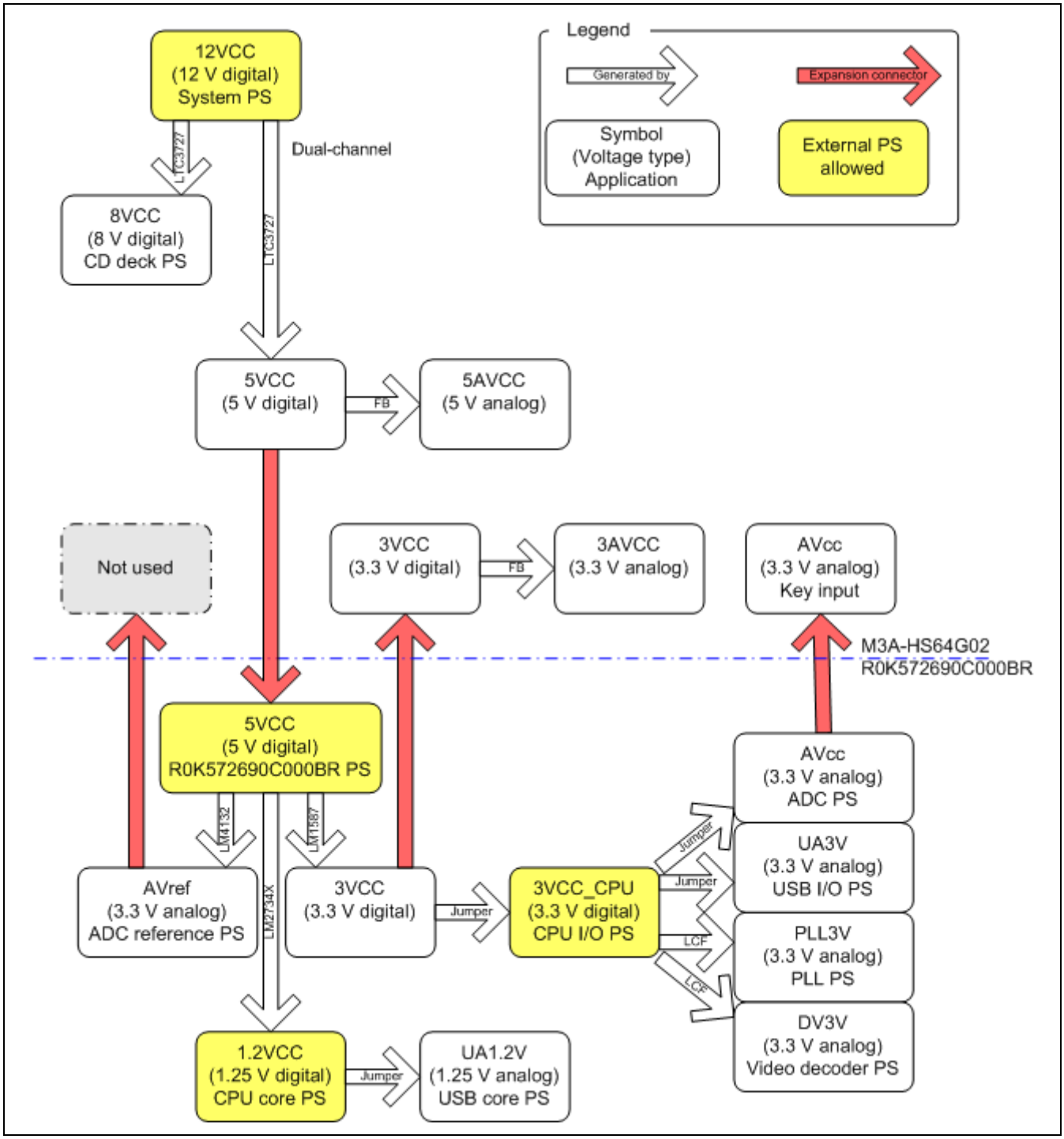

Figure 4.16.1 Power Supply Module Block Diagram

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5.R0K572690C000BR Operating Specification

5.1 Connectors

Figure 5.1.1and Figure 5.1.2 show the connectors for the R0K572690C000BR.

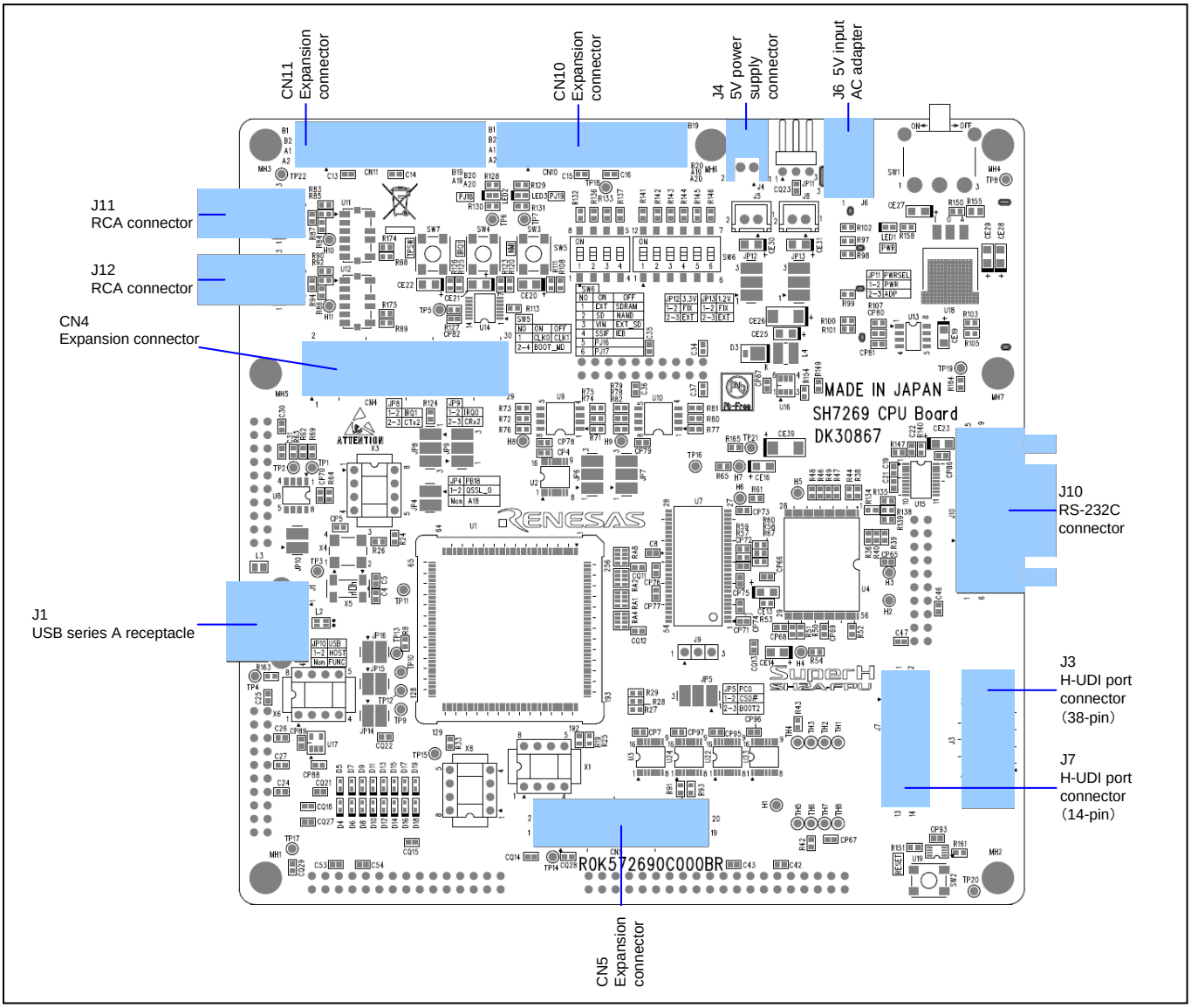


Figure 5.1.1 R0K572690C000BR Connector Assignments (Top view of the component side)

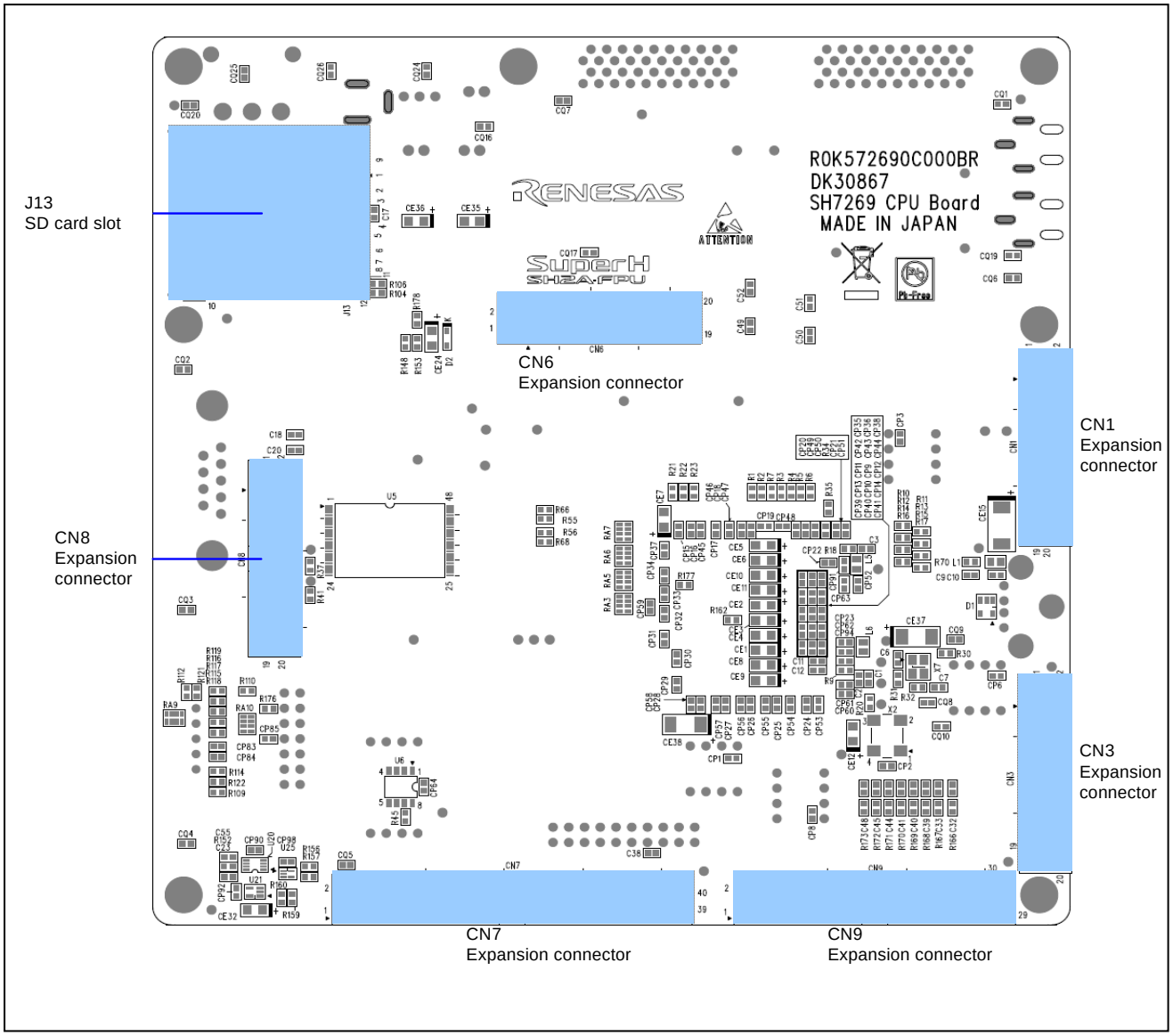


Figure 5.1.2 R0K572690C000BR Connector Assignments (Top view of the solder side)

5.1.1 USB Connectors (J1 and J2)

The R0K572690C000BR includes a USB Series-A receptacle (J1).
Remove the series-A receptacle to connect a USB mini-B receptacle (J2). Refer to Table 1.6.2 in Chapter 1 for the USB mini-B receptacle allowed on the R0K572690C000BR.
Figure 5.1.3 shows the Series-A receptacle pin assignments. Figure 5.1.4 shows the Mini-B receptacle pin assignments. Table 5.1.1and Table 5.1.2 list the pin descriptions for Series-A and Mini-B receptacles, respectively.

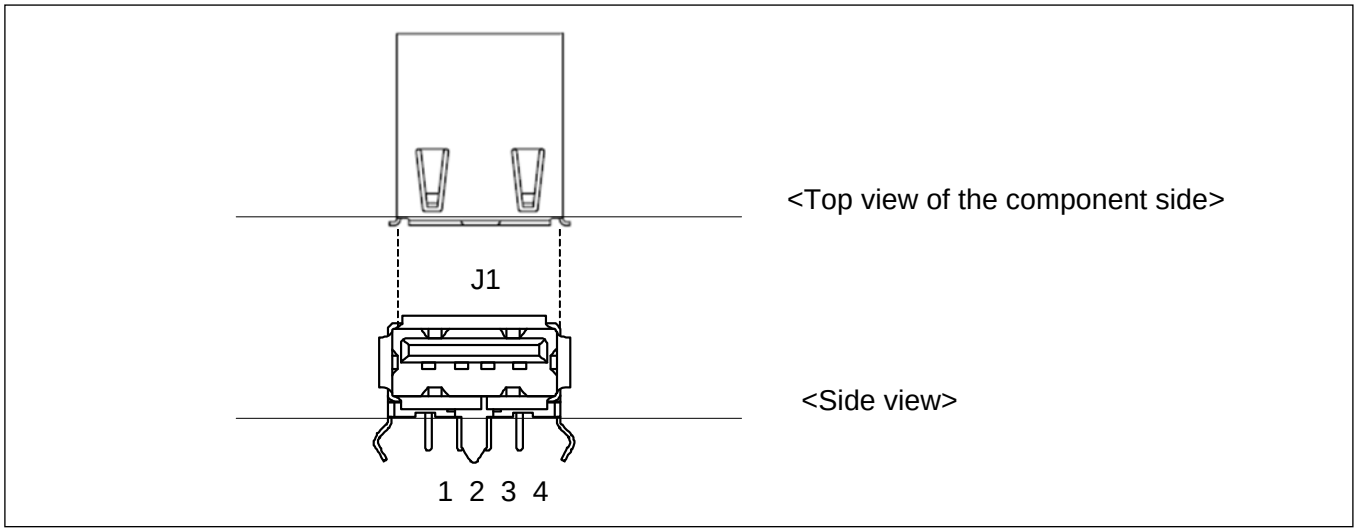
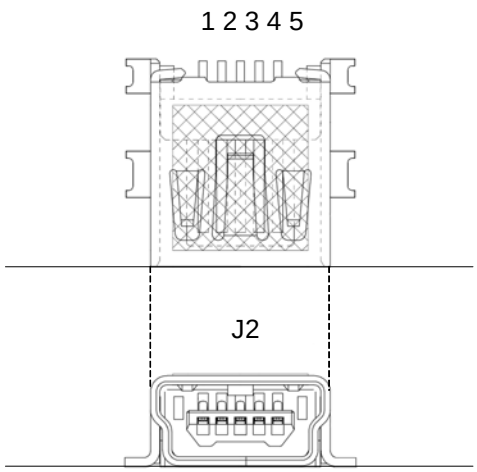


Figure 5.1.3 Series A Receptacle Pin Assignments (J1)

Table 5.1.1. Series A receptacle Pin Descriptions (J1)

Pin No.	Signal Name
1	VBUS
2	DM
3	DP
4	GND



<Top view of the component side>

<Side view>

Figure 5.1.4 Mini-B Receptacle Pin Assignments (J2)

Table 5.1.2 Mini-B Receptacle Pin Descriptions (J2)

Pin No.	Signal Name
1	VBUS
2	DM
3	DP
4	ID (connects to the test pin)
5	GND

5.1.2 H-UDI Port Connector (38-pin, J3)

The R0K572690C000BR includes a 38-pin H-UDI port connector (J3) to connect to an E10A-USB emulator.
Figure 5.1.5shows the H-UDI port connector pin assignments. Table 5.1.3 lists the pin descriptions (38-pin type).

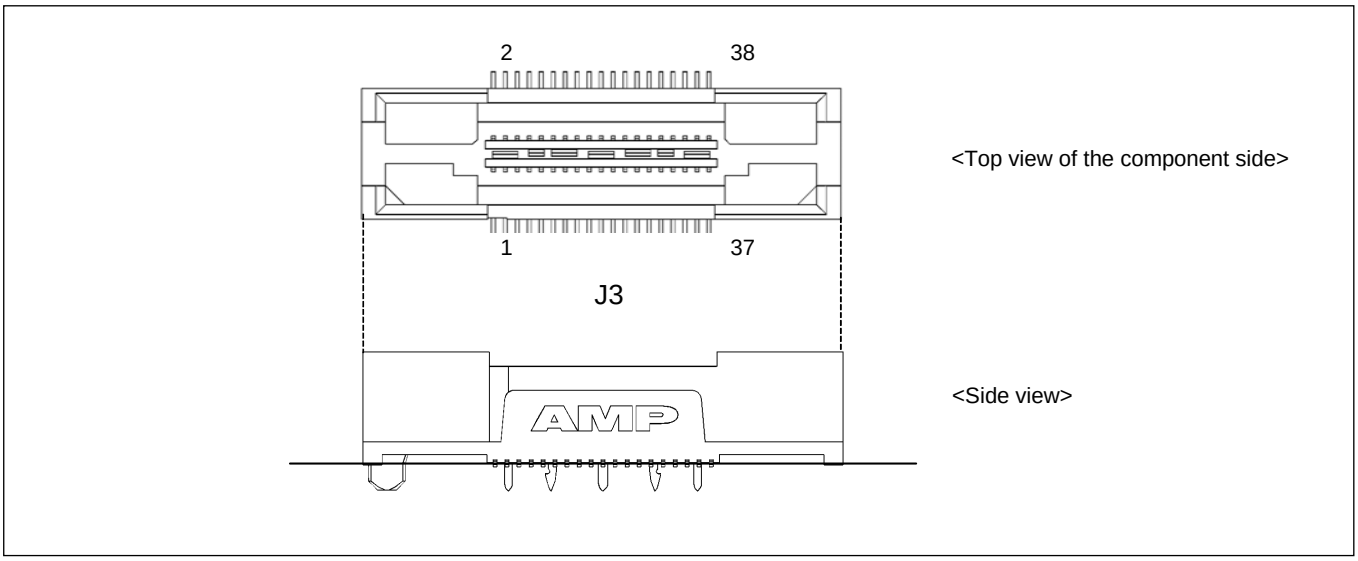


Figure 5.1.5 H-UDI Port Connector Pin Assignments (38-pin type, J3)

Table 5.1.3 H-UDI Port Connector Pin Descriptions (38-pin type, J3)

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	2	NC
3	ASEMD#	4	NC
5	GND	6	AUDCK
7	NC	8	ASEBRKAK#/ASEBRK#
9	RESET#	10	NC
11	TDO	12	+3.3V
13	NC	14	+3.3V
15	TCK	16	NC
17	TMS	18	NC
19	TDI	20	NC
21	TRST#	22	NC
23	NC	24	AUDATA3
25	NC	26	AUDATA2
27	NC	28	AUDATA1
29	NC	30	AUDATA0
31	NC	32	AUDSYNC#
33	NC	34	NC
35	NC	36	NC
37	NC	38	NC

5.1.3 5V Power Supply Connector (J4)

The R0K572690C000BR includes a system power supply connector.

Figure 5.1.6 shows the power supply connector pin assignments and Table 5.1.4 lists the pin descriptions.

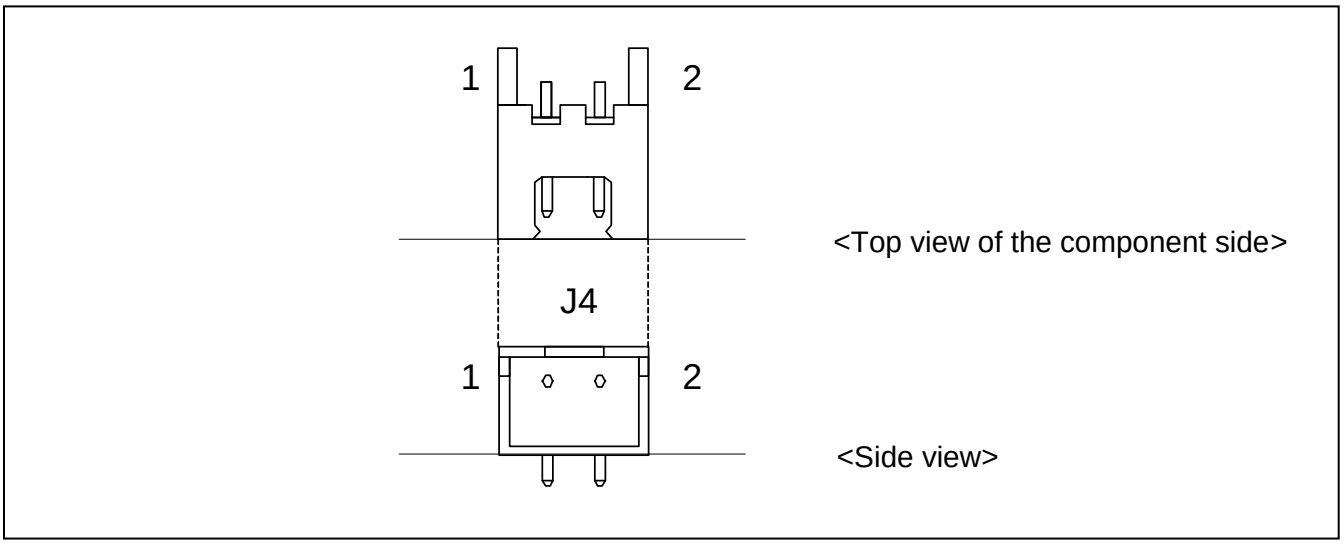


Figure 5.1.6 Power Supply Connector Pin Assignment (J4)

Table 5.1.4 Power Supply Connector Pin Descriptions (J4)

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V	2	GND

5.1.4 5V Input AC Adapter Jack (J6)

The R0K572690C000BR includes an AC adapter jack (J6) for DC5V input.

Figure 5.1.7 shows the pin deployment for 5V input AC adapter. Table 5.1.5 lists the pin descriptions.

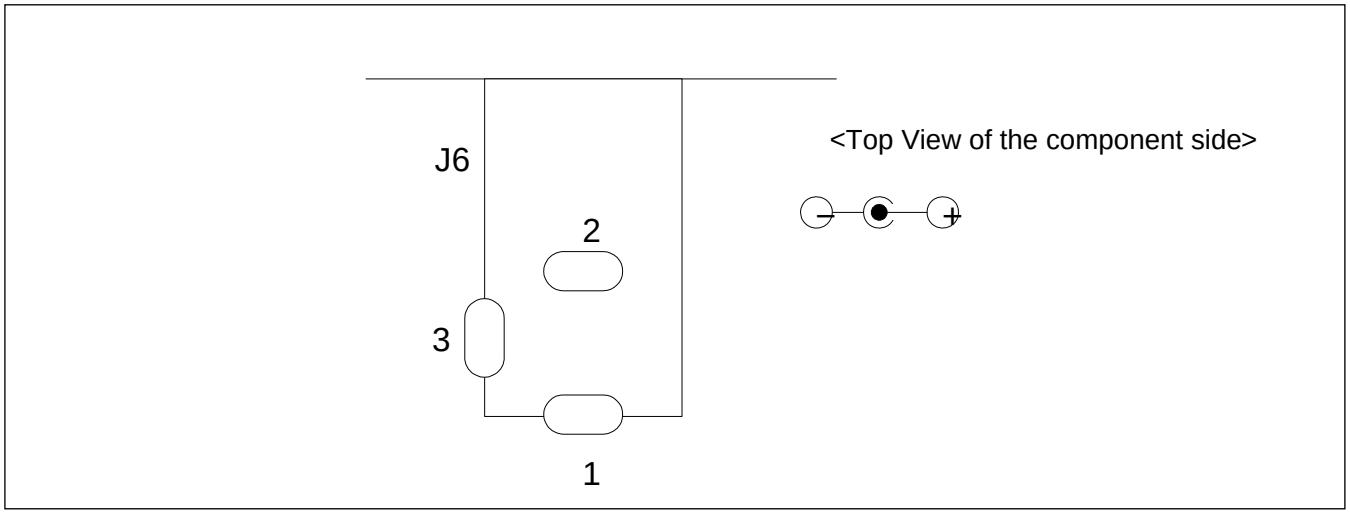


Figure 5.1.7 5V input AC adapter Jack Pin Assignments (J6)

Table 5.1.5 5V Input AC adapter Jack Pin Descriptions (J6)

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V	2	GND
3	GND	-	

5.1.5 H-UDI Port Connector (14-pin, J7)

The R0K572690C000BR includes a 14-pin H-UDI port connector (J3) to connect to an E10A-USB emulator.
Figure 5.1.8 shows the H-UDE port connector pin assignments. Table 5.1.6 lists the pin descriptions. (14-pin).

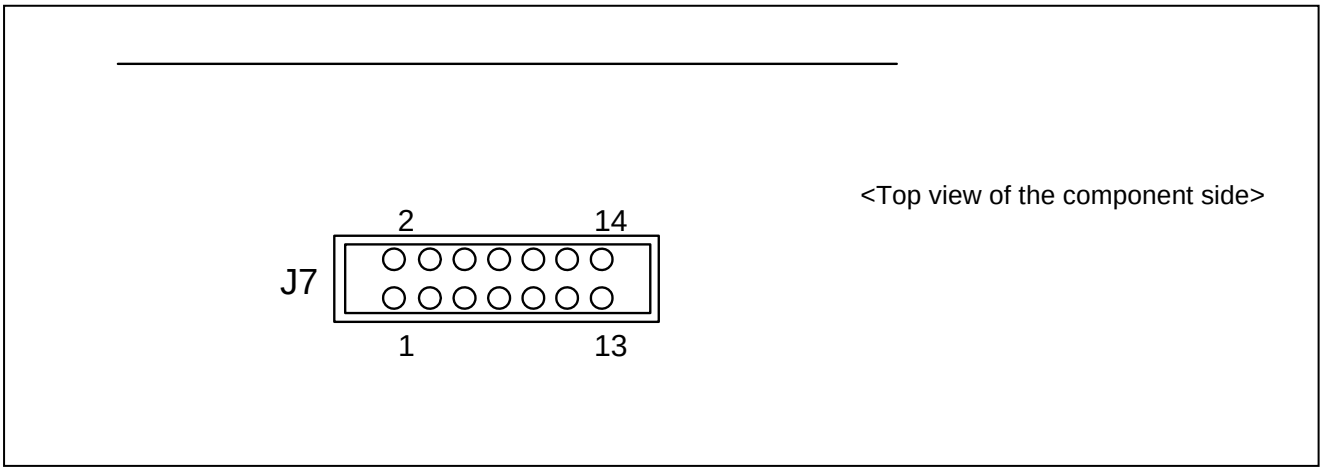


Figure 5.1.8 H-UDI Port Connector Pin Assignment (14-pin type, J7)

Table 5.1.6 H-UDI Port Connector Pin Descriptions (14-pin type, J7)

Pin No.	Signal Name	Pin No.	Signal Name
1	TCK	2	GND
3	TRST#	4	ASEMD#
5	TDO	6	NC
7	ASEBRKAK#/ASBRK#	8	+303V
9	TMS	10	NC
11	TDI	12	GND
13	REST#	14	GND

5.1.6 RS-232C Connector

The R0K572690C000BR includes an RS/232C connector (J10).

Figure 5.1.9shows the H-UDI port connector pin assignments. Table 5.1.7 lists the pin descriptions.

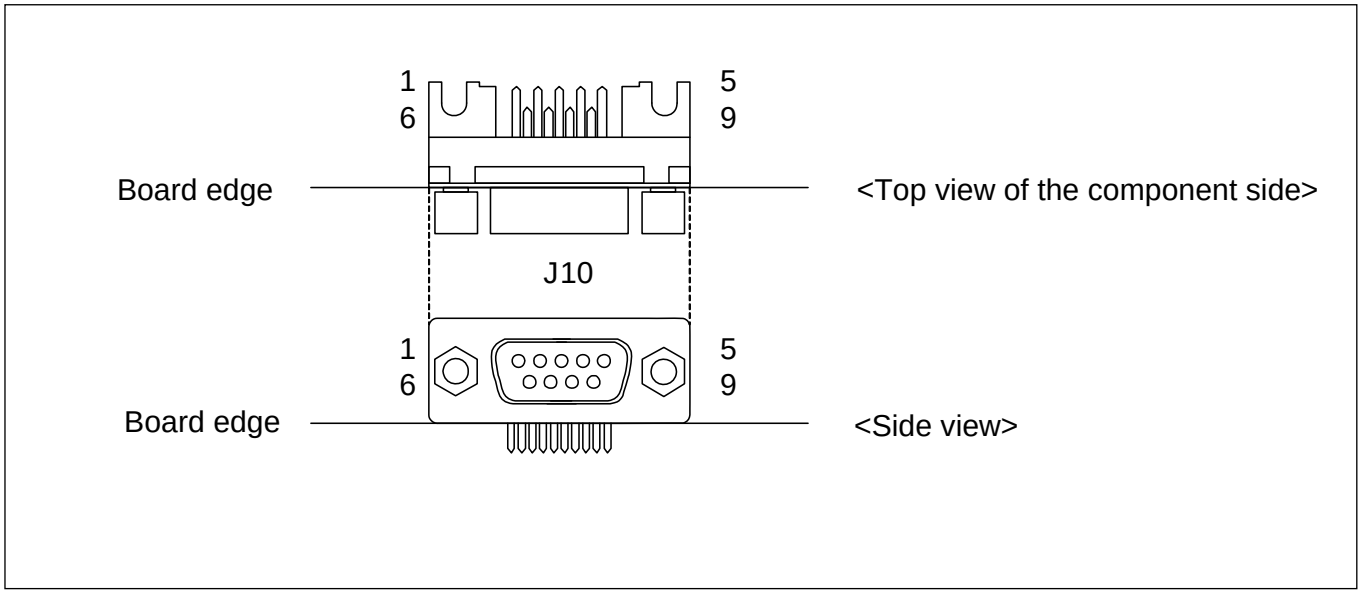


Figure 5.1.9 RS-232C Connector Pin Assignments (J10)

Table 5.1.7 RS-232C Connector Pin description (J10).

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	6	DSR#
2	RXD (PF14 / A25 / AAIWS2 /**RxD2**)	7	RTS#
3	TXD (PF15 / A0 / SSIDATA2 / WDTOVF# / **TxD2** / UBCTRG#)	8	CTS#
4	DTR#	9	NC
5	GND	-	

Note: The signal names in bold letters are setting function.
Pin number4 to 6, 7 to 8 are loopback-connected.

5.1.7 Expansion Connector (CN1, CN3 to CN11)

The R0K572690C000BR includes through-holes for mounting expansion connectors (CN1, CN3 to CN11).
Figure 5.1.10 and Figure 5.1.11 show the expansion connector pin assignments. From Table 5.1.8 to Table 5.1.18 list the pin descriptions.

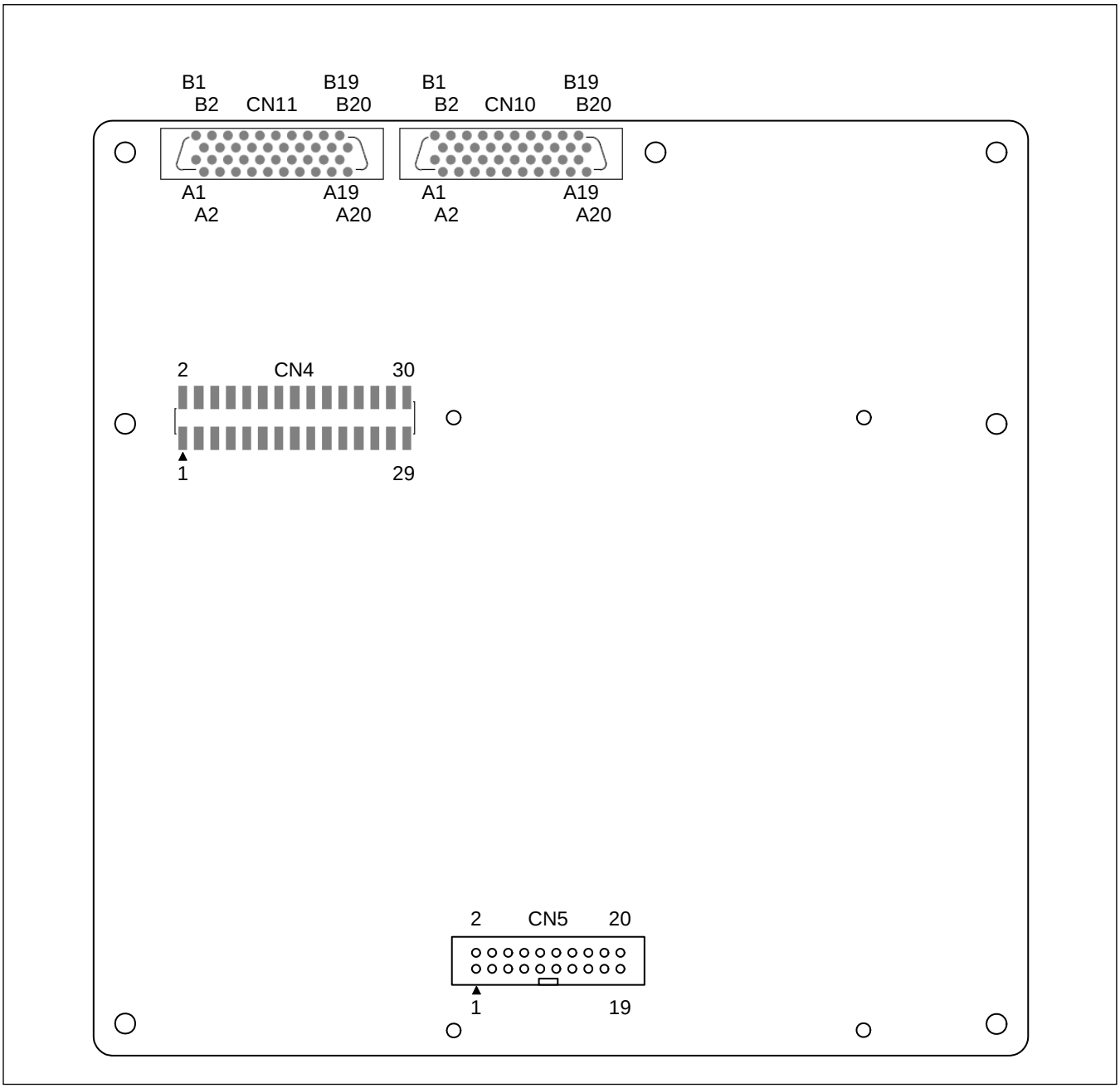


Figure 5.1.10 Expansion Connector Pin Assignments (Top view of the component side)

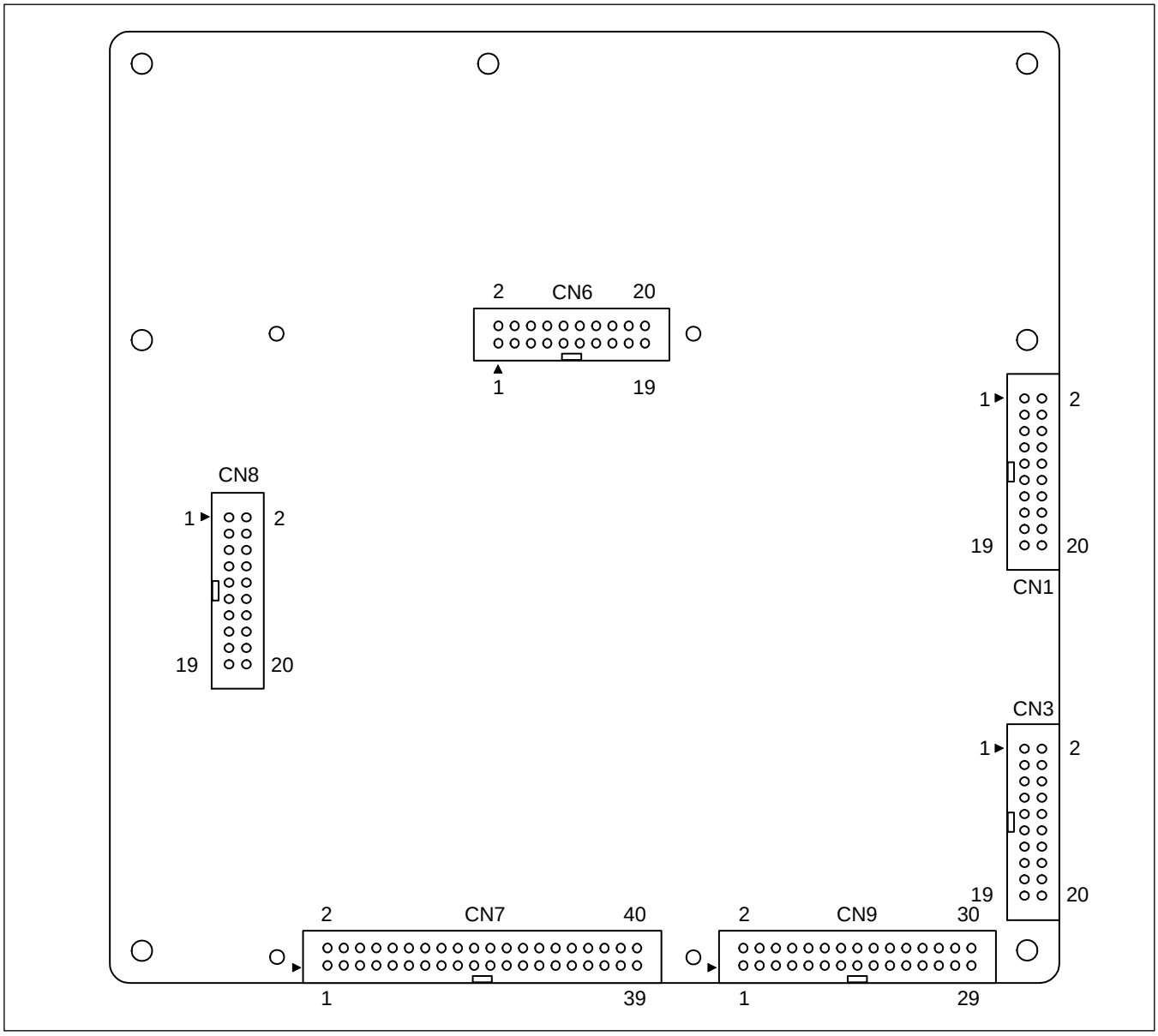


Figure 5.1.11 Expansion Connector Pin Assignments (Top view of the solder side)

Table 5.1.8 Expansion Connector Descriptions 1 (CN1)

Pin No.	Signal Name	Pin No.	Signal Name
1	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / PWM2D / SCK6	2	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7
3	+5V	4	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6
5	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / RTS5#	6	+3.3V
7	NC	8	NC
9	PA1 / MD_BOOT1	10	PA0 / MD_BOOT0
11	GND	12	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / CTS5#
13	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / SCK5#	14	PG23 / LCD_DATA23 / LCD_TCON6 / TxD5 / AUDATA3
15	PG22 / LCD_DATA22 / LCD_TCON5 / RxD5 / AUDSYNC#	16	GND
17	PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2	18	PJ21 / DV_DATA21 / LCD_DATA21 / LCD_TCON4 / IRQ1 / CTx2 / CTx0&CTx1&CTx2 PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1
19	PJ29 / SSIWS5 / TIOC2A / IERxD	20	PJ30 / SSIDATA5 / TIOC2B / IETxD

Legend: : 5V power supply, : 3.3V power supply, : GND

Table 5.1.9 Expansion Connector Descriptions 2 (CN3)

Pin No.	Signal Name	Pin No.	Signal Name
1	AVref	2	AVref
3	PH1 / AN1 / PINT1	4	PH0 / AN0 / PINT0
5	AVref	6	AVref
7	PH3 / AN3 / PINT3	8	PH2 / AN2 / PINT2
9	AVcc	10	AVcc
11	PH5 / AN5 / PINT5 / LCD_EXTCLK	12	PH4 / AN4 / PINT4
13	AVcc	14	AVcc
15	PH7 / AN7 / PINT7	16	PH6 / AN6 / PINT6
17	AVss	18	AVss
19	AVss	20	AVss

Legend: : 5V power supply, : 3.3V power supply, : GND

Table 5.1.10 Expansion Connector Descriptions 3 (CN4)

Pin No.	Signal Name	Pin No.	Signal Name
1	PB22 / A22 / CTx2 / IETxD / CS4#	2	PB21 / A21 / CRx2 / IERxD
3	PB20 / A20 / QMI_0/QIO1_0 / MISO0/ SPBMI_0/SPBIO1_0	4	PB19 / A19 / QMO_0/QIO0_0 / MOSI0 / SPBMO_0/SPBIO0_0
5	PB18 / A18 / QSSL_0 / SSL00 / SPBSSL	6	PB17 / A17 / QSPCLK_0 / RSPCK0 / SPBCLK
7	GND	8	GND
9	PB16 / A16 / QIO3_0 / SPBIO3_0	10	PB15 / A15 / QIO2_0 / SPBIO2_0
11	PB14 / A14 / QIO3_1 / SPBIO3_1	12	PB13 / A13 / QIO2_1 / SPBIO2_1
13	PB12 / A12 / TIOC3D	14	PB11 / A11 / TIOC3C
15	GND	16	GND
17	PB10 / A10 / TIOC3B	18	PB9 / A9 / TIOC3A
19	PB8 / A8 / TIOC2B	20	PB7 / A7 / TIOC2A
21	PB6 / A6 / TIOC1B	22	PB5 / A5 / TIOC1A
23	+3.3V	24	+3.3V
25	PB4 / A4 / TIOC0D	26	PB3 / A3 / TIOC0C
27	PB2 / A2 / TIOC0B	28	PB1 / A1 / TIOC0A
29	+5V	30	+5V

Legend: : 5V power supply, : 3.3V power supply, : GND

Table 5.1.11 Expansion Connector Descriptions 4 (CN5)

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	2	PF23 / SD_D2_0 / TxD3 / MMC_D2
3	PF22 / SD_D3_0 / RxD3 / MMC_D3	4	PF21 / SD_CMD_0 / SCK3 / MMC_CMD
5	PF20 / SD_CLK_0 / SSIDATA3 / MMC_CLK	6	+5V
7	PF19 / SD_D0_0 / SSIWS3 / IRQ7 / MMC_D0	8	PF18 / SD_D1_0 / SSISCK3 / IRQ6 / MMC_D1
9	GND	10	PF17 / SD_WP_0 / FRB / IRQ5
11	PF17 / SD_WP_0 / FRB / IRQ5	12	PF16 / SD_CD_0 / FCE# / IRQ4 / MMC_CD
13	PF16 / SD_CD_0 / FCE# / IRQ4 / MMC_CD	14	GND
15	PF15 / A0 / SSIDATA2 / WDTOVF# / TxD2 / UBCTRG#	16	PF14 / A25 / SSIWS2 / RxD2
17	PF13 / A24 / SSISCK2 / SCK2	18	PF9 / BS# / DV_DATA0 / SCK0 / MMC_D4 / RTS1#
19	PF8 / A23 / TxD0	20	PF1 / BACK# / QSSL_1 / SSL10 / TIOC4B / DACK0

Legend: : 5V power supply, : 3.3V power supply, : GND

Table 5.1.12 Expansion Connector Descriptions 5 (CN6)

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V	2	+5V
3	+5V	4	+5V
5	PC0 / CS0# / MD_BOOT2	6	PC1 / RD#
7	PC2 / RD/WR# / SCK6	8	PC3 / WE0#/DQMLL / RxD6
9	PC4 / WE1#/WE#/DQMLU / TxD6	10	+3.3V
11	+3.3V	12	PE6 / SCL3 / RxD6
13	PE7 / SDA3 / RxD7	14	PC5 / RAS# / CRx0 / CRx0/CRx1/CRx2 / IRQ0
15	PC6 / CAS# / SCK7 / CTx0 / CTx0&CTx1&CTx2	16	PC7 / CKE / RxD7 / CRx1 / CRx0/CRx1 / IRQ1
17	PC8 / CS3# / TxD7 / CTx1 / CTx0&CTx1	18	GND
19	GND	20	CKIO

Legend: : 5V power supply, : 3.3V power supply, :GND

Table 5.1.13 Expansion Connector Descriptions 6 (CN7-1)

Pin No.	Signal Name	Pin No.	Signal Name
1	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G	2	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H
3	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E	4	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / WM1F
5	PE0 / SCL0 / TCLKA / LCD_EXTCLK	6	RES#
7	PE2 / SCL1 / TCLKC / IOIS16# / DV_VSYNC	8	PE1 / SDA0 / TCLKB / AUDIO_CLK / DV_CLK PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2
9	PE4 / SCL2 / RxD4 / DV_VSYNC	10	PE3 / SDA1 / TCLKD / ADTRG# / DV_HSYNC
11	+3.3V	12	PE5 / SDA2 / RxD5 / DV_HSYNC
13	PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	14	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D
15	PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	16	PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
17	PF10 / CS1# / SSISCK1 / DV_DATA1 / SCK1 / MC_D5 PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	18	+5V
19	PF12 / SSIDATA1 / DV_DATA3 / TxD1 / MMC_D7 PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	20	PF11 / SSIWS1 / DV_DATA2 / RxD1 / MMC_D6 PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
21	GND	22	PJ28 / SSISCK5 / TIOC1B / RTS7# PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D
23	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / WM1F PJ30 / SSIDATA5 / TIOC2B / IETxD	24	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E PJ29 / SSIWS5 / TIOC2A / IERxD

Legend: : 5V power supply, : 3.3V power supply, :GND

Table 5.1.14 Expansion Connector Descriptions 7 (CN7-2)

Pin No.	Signal Name	Pin No.	Signal Name
25	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G PJ24 / SGOUT_0 / SSISCK4 / LCD_TCON3 / SPDIF_IN / SCK7	26	GND
27	PJ26 / SGOUT_2 / SSIDATA4 / LCD_TCON5 / TxD7 PJ31 / DV_CLK	28	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H PJ25 / SGOUT_1 / SSIWS4 / LCD_TCON4 / SPDIF_OUT / RxD7
29	GND	30	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / TIOC4A / DREQ0 / AUDCK
31	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1	32	PJ13 / DV_DATA13 / LCD_DATA13 / PINT5 / PWM2F / TxD5
33	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / SPBMI_1/SPBIO1_1	34	GND
35	PF5 / SSIWS0 / SGOUT_1	36	PF4 / CS5#/CE1A# / SSISCK0 / SGOUT_0
37	PF6 / CE2A# / SSITxD0 / SGOUT_2 PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#	38	PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#
39	GND	40	PJ19 / DV_DATA19 / LCD_DATA19 / MISO0 / TIOC0D/ SIOFRxD / AUDIO_XOUT

Legend: : 5V power supply, : 3.3V power supply, :GND

Table 5.1.15 Expansion Connector Descriptions 8 (CN8)

Pin No.	Signal Name	Pin No.	Signal Name
1	PD0 / D0 / PWM1A	2	PD8 / D8/NAF0 / PWM2A
3	PD1 / D1 / PWM1B	4	PD9 / D9/NAF1 / PWM2B
5	GND	6	PD2 / D2 / PWM1C
7	PD10 / D10/NAF2 / PWM2C	8	PD3 / D3 / PWM1D
9	PD11 / D11/NAF3 / PWM2D	10	GND
11	PD4 / D4/FRE# / PWM1E	12	PD12 / D12/NAF4 / PWM2E
13	PD5 / D5/FCLE / PWM1F	14	PD13 / D13/NAF5 / PWM2F
15	+3.3V	16	PD6 / D6/FALE / PWM1G
17	PD14 / D14/NAF6 / PWM2G	18	PD7 / D7/FWE# / PWM1H
19	PD15 / D15/NAF7 / PWM2H	20	+5V

Legend: : 5V power supply, : 3.3V power supply, :GND

Table 5.1.16 Expansion Connector Description 9 (CN9)

Pin No.	Signal Name	Pin No.	Signal Name
1	PG1 / D17 / LCD_DATA1 / IRQ1 / TIOC0B	2	PG0 / D16 / LCD_DATA0 / IRQ0 / TIOC0A
3	PG3 / D19 / LCD_DATA3 / IRQ3 / TIOC0D	4	PG2 / D18 / LCD_DATA2 / IRQ2 / TIOC0C
5	GND	6	PG4 / D20 / LCD_DATA4 / IRQ4 / TIOC1A
7	PG6 / D22 / LCD_DATA6 / IRQ6 / TIOC2A	8	PG5 / D21 / LCD_DATA5 / IRQ5 / TIOC1B
9	PG7 / D23 / LCD_DATA7 / IRQ7 / TIOC2B	10	GND
11	PG9 / D25 / LCD_DATA9 / PINT1 / TIOC3B	12	PG8 / D24 / LCD_DATA8 / PINT0 / TIOC3A
13	PG11 / D27 / LCD_DATA11 / PINT3 / TIOC3D	14	PG10 / D26 / LCD_DATA10 / PINT2 / TIOC3C
15	GND	16	PG12 / D28 / LCD_DATA12 / PINT4
17	PG14 / D30 / LCD_DATA14 / PINT6	18	PG13 / D29 / LCD_DATA13 / PINT5
19	PG25 / LCD_TCON0	20	PG15 / D31 / LCD_DATA15 / PINT7
21	PG26 / LCD_TCON1	22	+5V
23	PG24 / LCD_CLK	24	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
25	+3.3V	26	PG27 / LCD_TCON2 / LCD_EXTCLK
27	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / PWM2E / SCK7	28	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / TIOC4A / DREQ0 / AUDCK
29	PJ27 / SGOUT_3 / TIOC1A / CTS7#	30	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1

Legend: : 5V power supply, : 3.3V power supply, :GND

Table 5.1.17 Expansion Connector Description 10 (CN10)

Pin No.	Signal Name	Pin No.	Signal Name
A1	PG0 / D16 / LCD_DATA0 / IRQ0 / TIOC0A	B1	PG1 / D17 / LCD_DATA1 / IRQ1 / TIOC0B
A2	PG2 / D18 / LCD_DATA2 / IRQ2 / TIOC0C	B2	PG3 / D19 / LCD_DATA3 / IRQ3 / TIOC0D
A3	+3.3V	B3	PG4 / D20 / LCD_DATA4 / IRQ4 / TIOC1A
A4	PG5 / D21 / LCD_DATA5 / IRQ5 / TIOC1B	B4	PG6 / D22 / LCD_DATA6 / IRQ6 / TIOC2A
A5	PG7 / D23 / LCD_DATA7 / IRQ7 / TIOC2B	B5	+5V
A6	PG8 / D24 / LCD_DATA8 / PINT0 / TIOC3A	B6	PG9 / D25 / LCD_DATA9 / PINT1 / TIOC3B
A7	PG10 / D26 / LCD_DATA10 / PINT2 / TIOC3C	B7	PG11 / D27 / LCD_DATA11 / PINT3 / TIOC3D
A8	+3.3V	B8	PG12 / D28 / LCD_DATA12 / PINT4
A9	PG13 / D29 / LCD_DATA13 / PINT5	B9	PG14 / D30 / LCD_DATA14 / PINT6
A10	PG15 / D31 / LCD_DATA15 / PINT7	B10	+5V
A11	PG16 / WE2#/ICIORD#/DQMUL / LCD_DATA16 / AUDATA0	B11	PG17 / WE3#/ICIOWR#/AH#/DQMUU / LCD_DATA17 / AUDATA1
A12	PG18 / DV_DATA4 / LCD_DATA18 / SPDIF_IN / SCK4	B12	PG19 / DV_DATA5 / LCD_DATA19 / SPDIF_OUT / SCK5
A13	GND	B13	PG20 / DV_DATA6 / LCD_DATA20 / LCD_TCON3 / RxD4
A14	PG21 / DV_DATA7 / LCD_DATA21 / LCD_TCON4 / TxD4 / AUDATA2	B14	PG22 / LCD_DATA22 / LCD_TCON5 / RxD5 / AUDSYNC#
A15	PG23 / LCD_DATA23 / LCD_TCON6 / TxD5 / AUDATA3	B15	GND
A16	PG24 / LCD_CLK	B16	PG25 / LCD_TCON0
A17	PG26 / LCD_TCON1	B17	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
A18	GND	B18	PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1
A19	VIN1（NC）	B19	GND
A20	GND	B20	VIN2（NC）

Legend: : 5V power supply, : 3.3V power supply, :GND

Table 5.1.18 Expansion Connector Description 11 (CN11)

Pin No.	Signal Name	Pin No.	Signal Name
A1	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6	B1	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7
A2	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / SCK5#	B2	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / PWM2D / SCK6
A3	+3.3V	B3	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / RTS5#
A4	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / CTS5#	B4	PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2
A5	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H	B5	+5V
A6	PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	B6	PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
A7	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F	B7	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G
A8	+3.3V	B8	PJ18 / DV_DATA18 / LCD_DATA18 / MOSI0 / TIOC0C / SIOFTxD
A9	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E	B9	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D
A10	PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	B10	+5V
A11	PJ13 / DV_DATA13 / LCD_DATA13 / PINT5 / PWM2F / TxD5	B11	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / PWM2E / SCK7
A12	PJ19 / DV_DATA19 / LCD_DATA19 / MISO0 / TIOC0D/ SIOFRxD / AUDIO_XOUT	B12	PJ17 / DV_DATA17 / LCD_DATA17 / SSL00 / TIOC0B / SIOFSYNC
A13	GND	B13	PJ16 / DV_DATA16 / LCD_DATA16 / RSPCK0 / TIOC0A / SIOFSCK
A14	PJ21 / DV_DATA21 / LCD_DATA21 / LCD_TCON4 / IRQ1 / CTx2 / CTx0&CTx1&CTx2	B14	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
A15	PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1	B15	GND
A16	PJ31 / DV_CLK	B16	PJ31 / DV_CLK
A17	PE4 / SCL2 / RxD4 / DV_VSYNC	B17	PE5 / SDA2 / RxD5 / DV_HSYNC
A18	GND	B18	PH4 / AN4 / PINT4
A19	PH5 / AN5 / PINT5 / LCD_EXTCLK	B19	PH6 / AN6 / PINT6
A20	PH7 / AN7 / PINT7	B20	GND

Legend: : 5V power supply, : 3.3V power supply, :GND

5.2 R0K572690C000BR Operating Components

Figure 5.2.1 shows the operating components for the R0K572690C000BR.

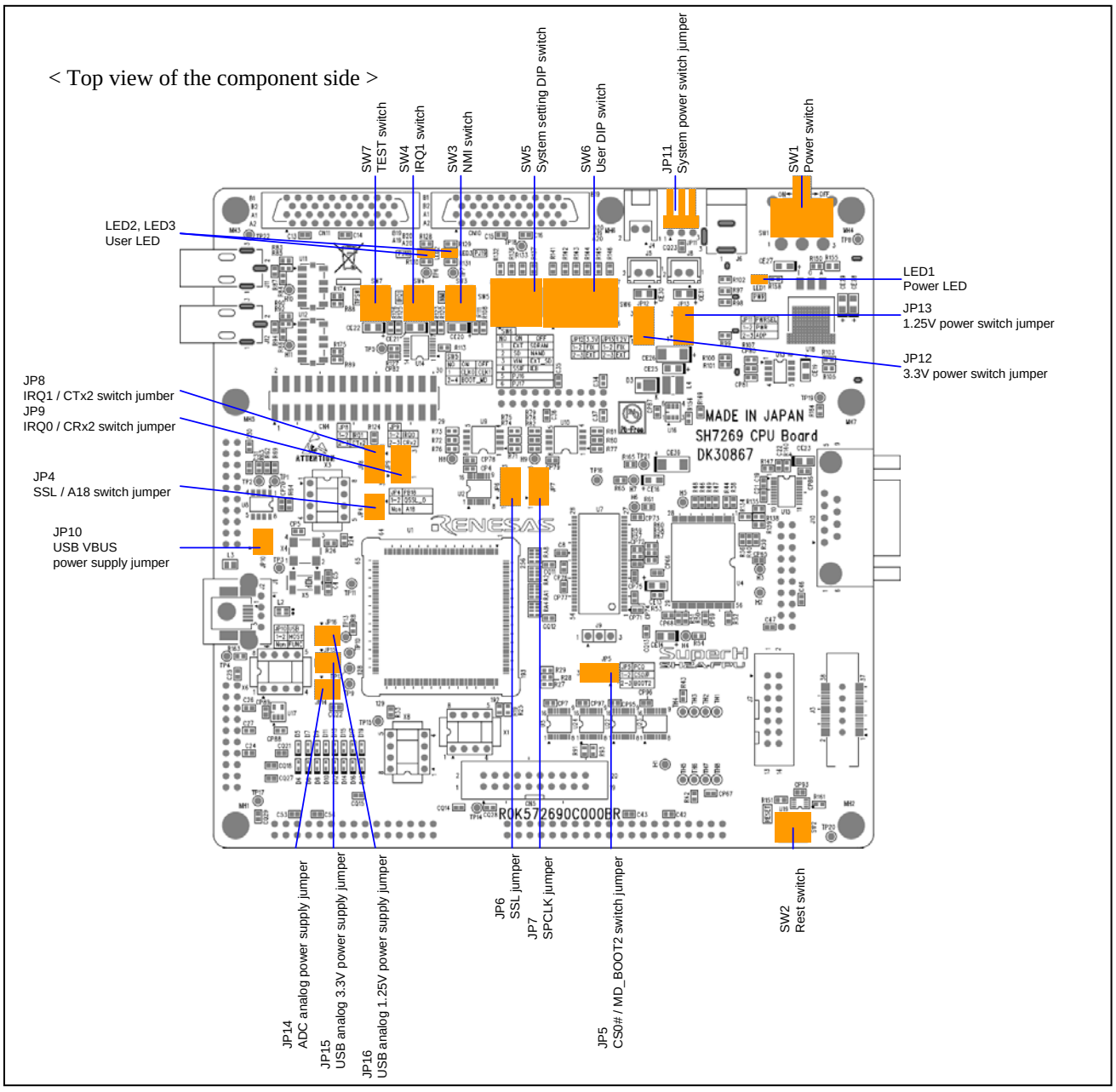


Figure 5.2.1 R0K572690C000BR Operating Components

5.2.1 Jumper (JP4 to JP16)

R0K572690C000BR includes thirteen jumpers. Figure 5.2.2 shows the jumper assignments. From Table 5.2.1 to Table 5.2.4 list the jumper setting for JP4 to JP16.

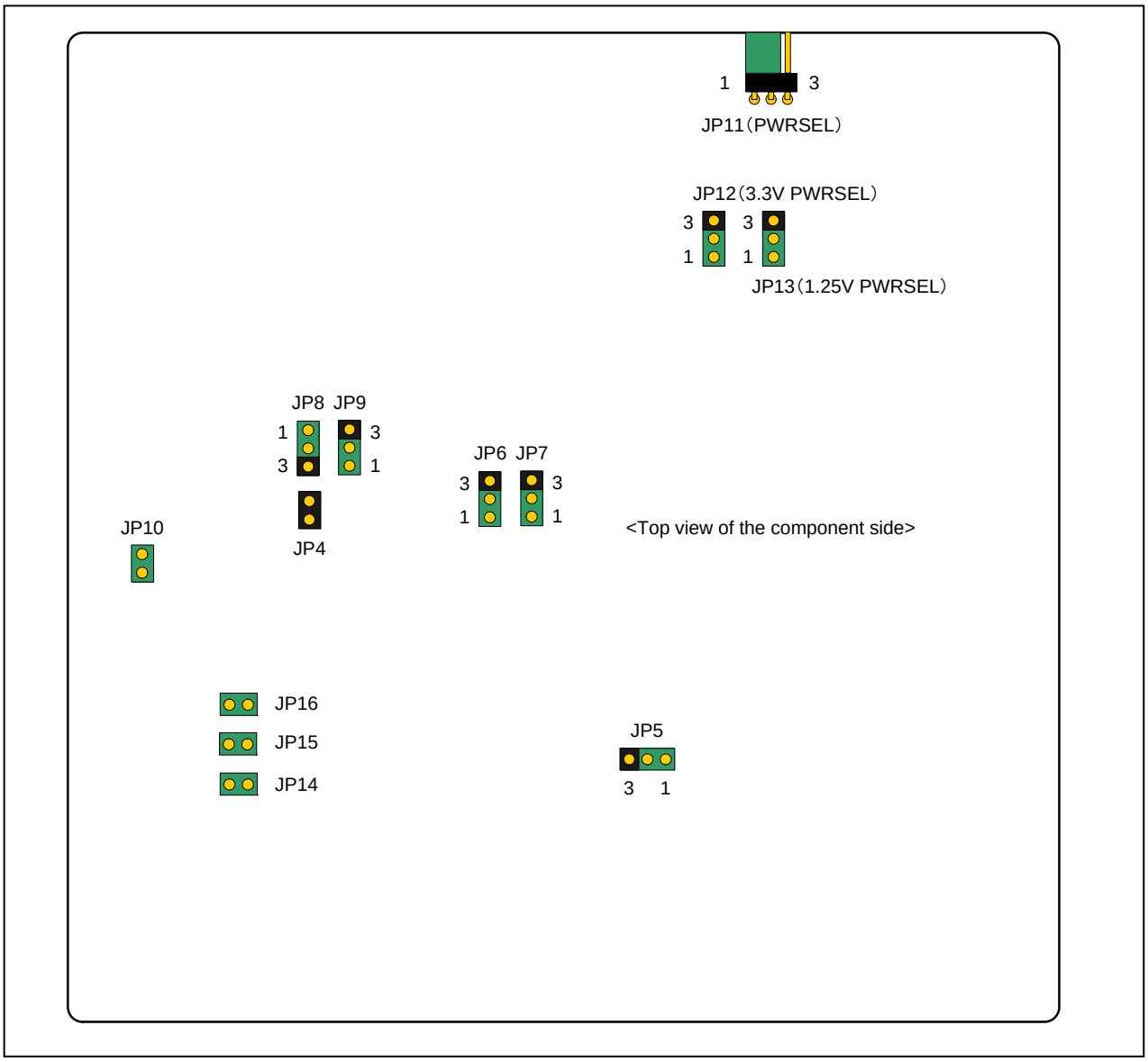


Figure 5.2.2 R0K572690C000BR Jumper Assignments (JP4 to JP16)

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Table 5.2.1 Multi Functional Pin Switch Jumper Settings (JP4, JP5, JP8 and JP9)

Jumper	Setting	Function
JP4 SSL/A18	1－2	Connects the serial flash memory (U9) as QSSL_0/SSL00 output pin
	None（open）	Connects the NOR flash memory (U4) as A18 output pin
JP5 CS0#/MD_BOOT2	1－2	Connects the NOR flash memory (U4) as CS0# output pin
	2－3	Connects the system setting DIP switch (SW5) as MD_BOOT2 input pin
JP6 SSL	1－2	Connects to the serial flash memory2(U10) as QSSL_1/SSL10 output pin
	2－3	Connects to the serial flash memory2(U10) as SPBSSL output pin
JP7 SPCLK	1－2	Connects to the serial flash memory2(U10) as QSPCLK_1/RSPCK1 output pin
	2－3	Connects to the serial flash memory2(U10) as SPBCLK output pin
JP8 IRQ1/CTx2	1－2	Connects the IRQ1 switch (SW4) as IRQ1 input pin
	2－3	Connects the expansion connector (CN1) as CTx2 output pin
JP9 IRQ0/CRx2	1－2	Connects the expansion connector (CN7) as IRQ0 input pin
	2－3	Connects the expansion connector (CN1) as CRx2 input pin

: setting by default

Note: Jumper settings shall not be changed while this evaluation board is under operation. Make sure to change settings with the power turned off.

Table 5.2.2 USB VBUS Power Supply Jumper Settings (JP10)

Jumper	Setting	Function
JP10	1－2	USB host mode (supply VBUS power)
	None（open）	USB function mode (Not supply VBUS power)

: setting by default

Note: Jumper settings shall not be changed while this evaluation board is under operation. Make sure to change settings with the power turned off.

Table 5.2.3 Power Select Jumper Settings (JP11 to JP13)

Jumper	Setting	Function
JP11 PWRSEL	1－2	Supplies the system power from J4
	2－3	Supplies the system power from J6 (with AC adapter)
JP12 3.3V PWRSEL	1－2	Supplies the 3.3V power for SH7269 from U18 (embedded power)
	2－3	Supplies the 3.3V power for SH7269 from J5 (external power)
JP13 1.25V PWRSEL	1－2	Supplies the 1.25V power for SH7269 from U16 (embedded power)
	2－3	Supplies the 1.25V power for SH7269 from J8 (external power)

: setting by default

Note: Jumper settings shall not be changed while this evaluation board is under operation. Make sure to change settings with the power turned off.

Table 5.2.4 Analog Power Supply Jumper Setting (JP14 to JP16)

Jumper	Setting	Function
JP14	1－2	Supplies the A/D converter analog 3.3V power (AVcc)
	None（open）	Does not supply the A/D converter analog 3.3V power (AVcc)
JP15	1－2	Supply USB analog 3.3V power (USBAPVcc)
	None（open）	Does not supply the USB analog 3.3V power (USBAPVcc)
JP16	1－2	Supply USB analog 1.25V power (USBAVcc)
	None（open）	Does not supply the USB analog 1.25V power (USBAVcc)

: setting by default

Note: Jumper settings shall not be changed while this evaluation board is under operation. Make sure to change settings with the power turned off.

5.2.2 Switch and LEDs

R0K572690C000BR includes seven switches and three LEDs.

Figure 5.2.3 shows the switch assignments and LED pin assignments. Table 5.2.5 describes about on-chip switches. Table 5.2.6 and Table 5.2.7 list LED descriptions. Table 5.2.8 described on-chip LEDs.

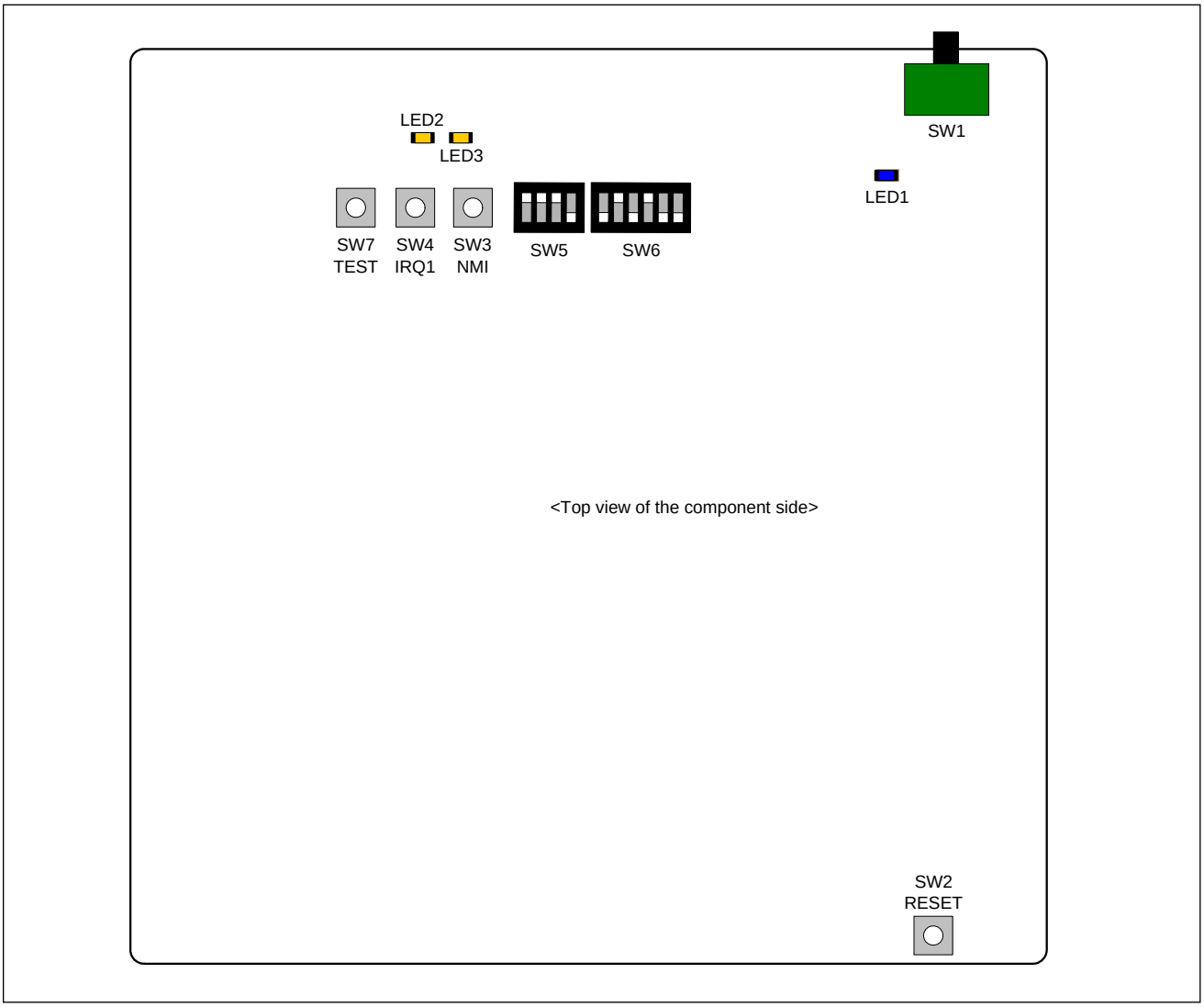

Figure 5.2.3 Diagram of Populated Switches and LEDs for R0K572690C000BR

Table 5.2.5 R0K572690C000BR Switches

No.	Function	Note
SW1	Power switch	-
SW2	Reset switch	For the details, refer to Section 2.9
SW3	NMI switch	For the details, refer to Section 2.7
SW4	IRQ1 switch	For the details, refer to Section 2.7
SW5	DIP switch for setting the system (with 4 poles)	For the details, refer to Table 5.2.6
SW6	DIP switch for users (with 6 poles)	For the details, refer to Table 5.2.7
SW7	TEST switch	For the details, refer to Section 2.7

Table 5.2.6 Explanation of DIP Switches for System setting

No.	Setting		Function	
SW5-1	OFF	MD_CLK0 is high	Prohibited setting	
MD_CLK0	ON	MD_CLK0 is low	Clock mode 0	
SW5-21	OFF	MD-BOOT0 is high	Boot mode MD_BOOT[2:0]	Boot device
MD-BOOT0	ON	MD-BOOT0 is low	0 (B'*00)	NOR flash memory (bus width is 16 bits)
SW5-3	OFF	MD-BOOT1 is high	1 (B'*10)	NOR flash memory (bus width is 32 bits)
MD-BOOT1	ON	MD-BOOT1 is low	2 (B'001)	NAND flash memory
SW5-4	OFF	MD-BOOT2 is high	3 (B'101)	Serial flash memory
MD-BOOT2	ON	MD-BOOT2 is low	4 (B'011)	eSD
			5 (B'111)	eMMC

: setting by default

Table 5.2.7 Explanation of the Function of User DIP Switch

No.	Setting		Function
SW6-1	OFF	EXT#/SDRAM is high	Connects to the SDRAM (U7)
Select PC[8:5] access point	ON	EXT#/SDRAM is low	Connects to the expansion connecter (CN6)
SW6-2	OFF	EXT#/SDRAM is high	Connects to the NAND flash memory (U5)
Select PF[17:16] access point	ON	EXT#/SDRAM is low	Connects t o the SD card slot (J13)
SW6-3	OFF	VIN#/EXT_SD is high	Connects to the expansion connecter (CN7)(SD card slot)
Select PJ[7:0] access point	ON	VIN#/EXT_SD is low	Connects to the expansion connecter (CN7) (video decoder)
SW6-4	OFF	VIN#/EXT_SD is high	Connects to the expansion connecter (CN1)(IEBus)
Select PJ[29:28] access point	ON	VIN#/EXT_SD is low	Connects to the expansion connecter (CN7)(DA converter2)
SW6-5	OFF	PJ16 is high	
PJ16	ON	PJ16 is low	
SW6-6	OFF	PJ17 is high	
PJ17	ON	PJ17 is low	

: setting by default

Table 5.2.8 LEDs

No.	Color	Function
LED1	Blue	Power source LED (illuminates when supplying 5V power)
LED2	Yellow	User LED (illuminates when PJ18 is low output)
LED3	Yellow	User LED (illuminates when PJ19 s low output)

5.3 R0K572690C000BR Dimensions

Figure 5.3.1 and Figure 5.3.2 show the dimensions of the R0K572690C000BR as top views on component side. Figure 5.3.3 shows the dimensions of R0K572690C000BR as a perspective view.

<Top view of the component side>

Unit : mm

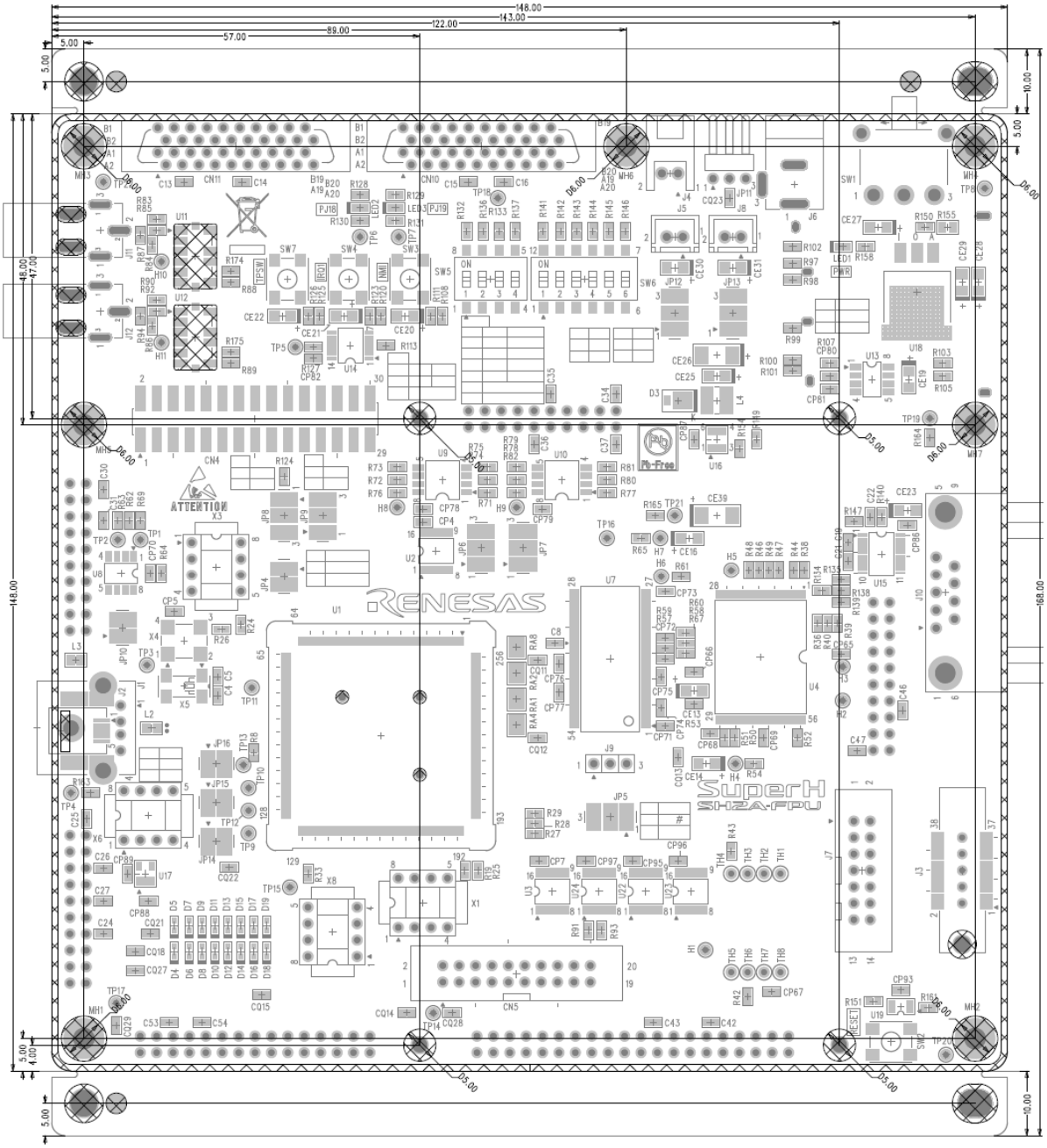

Figure 5.3.1 R0K572690C000BR Dimensions 1 (Top view of the component side)

<Top view of the component side>

Unit : mm

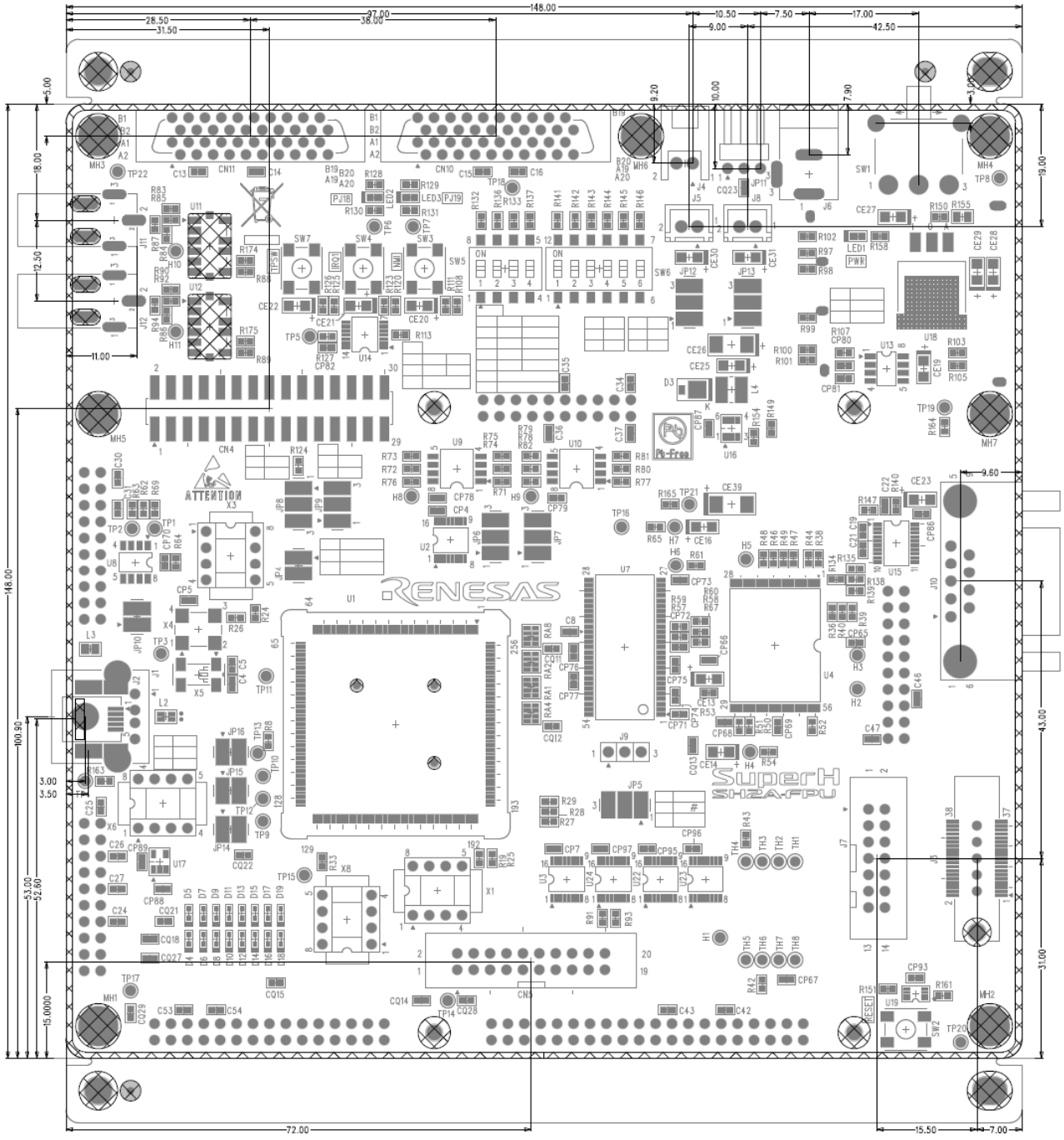

Figure 5.3.2 R0K572690C000BR Dimensions 2 (Top view of the component side)

<Perspective view of the component side>

Unit : mm

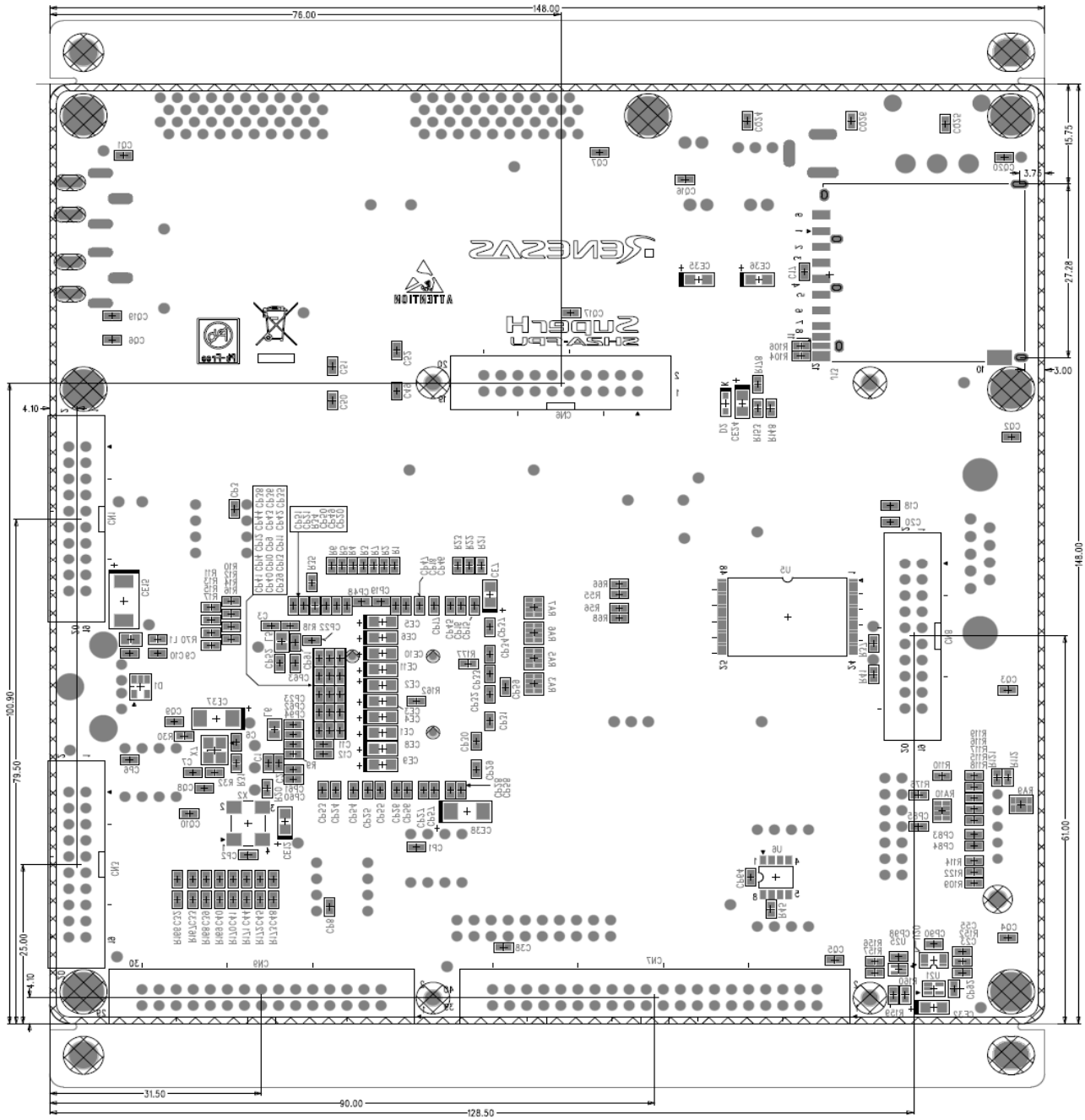

Figure 5.3.3 R0K572690C000BR Dimensions (Perspective view of the component side)

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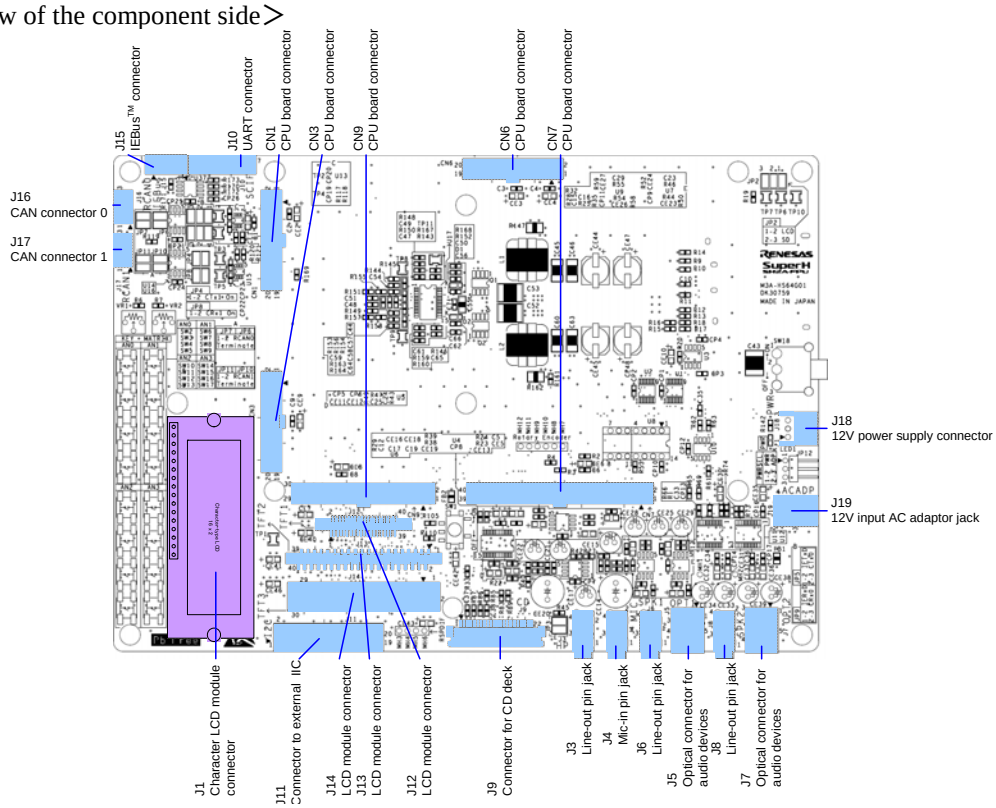
6. M3A-HS64G01 Operating Specification

6.1 M3A-HS64G01 Connectors

Figure 6.1.1 shows the connector assignments for the M3A-HS64G01.

＜Top view of the component side＞



＜Top view of the solder side＞

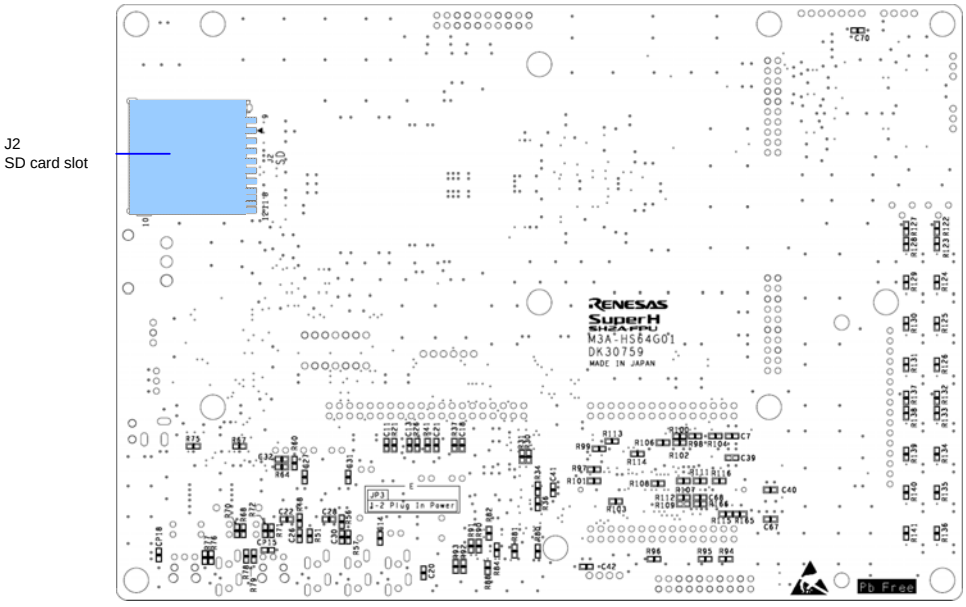


Figure 6.1.1 M3A-HS64G01 Connectors

6.1.1 Connectors to R0K572690C000BR（CN1, CN3, CN6, CN7 and CN9）

The M3A-HS64G01 includes MIL-spec connectors (CN1, CN3, CN6, CN7, and CN9) for connecting to R0K572690C000BR.

Figure 6.1.2 shows the connector pin assignments. From Table 6.1.1 to Table 6.1.6 list their descriptions.

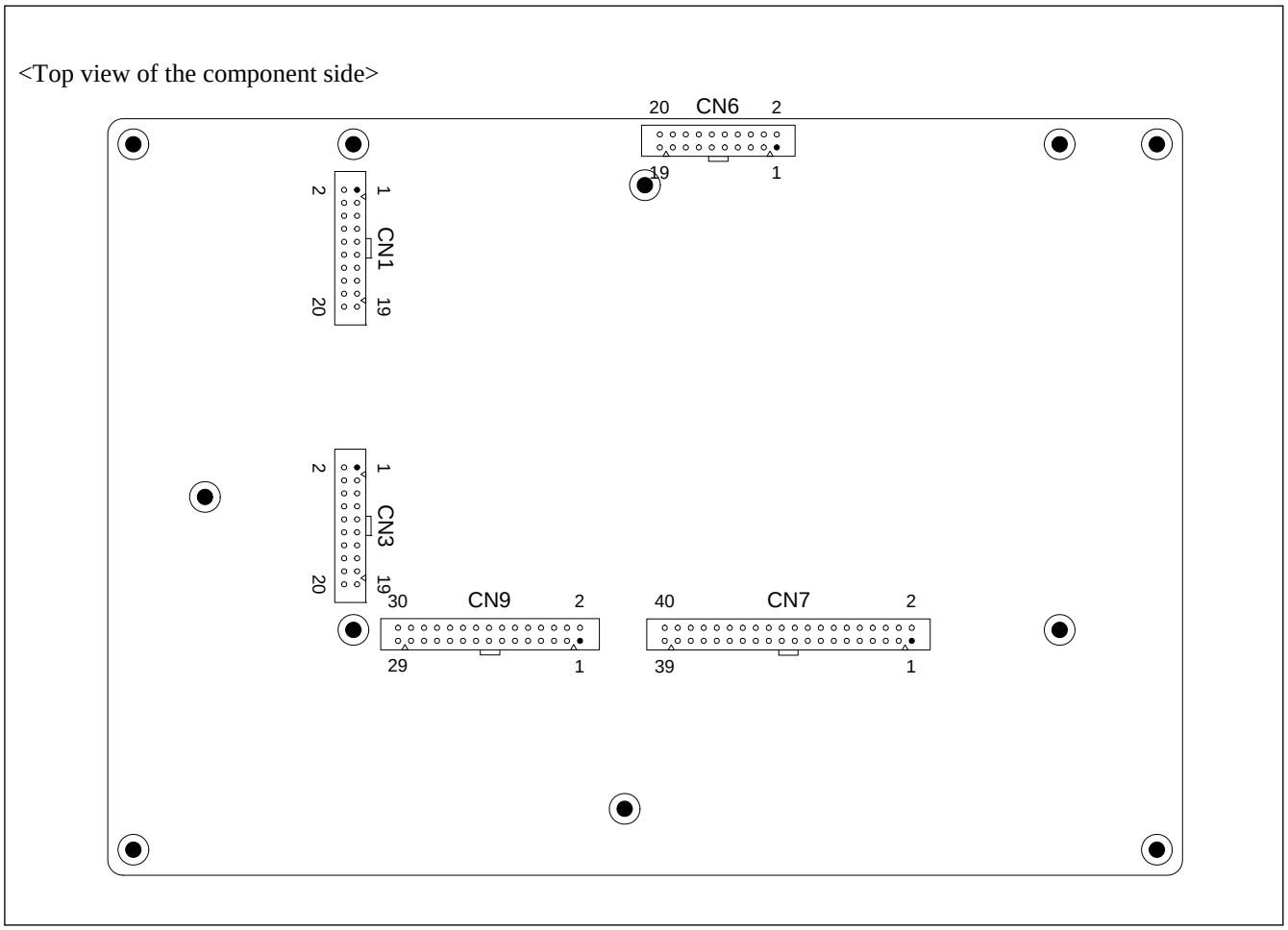


Figure 6.1.2 Connector Pin Assignments（CN1, CN3, CN6, CN7 and CN9）

Table 6.1.1 Connector Pin Descriptions 1（CN1）

Pin No.	Signal Name	Pin No.	Signal Name
1	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / PWM2D / SCK6（NC）	2	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7
3	+5V	4	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6
5	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / RTS5#	6	+3.3V
7	Not connected on the R0K572690C000BR（NC）	8	Not connected on the R0K572690C000BR（NC）
9	PA1 / MD_BOOT1（NC）	10	PA0 / MD_BOOT0（NC）
11	GND	12	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / CTS5#
13	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / SCK5#	14	PG23 / LCD_DATA23 / LCD_TCON6 / TxD5 / AUDATA3
15	PG22 / LCD_DATA22 / LCD_TCON5 / RxD5 / AUDSYNC#	16	GND
17	PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2	18	PJ21 / DV_DATA21 / LCD_DATA21 / LCD_TCON4 / IRQ1 / CTx2 / CTx0&CTx1&CTx2 PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1
19	PJ29 / SSIWS5 / TIOC2A / IERxD	20	PJ30 / SSIDATA5 / TIOC2B / IETxD

Legend : :5V power, :3.3V power, :GND

Table 6.1.2 Connector Pin Descriptions 2（CN3）

Pin No.	Signal Name	Pin No.	Signal Name
1	AVref（NC）	2	AVref（NC）
3	PH1 / AN1 / PINT1	4	PH0 / AN0 / PINT0
5	AVref（NC）	6	AVref（NC）
7	PH3 / AN3 / PINT3	8	PH2 / AN2 / PINT2
9	AVcc	10	AVcc
11	PH5 / AN5 / PINT5 / LCD_EXTCLK（NC）	12	PH4 / AN4 / PINT4（NC）
13	AVcc	14	AVcc
15	PH7 / AN7 / PINT7	16	PH6 / AN6 / PINT6（NC）
17	AVss	18	AVss
19	AVss	20	AVss

Legend : :5V power, :3.3V power, :GND

Table 6.1.3 Connector Pin Descriptions 3（CN6）

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V	2	+5V
3	+5V	4	+5V
5	PC0 / CS0# / MD_BOOT2（NC）	6	PC1 / RD#（NC）
7	PC2 / RD/WR# / SCK6（NC）	8	PC3 / WE0#/DQMLL / RxD6（NC）
9	PC4 / WE1#/WE#/DQMLU / TxD6（NC）	10	+3.3V
11	+3.3V	12	PE6 / SCL3 / RxD6
13	PE7 / SDA3 / RxD7	14	PC5 / RAS# / CRx0 / CRx0/CRx1/CRx2 / IRQ0（NC）
15	PC6 / CAS# / SCK7 / CTx0 / CTx0&CTx1&CTx2（NC）	16	PC7 / CKE / RxD7 / CRx1 / CRx0/CRx1 / IRQ1（NC）
17	PC8 / CS3# / TxD7 / CTx1 / CTx0&CTx1（NC）	18	GND
19	GND	20	CKIO（NC）

Legend : :5V power, :3.3V power, :GND

Table 6.1.4 Connector Pin Descriptions 4（CN7-1）

Pin No.	Signal Name	Pin No.	Signal Name
1	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G	2	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H
3	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E	4	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F
5	PE0 / SCL0 / TCLKA / LCD_EXTCLK	6	RES#
7	PE2 / SCL1 / TCLKC / IOIS16# / DV_VSYNC	8	PE1 / SDA0 / TCLKB / AUDIO_CLK / DV_CLK PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2
9	PE4 / SCL2 / RxD4 / DV_VSYNC	10	PE3 / SDA1 / TCLKD / ADTRG# / DV_HSYNC
11	+3.3V	12	PE5 / SDA2 / RxD5 / DV_HSYNC
13	PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	14	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D
15	PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	16	PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
17	PF10 / CS1# / SSISCK1 / DV_DATA1 / SCK1 / MMC_D5 PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	18	+5V
19	PF12 / SSIDATA1 / DV_DATA3 / TxD1 / MMC_D7 PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	20	PF11 / SSIWS1 / DV_DATA2 / RxD1 / MMC_D6 PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
21	GND	22	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D PJ28 / SSISCK5 / TIOC1B / RTS7#
23	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F PJ30 / SSIDATA5 / TIOC2B / IETxD	24	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E PJ29 / SSIWS5 / TIOC2A / IERxD

Legend : :5V power, :3.3V power, :GND

Table 6.1.5 Connector Pin Descriptions 5（CN7-2）

Pin No.	Signal Name	Pin No.	Signal Name
25	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G PJ24 / SGOUT_0 / SSISCK4 / LCD_TCON3 / SPDIF_IN / SCK7	26	GND
27	PJ26 / SGOUT_2 / SSIDATA4 / LCD_TCON5 / TxD7 PJ31 / DV_CLK	28	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H PJ25 / SGOUT_1 / SSIWS4 / LCD_TCON4 / SPDIF_OUT / RxD7
29	GND	30	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / TIOC4A / DREQ0 / AUDCK
31	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1	32	PJ13 / DV_DATA13 / LCD_DATA13 / PINT5 / PWM2F / TxD5
33	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / SPBMI_1/SPBIO1_1	34	GND
35	PF5 / SSIWS0 / SGOUT_1	36	PF4 / CS5#/CE1A# / SSISCK0 / SGOUT_0
37	PF6 / CE2A# / SSITxD0 / SGOUT_2 PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#	38	PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#
39	GND	40	PJ19 / DV_DATA19 / LCD_DATA19 / MISO0 / TIOC0D/ SIOFRxD / AUDIO_XOUT

Legend : :5V power, :3.3V power, :GND

Table 6.1.6 Connector Pin Descriptions 6（CN9）

Pin No.	Signal Name	Pin No.	Signal Name
1	PG1 / D17 / LCD_DATA1 / IRQ1 / TIOC0B	2	PG0 / D16 / LCD_DATA0 / IRQ0 / TIOC0A
3	PG3 / D19 / LCD_DATA3 / IRQ3 / TIOC0D	4	PG2 / D18 / LCD_DATA2 / IRQ2 / TIOC0C
5	GND	6	PG4 / D20 / LCD_DATA4 / IRQ4 / TIOC1A
7	PG6 / D22 / LCD_DATA6 / IRQ6 / TIOC2A	8	PG5 / D21 / LCD_DATA5 / IRQ5 / TIOC1B
9	PG7 / D23 / LCD_DATA7 / IRQ7 / TIOC2B	10	GND
11	PG9 / D25 / LCD_DATA9 / PINT1 / TIOC3B	12	PG8 / D24 / LCD_DATA8 / PINT0 / TIOC3A
13	PG11 / D27 / LCD_DATA11 / PINT3 / TIOC3D	14	PG10 / D26 / LCD_DATA10 / PINT2 / TIOC3C
15	GND	16	PG12 / D28 / LCD_DATA12 / PINT4
17	PG14 / D30 / LCD_DATA14 / PINT6	18	PG13 / D29 / LCD_DATA13 / PINT5
19	PG25 / LCD_TCON0	20	PG15 / D31 / LCD_DATA15 / PINT7
21	PG26 / LCD_TCON1	22	+5V
23	PG24 / LCD_CLK	24	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
25	+3.3V	26	PG27 / LCD_TCON2 / LCD_EXTCLK（NC）
27	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / PWM2E / SCK7	28	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / TIOC4A / DREQ0 / AUDCK
29	PJ27 / SGOUT_3 / TIOC1A / CTS7#	30	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1

Legend : :5V power, :3.3V power, :GND

6.1.2 Character LCD Module Connector（J1）

The M3A-HS64G01 includes a character LCD module connector (J1).

Figure 6.1.3 shows the character LCD module connector pin assignments. Table 6.1.7 lists their descriptions.

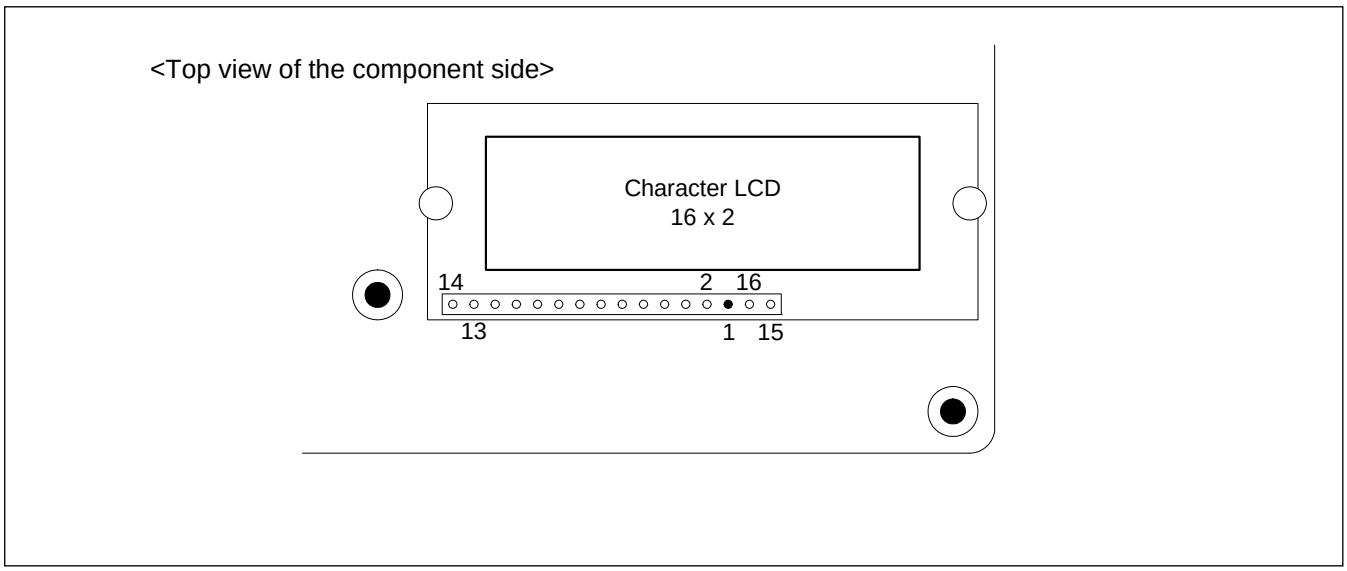


Figure 6.1.3 Character LCD Module Connector Pin Assignments (J1)

Table 6.1.7 Character LCD Module Connector Pin Descriptions (J1)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	+5V
3	Vo（adjust voltage by potentiometer, VR1, to input）	4	RS（**PE6** / SCL3 / RxD6）
5	R/W#（GND）	6	E（**PE7** / SDA3 / RxD7）
7	DB0（**PJ7** / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H）	8	DB1（**PJ6** / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G）
9	DB2（**PJ5** / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F）	10	DB3（**PJ4** / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E）
11	DB4（**PJ3** / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D）	12	DB5（**PJ2** / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C）
13	DB6（**PJ1** / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B）	14	DB7（**PJ0** / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A）
15	A（adjust +5V by the potentiometer, VR2, to input）	16	K（GND）

Note : The signal names in bold style show the setting functions.

6.1.3 SD Card Slot (J2)

The M3A-HS64G01 includes an SD card slot (J2).

Figure 6.1.4shows the SD card slot pin assignments. Table 6.1.8 lists the pin descriptions.

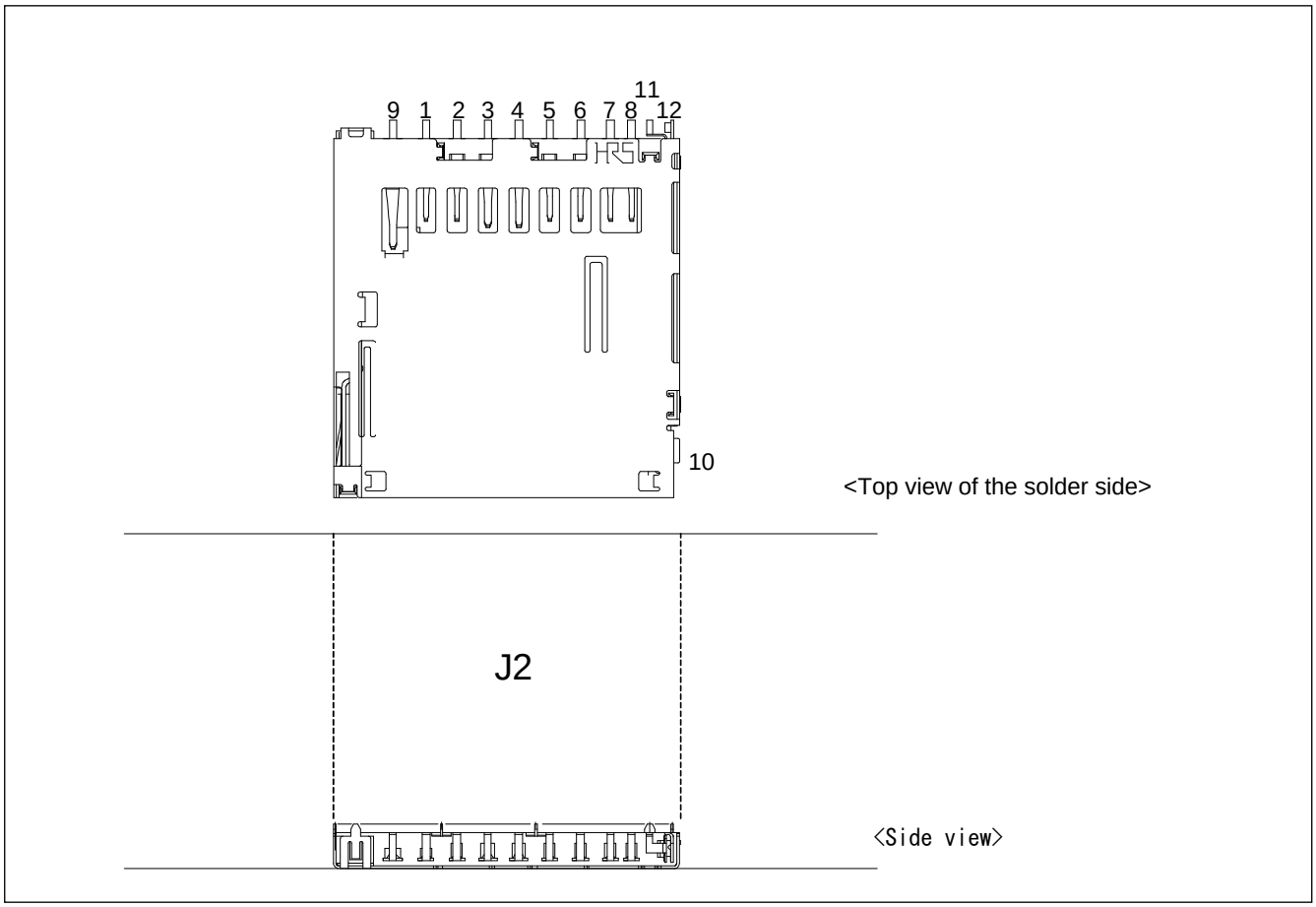


Figure 6.1.4 SD Card Slot Pin Assignments（J2）

Table 6.1.8 SD Card Slot Pin Descriptions（J2）

Pin No.	Signal Name	Pin No.	Signal Name
1	DAT3（PJ6 / DV_DATA6 / LCD_DATA6 / **SD_D3_1** / PWM1G）	2	CMD（PJ5 / DV_DATA5 / LCD_DATA5 / **SD_CMD_1** / PWM1F）
3	GND	4	+3.3V
5	CLK（PJ4 / DV_DATA4 / LCD_DATA4 / **SD_CLK_1** / PWM1E）	6	GND
7	DAT0（PJ3 / DV_DATA3 / LCD_DATA3 / **SD_D0_1** / PWM1D）	8	DAT1（PJ2 / DV_DATA2 / LCD_DATA2 / **SD_D1_1** / PWM1C）
9	DAT2（PJ7 / DV_DATA7 / LCD_DATA7 / **SD_D2_1** / PWM1H）	10	WP（PJ1 / DV_DATA1 / LCD_DATA1 / **SD_WP_1** / PWM1B）
11	CD（PJ0 / DV_DATA0 / LCD_DATA0 / **SD_CD_1** / PWM1A）	12	COMMON（GND）

Note : The signal names in bold style show the setting functions.

6.1.4 Line-out Pin Jacks（J3, J6 and J8）

The M3A-HS64G01 includes line-out pin jacks (J3, J6 and J8).

Figure 6.1.5 shows the pin assignments for the line-out pin jacks. Table 6.1.9lists the pin descriptions.

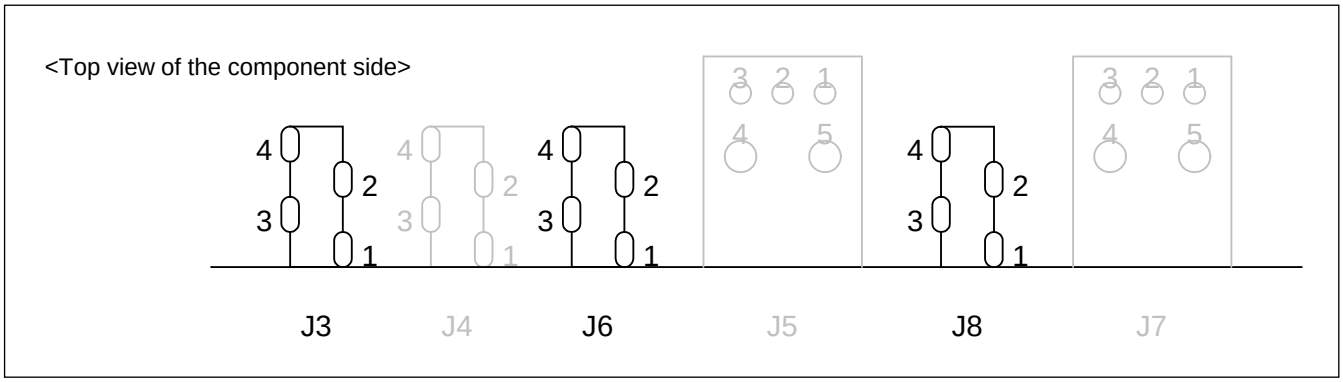


Figure 6.1.5 Assignments of Pins for the Line-out Pin Jacks. (J3, J6 and J8)

Table 6.1.9 Pin Descriptions for Line-out Pin Jacks. (J3, J6 and J8)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	AOUTL D/A converter output L pin）
3	AOUTR (D/A converter output R pin）	4	NC

6.1.5 Microphone Input Pin Jack (J4)

The M3A-HS64G01 includes a microphone input pin jack (J4).

Figure 6.1.6 shows the pin assignments for the microphone input pin jack. Table 6.1.10 lists their descriptions.

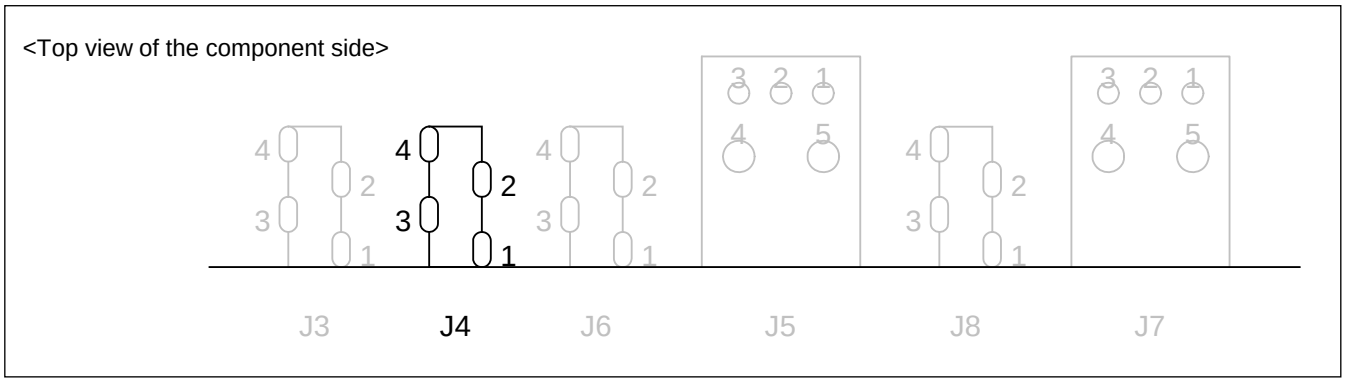


Figure 6.1.6 Pin Assignments for Microphone Input Pin Jack. (J4)

Table 6.1.10 Pin Descriptions for Microphone Input Pin Jack (J4)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	AINL(D/A converter input L pin)
3	AINR (D/A converter input R pin)	4	NC

6.1.6 Audio Connector (J5 and J7)

The M3A-HS64G01 includes optical connectors for audio device output. (J5, J7)

Figure 6.1.7 shows the optical connector pin assignments. Table 6.1.11 lists their descriptions.

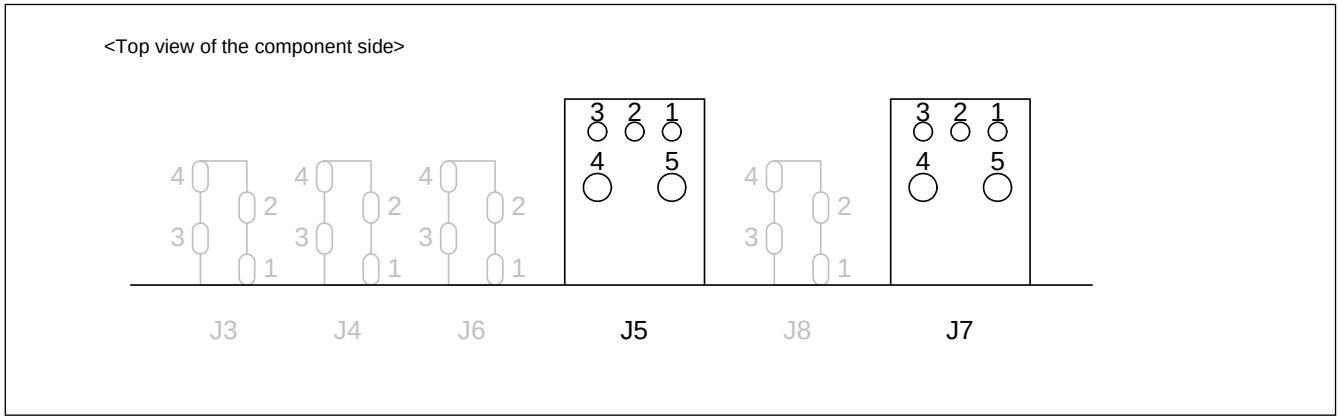


Figure 6.1.7 Optical Connector Pin Assignments (J5 and J7)

Table 6.1.11 Optical Connector Pin Descriptions. (J5 and J7)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	+3.3V
3	TX（D/A converter output pin）	4	NC
5	NC	-	

6.1.7 CD Deck Connector (J9)

The M3A-HS64G01 includes a flexible connecter (J9) for connecting a CD deck to the board.

Figure 6.1.8shows the connector assignments to connect CD deck interface.

Table 6.1.12 shows their descriptions.

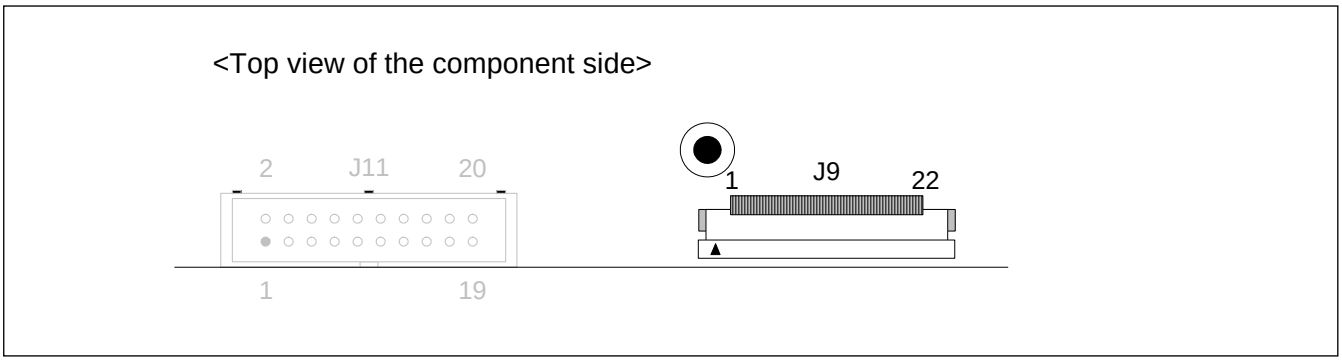


Figure 6.1.8 Assignments of Flexible Connector Pins（J9）

Table 6.1.12 Descriptions of Flexible Connector Pins（J9）

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	GND
3	+8V	4	+8V
5	FLAG6（**PJ14** / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6）	6	NC
7	CDRST (connect output for reset)	8	GND
9	+3.3V	10	+3.3V
11	GND	12	CDFS（**PJ13** / DV_DATA13 / LCD_DATA13 / PINT5 / PWM2F / TxD5）
13	CDSI（PF2 / WAIT# / QMO_1/QIO0_1 / **MOSI1** / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1）	14	CDCK（PF0 / BREQ# / QSPCLK_1 / **RSPCK1** / TIOC4A / DREQ0 / AUDCK）
15	CDSO（PF3 / CS2# / QMI_1/QIO1_1 / **MISO1** / TIOC4D / AUDIO_XOUT / SPBMI_1/SPBIO1_1）	16	NC
17	IIS_BCK（PJ24 / SGOUT_0 / **SSISCK4** / LCD_TCON3 / SPDIF_IN / SCK7）	18	IIS_LRCK（PJ25 / SGOUT_1 / **SSIWS4** / LCD_TCON4 / SPDIF_OUT / RxD7）
19	IIS_DATA（PJ26 / SGOUT_2 / **SSIDATA4** / LCD_TCON5 / TxD7）	20	BLKCK（PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / **IRQ0** / CRx2 / CRx0/CRx1/CRx2）
21	TRANS（**PJ15** / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7）	22	NC

Note : The signal names in bold style show the setting functions.

6.1.8 UART Connector（J10）

The M3A-HS64G01 includes a UART connector (J10) with TTL-level flow control.

Figure 6.1.9 shows the UART connector pin assignments.

Table 6.1.13 lists the pin descriptions.

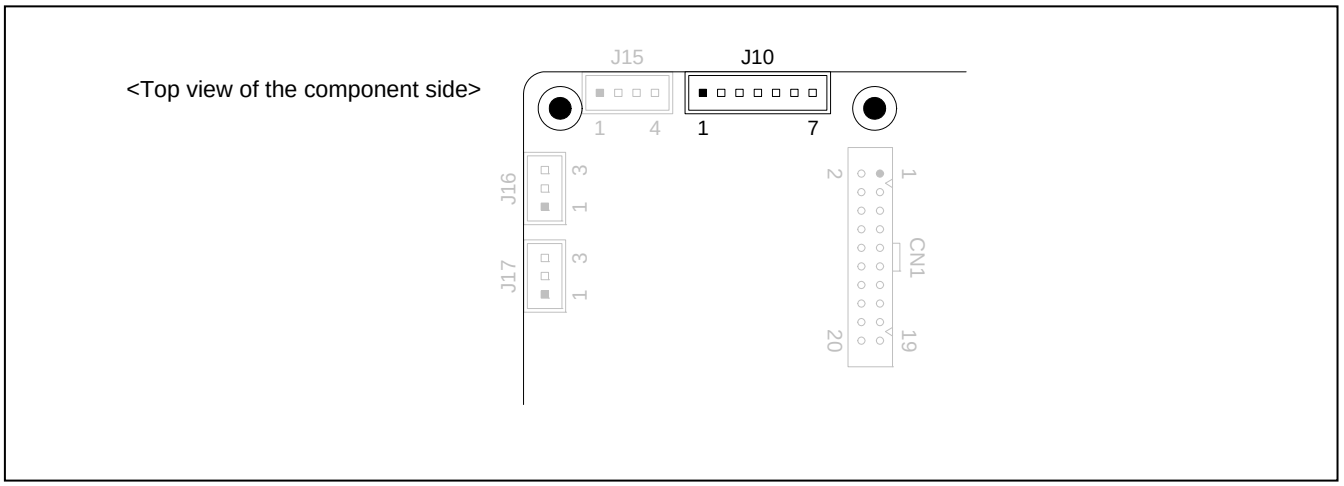


Figure 6.1.9 UART Connector Pin Assignments (J10)

Table 6.1.13 UART Connector Pin Descriptions (J10)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	RxD（PG22 / LCD_DATA22 / LCD_TCON5 / **RxD5** / AUDSYNC#）
3	TxD（PG23 / LCD_DATA23 / LCD_TCON6 / **TxD5** / AUDATA3）	4	SCK（PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / **SCK5#**）
5	CTS#（PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / **CTS5#**）	6	RTS#（PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / **RTS5#**）
7	GND	-	

Note: The signal names in bold style show the setting functions.

6.1.9 External IIC Connector (J11)

The M3A-HS64G01 includes an MIL-spec connector (J11) to connect the external IIC interface.
Figure 6.1.10 shows the external IIC connector pin assignments. Table 6.1.14 lists the pin descriptions.

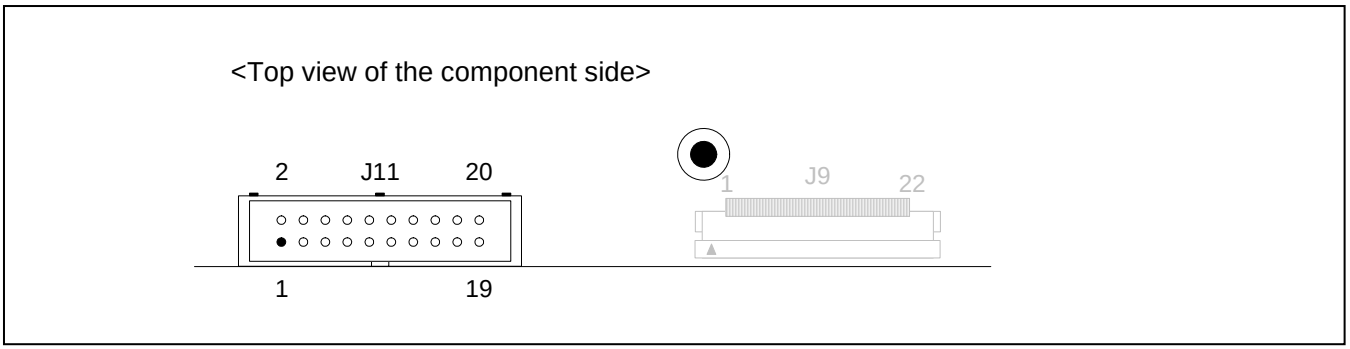


Figure 6.1.10 Assignments of Pins for Connecting External Interfaces (J11)

Table 6.1.14 Descriptions of Connector Pins (J11)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	NC	4	NC
5	NC	6	GND*1
7	NC	8	NC
9	NC	10	GND(1)
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	SCL（PE4 / **SCL2** / RxD4 / DV_VSYNC）	18	SDA（PE5 / **SDA2** / RxD5 / DV_HSYNC）
19	NC	20	GND*1

Note: The signal names in bold style show the setting functions.
1. For compatibility with other boards, this connector is connected via a zero-ohm resister.

6.1.10 LCD Module Connectors（J12 to J14）

The M3A-HS64G01 includes two flexible connectors (J12 and J13) and one MIL-spec connector (J14) for connecting an LCD module.

Figure 6.1.11 shows LCD module connector pin assignments.

Table 6.1.5 and Table 6.1.16 list the pin descriptions. Table 6.1.17 lists the LCD module MIL-spec connector pin descriptions.

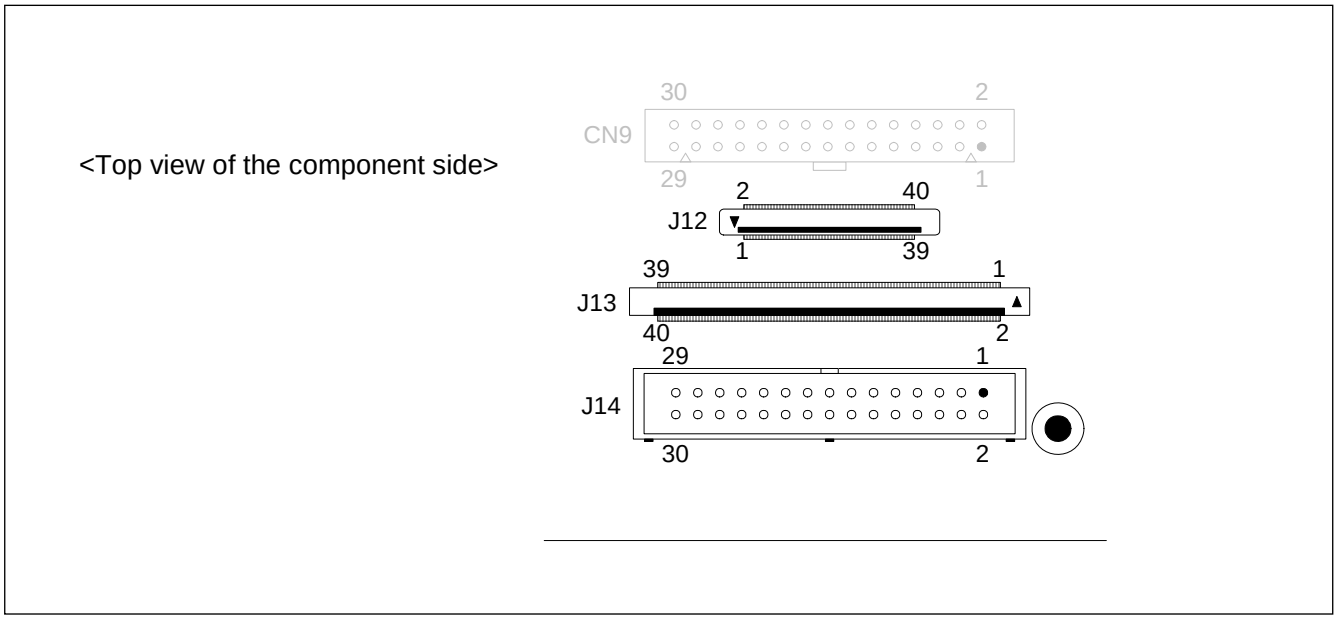


Figure 6.1.11 LCD Module Connector Pin Assignments

Table 6.1.15 LCD Module Connector Pin Descriptions 1 (J12)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	+3.3V	4	DCLK（PG24 / **LCD_CLK**）
5	GND	6	HSYNC（PG26 / **LCD_TCON1**）
7	GND	8	DTMG（PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1）
9	GND	10	NC
11	GND	12	R5（PG15 / D31 / **LCD_DATA15** / PINT7）
13	R4（PG14 / D30 / **LCD_DATA14** / PINT6）	14	R3（PG13 / D29 / **LCD_DATA13** / PINT5）
15	GND	16	R2（PG12 / D28 / **LCD_DATA12** / PINT4）
17	R1（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）	18	R0（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）
19	GND	20	G5（PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C）
21	G4（PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B）	22	G3（PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A）
23	GND	24	G2（PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B）
25	G1（PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A）	26	G0（PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B）
27	GND	28	B5（PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A）
29	B4（PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D）	30	B3（PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C）
31	GND	32	B2（PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B）
33	B1（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）	34	B0（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）
35	PCI（NC）	36	Vctrl（+3.3V）
37	NC	38	NC
39	NC	40	NC

Note: The signal names in bold style show the setting functions.

Table 6.1.16 LCD Module Connector Pin Descriptions 2 (J13)

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	2	DTMG（PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1）
3	HREV（+3.3V）	4	B5（PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A）
5	B4（PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D）	6	B3（PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C）
7	B2（PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B）	8	B1（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）
9	B0（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）	10	+3.3V
11	+3.3V	12	G5（PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C）
13	G4（PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B）	14	G3（PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A）
15	G2（PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B）	16	G1（PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A）
17	G0（PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B）	18	GND
19	R5（PG15 / D31 / **LCD_DATA15** / PINT7）	20	R4（PG14 / D30 / **LCD_DATA14** / PINT6）
21	R3（PG13 / D29 / **LCD_DATA13** / PINT5）	22	R2（PG12 / D28 / **LCD_DATA12** / PINT4）
23	R1（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）	24	R0（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）
25	VREV（+3.3V）	26	NC
27	NC	28	GND
29	DCLK（PG24 / **LCD_CLK**）	30	GND
31	GND	32	GND
33	GND	34	GND
35	TMZ（PH7 / **AN7** / PINT7）	36	GND
37	DIM（+3.3V）	38	NC
39	+5V	40	+5V

Note: The signal names in bold style show the setting functions.

Table 6.1.17 LCD Module Connector MIL-spec Pin Descriptions 3 (J14)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	+3.3V	4	PG15 / D31 / **LCD_DATA15** / PINT7
5	PG14 / D30 / **LCD_DATA14** / PINT6	6	PG13 / D29 / **LCD_DATA13** / PINT5
7	PG12 / D28 / **LCD_DATA12** / PINT4	8	PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D
9	PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C	10	PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B
11	PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A	12	PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B
13	PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A	14	PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B
15	PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A	16	PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D
17	PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C	18	PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B
19	PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A	20	GND
21	PG24 / **LCD_CLK**	22	PG26 / **LCD_TCON1**（LCD_HSYNC）
23	NC	24	NC（can supply 5V via zero-ohm resister）
25	PG25 / **LCD_TCON0**（LCD_VSYNC）	26	PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1（LCD_DE）
27	PJ23 / DV_DATA23 / LCD_DATA23 / **LCD_TCON6** / IRQ3 / CTx1 / CTx0&CTx1（LCD_M_DISP）	28	GND
29	GND	30	GND

Note: The signal names in bold style show the setting functions.

6.1.11 IEBus™ Connector (J15)

The M3A-HS64G01 includes an IEBusTM connector (J15).

Figure 6.1.12 shows the IEBus TM connector pin assignments. Table 6.1.18 lists the pin descriptions.

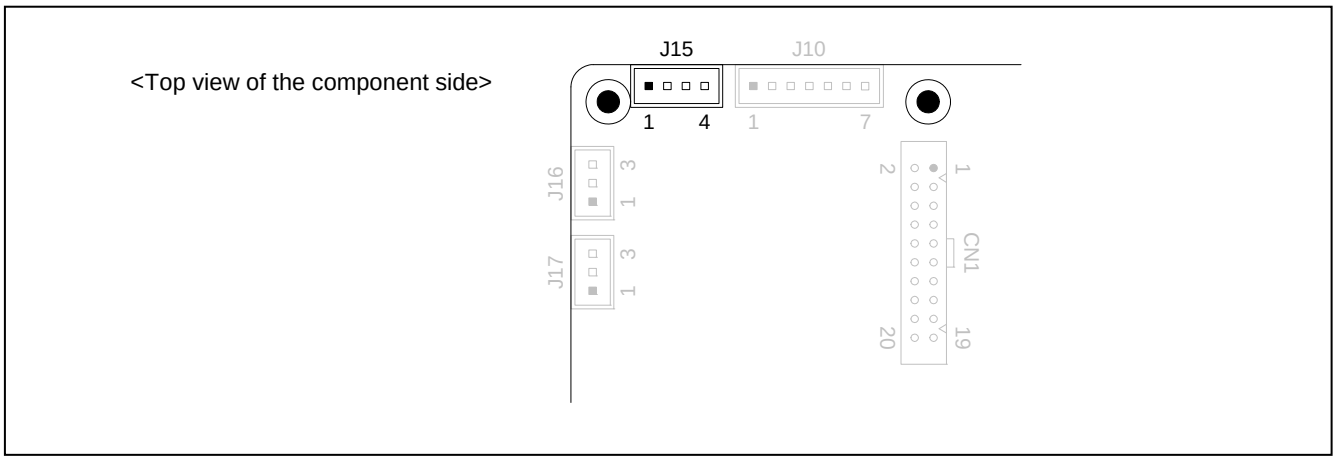


Figure 6.1.12 IEBus™ Connector Pin Assignments（J15）

Table 6.1.18 IEBus™ Connector Pin Descriptions（J15）

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V	2	BUS-
3	BUS+	4	GND

6.1.12 CAN Connector (J16 and J17)

The M3A-HS64G01 includes CAN connectors (J16 and J17). Only J17 can be used to connect R0K572690C000BR.

Figure 6.1.13 shows the CAN connector pin assignments.

Table 6.1.19 lists the pin descriptions.

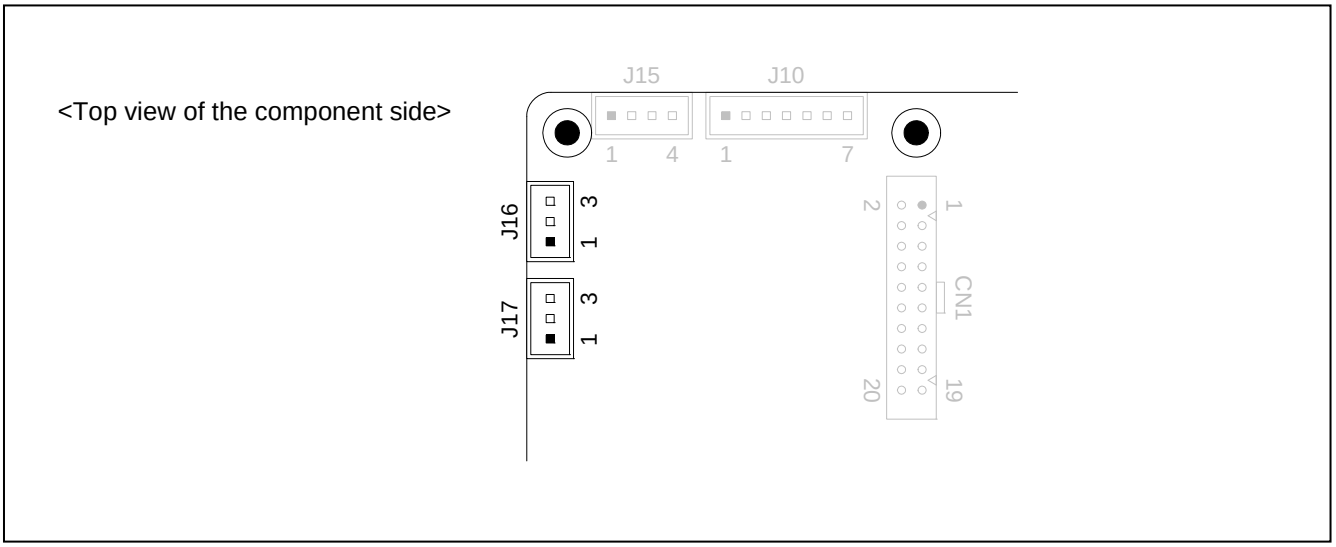


Figure 6.1.13 CAN Connector Pin Assignments（J16 and J17）

Table 6.1.19 CAN Connector Pin Descriptions（J16 and J17）

Pin No.	Signal Name	Pin No.	Signal Name
1	CANH	2	CANL
3	GND	-	

J17 is connected to the channel 2（CTx2/CRx2）.

6.1.13 12V Power Supply Connector (J18)

The M3A-HS64G01 includes a system power supply connector (J18). To avoid an improper insertion, the pin number differs from it for the power supply connector on the CPU board.

Figure 6.1.14 shows power connector pin assignments. Table 6.1.20 lists pin descriptions.

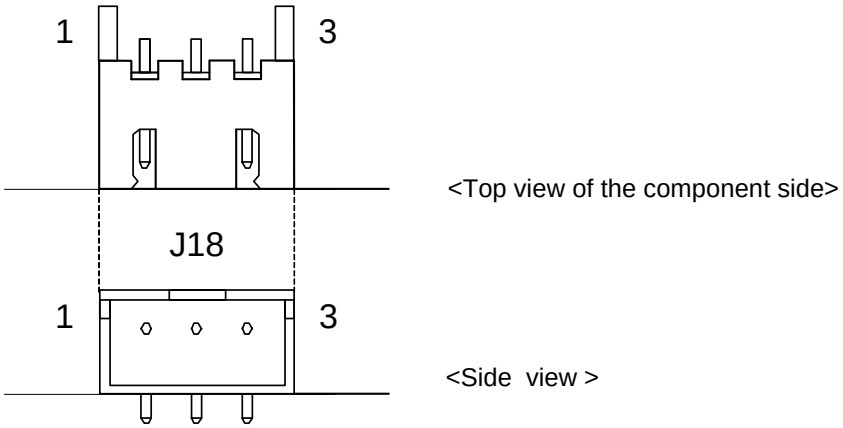


Figure 6.1.14 12V Power Supply Connector Pin Assignments (J18)

Table 6.1.20 12V Power Supply Connector Pin Descriptions (J18)

Pin No.	Signal Name	Pin No.	Signal Name
1	+12V	2	NC
3	GND	-	

6.1.14 12V Input AC Adapter Jack (J19)

The M3A-HS64G01 includes an AC adapter jack (J19) for DC12V input.

Figure 6.1.15 shows pin assignments for 12V input AC adapter jack. Table 6.1.21 lists the pin descriptions.

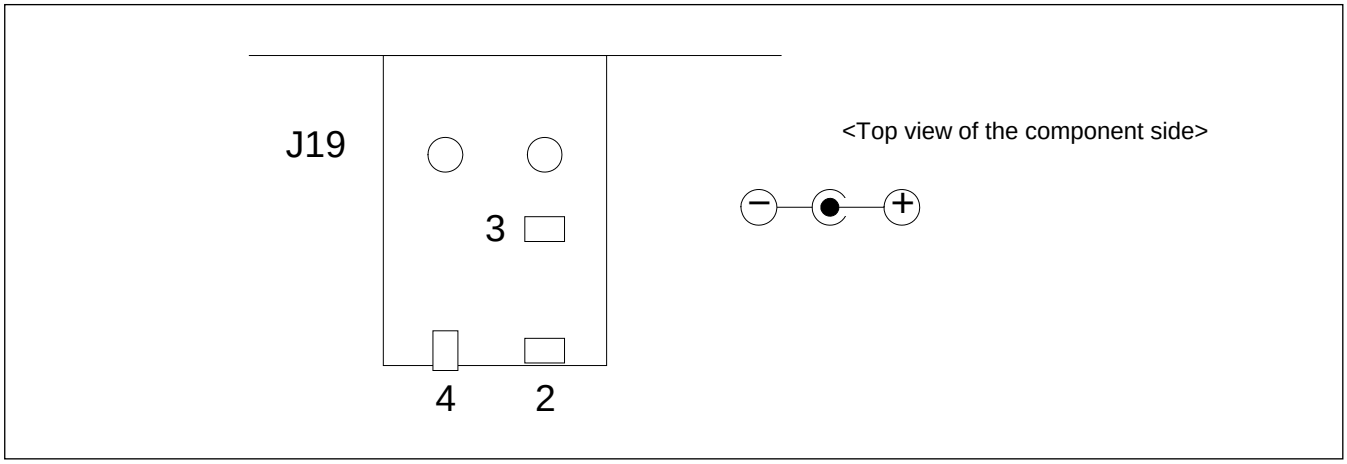


Figure 6.1.15 12V input AC Adapter Pin Assignments (J19)

Table 6.1.21 12V input AC Adapter Pin Descriptions (J19)

Pin No.	Signal Name	Pin No.	Signal Name
1	NC（No pins）	2	+12V
3	GND	4	GND

6.2 M3A-HS64G01 Operating Components

Figure 6.2.1 shows the assignments of the M3A-HS64G01 operating components.

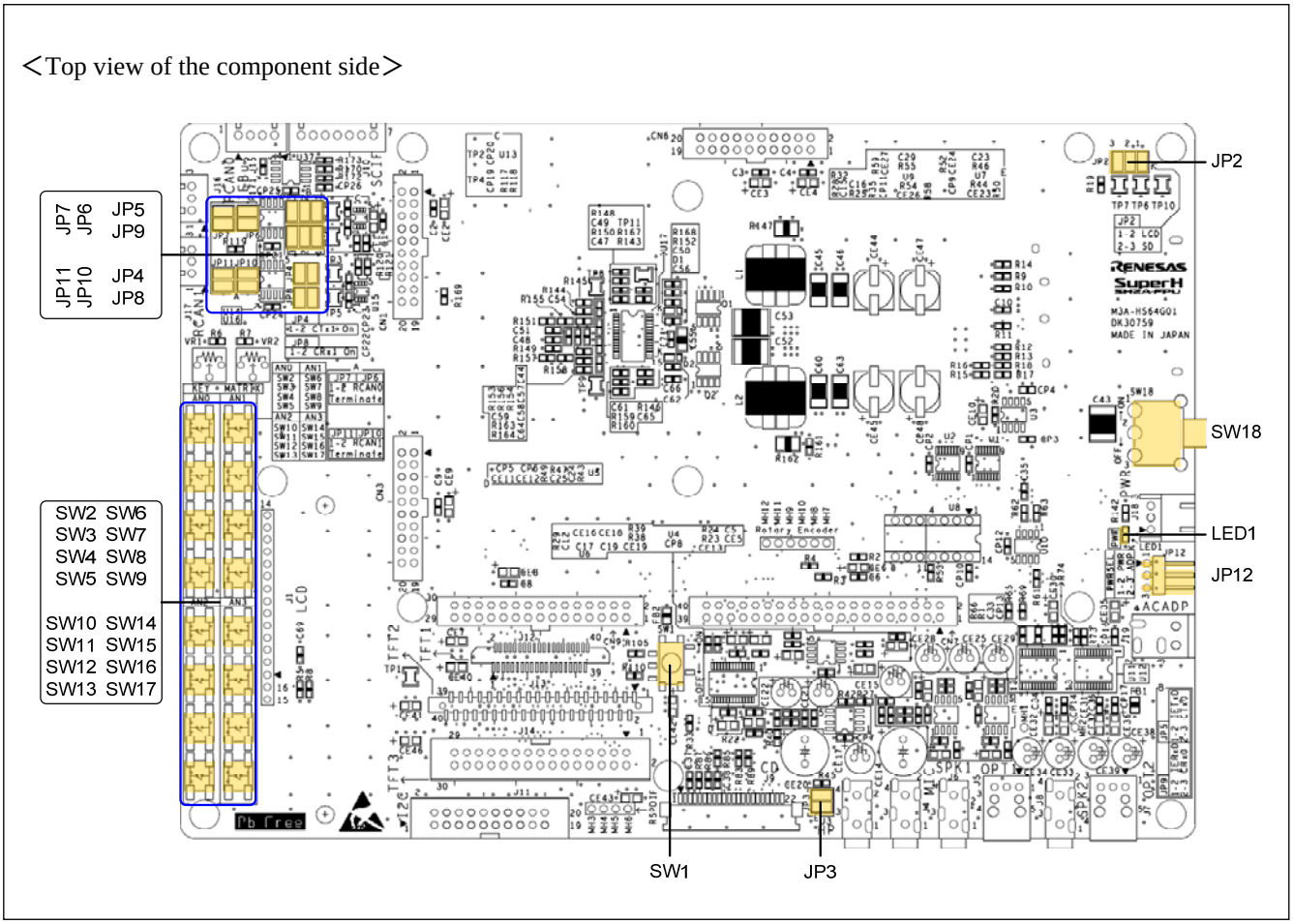


Figure 6.2.1 Assignments of the M3A-HS64G01 Operating Components

6.2.1 Jumpers (JP2 to JP12)

The M3A-HS64G01 includes eleven jumpers.

Figure 6.2.2 shows the jumper assignments. (JP2 to JP12). From Table 6.2.1 to Table6.2.4 list the jumper settings.

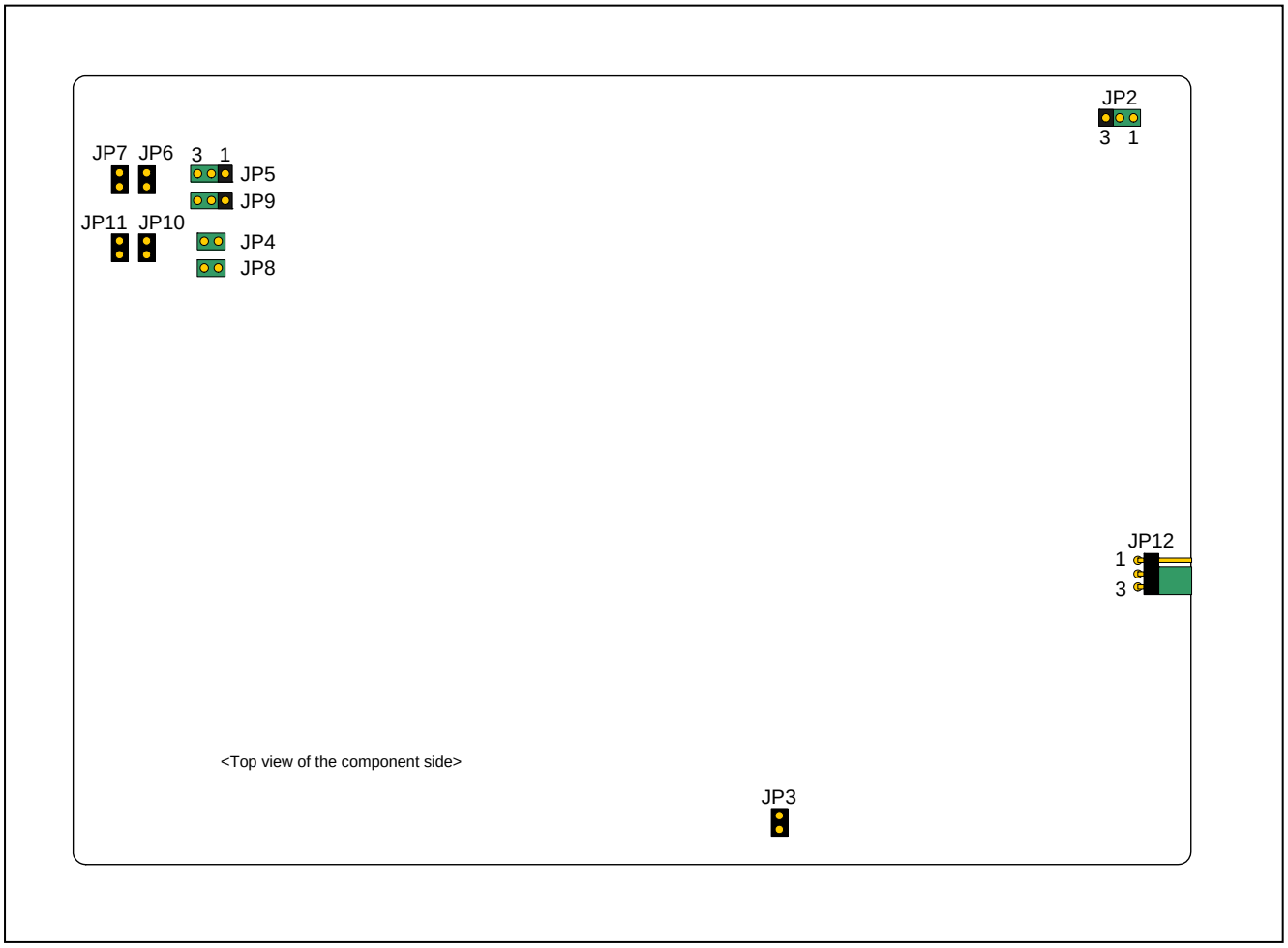


Figure 6.2.2 Jumper Assignments for M3A-HS64G01 (JP2 to JP12)

Table 6.2.1 Multiplexed Pin Switch Jumper Setting (JP2, JP5 and JP9)

Jumper	Setting	Function
JP2 LCD/SD	1−2	Connects the character LCD connector (J1) as the LCD data output pin
	2−3	Connects the SD card slot (J1) as the SDHI input-output pin
JP5 IETxD/PJ30	1−2	Connects to IEBus™ driver (J37) as the IETxD output pin
	2−3	Invalid to R0K572690C000BR
JP9 IERxD/PJ29	1−2	Connects to IEBus™ driver (J37) as the IETxD intput pin
	2−3	Invalid to R0K572690C000BR

: setting by default

Notes: The jumpers shall not changed their setting under operation of this evaluation board. Make sure to change the setting with the power turned off.

Table6.2.2 Plug-in Microphone Jumper Setting (JP3)

Jumper	Setting	Function
JP3	1－2	Supplies the power (Plug-in microphone)
	None(open)	Not supply power (Typical microphone)

: setting by default

Notes: The jumpers shall not changed their setting under operation of this evaluation board. Make sure to change the setting with the power turned off.

Table6.2.3 CAN Evaluation Jumper Setting (JP4, JP6 – JP8, JP10 and JP11)

Jumper	Setting	Function
JP4	1－2	Connects the CTx2 pin to the CAN driver (U16)
CTx2 scheme	None（open）	Leaves the CTx2 pin disconnected to the CAN driver (U16)
JP8	1－2	Connects the CTx2 pin to the CAN driver (U16)
CRx2 scheme	None（open）	Leaves the CTx2 pin disconnected to the CAN driver (U16)
JP6	1－2	Terminates the CANL（ch0）pin
CANL(ch0) end	None（open）	Leaves the CANL（ch0）pin non-terminated
JP7	1－2	Terminates the CANH（ch0）pin
CANH(ch0) end	None（open）	Leaves the CANH（ch0）pin non-terminated
JP10	1－2	Terminates the CANL（ch1）pin
CANL(ch1) end	None（open）	Leaves the CANL（ch1）pin non-terminated
JP11	1－2	Terminates the CANH（ch1）pin
CANH(ch1) end	None（open）	Leaves the CANH（ch1）pin non-terminated

: setting by default

Notes: The jumpers shall not changed their setting under operation of this evaluation board. Make sure to change the setting with the power turned off.

Table6.2.4 Power Supply Switch Jumper Setting (JP12)

Jumper	Setting	Function
JP12	1－2	Supplies the system power from J18
PWRSEL	2－3	Supplies the system power from J19 (with an AC adapter)

: setting by default

Notes: The jumpers shall not changed their setting under operation of this evaluation board. Make sure to change the setting with the power turned off.

6.2.2 Switches and LED

The M3A-HS64G01 includes eighteen switches and one LED.

Figure 6.2.3shows the pin assignments for switches and an LED. Table 6.2.5 lists the switches and Table 6.2.6 lists the LED.

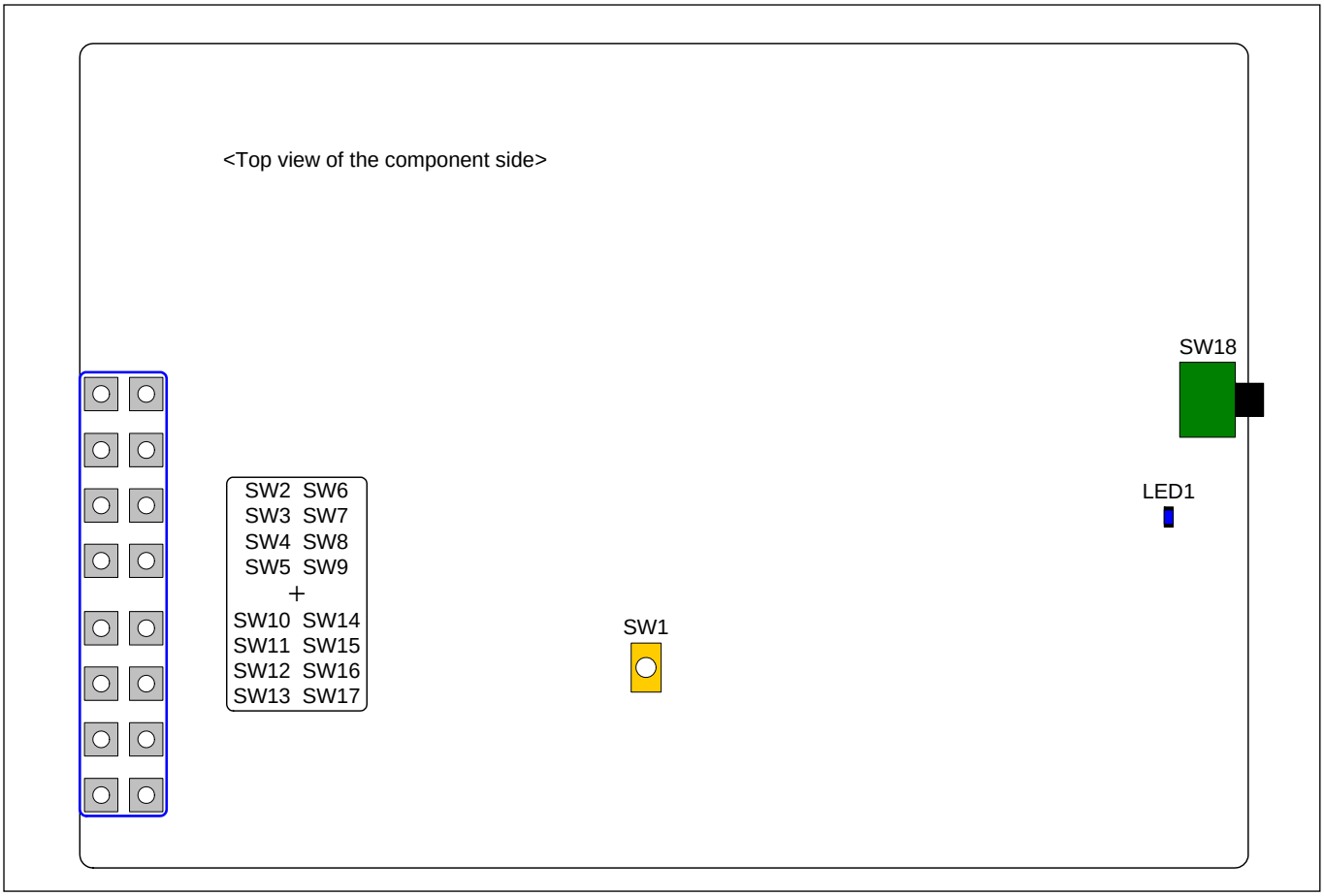


Figure 6.2.3 Switch Assignments on M3A-HS64G01

Table 6.2.5 Function of the Switches on M3A-HS64G01

Switch No.	Function	Notes
SW1	LCD module connector (J12) power switch	Optional
SW2-17	Key entry switch	For details, refer to Section 3.10
SW18	Power supply switch	—

Table 6.2.6 LED for M3A-HS64G01

LED NO.	Color	Function
LED1	Blue	Power supply LED (illuminated when 12V power is supplied)

6.3 M3A-HS64G01 Dimensions

Figure 6.3.1 shows M3A-HS64G01 dimensions as the top view of the component side.

Figure 6.3.2 shows M3A-HS64G01 dimensions as a perspective view.

＜Top view of the component side＞ Unit : mm

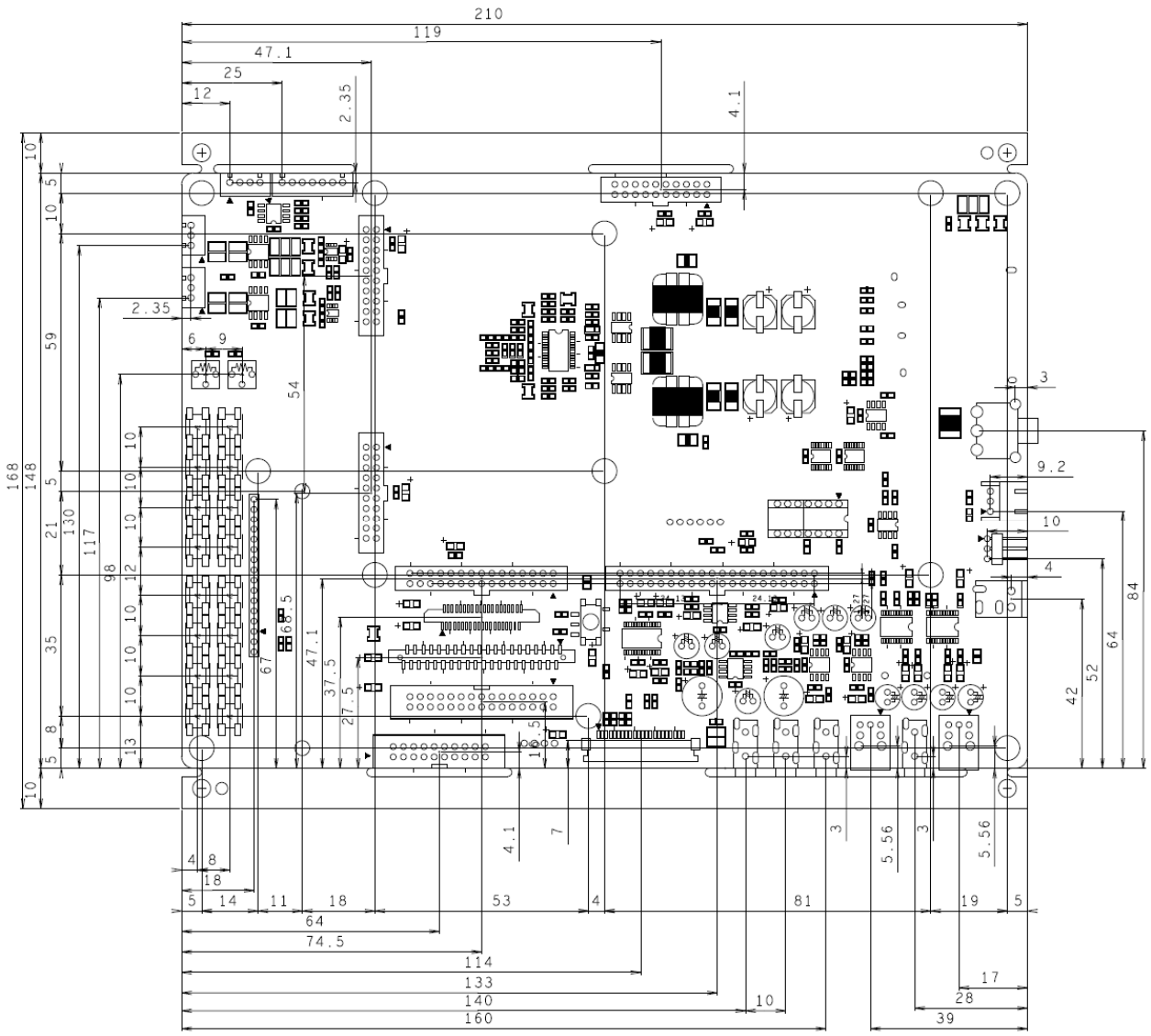


Figure 6.3.1 M3A-HS64G01 Dimensions

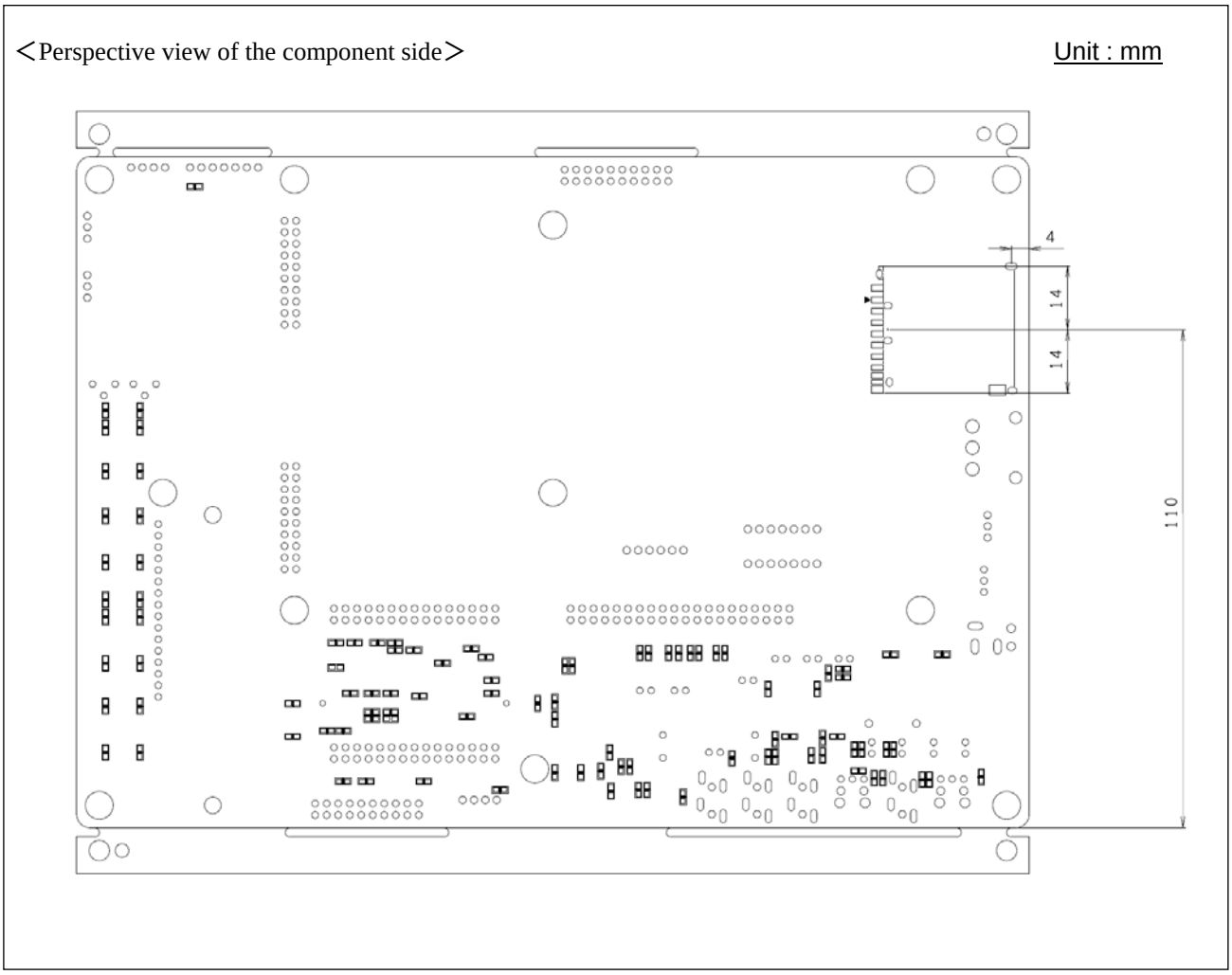


Figure 6.3.2 M3A-HS64G01 Dimensions

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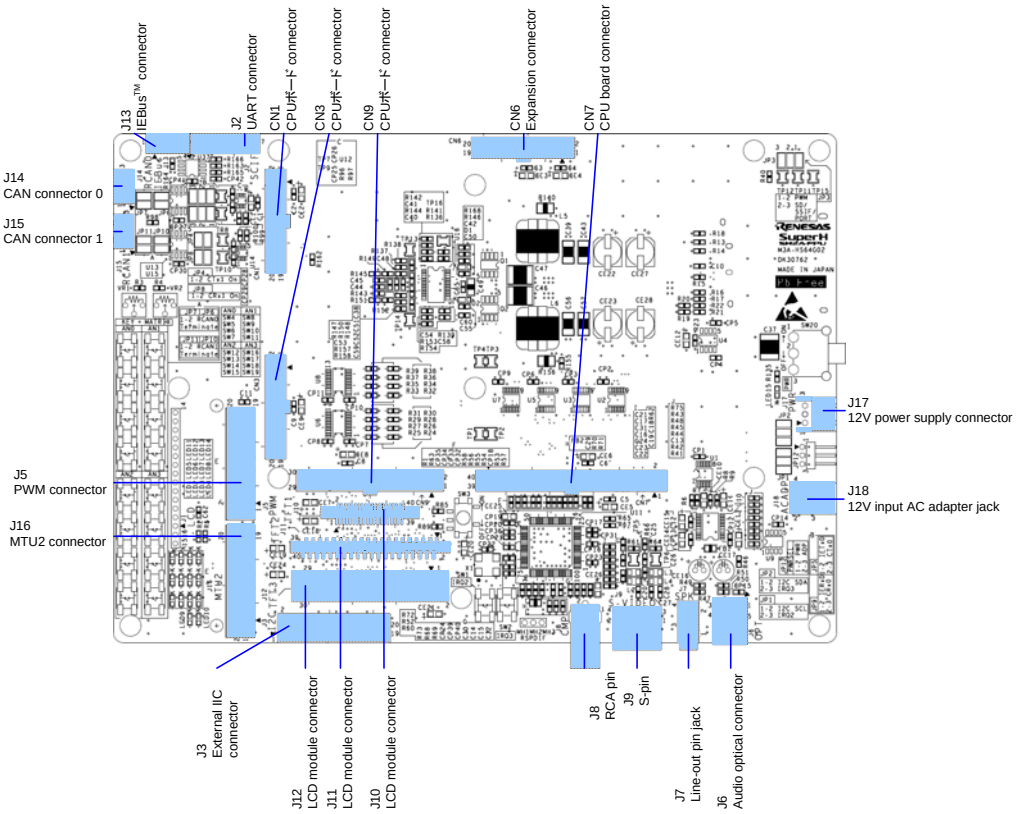
7. M3A-HS64G02 Operating Specification

7.1 M3A-HS64G02 Connectors

Figure 7.1.1 shows connectors assignments on M3A-HS64G02.

＜Top view of the component side＞



＜Top view of the solder side＞

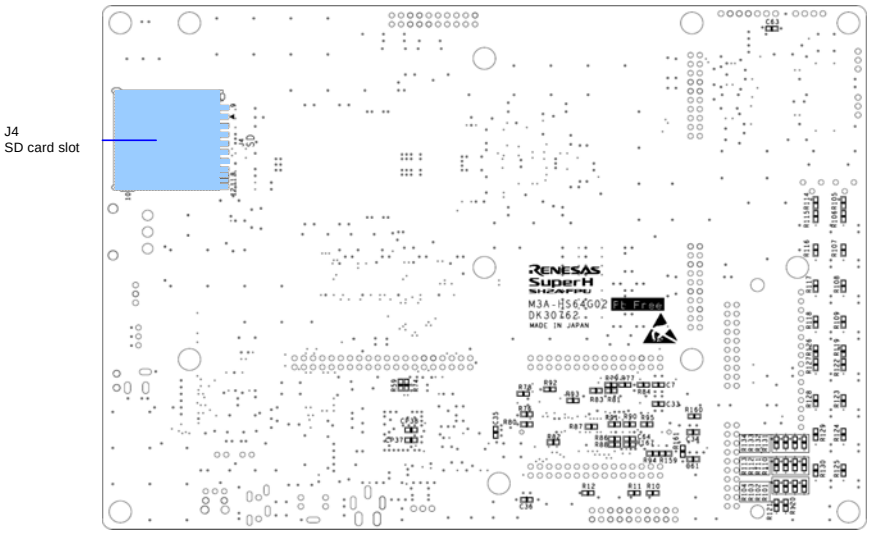


Figure 7.1.1 Connector Assignments on M3A-HS64G02

7.1.1 R0K572690C000BR Connectors (CN1, CN3, CN6, CN7 and CN9)

The M3A-HS64G02 includes MIL-spec connectors (CN1, CN3, CN6, CN7 and CN9) for connecting to R0K572690C000BR.

Figure 7.1.2 shows the connecter pin assignments to connect to R0K572690C000BR. From Table 7.1.1 to Table 7.1.6 list pin descriptions.

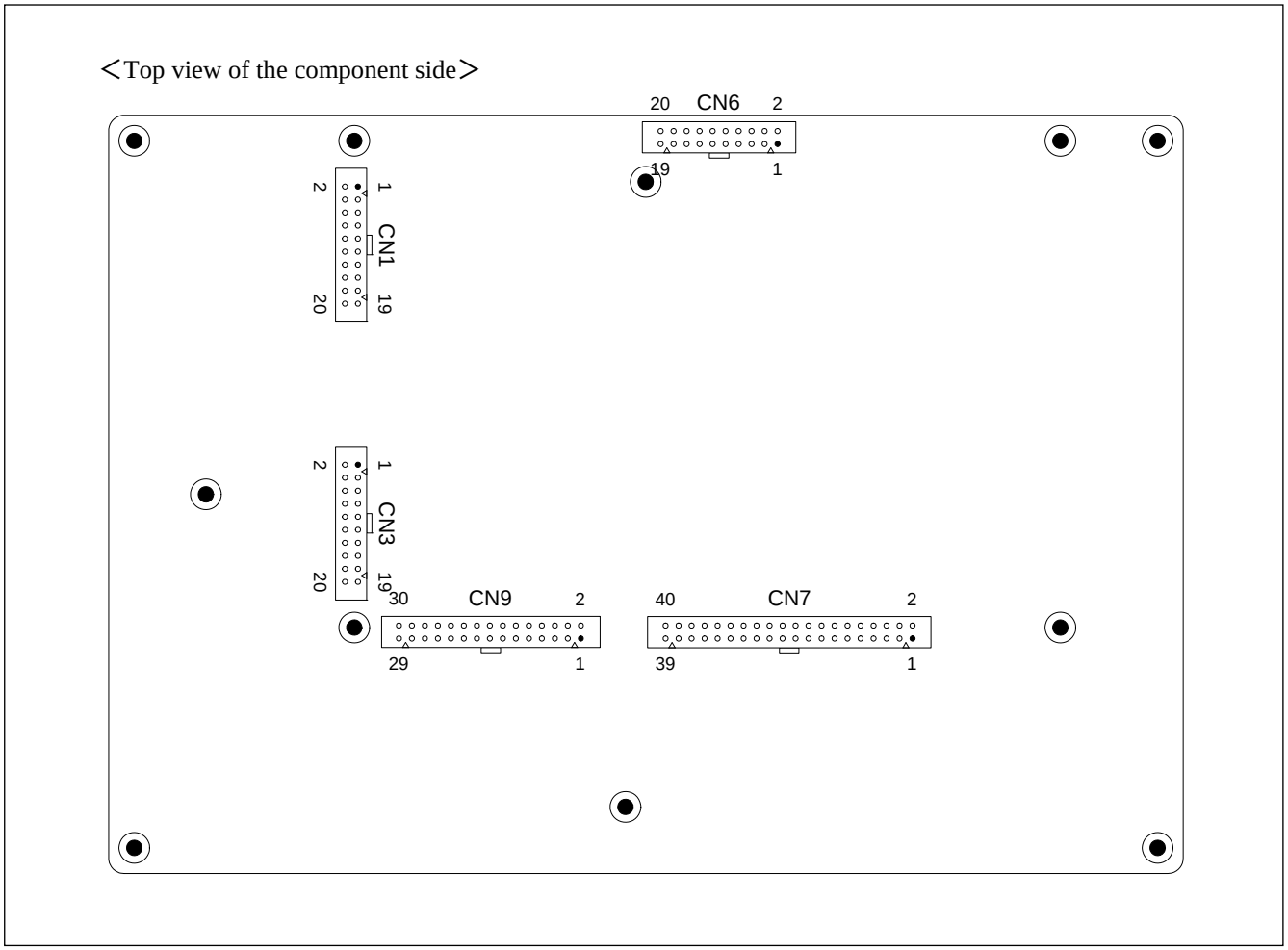


Figure 7.1.2 Connector Pin Assignments（CN1, CN3, CN6, CN7andCN9）

Table 7.1.1 Descriptions of Pins for Connecting to R0K572690C000BR 1 (CN1)

Pin No.	Signal Name	Pin No.	Signal Name
1	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / PWM2D / SCK6	2	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7
3	+5V	4	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6
5	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / RTS5#	6	+3.3V
7	Not connected on R0K572690C000BR（NC）	8	Not connected on R0K572690C000BR（NC）
9	PA1 / MD_BOOT1（NC）	10	PA0 / MD_BOOT0（NC）
11	GND	12	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / CTS5#
13	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / SCK5#	14	PG23 / LCD_DATA23 / LCD_TCON6 / TxD5 / AUDATA3
15	PG22 / LCD_DATA22 / LCD_TCON5 / RxD5 / AUDSYNC#	16	GND
17	PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2	18	PJ21 / DV_DATA21 / LCD_DATA21 / LCD_TCON4 / IRQ1 / CTx2 / CTx0&CTx1&CTx2 PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1
19	PJ29 / SSIWS5 / TIOC2A / IERxD	20	PJ30 / SSIDATA5 / TIOC2B / IETxD

Legend : :5V power, :3.3V power, :GND

Table 7.1.2 Descriptions of Pins for Connecting to R0K572690C000BR 2 (CN3)

Pin No.	Signal Name	Pin No.	Signal Name
1	AVref（NC）	2	AVref（NC）
3	PH1 / AN1 / PINT1	4	PH0 / AN0 / PINT0
5	AVref（NC）	6	AVref（NC）
7	PH3 / AN3 / PINT3	8	PH2 / AN2 / PINT2
9	AVcc	10	AVcc
11	PH5 / AN5 / PINT5 / LCD_EXTCLK（NC）	12	PH4 / AN4 / PINT4（NC）
13	AVcc	14	AVcc
15	PH7 / AN7 / PINT7	16	PH6 / AN6 / PINT6（NC）
17	AVss	18	AVss
19	AVss	20	AVss

Legend : :5V power, :3.3V power, :GND

Table 7.1.3 Descriptions of Pins for Connecting to R0K572690C000BR 3 (CN6)

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V	2	+5V
3	+5V	4	+5V
5	PC0 / CS0# / MD_BOOT2（NC）	6	PC1 / RD#（NC）
7	PC2 / RD/WR# / SCK6（NC）	8	PC3 / WE0#/DQMLL / RxD6（NC）
9	PC4 / WE1#/WE#/DQMLU / TxD6（NC）	10	+3.3V
11	+3.3V	12	PE6 / SCL3 / RxD6
13	PE7 / SDA3 / RxD7	14	PC5 / RAS# / CRx0 / CRx0/CRx1/CRx2 / IRQ0
15	PC6 / CAS# / SCK7 / CTx0 / CTx0&CTx1&CTx2	16	PC7 / CKE / RxD7 / CRx1 / CRx0/CRx1 / IRQ1
17	PC8 / CS3# / TxD7 / CTx1 / CTx0&CTx1	18	GND
19	GND	20	CKIO（NC）

Legend : :5V power, :3.3V power, :GND

Table 7.1.4 Descriptions of Pins for Connecting to R0K572690C000BR 4 (CN7-1)

Pin No.	Signal Name	Pin No.	Signal Name
1	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G	2	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H
3	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E	4	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F
5	PE0 / SCL0 / TCLKA / LCD_EXTCLK	6	RES#
7	PE2 / SCL1 / TCLKC / IOIS16# / DV_VSYNC	8	PE1 / SDA0 / TCLKB / AUDIO_CLK / DV_CLK PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2
9	PE4 / SCL2 / RxD4 / DV_VSYNC	10	PE3 / SDA1 / TCLKD / ADTRG# / DV_HSYNC
11	+3.3V	12	PE5 / SDA2 / RxD5 / DV_HSYNC
13	PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	14	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D
15	PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	16	PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
17	PF10 / CS1# / SSISCK1 / DV_DATA1 / SCK1 / MMC_D5 PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	18	+5V
19	PF12 / SSIDATA1 / DV_DATA3 / TxD1 / MMC_D7 PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	20	PF11 / SSIWS1 / DV_DATA2 / RxD1 / MMC_D6 PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
21	GND	22	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D PJ28 / SSISCK5 / TIOC1B / RTS7#
23	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F PJ30 / SSIDATA5 / TIOC2B / IETxD	24	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E PJ29 / SSIWS5 / TIOC2A / IERxD

Legend : :5V power, :3.3V power, :GND

Table 7.1.5 Descriptions of Pins for Connecting to R0K572690C000BR 5 (CN7-2)

Pin No.	Signal Name	Pin No.	Signal Name
25	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G PJ24 / SGOUT_0 / SSISCK4 / LCD_TCON3 / SPDIF_IN / SCK7	26	GND
27	PJ26 / SGOUT_2 / SSIDATA4 / LCD_TCON5 / TxD7 PJ31 / DV_CLK	28	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H PJ25 / SGOUT_1 / SSIWS4 / LCD_TCON4 / SPDIF_OUT / RxD7
29	GND	30	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / TIOC4A / DREQ0 / AUDCK
31	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1	32	PJ13 / DV_DATA13 / LCD_DATA13 / PINT5 / PWM2F / TxD5
33	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / SPBMI_1/SPBIO1_1	34	GND
35	PF5 / SSIWS0 / SGOUT_1	36	PF4 / CS5#/CE1A# / SSISCK0 / SGOUT_0
37	PF6 / CE2A# / SSITxD0 / SGOUT_2 PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#	38	PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#
39	GND	40	PJ19 / DV_DATA19 / LCD_DATA19 / MISO0 / TIOC0D/ SIOFRxD / AUDIO_XOUT

Legend : :5V power, :3.3V power, :GND

Table 7.1.6 Descriptions of Pins for Connecting to R0K572690C000BR 6 (CN9)

Pin No.	Signal Name	Pin No.	Signal Name
1	PG1 / D17 / LCD_DATA1 / IRQ1 / TIOC0B	2	PG0 / D16 / LCD_DATA0 / IRQ0 / TIOC0A
3	PG3 / D19 / LCD_DATA3 / IRQ3 / TIOC0D	4	PG2 / D18 / LCD_DATA2 / IRQ2 / TIOC0C
5	GND	6	PG4 / D20 / LCD_DATA4 / IRQ4 / TIOC1A
7	PG6 / D22 / LCD_DATA6 / IRQ6 / TIOC2A	8	PG5 / D21 / LCD_DATA5 / IRQ5 / TIOC1B
9	PG7 / D23 / LCD_DATA7 / IRQ7 / TIOC2B	10	GND
11	PG9 / D25 / LCD_DATA9 / PINT1 / TIOC3B	12	PG8 / D24 / LCD_DATA8 / PINT0 / TIOC3A
13	PG11 / D27 / LCD_DATA11 / PINT3 / TIOC3D	14	PG10 / D26 / LCD_DATA10 / PINT2 / TIOC3C
15	GND	16	PG12 / D28 / LCD_DATA12 / PINT4
17	PG14 / D30 / LCD_DATA14 / PINT6	18	PG13 / D29 / LCD_DATA13 / PINT5
19	PG25 / LCD_TCON0	20	PG15 / D31 / LCD_DATA15 / PINT7
21	PG26 / LCD_TCON1	22	+5V
23	PG24 / LCD_CLK	24	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
25	+3.3V	26	PG27 / LCD_TCON2 / LCD_EXTCLK（NC）
27	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / PWM2E / SCK7	28	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / TIOC4A / DREQ0 / AUDCK
29	PJ27 / SGOUT_3 / TIOC1A / CTS7#	30	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1

Legend : :5V power, :3.3V power, :GND

7.1.2 UART Connector (J2)

The M3A-HS64G02 includes UART connector (J2) with TTL level flow control.
Figure 7.1.3 shows the UART connector pin assignments. Table 7.1.7 lists the pin descriptions.

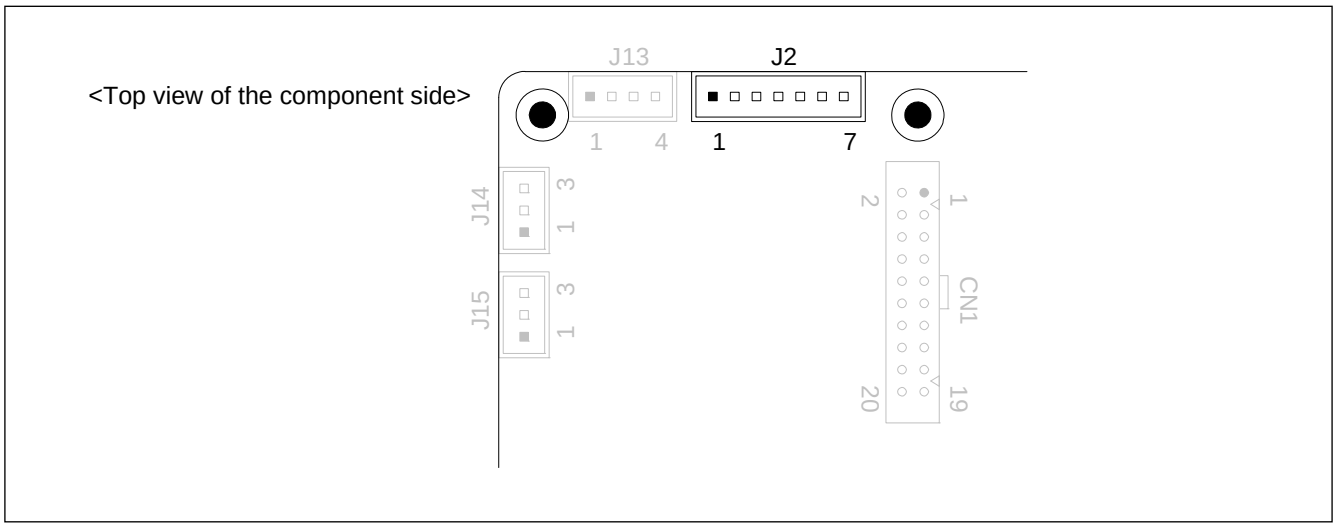


Figure 7.1.3 UART Connector Pin Assignments (J2)

Table 7.1.7 UART Connector Pin Descriptions (J2)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	RxD（PG22 / LCD_DATA22 / LCD_TCON5 / **RxD5** / AUDSYNC#）
3	TxD（PG23 / LCD_DATA23 / LCD_TCON6 / **TxD5** / AUDATA3）	4	NC
5	NC	6	NC
7	GND	-	

Note: The signal names in bold style are setting functions.

7.1.3 External IIC Connector (J3)

M3A-HS64G02 includes an MIL-spec connector (J3) for connecting external IIC interfaces.
Figure 7.1.4 shows the external IIC interfaces connector pin assignments. Table 7.1.8 lists the pin descriptions.

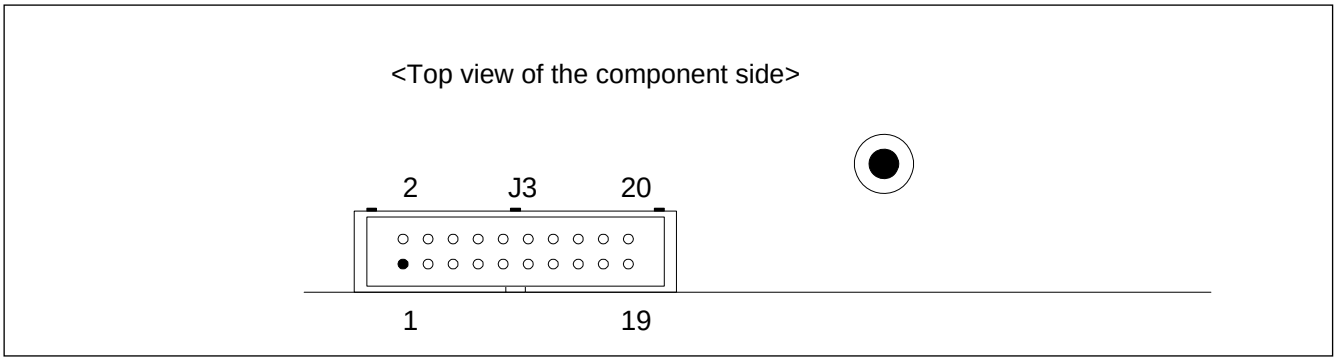


Figure 7.1.4 Connector Pin (J3) Assignments

Table 7.1.8 Connector Pin (J3) Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	NC	4	NC
5	NC	6	GND(1)
7	NC	8	NC
9	NC	10	GND(1)
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	SCL（PE0 / **SCL0** / TCLKA / LCD_EXTCLK）	18	SDA（PE1 / **SDA0** / TCLKB / AUDIO_CLK / DV_CLK）
19	NC	20	GND (1)

Notes: The signal names in bold style are setting functions.
1. For compatibility with other boards, this connector is connected via a zero-ohm resister.

7.1.4 SD Card Slot (J4)

M3A-HS64G02 includes an SD card slot (J4).

Figure 7.1.5 shows the deployment of the pins for SD card slot. Table 7.1.9 lists their descriptions.

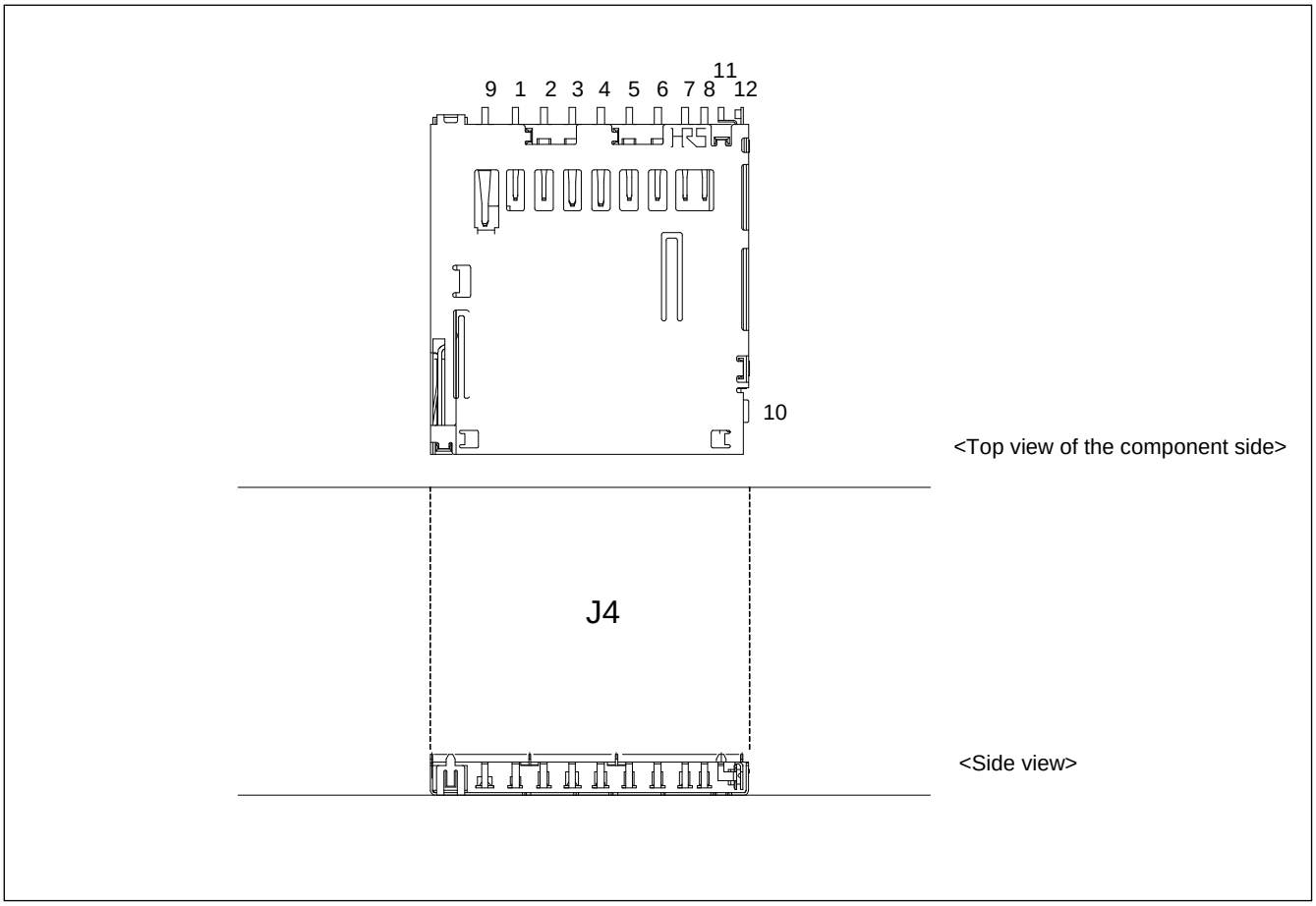


Figure 7.1.5 Diagram of the SD Card Slot (J4)

Table 7.1.9 Descriptions of the SD Card Slot (J4)

Pin No.	Signal Name	Pin No.	Signal Name
1	DAT3（PJ6 / DV_DATA6 / LCD_DATA6 / **SD_D3_1** / PWM1G）	2	CMD（PJ5 / DV_DATA5 / LCD_DATA5 / **SD_CMD_1** / PWM1F）
3	GND	4	+3.3V
5	CLK（PJ4 / DV_DATA4 / LCD_DATA4 / **SD_CLK_1** / PWM1E）	6	GND
7	DAT0（PJ3 / DV_DATA3 / LCD_DATA3 / **SD_D0_1** / PWM1D）	8	DAT1（PJ2 / DV_DATA2 / LCD_DATA2 / **SD_D1_1** / PWM1C）
9	DAT2（PJ7 / DV_DATA7 / LCD_DATA7 / **SD_D2_1** / PWM1H）	10	WP（PJ1 / DV_DATA1 / LCD_DATA1 / **SD_WP_1** / PWM1B）
11	CD（PJ0 / DV_DATA0 / LCD_DATA0 / **SD_CD_1** / PWM1A）	12	COMMON（GND）

Note : The signal names in bold style are setting functions.

7.1.5 PWM Connector (J5)

M3A-HS64G02 includes MIL standard connector (J5) for PWM output. Only one channel can be used on R0K572690C000BR.

Figure 7.1.6 shows the deployment of PWM connector pins. Table 7.1.10 lists their descriptions.

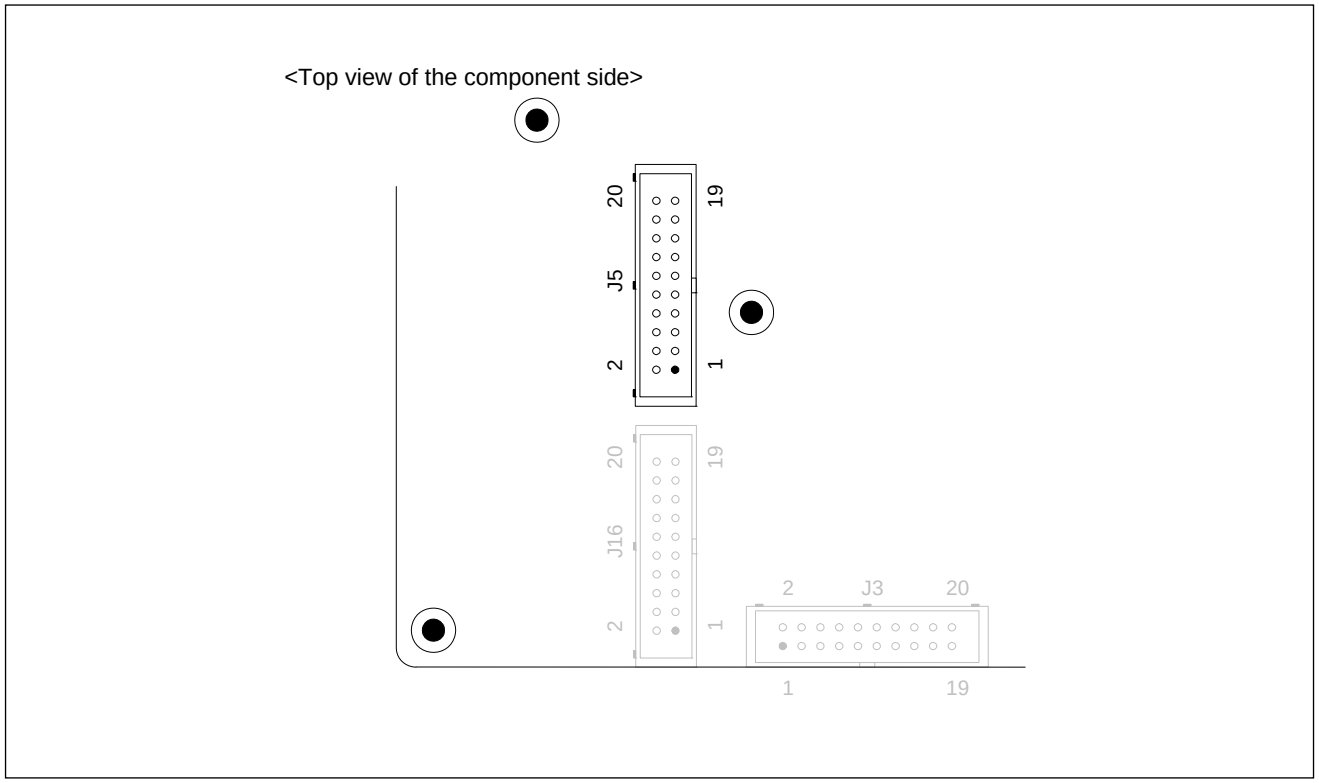


Figure 7.1.6 Diagram of PWM Connector (J5)

Table 7.1.10 Assignments of PWM Connector (J5)

Pin No.	Signal Name	Pin No.	Signal Name
1	PWM1A（PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / **PWM1H**）	2	PWM1B（PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / **PWM1G**）
3	PWM1C（PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / **PWM1F**）	4	PWM1D（PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / **PWM1E**）
5	PWM1E（PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / **PWM1D**）	6	PWM1F（PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / **PWM1C**）
7	PWM1G（PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / **PWM1B**）	8	PWM1H（PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / **PWM1A**）
9	GND	10	GND
11	PF4 / CS5#/CE1A# / SSISCK0 / SGOUT_0	12	PF5 / SSIWS0 / SGOUT_1
13	PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#	14	PF6 / CE2A# / SSITxD0 / SGOUT_2 PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#
15	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / RTS5#	16	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6
17	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7	18	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / PWM2D / SCK6
19	+5V	20	+5V

Note : The signal names in bold style are setting functions.

7.1.6 Audio Connector (J6)

M3A-HS64G02 includes an optical connector (J6) for connecting to audio devices.
Figure 7.1.7shows the deployment of the pins for the optical connector. Table 7.1.11 lists their descriptions.

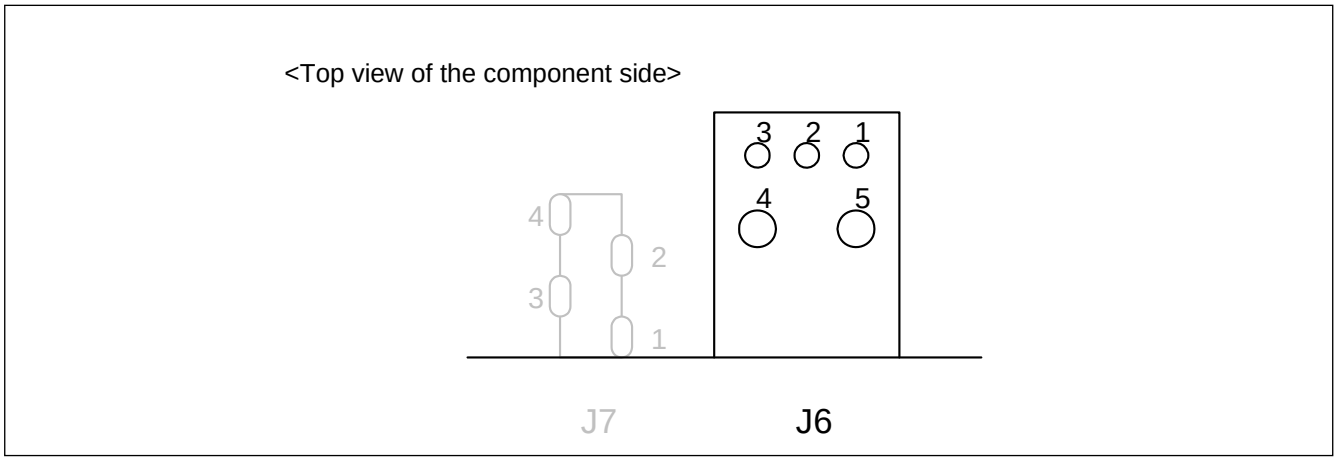


Figure 7.1.7 Diagram of the Optical Connector (J6)

Table 7.1.11 Assignments of the Optical Connector (J6)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	+3.3V
3	TX（for optical output on D/A converter）	4	NC
5	NC	-	

7.1.7 Line-out Pin jack (J7）

M3A-HS64G02 includes a line-out pin jack (J7).
Figure 7.1.8 shows the deployment of the pins of line-out pin jack. Table 7.1.12 lists their descriptions.

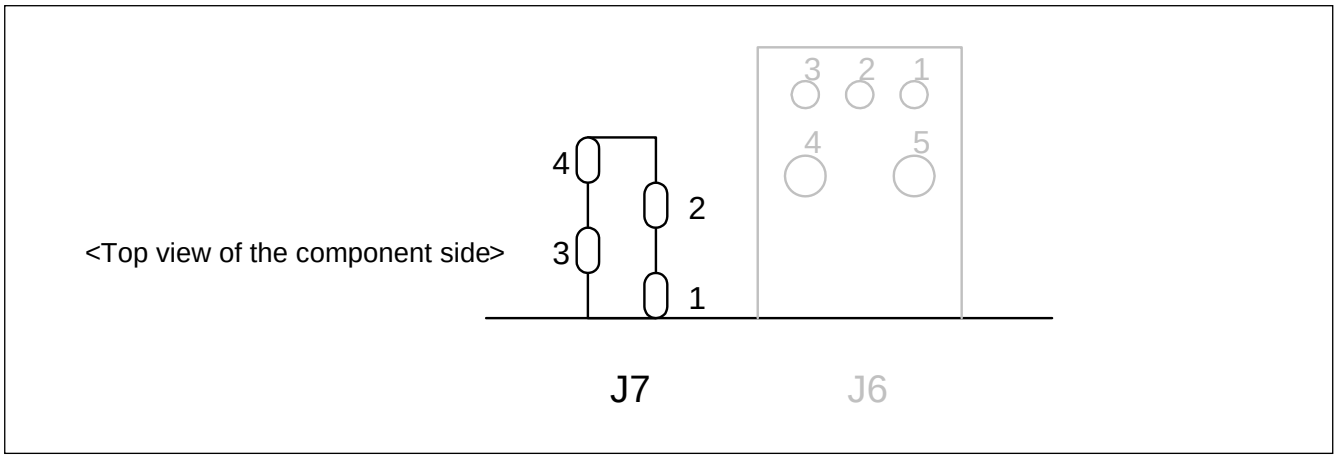


Figure 7.1.8 Diagram of Line-out Pin Jack (J7)

Table 7.1.12 Assignments of Line-out Pin Jack (J7)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	AOUTL（L-pin for analog output on D/A converter）
3	AOUTR（R-pin for analog output on D/A converter）	4	NC

7.1.8 RCA Connector (J8)

M3A-HS64G02 includes an RCA connector (J8).
Figure 7.1.9 shows the deployment of the RCA connector pins. Table 7.1.13 lists their descriptions.

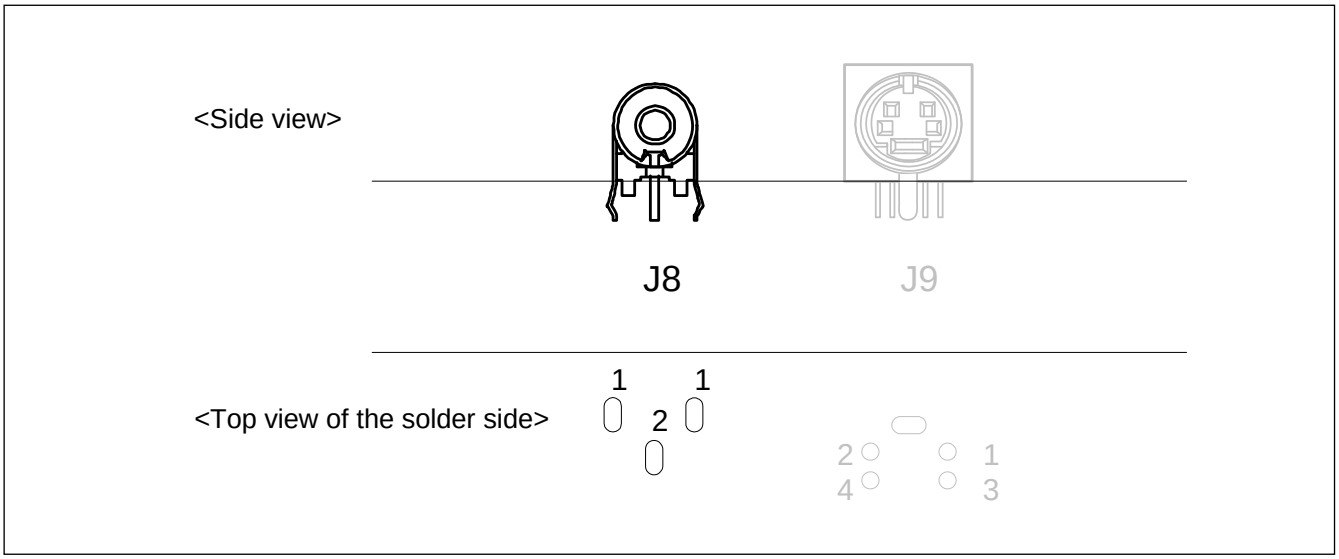


Figure 7.1.9 Diagram of RCA Connector Pins (J8)

Table 7.1.13 Descriptions of RCA Connector Pins (J8)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	AIN2（analog input pin for a video decoder）

7.1.9 S-pin Connector (J9)

M3A-HS64G02 includes S-pin connector (J9）.

Figure 7.1.10 shows the deployment of the S-pin connector. Table 7.1.14 lists its descriptions.

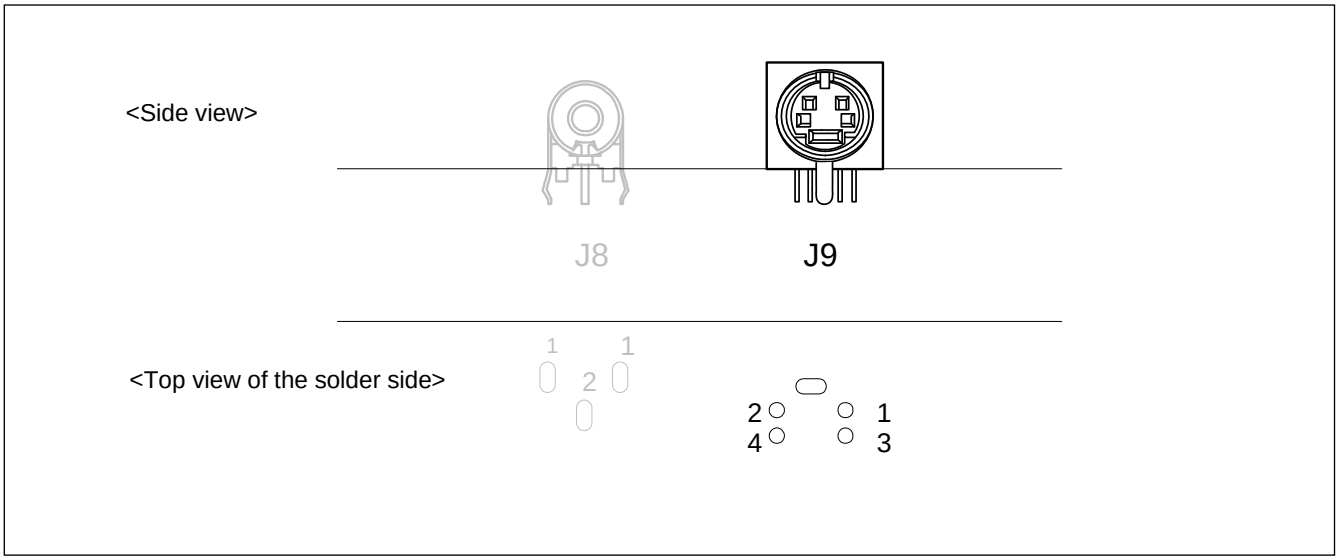


Figure 7.1.10 Diagram of S-Terminal Connector (J9)

Table 7.1.14 Assignments of S-Terminal Connector (J9)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	GND
3	AIN2（analog input pin for a video decoder）	4	AIN5（analog input pin for a video decoder）

7.1.10 LCD Module Connector (J10 to J12)

M3A-HS64G02 includes flexible connectors (J10 and J11) to connect to LCD module and one MIL standard connector (J12).

Figure 7.1.11 shows the flexible connector pins for LCD module. Table 7.1.15 and Table 7.1.16 list the descriptions for flexible connector pins for LCD module, and Table 7.1.17 lists descriptions of MIL standard connector pins.

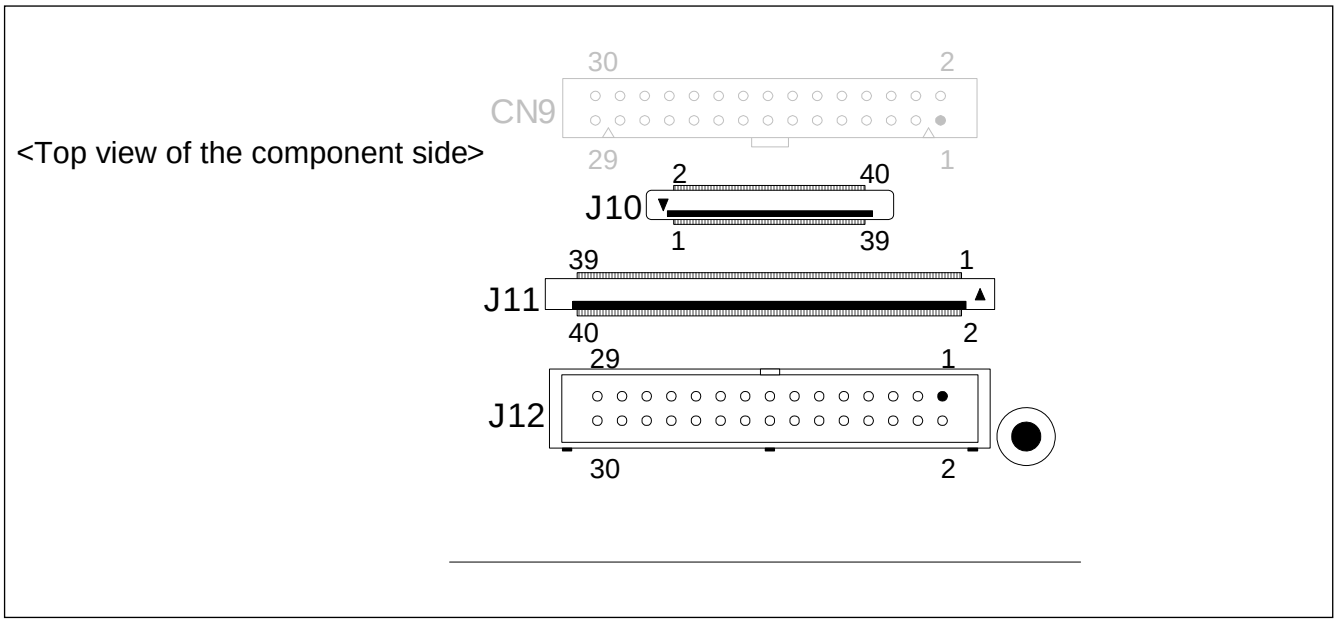


Figure 7.1.11 Diagram of Connector Pins for LCD Module (J10 to J12)

Table 7.1.15 Descriptions of Flexible Connector Pins for LCD Module 1 (J10)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	+3.3V	4	DCLK（PG24 / **LCD_CLK**）
5	GND	6	HSYNC（PG26 / **LCD_TCON1**）
7	GND	8	DTMG（PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1）
9	GND	10	NC
11	GND	12	R5（PG15 / D31 / **LCD_DATA15** / PINT7）
13	R4（PG14 / D30 / **LCD_DATA14** / PINT6）	14	R3（PG13 / D29 / **LCD_DATA13** / PINT5）
15	GND	16	R2（PG12 / D28 / **LCD_DATA12** / PINT4）
17	R1（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）	18	R0（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）
19	GND	20	G5（PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C）
21	G4（PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B）	22	G3（PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A）
23	GND	24	G2（PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B）
25	G1（PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A）	26	G0（PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B）
27	GND	28	B5（PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A）
29	B4（PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D）	30	B3（PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C）
31	GND	32	B2（PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B）
33	B1（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）	34	B0（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）
35	PCI（NC）	36	Vctrl（PF0 / BREQ# / QSPCLK_1 / RSPCK1 / **TIOC4A** / DREQ0 / AUDCK）
37	NC	38	NC
39	NC	40	NC

Note: The signal names in bold style are setting functions.

Table 7.1.16 Descriptions of Flexible Connector Pins for LCD Module 2 (J11)

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	2	DTMG（PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1）
3	HREV（+3.3V）	4	B5（PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A）
5	B4（PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D）	6	B3（PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C）
7	B2（PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B）	8	B1（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）
9	B0（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）	10	+3.3V
11	+3.3V	12	G5（PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C）
13	G4（PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B）	14	G3（PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A）
15	G2（PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B）	16	G1（PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A）
17	G0（PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B）	18	GND
19	R5（PG15 / D31 / **LCD_DATA15** / PINT7）	20	R4（PG14 / D30 / **LCD_DATA14** / PINT6）
21	R3（PG13 / D29 / **LCD_DATA13** / PINT5）	22	R2（PG12 / D28 / **LCD_DATA12** / PINT4）
23	R1（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）	24	R0（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）
25	VREV（+3.3V）	26	NC
27	NC	28	GND
29	DCLK（PG24 / **LCD_CLK**）	30	GND
31	GND	32	GND
33	GND	34	GND
35	TMZ（PH7 / **AN7** / PINT7）	36	GND
37	DIM（PF0 / BREQ# / QSPCLK_1 / RSPCK1 / **TIOC4A** / DREQ0 / AUDCK）	38	NC
39	+5V	40	+5V

Note: The signal names in bold style are setting functions.

Table 7.1.17 Descriptions of MIL Standard Connector Pins for LCD Module (J12)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	+3.3V	4	PG15 / D31 / **LCD_DATA15** / PINT7
5	PG14 / D30 / **LCD_DATA14** / PINT6	6	PG13 / D29 / **LCD_DATA13** / PINT5
7	PG12 / D28 / **LCD_DATA12** / PINT4	8	PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D
9	PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C	10	PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B
11	PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A	12	PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B
13	PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A	14	PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B
15	PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A	16	PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D
17	PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C	18	PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B
19	PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A	20	GND
21	PG24 / **LCD_CLK**	22	PG26 / **LCD_TCON1**（LCD_HSYNC）
23	NC	24	NC（can supply 5V power via zero-ohm resistor）
25	PG25 / **LCD_TCON0**（LCD_VSYNC）	26	PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1（LCD_DE）
27	PJ23 / DV_DATA23 / LCD_DATA23 / **LCD_TCON6** / IRQ3 / CTx1 / CTx0&CTx1（LCD_M_DISP）	28	GND
29	GND	30	GND

Note: The signal names in bold style are setting functions.

7.1.11 IEBus™ Connector (J13)

M3A-HS64G02 includes an IEBusTM connector (J13).

Figure 7.1.12 shows the deployment of the IEBusTM connector pins . Table 7.1.18 lists their descriptions

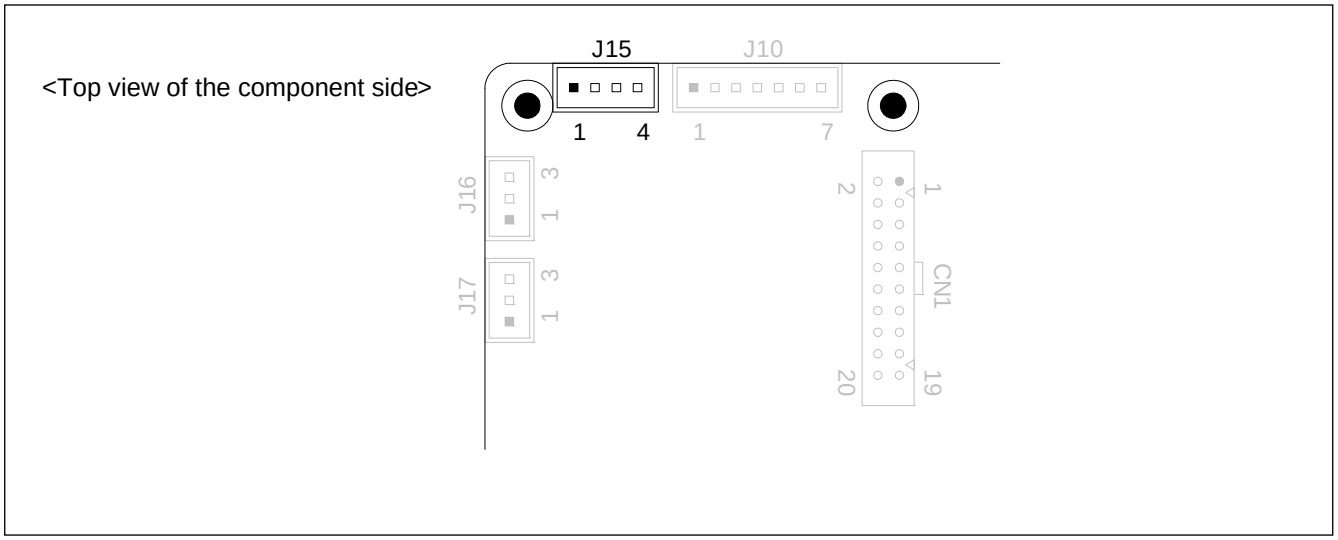


Figure 7.1.12 Diagram of IEBus™ Connector Pins (J13)

Table 7.1.18 Descriptions of IEBus™ Connector Pins (J13)

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V	2	BUS-
3	BUS+	4	GND

7.1.12 CAN Connectors (J14 and J15)

M3A-HS64G02 includes CAN connectors (J14 and J15). Only J15 can be used on the R0K572690C000BR.
Figure 7.1.13 shows the deployment of CAN connector pins. Table 7.1.19 lists their descriptions.

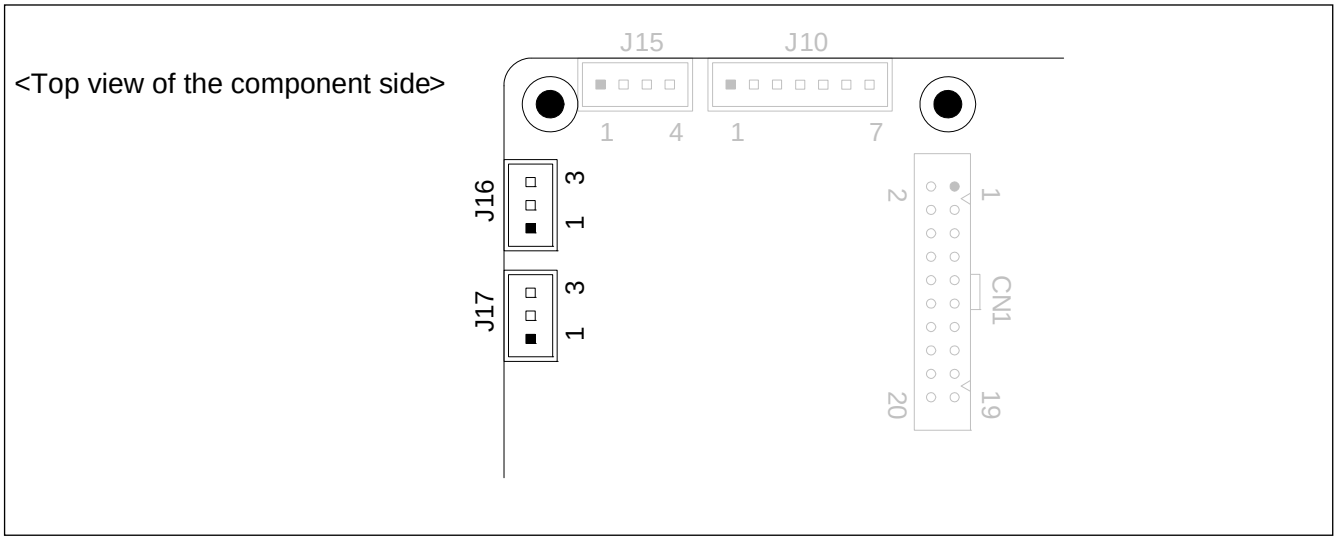


Figure 7.1.13 Diagram of CAN Connector (J14 and J15)

Table 7.1.19 Assignments of CAN Connector (J14 and J15)

Pin No.	Signal Name	Pin No.	Signal Name
1	CANH	2	CANL
3	GND	-	

Note: Channel 2 (CTx2/CRx2) is connected to J15.

7.1.13 MTU2 Connector (J16)

M3A-HS64G02 includes an MIL standard connector (J16) for MUT2 output.
Figure 7.1.14 shows the deployment of the MTU2 connector pins. Table 7.1.20 lists their descriptions.

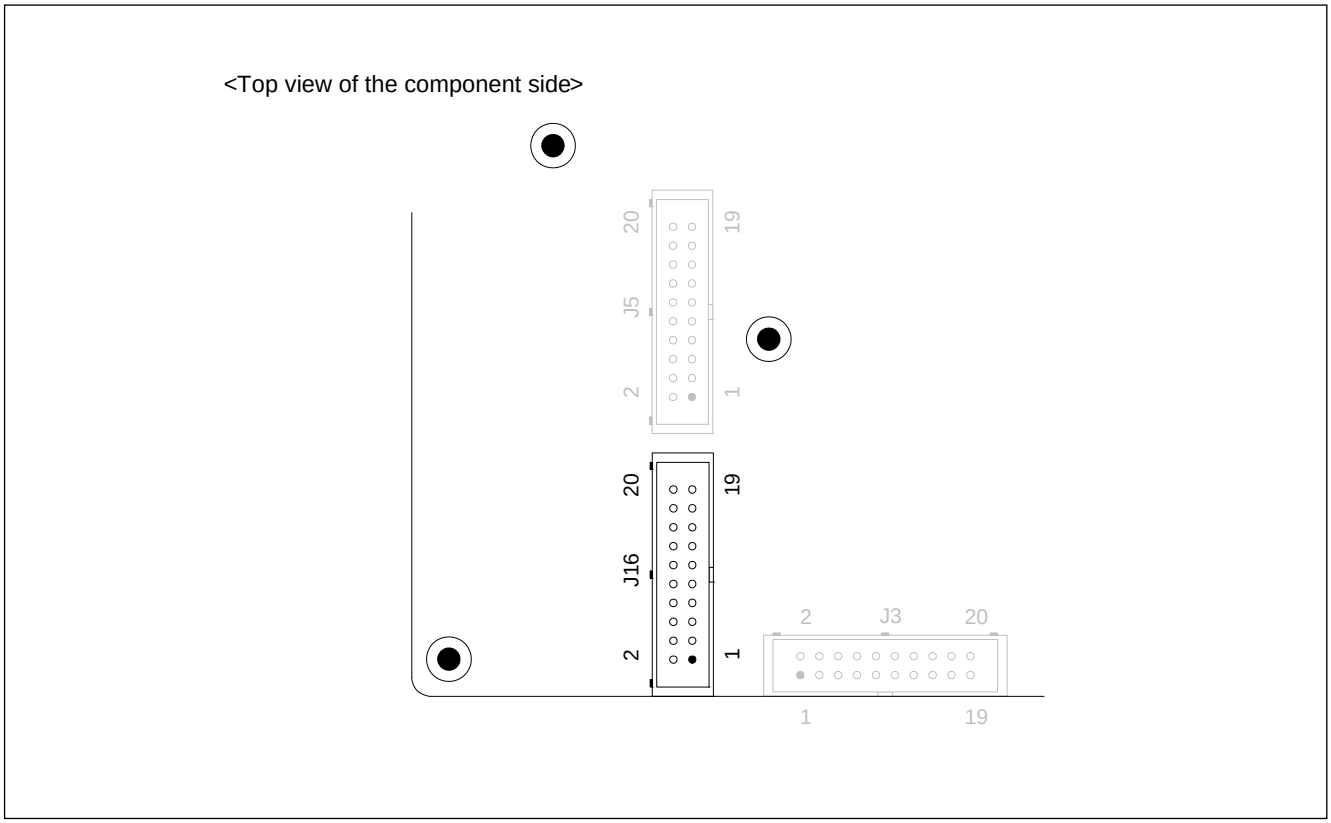


Figure 7.1.14 Diagram of MTU2 Connector Pins (J16)

Table 7.1.20 Descriptions of MTU2 Connector Pins (J16)

Pin No.	Signal Name	Pin No.	Signal Name
1	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / **TIOC4C** / TEND0 / SPBMO_1/SPBIO0_1	2	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / **TIOC4D** / AUDIO_XOUT / SPBMI_1/SPBIO1_1
3	GND	4	GND
5	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / PWM2E / SCK7	6	PJ27 / SGOUT_3 / **TIOC1A** / CTS7#
7	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / **TIOC4A** / DREQ0 / AUDCK	8	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / **TIOC4C** / TEND0 / SPBMO_1/SPBIO0_1
9	GND	10	GND
11	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / SCK5#	12	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / CTS5#
13	GND	14	GND
15	PC7 / CKE / RxD7 / CRx1 / CRx0/CRx1 / IRQ1	16	PC8 / CS3# / TxD7 / CTx1 / CTx0&CTx1
17	PC5 / RAS# / CRx0 / CRx0/CRx1/CRx2 / IRQ0	18	PC6 / CAS# / SCK7 / CTx0 / CTx0&CTx1&CTx2
19	PE6 / SCL3 / RxD6	20	PE7 / SDA3 / RxD7

Note: The signal names in bold style are setting functions.

7.1.14 12V Power Supply Connector (J17)

M3A-HS64G02 includes a system power supply connector (J17). To avoid the false insert, numbers of the pins are differed from other power connector on the CPU board.

Figure 7.1.15 shows the deployment of the power supply connector pins. Table 7.2.1 lists their descriptions.

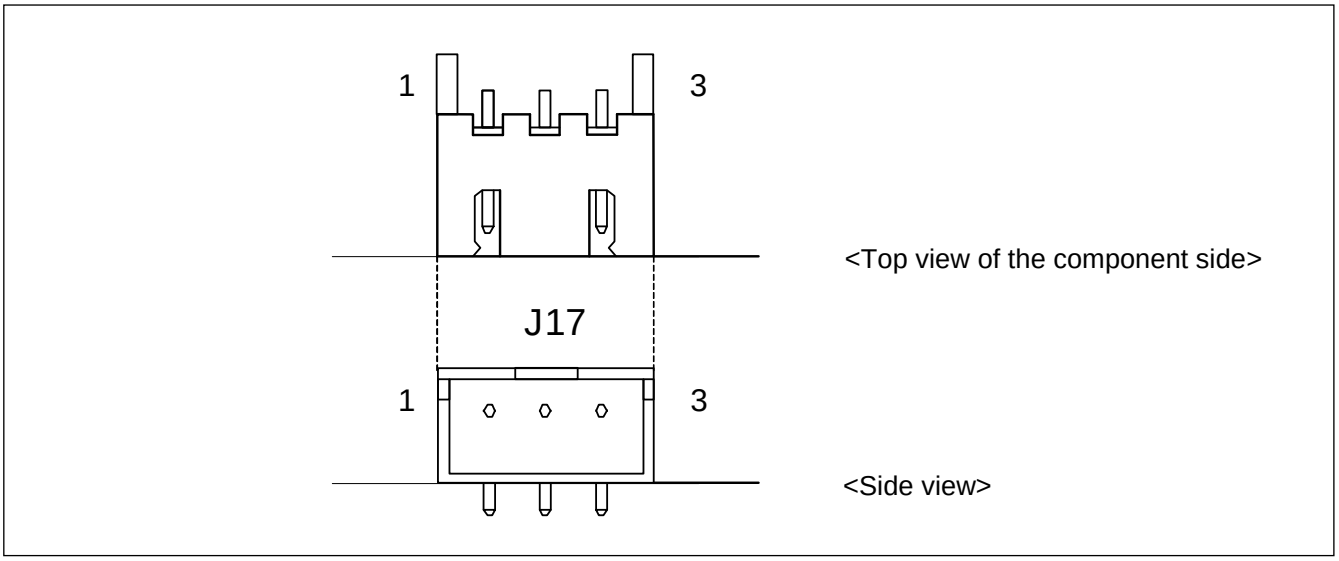


Figure 7.1.15 Diagram of 12V Power Supply Connector pins (J17)

Table 7.1.21 Descriptions of 12V Power Supply Connector Pins (J17)

Pin No.	Signal Name	Pin No.	Signal Name
1	+12V	2	NC
3	GND	-	

7.1.15 12V Input AC Adapter Jack（J18）

M3A-HS64G02 includes adapter jack (J18) for DC12V input.
Figure 7.1.16 shows 12V input AC adapter jack pins. Table 7.1.22 lists their descriptions.

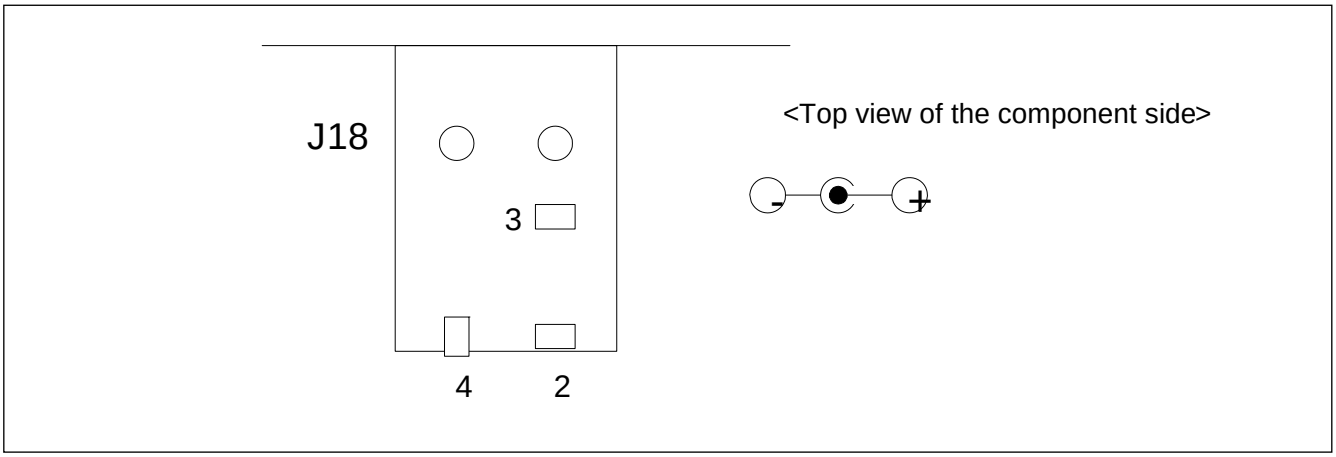


Figure 7.1.16 Diagram of 12V AC Adapter Jack Pins (J18)

Table 7.1.22 Descriptions of 12V AC Adapter Jack Pins (J18)

Pin No.	Signal Name	Pin No.	Signal Name
1	NC（without a terminal）	2	+12V
3	GND	4	GND

7.2 M3A-HS64G02 Operation Parts Layout

Figure 7.2.1 shows the layout of operation parts on M3A-HS64G02.

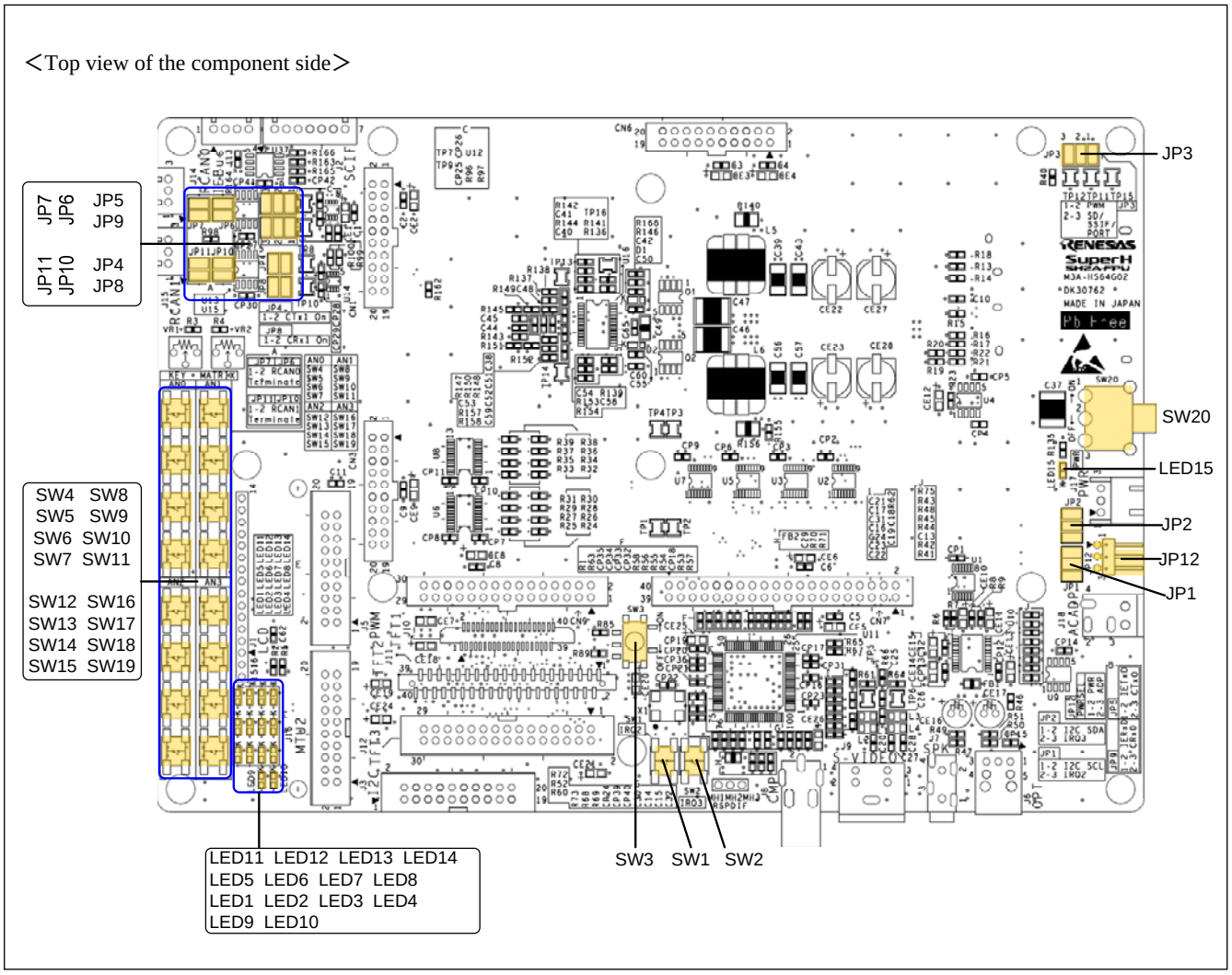


Figure 7.2.1 M3A-HS64G02 Operation Parts Layout

7.2.1 Jumper（JP1 to JP12）

M3A-HS64G02 includes twelve jumpers.

Figure 7.2.2 shows the deployment of the jumpers (JP1 to JP12). Table 7.2.1 to Table 7.2.3 list their settings.

Figure 7.2.2 Diagram of Jumper on M3A-HS64G02 (JP1 to JP12)

Table 7.2.1 List of Jumper Settings to Switch Multifunctional Terminal (JP1 to JP3, JP5, and JP9)

Jumper No.	Setting	Function
JP1	1－2	Connects to D/A converter device (U10) as an SCL1 output terminal.
SCL1/PE2	2－3	Connects t o a push switch (SW1) as a PE2 input terminal.
JP2	1－2	Connects to D/A converter device (U10) as an SDA1 input-output terminal.
SDA1/PE3	2－3	Connects t o a push switch (SW2) as a PE3 input terminal.
JP3	1－2	Connects to MIL standard connector (J5) as a PWM data output terminal.
PWM/ （SD/SSIF/PORT）	2－3	Connects to SD card slot (J4), D/A converter (U10), test terminal (TP1 – TP4) as input terminals, SDHI, SSIF, and PORT.
JP5	1－2	Connects to IEBus™ driver (U37) as an IETxD output terminal.
IETxD/PJ30	2－3	Invalid on R0K572690C000BR
JP9	1－2	Connects to an IEBus™ driver (U37) as an IETxD input terminal.
IERxD/PJ29	2－3	Invalid on R0K572690C000BR

: setting by default

Note: The jumper settings shall not changed under operation of this evaluation board. Make sure to use it with the power turned off.

Table 7.2.2 List of Jumper Settings for CAN Evaluation (JP4, JP6 to JP8, JP10, and JP11)

Jumper No.	Setting	Function
JP4 CTx2 connection	1−2	Connect CTx2 terminal to CAN driver（U16）
	None（open）	Not connect CTx2 terminal to CAN driver （U16）
JP8 CRx2 connection	1−2	Connect CRx2 terminal to CAN driver（U16）
	None（open）	Not connect CRx2 terminal to CAN driver （U16）
JP6 CANL（ch0）end	1−2	Terminate CANL（ch0）
	None（open）	Not terminate CANL（ch0）
JP7 CANH（ch0）end	1−2	Terminate CANH（ch0）
	None（open）	Not terminate CANH（ch0）
JP10 CANL（ch1）end	1−2	Terminate CANL（ch1）
	None（open）	Not terminate CANL（ch1）
JP11 CANH（ch1）end	1−2	Terminate CANH（ch1）
	None（open）	Not terminate CANH（ch1）

: setting by default

Note: The jumper settings shall not changed under operation of this evaluation board. Make sure to use it with the power turned off.

Table 7.2.3 List of Jumper Settings for Switching System Power (JP12)

Jumper No.	Setting	Function
JP12 PWRSEL	1−2	Supply system power from J17.
	2−3	Supply system power from J18 with an AC adapter

: setting by default

Note: The jumper settings shall not changed under operation of this evaluation board. Make sure to use it with the power turned off.

7.2.2 Switches and LEDs

M3A-HS64G02 includes twenty switches and fifteen LEDs.

Figure 7.2.3 shows the deployments of switches and the LEDs. Table 7.2.4 lists the switches and Table 7.2.5 lists LEDs.

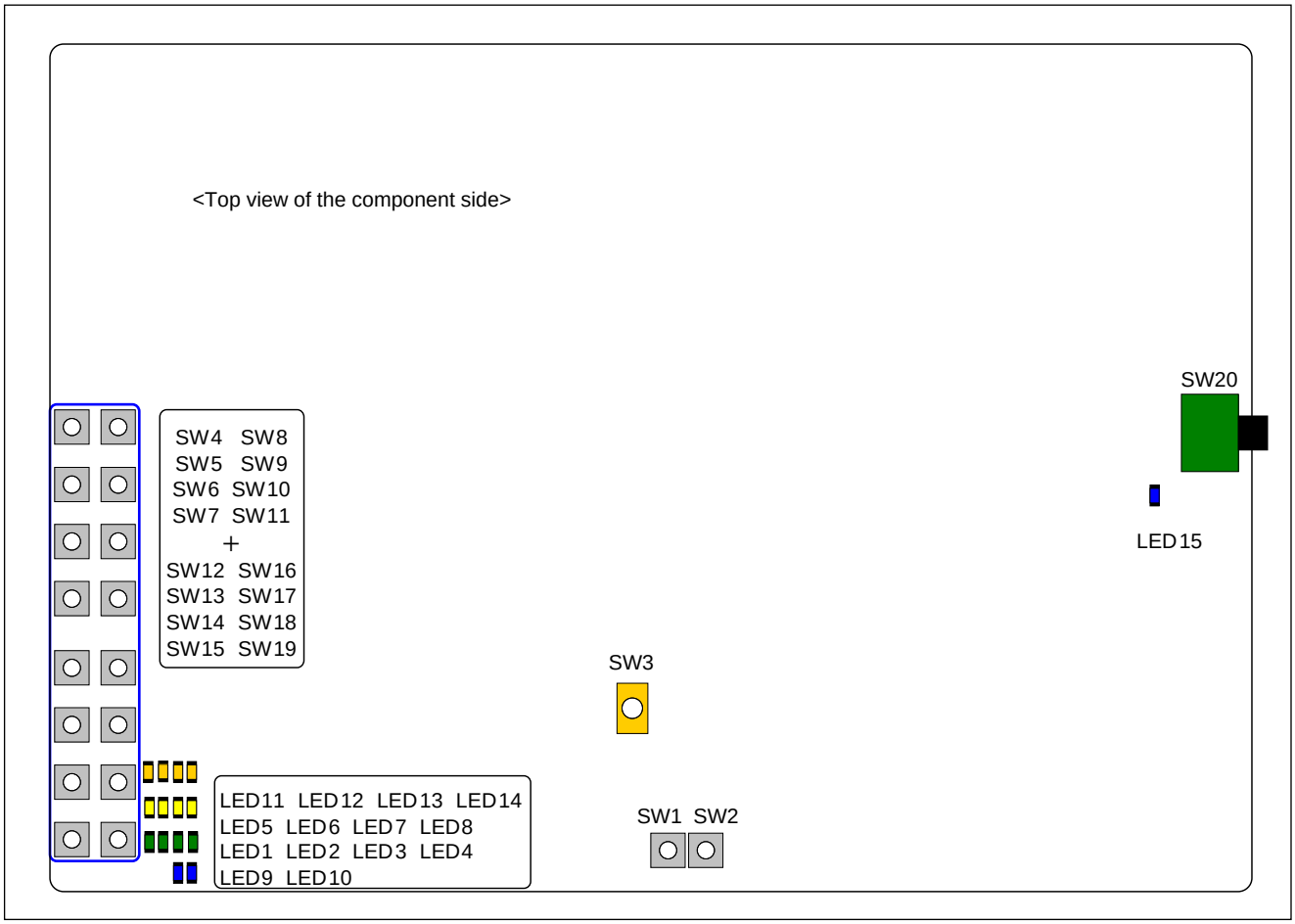


Figure 7.2.3 Diagram of Switches and LEDs on M3A-HS64G02

Table 7.2.4 List of switches on M3A-HS64G02

No.	Function	Notes
SW1	IRQ2 switch	For details, refer to Chapter 4.13
SW2	IRQ3 switch	For details, refer to Chapter 4.13
SW3	Power switch for LCD module connector（J10）	Not populated
SW4-19	Key input switch	For details, refer to Chapter 4.12
SW20	Power switch	–

Table 7.2.5 List of LEDs on M3A-HS64G02

No.	Color	Function
LED1-4	green	Refer to Chapter 4.11 for dimmer LED (MTU2 output pin is connected to TIOC4A, TIOC4C, TIOC1A).
LED5-8	Yellow	Refer to Chapter 4.11 for dimmer LED (invalid on R0K572690C000BR)
LED9-10	Blue	Refer to Chapter 4.11 for dimmer LED (MTU2 output pin is connected to TIOC4C, 4D)
LED11-14	Orange	Refer to Chapter 4.11 for dimmer LED (invalid on R0K572690C000BR)
LED15	blue	Power supply LED (light –up when 12V power is supplied.)

7.3 M3A-HS64G02 Dimensions

Figure 7.3.1 shows the dimensions of M3A-HS64G02 on the top of the component side. Figure 7.3.2 shows its dimensions as a perspective view.

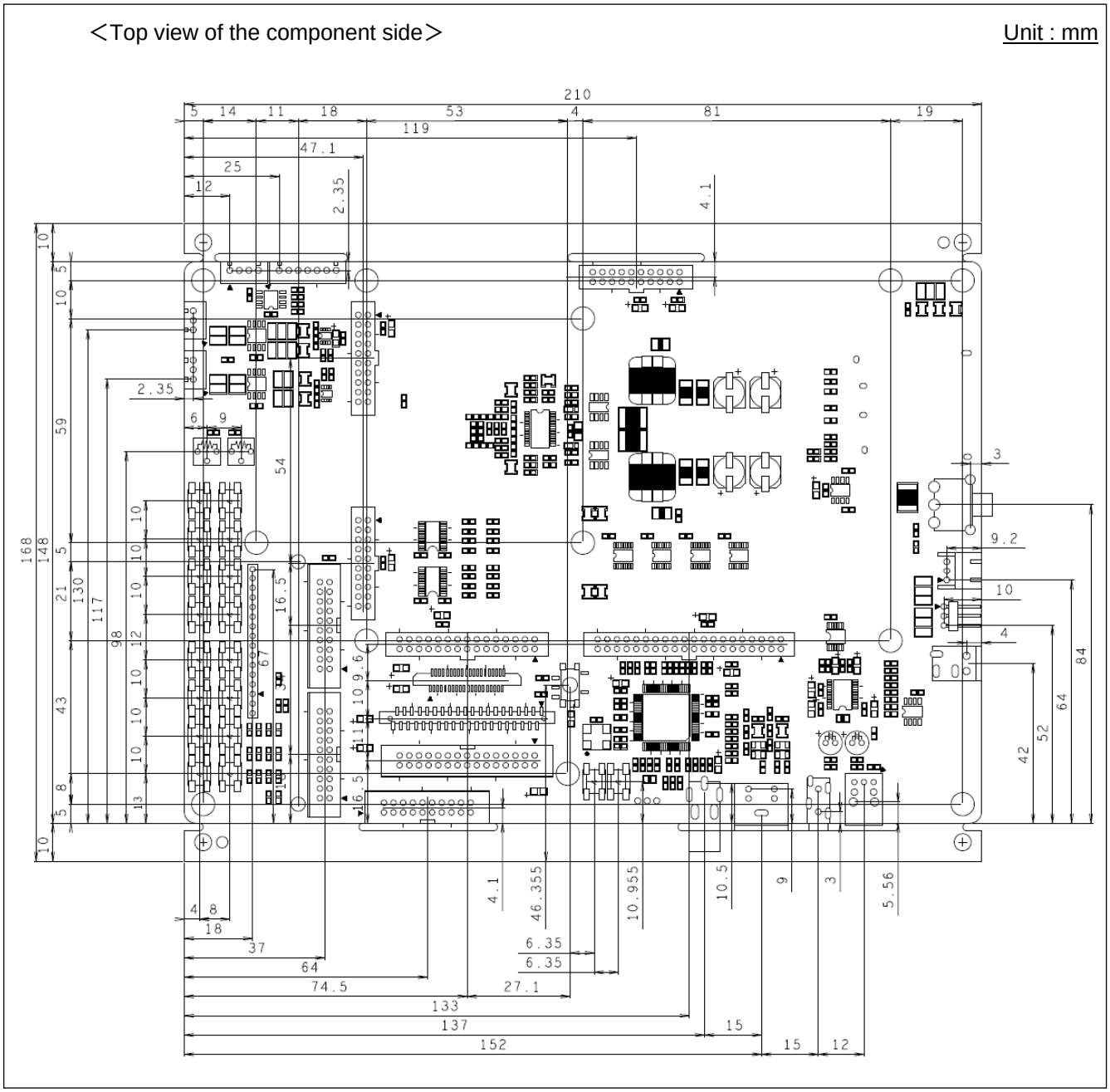


Figure 7.3.1 M3A-HS64G02 Dimensions

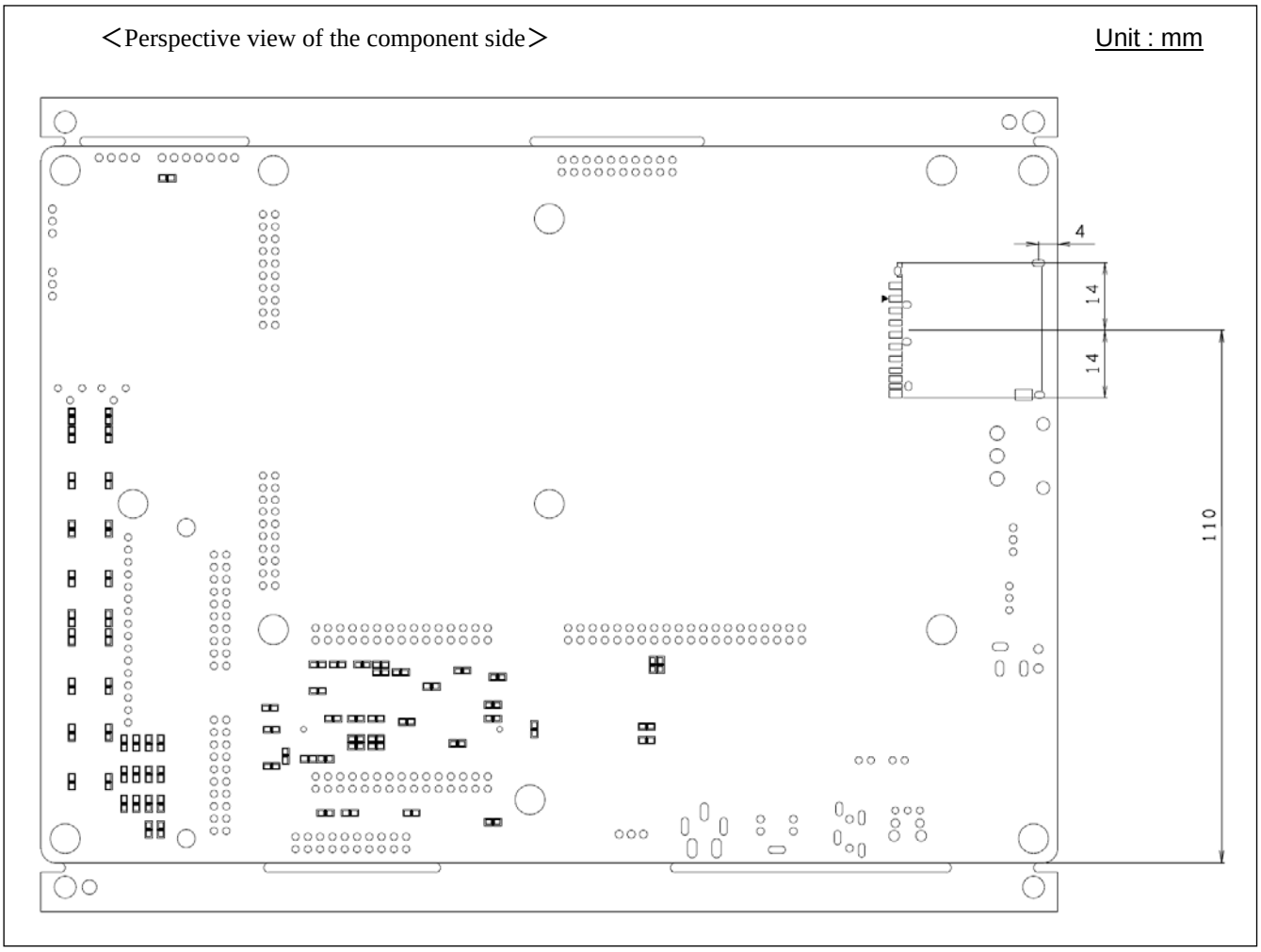


Figure 7.3.2 M3A-HS64G02 Dimensions

Appendix R0K572690C000BR Schematics

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SH7269 CPU board R0K572690C000BR SCHEMATICS

Note:

Digital GND (GND)

Analog GND (AVss)

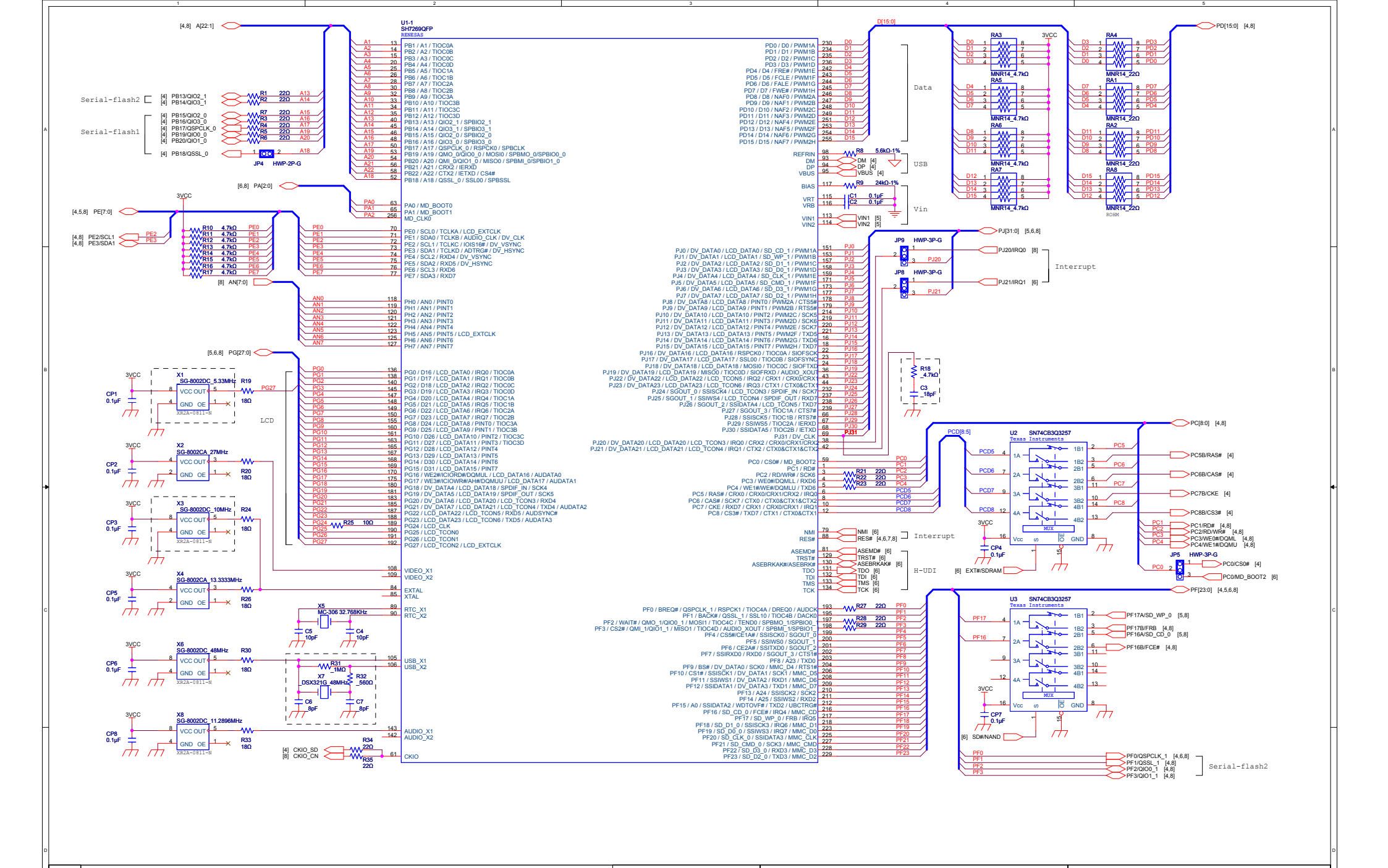
USB Analog GND (USB_AVSS)

Not mounted

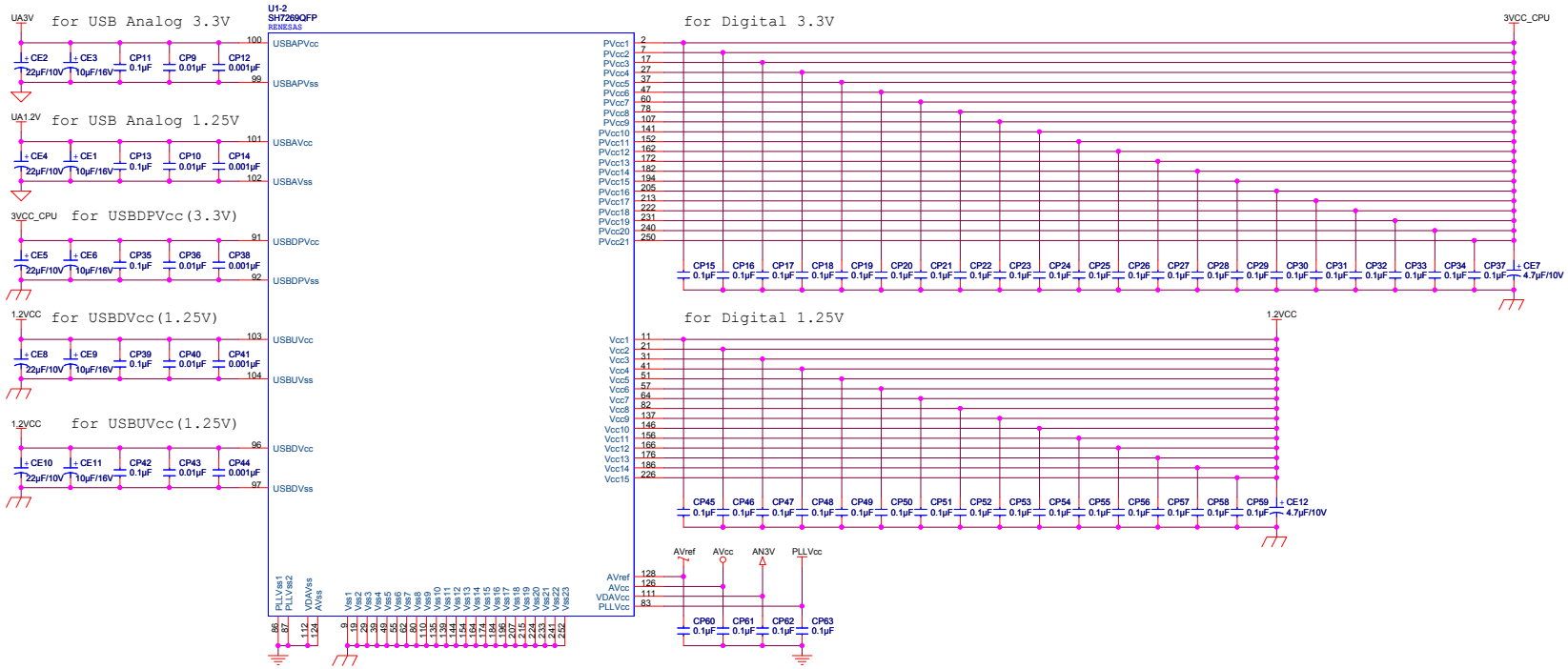
5VCC = Digital 5V
3VCC = Digital 3.3V
3VCC_CPU = 3.3V for CPU I/O
1.2VCC = 1.25V for CPU Core
PLLVcc = Analog 3.3V for PLL
UA3V = Analog 3.3V for USB
UA1.2V = Analog 1.25V for USB
AVcc = Analog 3.3V
AVref = 3.3V for ADC Voltage Reference
AN3V = Analog 3.3V for Video

R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

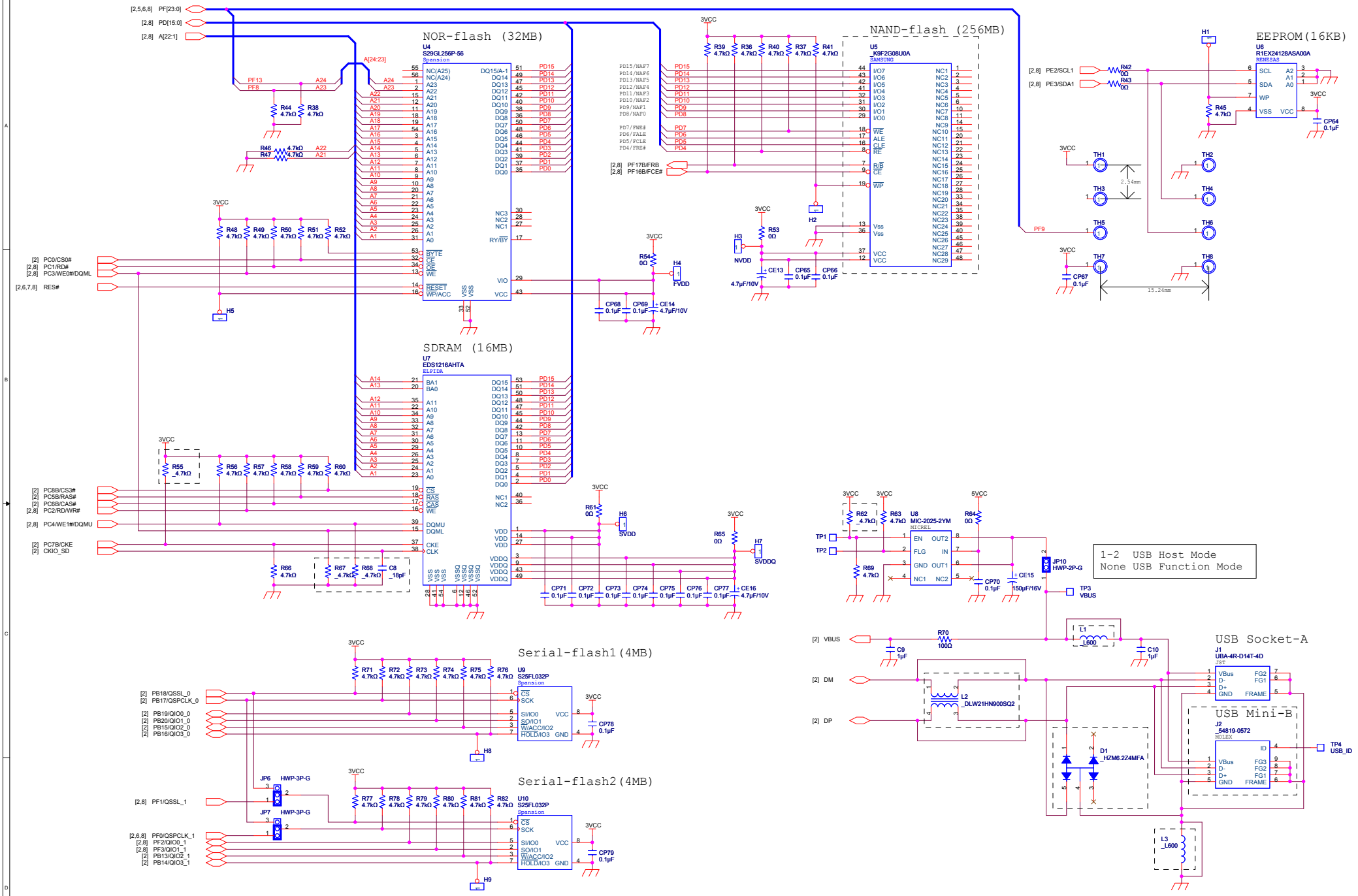
CHANGE		SCALE		Renesas Solutions Corp.				R0K572690C000BR INDEX (1 / 8)
				DRAWN	CHECKED	DESIGNED	APPROVED	
		DATE	11-08-29					D-R0K572690C000BR_C-A



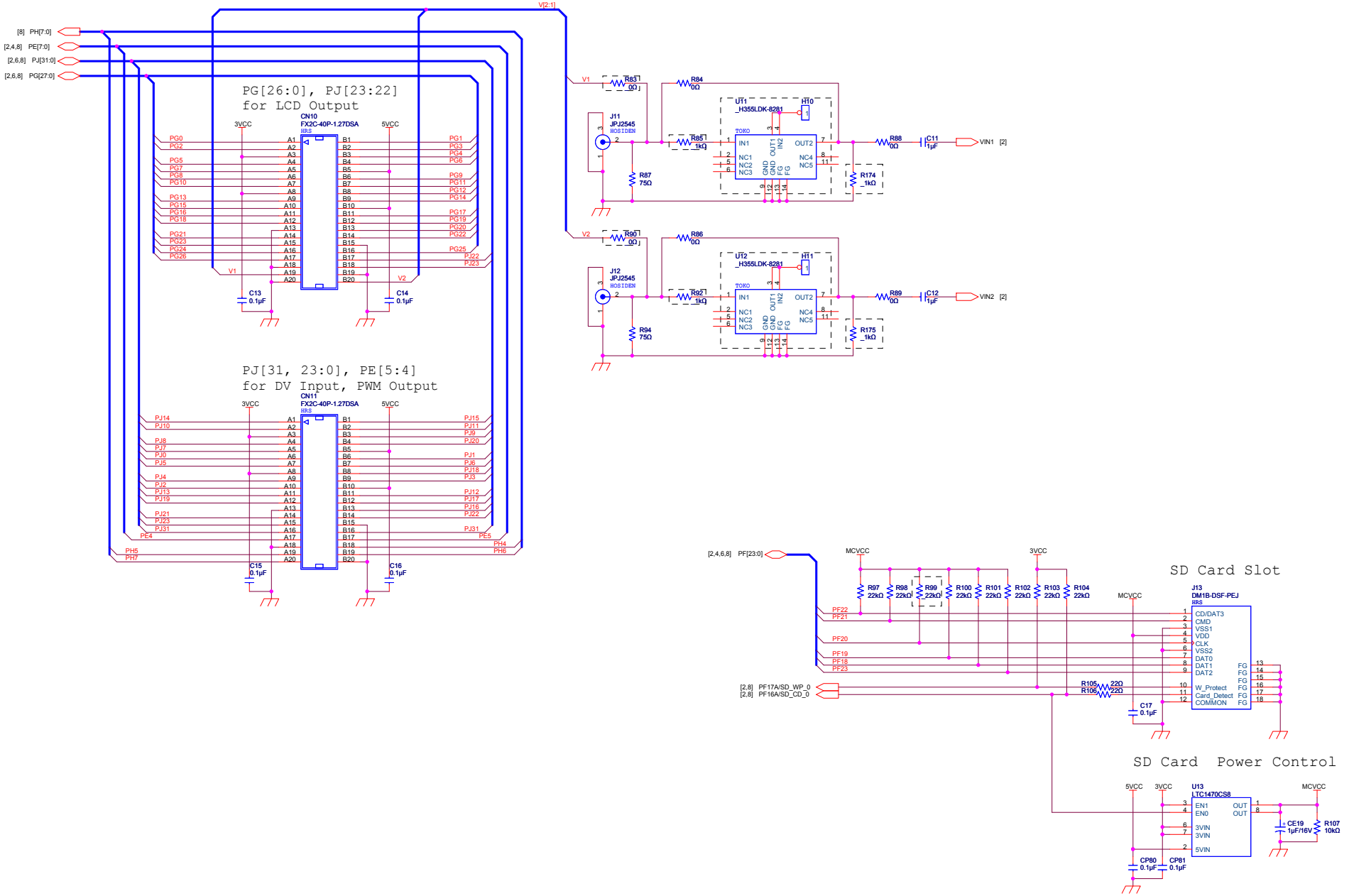
CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		CPU(SH7269), Clock (2 / 8)
		SCALE			
		DATE	11-08-29		D-R0K572690C000BR_C-A



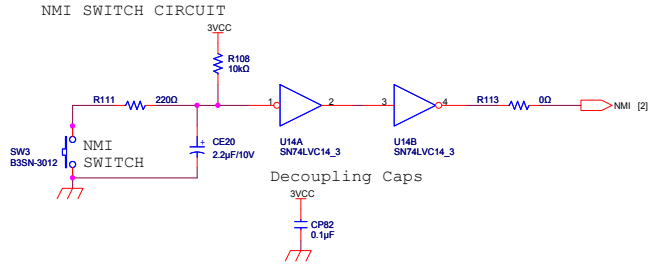
CHANGE						
			Renesas Solutions Corp.			R0K572690C000BR
			DRAWN	CHECKED	DESIGNED	APPROVED
		SCALE				CPU(SH7269)-power (3 / 8)
		DATE	11-08-29			D-R0K572690C000BR_C-A

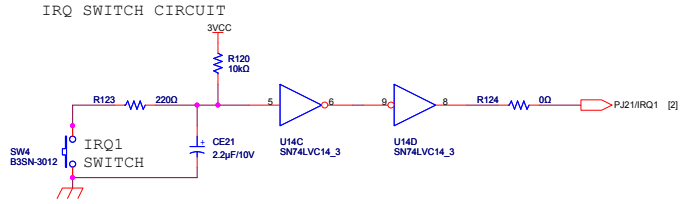


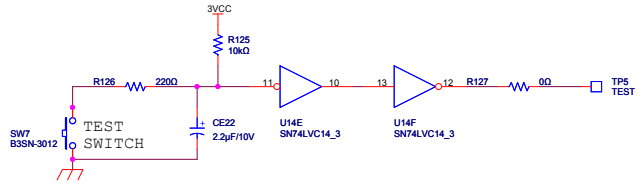
CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Memory, USB (4 / 8)
		SCALE			D-R0K572690C000BR_C-A
		DATE	11-08-29		

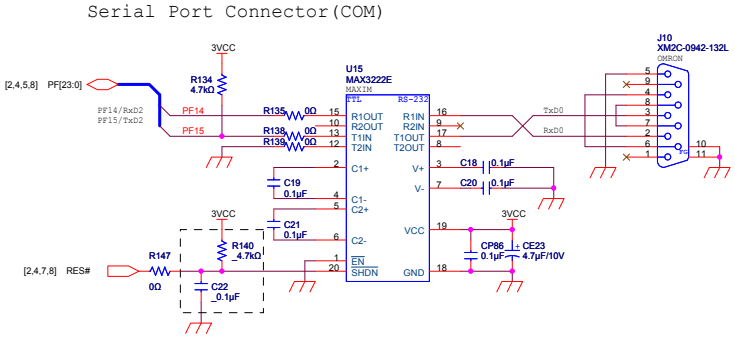


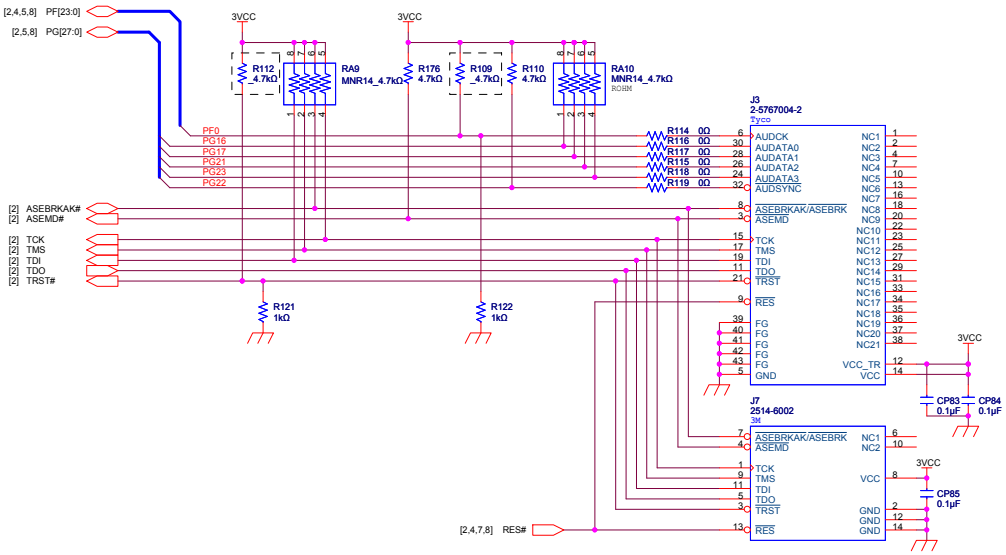
CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN	CHECKED / DESIGNED / APPROVED	VDC4, Vin, SD
		SCALE			(5 / 8)
		DATE	11-08-29		D-R0K572690C000BR_C-A

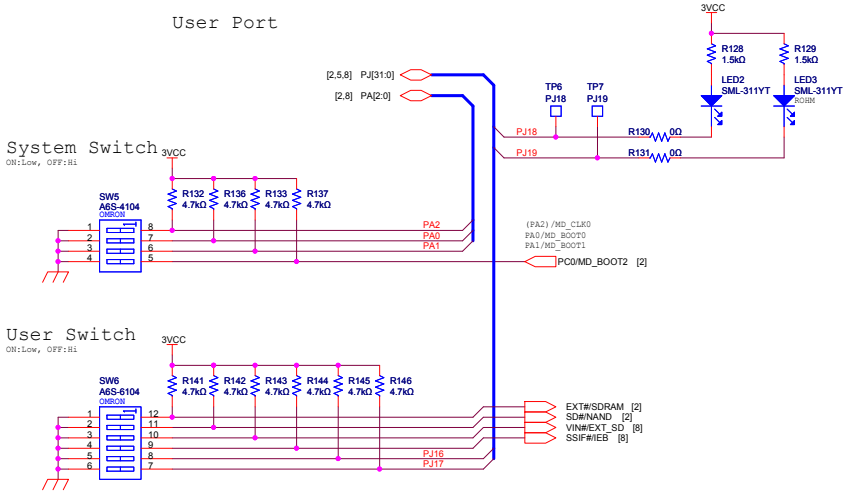




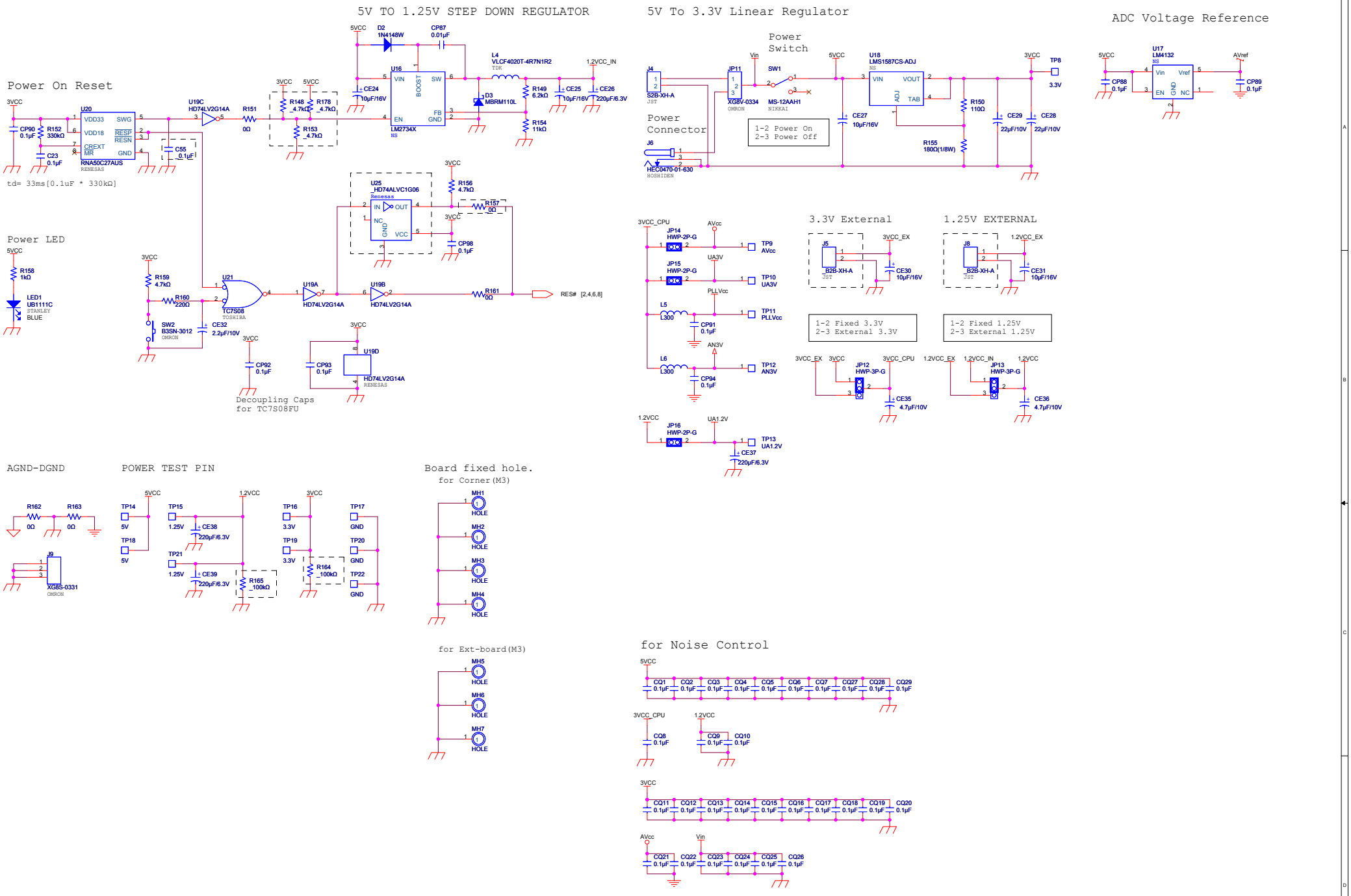




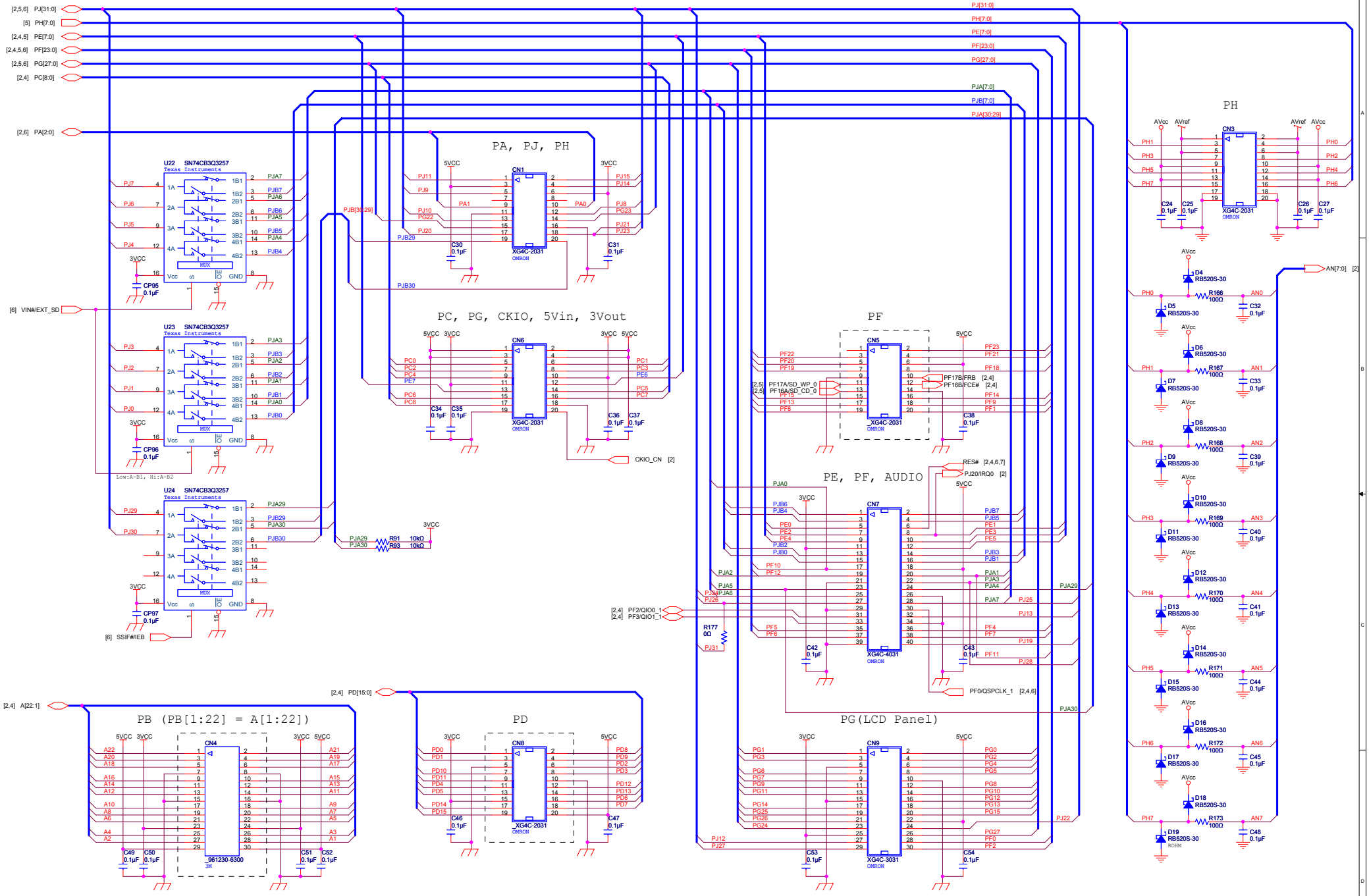




CHANGE			Renesas Solutions Corp.			R0K572690C000BR
			DRAWN	CHECKED	DESIGNED	APPROVED
		SCALE				Switch, RS-232C, H-UDI, UserI/F (6 / 8)
		DATE	11-08-29			D-R0K572690C000BR_C-A



CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Reset, Power (7 / 8)
	SCALE				
	DATE	11-08-29			D-R0K572690C000BR_C-A



CHANGE		SCALE		Renesas Solutions Corp.				R0K572690C000BR
		DATE	11-08-29	DRAWN	CHECKED	DESIGNED	APPROVED	Ext. Connector, AD Protection (8 / 8)
								D-R0K572690C000BR_C-A

SH7264/62 Optional board M3A-HS64G01 SCHEMATICS

Note:

Digital GND (GND)

Analog GND (AVSS)

Analog GND (AGND)

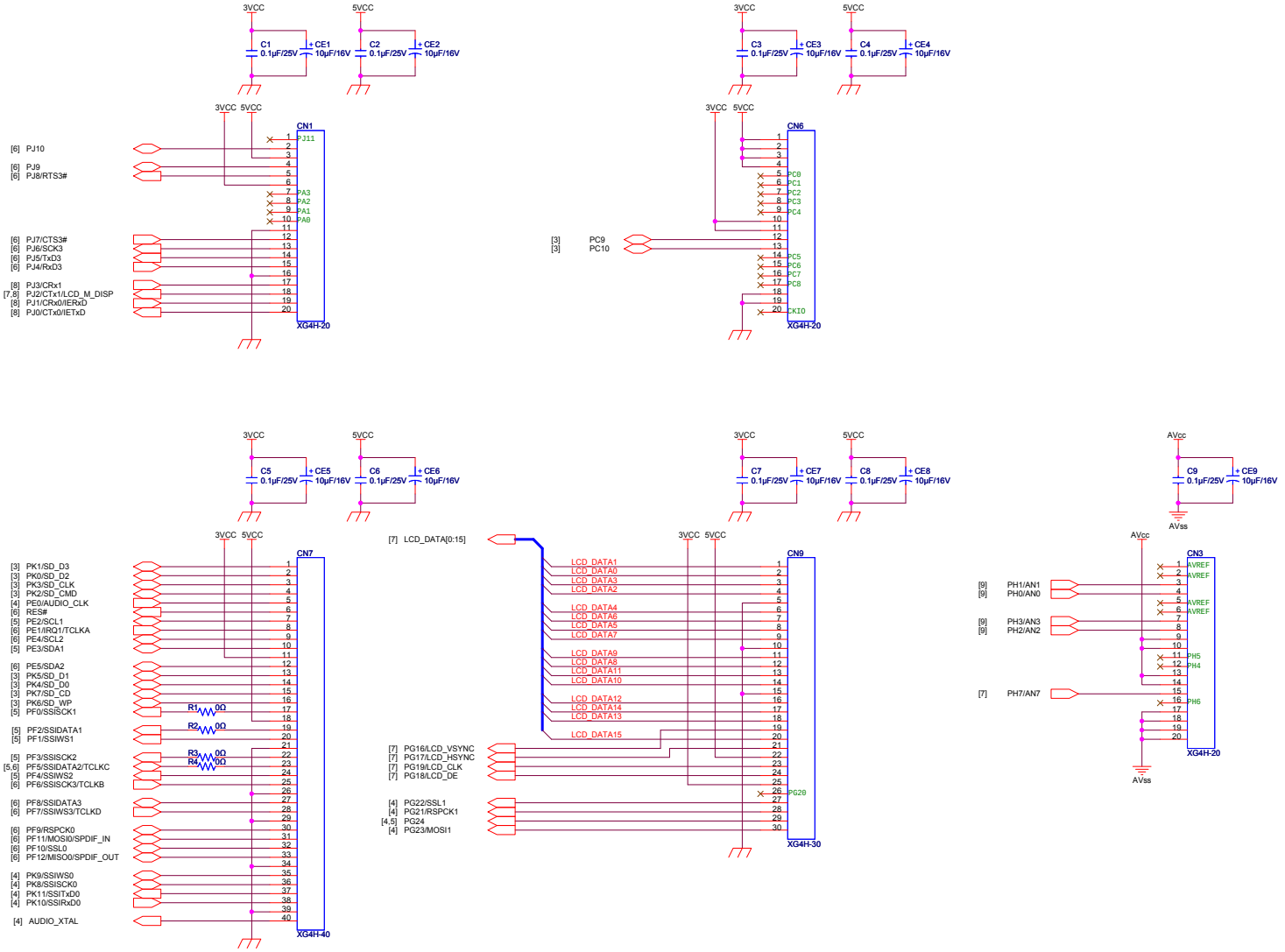
Not mounted

12VCC = Digital 12V Power in
8VCC = Digital 8V for CD
5VCC = Digital 5V
5AVCC = Analog 5V for Audio CODEC
3VCC = Digital 3.3V
3AVCC = Analog 3.3V for Audio DAC
AVcc = Analog 3.3V for Key Input
MCVCC = Digital 3.3V / 5V for SD

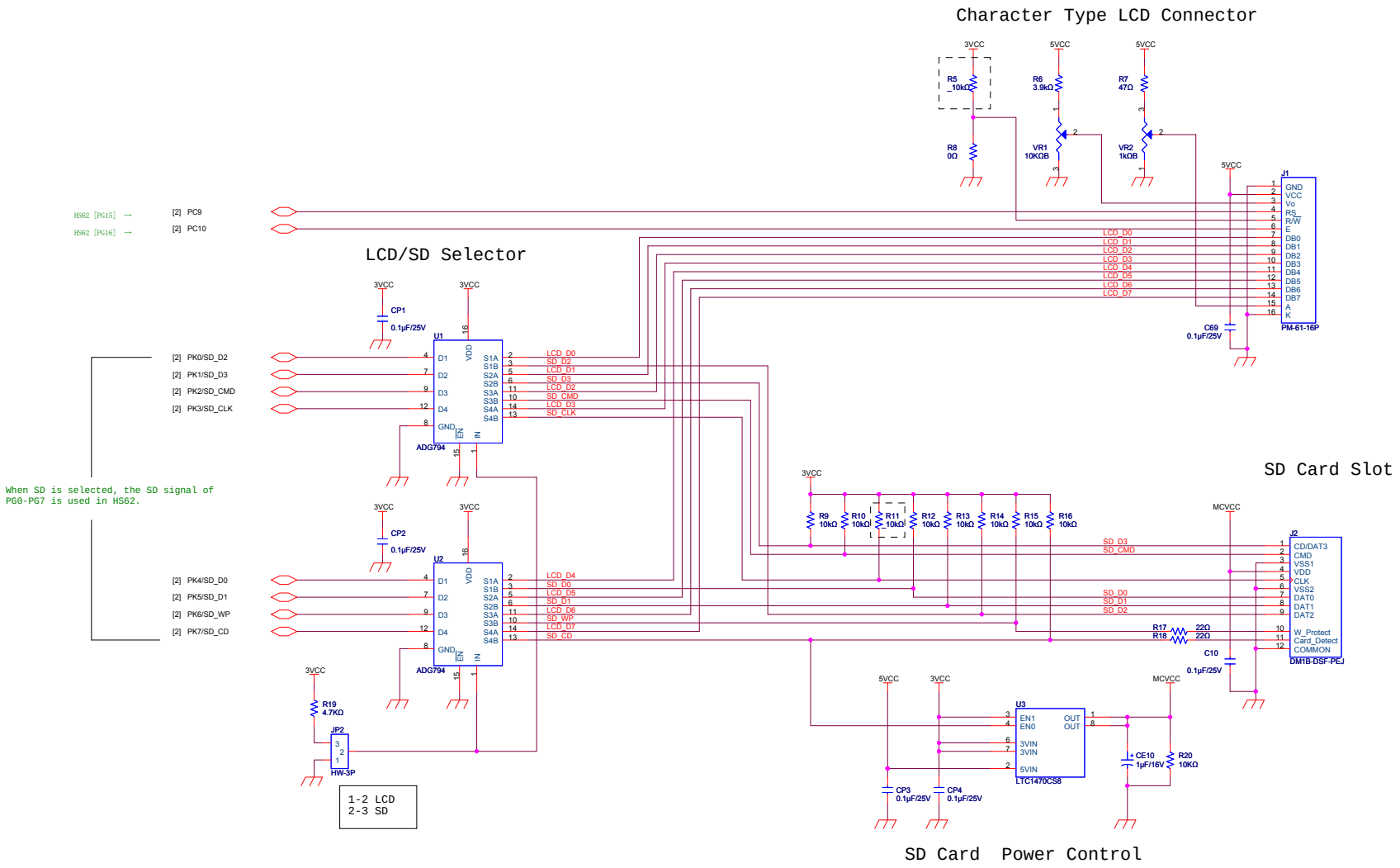
R = Fixed Resistors
C = Ceramic Caps
CP = Decoupling Caps
CE = Electrolytic Caps (Tantal / Electric)

CHANGE						
Ver. 1.00B	SCALE		Renesas Solutions Corp.			M3A-HS64G01
	DATE	09-03-02	DRAWN / CHECKED / DESIGNED / APPROVED			INDEX (1 / 10)
						DK30759

M3A-HS64/HS62 CPU Board Stack Connector

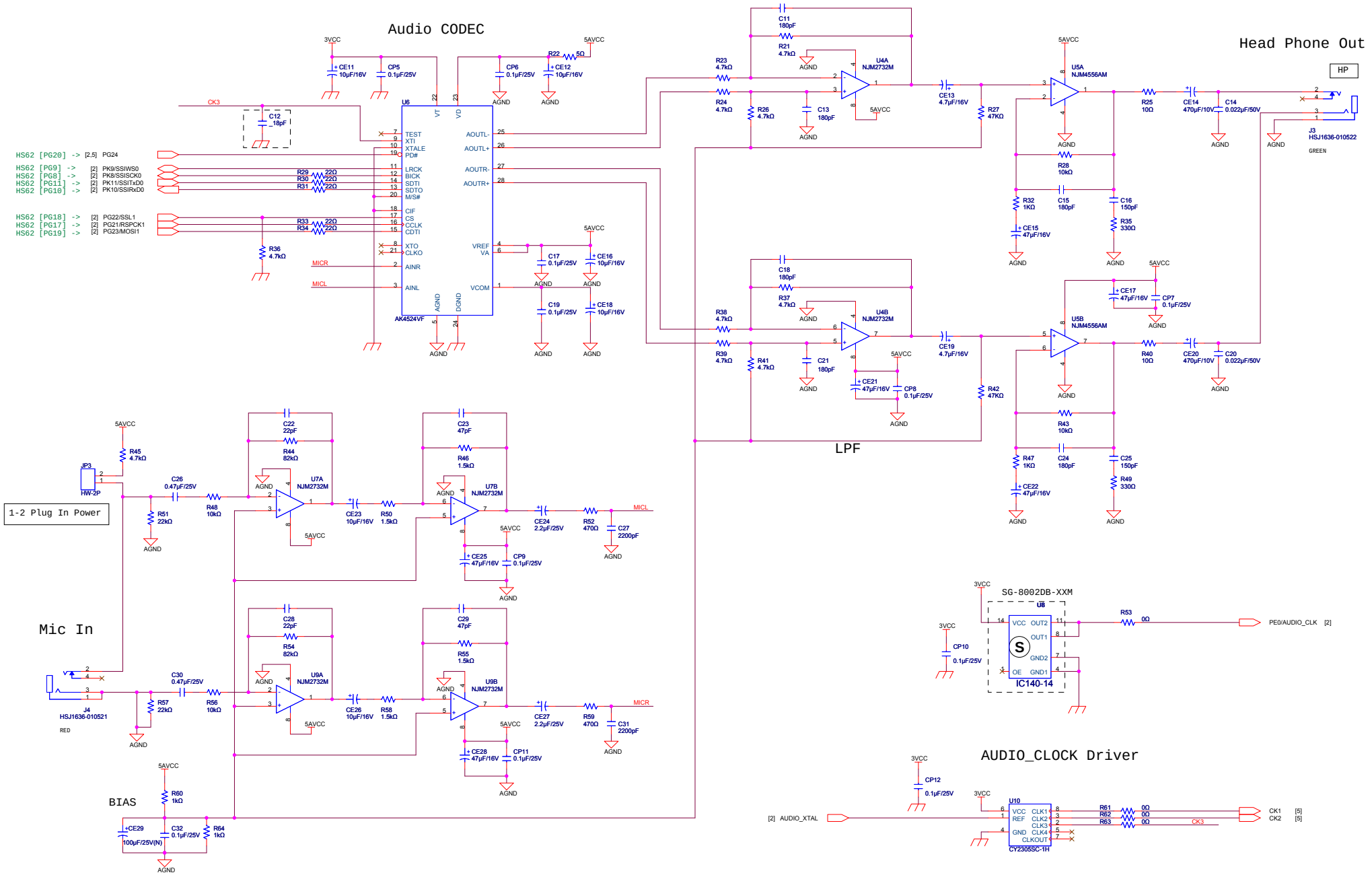


CHANGE			Renesas Solutions Corp.				M3A-HS64G01
			DRAWN	CHECKED	DESIGNED	APPROVED	CPU Board Stack Connector (2 / 10)
Ver. 1.00B		SCALE					DK30759
		DATE	09-03-02				



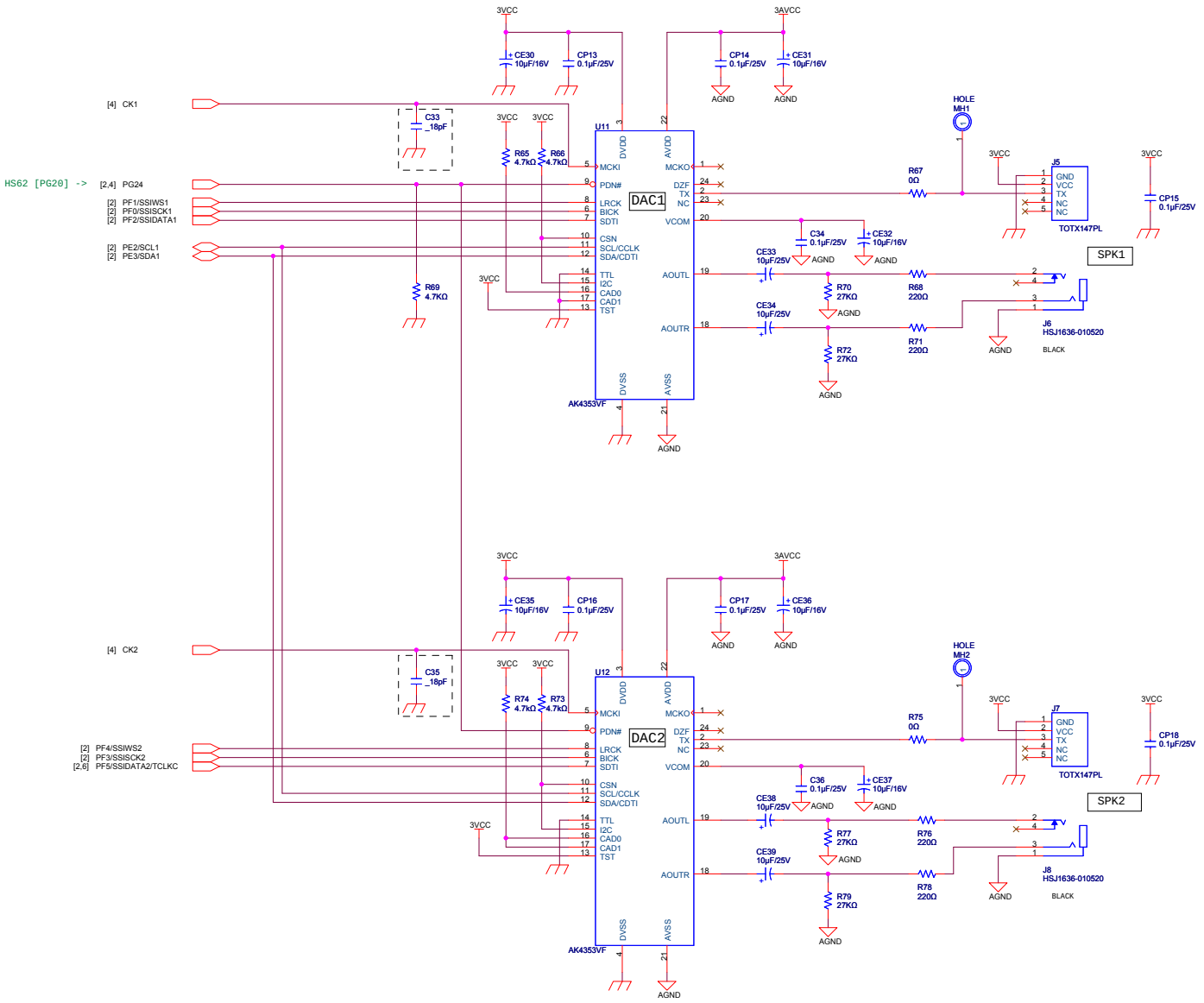
CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Character LCD/SD Card Slot (3 / 10)
Ver. 1.00B		SCALE			DK30759
		DATE	09-03-02		

Audio Interface



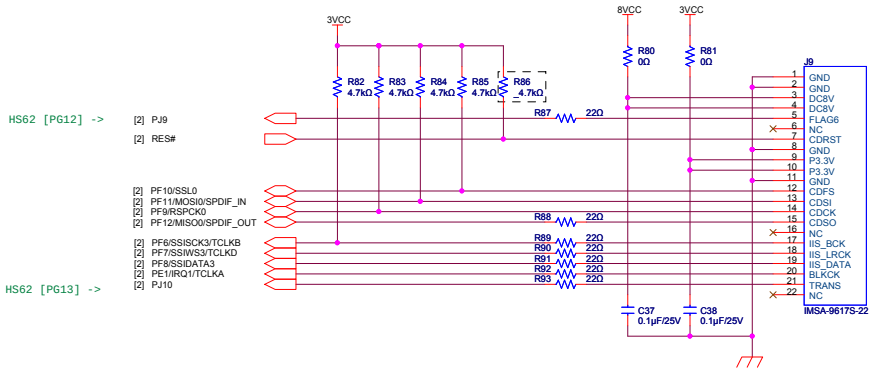
CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Audio CODEC (4 / 10)
Ver. 1.00B		SCALE			DK30759
		DATE	09-03-02		

Audio DAC

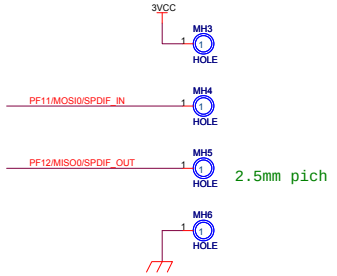


CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Audio D/A Converter (5 / 10)
Ver. 1.00B		SCALE			DK30759
		DATE	09-03-02		

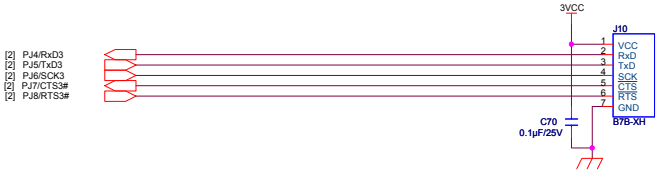
CD deck Interface



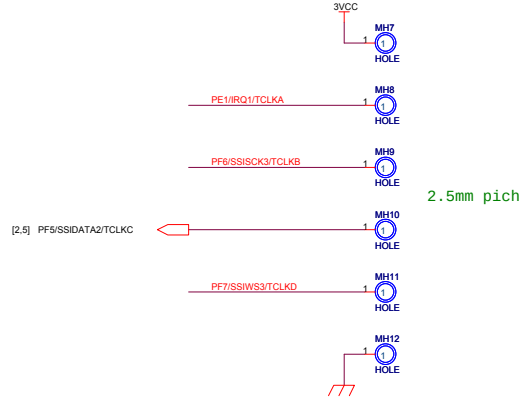
RSPDIF Through Hole.



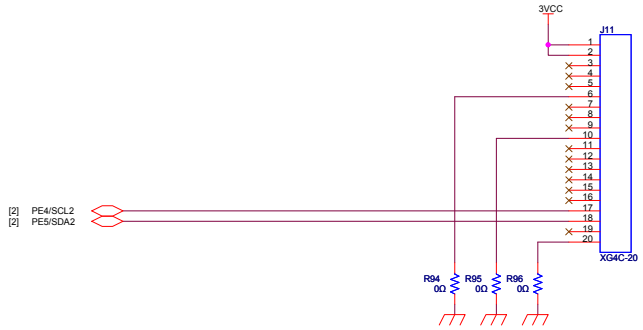
UART Interface



Rotary Encoder Through Hole.

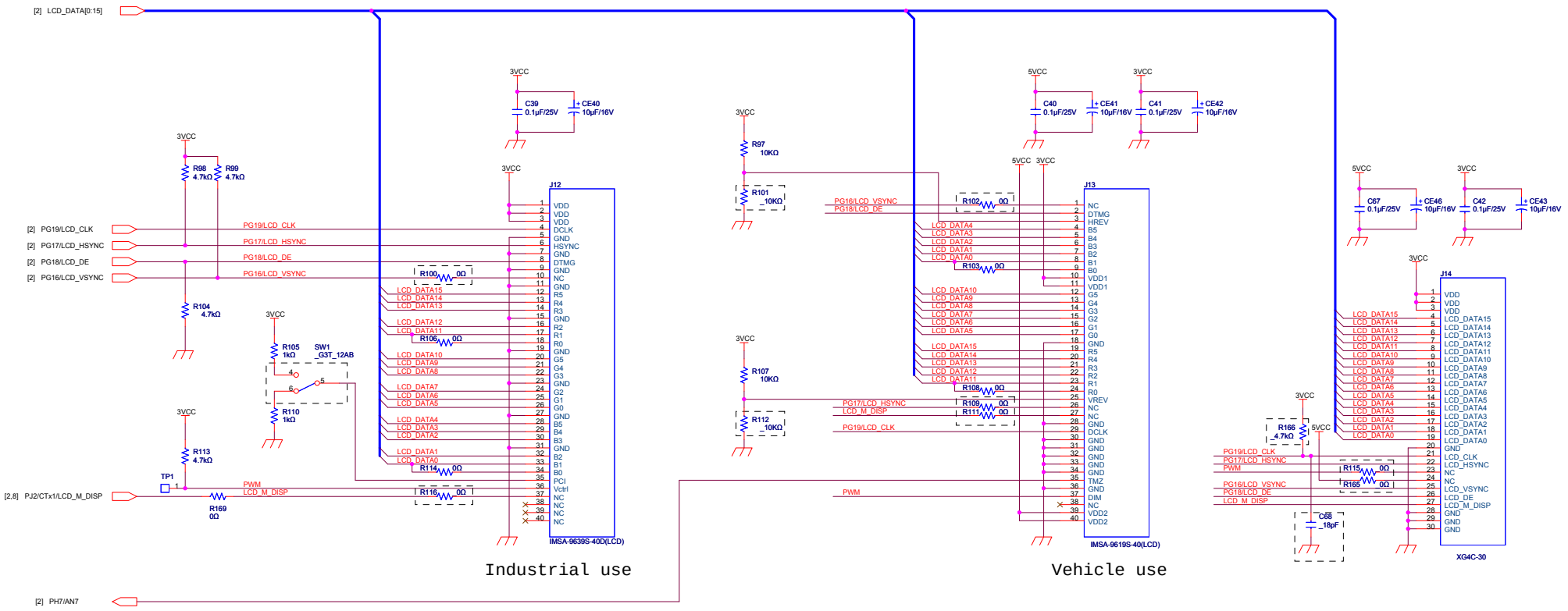


IIC Interface

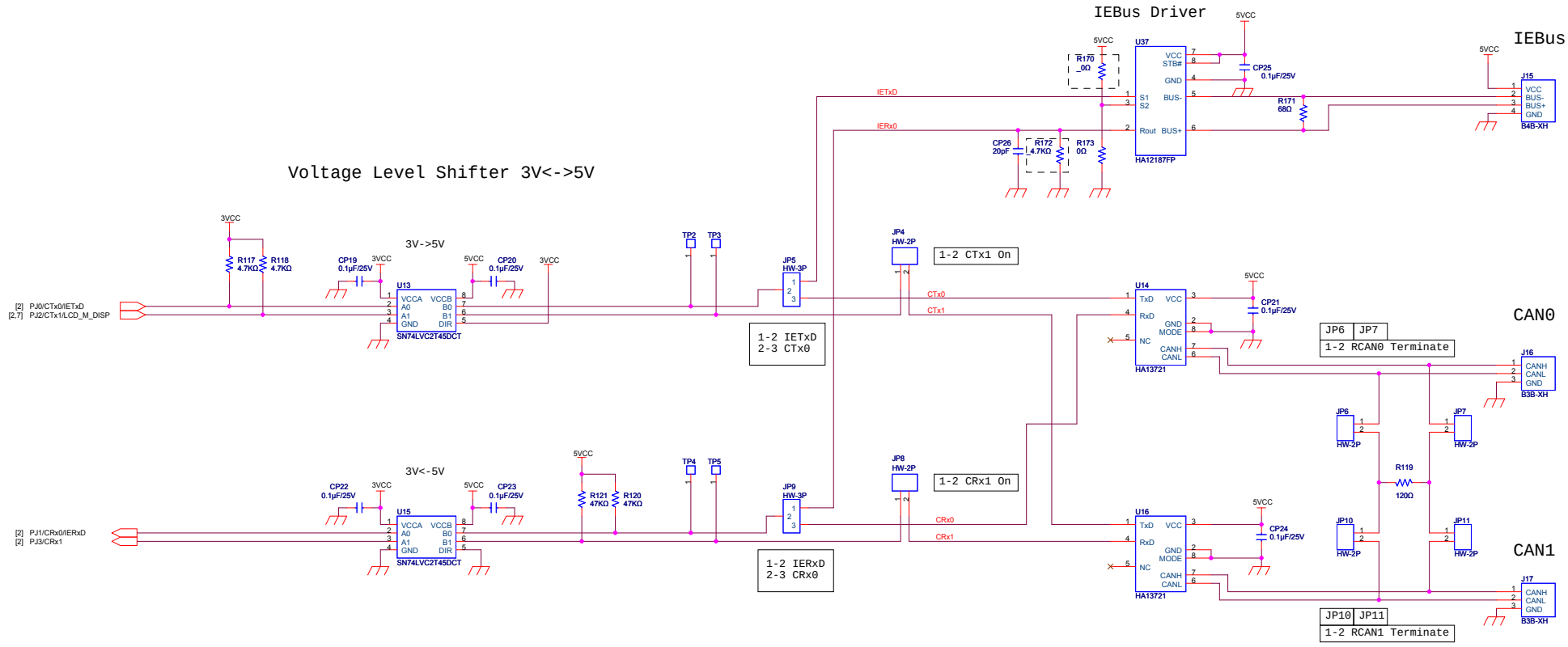


CHANGE						
Ver. 1.00B		Renesas Solutions Corp.				M3A-HS64G01
		DRAWN	CHECKED	DESIGNED	APPROVED	CD/UART/IIC/RSPDIF/Rotary Enc. (6 / 10)
	SCALE					
	DATE 09-03-02					DK30759

TFT LCD Module Interface

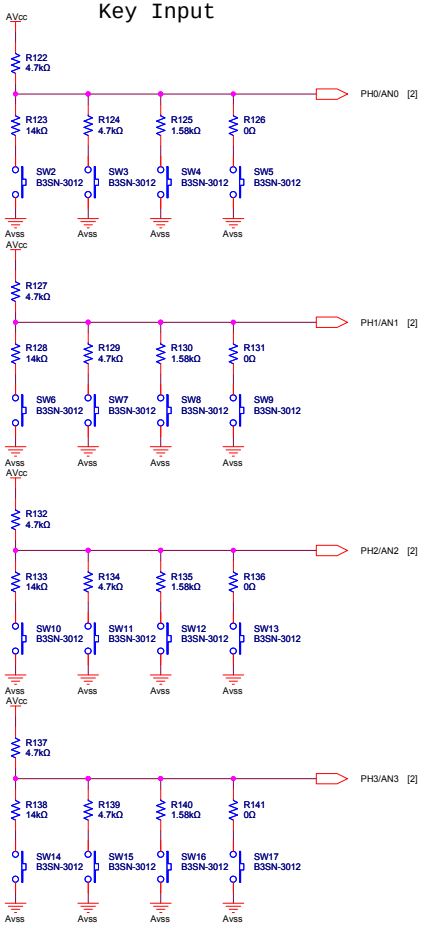


CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		LCD Module Connector (7 / 10)
Ver. 1.00B		SCALE			DK30759
		DATE	09-03-02		

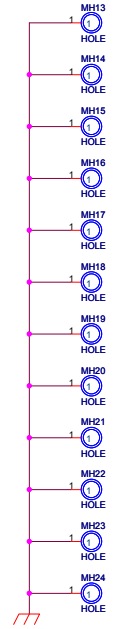


CHANGE					Renesas Solutions Corp.				M3A-HS64G01	
					DRAWN	CHECKED	DESIGNED	APPROVED	CAN/IEBus	(8 / 10)
	Ver. 1.00B	SCALE							DK30759	
		DATE	09-03-02							

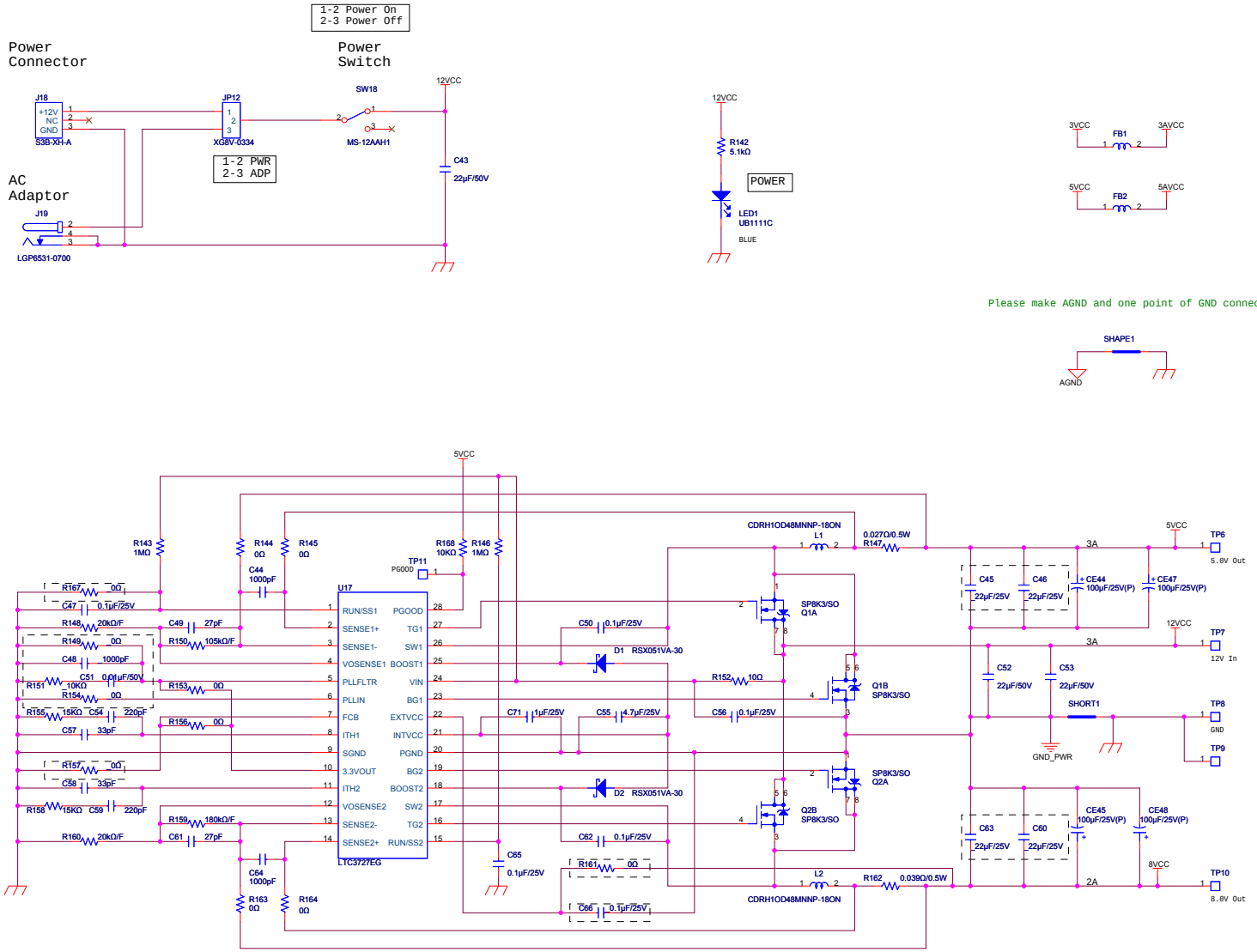
Key Input



Board fixed hole.



CHANGE						
Ver. 1.00B			Renesas Solutions Corp.			M3A-HS64G01
	SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	Key Input (9 / 10)
	DATE	09-03-02					DK30759



CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Power Generate (10 / 10)
Ver. 1.00B		SCALE			DK30759
		DATE	09-03-02		

SH7264 Optional board M3A-HS64G02 SCHEMATICS

Note:

Digital GND (GND)

Analog GND (AVSS)

Analog GND (AGND1,AGND2)

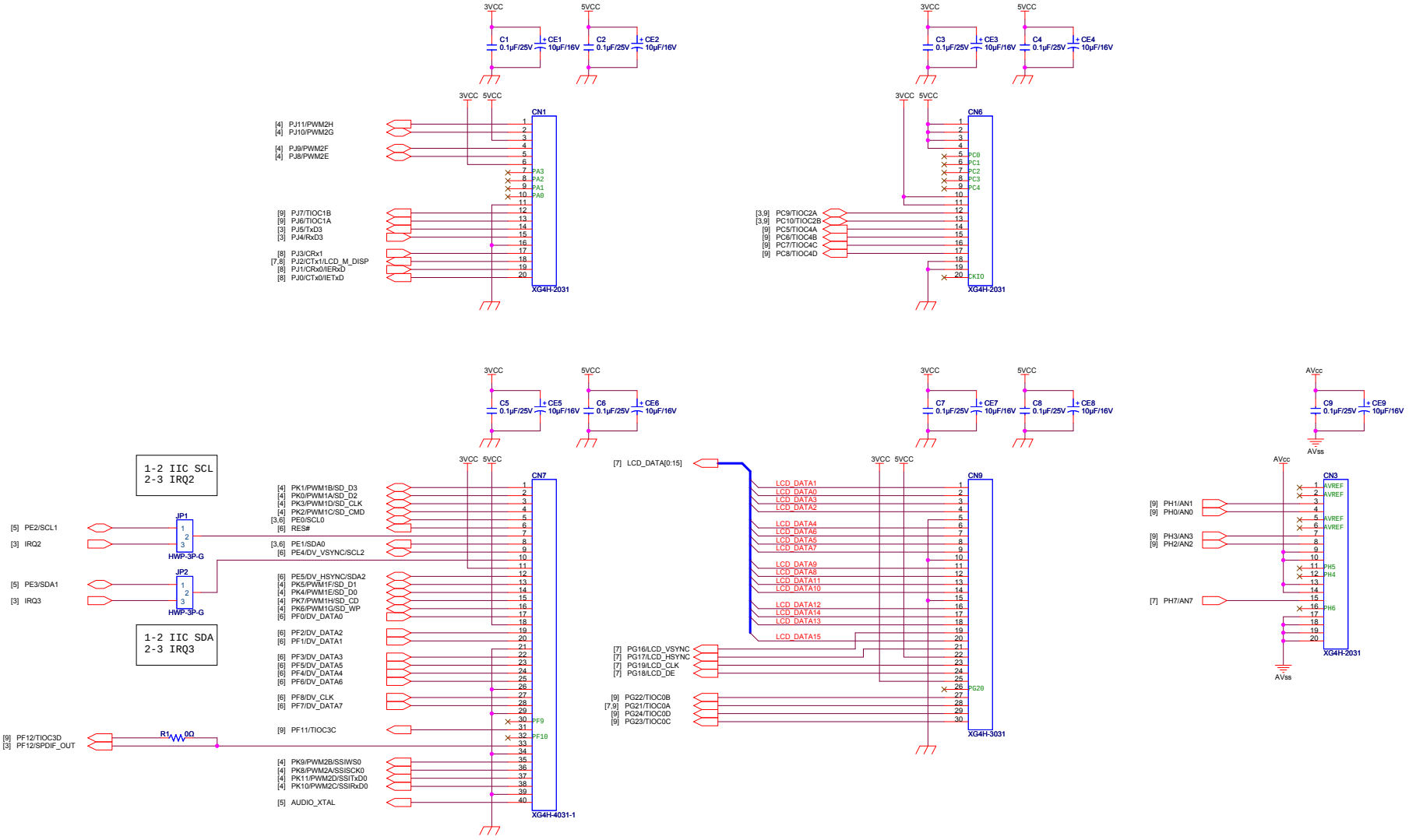
Not mounted

12VCC = Digital 12V Power in
8VCC = Digital 8V for CD
5VCC = Digital 5V
3VCC = Digital 3.3V
3AVCC1 = Analog 3.3V for Audio DAC
3AVCC2 = Analog 3.3V for Video Decoder
AVcc = Analog 3.3V for Key Input
MCVCC = Digital 3.3V / 5V for SD

R = Fixed Resistors
C = Ceramic Caps
CP = Decoupling Caps
CE = Electrolytic Caps (Tantal / Electric)

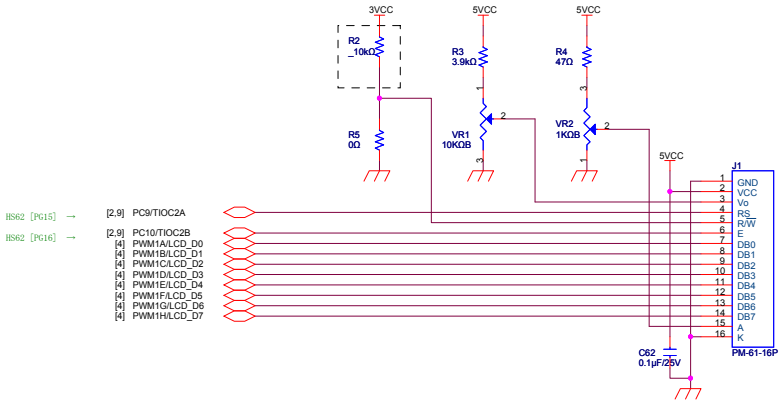
CHANGE						
Ver. 1.00B	SCALE		Renesas Solutions Corp.			M3A-HS64G02
	DATE	09-03-02	DRAWN	CHECKED	DESIGNED	APPROVED
						INDEX (1 / 10)
						DK30762

SH7264 Extension Connector



CHANGE			Renesas Solutions Corp.				M3A-HS64G02	
			DRAWN	CHECKED	DESIGNED	APPROVED	CPU Board Stack Connector	(2 / 10)
Ver. 1.00B		SCALE					DK30762	
		DATE	09-03-02					

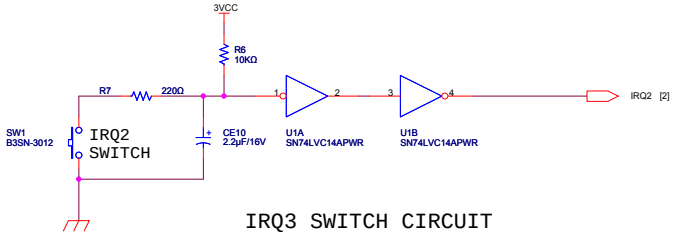
Character Type LCD Connector



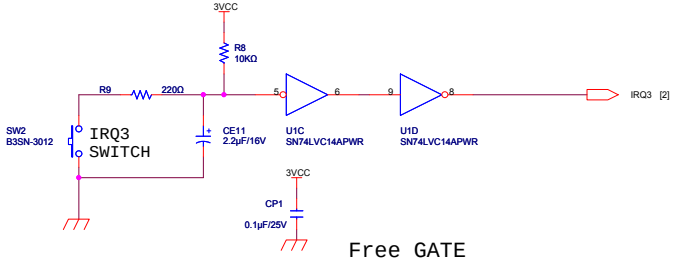
RSPDIF Through Hole.

UART Interface

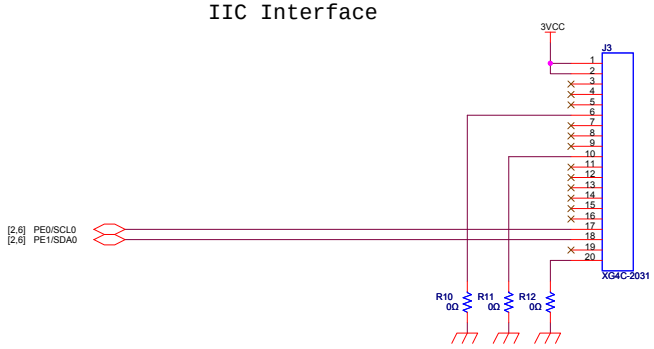
IRQ2 SWITCH CIRCUIT



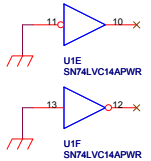
IRQ3 SWITCH CIRCUIT



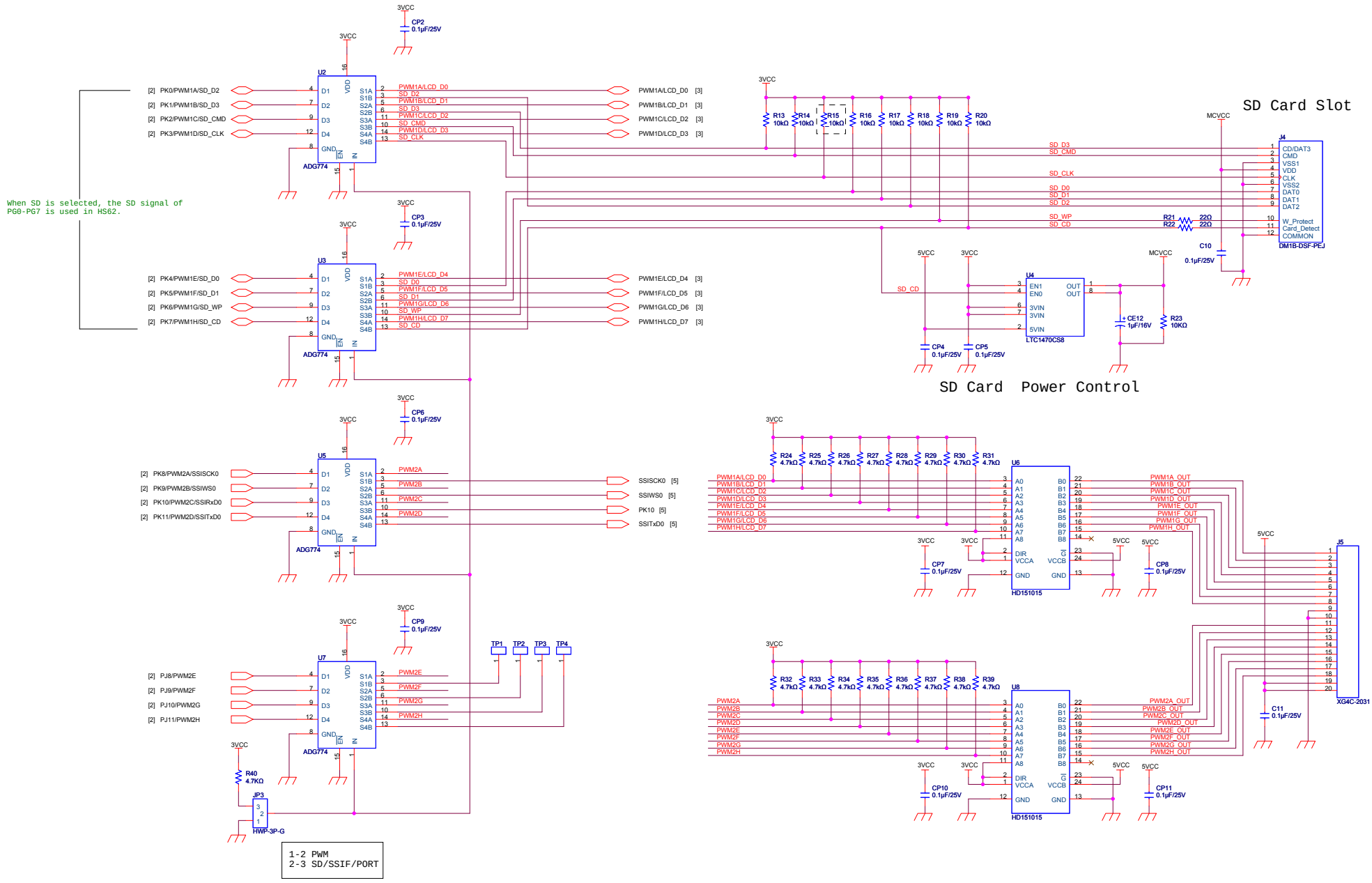
IIC Interface



Free GATE



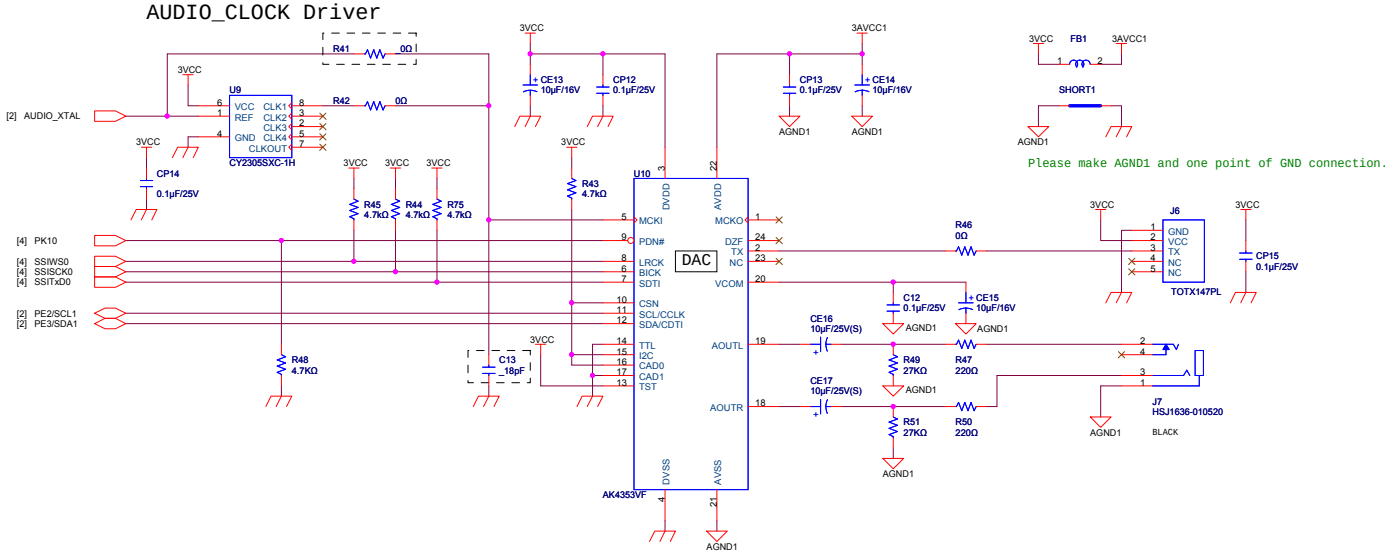
CHANGE	Ver. 1.00B		SCALE		Renesas Solutions Corp.	M3A-HS64G02
			DATE	09-03-02	DRAWN / CHECKED / DESIGNED / APPROVED	Character LCD/UART/IIC/IRQ (3 / 10)
						DK30762



CHANGE			Renesas Solutions Corp.		M3A-HS64G02
			DRAWN / CHECKED / DESIGNED / APPROVED		SD Card Slot/PWM (4 / 10)
Ver. 1.00B		SCALE			DK30762
		DATE	09-03-02		

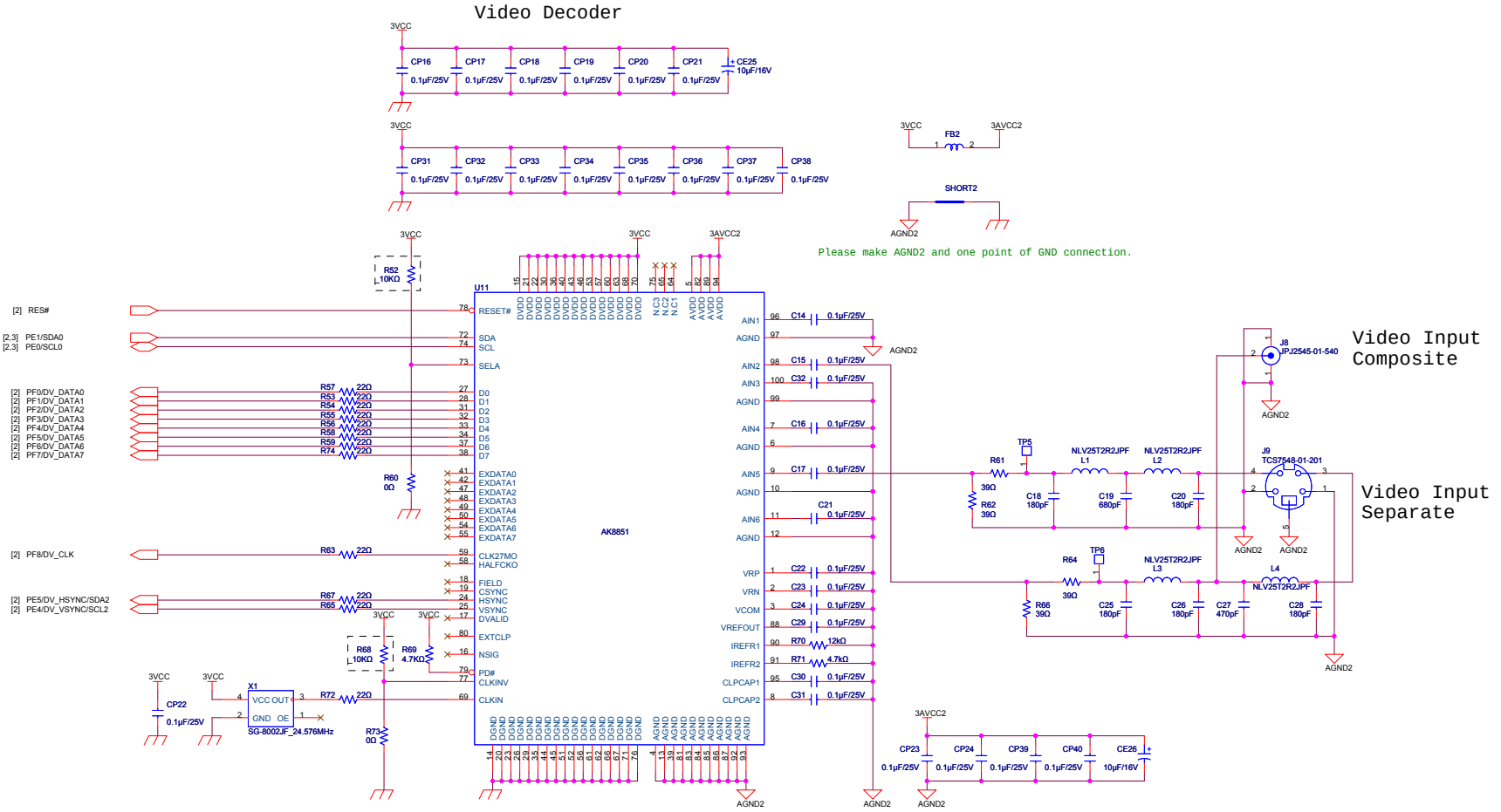
Audio Interface

AUDIO_CLOCK Driver



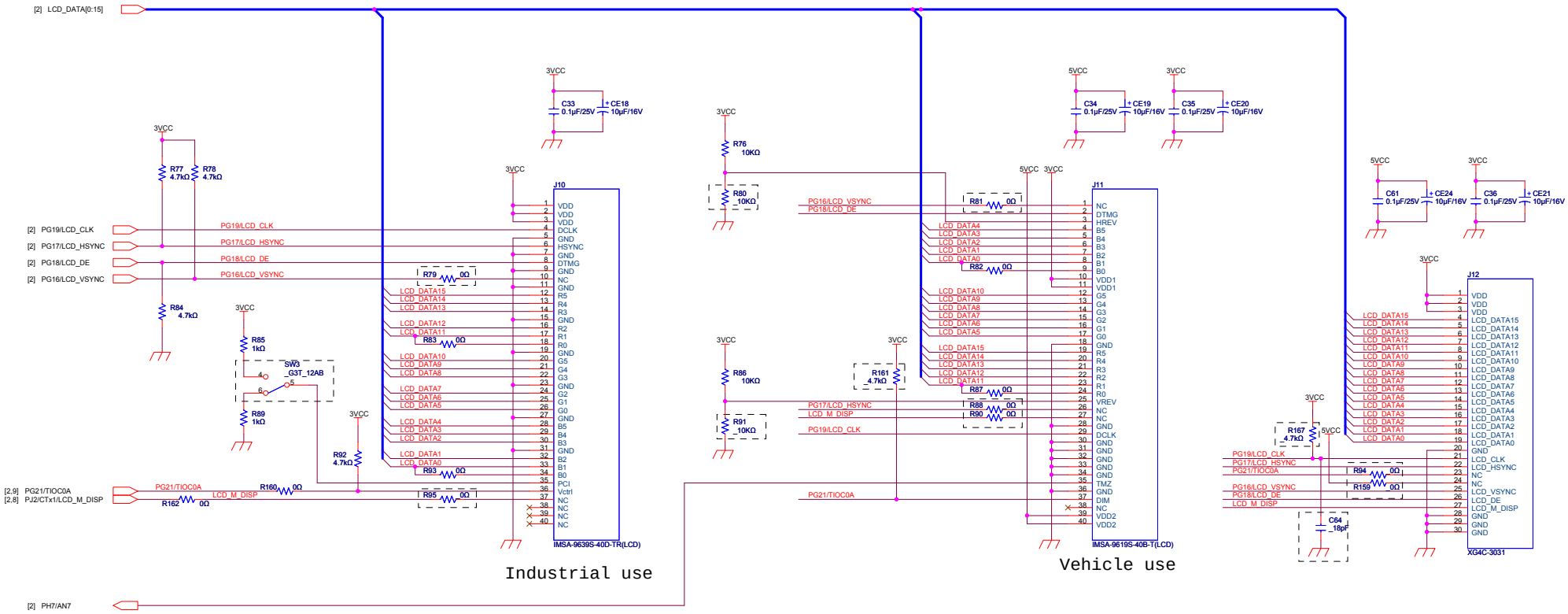
Please make AGND1 and one point of GND connection.

CHANGE	Ver. 1.00B		Renesas Solutions Corp.			M3A-HS64G02
			DRAWN	CHECKED	DESIGNED	APPROVED	Audio D/A Converter
		SCALE					(5 / 10)
		DATE	09-03-02				DK30762

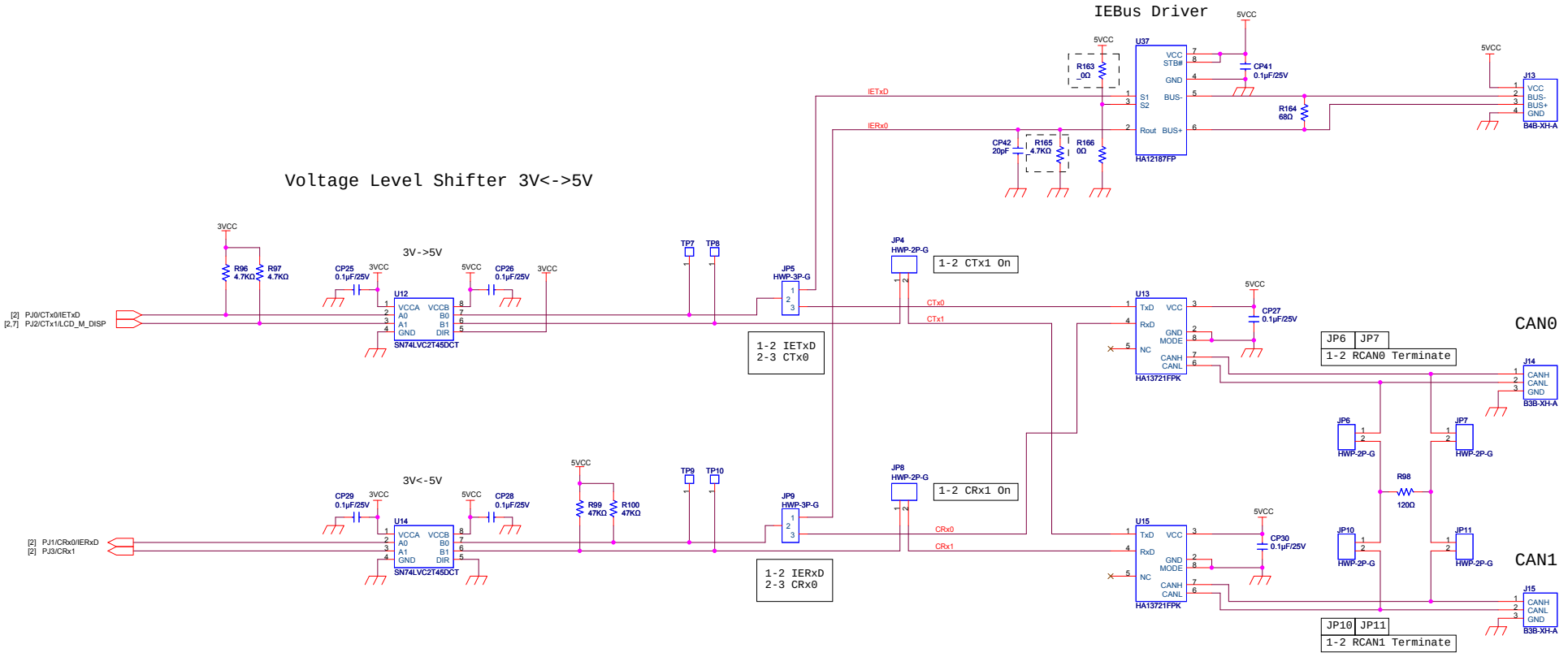


CHANGE			Renesas Solutions Corp.		M3A-HS64G02
			DRAWN	CHECKED / DESIGNED / APPROVED	Video Decoder (6 / 10)
Ver. 1.00B		SCALE			DK30762
		DATE	09-03-02		

TFT LCD Module Interface

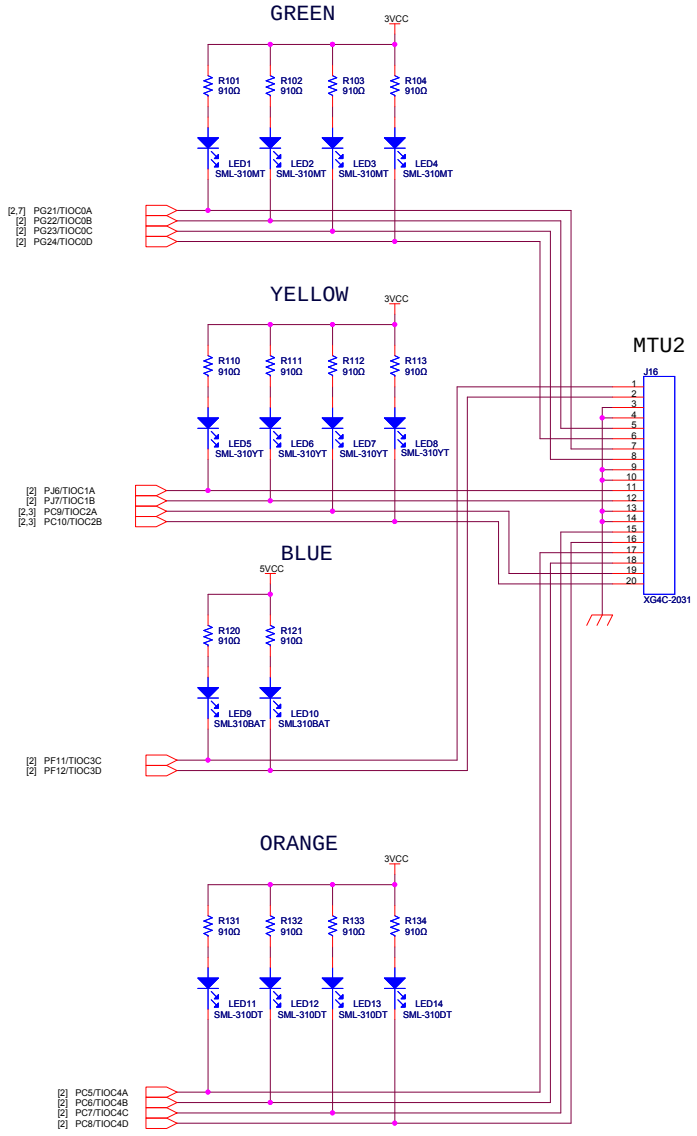


CHANGE			Renesas Solutions Corp.		M3A-HS64G02
			DRAWN / CHECKED / DESIGNED / APPROVED		LCD Module Connector (7 / 10)
Ver. 1.00B		SCALE			DK30762
		DATE	09-03-02		

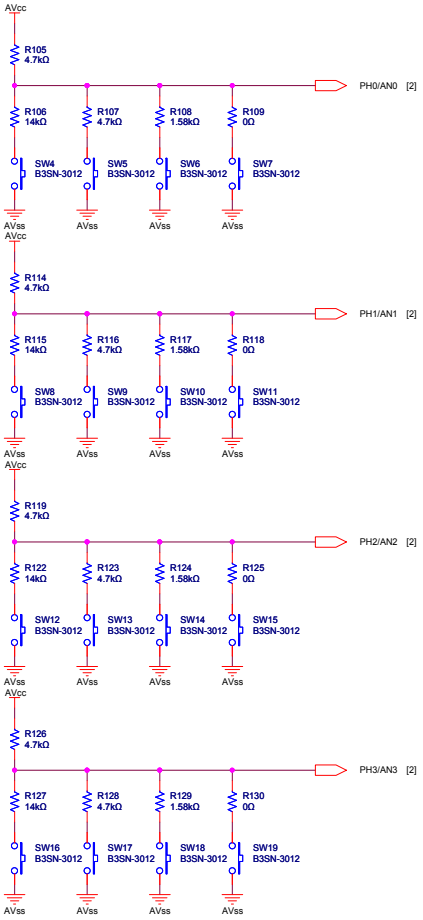


CHANGE			Renesas Solutions Corp.				M3A-HS64G02
			DRAWN	CHECKED	DESIGNED	APPROVED	CAN/IEBus (8 / 10)
Ver. 1.00B	SCALE						DK30762
	DATE	09-03-02					

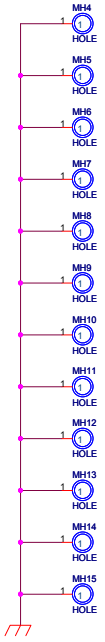
LED



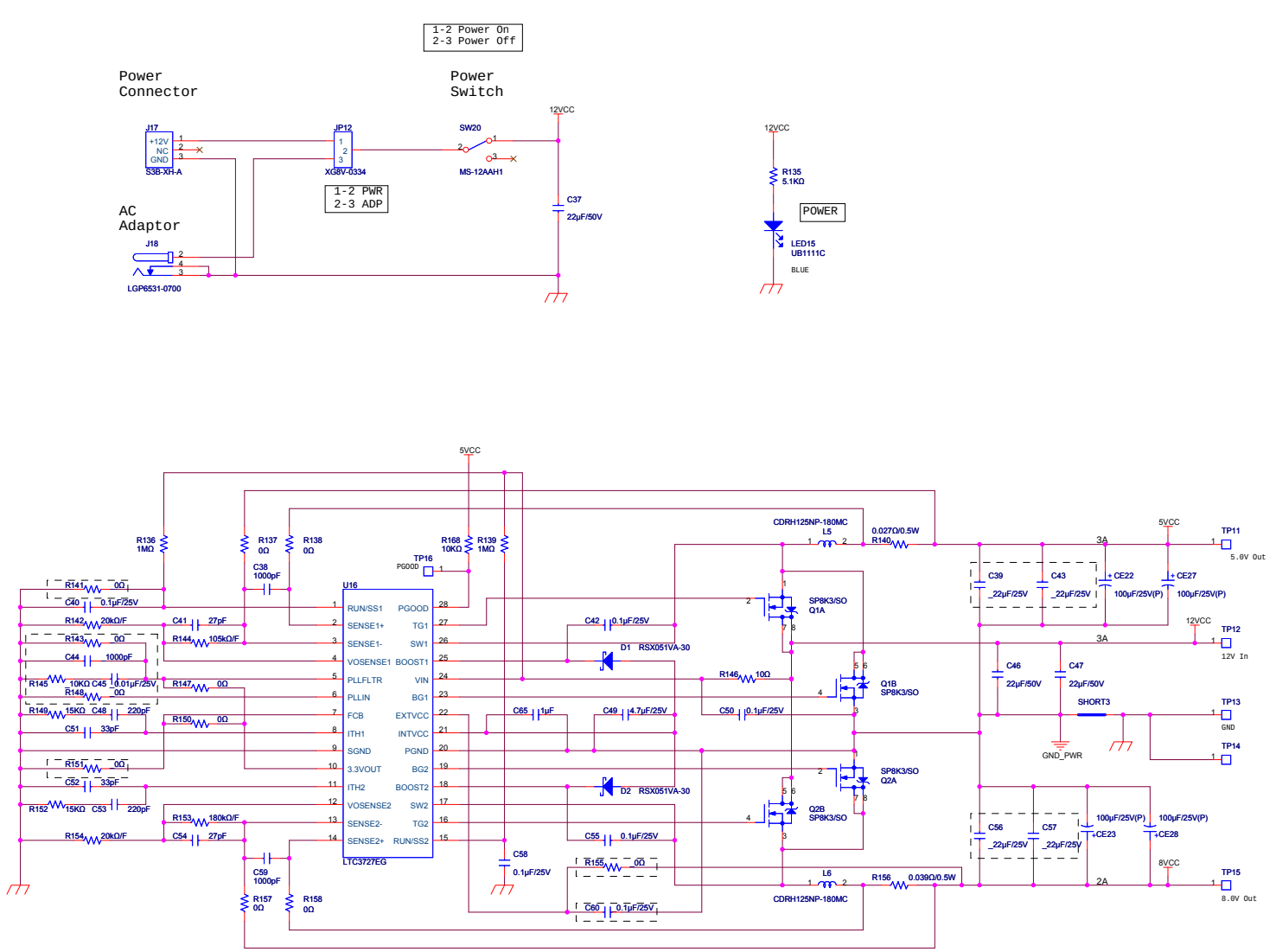
Key Input



Board fixed hole.



CHANGE					
Ver. 1.00B		Renesas Solutions Corp.			M3A-HS64G02
	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED	LED/Key Input
	DATE 09-03-02					(9 / 10)
						DK30762



CHANGE			Renesas Solutions Corp.		M3A-HS64G02
			DRAWN / CHECKED / DESIGNED / APPROVED		Power Generate (10 / 10)
Ver. 1.00B		SCALE			DK30762
		DATE	09-03-02		

REVISION HISTORY	SH7269 CPU Board R0K572690C000BR User's Manual

Rev.	Date	Description	
		Page	Summary
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Publication Date: Rev. 1.00 Dec. 07, 2011
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Colophon 1.1

SH7269 CPU Board
R0K572690C000BR

Renesas Electronics Corporation

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(Previous number:R20UT0159EJ0007)