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Using the Transient Load Generator on the ISL8200M 2-Phase Power Module Evaluation Board (ISL8200MEVAL2PHZ)

The Need for Testing Transient Load Response of POL (Point of Load) Regulators

Today's FPGAs, DSPs and other processors require higher load currents than in the past. It is not uncommon to see load currents in the 10A-20A range or higher. Manufacturers of these devices specify tight regulation of the supply even during load transients. In order to verify the POL regulators meet these requirements, it is necessary to test them with a load transient generator (also referred to as a load step generator).

Load transient testing also tells us a lot about the loop response and stability of the POL. A POL regulator may have a stable output under a steady state load, but then exhibit large voltage excursions, ringing, or even oscillations during a load transient due to an under damped or unstable control loop. The output may also be slow to respond to a load step indicating an over damped or low bandwidth loop response. Checking the POL regulator for these issues is a very important step in evaluating the overall regulator performance.

A similar transient load generator is also used on many Intersil evaluation boards including but not limited to the following part numbers: ISL6228, ISL62391, ISL62392, ISL62386, ISL6244, ISL6263, ISL6264, ISL6266, ISL62881, ISL62882 ISL62883, ISL62884, ISL6308, ISL6553, ISL6558, ISL6560, ISL6562, ISL6565, ISL8102, ISL8103, ISL95210, and ISL95870.

Limitations of Commercially Available Electronic Loads

Commercially available electronic loads can be used to generate steady-state load current as well as load transients. They are easy to use and highly programmable, but have limitations. Maximum programmable slew rates are typically in the 1A/µs to 2A/µs range, which may be acceptable for some lower load current applications, but can be too slow to adequately test higher current circuits. Additionally, the slew rates that are programmed are not the actual slew rates that are achieved directly at the load. This is due to the inductance limiting the di/dt in the long cabling that is typically required to connect the electronic load to the output of the regulator.

Figure 1 shows the typical setup of an electronic load applied to the output of a POL regulator. The load is set up for a 0A-4A step with a 4µs rise time or 1A/µs slew rate. Similarly, it is set up for a 4A-0A step with a 4µs fall time, which also gives a 1A/µs slew rate.

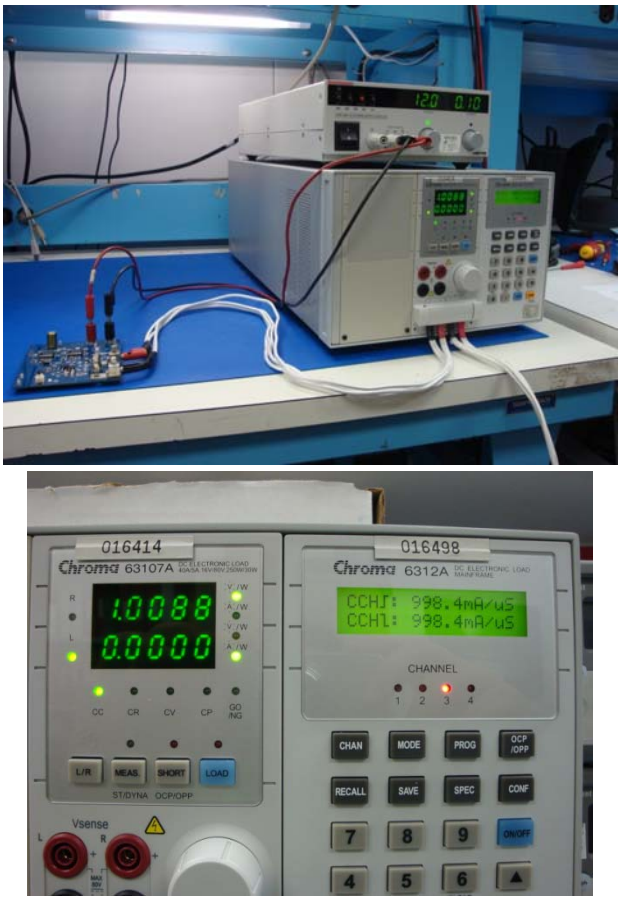


FIGURE 1. TYPICAL ELECTRONIC LOAD SETUP

Figure 2 is a scope shot of the waveform as it appears at the output of the regulator. Actual slew rates are reduced to approximately 0.27A/µs (73%) primarily due to the inductance of the cable from the electronic load to the output of the regulator.

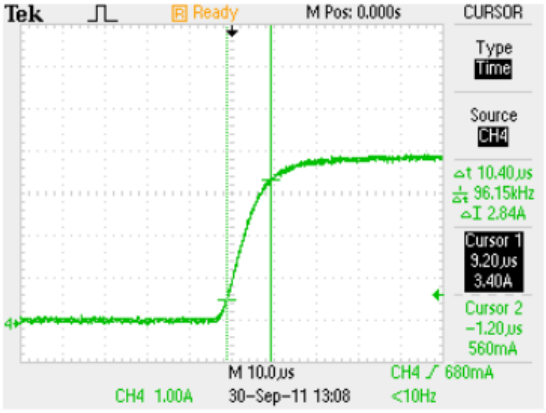


FIGURE 2. ACTUAL LOAD STEP AT LOAD

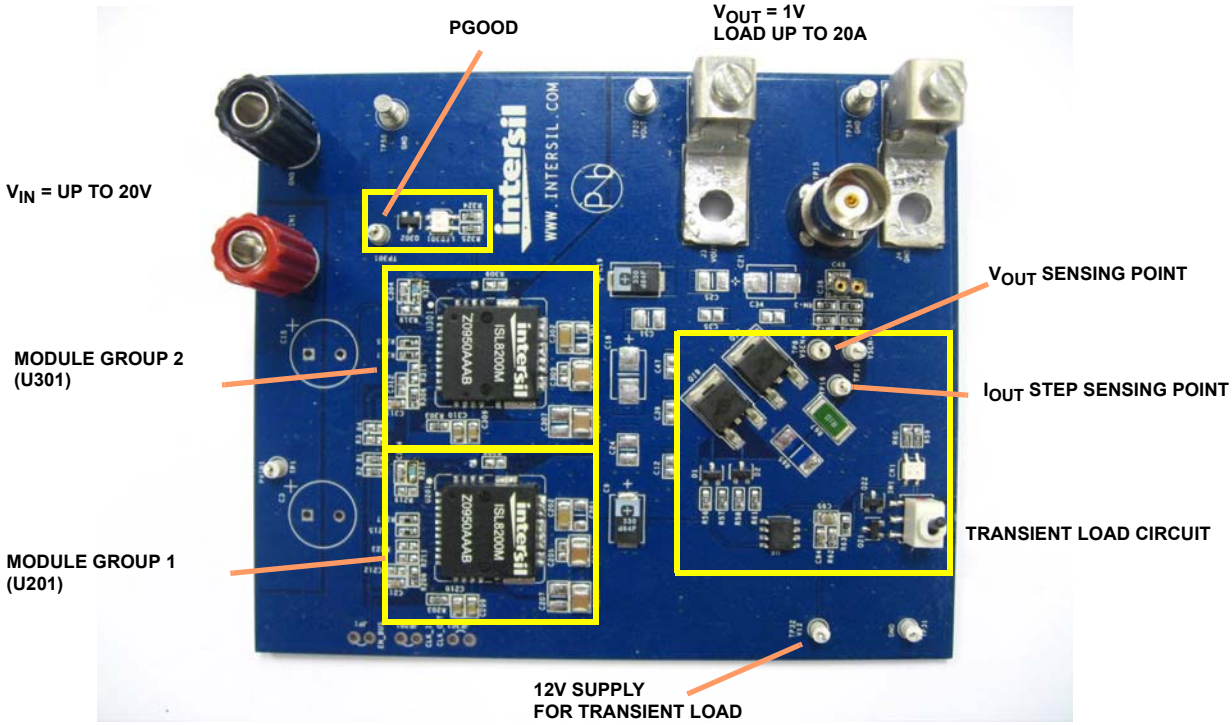


FIGURE 3. ISL8200MEVAL2PHZ EVALUATION BOARD

The ISL8200MEVAL2PHZ Evaluation Board

Due to the limitations of electronic loads, it is sometimes necessary to create your own transient load generator to generate the fast slew rates necessary to exercise high load current regulators. In the case of the ISL8200MEVAL2PHZ evaluation board, the load generator is provided directly on the board (see Figure 3). This is not only convenient, but it places the load directly on the output of the regulator, which minimizes the impact seen in long cabling.

The ISL8200M power module is capable of load current sharing up to six modules for 10A to 60A applications. The ISL8200MEVAL2PHZ evaluation board is set up with two ISL8200M Power Modules for up to 20A of load current. Please refer to Application Note 1544 (AN1544), “ISL8200MEVAL2PHZ Evaluation Board User’s Guide” for additional information about the evaluation board.

Using the Onboard Transient Load Generator of the ISL8200EVAL2PHZ for the First Time

Figure 4 shows the schematic for the load transient generator. Switch SW1 activates the load generator circuit in the schematic in the “on” position. Before powering up the ISL8200EVAL2PHZ board for the first time, it is recommended you verify that SW1 is in the “off” position. With the rest of the evaluation board unpowered (no voltage applied to V_{IN}), apply 12V across TP32(V12) and TP31(GND). If SW1 is in the “off” position, the red indicator LED in CR1 is forward biased and illuminates. If the green LED is lit, this indicates that SW1 is in the “on” position. If the green indicator is lit, flip SW1 to off and verify the red indicator LED is now lit. Once you’ve verified the load generator is off, you can power up the board by applying a voltage to V_{IN} (5V to 20V is recommended) and verify it is regulating. The board is set up for 1V V_{OUT}, so $1V_{DC}$ should be seen on a multimeter or on an oscilloscope. (Note: DNP or “Do Not Populate” are components that are not populated during the board assembly process and are place holders should the user want to populate them at a later time).

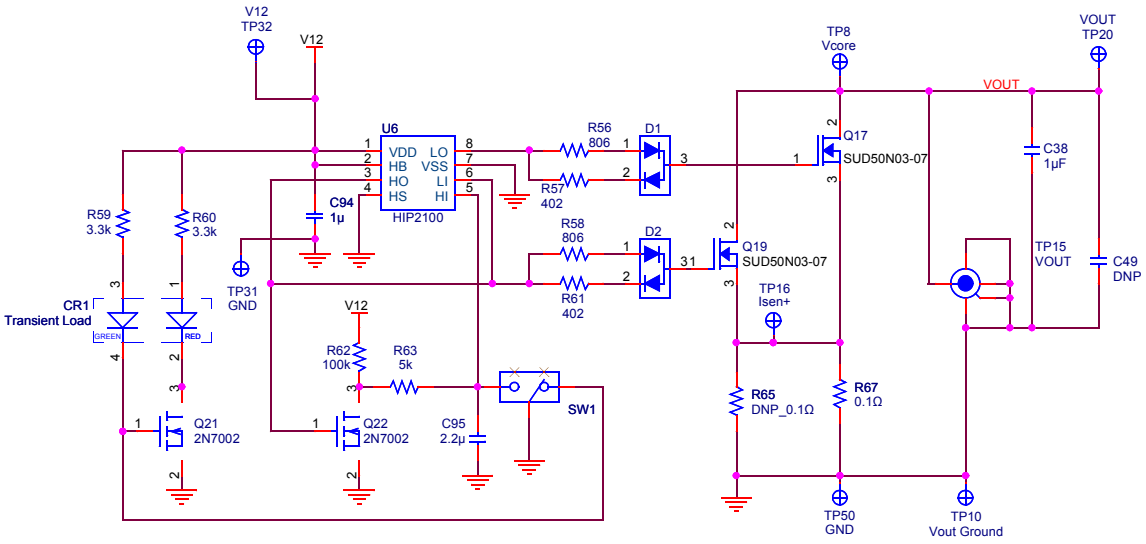


FIGURE 4. TRANSIENT LOAD GENERATOR SCHEMATIC ON ISL8200MEVAL2PHZ

Once regulation has been verified, the load generator can be used by switching SW1 to the “on” position. The output current waveform can be seen by placing a scope probe (voltage probe) on TP16. Figure 5 shows a scope shot of TP16 as well as V_{OUT} (TP20) at various input voltages.

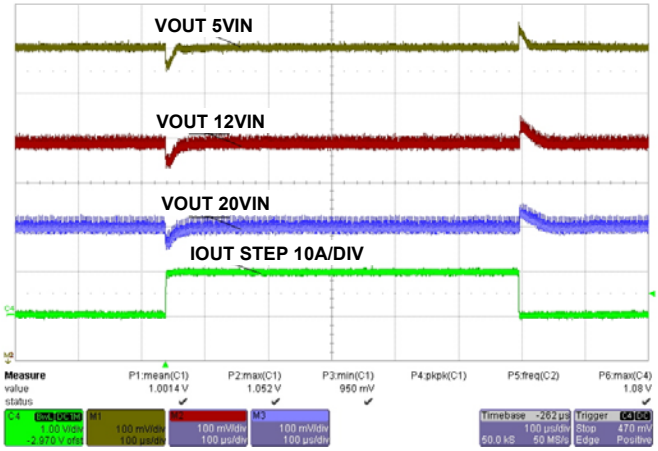
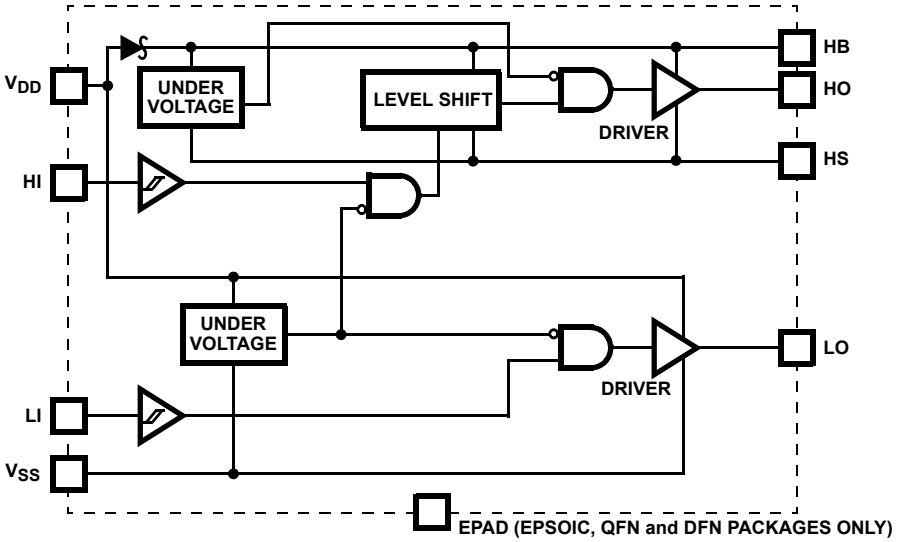


FIGURE 5. LOAD TRANSIENT (0A TO 10A STEP, SLEW RATE = 10A/µs) FOR INPUT = 5, 12, 20V



*EPAD = Exposed Pad. The EPAD is electrically isolated from all other pins. For best thermal performance connect the EPAD to the PCB power ground plane.

FIGURE 6. HIP2100 FUNCTIONAL BLOCK DIAGRAM

Analyzing the Transient Load Generator Circuit

The analysis of the circuit in Figure 4 will begin with a discussion of the operation of the HIP2100. HIP2100, U6, is a non-inverting half bridge MOSFET driver capable of driving up to 2A of gate drive into MOSFETs Q17 and Q19. Figure 6 depicts the simplified functional block diagram for the HIP2100. VDD and HB are tied to TP32(V12) and supplies the bias for the HIP2100 MOSFET driver. While the HIP2100 is generally used to drive two n-channel MOSFETs in a half-bridge configuration, in this case it is being used to simultaneously drive two parallel MOSFETs.

With SW1 is in the “off” position, HI of the HIP2100 is shorted to ground. This sets its respective output, HO to 0V. HO is tied to LI, so LI is also 0V and consequently LO is 0V. With both gate drives at 0V, both n-ch MOSFETs, Q17 and Q19, are turned off and the load is not applied.

When SW1 is switched to the “on” position, several things occur. First, Capacitor C95 begins to charge through R62 and R63. As it reaches the turn-on threshold of the HI input, HO will switch high (12V). LI also goes high, which causes LO to go high. Since LO and HO are both high, MOSFETS Q17 and Q19 are both on and current flows through R67.

The voltage developed at TP16, V_{Isens+}, can be described by a simple voltage divider (Equation 1) where $r_{DS(ON)}$ is the on-resistance of the MOSFETs and V_{OUT} = 1V. The $r_{DS(ON)}$ is divided by two since the MOSFETs are in parallel.

$$V_{Isens+} = (V_{OUT} \times R67)/(r_{DS(ON)}/2 + R67) = (1V \times 0.1\Omega)/(0.007\Omega/2 + 0.1\Omega) \quad \text{(EQ. 1)}$$

Since $r_{DS(ON)}/2 << R67$, V_{Isens+} can be approximated as shown in Equation 2.

$$V_{Isens+} = V_{OUT} = 1V \quad \text{(EQ. 2)}$$

The peak load current is then approximated as:

$$I_{load-pk} = V_{OUT}/R67 = 1V/0.1\Omega = 10A \quad \text{(EQ. 3)}$$

Because V_{Isens+} =~ 1V when $I_{load-pk}$ = 10A, the current can be easily monitored with a voltage probe on TP16. The voltage will change 100mV for every 1A of load current.

Q22 turns on because HO is high. C95 begins to discharge through R63 and Q22 to ground and HI will drop in voltage till it reaches the turn-off threshold of the HIP2100. Once HI reaches this threshold, HO, LI and LO all go low and Q17, Q19, and Q22 turn off. Since Q22 is off, C95 starts charging again and the process is repeated.

Figure 7 shows a scope shot of V_{Isens+} (TP16) with a time scale that allows the repetitive process to be seen.

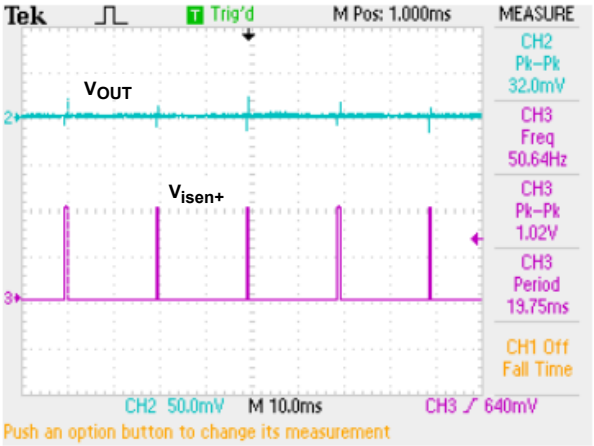


FIGURE 7. TRANSIENT LOAD GENERATOR OUTPUT WAVEFORMS (V_{isens+} AND V_{OUT})

Using an Electronic Load with the Onboard Transient Load Generator

It may be desirable to create a load step that does not go from no load to full peak load. That is, the user may want to have a load that steps from some nominal load current to the peak current and then back to the nominal current again. The easiest way to accomplish this is to set up an electronic load with a constant load current. Attach the output of the electronic load to output terminals J3 and J4 using the cables as shown back in Figure 1. Set the load current to the desired constant current (e.g. 5A). Next, turn on the onboard load generator on the ISL8200MEVAL2PHZ.

Figure 8 shows a scope shot of the voltage at Vsen+ (TP16). Since the voltage changes 100mV for every 1A in current, it can be seen that the output load is stepping form 5A to 15A and then back to 5A.

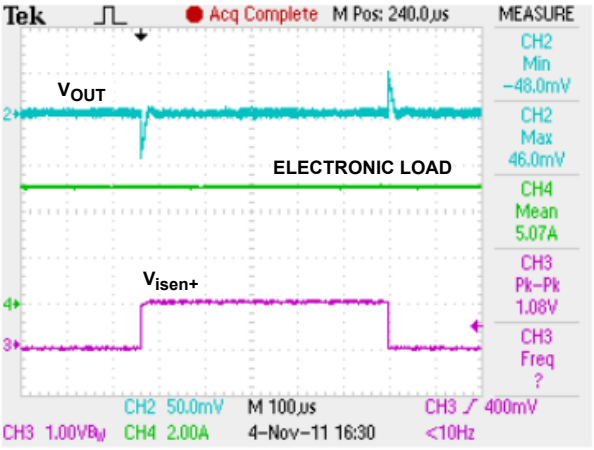


FIGURE 8. TRANSIENT LOAD GENERATOR OUTPUT WAVEFORMS, 5A TO 15A LOAD STEP

Changing the Characteristics of the Load Generator

There are several changes that can be made to the load generator to alter the load transient characteristics depending on the user requirements. These changes include the peak load current, rise/fall times (slew rates), and pulse duration/duty cycle.

Peak Load Current

The peak current is determined by V_{OUT} and R67. V_{OUT} can be changed by changing the voltage setting resistor as shown in Application Note 1544 (AN1544), "ISL8200MEVAL2PHZ Evaluation Board User's Guide" and in the ISL8200M datasheet. If V_{OUT} is changed, care should be taken to ensure that the peak currents of the load generator do not exceed the overcurrent protection trip current of the ISL8200M. Equation 3 can be rewritten as Equation 4 and the user can easily calculate a suitable resistance to achieve the desired peak load current based on the V_{OUT} that has been selected.

$$R67 = V_{OUT} / I_{load-peak} \quad \text{(EQ. 4)}$$

If the desired value of R67 is not a standard resistor value, the user can also populate R65. R65 is in parallel with R67 and can be used to create non-standard resistor values or to reduce power dissipation. There will be more on power dissipation in R67 in "Load Pulse On-Time/Duty Cycle" on page 5. R65 should equal R67 so that they share current equally.

Rise/Fall Times (Slew Rates)

The rise time of the load step is determined by the turn on times of MOSFETs Q17 and Q19. This is largely determined by the gate resistors (R56 & R58) and equivalent FET gate capacitance. R56 should be equal to R58 so that both MOSFETs turn on at the same time. Currently, R56 = R58 = 806Ω and this achieves a rise time of about 2.37µs. Figure 9 shows an approximate relationship between rising slew rate and R56 and R58.

Similarly, the fall times of the load step can be controlled with R57 and R61. The evaluation board is populated with R57 = R61 = 402Ω. This gives a fall time of around 1.6µs. Figure 9 also shows an approximate relationship between the falling slew rate and R57 and R61.

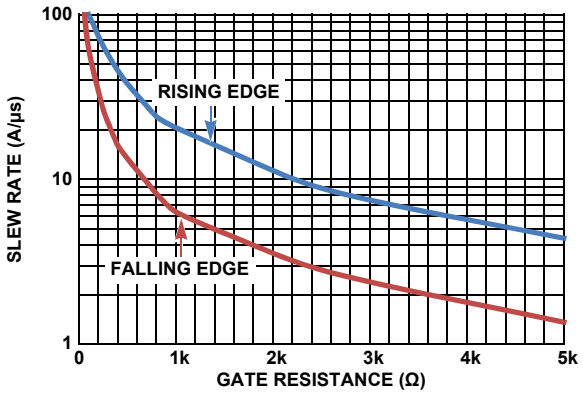


FIGURE 9. SLEW RATE vs. GATE RESISTANCE, R56 = R58, R57 = R61

Load Pulse On-Time/Duty Cycle

Figure 10 and 11 show the timing sequences for generating the load step pulse. When SW1 is initially switched to the "on" position, HI = HO = LI = LO = 0V, and Q22 is off. C95 begins to charge through R62 and R63. Once the voltage across C95 reaches the turn-on threshold of the HIP2100, HI = HO = LI = LO = 12V, and C95 begins to discharge through R63 and Q22. Once the voltage across C95 reaches the turn-off threshold of the HIP2100, HI = HO = LI = LO = 0V once again and the cycle repeats. See the HIP2100 datasheet for threshold information.

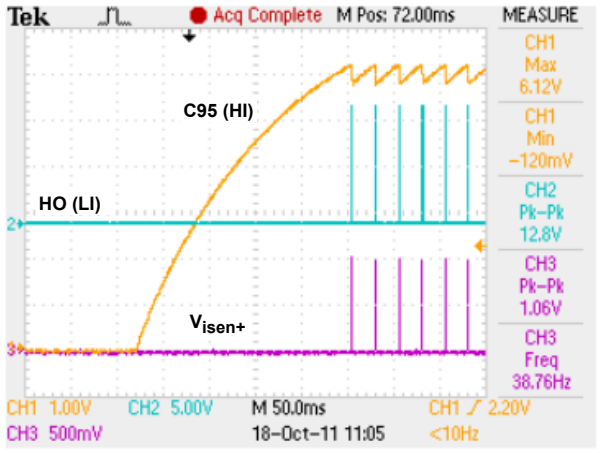


FIGURE 10. START-UP TIMING DIAGRAM FOR LOAD CYCLE

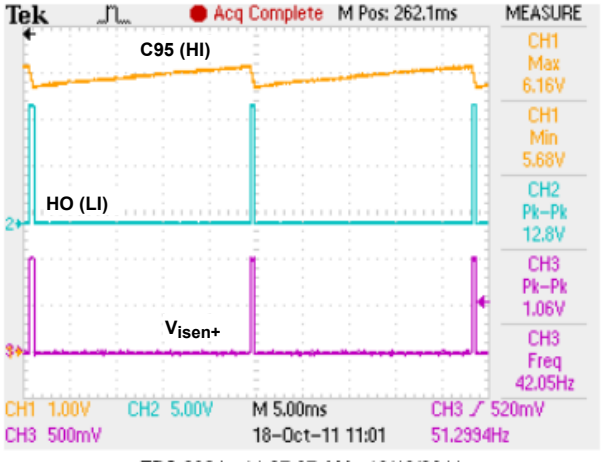


FIGURE 11. STEADY STATE TIMING DIAGRAM FOR LOAD CYCLE

The pulse duration is largely determined by the discharge time of the capacitor through R63, and the time between pulses is largely determined by the charge time through R62 + R63. The user can manipulate the resistance values to achieve the desired pulse time and duty cycle, however, the average power dissipation through R67 (and R65 if populated) needs to be considered. The evaluation board is set up for a pulse on time of around 0.528ms with time between pulses of 19.14ms for a Duty cycle of around 2.68%. R63 affects both charge and discharge time, while R62 only affects discharge time.

The average power dissipation in R67 is given by Equation 5.

$$P_{R67} = D \times (I_{load-pk})^2 \times R67 = 0.0268 \times (10)^2 \times 100m\Omega = 268mW \quad \text{(EQ. 5)}$$

R67 is rated for 1W, so this is sufficient. If the duty cycle is increased which subsequently increases the power dissipation in R67, R65 can also be populated to reduce the power dissipation. As stated before, R67 should be equal to R65 to equally share the current.

Figure 12 gives an approximate change in pulse on-time vs. R63 while Figure 13 shows the approximate time between pulses vs. R62.

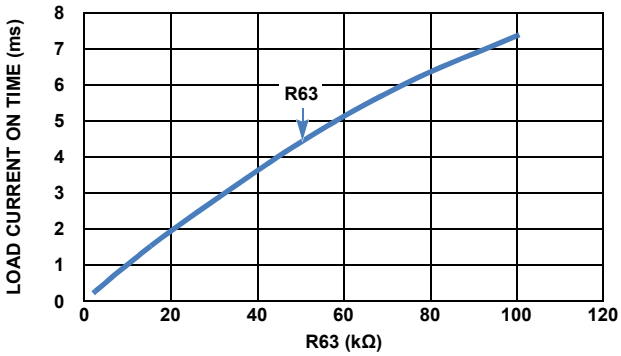


FIGURE 12. LOAD CURRENT ON-TIME vs. R63

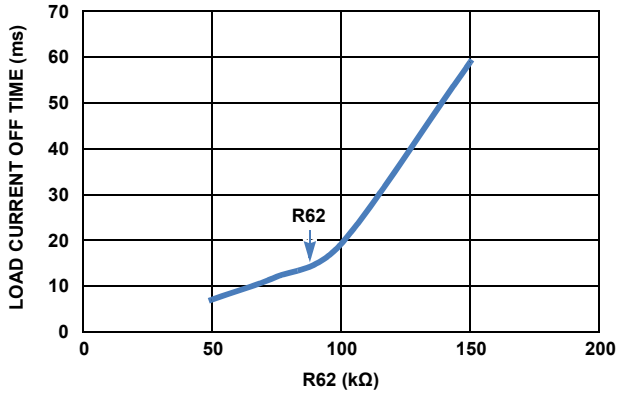


FIGURE 13. TIME BETWEEN CURRENT PULSES vs. R62. R63 = 5kΩ