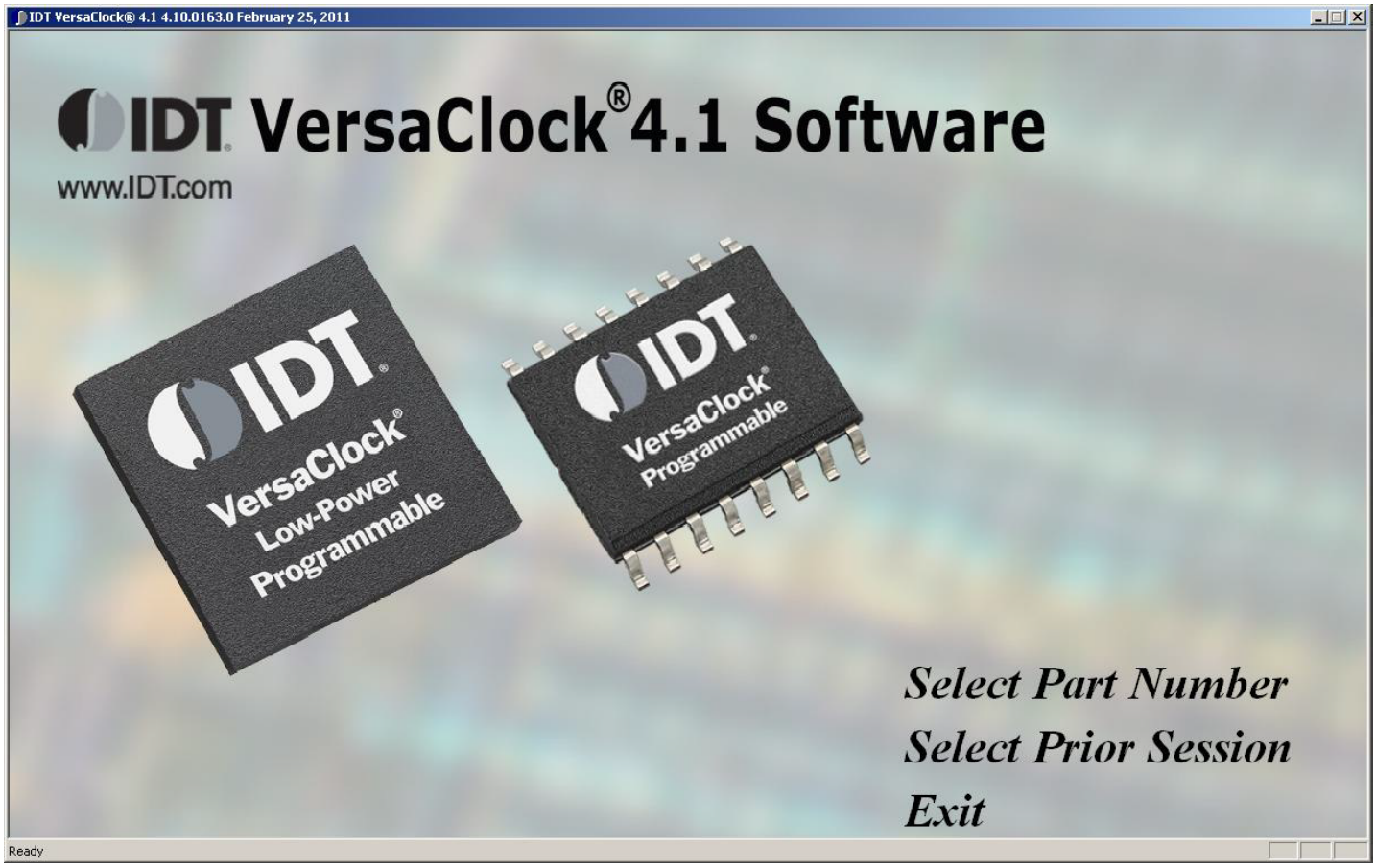

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Programmable Clocks - Introduction

The VersaClock LP programming software is targeted at enabling novice through experienced PLL designers to easily select and optimize performance from the IDT programmable clock product line. These products include devices that are EEPROM programmable through an I^2C port. The current release of the VersaClock software supports both VersaClock III (IDT5V19EExxx and IDT5V49EExxx) and VersaClock LP (IDT5P49EExxx) products.

The software evaluates the desired input and output frequencies and sets the corresponding PLL parameters to optimize the clock output jitter. For the given input frequency, a pin allocation map is generated.

The IDT VersaClock LP programmable clock portfolio contains products with the capability to incorporate Spread Spectrum functionality on selected clock outputs. Spread Spectrum creates a regular frequency “dithering” of the output frequency to reduce the electro-magnetic interference (EMI) radiation associated with a fundamental clock signal propagating around a system or across cabled interfaces.

The Spread Spectrum capability can be enabled with either “Center Spread” or “Down Spread” functionality at a variety of selectable percentage increments and modulation frequencies.

There is also a Detail View mode that allows the user to manipulate individual component settings. Changes in PLL configurations automatically provide loop bandwidth, damping factor and phase margin for the configuration. This will allow the user to better integrate the device into the specific application.

Installing IDT VersaClock 4.1 Software

a) Software is available for free download from:

http://www.idt.com/go/Versaclock

b) You must install this application onto your computer's hard disk; you cannot run this program from the Internet.

c) Supported Computer Configurations: Windows XP and Vista with a minimum of 32 MB of RAM and 10 MB of available hard disk space.

d) There are two operation modes of the VersaClock 4.1 software: “Web Based” and optional “Desktop” database.

- VersaClock 4.1 Web Based operation downloads the latest part information every time the software is used. VersaClock 4.1 Web Based requires that the computer be connected to the Internet to operate. Users must have a MY.IDT.com account to access the server.
- VersaClock 4.1 desktop operation allows non-Internet connected operation. A separate product database download is required after the application portion of the software is installed. New part information and software updates are provided only when downloaded and installed from the download site above.

Note: VersaClock 4.1 software utilizes Microsoft™ Windows Installer software.

By selecting to download the VersaClock 4.1 software, a ZIP file will try to be downloaded or opened. You do not need to download the compressed ZIP file, only open the file and extract the two files - VersaClock.MSI and Setup.EXE - to your desktop.

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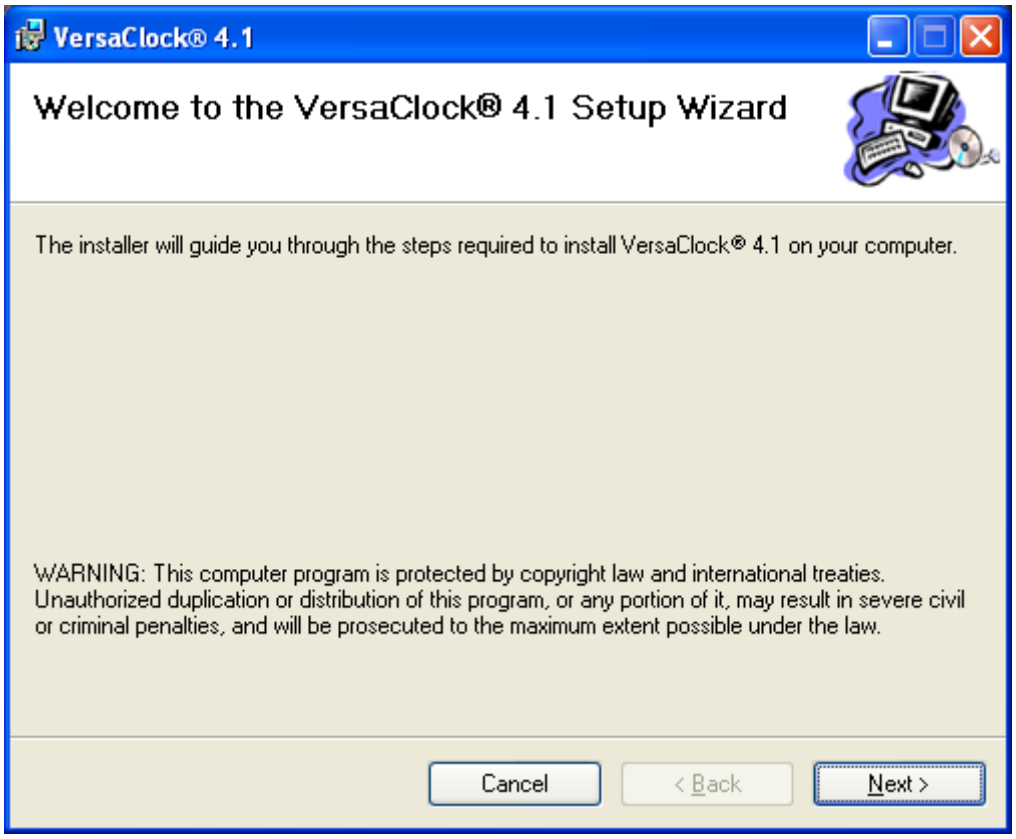
To Install the VersaClock 4.1 software, double click on the Setup.EXE file. The following screen will appear:



Select Next to automatically initiate the installation process and install over older versions of the software if defaults settings are used. Continue through the installation process and close the window when process is complete.

You do not need to restart your computer once the software is installed. You are now ready to use the IDT VersaClock 4.1 software. A VersaClock 4.1 icon will be placed in your Startup Menu as well as a shortcut on your Desktop.

You may also install the VersaClock Desktop Database file, to allow use of the software without connection to the internet.

*(**Note**: Periodically, the VersaClock 4.1 software will be updated and products added. When connecting to the product database, you will be alerted when new software is available. Desktop versions of the software must be manually checked and downloaded.)*

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Programming Software Operation

Getting Started

From your desktop, you will have an icon for “VersaClock 4.1”.

Double click on icon to start. You may also start from Start > Programs > VersaClock 4.1.

The VersaClock 4.1 software can be initiated by selecting the desired part number or by returning to a prior saved session. Selecting by part number provides a brief description of each part's functionality.

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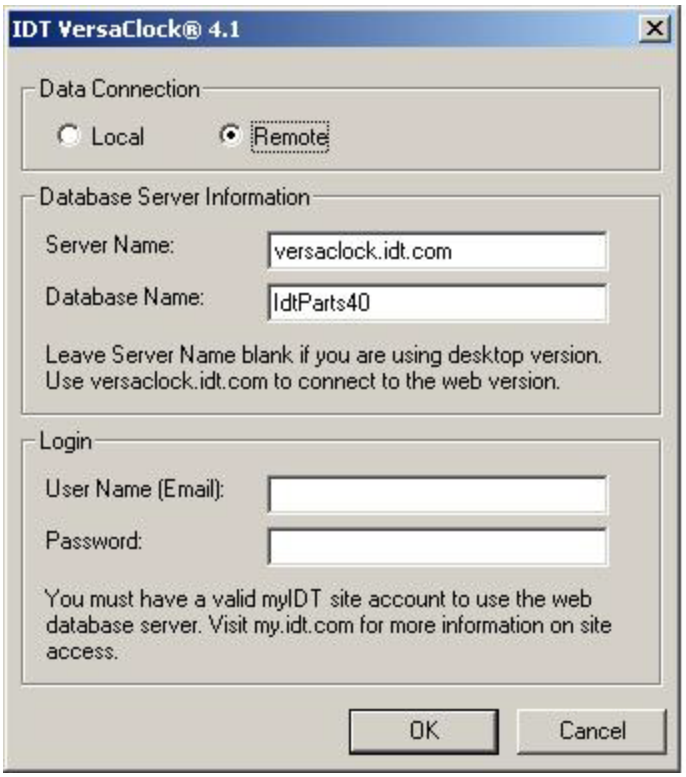
Connecting to VersaClock parts database



This dialog only appears on the first power up, or if accessed through the Settings menu.

VersaClock 4.1 operates in two modes: Remote (web) and Local (desktop). The **Remote mode** operation accesses the product database on the myIDT.com site, providing the latest product details supported by the software. You must have a myIDT account to access the site each time you initiate the software. Enter your myIDT user name (the email address associated with your account) and the password to connect to the web database and start the software.

The **Local mode** operation accesses a copy of the product database that was current at the time of installation. If you decide to use the local mode, it is up to the user to keep the database current through download and re-installation of the entire application. To start the software through local mode, click the Local Data Connection radio button. The Server Name will become blank and the Login fields will be greyed out. Selecting OK will access the database on your computer.

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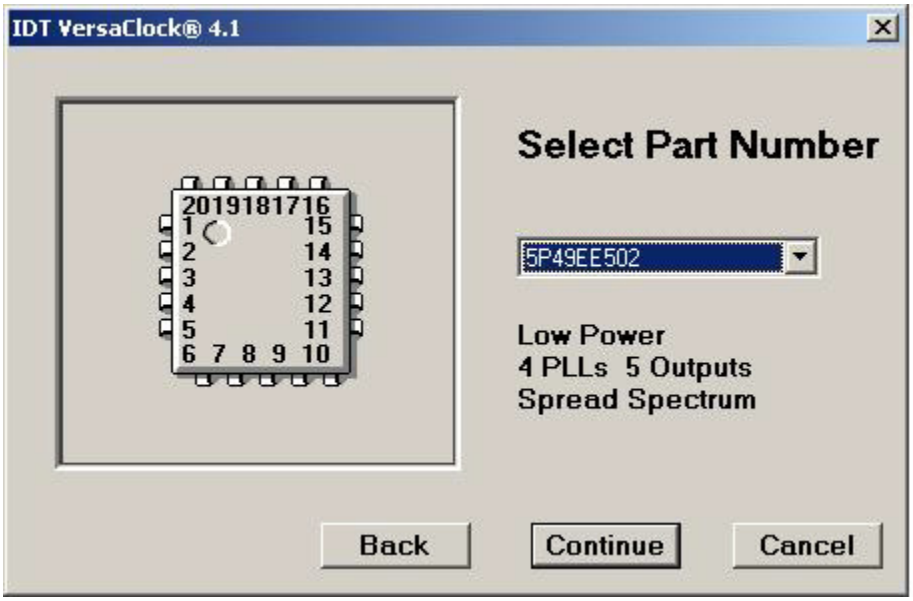
Selecting a Part



Each part is provided with a brief description of features that are available.

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Configuring Devices – Three Information Views

Single Configuration View (ALT+1) – Allows user to work on one register at a time.

Ability to configure outputs for a single register in a single screen.

Register Tabs across the top of the screen allow the user to select the register and copy/modify configurations on a register-by-register basis. There is the ability to copy contents of one register into another for configuration.

Selection of this mode is provided by selecting View > Single Register option.

All Configurations View (ALT+2) – Allows user to work on all configurations simultaneously.

All configuration inputs are entered in a matrix format to ensure that address selections conform to the anticipated changes.

To facilitate configurations, each output pin can be labeled to remind the user how each output will be used. Attribute tabs labeled with Req. ppm, Spread, Drive, etc. use the same matrix to apply the functionality to the target outputs during the single computation.

Selection of this mode is provided by selecting View > All Configurations option.

Detail View (ALT+3)– Allows user to manipulate individual register bit settings on one configuration at a time.

Ability to configure each PLL divider block, loop filter bandwidth and output configuration for a single configuration in a single screen. All selection have been mapped to human readable values, to minimize confusion.

Configuration Tabs across the top of the screen allow the user to select the each configuration and modify it configuration individually. There is the ability to copy contents of one configuration into another (ALT+C).

Selection of this mode is provided by selecting View > Detail option.

*(**Hint**: It is often useful to toggle between the three views to establish a complete configuration. For example, use* **All Configuration View** *or **Single Configuration View** to establish address frequency logic table, fix clock output and spread spectrum pin assignments. Once outputs are established, go to* **Detail View** *to adjust accuracy tolerance, spread spectrum amounts and/or clock output drive and voltage connection. **Detail View** should be the last configuration modified, as automated configuration overwrites hand modified settings. **Detail View** modifications may not be reflected back onto the **Single Configuration View** pin map. A warning that changes have been made in Detail View is shown on both Single and Multiple Configuration views.*

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Single Configuration View

Fields that are accessible to the user are in white. The user can include text information in the Company, Operator and Notes fields for reference. While the program is operating, the Company and Operator fields will default to the last session's values.

Input Frequency Selection

The user must select the starting frequency from which the operation of the PLL will be derived. Input frequency selection may impact the output clock accuracy, jitter or power consumption. Best performance is generated when the input frequency is an integer multiple of the desired output.

Users may select standard crystal frequencies from the pull down menu, or type in a value in the space provided.

Strategies for selecting the input frequency may include:

a) Use the target output frequency that is most sensitive in the system. It would ensure a 0 ppm solution (that is 0 ppm synthesis error) and lower phase noise performance.

b) Use of a common divider frequency to several outputs. This may minimize the number of PLLs that will be needed, thereby reducing power consumption.

A pull down menu of common input frequencies is provided. Other frequencies may be typed into the Reference Frequency window at any time. When typing in a frequency, place as many frequency decimal places as necessary, to insure best accuracy solution. Approximated frequencies (I.e. 33.3MHz instead of 33.3$\overline{3}$MHz) may change the starting frequency by 1000 ppm or more. The software cannot differentiate the intention of the user.

Target Output Frequency

At the top of this frame, the number of outputs for the device is indicated. In the interest of clarity, some outputs fields may be scrolled within the window.

a) **Pin No.** - Unassigned prior to the calculation unless the Manual Pin Assignment Option is applied (Options > Manual Pin Assignment). VersaClock software will assign pinout to minimize jitter and power by combining as many clock outputs on a PLL as possible.

b) **Desired MHz** - Target frequency to be synthesized. Always put in as many digits as will be allowed if non-zero. Last available digit is 1ppm value. This means enter 33.333333 MHz instead of 33.33 MHz.

   For those parts that support a separate 32.768kHz crystal, you must enter frequencies as 0.032678 (MHz) and VersaClock will assign the appropriate reference frequency output.

c) **Error ppm** - Synthesis accuracy tolerance window permissible for target frequency. Please consider that the input frequency source may have some error ppm and the synthesis error is additive to the source error.

   (For example, if the source has an accuracy of $\pm$20 ppm at room temperature and the output frequency is -5 ppm synthesis error, then the total output frequency accuracy at room temperature is +15/-25 ppm.)

   For each target output frequency, the user has the ability to specify the maximum tolerable output clock synthesis error in ppm (parts per million). This is the frequency error, which is additive to the error of the reference input. If no value is included, the default is zero. This is particularly helpful in cases where the input reference frequency does not allow, or gives poor solutions for 0 ppm accuracy.

   The software will provide the best performance solution within the given accuracy tolerance window. To achieve improved jitter performance, the window must be widened.

   Entering positive numbers - the accuracy window is the absolute value (+ and - ppm error values will be considered)

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Entering negative numbers - only frequencies lower than target frequency are considered.

The ppm accuracy has an upper bound of 9999, but the user should not exceed the deviations allowable by the user's system. While higher accuracy solutions may be achievable, a less accurate solution (within designated bounds) may be selected by the software, due to performance criteria.

Setting Differential Outputs

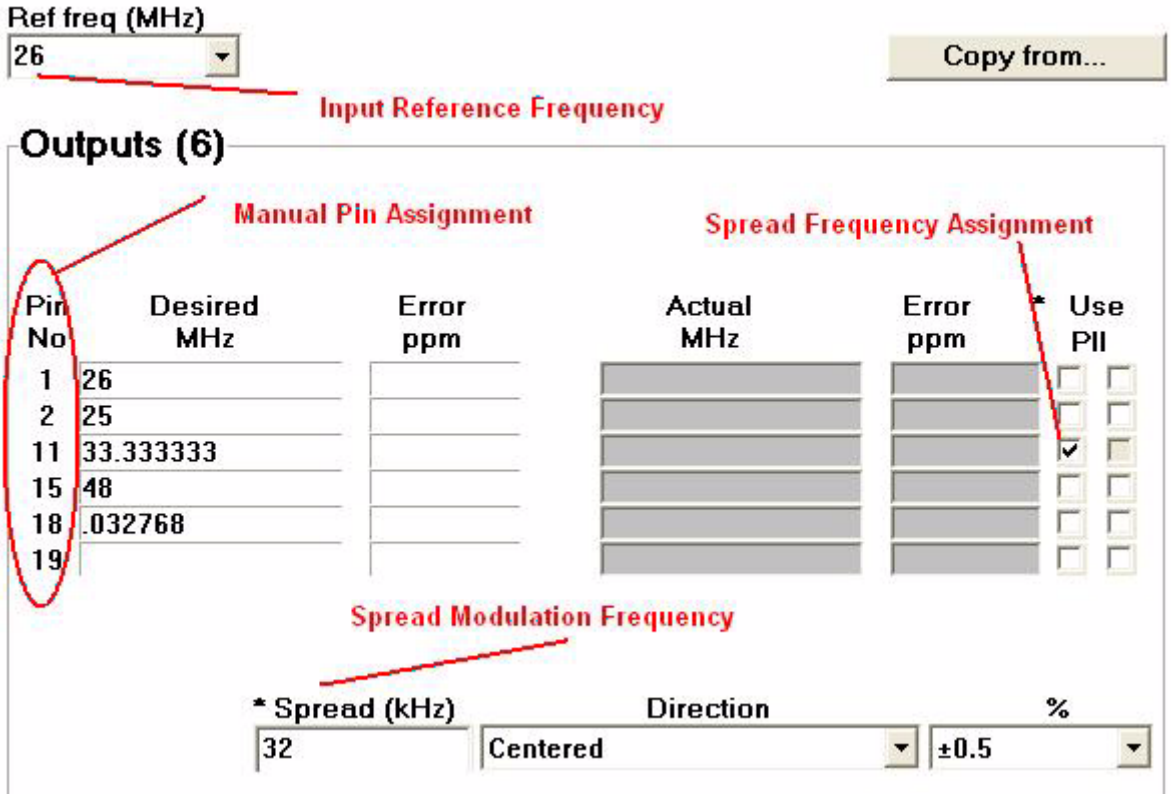
For differential outputs, a pair of identical target output frequencies must be set. The Versaclock software will arrange identical outputs on low skew output pairs. LVDS differential outputs are set in Detail View mode by selecting the Output Configuration pull down setting (VersaClock III parts), or selecting the LVDS ON radio button (VersaClock LP parts). (See Detail View section for additional information.)

Spread Spectrum

Spread Spectrum is a technique whereby the output frequency is modulated to minimize the system noise energy associated with the clocking of data around the system. This noise energy may generate radio frequency interference with other electronic devices and is a key component of U.S. FCC certification.

VersaClock III and LP parts have PLLs that support spread spectrum modulation. In devices with multiple Spread Spectrum PLL support, the software allows each configurations to be specified. The modulation rate, direction and amplitude may be set for Spread A and/or Spread B. Multiple output frequencies may be supported by a single spread PLL if the frequencies are integer divides of the respective PLL VCO frequency. If non-related frequencies are selected, then both PLLs will use the same modulation configuration at different VCO frequencies.

All output frequencies that are generated from the same PLL will have the same modulation rate, direction and modulation amplitude.



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a) Spread Modulation Rate

When selecting spread spectrum, the user has the option to input frequencies between 30 kHz and 120 kHz modulation rate. The PCI specification specifies that spread spectrum modulation must be between 31 and 33 kHz. For other applications, other modulation rates may be chosen.

A consideration for selecting the 32 kHz modulation rate is whether there is a “down stream” PLL or Zero Delay Buffer (ZDB) that the clock is driving. The PLL bandwidth being driven must be at least 20 times the modulation frequency. Faster modulation rates are more difficult for PLLs to track.

120 kHz modulation has been measured to provide approximately 25% additional EMI attenuation compared to 32 kHz at the same modulation amplitude. As previously stated, this is not always permissible in the system.

b) Center Spread

The frequency spread is distributed evenly, in both the positive and negative directions from the target output clock frequency. The average frequency, in this type of spread spectrum operation, is the same as the target frequency. Selection of the center spread percentage is defined as the deviation in both the positive and negative directions. The total spread excursion is 2x the selected value. (I.e. ±1% has a total spread deviation of 2%.)

c) Down Spread

Some systems cannot tolerate clock frequencies that exceed a target frequency. For example, some processor ICs are rated at a maximum operation frequency. Down spread reduces the target frequency such that with spread spectrum enabled, the maximum frequency generated (at the maximum, positive excursion from the new center frequency) is at or below the specified output clock frequency. Down spread reduces the average system clock frequency from the target frequency. The total spread excursion is equal to the selected spread percentage value.

PCIe specifies that a maximum of -0.5% spread may be used. This means that a center frequency offset of -0.25% is necessary.

d) Selecting Spread Spectrum Outputs

Once the Spread Spectrum direction, modulation rate, and percentage deviation are selected for either Spread A or Spread B, the outputs that will be modulated must be selected.

Modulation amounts may be assigned to frequencies by checking the radio boxes to the right of the target frequency. Select the radio button for the target frequency under A to enact spread configuration A. Similarly, the radio button selection under B will assign spread configuration B. Multiple output frequencies can share the same spread configuration, if the frequencies can be generated by a single PLL. (I.e. 100MHz and 25MHz can be generated from a single PLL, so spread spectrum applied to both of these frequencies will have the same amplitude and modulation rate specified.)

If multiple frequencies are selected for a given spread spectrum amount, and they cannot be generated from a single PLL, then both PLLs will be used to generate the given spread spectrum modulation.

Manual Pin Assignment

Manual pin assignment is accessible from the Options menu (Option > Manual Pin Assignment or ALT+M). Selecting Manual Pin Assignment will reset any present solution. Manual Pin Assignment is a toggled feature and may be turned on/off as desired.

When selecting Manual Pin Assignment, pin numbers are shown to the left of the frequency input fields. For configurations that require differential outputs, it is easiest to use Manual Pin Assignment to get both clock outputs on a differential pair. Check the specific device datasheet to see which outputs may be set as a differential pair.

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Configuration Tabs

Individual configurations may be inspected and edited by selecting the Configuration Tabs across the top of the input field.

Reset and Calculate buttons in the bottom left corner will clear and calculate only the configuration in view. Configurations are calculated independently. Go to All Configuration View to manipulate an entire part.

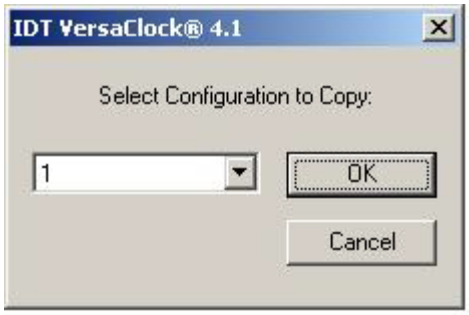
For each configuration address, a solution must be calculated individually. Only the address currently viewed will be calculated. (**Note**: If you change the Reference Frequency in one configuration, you must recalculate all configurations for the new frequency input setting.)

Copying Configurations

The contents of a configuration may be copied to another to maintain output pin assignments between configurations.

First, go to the target register into which you wish to copy.

Second, from the Options menu, select “Copy Register”. A window will open requesting that you select the register address *from* which menu you wish to copy. Select “OK” to enact the copy. (You can also use Options Copy or ALT-C to enact this function).



(**Tip**: The addition of Spread Spectrum to a previously calculated configuration automatically forces the entire solution to be recalculated. If the target device has configurations with Spread Spectrum turned on and similar outputs with Spread Spectrum off, you MUST calculate a Spread Spectrum ON configuration first, to establish the initial pin assignment. Not every PLL supports Spread Spectrum. Allocating the PLLs for the “worst case” requirement should be done first. You may start calculations on any configuration. It is not necessary to start with Configuration 0.)

Calculate Configuration - Solution Interpretation

Once you have entered the target configurations, the VersaClock software will automatically optimize the configuration by pressing the Calculate button on the lower left corner of the window.

When the calculation is complete, each successful synthesized output will show up with the pin number to the left of the frequency entry, as well as the actual frequency, error ppm and a graded color bar graph for each output.

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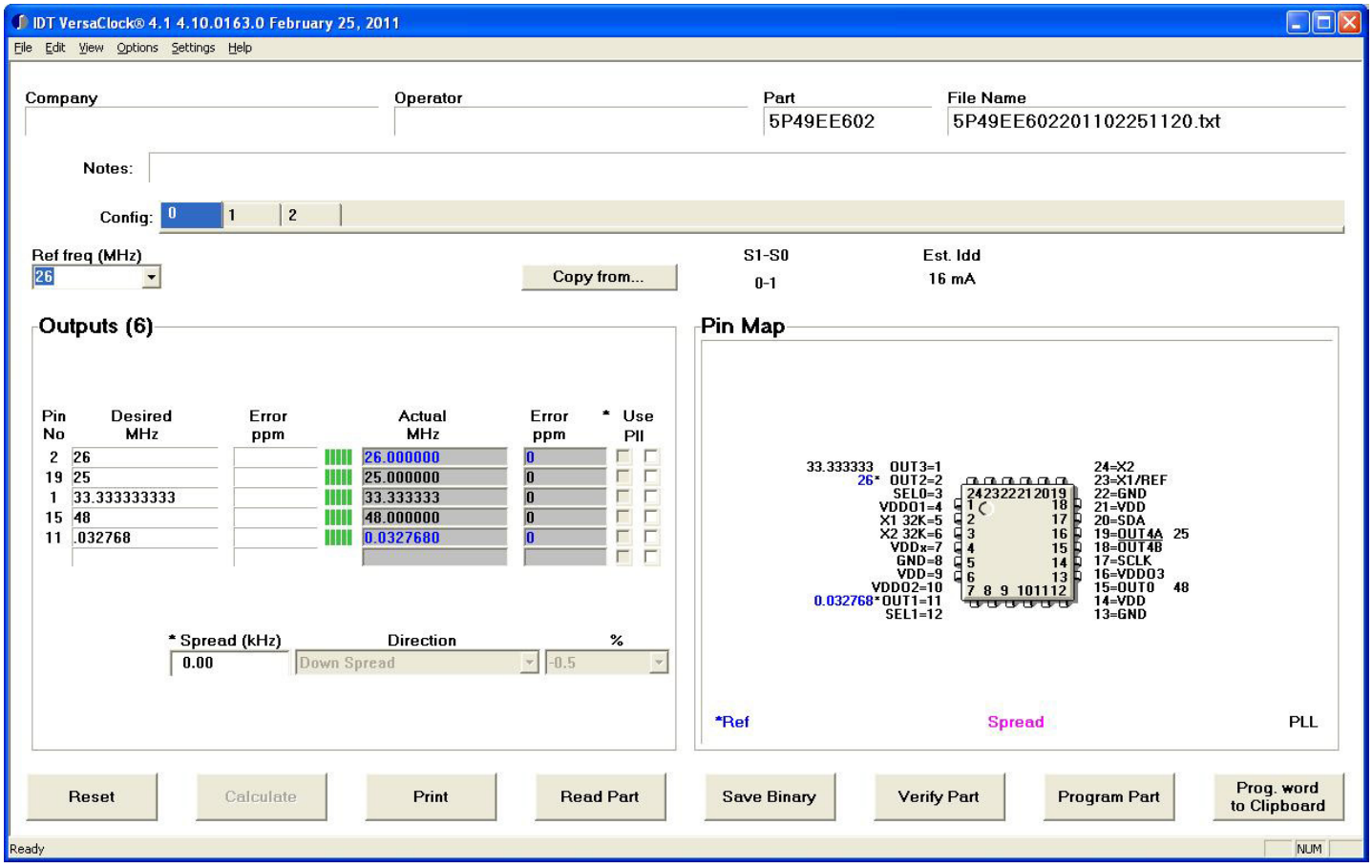

Actual Frequency Output

For both the Single Register and All Register Views, each target output, if a solution exists, will be displayed in a grayed box with the associated accuracy error. If Spread Spectrum is applied to an output, the accuracy will be noted as “Spread”. (Note: The minimum Spread value - 0.5% - is equivalent to 5000 ppm. The target center frequency of a Spread output will be within the stated desired accuracy.)

Solutions may not be available for a variety of reasons. Examples are: 1) no solution with equal or better accuracy to specified target frequency; 2) inadequate chip resources to support target frequency.

(Tip: If no solution is found for a target output, try widening the allowable accuracy error until a solution is provided. If this does not provide a solution, check to see if the number of discrete output frequencies (excluding direct reference frequency outputs) is greater than the number of PLLs provided on the selected part.)

(**Note**: For Output Clocks that are a buffer Reference Frequency output, the frequency on the Pin Map will be written in **Blue** and have an asterisk. For Output Clocks that have Spread Spectrum applied, the frequency will be written in **Magenta**. All non-spread, synthesized clock outputs will be written in black.)

The calculator optimizes the target frequency outputs for a given input. Occasionally, the calculator is unable to find a solution within the specified tolerance. This may be due to:

- Greater ppm error than specified for target frequency. Error PPM will specify minimum accuracy needed to obtain a solution (i.e. 5+ indicates that the Target Error PPM must be >= 5). Change the Error PPM value and recalculate.
- No Available Resources. When more non-related output frequencies are specified than the individual part may support at the same time, the Error PPM will provide a N/A (not available) notation. This occurs when, for example, 5 unrelated frequencies are targeted for a 3 PLL device. The user must then prioritize which frequencies are most

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important and omit the remainders, or increase the target Error PPM or change the target frequency, in the hope of being able to create an integer divisor of one of the existing PLL frequencies.

In the example above, notice that the target output of 24.576 MHz did not have a 0 ppm synthesis solution. The nearest solution is 4 ppm away. A minimum of 4 ppm Error target must be inserted for the output to find a solution. Only outputs that previously had no solution will be calculated.

Grade

After calculating in Single Configuration View Mode, grade attributes are displayed for each output frequency solution.

Each frequency solution will be given a 1- to 5-bar “grade” of how well the output frequency jitter performance can be anticipated for the configuration. The bar grade provided is not an absolute value, rather a relative strength within the PLL's operating parameters.

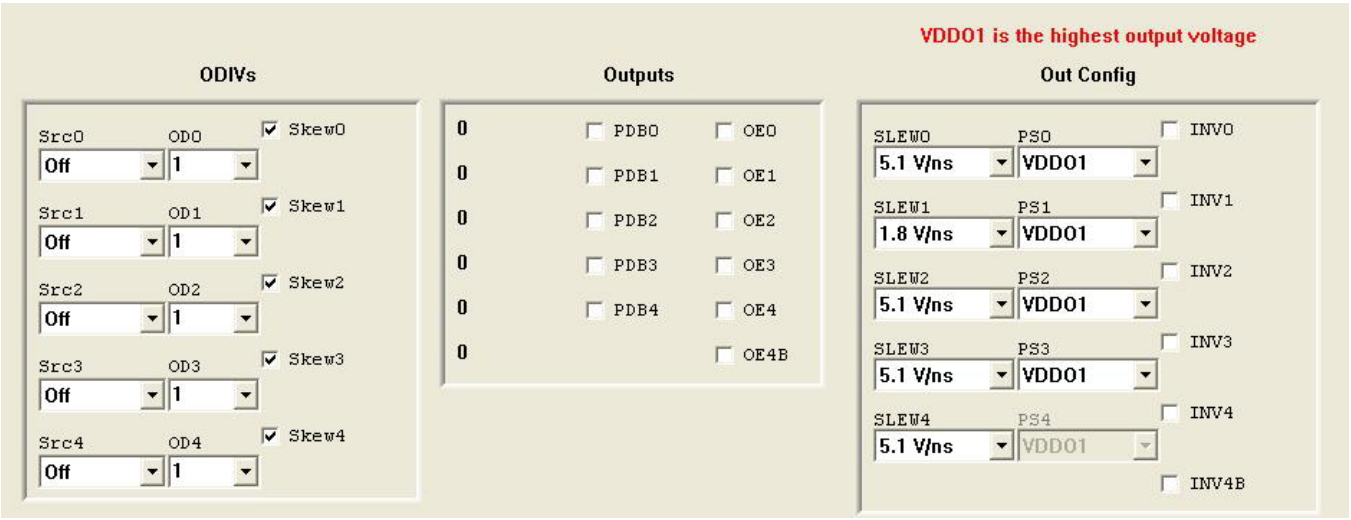
- 1-Bar - indicates that the PLL will operate at minimum performance criteria
- 3-Bars - indicates the PLL operates within the mid-range of operating criteria. Clock output performance will be suitable for most applications
- 5-Bars - indicates that the PLL is maximized for all parameters. This is the best solution.

Tip: To increase the performance grade for a given clock output, increase the allowable Error PPM. By widening the accuracy requirement, more solutions will become available. Within each accuracy requirement, the best jitter performance will be selected for each individual clock output.

Setting VDDO Voltage for Each Output (VersaClock LP devices only)

Although all of the output frequencies have been set in the single configuration view, the user still needs to go to the Detail view to set which voltage level each output will be connected. To minimize the interaction between the various output frequencies, it is advised to spread the output frequencies across the available VDDO pins. For example, for an 8 output device that has 3 VDDO pins, you should not have more than 3 or 4 outputs connected to an individual VDDO.

Output slew rates may also be set according to the VDDO voltage, output frequency and requirements of the device being driven. Slew rates for all outputs may be set at maximum levels for all VDDO voltage settings. Slower slew rates may be used for lower output frequencies operating a higher output voltage. 1.8V and 2.5V outputs should always use the fastest slew rate setting.



Save Binary

This button allows conversion of the VersaClock 4.1 session file into an Intel compatible hexidecimal format for

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production programming. The default extension for this file is *.hex. This format is used by third party programmers. (Note: Using this function does not produce a session file for later modification. Session files should be saved using Menu > File > Save As)

Verify Part

When connected to an IDT VersaClock evaluation board, selecting this button will read back the configuration of all registers of a programmed part and compare them to the hexadecimal value of the loaded file.

Read Part

When connected to an IDT VersaClock evaluation board, selecting this button will allow the software to upload the contents of a known programmed part. This will allow the configuration of additional parts with the same code. Because there is no input reference frequency, the VersaClock software will not be able to provide information on the configuration of the part. You will need to contact IDT Marketing to get information about how the part was configured.

(Note: You must first select the proper new part from the parts selection menu - File > New.)

Program Part

When connected directly to an IDT VersaClock evaluation board. Selecting this button will directly program the identified part. No exporting configuration files to another software applications is required.

If no evaluation board is available, or programmer socket is empty, selecting this button will return a message telling you that you need to take appropriate action before attempting to program a device.

Single Register View Only

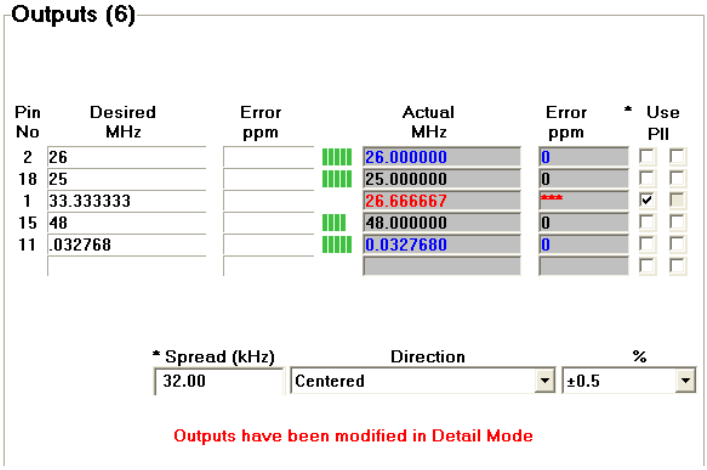
Solution Pin Map

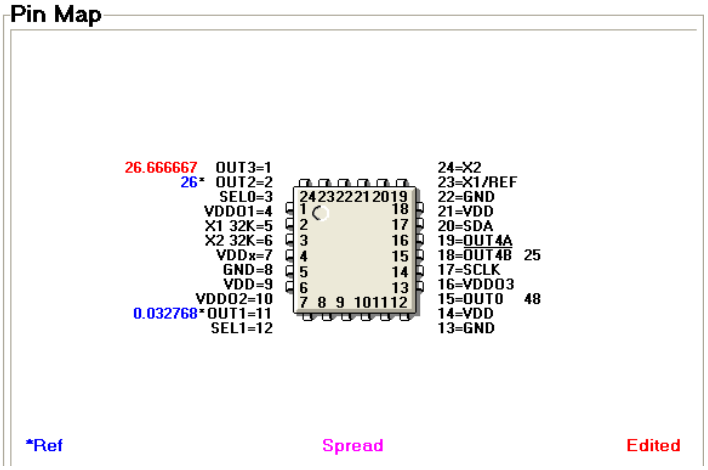
Upon completion of solution calculation, a description of each device pin is provided. The pin map displays the actual frequencies corresponding to that register address.

Frequencies that are the buffered reference frequency will be displayed in **Blue**.

Frequencies that have Spread Spectrum applied are displayed on the pin map in **Magenta**.

Outputs that have been modified in the Detail View will be displayed in both the Actual Frequency and Pin Map in **Red**. (VersaClock LP devices only).





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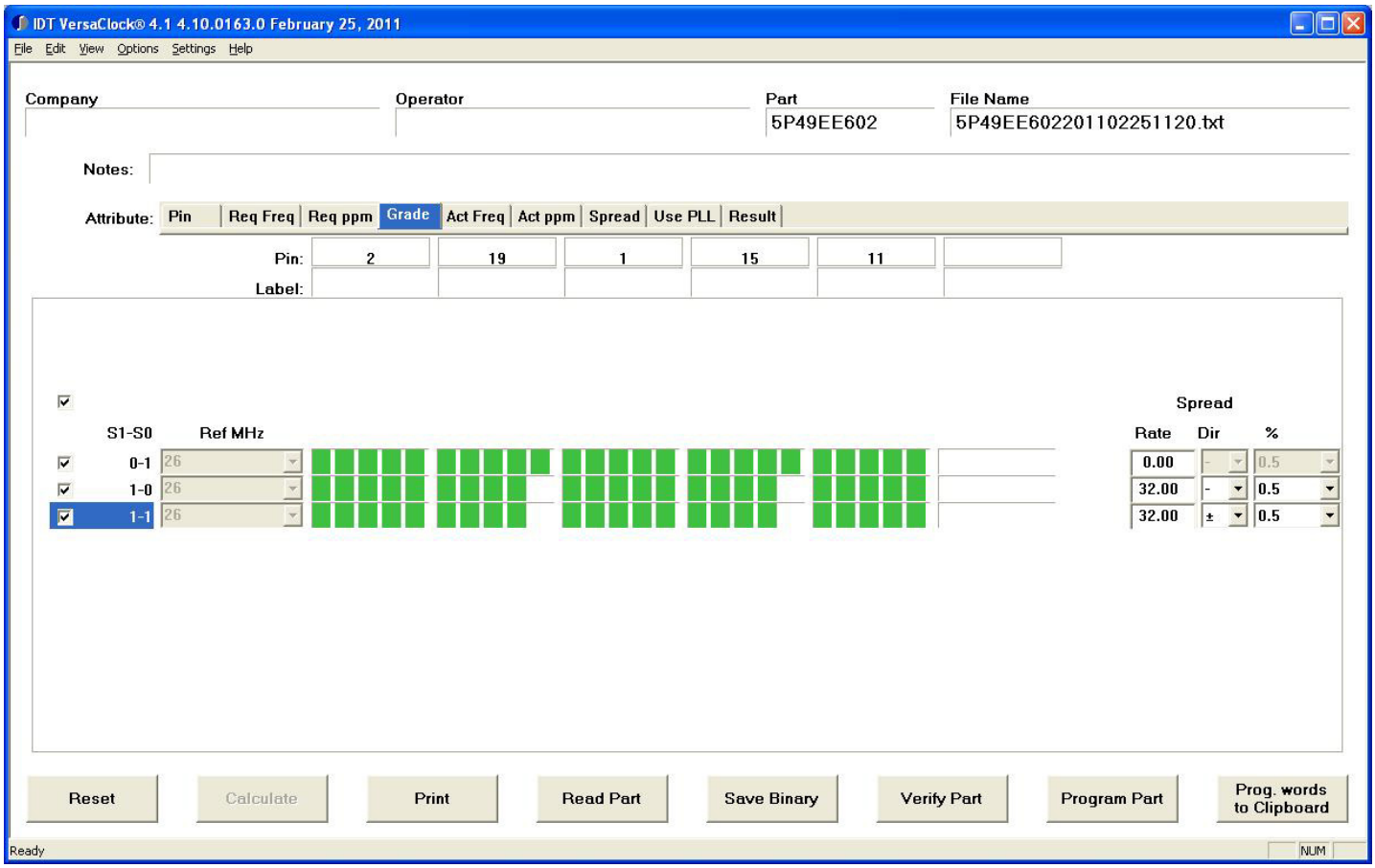
All Configurations View

Inserting Data



Fields that are accessible to the user are in white. The user can include text information in the Company, Operator and Notes fields for reference. While the program is operating, the Company and Operator fields will default to the last session's values.

The Configuration that is being modified and the Attribute that is active will be highlighted. This allows you to focus on the proper information to be entered. Make sure that the entries for each Attribute aligns in the matrix with the target frequency.

Attributes Tabs

Each of the attributes that were described above in single configuration view have their own tab to readily allow the configuration of the entire device. To keep frequency/pin assignments more manageable, individual pin labels are available in this mode, to allow attributes to be assigned without having the actual frequency displayed.

a) Pin - Unassigned prior to the calculation unless the Manual Pin Assignment Option is applied in the Options pull down menu.

b) Req. Freq - Target frequency to be synthesized.

c) Req. ppm - Accuracy tolerance window permissible for target frequency.

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For each target output frequency, the user has the ability to specify the maximum tolerable output clock synthesis error in ppm (parts per million). This is the frequency error additive to the error of the reference input. If no value is included, the default is zero. This is particularly helpful in cases where the input reference frequency does not allow, or gives poor solutions for 0 ppm accuracy.

The software will provide the best performance solution within the given accuracy tolerance window. To achieve improved jitter performance, the window must be widened.

Entering positive numbers - the accuracy window is the absolute value (+ and - ppm error values will be considered)

Entering negative numbers - only frequencies lower than target frequency are considered.

The ppm accuracy has an upper bound of 9999, but the user should not exceed the deviations allowed by the user's system. While higher accuracy solutions may be achievable, a less accurate solution (within designated bounds) may be selected by the software, due to performance criteria.

d) Grade - Solution rating from 1 red bar to 5 green bars for each target output. (See discussion on page 13)

e) Act. Freq - Solution actual output frequency calculated.

g) Act. ppm - Solution actual ppm accuracy of actual frequency from target.

h) Spread - Check box to turn on Spread Spectrum capability for target output.

i) Use PLL - Check box forces an output to be synthesized, rather than using a buffered, reference output. For outputs that must be synthesized, checking this box will not affect the output.

j) Result - The estimated current consumption (Idd) and Spread Spectrum modulation rate (where applicable).

Manual Pin Assignment

a) Manual pin assignment is accessible from the Options menu. Selecting Manual Pin Assignment will reset any present solution. Manual Pin Assignment is a toggled feature and may be turned on/off as desired.

b) With this feature turned on, target outputs be inserted in the field aligned to the pin number column.

Note: Spread Spectrum may not be available to all synthesized outputs. To modulate multiple frequencies, there must be a common PLL VCO frequency that is an integer multiple of all of the target frequencies. The Spread Spectrum magnitude percentage and direction will be the same for all outputs

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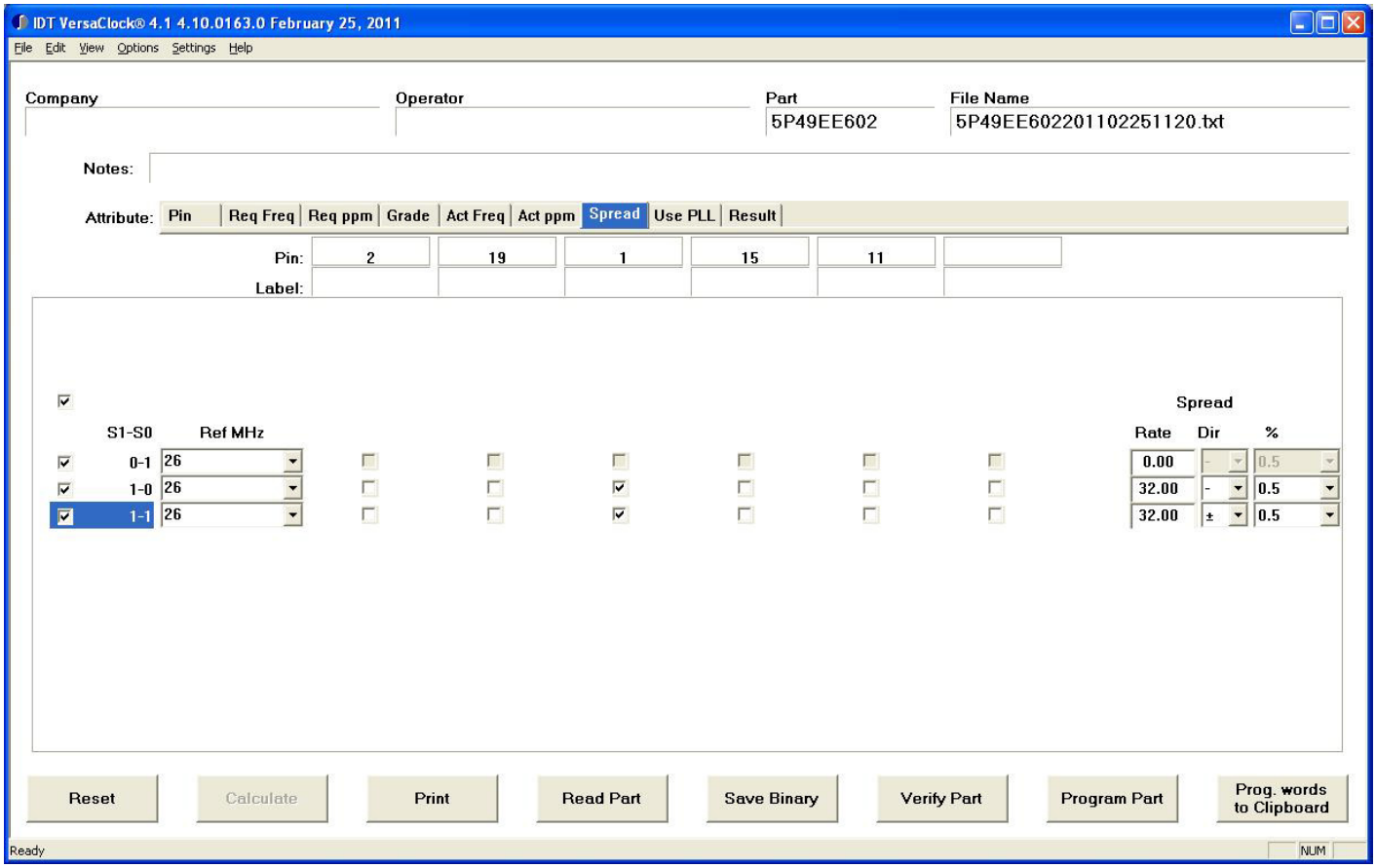
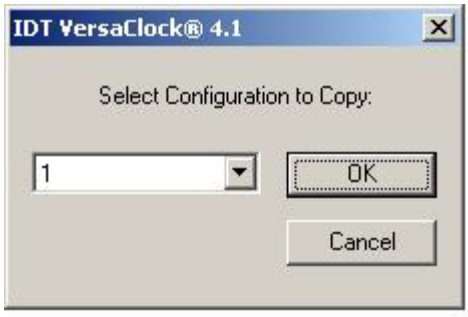


Copy Configuration

Calculated or un-calculated register configurations may be copied to other registers to facilitate the population of the target matrix.

To do so, you must first go to the address you wish to copy to. Clicking on the address or one of the target fields in that register, you will switch the focus to the register. In the example above, the address 0-1-1 is highlighted in blue.

Selecting Options > Copy Configuration (or ALT-C) displays a window that allows you to select the source register from which to copy.



The pull down menu allows the copying of any register to the target register. You do not need to go in any specific order.

Once copied, any field may be edited prior to configuration calculation.

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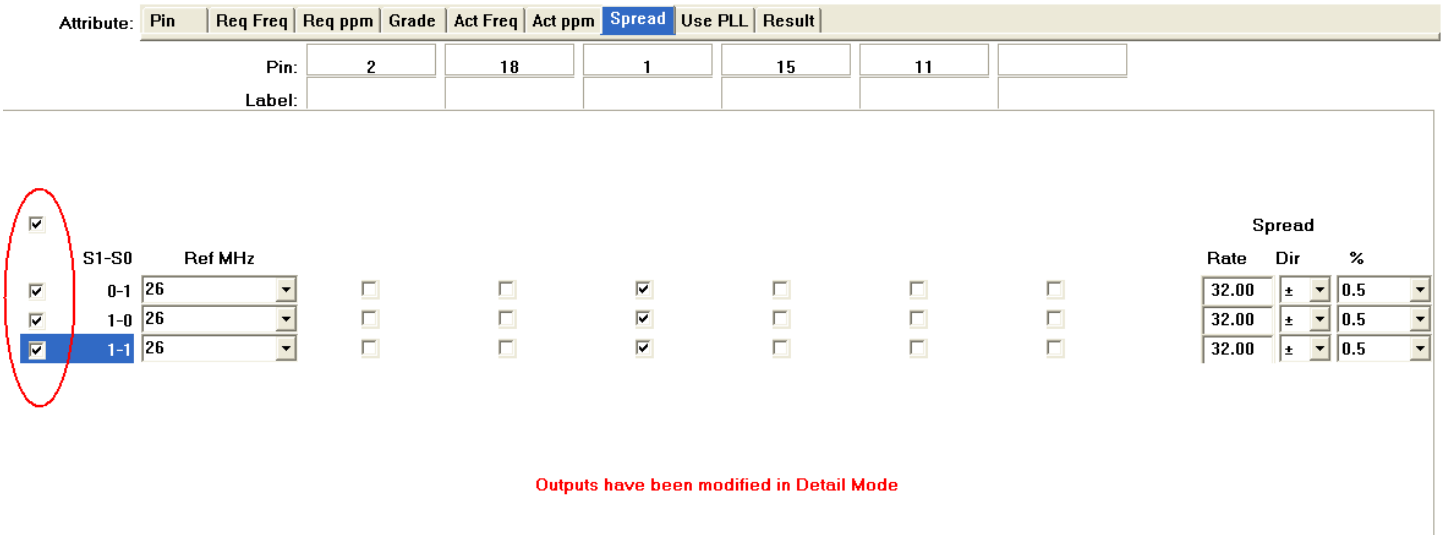
Calculation Reset



One or multiple registers can be Reset and Recalculated.

Registers with the box next to the address checked (seen above, circled in red) will be reset when the Reset button on the bottom left is selected. A master select (above the individual address select boxes) will select/reselect all register selects simultaneously.

Calculate Solution

Pressing the Calculate button in the lower left corner will calculate all selected registers together, to insure proper pin alignment between registers. Whether using Manual Pin Assignment or not, the outputs in a given column will appear on the same output pin for the specified register address.

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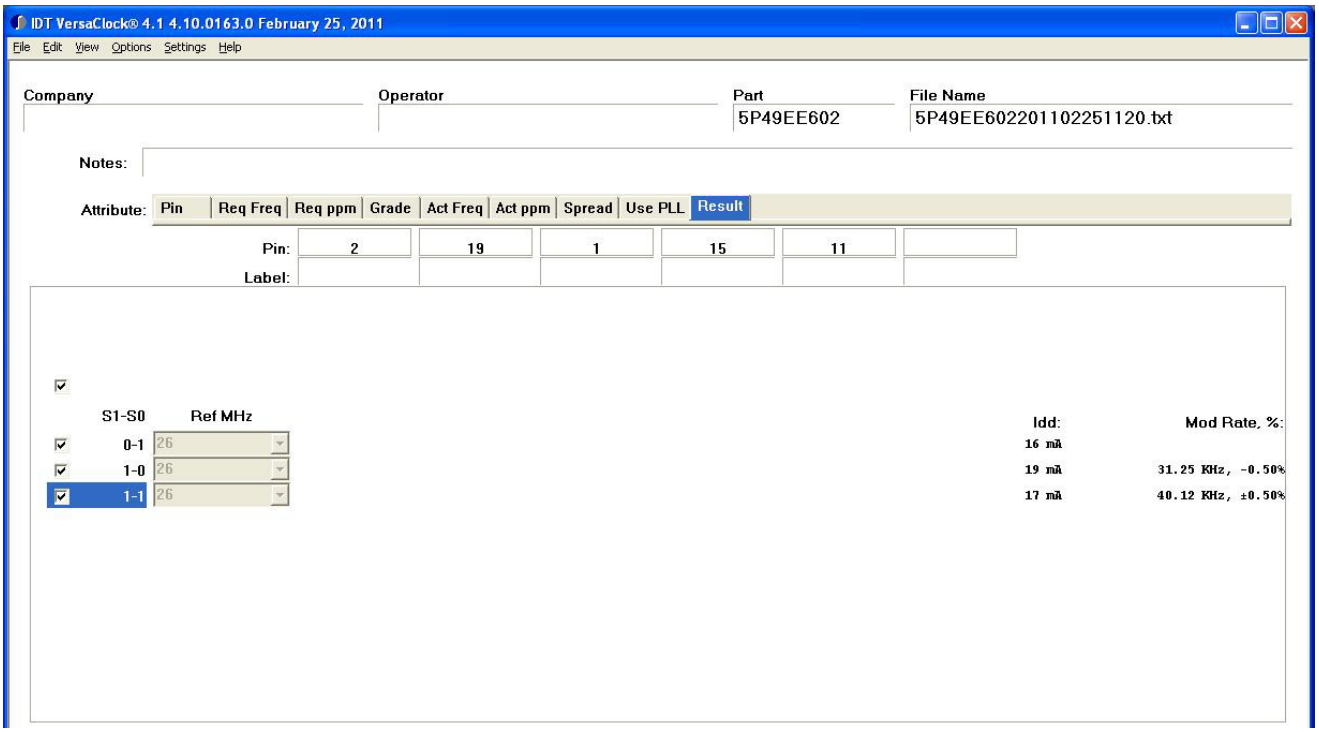
Results Tab



a) Estimated Idd

For the individual register configuration - including reference input value and all outputs - the estimated Idd has been characterized to be within 20% of the actual value.

b) Spread Spectrum Modulation Rate

For outputs with Spread Spectrum selected, the modulation frequency will be displayed. Typically, the modulation rate will be in the 31-33 kHz range, but may be substantially higher (above 40 kHz) for output frequencies above 125 MHz.

Outputs Turned Off - For registers with no target outputs, calculating in All Register View mode will automatically turn off unused registers. Address assertions to these registers will have all PLLs and outputs turned off.

For Register View mode, each unused register must be individually calculated to turn off outputs and set PLLs off. If this is not done, then these registers will remain in a non-programmed state.

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Detail View

The device is set up as functional blocks, that are separated into individual configuration tabs. All configurations are displayed in translated values. No binary translation or look-up tables are required.

Each editable function is activated when the mouse is clicked directly on the attribute. A pull-down menu of allowable options is then displayed. Allowed values may also be typed into the highlighted parameter. To allow quicker editing, function blocks that are highlighted are color coded and matched with all other components that point in sequence from input to output. Calculations are automatic, when a setting is changed. PLL loop filter values instantly reflect any setting within the PLL block.

All settings that are established in Single Configuration or All Configuration Views may be edited. However, once edited in Detail View, the calculated outputs may not be updated in the other two views. A warning in **RED**, in both the Single Configuration and All Configuration views will alert the user that output frequencies may be changed from the initial automated configuration. For configurations that are generated completely in Detail View, no configuration information will be displayed in either the Single or All Configuration views.

Configuration works best from left to right, with the Common block feeding the PLL block, into the ODIV (output divide) block. The OUT Config directs each of the output frequencies to a target output pin and provides the ability to set slew rate, inversion and any output enable or output suspend control desired.

Each of the six configurations may be modified separately except the Common and Output Configurations, that are configured once for the entire device.

Input/Common Block

Functions that affect all PLLs together. This includes crystal/clock selection and hardware/software control switches. There are differing functions for each device family. Consult individual datasheets for additional details.

For VersaClock III:

PrimClock - Selects input as either Crystal/REFIN (0) or CLKIN (1).

VCXO Gain and Offset - see datasheet for details

SM (clock source switch mode) - Revertive, Manual 0 or Manual 1. Selection of how the device interacts between multiple clock inputs when the primary clock disappears. Manual 0 selects Crystal/REFIN

For VersaClock LP:

32K Cap 1 and 2 - Sets the capacitive load for 32kHz crystal (for parts that have 32kHz crystal support only).

Xtal_Active_Low and 32K_Active_Low - Powers off the respective crystal oscillator circuit for additional power reduction. A checked radio button indicates that the oscillator has been turned off.

No PD - For SEL[1:0] =00, checking the radio button will keep the 32kHz oscillator and outputs active (sleep mode). Un-checking the radio button, the device will be in complete power down, with all outputs and PLLs turned off.

PLL Block

Each PLL has controls for input source, reference divide, feedback divide (and fractional divide, where applicable), PLL loop filter parameters, as well as spread spectrum modulation. Each is displayed in graphical terms, with multi-function inputs (drop down and keyed input). With the reference divide at set at 0 (zero) or PDPLL# checked, the entire PLL will be powered down.

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Input Source - MUX setting allows you to select what clock source is driving the PLL. This may be either a MHz crystal or clock, a 32.768kHz crystal or the output divide from another PLL. Each PLL may have different capabilities, so please check the specific part datasheet or the Detail View selection options.

(Note: For those devices that support 32.768 kHz PLL reference, the long term jitter is only appropriate for DSPs or processor device support but will have lower power consumption and allow the TCXO and MHz crystal oscillator to be turned off. The user may find that although the short term jitter is very low (200-300ps), the long term jitter (10000 cycle) will be in the microsecond range. The PLL update, or correction is only once every 32.768kHz period, so the loop may wander significantly more than PLLs utilizing a MHz reference input. PLL C has a second Feedback Divide (FB2) to get the VCO frequency into normal operating range.)

Reference Divide - divider that sets the PLL phase detect update rate. For lowest jitter performance, minimize the reference divide. This will provide highest PLL update rate. Try to keep the phase detection frequency as high as possible, and above 200kHz, if possible.

Feedback Divide - divider that sets the PLL VCO frequency. Higher VCO frequencies produce lower jitter outputs. Also, higher VCO frequencies consume more power. For low power operation, you will need to monitor VCO as a trade off between jitter performance and power consumption. For PLLs with fractional divide capability, check with the equation in the product datasheet.

PLL Loop Parameters - charge pump, zero resistor and zero capacitor settings, along with the phase detection frequency, set the loop bandwidth, damping factor and phase margin (stability) of the PLL. Whenever a parameter is changed in the PLL block, the loop bandwidth, damping factor and phase margin are automatically recalculated to provide the user feedback on loop performance.

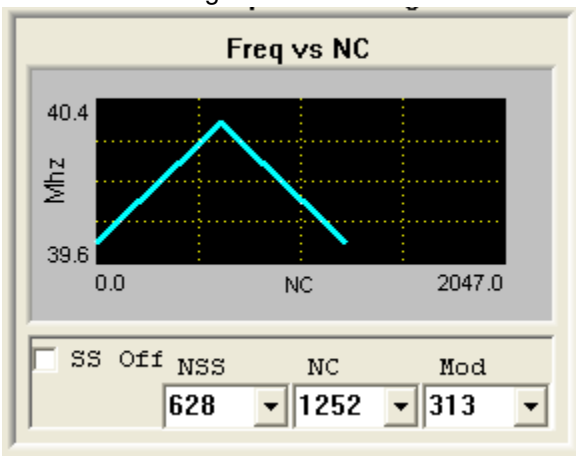
Loop Bandwidth - loop filter 3dB frequency bandwidth in kHz. Frequencies below this value will be filtered out. A calculation is provided for Phase Detect/Bandwidth (PD/BW). This needs to be above 10. For Spread Spectrum enabled operation, the bandwidth needs to be set a decade lower than the spread modulation frequency.

Damping Factor - loop responsiveness. Critical damping value is 0.707. This parameter should be set as close to critical damping as possible while maintaining the target phase detect/loop bandwidth ratio.

Phase Margin - loop stability. Should have a value above 45 degrees.

Spread Spectrum - spread loop configuration on PLLs that support this functionality. There are several different spread spectrum architectures used in these family of parts, so please check the datasheet for details relating to the calculation of parameter settings. For each spread modulation, there will be a graph to depict the parameter effect.

For VersaClock LP devices, the spread modulation in video applications would have the number of clock cycles per horizontal synch (NC) as the modulation period to eliminate screen artifacts. NC and MOD need to be solved for integer values, while NSS may be rounded to the nearest integer.



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Output Divide (ODIV) Blocks

The 7 output source MUXes (SRC0 - SRC8) can be configured to have one of the following inputs: 1) the reference clock (device input frequency - either MHz input or 32kHz crystal frequencies on those parts that support that function); 2) any of the 4 PLLs; or 3) another output (PM), so that differential pairs can be generated (VersaClock III only).

Each of these MUXes is joined to a dedicated Output Divide and output in a series. [Please note that each VersaClock III Output Divide goes through an external /2.]

To activate the MUX, change the source from off. A setting of “off” powers down the MUX.

As each output source MUX is activated, it will become color coded with the PLL source it is connected. This is to clarify how each PLL clock is connected to corresponding outputs.

As the output stream is established with an operating PLL or reference clock input, an output frequency is calculated and displayed in the OUTPUTs box to the right. You can dynamically configure and check your target frequency on the screen.

To obtain low skew pairs (in VersaClock III devices), for OUT1/OUT2 pair, set S1=PM2. SRC1 path will be ignored. Similarly, for OUT3/OUT6 pair, set S3-PM6. SRC3 path will be ignored.

OUTPUTs

This is a calculated display for each of the frequencies available to the various output pins. All frequencies are in MHz. Configuration of the PLLs, MUXes and ODIV blocks are reflected in these frequencies. If a number is in RED, then the frequency is out of range.

OUT Config Block - Setting Differential Outputs

This block allows control of the output standard for each clock output pin. Outputs have characteristics that are treated individually and in pairs.

VersaClock LP Parts - configure differential pairs by selecting LVDS ON check box for OUT4/OUT4B. One of the corresponding outputs must be inverted (INV).

VersaClock III Parts - configure output pairs (OUT1/OUT2, OUT3/OUT6, OUT4/OUT4B and/or OUT5/OUT5B); set corresponding LVL# to desired LVDS, LVPECL or HCSL; invert one of the corresponding outputs (INV) and check Common Mode Enable (CMEN) radio button for LVDS outputs only.

Differential outputs pairs need to insure that a phase relationship is maintained. This can only be assured if both signals are generated from the same output divide. For OUT4/OUT4B and OUT5/OUT5B, this is not an issue, since both output pairs are hard configured as output pairs. For OUT1/OUT2 output pair, set S1=PM2. This will drive the OUT1 to have the same output divide as OUT2. Similarly, for OUT3/OUT6, set S3=PM6.

Output Enable (OEM) allows the corresponding outputs to be set to tri-state, park high or park low states when the corresponding output is disabled.

Other characteristics may be individually set, such as slew rate (SLEW), 180 degree clock inversion (INV), output enable (OE) and power down output (PDB).

Clock Output Power Setting (VersaClock LP only)

Each output may be set to the different VDDOs on the device. Look at the corresponding datasheet to determine if the part in question has any limitations. Each output must have a VDDO specified, or else the output will be powered down.

Additional Functions

Save Binary

This button allows conversion of the VersaClock 4.1 session file into an Intel compatible hexidecimal format for production programming. The default extension for this file is *.hex. This format is used by third party programmers.

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Verify Part

When connected to a VersaClock LP or III evaluation board, selecting this button will read back the configuration of all registers of a programmed part and compare them to the hexadecimal value of the loaded file.

Read Part

When connected to a VersaClock LP or III evaluation board, selecting this button will allow the software to upload the contents of a known programmed part. This will allow the configuration of additional parts with the same code. Because there is no input reference frequency, the VersaClock software will not be able to provide information on the configuration of the part. You will need to contact IDT Marketing to get information about how the part was configured.

(Note: You must first select the proper new part from the parts selection menu - File > New.)

Program Part

When connected directly to an IDT VersaClock LP or III evaluation board, selecting this button will directly program the identified part. No exporting configuration files to another software applications is required.

If no programmer is available, or programmer socket is empty, selecting this button will return a message telling you that you need to take appropriate action before attempting to program a device.

Saving Solution

Multi-session programming (for direct use with IDT VersaClock LP evaluation board)

Device configurations may be saved into a uniquely named file for multi-session development. The “Program Chip” button will directly program the configuration into the chip on the IDT VersaClock evaluation board.

File Default Naming, File Default Annotation

All files default to a unique file name - the device number (I.e. IDT5P49EE601) and the date code in the format YYYYMMDDHHMM. An example is IDT5P49EE601201003011342 for a configuration first developed on 1 March 2010 at 1:42pm.

Annotations may be included in file, such as Company Name, Operator and other notes. Company Name and Operator used in a session will be the default of following session, as long as software is in use.

Returning to a Saved Solution

From Startup screen (see Image 1 on Page 4), select the Prior Session button to open a saved solution from a previous session. The saved solution will let the software know what part type was in use.

You may also return to a saved solution by selecting any part type from the Startup > Open screen, and selecting the desired file from the File Menu in the calculator workspace.

Programming a Device

First Time Setup

You will need to set up the Port connection to directly program the clock circuit from the software. When a VersaClock USB evaluation board is plugged into the computer’s USB port, either the software will acknowledge the type of evaluation board available in the programmer port selection - either VersaClock III or VersaClockLP will show up as the only port option. Make sure that this is selected. Nothing additional needs to be done.

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A pop-up window will appear for you to select the appropriate port from the pull down menu.

Programming the Device

When the device configuration is completed and calculated for the desired registers, select the Program Chip button in the bottom right corner. A message will be displayed when the transmission is successfully completed.

(**Note**: The software will notify the user when the programmer is not connected to the port and when the power to the programmer is not on.)

Device Program Verification

Once the device has been programmed, verify that it has been programmed correctly. With the device in the socket, select the “Verify Chip” button in the lower right side of the VersaClock window. If the device is exactly the same code as exists in all available registers, then a positive confirmation will be returned. If any single bit is incorrect, in any of the registers, then a negative response will be displayed.

Using with Total Phase Aardvark™ I²C/SPI Host Adapter

In order to use VersaClock 4.1 with a Total Phase Aardvark Host Adapter, download latest Aardvark Windows USB driver (version 2.02) and make sure that adapter is using the latest firmware (version 3.50).

Driver software available at http://www.totalphase.com/support/product/aardvark_i2cspi/

Install driver software and plug in Aardvark Host Adapter to USB port. Follow all installation instructions.

From VersaClock software application screen, open Menu Settings>Select Port... An Aardvark Port option should become available.

Connect Aardvark parallel ribbon cable to target device I^2C socket.

Select Program Part button on lower right corner of screen. Direct programming is now acheived through the Aardvark hardware.

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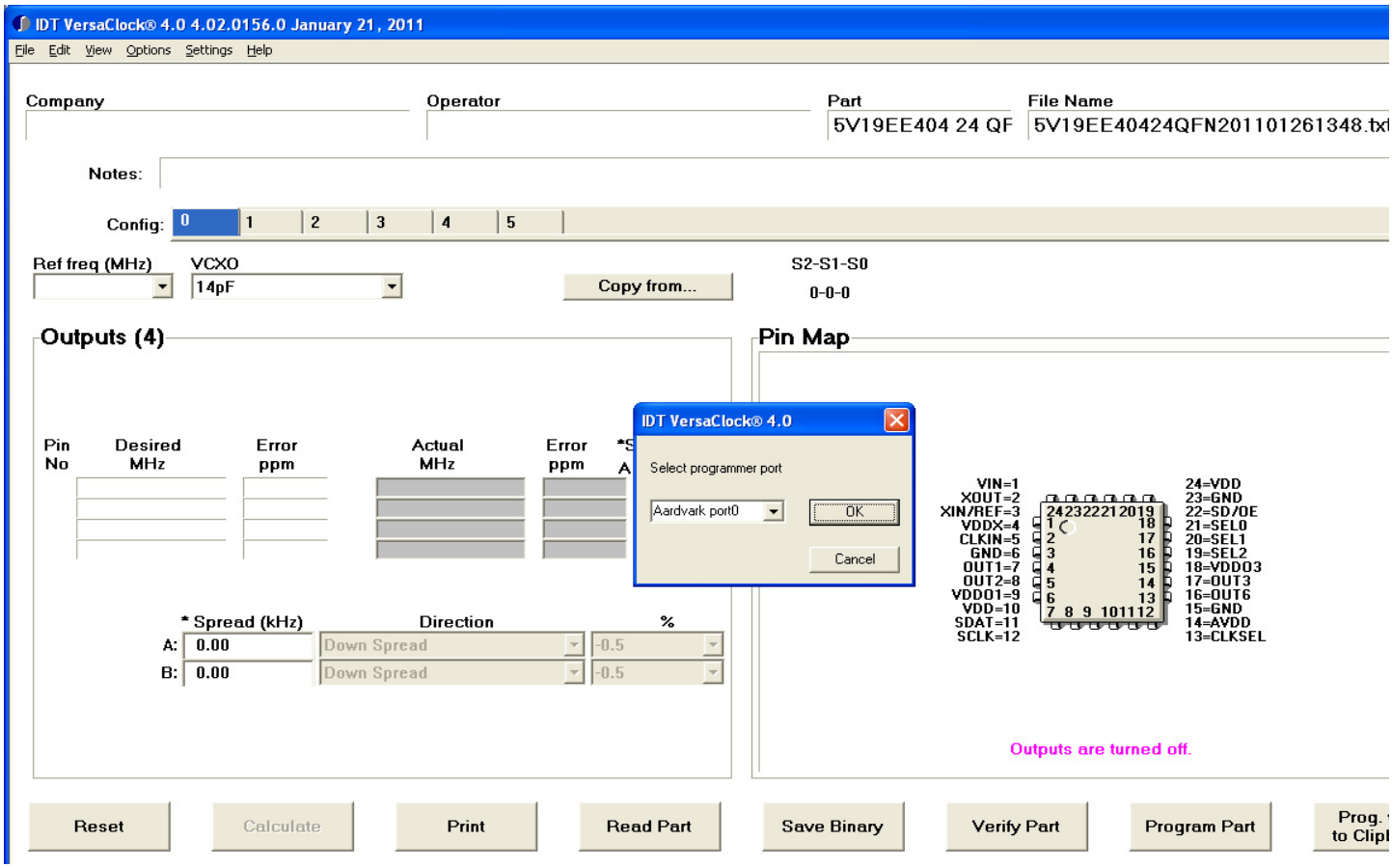
Verify Part and Read Part functions are also accessible through the Aardvark and VersaClock 4.1 software .



Help

A full copy of this user manual is available from Help menu. By selecting the User Manual, the user can toggle between the active VersaClock view (either Single Register or All Register View) and the user manual.

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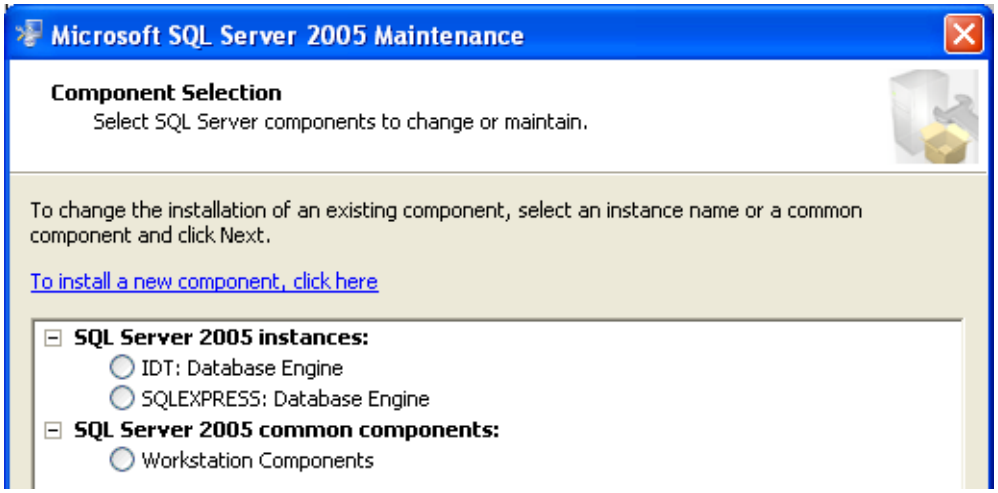
FAQ

I am unable to access the local database. What changes are necessary?

Occasionally, the VersaClock software is unable to access the local database that was separately installed on the computer. This is due to format or software incompatibilities that can easily be corrected.

First, verify that Microsoft SQL Server 2005 is installed correctly.

From Control Panel, open" Add or Remove Program". If the application is installed on your system, select "Change" option. You should see SQL Server 2005 Instance - "IDT: Database Engine"



If this doesn't exist on your machine, then you may have to install SQL Express Manually by downloading the application from: http://www.microsoft.com/Sqlserver/2005/en/us/express-down.aspx and follow the installation instructions.

After installation, uninstall the IDT Local Database and then re-install the local database. Make sure there are no error messages. The local database should work after this step.

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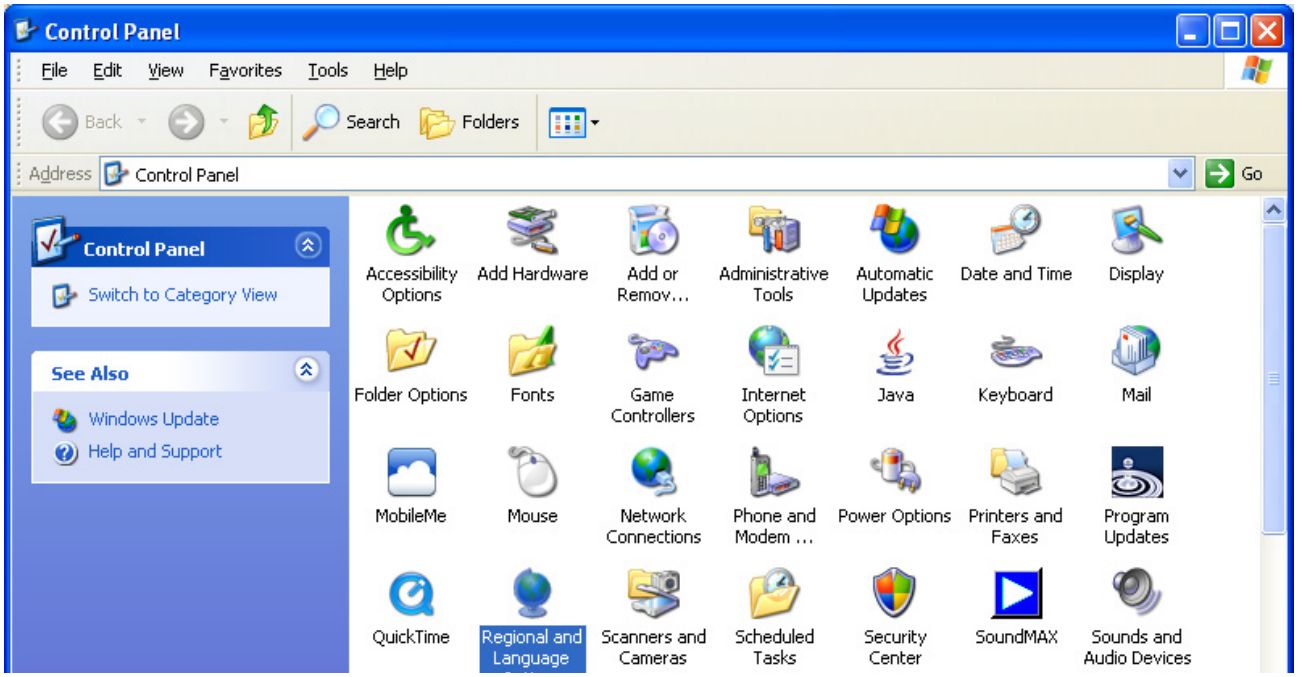
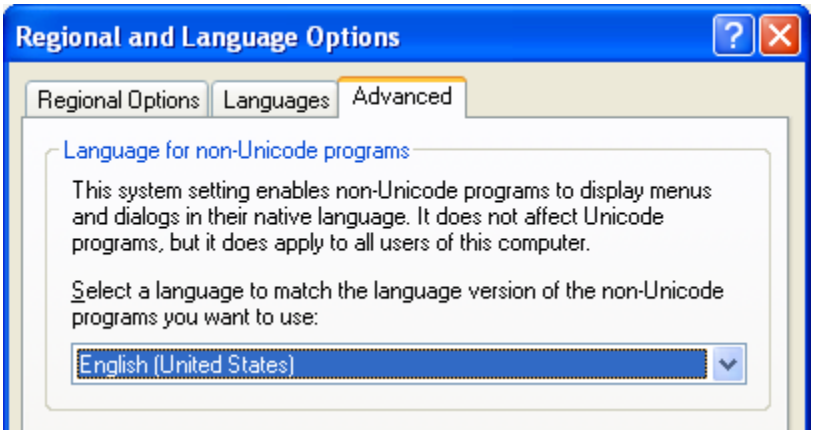
If you are still unable to access the local database, check the “Regional and Language Options” in the Control Panel



Select the “Advanced” tab “Language for non-Unicode programs” and select “*English (United States)*”. You may need to re-boot to have this change take effect. Uninstall both the VersaClock software and local database and re-install. You should now be able to operate correctly.



Where do I get the USB driver to support the VersaClock III or VersaClock LP Evaluation Board?

This driver is part of the application installation process. Once you have completed the installation process by running the setup.exe included in the zip file at www.IDT.com/go/VersaClockLP. The drivers will be installed onto your system. To get them to load, you may need to point the Windows Plug-n-Play wizard to the proper location on your system. You will find the drivers in a folder called “VersaClock III Evaluation Board”. For example, if you follow the defaults the drivers will be in:

C:\Program Files\Integrated Device Technology, Inc\VersaClock® 4.1\VersaClock Evaluation Board.

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Does it matter which order the outputs are entered?

No. The outputs are allocated independently of the order in which they are listed. Multiple copies of a desired output frequency do not have to be next to each other. If there are outputs that are unused, you may chose to insert additional copies of any of the output frequencies provided for that register address.

Spread Spectrum outputs are always allocated first, because only one of the PLLs has that capability. Always start calculation with a register that requires Spread Spectrum (if appropriate). It is then easier to maintain pin compatibility with other registers by modifying the spread percentage or turning off the feature.

How many outputs can have Spread Spectrum?

Spread Spectrum may be applied to some or all of the output frequencies. For example, if there are 4 copies of 14.31818MHz output requested, up to 4 copies of that output frequency can be selected.

Multiple frequencies derived from the same Spread Spectrum VCO frequency may also have Spread Spectrum modulation applied. Select the check buttons associated with the target Spread Spectrum frequencies. Multiple frequencies with simultaneous Spread Spectrum modulation will each have the same percentage and frequency modulation.

If two frequencies are derived using the same spread spectrum PLL, both outputs will have the same modulation rate and modulation amplitude.

Can I specify negative accuracy error only?

Yes. By placing a negative ppm accuracy value in Error ppm column, only negative accuracy error solutions will be considered. If a positive ppm accuracy value is provided, both positive and negative accuracy solutions will be considered.

What frequency does the Spread Spectrum modulate the output clock?

The software allows the entry of any frequency between 32 kHz or 120 kHz modulation. 32 kHz is a common modulation rate set to comply with PCI standard Spread Spectrum modulation requirements. The calculated modulate rate will be displayed in the upper right corner configuration screen, above the pin diagram.

Why do I sometimes get no available resources (N/A) instead of a solution for desired output frequencies?

Each programmable device has a limited number of PLLs and output dividers to generate output target frequencies. In some cases, individual resources may be required by multiple target outputs, but only one may be serviced. The other output will have an N/A notation. An example of this would be when 5 frequencies are selected, with no two being able to share a PLL. Once the resource has been used, it cannot be simultaneously used for another frequency.

Occasionally, you may be able to obtain a better solution by bringing the non-supported frequency to the top of the list. Although this does not guarantee a solution, it sometimes forces frequencies that take up limited resources in one solution to select a different configuration.

Can I turn off all outputs on a register to make sure that I am in the lowest power mode possible?

If you run calculate with no target outputs, you will receive a message “No target frequencies have been specified. Register will be programmed to “Off”. Proceed?” By selecting OK, a banner will be placed at the bottom of the device pin map that indicates all outputs are turned off.

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What file formats do the VersaClock 4.1 software recognize?

The VersaClock 4.1 software defaults to a *.TXT file format. When you save a file, no file extension is required, but a *.TXT extension is recommended to allow you to open the file in a text editor to manually read the file. Using no file extension or *.TXT works equally well with the software.

How can I save binary data string?

In all configuration modes, there is a button on the bottom of the screen that is labelled “Save Binary”. By setting the pull down menu (Menu > Settings > BinHex Output), the file that will be generated will either be: 1) BinHex and binary strings in text file (BinHex setting “Un-checked”; or 2) Intel formatted BinHex setting “checked”. The Intel formatted BinHex provides a 10 Byte line header and 2 Byte checksum for each data line.

Can I change the background colors of VersaClock?

The VersaClock 4.1 software determines it's color scheme from the Windows Display Properties. It can be changed by moving the cursor over the Windows background, right-click and selecting the Appearances tab.

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Revision History

Rev.	Originator	Date	Description of Change
A	RW	02/25/11	Initial release.

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