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[Description]

Page	Chapter	Description	Details
p.27	Chapter 1 Introduction	Modification of Table 1-1 V850E2/SG4-H products	Modified: <A/D converter A (ADCA)> 4 channels -> 8 channels
p.28	Chapter 1 Introduction	Modification of Table 1-1 V850E2/SG4-H products	Modified: <UART with LIN mastercontroller LMA (URTE)> 5 channels -> 4 channels
p.29	Chapter 1 Introduction	Modification of Figure 1-1 Block diagram of	Modified: ADCA0 (4 chn.) -> ADCA0 (8 chn.)
p.29	Chapter 1 Introduction	Modification of Figure 1-1 Block diagram of	Deleted: URTE/LMA10
p.30	Chapter 1 Introduction	Modification of Table 1-2 V850E2/SJ4-H products	Modified: <A/D converter A (ADCA)> 14 channels -> 16 channels
p.33	Chapter 1 Introduction	Modification of Figure 1-2 Block diagram of V850E2/SJ4-	Modified: ADCA0 (14 chn.) -> ADCA0 (16 chn.)
p.39	Chapter 1 Introduction	Addition of Table 1-6 Pin assignment (2/5)	Added: Note. Set the IC pin to low level.
p.42	Chapter 1 Introduction	Modification of Table 1-6 Pin assignment	Modified: <pin 176> "P25_2/MEMC0AD2/TAUA0I2/TAUA0O2/IISA0WS/CSIH0DCS/CSIH0SO" -> "P25_2/MEMC0AD2/TAUA0I2/TAUA0O2/IISA0WS/CSIH0SO"
p.77	Chapter 2 Pin Functions	Modification of (1) P0_0: RESETOUT	Modified: "After reset is cancelled, the P0_0 pin outputs an active RESETOUT signal." -> "P0_0 outputs a RESETOUT signal, which is low level during reset and after reset release."
p.77	Chapter 2 Pin Functions	Add of Caution for (1) P0_0: RESETOUT	Added: Caution Once asserted the RESETOUT remains on low level. It must be de-asserted by changing the port configuration of P0_0 after reset release.
p.78	Chapter 2 Pin Function	Addition of Note of Table 2-29 Permanent input pins	Note. Port group 10(P10) is possible to use as port input/output mode respectively. However the adjacent pin does I/O level changing and influence of the external circuit connected to the port pin during A/D conversion, the A/D conversion value may not be obtained.
p.82, p.83	Chapter 2 Pin Function	Addition of Table 2-31 V850E2/SG4-H general-purpose I/O operations	Added: "Port group 0:" --> "Port group 0 (Always-On-Area, E0VDD/E0VSS power supply):" "Port group 1:" --> "Port group 1 (Isolated-Area-0, E1VDD/E1VSS power supply):" "Port group 10:" --> "Port group 10 (Isolated-Area-0, AVDD/AVSS power supply):" "Port group 21:" --> "Port group 21 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 25:" --> "Port group 25 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 27:" --> "Port group 27 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group JP0:" --> "Port group JP0 (Always-On-Area, E0VDD/E0VSS power supply):"

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p.82, p.83	Chapter 2 Pin Function	Addition of Table 2-31 V850E2/SG4-H general-purpose I/O operations	Added: When using the following alternate-function pin, set PBDCn.PBDCn_m = 1. <IICB0SDA, IICB0SCL, IICB1SDA, IICB1SCL, IICB2SDA, IICB2SCL > ALT_IN4 -> ALT_OUT4
p.82	Chapter 2 Pin Function	Addition of Table 2-31 V850E2/SG4-H general-purpose I/O operations	Added: P10_4,P10_5,P10_6 and P10_7 row
p.83	Chapter 2 Pin Function	Modification of Table 2-31 V850E2/SG4-H general-purpose I/O operations	Delete: P27_4, P27_5 row
p.88 to p.91	Chapter 2 Pin Function	Addition of Table 2-34 V850E2/SJ4-H general-purpose I/O operations	Added: "Port group 0:" --> "Port group 0 (Always-On-Area, E0VDD/E0VSS power supply):" "Port group 1:" --> "Port group 1 (Isolated-Area-0, E1VDD/E1VSS power supply):" "Port group 3:" --> "Port group 3 (Isolated-Area-0, E1VDD/E1VSS power supply):" "Port group 10:" --> "Port group 10 (Isolated-Area-0, AVDD/AVSS power supply):" "Port group 21:" --> "Port group 21 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 25:" --> "Port group 25 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 26:" --> "Port group 26 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 27:" --> "Port group 27 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 28:" --> "Port group 28 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group JP0:" --> "Port group JP0 (Always-On-Area, E0VDD/E0VSS power supply):"
p.88 to p.91	Chapter 2 Pin Function	Addition of Table 2-34 V850E2/SJ4-H general-purpose I/O operations	Added: When using the following alternate-function pin, set PBDCn.PBDCn_m = 1. <IICB0SDA, IICB0SCL, IICB1SDA, IICB1SCL, IICB2SDA, IICB2SCL > ALT_IN4 -> ALT_OUT4
p.89	Chapter 2 Pin Function	Addition of Table 2-34 V850E2/SJ4-H general-purpose I/O operations	Added: P10_14 and P10_15 row
p.98 to p.101	Chapter 2 Pin Function	Addition of Table 2-38 V850E2/SK4-H general-purpose I/O operations	Added: "Port group 0:" --> "Port group 0 (Always-On-Area, E0VDD/E0VSS power supply):" "Port group 1:" --> "Port group 1 (Isolated-Area-0, E1VDD/E1VSS power supply):" "Port group 3:" --> "Port group 3 (Isolated-Area-0, E1VDD/E1VSS power supply):" "Port group 10:" --> "Port group 10 (Isolated-Area-0, AVDD/AVSS power supply):" "Port group 21:" --> "Port group 21 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 25:" --> "Port group 25 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 26:" --> "Port group 26 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 27:" --> "Port group 27 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group 28:" --> "Port group 28 (Isolated-Area-1, B0VDD/B0VSS power supply):" "Port group JP0:" --> "Port group JP0 (Always-On-Area, E0VDD/E0VSS power supply):"
p.98 to p.101	Chapter 2 Pin Function	Addition of Table 2-38 V850E2/SK4-H general-purpose I/O operations	Added: When using the following alternate-function pin, set PBDCn.PBDCn_m = 1. <IICB0SDA, IICB0SCL, IICB1SDA, IICB1SCL, IICB2SDA, IICB2SCL > ALT_IN4 -> ALT_OUT4

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p.117	Chapter 2 Pin Function	Addition of "Table 2-42 List of pin functions in alphabetical order	Added: Note. Set the IC pin to low level.
p.136	Chapter 2 Pin Function	Addition of 2.4.8 Recommended connection of unused pins	Added: IC: input the low-level voltage.
p.141	Chapter 2 Pin Function	Modification of Table 2-46 Input signals and control registers for ports that incorporate digital filter type D	Modified: "URTE2RX: DNFA11EN.DNFA11NFEN0 " -> "DNFA11EN.DNFA11NFEN8" "URTE3RX: DNFA11EN.DNFA11NFEN1" -> "DNFA11EN.DNFA11NFEN9"
p141	Chapter 2 Pin Function	Addition of Table 2-46 Input signals and control registers for ports that incorporate digital filter type D	Note : When using the input pin of Clocked Serial Interface(CSIGn and CSIHn) function , set bypass filter mode. These input port was allocated port filter (initial status is work) since communication error occurs. CSIG0SC: FCLA24CTL0 = 80H, CSIG0SI: FCLA24CTL2 = 80H, CSIG0SSI: FCLA24CTL3 = 80H CSIG4SC: FCLA7CTL2 = 80H, CSIG4SI: FCLA7CTL3 = 80H, CSIG4SSI: FCLA7CTL5 = 80H CSIH0SC: FCLA22CTL0 = 80H, CSIH0RYI: FCLA22CTL1 = 80H, CSIH0SI: FCLA22CTL2 = 80H, CSIH0SSI: FCLA22CTL3 = 80H CSIH1SC: FCLA22CTL4 = 80H, CSIH1RYI: FCLA22CTL5 = 80H, CSIH1SI: FCLA22CTL6 = 80H, CSIH1SSI: FCLA22CTL7 = 80H CSIH2SC: FCLA23CTL0 = 80H, CSIH2RYI: FCLA23CTL1 = 80H, CSIH2SI: FCLA23CTL2 = 80H, CSIH2SSI: FCLA23CTL3 = 80H
p.141	Chapter 2 Pin Function	Addition of Table 2-46 Input signals and control registers for ports that incorporate digital filter type D	Note : When using the receive data input pin(URTEnRX) of Asynchronous Serial Interface E (UARTE) function , set bypass filter mode. These input port was allocated port filter (initial status is work) since communication error occurs. URTE0RX: FCLA26CTL4 = 80H URTE1RX: FCLA26CTL5 = 80H URTE2RX: FCLA27CTL0 = 80H URTE3RX: FCLA27CTL1 = 80H URTE10RX: FCLA7CT
p.146	Chapter 2 Pin Function	Modification of 2.6.2 Digital filters	Modified : "Caution : After enabling the digital filter by setting DNFAnEN.DNAFnNFENm to1, the digital filter operates normally after the following time period elapses: Number of samples x 1/fs + 4 x 1/fDNFATCKI Note that an unexpected signal might be output within this time period. It is therefore important to wait for the above time period to elapse before enabling functions and sending signals." -> " Caution 1: In case where input signal altenate function from digital filter output signal, set digital filter after the following time have passed. the port set change to altrnative function mode. DNFAnNFSTS[1:0] x 1/fs + 4 x 1/fDNFATCKI Caution 2 : When using the event output signal of digital filter as interrupt, please set the digital filter effective (DNFAnEN.DNAFnENm = 1) by interrupt disabled status. set the digital filter after having passed following time after clearing the interrupt request flag, set Enable interrupt. DNFAnNFSTS[1:0] x 1/fs + 5 x 1/fDNFATCKI
p.164	Chapter 3 CPU System Function	Modification of Figure 3-4 V850E2/Sx4-H CPU	Added: FPU block on V850E2M CPU
p.164	Chapter 3 CPU System Function	Modification of Figure 3-4 V850E2/Sx4-H CPU	Delete: Cache for HBUS master I/F

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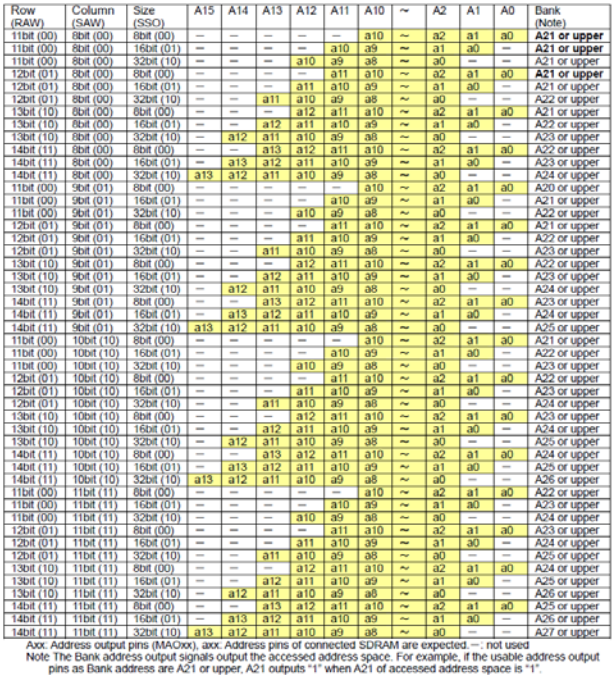
p.180	Chapter 3 CPU System Function	Addition of Table 3-22 Backup RAM area	Added: Before fetch does optional instruction code from a data RAM, please initialize 16 byte boundary line of a data RAM including the instruction code. 16 bytes boundary line is the range from address XXXX XXX0H to XXXX XXXFH. When initializing a data RAM, it's possible to write in a data value, but please be sure to set before fetch is done to be initialized. When instruction fetch from uninitialized data RAM space, Memory error exception (MEP) occurs. Remark: Before reading from data RAM, it's recommended to initialize the whole data RAM.
p180	Chapter 3 CPU System Function	Addition of Table 3-22 Backup RAM area	Added: Remark Instructions cannot be fetched from the backup RAM area.The backup RAM can be read/written in 32-bit units.
p.185	Chapter 3 CPU System Function	Additon of Caution for 3.9 HBUS Bridge in CPU Subsystem	Added: Caution V850E2/Sx4-H doesn't have Cache for HBUS Master interface. Thus, don't change the cache related bits on the registers from initial value.
p.227	Chapter 4 External Memory Controller (MEMC)	Addition of 4.2.11 SDCR - SDRAM configuration register	Added: Cautions 6 Please write only once in SDRAM configuration register after reset release.After writing, please do not change the value.When changing the value, it is can't normally access any more in SDRAM.
p.236	Chapter 4 External Memory Controller (MEMC)	Addition of 4.3.2 SDRAM bus cycle type	A connection list to SDRAM by address bus is given in the tables below.  Axx. Address output pins (MAOxx), axx. Address pins of connected SDRAM are expected. —: not used Note The Bank address output signals output the accessed address space. For example, if the usable address output pins as Bank address are A21 or upper, A21 outputs "1" when A21 of accessed address space is "1".
p.326	Chapter 6 DMA Controller (DMAC)	Modification of Table 6-2 DMA start sources	Modified: "INTADC0I0" -> "INTADCA0I0", "INTADC0I1" -> "INTADCA0I1", "INTADC0I2" -> "INTADCA0I2"
p.356	Chapter 6 DMA Controller (DMAC)	Modification of Table 6-18 DDCn register contents	Modified: "Data flash, external memory area, peripheral I/O area, and HBUS-RAM" -> " external memory area, peripheral I/O area, and HBUS-RAM"
p.356	Chapter 6 DMA Controller (DMAC)	Modification of Table 6-18 DDCn register contents	Modified: "Code flash and local RAM" -> "local RAM"
p.438 to p.439	Chapter 9 Clock Controller	Addition of 9.4.1 Clock domains of the Always-On area	Added: Caution If the Always-On area- is in STOP/DEEPSTOP mode, the clock selector control registers CKSC_1n and clock selector status registers CSCSTAT_1n are not accessible.
p.444 to p.455	Chapter 9 Clock Controller	Addition of 9.4.3 Isolated area 1 clock domain	Added: Caution If the Isolated-Area-1 is in STOP/DEEPSTOP mode, the clock selector control registers CKSC_1n and clock selector status registers CSCSTAT_1n are not accessible.

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p.444 to p.455	Chapter 9 Clock Controller	Addition of 9.4.3 Isolated area 1 clock domain	Added: Caution If the Isolated-Area-1 is in STOP/DEEPSTOP mode, the clock selector control registers CKSC_1n and clock selector status registers CSCSTAT_1n are not accessible.
p.459	Chapter 9 Clock Controller	Modification of Table 9-9 V850E2/Sx4-H CLMAn startup options	Modified: CLMA2CTL0.CLMAnCLME = OPBT[1] -> CLMA2CTL0.CLMAnCLME = 0, CLMA2CTL1.CLMAnOSEL = OPBT[2] -> CLMA2CTL1.CLMAnOSEL = 0
p.461	Chapter 9 Clock Controller	Modification of (1) Detection of abnormal clock frequencies	Modified: "8 cycles of the sampling clock CLMATSMP" -> "16 cycles of the sampling clock CLMATSMP"
p.474	Chapter 9 Clock Controller	Modification of Table 9-21 MOSCC register contents	Modified : "6 MHz < fX ≤ 20 MHz" -> "16 MHz < fX ≤ 20 MHz"
p.480	Chapter 9 Clock Controller	Modification of (8) ROSCE - High-speed IntOsc enable register	Modified: "ROSCDISTRG, R/W " -> "0a, R" a) set 0 at bit0
p.480	Chapter 9 Clock Controller	Modification of (8) ROSCE - High-speed IntOsc enable register	Delete: row of Bit position 0 "ROSCDISTRG"
p.500	Chapter 10 Standby Controller (STBC)	Modification of Table 10-9 Buffer operation in DEEPSTOP mode and after	Delete: line of I/O buffer power Delete: row of I/O buffer power Off
p.500	Chapter 10 Standby Controller (STBC)	Modification of Table 10-9 Buffer operation in DEEPSTOP mode and after	Delete: b) If the I/O buffer power supply is switched on before the isolated area has woken up from DEEPSTOP mode,the I/O buffer state becomes undefined.
p.500	Chapter 10 Standby Controller (STBC)	Modification of Table 10-9 Buffer operation in DEEPSTOP mode and after wake-up	Delete :Caution If Isolated area m is set to DEEPSTOP mode and the power supply of its I/O buffers is switched off, the buffer becomes inactive. If the I/O buffer power supply is switched on before the isolated area has woken up from DEEPSTOP mode, the I/O buffer state becomes undefined.
p.502	Chapter 10 Standby Controller (STBC)	Modification of 10.2.4 Examples of entering and exiting power save mode	Modified: "2. When stopping a clock source (high-speed internal oscillator, main clock oscillator, subclock oscillator, or PLLk) before entering standby mode, either switch all of the clock sources used in the clock domain to other clock sources, or clear the CKSC_mn register to 0 to disable outputting the relevant clock." ->"2. When stopping a clock source (main clock oscillator, subclock oscillator, or PLLk) before entering standby mode by each other setting the operation stop trigger bit（MOSCE.MOSCDISTRG，SOSCE.SOSCDISTRG，PLLkE.PLLkDISTRG), either switch all of the clock sources used in the clock domain to other clock sources, or clear the CKSC_mn register to 0 to disable outputting the relevant clock"
p.505	Chapter 10 Standby Controller (STBC)	Modification of Figure 10-3 Recommended flow for entering and exiting RUN mode (Iso1 STOP)	Delete: Initializing graphics subsystem
p.506	Chapter 10 Standby Controller (STBC)	Modification of Figure 10-4 Recommended flow for entering and exiting	Delete: After enabling interrupt servicing by executing the CPU instruction EI, a wakeup interrupt is serviced.

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p.507	Chapter 10 Standby Controller (STBC)	Modification of Figure 10-4 Recommended flow for entering and exiting DEEPSTOP mode	modified: "Enable interrupts (EI) | Interrupt service routine | RUN mode" -> "Enable interrupts (EI) | Wake-up factor read/write | Wake-up factor processing | Run mode"
p.528	Chapter 11 Code Protection and Security	Modification of (2) IDMODI - On-chip debug control register	Modified: "PROTCMD4" -> "PROTCMD3"
p.538	Chapter 12 Reset Controller	Modification of 12.2.4 RAM retention voltage indicator (RAMHF)	Modified: "VVLVI" -> "VRAMHF"
p.547	Chapter 12 Reset Controller	Modification of Table 12-5 LVICNT register contents	Modified: "LVI level 3 (2.8 V ±0.1 V)" -> "Setting prohibited"
p.548	Chapter 12 Reset Controller	Modification of 12.3.5 RAM retention voltage detection flag control registers	Modified: "Initial value 0000 0000H" -> "Initial value 0000 0001H"
p.570	Chapter 14 Window Watchdog Timer A (WDTA)	Modification of Table 14-7 WDTA start-up options	Modified: OPWDINT connected to "Fixed to 1" -> "Fixed to 0"
p.681	Chapter 15 Timer Array Unit A (TAUA)	Modification of (2) Equations	Modified: "(FFFFH × TAUAnCSRm.TAUAnOVF)" -> "(FFFFH + 1× TAUAnCSRm.TAUAnOVF)"
p.712	Chapter 15 Timer Array Unit A (TAUA)	Modification of Table 15-29 TAUAnCMURm settings for one-pulse output function	Modified: <TAUAnSTS[2:0]> "000" -> "001"
p.727	Chapter 15 Timer Array Unit A (TAUA)	Modification of Table 15-81 TAUAnCMURm settings for simultaneous rewrite trigger generation function type 2	Modified: "10: Rising and falling edge detection (low width measurement), 11: Rising and falling edge detection (high width measurement)" to "10: Rising and falling edge detection, 11: Setting prohibited"
p.789	Chapter 15 Timer Array Unit A (TAUA)	Modification of Table 15-127 Control bit settings for slave channel 1 of the synchronous channel output mode 1	Modified: <TAUAnTOC.TAUAnTOCm> "1: Set/reset mode" -> "0: Operation mode 1"
p.808	Chapter 15 Timer Array Unit A (TAUA)	Modification of (2) Equations	Modified: "Pulse width = (TAUAnCDRm (slave) + 1) x count clock cycle" -> "Pulse width = (TAUAnCDRm (slave)) x count clock cycle"
p.827	Chapter 15 Timer Array Unit A (TAUA)	Modification of (1) Overview	Modified: "This ensures that slave channel 2 is an odd channel, and slave channel 3 is an even channel." -> "This ensures that slave channel 2 is an even channel, and slave channel 3 is an odd channel."
p.925	Chapter 15 Timer Array Unit A (TAUA)	Modification of Table 15-254 TAUAnRDC register contents	Modified: "0: Have the channel generate the simultaneous rewrite trigger signal. 1: Do not have the channel generate the simultaneous rewrite trigger signal." -> "0: Do not have the channel generate the simultaneous rewrite trigger signal. 1: Have the channel generate the simultaneous rewrite trigger signal."
p.1011	Chapter 16 Timer Array Unit B (TAUB)	Modification of (2) Equations	Modified: "(FFFFH × TAUBnCSRm.TAUBnOVF)" -> "(FFFFH + 1× TAUBnCSRm.TAUBnOVF)"
p.1054	Chapter 16 Timer Array Unit B (TAUB)	Modification of (2) Equations	Modified: (FFFFH+1 × TAUBnCSRm.OVF) -> (FFFFH+1) × TAUBnCSRm.OVF
p.1115	Chapter 16 Timer Array Unit B (TAUB)	Modification of (1) Overview	Modified: "This ensures that slave channel 2 is an odd channel, and slave channel 3 is an even channel." -> "This ensures that slave channel 2 is an even channel, and slave channel 3 is an odd channel."

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p.1364	Chapter 20 Asynchronous Serial Interface E (UARTE)	Modification of Table 20-1 Instances of UARTE	Modified: 5 channels (UARTE0-UARTE3, UARTE10) -> SG4-H: 4 channels (UARTE0-UARTE3), SJ4-H and SK4-H: 5 channels (UARTE0-UARTE3, UARTE10)
p.1365	Chapter 20 Asynchronous Serial Interface E (UARTE)	Additon of Caution for Table 20-6 URTEn I/O signals	Added: Caution The receive input pins (URTEnRX) of Asynchronous Serial Interface E (URTE) are assigned the port filter. (These filters are active in default.) Because there are internal filters in URTE module, they should be active and port filers should be bypass. otherwise URTEnRX inputs can not work correctly. URTE0RX: FCLA26CTL4 = 80H URTE1RX: FCLA26CTL5 = 80H URTE2RX: FCLA27CTL0 = 80H URTE3RX: FCLA27CTL1 = 80H URTE10RX: FCLA7CTL0 = 80H
p.1409	Chapter 21 LIN Master Controller (LMA)	Modification of Table 21-1 Instances of LMAn	Modified: 5 channels (LMA0-LMA3, LMA10) -> SG4-H: 4 channels (LMA0-LMA3), SJ4-H and SK4-H: 5 channels (LMA0-LMA3, LMA10)
p.1409	Chapter 21 LIN Master Controller (LMA)	Modification of Table 21-2 Channels of CNTAn	Modified: 3 channels (CNTA0-CNTA2) -> SG4-H: 2 channels (CNTA0, CNTA1), SJ4-H and SK4-H: 3 channels (CNTA0-CNTA2)
p.1459	Chapter 22 CAN Controller (FCN)	Modification of Table 22-8 FCNn time stamp signals	Modified: <Connection of FCN1> "TAUA0 TAUA1TTIN0" -> "TAUA0 TAUA0TTIN1"
p.1480	Chapter 22 CAN Controller (FCN)	Modification of (2) FCNnGMCSPRE - FCNn global clock selection register	Modified: "FCN module system clock (fCANMOD)" -> "the CAN protocol layer pre-basic system clock (fCANPRE)"
p.1496	Chapter 22 CAN Controller (FCN)	Modification of (8) FCNnCMBRPRS - FCNn module bit rate prescaler register	Modified: "0 fCANMOD/1 1 fCANMOD/2 n fCANMOD/(n+1) ... ... 255 fCANMOD/256 (default value)" -> "0 fCANPRE/1 1 fCANPRE/2 n fCANPRE/(n+1) ... ... 255 fCANPRE/256 (default value)"
p.1546	Chapter 22 CAN Controller (FCN)	Modification of 22.14.1 Baud rate setting conditions	Modified: "SPT = FCNnCMBTS1LG[3:0] + 1" -> "SPT = TSEG1 + 1"
p.1546	Chapter 22 CAN Controller (FCN)	Modification of 22.14.1 Baud rate setting conditions	Modified: "DBT = FCNnCMBTS1LG[3:0] + FCNnCMBTS2LG[2:0] + 1 TQ = FCNnCMBTS2LG[2:0] + SPT" -> "DBT = TSEG1 + TSEG2 + 1 TQ = TSEG2 + SPT"
p.1546	Chapter 22 CAN Controller (FCN)	Modification of 22.14.1 Baud rate setting conditions	Modified: "1 TQ ≤ FCNnCMBTJWLG[1:0] (synchronization jump width) ≤ 4 TQ" -> "1 TQ ≤ SJW (synchronization jump width) ≤ 4 TQ"
p.1546	Chapter 22 CAN Controller (FCN)	Modification of 22.14.1 Baud rate setting conditions	Modified: "FCNnCMBTJWLG[1:0] ≤ DBT – SPT" -> "SJW ≤ DBT – SPT"
p.1546	Chapter 22 CAN Controller (FCN)	Modification of 22.14.1 Baud rate setting conditions	Modified: "4 ≤ FCNnCMBTS1LG[3:0] ≤ 16 [3 ≤ FCNnCMBTS1LG[3:0] ≤ 15]" -> "4 ≤ TSEG1 ≤ 16"
p.1546	Chapter 22 CAN Controller (FCN)	Modification of 22.14.1 Baud rate setting conditions	Modified: "1 ≤ FCNnCMBTS2LG[2:0] ≤ 8 [0 ≤ FCNnCMBTS2LG[2:0] ≤ 7]" -> "1 ≤ TSEG2 ≤ 8"
p.1546	Chapter 22 CAN Controller (FCN)	Modification of 22.14.1 Baud rate setting conditions	Modified: "The values FCNnCMBTS1LG[3:0], FCNnCMBTS2LG[2:0] and FCNnCMBTJWLG[1:0] are specified in the FCNnCMBTCTL register." -> "The values TSEG1, TSEG2, and SJW are specified in the bits of the following register." TSEG1 = FCNnCMBTCTL.FCNnCMBTS1LG[3:0] + 1 TSEG2 = FCNnCMBTCTL.FCNnCMBTS2LG[2:0] + 1 SJW = FCNnCMBTCTL.FCNnCMBTJWLG[1:0] + 1
p.1560	Chapter 22 CAN Controller (FCN)	Modification of Figure 22-19 “Message buffer redefinition during transmission”	Modified: <Remote frame> "Set FCNnMmDTLGB register Clear FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register" -> "Set FCNnMmDTLGB register Set FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register"

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p.1561	Chapter 22 CAN Controller (FCN)	Modification of Figure 22-20 “Message transmit processing”	Modified: <Remote frame> "Set FCNnMmDTLGB register Clear FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register" -> "Set FCNnMmDTLGB register Set FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register"
p.1563	Chapter 22 CAN Controller (FCN)	Modification of Figure 22-22 Transmission via interrupt (using FCNnCMLOSTR register)	Modified: <Remote frame> "Set FCNnMmDTLGB register Clear FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register" -> "Set FCNnMmDTLGB register Set FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register"
p.1564	Chapter 22 CAN Controller (FCN)	Modification of Figure 22-23 Transmission via interrupt (using FCNnCMTGTX register)	Modified: <Remote frame> "Set FCNnMmDTLGB register Clear FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register" -> "Set FCNnMmDTLGB register Set FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register"
p.1564	Chapter 22 CAN Controller (FCN)	Modification of Figure 22-23 Transmission via interrupt (using FCNnCMTGTX	Modified: "FCNnCMTGTX.FCNnCMTGTVFF = 0?" -> "FCNnCMTGTX.FCNnCMTGTVFF = 1?"
p.1566	Chapter 22 CAN Controller (FCN)	Modification of Figure 22-24 Transmission via software polling	Modified: <Remote frame> "Set FCNnMmDTLGB register Clear FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register" -> "Set FCNnMmDTLGB register Set FCNnMmSTRB.FCNnMmSSRT Set FCNnMmMID0W register"
p.1776	Chapter 24 Clocked Serial Interface G (CSIG)	Additon of Caution for Table 24-7 CSIGn I/O signals	Added: Caution The receive input pins of Clocked Serial Interface G (CSIG) are assigned the port filter. (These filters are active in default.) If CSIG modules are used, their port filers should be bypass. otherwise CSIG modules can not work correctly. CSIG0SC：FCLA24CTL0 = 80H, CSIG0SI：FCLA24CTL2 = 80H, CSIG0SSI：FCLA24CTL3 = 80H CSIG4SC：FCLA7CTL2 = 80H, CSIG4SI：FCLA7CTL3 = 80H, CSIG4SSI：FCLA7CTL5 = 80H
p.1823	Chapter 25 Clocked Serial Interface H (CSIH)	Additon of Caution for Table 25-8 CSIHn I/O signals	Added: Caution The receive input pins of Clocked Serial Interface H (CSIH) are assigned the port filter. (These filters are active in default.) If CSIH modules are used, their port filers should be bypass. otherwise CSIG modules can not work correctly. CSIH0SC：FLCA22CTL0 = 80H CSIH0RY：FLCA22CTL1 = 80H CSIH0SI：FLCA22CTL2 = 80H CSIH0SSI：FLCA22CTL3 = 80H CSIH1SC：FLCA22CTL4 = 80H CSIH1RY：FLCA22CTL5 = 80H CSIH1SI：FLCA22CTL6 = 80H CSIH1SSI：FLCA22CTL7 = 80H CSIH2SC：FLCA23CTL0 = 80H CSIH2RY：FLCA23CTL1 = 80H CSIH2SI：FLCA23CTL2 = 80H
p.2085	Chapter 27 IISA Interface (IISA)	Modification of (2) Baudrate generators	Modified: "N = CLKDakDIV.CLKDakDIV[8:0] + 1" -> "N = CLKDakDIV.CLKDakDIV[8:0]"
p.2086	Chapter 27 IISA Interface (IISA)	Modification of (1) CLKDakDIV – Divisor register	Modified: CLK00DIV: FF82 9000H, CLK01DIV: FF82 9100H, CLK10DIV: FF82 9200H, CLK11DIV: FF82 9300H, CLK20DIV: FF82 9400H, CLK21DIV: FF82 9500H ->> CLKD00DIV: FF82 9000H, CLKD01DIV: FF82 9100H, CLKD10DIV: FF82 9200H, CLKD11DIV: FF82 9300H, CLKD20DIV: FF82 9400H, CLKD21DIV: FF82 9500H

[Description]

p.2086	Chapter 27 IISA Interface (IISA)	Modification of Table 27-9 CLKDakDIV register contents	Modified: 000H: N = 1 001H: N = 2 002H: N = 3 ... 1FEH: N = 511 1FFH: N = 512 -> 000H: N = No output 001H: N = 1 002H: N = 2 ... 1FEH: N = 510 1FFH: N = 511
p.2100	Chapter 27 IISA Interface (IISA)	Additon of Caution for (1) IISAnCTL – IISA control register	Added: Caution Setting of IISAnCTL register becomes valid after time of 6*PCLK＋6*IISA0SCK. It's impossible to write it during no clock supply to PCLK and IISA0SCK.
p.2106	Chapter 27 IISA Interface (IISA)	Additon of Caution for (2) IISAnSTC – IISA status clear register	Added: Caution Setting of IISAnSTC register becomes valid after time of 6*PCLK＋6*IISA0SCK. It's impossible to write it during no clock supply to PCLK and IISA0SCK.
p.2175	Chapter 28 PCM Interface (PCM)	Modification of (13) PCMnCFG - PCM signal configuration register	Modified: "Access This register can be read or written in 8-bit units." -> "Access This register can be read or written in 32-bit units.", "0 0 0 0 0 0 PCMnCFGC PCMnCFGS" -> "0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 PCMnCFGC PCMnCFGS"
p.2314	Chapter 32 A/D Converter (ADCA)	Additon of Caution for Chapter 32 A/D Converter (ADCA)	Added: Caution The Sampling mode of V850E2/Sx4-H is mode A.
p.2314	Chapter 32 A/D Converter (ADCA)	Modification of Table 32-2 ADCAn channel indices	Modified: "V850E2/FG4-H: m = 0 to 3" -> "V850E2/SG4-H: m = 0 to 7"
p.2314	Chapter 32 A/D Converter (ADCA)	Modification of Table 32-2 ADCAn channel indices	Modified: "V850E2/FJ4-H: m = 0 to 13" -> "V850E2/SJ4-H: m = 0 to 13"
p.2333	Chapter 32 A/D Converter (ADCA)	Modification of Table 32-10 Conversion times for sampling mode A (product dependent)	Deleted: If conversion is performed continuously, conversion start request acceptance processing is not required the second and subsequent times.
p.2365	Chapter 32 A/D Converter (ADCA)	Modification of Table 32-19 ADCAnCGi register contents	Modified: <ADCAn.CGiS[23:00]> 0: Convert analog input ADCAnIm 1: Do not convert analog input ADCAnIm -> 0: Do not convert analog input ADCAnIm 1: Convert analog input ADCAnIm
p.2381	Chapter 32 A/D Converter (ADCA)	Modification of Table 32-35 ADCAnCTL2 register contents	Modified: 0: Perform upper/lower limit comparison for A/D conversion of CHm. 1: Do not perform upper/lower limit comparison for A/D conversion of CHm -> 0: Do not perform upper/lower limit comparison for A/D conversion of CHm 1: Perform upper/lower limit comparison for A/D conversion of CHm.