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RENESAS

User's Manual

μPD98405

(NEASCOT-S20™)

155M ATM Integrated SAR Controller

Document No. S12250EJ4V0UMJ1 (4th edition)
Date Published October 2000 N CP(K)

Printed in Japan

[MEMO]

SUMMARY OF CONTENTS

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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MAIN CHANGES IN THIS EDITION

Page	Description
p.20	**Chapter 1** Addition of a package to **Section 1.2**.
Throughout p.24, 28, 37, 44	**Chapter 2** Addition of a package. Addition of descriptions of REQ64_B, ACK64_B pin functions to **Section 2.3.2 (2)**. Addition of JRST_B pin functions to **Section 2.3.5**.
pp.77-82, 84, 85, 102, 106, 107, 115, 116	**Chapter 4** Addition of features to **Section 4.2.1**. Addition of descriptions to **Section 4.2.2**. Addition of descriptions to **Table 4-6**. Addition of **Section 4.2.3 (1)**. Addition of **Remark** and **Caution** to **Section 4.2.4 (1)**. Addition of descriptions to **Section 4.2.4 (3)**. Addition of **Remark** to **Section 4.2.8 (3)**. Addition of **Caution** to **Figure 4-31**. Addition of description to the table. Addition of **Caution** to **Section 4.5**. Change of description in • **Receive clock recovery PLL function**.
pp.119, 124, 129, 147, 165, 175, 177, 181, 193, 236, 242, 261	**Chapter 5** Addition of descriptions to **Sections 5.1** and **5.2 (3)**. Addition of **Caution 4** to **Section 5.3.1**. Addition of **Caution** to **Section 5.4.3 (3)**. Addition of **Caution 3** to **Section 5.4.4 (8)**. Addition of **Caution** to **Section 5.5.2 (1)**. Change of description in **Section 5.5.2 (2) <1>**. Addition of description to **5.5.3 (2) T1D**. Addition of **Caution** to **Section 5.5.4**. Addition of **Remark** to **Sections 5.9.1** and **5.10.1**. Addition of description to **Section 5.13 Remark**. Addition of **Caution** to **Section 5.14**.
p.267, 271, 272, 279, 282, 283, 286, 287	**Chapter 6** Change of **Section 6.1 (1) (a)**. Addition of descriptions to **Section 6.2 (2)** and **(4)**. Change of description in **Sections 6.2 (5)** and **6.3.1 (2)**. Change of description of LOS, LOP, and Path AIS in **Table 6-7**. Addition of OOL to **Table 6-7**. Addition of **Remark** to **Section 6.3.2 (3)**. Change of description of the insert register and drop register in **Section 6.4**.
p.306, 308, 309, 315, 316, 318, 321, 325, 333	**Chapter 7** Addition of descriptions to **Section 7.2 (6)**, **(11)** and **(12)** and **Section 7.3 (2)** and **(4)**. Addition of **Caution** to **Section 7.3 (7)**. Addition of descriptions to **Section 7.3 (12)** and **(18)**. Addition of description to **Section 7.4 (5) D2:RxCL**.
p.371, 384, 385	**Chapter 8** Addition of supported instructions in **Sections 8.1**, **8.7**, and **8.7.3**. Addition of description to **Section 8.6 (3)**.

The mark ★ shows major revised points.

PREFACE

Users This manual is for engineers who intend to learn the capabilities of the μPD98405 for application system design.

Purpose The purpose of this manual is to help users understand the hardware capabilities of the μPD98405 as listed below.

Organization This manual is organized as follows:

- Overview
- Pin functions
- Functional description
- Interfaces
- SAR function
- PHY function
- Registers
- JTAG boundary scan
- List of data formats

Guidance Before using this manual, the user should have a general knowledge of the electronics, logical circuit, and microcomputer fields.

- **To understand the general functions of the μPD98405**:
  Read the entire manual in the order of the table of contents.
- **To check the electrical characteristics of the μPD98405**:
  See the separate Data Sheet.

Conventions

Data weight	:	High-order digits on the left side Low-order digits on the right side
Active low	:	XXX_B (pin name, signal name, appended with _B)
Memory map address	:	Low-order address on the upper side High-order address on the lower side
Note	:	Explanation of the indicated part of the text
Caution	:	Information requesting the user's special attention
Remark	:	Supplementary information
Numeric value	:	Binary : xxxx or xxxxB Decimal : xxxx Hexadecimal : xxxxH

Related Documents The related documents indicated here may include preliminary versions. Note, however, that preliminary versions are not marked as such.

- Pamphlet : S12214E
- Data sheet : S12689E
- Application Note : S13369E
- Information Q&A : S14628E

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CHAPTER 1 OVERVIEW

The μPD98405 is a high performance ATM segmentation and reassembly chip (SAR chip). It features a PCI bus interface, a SONET/SDH 155 Mbps framer, clock recovery, and supports the ABR function in hardware. The chip conforms to the ATM Forum recommendations and implements the required AAL-5 SAR sublayer, ATM layer, and TC sublayer functions.

1.1 FEATURES

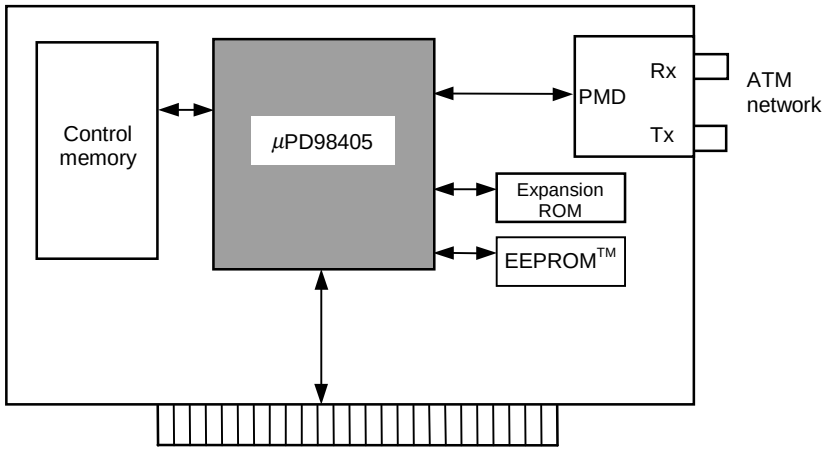
- Conforms to the ATM Forum recommendations.
- The PCI bus and generic bus are supported as host bus interfaces.
  - Built-in PCI bus interface (5/3.3 V, 32/64 bits, 33 MHz): Conforms to the PCI Specification Revision 2.1
  - Generic bus interface (5/3.3 V, 32 bits, 33 MHz)
- Implements the required AAL-5 SAR sublayer, ATM layer, and TC sublayer functions.
- Support of AAL-5 processing in hardware
- Software support of non-AAL-5 traffic
- Implements a SONET STS-3c/SDH STM-1 155 Mbps framer function.
- Implements clock recovery/clock synthesizer functions.
- Supports up to 32K virtual channels (VCs).
- 16 VBR traffic shapers for transmission scheduling
- Hardware support of CBR/VBR/ABR/UBR service
- Supports multi-cell burst transfer for transmission and reception.
- Implements an MIB counter.
- Supports the LAN emulation function.
- Receive FIFO which can contain up to 96 cells
- UTOPIA Level-1 interface for an external PHY layer device
- 0.35 μm CMOS technology and +5/3.3 V power supply
  - Bus interface +5 V: +5/3.3 V power supply
  - Bus interface +3.3 V: Single +3.3 V power supply
- 304-pin plastic QFP, 304-pin plastic FBGA

1.2 ORDERING INFORMATION

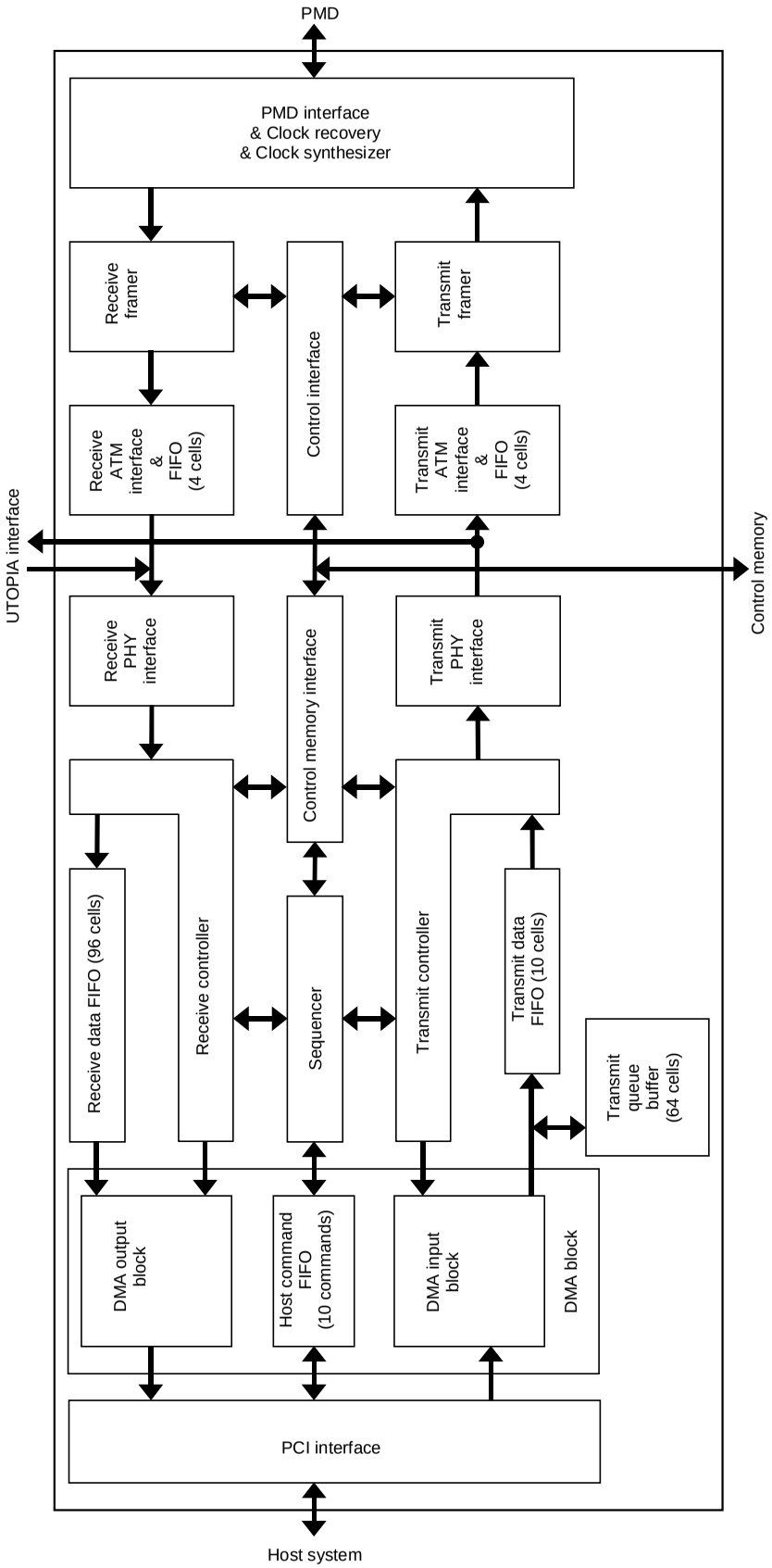
Part Number	Package
μPD98405GL-PMU	304-pin plastic QFP (0.5 mm, fine pitch) (40 x 40 mm)
★ μPD98405S1-6C	304-pin plastic FBGA (0.8 mm pitch) (19 x 19 mm)

1.3 APPLICATION EXAMPLE

ATM interface card



1.4 BLOCK DIAGRAM

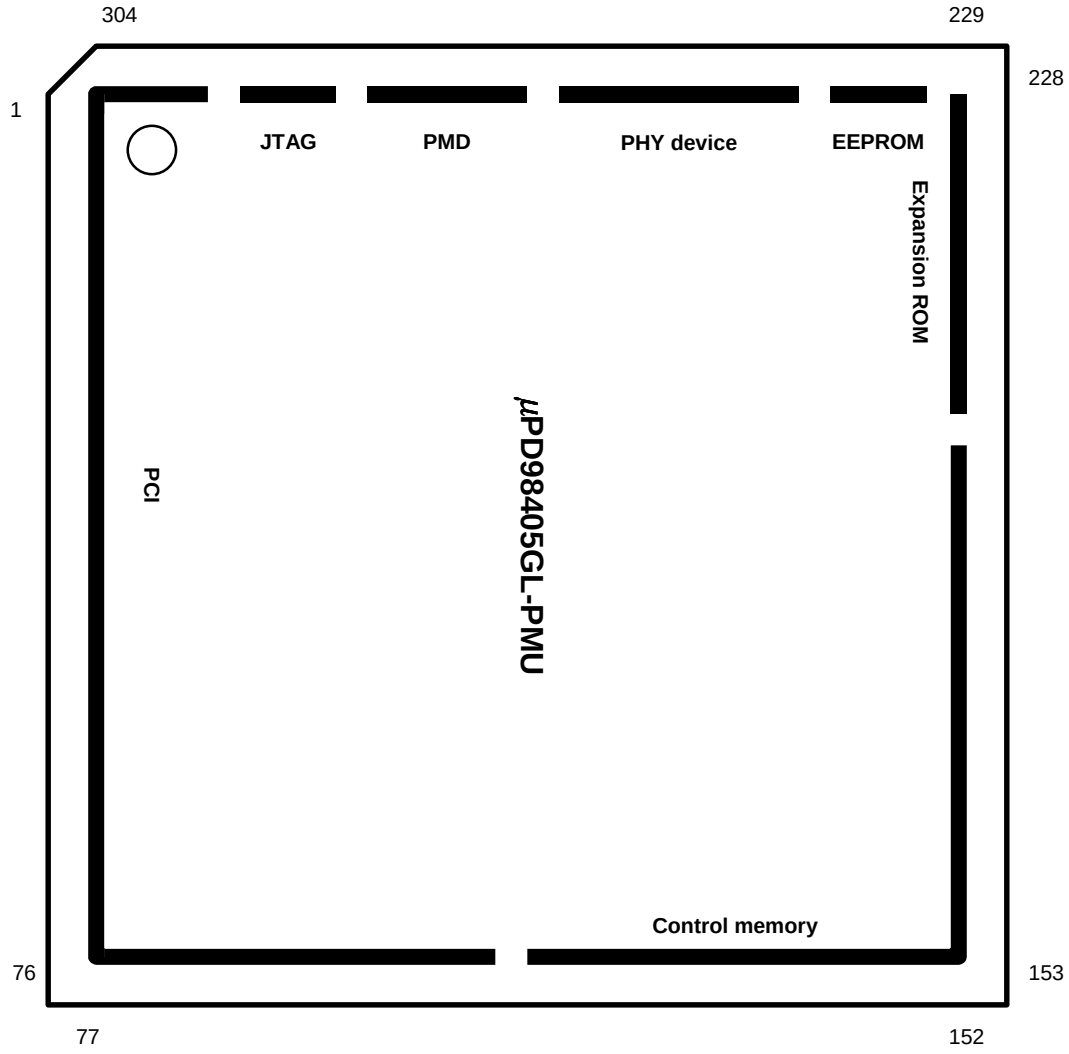


[MEMO]

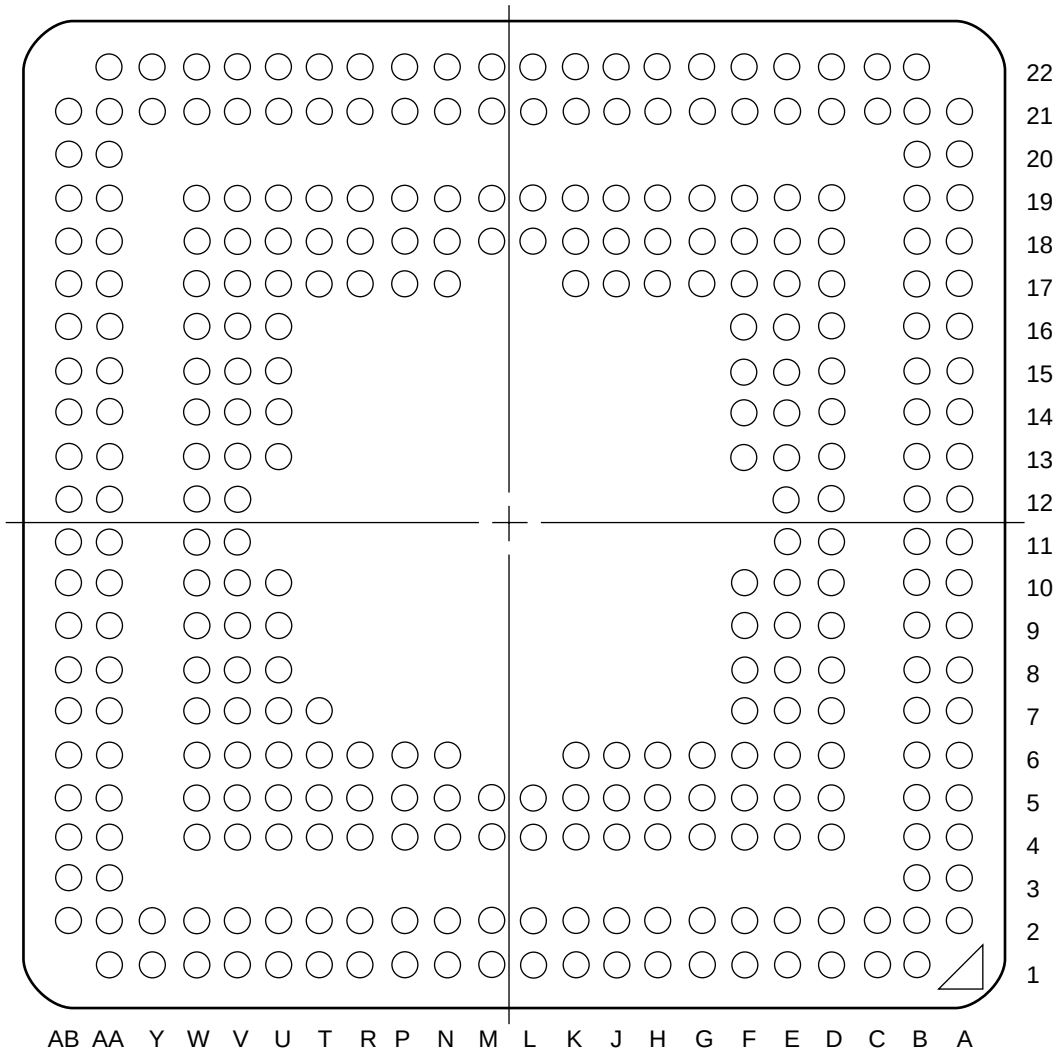
CHAPTER 2 PIN FUNCTIONS

2.1 PIN CONFIGURATION

- **304-pin plastic QFP (0.5 mm, fine pitch) (40 x 40 mm)**



★ • **304-pin plastic FBGA (0.8 mm pitch) (19 x 19 mm) (Bottom View)**



Pin Names

ABRT_B : Abort
ACK64_B : Acknowledge 64 bit Transfer
AD63-AD0 : Address/Data
AGND : Ground for Analog Part
ASEL_B : Slave Address Select
ATTN_B : Attention
AV_{DD3} : +3.3 V Power Supply for Analog Part
BE3_B-BE0_B : Byte Enable
CA18-CA0 : Control Memory Address
CBE3_B-CBE0_B : Local Port Byte Enable
CD31-CD0 : Control Memory Data
CLK : Clock
COE_B : Control Memory Output Enable
CPAR3-CPAR0 : Control Memory Parity
CWE_B : Control Memory Write Enable
DEVSEL_B : Device Select
DR/W_B : DMA Read/Write
EMPTY_B/RCLAV : PHY Empty/Rx Cell Available
ERR_B : Error
E2PCLK : Clock for EEPROM
E2PCS : EEPROM Chip Select
E2PDI : Serial Data Input from EEPROM
E2PDO : Serial Data Output from EEPROM
FRAME_B : Cycle Frame
FULL_B/TCLAV : PHY Buffer full/Tx Cell Available
GND : Ground for Digital Part
GNT_B : Grant
HGND : Ground for High-Speed Part
HV_{DD3} : +3.3 V Power Supply for High-Speed Part
IDSEL : ID Select
INITD : Initialization Disable
INTR_B : Interrupt
IRDY_B : Initiator Ready
JCK : JTAG Test Pin
JDI : JTAG Test Pin
JDO : JTAG Test Pin
JMS : JTAG Test Pin
JRST_B : JTAG Test Pin
OE_B : Output Enable
PAR : Parity
PAR3-PAR0 : Bus Parity
PAR64 : Parity 64 bit
PCBE7_B-PCBE0_B : Bus Command and Byte Enables
PCI_MODE : PCI Mode
PERR_B : Parity Error
PHCE_B : PHY Chip Enable
PHINT_B : PHY Interrupt
PHOE_B : PHY Output Enable
PHRST_B : PHY Reset
PHR/W_B : PHY Read/Write
PHYALM : Physical Alarm
RCIC : Receive Clock Input Complement
RCIT : Receive Clock Input True
RCLK : Receive Clock
RDIC : Receive Data Input Complement
RDIT : Receive Data Input True
RDY_B : Target Ready
REFCLK : Reference Clock
RENBL_B : Receive Enable
REQ64_B : Request 64 bit Transfer
REQ_B : Request
RGND : Ground for Receive PLL Part
ROMA15-ROMA0 : Expansion ROM Address
ROMCS_B : Expansion ROM Chip Select
ROMD7-ROMD0 : Expansion ROM Input Data
ROMOE_B : Expansion ROM Output Enable
RSOC : Receive Start Cell
RST_B : Reset
RV_{DD3} : +3.3 V Power Supply for Receive PLL Part
Rx7-Rx0 : Receive Data Bus
SCLK : SAR System Clock
SD : Signal Detect
SEL_B : Slave Select
SERR_B : System Error
SIZE2-SIZE0 : Burst Size
SR/W_B : Slave Read/Write
STOP_B : Stop
TCLK : Transmit Clock
TDOC : Transmit Data Output Complement
TDOT : Transmit Data Output True
TENBL_B : Transmit Enable
TEST : Test Mode Pin
TFKC : Transmit Reference Clock Complement
TFKT : Transmit Reference Clock True
TRDY_B : Target Ready
TSOC : Transmit Start of Cell
Tx7-Tx0 : Transmit Data Bus
V_{DD3} : +3.3 V Power Supply for Digital Part
V_{DD5} : +5 V Power Supply for Digital Part

2.2 PIN ASSIGNMENT

- **304-pin plastic QFP (0.5 mm, fine pitch) (40 x 40 mm)**

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No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode
1	GND	GND	38	V_{DD3}	V_{DD3}	75	AD58	-	112	AD35	-
2	V_{DD3}	V_{DD3}	39	AD12	AD12	76	GND	GND	113	AD34	-
3	AD24	AD24	40	AD11	AD11	77	GND	GND	114	AD33	-
4	PCBE3_B	BE3_B	41	AD10	AD10	78	V_{DD3}	V_{DD3}	115	AD32	-
5	IDSEL	-	42	AD9	AD9	79	AD57	-	116	PAR64	-
6	AD23	AD23	43	GND	GND	80	AD56	-	117	GND	GND
7	GND	GND	44	V_{DD5}	V_{DD5}	81	V_{DD5}	V_{DD5}	118	PCI_MODE	PCI_MODE
8	V_{DD5}	V_{DD5}	45	AD8	AD8	82	AD55	-	119	CD31	CD31
9	AD22	AD22	46	PCBE0_B	BE0_B	83	AD54	-	120	CD30	CD30
10	AD21	AD21	47	AD7	AD7	84	AD53	-	121	CD29	CD29
11	AD20	AD20	48	AD6	AD6	85	AD52	-	122	CD28	CD28
12	AD19	AD19	49	GND	GND	86	GND	GND	123	CD27	CD27
13	GND	GND	50	V_{DD3}	V_{DD3}	87	V_{DD3}	V_{DD3}	124	GND	GND
14	V_{DD3}	V_{DD3}	51	AD5	AD5	88	AD51	-	125	V_{DD3}	V_{DD3}
15	AD18	AD18	52	AD4	AD4	89	AD50	-	126	CD26	CD26
16	AD17	AD17	53	AD3	AD3	90	AD49	-	127	CD25	CD25
17	AD16	AD16	54	AD2	AD2	91	AD48	-	128	CD24	CD24
18	PCBE2_B	BE2_B	55	GND	GND	92	GND	GND	129	CD23	CD23
19	GND	GND	56	V_{DD5}	V_{DD5}	93	V_{DD5}	V_{DD5}	130	CD22	CD22
20	V_{DD5}	V_{DD5}	57	AD1	AD1	94	AD47	-	131	GND	GND
21	FRAME_B	SEL_B	58	AD0	AD0	95	AD46	-	132	CD21	CD21
22	IRDY_B	ASEL_B	59	ACK64_B	OE_B	96	AD45	-	133	CD20	CD20
23	TRDY_B	RDY_B	60	REQ64_B	DR/W_B	97	AD44	-	134	CD19	CD19
24	DEVSEL_B	SR/W_B	61	GND	GND	98	GND	GND	135	CD18	CD18
25	GND	GND	62	V_{DD3}	V_{DD3}	99	V_{DD3}	V_{DD3}	136	CD17	CD17
26	V_{DD3}	V_{DD3}	63	PCBE7_B	SIZE2	100	AD43	-	137	GND	GND
27	STOP_B	ABRT_B	64	PCBE6_B	SIZE1	101	AD42	-	138	V_{DD3}	V_{DD3}
28	PERR_B	ERR_B	65	PCBE5_B	SIZE0	102	AD41	-	139	CD16	CD16
29	SERR_B	-	66	PCBE4_B	PAR3	103	AD40	-	140	CD15	CD15
30	PAR	-	67	V_{DD5}	V_{DD5}	104	GND	GND	141	CD14	CD14
31	GND	GND	68	GND	GND	105	V_{DD5}	V_{DD5}	142	CD13	CD13
32	V_{DD5}	V_{DD5}	69	AD63	PAR2	106	AD39	-	143	CD12	CD12
33	PCBE1_B	BE1_B	70	AD62	PAR1	107	AD38	-	144	CD11	CD11
34	AD15	AD15	71	AD61	PAR0	108	AD37	-	145	GND	GND
35	AD14	AD14	72	V_{DD3}	V_{DD3}	109	AD36	-	146	CD10	CD10
36	AD13	AD13	73	AD60	-	110	GND	GND	147	CD9	CD9
37	GND	GND	74	AD59	-	111	V_{DD3}	V_{DD3}	148	CD8	CD8

(2/2)

No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode
149	CD7	CD7	188	CA0	CA0	227	V_{DD3}	V_{DD3}	266	PHYALM/ PHR/W_B	PHYALM/ PHR/W_B
150	CD6	CD6	189	GND	GND	228	GND	GND	267	SD/PHCE_B	SD/PHCE_B
151	V_{DD3}	V_{DD3}	190	V_{DD3}	V_{DD3}	229	GND	GND	268	REFCLK/ PHINT_B	REFCLK/ PHINT_B
152	GND	GND	191	CBE3_B	CBE3_B	230	ROMOE_B	-	269	AV_{DD3}	AV_{DD3}
153	GND	GND	192	CBE2_B	CBE2_B	231	E2PDI	-	270	AGND	AGND
154	V_{DD3}	V_{DD3}	193	CBE1_B	CBE1_B	232	E2PDO	-	271	TEST	TEST
155	CD5	CD5	194	CBE0_B	CBE0_B	233	E2PCLK	-	272	HGND	HGND
156	CD4	CD4	195	CWE_B	CWE_B	234	E2PCS	-	273	TDOT	TDOT
157	CD3	CD3	196	COE_B	COE_B	235	Rx7	Rx7	274	TDOC	TDOC
158	CD2	CD2	197	INITD	INITD	236	Rx6	Rx6	275	HV_{DD3}	HV_{DD3}
159	CD1	CD1	198	SCLK	SCLK	237	Rx5	Rx5	276	HV_{DD3}	HV_{DD3}
160	GND	GND	199	GND	GND	238	Rx4	Rx4	277	RDIC	RDIC
161	CD0	CD0	200	ROMA15	-	239	Rx3	Rx3	278	RDIT	RDIT
162	CPAR3	CPAR3	201	ROMA14	-	240	Rx2	Rx2	279	HGND	HGND
163	CPAR2	CPAR2	202	ROMA13	-	241	Rx1/TFKC	Rx1/TFKC	280	RV_{DD3}	RV_{DD3}
164	CPAR1	CPAR1	203	ROMA12	-	242	Rx0/TFKT	Rx0/TFKT	281	JRST_B	JRST_B
165	CPAR0	CPAR0	204	ROMA11	-	243	GND	GND	282	JCK	JCK
166	CA18	CA18	205	ROMA10	-	244	RCLK	RCLK	283	JMS	JMS
167	GND	GND	206	ROMA9	-	245	V_{DD3}	V_{DD3}	284	JDO	JDO
168	CA17	CA17	207	ROMA8	-	246	RENBL_B	RENBL_B	285	JDI	JDI
169	CA16	CA16	208	V_{DD3}	V_{DD3}	247	RSOC	RSOC	286	RGND	RGND
170	CA15	CA15	209	ROMA7	-	248	EMPTY_B/ RCLAV/RCIC	EMPTY_B/ RCLAV/RCIC	287	V_{DD5}	V_{DD5}
171	CA14	CA14	210	ROMA6	-	249	FULL_B/ TCLAV/RCIT	FULL_B/ TCLAV/RCIT	288	INTR_B	INTR_B
172	CA13	CA13	211	ROMA5	-	250	TSOC	TSOC	289	RST_B	RST_B
173	CA12	CA12	212	ROMA4	-	251	TENBL_B	TENBL_B	290	CLK	CLK
174	GND	GND	213	ROMA3	-	252	GND	GND	291	GNT_B	GNT_B
175	V_{DD3}	V_{DD3}	214	GND	GND	253	TCLK	TCLK	292	GND	GND
176	CA11	CA11	215	ROMA2	-	254	V_{DD3}	V_{DD3}	293	V_{DD3}	V_{DD3}
177	CA10	CA10	216	ROMA1	-	255	Tx7	Tx7	294	REQ_B	ATTN_B
178	CA9	CA9	217	ROMA0	-	256	Tx6	Tx6	295	AD31	AD31
179	CA8	CA8	218	ROMD7	-	257	Tx5	Tx5	296	AD30	AD30
180	CA7	CA7	219	ROMD6	-	258	Tx4	Tx4	297	AD29	AD29
181	CA6	CA6	220	ROMD5	-	259	GND	GND	298	GND	GND
182	GND	GND	221	ROMD4	-	260	Tx3	Tx3	299	V_{DD5}	V_{DD5}
183	CA5	CA5	222	ROMD3	-	261	Tx2	Tx2	300	AD28	AD28
184	CA4	CA4	223	ROMD2	-	262	Tx1	Tx1	301	AD27	AD27
185	CA3	CA3	224	ROMD1	-	263	Tx0	Tx0	302	AD26	AD26
186	CA2	CA2	225	ROMD0	-	264	PHRST_B	PHRST_B	303	AD25	AD25
187	CA1	CA1	226	ROMCS_B	-	265	PHOE_B	PHOE_B	304	GND	GND

Remark When using this chip in Generic mode, leave those pins to which no function is assigned (those pins marked with "-") other than pin No. 5 (IDSEL) open. Fix IDSEL to low/high.

★ • **304-pin plastic FBGA (0.8 mm pitch) (19 x 19 mm)**

(1/2)

No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode
B2	GND	GND	M1	AD11	AD11	W4	AD57	-	V12	PCI_MODE	PCI_MODE
C2	V_{DD3}	V_{DD3}	M2	AD10	AD10	AB3	AD56	-	U13	CD31	CD31
B1	AD24	AD24	M5	AD9	AD9	AA4	V_{DD5}	V_{DD5}	V13	CD30	CD30
C1	PCBE3_B	BE3_B	N6	GND	GND	U6	AD55	-	AB13	CD29	CD29
D2	IDSEL	-	N5	V_{DD5}	V_{DD5}	W5	AD54	-	AA13	CD28	CD28
E5	AD23	AD23	N1	AD8	AD8	AA5	AD53	-	W13	CD27	CD27
E4	GND	GND	N2	PCBE0_B	BE0_B	AB4	AD52	-	U14	GND	GND
E2	V_{DD5}	V_{DD5}	N4	AD7	AD7	V6	GND	GND	V14	V_{DD3}	V_{DD3}
D1	AD22	AD22	P6	AD6	AD6	W6	V_{DD3}	V_{DD3}	AB14	CD26	CD26
F5	AD21	AD21	P5	GND	GND	V7	AD51	-	AA14	CD25	CD25
F4	AD20	AD20	P1	V_{DD3}	V_{DD3}	AB5	AD50	-	W14	CD24	CD24
G5	AD19	AD19	P2	AD5	AD5	AA6	AD49	-	AB15	CD23	CD23
E1	GND	GND	P4	AD4	AD4	AB6	AD48	-	AA15	CD22	CD22
F2	V_{DD3}	V_{DD3}	R1	AD3	AD3	U7	GND	GND	W15	GND	GND
F1	AD18	AD18	R2	AD2	AD2	W7	V_{DD5}	V_{DD5}	U15	CD21	CD21
G6	AD17	AD17	R4	GND	GND	AA7	AD47	-	V15	CD20	CD20
G4	AD16	AD16	R6	V_{DD5}	V_{DD5}	AB7	AD46	-	AB16	CD19	CD19
G2	PCBE2_B	BE2_B	R5	AD1	AD1	V8	AD45	-	AA16	CD18	CD18
G1	GND	GND	T1	AD0	AD0	U8	AD44	-	W16	CD17	CD17
H5	V_{DD5}	V_{DD5}	T2	ACK64_B	OE_B	W8	GND	GND	U16	GND	GND
H6	FRAME_B	SEL_B	T4	REQ64_B	DR/W_B	AA8	V_{DD3}	V_{DD3}	AB17	V_{DD3}	V_{DD3}
H4	IRDY_B	ASEL_B	T6	GND	GND	AB8	AD43	-	AA17	CD16	CD16
H2	TRDY_B	RDY_B	U1	V_{DD3}	V_{DD3}	W9	AD42	-	AB18	CD15	CD15
H1	DEVSEL_B	SR/W_B	U2	PCBE7_B	SIZE2	AA9	AD41	-	V16	CD14	CD14
J4	GND	GND	V1	PCBE6_B	SIZE1	AB9	AD40	-	W17	CD13	CD13
J2	V_{DD3}	V_{DD3}	T5	PCBE5_B	SIZE0	V9	GND	GND	V17	CD12	CD12
J1	STOP_B	ABRT_B	U4	PCBE4_B	PAR3	U9	V_{DD5}	V_{DD5}	AB19	CD11	CD11
J5	PERR_B	ERR_B	U5	V_{DD5}	V_{DD5}	W10	AD39	-	AA18	GND	GND
J6	SERR_B	-	W1	GND	GND	AA10	AD38	-	W18	CD10	CD10
K4	PAR	-	V2	AD63	PAR2	AB10	AD37	-	U17	CD9	CD9
K2	GND	GND	V4	AD62	PAR1	V10	AD36	-	AA19	CD8	CD8
K1	V_{DD5}	V_{DD5}	V5	AD61	PAR0	U10	GND	GND	AB20	CD7	CD7
K5	PCBE1_B	BE1_B	W2	V_{DD3}	V_{DD3}	V11	V_{DD3}	V_{DD3}	W19	CD6	CD6
K6	AD15	AD15	Y1	AD60	-	AA11	AD35	-	AA20	V_{DD3}	V_{DD3}
L5	AD14	AD14	AA1	AD59	-	AB11	AD34	-	AB21	GND	GND
L2	AD13	AD13	Y2	AD58	-	W11	AD33	-	AA21	GND	GND
L1	GND	GND	AA2	GND	GND	W12	AD32	-	Y21	V_{DD3}	V_{DD3}
L4	V_{DD3}	V_{DD3}	AB2	GND	GND	AB12	PAR64	-	AA22	CD5	CD5
M4	AD12	AD12	AA3	V_{DD3}	V_{DD3}	AA12	GND	GND	Y22	CD4	CD4

(2/2)

No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode	No.	PCI mode	Generic mode
W21	CD3	CD3	L18	CBE0_B	CBE0_B	D19	E2PDI	-	A11	REFCLK/ PHINT_B	REFCLK/ PHINT_B
V18	CD2	CD2	K17	CWE_B	CWE_B	A20	E2PDO	-	B11	AV_{DD3}	AV_{DD3}
V19	CD1	CD1	K18	COE_B	COE_B	B19	E2PCLK	-	E11	AGND	AGND
V21	GND	GND	K22	INITD	INITD	F17	E2PCS	-	F10	TEST	TEST
W22	CD0	CD0	K21	SCLK	SCLK	D18	Rx7	Rx7	E10	HGND	HGND
U18	CPAR3	CPAR3	K19	GND	GND	B18	Rx6	Rx6	A10	TDOT	TDOT
U19	CPAR2	CPAR2	J17	ROMA15	-	A19	Rx5	Rx5	B10	TDOC	TDOC
T18	CPAR1	CPAR1	J18	ROMA14	-	E17	Rx4	Rx4	D10	HV_{DD3}	HV_{DD3}
V22	CPAR0	CPAR0	J22	ROMA13	-	D17	Rx3	Rx3	F9	HV_{DD3}	HV_{DD3}
U21	CA18	CA18	J21	ROMA12	-	E16	Rx2	Rx2	E9	RDIC	RDIC
U22	GND	GND	J19	ROMA11	-	A18	Rx1/TFKC	Rx1/TFKC	A9	RDIT	RDIT
T17	CA17	CA17	H22	ROMA10	-	B17	Rx0/TFKT	Rx0/TFKT	B9	HGND	HGND
T19	CA16	CA16	H21	ROMA9	-	A17	GND	GND	D9	RV_{DD3}	RV_{DD3}
T21	CA15	CA15	H19	ROMA8	-	F16	RCLK	RCLK	A8	JRST_B	JRST_B
T22	CA14	CA14	H17	V_{DD3}	V_{DD3}	D16	V_{DD3}	V_{DD3}	B8	JCK	JCK
R18	CA13	CA13	H18	ROMA7	-	B16	RENBL_B	RENBL_B	D8	JMS	JMS
R17	CA12	CA12	G22	ROMA6	-	A16	RSOC	RSOC	F8	JDO	JDO
R19	GND	GND	G21	ROMA5	-	E15	EMPTY_B/ RCLAV/ RCIC	EMPTY_B RCLAV/ RCIC	E8	JDI	JDI
R21	V_{DD3}	V_{DD3}	G19	ROMA4	-	F15	FULL_B/ TCLAV/ RCIT	FULL_B/ TCLAV/ RCIT	A7	RGND	RGND
R22	CA11	CA11	G17	ROMA3	-	D15	TSOC	TSOC	B7	V_{DD5}	V_{DD5}
P19	CA10	CA10	F22	GND	GND	B15	TENBL_B	TENBL_B	D7	INTR_B	INTR_B
P21	CA9	CA9	F21	ROMA2	-	A15	GND	GND	F7	RST_B	RST_B
P22	CA8	CA8	E22	ROMA1	-	D14	TCLK	TCLK	A6	CLK	CLK
P18	CA7	CA7	G18	ROMA0	-	B14	V_{DD3}	V_{DD3}	B6	GNT_B	GNT_B
P17	CA6	CA6	F19	ROMD7	-	A14	Tx7	Tx7	A5	GND	GND
N19	GND	GND	F18	ROMD6	-	E14	Tx6	Tx6	E7	V_{DD3}	V_{DD3}
N21	CA5	CA5	D22	ROMD5	-	F14	Tx5	Tx5	D6	REQ_B	ATTN_B
N22	CA4	CA4	E21	ROMD4	-	D13	Tx4	Tx4	E6	AD31	AD31
N18	CA3	CA3	E19	ROMD3	-	B13	GND	GND	A4	AD30	AD30
N17	CA2	CA2	E18	ROMD2	-	A13	Tx3	Tx3	B5	AD29	AD29
M18	CA1	CA1	D21	ROMD1	-	E13	Tx2	Tx2	D5	GND	GND
M21	CA0	CA0	C22	ROMD0	-	F13	Tx1	Tx1	F6	V_{DD5}	V_{DD5}
M22	GND	GND	B22	ROMCS_B	-	E12	Tx0	Tx0	B4	AD28	AD28
M19	V_{DD3}	V_{DD3}	C21	V_{DD3}	V_{DD3}	B12	PHRST_B	PHRST_B	A3	AD27	AD27
L19	CBE3_B	CBE3_B	B21	GND	GND	A12	PHOE_B	PHOE_B	D4	AD26	AD26
L22	CBE2_B	CBE2_B	A21	GND	GND	D12	PHYALM/ PHR/W_B	PHYALM/ PHR/W_B	B3	AD25	AD25
L21	CBE1_B	CBE1_B	B20	ROMOE_B	-	D11	SD/ PHCE_B	SD/ PHCE_B	A2	GND	GND

Remark When using this chip in Generic mode, leave those pins to which no function is assigned (those pins marked with "-") other than pin No. 5 (IDSEL) open. Fix IDSEL to low/high.

2.3 PIN FUNCTIONS

The μPD98405 is packaged in a 304-pin package. See **Chapter 4** for details of the pin functions and notes on use.

2.3.1 PHY Layer Device Interface Signals

Signals for interfacing with the PHY layer device are classified into UTOPIA interface signals used to transfer ATM cells between the μPD98405 and PHY device and PHY control interface signals used to control the PHY device.

The μPD98405 supports octet-level and cell-level modes for the UTOPIA interface. These modes are selected by setting the UOC bit of the GMR register.

The PHY layer device interface signals are for use with an external PHY layer device. When using the internal PHY layer, leave other than the common pins open. Even when using the internal PHY layer, however, an external receive FIFO can be connected to the μPD98405 via a UTOPIA interface. (See **Section 4.3.1 (3)**.)

(1) UTOPIA interface

(1/2)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
Rx7-Rx0 (Rx1, Rx0: Common with TFKC and TFKT pins)	235-242	D18, B18, A19, E17, D17, E16, A18, B17	I	TTL	Receive Data Bus Rx7-Rx0 is an 8-bit input bus used to receive the network traffic in byte form from the PHY layer device. The eight bits are input to the μPD98405 in synchronization with the rising edge of RCLK. Rx7-Rx2 : Internal pull-down signal. Leave open when not used. Rx1 : Connect a pull-down resistor when not used. Rx0 : Connect a pull-up resistor when not used.
RSOC	247	A16	I	TTL	Receive Start of Cell The RSOC signal is input in synchronization with the first byte of cell data received from the PHY layer device. Keep this signal high while the first byte of the header is being input to Rx7-Rx0. These pins are connected to internal pull-down resistors.
RENBL_B	246	B16	O	TTL	Receive Enable The RENBL_B signal indicates to the PHY layer device that the μPD98405 is ready to accept data in the next clock cycle.

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Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
EMPTY_B/ RCLAV (Common with RCIC pin)	248	E15	I	TTL	PHY Layer Buffer Empty/Receive Cell Available The EMPTY_B/RCLAV signal indicates, to the μPD98405, that the receive FIFO of the PHY device contains no cell data to be transferred and that the PHY device cannot provide receive data. When the UTOPIA interface is in octet-level handshaking mode, this pin functions as the EMPTY_B pin. The EMPTY_B signal indicates that data on Rx7 to Rx0 is invalid in the current clock cycle. In cell-level handshaking mode, this pin functions as the RCLAV pin. The RCLAV signal indicates that there are no more cells to be transferred once the current cell has been transferred. Connect a pull-down resistor when the EMPTY_B/RCLAV pin is not used.
RCLK	244	F16	O	TTL	Receive Clock The RCLK signal is a clock used to synchronize the reception of cell data from the PHY layer device. Once the system has been reset, the SAR system clock, input to the SCLK pin, is output as is.
Tx7-Tx0	255-258, 260-263	A14, E14, F14, D13, A13, E13, F13, E12	O	TTL	Transmit Data Bus Tx7 to Tx0 is an 8-bit output bus used to transmit the network traffic in byte form to the PHY layer device. The eight bits are output to the PHY layer device in synchronization with the rising edge of TCLK.
TSOC	250	D15	O	TTL	Transmit Start of Cell The TSOC signal is output in synchronization with the first byte of cell data to be transmitted.
TENBL_B	251	B15	O	TTL	Transmit Enable The TENBL_B signal indicates to the PHY layer device that Tx7 to Tx0 carries transmit data in the current clock cycle.
FULL_B/ TCLAV (Common with RCIT pin)	249	F15	I	TTL	PHY Layer Buffer Full/Transmit Cell Available The FULL_B signal indicates to the μPD98405 that the input buffer of the PHY device is full and cannot accept additional data. When the UTOPIA interface is in octet-level handshaking mode, the PHY device makes this signal inactive when it can receive cell data. In cell-level handshaking mode, this pin functions as the TCLAV pin. The PHY device inputs the signal to indicate that it can receive all the data in the next cell, once the current cell has been transferred. Connect a pull-up resistor when the FULL_B/TCLAV pin is not used.
TCLK	253	D14	O	TTL	Transmit Clock The TCLK signal is a clock used to synchronize the transmission of cell data to the PHY layer device. The SAR system clock, input to the SCLK pin, is output as is.

(2) PHY device control interface (External PHY mode: PHM of the GMR register = 1)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
PHR/W_B (Common with PHYALM pin)	266	D12	O	TTL	PHY Read/Write The PHR/W_B is asserted by the μPD98405 to indicate the direction of the PHY layer device control transaction. 1: Read 0: Write
PHOE_B	265	A12	O	TTL	PHY Layer Output Enable The PHOE_B is set to low by the μPD98405 to enable data output from the PHY layer device.
PHCE_B (Common with SD pin)	267	D11	O	TTL	PHY Layer Chip Enable The PHCE_B is set to low by the μPD98405 when it accesses the PHY layer device.
PHINT_B (Common with REFCLK pin)	268	A11	I	TTL	PHY Layer Interrupt The PHINT_B pin accepts an interrupt signal from the PHY layer device. If any interrupt occurs in the PHY layer device, it notifies the μPD98405 of the interrupt by driving PHINT_B low. Connect a pull-up resistor when the PHINT_B pin is not used.
PHRST_B	264	B12	O	TTL	PHY Layer Reset The PHRST_B signal is used to reset the PHY layer device. When a low level is input to RST_B or when a software reset is performed, the μPD98405 drives PHRST_B low for 17 clock cycles.

Caution The PHCE_B/SD pin has two functions. Which function is used depends on internal PHY mode or external PHY mode selected by the PHM bit of the GMR register. Since I/O of the PHCE_B/SD pin is switched according to mode switching, set the PHM bit of the GMR register carefully.

2.3.2 Bus Interface Signals

The μPD98405 supports a PCI or Generic bus interface. PCI or Generic mode is selected using the PCI_MODE signal.

The PCI bus interface can be connected directly to the PCI bus. The Generic bus interface can be connected to a general I/O bus with a minimum of external circuitry.

(1) Generic bus interface signals (Level of the PCI_MODE pin: Low)

(1/4)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
AD31-AD0	295-297, 300-303, 3, 6, 9-12, 15-17, 34-36, 39-42, 45, 47, 48, 51-54, 57, 58	E6, A4, B5, B4, A3, D4, B3, B1, E5, D1, F5, F4, G5, F1, G6, G4, K6, L5, L2, M4, M1, M2, M5, N1, N4, P6, P2, P4, R1, R2, R5, T1	I/O 3-state	TTL	Address/Data The AD31 to AD0 bus is a 32-bit, bi-directional, multiplexed address/data bus. During the first clock of a transaction, AD31 to AD0 contains a physical byte address. During subsequent clocks, AD31 to AD0 contains data. When the μPD98405 is not accessing the bus, it places the AD bus in the high impedance state.
BE3_B BE2_B BE1_B BE0_B	4 18 33 46	C1 G2 K5 N2	O 3-state	TTL	Byte Enable The BE3_B to BE0_B signals determine whether their corresponding bytes are valid in the μPD98405 master cycle. BE3_B corresponds to AD31 to AD24; BE0_B to AD7 to AD0. When the μPD98405 is not accessing the bus or accessing the bus as the slave, the BE3_B to BE0_B signals are placed in the high impedance state.
PAR3 PAR2 PAR1 PAR0	66 69 70 71	U4 V2 V4 V5	I/O 3-state	TTL	Bus Parity The PAR indicates the parity across AD31 to AD0. Parity checking is configured by setting the appropriate bits in the GMR. Parity checking may be enabled/disabled, even/odd, byte or word. When configured as byte parity, PAR3 represents AD31 to AD24 while PAR0 represents AD7 to AD0. When configured as word parity, PAR2 to PAR0 have no functions while PAR3 is a bi-directional signal: an output during address and write data phases and input during read data phases. When the μPD98405 is not accessing the bus it places PAR3 to PAR0 in the high impedance state. Connect a pull-up resistor when unused.

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<table>
<tr><th rowspan="2">Symbol</th><th colspan="2">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">I/O level</th><th rowspan="2">Function</th></tr>
<tr><th>QFP</th><th>FBGA</th></tr>
<tr><td>OE_B</td><td>59</td><td>T2</td><td>I</td><td>TTL</td><td>Output Enable
When the OE_B signal is low, the μPD98405 controls AD31 to AD0 and PAR3 to PAR0 as 3-state bidirectional pins (normal operation). When the OE_B signal is high, these pins are placed in the high impedance state. This signal is optional. Fix it to low unless the above pins need be forcibly set to high impedance.</td></tr>
<tr><td>SIZE2
SIZE1
SIZE0</td><td>63
64
65</td><td>U2
V1
T5</td><td>O</td><td>TTL</td><td>Burst Size
The SIZE2 to SIZE0 signals indicate the size of the current DMA transfer. These pins are provided to support interface to buses that require an explicit burst size (e.g., S bus).
<table>
<tr><th>SIZE2</th><th>SIZE1</th><th>SIZE0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>One-word transfer</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Two-word burst</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Four-word burst</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Eight-word burst</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Sixteen-word burst</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Twelve-word burst</td></tr>
<tr><td colspan="3">Others</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>DR/W_B</td><td>60</td><td>T4</td><td>O</td><td>TTL</td><td>DMA Read/Write
The DR/W_B signal determines the direction of DMA access.
1: Read access
0: Write access</td></tr>
<tr><td>ATTN_B</td><td>294</td><td>D6</td><td>O</td><td>TTL</td><td>Attention (DMA request)
The μPD98405 sets the ATTN_B signal to low when attempting to start DMA operation. Once only one word remains to be transferred, the ATTN_B signal becomes inactive at the rising edge of CLK.</td></tr>
<tr><td>GNT_B</td><td>291</td><td>B6</td><td>I</td><td>TTL</td><td>Grant
Set the GNT_B signal to low once the bus arbiter has granted bus mastership in response to a DMA request from the μPD98405. By detecting the GNT_B signal being set to active low, the μPD98405 assumes that bus mastership has been granted and starts DMA operation.</td></tr>
<tr><td>RDY_B</td><td>23</td><td>H2</td><td>I</td><td>TTL</td><td>Target Device Ready
RDY_B is used in DMA cycles to indicate to the μPD98405 that the transaction's target device is ready to input/output data. During the μPD98405 DMA read operation, the RDY_B signal should go low when valid data is present on AD31 to AD0. During the μPD98405 DMA write operation, the ATTN_B signal should go low when the target device is ready to accept data.
The timing at which the μPD98405 samples the RDY_B and ABRT_B signals can be changed to one clock earlier (early mode) by setting an internal register (GMR).</td></tr>
</table>

(3/4)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
ABRT_B	27	J1	I	TTL	Abort ABRT_B is used to abort a data transfer cycle. When this signal is low during the data transfer cycle, the cycle is aborted and the μPD98405 will retry the burst starting from the aborted data. Note that the RDY_B signal has no effect if the ABRT_B signal is low. The timing at which the μPD98405 samples the RDY_B and ABRT_B signals can be changed to one clock earlier (early mode) by setting an internal register (GMR). Connect a pull-up resistor when the ABRT_B pin is not used.
ERR_B	28	J5	I	TTL	System Bus Error The ERR_B signal is used by the bus control device to request the μPD98405 to halt operation if an error is detected on the system bus. Once this signal has been set to low, the μPD98405 immediately halts all bus operations, sets the system bus error bit (bit 25) in the GSR (if not masked) to generate an interrupt. Connect a pull-up resistor when this pin is not used.
SR/W_B	24	H1	I	TTL	Slave Read/Write The SR/W_B signal determines the direction of slave access. 1: Read access 0: Write access
SEL_B	21	H6	I	TTL	Slave Select Set the SEL_B signal to active low when selecting the μPD98405 as a slave. The SEL_B signal must be made low either at the same time as when the ASEL_B signal goes low, or subsequently. Once the SEL_B signal has been inactive, it must be held inactive for at least two system clock cycles before it can be active.
ASEL_B	22	H4	I	TTL	Slave Address Select The ASEL_B signal is used to select the μPD98405 directly addressed registers. When ASEL_B is low, the μPD98405 samples the AD lines at the first rising edge of CLK.
CLK	290	A6	I	TTL	Clock CLK is the system bus clock input pin. The clock rate is up to 33 MHz.
RST_B	289	F7	I	TTL	Reset The RST_B signal provides a means of initializing the μPD98405 (i.e. at power on). After the completion of a reset, the μPD98405 can start normal operation. Once RST_B has been set to low, it resets the μPD98405 internal state machines and registers, and forces all 3-state signals to the high impedance state. Reset input is performed asynchronously. If low during operation, current state will be lost. RST_B should be kept low for at least one clock cycle.

(4/4)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
INTR_B	288	D7	O	N-ch open-drain	Interrupt Output It is an open-drain pin and needs pull-up resistor connection. The INTR_B output is used to inform the CPU that an (unmasked) interrupt bit was set in the GSR.

(2) PCI bus interface signals (Level of the PCI_MODE pin: High)

The μPD98405 contains a 32/64-bit PCI bus interface. The PCI bus interface can be connected directly to a PCI bus. The μPD98405 also contains a serial EEPROM interface and expansion ROM interface.

<1> PCI bus interface signals

(1/3)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
AD31-AD0	295-297, 300-303, 3, 6, 9-12, 15-17, 34-36, 39-42, 45, 47, 48, 51-54, 57, 58,	E6, A4, B5, B4, A3, D4, B3, B1, E5, D1, F5, F4,G5, F1, G6, G4, K6, L5, L2, M4, M1, M2, M5, N1, N4, P6, P2, P4, R1, R2, R5, T1	I/O 3-state	PCI	Address/Data AD31 to AD0 constitute a 32-bit multiplexed address/data bus. When the μPD98405 operates as the bus master, it drives an address during the first clock. During subsequent clocks, the μPD98405 transfers data.
PCBE3_B PCBE2_B PCBE1_B PCBE0_B	4 18 33 46	C1 G2 K5 N2	I/O 3-state	PCI	Bus Command/Byte Enable During address phases, the PCBE3_B to PCBE0_B signals define a bus command (bus transaction to be generated). During data phases, these signals indicate whether their corresponding byte lanes contain valid data. The PCBE3_B pin corresponds to byte 3 (bits 31 to 24); the PCBE0_B pin to byte 0 (bits 7 to 0).
PAR	30	K4	I/O 3-state	PCI	Parity The PAR signal indicates the even parity across AD31 to AD0 and PCBE3_B to PCBE0_B including the PAR signal. When the μPD98405 operates as the master, the PAR signal is activated during the address and write data phases. When the μPD98405 operates as the target, the signal is activated during read data phases.
FRAME_B	21	H6	I/O Sustained 3-state	PCI	Frame The FRAME_B signal indicates the start and period of a bus transaction. This signal becoming active indicates that a bus transaction has started. While this signal is active, data is transferred. This signal is deactivated when the last data of the transaction is to be transferred in the next data transfer phase.

(2/3)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
TRDY_B	23	H2	I/O Sustained 3-state	PCI	Target Ready The TRDY_B signal goes low when the target device is ready to complete the transaction during the current data phase. This signal is used together with IRDY_B. When both the IRDY_B and TRDY_B signals are low, read/write data transfer is performed.
IRDY_B	22	H4	I/O Sustained 3-state	PCI	Initiator Ready The IRDY_B signal goes low when the initiator is ready to complete a transaction during the current data phase. This signal is used together with TRDY_B. When both the IRDY_B and TRDY_B signals are low, read/write data transfer is performed. When both FRAME_B and IRDY_B are deactivated, no bus cycles are executed. Until both IRDY_B and TRDY_B are activated, wait cycles are inserted.
STOP_B	27	J1	I/O Sustained 3-state	PCI	Stop The STOP_B signal goes low when the target device requests that the master device stop the current transaction.
DEVSEL_B	24	H1	I/O Sustained 3-state	PCI	Device Select When the μPD98405 operates as the target and recognizes an address after the FRAME_B signal has been activated, it drives the DEVSEL_B signal low. When the μPD98405 operates as the master, it samples the DEVSEL_B signal to check that the target device has been selected.
IDSEL	5	D2	I	PCI	Initial Device Select A high level is input as the IDSEL signal when the configuration register of the μPD98405 is read or written.
REQ_B	294	D6	O[Note]	PCI	Request The μPD98405 drives the REQ_B signal low to request bus mastership from the bus arbiter.
GNT_B	291	B6	I	PCI	Grant When the GNT_B signal is low, it indicates that the bus arbiter has granted bus mastership to the μPD98405.
PERR_B	28	J5	I/O Sustained 3-state	PCI	Parity Error The PERR_B signal is used to indicate that the μPD98405 has detected a data parity error. When the Parity Error Response bit of the configuration register is set to 1, this pin is enabled.

Note "PCI Local Bus Specification Revision 2.1" specifies that, while a low-level signal is being input to the RST_B pin, the REQ_B pin must be set to high impedance. With the μPD98405, however, the REQ_B pin outputs a high level signal.

(3/3)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
SERR_B	29	J6	O	N-ch open-drain	System Error The SERR_B signal is used to indicate that the μPD98405 has detected an address parity error. When both the Parity Error Response and System Error Enable bits of the configuration register are set to 1, this pin is enabled.
INTR_B	288	D7	O	N-ch open-drain	Interrupt Output INTR_B is an open-drain pin to which a pull-up resistor must be connected. INTR_B is used to inform the CPU that an (unmasked) interrupt bit was set in the GSR.
CLK	290	A6	I	PCI	Clock CLK is the system bus clock input pin. The maximum clock rate is 33 MHz.
RST_B	289	F7	I	PCI	Reset The RST_B signal provides a means of initializing the μPD98405 (i.e. at power on). When a low level is input to RST_B, the μPD98405 internal states machines and registers are reset, and all 3-state signals are placed in the high impedance state. Reset input is performed asynchronously. If this signal is input during operation, the current state will be lost. RST_B should be kept low for at least one clock cycle. The μPD98405 should not be accessed for at least 20 clock cycles after the system has been reset.

<2> PCI bus 64-bit expansion interface signals

When a 32-bit PCI bus interface signal is used, leave the AD63-AD32, PCBE7_B-PCBE4_B, and PAR64 signals open.

(1/2)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
AD63-AD32	69-71, 73-75, 79, 80, 82-85, 88-91, 94-97, 100-103, 106-109, 112-115	V2, V4, V5, Y1, AA1, Y2, W4, AB3, U6, W5, AA5, AB4, V7, AB5, AA6, AB6, AA7, AB7, V8, U8, AB8, W9, AA9, AB9, W10, AA10, AB10, V10, AA11, AB11, W11, W12	I/O 3-state	PCI	Address/Data AD63 to AD32 constitute a 32-bit multiplexed address/data bus for PCI bus 64-bit expansion. During address phases, AD63 to AD32 carry the 32 high-order bits of a 64-bit address. During data phases, when both REQ64_B and ACK64_B are asserted, AD64 to AD32 carry the data of the 32 high-order bits for 64-bit data transfer.

(2/2)

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
PCBE7_B PCBE6_B PCBE5_B PCBE4_B	63 64 65 66	U2 V1 T5 U4	I/O 3-state	PCI	Bus Command/Byte Enable During address phases, the PCBE7_B to PCBE4_B signals define a bus command (bus transaction to be generated). During data phases, these signals indicate whether their corresponding byte lanes hold valid data. The PCBE7_B pin corresponds to AD63 to AD56; the PCBE4_B pin to AD39 to AD32.
PAR64	116	AB12	I/O 3-state	PCI	Parity 64 The PAR64 signal indicates the even parity across AD63 to AD32 and PCBE7_B to PCBE4_B including the PAR64 signal. When the μPD98405 is operating as the master, the PAR signal is activated during the address and write data phases. When the μPD98405 operates as the target, the signal is activated during read data phases.
REQ64_B	60	T4	I/O Sustained 3-state	PCI	Request 64 The REQ64_B signal indicates the start and period of a 64-bit bus transaction. When the μPD98405 operates as the master, it activates REQ64_B to request 64-bit data transfer. The timing of REQ64_B is the same as that of FRAME_B. Connect an external pull-up resistor when using a 32-bit PCI bus.
ACK64_B	59	T2	I	PCI	Acknowledge 64 When the μPD98405 operates as the target and recognizes an address after the REQ64_B signal has been activated, it drives the ACK64_B signal low. When the μPD98405 operates as the master, it samples the ACK64_B signal to check that the target device responds to the 64-bit transfer request. The timing of ACK64_B is the same as that of DEVSEL_B. Connect an external pull-up resistor when using a 32-bit PCI bus.

<3> Serial EEPROM interface signals

The μPD98405 features an interface for a serial EEPROM which supports the MICROWIRE™ interface. The contents of the PCI configuration register can be loaded from the connected EEPROM.

Remark NEC recommends the use of the "NM93C46," manufactured by National Semiconductor, as the EEPROM to be connected.

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
E2PCS	234	F17	O	TTL	EEPROM Chip Select E2PCS is the EEPROM chip select signal.
E2PDI	231	D19	I	TTL	EEPROM Data Input Connect E2PDI to the data output pin of the EEPROM. This pin is connected to an internal pull-down resistor.
E2PDO	232	A20	O	TTL	EEPROM Data Output Connect E2PDO to the data input pin of the EEPROM.
E2PCLK	233	B19	O	TTL	EEPROM Clock E2PCLK is used to supply the clock required for data transfer to and from the EEPROM. The clock input to the CLK pin scaled by 36 is output.

<4> Expansion ROM interface signals

The μPD98405 provides an optional expansion ROM interface.

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
ROMA15- ROMA0	200-207, 209-213, 215-217	J17, J18, J22, J21, J19, H22, H21, H19, H18, G22, G21, G19, G17, F21, E22, G18	O	TTL	ROM Address The ROMA15 to ROMA0 signals indicate the address for accessing the 64K expansion ROM.
ROMD7- ROMD0	218 - 225	F19, F18, D22, E21, E19, E18, D21, C22	I	TTL	ROM Data The ROMD7 to ROMD0 signals indicate expansion ROM data. These pins are connected to internal pull-down resistors.
ROMCS_B	226	B22	O	TTL	ROM Select ROMCS_B is the chip select signal for
ROMOE_B	230	B20	O	TTL	ROM Output Enable The ROMOE_B signal is used to enable the output buffer of expansion ROM during a read

2.3.3 Control Memory Interface Signals

The control memory interface is used by the μPD98405 to enable access to the external control memory and external PHY layer device. The interface consists of non-multiplexed 19-bit address and 32-bit data buses. The host can access control memory only via this interface.

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
CD31-CD0	119-123, 126-130, 132-136, 139-144, 146-150, 155-159, 161	U13, V13, AB13, AA13, W13, AB14, AA14, W14, AB15, AA15, U15, V15, AB16, AA16, W16, AA17, AB18, V16, W17, V17, AB19 W18, U17, AA19, AB20, W19, AA22, Y22, W21, V18, V19, W22	I/O 3-state	TTL	Control Memory Data The CD31 to CD0 bus is a 32-bit, bi-directional, 3-state data bus used to transfer data to and from the control memory or the PHY layer device. These pins are connected to internal pull-down resistors.
CPAR3-CPAR0	162-165	U18, U19, T18, V22	I/O	TTL	Control Memory Parity The CPAR3 to CPAR0 signals indicate the parity on each octet of the CD31 to CD0 bus. The μPD98405 checks parity during read cycles (if enabled) and generates parity during write cycle. These pins are connected to internal pull-
CA18-CA0	166, 168-173, 176-181, 183-188	U21, T17, T19, T21, T22, R18, R17, R22, P19, P21, P22, P18, P17, N21, N22, N18, N17, M18, M21	O	TTL	Control Memory Address The 19-bit CA18 to CA0 bus specifies the address of the control memory or PHY layer device for a read or write operation.
CWE_B	195	K17	O	TTL	Control Memory Write Enable The CWE_B signal determines the direction of control memory access. Read access Write access
COE_B	196	K18	O	TTL	Control Memory Output Enable The COE_B signal enables/disables the control memory data output lines.
CBE3_B-CBE0_B	191-194	L19, L22, L21, L18	O	TTL	Local Port Byte Enable The CBE3_B to CBE0_B signals determine which byte or bytes out of the four on the control port is to be written in write cycle, and which of the bytes is read in read cycle.
INITD	197	K22	I	TTL	Initialization Disable The INITD signal is used to disable automatic initialization of the control memory when testing the chip. INITD must be directly connected to GND in normal operation other

2.3.4 PMD Interface Signals (Internal PHY Mode: PHM of the GMR Register = 0)

The PMD interface is used to connect an optical transceiver/receiver module.

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
RDIT	278	A9	I	P-ECL True(+)	Receive Serial Data Input Connect a pull-up resistor when the RDIT pin is not used.
RDIC	277	E9	I	P-ECL Complement (-)	Receive Serial Data Input Connect a pull-down resistor when the RDIC pin is not used.
RCIT (Common with FULL_B pin)	249	F15	I	P-ECL True(+)	Receive serial clock input This pin is used for external clock recovery/synthesizer connection (PLL of the GMR register = 1). Connect a pull-up resistor when the RCIT pin is not used.
RCIC (Common with EMPTY_B pin)	248	E15	I	P-ECL Complement (-)	Receive serial clock input This pin is used for external clock recovery/synthesizer connection (PLL of the GMR register = 1). Connect a pull-down resistor when the RCIC pin is not used.
REFCLK (Common with PHINT_B pin)	268	A11	I	TTL	Reference Clock The REFCLK pin is used to input the system clock (19.44 MHz) to the internal clock recovery/synthesizer. Connect a pull-up resistor when the REFCLK pin is not used.
TDOT	273	A10	O	P-ECL True(+)	Transmit Serial Data Output
TDOC	274	B10	O	P-ECL Complement (-)	Transmit Serial Data Output
TFKT (Common with Rx0 pin)	242	B17	I	P-ECL True(+)	Transmit serial clock input This pin is used for external clock recovery/synthesizer connection (PLL of the GMR register = 1). Connect a pull-up resistor when the TFKT pin is not used.
TFKC (Common with Rx1 pin)	241	A18	I	P-ECL Complement (-)	Transmit serial clock input This pin is used for external clock recovery/synthesizer connection (PLL of the GMR register = 1). Connect a pull-down resistor when the TFKC pin is not used.
PHYALM (Common with PHR/W_B pin)	266	D12	O	TTL	PHY Layer Alarm Detection The PHYALM signal becomes active high when one or more internally monitored error states (CMDARM, LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, and Path RDI) are detected. One or more error states to be indicated can be selected using the internal AMR1 and AMR2 registers.
SD (Common with PHCE_B pin)	267	D11	I	TTL	Signal Detect The SD pin is used to input the signal detect signal (LOS detection, etc.) of the PMD device. When a low level is input to SD, the μPD98405 assumes LOS detection. Connect a pull-up resistor when the SD pin is not used.

2.3.5 JTAG Boundary Scan Signals

Remark This function is supported only when requested by the user.

These signals conform to the IEEE 1149.1 JTAG Boundary-Scan Standard.

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
JDI	285	E8	I	TTL	Boundary Scan Data Input Connect JDI to ground when unused.
JDO	284	F8	O 3-state	TTL	Boundary Scan Data Output Leave JDO open when unused.
JMS	283	D8	I	TTL	Boundary Scan Mode Select Connect JMS to ground when unused.
JCK	282	B8	I	TTL	Boundary Scan Clock Input Connect JCK to ground when unused.
JRST_B	281	A8	I	TTL	Boundary Scan Reset Connect JRST_B to ground when unused. ★ For JTAG reset, see **8.6 TAP CONTROLLER INITIALIZATION**.

2.3.6 Other Signals

Symbol	Pin No.		I/O	I/O level	Function
	QFP	FBGA			
SCLK	198	K21	I	TTL	SAR System Clock SCLK is used to supply the clock for LSI internal operation. ★ Ver. 3.1 or before: 25 MHz MAX. Ver. 4.0 or later: 33 MHz MAX.
PCI_MODE	118	V12	I	TTL	PCI/Generic Bus Mode PCI_MODE is used to select PCI/Generic bus mode. 0: Generic bus mode 1: PCI bus mode
TEST	271	F10	I	TTL	Internal test pin Leave open. Inputting a high-level signal sets test mode. This pin is connected to an internal pull-down resistor. This test mode is for internal testing and, as such, is not available to users.

2.3.7 Power and Ground

Symbol	Pin No.		I/O	Function
	QFP	FBGA		
V_{DD5}	8, 20, 32, 44, 56, 67, 81, 93, 105, 287, 299	E2, H5, K1, N5, R6, U5, AA4, W7, U9, B7, F6	-	+5 V Power Supply (digital section) These V_{DD5} pins supply +5 V when bus interface 5 V mode is selected. In 3.3 V mode, supply +3.3 V.
V_{DD3}	2, 14, 26, 38, 50, 62, 72, 78, 87, 99, 111, 125, 138, 151, 154, 175, 190, 208, 227, 245, 254, 293	C2, F2, J2, L4, P1, U1, W2, AA3, W6, AA8, V11, V14, AB17, AA20, Y21, R21, M19, H17, C21, D16, B14, E7	-	+3.3 V Power Supply (digital section) These V_{DD3} pins supply +3.3 V to the chip.
AV_{DD3}	269	B11	-	+3.3 V Power Supply (analog section) Supply power with high quality by inserting a filter between AV_{DD3} and AGND.
HV_{DD3}	275, 276	D10, F9	-	+3.3 V Power Supply (high-speed section) Supply power with high quality by inserting a filter between HV_{DD3} and HGND.
RV_{DD3}	280	D9	-	+3.3 V Power Supply (receive PLL section) Supply power with high quality by inserting a filter between RV_{DD3} and RGND.
GND	1, 7, 13, 19, 25, 31, 37, 43, 49, 55, 61, 68, 76, 77, 86, 92, 98, 104, 110, 117, 124, 131, 137, 145, 152, 153, 160, 167, 174, 182, 189, 199, 214, 228, 229, 243, 252, 259, 292, 298, 304	B2, E4, E1, G1, J4, K2, L1, N6, P5, R4, T6, W1, AA2, AB2, V6, U7, W8, V9, U10, AA12, U14, W15, U16, AA18, AB21, AA21, V21, U22, R19, N19, M22, K19, F22, B21, A21, A17, A15, B13, A5, D5, A2	-	Ground (digital section)
AGND	270	E11	-	Ground (analog section)
HGND	272, 279	E10, B9	-	Ground (high-speed section)
RGND	286	A7	-	Ground (receive PLL section)

2.3.8 Pin States during and after a Reset

(1/2)

Symbol	During Reset	After Reset
RENBL_B	1	0
RCLK	CLK output	CLK output
Tx7-Tx0	0	0
TSOC	0	0
TENBL_B	1	1
TCLK	CLK output	CLK output
PHR/W_B (External PHY)/PHYALM (Internal PHY)	0	0
PHOE_B	1	1
PHCE_B (External PHY)/SD (Internal PHY)	Hi-Z (input)	Hi-Z (input)
AD31-AD0	Hi-Z (input)	Hi-Z (input)
PCB3_B-PCBE0_B (PCI)/BE3_B-BE0_B (Generic)	Hi-Z (input)	Hi-Z (input)
PAR	Hi-Z (input)	Hi-Z (input)
FRAME_B	Hi-Z (input)	Hi-Z (input)
TRDY_B	Hi-Z (input)	Hi-Z (input)
IRDY_B	Hi-Z (input)	Hi-Z (input)
STOP_B	Hi-Z (input)	Hi-Z (input)
DEVSEL_B	Hi-Z (input)	Hi-Z (input)
REQ_B (PCI)/ATTN_B (Generic)	1	1
PERR_B	Hi-Z (input)	Hi-Z (input)
SERR_B	Hi-Z	Hi-Z
INTR_B	Hi-Z	Hi-Z
AD63-AD61 (PCI)/PAR2-PAR0 (Generic)	Hi-Z (input)	Hi-Z (input)
AD60-AD56 (PCI)/(Generic)	Hi-Z (input)/Hi-Z (output)	Hi-Z (input)/Hi-Z (output)
AD55-AD32 (PCI)/(Generic)	Hi-Z (input)/0	Hi-Z (input)/0
PCBE7_B-PCBE5_B (PCI)/SIZE2-SIZE0 (Generic)	Hi-Z (input)/0	Hi-Z (input)/0
PCBE4_B (PCI)/PAR3 (Generic)	Hi-Z (input)	Hi-Z (input)
PAR64	Hi-Z (input)	Hi-Z (input)
REQ64_B (PCI)/DR/W_B (Generic)	Hi-Z/1	Hi-Z/1
E2PCS	0	0
E2PDO	0	0
E2PCLK	0	0
ROMA15-ROMA0	0	0
ROMCS_B	1	1
ROMOE_B	1	1
CD31-CD0	0	0
CPAR3-CPAR0	0	0
CA18-CA0	0	0
CWE_B	1	1

(2/2)

Symbol	During Reset	After Reset
COE_B	1	1
TDOT	Undefined	Undefined
TDOC	Undefined	Undefined
JDO[Note]	Hi-Z	Hi-Z

Note During JRST_B input

Remark Internal PHY mode (PHM of GMR = 0) is set after a reset.

[MEMO]

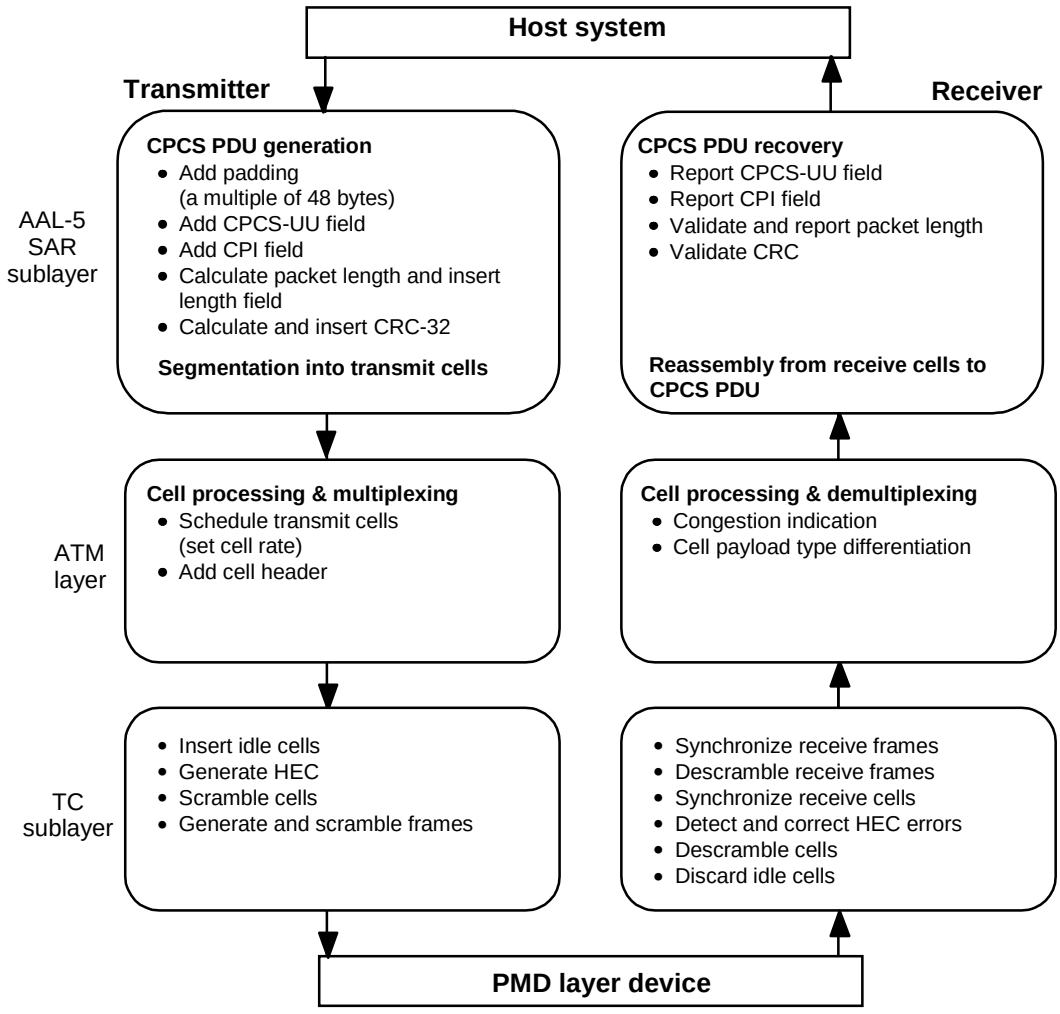
CHAPTER 3 FUNCTIONAL DESCRIPTION

This chapter outlines the functions of the μPD98405. For details of each function, see **Chapters 5 and 6**.

3.1 OVERVIEW

The μPD98405 supports the AAL-5 SAR sublayer, ATM layer, and TC sublayer of the ATM adaptation layer of the ATM protocol in hardware.

Figure 3-1. Functions of μPD98405



The μPD98405 provides an interface between a host system and a PMD layer device. It is controlled by the host system whenever the host system accesses the internal registers of the μPD98405 via the bus interface. Data is directly transmitted or received by the internal DMA controller of the μPD98405, to or from system memory under the management of the host system. An indication is written to system memory for each packet by means of a DMA status that indicates the end of transmission or reception. The host system must, therefore, allocate the following three areas in system memory to enable data to be transmitted or received using the μPD98405.

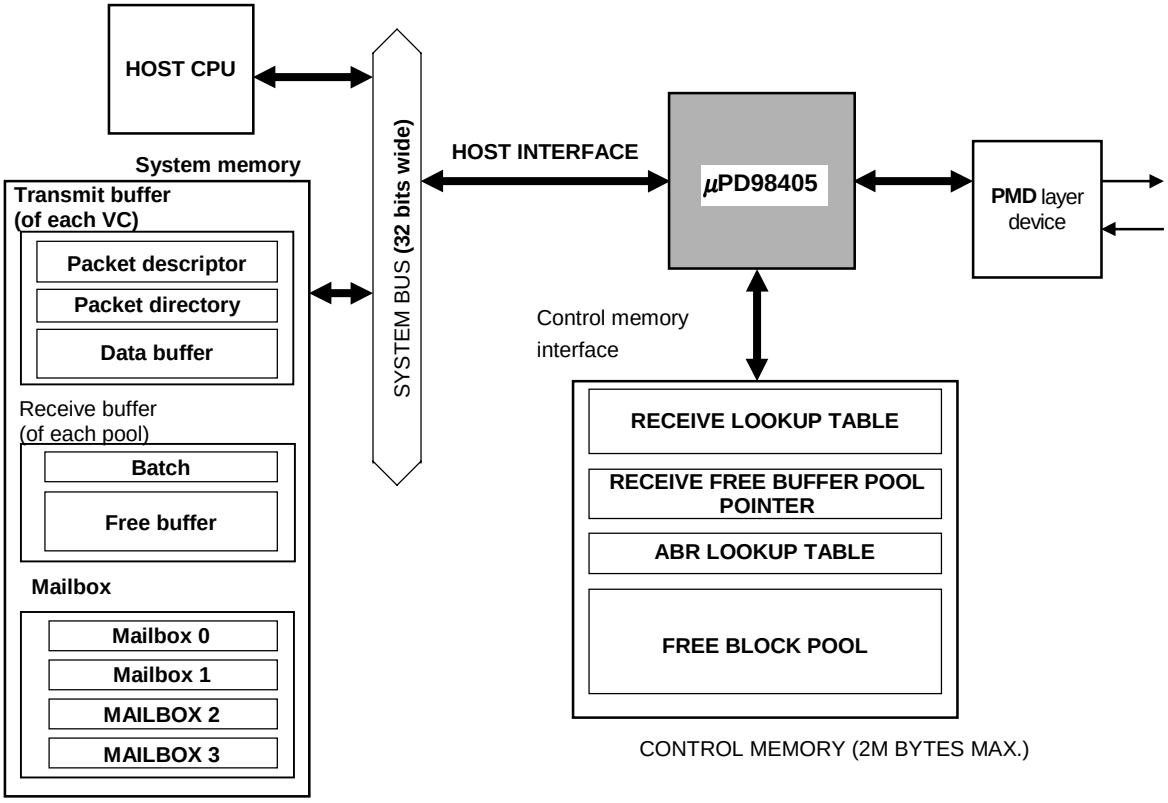
(a) Transmit buffer area: Saves transmit data.
(b) Receive buffer area: Saves receive data.
(c) Mailbox area: Saves transmit/receive indication.

The μPD98405 uses dedicated external memory as its control memory to execute reception processing. The control memory may have a capacity of up to 2M bytes. It is divided into the four areas described below. The size of the control memory is determined mainly by the number of channels through which the μPD98405 simultaneously transmits or receives data. The boundaries between the four areas are set, by the host system, into a register of the μPD98405.

<1> Receive lookup table area
<2> Receive free buffer pool pointer area
<3> ABR lookup table area
<4> Free block pool area

For details of the control memory, see **Section 5.2**.
Figure 3-2 shows an outline of the μPD98405 system.

Figure 3-2. Outline of μPD98405 System

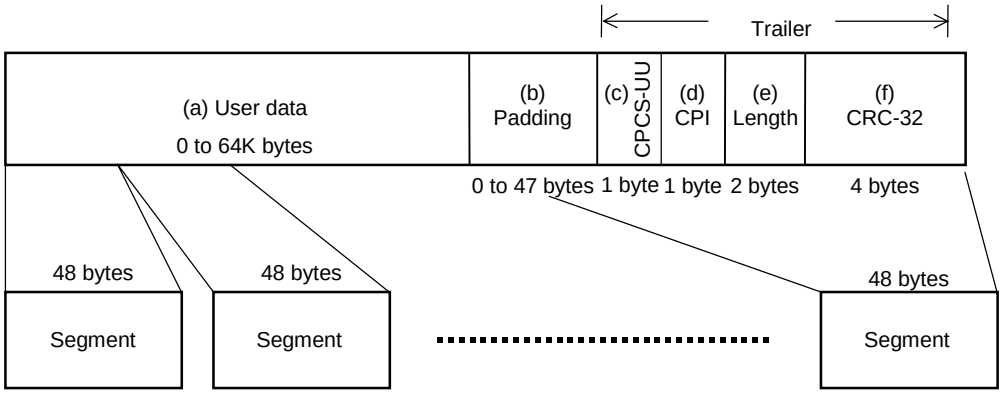


3.2 AAL-5 SAR SUBLAYER FUNCTION

The transmission function of the μPD98405 pads user data of different lengths (0 to 65,535 bytes) prepared by the host system, to the nearest multiple of 48 bytes, adds the trailer shown in Figure 3-3 to the data to create CPCS PDU, then disassembles the CPCS PDU of AAL-5 into 48-byte segments.

The reception function assembles a CPCS PDU from the received cells and stores it into the receive buffer. The μPD98405 checks the trailer of the packet, checks for errors, and reports those errors, if any, to the host. The receive data is stored in CPCS PDU format consisting not only of (a) user data field but also fields (b) through (f).

Figure 3-3. PDU Format of AAL-5



(a) User data field:

Data of up to 65,535 bytes.

(b) Padding field:

A field of 0 to 47 bytes, inserted between the user data and trailer, to increase the length of the CPCS PDU to the nearest multiple of 48 bytes. The μPD98405 automatically inserts all-zero data into this field.

(c) CPCS user-user information (CPCS-UU) field:

Used to transfer CPCS user-user information. The μPD98405 can set and transfer any data.

(d) Common part identification (CPI) field:

This field, containing all-zero data, is used to set the length of the CPCS PDU trailer to 8 bits. No other usage or set value is defined for this field. This field of a packet that is transmitted by the μPD98405 can be set in any way by the user.

(e) Packet length (Length) field:

Indicates the user data length (0 to 65,535) of the CPCS PDU, in binary. This field is calculated and inserted by the transmitter. The receiver is provided with a function to verify this field against the size of the packet actually received.

(f) CRC-32 field:

This field sets a CRC code, right-justified.

The creation polynomial is as follows:

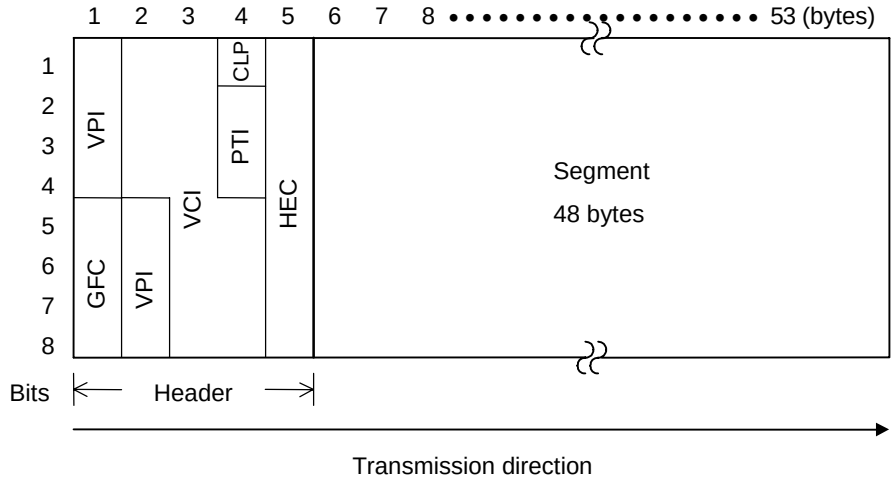
Expression = $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

3.3 ATM LAYER FUNCTION

3.3.1 Creating Cells

The μPD98405 creates cells by adding 5-byte header information to a segment as shown in Figure 3-4.

Figure 3-4. User Network Interface (UNI) of Cell Structure



Remark GFC: Generic Flow Control
VPI: Virtual Path Identifier
VCI: Virtual Channel Identifier
PTI: Payload Type Identifier
CLP: Cell Loss Priority
HEC: Header Error Control

The function of each field of the header and the functions supported by the μPD98405 are described below.

(1) GFC (generic flow control) field

The GFC field contains control information that is used to avoid cell collision.

<Processing performed by μPD98405>

Transmission: Inserts the user-specified pattern for each packet into this field.

Reception: Ignores this field and does not report its contents to the host (except for raw cell reception).

(2) VPI/VCI (virtual path identifier/virtual channel identifier) fields

VPI and VCI are routing bits used for identification when the virtual path (VP) level and virtual channel (VC) level are multiplexed.

<Processing performed by μPD98405>

Transmission: Inserts all the 24 bits of the user-specified VPI/VCI.

Reception: Supports up to 16 bits of the VPI/VCI. These bits consist of the low-order bits of the VPI and the low-order bits of the VCI. For details of the algorithm that reduces the number of bits from 24 to 16, see **Section 5.5.4**.

The μPD98405 divides the setting of one channel into a transmission VC and reception VC.

The μPD98405 can support up to 32K active VCs (virtual channels) (any combination of reception VC and transmission VC is supported). The VC (virtual channel) identifies the transmission and reception channels of the μPD98405, and differs in meaning from the VCI field.

(3) PTI (payload type identifier) field

This is a 3-bit field that indicates whether the payload type of a cell consists of user data or layer management information. It contains explicit forward congestion information (EFCI) and indicates that a cell has passed a congested network node.

The PTI field codes are assigned as follows:

PTI	Usage
000	User data cell, congestion not experienced, SDU type = 0
001	User data cell, congestion not experienced, SDU type = 1
010	User data cell, congestion experienced, SDU type = 0
011	User data cell, congestion experienced, SDU type = 1
100	OAM F5 cell (segment supported)
101	OAM F5 cell (end-end supported)
110	Resource management cell
111	Reserved for future function

SDU type = 0: All segments of an AAL-PDU except the last cell

SDU type = 1: The last cell of an AAL-PDU. This segment contains the trailer.

OAM F5 cell: Specific OAM cell containing virtual channel connection (VCC) operation information

<Processing performed by μPD98405>

Transmission: The μPD98405 sets the user-specified pattern in this field as is and transfers it. When the AAL-5 type processing is selected (the AAL bit of the packet descriptor is 1), the μPD98405 transmits the last segment after changing the least significant bit of this field to "1."

Reception: Monitors the PTI field of the reception cell to determine whether the cell is an OAM cell, resource management (RM) cell, or user data cell, and to subsequently perform processing accordingly. If a user data cell has been received, the μPD98405 checks the least significant bit, which indicates the last segment, to determine whether the reception of a packet has been completed.

(4) CLP (cell loss priority)

This field is used to indicate that the cell can be lost in the event of network congestion. When CLP = 1, the cell is lost.

<Processing performed by μPD98405>

Transmission: The user can select and set the following three modes for each transmission packet. The mode is set in the transmit packet descriptor.

- CLP = 0 for all cells
- CLP = 1 for all cells
- CLP = 1 for all cells except the last cell of a packet, and CLP = 0 for the last packet

Reception: Monitors each reception packet. When a cell for which CLP = 1 is set is received, it is reported to the host by the reception indication for that packet.

(5) HEC (header error control) field

This field is processed by the TC sublayer of the physical layer. It is used to synchronize cells and to detect and correct header errors.

<Processing performed by μPD98405>

Transmission: The ATM layer of the μPD98405 inserts dummy data "00H" into this field for transmission. (The TC sublayer generates and inserts the HEC field.)

Reception: This field is ignored.

3.3.2 Setting the Cell Transmission Rate

(1) VBR, CBR, and UBR cell scheduling

The μPD98405 has 16 VBR shapers that control the transmission rate of a created cell. The operation of each shaper is based on the dual leaky packet algorithm. The algorithm parameters are set for each shaper by the user. The user can set the use of a shaper for each channel.

Each of the 16 shapers have a priority. The shaper with highest priority can be used for CBR. The shaper with lowest priority can be used for UBR.

Of the 16 shapers, one or more can be set as unassigned cell generators. Those shapers set as unassigned cell generators function as shapers that transmit only unassigned cells at a rate specified by the user. By using this unassigned cell generator function, all the channels can limit the bandwidth at which the data will be transmitted.

(2) ABR cell scheduling

The μPD98405 features an ABR scheduler that controls the ABR service transmission rate. It automatically changes the transmission rate according to information of each received BRM cell.

3.3.3 Supporting Non-AAL-5 Traffic

The μPD98405 has a function for processing packets as raw cells to support traffic other than AAL-5, or for transmitting or receiving OAM cells. A VC set as a raw cell does not execute AAL-5 processing, such as adding a trailer, when it is transmitted. Instead, it merely creates cells from the data and transmits those cells. When such a VC is received, the 53-byte reception cell with a header is stored into system memory, together with 11-byte indication information (For an explanation of the format, see **Section 5.5.8**).

The header processing performed for each cell and payload processing are executed, using software, by the host.

The μPD98405 also supports a function for inserting or verifying CRC-10 for non-AAL-5 traffic to mitigate the processing by the host. When the user enables the insertion of CRC-10 by the transmission VC, the μPD98405 calculates CRC-10 for each cell, and inserts the result of the calculation into the last 10 bits of the payload of the cell. If verification is always performed and an error is detected as a result, an error occurrence flag is set as the indication of the raw cell data and this is reported to the host.

3.4 TC SUBLAYER FUNCTION

The transmission function of the μPD98405 TC sublayer inserts ATM cells, received from the ATM layer, into a SONET STS-3c/SDH STM-1 frame and outputs the frame to the PMD interface. The reception function extracts ATM cells from a SONET STS-3c/SDH STM-1 frame received from the PMD interface and passes the cells to the ATM layer.

Figure 3-5. Outline of Frame Transmission Function

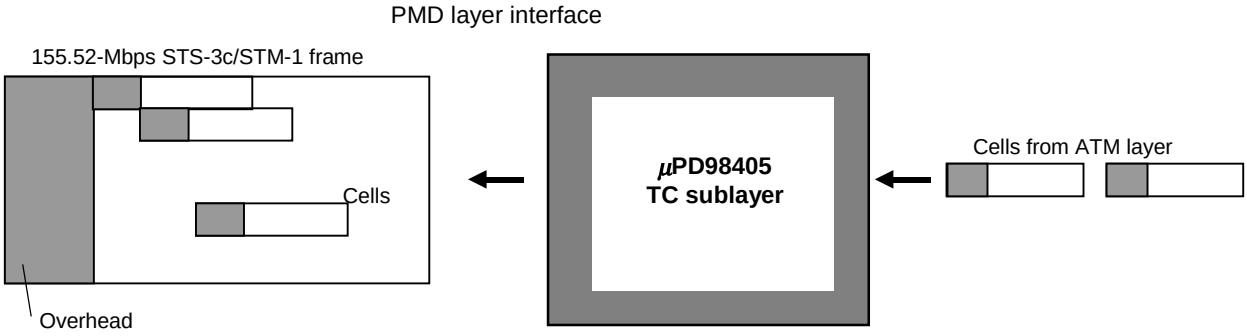
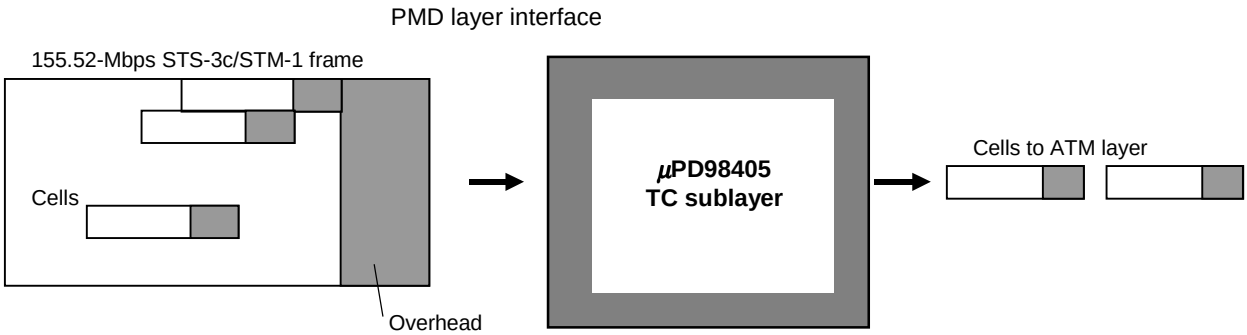


Figure 3-6. Outline of Frame Reception Function



The transmitter of the μPD98405 generates the HEC. The receiver of the μPD98405 detects and corrects HEC errors.

Generating HEC

The μPD98405 calculates a CRC for the 4 high-order bytes of the 5-byte header of each ATM cell, using the following polynomial. Then, it inserts the value obtained by adding "55H" to the result of the calculation into byte 5 of the ATM header as a header error check (HEC).

Polynomial: $G(X) = X^8 + X^2 + X + 1$

[MEMO]

CHAPTER 4 INTERFACES

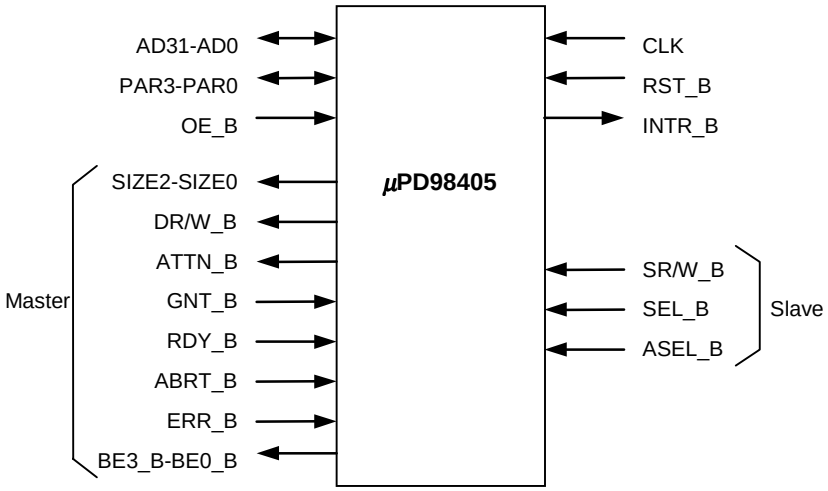
The μPD98405 has a host bus interface, PHY device interface, control memory interface, and PMD interface. The host bus interface supports either of two modes: Generic mode and PCI mode. These modes are selected using the PCI_MODE pin. When the level of the PCI_MODE signal is high, the host bus interface is placed in PCI bus interface mode; when the level is low, the interface is placed in Generic bus interface mode. The Generic bus interface can be connected to a general I/O bus with a minimum of external circuitry. The PCI bus interface can be connected directly to a PCI bus.

This chapter explains the functions and operations of each interface.

4.1 GENERIC BUS INTERFACE

The Generic bus interface of the μPD98405 is a 32-bit address/data multiplexed bus that uses different control signals for master (DMA) operation and slave operation. This bus interface is a Generic type that can be connected to a general I/O bus (such as S bus, GIO, and AP bus) with a minimum of external circuitry.

Figure 4-1. Bus Interface Signals



4.1.1 Bus Operation Control Pins

(1) OE_B pin

OE_B is an output enable signal input pin for AD31 through AD0 and PAR3 through PAR0 of the μPD98405. While a low level is input to the OE_B pin, the μPD98405 executes output from AD31 through AD0 and PAR3 through PAR0. When a high level is input as this signal, the μPD98405 sets AD31 through AD0 and PAR3 through PAR0 to high impedance. This operation is performed independently of the internal state of the μPD98405. For example, if a high level is input to the OE_B pin while the μPD98405 is operating as the master and performing DMA write, the μPD98405 immediately performs output to the high-impedance bus. Internally, however, the μPD98405 continues the DMA cycle. Consequently, data being transferred is lost.

This signal is used to forcibly abort the bus operation of the μPD98405 from an external source. Fix the OE_B signal to low level if there is no special case where output to the bus must be forcibly set to high impedance.

(2) ERR_B pin

The ERR_B pin enables the device controlling the system bus to input a signal to stop bus operation by the μPD98405 if an error is detected on the bus. If a low level is input to this pin during DMA transfer, the μPD98405 first stops DMA transfer then immediately deactivates the ATTN_B signal. In addition, the μPD98405 sets the SBE (system bus error) bit of the GSR register to 1, then issues an interrupt to the host provided the interrupt is not masked. A system bus error prevents the μPD98405 from continuing DMA transfer (master operation), thus disabling transmission/reception. Because the slaves can still be accessed, however, a software or hardware reset must be executed to recover from the error.

4.1.2 Parity Check Function

The μPD98405 has parity signal I/O pins PAR3 through PAR0 on the bus interface and, therefore, is capable of outputting/checking a parity signal.

The user can enable or disable the parity function, select byte or word parity, and odd or even parity by setting the GMR register accordingly.

Table 4-1. Bus Parity Mode Select Bits

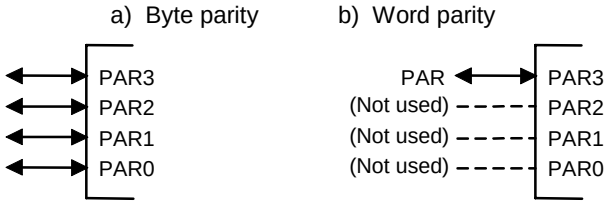
Enables or disables bus parity.		
BPE bit (GMR: bit 3)	0	Disable. μPD98405 does not check the bus parity.
	1	Enable. μPD98405 checks bus parity bit input and, if an error is detected, sets the SPE bit of the GSR register and generates an interrupt (if the interrupt is not masked).
	Default = 0	
Selects even or odd parity mode.		
PC bit (GMR: bit 4)	0	Even parity mode
	1	Odd parity mode
	Default = 0	
Selects byte or word parity mode.		
PM bit (GMR: bit 5)	0	Byte parity mode. Uses all bus parity pins PAR3 through PAR0.
	1	Word parity mode. Only the PAR3 pin is used as the bus parity pin.
	Default = 0	

The parity bit is input or output using parity pins PAR3 through PAR0. The pins to be used differ depending on whether byte parity mode or word parity mode is set.

In byte parity mode, all of pins PAR3 through PAR0 are used. PAR3 is used to input/output the parity bit of AD31-AD24/BE3_B, while PAR0 is used to input/output the parity bit of AD7-AD0/BE0_B. In word parity mode, the PAR3 pin inputs/outputs the parity bit of AD31-AD0/BE3_B-BE0_B.

These pins serve as output pins and output parity bits when the μPD98405 outputs addresses or writes data. These pins are used as input pins when the μPD98405 reads data, when they receive a parity bit from an external source to be checked internally. When the μPD98405 does not access the bus, PAR3 through PAR0 enter the high-impedance state.

Figure 4-2. Differences in Uses of Pins between Byte and Word Parity Modes



The μPD98405 generates the output parity and checks input parity regardless of whether it is operating as the master (DMA) or as a slave. When the bus inputs data from the host to the μPD98405, the μPD98405 checks the parity bit that is input together with an address and data. When the BPE bit of the GMR register is set to 1, enabling the use of the check function, the SPE bit of the GSR register is set to 1 and an interrupt is generated (provided the interrupt is not masked) when the μPD98405 detects a parity error.

The parity check for BE3_B to BE0_B is performed only during master operation and not during slave operation. Even during master operation, the parity check for BE3_B to BE0_B is not performed in the address phase.

Caution When a parity error is detected, the μPD98405 stops the master (DMA) operation, and no longer performs master operation. However, the μPD98405 allows a slave access. The operation of the μPD98405 is not guaranteed when and after a parity error has been detected, however. Whenever a parity error is detected, therefore, reset the μPD98405.

The PAR3 through PAR0 pins always function as 3-state I/O pins, regardless of whether the BPE bit of the GMR register is set (whether the bus parity is enabled or disabled). Therefore, perform pull-up processing when these pins are not used.

Caution Even if the parity check function is disabled (BPE bit = 0), the parity bit output function remains enabled, such that the μPD98405 always outputs parity bits from pins PAR3 through PAR0, when outputting an address or data to the bus. After power-on, therefore, until the host has set the parity mode in the GMR register, the host should not read a μPD98405 register and the μPD98405 should not perform DMA transfer. Otherwise, the host will detect a parity error.

4.1.3 Master Operation

The μPD98405 uses the internal 32-bit DMA controller to read the transmit data and descriptor in external system memory, or to write the indication of the transmission/reception completion status and receive data into external system memory, when it is operating as the bus master.

(1) Master (DMA) operation

The following I/O pins are used to control the master operation of the μPD98405.

Symbol	I/O	Function
ATTN_B	O	This is a DMA request signal, output to the host by the μPD98405. It is set to active status to inform the external bus arbiter that the μPD98405 has an internal source for DMA transfer. This signal is set to inactive status in synchronization with the rising edge of the clock when only one word of data remains to be transferred.
GNT_B	I	This signal is input when the bus arbiter grants the μPD98405 the right to use the bus in response to a DMA request received from the μPD98405.
DR/W_B	O	Indicates the direction in which DMA access is performed.
SIZE	O	Indicates the amount of data currently subject to DMA transfer.
RDY_B	I	Wait cycle control signal
ABRT_B	I	This signal is input if the host must cancel the DMA cycle currently being executed by the μPD98405.
BE3_B-BE0_B	O	Byte enable signals for the 32-bit data line during DMA cycles executed by the μPD98405.

Figure 4-3. 1-Word Write DMA Cycle Timing

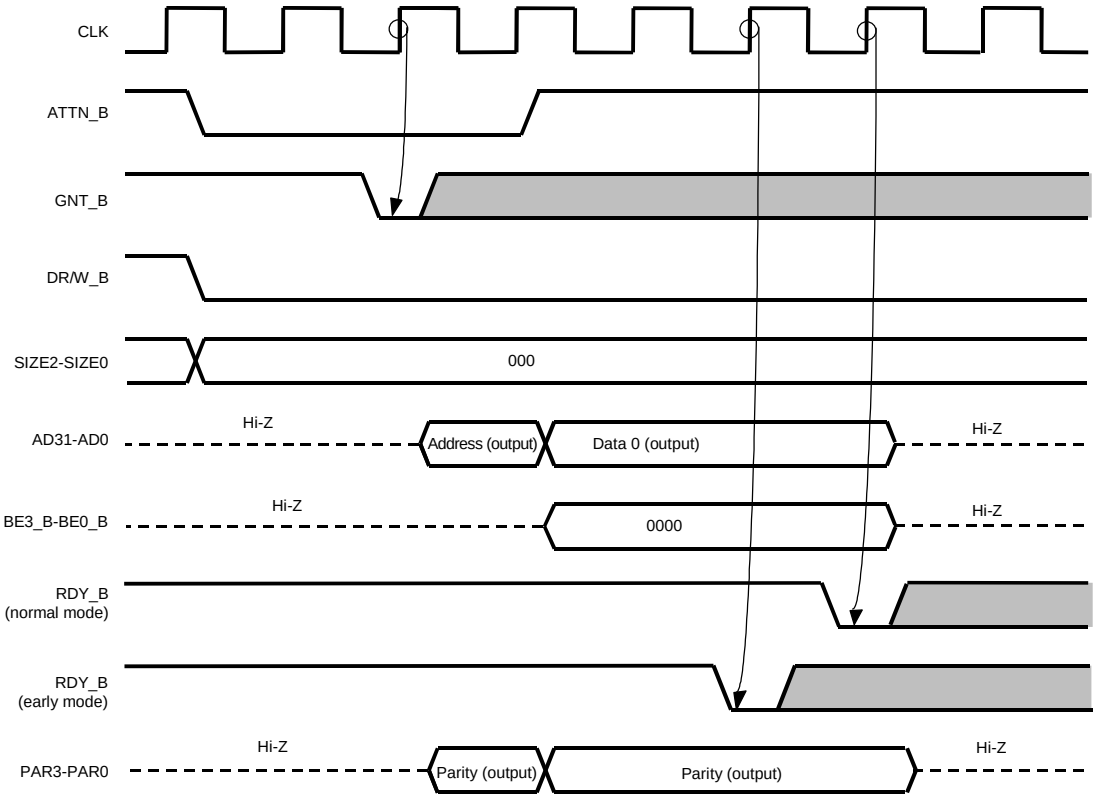
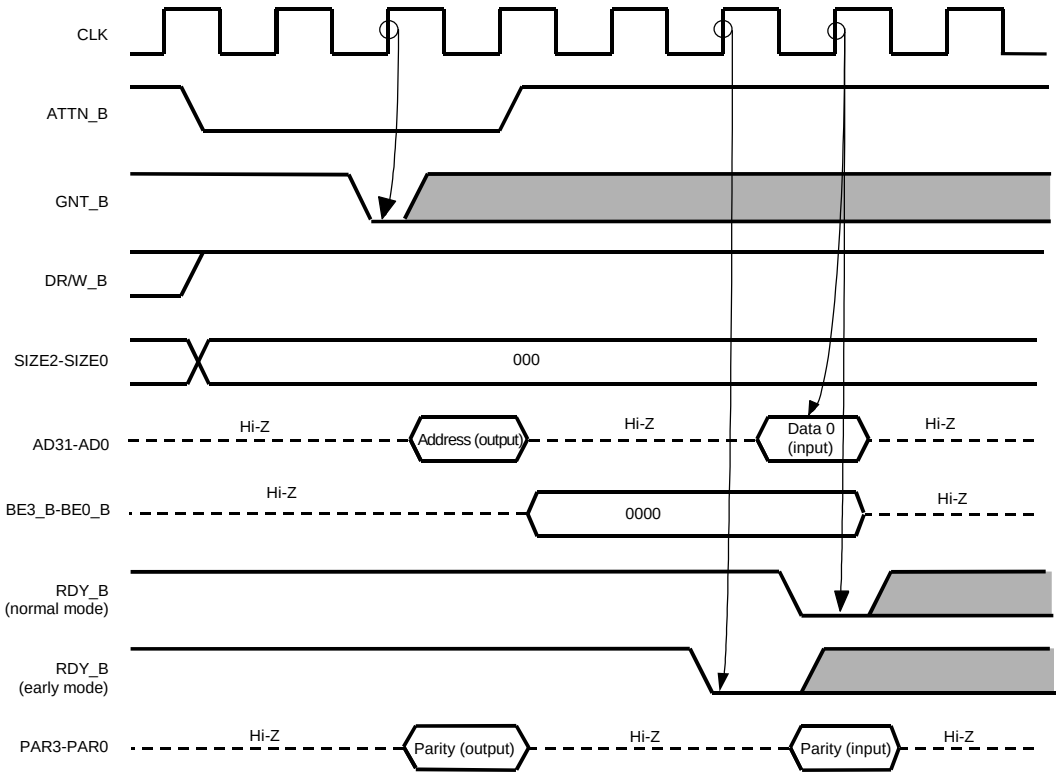


Figure 4-4. 1-Word Read DMA Cycle Timing



The μPD98405 requests the external bus arbiter for the bus by driving the ATTN_B signal low. At the same time, it indicates the direction of transfer by using DR/W_Bs and specifies the burst size with SIZE2 through SIZE0. The bus arbiter acknowledges the request by the ATTN_B signal by driving the GNT_B signal low, and grants bus mastership to the μPD98405. After driving the ATTN_B signal low, the μPD98405 samples the GNT_B signal at the rising edge of the clock. When the μPD98405 detects that GNT_B has been driven low, it outputs an address at the rising edge of the clock, and starts sampling the RDY_B signal. The μPD98405 requires one clock cycle to output an address for both read and write. After outputting the address, the μPD98405 starts sampling the RDY_B signal at the rising edge of the clock.

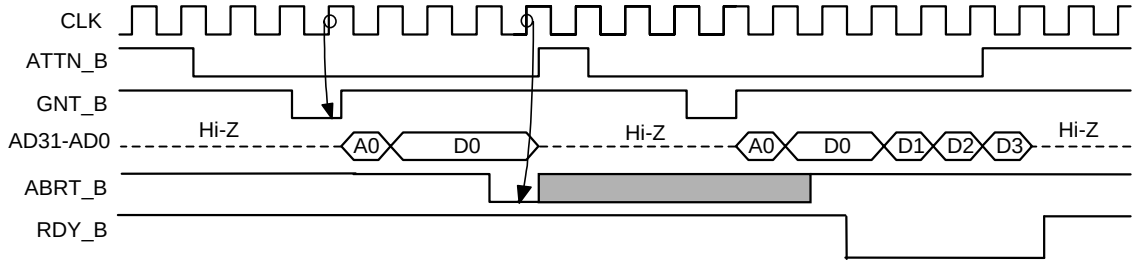
During a DMA read operation, the μPD98405 latches the data on AD31 through AD0 at the rising edge of the clock whenever a low level is input to the RDY_B pin. Upon a DMA write operation being performed, the μPD98405 outputs data to AD31 through AD0 immediately after completion of the address cycle. At the same time, the μPD98405 outputs byte enable signals to BE3_B through BE0_B. The data is retained until the level of the RDY_B signal goes low. The user can insert wait cycles by controlling the input of this RDY_B signal. The μPD98405 deactivates the ATTN_B signal at the first rising edge of the clock once all data except one word has been transferred. The GNT_B signal may always be set to low.

The ABRT_B signal is used to abort the data transfer cycle. The μPD98405 samples the ABRT_B signal, as well as the RDY_B signal in the data transfer cycle after outputting the address. If a low level is input to the ABRT_B pin in the data transfer cycle, the μPD98405 aborts DMA transfer in that cycle and makes the ATTN_B signal inactive. Subsequently, it makes the ATTN_B signal active again, then retries transfer of the aborted data. If a low level is input to the ABRT_B and RDY_B pins at the same time, the μPD98405 gives priority to the ABRT_B signal.

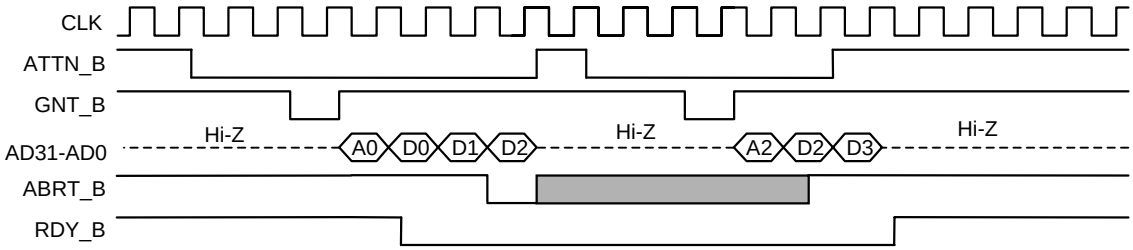
Figure 4-5 shows an example of the timing of the ABRT_B input signal.

Figure 4-5. ABRT_B Signal Input Timing

(a) To abort at the 1st word of a 4-word burst



(b) To abort at the 3rd word of a 4-word burst



The user can select "normal mode" or "early mode" as the mode in which the μPD98405 samples the RDY_B and ABRT_B signals. These modes can be selected independently regardless of whether a DMA read or DMA write operation is being executed. To set these modes, use the RA and WA bits of the GMR register.

In early mode, the μPD98405 detects RDY_B and ABRT_B at the rising edge of the system bus clock, one clock earlier than in normal mode.

Input timing of RDY_B/ABRT_B during read operation		
RA bit (GMR: bit 12)	0	Normal mode
	1	Early mode. Input one clock earlier.
	Default = 0, normal mode	
Input timing of RDY_B/ABRT_B during write operation		
WA bit (GMR: bit 13)	0	Normal mode
	1	Early mode. Input one clock earlier.
	Default = 0, normal mode	

Remark For an illustration of the differences between normal mode and early mode, see **Figure 4-3.**

(2) Burst transfer

The μPD98405 supports burst transfer of 1, 2, 4, 8, 12, or 16 words. The user can select the burst size to be enabled by setting the "SZ field" or "TBE field" of the GMR register.

Table 4-2. Selecting Burst Size to Be Enabled

Selects the burst size to be used (GMR register: Bits 11 through 8: SZ field, Bit 16: TBE field).		
SZ field	Bit 11	1: Enables 16-word burst, 0: Disabled
	Bit 10	1: Enables 8-word burst, 0: Disabled
	Bit 9	1: Enables 4-word burst, 0: Disabled
	Bit 8	1: Enables 2-word burst, 0: Disabled
TBE bit	Bit 16	1: Enables 12-word burst, 0: Disabled (The AD bit must always be set to 1.)
Default = All 0 (supports 1-word transfer only.)		

More than one burst size can be enabled at the same time. Regardless of the setting of the "SZ field" and "TBE field," 1-word transfer is always enabled. When the TBE bit is set to 1 to enable 12-word burst, the AD bit must always be set to 1 to disable the burst size select function. If 16-word transfer is enabled, the μPD98405 executes 16-word burst only when raw cells are written into system memory.

The master (DMA) operation performed by the μPD98405 is executed to transfer the following data listed in Table 4-3. For an explanation of the meaning of each operation, see **Chapter 5**. Some data types must always start on a word (32-bit) boundary. Other data types can start on a byte boundary.

Table 4-3. DMA Transfer by μPD98405

Read/write	Data type	Number of words	Can start on byte boundary?
Read	Packet descriptor	4 words	No
	Buffer descriptor	2 words	No
	Transmit cell data	1 to 12 words	Yes
	Receive batch (size, address)	2 words	No
	Receive batch link pointer	1 word	No
Write	Transmission indication	1 word	No
	Reception indication	4 words	No
	Receive cell data	1 to 12 words	Yes
	Receive batch link pointer	1 word	No
	Raw cell data	1 to 16 words	Yes

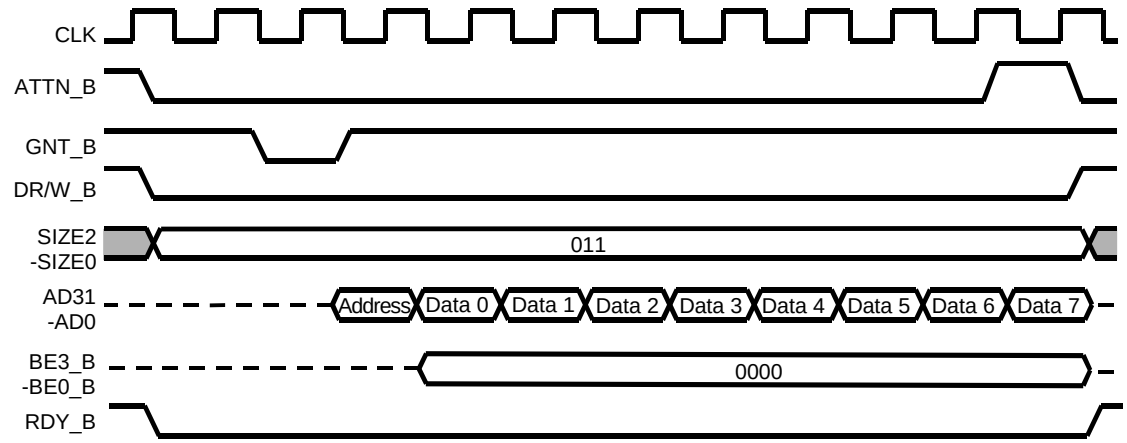
The burst size being used is coded as shown in Table 4-4 and output from the SIZE2 through SIZE0 pins.

Table 4-4. Burst Size Being Used

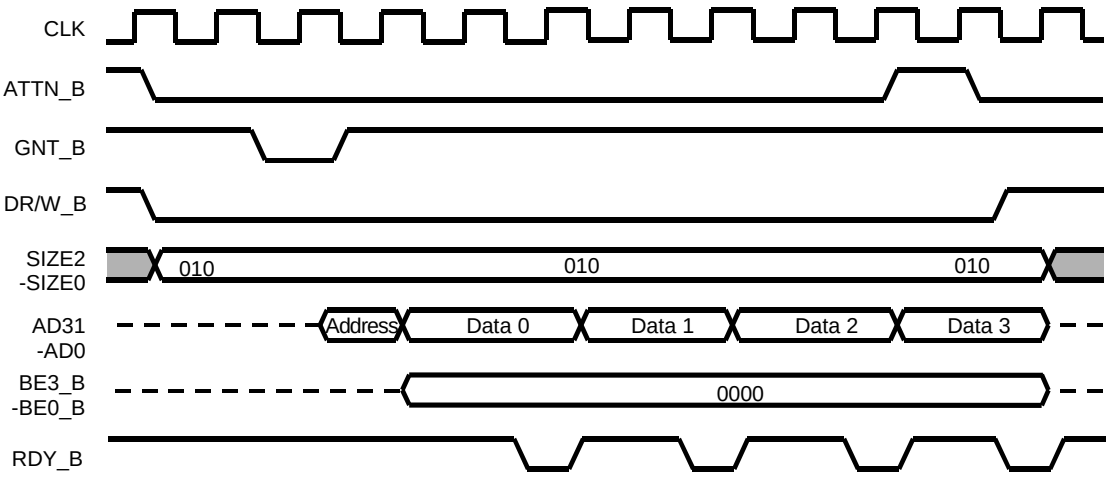
SIZE2 through SIZE0	Burst size being used
000	1-word transfer
001	2-word burst
010	4-word burst
011	8-word burst
100	16-word burst
101	12-word burst
110, 111	Undefined

Figure 4-6. Burst Write Cycle Timing

(a) Example of 8-word burst write cycle (no wait)



(b) Example of 4-word burst write cycle (with 1 wait cycle inserted)



(3) Burst size select function

If more than one burst size is enabled, the μPD98405 checks the address field at the transfer destination, and automatically selects the burst size to be used from the enabled burst sizes. This function is enabled for both DMA read and write cycles that are performed by the μPD98405. This function cannot be used when 12-word burst is enabled.

Transfer destination address	Executable burst size
xxxxxxxx xxxxxxxx xxxxxxxx xx0000xx	16-[Note], 8-, 4-, 2-, and 1-word burst
xxxxxxxx xxxxxxxx xxxxxxxx xxx000xx	8-, 4-, 2-, and 1-word burst
xxxxxxxx xxxxxxxx xxxxxxxx xxx100xx	4-, 2-, and 1-word burst
xxxxxxxx xxxxxxxx xxxxxxxx xxxx10xx	2- and 1-word burst
xxxxxxxx xxxxxxxx xxxxxxxx xxxxx1xx	1-word transfer

Note 16-word burst is assigned the highest priority only when transferring raw cell data.

Burst size	16	8	4	2	1
Priority	High → Low				

When performing DMA transfer, the μPD98405 counts the number of zeros in the transfer destination address field (AD2 to AD5), starting from the LSB. The size of the burst operation which can be executed is determined from the number of zeros. Higher priorities are assigned in the order of 8-, 4-, 2-, and 1-word bursts. The μPD98405 selects that burst size which has been assigned the highest priority, from among those executable and enabled, then executes burst transfer.

This function is enabled or disabled by using the "AD bit" of the GMR register.

Selects burst transfer mode.		
AD bit (GMR: bit 7)	0	When the μPD98405 performs DMA transfer, the function to check the transfer destination address field, and to select a burst size from the enabled sizes according to the address, is enabled.
	1	When the μPD98405 performs DMA transfer, the function to check the transfer destination address field is disabled. The μPD98405 simply selects and uses the biggest burst size from among those enabled.
	Default = 0	

Caution When the TBE bit is set to 1 to enable 12-word burst, the AD bit must always be set to 1 to disable this function.

The following describes an example of the processing performed when this function is enabled (AD = 0) or disabled (AD = 1).

<Example>

While the μPD98405 is receiving data, it stores data into system memory by performing the master (DMA) operation each time it receives one cell. Because the payload part of an ATM cell consists of 48 bytes, the cell data transferred by the μPD98405 consists of 12 words. Assuming the start address of the receive buffer to be "00000000H," the operation required to store the receive cell data in each case is shown below.

Example	AD bit	Enabled burst size
Case **<1>**	0	4 words, 8 words
Case **<2>**	1	4 words, 8 words
Case **<3>**	0	8 words only
Case **<4>**	0	2 words only (In this example, the operation is the same as that when AD = 1 because start address is all 0.)
Case **<5>**	0	Disables all burst sizes. (In this example, the operation is the same as that when AD = 1 because start address is all 0.)

Table 4-5. Burst Transfer Transition

Cell	Word	Address	Burst size generated in each case				
			<1>	**<2>**	**<3>**	**<4>**	**<5>**
1st cell	1	00000000	8	8	8	2	1
	2	00000004					1
	3	00000008				2	1
	4	0000000C					1
	5	00000010				2	1
	6	00000014					1
	7	00000018				2	1
	8	0000001C					1
	9	00000020	4	4	1	2	1
	10	00000024			1		1
	11	00000028			1	2	1
	12	0000002C			1		1
2nd cell	1	00000030	4	8	1	2	1
	2	00000034			1		1
	3	00000038			1	2	1
	4	0000003C			1		1
	5	00000040	8		8	2	1
	6	00000044					1
	7	00000048				2	1
	8	0000004C					1
	9	00000050		4		2	1
	10	00000054					1
	11	00000058				2	1
	12	0000005C					1
3rd cell	1	00000060	8	8	8	2	1
	2	00000064					1
	3	00000068				2	1
	4	0000006C					1

(4) Byte alignment transfer

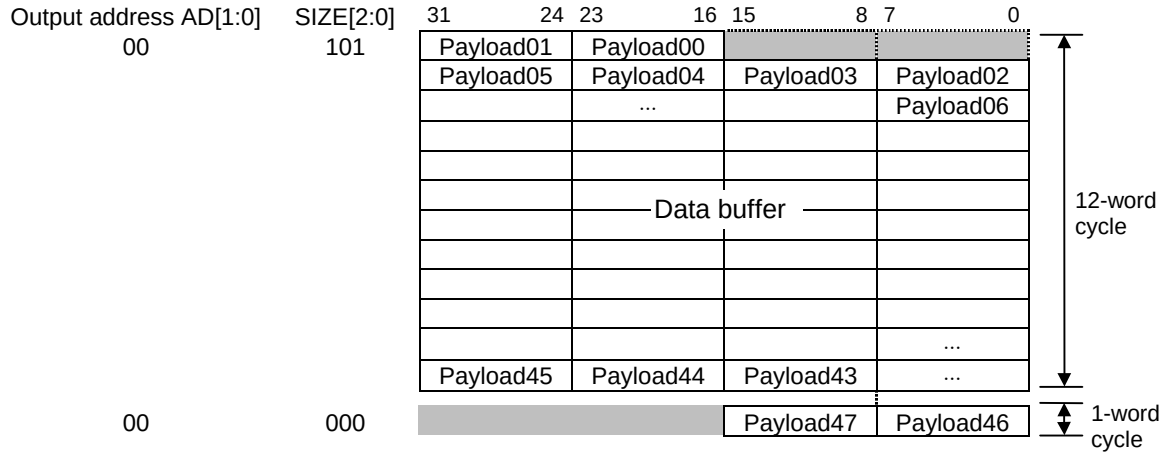
The μPD98405 can align transmit/receive cell data on byte boundaries in system memory. When the μPD98405 executes a DMA cycle, it checks the 2 low-order bits of the start address, AD1 and AD0. When these bits indicate other than 00, the μPD98405 executes byte alignment transfer.

(a) Byte alignment transfer for transmit cell data

The μPD98405 loads transmit cell data from the data buffer in system memory by performing DMA read cycles. The start address of the data buffer need not always be on a 32-bit boundary. When transmit cell data does not start on a 32-bit boundary, the μPD98405 performs DMA read cycles in 32-bit (word) units. Internally, it ignores any unnecessary bytes.

Figure 4-7 shows an example. In this example, the data buffer contains 12-word data that can configure 1 cell, the start address is on a byte boundary, and 12-word burst is enabled.

Figure 4-7. Transmit Cell Data Byte Alignment (in Little Endian Format)



First, the μPD98405 performs a DMA read cycle for 12-word burst. It internally discards the 2 high-order bytes of the first word. Then, the μPD98405 performs a 1-word DMA read cycle and discards the 2 low-order bytes. For these two DMA cycles, the address output by the μPD98405 indicates an address on a 32-bit boundary whose 2 low-order bits are 00.

(b) Byte alignment transfer for receive cell data

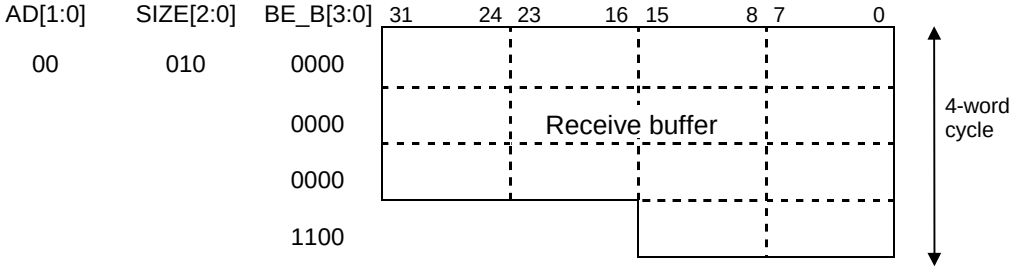
The μPD98405 stores receive cell data in the free buffer in system memory by performing DMA write cycles. The start address of the free buffer need not always start on a 32-bit boundary, and can start on a byte boundary. When the start address of the free buffer (set in the batch) is aligned with a byte boundary, the μPD98405 outputs "00," indicating a word boundary address, to the AD[1:0] pins and a low level from the BE_B[3:0] pins corresponding to the bytes to be written. It also outputs a burst size from the SIZE[2:0] pins.

When the 2 low-order bits of the buffer start address indicate 00 and the buffer size is not in word units (for example, 14 bytes), the μPD98405 determines the burst size in the same way as when the buffer starts on a word boundary and uses the BE_B[3:0] pins during transfer of the last word to control the byte enable status. This example is shown in Figure 4-8.

Figure 4-8. DMA Write Transfer to Receive Buffer in Byte Units

Receive buffer size: 14 words

Start address: 00H



4.1.4 Slave Operation

Slave operation is used when the host accesses the direct address register of the μPD98405, or when the host accesses the control memory, indirect address register, PHY register, or external PHY device via the direct address register. The following three pins are used to control slave operation.

- **SR/W_B** (slave read/write - input):
  Determines read or write direction for slave access.
- **SEL_B** (slave select - input):
  Selects slave operation of the μPD98405.
- **ASEL_B** (slave address select - input):
  Selects the direct address register of the μPD98405. When a low level is input to the ASEL_B pin, the μPD98405 samples the low-order 8 bits of AD31 through AD0 at the rising edge of the system bus clock and loads them as an address.

The host sets the SEL_B signal to active low to enable slave operation of the μPD98405.

At the same time, the host sets the ASEL_B signal to active low and outputs the address of the direct address register to be accessed to the AD bus.

The μPD98405 latches an address from AD31 through AD0 at the rising edge of the clock when a low level is input as the ASEL_B signal. The μPD98405 internally decodes only the low-order 8 bits of AD31 through AD0 as an address, and ignores the high-order 24 bits.

At this time, the μPD98405 checks the SR/W_B to determine whether the access direction is read or write.

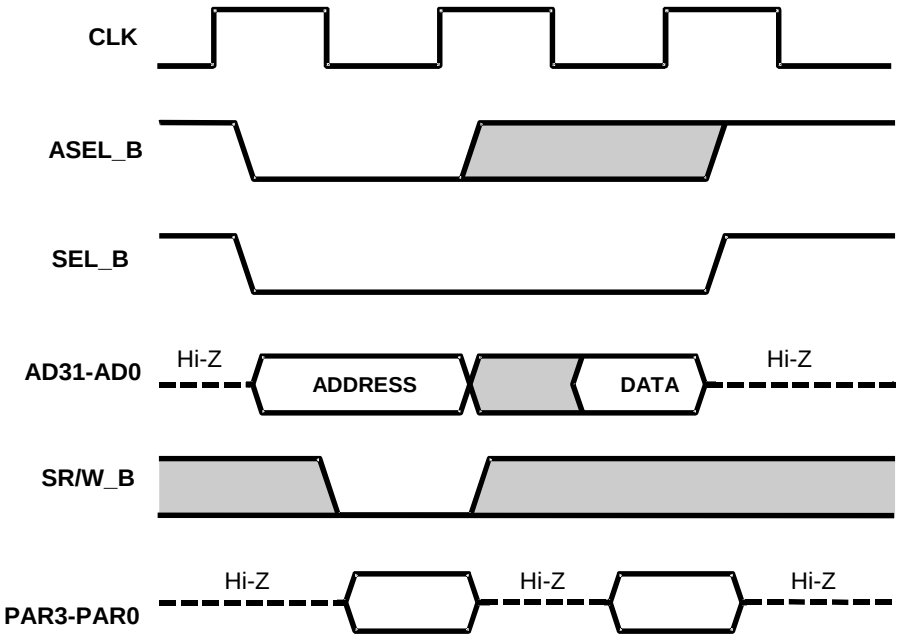
When data is written to the slave, the μPD98405 latches data on AD31 through AD0 at the rising edge of the clock immediately before that which makes the SEL_B signal inactive.

When data is read from the slave, the μPD98405 outputs data to AD31 through AD0 at the rising edge of the clock next to that at which a low level is input as the SEL_B signal. The μPD98405 retains the data output on AD31 through AD0 until the SEL_B signal goes high.

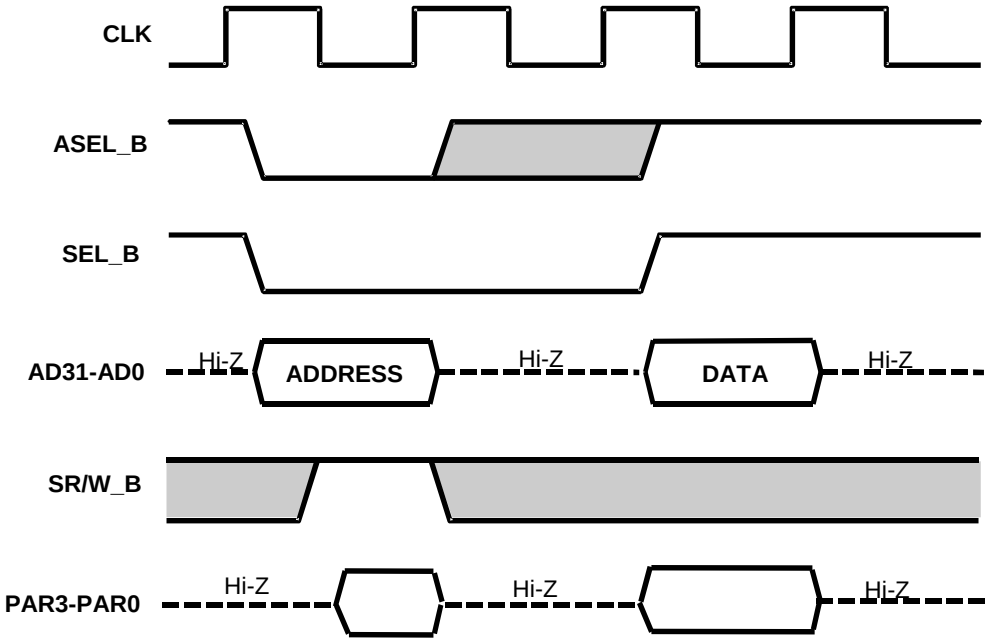
The user can change the timing of the latching and output of data by extending the low level width of the SEL_B signal. Figure 4-9 shows slave operation timing.

Figure 4-9. Slave Access Timing

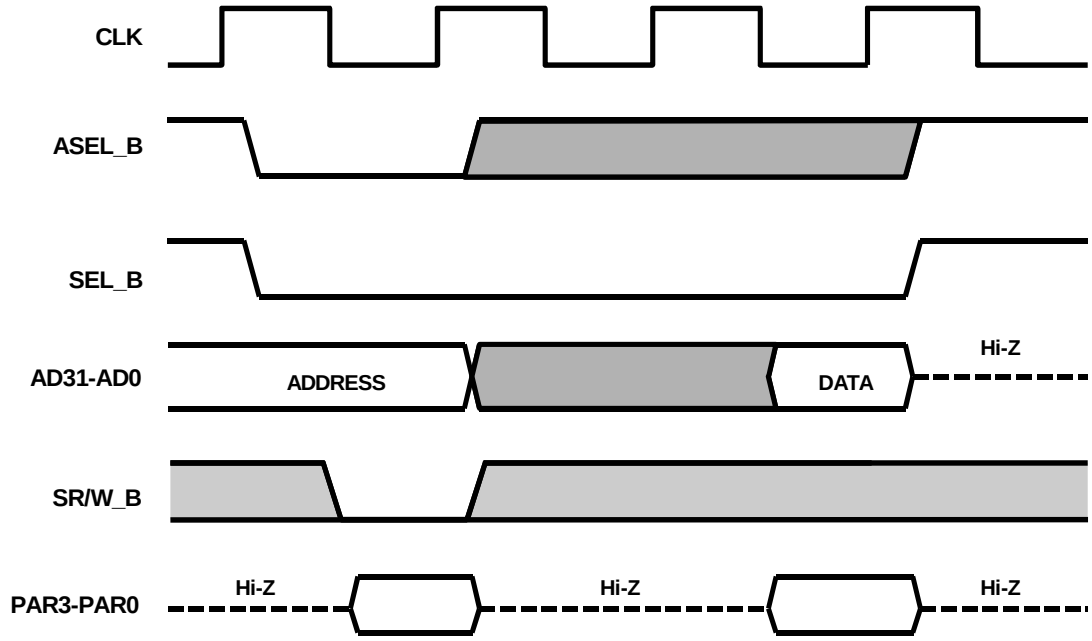
(a) Write timing



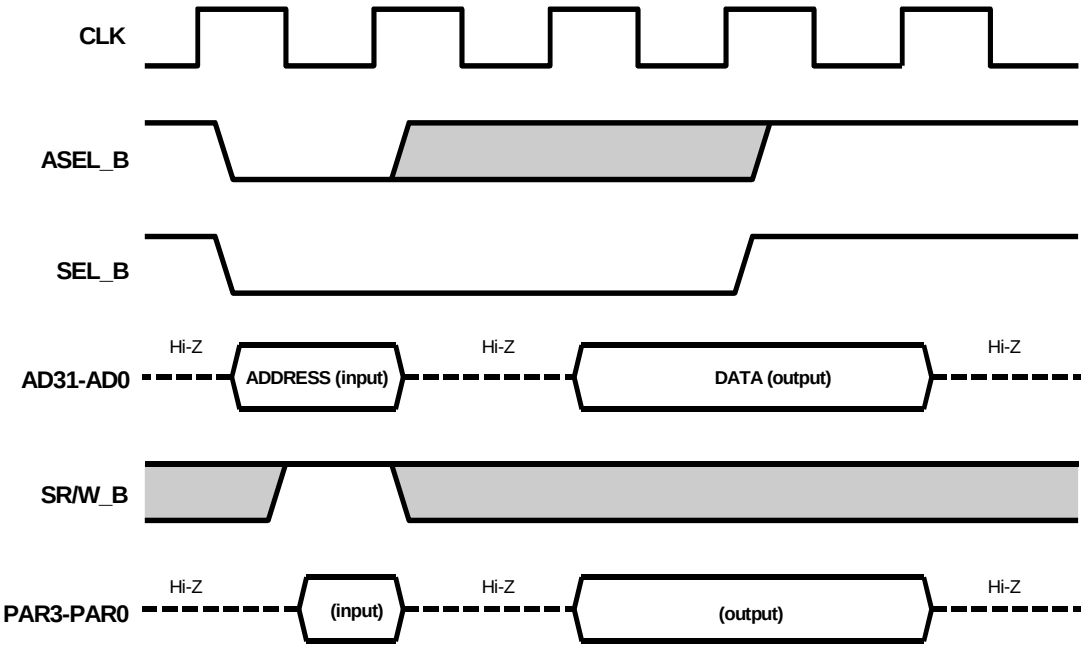
(b) Read timing



(c) Write timing with SEL_B signal extended



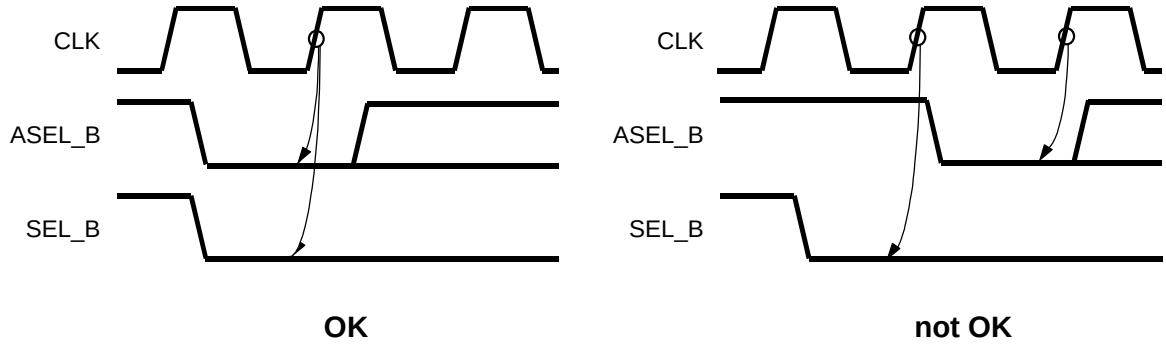
(d) Read timing with SEL_B signal extended



<Notes on slave operation>

1. No slave access requests can be accepted for 20 system bus clock cycles after the system has been reset.
2. If a low level is input to the SEL_B or ASEL_B pin while the μPD98405 is performing master (DMA) operation, the μPD98405 performs slave operation, and samples AD31 through AD0. If the user grants the μPD98405 bus mastership by using the bus arbiter, ensure that the SEL_B and ASEL_B signals do not become active, so that the master and slave operations do not contend.
3. Do not input the falling of the SEL_B signal at least one clock before the ASEL_B signal. Make sure that the μPD98405 detects the low level of the SEL_B signal at the rising of the same clock or a later clock than that at which the low level of the ASEL_B signal is detected. If the low level of the SEL_B signal is detected earlier than that of the ASEL_B signal, a malfunction may occur.

Figure 4-10. Input Timing of SEL_B and ASEL_B Signals



OK **not OK**

4. After the μPD98405 has detected the low level of the ASEL_B signal at the rising edge of the clock, the ASEL_B signal can be set high at the same time as or before the SEL_B signal goes high.
5. The SEL_B signal must be deactivated and held for at least two system bus clock cycles before it can be reactivated.

4.1.5 Little/Big Endian Select Function

The bus interface supports both the little endian and big endian data formats. These formats can be selected by using the "BO bit" of the GMR register.

Selects little or big endian.		
BO bit (GMR: bit 6)	0	Selects little endian. Data is transferred by the μPD98405 in little endian format.
	1	Selects big endian. Data is transferred by the μPD98405 in big endian format.
	Default = 0	

In little endian format, the MSB is stored to the highest address byte. Bits 31 through 24 of a data word are stored to byte 3, and bits 7 through 0 are stored to byte 0.

Figure 4-11. Little Endian Format

Halfword 1		Halfword 0	
Byte 3	Byte 2	Byte 1	Byte 0

AD31 AD16 AD15 AD0

In big endian format, the MSB is stored to the lowest address byte. Bits 31 through 24 of a data word are stored to byte 0, while bits 7 through 0 are stored to byte 3.

Figure 4-12. Big Endian Format

Halfword 0		Halfword 1	
Byte 0	Byte 1	Byte 2	Byte 3

AD31 AD16 AD15 AD0

Only transmit/receive data is subjected to byte order switching based on the little/big endian setting. Other information is always output to the bus, in the format described in this manual. For such information, the user need not check the byte order based on whether little or big endian is selected.

Data output in fixed format	Receive indication
	Transmit indication
	Packet descriptor
	Buffer descriptor
	Receive batch link pointer
	Buffer address and size within receive batch
	Indication of words 12 through 15 of raw cell data
Data output in byte order depending on little/big endian setting	Receive cell data
	Transmit cell data
	Data of words 0 through 11 of raw cell data

Caution The raw cell data transferred to system memory by the μPD98405 consists of data and indication sections. The data section, which consists 12 words from word 0 to word 11, is stored in byte order depending on the little/big endian setting. The indication section, which consists of four words from word 12 to word 15 is, however, stored in the format described in this manual, regardless of the little/big endian setting. Note, therefore, that the data and indication sections are handled differently.

4.2 PCI BUS INTERFACE

The μPD98405 contains a 32/64-bit PCI bus interface. This PCI bus interface can be connected directly to a PCI bus.

4.2.1 Features of the PCI Bus Interface

- Conforms to PCI Local Bus Specification Revision 2.1.
- Supports operation at up to 33 MHz.
- Responds to commands as a medium-speed device.
- Features a configuration register space which conforms to the specifications to enable response to configuration cycles.
- Responds to requests to access μPD98405 internal registers with both memory and I/O commands.
- Processes all memory read commands (Memory Read, Memory Read Multiple, and Memory Read Line) as the same memory read command.
- Processes all memory write commands (Memory Write, Memory Write and Invalidate) as the same memory write command.
- Can respond to each target termination (retry/disconnect/target abort) when the μPD98405 operates as the master.
- Can transfer data at 33 MHz in the zero wait state (as the master device).
- Supports fast back-to-back transactions.
- Supports 64-bit bus expansion (64-bit data transfer, 64-bit addressing).
- Supports the use of an expansion ROM interface (8-bit ROM interface).
- Supports the use of a serial EEPROM interface.
- ★ • The Retry Timer function and TRDY Timer function can be used to detect malfunctions of the target.
- ★ • 5 V PCI and 3.3 V PCI operation possible depending on the power supply (V_{DD5} pin).
- ★ • Supports arbitration parking master operations.

4.2.2 Configuration Register

The configuration register is mapped into the PCI configuration space. A software reset does not initialize the contents of the configuration register. A hardware reset initializes the entire contents of the configuration register to their default values.

For more information on the contents of the configuration register, see "PCI Local Bus Specification Revision 2.1."

★ Offset 40H is a register that is unique to the μPD98405 and is used for the settings of an additional function.

Figure 4-13. Layout of Configuration Register

Offset	31 24	23 16	15 8	7 0
00H	Device ID		Vendor ID	
04H	Status		Command	
08H	Class Code			Revision ID
0CH	BIST	Header Type	Latency Timer	Cache Line Size
10H	IO Base Address			
14H	Memory Base Address			
18H	Reserved			
1CH				
20H				
24H				
28H				
2CH	Subsystem ID		Subsystem Vendor ID	
30H	Expansion ROM Base Address			
34H	Reserved			
38H				
3CH	MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line
40H	Reserved		Retry Timer	TRDY Timer

Table 4-6. Configuration Register

(1/2)

Offset	Name	Bit(s)	R/W	Default	Description
00H	Device ID	31 - 16	R	001DH	μPD98405 device ID
	Vendor ID	15 - 0	R	1033H	NEC vendor ID
04H	Status	31	R/W	0	Detected Parity Error
		30	R/W	0	Signaled System Error
		29	R/W	0	Received Master Abort.
		28	R/W	0	Received Target Abort.
		27	R/W	0	Signaled Target Abort.
		26 - 25	R	01	DEVSEL_B timing. The μPD98405 supports Medium.
		24	R/W	0	Data Parity Error Reported.
		23	R	1	Fast Back-to-Back Capable.
		22 - 16	R	00H	Reserved
	Command	15 - 10	R	00H	Reserved
		9	R	0	Fast Back-to-Back Enable
		8	R/W	0	System Error Enable
		7	R	0	Wait Cycle Enable.
		6	R/W	0	Parity Error Response
		5	R	0	VGA Palette Snoop Enable.
		4	R/W	0	Memory Write and Invalidate Enable.
		3	R	0	Special Cycle Recognition.
		2	R/W	0	Bus Master Enable.
		1	R/W	0	Memory Access Enable
		0	R/W	0	I/O Access Enable
08H	Class Code	31 - 24	R	02	Basic class: Network controller
		23 - 16	R	03	Subclass: ATM controller
		15 - 8	R	00	Programming interface
	Revision ID	7 - 0	R	01H	Contains device revision information.
0CH	BIST	31 - 24	R	00H	Used to control the built-in self test and indicates its status.
	Header Type	23 - 16	R	00H	Configuration space header type
	Latency Timer	15 - 8	R/W	00H	Contains the master latency timer value for the PCI bus master. The low-order 3 bits of the set value are masked. The value becomes 8, 16, … , 248.
	Cache Line Size	7 - 0	R/W	00H	Specifies the system cache line size in word (32-bit) units. Only the values 4, 8 and 16 are valid. Cache Line Size is not set if other values are specified.
10H	IO Base Address	31 - 8	R/W	00H	Base address. 256-byte support.
		7 - 1	R	00H	Reserved
		0	R	1	IO space indicator

(2/2)

Offset	Name	Bit(s)	R/W	Default	Description
14H	Memory Base Address	31 - 12	R/W	00H	Base address. 4K-byte support.
		11 - 4	R	0H	Reserved
		3	R	0	Prefetch (disable)
		2 - 1	R	00	Type (the base address can be mapped onto any 32-bit boundary.)
		0	R	0	Memory Space Indicator
18H 1CH	Reserved	31 – 0	R	all 0	
20H 24H 28H	Reserved	31 - 0	R	all 0	
2CH	Subsystem ID	31 - 16	R	0000H	Subsystem ID. Can be loaded from an external serial EEPROM.
	Subsystem Vendor ID	15 - 0	R	0000H	Subsystem vendor ID. Can be loaded from an external serial EEPROM.
30H	Expansion ROM Base Address	31 - 16	R/W	0000H	Base address. Specifies the base address of the 64K-byte expansion ROM.
		15 - 1	R	all 0	Reserved
		0	R/W	0	Address Decode Enable. Enables access to the expansion ROM. 0: Disable (initial value), 1: Enable
34H 38H	Reserved	31 - 0	R	all 0	
3CH	MAX_LAT	31 - 24	R	00H	Sets the value of the latency timer. Can be loaded from an external serial EEPROM.
	MIN_GNT	23 - 16	R	00H	
	Interrupt Pin	15 - 8	R	01H	Specifies an interrupt pin using INTA#.
	Interrupt Line	7 - 0	R/W	00H	Specifies the interrupt line of the interrupt controller connected to μPD98405 interrupt signals.
40H	Reserved	31 - 16	R	all 0	
★	Retry Timer	15 - 8	R/W	00H	Specifies the maximum retry count for the μPD98405. After a reset, a value of 00H is loaded as the initial value and the timer is disabled. The maximum retry count includes retries, disconnects, and latency time-outs. To enable the timer, set a value other than 0. If no response is returned after the specified number of retries while the timer is enabled, the μPD98405 sets the FERR bit of the GSR register and stops the operation until it is reset.
	TRDY Timer	7 - 0	R/W	00H	Specifies the maximum number of clocks in which the μPD98405 waits for TRDY_B. After a reset, a value of 00H is loaded as the initial value and the timer is disabled. To enable the timer, set a value other than 0. If no response is made while the μPD98405 is waiting for TRDY_B in the specified number of clocks while the timer is enabled, the μPD98405 sets the FERR bit of the GSR register and stops the operation until it is reset.

When the μPD98405 recognizes that a serial EEPROM is connected, the Subsystem Vendor ID, Subsystem ID, and MIN_GNT/MAX_LAT fields of the configuration register are loaded from the external serial EEPROM after power-on.

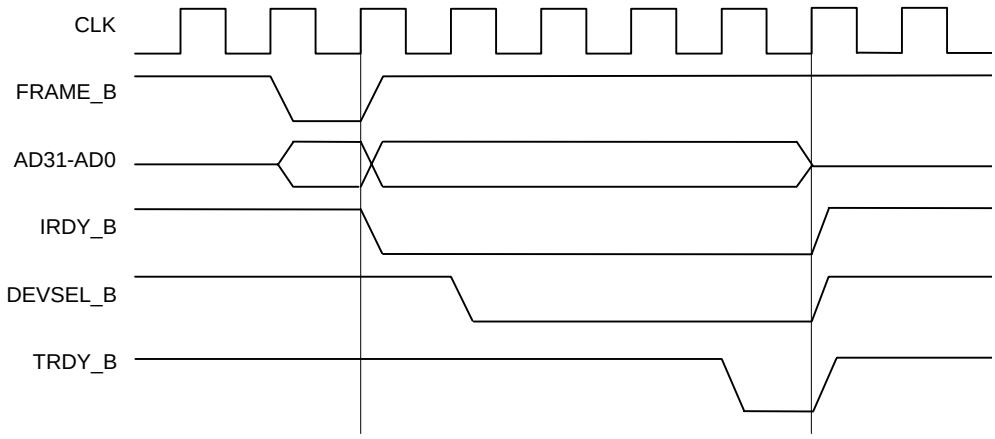
4.2.3 Slave Transactions

During slave transactions, the μPD98405 performs 1-word burst transfer. It also responds to memory commands and I/O commands when all of data byte enable 3 through 0 (PCBE_B[3:0]) are set to 0.

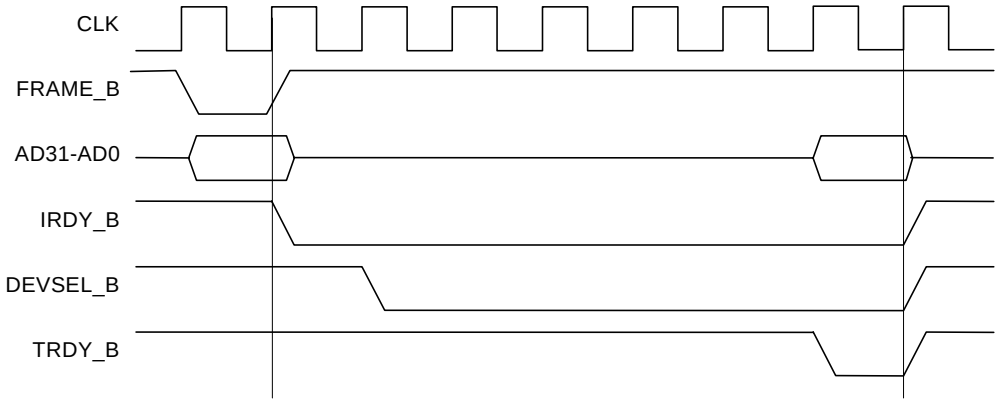
If the μPD98405 receives a slave access request with an invalid address, it does not respond to that request. (It does not activate DEVSEL_B.) The slave transaction timing is shown below.

Figure 4-14. Slave Transaction Timing

(a) Write transaction



(b) Read transaction



★ Characteristics of Slave Transmission

- Responds to medium speed device commands (DEVSEL_B response.)
- All memory read commands (memory read, memory read multiple and memory read line) are handled as memory read.
- All memory write commands (memory write, memory write and invalidate) are handled as memory write.

4.2.4 Master Transactions

(1) Master transactions

For master transactions, the μPD98405 supports 1- to 16-word burst transfer and multiple cell burst transfer. The μPD98405 activates REQ_B to request the bus arbiter for PCI bus mastership. When the bus arbiter activates GNT_B and grants bus mastership to the μPD98405, the μPD98405 samples FRAME_B and IRDY_B at the rising edge of the clock and waits for the PCI bus to enter the idle state. When the μPD98405 detects that both signals have been deactivated and that the PCI bus has entered the idle state, it starts a transaction.

For a write transaction in which data is transferred from the μPD98405 to system memory, the μPD98405 activates FRAME_B to indicate that it has started the transaction. FRAME_B is kept active immediately before transfer of the last data. An address phase starts at the first clock edge after the μPD98405 activates FRAME_B. The μPD98405 drives an address on AD31 through AD0 and a transaction type on PCBE3_B through PCBE0_B. A data phase starts at the next clock edge. The μPD98405 drives the data on AD31 through AD0. It also drives PCBE3_B through PCBE0_B to indicate the valid byte positions on AD31 through AD0. When the μPD98405 detects that both TRDY_B and IRDY_B have been activated, it recognizes the first data phase to be complete and drives the next data on AD31 through AD0.

For a read transaction in which data is transferred from system memory to the μPD98405, the μPD98405 activates FRAME_B to indicate that the μPD98405 has started a transaction. FRAME_B is kept active immediately before transfer of the last data. The μPD98405 drives an address on AD31 through AD0 and a transaction type on PCBE3_B through PCBE0_B at the first clock edge after FRAME_B is activated. At the next clock edge, the μPD98405 stops driving AD31 through AD0 and allows the target to control the bus. At the same clock edge, the μPD98405 changes the information driven on PCBE3_B through PCBE0_B to notification of the valid byte positions on AD31 through AD0. The μPD98405 also activates IRDY_B to indicate that it is ready to receive the first data from the target. When the μPD98405 samples TRDY_B and IRDY_B and detects that both signals have been activated, it latches the first data on AD31 through AD0. The target drives the next data and activates TRDY_B to indicate that the next data has been driven.

★ **Remark**

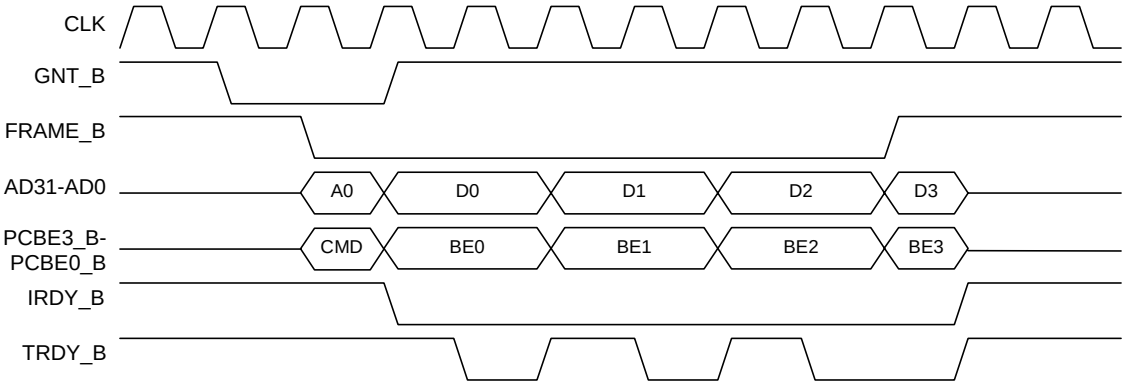
<REQ_B operation with master>

The μPD98405 de-asserts REQ_B when a latency timeout occurs. Burst transmission continues if GNT_B continues to be asserted, but transmission ends immediately with a timeout if GNT_B is de-asserted when REQ_B is de-asserted. Specify a larger value for the PCI configuration register Latency timer if you wish to assert REQ_B for longer.

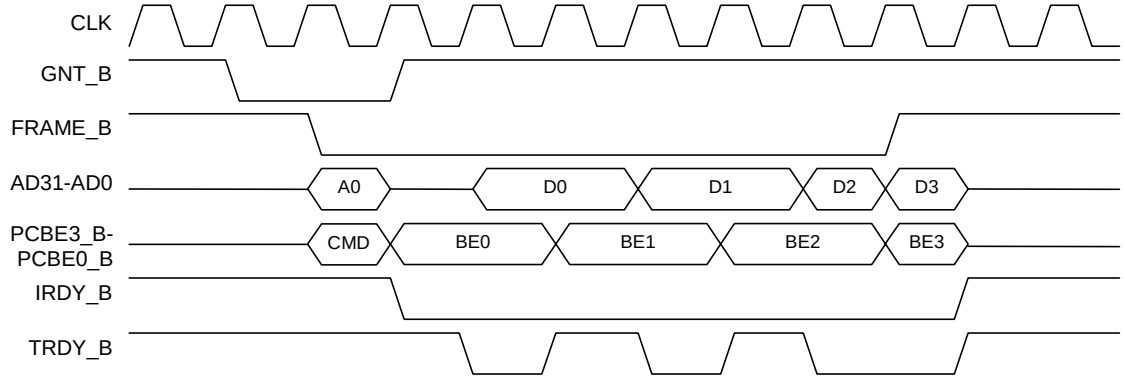
The following figure shows the master transaction timing.

Figure 4-15. Master Transaction Timing

(a) PCI write transaction (from μPD98405 to target)



(b) PCI read transaction (from target to μPD98405)



The μPD98405 issues a read/write command for a master transaction according to the following rules:

(a) Read transaction

- Memory Read (0110): When the number of words to be transferred is 1
- Memory Read Line (1110): When the number of words to be transferred is greater than 1 and data up to the next cache line boundary is to be read
- Memory Read Multiple (1100): When the data block to be read crosses a cache line boundary.

★ **Caution With the μPD98405, a memory read is always issued if Cache Line Size is not set (Cache Line Size is other than 4, 8 or 16).**

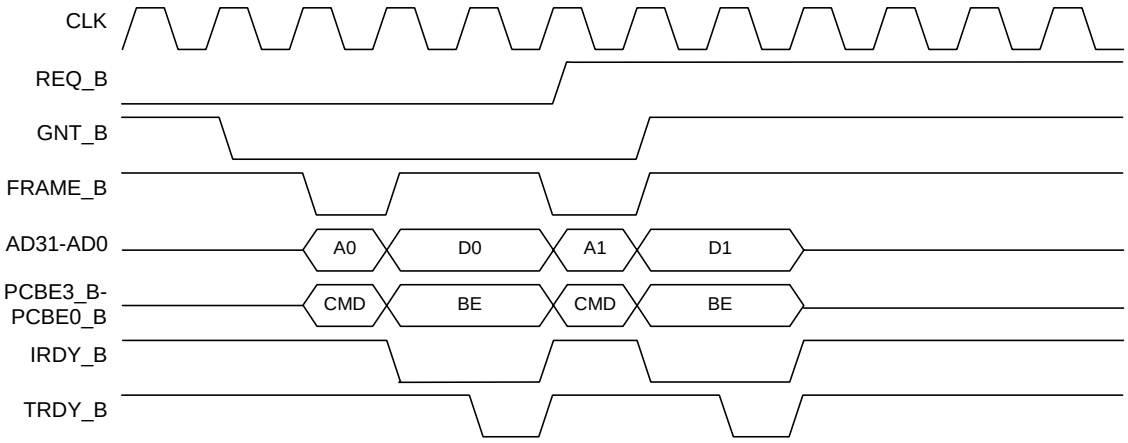
(b) Write transaction

- Memory Write And Invalidate (1111): When all the following three conditions are satisfied:
  - **<1>** The number of words to be transferred is equal to the number of cache lines.
  - **<2>** The Memory Write and Invalidate Enable bit of the configuration register is set to 1.
  - **<3>** The start address of the write transaction is on a cache boundary.
- Memory Write (0111): For cases other than the above

(2) Fast back-to-back transactions

For a given target, the μPD98405 supports fast back-to-back transactions. A fast back-to-back transaction is executed only for a write to write transition. Upon a transition from a write transaction to a read transaction, fast back-to-back transactions are terminated. The following figure shows the fast back-to-back transaction timing. This figure shows an example of 1-word burst.

Figure 4-16. Fast Back-to-Back Transaction Timing



Whether to enable fast back-to-back transactions is set in the BBL field of the GMR register. As many fast back-to-back transactions as the number set in the BBL field are enabled. The maximum count is 7. The following table lists each setting of the BBL field and the corresponding fast back-to-back transaction count.

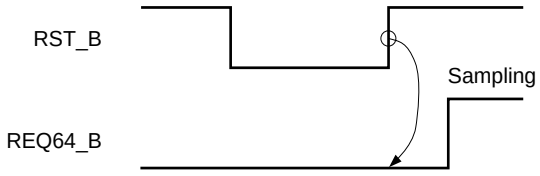
BBL field	Fast back-to-back transaction count
000	Disabled.
001	1
010	2
011	3
100	4
101	5
110	6
111	7
Default = 000: Disabled.	

When the setting in the BBL field enables fast back-to-back transactions, the μPD98405 attempts to execute master transactions in fast back-to-back mode whenever the target responds to a fast back-to-back transaction.

(3) 64-bit bus expansion

The μPD98405 supports 64-bit bus expansion (64-bit data transfer and 64-bit addressing).

When using 64-bit data transfer, set the E64 bit of the GMR register to 1. Make REQ64_B low at the end of a reset (when RST_B rises). The μPD98405 samples REQ64_B at the rise of RST_B.



When the E64 bit is set to 1, the μPD98405 requests 64-bit data transfer, and the target executes 64-bit data transfer in response. When the target fails to respond to the request (when ACK64_B is not set to active low), 32-bit data transfer is performed.

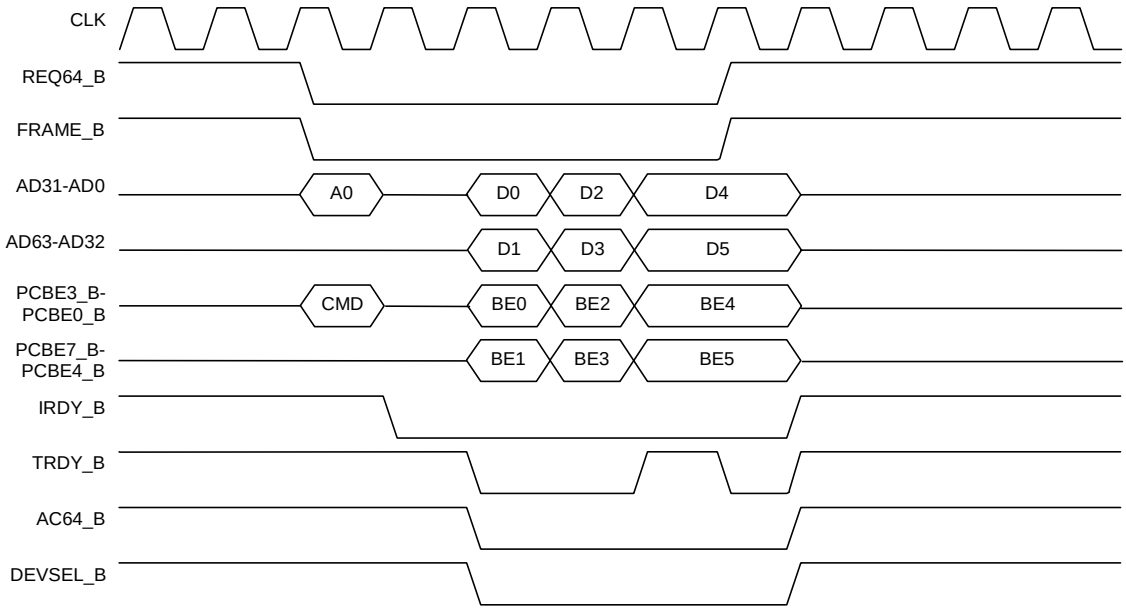
When using 64-bit addressing (DAC command), set the value of the high-order 32 bits of the 64-bit address in the PBAH register. The μPD98405 executes 64-bit addressing using the high-order 32-bit addresses set in the PBAH register. When 0 is set in the PBAH register, the μPD98405 executes 32-bit addressing.

The 64-bit bus expansion function is supported only when the μPD98405 is being used as a master. When the μPD98405 is acting as a target, the 32-bit bus function is used.

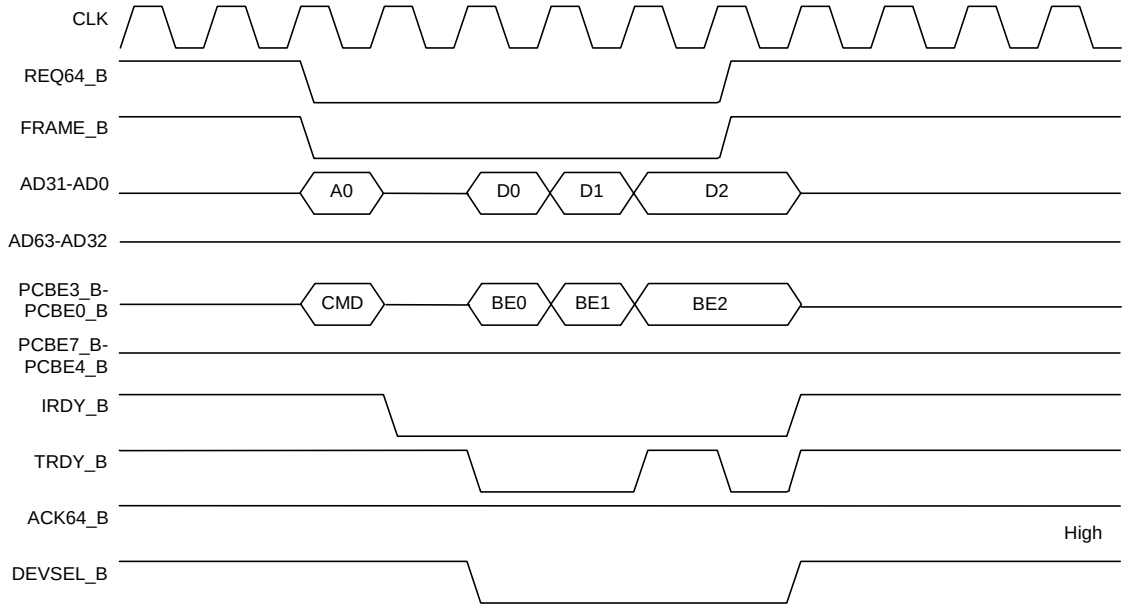
The following figure shows the 64-bit bus transaction timing.

Figure 4-17. 64-Bit Bus Transaction Timing

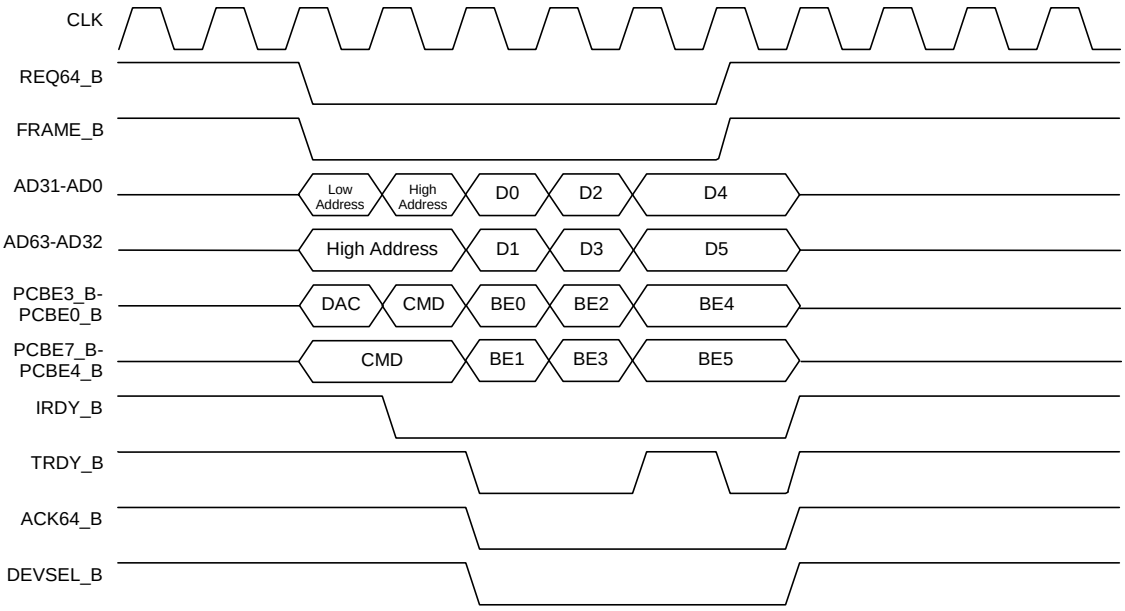
(a) 64-bit request and 64-bit transfer (read cycle)



(b) 64-bit request and 32-bit transfer (read cycle)



(c) 64-bit addressing and 64-bit transfer (read cycle)



(4) Master termination

When the μPD98405 operates as the master, it terminates the transaction in one of the following modes.

<1> The transaction terminates normally. (Normal end)

<2> Another master deactivates GNT_B for the μPD98405, to obtain bus mastership and the Latency Timer time has elapsed. (Time-out)

<3> No target responded to the address. (Master abort)

Figure 4-18. Time-Out Termination (Latency Timer: 8)

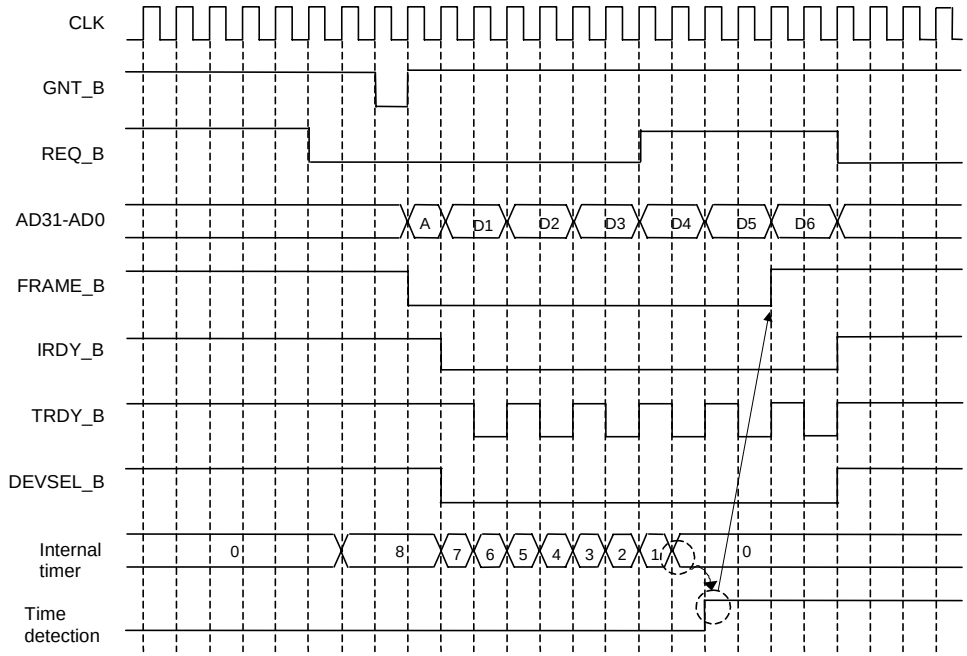
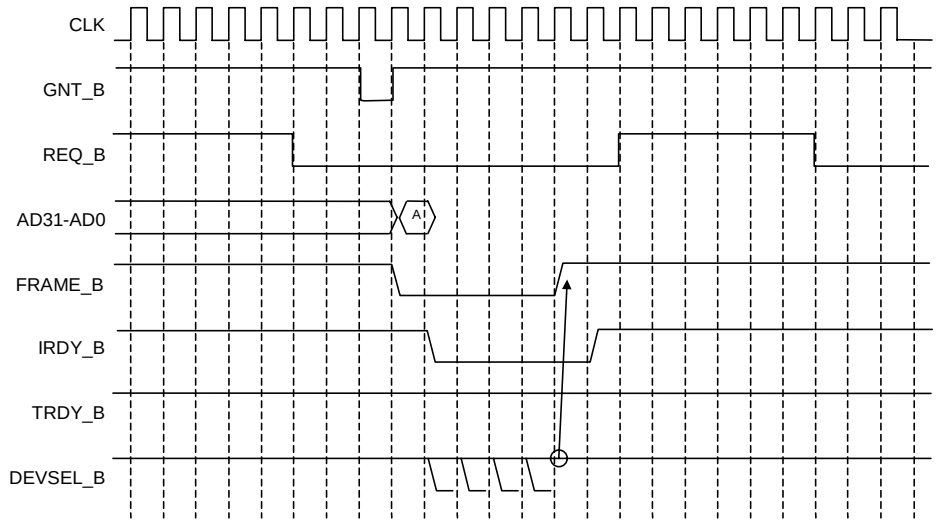


Figure 4-19. Master Abort Termination (No Target Responds to DEVSEL_B)



(5) Target termination

When the μPD98405 operates as the target, it may execute retry, disconnect, or target abort processing to request the termination of the transaction.

a) Retry

- The host system issues a command to the EECR register of the μPD98405 to access an external EEPROM. The μPD98405 cannot accept such a command successively because a fixed time is required for the μPD98405 to access the external EEPROM. Therefore, when the EECR register is accessed successively, the μPD98405 requests a retry.
- If the command FIFO is full when the host system attempts to issue a command, the μPD98405 request a retry.

b) Disconnect

- When a μPD98405 internal register (direct address register or configuration register) is accessed by performing burst transfer, the μPD98405 activates STOP_B to disconnect the transaction when 1-word transfer terminates.
- When an external expansion ROM is accessed by performing burst transfer, the μPD98405 disconnects the transaction.

c) Target abort

- When the μPD98405 receives an address and detects a parity error in it, it performs target abort processing.
- When PCBE3_B through PCBE0_B for a data transaction are not all 0, the μPD98405 performs target abort processing.

4.2.5 Burst Size

(1) Normal burst

The μPD98405 normally reads/writes cell data by performing 12-word burst DMA transfer. (When multi-cell transfer is enabled, the μPD98405 performs burst transfer for several cells. See **Section 4.2.5 (2)**.) 12-word burst means 1-cell burst transfer. When the transmit data or receive buffer is shorter than 12 words, the μPD98405 performs burst transfer of the corresponding size. The following table lists the burst sizes for other than cell data.

Table 4-7. DMA Transfer Burst Sizes

Read/write	Data type	Burst size
Read	Packet descriptor	4 words
	Buffer descriptor	2 words
	Receive batch (size, address)	2 words
	Receive batch link pointer	1 word
Write	Transmission indication	1 word
	Reception indication	4 words
	Receive batch link pointer	1 word
	Raw cell data	16 words

(2) Multi-cell transfer

The μPD98405 supports multi-cell burst transfer to improve the performance of the bus. The multi-cell burst transfer function is supported for cell data transfer for transmission and reception. The transmitter also supports per-VC queuing. Multi-cell burst transfer is not supported for raw cell reception.

Remark Multi-cell transfer means long burst in cell units. The μPD98405 does not support burst transfer such as 30-word (= 2.5 cells) burst transfer.

(Multi-transmit cell transfer and per-VC queuing)

The μPD98405 supports multi-cell transfer for each VC. Whether to enable multi-cell transfer is set in the MBL field of the transmit VC table. The maximum burst size for multi-cell transfer is 2 to 5 cells, and can be set in cell units. (1-cell transfer is always enabled.)

The following table lists each setting of the MBL field and the corresponding multi-cell transfer size.

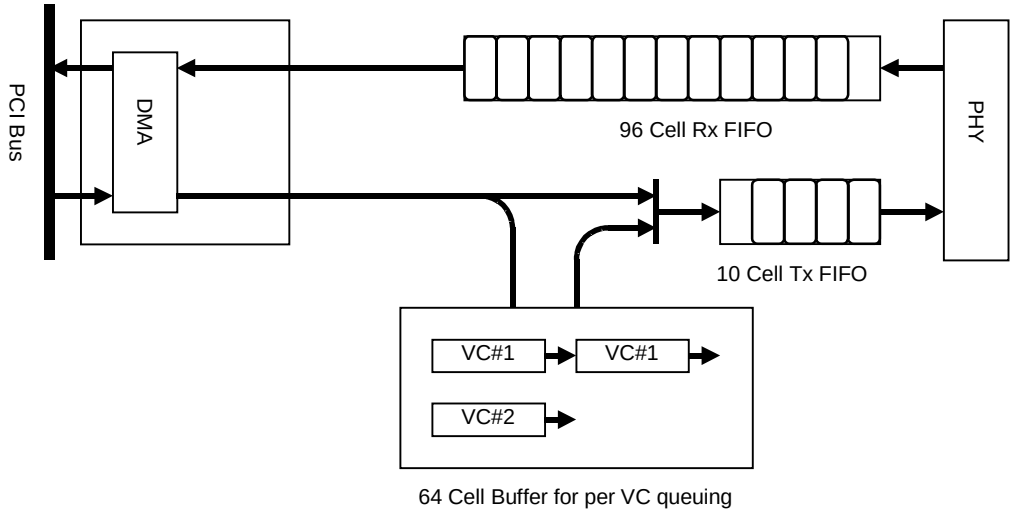
MBL field	Maximum burst size for multi-cell transfer
000	Disabled.
001	Disabled.
010	2 cells
011	3 cells
100	4 cells
101	5 cells
110	5 cells
111	5 cells

Multi-transmit cell transfer is supported by per-VC queuing. The μPD98405 contains a cell buffer which can contain up to 64 cells, for per-VC queuing. For a VC for which multi-cell transfer is enabled, the μPD98405 allocates a cell buffer area and performs per-VC queuing. When the μPD98405 has allocated the area, it creates a queue for each VC in the buffer and reads transmit data by performing multi-cell transfer. When multi-cell transfer is enabled for multiple VCs, it may not be possible to allocate an area of the size required for a VC. In this case, the μPD98405 reads as much data as the size of the cell buffer areas that can be allocated. For example, when 5-cell transfer is enabled for VC1, but only an area which can contain 2 cells can be allocated in the cell buffer, the μPD98405 performs 2-cell transfer. If no cell buffer area can be allocated, the μPD98405 performs normal 1-cell burst transfer. As the number of VCs for which multi-cell transfer is enabled increases, the more difficult it becomes to allocate a cell buffer area, so multi-cell transfer may not be performed for VCs.

A cell buffer area is requested when the target VC is selected by the scheduler and has data to be transmitted. When data received during multi-cell transfer has been stored into the transmit FIFO, the cell buffer area is released. When a VC is active, the μPD98405 does not always allocate a cell buffer area for the VC.

A block diagram of per-VC queuing is shown below.

Figure 4-20. Per-VC Queuing Block Diagram



(Multi-receive cell transfer)

The μPD98405 supports multi-receive cell transfer. Whether to enable multi-cell transfer is set in the MBL field of the receive VC table. The maximum burst size for multi-cell transfer is 2 to 5 cells, and can be set in cell units. (1-cell transfer is always enabled.)

The following table lists each setting of the MBL field and the corresponding multi-cell transfer size.

MBL field	Maximum burst size for multi-cell transfer
000	Disabled.
001	Disabled.
010	2 cells
011	3 cells
100	4 cells
101	5 cells
110	5 cells
111	5 cells

When the μPD98405 successively receives cells from the same VC (for which multi-cell transfer is enabled), that is, when cells from the same VC are contiguously stored into the receive FIFO, it writes the receive data into system memory by performing multi-cell transfer. When the μPD98405 does not successively receive cells from the same VC, it performs normal 1-cell burst transfer, regardless of whether multi-cell transfer is enabled for the VC. For example, when 5-cell transfer is enabled for VC1 and the μPD98405 receives a cell from another VC after successively receiving 2 cells from VC1, the μPD98405 performs 2-cell transfer for VC1.

Because the μPD98405 performs multi-cell transfer only when it successively receives cells from the same VC, multi-cell transfer for other VCs is not affected when multi-cell transfer is enabled for multiple VCs.

(3) Burst size split function

The μPD98405 performs 12-word burst transfer for normal DMA transfer and 1- to 5-cell burst transfer for multi-cell DMA transfer. During DMA transfer, the μPD98405 supports a function for automatically splitting the burst size with PCI bus cache boundaries considered.

When the AD bit of the GMR register is set to 1, this function is disabled. The μPD98405 attempts to perform DMA transfer in 12-word burst or multi-cell transfer mode without considering the DMA transfer start address or cache boundaries. When the AD bit is set to 0, the μPD98405 splits the burst size with the DMA transfer start address and cache boundaries considered. When this function is enabled, burst transfer is not disconnected at any cache boundary. For multi-cell transfer, the burst size is also split automatically. This function is also supported for non-cell data (such as transmission or reception indication) DMA transfer. By default, the AD bit is set to 0 to enable this function.

When the AD bit is set to 0 (the burst size split function is enabled), the μPD98405 splits the burst size using the DMA transfer start address and the value of the cache line size field of the configuration register so that the data to be transferred does not cross any cache boundaries. The host system must set its cache line size in the configuration register. If the cache line size is not set (if it is other than 4, 8, or 16), the burst size split function will not operate, regardless of whether the AD bit is set to 0. In this case, the μPD98405 operates in the same way as when the AD bit is set to 1.

When the AD bit is set to 0, the μPD98405 performs burst transfer for the data from the DMA transfer start address to the cache line size, then performs burst transfer for the remaining data.

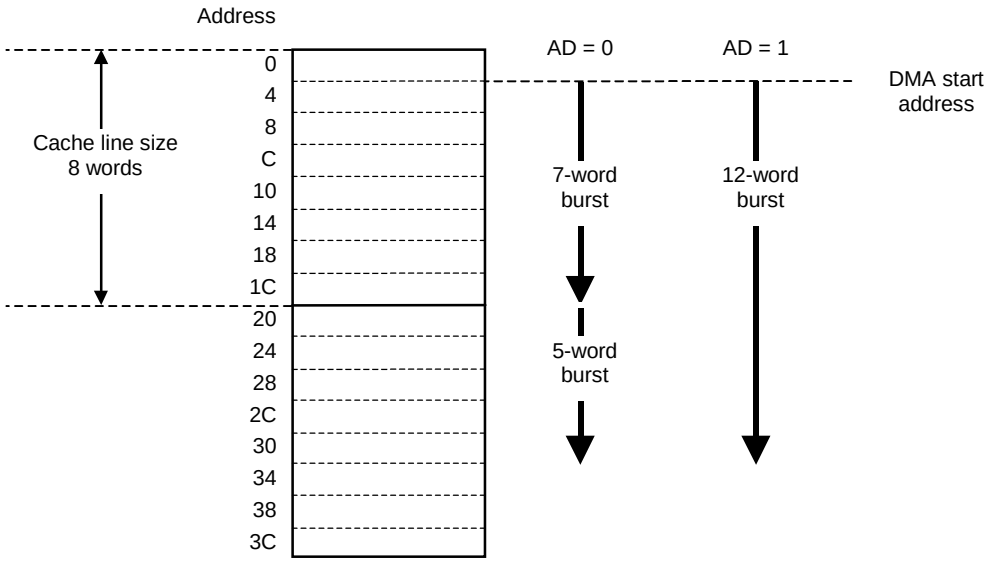
An example of the AD bit function is shown below.

Figure 4-21. Example of AD Bit Function

Cache line size: 8 words

DMA transfer start address: 04H

Multi-cell transfer is disabled.



The following figures show burst size transition when the AD bit is set to 0.

Figure 4-22. Burst Size Transition When AD = 0 (12-Word Transfer)

Cache size	8 words	8 words	16 words	16 words	16 words
DMA transfer start address	00H	04H	00H	04H	10H
1 cell	8W	7W	12W	12W	12W
	4W	5W			
1 cell	4W	3W	4W	3W	12W
	8W	8W	8W	9W	
		1W			
1 cell	8W	7W	8W	7W	4W
	4W	5W	4W	5W	8W
1 cell	4W	3W	12W	11W	8W
	8W	8W			
		1W		1W	4W
1 cell	8W	7W	12W	12W	12W
	4W	5W			
1 cell	4W	3W	4W	3W	12W
	8W	8W	8W	9W	
		1W			
1 cell	8W	7W	8W	7W	4W
	4W	5W	4W	5W	8W
1 cell	4W	3W	12W	11W	8W
	8W	8W			
		1W		1W	4W

Remark ---------- : Cache boundary

Figure 4-23. Burst Size Transition When AD = 0 (Multi-Cell Transfer (5 Cells))

Cache size	8 words	16 words	16 words
DMA transfer start address	00H	00H	10H
5 cells	8W	16W	12W
(60 words)	8W		
	8W	16W	16W
	8W		
	8W	16W	16W
	8W		
	8W	12W	16W
	4W		
5 cells	4W	4W	16W
(60 words)	8W	16W	
	8W		16W
	8W	16W	
	8W		16W
	8W	16W	
	8W		12W
	8W	8W	
5 cells	8W	8W	4W
(60 words)	8W	16W	16W
	8W		
	8W	16W	16W
	8W		
	8W	16W	16W
	8W		
	4W	4W	8W

Remark ---------- : Cache boundary

(4) Byte alignment data transfer

The μPD98405 supports a burst size select function for byte alignment data. The receive buffer may be located on a byte boundary. Transmission data may start on a byte boundary. For DMA read/write transfer in such a case, the μPD98405 adds 1 word to the burst size. For example, the μPD98405 performs 13-word burst for 12-word burst to transfer 1 cell.

- Byte alignment transfer for transmit data

  During a transmit data read transaction, the μPD98405 reads the data in 32-bit (word) units regardless of whether the transmit data starts on a word boundary, and internally ignores all unnecessary bytes. For example, when 1-cell transmit data starts on a byte boundary, the μPD98405 reads the data by performing 13-word burst and internally ignores all unnecessary bytes.

- Byte alignment transfer for receive data

  During a receive data write transaction, when the receive buffer is located on a byte boundary, the μPD98405 writes the data in word units and outputs signals indicating valid bytes on PCBE_B[3:0]. It outputs an address in word units. For example, the μPD98405 performs 13-word burst to write 1-cell receive data into the receive buffer on a byte boundary.

  This example is shown below.

Figure 4-24. Example of Storing Cell Data into a Buffer on a Byte Boundary

Buffer start address AD[1:0] = 10, 13-word burst

Buffer address[1:0] =	31 – 24	23 – 16	15 – 8	7 – 0	PCBE_B[3:0]
00	Payload1	Payload0	(don't care)	(don't care)	0 0 1 1
01	Payload5	Payload4	Payload3	Payload2	0 0 0 0
02	Payload9	Payload8	Payload7	Payload6	0 0 0 0
03	Payload13	Payload12	Payload11	Payload10	0 0 0 0
0a	Payload41	Payload40	Payload39	Payload38	0 0 0 0
0b	Payload45	Payload44	Payload43	Payload42	0 0 0 0
0c	(don't care)	(don't care)	Payload47	Payload46	1 1 0 0

The function for adding 1 word to the burst size for byte alignment data is supported not only for 1-cell transfer, but also for all burst sizes for transmission and reception. It is also supported for multi-cell transfer. For example, to perform byte alignment transfer for 5-cell (60-word) transfer, the μPD98405 transfers data with a 61-word burst size. In a mode in which the AD bit is set to 0 to consider cache boundaries, however, the μPD98405 does not add 1 word to the burst size when a cache boundary is crossed.

4.2.6 PCI Bus Status Information

The μPD98405 provides two status bits that are related to PCI bus operation in the GSR register. These bits are set only when the μPD98405 operates as the master.

(1) PERR: Bit 22

The PERR bit indicates a parity error state on the PCI bus interface. This bit is set to 1 when either of the following conditions is satisfied:

- When the μPD98405 writes data as the master, it detects that the target has activated PERR_B.
- When the μPD98405 reads data as the master, it detects a parity error during a data phase.

Caution The operation of the μPD98405 is not guaranteed when and after a parity error has been detected. Whenever a parity error is detected, reset the μPD98405.

(2) FERR: Bit 21

The FERR bit indicates that a fatal error like those listed below was detected during data transfer. When the FERR bit is set, the μPD98405 stops all bus operations other than responses to slave access requests. When this bit is set, reset the μPD98405. This bit indicates that one of the following errors has occurred:

- The μPD98405 performed master abort termination because the target had not activated DEVSEL_B.
- The target activated STOP_B and performed target abort processing.
- The retry timer counted up to the retry count set in the Retry Timer register of the configuration register, and the transaction terminated.
- The TRDY timer counted up to the clock count set in the TRDY Timer register of the configuration register, and the transaction terminated.

Figure 4-25. Transaction Termination by Retry Timer (Retry Timer Register: 2)

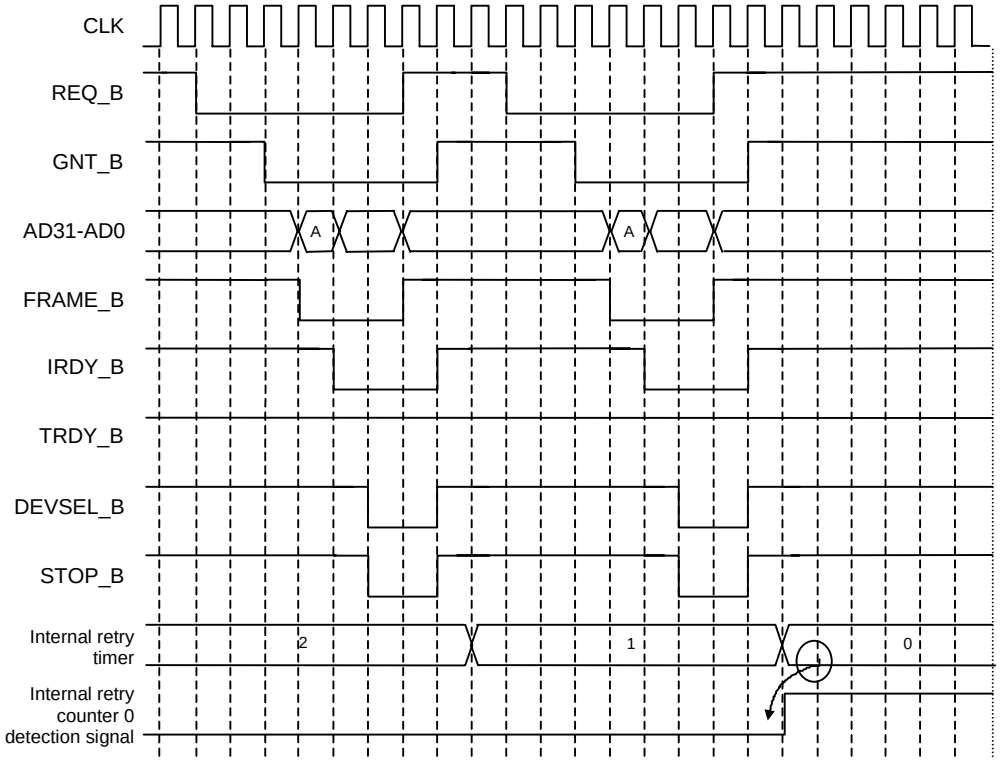
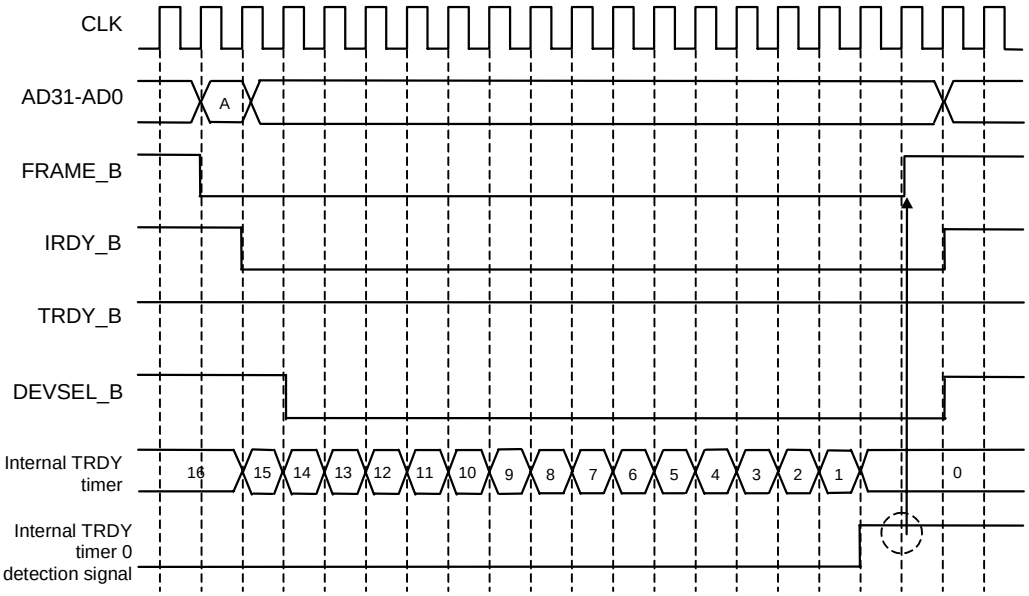


Figure 4-26. Transaction Termination by TRDY Timer (TRDY Timer Register: 16)



4.2.7 Expansion ROM Interface

The μPD98405 has a low-speed 8-bit ROM interface (with an access time of 200 ns) to connect an expansion ROM for loading the operating system. The ROM interface performs simple access of byte data at a 2-byte address using a chip select signal and output enable signal. This interface can be connected with +5 V or +3.3 V expansion ROM.

The expansion ROM interface has the following signals:

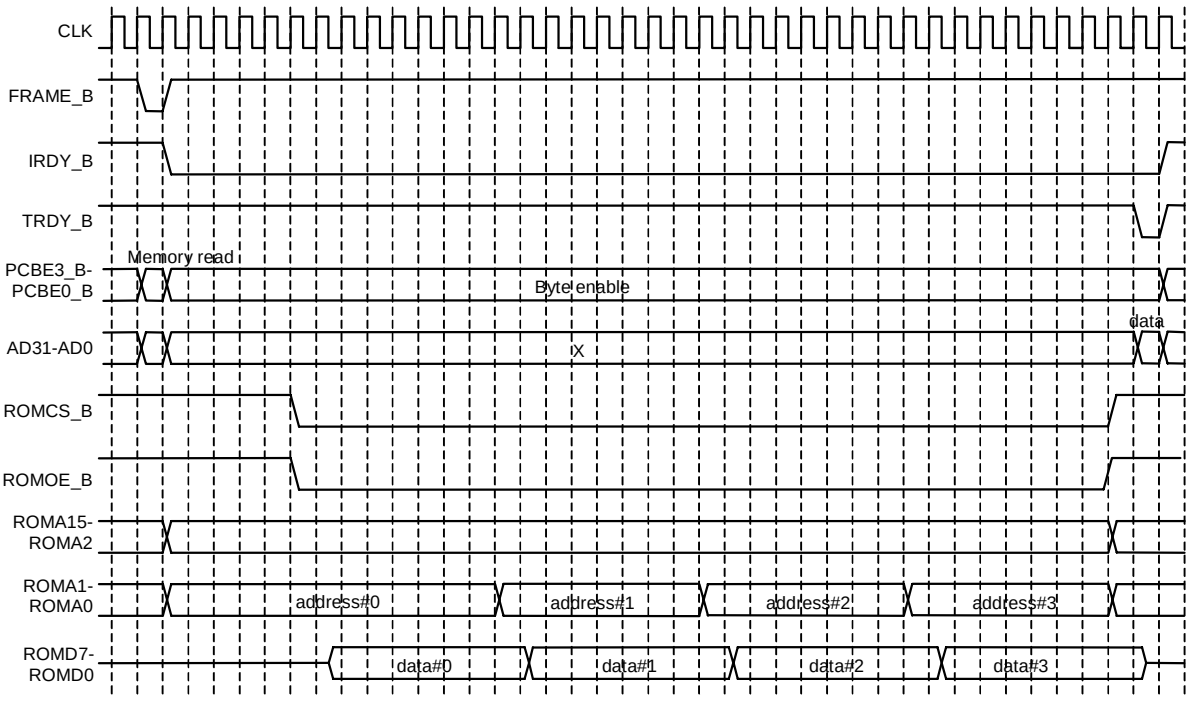
- ROMA15-ROMA0 (output): 16-bit address bus
- ROMD7-ROMD0 (input): 8-bit data bus
- ROMCS_B (output): Chip select
- ROMOE_B (output): Output enable signal

To enable access to an expansion ROM, the Expansion ROM Base Address field of the configuration register must be set.

Because the PCI bus interface is 32 bits wide, when the bus master reads ROM data, the μPD98405 obtains data from ROM four times, byte by byte, assembles 32-bit (word) data, then outputs the data to the bus. During this operation, the μPD98405 keeps the TRDY_B signal on the PCI bus active.

When the bus master attempts to perform burst transfer to the expansion ROM, the μPD98405 activates STOP_B and releases the bus after transferring 1-word data.

Figure 4-27. Expansion ROM Interface Timing



4.2.8 Serial EEPROM Interface

(1) Serial EEPROM interface

The μPD98405 can be connected to an external EEPROM. The external EEPROM is used to store part of the contents of the configuration register and automatically load it after a hardware reset. This interface can be connect with +5 V or +3.3 V EEPROM.

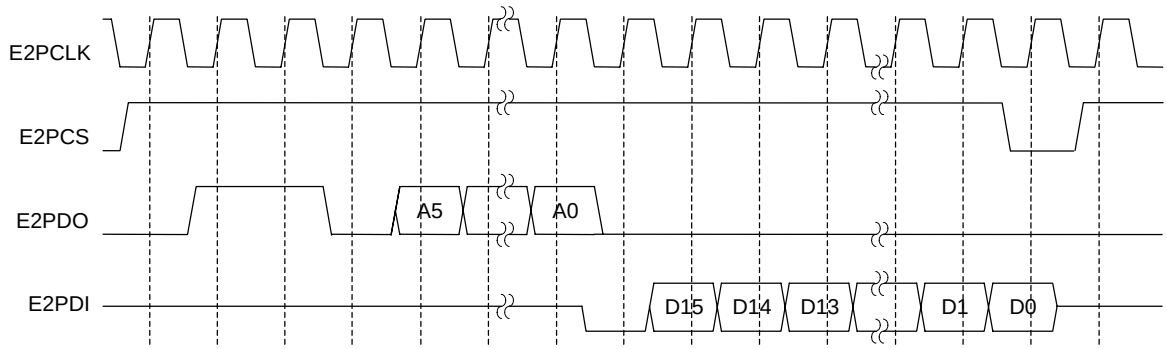
The EEPROM interface uses the following signal buses:

- E2PCS (output): Chip select bus
- E2PDI (input): Serial data input bus
- E2PDO (output): Serial data output bus
- E2PCLK (output): Clock output bus (System bus clock scaled by 36)

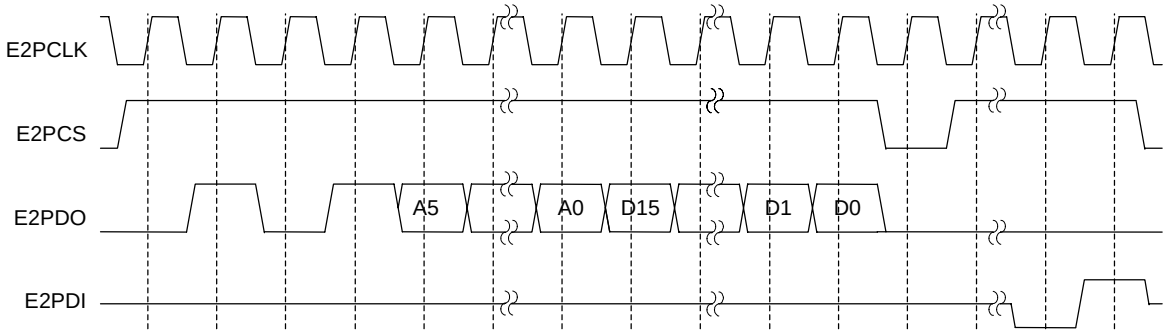
Remark The EEPROM interface of the μPD98405 is compatible with the MICROWIRE serial interface. Connection to the "NM93C46" serial EEPROM, manufactured by National Semiconductor, is recommended.

Figure 4-28. EEPROM Interface Timing

Read timing



Write timing



(2) Accessing EEPROM

The EEPROM is accessed via two direct address registers of the μPD98405: ECCR and ERDR.

ECCR register (Address = 0CH)

31 – 16	15 – 9	8 – 6	5 – 0
DATA	0	COMMAND	ADDRESS

DATA: 2-byte data to be written into the EEPROM is set.

COMMAND: An EEPROM command is set.

ADDRESS: An EEPROM address is set.

ERDR register (Address = 0DH)

31	30 – 16	15 – 0
B	0	READ DATA

B: Busy bit

0 = The data in the READ DATA field is valid.

1 = A READ command is being executed such that the data in the READ DATA field is still invalid.

READ DATA: Data read from the EEPROM

Table 4-8. EEPROM Commands

Bit 8	Bit 7	Bit 6	Bits 5-0	Command name	Description
1	1	0	A5-A0 (addressing)	READ	Reads data at the specified address in the EEPROM and stores it into the low-order 16 bits of the ERDR register.
1	0	1	A5-A0 (addressing)	WRITE	Writes the data set in the DATA field into the EEPROM.
1	1	1	A5-A0 (addressing)	ERASE	Erases addressed EEPROM data.
1	0	0	11xxxx	EWEN	Erase/Write Enable Enables write and erase operations for the EEPROM.
1	0	0	10xxxx	ERAL	Erases all EEPROM areas.
1	0	0	01xxxx	WRAL	Writes data set in the DATA field into all EEPROM areas.
1	0	0	00xxxx	EWDS	Erase/Write Disable Disables write and erase operations for the EEPROM.

To access the EEPROM, the host system writes a command into the ECCR register of the μPD98405. When the μPD98405 accepts the command, it executes the command via the EEPROM interface. During the 1-word write transaction in which the command is set, the μPD98405 activates TRDY_B and releases the bus for another master regardless of whether execution of the command is complete. If the host system starts a transaction to write another command into the ECCR register when the μPD98405 has not yet completed the processing for the command accepted by the μPD98405, the μPD98405 activates STOP_B and requests a retry.

To read EEPROM data, the host system sets an address and READ command in the ECCR register. When the μPD98405 accepts the command, it starts reading the data via the EEPROM interface. While the μPD98405 is reading data, the B bit of the ERDR register is set to 1. Once the μPD98405 finishes reading the data, it sets the B bit to 0 and stores the data in the READ DATA field. After issuing the command, the host system checks that the B bit of the ERDR register is set to 0, then obtains the data.

To write data into or erase data from the EEPROM, the host system must enable write and erase operations using the EWEN command in advance.

When no EEPROM is connected, accessing these registers is meaningless.

(3) EEPROM format

The Subsystem vendor ID, Subsystem ID, MIN_GNT, and MAX_LAT fields of the configuration register are stored into the EEPROM. After a hardware reset, the μPD98405 checks whether an EEPROM is connected. These fields are not automatically loaded if no EEPROM is connected, while they are automatically loaded when an EEPROM is connected.

The contents of the EEPROM are shown below.

Table 4-9. EEPROM Format

Address [Hex]	Contents
00	a5a5 [Hex] The μPD98405 requires this code to check whether an EEPROM is connected.
01	Subsystem Vendor ID
02	Subsystem ID
03	MAX LAT (high-order 8 bits), MIN GNT (low-order 8 bits)
04-3F	Not used. Applications can use this area in any way.

★ **Remark** The μPD98405 checks to see whether an EEPROM is connected after power is turned on (after reset). This takes about 600 clock cycles (CLK input). When the EEPROM is connected, about 2400 clock cycles (CLK input) are required from power application to completion of automatic loading. If an access is received from the host during this time (including the configuration cycle), the μPD98405 requests a retry.

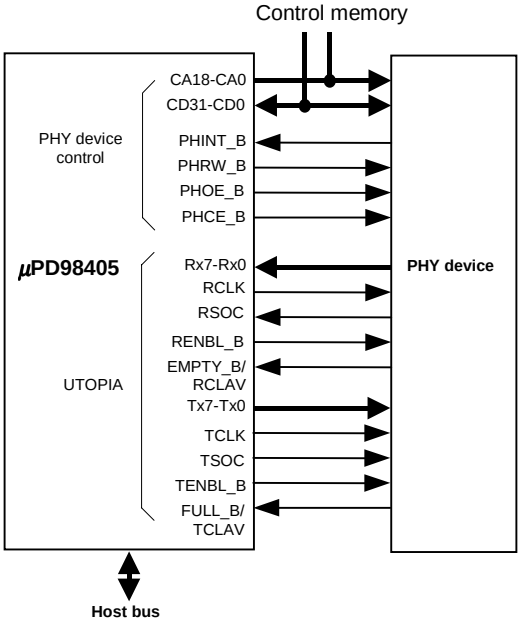
4.3 PHY LAYER DEVICE INTERFACES

The PHY layer device interfaces interface between the μPD98405 and an external PHY layer device. The μPD98405 can use an external PHY layer device instead of the internal PHY layer. These modes are selected using the PHM bit of the GMR register. When the PHM bit is set to 1, an external PHY layer device is used. When the internal PHY layer is used, leave the PHY layer device interface pins open.

To interface a PHY device, a UTOPIA interface that transfers cell data, and a PHY device control interface that controls the PHY device, or obtains its status, are provided.

This interface can be connected with a +5 V or +3.3 V device.

Figure 4-29. PHY Layer Interface for Data and Control



4.3.1 UTOPIA Interface

The μPD98405 adopts the UTOPIA interface, recommended by the ATM Forum, as the interface for transferring cell data to and from a PHY device. The μPD98405 supports two UTOPIA interface modes: octet-level and cell-level. These modes are selected using the UOC bit of the GMR register.

Selects UTOPIA interface mode.		
UOC bit (GMR: bit 26)	0	Octet-level handshaking mode
	1	Cell-level handshaking mode
	Default = 0	

The μPD98405 does not support multi PHY (UTOPIA Level 2). Therefore, do not place any signals in the high impedance state.

The UTOPIA interface consists of a clock signal bus for each of transmission and reception supplied by the μPD98405, an 8-bit data signal bus, and three control signal buses.

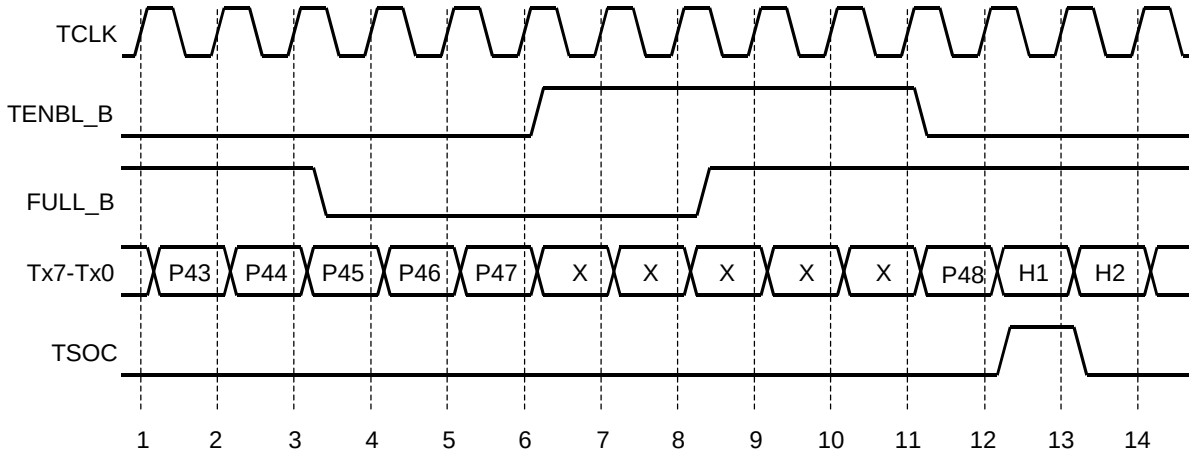
- **TCLK (output)**: Transmit clock. The SAR system clock, input to the SCLK pin, is output as is.
- **TENBL_B (output)**: Transmit enable signal. The TENBL_B signal notifies the PHY device that Tx7 through Tx0 carry transmit data in the current clock cycle.
- **FULL_B/TCLAV (input)**: The function of this pin differs between the octet-level and cell-level handshaking modes. In octet-level handshaking mode, this pin functions as the FULL_B pin to notify the μPD98405 that the PHY device can receive no more data because the buffer is full. In cell-level handshaking mode, this pin functions as the TCLAV pin to notify the μPD98405 whether the next cell can be received.
- **Tx7-Tx0 (output)**: Transmit data bus
- **TSOC (output)**: Transmit cell start signal. The TSOC signal is output in synchronization with the first byte of the transmit cell data.
- **RCLK (output)**: Receive clock. The SAR system clock, input to the SCLK pin, is output as is.
- **RENBL_B (output)**: Receive enable signal. The RENBL_B signal notifies the PHY device that the μPD98405 is ready to accept data in the next clock cycle.
- **EMPTY_B/RCLAV (input)**: The function of this pin differs between the octet-level and cell-level handshaking modes. In octet-level handshaking mode, this pin functions as the EMPTY_B pin and is used by the PHY device to notify the μPD98405 that the data on Rx7 through Rx0 is invalid because there is no receive data to be provided. In cell-level handshaking mode, this pin functions as the RCLAV pin to indicate whether subsequent cell data exists.
- **Rx7-Rx0 (input)**: Receive data bus
- **RSOC (input)**: Receive cell start signal. The RSOC signal is input in synchronization with the first byte of the cell data received from the PHY device.

(1) Transmit interface

(a) Octet-level handshaking mode

The μPD98405 outputs the SAR system clock input to the SCLK pin, from the TCLK pin, to synchronize cell data exchanged between the μPD98405 and a PHY device. The cell data in the transmit FIFO is transmitted onto 8 bits of data lines Tx7 through Tx0, at the rising edge of TCLK. While valid data is being transmitted onto Tx7 through Tx0, the enable signal, TENBL_B, is driven low. The TSOC signal is driven high in synchronization with the first byte of the cell header. The PHY device reads data from Tx7 through Tx0 if it detects the low level of the TENBL_B signal, and determines the cell start position by using the TSOC signal. Once the internal FIFO of the PHY device is full, the device drives the FULL_B signal low to inform the μPD98405 that the device can no longer receive transmit data. The μPD98405 samples the FULL_B signal at the rising edge of the TCLK clock. When the μPD98405 detects the low level of the FULL_B signal, it drives the TENBL_B signal high at the rising edge 2 clocks after the edge at which the low level of the FULL_B signal was detected, and stops transmitting valid cell data. Once the FULL_B signal becomes inactive high, the μPD98405 drives TENBL_B signal low at the rising edge 2 clocks after the edge at which the high level of the FULL_B signal was detected, and resumes transmitting cell data.

Figure 4-30. Transmit Timing in Octet-Level Handshaking Mode



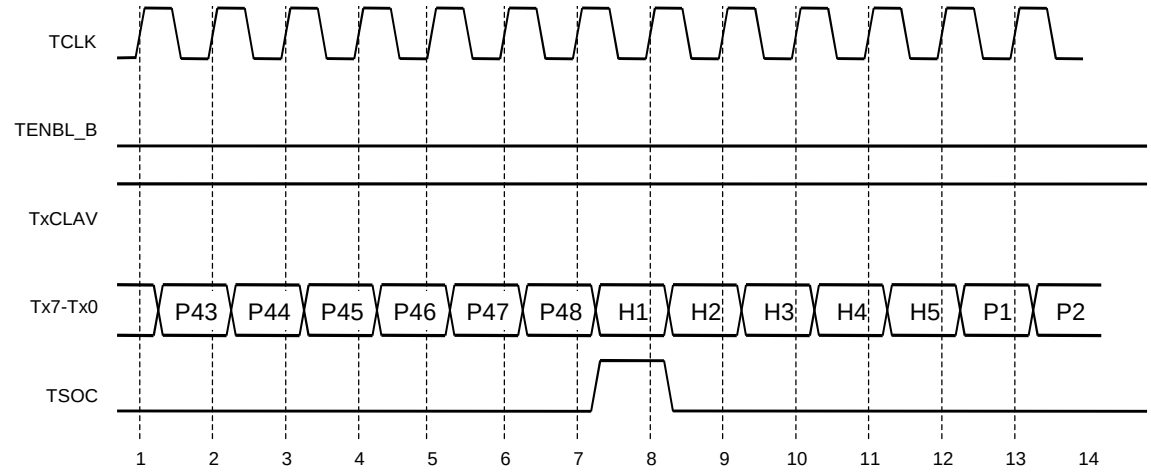
Remark H: ATM cell header P: ATM cell payload X: Invalid

(b) Cell-level handshaking mode

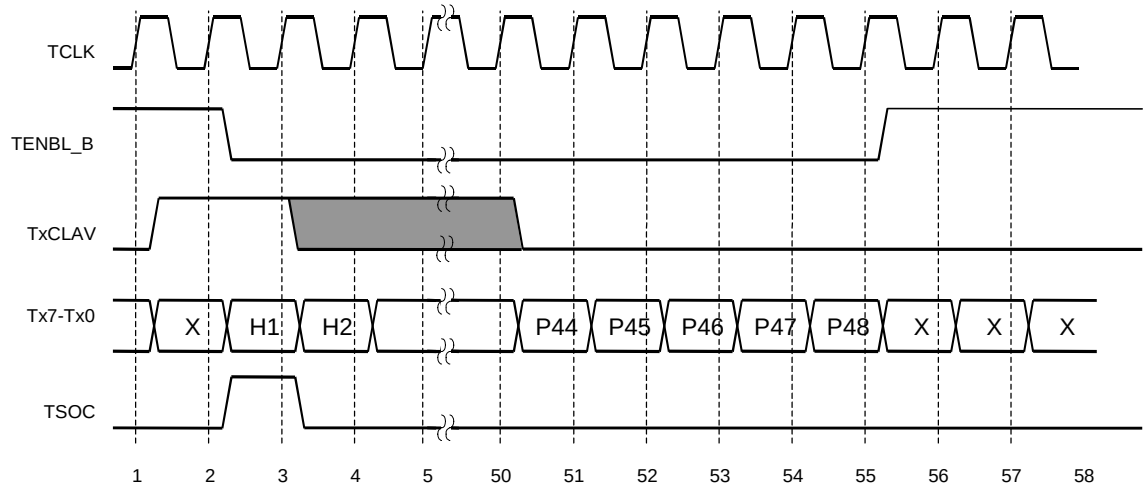
In cell-level handshaking mode, the signal timing is the same as that in octet-level handshaking mode, except that the FULL_B signal changes to the TCLAV signal. When the transmit buffer has space to receive the next cell, the PHY device drives the TCLAV signal high upon completion of the current cell transfer. When the buffer has no space to receive the next cell, the PHY device drives the TCLAV signal low in the cycle at least four clocks before the completion of the current cell transfer.

Figure 4-31. Transmit Timing in Cell-Level Handshaking Mode

(Example 1)



(Example 2)



★ **Caution Do not de-assert TCLAV during H1 (see Figure 4-31 (Example 2)).**

Remark H: ATM cell header P: ATM cell payload X: Invalid

(2) Receive interface

(a) Octet-level handshaking mode

The μPD98405 supplies the SAR system clock input to the SCLK pin, from the RCLK pin, to the PHY device as the receive cell data synchronization clock. The PHY device must output receive cell data to data lines Rx7 through Rx0 in synchronization with this RCLK clock, supplied from the μPD98405.

The μPD98405 latches the data at the rising edge of RCLK, and informs the PHY device, by using the RENBL_B signal, whether it can receive the cell data. If the internal receive FIFO of the μPD98405, which can store up to 96 cells, has become full such that the μPD98405 can no longer receive data, it drives the RENBL_B signal high in the cycle one clock before. When the PHY device detects that RENBL_B is high, it must stop transmitting receive cell data. Once the FIFO of the μPD98405 is empty, the RENBL_B signal is driven low again in the cycle one clock before.

The operation of the RENBL_B signal of the μPD98405 differs depending on whether DROP mode or No DROP mode is selected. These modes are selected using the DR bit of the GMR register.

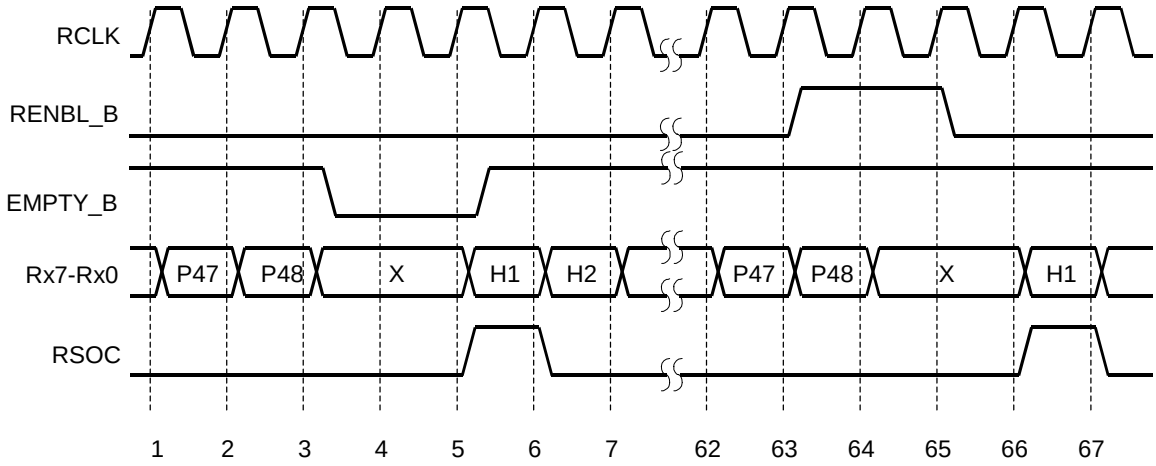
DROP mode/No DROP mode (GMR register: DR bit)	
DROP mode (DR bit = 0)	The μPD98405 keeps the RENBL_B signal active low even when its receive FIFO is full, and does not request PHY device to stop transmitting receive cell data. Therefore, a receive FIFO overrun may occur, the receive cell data responsible for the overrun being discarded.
No DROP mode (DR bit = 1)	The μPD98405 drives the RENBL_B signal high one clock before if its receive FIFO is full, such that the μPD98405 can no longer receive cell data. The PHY device must stop transmitting receive cell data once it detects that the RENBL_B signal has gone high. Once the receive FIFO is empty, the μPD98405 drives the RENBL_B signal low again. A receive FIFO overrun does not occur in No DROP mode.

★

The PHY device drives the EMPTY_B signal low and stops outputting valid receive data when its receive FIFO no longer contains any valid cell data to be output. The μPD98405 samples the EMPTY_B signal at the rising edge of the RCLK clock. When it detects that the EMPTY_B signal is low, it does not latch data at the rising edge of the clock. The PHY device must input a high level to the RSOC pin in synchronization with the first byte (first byte of the header) of the receive cell header. The μPD98405 samples the RSOC signal at the rising edge of the RCLK signal. When it detects that the RSOC signal is high, it starts counting the effective data bytes, starting from that data which is input at the same rising edge. Once 53 bytes have been counted, the μPD98405 assumes that the reception of one cell has been completed, so performs processing for the received cell.

Caution Do not specify high impedance as the input level for the Rx7 through Rx0 pins of the UTOPIA reception interface of the μPD98405.

Figure 4-32. Receive Timing in Octet-Level Handshaking Mode

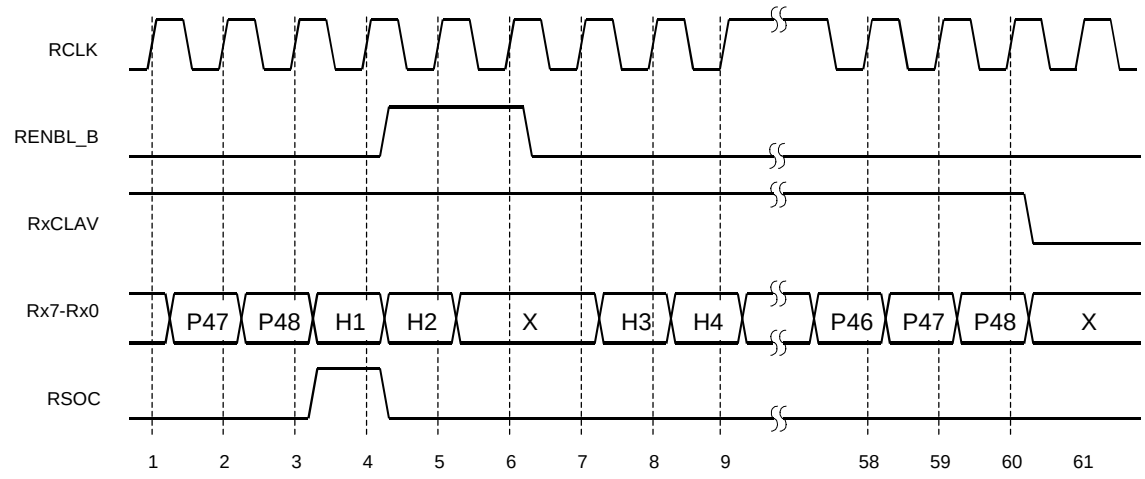


Remark H: ATM cell header P: ATM cell payload X: Invalid

(b) Cell-level handshaking mode

The signal timing in cell-level handshaking mode is the same as that in octet-level handshaking mode, except that the EMPTY_B signal is replaced by the RCLAV signal. The RCLAV signal is used by the PHY device to indicate whether there is subsequent cell data to be transmitted. When there is no more cell data, the PHY device drives the RCLAV signal low in the next cycle of the last octet of the cell data currently being transferred. The μPD98405 does not load the data on Rx7 through Rx0 in a cycle in which the RCLAV signal is low. The input timing of the RCLAV signal is the same as that for the EMPTY_B signal in octet-level handshaking mode.

Figure 4-33. Receive Timing in Cell-Level Handshaking Mode

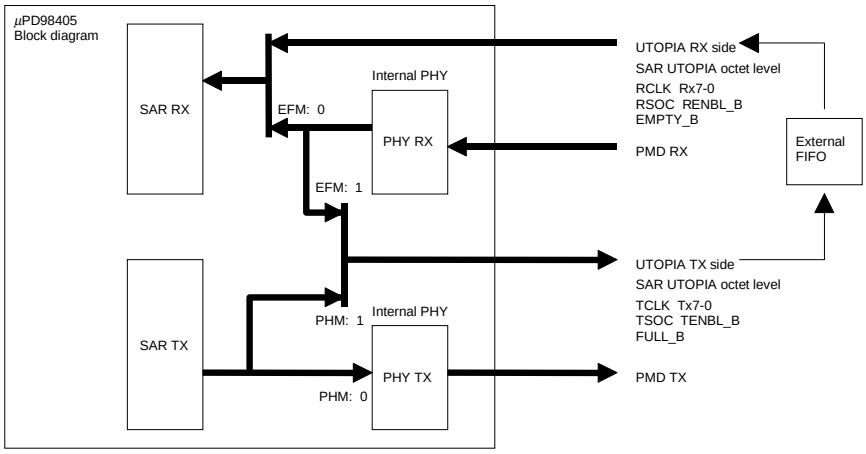


Remark H: ATM cell header P: ATM cell payload X: Invalid

(3) External receive FIFO use mode

Even when using an internal PHY layer, an external receive FIFO can be connected to the μPD98405 via a UTOPIA interface. When the PHM bit of the GMR register is 0 (the internal PHY layer is used) and the EFM bit is 1, the μPD98405 transmits the data, received at the internal PHY layer, from the transmission side of the UTOPIA interface in sync with the internal TCLK. In this case, the UTOPIA interface operates in an octet level handshake manner; the transmission side transmits the PHY layer data and the reception side receives the SAR layer data. The UTOPIA interface operates according to the SAR layer UTOPIA signal and timing. See **Section 4.3.1** for details of the UTOPIA interface signal timings. The block diagram of an external receive FIFO connection is shown below.

Figure 4-34. External FIFO Connection Block Diagram



Remark When using the built-in framer function and external clock recovery (when, in the GMR register, PHM is set to 0 or PLL is set to 1), the external receive FIFO cannot be used.

4.3.2 PHY Layer Device Control Interface

The μPD98405 has an interface that controls the reading and writing of the registers of an external PHY device. When this interface is used, an interface circuit between the host and PHY device is not necessary.

The control interface of the PHY device is a simple memory type slave interface. Its address lines and data lines are multiplexed with the control memory interface. The control memory interface of the μPD98405 has 32 data lines (CD31 through CD0) and 19 address lines (CA18 through CA0). The PHY device can be connected to all or some of these 32 data lines and 19 address lines.

When the host accesses the PHY device, it uses one of the μPD98405's commands, Indirect_Access. If the Indirect_Access command is issued to the PHY device, the μPD98405 starts a PHY control cycle, and manipulates the following control signals.

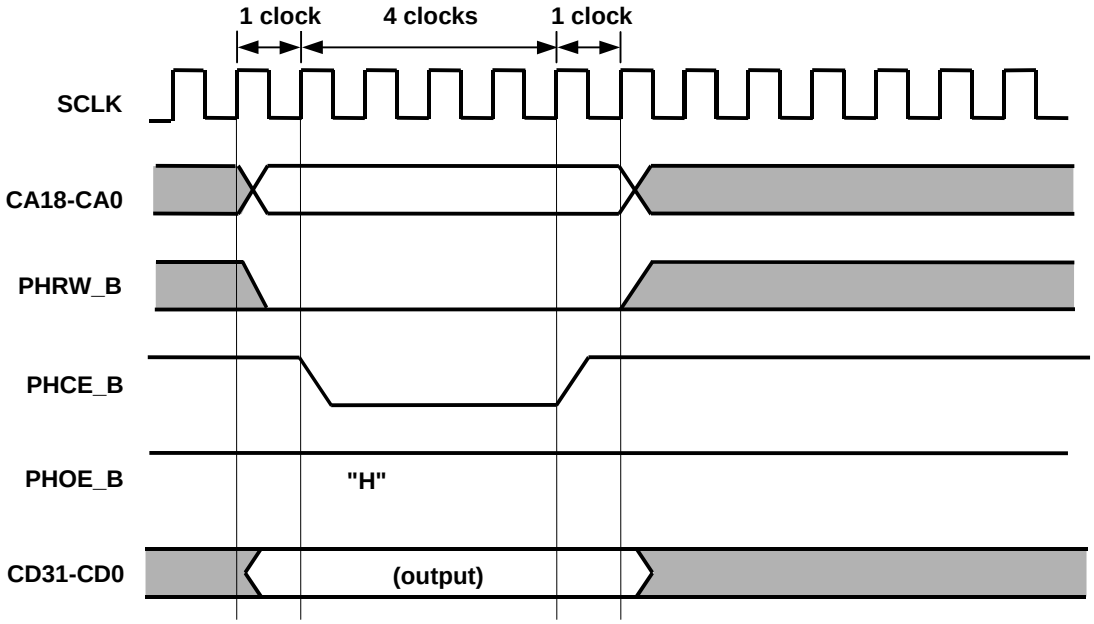
For details of the Indirect_Access command, see **Section 5.10**.

- **PHCE_B (output)**: Chip enable signal to the PHY device. This pin goes low when the host issues the Indirect_Access command to the PHY device via the μPD98405.
- **PHRW_B (output)**: Indicates whether the PHY device is accessed for read or write. This signal goes high when the device is accessed for read, and goes low when the device is accessed for write.
- **PHOE_B (output)**: Output enable signal to make the output lines of the PHY device active.
- **PHINT_B (input)**: Inputs an interrupt request signal from the PHY device. When a low level is input to the PHINT_B pin, the μPD98405 sets the PHY interrupt (PI) bit of the GSR register to issue an interrupt to the host.
- **PHRST_B (output)**: PHY device reset signal. When the RST_B signal is asserted, the μPD98405 asserts PHRST_B and keeps PHRST_B low for at least 17 clocks after RST_B is deasserted. When a software reset (write access to the SWR register) is performed, the μPD98405 asserts PHRST_B and keeps PHRST_B low for at least 17 clocks.

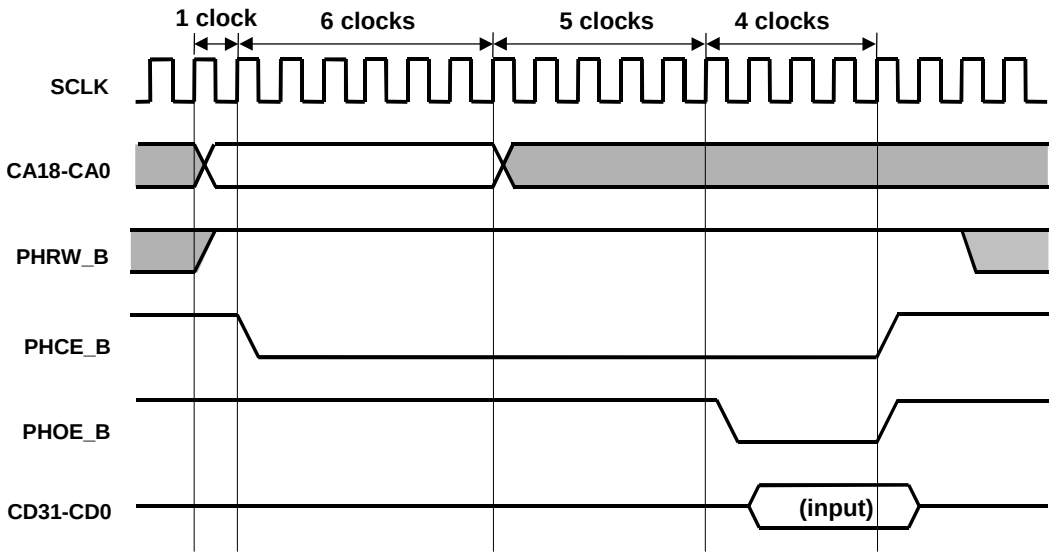
Remark The PHINT_B signal, used to input an interrupt request signal from the PHY device, can also be used as a Generic port for which the level is detected via the μPD98405.

Figure 4-35. PHY Device Control Signal Timing

(a) Write operation



(b) Read operation



4.4 CONTROL MEMORY INTERFACE

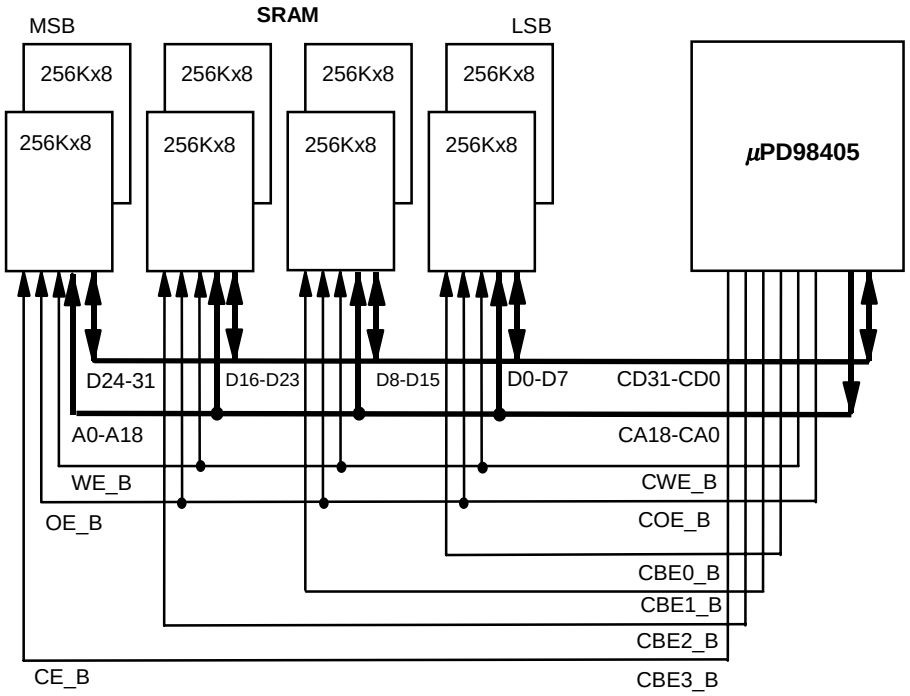
External control memory (CM) is essential for the μPD98405 to perform transmission or reception. The control memory interface accesses the control memory, and can be also used as a port to control the PHY device. This interface can be connected with +5 V or +3.3 V SRAM. The control memory interface has the following signal lines.

- CD31 through CD0: 32 data I/O signals. These pins are connected to internal pull-down resistors.
- CA18 through CA0: 19 address signals
- CBE3_B through CBE0_B: 4 byte enable signals
- COE_B: Output enable signal
- CWE_B: Write enable signal
- CPAR3 through CPAR0: Parity bit I/O signals. These pins are connected to internal pull-down resistors.

The μPD98405 writes or reads the control memory by controlling these signals. The size of the memory connected as control memory depends on the number of channels simultaneously supported by the μPD98405, up to a maximum of 512K words (1 word = 32 bits) or 2M bytes. (For details about how the capacity is determined, see **Section 5.2**.)

Figure 4-36 shows an example of connecting the control memory.

Figure 4-36. Control Memory Interface Using Standard SRAMs



Basically, the control memory is managed by the μPD98405. The μPD98405 toggles the COE_B signal at fixed intervals (low level for 20 clocks in SAR system clock (SCLK pin input clock) cycle, then high level for 16 clocks) even when it is not transmitting or receiving data. The μPD98405 makes CBE_B active while COE_B is low, successively executing read operations, and makes CWE_B and CBE_B active while COE_B is high, successively executing write operations.

The μPD98405 also changes the number of bytes accessed by the control memory as necessary. The control memory may perform access one word (32 bits) at a time, of the low-order and high-order half words, or in 1-byte units. The type of access used is selected by the μPD98405, by controlling the CBE_B signal. The memory to be connected, therefore, must support being enabled or disabled in 1-byte units.

The control memory interface supports functions for appending and checking a parity bit. The parity bit is input or output via CPAR3 through CPAR0. These parity bit lines indicate the parity of CD31 through CD0 in 8-bit units, and calculate an even parity. During a read operation, the parity bit input from CPAR3 through CPAR0 is checked. Whether the function for checking the input parity bit is enabled or disabled is selected by the CPE bit (bit 15) of the GMR register.

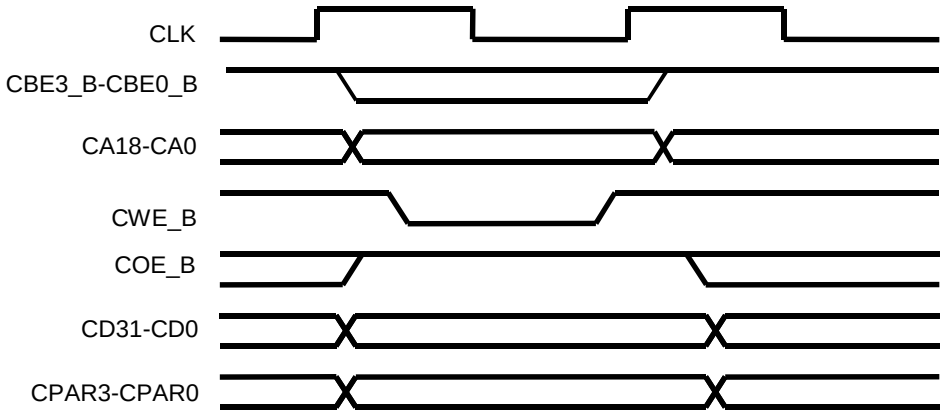
Selects the control memory parity check function (GMR register: bit 15).		
CPE bit	0	Disables the control memory parity check function. The μPD98405 does not detect errors in the parity bit input from CPAR3 through CPAR0.
	1	Enables the control memory parity check function. The μPD98405 detects errors in the parity bit input from CPAR3 through CPAR0. If it detects an error, the μPD98405 sets the CPE bit of the GSR register to 1, and informs the host by using an interrupt (provided interrupts are not masked).
	Default = 0	

During a write operation, parity calculation bits in 8-bit units are output from CPAR3 through CPAR0. The parity bit is always output regardless of the setting of the CPE bit of the GMR register. Because pins CPAR3 through CPAR0 are connected to internal pull-down resistors, they are not set to high impedance state while not being used.

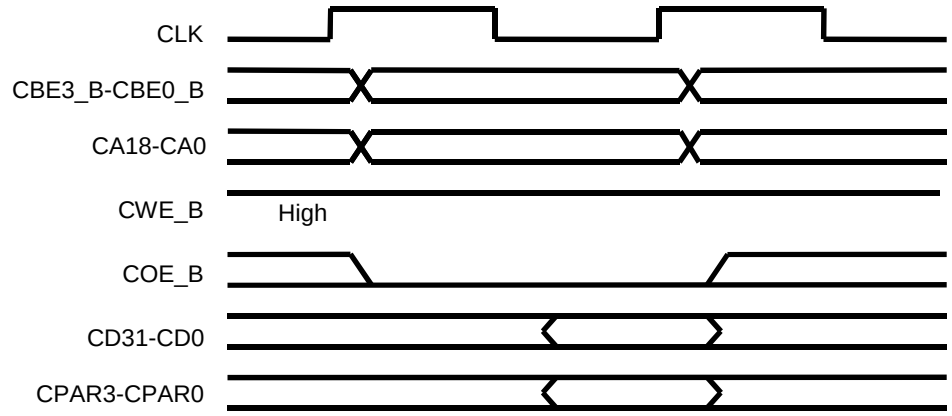
Caution If a parity error is detected on the control memory interface, the operation of the μPD98405 cannot be guaranteed. Whenever a parity error is detected, therefore, reset the μPD98405.

Figure 4-37. Control Memory Access Timing

(a) Write



(b) Read



4.5 PMD INTERFACE

A PMD interface is used to connect an optical transceiver/receiver module. The PMD interface of the μPD98405 is a serial interface that uses the internal or external clock recovery/synthesizer.

Including those situations where an external PHY device is being used, the μPD98405 supports a total of four modes, as listed below. These modes are selected by setting the PHM, PLL, and EFM bits of the GMR register.

Mode	PHM	PLL	EFM
Built-in framer, clock recovery mode	0	0	0
Built-in framer, clock recovery, external FIFO mode	0	0	1
Built-in framer, external clock recovery mode	0	1	don't care
External PHY mode	1	don't care	don't care

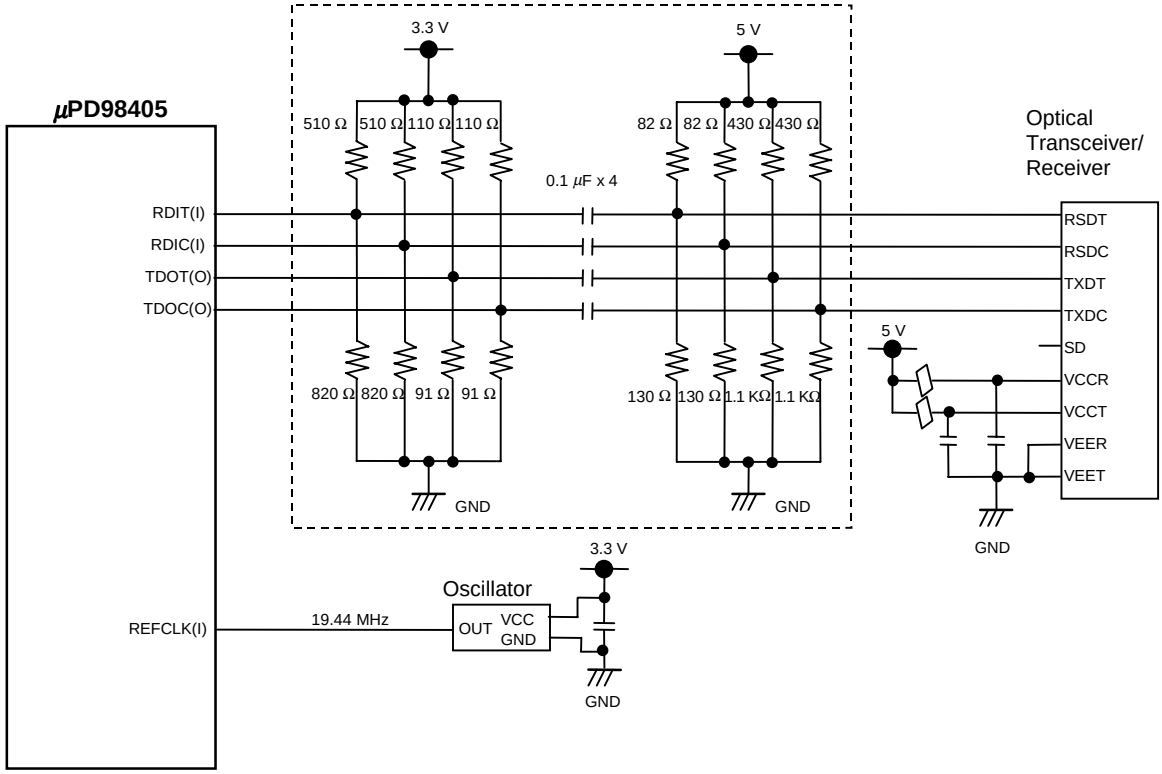
For details of the "external PHY mode", and "built-in framer, clock recovery, and external FIFO mode", see **Section 4.3.1**.

★ **Caution The "built-in framer, external clock recovery" mode cannot be used. Please use one of the other modes.**

(1) Built-in framer, clock recovery mode

An example of PMD interface connection is shown in Figure 4-38. In this mode, the transmit/receive clock input TFKT/TFKC and RCIT/RCIC pins are not used.

Figure 4-38. Example of Connecting the PMD Interface (Connecting 5 V Optical Module)



★ Input a standard clock signal from a clock synthesizer or clock recovery training clock signal to the REFCLK pin.

Pin	Use	Connection value
REFCLK	Standard clock signal from a clock synthesizer or clock recovery training clock signal	19.44 MHz

★ • **Receive clock recovery PLL function**

The clock recovery PLL extracts the receive clock from the receive data strings input to the RDIT/RDIC pin. The μPD98405 contains an OOL (Out of Link) detection circuit. This circuit monitors whether the receive clock recovery PLL has successfully been locked to the receive data string to extract an expected clock. The circuit compares an eight-divided clock, generated by the PLL, with the clock frequency input to the REFCLK pin. When the difference is more than 244 ppm, the circuit assumes that the receive clock recovery PLL has failed to lock successfully and enters the OOL status. When the difference is less than 244 ppm, the OOL status is released. The OOL status is applied to a bit of the PICR register and can cause an interrupt.

To prevent the receiver circuit from operating with an unstable clock in the OOL status, the receive clock that is used by the receiver circuit as a source clock can be automatically changed to the clock generated by the transmit synthesizer. When the OOL status is cleared, the recovery clock is used as the receive clock again. This function is enabled by default. It can be disabled by setting the oolenb bit of the mode

register 2 (MDR2) to 1.

Immediately after power application, the receive clock recovery PLL starts extracting the clock, but it enters the OOL status because data synchronization cannot be established immediately. When a correct data string is input to RDIT/RDIC, it takes the OOL detection circuit about 0.6 s to judge whether the frequency difference between the recovered clock and REFCLK clock is within 244 ppm. The OOL status is cleared, therefore, after 0.6 s, and the recovery clock is supplied to the receiver circuit.

If the oolenb bit is disabled, however, and if receive data is correctly input in the OOL status, the receive clock recovery PLL is synchronized within 1 ms.

Caution If a circuit signal loss (LOS) error occurs, the receive PLL enters the free-run status. Consequently, the frequency shifts from that of REFCLK, resulting in the OOL status. If the oolenb bit of the mode register 2 (MDR2) is 0 at this time, the clock generated by the transmit synthesizer PLL is automatically switched to the receive clock. If this happens, the OOL detection circuit compares the clock of the transmit synthesizer PLL with REFCLK. As a result, the OOL status is cleared and the recovery clock is switched to the receive clock again.

While LOS is detected, the OOL status takes place and is cleared repeatedly. If interrupt servicing mode 2 is selected, note that the OOL bit of the interrupt cause register (PICR) is repeatedly set and reset in accordance with this operation. It is recommended to mask the interrupt caused by the OOL status in this mode.

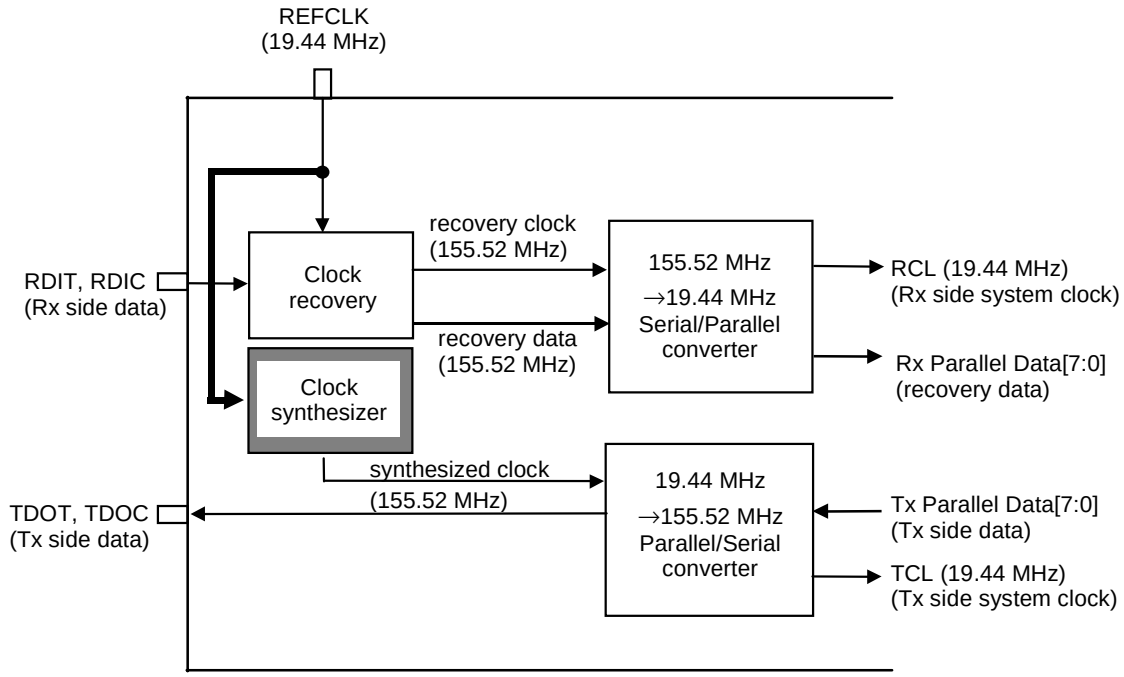
The receive clock can be forcibly switched to the clock generated by the transmit synthesizer PLL for testing by setting the RxCL bit of the mode register 2 (MDR2), as follows:

Setting of RxCL Bit	Receive Clock
1	Clock generated by transmit synthesizer PLL
0	Clock extracted by receive clock recovery PLL

- **Transmit PLL function**

The transmit clock is a 155.52 MHz clock signal generated by the internal synthesizer based on the 19.44 MHz REFCLK pin input.

Figure 4-39. Synthesizer Reference Clock



CHAPTER 5 SAR FUNCTION

This chapter explains the SAR functions of the μPD98405.

5.1 INITIALIZATION

(1) Initializing the chip

Before the μPD98405 can function normally, it must be initialized to set the internal states and registers to their defaults. A hardware reset is executed by inputting a low level signal to the RST_B pin. During normal operation, the chip can be also initialized by means of a software reset. A software reset is executed by writing to the SWR register.

The hardware and software resets have the same effect on the μPD98405 except the following, such that the same status is established after either is effected.

★ • The PCI configuration register, and ECCR and ERDR registers are not initialized after a software reset, and the EEPROM connection check is not carried out.

Caution The μPD98405 requires 20 clock cycles (SCLK input) to initialize its internal circuitry. Do not attempt to access the μPD98405 as a slave (including the PCI configuration access) until 20 clock cycles have elapsed after a hardware or software reset.

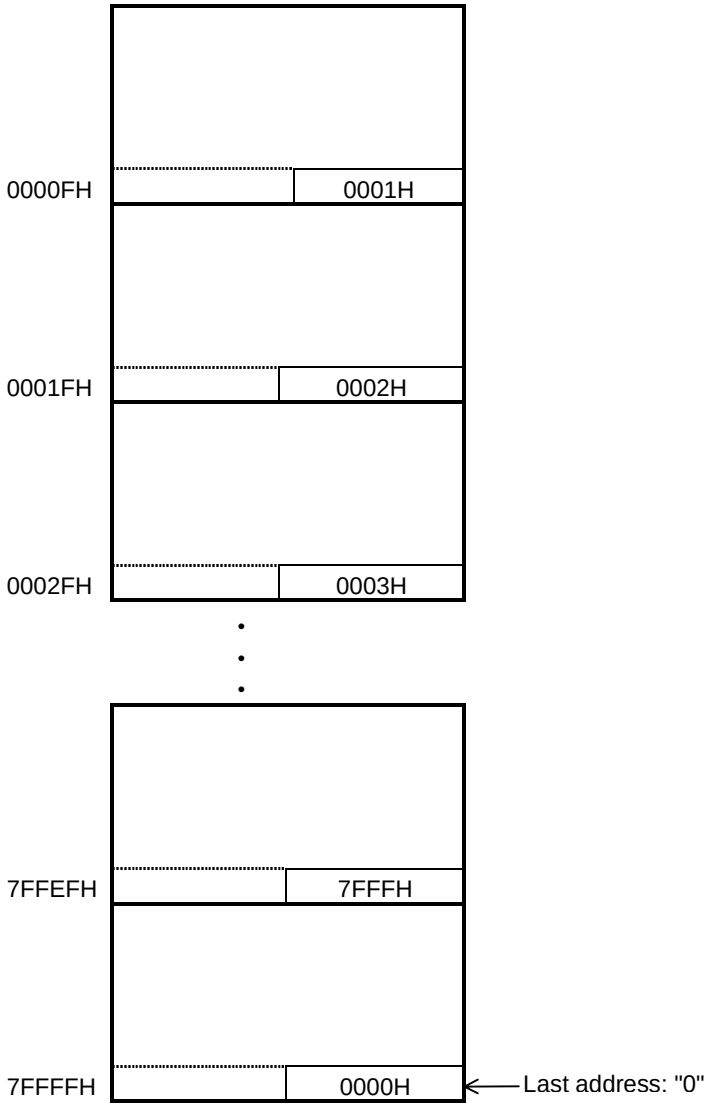
(2) Initializing the control memory

After a hardware or software reset, the μPD98405 initializes the connected control memory. The μPD98405 operates assuming that the maximum of 512K words (2M bytes) of control memory have been allocated.

When a reset is effected, the μPD98405 writes "0000H" to the low-order 16 bits of the last word address ("7FFFFH") as a block number, then decrements the addresses in 16-word units to 7FFEF, 7FFDF, 7FFCF, and so on, writing block numbers to the low-order 16 bits of each address 32K times each time, decrementing the block number to 7FFF, 7FFE, 7FFD, and so on. After block number "0001H" has been written to address "0000FH," the μPD98405 writes "0000H" to address "7FFFFH" again, at which point initialization is complete. Areas other than the block number area are not cleared to 0.

The written block number functions as a pointer to the first address of the next block. Those blocks for which all the areas are divided by 16 words are chained. This chain information is used by the μPD98405 to manage the "free block pool" of the control memory and is rewritten as necessary to open/close the VC and transmit/receive data.

Figure 5-1. Control Memory after Initialization



This automatic initialization processing can be disabled whenever a test is conducted. To disable initialization, input "1" (high level) to external pin INITD. During normal operation, input "0" (low level) to the INITD pin.

INITD pin input	0	The μPD98405 initializes the control memory after a reset.
	1	The μPD98405 does not initialize the control memory after a reset.

When the input to the INITD pin is 0, the μPD98405 immediately starts writing block numbers into control memory after a reset. Because one block number can be written per clock cycle, 32K clock cycles are required to write all block numbers. At this time, the host cannot use the control memory interface because it is being used by the μPD98405. Within the 32K clock cycles, therefore, the host can perform only slave access to direct access registers, other than CMR/CMR_L and CER/CER_L. Within this period, do not issue a command which uses CMR.

After the control memory has been initialized, the μPD98405 sets the IND bit of the GSR register to 1, and generates an interrupt provided it is not masked.

If the INITD pin is high, the IND bit is also set to 1 immediately after a reset.

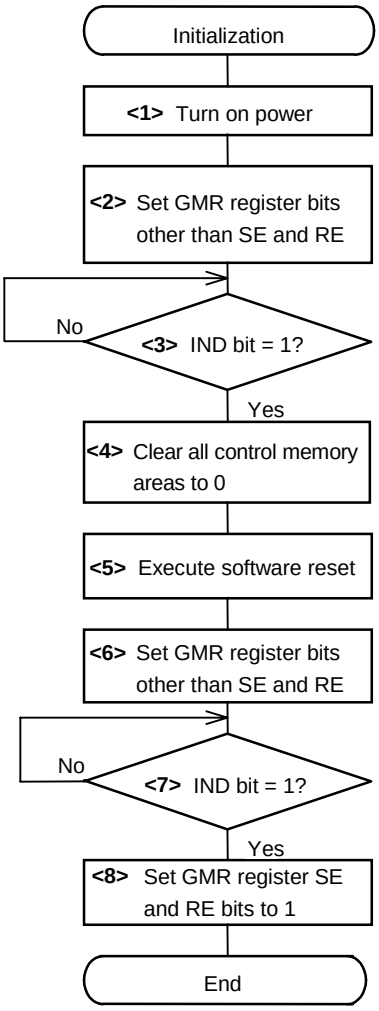
<Notes on initializing control memory>

As described above, the μPD98405 does not clear the contents of control memory to 0. Some areas of control memory cannot operate normally, however, unless their initial values are "0" when control memory is read while the μPD98405 is transmitting/receiving data. Therefore, always clear the contents of control memory to 0 with software after applying the power.

<Example of initialization sequence>

Figure 5-2 shows an example of chip initialization.

Figure 5-2. Initialization Sequence Flowchart



<1> Turning on the power causes a hardware reset to be executed, after which the μPD98405 starts writing block numbers to control memory.

<2> The host sets the parity mode in the GMR register, and writes 0 to the SE and RE bits. The parity output function of the μPD98405 is always enabled. If a slave register is read before the parity mode is set after power-on, the μPD98405 outputs the parity bits in default mode, such that the host system will detect a parity error. To prevent this, the parity bits of the GMR register must be set first. The SE and RE bits are not set above, because the scheduler register parameters must be cleared to 0 before the SE bit is set to 1.

<3> Wait until the IND bit of the GSR register is set to 1. Polling or an interrupt can be used to detect that the IND bit has been set to 1. To use an interrupt for detection, that interrupt must be unmasked beforehand using the interrupt mask register (IMR).

<4> Once the IND bit has been set to 1, the Indirect_Access command is enabled. The host uses this command to write 0 to all control memory areas.

<5> Execute a software reset. The μPD98405 overwrites the control memory with block numbers, after it has been cleared to 0.

<6> Set the parity mode in the GMR register again. Do not set the SE and RE bits yet.

<7> Check that the IND bit is set to 1, and that block number write has been completed.

<8> Set the SE and RE bits of the GMR register to 1.

5.2 SETTING THE CONTROL MEMORY

The size of the control memory is set to between 0 and 512K words (1 word = 32 bits) depending on the number of channels supported by the μPD98405. The control memory is divided into the four areas described below ("1 block" in the following description corresponds to 16 words).

(1) Receive lookup table:

This area stores the "enable bit" and "VC NUMBER" according to the pattern of the receive VPI/VCI. This area can consist of up to 2,048 blocks, the actual value depending on the supported receive VPI/VCI. For details, see **Section 5.5.4**.

(2) Receive free buffer pool pointer:

This area saves "pool descriptors." The size of this area differs depending on the number of pools set. Because up to 32 two-word descriptors can be set, a maximum of four blocks are occupied. For details, see **Section 5.5.2 (2)**.

(3) ABR lookup table:

This area is used by the μPD98405 to save the "VC NUMBER" of the channel (VC) selected by the ABR scheduler. This area can consist of up to 8 blocks, the actual value depending on the number of supported active ABR channels. The μPD98405 supports two active ABR channels per word. The host need not access this area. It is used only by the μPD98405.

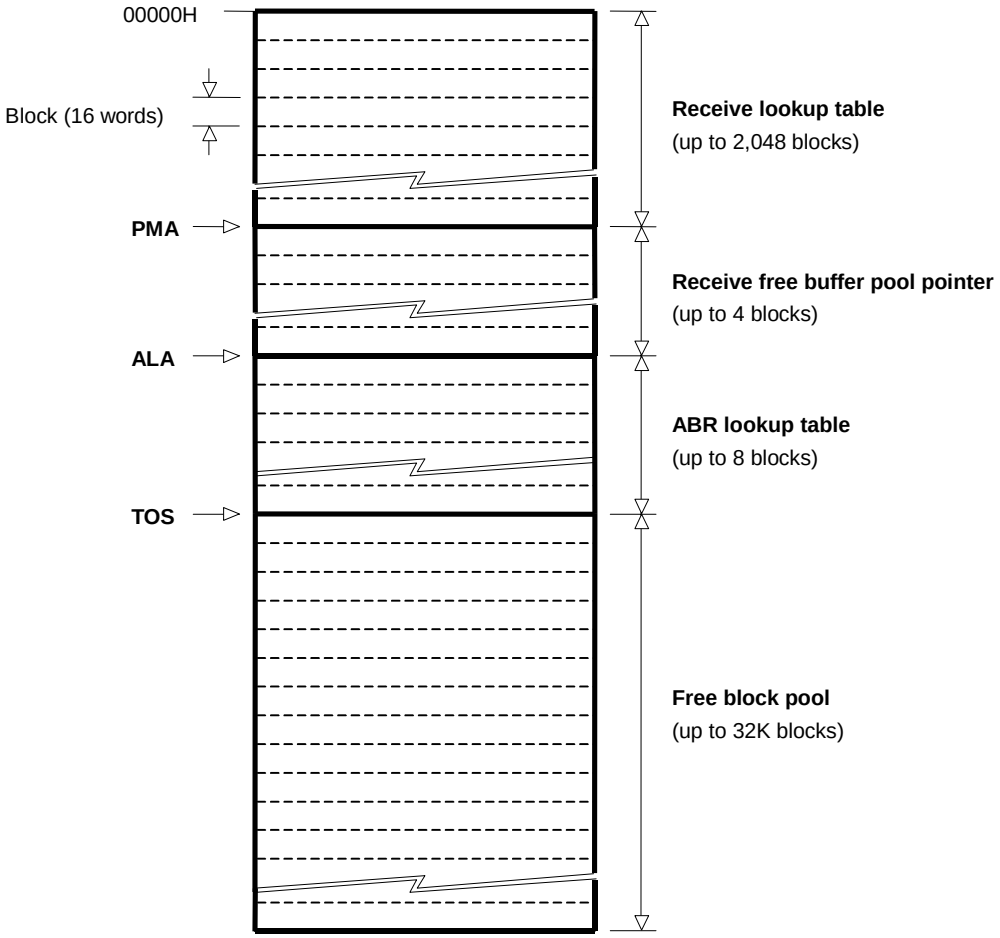
★ Set ALA = TOS when not using the ABR service. In this case, the ABR look-up table can be deleted.

(4) Free block pool:

This area saves the transmit/receive VC tables. The size of this area differs depending on the number of VC tables set, but fills within a range of 0 to 32K blocks. Because one transmit/receive VC table uses one block (16 words), 32 blocks are occupied when sixteen transmit/receive channels are set.

For details, see **Sections 5.4.3** and **5.5.3**.

Figure 5-3. Control Memory Configuration



The control memory is divided before the user starts transmission/reception. How the area is divided is determined by setting the start address of each area in the indirect address registers of the μPD98405. The start addresses are set in the following three registers.

- PMA register: Sets the start address of the receive free buffer pool descriptor area.
- ALA register: Sets the start address of the ABR lookup table.
- TOS register: Sets the start address of the free block pool.

Set these three areas by observing the following rules.

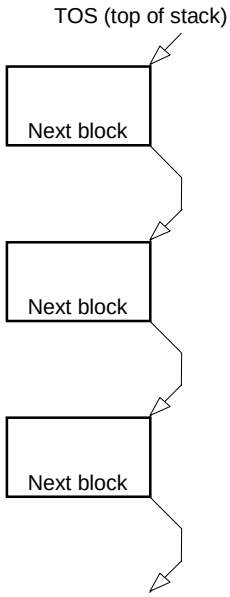
<1> The receive lookup table must always start from address 0. Its size must always be 2^n words.

<2> The receive free buffer pool must always start from an address in which the size of the pool is specified in the low-order bits (if, for example, the size of the free buffer pool is 64 words, clear the low-order six bits of the start address (PMA) to 0).

<3> The ABR lookup table must always start from an address in which the size of the table is specified in the low-order bits (if, for example, the size is 128 words, clear the low-order seven bits of the start address (ALA) to 0).

TOS (top of stack) is a register for which the user sets an initial value but which is subsequently used by the μPD98405 as a stack pointer that indicates the beginning of the free block pool, its contents being changed as necessary. The μPD98405 sequentially connects the blocks of the free block pool (see **Section 5.1 (2)**). Each time the host issues an Open_Channel command, the μPD98405 returns the address indicated by TOS from the free block pool by using command indication, then allocates one block. At this time, the μPD98405 updates the contents of the TOS register with the pointer to the next block. Each time the host issues the Close_Channel command, the μPD98405 returns a block to the free block pool and allocates it to TOS.

Figure 5-4. Free Block Pool Stack



Remark The PMA, ALA, and TOS registers, used for control memory, are frequently accessed by the μPD98405 during transmission/reception. The host can write appropriate values to these registers only as part of initialization after a reset. Do not modify the contents of these registers once transmission or reception has started. Modifying their contents during transmission or reception will result in a malfunction. Reading of the registers is, however, always possible.

<Example of determining the size of control memory>

As an example, the required size for the control memory is calculated for the following conditions:

Condition 1: Type of receive VPI/VCI supported = Up to 64K types of VPIs/VCIs are supported.

Condition 2: Number of pools to be set = Pool 0 only

Condition 3: Number of active ABR channels supported = 256

Condition 4: Number of transmit/receive channels supported = Transmit channels: 16

Receive channels: 16

(Size)

Receive lookup table = 32,768 words (Up to 65,536 types of VPIs/VCIs are supported.)

Receive free buffer pool pointer = 2 words (Each pool descriptor consists of 2 words.)

ABR lookup table = 128 words (Each word supports two active ABR channels)

Free block pool = transmit 16 x 16 + receive 16 x 16 = 512 words (Each VC table consists of 16 words.)

Total: 33,410 words

5.3 SETTING A MAILBOX

5.3.1 Setting a Mailbox

A mailbox is an area prepared by the host in system memory, that is used to store indications issued by the μPD98405. Such indications consist of the status information that the μPD98405 issues for each transmit/receive packet. For details of the contents of the transmit/receive indication, see **Section 5.6**.

The μPD98405 can support up to four mailboxes, using two each for transmission and reception. The four mailboxes are assigned numbers 0 to 3. These numbers identify whether the mailboxes are for transmission or reception (it is not always necessary to use all four of the mailboxes).

- Receive mailboxes: numbers 0 and 1
- Transmit mailboxes: numbers 2 and 3

The μPD98405 uses the mailboxes as ring buffers in system memory. These buffers are defined by the following addresses.

- Mailbox start address high (MSH): High-order 16 bits of the starting address of a mailbox
- Mailbox start address low (MSL): Low-order 16 bits of the starting address of a mailbox
- Mailbox bottom address (MBA): Low-order 16 bits of the address next to the last address of a mailbox
- Mailbox write address (MWA): Low-order 16 bits of the write pointer managed by the μPD98405
- Mailbox tail address (MTA): Low-order 16 bits of the address that is updated to the location read by the host

All mailbox pointers consist of 16 bits. The μPD98405 creates 32-bit addresses by concatenating the pointers with the high-order 16 bits of a mailbox start address. Each mailbox can consist of a maximum of "64K bytes - one indication". All mailbox pointers are located in the direct address registers of the μPD98405. The host sets the initial value of each mailbox pointer in a register before starting transmission/reception. The initial values of MWA and MTA are set in the same manner as MSL.

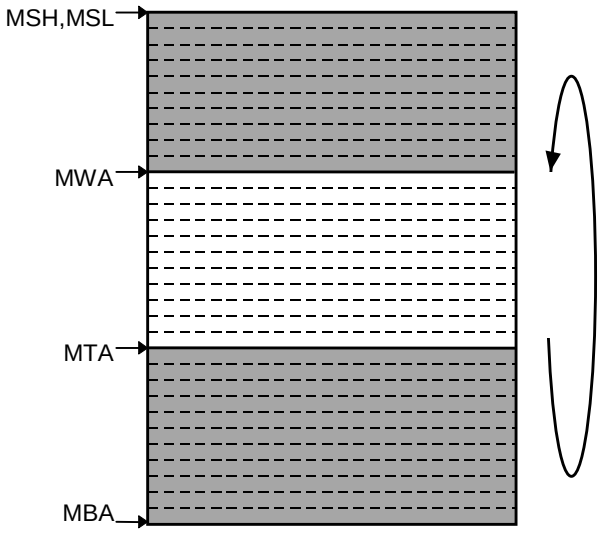
Cautions 1. A receive indication consists of four words. The size of a receive mailbox must, therefore, be a multiple of four words.

2. Do not set the same value in both MSL and MBA. If an attempt is made to use the entire 64K-byte area of a mailbox with MSL set to "0000H", MBA will be "0000H" because it exists at the address next to the last address. To use the entire 64K bytes of a mailbox, therefore, specify one indication less than 64K bytes for MBA.
Transmission: FFFCH, reception: FFF0H

3. **MTA is the only register related to mailboxes that can be updated and controlled by the host. MSH, MSL, MWA, and MBA must be written by the host during initialization but cannot be modified while the μPD98405 is performing transmission or reception. The μPD98405 frequently accesses and controls these registers during transmission/reception. Modifying them during transmission/reception will thus cause a malfunction.**

★ 4. **A mailbox cannot be located on a 64K byte boundary in system memory. Locate a mailbox within a 64K byte area.**

Figure 5-5. Mailbox Structure



5.3.2 Mailbox Operation

The μPD98405 increments the write pointer (MWA) every time it writes an indication. Each time an indication is written, the μPD98405 sets the MM bit of the GSR register corresponding to the mailbox, and generates an interrupt, provided it is not masked.

If the bottom address (MBA) is reached while the μPD98405 is updating the write pointer (MWA), the MWA jumps to the start address (MSL).

The read pointer (MTA) is used to prevent the μPD98405 from overwriting an indication that has not yet been read by the host. The read pointer (MTA) for each mailbox is managed and updated by the host. Each time the host reads an indication from a mailbox, it writes, to the read pointer (MTA), the address next to that of the indication which has just been read. MTA can be updated only by the host, and read only by the μPD98405.

If the write pointer (MWA) is set to the same address as the read pointer (MTA), the μPD98405 sets, in the GSR register, the MF bit corresponding to the mailbox to indicate mailbox full (MF) status, and generates an interrupt provided it is not masked. In MF status (MWA = MTA), the μPD98405 does not issue subsequent indications to the mailbox. The host must read an indication from the mailbox in MF status, and immediately update MTA.

Caution If the μPD98405 is forced to wait for DMA transfer of an indication because the mailbox has entered the MF status, all DMA operations are stopped until the indication has been transferred. If the MF status occurs frequently, therefore, transmission/reception may be adversely affected.

Table 5-1. μPD98405 Mailbox Operation

(a)	When an indication is issued, the value of MWA is changed to current MWA + number of bytes of one indication.
(b)	If MWA = MBA, MWA is changed to MSL.
(c)	If MWA = MTA, the MF bit of the GSR register is set.
(Number of bytes of one indication Receive = 16 bytes (4 words) Transmit = 4 bytes (1 word))	

5.4 TRANSMISSION FUNCTION

5.4.1 Transmission Processing Flow

The transmission of cells by the μPD98405 is divided into several stages as illustrated below.

Figure 5-6. Outline of Transmission Flow

	Host processing
(1)	Sets scheduler register
(2)	Sets transmit data
(3)	Open_Channel command
(4)	Sets VC table
(5)	Tx_Ready command
	:
	:
(13)	Reads transmit indication
(14)	Updates mailbox pointer (MTA)

	μPD98405 operation
(6)	Activates shaper and links VC with shaper
(7)	Scheduling
(8)	Fetches packet descriptor
(9)	Fetches data from system memory in VC segment units
(10)	Creates cells (inserts AAL-5 trailer or CRC-10 as necessary)
(11)	Transmits cells to PHY layer device
(12)	Stores transmit indication and issues interrupt

The μPD98405 can support up to 32K channels consisting of any combination of transmit VCs and receive VCs.

(1) The host sets the scheduler register to the indirect address register of the μPD98405 to determine the transmission rate before transmission can be started.

(2) The transmit data is stored into system memory and is managed by the host using a transmit queue set for each transmit channel. The transmit queue stores the descriptor of each packet.

(3) The host opens a channel (VC) by issuing an Open_Channel command to each connection to be set. The μPD98405 allocates a block to be used as a VC table, from the free block pool of control memory, and returns the address of the block to the host.

(4) The host sets an initial value in the VC table. This completes the preparation required prior to starting transmission.

(5) The host issues the Tx_Ready command to the μPD98405 so that the μPD98405 can start transmission.

(6) Upon receiving this command, when the VC uses the VBR service, the μPD98405 activates the shaper to which the VC is to be linked and adds that VC to the shaper link list. When the VC uses the ABR service, the μPD98405 registers that VC in the ABR scheduler.

(7) Subsequently, the μPD98405 performs following procedure in accordance with the scheduling.

(8) Reads the transmit descriptor and writes it in the VC table.

(9) Fetches data in units of segments.

(10) Generates cells internally.

(11) Transmits cells to the PHY layer, then repeats steps (8) through (11) until a complete packet has been transmitted.

(12) The μPD98405 stores the transmit indication to a mailbox as status information for each packet, then issues an interrupt.

(13) The host reads the mailbox.

(14) Updates the read pointer of the mailbox, a register of μPD98405.

Note that Figure 5-6 only outlines the flow of transmission processing.

5.4.2 Transmit Data Structure

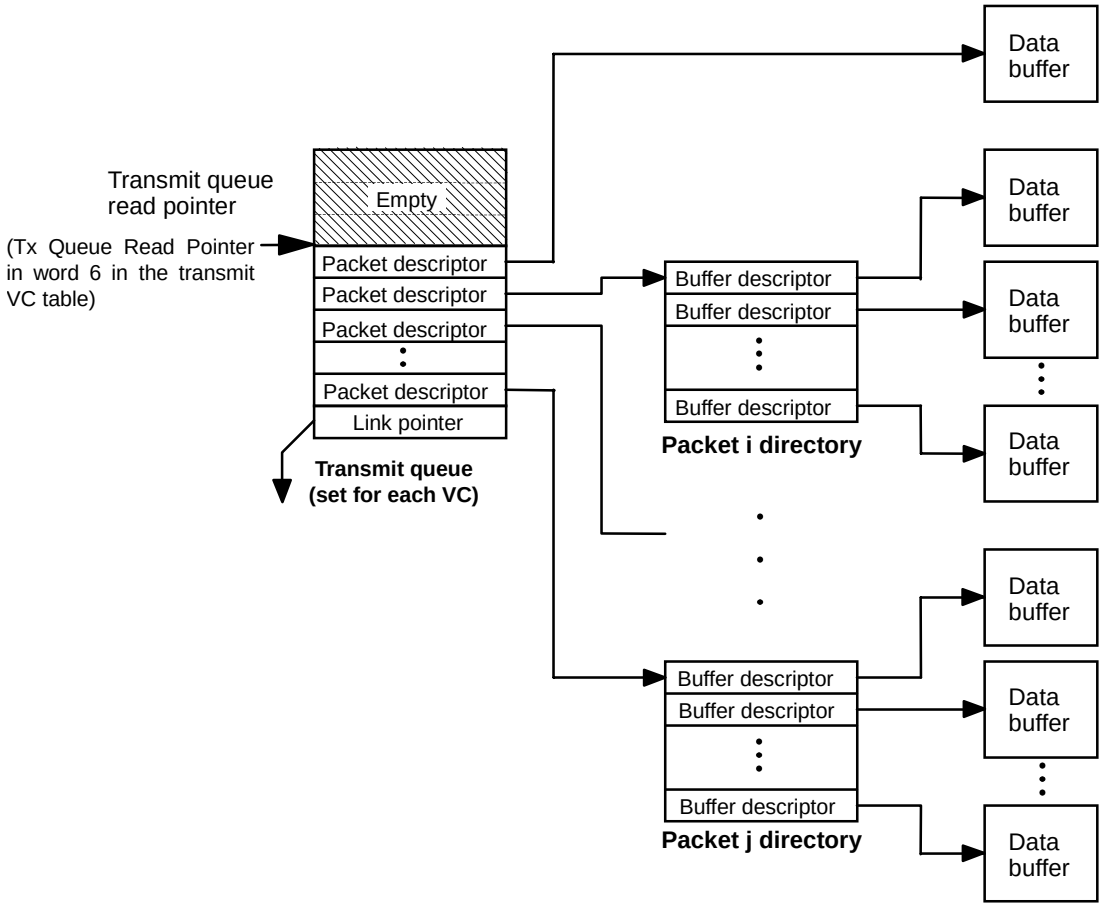
Transmit data is stored into the system memory managed by the host. The transmit data of each VC set in system memory consists of the following three elements. Figure 5-7 shows the structure of the transmit data.

(1) Transmit queue

(2) Packet directory

(3) Data buffer

Figure 5-7. Structure of Transmit Data in System Memory



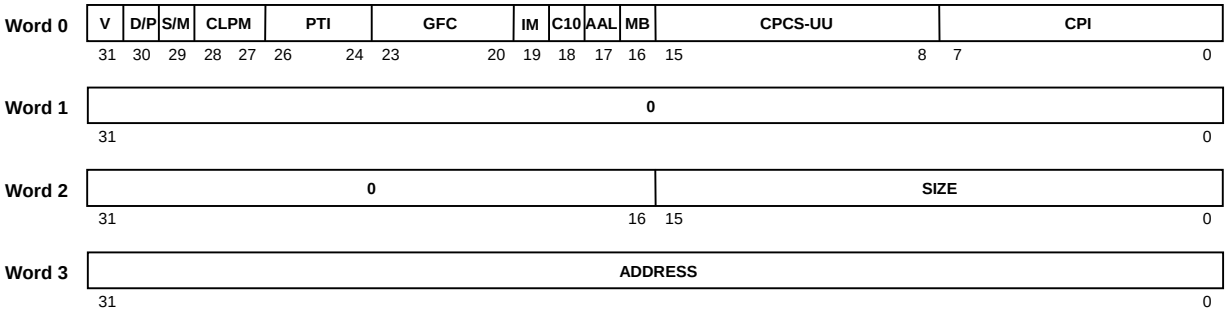
(1) Transmit queue

The host creates and manages a transmit queue for each channel (transmit VC). The transmit queue consists of the packet descriptors for the corresponding channel. Each packet has one or more data buffers. The read pointer of the transmit queue, in the corresponding transmit VC table of control memory, is initialized by the host. Subsequently, the read pointer is updated and managed by the μPD98405 each time the transmit packet descriptor is fetched.

Do not release the transmit queue for a VC while that VC exists. A transmit queue is set for each VC. The host sets the initial value of the read pointer for that queue (Tx Queue Read Pointer) in the transmit VC table. The read pointer value is updated each time the μPD98405 transmits a packet. During transmission, the μPD98405 reads the packet descriptor in system memory pointed to by the read pointer. Packet descriptor control by the host and read access to a packet descriptor by the μPD98405 are not synchronized. If the host releases a transmit queue area in system memory, therefore, the μPD98405 cannot obtain correct information from the packet descriptor, such that a malfunction occurs. Before releasing a transmit queue area, therefore, first close the VC for that queue by executing the Close_Channel command.

Figure 5-8 shows the format of the packet descriptor.

Figure 5-8. Format of Packet Descriptor



A "packet descriptor" consists of four words, and is located at a word boundary in system memory. One packet descriptor is set for each transmit packet. The packet descriptor can store the pointer to a data buffer or that to a packet directory. Each field of the packet descriptor is described below.

<1> V, D/P, S/M bit

Table 5-2. Function of Packet Descriptor

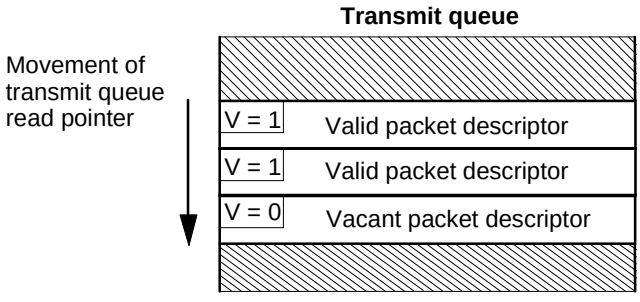
V	D/P	S/M	Function
0	-	-	Vacant packet descriptor
1	0	-	Link pointer
1	1	0	Packet descriptor in multi-buffer mode
1	1	1	Packet descriptor in single-buffer mode

The V bit is set to "1" if the packet descriptor contains data to be transmitted or if the packet descriptor is functioning as a link pointer, indicating that the packet descriptor is valid. If the V bit is cleared to "0," the packet descriptor is handled as a "vacant packet descriptor."

The vacant packet descriptor is required to enable the μPD98405 to recognize the last valid packet descriptor in a chain of packet descriptors. Therefore, the vacant packet descriptor must be located immediately after one or more valid packet descriptors. If the V bit is set to "0," indicating a vacant packet descriptor, areas other than the V bit of that packet descriptor have no meaning, such that the μPD98405 ignores these areas. Because the μPD98405 reads a packet descriptor in 4-word units, even a vacant packet must occupy a 4-word area.

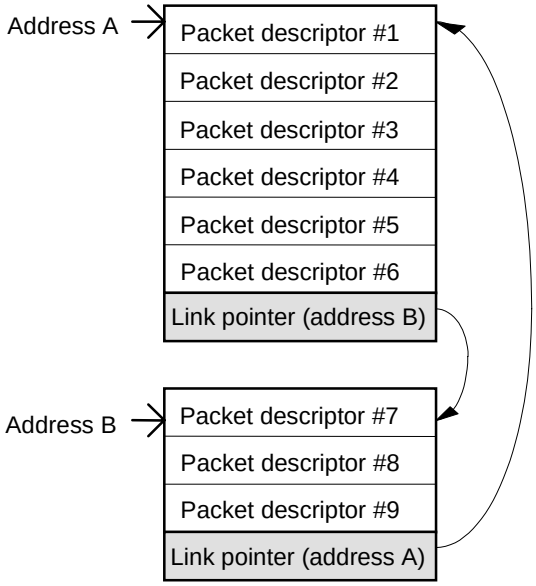
Caution The host must not set the V bit to 1 until all packet descriptor areas other than the V bit have been set. If the V bit in Word 0 is set to 1 before Words 1 to 3 have been set, the μPD98405 will finish processing of the previous packet descriptor before the host finishes setting it as a valid packet descriptor. This operation may result in a malfunction.

Figure 5-9. Location of Vacant Descriptor



The packet descriptor can also function as a "link pointer" depending on the setting of the D/P bit. This allows the user to handle a transmit queue either as a linear or ring arrangement. When the packet descriptor is used as a link pointer, the first address of the next valid packet descriptor is stored into the "ADDRESS" field. In this case, those fields other than the V and D/P bits and ADDRESS field of the packet descriptor have no meaning, and are ignored by the μPD98405.

Figure 5-10. Location of Transmit Queue

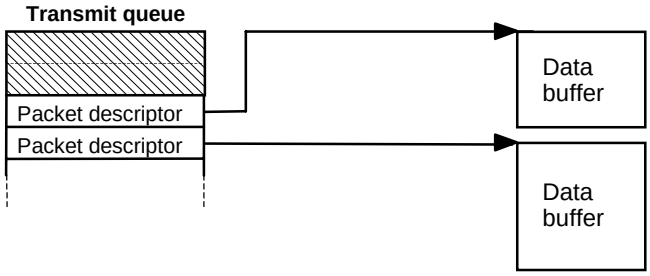


The S/M bit of a packet descriptor indicates whether this transmit packet conforms to single-buffer mode or multi-buffer mode.

- **Single-buffer mode**

  In single-buffer mode, one transmit packet consists of one data buffer. In this case, the "ADDRESS" field of the packet descriptor stores the start address of the data buffer.

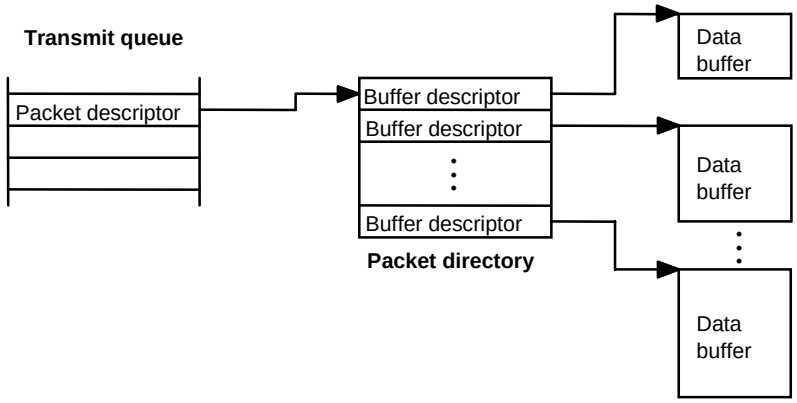
Figure 5-11. Single-Buffer Mode



- **Multi-buffer mode**

  In multi-buffer mode, one transmit packet consists of two or more data buffers distributed in system memory. In this case, the data buffers are bundled by using a "packet directory." The "ADDRESS" field of the packet descriptor contains the start address of the packet directory.

Figure 5-12. Multi-Buffer Mode



Packet descriptors in single-buffer mode and multi-buffer mode can be mixed in the single transmit queue.

<2> CLPM

This field selects the transmission mode for the "CLP" bit in the cell header with which this packet will be transmitted. The μPD98405 changes and transmits the CLP bit in accordance with the setting of this field.

Bit	Mode
00	Clears the CLP bit of all cells with which this packet is to be transmitted, to "0."
11	Sets the CLP bit of all cells with which this packet is to be transmitted, to "1."
01	Sets the CLP bit of all cells with which this packet is to be transmitted, except the last cell, to "1." Simultaneously, it clears the CLP bit of the last cell to "0."
10	Setting prohibited

Do not set code "10" in the CLPM field. When a raw, OAM, or RM cell is transmitted, only "00" or "11" is valid. "01" must not be set.

<3> PTI

The three bits set by the user in this field are inserted into the "PTI" field of each cell header when a transmit packet is disassembled into cells prior to transmission.

The μPD98405 recognizes the pattern set in this field when it transmits data. The actual transmission operation differs depending on whether the packet is an OAM F5 cell code (100 or 101).

- **If the pattern (100 or 101) for the OAM F5 cell is set:**

  The μPD98405 unconditionally transmits that packet as an OAM cell. The transmission of an OAM cell differs from that of an AAL-5 or raw cell (including the RM cell). See **Section 5.4.6**.

  If the pattern of an OAM F5 cell is set, clear the AAL bit to "0" to select raw cells.

  When using packet descriptors for OAM F5 cell transmission, use a single packet descriptor for each OAM F5 cell. The buffers indicated by a packet descriptor for OAM F5 cell transmission must be used in single-buffer mode, not multi-buffer mode.

- **If a pattern other than that for the OAM F5 cell is set:**

  Whether the packet is processed as the transmit packet of AAL-5, or as a raw cell, is determined by the setting of the AAL bit.

  - **If AAL-5 type is set (AAL bit = 1):**

    The μPD98405 inserts the code set in this field as is for cells other than the last cell. The μPD98405 transmits the last cell of a packet after changing the least significant bit to "1."

  - **AAL type other than AAL-5 (AAL bit = 0):**

    The μPD98405 inserts the contents set in this field into all the headers of the transmit packet prior to transmission. The μPD98405 transmits the last cell without changing the least significant bit of the PTI field to "1."

<4> GFC

This field contains the GFC patterns of all the cells of this transmit packet. The μPD98405 inserts the contents arbitrarily set by the user into all the GFC fields prior to transmission.

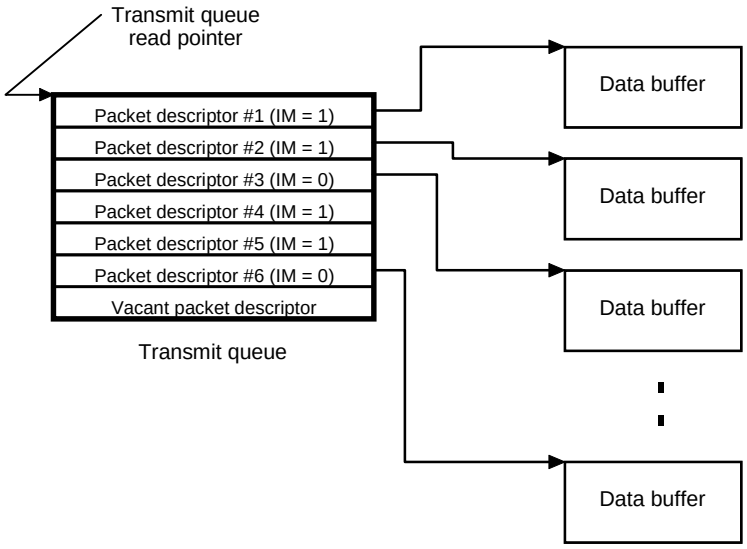
<5> IM

This bit specifies whether the μPD98405 informs the host of the completion of packet transmission.

IM	1	The μPD98405 does not inform the host of the completion of packet transmission.
	0	The μPD98405 informs the host of the completion of packet transmission by means of an interrupt, and stores an indication into the mailbox.

If this bit is set to "1," the μPD98405 does not issue a packet transmission completion interrupt to the host or store an indication into the mailbox. The following example shows how a packet for which the transmission completion interrupt is masked is handled.

Figure 5-13. Transmit Queue Containing Interrupt Mask Packets



The host sets interrupt mask packets in packet descriptors #1, #2, #4, and #5. The μPD98405 does not inform the host of when it has transmitted packets #1 and #2. Once it has transmitted packet #3, it informs the host by issuing an interrupt, and stores the relevant indication into the mailbox. Upon being informed of the completion of the transmission of packet #3 by means of the indication, the host releases the data buffers for packets #1, #2, and #3. In this way, it is possible to process more than one complete packet through one transmission completion interrupt.

<6> C10

This bit specifies whether a CRC-10 error detection code is inserted.

C10	1	The μPD98405 inserts a 10-bit CRC-10 error detection code in each cell.
	0	The μPD98405 does not insert a CRC-10 code.

If this bit is set to "1," the μPD98405 executes a CRC operation on the field having the payload part, excluding the last 10 bits, and inserts the result at the end of the cell as a 10-bit CRC-10 error detection code.

Figure 5-14. Inserting CRC-10

Header 5 bytes	Payload 46 bytes + 6 bits	CRC-10 10 bits

The polynomial used for generating CRC-10 is as follows:

$$G(X) = 1 + X + X^4 + X^5 + X^9 + X^{10}$$

When using the CRC-10 error detection function of the μPD98405, note the following points.

Cautions 1. The μPD98405 reads 48 bytes of data, corresponding to one cell, from the data buffer at a time. However, the last 10 bits of these 48 bytes are overwritten with a CRC-10 error detection code. Therefore, inserting dummy data or other processing must be performed for that part of the data buffer to which the CRC code will be inserted, given that that part will ultimately be overwritten.

2. Ensure that the AAL bit is set to 0, before attempting to set the C10 bit to 1 to enable the CRC-10 insertion function.

<7> AAL

This field specifies whether the transmit packet is handled as an AAL-5 type packet or as some other type.

AAL	1	The μPD98405 handles this packet as an AAL-5-PDU.
	0	The μPD98405 handles this packet as a raw cell.

<8> MB

This field specifies either the second or third mailbox as that mailbox into which a packet transmit indication will be stored.

MB	1	Specifies mailbox 3.
	0	Specifies mailbox 2.

For details of the mailboxes, see **Section 5.3**.

<9> CPCS-UU, CPI

The μPD98405 inserts the patterns set by the user in these fields, into the CPCS-UU and CPI fields of the AAL-5 trailer. These fields are valid only when a packet of AAL-5 type is transmitted (when AAL bit = 1); otherwise, the μPD98405 ignores these fields.

CPCS-UU: CPCS user-user indication

CPI: Common part indication

<10> SIZE

Single-buffer mode: Stores the size of the buffer, in bytes.

Multi-buffer mode: This field is meaningless and is ignored by the μPD98405.

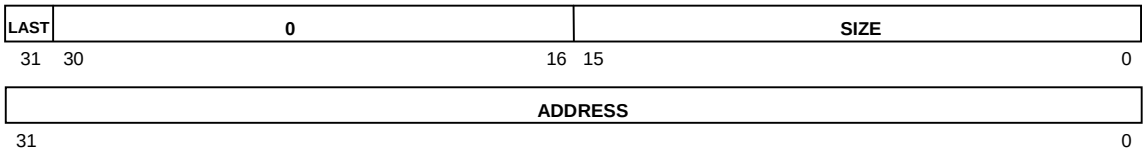
<11> ADDRESS

Single-buffer mode	Stores the data buffer start address. Data buffers can be allocated starting from a byte boundary in system memory. This field, therefore, stores a 32-bit byte address.
Multi-buffer mode	Stores the start address of the first buffer descriptor in the packet directory. Buffer descriptors must be allocated starting from word boundaries in system memory. The low-order two bits of the address stored in this field must, therefore, be 00.
Link pointer (D/P = 0)	Stores the start address of the first packet descriptor in the next transmit queue. Packet descriptors must be allocated starting from word boundaries in system memory. The low-order two bits of the address stored in this field must, therefore, be 00.

(2) Packet directory

The packet directory is set when a transmit packet is configured in multi-buffer mode. It need not be set in single-buffer mode. The packet directory consists of contiguous 2-word buffer descriptors, as shown in Figure 5-15. The buffer descriptor is a pointer to the first address of the data buffer.

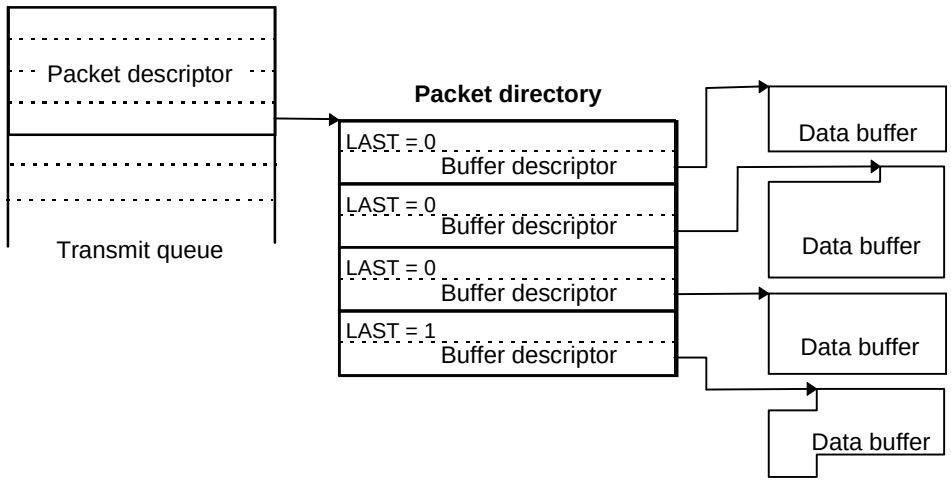
Figure 5-15. Format of Buffer Descriptor



<1> LAST

This bit is set to "1" if the buffer descriptor indicates the last data buffer of a transmit packet.

Figure 5-16. Setting of LAST Bit



<2> SIZE

This field sets the size of the data buffer, in bytes.

<3> ADDRESS

This field sets the start address of the data buffer. Data buffers can be allocated starting from a byte boundary in system memory. This field, therefore, stores a 32-bit byte address.

Remark The transmit queue for a single VC can simultaneously contain packet descriptors for AAL-5, OAM F5 transmission, and raw cell transmission.

(3) Data buffer

The data buffer stores the transmit data that is actually transmitted. The transmit data can be located at a byte boundary in system memory, and a size of up to 64K bytes can be specified. For data of AAL-5 type, the transmit data coincides with the "user data" field of CPCS-PDU.

5.4.3 Transmit Channel

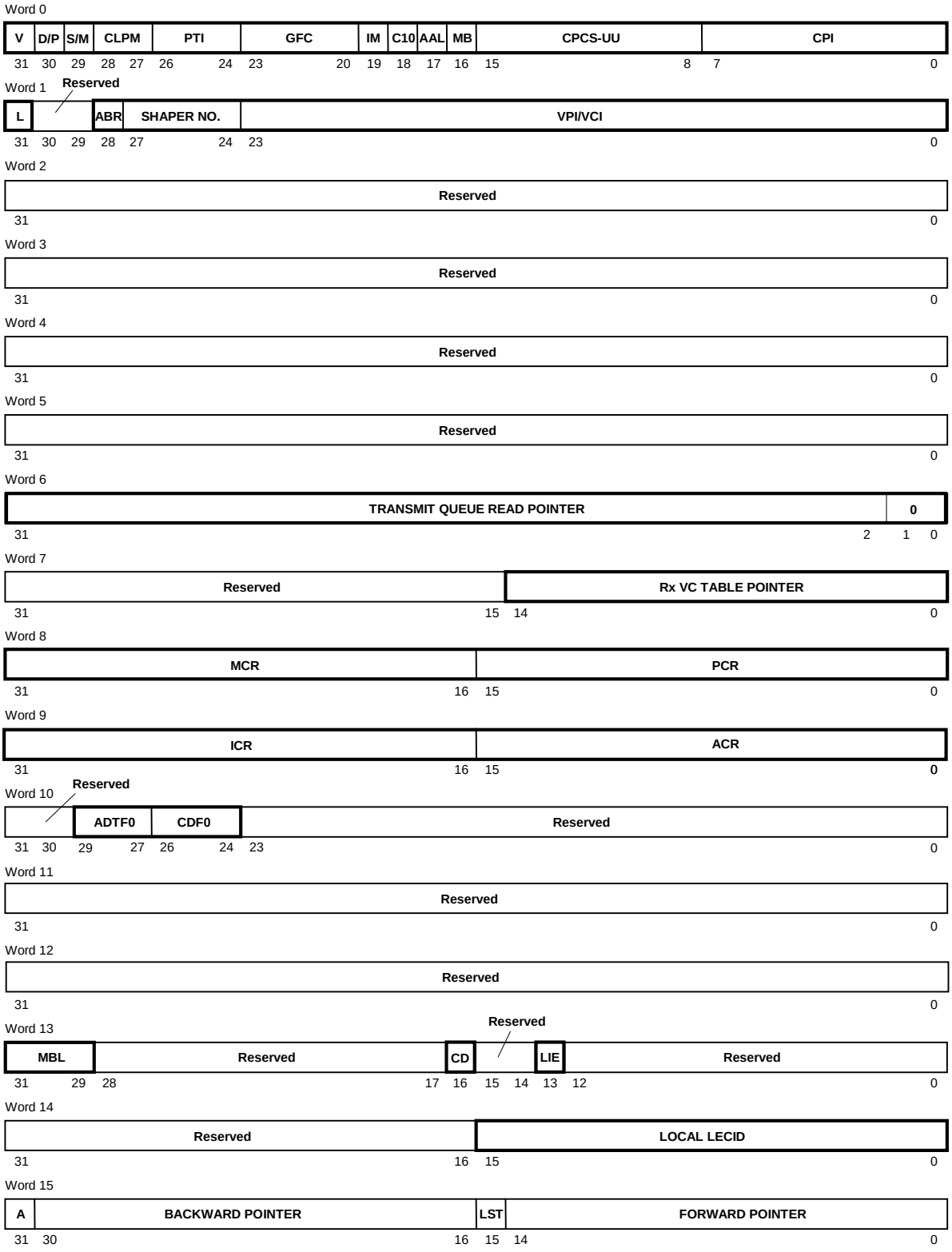
(1) Opening the transmit channel

When the host issues an Open_Channel command, the μPD98405 allocates the block indicated by TOS (top of stack) from the free block pool in control memory, and issues a response to the host by using the first address of the block as a command indication. The μPD98405 assigns one block (16 words), using the Open_Channel command. The host specifies the use of the allocated block as a transmit VC table.

(2) Setting the transmit VC table

For each VC, the host sets an 16-word block, allocated from the free block pool of control memory, as a transmit VC table. The structure of this block is shown in Figure 5-17. The host sets initial values into those portions indicated by bold lines in the figure. The host uses the Indirect_Access command to write the VC table. Those areas indicated by other than bold lines are used by the μPD98405 for transmission.

Figure 5-17. Transmit VC Table



Remark ☐: The host sets initial values in those fields that are indicated by thick frames.

Word 0 The contents of Word 0 in the packet descriptor, read from system memory by the μPD98405, are stored as is. Word 0 must be initially cleared to all 0.

L Bit used by the μPD98405 as a flag. Set this bit to "1" as the initial value.

ABR ABR bit.
This bit specifies whether the VC uses the ABR service.
1: ABR service
0: CBR, VBR, and UBR services

SHAPER NO. Shaper number.
This field specifies the number of a shaper with which this VC is to be linked.
When the ABR bit is set to "1," this field has no meaning.

VPI/VCI VPI/VCI field of cell header.

Tx QUEUE READ POINTER Pointer that indicates the first address of the next packet descriptor.
The initial value is set by the host. Packet descriptors must be allocated starting from word boundaries. The low-order two bits of the address stored in this pointer must, therefore, be 00. The μPD98405 updates this pointer each time it transmits a packet. Do not modify the value of this pointer other than when performing initialization. Upon the termination of packet queue transmission, this pointer points to an empty packet.

Rx VC TABLE POINTER[Note] Pointer that indicates the address of the receive VC table.
This field is set with the VC NUMBER (excluding the low-order four bits of the VC table address) of the VC table used to receive a turn-around BRM cell. It is specified when this VC uses the ABR service.

MCR[Note] Minimum cell rate.
This is specified when this VC uses the ABR service.

PCR[Note] Peak cell rate.
This is specified when this VC uses the ABR service.

ICR[Note] Initial cell rate.
This is specified when this VC uses the ABR service.

ACR[Note] Allowed cell rate.
This field must be set to the same initial value as that of the ICR. This is specified when this VC uses the ABR service.

Note The fields are used only by the VC which uses the ABR service. These fields must all be reset to "0" if the ABR bit is "0."

ADTF0[Note] ACR decrease time factor.

Time limit for the FRM transmission interval. If the FRM is not transmitted within this time, the ACR is reduced to the ICR. The ADTF is expressed as follows:

ADTF (milliseconds) = $10*2^{ADTF0}$

This is specified when this VC uses the ABR service.

CDF0[Note] Cutoff decrease factor.

This factor is used to control the decrease of ACR together with the CRM. The CDF is represented as follows:

CDF = $1/2^{CDF0}$ when CDF0 = 0 to 6

CDF = 0 when CDF0 = 7

This is specified when this VC uses the ABR service.

MBL Maximum burst size for multicell transfer.

The μPD98405 supports multicell transfer only in PCI bus mode. The maximum size for multicell transfer is 5 cells. The host must specify the MBL in cell units. If the MBL is "000" or "001," the multicell transfer function is disabled, and the μPD98405 performs transfer in 1-cell units. If the MBL is either "110" or "111," it is recognized as being "101" to support transfer in 5-cell units. The MBL must be "000" for Generic bus mode.

CD Close channel disable.

This is used to indicate that if the CD bit is "1," a Close_Channel command for this channel cannot be accepted. If the CD bit is set to "1," when the host issues a Close_Channel command, the response returned is a command indication of a failure in closing a channel. This bit must initially be set to "0."

LIE Transmit LECID insert enable.

This bit specifies whether to enable the transmit LECID insert function.

1: Enable

0: Disable

When the transmit LECID insert function is enabled, a value for the LOCAL LECID field is automatically inserted as an LECID into a transmit packet.

LOCAL LECID Local LECID.

When the transmit LECID insert function is enabled, a value from this field is automatically inserted as an LECID into a transmit packet. If the LIE bit is "0," this field has no meaning.

A Active bit.

Indicates whether this VC table is in the active or idle status.

1: Active status

0: Idle status

Note The fields are used only by the VC which uses the ABR service. These fields must all be reset to "0" if the ABR bit is "0."

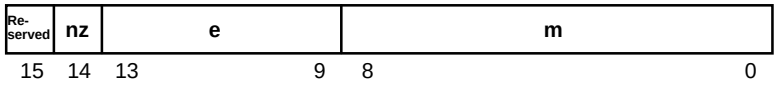
BACKWARD	
POINTER	Pointer to the preceding VC in the shaper link list.
LST	Last VC.
	"1" indicates that this VC is the last VC in the shaper link list.
FORWARD	
POINTER	Pointer to the next VC in the shaper link list.

Remarks 1. Those fields indicated as "Reserved" are reserved for the μPD98405. Do not modify these fields except at initialization. Reset all of them to 0 at initialization.

2. Do not modify Word 15 even at initialization for open VC tables. Word 15 of the transmit VC table holds the pointers and flags required for the μPD98405 to manage the VC table. If Word 15 is modified by an external host, it becomes impossible for the μPD98405 to manage correctly.

3. The rate fields (MCR, PCR, ICR, and ACR) are represented as follows:

Rate = 2^e*(1 + m/512)*nz cells/s



4. See also **Section 5.8.4** for details of the ABR parameter.

(3) Status transition of transmit channel

The transmit channel can assume one of three statuses: non-existent, idle, and active. The host opens a channel by issuing an Open_Channel command. After the μPD98405 receives this command, it reports the address of the transmit VC table to the host, as a command indication from the free block pool of control memory. Next, the host writes appropriate parameters (such as VPI/VCI, the shaper to be used, and the transmit queue read pointer) to the allocated block by using the Indirect_Access command. Thus, this block is set as a transmit VC table, and the channel enters the idle status.

While the channel is in the idle status (once all parameters have been set), the VC is ready to perform transmission. In this status, once the data to be transmitted has been generated and the host has prepared a valid packet descriptor, the host issues a Tx_Ready command to the μPD98405. Upon receiving this command, the μPD98405 sets bit "A" in Word 15 of the VC table to "1," then adds the VC table to the link list of the shaper. For the VC that uses the ABR service, that VC is linked to the ABR scheduler. As a result, the channel enters the active status.

The VC in the active status starts cell transmission at a timing that depends on the rate determined by the scheduler. When first using this VC to transmit cells, the μPD98405 reads the packet descriptor in system memory pointed to by the transmit queue read pointer (Tx Queue Read Pointer: Word 6 in the VC table), then updates Word 0 in the VC table. At this time, if the packet descriptor is vacant (V = 0), the μPD98405 clears bit "A" to "0" in that VC table, thus returning the channel to the idle status. If the packet descriptor is valid (V = 1), cell transmission is started. The μPD98405 increments the transmit queue read pointer for the transmit VC table by four words, so that it points to the next packet descriptor.

Once the μPD98405 has read all the data in the packet, it fetches the next packet descriptor. Provided this is a valid packet descriptor, the channel remains active and continues packet transmission. The channel remains active for as long as the transmit queue contains valid packet descriptors.

Upon reading a vacant packet descriptor (V = 0), the μPD98405 recognizes that all packets have been read. Once all the data in the last packet has been read, the μPD98405 stores a transmit indication, removes the transmit VC table from the shaper link list, then clears bit "A" to 0, thus returning the channel to the idle status. Note that the channel returns to the idle status once reading from system memory has been completed, not when the μPD98405 has finished transmitting all the data of the packet.

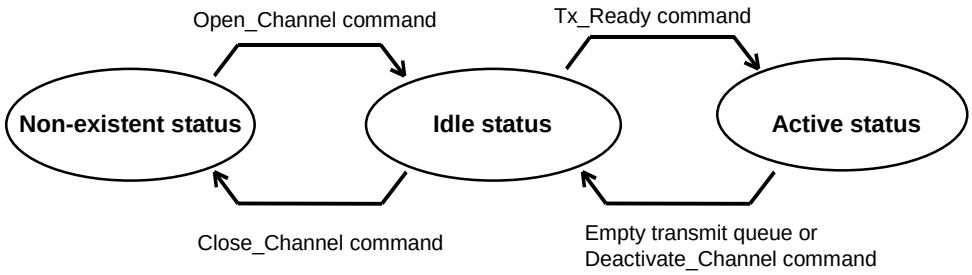
The transmit queue read pointer of the channel that has again entered the idle status indicates the last vacant packet descriptor. The next setting of a valid packet descriptor will be started from this vacant packet descriptor. The transmit queue read pointer, therefore, need not be modified by the host. The host accesses the transmit queue read pointer only when setting the initial value. When the Tx_Ready command is issued after a valid packet descriptor has been set, the channel enters the active status again.

★ **Caution When the send queue has the order "valid packet descriptor → link pointer → empty packet descriptor", the send queue read pointer points to the link pointer position after transmission is completed. The setting of the next valid packet descriptor should start from the position of the empty packet descriptor even in this case.**

The host can forcibly stop the use of a channel for transmission and return it to the idle status by issuing a Deactivate_Channel command. Once a Deactivate_Channel command is issued during transmission, the μPD98405 stops packet transmission to the channel and returns the channel to the idle status. If a Deactivate_Channel command is issued while the channel is in the idle status, the command is ignored.

To terminate the use of this channel, the host issues the Close_Channel command and returns the VC table to the free block pool while the channel is in the idle status. Consequently, the channel ceases to exist and therefore enters the non-existent status.

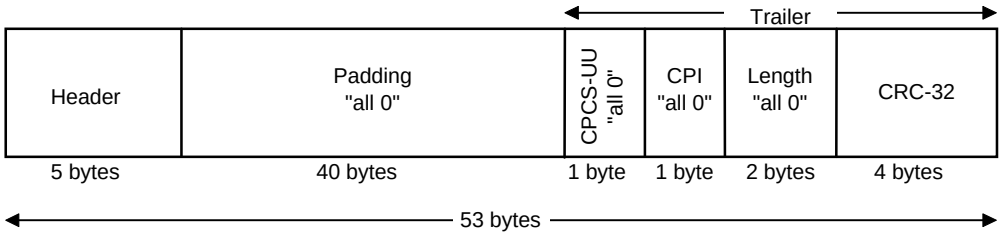
Figure 5-18. Status Transition of Transmit Channel



(4) Transmit Deactivate_Channel command

The μPD98405 can forcibly stop the use of a channel for transmission and return it to the idle state, using the Deactivate_Channel command. When the host issues a Deactivate_Channel command during packet transmission, the μPD98405 stops packet transmission and prepares a final user abort cell. The final user abort cell is a final AAL-5 PDU cell in which the AAL-5 trailer packet length field (Length) is "0." The final user abort cell is shown below.

Figure 5-19. Final User Abort Cell



Usually, if the receiving end receives a final user abort cell, it discards the relevant packet.

Upon receiving a Deactivate_Channel command during packet transmission, the μPD98405 terminates packet transmission immediately, then transmits all the cells in its internal transmit FIFO and a final user abort cell, in that order. Next, it issues an interrupt to the host in the same manner as at the normal end of packet transmission, and stores the relevant indication into the mailbox. The A bit of this indication is set to "0."

The indication is also issued even when the Deactivate_Channel command is received during the transmission of a packet with its indication masked (with the IM bit of the packet descriptor set to 1).

If the μPD98405 receives a Deactivate_Channel command when a packet is not being transmitted, the μPD98405 ignores the command and does not transmit a final user abort cell.

When packet transmission is stopped by the Deactivate_Channel command, the address of the next packet to the stopped packet is stored in Tx QUEUE READ POINTER of the transmit VC table.

Caution When packet transmission is stopped by a Deactivate_Channel command issued by the host, make sure that the VC is inactive (the A bit of the VC table is 0) before issuing a Tx_Ready command to the VC.

(5) Closing a transmit channel

To terminate the use of a channel, the host issues a Close_Channel command when the channel is in the idle state. The channel can be placed in the idle state by emptying the transmit queue or by issuing a Deactivate_Channel command.

When the host issues a Close_Channel command, the response returned is a Close_Channel indication. If the indication has the VC NUMBER of a channel to be closed, it means that the Close_Channel command was executed successfully. The μPD98405 returns the VC table to the free block pool. Consequently, the channel cease to exist and therefore enters the non-existent state.

If the host issues a Close_Channel command to a channel while it is in the idle state (A bit is "0"), a Close_Channel indication, indicating a failure in closing the channel, may be returned as a response. This is because the channel is in the idle state, but those cells in the internal transmit FIFO have not yet been transmitted to the PHY layer. In this case, the μPD98405 is performing internal processing related to the channel and does not allow the VC table to be released. If the host receives a close failure indication, it must continue to issue Close_Channel commands until one is accepted. If execution of a Close_Channel command fails, the CD bit of the relevant VC table is set to 1.

5.4.4 Traffic Control

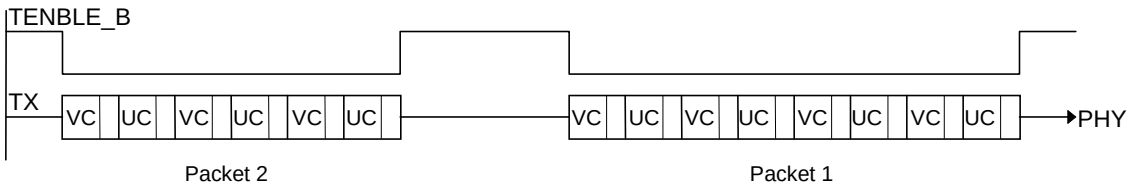
This section mainly describes VBR and CBR traffic control. It focuses on the behavior of the VBR shaper and scheduler. See **Section 5.8** for a description of ABR traffic control.

(1) Cell transmission

The ATM layer of the μPD98405 transmits cells to an external PHY layer device via the UTOPIA interface. It also sends them to the built-in PHY layer.

Cells are transmitted continuously if at least one transmit VC is active or if a shaper is specified as an unassigned/idle cell generator. In all other cases, the TENBL_B signal is deactivated, preventing cells from being transmitted (from the ATM layer). See **Chapter 6** for an explanation of cell transmission from the built-in PHY layer to a PMD device. The cell transmission rate is controlled in cell units. Up to 16 different rates can be specified for VBR. For those channels that use the ABR service, the ABR scheduler performs this control.

Example: One-VC transmission with I/M = 1/2, P = 1, C = 1, and ICM = "0"



VC: Data cell
UC: Unassigned cell

(2) Scheduling

The term "scheduling" refers to determining the channel (transmit VC) from which cells will next be transmitted and the transmission sequence of those cells. The term "scheduler" refers to that module that performs scheduling. Scheduling is realized using 16 VBR traffic shapers, ABR schedulers, and the scheduler that supervises them.

Each VBR shaper has its own scheduler register. The host loads the scheduler register of the shaper to be used with parameters for determining the peak and average rates at which cells are transmitted. Each shaper performs a dual leaky bucket algorithm operation according to given parameters to generate the cell transmission timing. The host selects a shaper whose transmission rate is to be used for an open transmit VC and sets it in the transmit VC table. When an effective packet has been prepared for a transmit VC, and the transmit VC is activated by the Tx_Ready command, the transmit VC is linked to the specified shaper under the control of a shaper link list and shaper pointer entry. Each VBR shaper has a priority. The VBR shaper with highest priority can be used for CBR.

The scheduler checks the parameters of all the enabled shapers once every 36 system clock pulses to identify those shapers which are at the transmit timing. It then selects the shaper having the highest priority. The scheduler also transmits a cell in the transmit VC linked with that shaper. Traffic control consists of repeating this cycle.

Figure 5-20. Concept of Scheduling

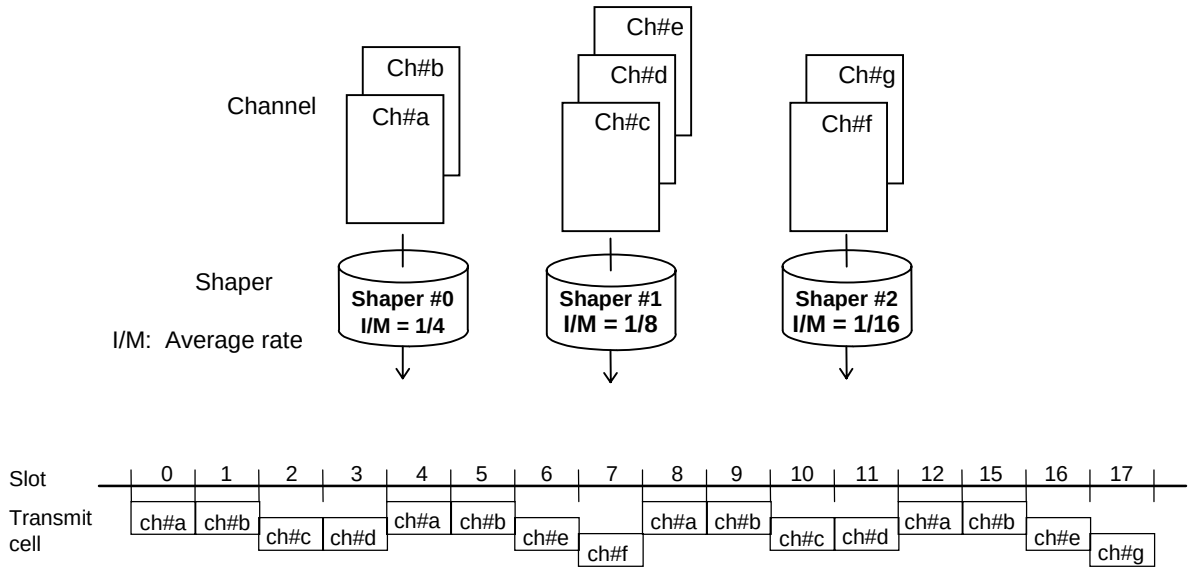
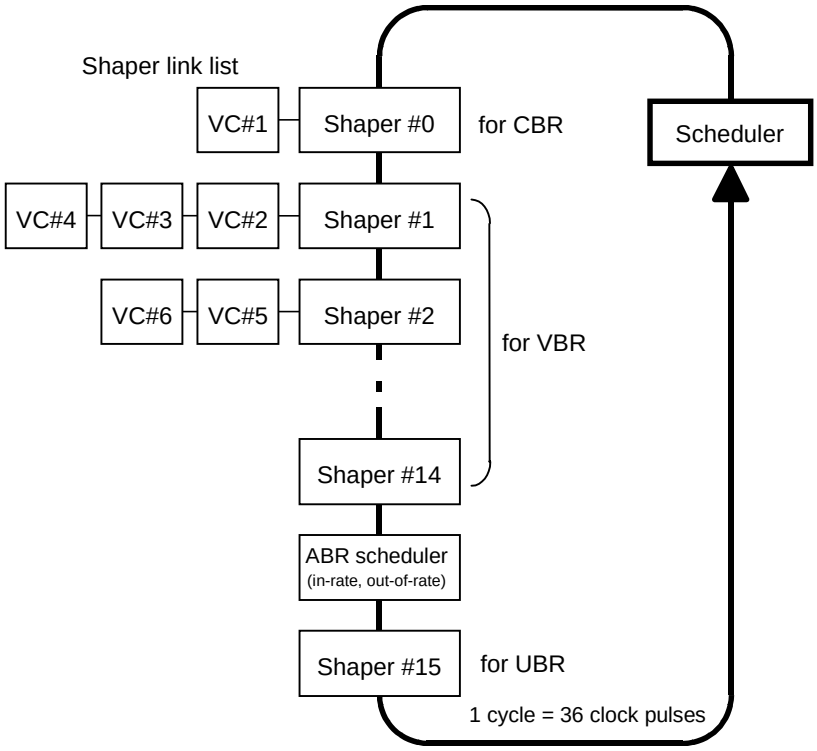


Figure 5-21. Overview of Scheduler Operation



(3) Unassigned/idle cell transmission

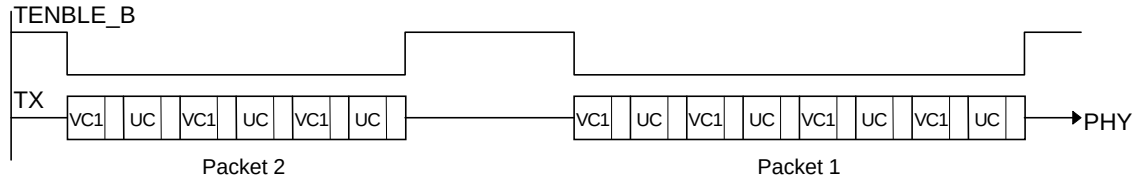
(a) Transmitting unassigned/idle cells for rate adjustment

While at least one transmit VC is active, the μPD98405 transmits cells continuously. (Note, however, that even when a VC is active, congestion of the host bus may cause the TENBL_B signal to be set to inactive, such that cells are not transmitted, once the transmit FIFO empties.) Data cells of the active VC are transmitted at the average and peak rates specified for the relevant shaper. If a shaper has no data cell to be transmitted, the μPD98405 transmits unassigned/idle cells for rate adjustment. The user can select either an unassigned or idle cell for rate adjustment and have the selected cell transmitted by the μPD98405. Cell selection is performed using the corresponding bit of the GMR register. The default setting is to transmit an unassigned cell.

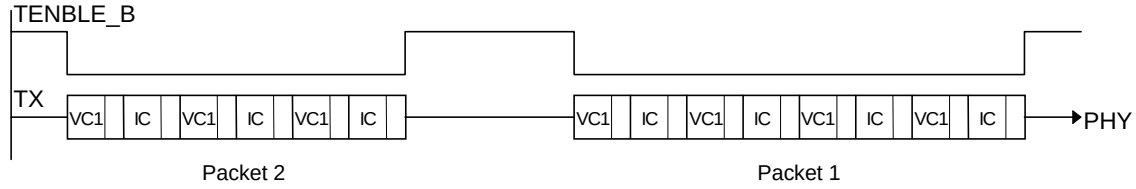
Rate adjustment cell selection		
ICM bit (Bit 28 of the GMR)	0	An unassigned cell is inserted.
	1	An idle cell is inserted.
	Default setting = 0	

Example: One-VC transmission with a shaper setting of I/M = 1/2, C = 1, and P = 0

If ICM = "0"



If ICM = "1"



VC1 = VC1 data cell; UC = unassigned cell; IC = idle cell

- Rate adjustment cell format

Unassigned cell

Header = all 00s in hex; payload = all 00s in hex

	Header					Payload				
	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 1	Byte 2	...	Byte 47	Byte 48
Content	00	00	00	00	00	00	00	...	00	00

Idle cell

Header = all 00s in hex except for CLP = 1; payload = all 6As in hex

	Header					Payload				
	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 1	Byte 2	...	Byte 47	Byte 48
Content	00	00	00	01	00	6A	6A	...	6A	6A

(b) Mode in which neither an unassigned nor idle cell is transmitted for rate adjustment

The μPD98405 can select a mode in which neither an unassigned nor idle cell is transmitted for rate adjustment. In this mode, neither an unassigned nor idle cell is output at any time. The μPD98405 transmits data cells (including RM and OAM cells) only. This mode can be selected using the UID bit of the GMR register.

Mode in which a cell is not transmitted for rate adjustment		
UID bit (Bit 29 of the GMR)	0	A rate adjustment cell is inserted.
	1	No rate adjustment cell is inserted.
	Default setting = 0	

In the mode in which a rate adjustment cell is not transmitted, if there is no data cell to be transmitted, the μPD98405 deactivates the TENBL_B signal to disable cell transmission. If no cell is transmitted, it is impossible for the built-in PHY layer and ATM PHY layer chips to adjust the timing to maintain the transmission rate. This mode is useful, therefore, in those cases in which no built-in or ATM PHY layer is used.

(4) Scheduler register

Each of the 16 shapers has a scheduler register that stores the parameters set by the host, as well as the variables managed by the μPD98405. For details, see **Section 7.3 (20)**.

The user sets the following parameters in the scheduler register of each shaper to be used, to determine the rate before starting transmission. The scheduler register is an indirect address register, such that the host can read/write the scheduler register by using the Indirect_Access command.

Remark For details of the ABR scheduler setting, see **Section 5.8.5**.

Table 5-3. Scheduler Register Bit Functions

Bit	Description
I (8 bits), M (24 bits)	Average rate. These bits specify the average rate parameter in cell units. The average rate is specified as I/M, where I cells are transmitted for every M cells.
P (peak, 8 bits)	Peak cell rate. These bits specify a minimum time difference between two consecutive cells transmitted over a channel linked to the shaper. The value is in cell units.
C (credit, 8 bits)	Credit. These bits specify the maximum number of credits that can be accumulated by a shaper. The I, M, P, and C parameters control the maximum cell count (maximum burst size) for which continuous transmission is possible at the peak rate.
AGM (Aggregate mode, 1 bit)	Selects the transmit rate control mode. 0: Normal mode. The set rate parameter is converted to VC units. 1: Aggregate mode. The set rate parameter is converted to shaper units. See **Section 5.4.4 (9)** for details.
PRIORITY (priority, 5 bits)	Priority. These bits specify the priority of the shaper. "00000" is the highest priority, while "11111" is the lowest priority.
E (enable, 1 bit)	Enables the shaper.

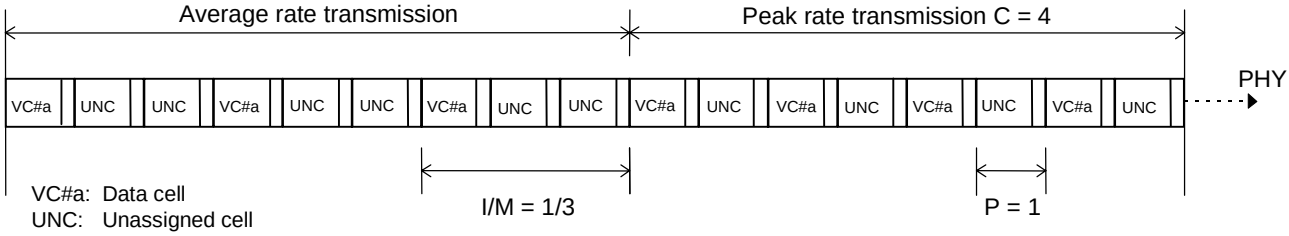
Figure 5-22. Example of Parameter Settings

Example

I/M = 1/3 (average rate)

P = 1 (peak rate)

C = 4 (maximum number of cells that can be transmitted successively at the peak rate)



The μPD98405 internally generates variables for each shaper, based on the parameters set by the user, then executes an algorithm operation. Each shaper has flags that indicate the status of the shaper. These variables and flags are stored in each scheduler register and are managed by the μPD98405. The register is enabled and updated if the enable bit "E" of each shaper is set to "1" and when the shaper enable bit "SE" of the GMR register is set to "1" by the host.

Variable	x (32 bits)
	y (32 bits)
	p (8 bits)
	c (8 bits)
Flag	S (scan, 1 bit)
	R (round robin, 1 bit)
	A (active, 1 bit)

Cautions 1. Do not set the enable (E) bit of the scheduler register to 1 before the variables and flags used by the μPD98405 have been cleared to 0 and the parameters (such as I, M, P, C, and Priority) have been set up.

2. When operation begins, the variables and flags in the scheduler register must all be set to 0.

3. The contents of the scheduler register cannot be changed if the A bit is set to 1 and the relevant shaper is active. A shaper becomes inactive when there is no linked VC table. Before changing parameters I, M, P, and C, make sure that the relevant shaper is inactive (that the A bit is set to 0) and reset the enable (E) bit to 0. Also, clear all the variables and flags used by the μPD98405 to 0.

4. The host can change only the Priority parameter at any time, even when the shaper is active (while the A bit is set to 1). In this case, set only the byte enable B3 bit of the Indirect_Access command to 1; be careful not to overwrite any other fields.

(a) Setting the transmit rate parameters

The μPD98405 performs cell scheduling according to the I, M, P, and C parameters set in the scheduler register. This section explains the setting of these parameters. The I, M, P, and C parameters are all set in VC units (except in Aggregate mode).

- I, M (average rate)

  The μPD98405 usually transmits cells at the average rate set with the I and M parameters. The average rate is specified as I/M, where I cells are transmitted for every M cells. Note, however, that the settings of the P and C parameters take priority over those of the I and M parameters. For example, if I/M = 1/1, P = 2, and C = 2 are set, cells are transmitted at a rate of 1/3.

- P (peak rate)

  The μPD98405 usually transmits cells at the average rate set as I/M. If, however, any credits (C) have been accumulated, cells are transmitted at the peak rate specified with P. The peak rate P is set for a given VC based on the amount of space between consecutive cells, in units of cells. For example, if P is set to 3, then an inter-cell space equal to three cells is always inserted. The value of the peak rate will be 1/(P + 1) = 1/4. Furthermore, regardless of whether any credits have been accumulated, the setting of P takes priority over that of I/M. For example, if I/M = 1, P = 3, and C = 2 are set (if the peak rate is lower than the average rate), cells are transmitted at the peak rate of 1/4, even during normal transmission.

- C (credit)

  When credits (C) have been accumulated, the μPD98405 transmits cells at the peak rate. The maximum number of credits that the shaper can accumulate is set in C (in VC units).
  Credits are accumulated according to the following conditions.

  - Starting from the instant that a shaper is enabled (E = 1), that shaper is scanned and, whenever the time to transmit a cell is reached, a credit is accumulated, one by one. That is, credits are accumulated starting from before the Tx_Ready command is issued, setting the shaper to the active status. At the start of cell transmission, the accumulated credits (and any in addition to this) are transmitted at the peak rate.
  - For a given shaper, whenever the cell transmission timing is reached, but the cell can not be transmitted, a credit is added. For example, if a low-priority shaper can not transmit a cell because of a timing conflict with a high-priority shaper, a credit is added to the credits of the low-priority shaper.
  - For a shaper for which credits have been accumulated, and which is transmitting those credits at the peak rate, a credit is added upon reaching the timing at which the cells are to be transmitted at the average rate. Those cells in excess of the credits set in C are transmitted at the peak rate.

  That is, the maximum number of cells that can be transmitted at the peak rate (maximum burst size) is determined from the I, M, P, and C parameters. (See **Section 5.4.4 (7)** for details.) The maximum burst size (MBS) can be determined from the following.

  MBS = (1/(P + 1)*C)/(1/(P + 1) – (I/M))

  Because the credits set the number of cells to be transmitted at the peak rate, setting C = 1 results in only one cell being transmitted at the peak rate, while a space that is transmitted at the peak rate will be at least one cell in size. For example, when one VC is linked to one shaper, setting I/M = 1/1, P = 0, and C = 1 causes transmission to be performed at a rate of 1/2. That is, when C = 1 is set, there will be occasions when transmission at the specified rate can not be performed. To

prevent this, when N VCs are linked to one shaper, and if the set rate for that shaper exceeds 1/(N + 1), set C to at least 2. Note that setting C to 0 totally disables cell transmission. Therefore, always set C to at least 1.

(b) Setting the scheduler register for CBR

When 0 is set in the priority field for a VBR shaper, according to the highest priority, that shaper can be used as a CBR. Essentially, there is no difference between the operation of a shaper that is used as a CBR and a VBR shaper. Setting the maximum priority results only in any cell delay being eliminated.

When using a shaper as a CBR, to prevent burst transmission at the peak rate, set P = 0 for the peak rate, C = 1 for the credits, and the transmission rate for I/M.

Note that, in the above case where N VCs are linked to 1 shaper, if the transmission rate (I/M) for that shaper exceeds 1/(N + 1) when C = 1 has been set, transmission at this rate is not possible. In this case, it is necessary to set C = 2 but this results in burst transmission occurring. Therefore, when I/M > 1/(N + 1), full CBR support can not be provided. At the head of a transmission packet, therefore, burst transmission is likely to occur.

(5) Shaper link list

The user selects the link destination shaper for each transmit VC, after which the host sets the corresponding 4-bit "Shaper No." field in the transmit VC table. Several VCs can be linked to a specific shaper. The μPD98405 automatically links or unlinks a transmit VC to or from a shaper.

The μPD98405 creates a link list of VC tables for each shaper to enable the management of multiple active VCs. The link list of the shaper is managed by using the fifteenth word of the VC table. This word has a "Forward Pointer" and "Backward Pointer," as well as an "Lst" bit that indicates the end of the list. A "VC NUMBER" code is written to the pointers to indicate the beginning of the VC table. By changing this code as necessary, the μPD98405 can link or unlink a VC and shaper.

Figure 5-23. Pointers Used for Linking

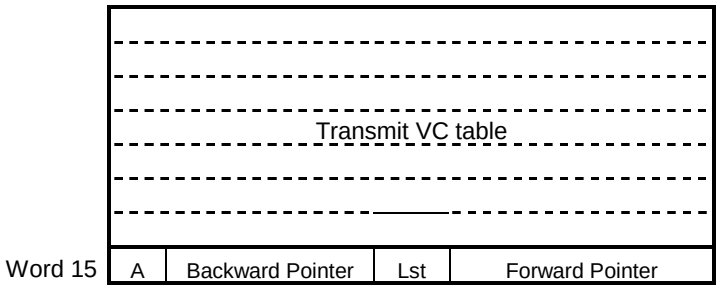
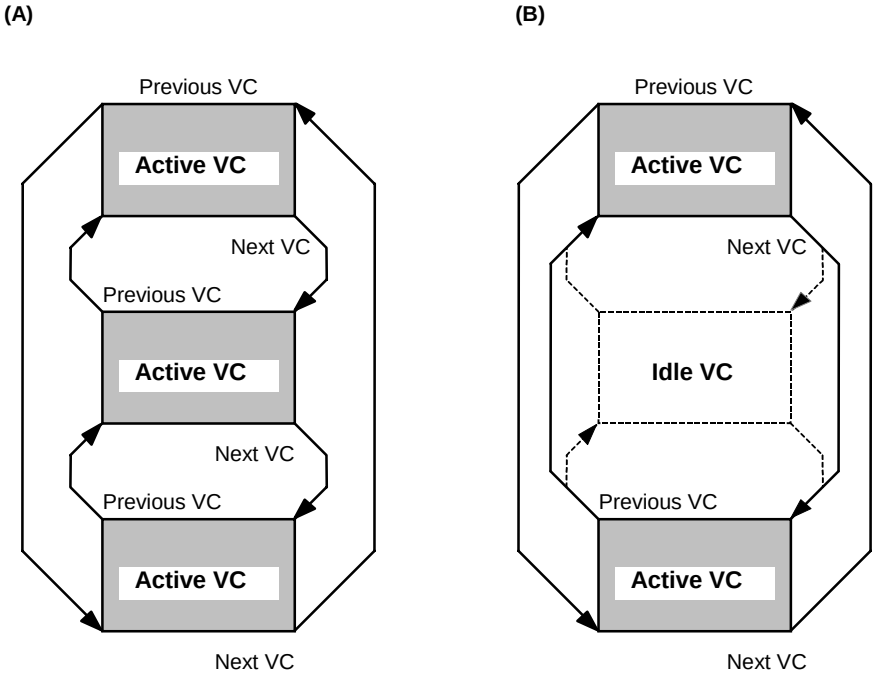


Figure 5-24. Linking and Unlinking of Transmit VC to and from Traffic Shaper



(a) Linking to shaper

A transmit VC is linked to a shaper when the host issues a Tx_Ready command to an idle transmit VC for the VBR (A bit = 0). The μPD98405 determines the number of the shaper to which the transmit VC is to be linked by referencing the "Shaper No." field of the VC table, and rewrites the "Forward Pointers" and "Backward Pointers" of the VC linked to the end of the link list of the shaper and the VCs to be newly linked. At this point, active bit A of the VC table is set to 1 to make the VC active. If no VC is linked to the shaper and provided the VC to be linked is the first VC in the link list, the settings of the active flag "A bit" of the scheduler register of the shaper, and the "a bit" of the shaper pointer entry, are switched from 0 to 1 to make the shaper active.

If the Tx_Ready command is issued to the VC in the link list of the shaper, that is currently active, the μPD98405 does not perform any processing.

(b) Unlinking

A VC is unlinked if the status of that VC changes from active to idle. If the packet descriptor of the fetched packet is vacant, and all the data in the packet to be transmitted has been read, rewriting of the "Forward Pointers" and "Backward Pointers" of the VC, and the VCs before and after it, is started. As a result, the VC is released from the link list. At this time, active bit A of the VC table is switched from 1 to 0.

If the VC to be unlinked is the last VC remaining linked to the shaper, the "A bit" in the scheduler register and the "a bit" of the shaper pointer entry are switched from 1 to 0 and the shaper itself is made inactive as soon as it has been unlinked.

The μPD98405 uses the "Forward Pointer" in the link list to control transmission processing for each VC. The μPD98405 stores the "VC NUMBER" in the "Forward Pointer" of the VC table, i.e., the "VC NUMBER" of the VC to be processed next, into the shaper pointer entry when it executes transmission processing for a certain VC. In this way, the μPD98405 determines the VC from which it should start processing after moving from one shaper to another.

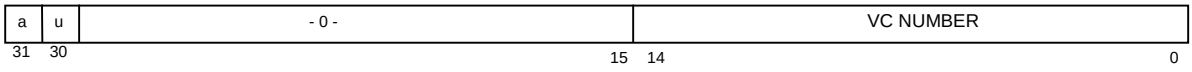
(6) Shaper pointer entry

The shaper pointer entry is a table for indicating which VCs have been processed when the μPD98405 moves from one shaper to another. It is located in the shaper pointer entry register (SPE0 to SPE15). SPE0 is the shaper pointer entry for shaper 0, while SPE15 is the shaper pointer entry for shaper 15.

The shaper pointer entry is used and managed by the μPD98405 as a table. The host can read/write this register by using the Indirect_Access command. However, the host accesses this register only when it uses the unassigned cell generator function. It does not need to access this area otherwise.

The format of the shaper pointer entry is as follows:

Figure 5-25. Shaper Pointer Entry Format



a — Active flag. This bit is used by the μPD98405 as an internal flag.
1 - At least one active VC is linked to the shaper.
0 - No active VC is linked to the shaper.
When this shaper is used as an unassigned cell generator, this bit and the u bit are set to 1 by the host.

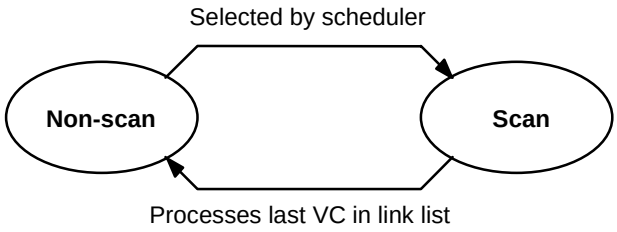
u — Unassigned cell generator. Only when this shaper is used as an unassigned cell generator, this bit is set to 1 by the host. (See **Section 5.4.4 (8)** for details.)

VC NUMBER — This field is used as a table to stack the "VC NUMBER" of the VC the μPD98405 is to transmit next. If no VC is linked to the shaper, this field consists entirely of zeros.

(7) Algorithm operation

The cell rate is controlled by executing a dual leaky bucket algorithm operation for each shaper when selected by the scheduler. The scheduler checks the variables and parameters of all the shapers once every 36 system clocks and selects one shaper to transmit data. When a shaper is selected, it is said to be in the "scan state." When it is not selected, it is said to be in the "non-scan state." These states are indicated using the "S flag" in the scheduler register. If the S flag for a shaper is set to 1, the shaper transmits the cells of the VC linked to it.

Figure 5-26. Status of Shaper



A shaper is selected by the scheduler when it satisfies all the following conditions.

<1> SE = 1 (GMR register)

All the shapers are enabled. The host sets the GMR register.

<2> E bit = 1 (scheduler register)

The shaper is enabled. The host sets the scheduler register of the shaper to be used.

<3> A = 1 (scheduler register)

An active VC to be transmitted is linked to the shaper. This is set by the μPD98405.

<4> c variable > 0 (scheduler register)

The μPD98405 updates this variable according to the I, M, and C parameters specified by the user.

<5> p variable = 0 (scheduler register)

The μPD98405 updates this variable according to the P parameter specified by the user.

Conditions **<1>** through **<3>** indicate that the shaper is enabled and that a VC to be transmitted is linked to the shaper, such that the transmission rate is not directly affected. The transmission rate is determined under conditions **<4>** and **<5>**, that is, when the c parameter is incremented to 0 or greater, and the p parameter becomes 0.

Condition **<4>**, under which the 8 bits of "c" of the scheduler register are incremented, is as follows:

(a) SE = 1

(b) E = 1

(c) $x \geq y$

(d) $c < C$

The "c" parameter is incremented according to the relationship between variable parameters x and y that are managed by the μPD98405, in addition to conditions (a) and (b), above, under which operation of the shaper is enabled. The maximum value to which this parameter can be incremented is given by the value of the C parameter, specified by the user.

The x and y variable parameters are updated by the μPD98405, according to the following rule, in a 36-clock cycle in which the scheduler checks all the shaper parameters according to the I and M parameters specified by the user.

- When x = y → I and M are loaded into x and y, respectively.
- When x > y → I is added to x and M is added to y.
- When x < y → I is added to x.

"c" is incremented when x ≥ y. When "c" is c > 0 and p = 0, the shaper may be selected by the scheduler. Upon being selected, a shaper enters scan status and starts transmitting cells.

Each time the shaper changes from scan status to non-scan status (i.e., when the transmission of all linked VCs has been completed), the c parameter is decremented.

The conditions for incrementing "c" do not require that the shaper be active (the A bit of the scheduler register is set to 1). The "c" parameter is incremented at I/M intervals until it reaches "C" (maximum) regardless of whether the shaper has an active VC.

When the shaper is selected and enters the scan state, the "p" parameter is loaded with "P" as specified by the user, and decremented by one each time the scheduler has dealt with all the shapers (every 36 clock pulses). The parameter for a specific shaper must have been decremented to 0 before the scheduler can select that shaper again. Therefore, as a minimum, the peak rate "P" must be maintained between the cells of the same VC.

Example: When only shaper 0 is used and the following parameters are set in the scheduler register:

I = 3, M = 10, P = 0, C = 4

(Transmit channel (VC #a) is opened and linked to shaper 0.)

U/I: Unassigned or idle cell

VC: Data cell

	Slot	x value	y value	x ? y	c	Scan	Transmit cell
	1 Initial value	0	0	x = y	1		
	2	3	10	x < y	1		
	3	6	10	x < y	1		
	4	9	10	x < y	1		
	5	12	10	x > y	2		
	6	15	20	x < y	2		
	7	18	20	x < y	2		
	8	21	20	x > y	3		
	9	24	30	x < y	3		
	10	27	30	x < y	3		
	11	30	30	x = y	4		
	12	3	10	x < y	4		
	13	6	10	x < y	4		
	14	9	10	x < y	4		
Tx_Ready command issued →	15	12	10	x > y	4		
	16	15	20	x < y	4	•	VC
	17	18	20	x < y	3	•	VC
	18	21	20	x > y	3	•	VC
	19	24	30	x < y	2	•	VC
	20	27	30	x < y	1	•	VC
	21	30	30	x = y	1	•	VC
	22	3	10	x < y	0		U/I
	23	6	10	x < y	0		U/I
	24	9	10	x < y	0		U/I
	25	12	10	x > y	1	•	VC
	26	15	20	x < y	0		UI
	27	18	20	x < y	0		U/I
	28	21	20	x > y	1	•	VC
	29	24	30	x < y	0		U/I
	30	27	30	x < y	0		U/I
	31	30	30	x = y	1	•	VC
	32	3	10	x < y	0		U/I
	33	6	10	x < y	0		U/I

Slot	x value	y value	x ? y	c	Scan	Transmit cell
34	9	10	x < y	0		U/I
35	12	10	x > y	1	•	VC
36	15	20	x < y	0		U/I
37	18	20	x < y	0		U/I
38	21	20	x > y	1	•	VC
39	24	30	x < y	0		U/I
40	27	30	x < y	0		U/I
41	30	30	x = y	1	•	VC
42	3	10	x < y	0		U/I
43	6	10	x < y	0		U/I
44	9	10	x < y	0		U/I
45	12	10	x > y	1	•	VC
46	15	20	x < y	0		U/I
47	18	20	x < y	0		U/I
48	21	20	x > y	1	•	VC
49	24	30	x < y	0		U/I
50	27	30	x < y	0		U/I
51	30	30	x = y	1	•	VC
52	3	10	x < y	0		U/I
53	6	10	x < y	0		U/I
54	9	10	x < y	0		U/I
55	12	10	x > y	1	•	VC
56	15	20	x < y	0		U/I
57	18	20	x < y	0		U/I
58	21	20	x > y	1	•	VC
59	24	30	x < y	0		
60	27	30	x < y	0		
61	30	30	x = y	1		
62	3	10	x < y	1		
63	6	10	x < y	1		
64	9	10	x < y	1		
65	12	10	x > y	2		
66	15	20	x < y	2		
67	18	20	x < y	2		
: :	: :	: :	: :	: :		: :

3/10

Packet completed →

Remark "C" specifies the number of cells that can be transmitted continuously at the peak rate. If C = 1 is specified for a shaper, an unassigned cell is inserted, because the shaper cannot transmit more than one cell continuously at the peak rate intervals.

Example: Setting the shaper (without taking Priority into consideration)

- I/M = 1/1
- P = 0

- If C = 1

VC#a		UC		VC#a		UN		VC#a		UN		→

An unassigned cell is inserted because it is impossible to transmit more than one cell continuously.

- If C = 2

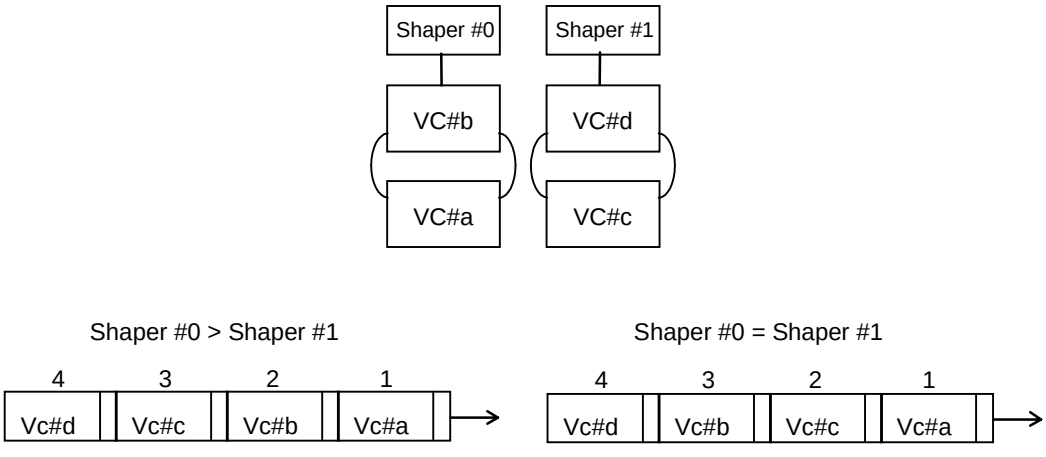
VC#a		VC#a		VC#a		VC#a		VC#a		VC#a		→

More than one cell can be transmitted continuously.

When the scheduler checks all the shapers, it selects the shaper having the highest priority from among two or more candidates that satisfy the conditions. The priority of a shaper is set by the user in the "Priority" parameter. The priority can be specified regardless of the shaper number.
If there are two or more shapers having the same priority, the scheduler selects one shaper at a time by applying a round robin algorithm. The μPD98405 uses the round robin (R) bit of the scheduler register to manage the round robin algorithm.

Example: When two shapers are used and two VCs are linked to each shaper, the cell transmission sequence will be as shown in Figure 5-27, depending on the set priority.

Figure 5-27. Cell Transmission Sequence according to Priority



(8) Unassigned (idle) cell generator function

The user can use one or more shapers as unassigned cell generators to limit the band used by the active VC. A shaper set as an unassigned cell generator functions as if it were linked to a VC that transmits a cell consisting of an all-zero header and all-zero data. By assigning a priority higher than that of the data transmission shaper to a shaper specified as an unassigned cell generator, the band used by the data can be limited.

The unassigned cell may be switched to an idle cell according to the ICM bit of the GMR register.

An unassigned cell generator is selected by means of the following procedure.

<1> Set bits 31 and 30, the "a" and "u" bits, of the shaper pointer entry of the shaper to be selected as an unassigned cell generator, to 1.

<2> Set parameters in the scheduler register. At this time, set active bit "A" to 1 at the same time as enable bit E.

Cautions 1. A normal VC cannot be linked to a shaper that is specified as being an unassigned cell generator.

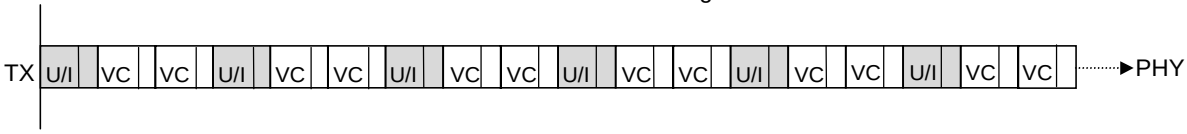
2. The host need not set the shaper pointer entry "a" bit and scheduler register "A" bit to 1, except when using the unassigned cell generator function. For a data transmit shaper, the μPD98405 automatically sets these bits to 1.

★ **3. When using the mode where unassigned cells are not transmitted for rate adjustment (UID bit of GMR register is 1), the TENBL signal goes inactive at the same timing as if unassigned cells were being transmitted.**

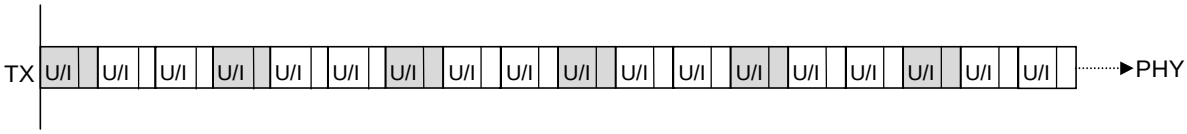
Example: Shaper 0: Set as the unassigned cell generator, and I/M = 1/3

Shaper 1: Set with usual data cell, I/M = 1/1

Those data cells to be transmitted are embedded between unassigned cells.



When there is no data cell to be transmitted



: Cell generated by the unassigned cell generator

U/I: Unassigned cell if ICM = 0
Idle cell if ICM = 1

VC: Data cell

(9) Cell transmission mode for a shaper in the scan status

A shaper that is in the scan status outputs linked VC cells. Once these cells have been transmitted, the shaper returns to the non-scan status. The conditions governing whether the shaper returns to the non-scan status vary with the following two modes. By changing the conditions under which the shaper returns to the non-scan mode, it is possible to select whether the rate parameter set for the shaper is controlled in VC units or shaper units.

A different mode can be set for each shaper. The mode is switched by setting the AGM bit of the scheduler register.

(a) Normal mode (AGM bit = 0)

A shaper in the scan status transmits the cells of all linked VCs in order, one-by-one, then returns to the non-scan status as soon as all the cells of the linked VCs (LST bit = 1) have been transmitted. In this mode, the transmission rate set for a shaper is used to control the rate set for each VC. The area that is occupied by one shaper depends on the number of VCs that is linked to that shaper.

(b) Aggregate mode (AGM bit = 1)

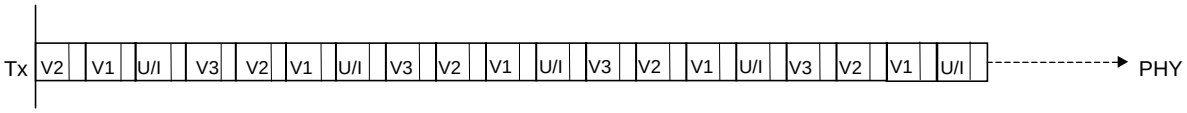
A shaper in the scan status transmits one cell to one of the linked VCs, then returns to the non-scan status. If that shaper again enters the scan status, it transmits one cell to the next VC, according to the link list. In this mode, the area for a shaper is controlled based on the set rate parameter. According to the transmission rate for each VC, the area for a shaper is assigned to the linked VCs. The area that is occupied by one shaper is not affected by the number of VCs that is linked to that shaper.

In aggregate mode, the I, M, P, and C parameters are set in the units for the given shaper, rather than in VC units. That is, the settings for I, M, P, and C are all satisfied by one unit for all the VCs that are linked to that shaper. Each VC that is linked to a shaper in aggregate mode operates at the rate that is assigned by those VCs according to the settings of I, M, P, and C. For example, if I/M = 1/4 is set for a shaper in aggregate mode, three VCs are linked to that shaper and each VC transmits cells at a rate of 1/12.

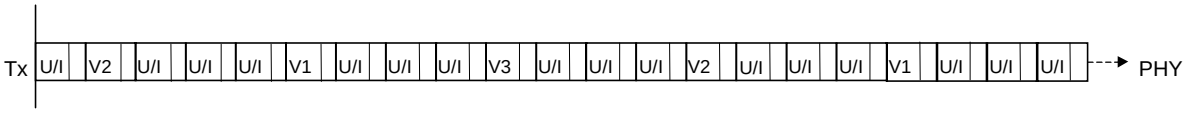
Figure 5-28. Differences in Cell Transmission Order in Different Modes

When three VCs (VC1, VC2, and VC3) are linked to a shaper for which I/M = 1/4

Normal mode



Aggregate mode



U/I: When ICM = 0, unassigned cell
When ICM = 1, idle cell
V#: Tx VC cell data, V1 = VC1 data, V2 = VC2 data, V3 = VC3 data

5.4.5 Transmit Operation

The μPD98405 takes out a transmit segment (48-byte payload data of a cell) from the packet stored in system memory, adds the AAL-5 trailer or CRC-10 as necessary, and transmits a cell to the PHY layer device.

The μPD98405 features an FIFO of 10 cells. During normal operation, the FIFO stores data received from system memory, becoming empty once the cell has been transmitted to the PHY layer device.

The transmit machine reads a segment from system memory in the VC sequence as determined by the scheduler.

The μPD98405 organizes a cell from a segment (48-byte payload data) taken out of system memory and the information on the cell header stored to the control memory. At this time, dummy data "00H" is inserted into the HEC field of the cell header.

The GFC, VPI/VCI, PTI, and CLP fields of the cell header are taken out from Word 0 of the VC table and generated. The first word of the VC table is updated by the μPD98405 by receiving a packet descriptor for each transmit packet.

In the case of the last cell, the μPD98405 sets "1" for the LSB of the PTI field, while the CLP bit is set in the CLP mode indicated by the VC table.

As the payload data of the cell, 48 bytes are read from system memory and embedded.

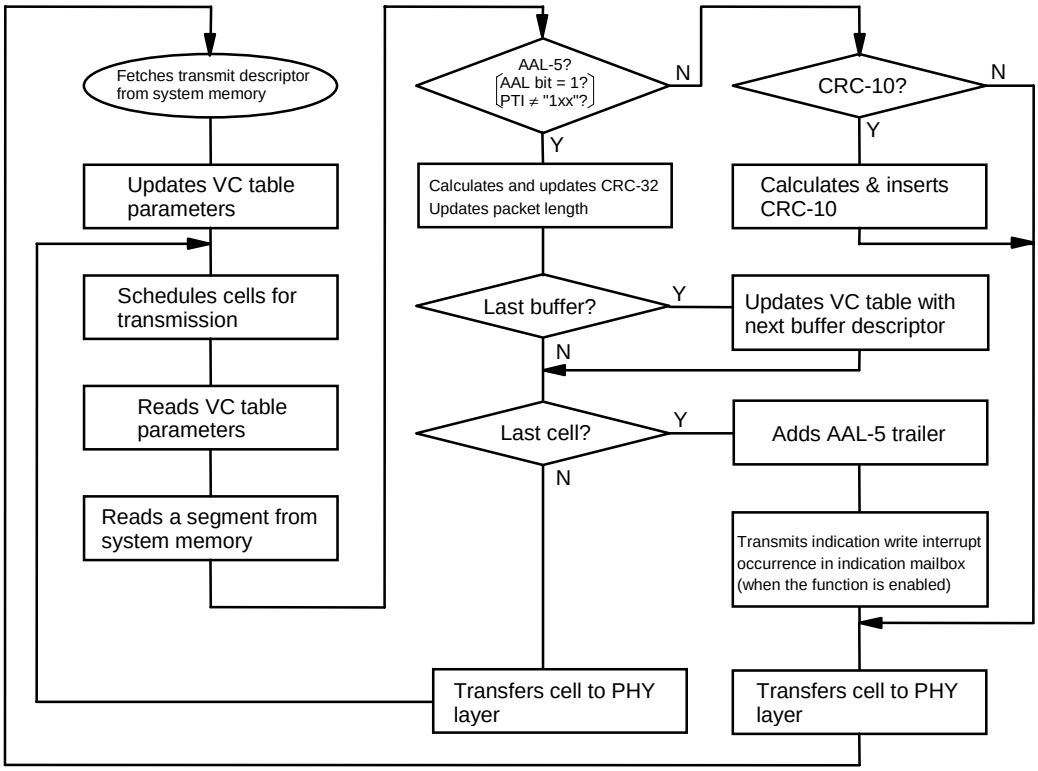
If the current transmit buffer indicates the last buffer, and if the remaining field of the VC table consists of less than 40 bytes, the cell is the last cell of AAL5-PDU.

If the current cell is the last cell of AAL5-PDU and an 8-byte AAL-5 trailer can be added, the μPD98405 adds the trailer, padded with an appropriate number of zeros. If the 8 bytes of the trailer cannot be added to the last cell, a cell containing only information on the trailer, plus padding, is added to the end and transmitted.

For AAL-5 traffic (packet descriptor AAL bit = 1), the transmit machine stores the result of the CRC-32 operation for each segment and the preliminary result of the packet length into the VC table each time it reads a segment from system memory. Once the last segment of the AAL-5 PDU has been read, the final value of CRC-32 and the packet length are inserted into the trailer of the AAL-5 PDU, and the contents of the first word are inserted into the CPCS-UU and CPI fields to generate an AAL-5 trailer.

The transmit machine deactivates the VC once no more valid packet descriptors remain in the transmit queue. The host detects there being no more valid packet descriptors in the transmit queue by locating a vacant packet descriptor with V bit = 0 at the end of the list of the valid packet descriptors.

Figure 5-29. Outline of Transmit Operation Flow



5.4.6 Support of Non-AAL-5 Traffic

The μPD98405 supports a function which does not add the AAL-5 trailer, instead transmitting raw cells to enable the support of non-AAL-5 traffic. The μPD98405 executes transmission as non-AAL-5 traffic when (1) OAM F5 cell is transmitted and (2) raw cell is transmitted.

(1) OAM F5 cell transmission

When the host sets a pattern for the OAM F5 cells (PTI = 1xx) in the PTI field of the packet descriptor, the μPD98405 does not add the AAL-5 trailer. When transmitting OAM F5 cells, the host sets one packet descriptor per OAM F5 cell.

A CRC-10 operation can be inserted into OAM F5 cells. If the C10 bit of the packet descriptor is set to 1, the μPD98405 executes a CRC-10 operation on the 46 bytes and 6 bits of the 48 bytes of each OAM F5 cell segment, and overwrites the last 10 bits of the cell with the result, as a CRC-10 error detection code. When enabling the CRC-10 operation insertion function, therefore, the host must set dummy data (all 0, etc.) in the last 10 bits of the data buffer, so that the last 10 bits of the segment can be overwritten with an error detection code.

When setting a packet descriptor for OAM F5 cell transmission, also note the following:

- **For OAM F5 cell transmission, the "AAL" bit must be set to 0.**
- **Multi-buffer mode cannot be used. Always use single-buffer mode.**
- **For OAM F5 cell transmission, set the size of the transmission buffer to 48 bytes, and set 48 bytes for the "SIZE" field of the packet descriptor.**

(2) Raw cell transmission

When transmitting a non-AAL-5 packet other than an OAM F5 cell, the host must clear the "AAL" bit of the packet descriptor to 0 and set the PTI field to "0xx" (000 to 011), thus indicating a user data cell. The μPD98405 does not execute AAL-5 trailer operation, nor does it add a trailer to the packet, if the "AAL" bit of the packet descriptor is set to 0. The μPD98405 performs raw cell transmission during which it repeatedly reads 48 bytes of a transmission segment from the data buffer, creates a cell, then transmits the cell to the PHY layer device. One packet of transmit data can consist of up to 65,535 bytes and a data buffer can be configured in multi-buffer mode. Note, however, that for raw cell transmission, the host must use a 1-packet transmission buffer of a size that is an integer multiple of 48 bytes. Therefore, in the "SIZE" field of the packet descriptor, set a 48-byte integer multiple. In multi-buffer mode, the total size of the 1-packet transmission buffers that constitute a multi-buffer must be set to a size equal to an integer multiple of 48 bytes. To transmit data of a size other than an integer multiple of 48 bytes, the host must first append dummy data (all zeros) to that data to make its size a multiple of 48 bytes.

If necessary, the host sets the "C10" bit of the packet descriptor to 1 to enable the CRC-10 operation insertion function of the μPD98405. When this function is enabled, the μPD98405 executes a CRC-10 operation on the 46 bytes and 6 bits of the 48-byte segment read from the data buffer of system memory, overwriting the last 10 bits of the cell with the result as an error code. When preparing non-AAL-5 data in system memory, the host must insert dummy data into the 10 bits of the segment units that are to be overwritten by CRC-10.

During raw cell transmission, the last cell is also transmitted according to the pattern specified in the PTI field of the packet descriptor. The least significant bit of the PTI field is thus not automatically changed to "1."

Note the following when performing raw cell transmission.

- **For Raw cell transmission, the "AAL" bit must be set to 0.**
- **For Raw cell transmission, the size of the 1-packet transmission buffer must be set to an integer multiple of 48 bytes (other than 0).**

5.4.7 Issuing a Transmit Indication

The μPD98405 writes a transmit indication into a mailbox for each packet descriptor. The mailbox used for transmission is mailbox 2 or 3, which stores the indication to either of the mailboxes according to the "MB" bits of the packet descriptor set by the host. For a packet for which the transmit indication is masked (while the IM bit of the packet descriptor is 1), however, neither a transmit indication nor an interrupt is issued.

The μPD98405 executes writing of the transmit indication once all the data in a packet has been read. Note that even if the transmission indication has been issued, it does not indicate that transmission to the PHY layer device of that packet has been completed.

The μPD98405 also issues a transmit indication when a Deactivate_Channel command is issued during packet transmission. Even when a packet for which transmit indication is masked is being transmitted, the μPD98405 issues a transmit indication if transmission is interrupted by the execution of a Deactivate_Channel command.

When the transmit indication is stored, the μPD98405 sets the corresponding MM bit of the GSR register to 1, and, provided it is not masked, issues an interrupt.

Caution A transmit indication is issued for each packet for all data of both AAL-5 and non-AAL-5 packets (OAM F5 and raw cell transmission packets), unlike a receive indication.

For an explanation of the contents and processing of the indication, see **Section 5.6**.

The μPD98405 supports the following three types of transmission, which can be selected using a packet descriptor:

Table 5-4. Data Supported by the μPD98405 Transmit Function

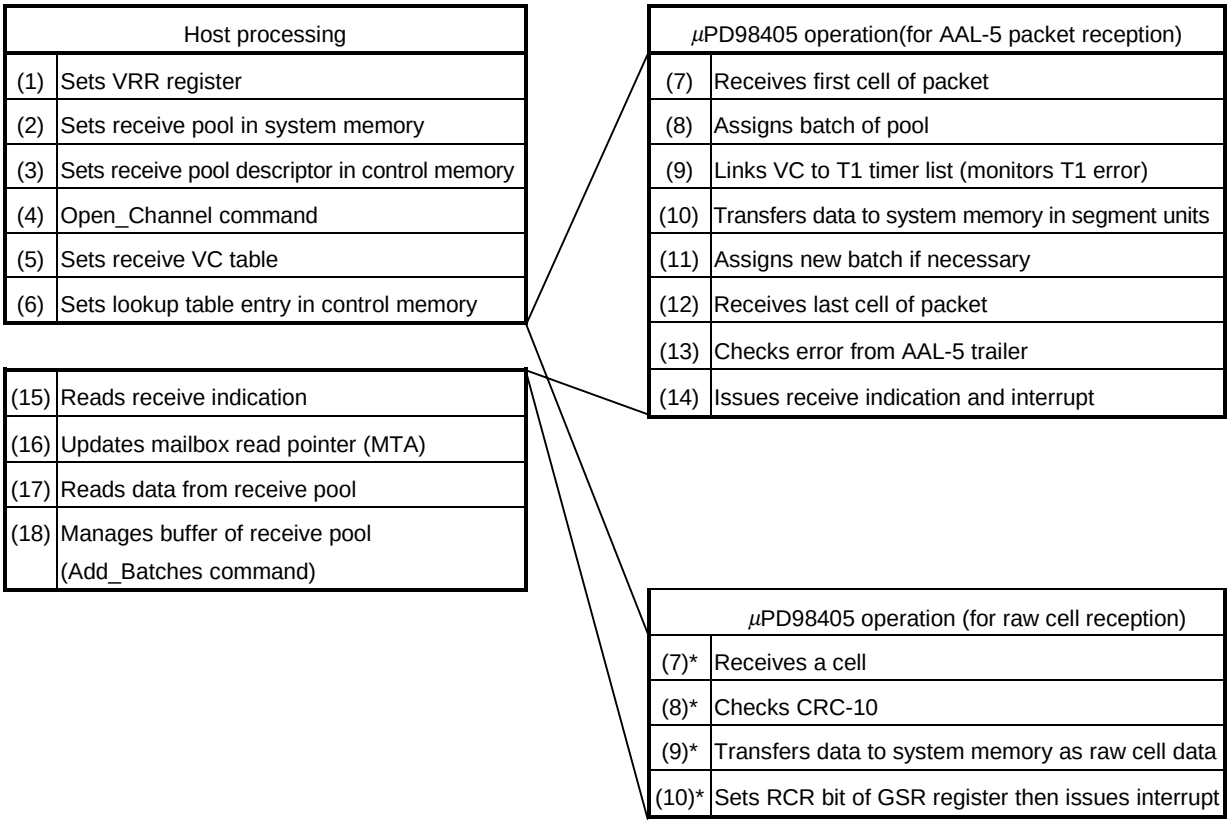
	Setting	Data length	Indication	AAL-5 trailer	CRC-10	Remarks
AAL-5 data	PTI = "0xx" AAL = 1	Up to 65,535 bytes	Issued	Automati-cally added	Cannot be inserted	
Transmission of other than AAL-5 packet (raw cell transmission)	PTI = "0xx" AAL = 0	Up to 65,535 bytes (only a multiple of 48 bytes)	Issued	Not added	Can be inserted	• The CLPM field cannot be set to "01." • The least significant bit of the PTI field is not changed for the last cell.
OAM F5 cell transmission	PTI = "1xx" AAL = 0	48 bytes	Issued	Not added	Can be inserted	• The CLPM field cannot be set to "01." • Only single-buffer mode can be used.

5.5 RECEPTION FUNCTION

5.5.1 Reception Processing Flow

The reception of cells by the μPD98405 is divided into several stages as illustrated below.

Figure 5-30. Outline of Reception Flow



The μPD98405 supports 32K VCs (any combination of receive VCs and transmit VCs). The number of receive VCs actually supported is determined by setting the bits of the VPI/VCI field.

(1) The μPD98405 supports up to 16 bits of the 24 bits of a receive VPI/VCI. The user determines the method to be used to convert the 24 bits of the VPI/VCI to be received into a 16-bit logic code, and sets this method in the VRR register.

(2) Before reception, a receive pool that stores receive data is prepared in system memory.

(3) Information such as the receive pool size of the system memory and address is set in the free buffer pool pointer area of the control memory as a pool descriptor.

(4) The host issues an Open_Channel command for each connection to be received to open a channel (VC). The μPD98405 allocates a block to be used as the VC table from the free block pool of control memory and returns the address of that block to the host.

(5) The host initializes the parameters of the VC table.

(6) Next, the host sets the address of the VC table in the lookup table to actually start reception, and enables reception.

(7) When the μPD98405 receives the first cell of the packet from the PHY layer device, it references the lookup table to determine whether the cell is to be received or discarded.

(8) When reception is enabled, the μPD98405 accesses the VC table and assigns the batch of the pool to that VC.

(9) When the VC T1 timer function is enabled, the μPD98405 also adds the VC to the T1 timer list and monitors timeout.

(10) Each time the μPD98405 receives a cell, it repeatedly transmits the cell to system memory in segment units (when multi-cell transmission is disabled).

(11) If the batch becomes full before the completion of processing, the μPD98405 fetches and assigns a new batch.

(12) Once the last cell of the packet has been received,

(13) Whether an error has occurred is checked from the trailer information contained in the cell,

(14) Receive indication is issued to a specified mailbox, and the host is notified by an interrupt provided it is not masked.

(15) The host reads the receive indication.

(16) Changes the read pointer of the mailbox.

(17) Receives the data from the pool.

(18) The host issues an Add_Batch command to add a batch if the remaining batches in the system memory pool have been exhausted during reception.

The μPD98405 also supports a raw cell reception function, used to receive traffic of other than AAL-5 type. When this function is used, the received cells are transferred to system memory as is, in units of cells. During raw cell reception, once a cell has been received (7)*, CRC-10 is checked (8)* then that cell is transferred to a free buffer for the specified pool as raw cell data (9)*. Processing for raw cell reception is completed in units of cells and no receive indication is stored to a mailbox, unlike AAL-5 packet reception. Each time a cell is stored, the RCR bit of the GSR register is set, after which an interrupt is issued (10)*.

Remark For a VC that uses the ABR service, received RM cells are not stored in system memory. Instead, the μPD98405 processes such cells internally.

The reception processing flow illustrated above merely outlines the reception processing.

5.5.2 Receive Data Structure

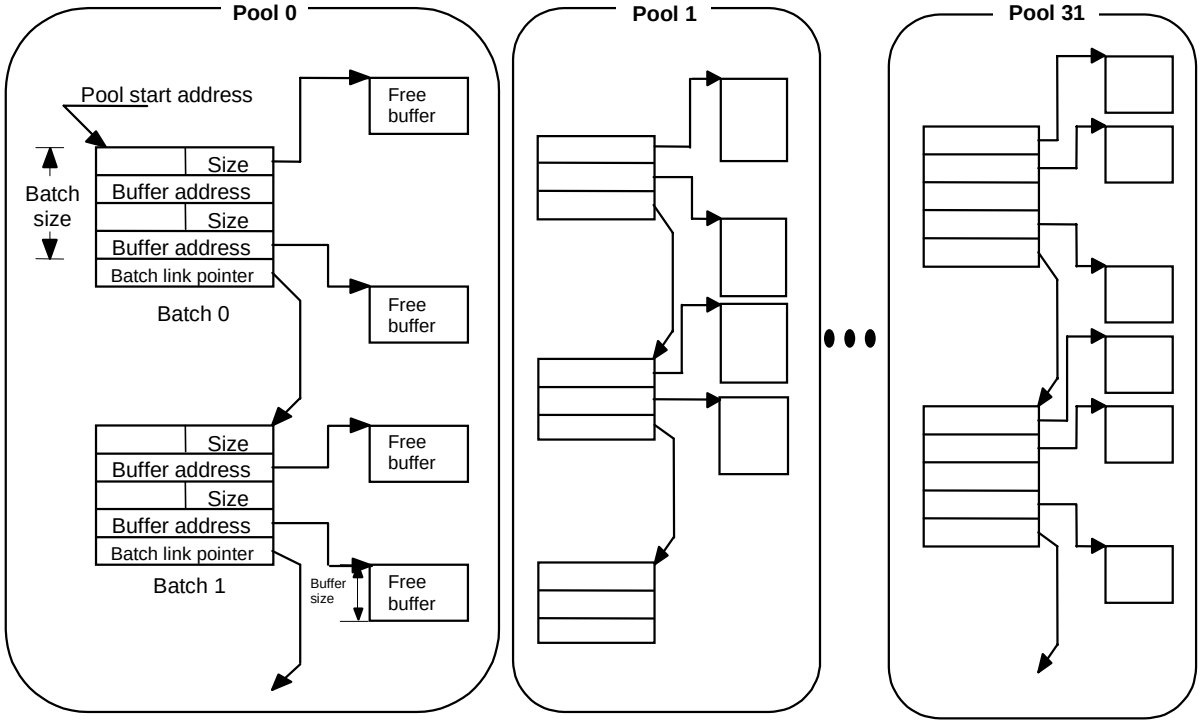
(1) Receive pool

This section explains the structure of the receive pool in system memory.

The μPD98405 stores received data into a pool provided by the host in system memory.

The user must create a pool in system memory according to the rules described below before starting reception processing by the μPD98405. Information relating to the pool in system memory, such as the address and size of the pool, is written by the host to the "receive free buffer pool pointer" area of control memory.

Figure 5-31. Structure of Receive Pool in System Memory

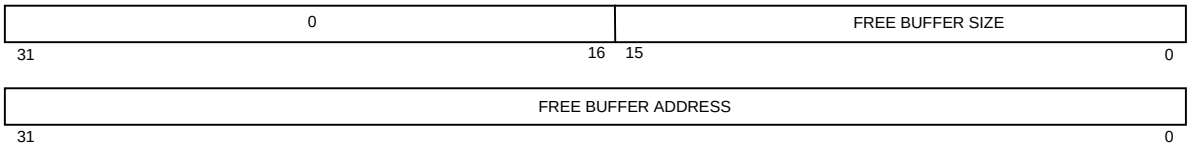


Each pool consists of the following elements.

- Batch: A block that bundles the start addresses and size of the free buffers. The addresses and size of one to 255 buffers can be stored. The number of free buffers bundled by each batch must be the same. A batch must be allocated starting from a 32-bit boundary in system memory. The last word of a batch is used as a link pointer to store the first address of the next batch, such that all batches can be chained.

The formats of the free buffer address, size, and link pointers, which constitute a batch, are as follows:

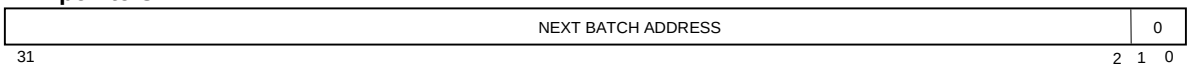
Buffer address and size



FREE BUFFER SIZE: Stores the size (in byte units) of the free buffer which actually stores the receive data. (1 to 64K bytes)

FREE BUFFER ADDRESS: Stores the 32-bit start address of the free buffer which actually stores the receive data.

Link pointers



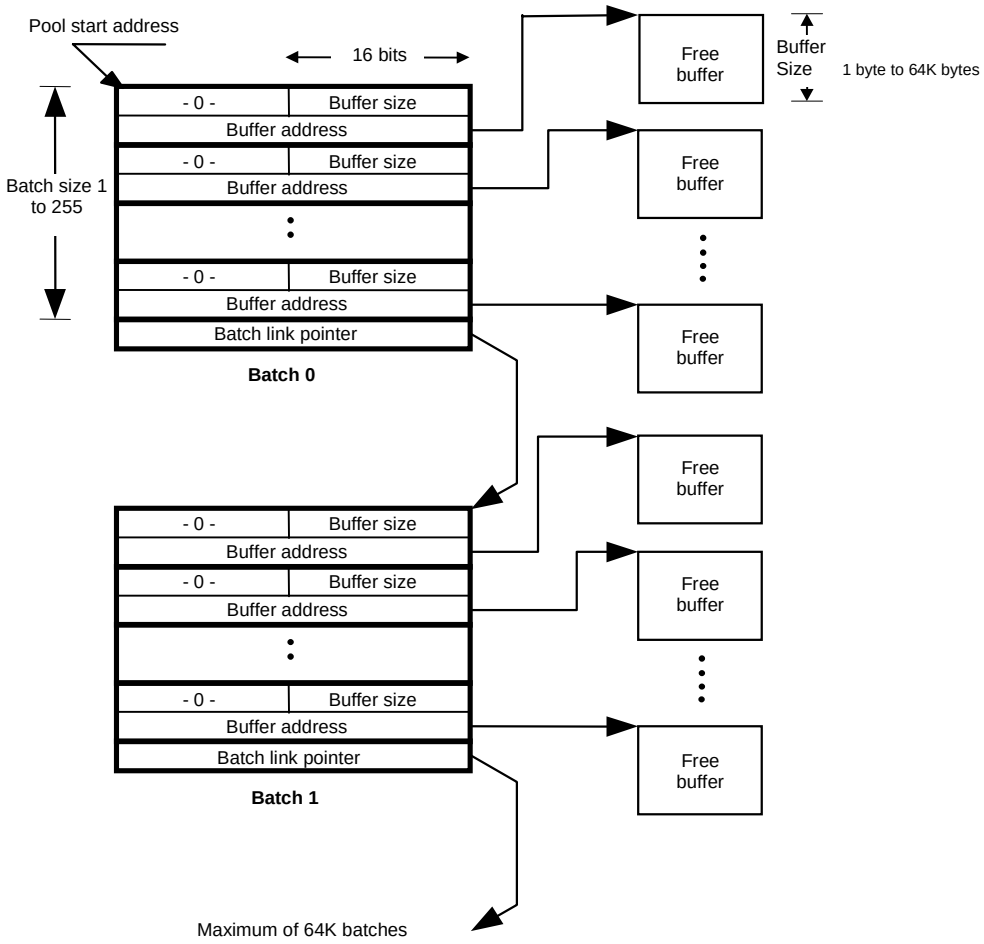
NEXT BATCH ADDRESS: Stores the 32-bit start address of the next batch. Because a batch is allocated starting from a 32-bit boundary, the low-order two bits of the address must be set to "00."

Remark The link pointer of the last batch in the chain may be assigned any address, but it is recommended that the start address of the first batch or the start address of any batch in the chain be specified to protect other areas in system memory.

- Free buffer: The area to which the μPD98405 actually stores the received data. One buffer size can be set in bytes within the range of 1 byte to 64K bytes. The size is set in the batch FREE BUFFER SIZE field. The free buffer can be aligned with a byte boundary in system memory.

★ **Caution Make sure that the buffer total is always 48 bytes or more in one batch. For example, make sure the buffer size is 48 bytes or more when assigning one batch to one buffer.**

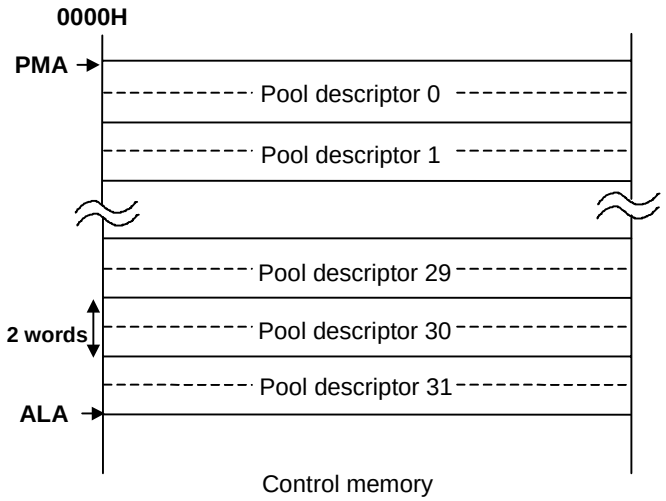
Figure 5-32. Configuration of Pool



(2) Receive free buffer pool pointer

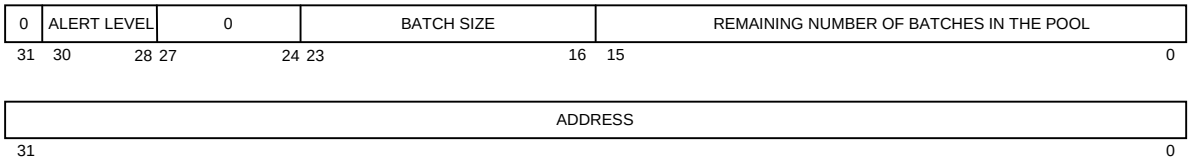
The pools prepared by the host in system memory are numbered 0 to 31. Information relating to each pool, such as its address and size, is set as a 2-word pool descriptor in the "receive free buffer pool pointer" area. This area starts from the PMA address in control memory. The μPD98405 recognizes pool 0, pool 1, pool 2, and so on, starting from the PMA address. When the μPD98405 accesses the descriptor of pool 3, for example, it accesses an address equal to the PMA address added by 6 or 7. Once all the 32 pools have been set, the receive free buffer pool pointer can be a maximum of 64 words wide. By using fewer than 32 pools, the size of the area between the PMA and ALA addresses can be reduced accordingly.

Figure 5-33. Arrangement of Pool Descriptors in Receive Free Buffer Pool Pointer



The format of the pool descriptor is as follows:

Figure 5-34. Format of Pool Descriptor



<1> ALERT LEVEL

This field sets an "alert level" for a pool. If the number for batches remaining in a pool falls to the value set in this field, the μPD98405 sets the corresponding bit of the RQA register and the RQA bit of the GSR register to "1". Provided the interrupt is not masked, a report is also posted to the host using the interrupt.

★ This function can be used on both the AAL-5 type receive pool and the Raw Cell data storage pool.

Setting: When "n" is written to this field, "n x 4" (the number of remaining batches 4, 8, 12, ... 28) is specified. When "000" is specified, this function is disabled, and no report is posted to the host.

<2> BATCH SIZE

This field specifies the number of buffers in one batch located in this pool.

Setting: The end of a batch is always a "batch link pointer." This field specifies the number of buffers n, excluding the batch link pointer. The amount of system memory actually used by one batch is equal to the number of buffers, plus "link pointer," i.e., 2n + 1 words. The value of n must be set to 1 or greater. The μPD98405 recognizes the position of the link pointer from the contents of this "BATCH SIZE" field.

<3> REMAINING NUMBER OF BATCHES

The host writes the number of batches n, prepared in the pool, to this field during initialization. This field is then managed by the μPD98405 and indicates the number of batches remaining in the pool. The μPD98405 subtracts the value in this field each time it fetches a batch from the pool, and adds it each time it receives the Add_Batches command.

<4> ADDRESS

The host sets the first address of the first batch in the pool to this field during initialization. Subsequently, the μPD98405 uses this field as a pointer to the next batch.

(3) Pool for storing raw cell

The μPD98405 uses different pool numbers depending on the type of the data it receives. When AAL-5-type data is received, the user can specify any of pools 0 through 31 for each VC. If raw cell data is received, pools 0 through 7 can be specified. When OAM F5 or RM cell is received, however, the μPD98405 unconditionally stores that cell to pool 0. If the reception of an OAM F5 or RM cell has been set, the user must always set the storing of raw cell data of the OAM or RM cell to pool 0.

Table 5-5. Types of Receive Data and Pools Used

Data type	Pool used
AAL-5-type packet reception	Pool 0 to 31
Raw cell data	Pool 0 to 7
OAM F5 or RM cell data	Pool 0 only

The μPD98405 stores the data of a single raw cell, consisting of 64 bytes, to each free buffer. For a pool used to store raw cell data, therefore, set the size of a free buffer to 64 bytes. If the free buffer size is set to more than 64 bytes, the μPD98405 ignores the area. Even if the free buffer size is set to less than 64 bytes, the μPD98405 assumes the actual buffer size to be 64 bytes.

Remark For a VC that uses the ABR service, received RM cells are not stored into pool 0. Instead, the μPD98405 processes such cells internally.

5.5.3 Receive Channel

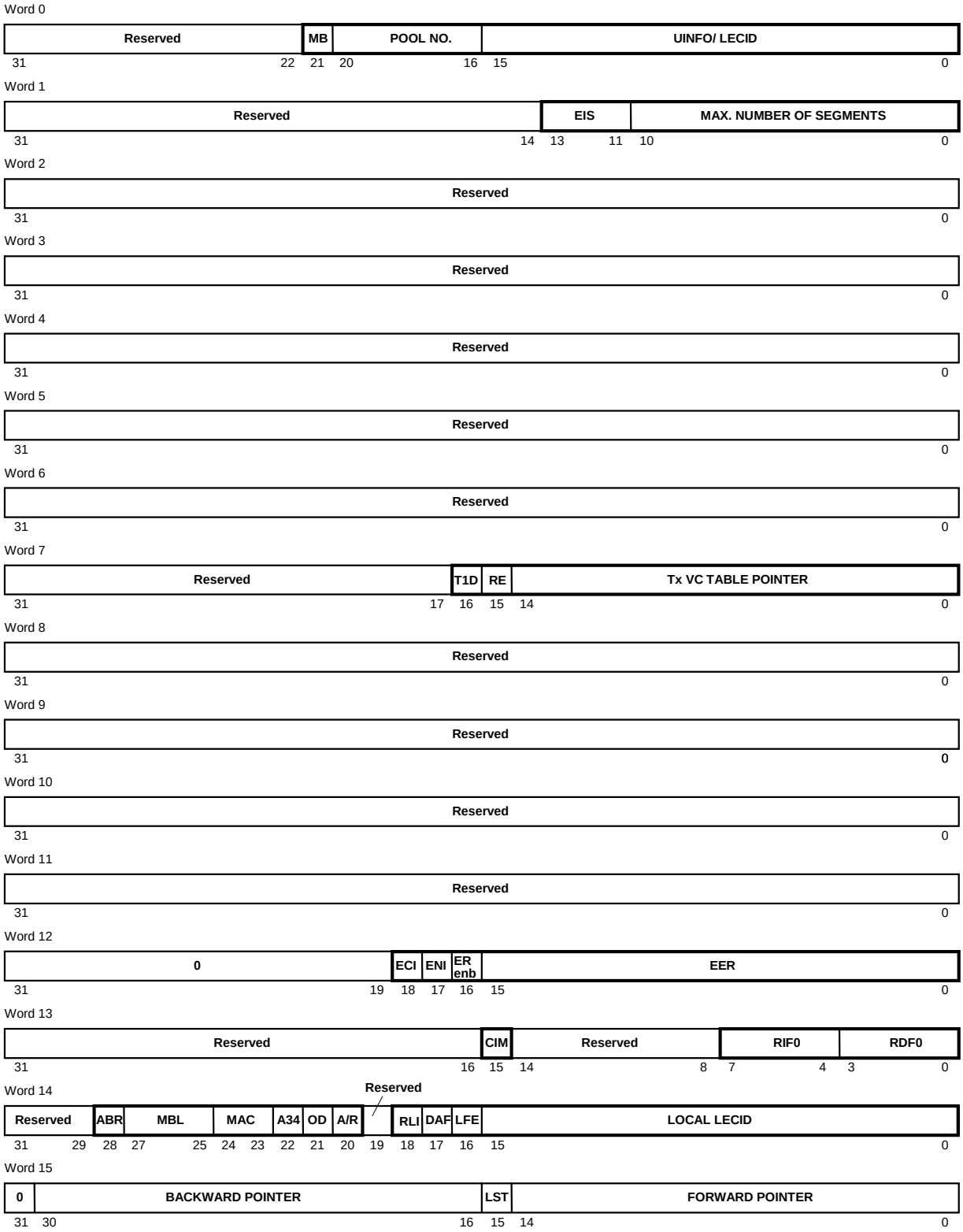
(1) Opening a receive channel

A receive channel is opened when the host issues an Open_Channel command. When the μPD98405 receives this command, it allocates the block indicated by TOS (top of stack) from the free block pool of control memory, and issues a response to the host by using the first address of this block as a command indication. The μPD98405 assigns one block (16 words) using an Open_Channel command. The host sets the allocated block as a receive VC table.

(2) Setting a receive VC table

The host sets a 16-word block, allocated from the free block pool of control memory, as a receive VC table for each VC. The structure of this table is as illustrated in Figure 5-35. The host sets initial values in the areas indicated by thick frames. The host uses the Indirect_Access command to write to the VC table. The areas other than those indicated by thick frames are used by the μPD98405 for reception.

Figure 5-35. Receive VC Table



Remark ☐ : The host sets initial values in those fields indicated by thick frames.

MB Mailbox.

Select a mailbox to store the receive indication in this VC.

1: Mailbox 1

0: Mailbox 0

POOL NO. Pool number.

Select one of the 32 pools for this VC.

UINFO/LECID User information/receive LECID.

If the RLI bit of the receive VC table is set to "0," this field contains user information. The user can set any pattern in this field. The μPD98405 transmits this pattern in a receive indication. If the RLI bit of the receive VC table is "1," the μPD98405 uses this field to store the LECID for a received packet. In this case, the user cannot use this field for user information. Also, the user cannot use UINFO for the OAM/RM/Reserved cell received by the same VC.

EIS Early interrupt size.

To enable the use of the early interrupt function, it is necessary to set the size, in cell units, in this field. The μPD98405 informs the host when it has received the number of cells specified in the EIS field, using an early interrupt. Resetting the EIS field to 000 disables the early interrupt function.

MAX. NO. OF SEGMENTS The maximum number of segments (48-byte payload of the receive cell) that can be contained in one packet.

This field sets the maximum number of segments that can be contained in the packet received by this VC. If the last cell of the packet is not received, despite the current number of segments of the received packet reaching the number of segments set in this field, receive indication including an error status is issued immediately.

★ Do not write 0 to this field.

T1D Disable T1 timer.

This bit is used to disable the T1 timer function of this VC.

1: Disable

0: Enable

RE[Note] Enable rate calculation/turn-around processing based on RM cell reception.

When an BRM/FRM cell is received for this VC, this bit is used to specify whether to perform rate calculation/turn-around processing. If the RE bit is set to "0," the μPD98405 does not perform rate calculation/turn-around processing or access the transmit VC table indicated by the Tx VC TABLE POINTER. This bit is set to enable the use of the ABR service by this VC.

Note These fields are used only by a VC which uses the ABR service. These fields must all be reset to "0" if the ABR bit is set to "0".

Tx VC TABLE

POINTER[Note] Pointer to the address of the transmit VC table.

When an FRM cell is received, the POINTER is used to specify the VC NUMBER (VC table address excluding the low-order 4 bits) of the VC table from which a turn-around BRM cell is transmitted. It is set to enable the use of the ABR service by this VC.

ECI[Note] Flag for setting the CI bit of a turn-around BRM cell.

Setting the ECI bit to "1" enables the host to forcibly set the CI bit of the turn-around BRM cell, to be sent back from this VC, to "1" (for test purposes). While the ECI bit is set to "1," the CI bit of the turn-around BRM cell to be sent back from the VC is held at "1." This bit must be initialized to "0." It is set to enable the use of the ABR service by this VC.

ENI[Note] Flag for setting the NI bit of a turn-around BRM cell.

Setting the ENI bit to "1" enables the host to forcibly set the NI bit of the turn-around BRM cell, to be sent back from this VC, to "1" (for test purposes). While the ENI bit is set to "1," the NI bit of the turn-around BRM cell to be sent back from the VC is held at "1." This bit must be initialized to "0." It is set to enable the use of the ABR service by this VC.

ER enb[Note] Flag for setting the ER bit of a turn-around BRM cell.

Setting the ER enb bit to "1" enables the host to set the ER field of the turn-around BRM cell, to be sent back from this VC, to a value from the EER field of the VC table (for test purposes). The μPD98405 compares the ER value of a received FRM cell with the EER value of the VC table and sets a smaller value in the ER field of the turn-around BRM cell. While the ER enb bit is set to "1," the ER field of the turn-around BRM cell, to be sent back from this VC, is set with the ER or EER value, whichever is smaller. The ER enb bit must be initialized to "0." It is set to enable the use of the ABR service by this VC.

EER[Note] Explicit rate.

This bit is used to set the ER field of a turn-around BRM cell. While the ER enb bit is set to "1," the ER field of the turn-around BRM cell, to be sent back from this VC, is set with the ER or EER value, whichever is smaller. The EER bit must be initialized to "0." It is set to enable the use of the ABR service by this VC.

Note These fields are used only by a VC which uses the ABR service. These fields must all be reset to "0" if the ABR bit is set to "0".

CIM Channel indication mode.

This bit specifies whether the VC NUMBER or VPI/VCI value is to be set as the indication of the end of reception of a packet to be stored into the mailbox.

1: VPI/VCI value (value reduced to a length of 16 bits using the VRR register)

0: VC NUMBER

RIF0[Note] Rate increase factor.

This factor is used to control the increase in the transmission rate due to RM cell reception. RIF is represented as follows:

$RIF = 1/2^{RIF0}$

It is set to enable the use of the ABR service by this VC.

RDF0[Note] Rate decrease factor

This factor is used to control the decrease in the transmission rate. RDF is represented as follows:

$RDF = 1/2^{RDF0}$

It is set to enable the use of the ABR service by the VC.

ABR ABR bit.

This bit specifies whether this VC uses the ABR service.

1: ABR service

0: CBR, VBR, UBR service

MBL Maximum burst size for multicell transfer

The μPD98405 supports multicell transfer only in PCI bus mode. The maximum size supported is 5 cells. The host must set the MBL in cell units. If the MBL is "000" or "001", the multicell transfer function is disabled, and the μPD98405 performs one-cell transfer. If the MBL is "110" or "111," it is recognized as being "101," such that five-cell transfer is supported. In the Generic bus mode, the MBL must be "000."

MAC MAC address filtering offset.

This field is used to set the position of the 48-bit destination address within the packet to use MAC address (destination address) filtering. The position is set as an offset relative to the beginning of the packet. The relationships between the MAC field values and the offsets relative to the beginning of the packet are as follows:

"00": 2 bytes (Ethernet™ LAN Emulation Data Frame)

"01": 4 bytes (Token-Ring LAN Emulation Data Frame)

"10": 6 bytes

"11": 10 bytes

Note These fields are used only by a VC which uses the ABR service. These fields must all be reset to "0" if the ABR bit is set to "0".

A34 AAL-3/4 bit.

When the A34 bit is "1," this VC is used for reception of the raw cell of the AAL-3/4 packet. The μPD98405 checks the first two bits (ST field) of the cell's payload. The μPD98405 issues an RCR interrupt only if the received cell contains "01" or "11" in its ST field. An RCR interrupt will not occur in cell units. When this bit is set to "1," the A/R bit must be reset to "0."

OD OAM reception/discard.

When an RM or OAM F5 cell in its PTI field and pattern "1xx" arrives at this VC, the OD bit is used to specify whether to accept it.

1: Ignores and discards OAM F5 or RM cells.

0: Accepts OAM F5 or RM cells.

If the use of the ABR service has been set for this VC (the ABR bit is set to "1"), RM cells are processed as RM cells for ABR. The μPD98405 will not store RM cells into a pool.

A/R AAL-5 reception/raw cell reception.

This bit specifies whether a cell arriving at this VC is to be processed as an AAL-5 or raw cell.

1 - Received as an AAL-5 cell

0 - Received as a raw cell

RLI Indication of receive LECID.

This bit specifies whether to indicate LECID reception by using a receive indication.

1 - Receive LECID reported using an indication

0 - Receive LECID not reported using an indication

When this function is enabled, the μPD98405 stores a receive LECID into the UINFO/LECID field of the VC table and indicates this in the UINFO/LECID field of the indication; subsequently the UINFO/LECID field cannot be used for user information.

DAF Enable destination address filtering.

This bit specifies whether to use the destination address filtering function.

1 - Enable

0 - Disable

When this function is enabled, the μPD98405 executes destination address filtering for LAN emulation by setting the MAU, MAL, HTU, and HTL register addresses.

LFE Enable receive LECID filtering.

This bit specifies whether to use the receive LECID filtering function.

1 - Enable

0 - Disable

When this function is enabled, if a received packet has the same LECID as that set in the LOCAL LECID field, all cells in the packet are discarded.

LOCAL LECID Local LECID.

When the receive LECID filtering function is enabled, the μPD98405 compares the value in this field with the receive LECID. If they match, all cells in the packet are discarded. If the LFE bit is set to "0," this field has no meaning.

BACKWARD POINTER "VC NUMBER" of the VC linked to the T1 list prior to this VC.

LST This bit is set to "1" if the VC is linked to the end of the T1 list.

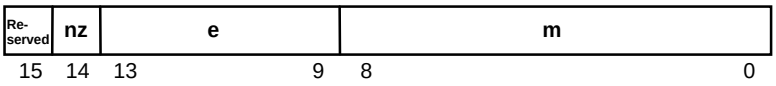
FORWARD POINTER "VC NUMBER" of the VC linked to the T1 list subsequent to this VC.

Remarks 1. Those fields indicated as "Reserved" are reserved for the μPD98405. Do not attempt to modify these fields except for initialization. Reset all of these fields to 0 at initialization.

2. Do not modify Word 15, even at initialization, for open VC tables. Word 15 of the receive VC table holds the pointers and flags required to enable the μPD98405 to manage the VC table. If Word 15 is modified by an external host, it becomes impossible for the μPD98405 to manage correctly.

3. The rate field (EER) is represented as follows:

Rate = 2^e*(1 + m/512)*nz cells/s



4. See also **Section 5.8.4** for details of the ABR parameter.

(3) Status transition of receive channel

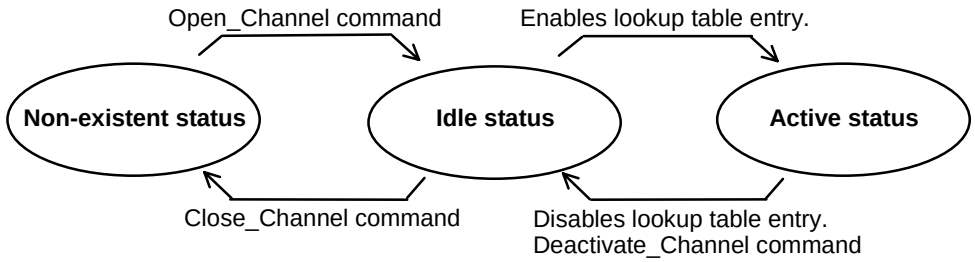
The receive channel can assume one of three statuses: non-existent, idle, and active. The host opens a channel by issuing an Open_Channel command. When the μPD98405 receives this command, it reports the address of the VC table to the host as a command indication from the free block pool in control memory. Next, the host writes appropriate parameters (such as the pool number used, AAL-5 processing/raw cell processing, and the maximum allowed segment numbers) to the allocated block by using the Indirect_Access command. Thus, this block becomes a receive VC table, and the channel enters idle status.

To activate the channel, enter "VC NUMBER" and set the enable bit in the lookup table. For an explanation of lookup table specification, see **Section 5.5.4**. As a result, the channel enters the active status and, when the μPD98405 receives a cell that has the corresponding VPI/VCI from a PHY layer device, it starts receive processing. The channel remains in this status as long as the enable bit of the lookup table entry is set to 1. The channel subsequently returns to the idle status when the enable bit of the lookup table entry is disabled and the Deactivate_Channel command is issued.

To disable this channel, the host disables the lookup table and issues the Deactivate_Channel command, returns the channel to the idle status, and issues the Close_Channel command. This returns the VC table to the free block pool, and results in the channel no longer existing, such that the non-existent status is set.

The Deactivate_Channel command must be issued at least 72 clocks after the lookup table has been disabled. Create this timing by issuing the NOP command twice.

Figure 5-36. Receive Channel Status



(4) Closing a receive channel

To terminate the use of a channel, the host issues a Close_Channel command while the channel is in the idle state. The channel is placed in the idle state by first disabling the lookup table entry and issuing an NOP command twice, then issuing a Deactivate_Channel command.

When the host issues a Close_Channel command, a Close_Channel indication is returned as a response. If the indication includes the VC NUMBER of the channel to be closed, it means that execution of the Close_Channel command was successful. The μPD98405 returns the VC table to the free block pool. Consequently, the channel cease to exist and therefore enters the non-existent state.

A Deactivate_Channel command must be issued for any VC for which a Close_Channel command has not been issued. Even if two or more VCs are to be closed, it is impossible to issue Deactivate_Channel commands continuously.

If the host issues a Close_Channel command to a channel for which a Deactivate_Channel command has been issued to set the channel in the idle state, a Close_Channel indication may be returned in response, indicating a failure in closing the channel. This is because the channel is in the idle state, but processing of those cells in the internal receive FIFO has not yet been completed. In this case, the μPD98405 is performing internal processing related to the channel and does not allow the VC table to be released. If the host receives a close failure indication, it must continuously issue Close_Channel commands until one is accepted. Once a receive indication corresponding to the Deactivate_Channel command is issued, the μPD98405 will accept a Close_Channel command.

5.5.4 Setting Receive Lookup Table

The lookup table exists in control memory and is used to map the VPI/VCI to be received according to the receive VC table. The lookup table always starts from 0000H in control memory, and its size is determined by the setting of the VRR register to be received, as well as the pattern of VPI/VCI to be received.

The μPD98405 internally converts the 24 bits of the VPI/VCI included in the receive cell into a 16-bit logic code. This conversion is performed according to the setting of the "SHIFT" and "MASK" fields of the VRR register. Based on the converted logic code, whether the cell of the VPI/VCI is to be received is set in the receive lookup table entry, by means of the following procedure.

<1> The VPI is shifted to the VCI side by an amount equal to the number set in the "SHIFT" field of the VRR register. At this time, the VPI can be shifted by up to 15 bits. When it has been shifted by 8 bits or more, 0 is added to the high-order bit positions.

<2> The 16 bits created in **<1>** and the contents of the "MASK" field of the VRR register are ANDed.

<3> The high-order 15 bits of the ANDed 16 bits are part of the address of the receive lookup table.

<4> The least significant bit ("L" in Figure 5-37) indicates the high-order 16 bits or low-order 16 bits of the word corresponding to the address. If the least significant bit is "0", the high-order 16 bits are indicated. If it is "1," the low-order 16 bits are indicated.

<5> The host stores a 16-bit code that combines the enable bit ("ENBL" bit) and the "VC NUMBER" of the VC to the lookup table address created in this way.
When the enable bit is set to "1," the VC enters the active status.

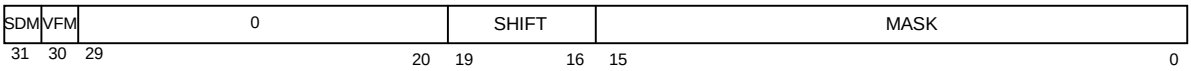
When the μPD98405 receives a cell from a PHY layer device, it creates the address of the receive lookup table in the same manner as described above, in accordance with the VPI/VCI in the header of the receive cell, and the setting of the VRR register. The μPD98405 accesses the lookup table entry from that address, receiving cells if the enable bit is "1," or discarding cells if the enable bit is "0." To receive cells, the address of the corresponding VC table is created from the "VC NUMBER" stored together with the 16-bit code, and the setting to be used for processing is either confirmed or updated.

The size occupied by the lookup table in control memory is determined from the number of VPI/VCI patterns to be received. The capacity of this table must be sufficient to store the specified number of lookup table entries in the VPI/VCI to be received.

Caution "VC NUMBER" is not a physical address that indicates the beginning of the VC table in the free block pool. Instead, it is a code obtained by shifting the low-order 4 bits of the physical address.

When reducing the VPI/VCI from 24 to 16 bits, the μPD98405 can select whether to discard or receive the reception packet in which the area ignored by "SHIFT" has a value other than 0. This function can be specified by the VFM it of the VRR register. For example, when VFM = 0 and SHIFT = 4, the μPD98405 discards the reception packet in which the high-order 4 bits of the VPI or VCI have a value other than 0. The configuration of the VRR register and a VPI/VCI reduction example are shown below.

VRR register - Address: 301H

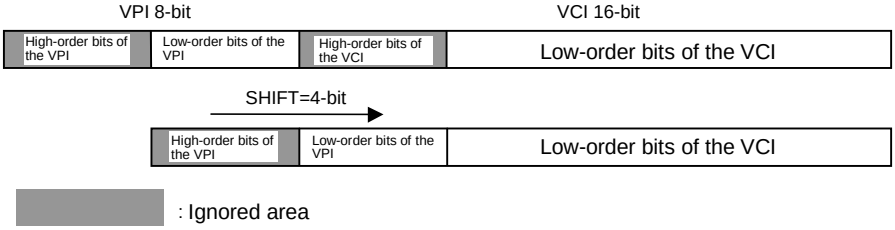


VFM : VPI/VCI filtering mode

0 : Enables the VPI/VCI filtering function (discard mode)

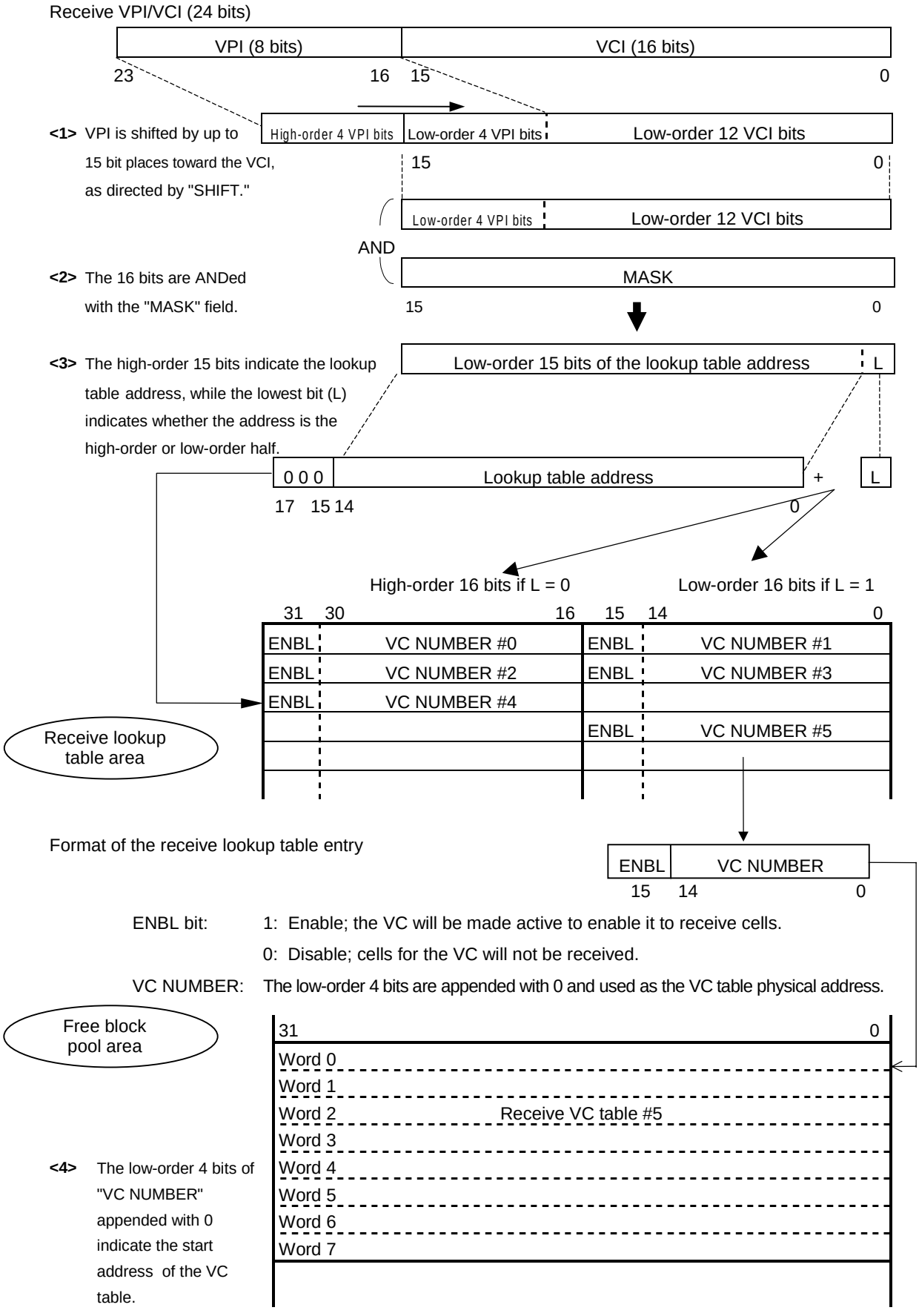
1 : Disables the VPI/VCI filtering function (receive mode)

VPI/VCI reduction example (when SHIFT = 4)



★ **Caution The VPI/VCI filtering function does not work on the area that is ignored using the mask function.**

Figure 5-37. Receive Lookup Table (When SHIFT = 4)



5.5.5 Receive Operation

(1) Receive operation

The μPD98405 receives cells from the PHY layer, and stores them to the receive FIFO. The receive FIFO has a capacity of 96 cells. If the VPI/VCI pattern of the header of the incoming cell consists entirely of zeroes, the cell is recognized as being an invalid cell. It is not stored to the receive FIFO, and instead is discarded.

If the cell is not an unassigned or idle cell, an address that indicates the lookup table in control memory is created from the 24-bit pattern of the VPI/VCI, in accordance with the setting of the "SHIFT" and "MASK" fields of the VRR register.

The entry of the lookup table indicating the created address is read. If the enable bit (ENBL bit) is set to "1," the cell is stored to the receive FIFO and processing continues. If the ENBL bit is set to "0," indicating that mapping to the lookup table is not performed, the cell is discarded.

When the ENBL bit = 1, the VC table of the free block pool is read from the "VC NUMBER" stored in the lookup table together with the ENBL bit, and the pool number or address information of the system memory to be stored is obtained.

If the cell is the first cell of a packet to which no batch of the receive pool is allocated, or if the current batch has been exhausted, the μPD98405 fetches a new batch from the "ADDRESS" field of the pool descriptor in the receive free buffer pool pointer area of control memory.

Once a new batch has been fetched, the value of the "REMAINING NUMBER OF BATCHES IN THE POOL" field of the pool descriptor is decremented by one, and the "ADDRESS" field is changed to indicate the first address of the next batch.

The μPD98405 transfers a segment (48-byte payload of the receive cell) to the first buffer in system memory by means of DMA. The free buffer address of the fetched batch is stored to the VC table, and is updated each time the μPD98405 transfers a segment. The pool descriptor is accessed whenever a new batch is necessary.

If the cell is the first cell of a packet, the T1 time stamp is stored to the VC table, after which the VC table is added to the T1 link list (only when the T1 timer function of the VC is enabled).

Each time the μPD98405 receives a cell of the VC, it transfers the cell to system memory in units of segments, and updates the free buffer address. It also calculates the CRC-32 and packet length for each segment, and updates the process in the VC table.

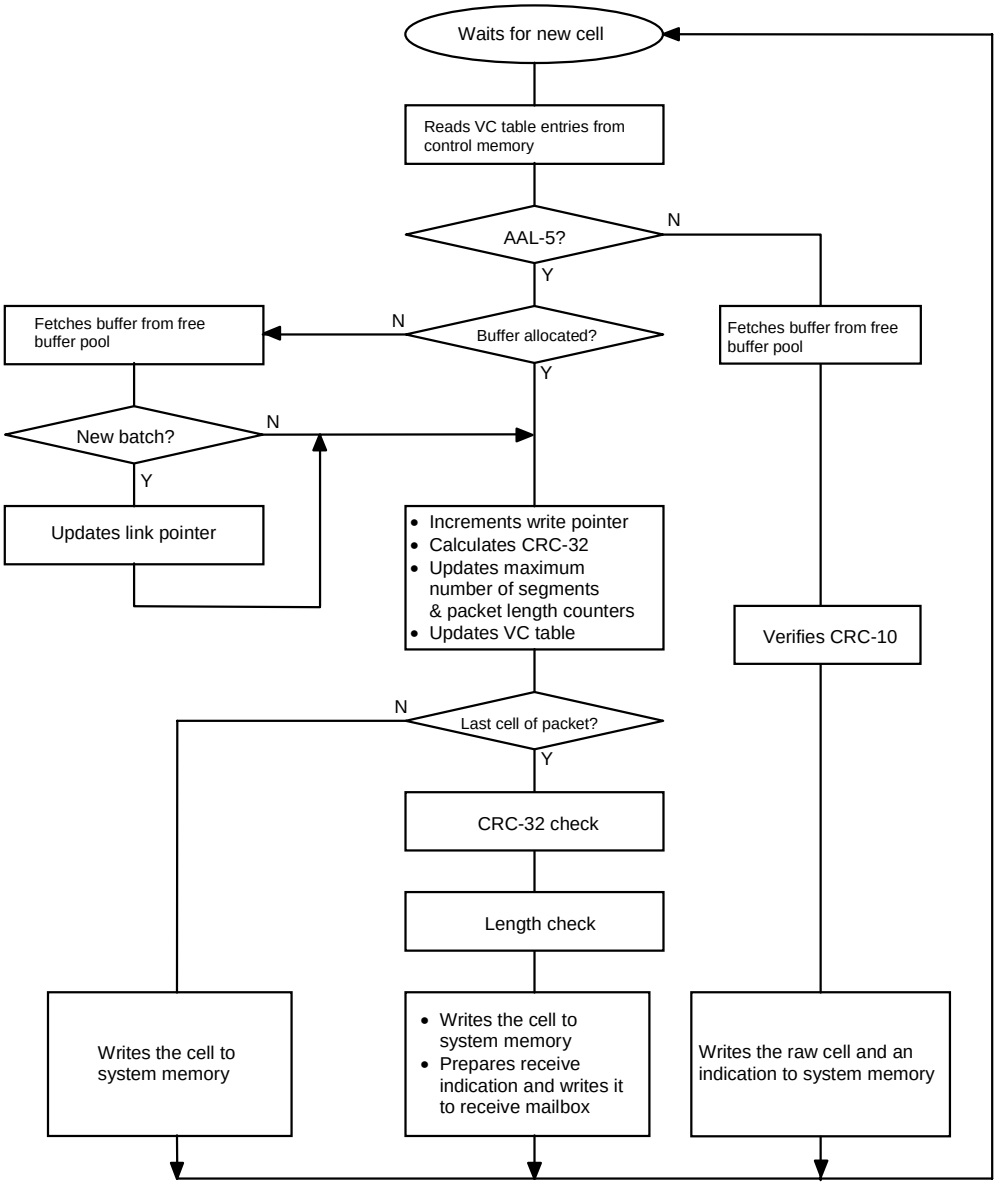
If the free buffer used by the VC becomes full before the last cell of the packet has been received, the μPD98405 fetches the address of a new free buffer from the batch in system memory. When the μPD98405 has exhausted that batch, it fetches a new batch from the pool descriptor.

If one packet straddles two or more batches, the μPD98405 overwrites the link pointer of the batch it has used to modify the chain.

When the μPD98405 has received a packet for which the LSB bit of the PTI field of the cell header is set to 1, it recognizes that cell as being the last cell, and compares the result of calculating CRC-32 and the number of cell counts with "CRC-32" and "Length" in the AAL-5 trailer of the last cell.

Next, the μPD98405 stores receive indication to the mailbox set as a VC table. If an error is found, its status information is also included. An interrupt will occur provided it is not masked.

Figure 5-38. Receive Operation Flow



(2) Storing receive data

This section explains the procedure by which the μPD98405 stores receive data to system memory, and by which the host is operated. The procedure used by the μPD98405 to use a pool differs depending on whether the pool is for AAL-5-type packet data or for raw cell data.

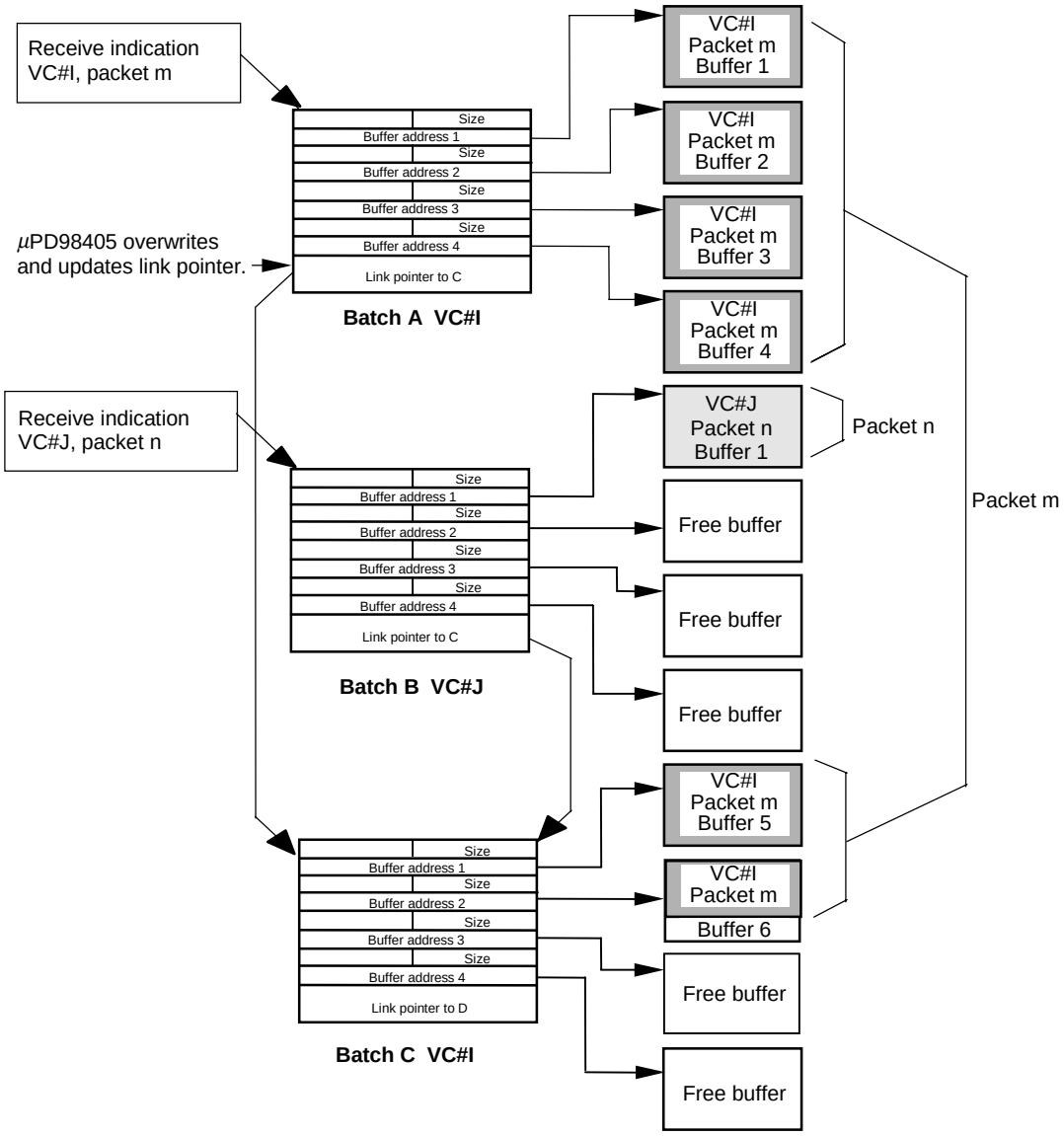
(a) Pool used to store AAL-5-type packets

The user can store each VC to one of the 32 pools by setting VC table "POOL NO.". One pool can store the receive packets for two or more VCs. For AAL-5 traffic, the VC fetches free buffers in batch units. Therefore, each packet always starts with a new batch. To store a received packet, the VC uses two or more free buffers from one of the batches. Sometimes all the free buffers of one batch are used, while in other cases free buffers straddling two or more batches are used. If the stored packet straddles two or more batches, the μPD98405 overwrites the link pointer of the batch by means of DMA, and updates the link information.

An example of AAL-5 traffic reception is shown below.

The pool shown in Figure 5-39 has batches A, B, C, and so on, each batch having four free buffers. VC#I and VC#J are stored to the same pool.

Figure 5-39. Example of Receive Data Configuration



- The first cell of packet m of VC#I is received. The μPD98405 reads the pool descriptor to fetch a batch. At this time, batch A is allocated to packet m of VC#I because the first address of batch A is stored to the pool descriptor.
- Because batch A has been exhausted, the μPD98405 updates the pool descriptor so that it indicates the beginning of batch B.
- While packet m is being received, the first cell of packet n of VC#J is received. The μPD98405 allocates batch B to packet n in the same manner as above.
- VC#I fills the four free buffers of batch A before the packet has been entirely received, and newly allocates batch C. At this time, the μPD98405 overwrites, by means of DMA write, the link pointer of batch A that points to batch B so that it indicates the beginning of batch C, and updates the link information to "from batch A to batch C."

- To store all the packets of VC#I, two free buffers from batch C are required. After the μPD98405 has stored all the data of packet m to the free buffers, it creates the receive indication for packet m. To this indication, the first address of batch A is stored as the start address of the packet, along with the packet size in cell units. The host processes the receive data on the basis of this information and the updated link pointer.
- Packet n only requires one free buffer of batch B. To the receive indication that is issued after packet n has been stored, the first address and size of batch B are returned.

The host can specify an "alert level (ALERT LEVEL)" to the pool descriptor to manage the receive pool. The μPD98405 decrements the number of batches remaining in the pool, "REMAINING NO. OF BATCHES IN THE POOL," each time it consumes a batch. If the number of batches falls to a value less than that specified for ALERT LEVEL, the μPD98405 sets the corresponding bit of the RQA register to 1, sets the RQA bit of the GSR register, and issues a report to the host by using an interrupt. In response, the host issues the Add_Batch command to the pool to add a new batch.

When a new cell is received and is about to be transferred to the pool, if the value of "REMAINING NO. OF BATCHES IN THE POOL" of that pool is already 0, a receive queue underrun occurs. The μPD98405 sets the corresponding bit of the RQU register to 1, sets the RQU bit of the GSR register, then issues an interrupt if it is not masked.

The initial information for the receive pool is written by the host, using the Indirect_Access command, to the pool descriptor in control memory. Subsequently, the host uses the Add_Batches command to add batches to the pool. When the μPD98405 receives the Add_Batches command, it updates the contents of the pool descriptor. Note that the host does not directly update the value of the pool descriptor in control memory.

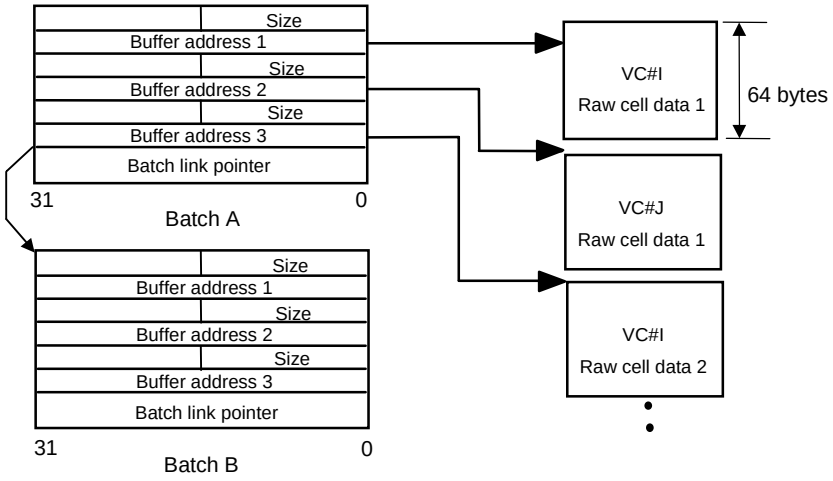
(b) Pool used to store raw cell data

Unlike the pool used to store AAL-5-type traffic, the pool used to store raw cell data does not allocate a batch to each packet. One free buffer is allocated to each item of raw cell data. When the μPD98405 receives a cell, it sequentially fetches the first free buffer of the first batch of the pool that stores the cell, and stores the raw cell data to the buffer. When storing raw cell data, the μPD98405 does not store a receive indication, unlike when storing an AAL-5 packet. Instead, each time it stores a single raw cell, the μPD98405 sets that bit corresponding to the pool, among bits RCR7 to RCR0 of the GSR register, to 1, then notifies the host of reception by issuing an interrupt, provided it is not masked.

Because the μPD98405 does not notify the host of the address of the free buffer in which the data has been stored, the host must store the address of the free buffer which was used previously. A single pool can be specified to store raw cell data for two or more VCs. In such a case, cells are stored in free buffers in the order in which they are received, regardless of the VC. For a pool used to store AAL-5 packets, the "ADDRESS" field of the pool descriptor stores the start address of the batch to which the μPD98405 will store the next data. For a pool used to store raw cell data, however, the "ADDRESS" field stores the address of the next buffer address field in the batch. If all free buffers in the batch have been used up, the μPD98405 will store the raw cell data in the next batch.

Figure 5-40. Structure of Raw Cell Data Storing Pool

(When specified to store raw cell data of VC#I and VC#J in the same pool)



For an explanation of the raw cell data, see **Section 3.3.3**. An AAL-5 packet cannot be stored to a pool specified to store raw cell data. Note that a single pool cannot contain more than one type of data.

(3) T1 timer (reassembly timer)

The μPD98405 supports a function for specifying the time required for one packet to arrive by using the hardware watchdog timer. This function is called the T1 timer (reassembly timer) function. The user sets the time allowed for the last cell to arrive, after the first cell of the packet to a register. The μPD98405 monitors whether packet reception is performed within the set time. If the time is exceeded, reception of that packet is stopped, and a T1 error is reported to the host as the receive indication.

The μPD98405 is provided with the following two registers for the T1 timer function:

- TSR register: 32-bit counter which counts up at the system clock cycle. The μPD98405 references this counter to obtain the current time. This counter starts counting immediately after a reset.
- T1R register: Register in which the host sets the time allowed to receive a single packet (T1 time). The time is defined using the high-order 16 bits of a 32-bit value. The time value is set in units of 65,536 system clock cycles (see the description of the TSR register, above). The low-order 16 bits are set to 0000H and are not used.

Note that the actual time differs even if the value set for T1R is the same, depending on the system clock of the μPD98405.

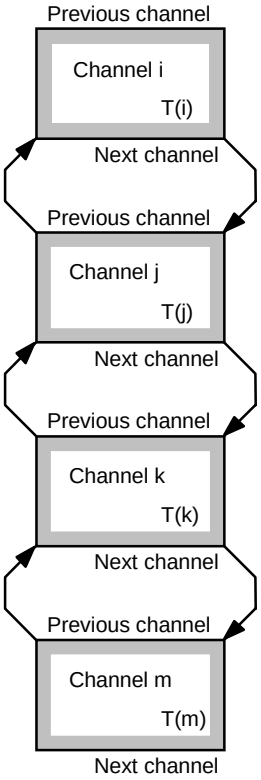
To monitor the T1 time, a link list created by using "FORWARD POINTER" and "BACKWARD POINTER" at the seventh word of the VC table is used. These pointers store the "VC NUMBER" of the VC. Each time the first cell of a new packet arrives, the μPD98405 writes the contents of the TSR register to the "T1 TIME STAMP" field of the VC table. In addition, the VC table is added to the end of the link list by correcting "FORWARD POINTER" and "BACKWARD POINTER" of the VC table and the corresponding pointers of the previously received VC. In other words, the link list starts with the "VC that started reception first" and ends with the "VC that started reception most recently," and the list is enabled. Using this list, the μPD98405 has only to check the "contents of the TSR register ≥ T ("T1 TIME STAMP")" of the "VC that started reception first." Once the last cell of the packet has arrived, the μPD98405 removes the VC table of the VC from the link list.

For normal operation, the T1 time is set so that the packet can be received correctly.

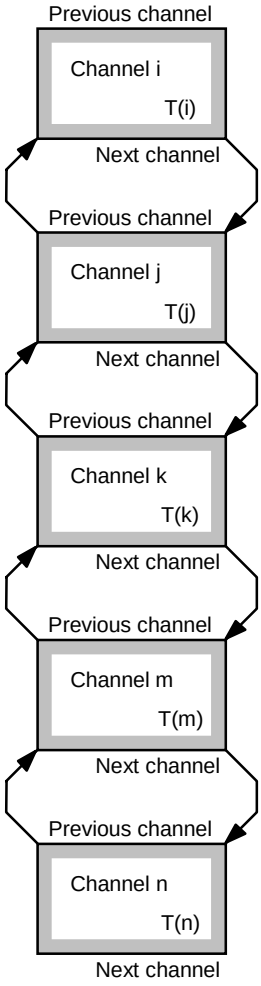
Remark The host can disable the T1 timer function for individual VCs separately. The T1 timer function is disabled for a VC for which the T1D bit of the receive VC table is set to 1. The μPD98405 does not monitor the T1 timer for this VC. Also, the VC is not linked to the T1 link list. The T1 timer disable function is useful mainly for VCs that use the ABR service, in which it may prove impossible to estimate the T1 time when packet reception ends due to changes in the rate.

Figure 5-41. Reassembly Timer (T1)

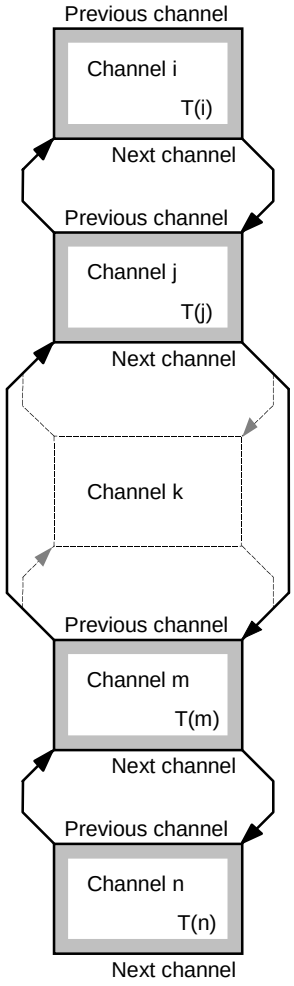
(a) Current status of T1 list



(b) Start of PDU in channel n
Channel n added to the list
T(n) = Current time + T1 value



(c) End of PDU in channel k
Channel k removed from the list



(4) AAL-5 packet receive error detection

The μPD98405 checks for errors in the assembly of packets based on the AAL-5 trailer information, either during reception or at the end of reception. If an error is detected, the μPD98405 reports the error type, and the start address and size of the data which was transferred to system memory prior to the occurrence of the error, to the host by using the receive indication stored in the mailbox.

If the host receives a receive indication containing an error status, it executes appropriate processing and discards the packet containing the error.

The following errors may be reported by a receive indication.

(a) Free buffer underflow

After reception of an AAL-5 packet, the μPD98405 transfers the segment obtained from a received cell to system memory. If the free buffer does not contain free space, however, the μPD98405 discards the cell. If the discarded cell is an intermediate cell, or the last cell, of the packet, the μPD98405 suspends packet reception then issues a receive indication for reporting a free buffer underflow error. If a free buffer underflow occurs, an RQU interrupt for the relevant pool occurs simultaneously (see **Section 7.2 (4)**). The μPD98405 discards all remaining cells, up to the last cell in this packet.

If the discarded cell is the first cell of the AAL-5 packet, no receive indication is issued to report free buffer underflow. Only an RQU interrupt is issued to report that no free buffer is available in the pool.

To enable reception, the host must add, using the Add_Batches command, a batch to the pool for which an RQU interrupt has been issued.

(b) Receive FIFO overrun

During the reception of an AAL-5 packet in DROP mode (GMR register DR bit = 0), if the receive FIFO, which can store 96 cells, is full upon the reception of a cell of the packet, the μPD98405 discards that cell. The μPD98405 discards all remaining cells, up to the last cell in this packet.

If a receive FIFO overrun occurs, the corresponding receive indication is issued in the following two ways:

- If FIFO overrun is cleared while the cells of a packet that has an error are arriving, the μPD98405 issues an indication to report the receive FIFO overrun once the last cell of the packet has arrived.
- If a FIFO overrun is not cleared before the last cell of the erroneous packet arrives, the μPD98405 does not issue an indication to report the receive FIFO overrun.

(c) "MAX. NUMBER OF SEGMENTS" violation

This error occurs if the last cell of the packet has not yet been received, despite the number of received cells reaching the value of "MAX. NUMBER OF SEGMENTS," set by the user in the VC table. The data received prior to "MAX. NUMBER OF SEGMENTS" being reached is stored in system memory. A receive indication is issued upon the reception of the cell next to that at which "MAX. NUMBER OF SEGMENTS" was reached. The μPD98405 discards all remaining cells, up to the last cell in this packet.

If, for example, the user has set 100 for "MAX. NUMBER OF SEGMENTS," the last cell must be received before 100 cells are received. If the last cell has not yet been received when 100 cells have been received, a receive indication for reporting a "MAX. NUMBER OF SEGMENTS" violation is issued upon the reception of the 101st cell. The μPD98405 discards the subsequently received cells, from the 101st to the last cells.

(d) CRC-32 error

Upon the completion of the transmission of all packet data to system memory, if the verification of the CRC-32 result and the CRC-32 field in the received trailer produces a mismatch, notification of this mismatch is posted.

A CRC-32 error is appended to the AAL-5 trailer, the last part of a packet to be received. Therefore, the μPD98405 does not detect an error until all of the packet data has been received and stored into the receive buffer. Therefore, even if a packet causes a CRC error, all of the data for that packet will be stored into the receive buffer.

If the AAL-5 trailer check reveals that a received packet contains both a CRC-32 error and “Length” error, the posted error status will indicate the reception of a CRC-32 error.

(e) User abort

This error is reported if the "Length" field included in the receive trailer is found to be "0" when the field is checked after all the packet data has been transferred to system memory. In this case, the received packet is usually discarded as an invalid packet to the host.

(f) "Length" error

Once all the data of a packet has been transferred to system memory, the μPD98405 checks the calculated packet length and the "Length" field included in the receive trailer. A "Length" error is reported if either of the following conditions is satisfied:

- ("Number of receive cells x 48 bytes" - "Length value" in trailer") > 55 bytes
- ("Number of receive cells x 48 bytes" - "Length value" in trailer") < 8 bytes

(g) T1 timeout

A T1 error occurs if the last cell does not arrive within the T1R time, set by the user, of receiving the first cell of the receive packet. The received data is retained in system memory until the T1R time elapses. The start address and size of the packet are reported with a receive indication for reporting a T1 timeout. The μPD98405 discards all remaining cells, up to the last cell in this packet.

(h) Execution of Deactivate_Channel command

When the host issues a Deactivate_Channel command to the receive VC, the termination of command processing is reported by the receive indication, regardless of whether a packet is currently being received.

If the command is issued while the packet of the VC is being received, the cells stored in the receive FIFO prior to the command being issued are transferred to system memory, and the start address and size of the packet are reported by the same receive indication. While a packet is not being received, 0 is stored as the size in the receive indication.

Table 5-6. Errors Which May Occur for All of the First, Intermediate, and Last Cells of the Packet

Error	Timing of cell discard	Timing of issue of receive indication	Cells arriving after occurrence of error
Free buffer underflow	Cells received when no free buffer is available are discarded.	When transfer becomes impossible during the transfer of a segment	Discarded up to the last cell of the packet
Receive FIFO overrun	Cells received when the receive FIFO is full are discarded.	When the last cell of the same packet arrives after a cell is discarded	Discarded up to the last cell of the packet
"MAX. NUMBER OF SEGMENTS" error	Cells from the cell next to that at which "MAX. NUMBER OF SEGMENTS" is reached to the last cell are discarded.	When the cell next to that at which "MAX. NUMBER OF SEGMENTS" is reached arrives	Discarded up to the last cell of the packet
T1 error	Cells which arrived after time T1 elapses are discarded.	When time T1 elapses	Discarded up to the last cell of the packet
Deactivate_Channel	Cells which arrived after the Deactivate_Channel command is executed, are discarded.	When execution of the command is completed	All cells which arrive in the VC are discarded.

Errors of different types may occur simultaneously, but only a single error is reported by a receive indication. The following table indicates the error which takes precedence, for every possible combination of errors which may occur simultaneously.

Table 5-7. Error Which Takes Precedence upon Occurrence of Multiple Errors

	Underflow	Overrun	MAX. error	CRC error	Abort	Length	T1 error
Underflow	-	-	Underflow	Underflow	Underflow	Underflow	Underflow
Overrun	-	-	Overrun	Overrun	Overrun	Overrun	Overrun
MAX. error	-	-	-	MAX. error	MAX. error	MAX. error	MAX. error
CRC error	-	-	-	-	CRC error	CRC error	CRC error
Abort	-	-	-	-	-	-	Abort
Length	-	-	-	-	-	-	Length
T1 error	-	-	-	-	-	-	-

5.5.6 Issuing Receive Indication

In the case of a packet of AAL-5-type traffic, the μPD98405 issues receive indication to report to the host that it has received a packet. As the receive indication, 4-word information is generated for each packet and stored to a mailbox. The mailbox used for reception is mailbox 0 or 1. Which mailbox is to be used is selected by the host by setting the "MB" bit of the VC table for each VC. When the receive indication is stored, the corresponding MM bit of the μPD98405's GSR register is set to 1, and an interrupt is issued provided it is not masked. The receive indication contains the start address and size of the batch used by the μPD98405 to store the packet. The host can process the packet data that has arrived by reading the receive indication.

The receive indication is issued once all data (including the AAL-5 trailer) has been stored to the receive buffer after the packet has been received normally. If a packet containing an error has been received, and if the error is a "CRC-32 error" or "Length error," the indication is issued when all the data (including the AAL-5 trailer) has been stored to the receive buffer. If any other error occurs, the indication is issued as soon as the error (except the FIFO overrun) has been detected. The detected error is reported in the indication as an error status. If the host reads a receive indication that contains an error status, it performs appropriate processing, and discards the error packet.

The receive indication is issued also when a Deactivate_Channel command or early receive interrupt is issued.

For details of the format of the receive indication, see **Section 5.6 (2)**.

5.5.7 Early Receive Interrupt

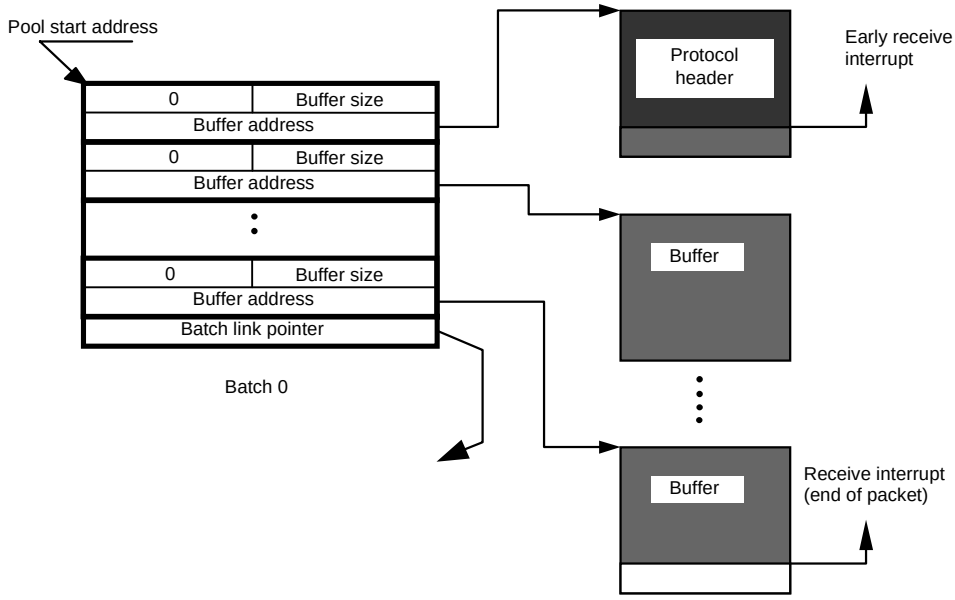
For AAL-5 traffic packets, the μPD98405 supports the early receive interrupt function for requesting an interrupt to the host when it has received several cells of the packet, and reporting with a receive indication. An early receive interrupt is set up separately for individual VCs. The timing of early receive interrupts can be specified in receive cell units.

An early receive interrupt is specified in the EIS field of a receive VC table. If the EIS field is set to "001" or greater, the early receive interrupt is enabled. Once the μPD98405 has received the number of cells specified in the EIS field, it requests an interrupt to the host to set an early receive indication in the mailbox. The early receive indication contains "1111" in its STATUS field. In the early receive indication, the CI and CLP bits are meaningless. These bits are set to 0. The PACKET SIZE in the receive indication is indicated in cell units, even in Length mode. The number of cells received before the early receive interrupt is issued to the host is stored. The other fields of the early receive indication have the same meaning as in the case of normal receive indication.

If the EIS field contains "000," the early receive interrupt is disabled, then the μPD98405 requests an interrupt and stores a receive indication, but only once it has received a complete packet.

The early receive interrupt is useful in protocol header processing. The host can perform protocol header processing for a packet as soon as it has received an early receive indication in which the STATUS field contains "1111" for that packet. In other words, header processing can be performed before the μPD98405 receives a complete packet, that is immediately after it has received the protocol header.

Figure 5-42. Early Receive Interrupt



5.5.8 Receiving Non-AAL-5 Traffic

(1) Reception of raw cell data

In the following two cases, 64-byte raw cell data including 53 bytes of raw cell data and an 11-byte indication is created and stored to an appropriate free buffer pool each time a receive cell arrives. Subsequently, the corresponding bit of RCR7 through RCR0 of the GSR register is set, and an interrupt is issued provided it is not masked.

When raw cell data is received, processing is not performed in units of packets but in units of cells. Consequently, receive indication is not stored to the mailbox.

When raw cell data is received, the verify function of the CRC-10 error code, that is added in cell units, is always enabled. If an error is detected, the error bit in the raw cell data is set and the error is reported to the host.

<1> OAM F5 and RM cell data

When the user sets the OD bit of the VC table to "0" (to enable the reception of an OAM F5 cell) and the μPD98405 receives a cell in which PTI field of the header is of "1XX" format, which indicates OAM F5 and resource management cells, it creates raw cell data and stores it to pool 0. The RCR0 bit of the GSR register is set to 1 and an interrupt is generated provided it is not masked. The μPD98405 always stores these cells to pool 0. If the OD bit is cleared to "0," therefore, pool 0 must be set as a pool that stores raw cell data.

The OD bit can be set to 0 regardless of whether the A/R bit is set to 0 or 1. For example, when OD = 0, A/R = 1, and "POOL NO." = 8, a received cell for which the PTI field contains a user data code is stored in pool 8 as an AAL-5 packet. If a cell for which the PTI field contains an OAM F5 or RM cell code is received, that cell is stored in pool 0 as raw cell data. If at least one channel receives OAM F5 or RM cell, however, pool 0 is used exclusively to store raw cell data. In such a case, a pool other than pool 0 must be specified for storing AAL-5 packets. A single pool cannot contain both raw cell data and an AAL-5 packet.

Remark If a receive VC uses the ABR service (the ABR bit is set to 1), RM cells received by this VC are processed as RM cells for ABR. Even if the OD bit is set to 0, the μPD98405 does not store RM cells in pool 0. Even if the OD bit is set to 1, the μPD98405 does not discard RM cells. Instead, it processes them as RM cells for ABR.

<2> Non-AAL-5 traffic

If the A/R bit of a VC table that has been opened by the user is cleared to "0," each time a cell of the VC is received, it is transferred to system memory as raw cell data. When raw cell data is received, the user can specify any of pools 0 through 7 for "POOL NO.". The specified pool must be prepared to store the raw cell data. This function allows the user to receive cells of non-AAL-5 traffic. The assembly of a packet from raw cell data and trailer processing are executed by software in system memory. When non-AAL-5 traffic is received as raw cell data, processing is completed in cell units and no receive indication for each packet is issued, unlike in the case of AAL-5 packets. An error report function such as that supported for AAL-5 packet reception is, therefore, not supported for non-AAL-5 traffic. Even if a cell is discarded due to a free buffer underflow or receive FIFO overrun, the μPD98405 does not report it to the host, and the monitoring of "MAX. NUMBER OF SEGMENTS" and the detection of a T1 error are disabled. An RQU interrupt is, however, issued and an indication for reporting the completion of the Deactivate_Channel command is also issued.

During raw cell reception with A/R = 0, if a cell for which the PTI field contains an OAM F5 or RM cell code is received, that cell is stored in pool 0, provided OD is set to 0.

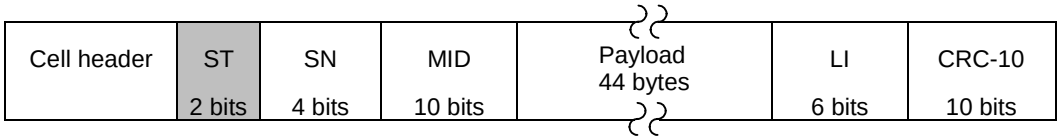
- **AAL-3/4 packet raw cell reception assist function**

  Normally, in raw cell reception, each time a cell is received, an RCR interrupt occurs to cause the host to process the cell separately from other cells. For AAL-3/4 packet reception, a switching function is provided to reduce the load on the host. With this function, the interrupt is issued only when the last cell of a packet or single-cell data has been received.

  If the A34 bit of a receive VC table is set, the μPD98405 checks the segment type (ST field) in the MSB and subsequent bit in the first byte of the payload of a received cell. It issues an RCR interrupt only when the two ST field bits are set to "01" (end of message) or to "11" (single-segment message). If any other type of cell is received, the raw cell data is stored into system memory, but an RCR interrupt does not occur.

  When the A34 bit is set to 1, the A/R bit must be set to 0.

AAL3/4 cell



Remark ST: Segment type LI: Length (payload length) indication

SN: Sequence number MID: Multiplexing identification

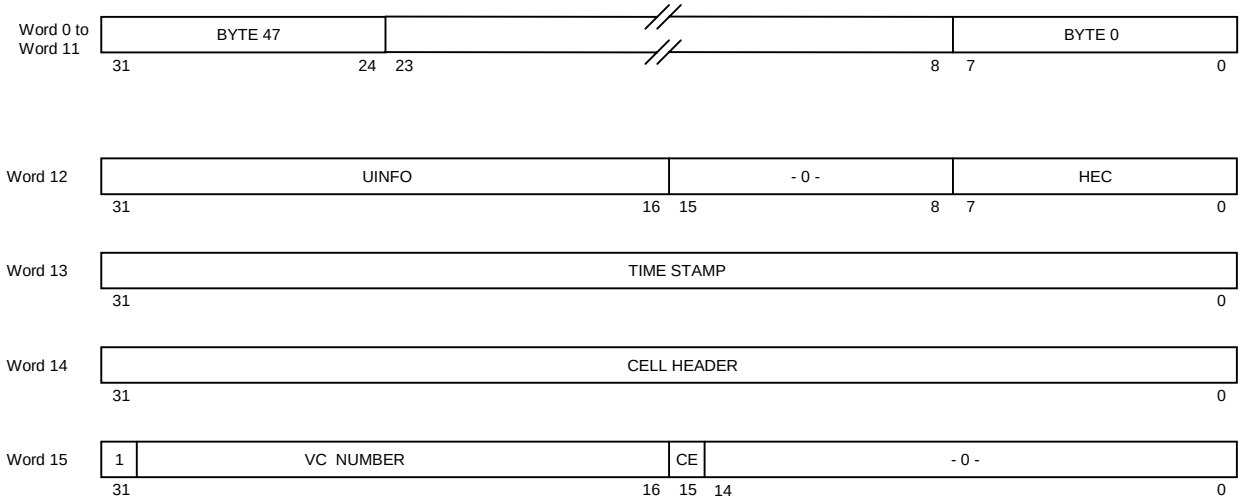
CRC: Cyclic redundancy check code

ST bits	Segment type
10	BOM (beginning of message)
00	COM (continuation of message)
01	EOM (end of message)
11	SSM (single-segment message)

(2) Raw cell data

The raw cell data format is shown below (little endian).

Figure 5-43. Format of Raw Cell Data



BYTE0-BYTE47 ..Segment data of receive cell

UINFO.....User information. The pattern that the user sets in the UNIFO field of the VC table for this channel is stored as is. Note, however, that for an OAM/RM/Reserved cell received by a VC that also receives an AAL-5 packet, when LECID insertion is used for that VC (RLI of the receive VC table is set to 1), this UINFO field cannot be used and the stored value will be undefined.

HEC .....Pattern of HEC field included in header of this cell

TIME STAMP .....Value of TSR register when this cell is received

CELL HEADER ...First 4 bytes of header of this cell (HEC at fifth byte is not included.)

VC NUMBER.....VC NUMBER of VC of this cell

CE .....Verify result of CRC-10 error calculation

0: No error

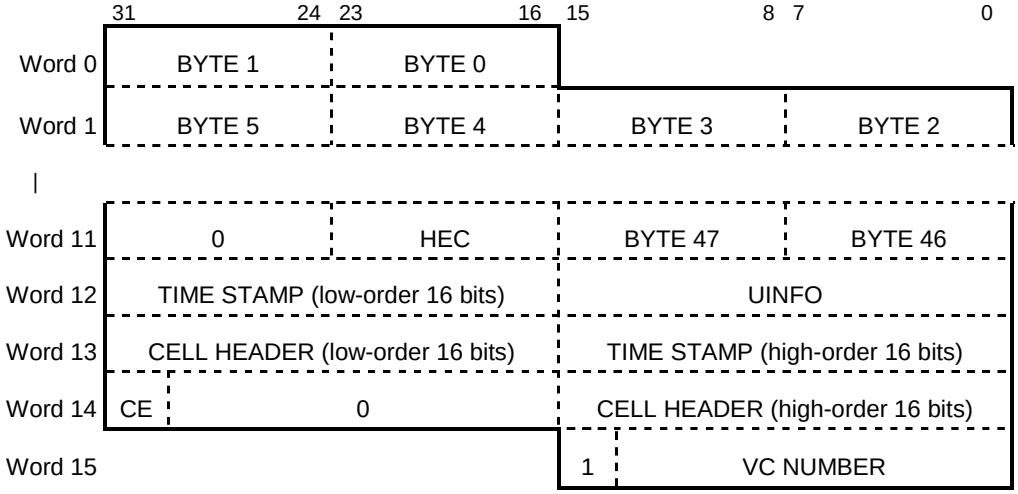
1: CRC-10 error detected

The above is little endian format. In big endian format, the byte location of the data (Word 0 through Word 11) is changed, but the indication (Word 12 through Word 15) is not changed.

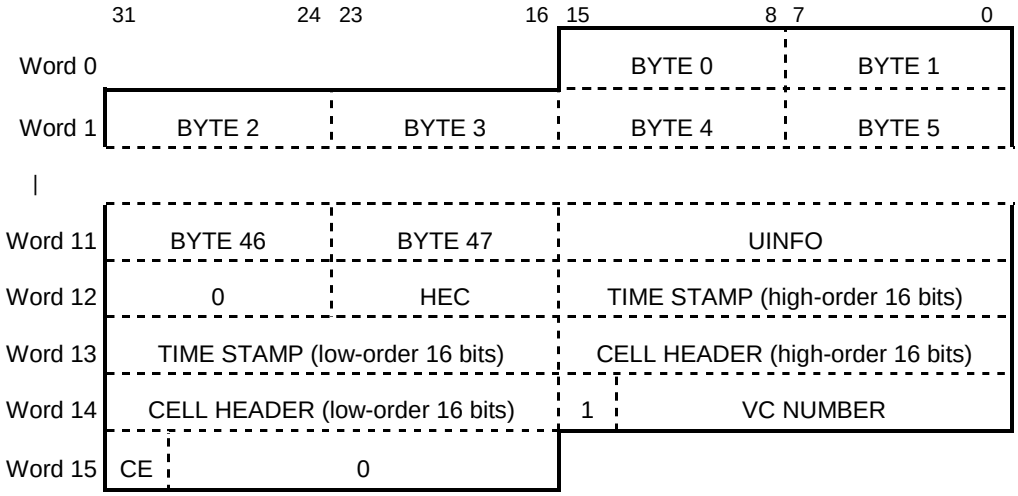
The following example of storing raw cell data illustrates the case where the receive buffer is aligned with a byte boundary.

Figure 5-44. Example of Storing Raw Cell Data

<1> Little endian



<2> Big endian



5.6 TRANSMIT/RECEIVE INDICATION

The μPD98405 sends an indication to the host as a status indicating the completion of transmission/reception for each packet. The transmit/receive indication is issued at the following timing.

- Transmit indication:
  - Once all the data in one transmit packet has been read
  - When a Deactivate_Channel command has been received during packet transmission and command processing has been completed

- Receive indication:
  - Once all the data in one receive packet has been transferred to system memory
  - When the reception of a packet has been stopped due to an error
  - When the Deactivate_Channel command has been received and command processing has been completed
  - Early indication based on the early receive interrupt function

The indication is stored to one of the four mailboxes managed by system memory. Two of the mailboxes are used for storing transmit indication, while the other two are used for storing receive indication. Which of the two mailboxes is to be used can be selected by the user for each VC.

- Transmit indication: Mailbox 2 or 3, set to packet descriptor
- Receive indication: Mailbox 0 or 1, set to VC table

When the μPD98405 stores the indication to the mailbox, it sets the corresponding MM bit of the GSR register to "1", and generates an interrupt if the corresponding bit of interrupt mask register IMR is enabled.

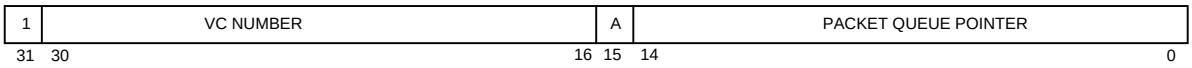
Bit 31 of the transmit indication and bit 15 of Word 3 of the receive indication stored by the μPD98405 must be always set to "1." The host uses this bit of an indication as a flag to indicate whether the indication in the mailbox "has been processed," by resetting this bit to "0" after reading the indication. By using this bit as a flag, two or more indications can be processed at one time by continuing the processing for as long as a "1" indication is followed by another (this flag does not always have to be changed).

The receive indication stores information relating to the batch and free buffer to which a packet has been stored. The host processes the receive data (such as padding and removing the AAL-5 trailer) based on the indication, then transfers the data to an application that is higher in the hierarchy. Then, the host releases the batch and free buffer it has used to system memory, or adds them to the chain as a new batch and free buffer for recycling.

The format of the transmit/receive indication is explained below.

(1) Transmit indication

The format of the transmit indication is as shown below (the format is the same for both big endian and little endian).



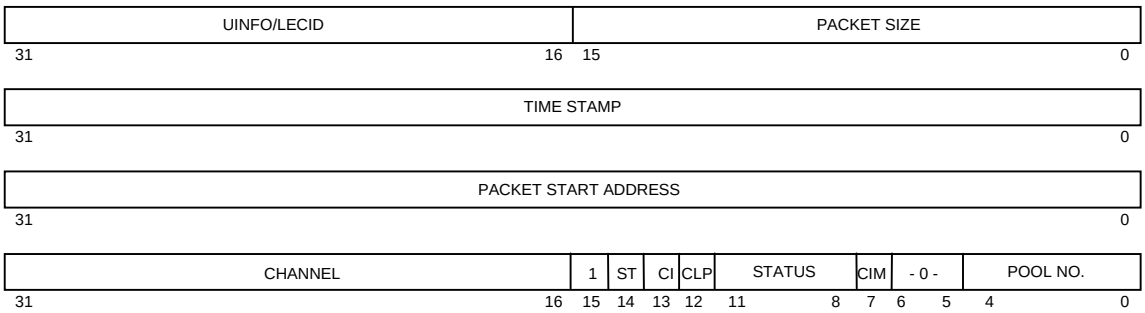
VC NUMBER "VC NUMBER" used by this VC

A (Active)
0: The next packet descriptor is vacant. Or, the transmission of this packet was terminated as a result of a Deactivate_Channel command being received during packet transmission.
1: VC remains in the active status because the next packet descriptor is also valid.

PACKET QUEUE POINTER Pointer indicating the address of the next packet in transmit queue.
Low-order 15 bits of start address of the packet descriptor

(2) Receive indication

Receive indication is issued for a packet of AAL-5-type traffic. It is not issued when raw cell data of non-AAL-5 traffic is processed. The format of the receive indication is as shown below (the format is the same for both big endian and little endian).



UINFO/LECID User information/receive LECID

This field is used to contain user information if the RLI bit of a receive VC table is set to 0. This user information is of the same pattern as that set in the "UINFO" area of the receive VC table by the host. If the RLI bit of a receive VC table is set to 1, the field holds receive LECID, which is supplied from the LECID field of the receive packet.

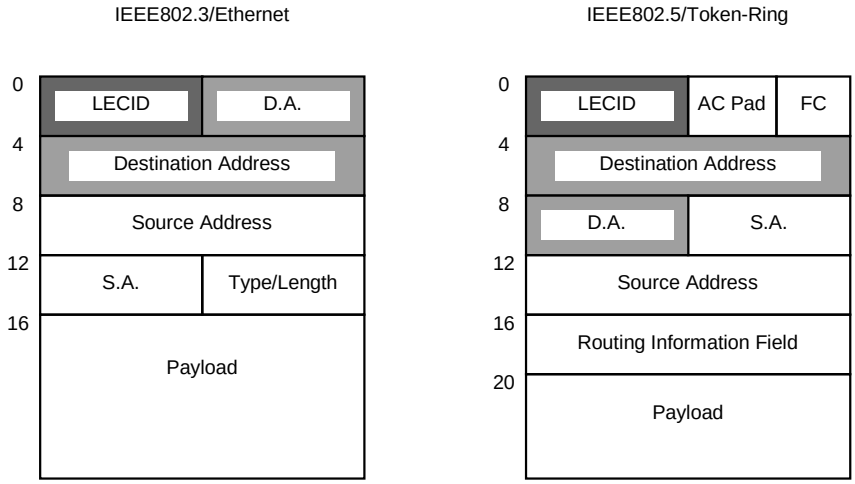
PACKET SIZE	Receive packet size. The receive packet size is given either in cell units or in the Length value, either of which is selected by setting the PSM bit of the GMR register. PSM = 1: The PACKET SIZE field contains the same value as that in the AAL-5 trailer Length field. It is the user data length of AAL-5 PDU, in byte units. PSM = 0: The PACKET SIZE field indicates the size of the receive packet (including the AAL-5 trailer), in cell units. For an indication to report an error or an early receive indication, the receive packet size is given in cell units even when the PSM bit is set to 1.
TIME STAMP	Value of TSR register when this packet was received
PACKET START ADDRESS	Start address of the used batch
CHANNEL	VC NUMBER or VPI/VCI value. Stores the VC NUMBER or VPI/VCI value of the channel that was used to received this packet. This mode is set with the CIM bit of the VC table for each receive VC. Also, the CIM bit of the indication is used to post notification of which value is to be stored. CIM = 1: The VPI/VCI value, the length of which has been reduced to 16 bits using the VRR register, is stored into the field. CIM = 0: The VC NUMBER of the channel on which this packet was received is stored in bits 16 to 30. Bit 31 is set to 0.
ST	Status indication. 1: The indication status field contains a value other than 0 (normal). 0: The indication status field contains 0 (normal).
CI	Congestion indication. Indicates that at least one of the cells belonging to this packet has arrived with a congestion code in the PTI field of the header.
CLP	CLP = 1. Indicates that at least one of the cells belonging to this packet has arrived with the CLP field in the header set to "1."

STATUS	Status of indication '0000': Normal '0001': Free buffer underflow '0010': Receive FIFO overrun '0011': MAX. NUMBER OF SEGMENTS violation '0100': CRC-32 error '0101': User abort '0110': Length error '0111': T1 timeout '1000': Issue of Deactivate_Channel command '1111': Early receive interrupt For an explanation of how to detect each error, see **Section 5.5.5 (4)**.
CIM	Channel Indication Mode The CHANNEL field of this indication specifies whether the VC NUMBER or VPI/VCI 16-bit reduction value has been stored. 1: VPI/VCI 16-bit reduction value 0: VC NUMBER
POOL NO.	Number of pool being used

5.7 LAN EMULATION FUNCTION

The μPD98405 supports several types of LAN emulation function in order to reduce the load related to LAN emulation on the host system. The μPD98405's LAN emulation assist function is valid only for type AAL-5 packets. The μPD98405 supports flexible frame formats such as Ethernet and token-ring frame formats. The Ethernet and token-ring frame formats are shown below.

Figure 5-45. Ethernet and Token Ring Frame Formats



(1) Storing the receive LECID in the receive indication

The μPD98405 can store the receive LECID (LAN Emulation Client Identifier) for each receive VC in a separate receive indication. If the RLI bit of the receive VC table is set to 1, the μPD98405 loads the first two bytes of the receive packet with an LECID to report it in the receive indication. The receive LECID is indicated in the UINFO/LECID field of the receive indication. Upon receiving this indication, the host can start processing of the LECID. The LECID is also stored into the receive buffer.

Remark Enabling this function (RLI = 1) prevents the host from using the "user information (UINFO)." The μPD98405 stores the receive LECID into the UINFO/LECID field of the VC table, and indicates such in the UINFO/LECID field of the indication.

(2) Automatically inserting the transmit LECID into the transmit packet

The μPD98405 can automatically insert its LECID at the beginning of the transmit packet. The LECID for each VC can be set separately in the LOCAL LECID field of the transmit VC table. This enables connection to more than one emulated LAN.

If the LIE bit of the transmit VC table is set to 1, the μPD98405 treats the value in the LOCAL LECID field of the VC table as an LECID, and inserts it at the beginning of the VC transmit packet. The first two bytes of the first buffer of the packet will not be overwritten with the LECID. The μPD98405 creates a transmit packet by adding the LECID to the contents of the transmit buffer.

(3) Discarding a receive packet by LECID matching

The μPD98405 can automatically discard a receive packet if it has the same LECID as its own LECID. The μPD98405's LECID, which will be compared with a receive LECID, can be set in the LOCAL LECID field of the receive VC table for each VC. This enables connection to more than one emulated LAN. If the LFE bit of the receive VC table is set to 1, the μPD98405 compares the value in the LOCAL LECID field of a receive VC table with the receive LECID of the relevant VC. If they match, the μPD98405 discards all the cells, up to the last one, that belong to this receive packet.

(4) Receive packet filtering based on MAC address matching

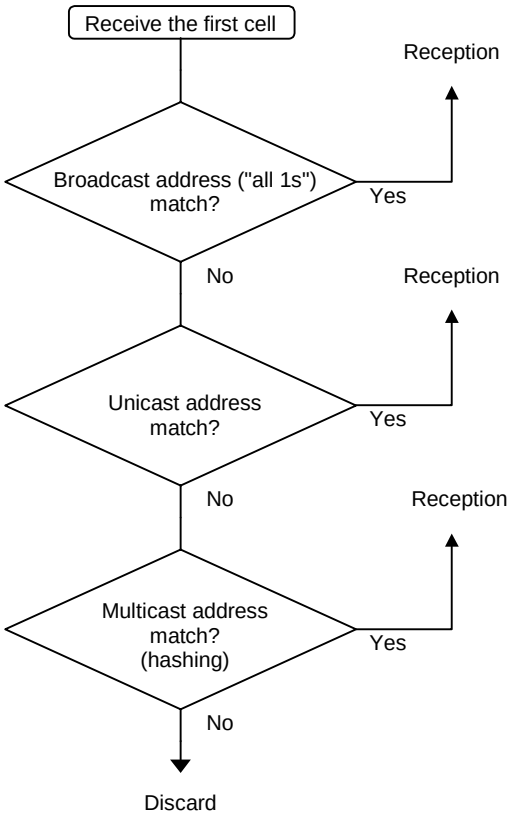
The μPD98405 supports receive packet filtering based on MAC address (destination address) matching. Whether to enable or disable filtering can be selected separately for individual VCs. If the DAF bit of a receive VC table is set to 1, filtering is enabled for the VC table. The host sets the destination address to be submitted to filtering reception in the MAU, MAL, HTU, and HTL registers. The position of the destination address within the receive packet is variable. This configuration enables the support of frame formats such as the Ethernet and token-ring frame formats. The host loads the MAC field of a receive VC table with the byte position of the destination address relative to the beginning of the receive packet. The μPD98405 identifies the destination address according to the value in the MAC field, as listed below:

MAC field value	Byte position relative to the beginning of the receive packet
"00"	2 bytes (Ethernet)
"01"	4 bytes (Token-Ring)
"10"	6 bytes
"11"	10 bytes

The size of the destination address used in filtering is fixed to 6 bytes.

The μPD98405 checks the destination address in the receive packet, and determines whether to accept or discard the receive packet. Filtering is executed by means of the following three steps:

Figure 5-46. Receive Packet Filtering Flow

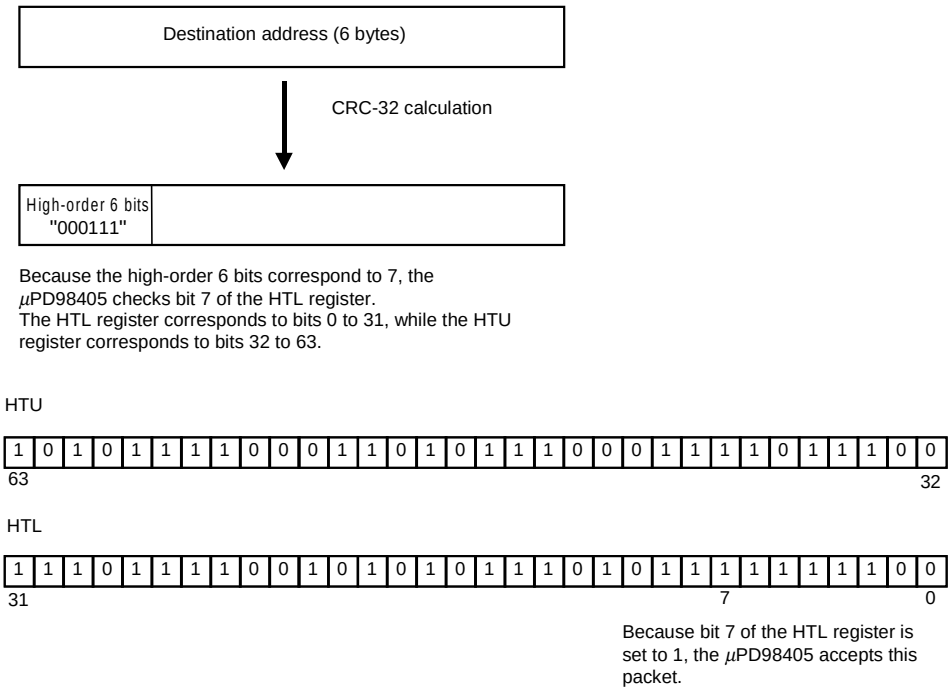


<1> Upon receiving the first cell of a packet, the μPD98405 recognizes the position of the destination address from the offset set in the MAC field of the VC table, then compares the destination address of the receive packet with the broadcast address (that consisting of "all 1s"). If they match, the μPD98405 accepts the packet.

<2> The μPD98405 compares the 6-byte unicast address in the MAU and MAL registers with the destination address of the receive packet. If they match, the μPD98405 accepts the packet. The host must set its own MAC address (unicast address) in the MAU and MAL registers in advance.

<3> The μPD98405 checks for multicast address matching, which is based on a hash method. First, the μPD98405 performs CRC-32 calculation for the destination address of the receive packet, then makes the high-order 6 bits of the calculation result valid. If those bits of the HTU and HTL registers which correspond to the value in these 6 bits are set to 1, the μPD98405 accepts the packet. If these bits of the HTU and HTL registers are instead set to 0, the μPD98405 discards all cells, up to the last one, that belong to that packet. An example of using the hash method is shown below:

Figure 5-47. Multicast Address Matching Hash Method



The host must set those bits of the HTU and HTL registers, which correspond to the desired multicast address, in advance. Perform CRC-32 calculation for the multicast address, and set those bits of the HTU and HTL registers that correspond to the high-order 6 bits of the calculation result to 1. The HTL register corresponds to bits 0 to 31, while the HTU register corresponds to bits 32 to 63. The CRC-32 generating polynomial is as follows:

Expression = $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

5.8 ABR FUNCTION

5.8.1 Overview

The μPD98405 supports the ABR service by hardware. It controls the resource management cell (RM cell) according to ATM Forum Traffic Management Specification Version 4.0. Upon receiving a forward RM cell (FRM cell), the μPD98405 automatically returns a backward RM cell (BRM cell) using an in-rate or out-of-rate stream. Upon receiving a BRM cell, the μPD98405 automatically changes the data cell transmission rate according to the congestion information (CI, NI, and ER) of the BRM cell.

The features of the ABR service supported by the μPD98405 are as follows:

- Complies with ATM Forum Traffic Management Specification Version 4.0 (af-tm-0056.000).
- Supports the source/destination behavior of the ATM Forum's ABR flow control.
- Supports 256 active ABR channels.
- Contains an in-rate buffer and out-of-rate queue for the ABR service.
- Supports local congestion management (source/destination).

Remarks **1**. A BRM cell that is sent back is called a turn-around BRM cell.

2. A cell stream with CLP = 0 is called an in-rate stream, while one with CLP = 1 is called an out-of-rate stream.

5.8.2 Source/Destination Behavior

This section describes the behavior of the source/destination supported by the μPD98405 by hardware.

(1) Source behavior

1. The ACR value will never exceed the PCR, nor become smaller than the MCR. The μPD98405 will not transmit in-rate cells at a rate higher than the ACR. The μPD98405 transmits in-rate cells at the ACR rate or slower.
2. Once a connection has been set up, the ACR value is set in the ICR before the μPD98405 transmits the first cell. The first in-rate cell to be transmitted is an FRM cell.
3. Once the first in-rate FRM cell has been transmitted, the other in-rate cells are transmitted according to the rules stated below:
   a) When at least Mrm in-rate cells have been transmitted, and a period at least equal to Trm has elapsed, or when Nrm - 1 in-rate cells have been transmitted since the latest FRM cell transmission, the next in-rate cell to be transmitted will be an FRM cell.
   b) When condition a) does not apply, a BRM cell is waiting to be transmitted, and no in-rate BRM cell has been transmitted since the latest FRM cell transmission, or no data cell is waiting to be transmitted, the next in-rate cell to be transmitted will be a BRM cell.

c) When neither condition a) nor b) applies, and a data cell is waiting to be transmitted, the next in-rate cell to be transmitted will be a data cell.

4. Cells for which CLP = 0 are transmitted according to rules #1, #2, and #3.
5. If a calculated ACR for an in-rate FRM cell is higher than the actual rate, and the difference is greater than the threshold value, the ACR is reduced to ACR*15/16 before the in-rate FRM cell is transmitted. This reduction is repeated continuously for as long as the rate remains higher than the MCR. If this reduction makes the ACR smaller than the MCR, the ACR is set to the same value as the MCR. The subsequent rate increase is prohibited. (Use-it-or-lose-it function: see **Section 5.8.6**.)
6. After ACR adjustment by #5 has been performed, but before the in-rate FRM cell has been transmitted, the following ACR adjustment is performed: If at least CRM in-rate FRM cells have been transmitted since a BRM cell was last received (with BN = 0 and generated by the source), the ACR is reduced to ACR*CDF. This reduction is repeated continuously for as long as the rate remains higher than the MCR. If this reduction makes the ACR smaller than the MCR, the ACR is set to the same value as the MCR.
7. If the ACR is reduced according to rule #5 or #6, the new ACR value is placed in the CCR field of the FRM cell that is to be transmitted. The new rate, however, is applied to the in-rate cell to be transmitted after this FRM cell.
8. If a BRM cell arrives with CI = 1, the ACR is reduced to ACR*RDF. In addition, if LCI = 1 (see #14), the ACR is reduced to prevent internal congestion. If the rate becomes lower than the MCR in both cases, the ACR is set to the same value as the MCR. If a BRM cell arrives with CI = 0, NI = 0, and LCI = 0, the ACR is increased by RIF*PCR. In this case, the ACR is kept below the PCR. If a BRM cell arrives with NI = 1, the ACR will not be increased. (Internal congestion control: see **Section 5.8.6**.)
9. After a BRM cell has been received, and ACR adjustment according to rule #8 is performed, an ACR is set to a value calculated according to rule #8, or to the value in the ER field of the BRM cell, whichever is smaller. It will not, however, become smaller than the MCR.
10. When the source generates an FRM cell, the μPD98405 sets an appropriate value in the RM cell field. (See **Section 5.8.3**.)
11. If the ACR is 0 cells/s, the μPD98405 transmits the out-of-rate FRM cell at the TCR rate (10 cells/s). When the ACR becomes higher than 0 cells/s, the μPD98405 stops transmitting the out-of-rate FRM cell at the TCR rate.
12. An RM cell (either FRM or BRM) may be transmitted as an out-of-rate cell with CLP = 1. The data cell is always transmitted with CLP = 0.
13. The μPD98405 resets the EFCI of all the data cells it transmits.
14. If the difference between the service time of a transmit in-rate cell and the programmed time is greater than the threshold value, or if the ACR total is greater than the ABR band, the μPD98405 detects it as being congestion internal to the source, and sets the LCI (internal flag that indicates internal congestion) to 1. (Internal congestion control: see **Section 5.8.6**.)

15. When a period at least equal to ADTF has elapsed since the latest in-rate FRM cell transmission, and neither a data cell nor BRM cell is waiting:
    a) If ACR ≥ ICR, the μPD98405 sets the ACR with ICR, and removes the relevant channel from the ABR scheduler.
    b) If ACR < ICR, the μPD98405 keeps the ACR as is, and removes the relevant channel from the ABR scheduler.

Remarks 1. Nrm, Trm, Mrm, and CRM are specified for individual ports. (These parameters are set in indirect address registers.)

2. PCR, MCR, ICR, RIF, CDF, RDF, and ADTF are specified for individual VCs. (These parameters are set in the VC table.)

3. In-rate FRM and BRM cell transmission is included in the source rate assigned to the relevant VC.

4. The ABR scheduler is a module for controlling the transmit cell time interval determined by the ACR.

(2) Destination behavior

1. Upon receiving a data cell, the μPD98405 saves the EFCI of the data cell as the EFCI state of the connection.
2. Upon receiving an FRM cell, the μPD98405 transmits a turn-around BRM cell to send back an RM cell to the source. The DIR bit of the RM cell to be sent back is changed from forward (DIR = 0) to backward (DIR = 1). The BN bit is reset to 0. The CCR, MCR, ER, CI, and NI fields are not changed except in the following cases.
    a) If the preserved EFCI state is set to 1, the μPD98405 sets the CI bit of the RM cell to 1, and resets the preserved EFCI state.
    b) Upon receiving an internal congestion command (Set_Rx_Congestion command) from the host, the μPD98405 sets the CI and/or NI of all BRM cells to 1.
    c) If the number of cells in the receive FIFO becomes greater than the threshold value, the μPD98405 sets the CI of all BRM cells to 1. (Internal congestion control: see **Section 5.8.6**.)
    d) If there is no remaining capacity of the receive pool, the μPD98405 sets the CI of those BRM cells returned from the VC that belongs to this receive pool to 1.
3. If an FRM cell is received before a turn-around BRM cell is scheduled for in-rate transmission (at the relevant connection), the μPD98405 schedules the turn-around BRM cell for in-rate transmission.
4. If the μPD98405 receives an FRM cell when another turn-around BRM cell is being scheduled for in-rate transmission (at the relevant connection):
    a) The contents of a BRM cell that has already been scheduled are overwritten with the contents of the new BRM cell.

b) If no RM cell is waiting for out-of-rate transmission, the new BRM cell will be scheduled for out-of-rate transmission.

c) If there is another RM cell waiting for out-of-rate transmission, it will be replaced with the new BRM cell.

Remark The term "turn-around" pertains to the behavior of the destination to which a BRM cell is transmitted in response to a received FRM cell.

5.8.3 RM Cell Format

The format of an RM cell generated by the μPD98405 is shown below.

Figure 5-48. RM Cell Format

ATM header						(Octets 1-5)
Protocol ID						(Octet 6)
DIR	BN	CI	NI	RA	Reserved	(Octet 7)
ER						(Octets 8-9)
CCR (Octets 10-11)						(Octets 10-11)
MCR (Octets 12-13)						(Octets 12-13)
QL (Octets 14-17)						(Octets 14-17)
SN (Octets 18-21)						(Octets 18-21)
Reserved (Octets 22-51; octet 52,bits 8-3)						(Octets 22-51; bits 8-3 of octet 52)
CRC10 (Octet 52, bits 2-1; octet 53)						(Bits 2-1 of octet 52; octet 53)

Table 5-8. Descriptions of RM Cell Fields

Field	Function	FRM cell	BRM cell[Note]
ATM header	ATM header	PTI: "110"	PTI: "110"
Protocol ID	Protocol ID	"00000001"	"00000001"
DIR	Direction 1: Backward RM cell 0: Forward RM cell	0	1
BN	BECN cell 1: RM cell generated by an entity other than the source 0: RM cell generated by the source	0	1
CI	Congestion notice 1: Congestion 0: No congestion	0	0 or 1
NI	No increase 1: Rate increase disabled 0: Rate increase enabled	0	0 or 1
RA	Request/acknowledge	0	0
Reserved in Octet 7	Reserved	0	0
ER	Explicit cell rate	PCR (VC table)	Arbitrary rate
CCR	Current cell rate	ACR (VC table)	0
MCR	Minimum cell rate	MCR (VC table)	0
QL	Queue length	0	0
SN	Sequence number	0	0
Reserved in Octet 22-51	Reserved	"6AH" for each octet	"6AH" for each octet
Reserved in Octet 52	Reserved	0	0
CRC-10	CRC-10	CRC-10	CRC-10

Note This is a BRM cell, generated at the destination (by using the BRM_Tx command). See **Section 5.8.2 (2)** for details of the BRM cell to be sent back (turn-around BRM cell).

Remark For both the BRM cell generated at the destination and a turn-around BRM cell, the GFC field of the ATM header is 0.

5.8.4 ABR Parameters

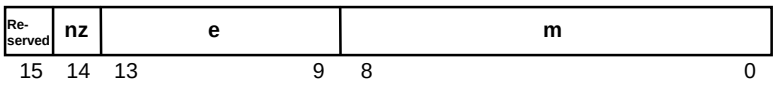
The following table lists the ABR parameters defined by the ATM Forum. Their initial values are also defined by the ATM Forum.

Table 5-9. ABR Parameters

Label	Function	Unit and range	Initial value
PCR	Peak cell rate	Unit: cells/s Range: (**Note**)	–
MCR	Minimum cell rate	Unit: cells/s Range: (**Note**)	–
ICR	Initial cell rate, which is valid at initialization and in the idle state	Unit: cell/s Range: (**Note**)	–
RIF	Rate increase factor, which is used to control the way the cell is increased at RM cell reception	Power of 2 Range: 1/32,768 to 1	1
Nrm	Maximum number of cells that can be transmitted between FRM cell transmission sessions	Power of 2 Range: 2 to 256	32
Mrm	The number (minimum number) of cells that are transmitted between FRM cell transmission sessions is controlled.	Constant: 2	2
RDF	Rate decrease factor, which is used to control the way the transmission cell rate is decreased	Power of 2 Range: 1/32,768 to 1	1/32,768
ACR	Allowed cell rate, which is the current cell rate that can be applied to transmission from the source	Unit: cells/s Range: (**Note**)	ICR
CRM	Missing RM cell count, which is used to control the number of FRM cells that can be transmitted before a BRM cell is sent back	Unit: cells: Integer	–
ADTF	ACR decrease time factor, that is, time limit between FRM transmission sessions. If no FRM is transmitted even after this time interval has elapsed, the rate is decreased to the ICR.	Unit: seconds Range: 0.01 to 10.23 (in 10 ms steps)	0.5
Trm	Time between FRM cell transmission sessions for the active source	Unit: milliseconds 100 times power of 2 Range: $100*2^{-7}$ to $100*2^{0}$	100
FRTT	Fixed round trip time, which is the total propagation delay from the source to the destination	Unit: microseconds Range: 0 to 16.7 s	–
TBE	Transient buffer exposure, which is a parameter used by the network to limit the number of cells that can be transmitted from the source within the start-up period before the first RM cell is returned	Unit: cells Range: 0 to 16,777,215	16,777,215
CDF	Cut-off decrease factor, which is used to control the way the ACR and the CRM are decreased	0 or power of 2 Range: 0, 1/64 to 1	1/16
TCR	Tagged cell rate, at which the source can transmit out-of-rate FRM cells	Constant: 10 cells/s	10

Note The rate field is represented as shown below:

$$Rate = 2^{e}*(1 + m/512)*nz \text{ cells/s}$$



The FRTT and TBE parameters are used to determine the other parameters. The μPD98405 has no field for setting these parameters. The host must determine the other parameters from the FRTT and TBE parameters that are obtained through negotiation. The parameters determined from FRTT and TBE are as follows:

CRM = TBE/Nrm

ICR = min(ICR, TBE/FRTT)

5.8.5 ABR Service Processing

This section describes the processing that the host must perform to enable the use of the ABR service. It focuses on processing unique to the ABR service. The host should also perform the same processing as that performed when using the VBR service. Before attempting to use the ABR service, read and become familiar with the contents of **Chapter 5**.

Remark The terms "transmission" and "reception," as used in this section, have the same meanings as the source and destination, respectively.

(1) Setting control memory

To use the ABR service, it is necessary to allocate an ABR lookup table in control memory (see **Section 5.2**). The host sets the start address of the ABR lookup table in the ALA register. An area from the ALA register to the TOS register is assigned as the ABR lookup table. This table can consist of up to 8 blocks (each block having 16 words). The actual number of blocks varies with the number of active ABR channels that are supported. The μPD98405 can support up to 256 active ABR channels. When 256 active ABR channels are supported, the ABR lookup table will consist of 8 blocks. An active ABR channel is a channel that is currently transmitting data (or that is active). The μPD98405 can support up to 256 active ABR channels simultaneously. Similarly to the VBR service, the ABR service can support 32K channels (VC) if they are open and placed in the idle state by setting a VC table for them.

The ABR lookup table is an area used by the μPD98405. The host need not access this area.

- **Active channel support for 256 and more VCs**

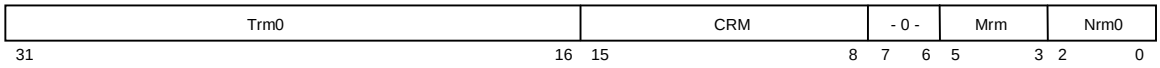
  For the μPD98405, a maximum of 256 active ABR channels can be registered in the ABR lookup table. Therefore, no more than 256 VCs can be supported. This band is used, by the ABR scheduler, to perform ABR scheduling. Even if more than 256 VCs are active, the μPD98405 will not malfunction. Those VCs in excess of 256 are made to wait to be registered in the ABR lookup table and, when a VC becomes inactive, one of the waiting VCs is registered and data transmission starts. Note, however, that there will be a period during which those VCs that are being made to wait are not subject to control by the ABR scheduler. As a result, rate control can not be performed successfully. In other words, if more than 256 VCs are active, the μPD98405 will not actually malfunction, but rate control will not be applied during data sending.

(2) Setting registers for the ABR

The ABR service uses the APR, TBW, and AUB registers. The host must set values in these registers. In addition, values must also be set in those registers that are responsible for internal congestion control (see **Section 5.8.6**).

- **APR register**

The APR register is set with parameters for each port used for the ABR service. The parameters set in the APR register are common to all ABR channels. Those parameters that are separately specified for each channel (VC) are set in the transmit/receive VC table. The host sets, in the APR register, the ABR parameters obtained through negotiation.



Trm0 The Trm parameter is used to set the length of the period during which FRM cell transmission is performed for the active source.

For the host, set Trm0 so that Trm is displayed in cell time units. (1 cell time = 2.8312 μs; the μPD98405 ignores the SONET/SDH overhead and performs rate calculation with the maximum rate fixed to 149.76 Mbps.)

Trm (milliseconds) = Trm0*2.8312/1,000

Default value after a reset (Trm0): 35,321 (89F9H)

CRM Missing RM cell count.

The CRM parameter controls the number of FRM cells that can be transmitted before a BRM cell is returned.

Default value after a reset: 255

Mrm The Mrm parameter controls the assignment of the bandwidth (cell count) for BRM cells or data cells during FRM cell transmission.

Default value after a reset: 2

Nrm0 The Nrm parameter sets the maximum number of cells that the source can transmit during FRM cell transmission.

Nrm is expressed as follows.

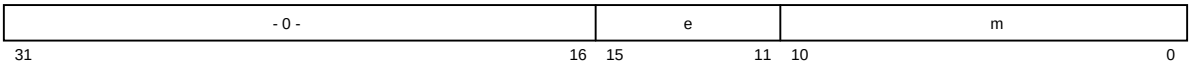
Nrm = $2*2^{Nrm0}$

Default value after a reset (Nrm0): 4

- **TBW register**

The host sets, in the TBW register, all the bands that can be used by the μPD98405, such as 155.52 and 25.6 Mbps. Obtain each band to be specified, using the following expression, and express it in cells/s.

Band = 2^e*(1 + m/2,048) cells/s



A band specified in the TBW register must be one that can be used by the ATM layer, that is, a band that does not include the SONET/SDH overhead. The following table lists examples of the settings made for the 155.52 Mbps SONET/SDH framer or 25.6 Mbps PHY device.

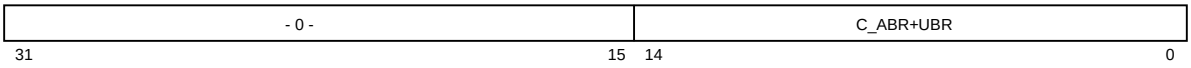
155.52 Mbps (149.76 Mbps)	e = 18, m = 711
25.6 Mbps (25.126 Mbps)	e = 15, m = 1,656

Because 149.76 Mbps (e = 18 and m = 711) is specified initially, it need not be specified if the built-in PHY layer is used.

- **AUB register**

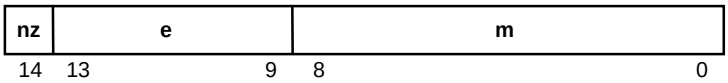
The host sets, in the AUB register, a band that is exclusively used for the ABR or UBR service. If the UBR service is not being used, the value set in the register will correspond to the band used for the ABR service. The host can change this value at any time. When ABR and UBR are used simultaneously, the total of C_ABR (band for ABR) and C_UBR (band for UBR) is C_ABR+UBR. See **Section 5.9** for details.

The AUB register is used with the source internal congestion control. See **Section 5.8.6** for details.



C_ABR+UBR: ABR and UBR bands. Bands used exclusively for the ABR and/or UBR service are specified using the rate expression described below:

Rate = 2^e*(1 + m/512)*nz cells/s



Remark The μPD98405 performs rate adjustment based on the band that can be used in the ATM layer (excluding the overhead incurred by SONET/SDH). Make the rate settings for the AUB register, PCR, MCR, and ICR in that band of the ATM layer (excluding the overhead) that can be used. When the 155.52 Mbps SONET/SDH framer is being used, the maximum rate that can be set is 149.76 Mbps.

(3) Setting the ABR scheduler

The μPD98405 links a VC that uses the ABR service to the ABR scheduler that performs automatic rate control. The host need only specify the priority of the ABR scheduler. (See **Section 7.3**.)

The ABR scheduler is handled as shaper 16. The μPD98405 has an in-rate buffer and out-of-rate queue in the ABR scheduler. The in-rate buffer and out-of-rate queue have their own priority registers, and the host specifies priority in these registers. Usually, the in-rate buffer has a higher priority than the out-of-rate queue. The host must assign the ABR scheduler (for both the in-rate buffer and out-of-rate queue) a priority lower than that of the shaper used for VBR but higher than that of the shaper used for UBR.

The assigned priority can be changed at any time. To change it, set the B3 bit (byte enable) of the Indirect_Access command to 1 without overwriting the other fields of the priority register.

(4) Open channel

ABR channels are opened using an Open_Channel command, similarly to VBR channels. The host opens two channels at a time. To enable the use of the ABR service, the μPD98405 must have two channels, a transmit VC and receive VC. The ABR service always uses both a transmit VC and a receive VC. A receive VC is needed even if data is only transmitted, because it is used to receive a BRM cell. If data is only received, a transmit VC is required to send back a BRM cell. If data is both transmitted and received, the same VC can be used for both data reception and turn-around BRM cell reception, and the same VC can be used for both data transmission and BRM cell return. To sum up, data transmission and reception only require one transmit VC and one receive VC. No extra VC is required for turn-around BRM cell reception or BRM cell return.

(5) Setting the VC table

The host sets initial values for the transmit and receive VCs which it opened. For details of the format of the VC table, see **Sections 5.4.3** and **5.5.3**.

- **Setting the transmit VC table**

  The host sets the transmit VC table with its initial values. In addition to the settings for the VBR VC table, the host must set values that are specific to the ABR service. The settings specific to the ABR transmit VC are as follows:

  <1> Set the ABR bit to 1 to indicate that the VC uses the ABR service. The SHAPER NO. field has no meaning for the ABR service, because the ABR service uses the ABR scheduler. This field must always be set to 0.

  <2> Set, in the Rx VC TABLE POINTER field of word 7, the VC NUMBER of a receive VC (VC used to receive a turn-around BRM cell) that is paired with this transmit VC.

  <3> Set the ABR parameter obtained through negotiation. (See **Section 5.8.4**.)

- **Setting the receive VC table**

  The host sets the receive VC table to its initial values. In addition to the settings for the VBR VC table, the host must set values specific to the ABR service. The settings specific to the ABR receive VC are as follows:

  <1> Set the ABR bit to 1 to indicate that the VC uses the ABR service. Also, set the RE bit to 1.

  <2> Set, in the Tx VC TABLE POINTER field of word 7, the VC NUMBER of a transmit VC (VC used to send back a BRM cell) that is paired with this receive VC.

  <3> Set the ABR parameter obtained through negotiation. (See **Section 5.8.4**.)

(6) Setting the receive lookup table entry

It is necessary to specify the receive lookup tale entry, because the ABR service uses a receive VC regardless of whether data is being transmitted or received.

At the data receiving end (destination), a receive pool is allocated in system memory. Setting a receive VC NUMBER in the receive lookup table entry and enabling table entry ready the receiving end for reception (the receive VC becomes active). The structure and behavior of the receive pool are the same as for the VBR VC. See **Section 5.5** for details.

No receive pool is required for the ABR service if it is used only at the data transmitting end (source), when no data cell is received at the turn-around BRM cell receive VC. The μPD98405 does not store RM cells in the receive pool. It only requires that the receive lookup table entry be set.

(7) Tx_Ready command

When the host issues a Tx_Ready command, it makes the ABR transmit VC active, causing the μPD98405 to begin data transmission. The transmission rate used here is adjusted automatically according to the behavior of the source. The receive lookup table entry must be enabled before the Tx_Ready command is issued. The structure of the transmit data is the same as that for the VBR VC. See **Section 5.4** for details.

(8) Processing transmit and receive indications

The μPD98405 posts notification of when data transmission or reception ends, by using an indication. Processing of the indication and mailbox at the end of data transmission or reception is the same as for the VBR VC. See **Section 5.6** for details.

(9) Closing the ABR channel

Transmit and receive VCs are always used as a pair when the ABR service is used. When the host terminates the use of ABR channels, it must close the corresponding transmit and receive VCs in a specified sequence, described below:

<1> Reset the RE bit in the receive VC table.

<2> Close the transmit channel.

<3> Close the receive channel.

- **Resetting the RE bit in the receive VC table**

  To close an ABR channel, it is necessary to first reset the RE bit in the receive VC table to 0. The RE bit is used to specify whether to perform rate calculation/turn-around processing when an BRM/FRM cell is received. If the RE bit is set to 0, the μPD98405 does not access the transmit VC indicated by the Tx VC TABLE POINTER in the receive VC table. When an ABR channel is closed, the transmit VC is closed before the receive VC. When an RM cell is received at a receive VC, if a transmit VC that is accessed has already been closed, a malfunction will occur in the μPD98405.

- **Closing the transmit channel**

  To close an ABR channel, it is necessary to close the transmit VC before the receive VC. Resetting the RE bit disables rate calculation for subsequent RM cell reception, but performing rate calculation for an RM cell received just before the RE bit is reset may cause the μPD98405 to access the receive VC indicated by the Rx VC TABLE POINTER in the transmit VC table. If the receive VC has been closed, however, a malfunction will occur in the μPD98405.

  The ABR transmit channel is closed in the same way as the VBR VC transmit channel. See **Section 5.4.3** for details. A Deactivate_Channel command can also be used to force the transmit channel into the idle state.

- **Closing the receive channel**

  The receive channel must be closed after the transmit channel is closed.

  The ABR receive channel is closed in the same way as the VBR VC receive channel. See **Section 5.5.3** for details. Basically, the ABR receive channel is closed by first disabling the receive lookup table entry and issuing a NOP command twice, followed by the Deactivate_Channel and Close_Channel commands.

5.8.6 Internal Congestion Control

This section explains the internal congestion control that is supported by the μPD98405 using hardware. For the source and destination, the μPD98405 uses hardware to support internal congestion and "Use-it-or-lose-it" (source only) functions.

(1) Source internal congestion

The μPD98405 uses hardware to support internal congestion for the source. The internal congestion supported by the source corresponds to source operations 8 and 14 (see **Section 5.8.2**). If internal congestion is detected under the conditions for source operation 14, the μPD98405 sets internal flag LCI to 1, and reduces the value of ACR. This reduction is not performed for any VC for which the rate is smaller than that of the LCR register. The following explains the internal congestion detection conditions for the source, and ACR reduction.

(Program timer - Service timer) > Time_th0 or sum_of_ACR > C_{ABR} then

if ((Program timer - Service timer) <= Time_th1) then ACR = ACR_tmp

if ((Program timer - Service timer) > Time_th1) then ACR = ACR_tmp*α

ACR_tmp	sum_of_ACR - C_{ABR}
ACR/16	2*C_{ABR} or greater
ACR/8	2*C_{ABR} to C_{ABR}
ACR/4	C_{ABR} to (C_{ABR}-C_{ABR}/4)
ACR/2	(C_{ABR}-C_{ABR}/4) to C_{ABR}/2
ACR-ACR/4	C_{ABR}/2 to C_{ABR}/4
ACR-ACR/8	C_{ABR}/4 to C_{ABR}/8
ACR-ACR/16	C_{ABR}/8 to C_{ABR}/16
ACR	C_{ABR}/16 to 0

Program timer: Internal timer that manages ideal cell transmission

Service timer: Internal timer that manages actual cell transmission

Time_th0, Time_th1: Register settings that control internal congestion detection and ACR reduction

sum_of_ACR: Total of ACRs in active ABR VCs

C_{ABR}: Generic band that can be used with ABR (band excluding that starting from the value set with the AUB register, to the band used with the UBR)

ACR_tmp: Reduced ACR value (value in the above table)

α: $\alpha = 1/2^{alpha}$ (alpha: register setting)

Internal congestion is recognized upon the ACR total exceeding the band that can be used by the ABR (AUB register setting), or upon the detection of the internal timer, that is used to manage cell transmission, going out of synchronization. After the detection of internal congestion, the μPD98405 reduces ACR, based on the above expression, according to the difference between the ACR total and the value of the AUB register.

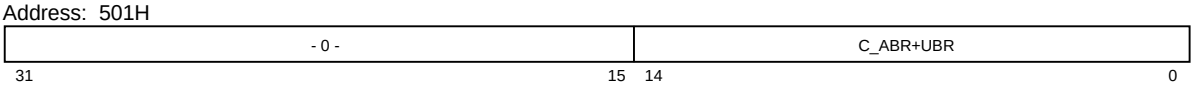
When internal congestion does not occur, the Program timer and Service timer both count up in exactly the same way. Upon the occurrence of internal congestion, the Service timer will lag behind the Program timer. If internal congestion is averted, the operation of the Service timer will follow that of the Program timer. Time_th0 is a threshold value used to detect internal congestion when a difference arises between the Service Timer and the Program Timer. Time_th1 is a threshold value used to determine the rate of reduction for ACR when internal congestion is detected.

The internal timer advances by 1 every 36 system clocks (this clock is input to the SCLK pin). Set Time_th0 and Time_th1 using the value of this counter. For example, to set Time_th1 to 10, a time of 360 system clocks is shown. For every one count that this timer value is delayed, the μPD98405 applies internal control to introduce a delay of one cell time.

The formats of the registers used for detecting internal congestion, and for ACR reduction, are shown below.

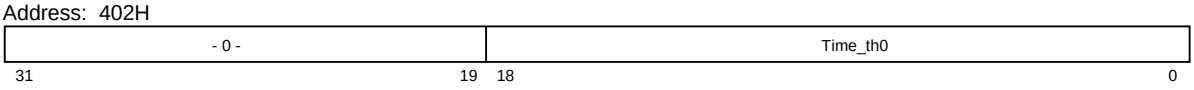
AUB (ABR, UBR band register)

Address: 501H



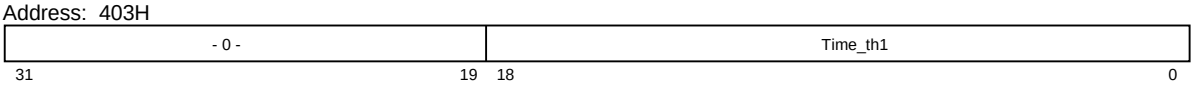
TTH0 (Time threshold register 0)

Address: 402H



TTH1 (Time threshold register 1)

Address: 403H



UBCR (UBR band control register)

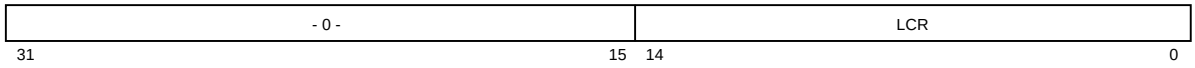
Address: 500H

- **LCR register setting**

  Rate reduction, performed in response to internal congestion, is not applied to those VCs that are transmitting at a rate less than that set in the LCR register. By setting a rate in this register, those VCs that transmit at low rates can be excluded from the rate reduction performed as a result of internal congestion control. When this register is set to the default value of 0, this function is disabled.

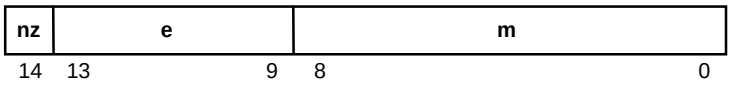
LCR (Internal congestion cell rate register)

Address: 502H



LCR: Set the internal congestion cell rate using the following rate expression.

Rate = 2^e*(1 + m/512)*nz cells/seconds



- **Using source internal congestion**

  This section explains the recommended methods of using the source internal congestion with the μPD98405, and the values to be set in the registers.

  Source internal congestion control is applied by initially setting the TTH0, TTH1, and LCR registers, as well as the alpha parameter of the UBCR register then, when changing the band that can be used by ABR, setting the band in the AUB register. The host can change the values of the TTH0, TTH1, LCR, UBCR, and AUB registers at any time. The settings to be made for each register are explained below.

  - **TTH0 register**

    The TTH0 register, in combination with the AUB register, controls internal congestion detection. To enable the quickest possible detection of internal congestion, it is recommended that TTH0 be set to 0.

  - **TTH1 register, UBCR register alpha parameter**

    The TTH1 register and UBCR register alpha parameter control the rate of ACR reduction, applied after the detection of internal congestion. Although, upon the detection of internal congestion, the μPD98405 performs ACR reduction as described above, it is also possible to reduce the rate by setting the TTH1 register and the UBCR register alpha parameter. Basically, setting TTH1 = 7FFFH eliminates the need to use rate reduction (when the band used by ABR is unusually small, or the number of VCs is extremely large, the rate of ACR reduction performed upon internal congestion can be increased by setting a small value for TTH1 and setting alpha to 1 (α = 1/2)).

- **LCR register**

  Rate reduction based on internal congestion is not applied to any VCs that are transmitting at a rate less than that set in the LCR register. If VCs that are transmitting at a given rate (about 5% of the band that can be used by ABR) are not to be subject to any further rate reduction upon the occurrence of internal congestion, set that rate in LCR.

- **AUB register**

  The μPD98405 uses the value set in the AUB register to detect internal congestion. Also, upon the detection of internal congestion, ACR reduction is performed based on this value. Therefore, it is necessary for the host to set, in the AUB register, the band that can be used by ABR. For example, at the start of VC transmission by the VBR, if the band that can be used by ABR is too small, the value set in the AUB register must exclude the VBR band. However, once the VC of the VBR has finished transmitting, and the band that can be used by the ABR increases, it becomes necessary to set a larger value in the AUB register.

  When the VBR is not being used, the full band can be used with the ABR. Therefore, a band of 149.76 Mbps can be used with ABR (when using the 155.52 Mbps SONET/SDH framer). At this time, set AUB to 149.76 Mbps. Subsequently, for example, if the VC of the VBR starts transmitting at 30 Mbps, the setting for AUB must be changed to 110.76 Mbps. Upon the completion of transmission by that VC, return the setting of AUB to 149.76 Mbps.

  When using both ABR and UBR, set the band that ABR and UBR can use in the AUB register. The μPD98405 automatically assigns the band to the ABR and UBR. For details of assigning a band to the UBR, see **Section 5.9.2**.

(2) Use-it-or-lose-it

The μPD98405 supports a Use-it-or-lose-it function in hardware. The use-it-or-lose-it function supported by the μPD98405 corresponds to source operation number 5 (see **Section 5.8.2**).

The Use-it-or-lose-it function reduces ACR if the calculated ACR is greater than the actual rate. Upon detecting Use-it-or-lose-it the μPD98405 reduces ACR to ACR*15/16. The conditions related to Use-it-or-lose-it are given bleow.

First, in order to display the actual rate, the μPD98405 displays the average in-rate FRM cell interval (Ta). This value is obtained using the following expression.

$Ta(t) = a*T + (1 - a)*Ta(t - 1)$

Ta: Average in-rate FRM cell transmission interval (units: cells)

a: $a = 1/2^{a0}$ (a0: register setting)

T: Interval between current and previous in-rate FRM cell transmission (units: cells)

The Use-it-or-lose-it detection conditions are as follows.

C_{link}*Nrm/ACR <= Ta*b

C_{link}: Link capacity (149.76 Mbps)

b: b = 1 - $1/2^{b0}$ (b0: Register setting)

The a and b parameters used for Use-it-or-lose-it control can be set to a value within the following ranges.

a: (1, 0.5, 0.25, 0.125, 0.0625, 0.03125, 0.015625, 0.0078125)

b: (0, 0.5, 0.75, 0.875, 0.9375, 0.96875, 0.984375, 0.9921875)

Every time a larger value is set for a, the actual rate is newly calculated and applied. Similarly, every time a smaller value is set for b, if a difference arises between ACR and the actual rate, the margin by which ACR is reduced to ACR*15/16 is enlarged.

NEC recommends that the Use-it-or-lose-it parameters be set to a = 1 and b = 0.96875 (a0 = 0, b0 = 5).

The format of the register used for the Use-it-or-lose-it function is shown below. The default values are a0 = 1, b0 = 1. NEC recommends setting a0 = 0 and b0 = 5.

ULR (Use-it-or-lose-it register)

Address: 405H

31 – 6	5 – 3	2 – 0
- 0 -	a0	b0

(3) Destination internal congestion

The μPD98405 supports destination internal congestion in hardware. The destination internal congestion supported by the μPD98405 corresponds to destination operations 2-c and 2-d (see **Section 5.8.2**). Upon detecting internal congestion at the destination, the μPD98405 sets CI = 1 for the BRM cell and outputs notification of congestion. Congestion of a receive FIFO is detected based on the number of cells accumulated by that FIFO. The host can set, in cell units in the RFTH register, the number of FIFO-accumulated cells that correspond to internal congestion. The format of the RFTH register is shown below. The default for this register is 7FH which, when set, disables this function.

In order to use this function, set a value of up to 96 in this register (the size of the built-in receive FIFO of the μPD98405 is equal to 96 cells).

RFTH (Receive FIFO threshold register)

Address: 404H

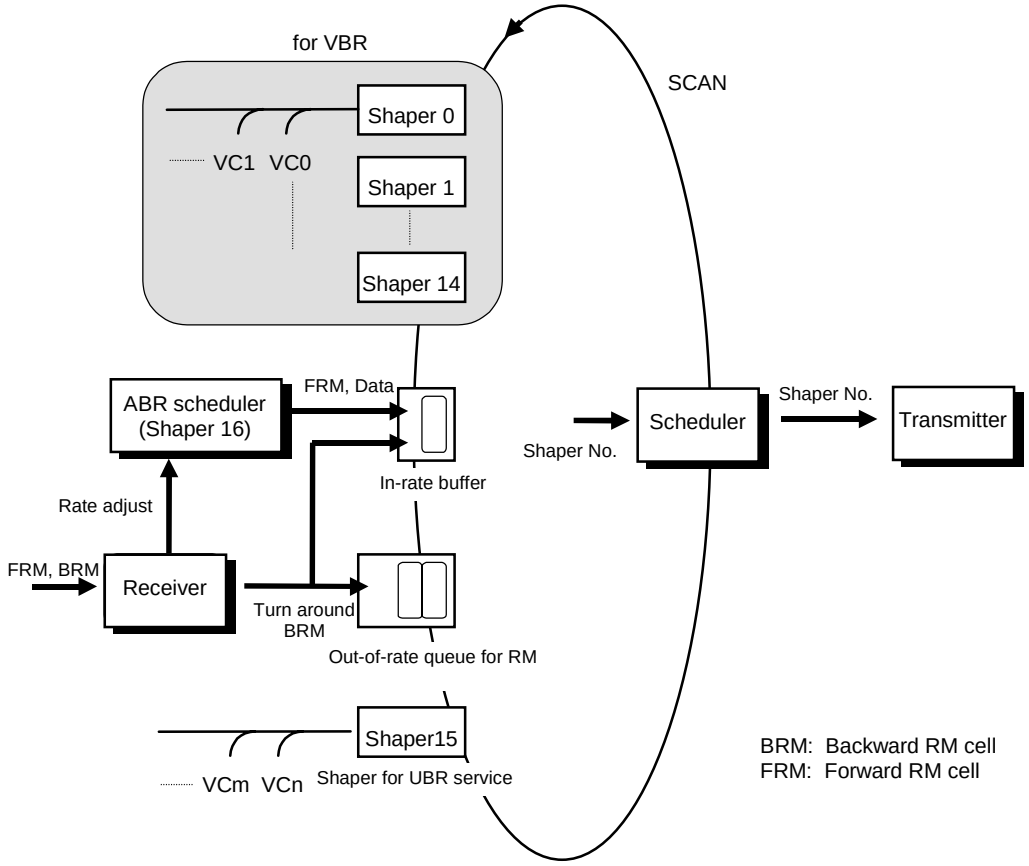
31 – 7	6 – 0
- 0 -	rfifo_th

5.8.7 ABR Behavior

(1) ABR scheduling

A brief description of how ABR scheduling is performed is given below:

Figure 5-49. ABR Scheduling Overview



The ABR scheduler schedules transmit cells for the ABR service. The ABR scheduler determines the data cell rate and the type of cells (FRM cell, BRM cell, or data cell) to be transmitted depending on the behavior of the source or destination (see **Section 5.8.2**). The ABR scheduler has an in-rate buffer and out-of-rate queue, and stores the FRM or BRM cell into the corresponding queue depending on the behavior of the source or destination. Data cells are stored in the in-rate buffer.

The ABR scheduler is handled as shaper 16. The μPD98405 has an in-rate buffer and out-of-rate queue in the ABR scheduler. The in-rate buffer and out-of-rate queue have their own priority registers, and the host specifies a priority in these registers. Usually, the in-rate buffer is assigned a higher priority than the out-of-rate queue. The host must assign the ABR scheduler (for both the in-rate buffer and out-of-rate queue) a priority lower than that of the shaper used for VBR but higher than that of the shaper used for UBR.

The scheduler that supervises both the VBR shapers and ABR schedulers searches through the VBR shapers and ABR schedulers to select a shaper having the cell to be transmitted next and issues a request to the transmitter to send the cell.

(2) Processing RM cells

The μPD98405 internally processes all the RM cells used for the ABR service. The host need not specify anything for the RM cells. Indeed, it need not process them at all. The μPD98405 processes RM cells differently depending on the behavior of the source or destination. For testing purposes, however, the host can cause an RM cell to include congestion information (using a Set_Rx_Congestion command), as well as cause RM cells to be transmitted (using a BRM_Tx command).

- **Processing RM cells on the source side**

  The μPD98405 transmits an FRM cell at regular intervals. It also enables the automatic transmission of an out-of-rate FRM cell at the TCR rate. When the μPD98405 receives the BRM cell, it changes the transmission rate according to the BRM cell information. This is performed as a source operation. The host need not prepare FRM cell data in the transmit buffer in system memory.

- **Processing RM cells on the destination side**

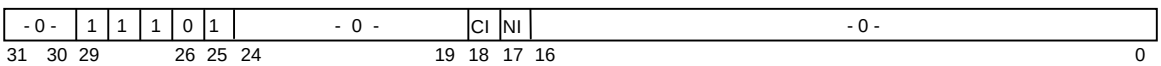
  Upon receiving an FRM cell, the μPD98405 automatically returns a BRM cell. This is performed as a destination operation. A received FRM cell is not stored into the receive pool in system memory. Instead, it is processed within the μPD98405.

5.8.8 ABR Command

The μPD98405 is provided with ABR service host commands for testing. Using these commands, the host causes a BRM cell to include congestion information and a non-turn-around BRM cell to be transmitted. In addition to these commands, setting the ECI, ENI, ERenb, and EER fields of the receive VC table can cause a BRM cell to include congestion information (see **Figure 5-35 in Section 5.5.3**).

(1) Set_Rx_Congestion command (for testing)

Command register programming



Parameter description

CI: This is the CI bit of a BRM cell. Once this bit is set to 1, the CI bit of a BRM cell sent back from any channel is set to 1.

NI: This is the NI bit of a BRM cell. Once this bit is set to 1, the NI bit of a BRM cell sent back from any channel is set to 1.

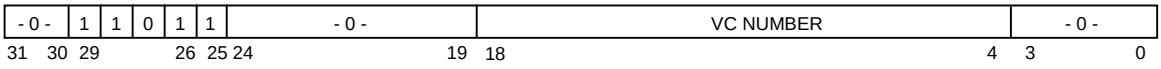
Command description

Using the Set_Rx_Congestion command, the host forcibly sets the CI and NI bits of a BRM cell, sent back from any channel, for testing purposes. When the Set_Rx_Congestion command is issued, the μPD98405 ORs the CI and NI bits of the command with the CI and NI bits of a BRM cell, and sets the result of ORing in the CI and NI bits of the BRM cell to be sent back. Once this command has been issued, it remains effective until it is cleared. To clear the function of this command, it is necessary to issue another Set_Rx_Congestion command with the CI and NI bits reset to 0.

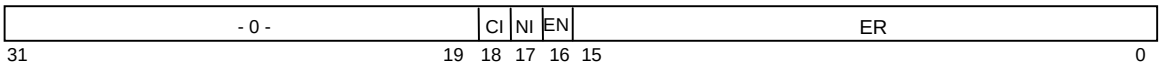
(2) BRM_Tx command (for testing)

Command register programming

CMR



CER



Parameter description

VC NUMBER: Number of a transmit VC used to transmit an out-of-rate BRM cell

CI: CI bit of a BRM cell

NI: NI bit of a BRM cell

EN: Enable ER field

1: Enable

0: Disable

ER: ER field of a BRM cell (explicit rate)

Command description

The BRM_Tx command is a test command used for transmitting one out-of-rate BRM cell (non-turn-around BRM cell). Once the BRM_Tx command has been issued, the μPD98405 transmits one out-of-rate BRM cell from the transmit VC specified in the VC NUMBER field. The contents of this BRM cell are prepared based on the parameters specified in the CER. If the EN bit indicates "disable," the ER value that the μPD98405 saves for the receive VC when the command is issued is set in the ER field. If the EN bit indicates "enable," a value in the ER field specified in the CER is set in the ER field.

(3) BRM_Tx indication

Command register contents

Undefined	VC NUMBER	- 0 -
31 19	18 4	3 0

Parameter

VC NUMBER (bit 18-bit 4): Contains the number of the transmit VC of the channel that transmitted the out-of-rate BRM cell. When this band contains 0, it indicates that the μPD98405 rejected the issued BRM_Tx command (due to the processing of another BRM_Tx command not yet having been completed). Thus, to obtain VC NUMBER, the host must issue the BRM_Tx command repeatedly.

Indication

To indicate execution of the BRM_Tx command, the μPD98405 stores VC NUMBER of the transmit VC table of the corresponding channel into the command register.

There are occasions when the μPD98405 will return 0 as the BRM_Tx command indication. This occurs because the processing of another BRM_Tx command has not yet ended, causing the most-recently issued BRM_Tx command to be rejected, and preventing the transmission of an out-of-rate BRM cell. In this case, the host must continue to issue the BRM_Tx command until it can obtain VC NUMBER of the transmit VC that is to transmit the out-of-rate BRM cell.

5.9 UBR FUNCTION

5.9.1 UBR Service Processing

The μPD98405 supports the UBR service. To enable the use of the UBR service, it is necessary to perform the following in addition to the VBR processing.

- Setting a shaper
- Setting the SCR register

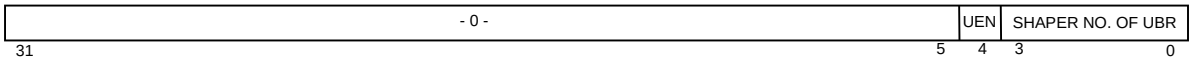
(1) Setting a shaper

A VBR shaper (one of shapers 0 to 15) is used for the UBR service. The host must set the parameters for a shaper to be used for the UBR service. The priority of this shaper must be the lowest.

(2) Setting the SCR register

The host must set the number of a shaper to be used for UBR service in the SCR register, and set the enable bit of the SCR register to 1. The use of the shaper as a VBR shaper is thus disabled.

The format of the SCR register is as follows:



SHAPER NO. OF UBR: Number of a shaper to be used for the UBR service

UEN: Enable bit for the UBR service

★ **Remark** It is necessary to set the SCR register when using the ABR and UBR services together. It is not necessary to set the SCR register when using the VBR and UBR services together, or when using the UBR service alone.

5.9.2 UBR Bands

The UBR service has no mechanism for guaranteeing cell transfer. So, no band is assigned to it in advance. If both VBR and UBR exist, any bands that are not assigned to the VBR are used for the UBR. If the VBR, ABR, and UBR exist, any bands that are not assigned to the VBR are shared between the ABR and UBR. In this case, a band may become unavailable to the UBR service, which has the lowest priority, because the ABR service changes the rate dynamically. The μPD98405 is provided with a function that can assign some bands to the UBR even in such situations.

When the ABR and UBR exist, the UBCR register is used to assign bands to the UBR. The format of the UBCR register is as follows:

Nubr_th	- 0 -	alpha	- 0 -	beta2	beta1
31 16	15 12	11 8	7 6	5 3	2 0

Nubr_th: Number of UBR service VCs. Nubr_th is used as the threshold value in calculation of the band allocated to UBR.

Initial value after a reset: 0

alpha: Used for ABR internal congestion control. Sets the proportion by which the rate will be reduced in response to internal congestion. (See **Section 5.8.6**.)

Initial value after a reset: 0

beta2: β2, that is, the ratio of bands to be assigned to the UBR when the number of actual active UBR VCs is greater than Nubr_th

$\beta 2 = 1/2^{beta2}$

Initial value after a reset: 0

beta1: β1, that is, the ratio of bands to be assigned to the UBR when the number of actual active UBR VCs is less than Nubr_th

$\beta 1 = 1 - 1/2^{beta1}$

Initial value after a reset: 7

The bands to be assigned to the UBR are obtained using the following:

if (n_ubr = 0) then $C_{ABR} = C_{ABR+UBR}$

$C_{UBR} = 0$

if (0 < n_ubr < Nubr_th) then $C_{ABR} = (C_{ABR+UBR} - \text{sum of MCR}) * \beta 1 + \text{sum of MCR}$

$C_{UBR} = (C_{ABR+UBR} - \text{sum of MCR}) * (1 - \beta 1)$

if (n_ubr ≥ Nubr_th) then $C_{ABR} = (C_{ABR+UBR} - \text{sum of MCR}) * \beta 2 + \text{sum of MCR}$

$C_{UBR} = (C_{ABR+UBR} - \text{sum of MCR}) * (1 - \beta 2)$

n_ubr: Actual active UBR VCs

C_{ABR}: ABR band

C_{UBR}: UBR band

$C_{ABR+UBR}$: ABR and UBR bands (value in the AUB register)

sum of MCR: MCR total

β1: $\beta 1 = 1 - 1/2^{beta1}$

β2: $\beta 2 = 1/2^{beta2}$

The ranges of the values set for the parameters in the above expressions are:

β1: (0, 0.5, 0.75, 0.85, 0.9375, 0.96875, 0.984375, 0.9921875)

β2: (1, 0.5, 0.25, 0.125, 0.0625, 0.03125, 0.015625, 0.0078125)

Nubr_th: (0 to 65,535)

As can be seen from the above expressions, Nubr_th must be set to 0, if bands need not be assigned to the UBR at all. To assign some bands to the UBR, it is necessary to set the number of UBR service VCs, in Nubr_th. The ratio of bands to be assigned to the UBR is specified as β1 and β2. The Nubr_th parameter is used to set the threshold value (number of VCs) that determines the ratio of bands to be assigned to the UBR when the number of UBR VCs is greater or lesser than Nubr_th. β1 is a parameter applied when the number of actual active UBR VCs is less than Nubr_th. The smaller the value of β1, the larger the band to be assigned to the UBR. β2 is a parameter applied when the number of actual active UBR VCs is greater than Nubr_th. The smaller the value of β2, the larger the band to be assigned to the UBR.

No matter what value is set in Nubr_th, β1, or β2, these expressions guarantee the band for the MCR (minimum cell rate) for the ABR service VCs.

5.10 COMMANDS

The host controls the μPD98405 using the nine commands listed in Table 5-10. These commands can be issued in either of two different modes, a mode in which the built-in command FIFO is used (use-command-FIFO mode) and a mode in which the built-in command FIFO is not used (not-use-command-FIFO mode). The host specifies either command issuing mode, by setting the CFE bit of the GMR register. Setting the CFE bit to 1 selects use-command-FIFO mode. This mode can be used only in PCI mode. In Generic mode, only not-use-command-FIFO mode can be used. In Generic mode, the CFE bit must be set to 0. This bit must not be reset while the μPD98405 is operating.

The command issuing mode specified at initialization cannot be re-selected.

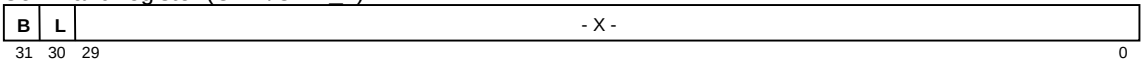
Table 5-10. Commands

Command name
Open_Channel command
Close_Channel command
Deactivate_Channel command
Tx_Ready command
Add_Batches command
NOP command
Indirect_Access command
Set_Rx_Congestion command
BRM_Tx command

(1) Command register (CMR) and command extension register (CER)

Commands are input to the μPD98405 via the command register and command extension register. Each register has two addresses: CMR and CMR_L, and CER and CER_L, respectively. The table below indicates the correspondence between the registers and addresses. The command register has a "busy flag" and "lock flag" that function as command status flags.

Command register (CMR/CMR_L)



B bit: Busy flag

L bit: Lock flag

X: Command code, parameter

Command extension register (CER/CER_L)

Name	Register name	Address	
		Word address mode	Byte address mode
Command register	CMR	08H	20H
	CMR_L	09H	24H
Command extension register	CER	0AH	28H
	CER_L	0BH	2CH

The μPD98405 uses different registers depending on whether it is controlled by a single host CPU in a single-host system or by two or more host CPUs in a multi-host system.

<1> In a single-host system

When the host issues commands to the μPD98405, only CMR and CER of the command and command extension registers are effective. CMR_L and CER_L are not used.

<2> In a multi-host system

When the host CPUs issue commands to the μPD98405, all the command and command extension registers, CMR, CMR_L, CER, and CER_L, are used.

(2) Commands returning command indication

When an Open_Channel or Close_Channel command is executed, the μPD98405 stores a command indication to the command register.

When the host has issued a command having a command indication, it reads the command register to obtain the command indication. The μPD98405 stores the command indication to the command register upon the completion of command execution. The B bit being set to "1" indicates that the command has not yet been completed, and that the command indication has not been stored to the command register. When the B bit is set to "0," the command indication is stored to the command register. The host polls the command register until the B bit is cleared to "0."

(3) Commands using command extension register

The Indirect_Access and Add_Batches commands use the command extension register because these commands require that parameters be set.

When data is written, it is first written to the command extension register, after which a command is set to the command register. As soon as the data has been written to the command register, the μPD98405 executes the command. Consequently, the data in the command extension register must be changed before the command register is written.

When data is read, a command is written to the command register, and the host takes over the data stored to the command extension register (indication) once execution of the command has been completed. The μPD98405 stores data to the command extension register once execution of the command has been completed. The host reads the command extension register after it has confirmed that the B bit has been cleared to "0."

The parameters to be set to the CER register depend on the command to be executed. For details, see the description of each command.

5.10.1 Not-Use-Command-FIFO Mode

If the CFE bit of the GMR register is set to 0, the host is in not-use-command-FIFO mode. In Generic mode, the CFE bit must be set to 0 so that commands are issued in not-use-command-FIFO mode.

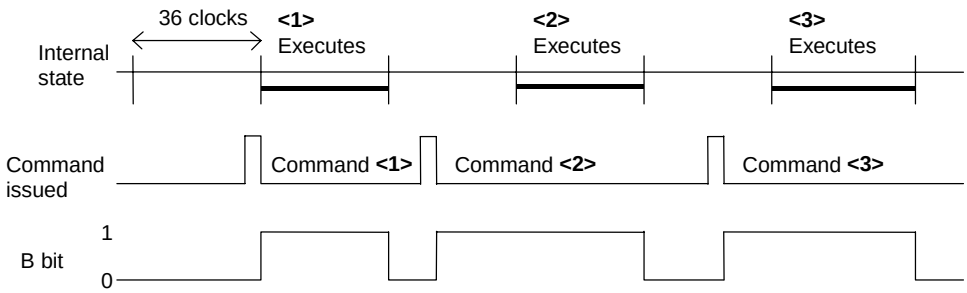
(1) Busy flag

The host writes commands to the command register together with appropriate parameters.

The μPD98405 internal operation is performed in units of states, each of which is equivalent to 36 system clocks. The μPD98405 receives a command from the host in one state, then executes that command in the next state. Because the μPD98405 can execute no more than one command in each state, whenever it receives a command, it sets bit 31 (B bit) of the command register to "1," indicating that the next state is busy. In other words, this B bit functions as a busy flag that indicates that the μPD98405 is executing a command.

While the B bit is set to "1," the μPD98405 cannot receive a command. Even if the command register is overwritten with a new command while the B bit is set to 1, the μPD98405 regards that command as being invalid and ignores it. The host can issue a new command only when the B bit is set to "0." The μPD98405 clears the B bit to "0" upon the completion of command execution in the state next to that in which it received the command.

Figure 5-50. Command Issue and B Bit



Therefore, the host must confirm that the B bit is set to "0" (that the preceding command has been completed) by reading the command register once before issuing a new command. Or, it must wait for at least 2 states (72 clocks) after issuing a command before issuing the next command.

★ **Remark** Command execution may take over 72 clock cycles when using ABR. Check that the B bit = 0 before executing the next instruction when using ABR.

(2) Lock flag (supporting a multi-host system)

In a multi-host system where the μPD98405 is controlled by two or more host CPUs, bit 30 (L bit) of the command register is used. The L bit functions as a lock flag that prevents two or more host CPUs from writing a command to the μPD98405 before the completion of command execution by another host.

For example, suppose that one μPD98405 is controlled by two host CPUs, and that both host CPUs attempt to write a command to the CMR register. The two hosts first read CMR and confirm that the B bit is not set to "1" (that the μPD98405 is not busy). Next, each host writes its command to the CMR register. As a result, one host will write its command over the command written by the other host.

To prevent this from happening, the L bit at the 30th bit position of the CMR register functions as a lock flag that indicates that another host is now accessing the CMR register. When the L bit is set to 1, it indicates the locked state, that is, that another host is executing a command and the μPD98405 cannot accept another command. When the L bit is set to 0, it means that no other host is executing a command.

To set or reset the lock flag or L bit, the two addresses of each of the command and command extension registers are used. The μPD98405 is locked or unlocked as listed in Table 5-11 when the hosts access the respective registers. In the busy state, however, the lock/unlock state is not changed regardless of which register is accessed. For example, the μPD98405 will not be unlocked if both the B and L bits, obtained by reading CMR_L, are 1.

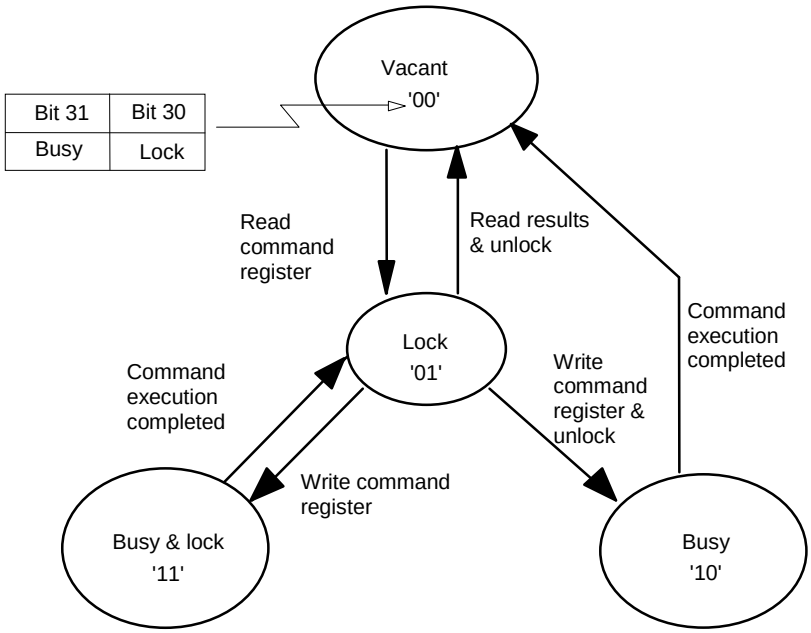
Table 5-11. L Bit State Transition due to Register Access

Operation	L bit state transition	Read	Write
Lock	0 → 1	CMR CMR_L CER CER_L	CMR_L
Unlock	1 → 0	CMR_L CER_L	CMR
Kept locked	1 → 1	CMR CER	CMR_L CER CER_L
Kept unlocked	0 → 0	–	CMR CER CER_L

All the hosts read CMR before issuing a command, each of the hosts being restricted such that it is granted the right to issue a command only while the L bit is set to "0." While the L bit is set to "1," the host must wait until it is cleared to "0." The host granted the right to issue a command locks the μPD98405 by keeping the L bit set to "1" until the completion of command execution. Once execution of the command has been completed, the host is responsible for clearing the L bit to "0" to unlock the μPD98405.

It is also possible to execute the next command while the L bit remains set to "1." The user can give a host a priority higher than that of another host by maintaining the lock status.

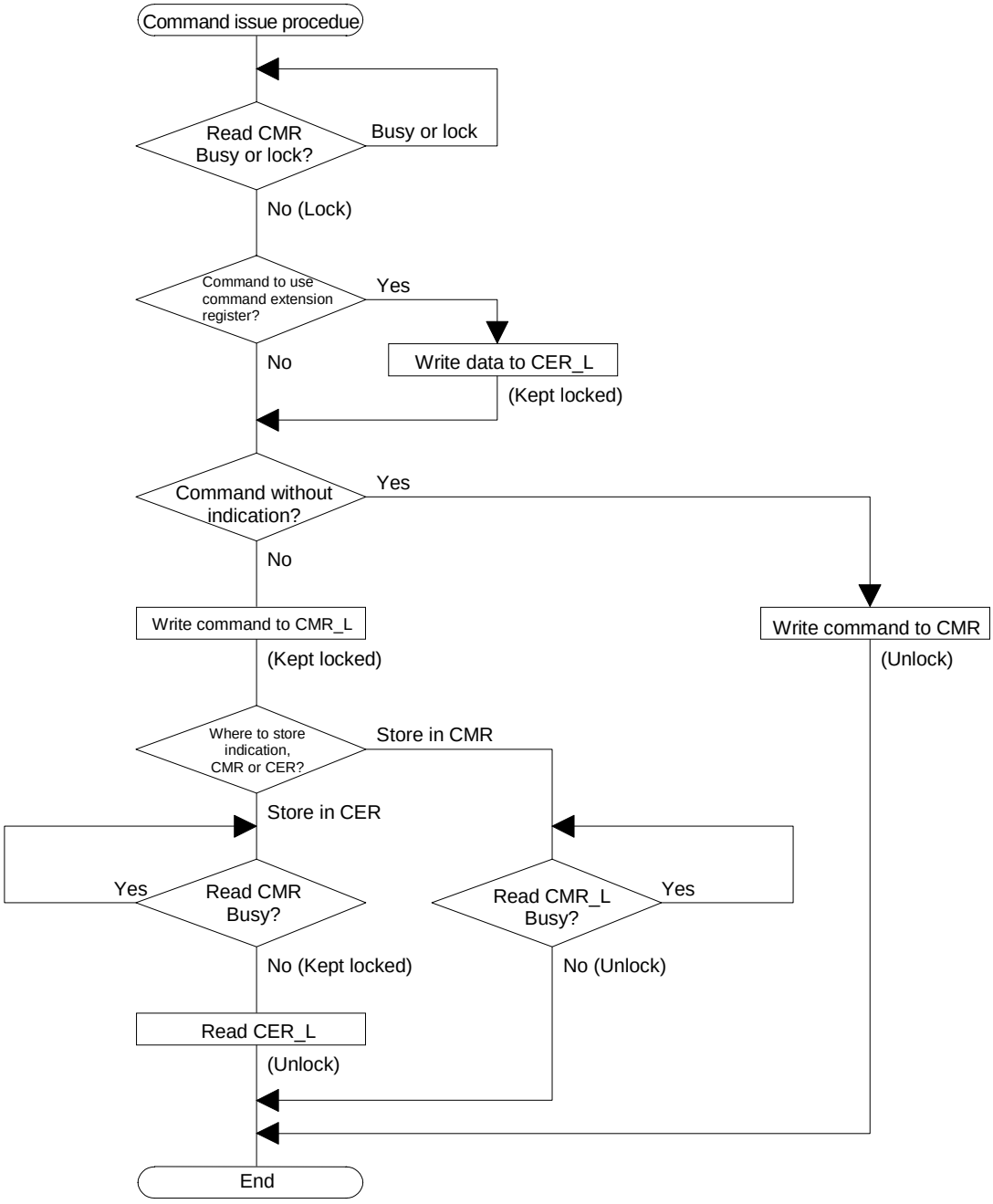
Figure 5-51. Status Transition of Command Register



(3) Example of issuing commands in a multi-host system

The following flowchart shows how commands are issued in a multi-host system. It is only an example. There is no need to follow the order shown in the example when actually issuing commands.

Figure 5-52. Flow of Command Issue (Not-Use-Command-FIFO Mode, Multi-Host)



5.10.2 Use-Command-FIFO Mode

If the CFE bit of the GMR register is set to 1, commands are issued in use-command-FIFO mode. This mode is valid only in PCI mode. In Generic mode, the CFE bit must be set to 0 so that commands are issued in not-use-command-FIFO mode.

The μPD98405 has a built-in command FIFO that can accommodate up to 20 host commands (10 CMR commands and 10 CER commands). By using the command FIFO, the host can issue commands without checking the busy bit, thus improving system performance.

When the host is about to issue a command (that is, about to access the CMR, CMR_L, CER, or CER_L in slave mode), if the command FIFO is full, the μPD98405 executes target termination using retry control at the PCI interface. In addition, the host can detect whether the command FIFO is busy. Reading the command FIFO register (CFR) enables detection of the number of commands in the command FIFO.

(1) Busy flag

The busy flag (B bit) indicates that the μPD98405 has a command for which a response will be returned (an indication in the command FIFO) or executed. The μPD98405 sets the B bit to 1 only when the host has issued a command for which an indication will be issued as a response. The B bit remains set to 1 not only when the command is being executed but also when the command FIFO contains a command for which an indication will be issued as a response.

For those commands for which an indication will not be issued as a response, the B bit is not set to 1. The host can issue such a command at any time without checking the B bit. It need not check the end of the command either.

After issuing a command for which an indication will be issued as a response, the host checks the B bit. If the B bit is set to 0, the μPD98405 terminates command execution and stores the indication. If the host has issued a command for which an indication will be issued as a response, and if the B bit is set to 1, no more commands for which an indication will be issued as a response can be issued. Before issuing such a command, it is necessary to wait until the completion of the previous command and receive the corresponding indication. A command for which an indication will not be issued as a response can be issued at any time even if the B bit is set to 1. Table 5-12 lists those commands for which an indication is issued as a response, as well as those that will not.

Table 5-12. Commands for Which an Indication Is Issued as a Response/Not Issued

Command for which indication is issued	Command for which indication is not issued
Open_Channel command	Deactivate_Channel command
Close_Channel command	Tx_Ready command
Indirect_Access read command	Add_Batches command
BRM_Tx command	NOP command
	Indirect_Access write command
	Set_Rx_Congestion command

(2) Lock flag (multi-host system support)

Bit 30 (L bit) of the command register is used in a multi-host system, in which the μPD98405 is controlled by more than one host CPU. The L bit functions as a lock flag to prevent each of the hosts from writing a command for which an indication is issued before a similar command, issued by another host, has terminated. When the L bit is set to 1, it indicates the locked state, that is, that another host is executing a command. When the L bit is set to 0, it means that no other host is executing a command.

The two addresses in the command register and command expansion register are used to set and reset the L bit, being used as the lock flag. Table 5-13 lists whether the hosts are in a locked state when they read-access their respective registers. Write-accessing these registers does not affect the locked/unlocked state. In the busy state, accessing a register does not cause transition from the locked state to the unlocked state, or vice versa. For example, if the B and L bits are set to 1 when the CMR_L is read, the locked state is maintained.

Table 5-13. L Bit State Transition due to Register Read-Access

Operation	L bit state transition	Read
Lock	0 → 1	CMR CMR_L CER CER_L
Unlock	1 → 0	CMR_L CER_L
Kept locked	1 → 1	CMR CER
Kept unlocked	0 → 0	–

Before issuing a command for which an indication will be returned, or using the command extension register (CER), all of the hosts are required to read the CMR register. A host has the right to issue a command only when the L bit of the CMR register is found to be 0. If the L bit is set to 1, the hosts must wait until the L bit becomes 0. Once a host obtains the right to issue a command, the host keeps the L bit set to 1 until it finishes executing the command. When a host receives an indication corresponding to the command it issued, it resets the L bit to 0 for unlocking.

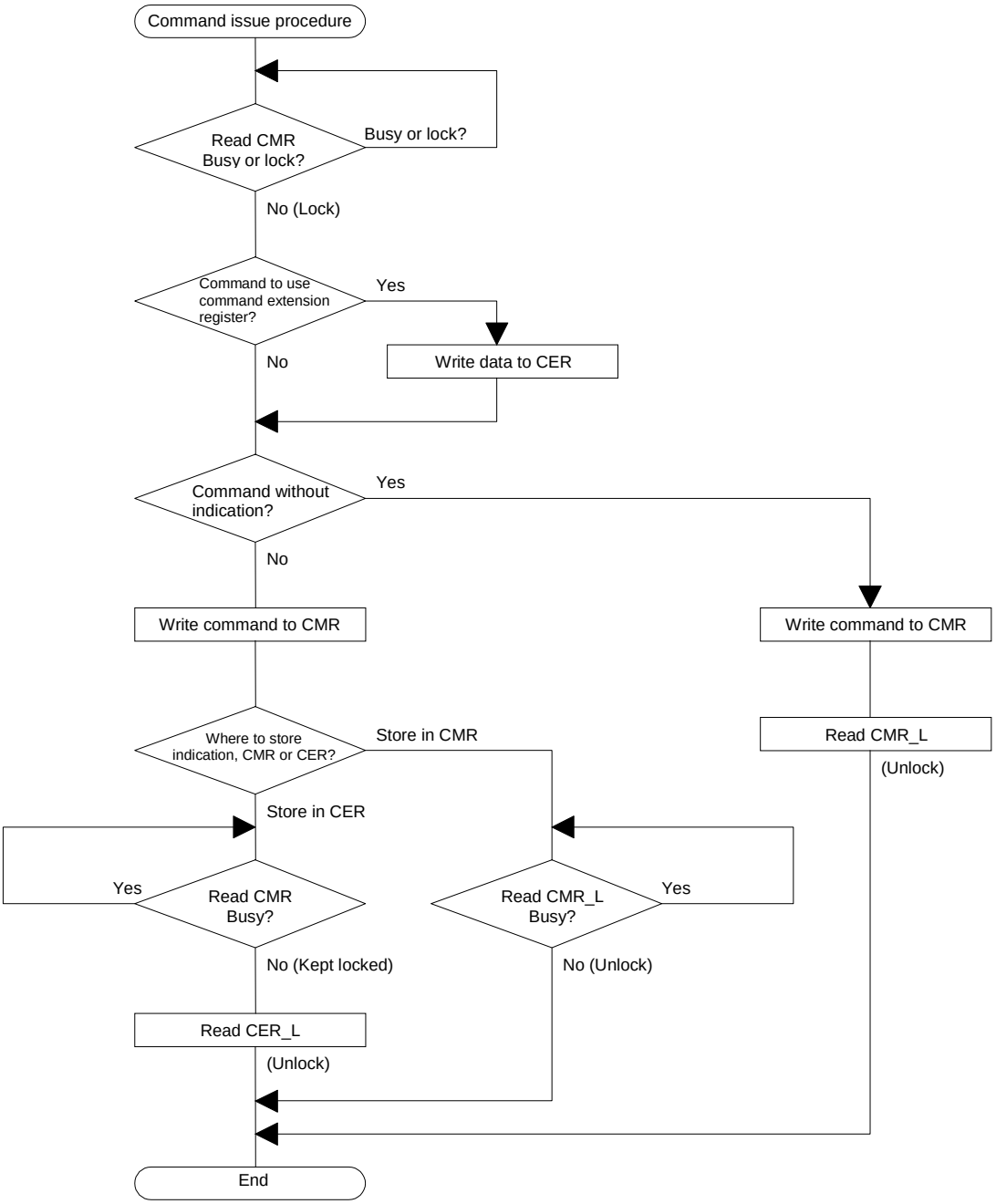
Some accesses enable a command shift with the L bit setting held to 1. By maintaining the locked state, the user can allow one host to take precedence over the others in issuing commands.

For commands that do not return an indication, and those commands that do not use the command extension register (CER), the hosts do not have to check either the L bit or the B bit. A host can issue a command for which no indication will be issued at any time, regardless of whether the host is in the locked or busy state. Once issued, a command is stored in the command FIFO. A command for which an indication will not be issued can be issued at any time, but once it has been issued, the command register must not be read-accessed. Read-accessing the command register causes transition between locked and unlocked states, while write-accessing does not.

(3) Example of issuing commands in a multi-host system

The following flowchart shows the way in which commands for which an indication will be issued and those that use the command extension register (CER) are issued in a multi-host system. Commands for which an indication is not issued or those that do not use the command extension register (CER) can be issued at any time without checking for the locked and busy states. This flowchart is only an example. There is no need to follow the order shown in the example when actually issuing commands.

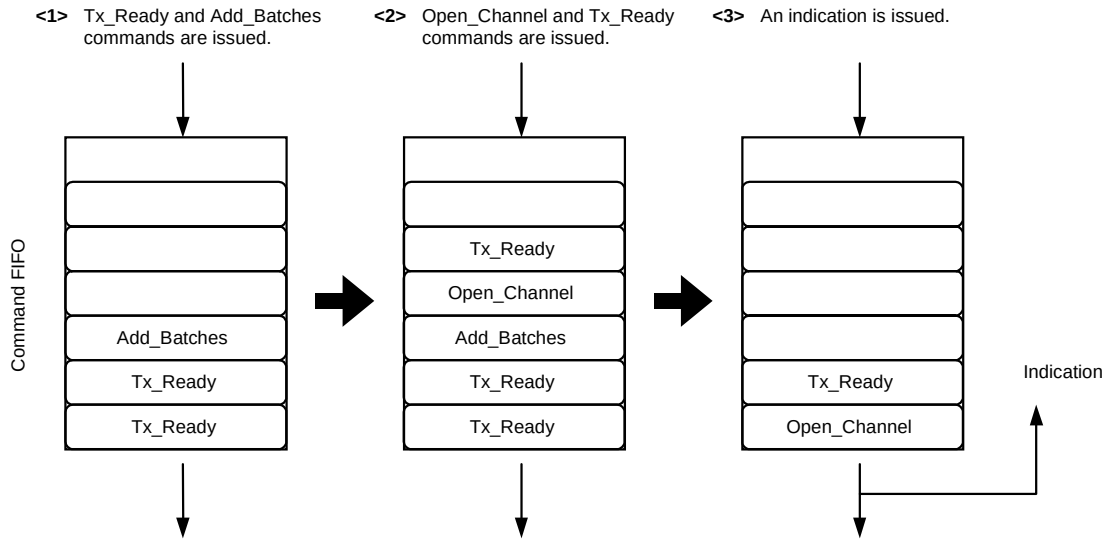
Figure 5-53. Flow of Command Issue (Use-Command-FIFO Mode, Multi-Host)



(4) Command FIFO state

The following figure and paragraphs explain how commands are stored into the command FIFO and the way that the μPD98405 executes those commands (for the single-host system).

Figure 5-54. Command FIFO State



<1> The host can issue commands for which an indication will not be issued, such as Tx_Ready and Add_Batches, at any time. These commands are stored into the command FIFO and are executed by the μPD98405 as required.

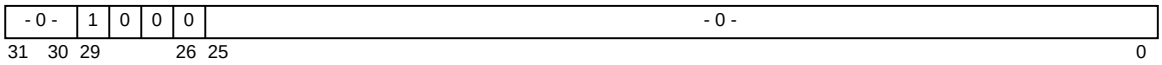
<2> When the host issues a command for which an indication will be issued, such as Open_Channel, it also is stored into the command FIFO. The busy flag in the command register is set at the same time as the command is stored into the command FIFO. If the command FIFO contains at least one command for which an indication will be issued (that has not been executed), the host is not allowed to issue any more such commands. A command for which an indication will not be issued, such as Tx_Ready, can be issued at any time.

<3> A stored Open_Channel command is executed only once all the commands that were previously stored into the command FIFO have been executed. The μPD98405 informs the host of when it has completed the execution of the Open_Channel command, by using an indication. Upon reading this command, the host issues another command for which an indication will be issued as a response. If the command FIFO already contains other commands when the host issues an Open_Channel command, it takes longer for the indication to return.

5.10.3 Command Description

(1) Open_Channel command

Programming of command register

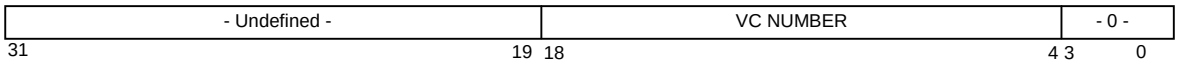


Command description

The Open_Channel command is used to open a new channel to be used for transmission or reception. Once the μPD98405 has received this command, it stores the contents of the TOS register to the command register, and stores the contents to the CMR register as an Open_Channel indication. Subsequently, the contents of the TOS register are updated to the value indicated by "FORWARD POINTER" of the VC table. This command is used for both transmission and reception.

(1-1) Open_Channel indication

Contents of command register



Parameter description

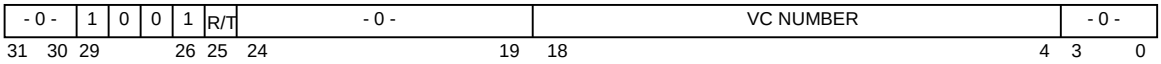
VC NUMBER (bits 4 through 18): VC NUMBER of VC table for the new channel
If this area contains 0, a new channel cannot be opened.

Indication description

When the μPD98405 executes an Open_Channel command, it stores part of the start address (VC NUMBER) of the new VC table as an indication to the command register. The μPD98405 stores this indication to the command register upon the completion of Open_Channel command execution. The host confirms that the B bit is set to 0 and receives the indication after issuing the Open_Channel command.
If "0000" is added to the low-order 4 bits of this parameter, the parameter is used as a physical address indicating Word 0 of the VC table in control memory.

(2) Close_Channel command

Programming of command register



Parameter description

R/T: Indicates whether the receive or transmit channel is to be closed.

1: Receive channel

0: Transmit channel

VC NUMBER (bits 4 through 18): VC NUMBER of the channel to be closed

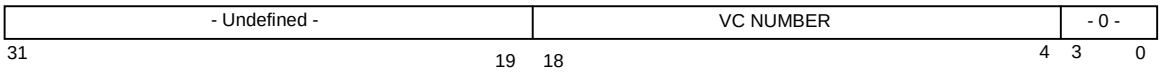
Command description

The Close_Channel command is used to close a receive or transmit channel.

When the μPD98405 receives this command, it returns the specified VC table to the free block pool and updates the contents of the TOS register so that they indicate the specified VC table.

(2-1) Close_Channel indication

Contents of command register



Parameter description

VC NUMBER (bits 18 through 4): Stores the VC NUMBER of the VC table of the closed channel. If this area contains 0, it indicates that the μPD98405 has rejected the issued Close_Channel command. The host repeatedly issues the Close_Channel command until it obtains VC NUMBER.

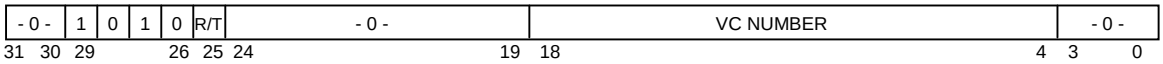
Indication description

When the Close_Channel command is issued, the μPD98405 stores the VC NUMBER of the VC table of the closed channel to the command register as an indication. The μPD98405 stores this indication into the command register once execution of the Close_Channel command has been completed. After issuing the Close_Channel command, the host confirms that the B bit is set to 0, and then receives the indication.

The μPD98405 may return "0" as the indication of the Close_Channel command. This indicates that the specified channel could not be closed. Should this occur, the host must repeatedly issue the Close_Channel command until it obtains the "VC NUMBER" of the VC to be closed.

(3) Deactivate_Channel command

Programming of command register



Parameter description

R/T: Indicates whether a receive or transmit channel is to be deactivated.

1: Receive channel

0: Transmit channel

VC NUMBER (bits 4 through 18): VC NUMBER of channel to be deactivated

Command description

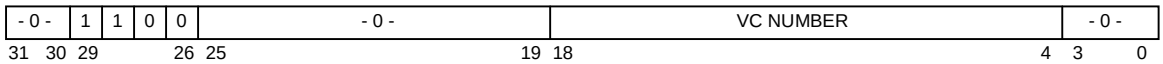
The Deactivate_Channel command shifts the transmit and receive channels from the active to the idle state. In this case, the transmit and receive channels behave a little differently from each other. See **Sections 5.4.3** and **5.5.3** for details.

To deactivate the receive channel, the host must disable the lookup table entry for the channel, wait for a period equal to 72 clock pulses, then issue a Deactivate_Channel command. The wait timing of 72 clock pulses can be generated by issuing two NOP commands continuously.

Remark Upon the completion of the execution of the Deactivate_Channel command, the μPD98405 stores the corresponding receive indication (containing the status code) into the receive mailbox.

(4) Tx_Ready command

Programming of command register



Parameter description

VC NUMBER (bits 4 through 18): VC NUMBER of a channel for which the μPD98405 starts transmission.

Command description

The Tx_Ready command is used by the host to notify the μPD98405 that a transmit packet has been added to this channel (i.e., a new packet descriptor has been added to the transmit queue). The μPD98405 makes the targeted transmit VC table active and starts transmission once it has received the Tx_Ready command.

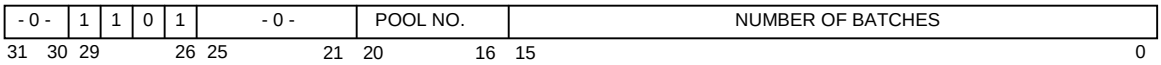
Until a packet descriptor in which the V bit is set to 0 is reached, the μPD98405 maintains the channel in the active state and transmits packets continuously. Therefore, one Tx_Ready command need not always be issued for one transmit packet.

For example, if the Tx_Ready command is issued with three valid packet descriptors arranged consecutively in the transmit queue, the μPD98405 transmits the three packets and then enters the idle status. The μPD98405 ignores the Tx_Ready command that is issued to the channel in the active status such that the transmit operation for that channel is not affected.

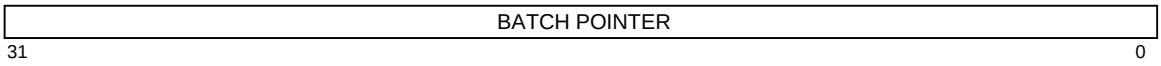
(5) Add_Batches command

Programming of command register

CMR



CER



Parameter description

POOL NO.: Specifies pool number 0 to 31 (0000B to 11111B).

NUMBER OF BATCHES: Writes the number of batches to be newly added.

BATCH POINTER: Writes the first address of the first batch of the batch list to be newly added.

Command description

The host uses the Add_Batches command to add unused batches to one of the 32 receive free buffer pools. This command is used to manipulate the command extension register (CER/CER_L). The host first writes "BATCH POINTER" to the command extension register, then writes a command to the command register (CMR/CMR_L).

Before issuing an Add_Batches command, the host must perform some tasks. The host allocates a batch to be added and the related buffer in system memory. If more than one batch is to be added, they must be linked to one another in advance. The host writes the link pointer, at the last batch in the existing batch list in the pool, to the start address of the batches. Once this task has been completed, the host can issue the Add_Batches command.

The operation of the μPD98405 after receiving the Add_Batches command differs depending on whether any unused batches remain in the targeted pool at that time.

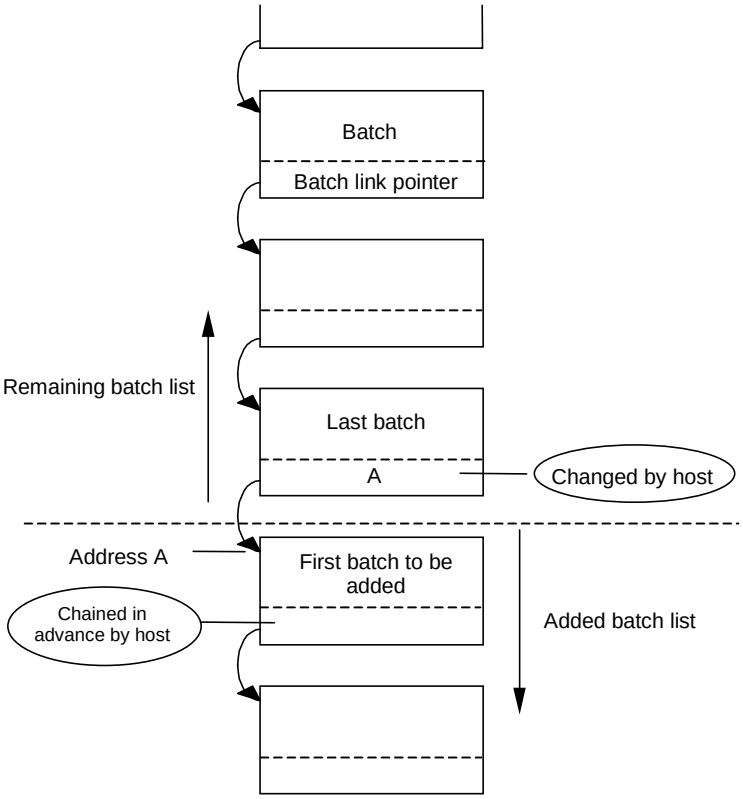
(a) If any unused batches remain in the pool

(If "REMAINING NUMBER OF BATCHES" of the pool descriptor is set to other than "0")

The μPD98405 adds batches by number set in "NUMBER OF BATCHES" to "REMAINING NUMBER OF BATCHES" of the pool descriptor. At this time, the "batch link pointer" of the remaining batches must be changed to the first address of the batches to be newly added (see **Figure 5-55**).

The batches to be newly added must be chained by the link pointer.

Figure 5-55. Host Operation before Issue of Add_Batches Command



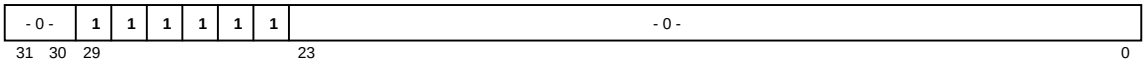
(b) When pool is empty

(When "REMAINING NUMBER OF BATCHES" of the pool descriptor is "0" = RQU status)

If the Add_Batches command is received when the pool is empty, the "NUMBER OF BATCHES" and "BATCH POINTER" of the command are loaded to the "REMAINING NO. OF BATCHES" and "ADDRESS" fields of the pool descriptor in control memory.

(6) NOP command

Programming of command register



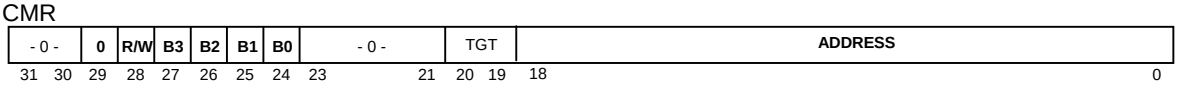
Command description

The NOP command is used by the host to delay the execution of the other commands (such as the Deactivate_Channel command). Upon receiving this command, the μPD98405 stops its internal operation for a period equal to at least 36 clock pulses.

(7) Indirect_Access command

Programming of command register

CMR



CER

Parameter description

R/W: Specifies whether the target is accessed for read or write

1: Read

0: Write

B0, B1, B2, B3: Byte enable bits for write access. The B3 bit corresponds to the highest byte, while the B0 bit corresponds to the lowest byte.

1: Enable

0: Disable

These bits are effective only during access to control memory, the scheduler register, and shaper pointer entry. They cannot be used when write-accessing other indirect registers. The settings of these bits are ineffective for read access. All 32-bit data is read into the CER.

TGT (Target): Specifies the target device.

'00' : Control memory

'01' : Indirect address register

'11', '10' : Internal PHY register or external PHY layer device

ADDRESS: Address output to the target device

DATA: Contents written by the host to the specified address during write.

During read, the contents received from the target to be addressed are stored by the μPD98405.

Command description

The Indirect_Access command is used by the host to read/write the following target devices.

- Indirect address register
- Control memory
- Internal PHY register or external PHY layer device

This command is used together with the command extension register (CER/CER_L).

During write access, the host stores the data to be written to the target device to the command extension register. It then writes the command to the command register. The μPD98405 starts a write cycle for the target device upon receiving this command.

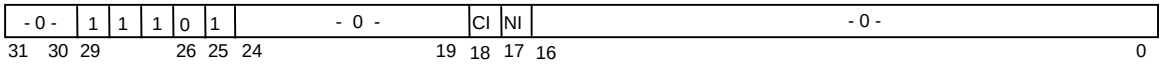
During read access, the host writes the command to the command register. The μPD98405 executes a read cycle for the target device, and stores the requested data to the command extension register. The host confirms that execution of the command has been completed, and reads the command extension register.

The read/write cycle started by the Indirect_Access command differs depending on the target device. The cycle for accessing an internal indirect address register or PHY register of the μPD98405 is executed by using the internal bus of the μPD98405. The cycle for accessing control memory is executed by using the control memory interface. The cycle for accessing the external PHY layer device is executed by using the address lines (CA18 through CA0) and data lines (CD31 through CD0) of the control memory interface, and the control signals (PHOE_B, PHCE_B, and PHRW_B) of the PHY layer device interface.

When the data bus of the PHY layer device is connected to part of the control memory interface, the user establishes a correspondence between the locations of the data to be read from or written to the command extension register, and the connected signals. For example, if the data bus of the PHY layer device is 8 bits wide and connected to CD7 through CD0 of the control memory interface, the host sets data in low-order bits 7 through 0 of the command extension register. The high-order 24 bits are ignored during a write, undefined values being stored to them during a read.

(8) Set_Rx_Congestion command (for testing)

Programming of command register



Parameter description

CI: This is the CI bit of a BRM cell. Once this bit has been set to 1, the CI bit of a BRM cell returned from any channel is set to 1.

NI: This is the NI bit of a BRM cell. Once this bit has been set to 1, the NI bit of a BRM cell returned from any channel is set to 1.

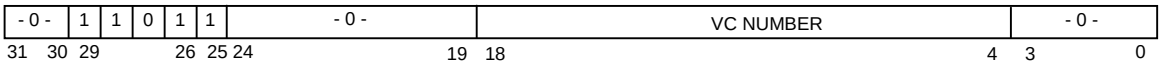
Command description

With the Set_Rx_Congestion command, the host forcibly sets the CI and NI bits of a BRM cell returned from any channel for testing purposes. When the Set_Rx_Congestion command is issued, the μPD98405 ORs the CI and NI bits of the command with the CI and NI bits of a BRM cell, and sets the result of ORing in the CI and NI bits of the BRM cell to be sent back. Once this command is issued, it remains effective until it is cleared. To clear this command, it is necessary to issue another Set_Rx_Congestion command with the CI and NI bits reset to 0.

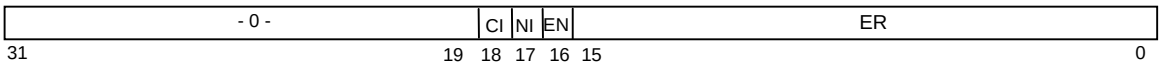
(9) BRM_Tx command (for testing)

Programming of command register

CMR



CER



Parameter description

VC NUMBER: Number of a transmit VC used to transmit an out-of-rate BRM cell

CI: CI bit of a BRM cell

NI: NI bit of a BRM cell

EN: Enable ER field

1: Enable

0: Disable

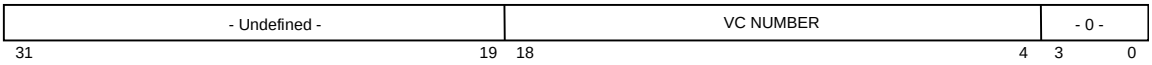
ER: ER field of a BRM cell (explicit rate)

Command description

The BRM_Tx command is a test command for transmitting one out-of-rate BRM cell (non-turn-around BRM cell). Once the BRM_Tx command has been issued, the μPD98405 transmits one out-of-rate BRM cell from the transmit VC specified in the VC NUMBER field. The contents of this BRM cell are prepared based on the parameters specified in the CER. If the EN bit indicates "disable," the ER value saved by the μPD98405 for the receive VC when the command is issued is set in the ER field. If the EN bit indicates "enable," the value in the ER field specified in the CER is set in the ER field.

(9-1) BRM_Tx indication

Command register contents



Parameter

VC NUMBER (bit 18-bit 4): Contains the number of the transmit VC of the channel that transmitted the out-of-rate BRM cell. When this band contains 0, it indicates that the μPD98405 rejected the issued BRM_Tx command (due to the processing of another BRM_Tx command not yet having been completed). Thus, to obtain VC NUMBER, the host must issue the BRM_Tx command repeatedly.

Indication

To indicate execution of the BRM_Tx command, the μPD98405 stores VC NUMBER of the transmit VC table of the corresponding channel into the command register.

There are occasions when the μPD98405 will return 0 as the BRM_Tx command indication. This occurs because the processing of another BRM_Tx command has not yet ended, causing the most-recently issued BRM_Tx command to be rejected, and preventing the transmission of an out-of-rate BRM cell. In this case, the host must continue to issue the BRM_Tx command until it can obtain VC NUMBER of the transmit VC that is to transmit the out-of-rate BRM cell.

5.11 MIB COUNTER

The μPD98405 has four 32-bit MIB counters for ATM layer statistical information. These counters are described below.

- Receive cell counter: ATM ILMI MIB
  Number of cells received on the ATM layer (excluding unassigned/idle cells and cells having invalid VPI/VCI values)
  Register name: RCC
- Transmit cell counter: ATM ILMI MIB
  Number of cells transmitted from the ATM layer (excluding unassigned/idle cells)
  Register name: TCC
- Invalid VPI/VCI receive cell error counter: ATM ILMI MIB
  Number of cells received but discarded because they have invalid VPI/VCI values
  Register name: RUEC
- Received-but-discarded-cell counter
  Number of cells received but discarded because of internal congestion (receive buffer underflow and receive FIFO overrun)
  Register name: RIDC

These counter registers are cleared upon a reset and whenever the host read-accesses them. They are read-accessed separately for clearing, that is, any register that is not accessed remains uncleared. When a counter overflows, the μPD98405 issues an interrupt to inform the host of the overflow, and sets the relevant bit to 1 in the MIB field of the GSR register. The counter restarts counting from 0.

Remark ATM ILMI MIB (ATM Interim Local Management Interface Management Information Base): MIB defined by the ATM Forum UNI.

5.12 INTERRUPT FUNCTION

The μPD98405 has one open-drain interrupt output pin (INTR_B). This pin can be set to active status by several sources. Each interrupt source is allocated to the corresponding bit of the GSR register. When an interrupt source is generated, the corresponding bit of this register is set to 1.

The bits of the GSR register correspond to the bits of each interrupt mask register IMR. When a bit of the GSR register is set, the interrupt pin becomes active only when the corresponding bit of the IMR register is set to 1.

An interrupt can also be activated by setting the corresponding IMR register bit to 1, thus unmasking the interrupt, when the corresponding bit of the GSR register has already been set to 1.

The GSR register is cleared to 0 each time it has been read by the host. If the same interrupt source is generated when an interrupt has been issued and before the host clears the GSR register by reading it, the bit of the GSR register is overwritten to 1.

After a reset, all the bits of the GSR and IMR registers are cleared to 0, and all the interrupt sources are masked.

Of the 32 bits of the GSR register, the PI bit for PHY interrupt is used to input an interrupt of an external device such as internal and external PHY layer devices. When the PHY interrupt becoming active is detected, the PI bit is set, and the interrupt is issued to the host. In response, the host issues the Indirect_Access command, accesses the PHY registers or the register of the external PHY layer device, and reads the detailed interrupt source as data.

For details of the GSR and IMR registers, see **Sections 7.2 (2)** and **(3)**.

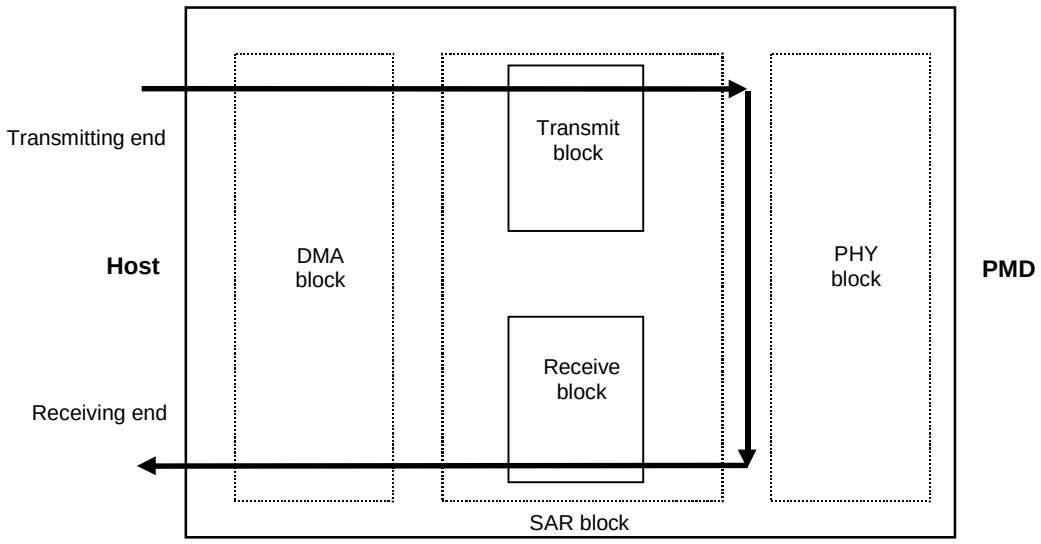
5.13 LOOPBACK FUNCTION

The μPD98405 supports a loopback function for testing. This function is executed by setting the LP bit of the GMR register to 1. While the loopback function is activated, the μPD98405 sends data it has received from the host to the PHY layer via the transmission block, returns it in the internal circuit of the PHY layer interface, and sends it back to the host via the reception block (see **Figure 5-56**). A transmit/receive indication is also issued normally. During loopback, the transmit data is not sent out to the PHY layer or the outside.

Remark The μPD98405 has two loopback modes in the PHY block also. These loopback modes are indicated in the LP (1:0) bit of the MDR2 register. Thus, the μPD98405 has a total of three different loopback modes.

★ The SAR loopback function and RPLP mode of PHY loopback can be used at the same time.

Figure 5-56. SAR Loopback Function



5.14 GLOBAL SHUTDOWN FUNCTION

Global shutdown is executed by setting the SDM bit of the VRR register. The μPD98405 stops the current processing of all receive VCs once it has received this instruction. Subsequently, the μPD98405 does not receive cells and stops its reception processing function. The transmission function is not affected and continues operating, however.

Upon the completion of reception processing, the RD bit of the GSR register is set to 1, and an interrupt is issued to the host provided it is not masked.

The reception function of the μPD98405 cannot be enabled again once this command has been issued to the μPD98405. To subsequently activate the function again, a software reset or hardware reset must be executed for the μPD98405.

★ **Caution The global shutdown function cannot be used.**
Set the SDM bit of the VRR register to 0.

[MEMO]

CHAPTER 6 PHY FUNCTION

The PHY function of the μPD98405 inserts an ATM cell received from the ATM layer into the 155 Mbps SONET STS-3c/SDH STM-1 frame and outputs it to the circuit side, or extracts an ATM cell from the received SONET/SDH frame and outputs it to the ATM layer.

Caution The μPD98405 sequentially transmits the data bit string of the SONET/SDH framer from the PMD interface, starting from the MSB. Note that, in this manual, the bit names in a byte in the overhead of the SONET/SDH framer are referred to in the following two ways.

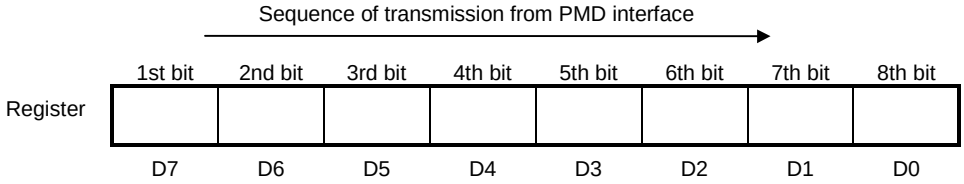
(1) First bit to eighth bit

This notation is mainly used to indicate the bit string of the overhead byte in the SONET/SDH frame, and depends on the order of the output from the PMD interface.

(2) D7 bit to D0 bit

This notation is mainly used to indicate the bits in an internal register of the μPD98405, and refers to pins D7 through D0 of the external management interface.

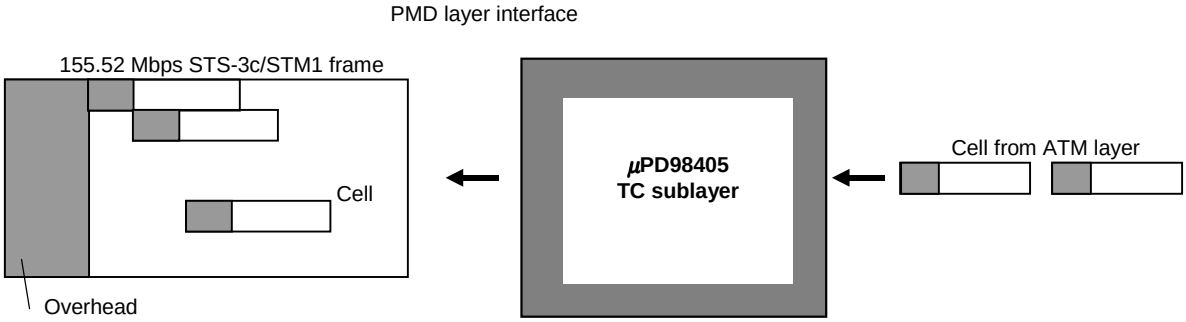
- Notation used for bits in internal register



6.1 TRANSMISSION FUNCTION

The transmission function of the μPD98405 inserts the ATM cell received from the ATM layer into the SONET STS-3c/SDH STM-1 frame, then outputs it to the PMD interface. This section explains the frame transmission function of the μPD98405, based mainly on the processing flow.

Figure 6-1. Outline of μPD98405 Frame Transmission Function



When power is first applied, the μPD98405 starts operating in the mode specified by the default value of each mode register, and transmits the STS-3c frame, until the value of the mode register is changed. At this time, the μPD98405 inserts an idle cell (empty cell) into the frame then transmits the cell, until it receives an ATM cell from the ATM layer.

Figure 6-2. Outline of Frame Format (1/2)

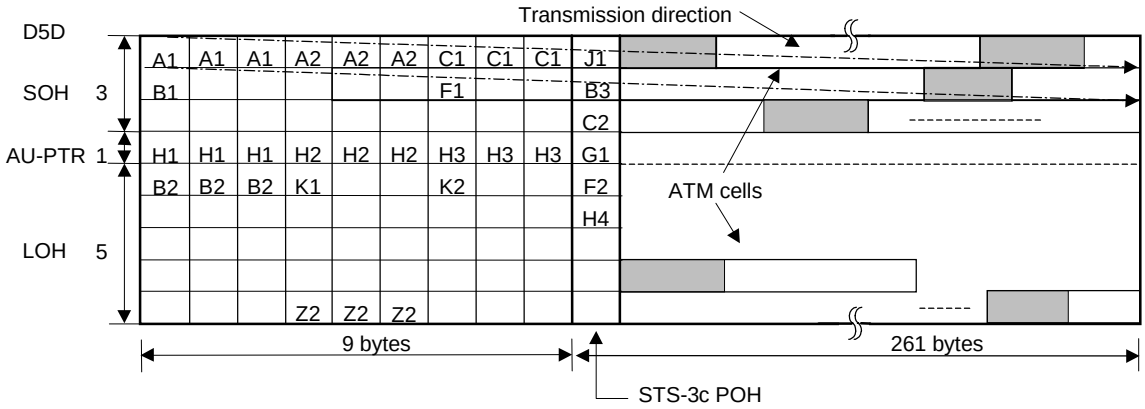


Figure 6-2. Outline of Frame Format (2/2)

A1 (F6)	A1 (F6)	A1 (F6)	A2 (28)	A2 (28)	A2 (28)	C1 (01)	C1 (02)	C1 (03)	J1 (00)
B1 (--)						F1 (00)			B3 (--)
									C2 (13)
H1 (62)	H1 (93)	H1 (93)	H2 (0A)	H2 (FF)	H2 (FF)	H3 (00)	H3 (FF)	H3 (FF)	G1 (--)
B2 (--)	B2 (--)	B2 (--)	K1 (00)			K2 (00)			F2 (00)
									H4 (00)
			Z2 (00)	Z2 (00)	Z2 (--)				

Remark () : Default value for transmission (H)

B1, B2, B3, H2, H3, G1, Z2 : Byte area which is automatically inserted and checked

C1, C2, F1, F2, K1, H4 : Byte area which can be read or written by accessing a register

H1, K2 : Byte area in which some bits can be changed by writing to a register
(Only the SS bit can be rewritten in the H1 byte.)
(The first to fifth bits can be rewritten in the K2 byte.)

Space : Unused byte area. 00H is inserted.

A1, A2: Frame synchronization
C1: Frame identification
B1: Error monitor
F1: User channel
H1, H2, H3: Pointer operation
B2: Error monitor
K1: Selection control
K2: Section alarm indication
Z2: Error report (FEBE)
J1: Path conduction monitor
B3: Error monitor
C2: Path signal identification
G1: Error report (FEBE), path alarm indication
F2: Maintenance channel
H4: Position indication

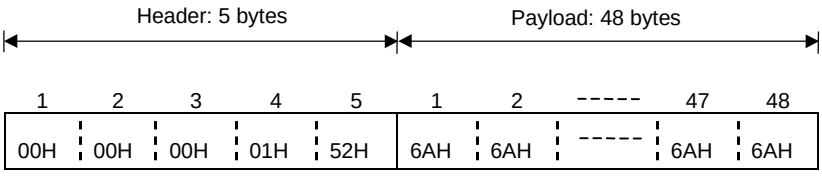
The μPD98405 processes the transmit data in the following sequence.

(1) Reception of cell data from ATM layer

The μPD98405 receives cell data from the ATM layer via the ATM layer interface and stores that data into the transmit FIFO. The transmit FIFO has a capacity of four cells and a buffer function for adjusting the rate between the ATM layer side and PMD side.

While no cell data is being transmitted from the ATM layer and the amount of transmit data remaining in the FIFO falls to less than one cell, an idle cell (empty cell) is inserted. Figure 6-3 shows the format of the idle cell.

Figure 6-3. Format of Idle Cell (Empty Cell)



(2) Creation of HEC

CRC calculation is performed by using the following polynomial expression with the higher four of the five bytes of the ATM cell header. A value of "55H" is added to the result of the CRC calculation, and the result of this addition is inserted into the fifth byte of the ATM header to enable HEC (Header Error Check).

Expression $G(X) = X^8 + X^2 + X + 1$

(3) Scrambling of ATM cell

The data of the ATM cell is scrambled by using the following polynomial expression. The range of the scrambling is limited to the payload of the ATM cell.

Expression $G(X) = X^{43} + 1$

A user can set scramble stop mode to enable testing. Scramble stop mode is set by using the CRCRM bit of mode register 3 (MDR3).

(4) Creation of SONET/SDH frame

The SONET STS-3c/SDH STM-1 frame format is created by multiplexing the overhead information of the SONET/SDH frame with subsequent ATM cells. The μPD98405 creates the H1, H2, H3, K2, Z2, G1, A1, and A2 bytes as frame overhead information and links these bytes to the payload.

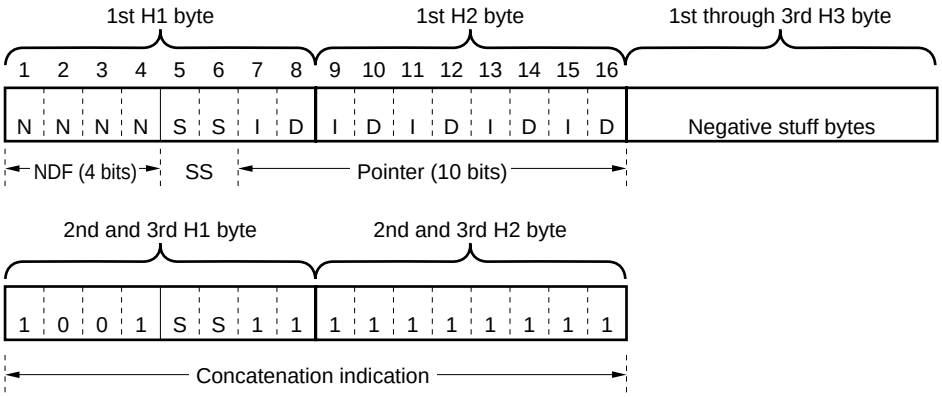
The frame format is shown in **Figure 6-2**.

★ **(a) Creating AU pointer and byte information**

The transmit frame sent out by the μPD98405 does not change the position of POH (Path Overhead). Nor is the position of the J1 byte changed. Therefore, the pointer value to be assigned to the H1 and H2 bytes is always 20AH = “1000001010”, and NDF is fixed to “0110” (disable). The SS bits, which are the fifth and sixth bits of the H1 byte, are “00” as default assumption. These bits can be changed by setting the SS bit table of the MDR1 register.

Because the transmission side does not request Frequency Justification (stuff operation), data is not stored in the H3 byte, which is used as a destuff byte.

Figure 6-4. Format of AU Pointer (H1 through H3 bytes)



Remark NDF : New Data Flag. Enable or disable command when the pointer value is changed. The μPD98405 does not change the pointer value (disable).

SS bit : Indicates the type of the virtual container. Insert the bit stored in the SS table of MDR1. The default value is “00”.

Pointer : Indicates the position of the first byte J1 of POH and indicates Frequency Justification (stuff operation).

I (Increment bit) : Positive Justification (positive stuff) operation request

D (Decrement bit) : Negative Justification (negative stuff) operation request

Concatenation indication : Indicates concatenation.

H1 through H3 Bytes of Transmit Frame

	H1 Byte	H2 Byte	H3 Byte
1st	0110 SS10	0000 1010	0000 0000
2nd	1001 SS11	1111 1111	1111 1111
3rd	1001 SS11	1111 1111	1111 1111

Insert registers are available for bytes J0, Z0, F1, K1, K2, F2, C2, and H4 of the byte information of the overhead. Any value can be stored and transmitted by setting the insert register. The μPD98404 transmits the default value unless changed.

(b) Creating a transmit BIP

The μPD98405 executes BIP (Bit Interleaved Parity) calculation in respect to the transmit data, and inserts the result of the calculation into the positions corresponding to the B1, B2, and B3 bytes of the next transmit overhead data.

BIP calculation for each byte is as follows:

B1: BIP-8 (even parity, 8 bits wide)

BIP-8 calculation is performed for all the bits (including the A1, A2, and C1 bytes after frame scrambling) of the transmit data. The result of the calculation is stored into the overhead B1 byte of the next frame.

B2: BIP-24 (even parity, 24 bits wide)

BIP-24 calculation is performed on the bits, excluding those on lines 1 through 3 in the SOH area of the transmit data (before frame scrambling). The result of the calculation is stored into the overhead B2 byte of the next frame.

B3: BIP-8 (even parity, 8 bits wide)

BIP-8 calculation is performed on all the bytes in the payload (SPE: Synchronous Payload Envelope) of the transmit data (before frame scrambling). The result of the calculation is stored into the overhead B3 byte of the next frame.

(5) Scrambling the STS-3c/SDH STM-1 frame

The STS-3c/SDH STM-1 frame to be transmitted is scrambled by using the polynomial expression shown below. All the ranges of the STS-3c/SDH STM-1 frame, excluding the first nine bytes, "A1 (1), A1 (2), A1 (3), A2 (1), A2 (2), A2 (3), C1 (1), C1 (2), and C1 (3)", are scrambled.

Expression $G(X) = 1 + X^6 + X^7$

The user can set scramble stop mode to enable testing. Scramble stop mode can be set by using the FSCRM bit of mode register 3 (MDR3).

(6) Output from PMD interface

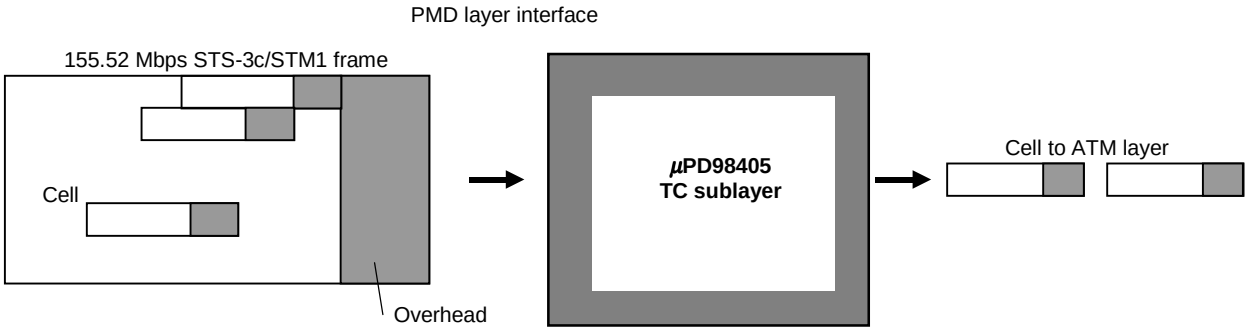
The μPD98405 converts cell data into serial data and outputs it from the PMD interface.

For details of the PMD interface, see **Section 4.5**.

6.2 RECEPTION FUNCTION

The reception function of the μPD98405 extracts the ATM cells from SONET STS-3c/SDH STM-1 frames received from the PMD interface, outputs those cells to the ATM interface side, then passes it to the ATM layer device.

Figure 6-5. Outline of Frame Reception Function of μPD98405



When power is first applied, the μPD98405 immediately starts receiving the frame in the default operation mode.

This section explains the reception function of the μPD98405, based mainly on the processing flow.

The μPD98405 receives data in the following sequence.

(1) Frame reception

The μPD98405 receives the data of the SONET STS-3c/SDH STM-1 frame from the PMD interface.

In serial interface mode, the μPD98405 samples the data signal input to the RDIC/RDIT pin at the clock synchronized with the receive clock generated by internal clock recovery.

For details of the PMD interface, see **Section 4.5**.

(2) Synchronizing of the receive frame

The μPD98405 monitors the bit string of the receive data while frame synchronization is not established. Once it has detected the synchronization pattern (STS-3c/STM-1: 6 bytes) of the A1 and A2 bytes in a bit string, the μPD98405 checks the bit string at the A1 and A2 byte positions in the next frame. If the bit string again conforms to the A1 and A2 byte synchronization pattern, **frame synchronization status (In frame)** is judged to have been established.

Table 6-1. Frame Synchronization Pattern

Frame synchronization pattern	
STS-3c/STM-1	6 bytes (A1, A1, A1, A2, A2, and A2)

Table 6-2. Synchronization Byte

Frame synchronization byte	
A1	11110110 (F6H)
A2	00101000 (28H)

Even in frame synchronization status, the μPD98405 always monitors the A1 and A2 byte positions (6 bytes) of the receive frame. If more than four frames having a pattern different from the A1 and A2 byte patterns are detected at the A1 and A2 byte positions, the frame is judged as being **no longer synchronized (Out Of Frame status)**.

★ Furthermore, the status becomes LOF (Loss OF Frame) if the OOF state lasts for 3 ms. LOF is cleared if frame synchronization lasts for 3 ms.

(3) Descrambling the receive frame

Once synchronization has been established, the received STS-3c/STM-1 frame is descrambled by using the following polynomial expression. All the ranges of the STS-3c/STM-1 frame, excluding the first nine bytes, "A1 (1), A1 (2), A1 (3), A2 (1), A2 (2), A2 (3), C1 (1), C1 (2), and C1 (3)", are descrambled.

Expression $G(X) = 1 + X^6 + X^7$

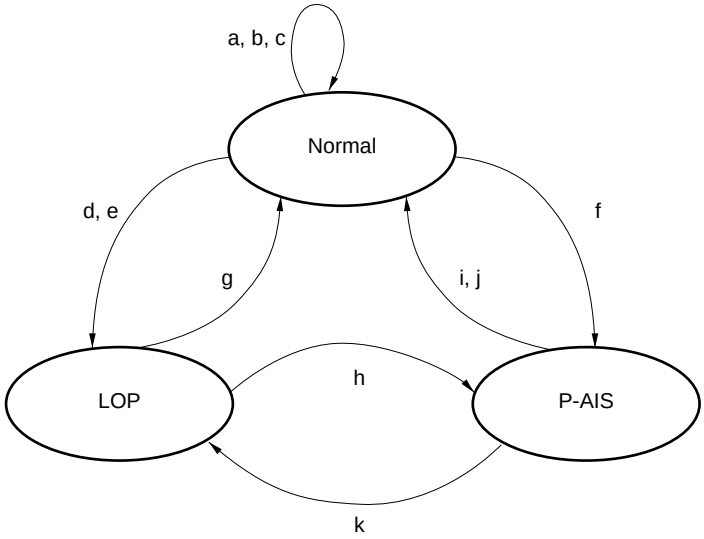
The user can set descramble stop mode to enable testing. Descramble stop mode can be set by using the FSCRM bit of mode register 3 (MDR3).

★ **(4) Pointer processing**

The μPD98405 detects a pointer indicating the first J1 byte address of POH (Path Overhead) from the H1 and H2 bytes of SOH (Section Overhead), to extract the payload area from a receive frame. This pointer is updated each time a frame is received.

The pointer can no longer be updated in the LOP (Loss Of Pointer) status. Moreover, Path AIS is detected from the H1 and H2 bytes of SOH.

Figure 6-6. Pointer Status Transition



Normal status : The received pointer is normal and reception is performed normally.

Path-AIS status : An error occurred in an upstream unit or transmission path, and reception is not performed normally.

LOP status : The received pointer value is abnormal and reception is not performed normally.

Transition		Condition
a	Normal → Normal	NDF Disable + Same valid pointer three times in a row
b		NDF Enable + Valid pointer
c		Positive justification/negative justification
d	Normal → LOP	Eight pointers other than valid pointer in a row
e		Eight NDF Enables in a row
f	Normal → Path-AIS	H1 and H2 bytes are all “1” three times in a row.
g	LOP → Normal	NDF Disable + Same valid pointer three times in a row
h	LOP → Path-AIS	H1 and H2 bytes are all “1” three times in a row.
i	Path-AIS → Normal	NDF Disable + Same valid pointer three times in a row
j		NDF Enable + Valid pointer
k	Path-AIS → LOP	H1 and H2 bytes are not all “1” and eight pointer values in a row that do not satisfy the above conditions i and j.

★ **(5) Reception Frequency Justification (stuff operation)**

Frequency Justification (stuff operation) is detected and the following operation is performed if three or more bits of the I/D bits (5 bits) are inverted during pointer processing (refer to **Figure 6-4 Format of AU Pointer** (**H1 through H3 bytes**).

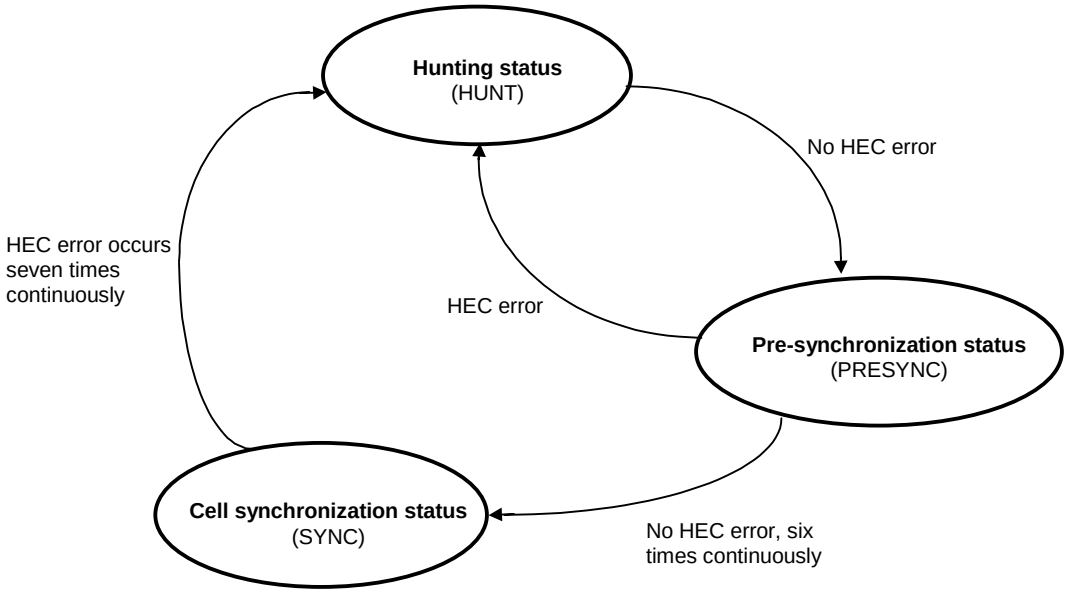
Positive Justification (positive stuff) : The byte at pointer address 0 is not received as payload data if it is detected that three or more bits of I bits are inverted.

Negative Justification (negative stuff) : The H3 byte area is received as payload data if it is detected that three bits or more of the D bits are inverted.

(6) Cell synchronization

To extract an ATM cell from an area excluding the overhead in the SONET STS-3c/SDH STM-1 frame, the cell boundary is detected. If the boundary is detected correctly and the cell is extracted, the cell is synchronized. The cell boundary is detected by HEC (Header Error Check) processing that is included in the header of the cell, as shown in Figure 6-7. The number of protection stages is seven forwards and six backwards.

Figure 6-7. Cell Synchronization Status Transition



- In the hunting status, whether an HEC error has occurred is verified. Once HEC coincides, and HEC without error is detected, the pre-synchronization status is established.
- In the pre-synchronization status, the reception of HEC is repeated until HEC without an error is received six times continuously. If an HEC error is detected, the hunting status is restored.
- In the cell synchronization status, it is judged that cell synchronization is no longer established if an HEC error is detected seven times continuously, and the hunting status is entered.
- Whether cell synchronization is established is indicated by the **OCD (Out of Cell Delineation)** bit of the ACR register.

Table 6-3. OCD Bit

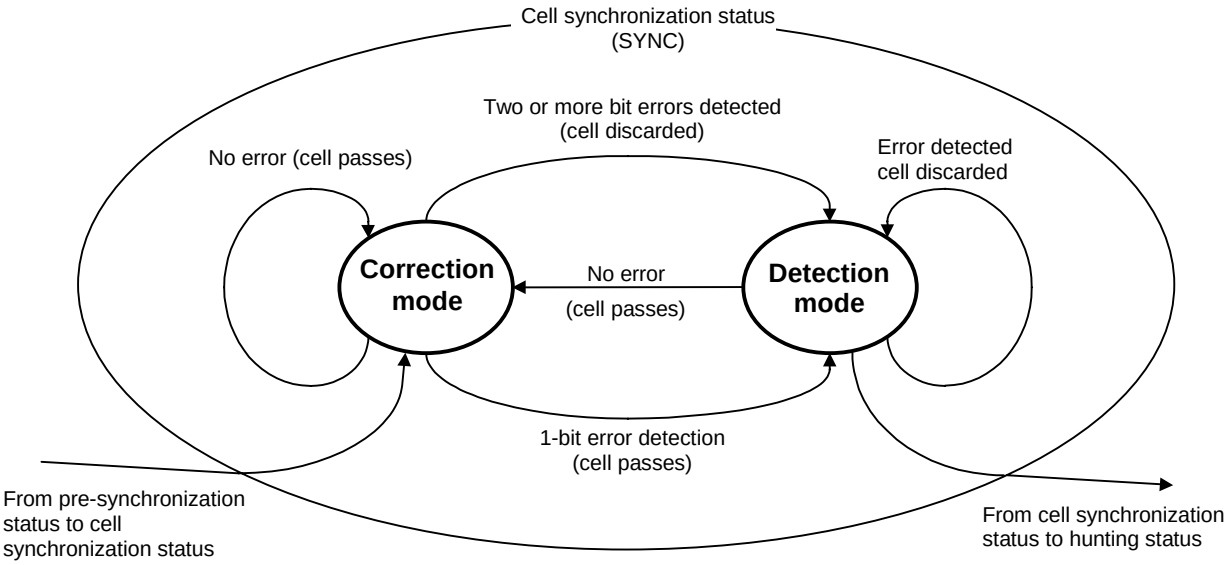
Status	OCD bit
HUNT/PRESYNC status	1
SYNC status	0

- If the OCD status continues for 4 ms, the **LCD (Loss of Cell Delineation) status** is established. LCD is cleared if the cell synchronization status continues for 4 ms.

(7) HEC error detection/correction

While cell synchronization is established, the occurrence of an HEC error is checked. If an HEC error occurs, it is detected and corrected.

Figure 6-8. Transition of HEC Verification Status in Cell Synchronization Status



- Only an error of 1 bit is corrected in correction mode. Then, detection mode is set.
- If an HEC error is detected seven times continuously in detection mode, the status changes from cell synchronization status to hunting status.
- Cell header error controls differ depending on the setting of the HECENB and CORENB bits of mode register 3 (MDR3).

The μPD98405 can update HEC verification processing in the cell synchronization status as follows, depending on the setting of the HECENB and CORENB bits of the MDR3 register.

Table 6-4. HEC Error Correction Mode

HECENB	CORENB	Current mode	Event	Processing	Mode to be set
0	0	Correction mode	No error	Cell processing	Correction mode
			1-bit error detection	Error correction	Detection mode
			Multiple bit error detection	Cell discarded	Detection mode
		Detection mode	No error	Cell processing	Correction mode
			1-bit error detection	Cell discarded	Detection mode
			Multiple bit error detection	Cell discarded	Detection mode
	1	Correction mode	No error	Cell processing	Correction mode
			1-bit error detection	Cell discarded	Detection mode
			Multiple bit error detection	Cell discarded	Detection mode
		Detection mode	No error	Cell processing	Correction mode
			1-bit error detection	Cell discarded	Detection mode
			Multiple bit error detection	Cell discarded	Detection mode
1	x	Correction mode	No error	Cell processing	Correction mode
			1-bit error detection	Cell processing	Detection mode
			Multiple bit error detection	Cell processing	Detection mode
		Detection mode	No error	Cell processing	Correction mode
			1-bit error detection	Cell processing	Detection mode
			Multiple bit error detection	Cell processing	Detection mode

(8) Descrambling of ATM cell

The data of the ATM cell is descrambled in the cell synchronization status by using the following polynomial expression. The range of descrambling is limited to the payload of the ATM cell.

Expression $G(X) = X^{43} + 1$

The user can set descramble stop mode to enable testing. Descramble stop mode can be set by using the CSCRM bit of mode register 3 (MDR3).

(9) Discarding an idle cell (empty cell)

The μPD98405 discards an ATM cell, when the high-order four bytes of the ATM header are "00 00 00 01H", as an idle cell if it receives such a cell.

(10) Unassigned cell discard mode

When the power is first applied, the μPD98405 passes an unassigned cell, while the high-order four bytes of the ATM header are "00 00 00 00H", to the ATM layer as a valid cell, if it receives such a cell. The μPD98405 also supports a mode in which an unassigned cell is discarded if received. To operate the μPD98405 in unassigned cell discard mode, set the CLP bit of both the DCHPR and DCHPMR registers.

*** Functions of the DCHPR and DCHPMR registers**

The CLP field of the receive cell whose VPI/VCI field is all 0 is compared with the contents of the DCHPR register. If the contents of the CLP field coincide with those of the DCHPR register, the cell is discarded. DCHPMR is a register that masks the bits to be compared. If the CLP bit of this register is set to "1", the field of the receive cell is not compared with the CLP bit of DCHPR.

CLP bit of DCHPR	CLP bit of DCHPMR	Discarding of cell
1	0	Idle cell discarded (default mode)
0	0	Unassigned cell discarded
X	1	Idle cell and unassigned cell discarded

(11) Outputting ATM cell from ATM layer interface

To adjust the rate with the ATM layer interface, the ATM cell is stored into a receive FIFO having a capacity of about four cells (256 bytes). The ATM cell can be output to the ATM layer device via the ATM layer interface at any time.

6.3 OAM INFORMATION CONTROL FUNCTION

The μPD98405 has an OAM (Operation And Maintenance) function that is used to maintain and monitor the network. This section explains the OAM function supported by the μPD98405.

6.3.1 Transmission OAM Control

(1) Transmitting an alarm

The μPD98405 transmits an alarm by writing it into a specific overhead area of the transmit frame.

Table 6-5. Transmitting an Alarm

Alarm	Transmission method
Line AIS/Path AIS	Transmitted or canceled by a command
Line RDI Path RDI	• Transmitted or canceled by a command • Automatically transmitted upon occurrence of internal cause (Automatic transmission can be masked.)
Line FEBE/Path FEBE	Automatically generated internally

(a) Transmitting Line AIS (Line Alarm Indication Signal)

Line AIS is a line alarm indication signal that reports, to units downstream, that a fault has been detected upstream and that an alarm has been issued.

The μPD98405 changes the sixth through eighth bits of the K2 byte of the transmit frame to "111" and sets the bits of all areas other than SOH to "1" (before scrambling) for transmission if the LAIS bit of command register 1 (PCMR1) is set to 1. Whether Line AIS is transmitted or transmission is canceled is determined by the user.

Transmit overhead:	K2 byte (6th through 8th bits) = 111, and areas other than SOH = 1
Transmission/cancellation condition:	The host controls the transmission or cancellation of transmission according to the setting of the LAIS bit of command register 1 (PCMR1).

(b) Transmitting Path AIS (Path Alarm Indication Signal)

Path AIS is path remote end receive failure information that reports, to units downstream, that a failure has been detected upstream during relay and that an alarm has been issued.

The μPD98405 changes all the bits of the overhead H1, H2, and H3 bytes of the transmit frame to "1" and, at the same time, changes all the bits in the SPE area (before scrambling) to "1" for transmission, if the PAIS bit of the command register 1 (PCMR1) is set to 1.

Transmit overhead:	H1 through H3 bytes = all "1" & SPE bit area = all "1"
Transmission/cancellation condition:	The host controls transmission or the cancellation of transmission by setting the PAIS bit of command register 1 (PCMR1).

(c) Transmitting Line RDI (FERF) (Line Remote Detect Indication/Far End Receive Failure)

This signal reports, to units upstream, that a line receive failure (LOS, LOF, Line AIS) has been detected.

The μPD98405 sets the sixth through eighth bits of the overhead K2 byte of the transmit frame to "110" for transmission if the LRDI bit of the command register 1 (PCMR1) is set to 1. If an internal cause (occurrence of LOS, LOF, Line AIS) is detected, it is transmitted automatically. This automatic transmission upon the occurrence of an internal cause can be masked by the IACM register.

Transmit overhead:	K2 byte (6th through 8th bits) = 110
Transmission/cancellation condition:	• Setting by the command register • Automatic transmission/cancellation upon occurrence of the following internal causes (can be masked by the IACM register) Detection/cancellation of LOF Detection/cancellation of LOS Detection/cancellation of Line AIS

(d) Transmitting Path RDI (FERF) (Path Remote Detect Indication/Far End Receive Failure)

This signal reports, to units upstream, that a path receive failure (LOS, LOF, Line AIS, LOP, LCD, Path AIS) has been detected. The μPD98405 sets the fifth bit of the overhead G1 byte of the transmit frame to "1" for transmission if the PRDI bit of command register 1 (PCMR1) is set to 1. If an internal cause (occurrence of LOS, LOF, Line AIS, LOP, LCD, Path AIS) is detected, it is automatically transmitted. This automatic transmission upon the occurrence of an internal cause can be masked by the IACM register.

Transmit overhead: G1 byte (5th bit) = 1

Transmission/cancellation condition:

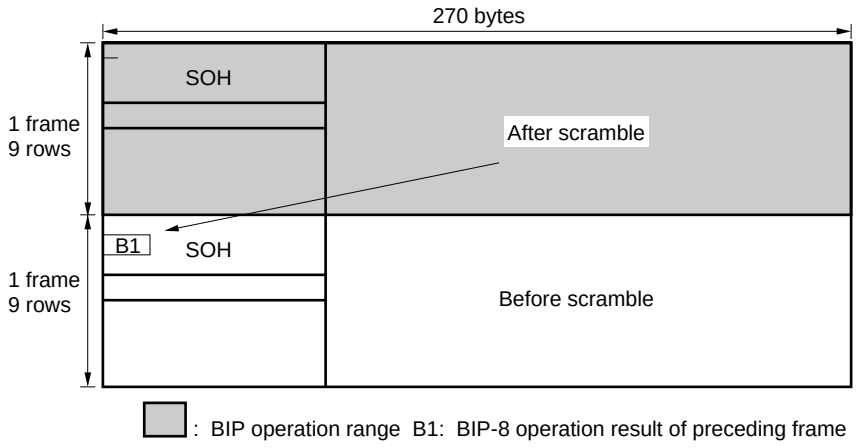
- Setting by the command register
- Automatic transmission/cancellation upon the occurrence of the following internal causes (can be masked)
  - Detection/cancellation of LOF
  - Detection/cancellation of LOS
  - Detection/cancellation of LOP
  - Detection/cancellation of LCD
  - Detection/cancellation of Line AIS
  - Detection/cancellation of Path AIS

★ **(2) Monitoring circuit quality (performance monitor)**

(a) Bit Interleaved Parity (BIP)

B1 byte (Section BIP-8):

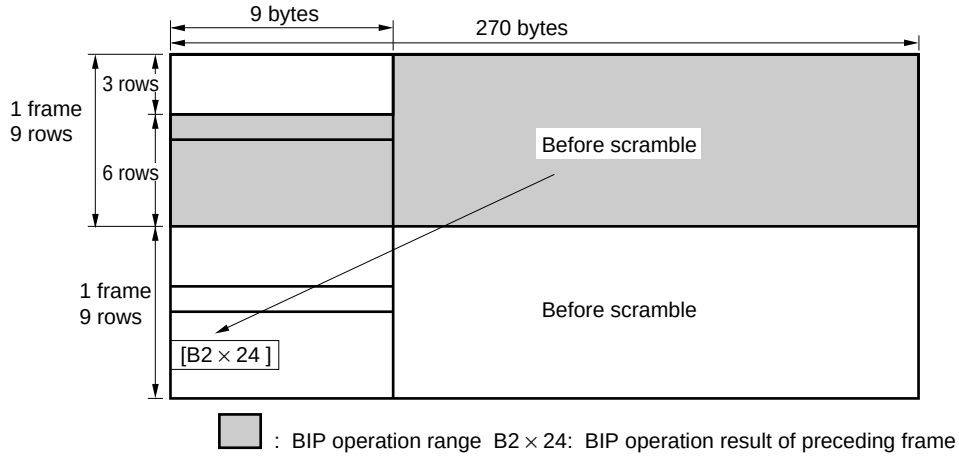
BIP-8 calculation is performed for all frame data (scrambled data) except the first line of the SOH (section overhead) of the transmit frame, BIP8 calculation is performed on a specific area, and the result of the calculation is inserted into the B1 byte of the next transmit frame for transmission.



: BIP operation range B1: BIP-8 operation result of preceding frame

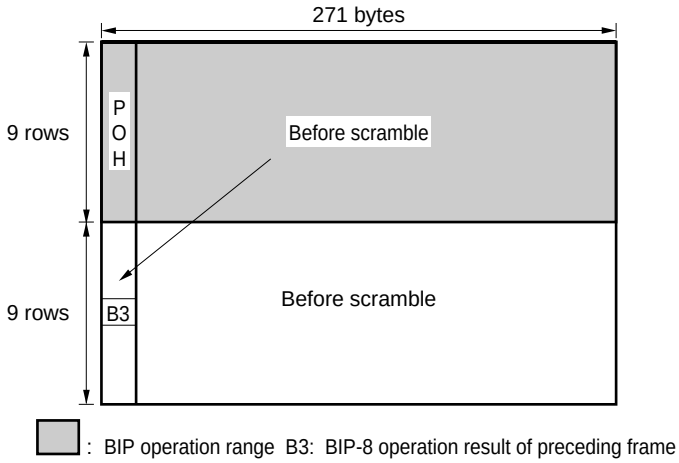
B2 byte (Line BIP-24):

BIP-24 calculation is performed for all frame data (data after descrambling) except the first, second, and third lines of the SOH of the previous frame, and the result of the calculation is inserted into the B2 byte of the next transmit frame for transmission.



B3 byte (Path BIP-8):

BIP-8 calculation is performed for all payload data (data after descrambling) of the transmit frame, and the result of the calculation is inserted into the B3 byte of the POH (path overhead) of the next transmit frame for transmission.



(b) Transmitting Line FEBE (Line Far End Block Error)

A report is issued, to units upstream, of whether a Line BIP-24 error has occurred.

When the μPD98405 detects a B2 error in the receive frame, it automatically stores the number of erroneous bytes into the third Z2 byte (fourth through eighth bits) of the transmit frame for transmission.

(c) Transmitting Path FEBE (Path Far End Block Error)

A report is issued, to units upstream, of whether a Path BIP-8 error has occurred.

When the μPD98405 detects a B3 error in the receive frame, it automatically stores the number of erroneous bytes into the G1 byte (first through fourth bits) of the transmit frame for transmission.

(3) Dummy error frame generation/transmission function

The μPD98405 has a function for internally generating the dummy error frames listed in Table 6-6. This function is useful for testing a system and can be executed by setting command register 3 (PCMR3).

Table 6-6. Dummy Error Frames

Error	Generation of dummy error
LOS frame generation	Fix transmit data to 00H.
OOF/LOF frame generation	Fix A1 and A2 bytes to 00H.
LOP frame generation	Fix H1, H2, and H3 bytes to FFH, FEH, and FFH.
OCD and LCD frame generation	Invert LSB bit of HEC field.
Generation of B1 error	Invert and transmit LSB bit of B1 byte.
Generation of B2 error	Invert and transmit LSB bit of B2 byte.
Generation of B3 error	Invert and transmit LSB bit of B3 byte.
Generation of Line FEBE	Invert and transmit LSB bit of 3rd Z2 byte (4th through 8th bits).
Generation of Path FEBE	Invert and transmit LSB bit of G1 byte (1st through 4th bits).

6.3.2 Reception OAM Control

(1) Detection of alarm and failure

If the μPD98405 detects any of the alarms or failures listed below, it sets the bits of the internal interrupt source register and issues a report to the host by means of an interrupt signal. The host can identify the type of the detected alarm or failure by reading each interrupt source register. Each source of the interrupt can be either masked or unmasked. The detection of an alarm or failure can be reported by outputting a signal from the PHYALM output pin. Which alarm or failure is to be output to the PHYALM pin is specified by the AMR1 and AMR2 registers.

Table 6-7. Alarms and Failures (1/2)

★ **LOS (Loss Of Signal)**
Loss of receive signal Detection: When patterns of all 0 or all 1 are received continuously for about 80 μs, or when the SD pin goes low. Clear: When the LOS condition has not been detected for 125 μs.
OOF (Out Of Frame)
Out of frame synchronization Detection: When a frame synchronization pattern (A1, A2) error in the receive data is detected in four successive frames Clear: When a frame synchronization pattern is detected in two successive frames
LOF (Loss Of Frame)
Loss of frame Detection: When OOF status lasts for 3 ms Clear: When status out of OOF status lasts for 3 ms
★ **LOP (Loss Of Pointer)**
Pointer failure detection Detection: See **6.2 (4)**. Clear: See **6.2 (4)**. The LOP status is forcibly set when OOF is detected.
OCD (Out of Cell Delineation)
Out of cell delineation Detection: When seven cells, having a header in which an error is detected in the HEC verification result, are received continuously. When OOF, LOP, or Path AIS is detected, OCD status is forcibly set. Clear: When seven cells having a valid header are received continuously
LCD (Loss Of Cell Delineation)
Loss of cell delineation Detection: When OCD status continues for 4 ms Clear: When cell synchronization status continues for 4 ms
Line AIS (Line Alarm Indication Signal)
Line alarm indication signal. Detects the occurrence of Line AIS in the unit at the transmission source (upstream). Detection: When five frames, with the overhead K2 byte (6th through 8th bits) set to "111", are received continuously Clear: When five frames, with the overhead K2 byte (6th through 8th bits) not set to "111", are received continuously
★ **Path AIS (Path Alarm Indication Signal)**
Path alarm indication signal. Detects the occurrence of Path AIS at the transmission source (upstream). Detection: See **6.2 (4)**. Clear: See **6.2 (4)**.

Table 6-7. Alarms and Failures (2/2)

Line RDI (Line Remote Defect Indication)
Line remote end receive failure information. Indicates that a line receive failure (LOS, LOF, Line AIS) was detected in the unit at the transmission destination (downstream). Detection: When five frames with the overhead K2 byte (6th through 8th bits) set to "110" are received continuously Clear: When five frames with the overhead K2 byte (6th through 8th bits) set to other than "110" are received continuously
Path RDI (Path Remote Defect Indication)
Path remote end receive failure information. Indicates that a path receive failure (LOS, LOF, Line AIS, LOP, LCD, Path AIS) has been detected in the unit at the transmission destination (downstream). Detection: When five frames for which the fifth bit of the overhead G1 byte is set to "1" are received continuously Clear: When five frames for which the fifth bit of the overhead G1 byte is reset to "0" are received continuously
★ **OOL (Out Of Link)**
Indicates whether the receive clock recovery PLL has correctly locked on to the receive data stream, and whether it is the expected clock signal. Detection: When the difference between the clock signal input to the REFCLK pin and the clock signal generated by the recovery PLL divided by eight is greater than 244 ppm. Clear: When the difference between the clock signal input to the REFCLK pin and the clock signal generated by the recovery PLL divided by eight is within 244 ppm.

(2) Reporting circuit quality deterioration (performance monitor)

When the μPD98405 detects a cause of circuit quality deterioration while monitoring the circuit quality, it sets a bit of an internal interrupt source register to issue a report to the host by means of an interrupt signal. The host can identify the type of the cause of circuit quality deterioration by reading the interrupt source register. Each source of the interrupt can either be masked or unmasked.

Table 6-8. Performance Cause Register (PCR Register)

B1 error detection
Detects a section layer BIP-8 error in the receive data. BIP-8 calculation is performed for all frame data (scrambled data) except the first line of the previous frame's SOH, and the result of this calculation is verified against the result of the Section BIP-8 calculation executed at the transmission source (upstream) and stored into the B1 byte of the current frame, to detect a B1 error.
B2 error detection
Detects a line layer BIP-24 error in the receive data. BIP-24 calculation is performed on all the frame data (data after descrambling), except the first, second, and third lines of the previous frame's SOH, and the result of this calculation is verified against the result of the Line BIP-24 calculation executed at the transmission source (upstream) and stored into the B2 byte of the current frame, to detect a B2 error.
B3 error detection
Detects a bus layer BIP-8 error in the receive data. BIP-8 calculation is performed for all the payload data (data after descrambling) in the previous frame, and the result of this calculation is verified against the result of the Path BIP-8 calculation executed at the transmission source (upstream) and stored into the B3 byte of the current frame, to detect a B3 error.
Line FEBE detection (Line Far End Block Error)
Line far end block error information. Detects whether a Line BIP-24 error has occurred in the unit at the transmission destination (downstream). Detection: Detects Line FEBE if the 4th through 8th bits of the receive Z2 (M1) byte are 01 to 18(H). Clear: Clears Line FEBE if the 4th through 8th bits of the receive Z2 (M1) byte are 00(H).
Path FEBE detection (Path Far End Block Error)
Path far end block error information. Detects whether a Path BIP-8 error has occurred in the unit at the transmission destination (downstream). Detection: Detects Path FEBE if the 1st to 4th bits of the receive G1 byte are 1 to 8(H). Clear: Clears Path FEBE if the 1st to 4th bits of the receive G1 byte are 0(H).
Frequency Justification occurrence
Detects the occurrence of Frequency Justification.

(3) Circuit quality monitor with count register

To monitor the circuit quality, the μPD98405 counts the number of circuit quality deterioration causes, the number of times receive Frequency Justification has been applied, and the number of cells dropped because of the occurrence of an HEC error by using counters. The host can check the counts by reading the registers.

Table 6-9. Counters

Counter name	Description	Number of counter bits
B1E counter	Number of times B1 error has been detected	16
B2E counter	Number of times B2 error has been detected	20
B3E counter	Number of times B3 error has been detected	16
L-FEBE counter	Total number of errors received by Line FEBE	20
P-FEBE counter	Total number of errors received by Path FEBE	16
FJ counter	Number of Frequency Justification operations	12
HEC counter	Total number of cells dropped by HEC processing	20
FIFO full counter	Total number of cells dropped because of FIFO overflow	20
Idle cell counter	Total number of received idle cells (cells dropped as a result of setting the DCHPR and DCHPMR registers)	20
Information cell counter	Total number of valid cells transferred to ATM layer device	20

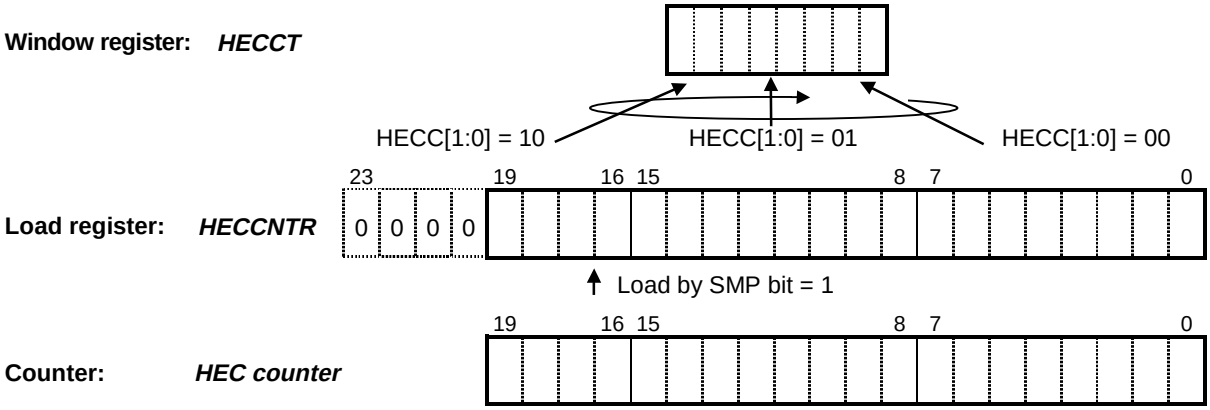
The counter function is implemented by these registers. These registers are provided for each of the above counters.

Counter: This counter counts the number of internal events for the μPD98405. When the count value reaches all "F(H)", the corresponding bits of the PCOCR1 and PCOCR2 registers are set, and the detection of an overflow is reported. The count value then returns to 0, and the counter continues counting.

Load register: If the SMP bit of the PCSR register is set to "1" by the host, all the values of the counters at that time are stored into the corresponding load registers. The contents of this register are held until new data is loaded into the register.

Window register: This is an 8-bit register used by the host to read the contents of the load register. To obtain the 12- or 16-bit value of the load register, the value of the load register is output in 8-bit units, the low-order 8 bits being output first, followed by the high-order 8 bits, each time the host reads the window register. Therefore, the host reads the window register two times continuously. Whether the low-order or high-order 8 bits are output when the host next reads the window register is indicated by the corresponding bits of the PCPR1 and PCPR2 registers. To read a 20-bit load register, the window register is read three times, in the order of the low-order bits, middle bits, then high-order bits.

Figure 6-9. Counter-Related Registers (Example: HEC Error Counter)



The counter also has the following functions:

(a) Clearing all counters

By setting the PCR bit of command register 2 (PCMR2) to "1", all the counters can be cleared to 0. The PCR bit is automatically reset to 0 after the counters have been cleared.

(b) Clearing each counter

When the bit of the PCIR1 and PCIR2 registers corresponding to the counter to be cleared is set to "1", only the corresponding counter is cleared to 0. The set bit is automatically reset to 0 after the counter has been cleared.

(c) Loading all counters

When the SMP bit of the PCSR register is set to "1", the current values of all the counters are stored into the corresponding load registers. The SMP bit is reset to 0 after the counter values have been stored into the load registers.

(d) Stopping an unused counter

To reduce the power consumption, unused counters can be stopped. When the bit of the PCFR1 and PCFR2 registers corresponding to a counter that is not to be used is set to 1, that counter is stopped.

(e) Reporting overflow of each counter

If the count value exceeds all "F", the μPD98405 sets the corresponding bit of the PCOCR1 and PCOCR2 registers to "1", reporting the occurrence of an overflow by using an interrupt. The interrupt can be masked bitwise.

★ **Remark** All counters stop when any one of the LOS, LOF, LOP, LAIS or PAIS errors occurs. The cell counters (HECCT, FULCT, IDLCT, INFCT) stop when either the LCD or OCD error occurs.

6.4 FRAME OVERHEAD INSERT/DROP FUNCTION

The μPD98405 has an insert/drop register in the following byte area of the frame overhead, and can set any value into a transmit frame for transmission, or read a value stored into a receive frame.

Figure 6-10. Overhead Byte with Insert/Drop Register

SOH (section overhead)	1st C1 byte
	2nd C1 byte
	3rd C1 byte
	F1 byte
LOH (line overhead)	K1 byte
	K2 byte
POH (path overhead)	F2 byte
	C2 byte
	H4 byte

- **Insert register**

  The μPD98405 stores the value, written by the host into the insert register, into the corresponding byte area of the overhead of the frame to be transmitted. Unless changed by the host, the μPD98405 stores and transmits the default value of the insert register.

★ The value of the insert register is ignored if the 6th to 8th bit of the K2 byte are used for Line-RDI transmission.

- **Drop register**

  The μPD98405 stores the contents of the overhead of the receive frame into the corresponding drop register, and updates the contents of the drop register each time it receives a frame. The host can determine the value of the byte area to be stored into the overhead of the receive frame by reading each drop register.

★ The POH register is not updated in the LOP or Path-AIS status. None of the registers are updated if out of frame synchronization (OOF) occurs.

6.5 ALARM REPORT PIN

(1) PHYALM pin

The μPD98405 is provided with the PHYALM pin that outputs a signal that indicates, to the peripheral device, that an alarm or error has been detected. The user can specify the output of one or more of the alarm or error items, listed in Table 6-10, to the PHYALM pin. The alarm or error item(s) are specified by using two registers of AMR1 and AMR2. The bit corresponding to each alarm/error is masked or unmasked by using the AMR1 and AMR2 registers. When an alarm or error that is not masked by these registers is detected, the PHYALM output is modified accordingly.

Table 6-10. Report by PHYALM

Reported item	PHYALM output timing
CMD	The PHYALM pin goes high if the host sets 1 in the ALM bit of command register 1. The PHYALM pin can be also used as a Generic output port pin.
LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI	The PHYALM pin goes high if any alarm or error is detected. The level of the PHYALM pin remains high until each cause is cleared.

(2) SD pin

The μPD98405 is provided with the SD external input port to detect LOS. The input level of this pin is added to the LOS detection condition. This bit is connected to the LOS output signal, etc., of the PMD device.

Table 6-11. SD Pin Function

SD pin input	Status
High	Normal status
Low	LOS detection

6.6 REGISTER FUNCTION

The μPD98405 contains multiple PHY registers. The host accesses these registers by issuing the Indirect_Access command. By accessing the registers, the host sets the operating mode of the μPD98405, transmits alarms, and performs interrupt processing. The functions of the registers can be classified as follows:

Table 6-12. Types of μPD98405 PHY Registers

Classification	Function outline	Register name
Command-related	Sets the command that sends an error frame, etc., to μPD98405.	PCMR1, PCMR2, PCMR3
Mode setting-related	Selects the mode in which μPD98405 operates.	MDR1, MDR2, MDR3
Interrupt-related	Status registers indicating an interrupt source, and mask registers specifying whether each interrupt is masked	PICR, PIMR, ACR, ACMR, PCR, PCMR, IACMR
Counter-related	Stores the values of performance counters.	B1ECT, B2ECT, B3ECT, LFBCT, PFBCT, FJCT, HECCT, FULCT, IDLCT, INFCT, PCPR1, PCPR2, PCSR, PCIR1, PCIR2, PCFR1, PCFR2, PCOCR1, PCOCR2, PCOMR1, PCOMR2
PHYALM pin output signal setting	Selects the information to be output to PHYALM pin.	AMR1, AMR2
Drop cell	Determines the cell to be discarded, other than an idle cell.	DCHPR, DCHPMR
Insert/drop	Insert registers for inserting overhead of transmit frame and drop registers to which the contents of the receive frame overhead are to be stored	C11R, C12R, C13R, F1R, K1R, K2R, C2R, F2R, H4R, C11T, C12T, C13T F1T, K1T, K2T, F2T, C2T, F2T, H4T

For details of the registers, see **Section 7.4**.

6.7 LOOPBACK FUNCTION

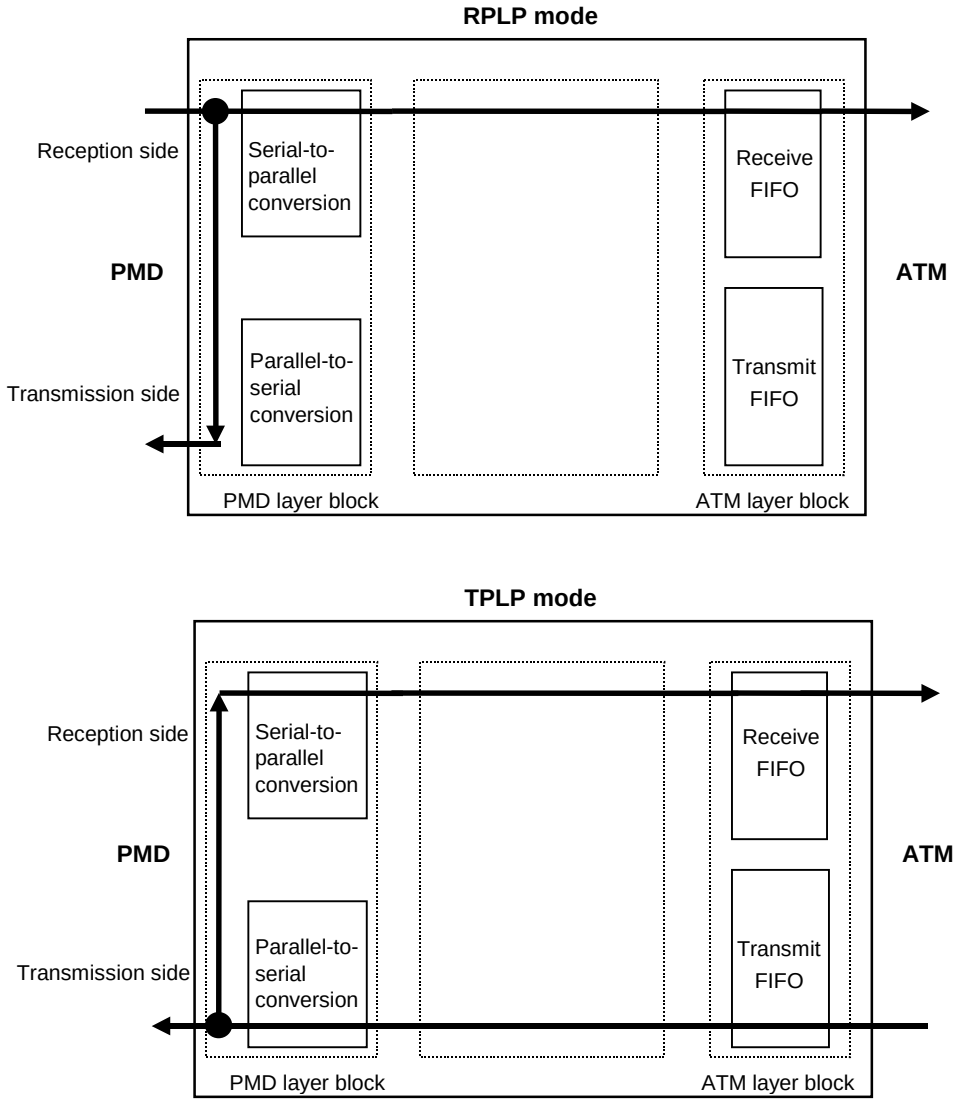
The μPD98405 supports a loopback mode in which the transmit/receive data is looped back within the LSI during a test. The following two loopback modes are supported for PHY. These modes are selected by the LP (1, 0) bit of mode register 2 (MDR2).

Remark The μPD98405 also has one loopback mode in SAR. This loopback mode is set using the LP bit of the GMR register. Therefore, the μPD98405 supports a total of three loopback modes.

Table 6-13. PHY Loopback Function

LP[1:0]	Mode
00	Normal mode
01	**PMD layer loopback <1>: RPLP mode** Loops back the data input from the reception side of the PMD layer interface before the serial/parallel converter of the PMD layer, and outputs it from transmission side of the PMD layer interface. Received data is also output from the ATM layer interface.
10	**PMD layer loopback <2>: TPLP mode** Performs internal processing of the transmit cell data received from the ATM layer interface up to the PMD side, loops back the cell on the PMD layer side, and outputs the cell from the reception side of the ATM layer. At this time, the received cell is also output from transmission side of the PMD layer interface.

Figure 6-11. PHY Loopback Function



6.8 INTERRUPT PROCESSING

The μPD98405 uses the PI bit of the GSR register to post notification of an interrupt from the built-in PHY layer. Using this bit, the μPD98405 posts notification of a circuit error, counter overflow, etc, by issuing an interrupt to the host.

If any bit of the PHY interrupt cause register (PICR) is set to 1, the PI bit of the GSR register is made active. When the host detects that the PI bit has been made active, it first reads the PICR register and determines the cause of the interrupt. When the interrupt has been caused by ALM, PFM, or PCO, the host reads the reads the corresponding ACR, PCR and PCOCR1/2 registers to determines the details of the interrupt cause. To enable the analysis of the cause of the interrupt, the relationship between the registers is shown in Figure 6-12. Also, the user can set interrupt masking for each interrupt cause. There are three modes of resetting the bit status after the host has read the PHY interrupt registers (PICR, ACR, and PCR). Mode selection is performed by setting the RCM[1:0] bit of mode register 2 (MDR2).

(1) Interrupt processing mode selection (MDR2: RCM[1:0])

- **Interrupt processing mode 1 (MDR2: RCM[1:0] = 00)**

  Upon the occurrence of an interrupt, one of the bits of the PICR register will be set, causing the PI bit of the GSR register to be set also. Even if the cause of the interrupt is cleared, the bit settings of the PHY interrupt registers (PICR, ACR, and PCR) are maintained provided they are not read by the host. However, when the cause of the interrupt has been cleared, and the host then performs register read, the bits are reset. The use of this mode is appropriate when obtaining the event history for a fixed period.

- **Interrupt processing mode 2 (MDR2: RCM[1:0] = 01)**

  Upon the occurrence of an interrupt, one of the bits of the PICR register is set, causing the PI bit of the GSR register to be set also. The bits of the PHY interrupt registers (PICR, ACR, and PCR) are reset when the cause of the interrupt is cleared. Even if the host reads the registers, if the cause of the interrupt has not been cleared, the bits are not reset.

- **Interrupt processing mode 3 (MDR2: RCM[1:0] = 1X)**

  Upon the occurrence of an interrupt, one of the bits of the PICR register is set, causing the PI bit of the GSR register to be set also. The bits of the PHY interrupt registers (PICR, ACR, and PCR) are reset when the host reads the registers. Even if the cause of the interrupt has not been cleared, the bits are reset if the host reads the registers.

Caution Although the cause of an interrupt is reset according to the above modes, the reset conditions vary depending on which bits are set. For details, see Figure 6-14.

Figure 6-12. Relationship between Interrupt Cause Registers

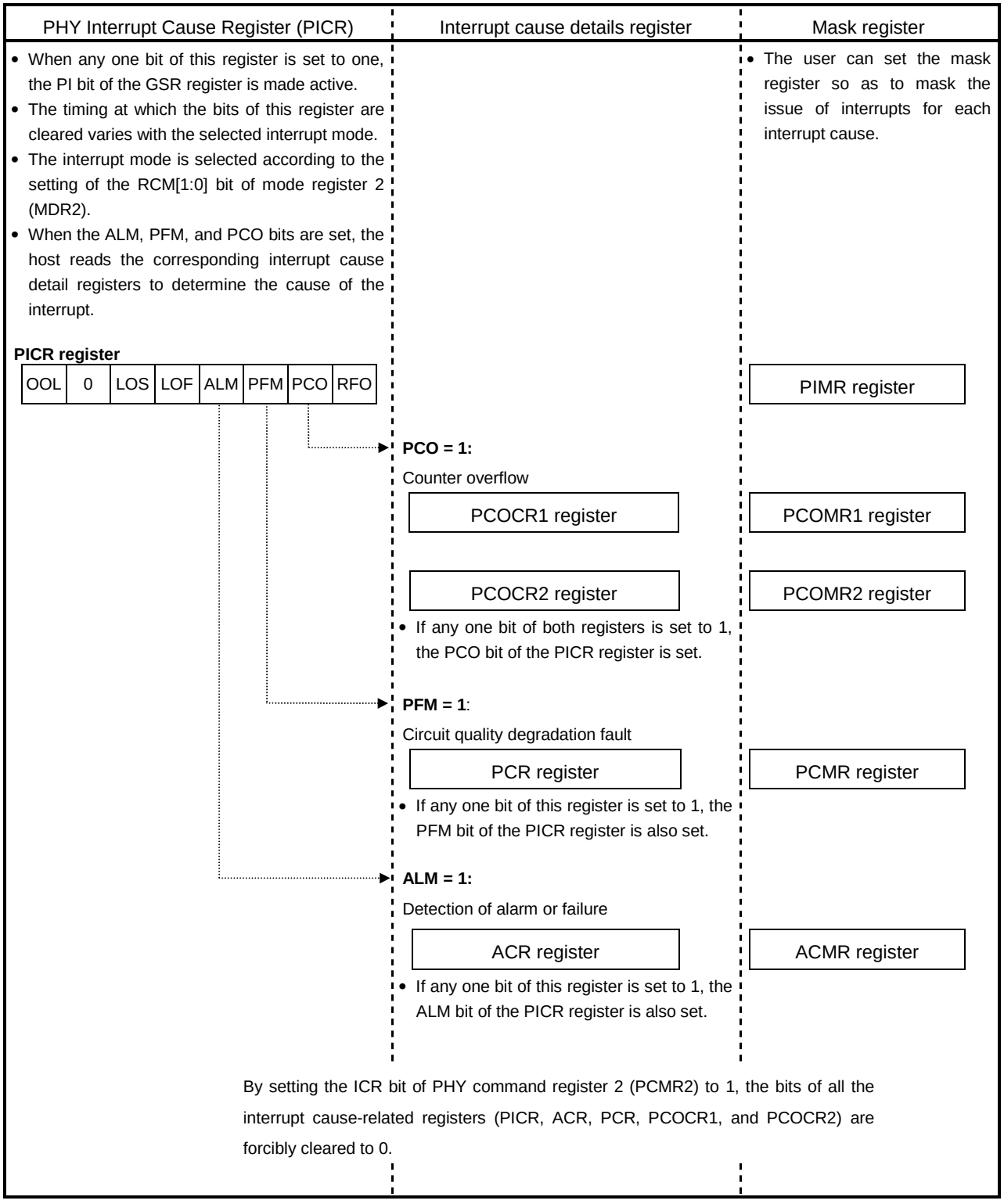


Table 6-14. Set/Reset Conditions for Interrupt Register Bits

Register name	Bit name	Set conditions	Reset conditions		
			Interrupt mode 1 RCM[1:0] bit = 00	Interrupt mode 2 RCM[1:0] bit = 01	Interrupt mode 3 RCM[1:0] bit = 1x
PICR	OOL LOF LOS	Occurrence of each cause	This register is read (Cause of the interrupt must have been cleared)	Cause is cleared	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)
	ALM	Any bit of the ACR register is set	This register is read (All bits of the ACR register must be set to 0)	All bits of the ACR register are set to 0	This register is read (Whether cause of the interrupt of the ACR register is continued or cleared is irrelevant)
	PFM	Any bit of the PCR register is set	This register is read (All bits of the PCR register must be set to 0)	All bits of the PCR register are set to 0	This register is read (Whether cause of the interrupt of the PCR register is continued or cleared is irrelevant)
	PCO	Any bit of the PCOCR1 and PCOCR2 registers is set	This register is read (All bits of the PCOCR1 and PCOCR2 registers must be set to 0)	All bits of the PCOCR1 and PCOCR2 registers are set to 0	This register is read (Whether cause of the interrupt of the PCOCR1 and PCOCR2 registers continued or cleared is irrelevant)
	RFO	Receive FIFO overrun	This register is read (Cause of the interrupt must have been cleared)	Cause of the interrupt is cleared	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)
ACR	OOF LOP OCD LCD LAIS PAIS LRDI PRDI	Occurrence of each cause	This register is read (Cause of the interrupt must have been cleared)	Cause of the interrupt is cleared	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)
PCR	FJ B1E B2E B3E LFEB PFEB	Occurrence of each cause	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)
PCOCR1	B1EC B2EC B3EC LFBC PFBC FJC	Counter value becomes all FF	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)
PCOCR2	HECC FULC IDLC INFC	Counter value becomes all FF	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)	This register is read (Whether cause of the interrupt is continued or cleared is irrelevant)

CHAPTER 7 REGISTERS

The μPD98405 features three types of internal registers: direct address registers, indirect address registers, and PHY registers. Direct address registers are accessed directly via the bus interface. Indirect address registers and PHY registers are accessed by executing an Indirect_Access command.

Caution Do not access an address that is not assigned to a register. Also, do not perform access in other than the specified access mode (do not attempt to write to a read-only register).

7.1 REGISTER MAP

(1) Direct address registers

(1/2)

Address W (H)	Address B (H)	Register	Function	R/W	Default value
00	00	GMR	General mode register	R/W	00H
01	04	GSR	General status register	R	00H
02	08	IMR	Interrupt mask register	R/W	00H
03	0C	RQU	Receive queue underrun	R	00H
04	10	RQA	Receive queue alert	R	00H
05	14	ADDR	Last burst address	R	00H
06	18	VER	Version number	R	-
07	1C	SWR	Software reset	W	00H
08	20	CMR	Command register (with lock/without unlock)	R/W	00H
09	24	CMR_L	Command register (with lock/unlock)	R/W	00H
0A	28	CER	Command extension register (without unlock)	R/W	00H
0B	2C	CER_L	Command extension register (with unlock)	R/W	00H
0C	30	ECCR	EEPROM command control register	R/W	00H
0D	34	ERDR	EEPROM read data register	R	Not defined
0E	38	CFR	Command FIFO register	R	00H
10	40	MSH0	Mailbox 0 start address high	R/W	Not defined
11	44	MSH1	Mailbox 1 start address high	R/W	Not defined
12	48	MSH2	Mailbox 2 start address high	R/W	Not defined
13	4C	MSH3	Mailbox 3 start address high	R/W	Not defined
14	50	MSL0	Mailbox 0 start address low	R/W	Not defined
15	54	MSL1	Mailbox 1 start address low	R/W	Not defined
16	58	MSL2	Mailbox 2 start address low	R/W	Not defined
17	5C	MSL3	Mailbox 3 start address low	R/W	Not defined
18	60	MBA0	Mailbox 0 bottom address	R/W	Not defined
19	64	MBA1	Mailbox 1 bottom address	R/W	Not defined
1A	68	MBA2	Mailbox 2 start address high	R/W	Not defined
1B	6C	MBA3	Mailbox 3 start address high	R/W	Not defined
1C	70	MTA0	Mailbox 0 tail address	R/W	Not defined
1D	74	MTA1	Mailbox 1 tail address	R/W	Not defined

(2/2)

Address W (H)	Address B (H)	Register	Function	R/W	Default value
1E	78	MTA2	Mailbox 2 tail address	R/W	Not defined
1F	7C	MTA3	Mailbox 3 tail address	R/W	Not defined
20	80	MWA0	Mailbox 0 write address	R/W	Not defined
21	84	MWA1	Mailbox 1 write address	R/W	Not defined
22	88	MWA2	Mailbox 2 write address	R/W	Not defined
23	8C	MWA3	Mailbox 3 write address	R/W	Not defined
24	90	RCC	Receive cell counter	R	00H
25	94	TCC	Transmit cell counter	R	00H
26	98	RUEC	Invalid VPI/VCI receive cell error counter	R	00H
27	9C	RIDC	Internally discarded receive cell counter	R	00H
28	A0	PBAH	PCI base address high	R/W	00H

(2) Indirect address registers

To access the indirect address registers, the Indirect_Access command is used.

Scheduler registers

Address (H)	Register	Function	R/W	Default value
0 - F	I, M	I and M entry of schedulers 0 through 15	R/W	00000000H
10 - 1F	X	X entry of schedulers 0 through 15	R/W	00000000H
20 - 2F	Y	Y entry of schedulers 0 through 15	R/W	00000000H
30 - 3F	P, C, p, c	P, C, p, c entries of schedulers 0 through 15	R/W	00000000H
40 - 4F	Pri & Status	Priority and status of schedulers 0 through 15	R/W	00000000H
50	Priority	ABR scheduler priority (in-rate)	R/W	00000000H
51	Priority	ABR scheduler priority (out-of-rate)	R/W	00000000H

Other registers

(1/2)

Address (H)	Register	Function	R/W	Default value
100	TOS	Control memory address of top of stack	R/W	00000000H
101	SCR	Shaper control register	R/W	00000000H
102 - 111	SPE	Shaper pointer entries 0 through 15	R/W	00000000H
200	ALA	Control memory start address of ABR lookup table	R/W	00000000H
201	PMA	Control memory start address of receive pool	R/W	00000000H
300	T1R	T1 register	R/W	0000FFFFH
301	VRR	VPI/VCI reduction register/global shutdown	R/W	0000FFFFH
302	TSR	Time stamp register	R/W	00000000H
305	HTU	Upper 32 bits of hashing table register	R/W	00000000H
306	HTL	Lower 32 bits of hashing table register	R/W	00000000H
307	MAU	Upper 32 bits of MAC address	R/W	00000000H
308	MAL	Lower 16 bits of MAC address	R/W	00000000H
400	APR	ABR parameter register	R/W	89F9FF14H
401	TBW	Total bandwidth register	R/W	000092C7H
402	TTH0	Time threshold register 1	R/W	00007FFFH
403	TTH1	Time threshold register 2	R/W	00007FFFH

(2/2)

Address (H)	Register	Function	R/W	Default value
404	RFTH	Receive FIFO threshold register	R/W	0000007FH
405	ULR	Use-it-or-lose-it register	R/W	00000009H
500	UBCR	UBR bandwidth control register	R/W	00000000H
501	AUB	ABR, UBR bandwidth register	R/W	00000000H
502	LCR	Internal congestion cell rate register	R/W	00000000H

(3) PHY register

To access the PHY register, the Indirect_Access command is used.

Address	Register	Function	R/W	Default value
00H	PCMR1	Command register 1. Used to set alarm frame transmission.	R/W	00H
01H	PCMR2	Command register 2. Used to initialize a register.	R/W	00H
02H	PCMR3	Command register 3. Used to set dummy error frame transmission.	R/W	00H
03H	MDR1	Mode register 1. Used to set the interface mode.	R/W	00H
04H	MDR2	Mode register 2. Used to set interrupt loopback mode.	R/W	00H
05H	MDR3	Mode register 3. Used to set scramble mode and TCLAV mode.	R/W	00H
06H	PICR	Indicates the cause of an interrupt.	R	00H
07H	PIMR	Masks the cause of an interrupt.	R/W	00H
08H	ACR	Displays details of the cause of a circuit fault interrupt.	R	00H
09H	ACMR	Masks the cause of a circuit fault interrupt.	R/W	00H
0AH	PCR	Displays details of the cause of a performance monitoring interrupt.	R	00H
0BH	PCMR	Masks the details of the cause of a performance monitoring interrupt.	R/W	00H
0CH	IACM	Masks automatic transmission of Path/Line RDI.	R/W	00H
0DH	B1ECT	Window register used to read the B1 error counter.	R	00H
0EH	B2ECT	Window register used to read the B2 error counter.	R	00H
0FH	B3ECT	Window register used to read the B3 error counter.	R	00H
10H	LFBCT	Window register used to read the Line-FEBE counter.	R	00H
11H	PFBCT	Window register used to read the Path-FEBE counter.	R	00H
12H	FJCT	Window register used to read the Frequency Justifications counter.	R	00H
13H	HECCT	Window register used to read the HEC error cell discard counter.	R	00H
14H	FULCT	Window register used to read the FIFO full cell discard counter.	R	00H
15H	IDLCT	Window register used to read the receive idle cell counter.	R	00H
16H	INFCT	Window register used to read the receive valid cell counter.	R	00H
19H	PCPR1	Indicates the location of the value read by the counter.	R/W	00H
1AH	PCPR2	Indicates the location of the value read by the counter.	R/W	00H

Address	Register	Function	R/W	Default value
1BH	PCSR	Used to set sample timing in the load register of the counter.	R/W	00H
1CH	PCIR1	Used to set initialization of the counters (B1EC, B2EC, B3EC, LFBC, PFBC, FJC).	R/W	00H
1DH	PCIR2	Used to set initialization of the counters (HECC, FULC, IDLC, INFC).	R/W	00H
1EH	PCFR1	Used to disable use of the counters (B1EC, B2EC, B3EC, LFBC, PFBC, FJC).	R/W	00H
1FH	PCFR2	Used to disable use of the counters (HECC, FULC, IDLC, INFC).	R/W	00H
20H	PCOCR1	Indicates the cause of a counter overflow.	R	00H
21H	PCOCR2	Indicates the cause of a counter overflow.	R	00H
22H	PCOMR1	Masks an interrupt due to a counter overflow.	R/W	00H
23H	PCOMR2	Masks an interrupt due to a counter overflow.	R/W	00H
25H	AMR1	Masks the alarm output from the PHYALM pin.	R/W	00H
26H	AMR2	Masks the alarm output from the PHYALM pin.	R/W	00H
27H	DCHPR	Used to set the drop cell header pattern.	R/W	01H
28H	DCHPMR	Masks the drop cell header pattern.	R/W	00H
2AH	C11R	Stores the first C1 byte of the receive frame.	R	00H
2BH	C12R	Stores the second C1 byte of the receive frame.	R	00H
2CH	C13R	Stores the third C1 byte of the receive frame.	R	00H
2DH	F1R	Stores the F1 byte of the receive frame.	R	00H
2EH	K1R	Stores the K1 byte of the receive frame.	R	00H
2FH	K2R	Stores the K2 byte of the receive frame.	R	00H
30H	C2R	Stores the C2 byte of the receive frame.	R	00H
31H	F2R	Stores the F2 byte of the receive frame.	R	00H
32H	H4R	Stores the H4 byte of the receive frame.	R	00H
33H	C11T	Used to set the first C1 byte of the transmit frame.	R/W	01H
34H	C12T	Used to set the second C1 byte of the transmit frame.	R/W	02H
35H	C13T	Used to set the third C1 byte of the transmit frame.	R/W	03H
36H	F1T	Used to set the F1 byte of the transmit frame.	R/W	00H
37H	K1T	Used to set the K1 byte of the transmit frame.	R/W	00H
38H	K2T	Used to set the K2 byte of the transmit frame.	R/W	00H
39H	C2T	Used to set the C2 byte of the transmit frame.	R/W	13H
3AH	F2T	Used to set the F2 byte of the transmit frame.	R/W	00H
3BH	H4T	Used to set the H4 byte of the transmit frame.	R/W	00H

7.2 DIRECT ADDRESS REGISTERS

The address locations of the direct address registers can assume either of two modes: word address mode or byte address mode. These modes can be selected by the SLM bit of the GMR register. Select a mode suitable for the address decode method used by the system to be organized. In PCI mode, only byte address mode can be used. Byte address mode is set automatically, regardless of the setting of the SLM bit.

(1) GMR (general mode register)

Address: 00H

Access mode: Read/write

The GMR register is mainly set by the host to select the operation mode of the μPD98405 and to enable or disable the transmission/reception function. The host sets this register first after the device has been reset. Because this register sets the basic operation mode of the μPD98405, do not change its contents once the host has set the SE or RE bit of this register, at which point the μPD98405 starts transmission and reception. Otherwise, a malfunction may occur.

Bits 31 and 25 can be written. Set these bits to 0.

0	SLM	UID	ICM	PSM	UOC	0	BBL	PLL	EFM	E64	PHM	CFE	TBE	CPE	LP	WA	RA	SZ	AD	BO	PM	PC	BPE	DR	SE	RE
31	30	29	28	27	26	25	24 – 22	21	20	19	18	17	16	15	14	13	12	11 – 8	7	6	5	4	3	2	1	0

Field	Function	Value after reset
SLM[Note]	Sets the addressing of direct address register to either of two modes: word or byte. 0: Word address mode (address W in Register Map) 1: Byte address mode (address B in Register Map) This bit is valid only in Generic mode. In PCI mode, byte address mode is set regardless of the setting of the SLM bit.	0: Word address mode
UID	Unassigned/idle cell disable. 0: Transmits the unassigned/idle cells used for rate adjustment to the PHY layer. 1: Disables the transmission of the unassigned/idle cells used for rate adjustment. In all cases, unassigned/idle cells are not transmitted to the PHY layer.	0: Transmits the unassigned/idle cells used for rate adjustment
ICM	Idle cell mode. 0: Transmits unassigned cells as the cells used for rate adjustment. 1: Transmits idle cells as the cells used for rate adjustment. Those cells that are transmitted by the unassigned cell generator function also become idle cells.	0: Transmits unassigned cells
PSM	Receive packet size notification mode, used for receive indication. 0: Performs notification in units of cells. 1: Performs notification using the Length field. Notification in units of bytes is performed only for the user data length. Error packet notification is performed in units of cells.	0: Notification is performed in units of cells.

Note This field is valid only in Generic mode.

Field	Function	Value after reset
UOC	UTOPIA interface mode 0: Octet level mode 1: Cell level mode When the internal PHY layer is used (the PHM bit is 0), octet level mode is set irrespective of the UOC bit setting.	0: Octet level mode
BBL[Note 1]	Maximum length for fast back-to-back. Set the maximum number of times that fast back-to-back transfer can be performed. A value of up to 7 can be set. When 000 is set in this field, the fast back-to-back transfer function is disabled. This field is valid only in PCI mode. For Generic mode, 000 must be set.	All 0: Disable
PLL	External clock recovery mode Set when using external clock recovery/synthesizer. 0: Internal clock recovery/synthesizer mode 1: External clock recovery/synthesizer mode	0: Internal clock recovery/synthesizer mode
EFM	External receive FIFO mode When using the both internal PHY layer and external receive FIFO, 1 must be set. 0: Normal mode 1: External receive FIFO use mode. The μPD98405 transmits the data, received at the internal PHY layer, from the transmission side of the UTOPIA interface in sync with the internal RCLK. In this case, the UTOPIA interface operates in an octet level handshake manner.	0: Normal mode
E64[Note 1]	64-bit data transfer enable When using 64-bit data transfer of PCI 64-bit expansion, 1 must be set. 0: 32-bit data transfer 1: 64-bit data transfer This bit is valid only in PCI mode. For Generic mode, 0 must be set.	0: 32-bit data transfer
PHM	PHY mode Used to set the use of either the internal PHY layer or an externally connected PHY layer device. 0: Internal PHY layer 1: Externally connected PHY layer device **Caution The function of each two-function pin is switched according to the PHM bit setting. Set the PHM bit carefully.**	0: Internal PHY layer
CFE[Note 1]	Command FIFO enable Used to select the command issue mode. 0: Command FIFO not used mode. 1: Command FIFO used mode. This bit is valid only in PCI mode. For Generic mode, 0 must be set.	0: Command FIFO not used mode
TBE[Note 2]	12-word burst enable. 0: Disable 1: Enable Whenever 12-word burst mode is enabled, it is also necessary to set the AD bit to 1. This bit is valid only in Generic mode. For PCI mode, 0 must be set.	0: Disable

Notes 1. These fields are valid only in PCI mode.

2. This field is valid only in Generic mode.

Field	Function	Value after reset
CPE	Enables/disables the control memory parity check function. 0: Parity disabled 1: Parity enabled	0: Control memory parity disabled
LP	Sets loopback mode. 0: Normal operation 1: Loopback mode	0: Normal operation
WA[Note]	ABRT_B signal and RDY_B signal sampling timing of DMA write operation. 0: Normal mode 1: Early mode This bit is valid only in Generic mode. For PCI mode, 0 must be set.	0: Normal
RA[Note]	ABRT_B signal and RDY_B signal sampling timing of DMA read operation. 0: Normal mode 1: Early mode This bit is valid only in Generic mode. For PCI mode, 0 must be set.	0: Normal mode
SZ[Note]	Enables burst size. Two or more bursts can be enabled. Bit 8 '1' - Enables 2-word burst Bit 9 '1' - Enables 4-word burst Bit 10 '1' - Enables 8-word burst Bit 11 '1' - Enables 16-word burst This field is valid only in Generic mode. For PCI mode, 0000 must be set. **Remark** μPD98405 uses 16-word burst only to store raw cell data.	All 0. All multiple-word DMA transfer disabled. Only one-word transfer enabled.
AD	Enables or disables function for checking address field of transfer destination and for automatically selecting burst size when μPD98405 executes DMA transfer. 0: Enable 1: Disable	0: Enable
BO[Note]	Selects big endian or little endian. 0: Little endian 1: Big endian This bit is valid only in Generic mode. For PCI mode, 0 must be set.	0: Little endian
PM[Note]	Selects bus parity mode. 0: Byte parity 1: Word parity This bit is valid only in Generic mode. For PCI mode, 0 must be set.	0: Byte parity
PC[Note]	Controls even/odd of bus parity. 0: Even parity 1: Odd parity This bit is valid only in Generic mode. For PCI mode, 0 must be set.	0: Even parity
BPE[Note]	Enables or disables bus parity check. 0: Bus parity disabled 1: Bus parity enabled This bit is valid only in Generic mode. For PCI mode, 0 must be set.	0: Bus parity disabled

Note These fields are valid only in Generic mode.

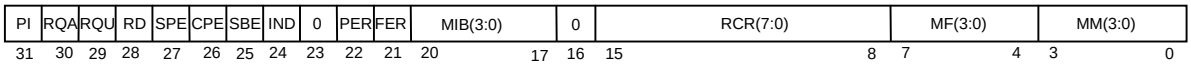
Field	Function	Value after reset
DR	Selects receive discard mode. 0: Drop mode. When receive FIFO is full, overrun occurs and cells are internally discarded. 1: No Drop mode. When receive FIFO is full, requests PHY layer to stop transferring cells by issuing RENBL_B signal. μPD98405 does not discard cells.	0: Drop mode
SE	Enables or disables shaper. This bit enables transmission function of μPD98405. 1: Enables transmission 0: Disables transmission	0: Transmission disabled
RE	Enables or disables reception function. This bit enables reception function of μPD98405. 1: Enables reception 0: Disables reception	0: Reception disabled

(2) GSR (general status register)

Address: 01H

Access mode: Read only

The GSR register indicates the source of an interrupt. When an internal interrupt occurs, the corresponding bit of this register is set to 1. If the interrupt is unmasked by the corresponding bit of interrupt mask register IMR, the interrupt occurs. This register is cleared when it is read by the host. If the same source issues another interrupt before the register is cleared, the contents of the register are overwritten with 1.



Field	Function	Value after reset
PI	Interrupt from PHY layer. '1' indicates that an interrupt has been received from the internal PHY layer, or that a low-level signal has been input from the externally connected PHY layer device to the PHINT_B pin, thus causing an interrupt.	0
RQA	Receive buffer alert. Indicates the existence of a pool for which "REMAINING NO. OF BATCHES IN THE POOL" of pool descriptor exceeds "ALERT LEVEL". The host reads the RQA register to check in which pool this error has occurred.	0
RQU	Receive free buffer underflow. Indicates the existence of a pool for which "REMAINING NO. OF BATCHES IN THE POOL" of pool descriptor is 0 (there is no unused batch). The host reads the RQU register to determine in which pool this error has occurred.	0
RD	Receiver deactivate complete. '1' indicates that the execution of global shutdown has been completed and that reception function has stopped.	0
SPE[Note]	Bus parity error detection. '1' indicates detection of parity error on host bus interface. This bit is valid only in Generic mode. This interrupt is not generated in PCI mode.	0
CPE	Control memory interface parity error detection. '1' indicates detection of parity error on control memory interface.	0
SBE[Note]	Bus error detection. '1' indicates low level is input to ERR_B input pin. This bit is valid only in Generic mode. This interrupt is not generated in PCI mode.	0
IND	Control memory initialization complete. '1' indicates completion of control memory initialization by μPD98405 after reset. About 32K system clocks must elapse between the μPD98405 being reset and this bit being set. During this period, host can only access direct address registers of μPD98405 other than command register.	0

Note These fields are valid only in Generic mode.

Field	Function	Value after reset
PER[Note]	PCI parity error detection. '1' indicates that one of the following errors has been detected. - The target asserted PERR_B while the μPD98405 was performing a master write cycle. - A data phase parity error was detected while the μPD98405 was performing a master read cycle. This bit is valid only in PCI mode. This interrupt is not generated in Generic mode.	0
FER[Note]	PCI fatal error detection. '1' indicates that one of the following errors was detected during data transfer. - Because the target did not assert DEVSEL_B, the μPD98405 executed master abort termination. - The target asserted STOP_B, and executed target abort termination. - Data transfer terminated due to the termination of the retry timer. - Data transfer terminated due to the termination of the TRDY timer. This bit is valid only in PCI mode. This interrupt is not generated in Generic mode.	0
MIB3-MIB0	MIB counter overflow '1' indicates that the MIB counter has overflowed. The following indicates the correspondence between bits and counters. Bit 17 - Received cell counter (RCC) Bit 18 - Transmitted cell counter (TCC) Bit 19 - Invalid VPI/VCI receive cell error counter (RUEC) Bit 20 - Received internally discarded cell counter (RIDC)	0
RCR7-RCR0	Raw cell data reception. '1' indicates that μPD98405 has stored raw cell data to pool. Bit 8 corresponds to RCR0, and indicates that data has been stored to pool 0.	0
MF3-MF0	Mailbox full. '1' indicates that write pointer (MWA) of the μPD98405 has caught up and coincides with read pointer (MTA) of host in mailbox corresponding to bit of this field. Bit 4 corresponds to MF0 and indicates that mailbox 0 is full.	0
MM3-MM0	Stores indication to mailbox. '1' indicates that μPD98405 stores new indication to mailbox corresponding to bit of this field. Bit 0 corresponds to MM0, and indicates that indication has been stored to mailbox 0.	0

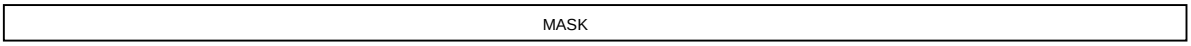
Note These fields are valid only in PCI mode.

(3) IMR (interrupt mask register)

Address: 02H

Access mode: Read/write

The IMR register masks or unmasks the issue of an interrupt from each interrupt source. Mask bits corresponding to the bits of the GSR register are located at the same positions in the IMR register. When the bit of the GSR register corresponding to an unmasked bit is set to 1, the corresponding interrupt output pin is made active.



Field	Function	Value after reset
Mask	Mask bit corresponding to each bit of GSR register is located at same position in mask register. 0: Mask 1: Unmask. When 1 is set in GSR register, corresponding interrupt is issued.	All 0. All interrupts are masked.

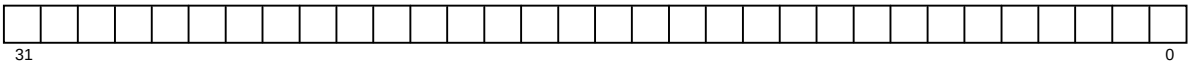
(4) RQU (free buffer underflow register)

Address: 03H

Access mode: Read only

The RQU register bit is set to 1 when the pool corresponding to that bit no longer has a free buffer.

If any one of the bits of this register is set to 1, the RQU bit of the GSR register is set to 1. The μPD98405 detects that no free buffer is available when it has received a cell and transfers its data to the system memory. Until free buffers again become available, any VC cells that are set in a pool having no free buffers are discarded, and this bit is set every time a new packet arrives. The RQU register is a read-clear register.



Field	Function	Value after reset
Receive Queue Underflow	Bit 0 corresponds to pool 0 and bit 31 corresponds to pool 31. '1' indicates that pool corresponding to that bit no longer has a free buffer.	All 0

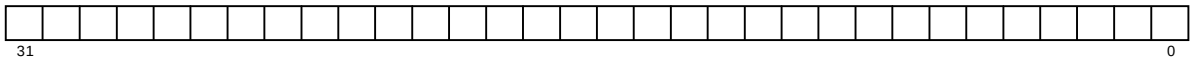
(5) RQA (receive queue alert register)

Address: 04H

Access mode: Read only

The RQA register is set to 1 if the batches of the pool have been exhausted and "REMAINING NO. OF BATCHES IN THE POOL" of the pool descriptor that indicates the number of remaining batches becomes equal to the number of batches set in "ALERT LEVEL" by the user.

If one of the bits of this register is set to 1, the RQA bit of the GSR register is set to 1. The RQU register is a read-clear register.



Field	Function	Value after reset
Receive Queue Alert	Bit 0 corresponds to pool 0 and bit 31 corresponds to pool 31. '1' indicates that number of remaining batches in pool corresponding to position of that bit exceeds ALERT LEVEL, and that free buffers in the pool will soon be exhausted.	All 0

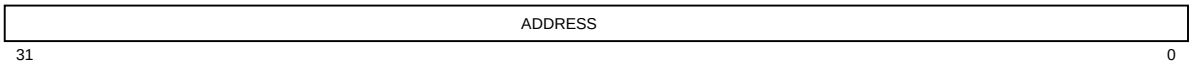
(6) ADDR (burst address register)

Address: 05H

Access mode: Read only

The ADDR register is used to test a device. This register stores the address of the last DMA cycle executed by the μPD98405 before the host reads this register.

★ The ADDR register is only valid in Generic mode. This function cannot be used in the PCI mode, and the value is undefined.



Field	Function	Value after reset
ADDRESS	Last burst address. Transfer address of last DMA cycle executed before host reads this register.	All 0

(7) VER (version register)

Address: 06H

Access mode: Read only

This register stores the code indicating the version of this chip. By reading this register, the version of the chip can be determined.

- 0 -	MAJOR REVISION	MINOR REVISION
31 16	15 8	7 0

Field	Function	Value after reset
MAJOR REV.	Stores code indicating version of this chip.	01H
MINOR REV.	Stores code indicating version of this chip.	Ask our sales person for further information of newest release.

(8) SWR (virtual software reset register)

Address: 07H

Access mode: Write only

SWR is a virtual register. Any operation performed on address 07H causes a software reset.

(9) CMR and CMR_L (command register)

Address: CMR: 08H

CMR_L: 09H

Access mode: Read/write

The CMR register is used by the host to write a command to the μPD98405 and to receive a command indication in response to the written command. For details of how to use this register, see **Section 5.10**. The CMR_L register is used in a multi-host system where the μPD98405 is controlled by two or more hosts. In a single-host system where the μPD98405 is controlled by only one host, the CMR_L register is not used. Only the CMR register is used.

(10) CER and CER_L (command extension register)

Address: CER: 0AH

CER_L: 0BH

Access mode: Read/write

The CER register is used when an Indirect_Access command or Add_Batches command is issued. For details of how to use this register, see **Section 5.10**. The CER_L register is used in a multi-host system, like CMR_L.

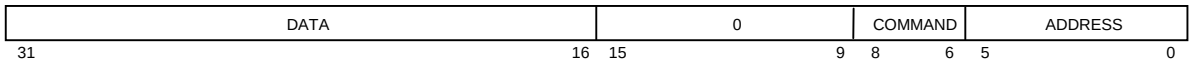
(11) ECCR (EEPROM command control register)

Address: 0CH

Access mode: Read/write

The ECCR register is used when accessing an EEPROM. When an EEPROM is not actually present, any attempt to access this register is ignored. It is not possible to write to bits 15 to 9. Upon a read, 0 is returned.

★ The ECCR register is only initialized by a hardware reset. A software reset does not initialize it.



Field	Function	Value after reset
DATA	Used to save data written upon the execution of the Write command.	0
COMMAND	Command field	0
ADDRESS	Address field	0

The following table lists the correspondences between commands and the setting of the ADDRESS and COMMAND fields of bits 0 to 8.

Bit 8	Bit 7	Bit 6	Bits 5-0	Command
1	1	0	A5-A0 (address)	READ
1	0	1	A5-A0 (address)	WRITE
1	1	1	A5-A0 (address)	ERASE
1	0	0	11xxxx	EWEN
1	0	0	10xxxx	ERAL
1	0	0	01xxxx	WRAL
1	0	0	00xxxx	EWDS

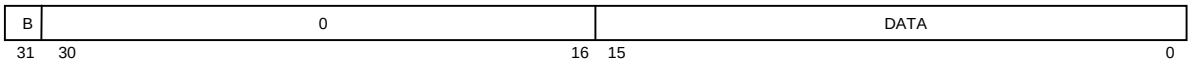
(12) ERDR (EEPROM read data register)

Address: 0DH

Access mode: Read only

The ERDR register is used to store the data read by execution of the EEPROM Read command. Read data is stored into the ERDR register after the EEPROM Read command has been issued from the ECCR register. While the EEPROM Read command is being executed, the B bit is set to 1. Once the data has been stored, the B bit is set to 0. When an EEPROM is not actually present, any attempt to access this register is ignored.

★ The ERDR register is only initialized by a hardware reset. A software reset does not initialize it.



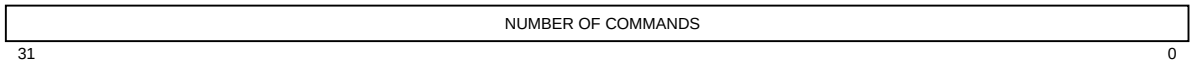
Field	Function	Value after reset
B	Busy bit. 0: EEPROM read data is available. 1: The EEPROM read command is being executed. EEPROM read data has not yet been stored.	Not defined
DATA	EEPROM read data.	Not defined

(13) CFR (command FIFO register) - for testing

Address: 0EH

Access mode: Read only

The CFR register is used to display the number of commands that have been stored into the internal host command FIFO of the μPD98405. This register can be used when the command issue mode is set to command FIFO use mode. By reading the contents of the CFR register, the host can determine the number of commands currently stored in the command FIFO. The internal host command FIFO can store up to 10 commands. The CFR register can be used to store a value of between 0 and 10. After a reset, the contents of the register are initialized to 0.

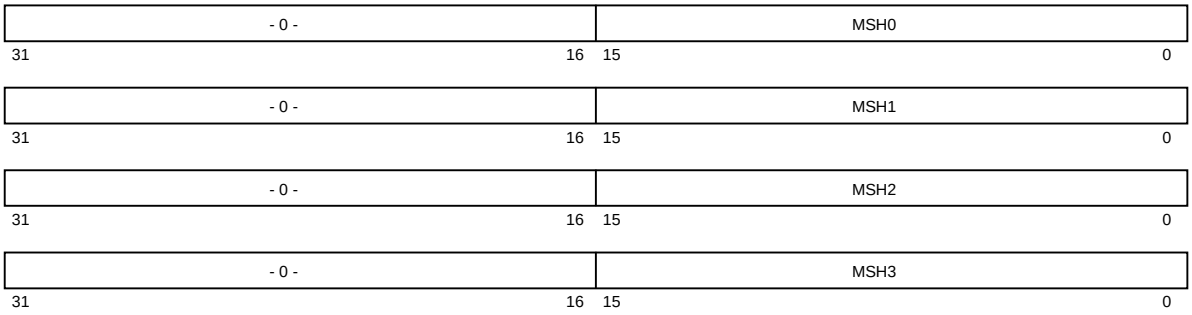


(14) MSH0 to MSH3 (mailbox start address, high)

Address: 10H - MSH0: mailbox 0
11H - MSH1: mailbox 1
12H - MSH2: mailbox 2
13H - MSH3: mailbox 3

Access mode: Read/write

MSH0 to MSH3 set the high-order 16 bits of the 32-bit start addresses of the four mailboxes set to system memory. The host sets MSH of the mailbox to be selected from the four mailboxes. The default value after a reset is undefined. It is not possible to write to bits 31 to 16. Upon a read, 0 is returned.

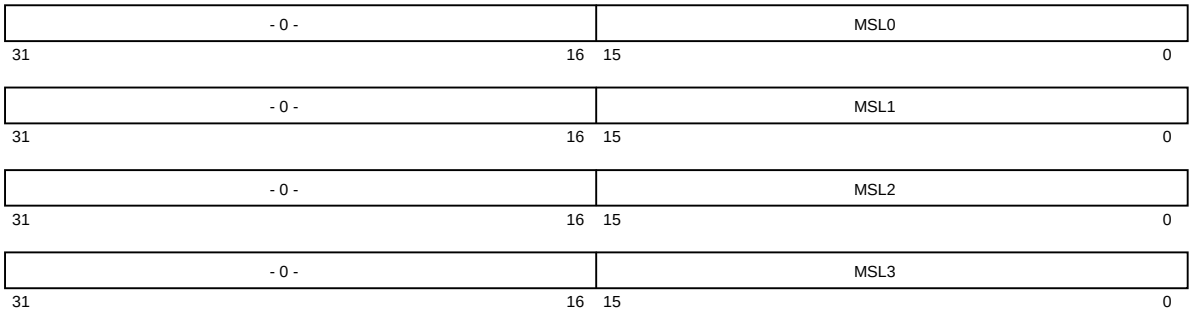


(15) MSL0 to MSL3 (mailbox start address, low)

Address: 14H - MSL0: mailbox 0
15H - MSL1: mailbox 1
16H - MSL2: mailbox 2
17H - MSL3: mailbox 3

Access mode: Read/write

MSL0 to MSL3 set the low-order 16 bits of the 32-bit start addresses of the four mailboxes set to system memory. The host sets MSL of the mailbox to be selected from the four mailboxes. The default value after a reset is undefined. It is not possible to write to bits 31 to 16. Upon a read, 0 is returned.

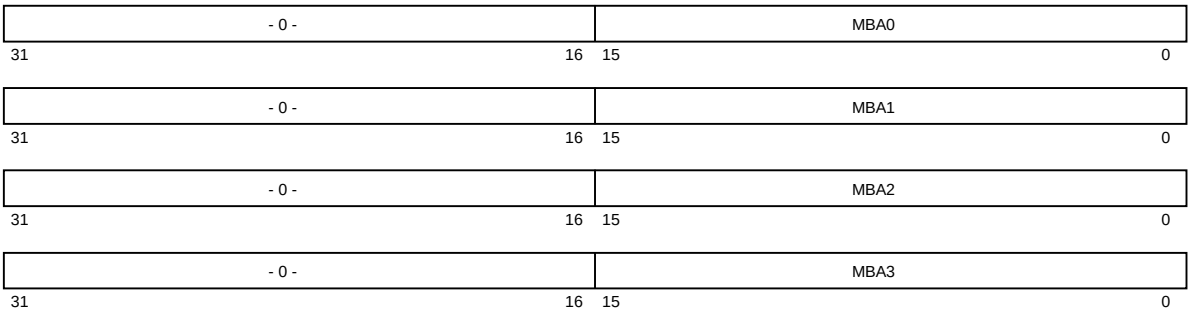


(16) MBA0 to MBA3 (mailbox bottom address)

Address: 18H - MBA0: mailbox 0
19H - MBA1: mailbox 1
1AH - MBA2: mailbox 2
1BH - MBA3: mailbox 3

Access mode: Read/write

MBA0 to MBA3 set the low-order 16 bits of the 32-bit bottom addresses of the four mailboxes set to system memory. The bottom address stores the address next to the last word in the area used as a mailbox area. The host sets MBA of the mailbox to be selected from the four mailboxes. For the μPD98405, MSH is used as the high-order 16 bits of an address. The values set to these registers must not be the same as those set to MSL. The default value after a reset is undefined. It is not possible to write to bits 31 to 16. Upon a read, 0 is returned.



(17) MTA0 to MTA3 (mailbox tail address)

Address: 1CH - MTA0: mailbox 0
1DH - MTA1: mailbox 1
1EH - MTA2: mailbox 2
1FH - MTA3: mailbox 3

Access mode: Read/write

MTA0 to MTA3 store the low-order 16 bits of the read pointers read by the host from the four mailboxes. These registers are managed by the host. The host writes and updates the start address of the indication next to that processed each time it has completed processing of the transmit/receive indication. At initialization, set the same values as those set for MSL. The default value after a reset is undefined. It is not possible to write to bits 31 to 16. Upon a read, 0 is returned.

- 0 -	MTA0
31 16	15 0

- 0 -	MTA1
31 16	15 0

- 0 -	MTA2
31 16	15 0

- 0 -	MTA3
31 16	15 0

(18) MWA0 to MWA3 (mailbox write pointer)

Address: 20H - MWA0: mailbox 0
21H - MWA1: mailbox 1
22H - MWA2: mailbox 2
23H - MWA3: mailbox 3

Access mode: Read/write

MWA0 to MWA3 store the low-order 16 bits of the write pointers of the four mailboxes. These registers are managed by the μPD98405. The μPD98405 increments and updates the addresses of these registers each time it has stored an indication. At initialization, set the same values as those set for MSL. The default value after a reset is undefined. It is not possible to write to bits 31 to 16. Upon a read, 0 is returned.

- 0 -	MWA0
31 16	15 0

- 0 -	MWA1
31 16	15 0

- 0 -	MWA2
31 16	15 0

- 0 -	MWA3
31 16	15 0

(19) RCC (Receive cell counter)

Address: 24H

Access mode: Read only

RCC is a counter that is used to store the number of cells received by the ATM layer. Unassigned/idle cells, as well as cells having an invalid VPI/VCI value, are not counted. When the host performs a read operation, the value of the counter is cleared to 0. If the counter should overflow, the host is notified by the issue of an interrupt, after which counting starts again from 0. After a reset, the counter is initialized to 0.

COUNT
31 ... 0

(20) TCC (transmit cell counter)

Address: 25H

Access mode: Read only

TCC is a counter that is used to store the number of cells transmitted from the ATM layer. Unassigned/idle cells are not counted. When the host performs a read operation, the value of the counter is cleared to 0. If the counter should overflow, the host is notified by the issue of an interrupt, after which counting starts again from 0. After a reset, the counter is initialized to 0.

COUNT
31 ... 0

(21) RUEC (invalid VPI/VCI receive cell error counter)

Address: 26H

Access mode: Read only

RUEC is a counter that is used to store the number of received cells that have been internally discarded as a result of their having an invalid VPI/VCI value. When the host performs a read operation, the value of the counter is cleared to 0. If the counter should overflow, the host is notified by the issue of an interrupt, after which counting starts again from 0. After a reset, the counter is initialized to 0.

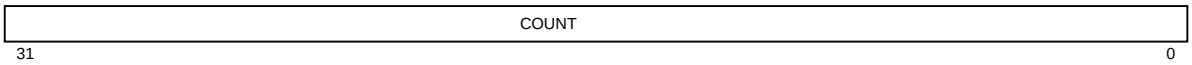
COUNT
31 ... 0

(22) RIDC (receive internally discarded cell counter)

Address: 27H

Access mode: Read only

RIDC is a counter that is used to store the number of received cells that have been discarded as a result of internal congestion (receive buffer underflow, receive FIFO overrun). When the host performs a read operation, the value of the counter is cleared to 0. If the counter should overflow, the host is notified by the issue of an interrupt, after which counting starts again from 0. After a reset, the counter is initialized to 0.

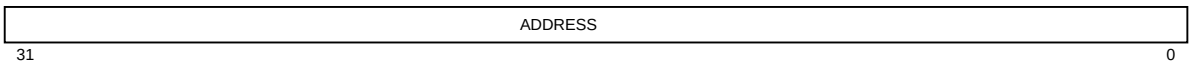


(23) PBAH (PCI base address high)

Address: 28H

Access mode: Read/write

When the host system is using PCI bus 64-bit addressing, set the high-order 32 bits of the PCI base address in the PBAH register. The μPD98405 supports any 4-gigabyte area that is set in the PBAH register. When 0 is set in the PBAH register, 64-bit addressing is disabled, and 32-bit addressing is used. The default value after a reset is 0.



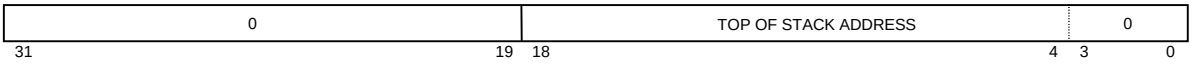
7.3 INDIRECT ADDRESS REGISTER

(1) TOS (top of stack)

Address: 100H

Access mode: Read/write

The host sets the start address of the free block pool of control memory. Subsequently, this register is managed by the μPD98405 and functions as a pointer to the free block that can be allocated as the VC table. The default value after a reset is 0. It is not possible to write to bits 31 to 19 or bits 3 to 0. Upon a read, 0 is returned.

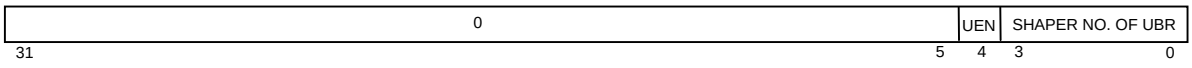


(2) SCR (shaper control register)

Address: 101H

Access mode: Read/write

The host uses the SCR register to set the number of the shaper that uses the UBR service. Subsequently, when this shaper is used as the UBR service, the UEN bit is set to 1 (enable). For the shaper set in the ★ SCR register, set the lowest priority. It is necessary to set the SCR register when using the ABR and UBR services together. It is not necessary to set the SCR register when using the VBR and UBR services together, or when using the UBR service alone. After a reset, this counter is initialized to 0. It is not possible to write to bits 31 to 5. Upon a read, 0 is returned.

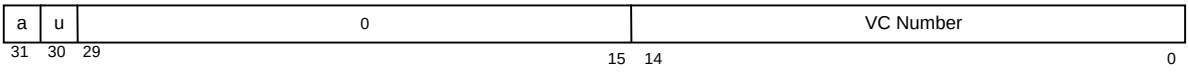


(3) SPE0 to SPE15 (shaper pointer entry 0 to 15)

Address: 102H - 111H

Access mode: Read/write

The μPD98405 mainly uses the SPE register as a table and manages it. The host accesses this area only when initializing its value to 0, or when using the cell generator function. Otherwise, the host has no reason to access this register. SPE0 corresponds to address 102H and shaper number 0, while SPE15 corresponds to address 111H and shaper number 15. The default value will be 0 after a reset. It is not possible to write to bits 29 to 15. Upon a read, 0 is returned.



a Active flag. This bit is mainly used as an internal flag by the μPD98405.

1: At least one active VC is linked to the shaper.

0: There are no active VCs.

When using this shaper as an unassigned/idle cell generator, the host sets both this bit and the u bit to 1.

u Unassigned/idle cell generator. The hosts sets this bit to 1 only when forcing this shaper to function as an unassigned/idle cell generator.

VC Number The μPD98405 uses this as a table to stack the VC Number of the VC that will next perform transmit processing. When no VCs are linked to the shaper, this bit is set to 0.

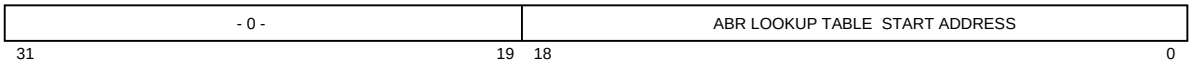
(4) ALA (ABR lookup table start address)

Address: 200H

Access mode: Read/write

The ALA register is used by the host to set the start address of the control memory ABR lookup table area. The ABR lookup table in control memory is an area that is used as a table by the μPD98405. The host only ever accesses the ABR lookup table when performing initialization. Set ALA = TOS when not using the ABR service. In this case, the ABR look-up table can be deleted.

The default value after a reset is 0. It is not possible to write to bits 31 to 19. Upon a read, 0 is returned.

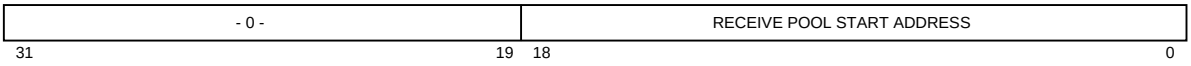


(5) PMA (receive free buffer pool pointer start address)

Address: 201H

Access mode: Read/write

The PMA register is used by the host to set the start address of the receive free buffer pool pointer area in control memory. The default value after a reset is 0. It is not possible to write to bits 31 to 19. Upon a read, 0 is returned.

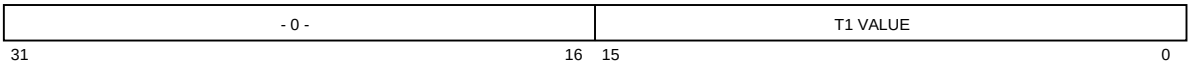


(6) T1R (T1 time)

Address: 300H

Access mode: Read/write

T1R sets the user-specified time during which the reception of one packet is enabled. The time is defined by the high-order 16 bits of the 32-bit value, in units of system clock cycles. Set the low-order 16 bits to "0000H." The default value for this register is "FFFFH" after a reset. It is not possible to write to bits 31 to 16. Upon a read, 0 is returned.



(7) VRR (VPI/VCI reduction register)

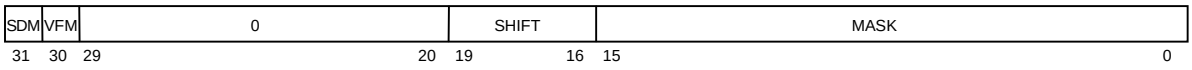
Address: 301H

Access mode: Read/write

The VRR register is used to reduce the 24-bit pattern of the received VPI/VCI value to the 16 bits of an internal logic code. Set the 4-bit "SHIFT" parameter and 16-bit "MASK" parameter. Setting a VFM bit enables filtering of received VPI/VCI values.

For an explanation of the conversion algorithm, see **Section 5.5.4**.

The MSB bit is used as the bit of the "global shutdown" command. When the host writes 1 to this bit, the μPD98405 stops all reception processing currently being executed, sets the RD bit of the GSR register to 1, and issues an interrupt provided it is not masked. The default value of this register is "0000FFFFH" after a reset. It is not possible to write to bits 29 to 20. Upon a read, 0 is returned.



SDM: Global shutdown bit

0: Normal operation

1: Execution of global shutdown

VFM: VPI/VCI filtering mode

0: Enables the VPI/VCI filtering function

1: Disables the VPI/VCI filtering function

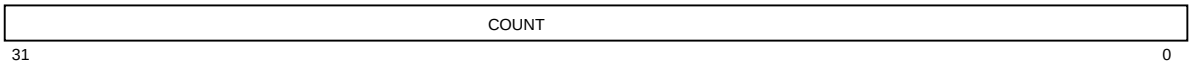
★ **Caution The global shutdown function cannot be used. Set the SDM bit of the VRR register to 0.**

(8) TSR (time stamp register)

Address: 302H

Access mode: Read/write

The TSR register is a 32-bit counter register with which the μPD98405 counts up in sync with the system clock. It is used to set the packet arrival start time of the T1 timer function. The default value of this register is 0 after a reset. The μPD98405 starts counting up immediately after a reset.



(9) HTU (hashing table register upper 32 bits)

Address: 305H

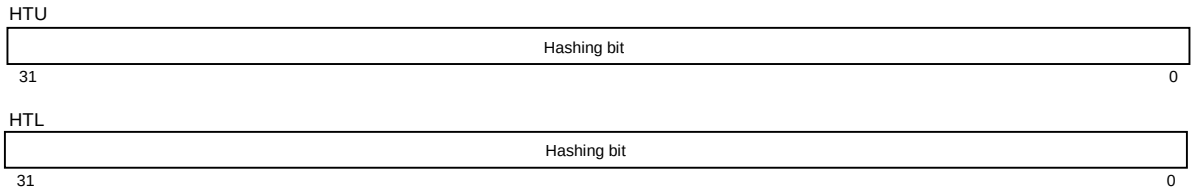
Access mode: Read/write

HTL (hashing table register lower 32 bits)

Address 306H

Access mode: Read/write

The HTU and HTL registers are set when performing MAC address filtering, one of the LAN emulation functions of the μPD98405. The μPD98405 performs filtering using the 64-bit hashing bits set in the HTU and HTL registers. The host must set the hashing bit of the HTU and HTL registers corresponding to the multicast address to be received to 1. The hashing rule uses CRC-32 calculation. The value of the high-order six bits obtained as a result of MAC address (destination address) CRC-32 calculation becomes the corresponding hashing bit. When the corresponding hashing bits of the HTU and HTL registers are set to 1, the μPD98405 receives a packet. The default values of these registers will be 0 after a reset. For details, see **Section 5.7**.



(10) MAU (MAC address upper 32 bits)

Address: 307H

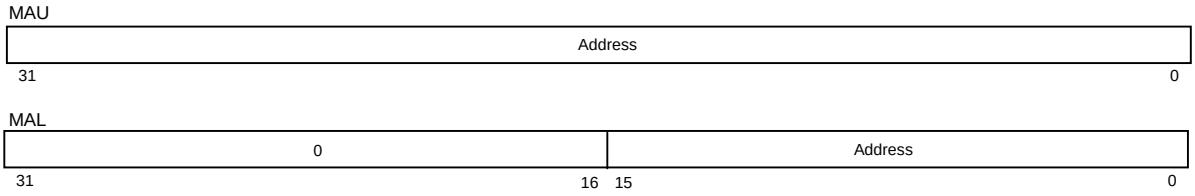
Access mode: Read/write

MAL (MAC address lower 16 bits)

Address: 308H

Access mode: Read/write

The MAU and MAL registers are set when performing MAC address filtering, one of the LAN emulation functions of the μPD98405. The μPD98405 performs filtering using the 48-bit MAC address set in the MAU and MAL registers. For the host, set its own 48-bit MAC address (UNI cast address) in the MAU and MAL registers. The μPD98405 discards those received packets whose destination addresses do not match the 48-bit MAC address set in the MAU and MAL registers. The default values of these registers will be 0 after a reset. For details, see **Section 5.7**. It is not possible to write to bits 31 to 16 of the MAL register. Upon a read, 0 is returned.

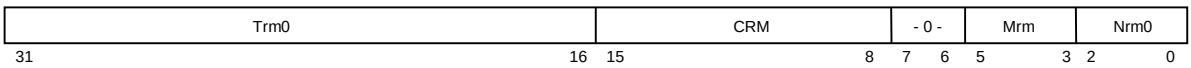


(11) APR (ABR parameter register)

Address: 400H

Access mode: Read/write

The APR register is used to set the parameters for each of the ABR service ports. The parameters set for each channel (VC) are set in the transmission/reception VC table. It is not possible to write to bits 7 and 6. Upon a read, 0 is returned.



Trm0 The Trm parameter is used to set the time required to transmit the FRM cell required by the active source.

The host must set Trm0 so that Trm is expressed in cell time units. (1 cell time = 2.8312 μs. The μPD98405 performs rate calculation by excluding the overhead incurred by SONET/SDH, giving a maximum rate of 149.76 Mbps).

Trm (milliseconds) = Trm0*2.8312/1000

Default value after reset (Trm0): 35,321 (89F9H)

CRM Missing RM cell count.

The CRM parameter is used to set the maximum number of FRM cells that can be transmitted prior to reception of the BRM cell.

Default value after reset: 255

Mrm The Mrm parameter is used to control the bandwidth (cell count) allotted to BRM cells or data cells while FRM cells are being transmitted.

Default value after reset: 2

Nrm0 The Nrm parameter is used to set the maximum number of cells that can be transmitted by the source while FRM cells are being transmitted.

Nrm is expressed as shown below.

$Nrm = 2*2^{Nrm0}$

Default value after reset (Nrm0): 4

(12) TBW (total bandwidth register)

Address: 401H

Access mode: Read/write

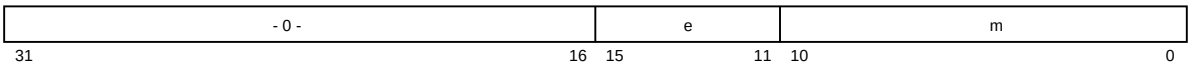
The TBW register is used to set the total bandwidth available to the μPD98405. A bandwidth of 155 Mbps or 25 Mbps can be set. Calculate the bandwidth using the following expression, and set a value in units of cells/second.

$Bandwidth = 2^{e}*(1 + m/2,048)$ cells/second

The default is 155 Mbps, expressed as e = 18, m = 711. It is not possible to write to bits 31 to 16. Upon a read, 0 is returned.

★ It is not necessary to set the TBW register when not using the ABR service.

Remark The bandwidth setting differs slightly from the rate expression laid down by the ATM Forum. e is 5 bits wide, while m is 11 bits wide.

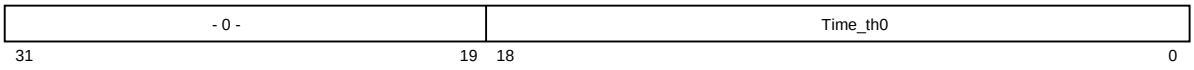


(13) TTH0 (time threshold register 0)

Address: 402H

Access mode: Read/write

The TTH0 register is used to set the threshold value used to detect internal congestion as part of the source internal congestion control of the ABR service. The default value after a reset is 7FFFFH. It is not possible to write to bits 31 to 19. Upon a read, 0 is returned (see **Section 5.8.6**).

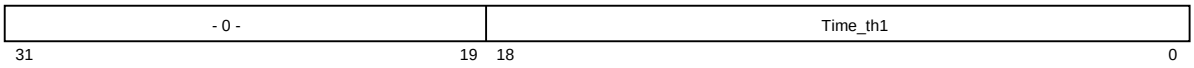


(14) TTH1 (time threshold register 1)

Address: 403H

Access mode: Read/write

The TTH1 register is used to set the rate reduction threshold value used after the detection of internal congestion as part of the source internal congestion control of the ABR service. The default value after a reset is 7FFFFH. It is not possible to write to bits 31 to 19. Upon a read, 0 is returned (see **Section 5.8.6**).

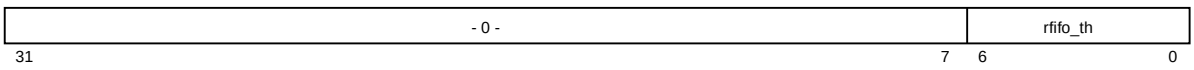


(15) RFTH (receive FIFO threshold register)

Address: 404H

Access mode Read/write

The RFTH register is used to set the threshold value used to detect internal congestion of the receive FIFO as part of the destination internal congestion control of the ABR service. The number of cells that must be accumulated in a receive FIFO to constitute congestion is set in this register. The default value after a reset is 7FH. It is not possible to write to bits 31 to 7. Upon a read, 0 is returned (see **Section 5.8.6**).

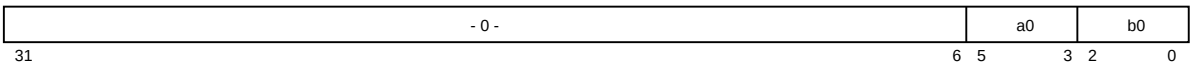


(16) ULR (Use-it-or-lose-it register)

Address: 405H

Access mode: Read/write

The ULR register is used to set Use-it-or-lose-it detection as part of the Use-it-or-lose-it control of the ABR service. The default value after a reset is 0. It is not possible to write to bits 31 to 6. Upon a read, 0 is returned (see **Section 5.8.6**).



The Use-it-or-lose-it function is used to reduce the value of ACR if the calculated ACR is greater than the actual rate. Upon the detection of Use-it-or-lose-it, the μPD98405 reduces ACR to a value equal to ACR*15/16. The conditions used to detect Use-it-or-lose-it are as follows.

In order to obtain the actual rate, the μPD98405 first obtains the average value of the in-rate FRM cell transmission interval (Ta). This is obtained using the following expression.

$Ta(t) = a*T + (1 - a)*Ta(t - 1)$

Ta: Average value of the in-rate FRM cell transmission interval (units: cells)

a: $a = 1/2^{a0}$ (a0: register setting)

T: Interval between the last and previous in-rate FRM cell to be transmitted (units: cells)

The conditions used to detect Use-it-or-lose-it are as follows.

$C_{link}*Nrm/ACR <= Ta*b$

C_{link}: Link capacity (149.76 Mbps)

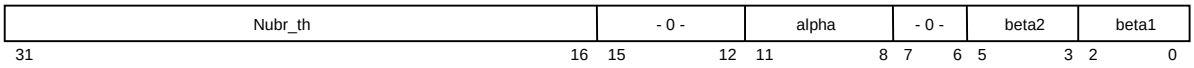
b: $b = 1 - 1/2^{b0}$ (b0: register setting)

(17) UBCR (UBR bandwidth control register)

Address: 500H

Access mode: Read/write

The UBCR register is used to set the band allocation for the UBR when both the ABR and UBR services are being used. It is not possible to write to bits 15 to 12, 7, and 6. Upon a read, 0 is returned.



Nubr_th Sets the number of VCs for the UBR service. Used as a threshold value when calculating the band allocation ratio for the UBR.

Default value after reset: 0

alpha Used for ABR internal congestion control. Sets the rate reduction allocation applied upon internal congestion (see **Section 5.8.6**).

Default value after reset: 0

beta2 If the actual UBR active VC count exceeds the value set with Nubr_th, the bandwidth allotted to UBR is set to the ratio specified with β2.

$\beta 2 = 1/2^{beta2}$

Default value after reset: 0

beta1 If the actual UBR active VC count is less than the value set with Nubr_th, the bandwidth allotted to UBR is set to the ratio specified with β1.

$\beta 1 = 1 - 1/2^{beta1}$

Default value after reset: 7

The bandwidth allotted to UBR is indicated by the following expressions.

if (n_ubr = 0) then	$C_{ABR} = C_{ABR+UBR}$
	$C_{UBR} = 0$
if (0 < n_ubr < Nubr_th) then	$C_{ABR} = (C_{ABR+UBR}$ - sum of MCR)* β1 + sum of MCR
	$C_{UBR} = (C_{ABR+UBR}$ - sum of MCR)*(1 - β1)
if (n_ubr ≥ Nubr_th) then	$C_{ABR} = (C_{ABR+UBR}$ - sum of MCR)* β2 + sum of MCR
	$C_{UBR} = (C_{ABR+UBR}$ - sum of MCR)*(1 - β2)

n_ubr: Actual UBR active VC count

C_{ABR}: ABR bandwidth

C_{UBR}: UBR bandwidth

$C_{ABR+UBR}$: ABR & UBR bandwidth (value set with the AUB register)

sum of MCR: Total of MCR values

β1: $\beta 1 = 1 - 1/2^{beta1}$

β2: $\beta 2 = 1/2^{beta2}$

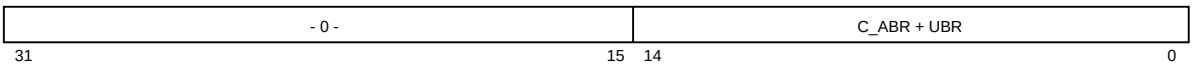
(18) AUB (ABR, UBR bandwidth register)

Address: 501H

Access mode: Read/write

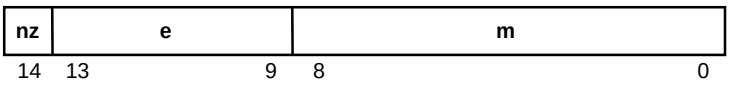
The AUB register is used to set the bandwidth that is exclusively occupied by the ABR and UBR services. The default value after a reset is 0. It is not possible to write to bits 31 to 15. Upon a read, 0 is returned.

★ It is not necessary to set the AUB register when not using the ABR service.



C_ABR+UBR ABR and UBR bandwidth. The bandwidth that is exclusively occupied by the ABR and UBR services is set according to the rate expression shown below.

Rate = $2^{e}*(1 + m/512)*nz$ cells/second

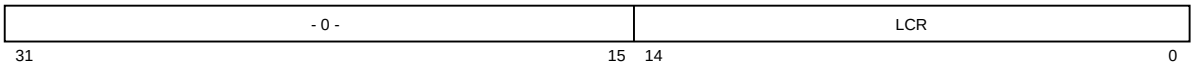


(19) LCR (internal congestion cell rate register)

Address: 502H

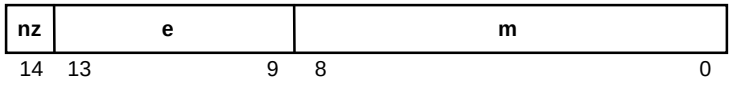
Access mode: Read/write

If a VC is performing transmission at a rate less than that set in the LCR register, rate reduction is not applied upon the detection of source internal congestion by the ABR service. To prevent rate reduction from being applied to a VC that is performing transmission at less than a given rate upon the occurrence of internal congestion, set that rate in the LCR register. The default value after a reset is 0. It is not possible to write to bits 31 to 15. Upon a read, 0 is returned.



LCR: Sets the internal congestion cell rate, obtained using the expression shown below.

Rate = 2^{e}*(1 + m/512)*nz cells/second



(20) Scheduler registers

Each of the sixteen shapers (for VBR) has five 32-bit registers. The host sets parameters that determine the average rate, peak rate, and priority of the shaper to be used. The μPD98405 uses these registers to store variables used for calculation during traffic control, and flags indicating the statuses of the shapers.

Two priority registers (addresses: 50H & 51H) are provided for the ABR scheduler. These registers are used to set the priorities of the ABR scheduler (in-rate/out-of-rate). For the ABR service priority, set a value less than that of VBR, but greater than UBR.

The default values of all these registers are 0. It is not possible to write to bits 26 to 5 of the Pri & Status register, or to bits 26 to 3, 1, and 0 of the Priority register. Upon a read, 0 is returned.

Cautions 1. The variables and flags used by the μPD98405 must be cleared to 0 and the parameters (I, M, P, C, and Priority) must be set before the enable bit (E) of a scheduler register can be set to 1.

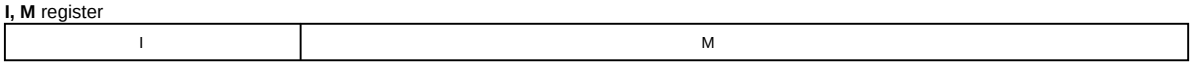
2. All the variables and flags in the scheduler registers of a shaper must be cleared to 0 before operation of the shaper can start.

3. The contents of the scheduler registers cannot be changed while the A bit is set to 1, that is, while the corresponding shaper is active. A shaper is inactive while no VC table is linked to it. Before attempting to change the I, M, P, or C parameter, ensure that the shaper is inactive (A bit = 0) then clear its enable bit (E) to 0. In such a case, all the variables and flags used by the μPD98405 must also be cleared to 0.

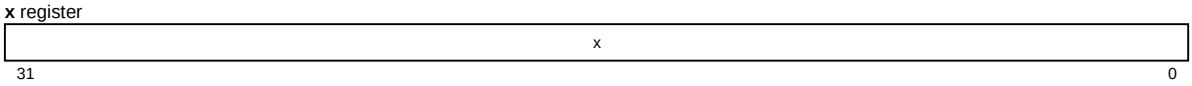
4. The host can modify the value of the priority parameter, but no other parameters, at any time. Furthermore, modification is also possible while the shaper is active (A bit = 1). In this case, set only the byte enable B3 bit of the Indirect_Access command to 1 to ensure that all other fields are not overwritten.

Address (H)	Register	Access mode	Function
0 - F	I, M	Read/write	I and M parameters of schedulers 0 through 15
10 - 1F	x	Read/write	x value of schedulers 0 through 15
20 - 2F	y	Read/write	y value of schedulers 0 through 15
30 - 3F	P, C, p, c	Read/write	P and C parameters and p and c values of schedulers 0 through 15
40 - 4F	Pri & Status	Read/write	Priority and status of schedulers 0 through 15
50	Priority	Read/write	Priority of ABR scheduler (in-rate)
51	Priority	Read/write	Priority of ABR scheduler (out-of-rate)

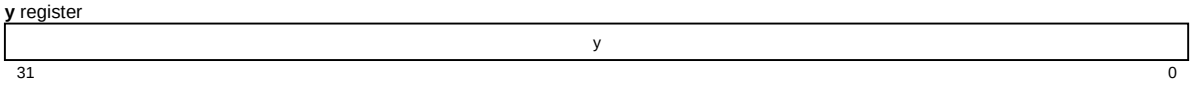
I, M register



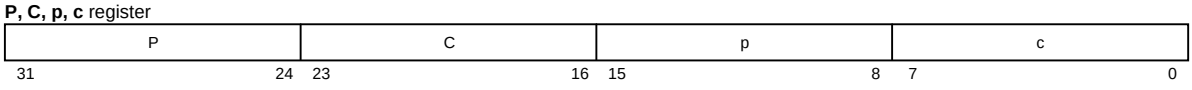
x register



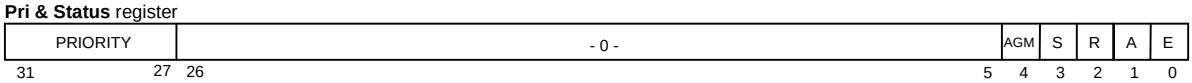
y register



P, C, p, c register

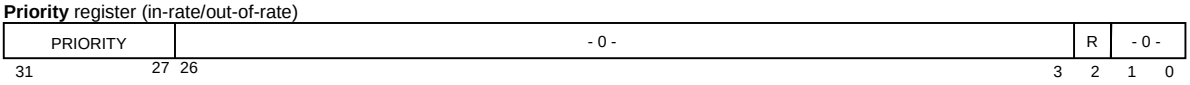


Pri & Status register



Field	Function	Value after reset
I, M	Average rate. The average rate parameter is set in cells. "I" cells are transmitted per "M" cell-times (I/M).	0
x, y	Used by μPD98405 to store temporary parameter.	0
P	Peak cell rate. Minimum time difference in transmission between two successive cells in channel linked to shaper. Specified in cells.	0
C	Credit. These bits specify the maximum number of credits that can be accumulated by a shaper. The I, M, P, and C parameters determine the maximum number of cells that can be transmitted continuously at the peak rate (maximum burst size).	0
p	Used by μPD98405 to store temporary parameter.	0
c	Used by μPD98405 to store temporary parameter.	0
PRIORITY	Priority. Host sets priorities of this shaper. '00000' is highest, and '11111' is lowest.	0
AGM	Aggregate mode. Sets the cell output mode. 0: Normal mode. The rate setting is applied in VC units. 1: Aggregate mode. The rate setting is applied in shaper units.	
S	Scan flag. Used by μPD98405 to manage status of shaper. Do not change value of this field.	0
R	Round robin flag. Used by μPD98405 to manage status of shaper. Do not change value of this field.	0
A	Active flag. Used by μPD98405 to manage status of shaper. 1: Shaper is active. 0: Shaper is inactive. This bit is set to 1 by host only when unassigned cell generator function is used.	0
E	Enable. Set to '1' by host when this shaper is used. 1: Enables shaper. 0: Disables shaper.	0

Priority register (in-rate/out-of-rate)



Field	Function	Value after reset
PRIORITY	Priority. Host sets priorities of this shaper. '00000' is highest, and '11111' is lowest.	0
R	Round robin flag. Used by μPD98405 to manage status of shaper. Do not change value of this field.	0

7.4 PHY REGISTER

(1) PHY command register 1 (PCMR1)

This register is used to set transmission of the Line AIS, Path AIS, Line RDI(FERF), and Path RDI(FERF) alarms, as well as the PHYALM pin output.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCMR1	0	0	0	ALM	LAIS	PAIS	LRDI	PRDI	00H	00H	R/W

Field	Function		Default value
Bit 4: ALM	Sets the output level of the PHYALM pin when the CMD bit of the AMR1 register is not masked.		0
	1	Sets the PHYALM pin output to high level.	
	0	The PHYALM pin output is not set.	
Bit 3: LAIS	Used to set Line AIS transmission.		0
	1	Sets Line AIS transmission. Changes the K2 byte (bit 6 to bit 8) of the transmission frame to 111 and, before scrambling all bytes other than the section overhead byte, changes all the bits of the transmission frame to 1.	
	0	Line AIS is not set.	
Bit 2: PAIS	Used to set Path AIS transmission.		0
	1	Sets Path AIS transmission. Changes all the bits of H1 to H3 of the transmission frame, as well as all the bits of the payload area, to 1.	
	0	Path AIS is not set.	
Bit 1: LRDI	Used to set Line RDI transmission.		0
	1	Sets Line RDI transmission. Changes the K2 byte (bit 6 to bit 8) of the transmission frame to 110.	
	0	Line RDI is not set.	
Bit 0: PRDI	Used to set Path RDI transmission.		0
	1	Sets Path RDI transmission. Changes bit 5 of the G1 byte of the transmission frame to 1.	
	0	Path RDI is not set.	

Remarks 1. If both Line AIS and Line RDI are set for the same frame, Line AIS takes priority.

2. Upon reading this register, 0 will be returned for the high-order three bits. It is not possible to write to the high-order three bits.

(2) PHY command register 2 (PCMR2)

This register is used to initialize the registers of the μPD98405.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCMR2	0	0	0	0	0	ICR	PCR	ALR	01H	00H	R/W

Field	Function		Default value
D2: ICR	Used to initialize all interrupt cause registers.		0
	1	Initializes all interrupt cause registers (PICR, ACR, PCR, PCOCR).	
	0	Interrupt cause registers are not initialized.	
D1: PCR	Used to initialize all performance counters.		0
	1	Initializes all performance counters (counter value, load register, and point register).	
	0	Performance counters are not initialized.	
D0: ALR	Used to set the initialization of all registers.		0
	1	All LSI registers are initialized to their default values.	
	0	Registers are not initialized.	

Remark Upon reading this register, 0 will be returned for the high-order five bits. It is not possible to write to the high-order five bits.

(3) PHY command register 3 (PCMR3)

This register is used to transmit frames containing alarms or error notification. Using this function, a user can forcibly transmit a dummy frame containing notifications of errors. This function can be used while performing testing.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCMR3	0	0	0	0	CM3	CM2	CM1	CM0	02H	00H	R/W

Field	Function	Default value
D3-D0: CM3-CM0	Used to transmit dummy error frames containing alarms or notifications of errors.	All 0

CM3-CM0	Transmit frame
0000	Normal frame
0001	LOS frame
0010	OOF frame
0011	LOF frame
0100	LOP frame
0101	OCD frame
0110	LCD frame
0111	B1 error frame
1000	B2 error frame
1001	B3 error frame
1010	Line FEBE frame
1011	Path FEBE frame
Others	Normal frame

Remark Upon reading this register, 0 will be returned for the high-order four bits. It is not possible to write to the high-order four bits.

(4) Mode register 1 (MDR1)

This register is used to select the mode of the μPD98405.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
MDR1	0	SS1	SS0	0	0	0	0	0	03H	00H	R/W

Field	Function	Default value
D6, D5: SS1, SS0	Used to set the SS bit code of the 1st to 3rd H1 bytes of the transmission frame overhead.	00

	B7	B6	B5	B4	B3	B2	B1	B0
1st H1	0	1	1	0	SS1	SS0	1	0
2nd H1	1	0	0	1	SS1	SS0	1	1
3rd H1	1	0	0	1	SS1	SS0	1	1

Remark Upon reading this register, 0 will be returned for the D7 bit and the D2 to D0 bits. It is not possible to write to these bits. Writing to the D4 and D3 bits is possible, however. Set these bits to 0.

(5) Mode register 2 (MDR2)

This register is used to select the mode of the μPD98405.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
MDR2	0	oolenb	idlenb	LP1	LP0	RxCL	RCM1	RCM0	04H	00H	R/W

Field	Function		Default value
D6: oolenb	Used to set the automatic switching function of the receive clock in the OOL status.		0
	1	Uses the receive clock when the receive clock recovery PLL has failed to lock successfully (OOL status).	
	0	Automatically uses the transmission clock as the receive clock in the OOL status.	
D5: idlenb	Used to select the format of a free cell to insert.		0
	1	Inserts an unassigned cell as a free cell.	
	0	Inserts an idle cell as a free cell.	
D4: LP1 D3: LP0	Used to set the loopback mode.		00

LP[1:0]	Mode
00	Sets normal mode.
01	**RPLP mode** Sets loopback from the PMD input to the PMD output, before the serial/parallel converter circuit.
10	**TPLP mode** Sets loopback from the ATM input to the ATM output, via the serial/parallel converter circuit.
11	Cannot be set.

★	D2: RxCL	Used to select the source of the receive clock. This function is for testing. Set RxCL = 0 during normal operation.		0
		1	Uses the clock generated by the transmission synthesizer PLL as the receive clock.	
		0	Uses the clock extracted by the receive clock recovery PLL as the receive clock.	
	D1: RCM1 D0: RCM0	Used to select the interrupt mode.		00

RCM[1:0]	Mode
00	Selects interrupt mode 1. The bits of the PHY interrupt registers are held as is until read by the host. Even if the source target is cleared, the status bit remains set.
01	Selects interrupt mode 2. Even if the host reads the contents of a PHY interrupt register, the bits are not reset. The status remains set until the source itself is cleared.
1X	Selects interrupt mode 3. Even if the cause of an interrupt has not been cleared, this bit is reset when the host reads the PHY interrupt register.

PHY interrupt registers: PICR, ACR, PCR
For details of operations of these registers, see **Section 6.8**.

Remark Upon reading this register, 0 is returned for the D7 bit. It is not possible to write to the D7 bit.

(6) Mode register 3 (MDR3)

This register is used to select the mode of the μPD98405.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
MDR3	INTENB	FSCRM	CSCRM	HECENB	CORENB	0	0	0	05H	00H	R/W

Field		Function	Default value
D7: INTENB	Used to select the cell synchronous status transition.		0
	1	The cell synchronous state is not changed to the hunting state when the line failure (OOF, LOP, or PAIS) field becomes active.	
	0	The cell synchronous state is forcibly changed to the hunting state when the line failure (OOF, LOP, or PAIS) field becomes active.	
D6: FSCRM	Used to select the frame scramble/descramble mode.		0
	1	Frame scramble/descramble is not performed.	
	0	Frame scramble/descramble is performed.	
D5: CSCRM	Used to select the cell scramble/descramble mode.		0
	1	Cell scramble/descramble is not performed.	
	0	Cell scramble/descramble is performed.	
D4: HECENB	Used to select the HEC error cell discard mode.		0
	1	Cells in which an HEC error is detected are not discarded.	
	0	Cells in which an HEC error is detected are discarded.	
D3: CORENB	Used to select the HEC error correction mode.		0
	1	1-bit HEC errors are not corrected. Cells in which a 1-bit HEC error is detected are discarded.	
	0	1-bit HEC errors are corrected.	

Remark Upon reading this register, 0 will be returned for the low-order three bits. It is not possible to write to the low-order three bits.

(7) PHY interrupt cause register (PICR)

This register is used to indicate the cause of an interrupt request.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PICR	OOL	0	LOS	LOF	ALM	PFM	PCO	RFO	06H	00H	R

Field		Function	Default value
D7: OOL	Used to indicate the lock state of the clock recovery PLL.		0
	1	Indicates that the clock recovery PLL has been unlocked.	
	0	Indicates that the clock recovery PLL operates normally.	
D5: LOS	Used to indicate the LOS state.		0
	1	Indicates the occurrence of LOS (Loss Of Signal).	
	0	Indicates that LOS has not occurred.	
D4: LOF	Used to indicate the LOF state.		0
	1	Indicates the occurrence of LOF (Loss Of Frame).	
	0	Indicates that LOF has not occurred.	
D3: ALM	Used to indicate the ACR register state.		0
	1	Indicates the occurrence of a circuit failure, as indicated by the ACR register (OOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI).	
	0	Indicates the non-occurrence of the circuit failure indicated by the ACR register.	
D2: PFM	Used to indicate the PCR register state.		0
	1	Indicates the detection of the performance detailed cause indicated by the PCR register (Frequency justification, B1E, B2E, B3E, Line FEBE, Path FEBE).	
	0	Indicates that the performance detailed cause indicated by the PCR register has not been detected.	
D1: PCO	Used to indicate the state of the performance counter.		0
	1	Indicates that a performance counter (B1EC, B2EC, B3EC, LFBC, PFBC, FJC, HECC, FULC, IDLC, INFC) overflow has occurred.	
	0	Indicates that the performance counter has not overflowed.	
D0: RFO	Used to indicate the occurrence of a receive FIFO overrun.		0
	1	Indicates that a receive FIFO overrun has occurred.	
	0	Indicates that a receive FIFO overrun has not occurred.	

Remarks 1. Upon reading this register, 0 will be returned for the D6 bit. It is not possible to write to the D6 bit.

2. If any one bit of these registers is set to 1, the PI bit of the GSR register will be set to 1.

(8) PHY interrupt mask register (PIMR)

This register is used to set the masking of the cause of each PICR (06H) interrupt.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PIMR	OOL	0	LOS	LOF	ALM	PFM	PCO	RFO	07H	00H	R/W

Field		Function	Default value
D7: OOL	Used to mask/unmask an interrupt request due to OOL occurrence.		0
	1	Does not mask an interrupt request due to OOL occurrence.	
	0	Masks an interrupt request due to OOL occurrence.	
D5: LOS	Used to mask/unmask an interrupt request due to LOS occurrence.		0
	1	Does not mask an interrupt request due to LOS occurrence.	
	0	Masks an interrupt request due to LOS occurrence.	
D4: LOF	Used to mask/unmask an interrupt request due to LOF occurrence.		0
	1	Does not mask an interrupt request due to LOF occurrence.	
	0	Masks an interrupt request due to LOF occurrence.	
D3: ALM	Used to mask/unmask an interrupt request due to circuit failure occurrence.		0
	1	Does not mask an interrupt request due to the occurrence of a circuit failure (OOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI), indicated in the ACR register (address: 08H).	
	0	Masks an interrupt request due to the occurrence of a circuit failure, indicated in the ACR (Alarm Cause Register, address: 08H).	
D2: PFM	Used to mask/unmask an interrupt request due to a performance detailed cause.		0
	1	Does not mask an interrupt request due to a performance detailed cause (B1EC, B2EC, B3EC, LFBC, PFBC, FJC, HECC, FULC, IDLC, INFC), indicated in the PCR register (address: 0AH).	
	0	Masks an interrupt request due to a performance detailed cause, indicated in the PCR.	
D1: PCO	Used to mask/unmask an interrupt request due to performance counter overflow occurrence.		0
	1	Does not mask an interrupt request due to performance counter overflows.	
	0	Masks an interrupt request due to performance counter overflows.	
D0: RFO	Used to mask/unmask an interrupt request due to receive FIFO overflows.		0
	1	Does not mask an interrupt request due to receive FIFO overflows.	
	0	Masks an interrupt request due to receive FIFO overflows.	

Remark Upon reading this register, 0 will be returned for the D6 bit. It is not possible to write to the D6 bit.

(9) Alarm cause register (ACR)

This register is used to indicate the cause of a circuit failure.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ACR	OOF	LOP	OCD	LCD	LAIS	PAIS	LRDI	PRDI	08H	00H	R

Field	Function		Default value
D7: OOF	Used to indicate the OOF (Out Of Frame) status.		0
	1	Indicates that OOF has occurred.	
	0	Indicates that OOF has not occurred.	
D6: LOP	Used to indicate the LOP (Loss Of Pointer) status.		0
	1	Indicates that LOP has occurred.	
	0	Indicates that LOP has not occurred.	
D5: OCD	Used to indicate the OCD (Out of Cell Delineation) status.		0
	1	Indicates that OCD has occurred.	
	0	Indicates that OCD has not occurred.	
D4: LCD	Used to indicate the LCD (Loss of Cell Delineation) status.		0
	1	Indicates that LCD has occurred.	
	0	Indicates that LCD has not occurred.	
D3: LAIS	Used to indicate the Line AIS status.		0
	1	Indicates that Line AIS has occurred.	
	0	Indicates that Line AIS has not occurred.	
D2: PAIS	Used to indicate the Path AIS status.		0
	1	Indicates that Path AIS has occurred.	
	0	Indicates that Path AIS has not occurred.	
D1: LRDI	Used to indicate the Line RDI status.		0
	1	Indicates that Line RDI has occurred.	
	0	Indicates that Line RDI has not occurred.	
D0: PRDI	Used to indicate the Path RDI status.		0
	1	Indicates that Path RDI has occurred.	
	0	Indicates that Path RDI has not occurred.	

Caution In pointer status transition, an LOP bit is not cleared for an LOP → Path-AIS transition. To determine LOP by software, include a condition that the PAIS bit must be 0.

Remark If any one bit of these registers is set to 1, the ALM bit of PICR (address: 06H) will be set to "1."

(10) Alarm cause mask register (ACMR)

This register is used to set the masking of the cause of a circuit failure, held in the ACR (address: 08H). When masking is set, the ALM bit of the PICR (address: 06H) is not set.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ACMR	OOF	LOP	OCD	LCD	LAIS	PAIS	LRDI	PRDI	09H	00H	R/W

Field	Function		Default value
D7: OOF	Used to set masking of the notification of OOF (Out Of Frame) detection.		0
	1	Does not mask notification of OOF.	
	0	Masks notification of OOF.	
D6: LOP	Used to set masking of the notification of LOP (Loss Of Pointer) detection.		0
	1	Does not mask notification of LOP.	
	0	Masks notification of LOP.	
D5: OCD	Used to set masking of the notification of OCD (Out of Cell Delineation) detection.		0
	1	Does not mask notification of OCD.	
	0	Masks notification of OCD.	
D4: LCD	Used to set masking of the notification of LCD (Loss of Cell Delineation) detection.		0
	1	Does not mask notification of LCD.	
	0	Masks notification of LCD.	
D3: LAIS	Used to set masking of the notification of Line AIS detection.		0
	1	Does not mask notification of Line AIS.	
	0	Masks notification of Line AIS.	
D2: PAIS	Used to set masking of the notification of Path AIS detection.		0
	1	Does not mask notification of Path AIS.	
	0	Masks notification of Path AIS.	
D1: LRDI	Used to set masking of the notification of Line RDI detection.		0
	1	Does not mask notification of Line RDI.	
	0	Masks notification of Line RDI.	
D0: PRDI	Used to set masking of the notification of Path RDI detection.		0
	1	Does not mask notification of Path RDI.	
	0	Masks notification of Path RDI.	

(11) Performance cause register (PCR)

This register is used to indicate a performance detailed cause.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCR	0	0	FJ	B1E	B2E	B3E	LFEB	PFEB	0AH	00H	R

Field	Function		Default value
D5: FJ	Used to indicate the FJ (Frequency Justification) status.		0
	1	Indicates that FJ has been applied.	
	0	Indicates that FJ has not been applied.	
D4: B1E	Used to indicate the B1 error status.		0
	1	Indicates that a B1 error has occurred.	
	0	Indicates that a B1 error has not occurred.	
D3: B2E	Used to indicate the B2 error status.		0
	1	Indicates that a B2 error has occurred.	
	0	Indicates that a B2 error has not occurred.	
D2: B3E	Used to indicate the B3 error status.		0
	1	Indicates that a B3 error has occurred.	
	0	Indicates that a B3 error has not occurred.	
D1: LFEB	Used to indicate the Line FEBE status.		0
	1	Indicates that Line FEBE has occurred.	
	0	Indicates that Line FEBE has not occurred.	
D0: PFEB	Used to indicate the Path FEBE status.		0
	1	Indicates that Path FEBE has occurred.	
	0	Indicates that Path FEBE has not occurred.	

Remarks 1. Upon reading this register, 0 will be returned for the high-order two bits. It is not possible to write to the high-order two bits.

2. If any one bit of these registers is set to 1, the PFM bit of PICR (address: 06H) will be set to 1.

(12) Performance cause mask register (PCMR)

This register is used to set masking of the performance detailed cause of PCR (address: 0AH). When masking is applied, the PFM bit of PICR (address: 06H) is not set.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCMR	0	0	FJ	B1E	B2E	B3E	LFEB	PFEB	0BH	00H	R/W

Field	Function		Default value
D5: FJ	Used to set masking of the notification of FJ (Frequency Justification) application.		0
	1	Does not mask notification of FJ application.	
	0	Masks notification of FJ application.	
D4: B1E	Used to set masking of the notification of B1 error detection.		0
	1	Does not mask notification of B1 error detection.	
	0	Masks notification of B1 error detection.	
D3: B2E	Used to set masking of the notification of B2 error detection.		0
	1	Does not mask notification of B2 error detection.	
	0	Masks notification of B2 error detection.	
D2: B3E	Used to set masking of the notification of B3 error detection.		0
	1	Does not mask notification of B3 error detection.	
	0	Masks notification of B3 error detection.	
D1: LFEB	Used to set masking of the notification of Line FEBE detection.		0
	1	Does not mask notification of Line FEBE detection.	
	0	Masks notification of Line FEBE detection.	
D0: PFEB	Used to set masking of the notification of Path FEBE detection.		0
	1	Does not mask notification of Path FEBE detection.	
	0	Masks notification of Path FEBE detection.	

Remark Upon reading this register, 0 will be returned for the high-order two bits. It is not possible to write to the high-order two bits.

(13) Internal alarm cause mask register (IACM)

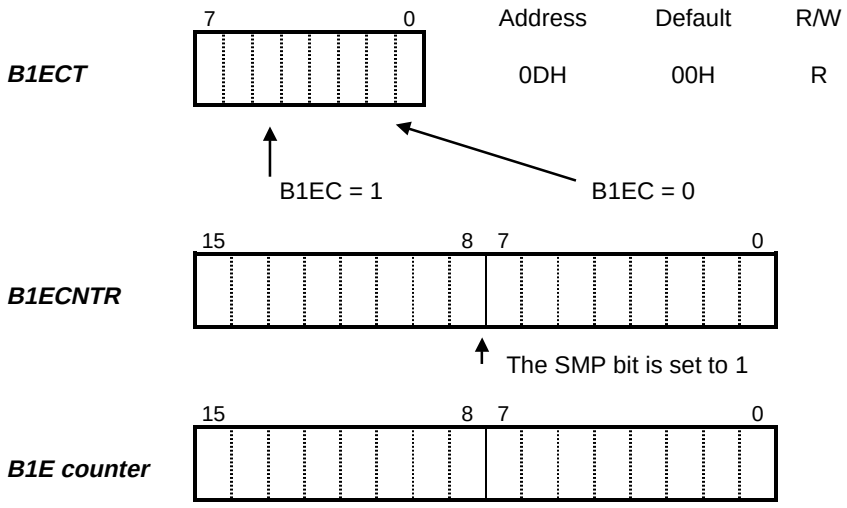
This register is used to set masking of the transmission of alarm frames that are internally generated automatically.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
IACM	0	0	0	0	0	0	LRDI	PRDI	0CH	00H	R/W

Field	Function		Default value
D1: LRDI	Used to set masking of Line RDI automatic transmission.		0
	1	Does not mask transmission of Line RDI that is automatically generated internally.	
	0	Masks transmission of Line RDI that is automatically generated internally.	
D0: PRDI	Used to set masking of Path RDI automatic transmission.		0
	1	Does not mask transmission of Path RDI that is automatically generated internally.	
	0	Masks transmission of Path RDI that is automatically generated internally.	

Remark Upon reading this register, 0 will be returned for the high-order six bits. It is not possible to write to the high-order six bits.

(14) B1 error count register (B1ECT)



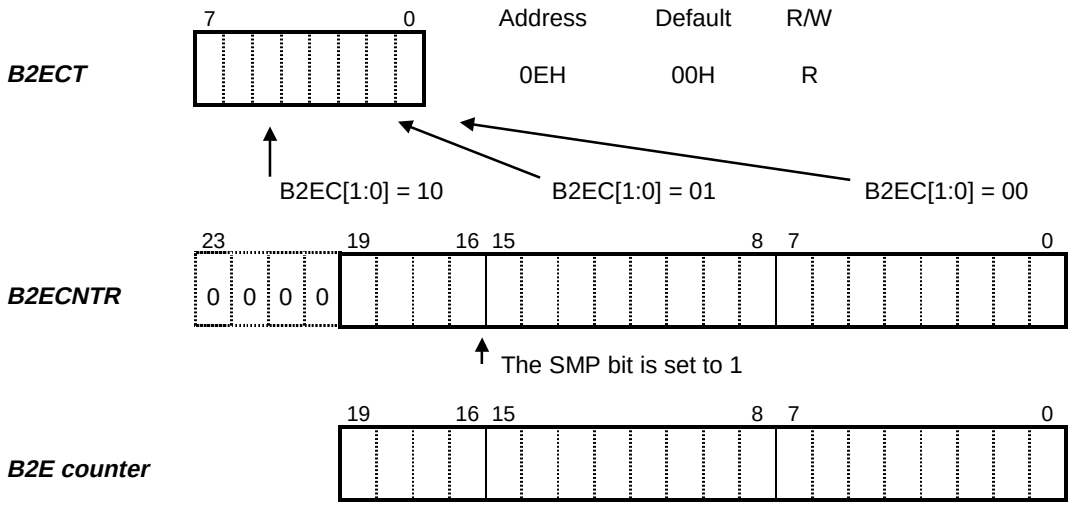
This is a window register that is used to read the value held in the 16-bit **B1ECNTR** register by repeatedly reading eight bits, two times. First, the low-order eight bits of the register (**B1ECNTR[7:0]**) are read out, after which the high-order eight bits (**B1ECNTR[15:8]**) are read. Whether the high- or low-order eight bits are read is indicated by the setting of the **B1EC** bit of the **PCPR1** register (address: 19H). By default the **B1EC** bit of the **PCPR1** register is set to 0, this changing automatically (from 0 to 1 to 0, etc.) every time the **B1ECT** register is read.

B1ECNTR is a load register that is used to sample (store) the value of the B1 error counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **B1E counter** is stored into the **B1ECNTR** register. This value indicates the number of B1 errors that have occurred since the contents of the **B1E counter** were last sampled. The value stored into the **B1ECNTR** register is held until the **B1E counter** is next sampled.

Sampling the contents of the **B1E counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **B1EC** bit of the **PCIR1** register (address: 1CH) is set to 1.

When the value of the counter is all F, the **B1EC** bit of the **PCOCR1** register (address: 20H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **B1E counter** again starts to count up from 0.

(15) B2 error count register (B2ECT)



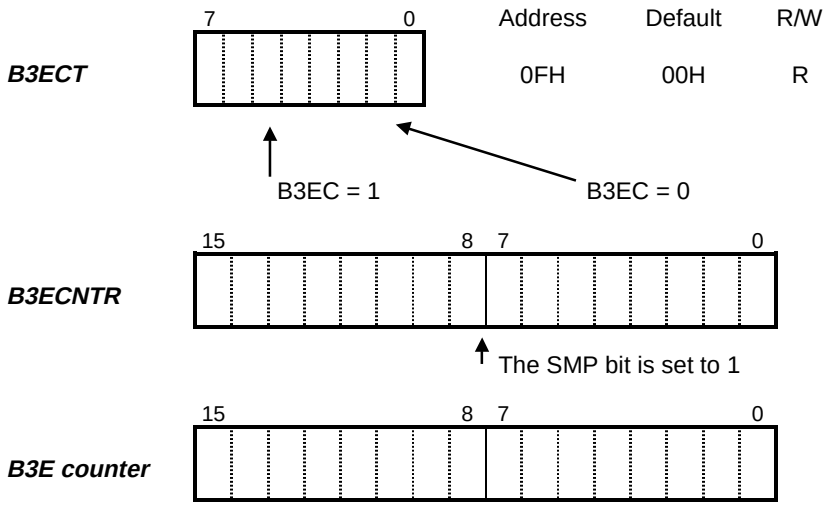
This is a window register that is used to read the contents of the 20-bit **B2ECNTR** register by reading eight bits, eight bits, and four bits, three times. First, the low-order eight bits (**B2ECNTR[7:0]**) are read, then the middle eight bits (**B2ECNTR[15:8]**), and finally the high-order four bits (**B2ECNTR[19:16]**). Which of the low-order, middle, or high-order bits is read is indicated by the **B2EC1** and **B2EC0** bits of the **PCPR1** register (address: 19H). For each of these bits, the default value is 00. Each time the **B2ECT** register is read, the value of these bits changes in the order of 00 → 01 → 10 → 00 → 01.

B2ECNTR is a load register that is used to sample (store) the value of the B2 error counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **B2E counter** is stored into the **B2ECNTR register**. This value indicates the number of B2 errors that have occurred since the contents of the **B2E counter** were last sampled. The value stored into the **B2ECNTR** register is held until the **B2E counter** is next sampled.

Sampling the contents of the **B2E counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **B2EC** bit of the **PCIR1** register (address: 1CH) is set to 1.

When the value of the counter is all F, the **B2EC** bit of the **PCOCR1** register (address: 20H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **B2E counter** again starts to count up from 0.

(16) B3 error count register (B3ECT)



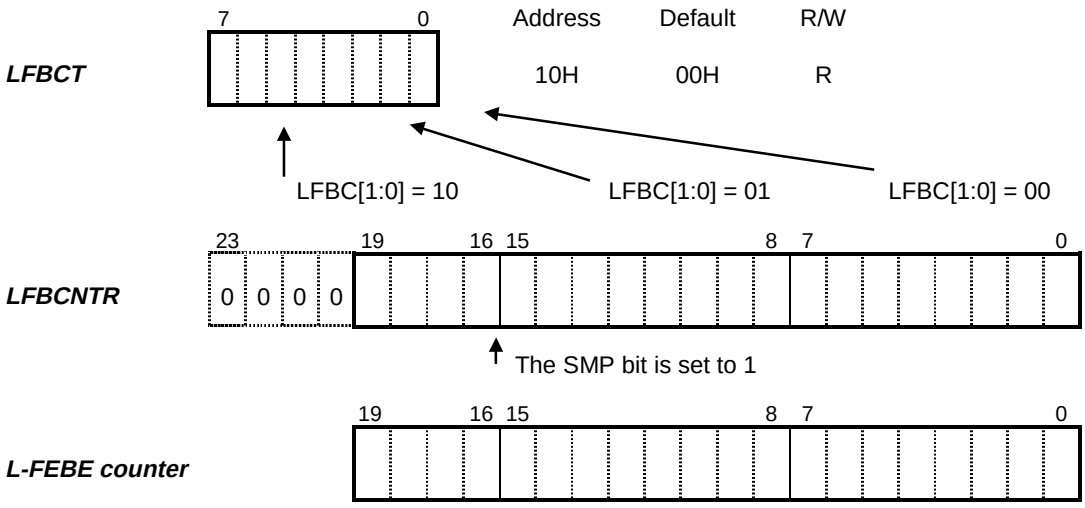
This is a window register that is used to read the contents of the 16-bit **B3ECNTR** register by repeatedly reading eight bits, two times. First, the low-order eight bits (**B3ECNTR[7:0]**) are read, followed by the high-order eight bits (**B3ECNTR[15:8]**). Whether the low- or high-order bits are read is indicated by the **B3EC** bit of the **PCPR1** register (address: 19H). The default value of the **B3EC** bit of the **PCPR1** register is 0. Each time the **B3ECT** register is read, the value of this bit changes in the order of 0 $\rightarrow$ 1 $\rightarrow$ 0.

B3ECNTR is a load register that is used to sample (store) the value of the B3 error counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **B3E counter** is stored into the **B3ECNTR** register. This value indicates the number of B3 errors that have occurred since the contents of the **B3E counter** were last sampled. The value stored into the **B3ECNTR** register is held until the **B3E counter** is next sampled.

Sampling the contents of the **B3E counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **B3EC** bit of the **PCIR1** register (address: 1CH) is set to 1.

When the value of the counter is all F, the **B3EC** bit of the **PCOCR1** register (address: 20H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **B3E counter** again starts to count up from 0.

(17) Line FEBE error count register (LFBCT)



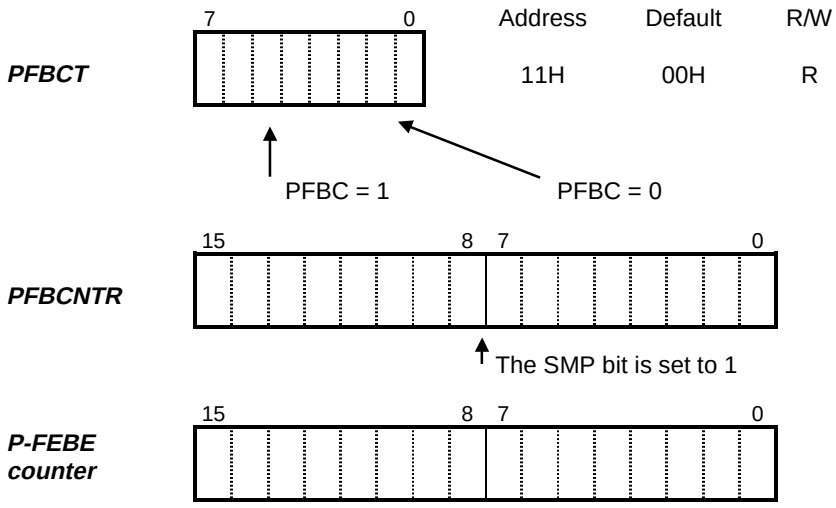
This is a window register that is used to read the contents of the 20-bit **LFBCNTR** register by reading eight bits, eight bits, and four bits, three times. First, the low-order eight bits (**LFBCNTR[7:0]**) are read, then the middle eight bits (**LFBCNTR[15:8]**), and finally the high-order four bits (**LFBCNTR[19:16]**). Which of the low-order, middle, or high-order bits is read is indicated by the **LFBC1** and **LFBC0** bits of the **PCPR1** register (address: 19H). For each of these bits, the default value is 00. Each time the **LFBCT** register is read, the value of these bits is automatically changed in the order of 00 → 01 → 10 → 00 → 01.

LFBCNTR is a load register that is used to sample (store) the value of the **L-FEBE counter**. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **L-FEBE counter** is stored into the **LFBCNTR** register. This value indicates the number of times **Line-FEBE** has been detected since the contents of the **L-FEBE counter** were last sampled. The value stored into the **LFBCNTR** register is held until the **L-FEBE counter** is next sampled.

Sampling the contents of the **L-FEBE counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **LFBC** bit of the **PCIR1** register (address: 1CH) is set to 1.

When the value of the counter is all F, the **LFBC** bit of the **PCOCR1** register (address: 20H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **L-FEBE counter** again starts to count up from 0.

(18) Path FEBE error count register (PFBCT)



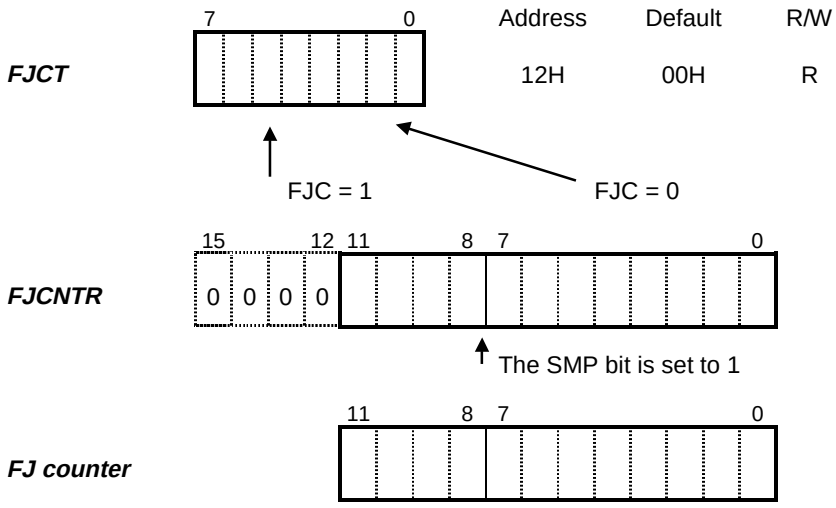
This is a window register that is used to read the value held in the 16-bit **PFBCNTR** register by repeatedly reading eight bits, two times. First, the low-order eight bits of the register (**PFBCNTR[7:0]**) are read, after which the high-order eight bits (**PFBCNTR[15:8]**) are read. Whether the high- or low-order eight bits are read is indicated by the setting of the **PFBC** bit of the **PCPR1** register (address: 19H). By default the **PFBC** bit of the **PCPR1** register is set to 0. This is changed automatically (from 0 to 1 to 0, etc.) every time the **PFBCT** register is read.

PFBCNTR is a load register that is used to sample (store) the value of the P-FEBE counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **P-FEBE counter** is stored into the **PFBCNTR** register. This value indicates the number of times Path-FEBE has been detected since the contents of the **P-FEBE counter** were last sampled. The value stored into the **PFBCNTR** register is held until the **P-FEBE counter** is next sampled.

Sampling the contents of the **P-FEBE counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **PFBC** bit of the **PCIR1** register (address: 1CH) is set to 1.

When the value of the counter is all F, the **PFBC** bit of the **PCOCR1** register (address: 20H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **P-FEBE counter** again starts to count up from 0.

(19) Frequency Justification count register (FJCT)



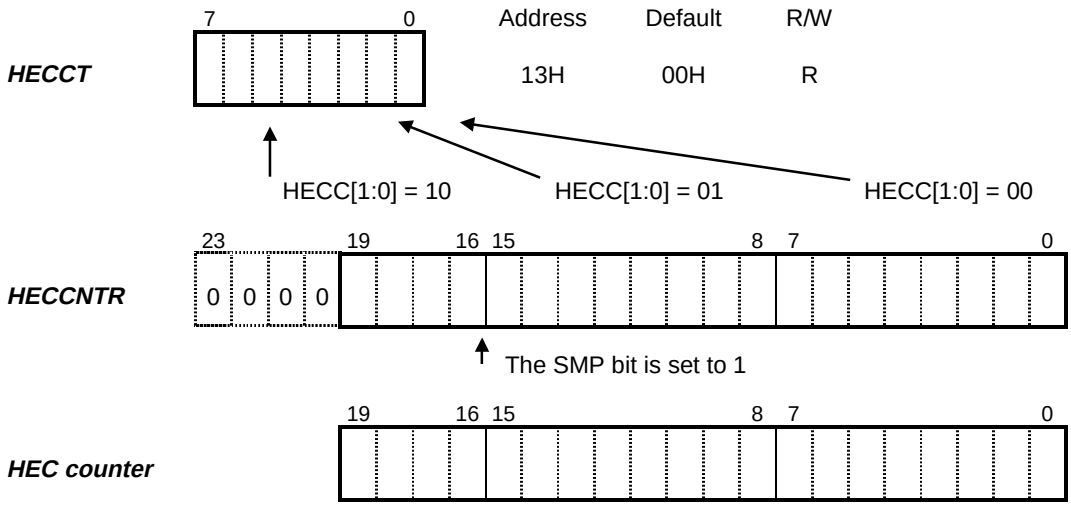
This is a window register that is used to read the value held in the 12-bit **FJCNTR** register by reading eight bits and four bits, two times. First, the low-order eight bits of the register (**FJCNTR[7:0]**) are read, after which the high-order four bits (**FJCNTR[11:8]**) are read. Whether the high- or low-order bits are read is indicated by the setting of the **FJC** bit of the **PCPR1** register (address: 19H). By default the **FJC** bit of the **PCPR1** register is set to 0. This is changed automatically (from 0 to 1 to 0, etc.) every time the **FJCT** register is read.

FJCNTR is a load register that is used to sample (store) the value of the **FJ counter**. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **FJ counter** is stored into the **FJCNTR** register. This value indicates the number of times Frequency Justification has been applied since the contents of the **FJ counter** were last sampled. The value stored into the **FJCNTR** register is held until the **FJ counter** is next sampled.

Sampling the contents of the **FJ counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **FJC** bit of the **PCIR1** register (address: 1CH) is set to 1.

When the value of the counter is all F, the **FJC** bit of the **PCOCR1** register (address: 20H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **FJ counter** again starts to count up from 0.

(20) HEC error count register (HECCT)



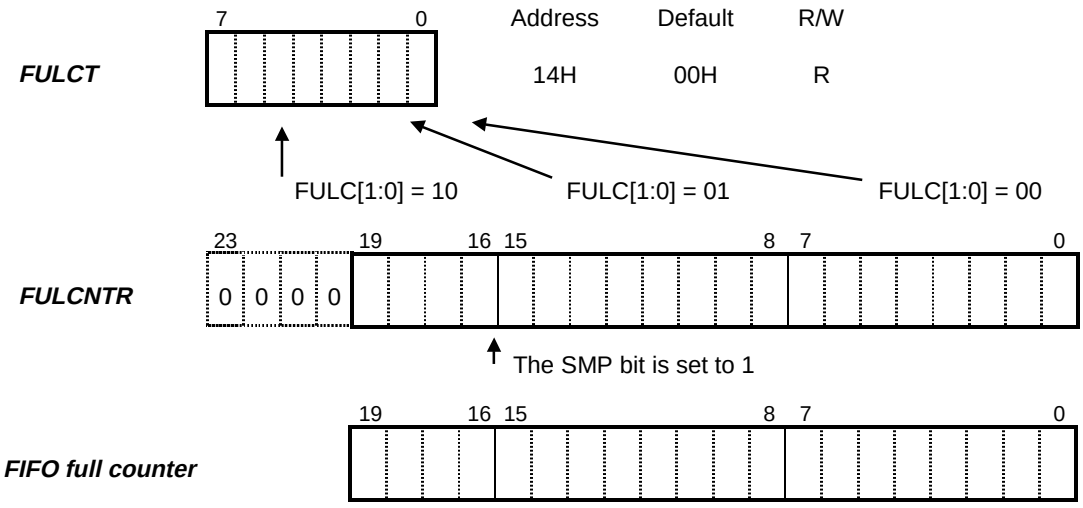
This is a window register that is used to read the contents of the 20-bit **HECCNTR** register by reading eight bits, eight bits, and four bits, three times. First, the low-order eight bits (**HECCNTR[7:0]**) are read, then the middle eight bits (**HECCNTR[15:8]**), and finally the high-order four bits (**HECCNTR[19:16]**). Which of the low-order, middle, or high-order bits is read is indicated by the **HECC1** and **HECC0** bits of the **PCPR2** register (address: 1AH). For each of these bits, the default value is 00. Each time the **HECCT** register is read, the value of these bits is automatically changed in the order of 00 → 01 → 10 → 00 → 01.

HECCNTR is a load register that is used to sample (store) the value of the HEC counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **HEC counter** is stored into the **HECCNTR** register. This value indicates the number of cells that have been discarded as a result of HEC errors since the contents of the **HEC counter** were last sampled. The value stored into the **HECCNTR** register is held until the **HEC counter** is next sampled.

Sampling the contents of the **HEC counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **HECC** bit of the **PCIR2** register (address: 1DH) is set to 1.

When the value of the counter is all F, the **HECC** bit of the **PCOCR2** register (address: 21H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **HEC counter** again starts to count up from 0.

(21) FIFO full count register (FULCT)



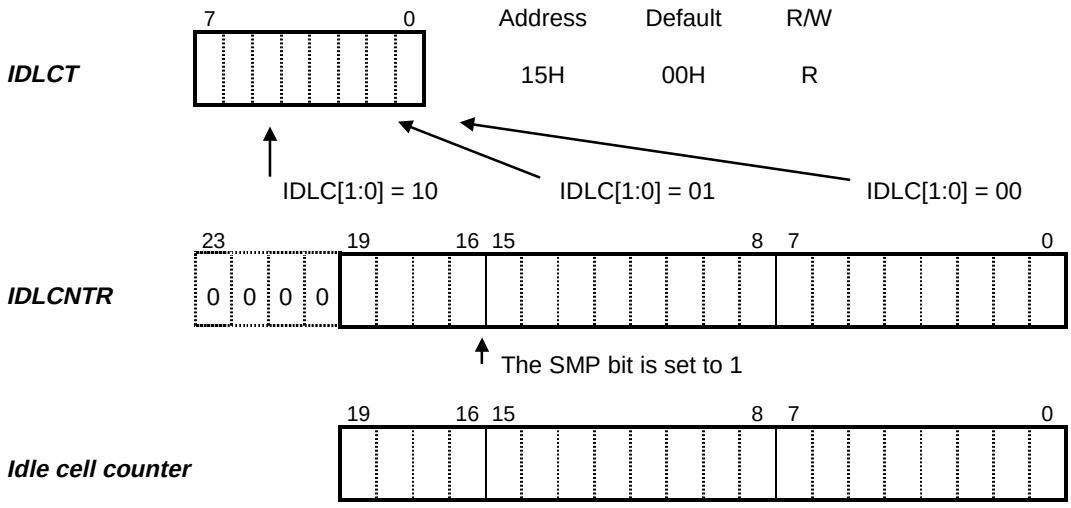
This is a window register that is used to read the contents of the 20-bit **FULCNTR** register by reading eight bits, eight bits, and four bits, three times. First, the low-order eight bits (**FULCNTR[7:0]**) are read, then the middle eight bits (**FULCNTR[15:8]**), and finally the high-order four bits (**FULCNTR[19:16]**). Which of the low-order, middle, or high-order bits is read is indicated by the **FULC1** and **FULC0** bits of the **PCPR2** register (address: 1AH). For each of these bits, the default value is 00. Each time the **FULCT** register is read, the value of these bits is automatically changed in the order of 00 → 01 → 10 → 00 → 01.

FULCNTR is a load register that is used to sample (store) the value of the FIFO full counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **FIFO full counter** is stored into the **FULCNTR** register. This value indicates the number of cells that have been discarded as a result of the FIFO full since the contents of the **FIFO full counter** were last sampled. The value stored into the **FULCNTR** register is held until the **FIFO full counter** is next sampled.

Sampling the contents of the **FIFO full counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **FULC** bit of the **PCIR2** register (address: 1DH) is set to 1.

When the value of the counter is all F, the **FULC** bit of the **PCOCR2** register (address: 21H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **FIFO full counter** again starts to count up from 0.

(22) Idle cell (empty cell) count register (IDLCT)



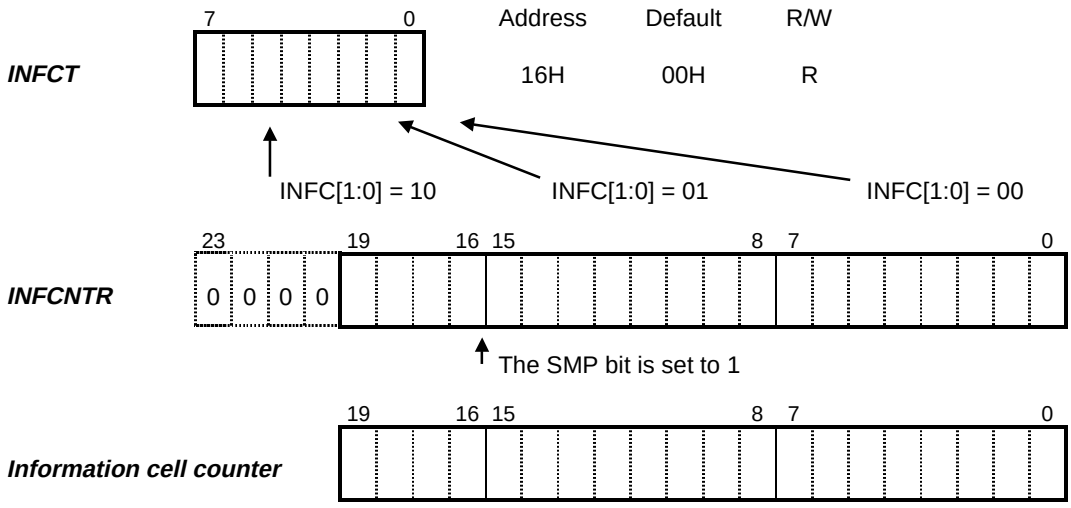
This is a window register that is used to read the contents of the 20-bit **IDLCNTR** register by reading eight bits, eight bits, and four bits, three times. First, the low-order eight bits (**IDLCNTR[7:0]**) are read, then the middle eight bits (**IDLCNTR[15:8]**), and finally the high-order four bits (**IDLCNTR[19:16]**). Which of the low-order, middle, or high-order bits is read is indicated by the **IDLC1** and **IDLC0** bits of the **PCPR2** register (address: 1AH). For each of these bits, the default value is 00. Each time the **IDLCT** register is read, the value of these bits is automatically changed in the order of 00 → 01 → 10 → 00 → 01.

IDLCNTR is a load register that is used to sample (store) the value of the idle cell counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **idle cell counter** is stored into the **IDLCNTR** register. This value indicates the number of idle cells (empty cells) that have been received since the contents of the **idle cell counter** were last sampled. The value stored into the **IDLCNTR register** is held until the **idle cell counter** is next sampled.

Sampling the contents of the **idle cell counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **IDLC** bit of the **PCIR2** register (address: 1DH) is set to 1.

When the value of the counter is all F, the **IDLC** bit of the **PCOCR2** register (address: 21H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **idle cell counter** again starts to count up from 0.

(23) Information cell count register (INFCT)



This is a window register that is used to read the contents of the 20-bit **INFCNTR** register by reading eight bits, eight bits, and four bits, three times. First, the low-order eight bits (**INFCNTR[7:0]**) are read, then the middle eight bits (**INFCNTR[15:8]**), and finally the high-order four bits (**INFCNTR[19:16]**). Which of the low-order, middle, or high-order bits is read is indicated by the **INFC1** and **INFC0** bits of the **PCPR2** register (address: 1AH). For each of these bits, the default value is 00. Each time the **INFCT** register is read, the value of these bits is automatically changed in the order of 00 → 01 → 10 → 00 → 01.

INFCNTR is a load register that is used to sample (store) the value of the information cell counter. By setting the **SMP** bit of the **PCSR** register (address: 1BH) to 1, the value of the **information cell counter** is stored into the **INFCNTR** register. This value indicates the number of valid cells that have been received (cells that have been transferred to the ATM layer device) since the contents of the **information cell counter** were last sampled. The value stored into the **INFCNTR** register is held until the **information cell counter** is next sampled.

Sampling the contents of the **information cell counter** causes the counter to be cleared to 0. The counter is also cleared to 0 when the **INFC** bit of the **PCIR2** register (address: 1DH) is set to 1.

When the value of the counter is all F, the **INFC** bit of the **PCOCR2** register (address: 21H) is set to 1 to indicate a counter overflow being detected. Also, the **PCO** bit of the **PICR** register (address: 06H) is set to 1, thus causing an interrupt. After the occurrence of an overflow, the **information cell counter** again starts to count up from 0.

(24) Performance counter point register 1 (PCPR1)

This register is used to indicate, for each of the window registers, the byte of the load register to be read next.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCPR1	B1EC	B2EC1	B2EC0	B3EC	LFBC1	LFBC0	PFBC	FJC	19H	00H	R/W

Field	Function		Default value
D7: B1EC	Used to indicate which part of B1ECNTR is to be read next.		0
	1	The high-order eight bits of B1ECNTR [15-8] are read next.	
	0	The low-order eight bits of B1ECNTR [7-0] are read next.	
D6: B2EC1 D5: B2EC0	Used to indicate which part of B2ECNTR is to be read next.		00

B2EC[1:0]	Part of B2ECNTR to be read next
00	Low-order eight bits [7-0]
01	Middle eight bits [15-8]
10	High-order four bits [19-16]

Field	Function		Default value
D4: B3EC	Used to indicate which part of B3ECNTR is to be read next.		0
	1	The high-order eight bits of B3ECNTR [15-8] are read next.	
	0	The low-order eight bits of B3ECNTR [7-0] are read next.	
D3: LFBC1 D2: LFBC0	Used to indicate which part of LFBCNTR is to be read next.		00

LFBC[1:0]	Part of LFBCNTR to be read next
00	Low-order eight bits [7-0]
01	Middle eight bits [15-8]
10	High-order four bits [19-16]

Field	Function		Default value
D1: PFBC	Used to indicate which part of PFBCNTR is to be read next.		0
	1	The high-order eight bits of PFBCNTR [15-8] are read next.	
	0	The low-order eight bits of PFBCNTR [7-0] are read next.	
D0: FJC	Used to indicate which part of FJCNTR is to be read next.		0
	1	The high-order four bits or FJCNTR [11-8] are read next.	
	0	The low-order eight bits of FJCNTR [7-0] are read next.	

(25) Performance counter point register 2 (PCPR2)

This register is used to indicate, for each of the window registers, the byte of the load register to be read next.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCPR2	HECC1	HECC0	FULC1	FULC0	IDLC1	IDLC0	INFC1	INFC0	1AH	00H	R/W

Field	Function	Default value
D7: HECC1 D6: HECC0	Used to indicate which part of HECCNTR is to be read next. HECC[1:0] / Part of HECCNTR to be read next 00 / Low-order eight bits [7-0] 01 / Middle eight bits [15-8] 10 / High-order four bits [19-16]	00
D5: FULC1 D4: FULC0	Used to indicate which part of FULCNTR is to be read next. FULC[1:0] / Part of FULCNTR to be read next 00 / Low-order eight bits [7-0] 01 / Middle eight bits [15-8] 10 / High-order four bits [19-16]	00
D3: IDLC1 D2: IDLC0	Used to indicate which part of IDLCNTR is to be read next. IDLC[1:0] / Part of IDLCNTR to be read next 00 / Low-order eight bits [7-0] 01 / Middle eight bits [15-8] 10 / High-order four bits [19-16]	00
D1: INFC1 D0: INFC0	Used to indicate which part of INFCNTR is to be read next. INFC[1:0] / Part of INFCNTR to be read next 00 / Low-order eight bits [7-0] 01 / Middle eight bits [15-8] 10 / High-order four bits [19-16]	00

(26) Performance counter sample register (PCSR)

This register is used to set the performance counter sample timing. By setting the SMP bit to 1, all of the current counter values are stored into the corresponding load registers, and the counter values are cleared to 0.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCSR	0	0	0	0	0	0	0	SMP	1BH	00H	R/W

Field	Function		Default value
D0: SMP	Used for sampling the counter value.		0
	1	The contents of all the counters are sampled (stored) into the corresponding load registers. The counters are initialized as a result.	
	0	The counters are not sampled.	

Remarks 1. The SMP bit, if set to 1, automatically returns to 0 upon the completion of sampling.

2. When this register is read, 0 is returned for the high-order seven bits. The high-order seven bits cannot be written.

(27) Performance counter initialization register 1 (PCIR1)

This register is used to initialize each performance counter. The internal counters are cleared to 0. The values saved into the corresponding load registers are not cleared, however.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCIR1	0	0	B1EC	B2EC	B3EC	LFBC	PFBC	FJC	1CH	00H	R/W

Field	Function		Default value
D5: B1EC	Used to initialize the value of the B1E counter.		0
	1	Value of the B1E counter is cleared to 0.	
	0	Value is not cleared.	
D4: B2EC	Used to initialize the value of the B2E counter.		0
	1	Value of the B2E counter is cleared to 0.	
	0	Value is not cleared.	
D3: B3EC	Used to initialize the value of the B3E counter.		0
	1	Value of the B3E counter is cleared to 0.	
	0	Value is not cleared.	
D2: LFBC	Used to initialize the value of the L-FEBE counter.		0
	1	Value of the L-FEBE counter is cleared to 0.	
	0	Value is not cleared.	
D1: PFBC	Used to initialize the value of the P-FEBE counter.		0
	1	Value of the P-FEBE counter is cleared to 0.	
	0	Value is not cleared.	
D0: FJC	Used to initialize the value of the FJ counter.		0
	1	Value of the FJ counter is cleared to 0.	
	0	Value is not cleared.	

Remarks 1. All the bits of this register are automatically set to 0 upon the completion of initialization.

2. When this register is read, 0 is returned for the high-order two bits. The high-order two bits cannot be written.

(28) Performance counter initialization register 2 (PCIR2)

This register is used to initialize each performance counter. The internal counters are cleared to 0. The values saved into the corresponding load registers are not cleared, however.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCIR2	0	0	0	0	HECC	FULC	IDLC	INFC	1DH	00H	R/W

Field	Function		Default value
D3: HECC	Used to initialize the value of the HEC counter.		0
	1	Value of the HEC counter is cleared to 0.	
	0	Value is not cleared.	
D2: FULC	Used to initialize the value of the FIFO full counter.		0
	1	Value of the FIFO full counter is cleared to 0.	
	0	Value is not cleared.	
D1: IDLC	Used to initialize the value of the idle cell counter.		0
	1	Value of the idle cell counter is cleared to 0.	
	0	Value is not cleared.	
D0: INFC	Used to initialize the value of the information cell counter.		0
	1	Value of the information cell counter is cleared to 0.	
	0	Value is not cleared.	

Remarks 1. All the bits of this register are automatically set to 0 upon the completion of initialization.

2. When this register is read, 0 is returned for the high-order four bits. The high-order four bits cannot be written.

(29) Performance counter freeze register 1 (PCFR1)

This register is used to freeze the operation of those counters that are currently not being used. This setting is effective for reducing the overall power consumption.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCFR1	0	0	B1EC	B2EC	B3EC	LFBC	PFBC	FJC	1EH	00H	R/W

Field	Function		Default value
D5: B1EC	Used to freeze the operation of the B1E counter.		0
	1	Enables operation of the B1E counter.	
	0	Disables operation of the B1E counter.	
D4: B2EC	Used to freeze the operation of the B2E counter.		0
	1	Enables operation of the B2E counter.	
	0	Disables operation of the B2E counter.	
D3: B3EC	Used to freeze the operation of the B3E counter.		0
	1	Enables operation of the B3E counter.	
	0	Disables operation of the B3E counter.	
D2: LFBC	Used to freeze the operation of the L-FEBE counter.		0
	1	Enables operation of the L-FEBE counter.	
	0	Disables operation of the L-FEBE counter.	
D1: PFBC	Used to freeze the operation of the P-FEBE counter.		0
	1	Enables operation of the P-FEBE counter.	
	0	Disables operation of the P-FEBE counter.	
D0: FJC	Used to freeze the operation of the FJ counter.		0
	1	Enables operation of the FJ counter.	
	0	Disables operation of the FJ counter.	

Remark When this register is read, 1 is returned for the high-order two bits. The high-order two bits cannot be written.

(30) Performance counter freeze register 2 (PCFR2)

This register is used to freeze the operation of those counters that are currently not being used. This setting is effective for reducing the overall power consumption.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCFR2	0	0	0	0	HECC	FULC	IDLC	INFC	1FH	00H	R/W

Field	Function		Default value
D3: HECC	Used to freeze the operation of the HEC counter.		0
	1	Enables operation of the HEC counter.	
	0	Disables operation of the HEC counter.	
D2: FULC	Used to freeze the operation of the FIFO full counter.		0
	1	Enables operation of the FIFO full counter.	
	0	Disables operation of the FIFO full counter.	
D1: IDLC	Used to freeze the operation of the idle cell counter.		0
	1	Enables operation of the idle cell counter.	
	0	Disables operation of the idle cell counter.	
D0: INFC	Used to freeze the operation of the information cell counter.		0
	1	Enables operation of the information cell counter.	
	0	Disables operation of the information cell counter.	

Remark When this register is read, 1 is returned for the high-order four bits. The high-order four bits cannot be written.

(31) Performance counter overflow cause register 1 (PCOCR1)

This register is used to indicate the cause of a performance counter overflow.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOCR1	0	0	B1EC	B2EC	B3EC	LFBC	PFBC	FJC	20H	00H	R

Field	Function		Default value
D5: B1EC	Used to indicate whether a B1E counter overflow has occurred.		0
	1	Indicates that the B1E counter has overflowed.	
	0	Indicates that the B1E counter has not overflowed.	
D4: B2EC	Used to indicate whether a B2E counter overflow has occurred.		0
	1	Indicates that the B2E counter has overflowed.	
	0	Indicates that the B2E counter has not overflowed.	
D3: B3EC	Used to indicate whether a B3E counter overflow has occurred.		0
	1	Indicates that the B3E counter has overflowed.	
	0	Indicates that the B3E counter has not overflowed.	
D2: LFBC	Used to indicate whether an L-FEBE counter overflow has occurred.		0
	1	Indicates that the L-FEBE counter has overflowed.	
	0	Indicates that the L-FEBE counter has not overflowed.	
D1: PFBC	Used to indicate whether a P-FEBE counter overflow has occurred.		0
	1	Indicates that the P-FEBE counter has overflowed.	
	0	Indicates that the P-FEBE counter has not overflowed.	
D0: FJC	Used to indicate whether an FJ counter overflow has occurred.		0
	1	Indicates that the FJ counter has overflowed.	
	0	Indicates that the FJ counter has not overflowed.	

Remarks **1**. When this register is read, 0 is returned for the high-order two bits. The high-order two bits cannot be written.

2. While any one bit of this register is set to 1, the PCO bit of the PICR register (address: 06H) is also set to 1.

3. This register is cleared upon being read.

(32) Performance counter overflow cause register 2 (PCOCR2)

This register is used to indicate the cause of a performance counter overflow.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOCR2	0	0	0	0	HECC	FULC	IDLC	INFC	21H	00H	R

Field	Function		Default value
D3: HECC	Used to indicate whether an HEC counter overflow has occurred.		0
	1	Indicates that the HEC counter has overflowed.	
	0	Indicates that the HEC counter has not overflowed.	
D2: FULC	Used to indicate whether a FIFO full counter overflow has occurred.		0
	1	Indicates that the FIFO full counter has overflowed.	
	0	Indicates that the FIFO full counter has not overflowed.	
D1: IDLC	Used to indicate whether an idle cell counter overflow has occurred.		0
	1	Indicates that the idle cell counter has overflowed.	
	0	Indicates that the idle cell counter has not overflowed.	
D0: INFC	Used to indicate whether an information cell counter overflow has occurred.		0
	1	Indicates that the information cell counter has overflowed.	
	0	Indicates that the information cell counter has not overflowed.	

Remarks **1**. When this register is read, 0 is returned for the high-order four bits. The high-order four bits cannot be written.

2. While any one bit of this register is set to 1, the PCO bit of the PICR register (address: 06H) is also set to 1.

3. This register is cleared upon being read.

(33) Performance counter overflow mask register 1 (PCOMR1)

This register is used to set masking of the cause of an overflow, as indicated by the PCOCR1 register (address: 20H). When masking is applied, the PCO bit of the PICR register (address: 06H) is not set even when the cause of the overflow is set.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOMR1	0	0	B1EC	B2EC	B3EC	LFBC	PFBC	FJC	22H	00H	R/W

Field	Function		Default value
D5: B1EC	Used to set masking of the occurrence of a B1E counter overflow.		0
	1	Does not mask the occurrence of a B1E counter overflow.	
	0	Masks the occurrence of a B1E counter overflow.	
D4: B2EC	Used to set masking of the occurrence of a B2E counter overflow.		0
	1	Does not mask the occurrence of a B2E counter overflow.	
	0	Masks the occurrence of a B2E counter overflow.	
D3: B3EC	Used to set masking of the occurrence of a B3E counter overflow.		0
	1	Does not mask the occurrence of a B3E counter overflow.	
	0	Masks the occurrence of a B3E counter overflow.	
D2: LFBC	Used to set masking of the occurrence of an L-FEBE counter overflow.		0
	1	Does not mask the occurrence of an L-FEBE counter overflow.	
	0	Masks the occurrence of an L-FEBE counter overflow.	
D1: PFBC	Used to set masking of the occurrence of a P-FEBE counter overflow.		0
	1	Does not mask the occurrence of a P-FEBE counter overflow.	
	0	Masks the occurrence of a P-FEBE counter overflow.	
D0: FJC	Used to set masking of the occurrence of an FJ counter overflow.		0
	1	Does not mask the occurrence of an FJ counter overflow.	
	0	Masks the occurrence of an FJ counter overflow.	

Remark When this register is read, 0 is returned for the high-order two bits. The high-order two bits cannot be written.

(34) Performance counter overflow mask register 2 (PCOMR2)

This register is used to set masking of the cause of an overflow, as indicated by the PCOCR1 register (address: 20H). When masking is applied, the PCO bit of the PICR register (address: 06H) is not set even when the cause of the overflow is set.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOMR2	0	0	0	0	HECC	FULC	IDLC	INFC	23H	00H	R/W

Field	Function		Default value
D3: HECC	Used to set masking of the occurrence of an HEC counter overflow.		0
	1	Does not mask the occurrence of an HEC counter overflow.	
	0	Masks the occurrence of an HEC counter overflow.	
D2: FULC	Used to set masking of the occurrence of a FIFO full counter overflow.		0
	1	Does not mask the occurrence of a FIFO full counter overflow.	
	0	Masks the occurrence of a FIFO full counter overflow.	
D1: IDLC	Used to set masking of the occurrence of an idle cell counter overflow.		0
	1	Does not mask the occurrence of an idle cell counter overflow.	
	0	Masks the occurrence of an idle cell counter overflow.	
D0: INFC	Used to set masking of the occurrence of an information cell counter overflow.		0
	1	Does not mask the occurrence of an information cell counter overflow.	
	0	Masks the occurrence of an information cell counter overflow.	

Remark When this register is read, 0 is returned for the high-order four bits. The high-order four bits cannot be written.

(35) Output alarm mask register 1 (AMR1)

This register is used to select the alarm or error (CMD, PMD, LOS, OOF, LOF, LOP, OCD, LCD) to be output from the PHYALM pin. Upon the detection of an alarm or error for which 1 has been set using this register, the level of the signal output from the PHYALM pin remains high until the cause of the alarm or error is cleared.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
AMR1	CMD	0	LOS	OOF	LOF	LOP	OCD	LCD	25H	00H	R/W

Field		Function	Default value
D7: CMD		Used to set whether notification of the setting of the ALM bit of command register 1 is to be output from the PHYALM pin.	0
	1	When the ALM bit is set, notification is posted by outputting a high-level signal from the PHYALM pin.	
	0	Notification of the ALM bit being set is not posted.	
D5: LOS		Used to set whether notification of LOS detection is to be output from the PHYALM pin.	0
	1	Upon LOS detection, the level of the signal output from PHYALM goes high.	
	0	Notification of LOS detection is not posted.	
D4: OOF		Used to set whether notification of OOF detection is to be output from the PHYALM pin.	0
	1	Upon OOF detection, the level of the signal output from PHYALM goes high.	
	0	Notification of OOF detection is not posted.	
D3: LOF		Used to set whether notification of LOF detection is to be output from the PHYALM pin.	0
	1	Upon LOF detection, the level of the signal output from PHYALM goes high.	
	0	Notification of LOF detection is not posted.	
D2: LOP		Used to set whether notification of LOP detection is to be output from the PHYALM pin.	0
	1	Upon LOP detection, the level of the signal output from PHYALM goes high.	
	0	Notification of LOP detection is not posted.	
D1: OCD		Used to set whether notification of OCD detection is to be output from the PHYALM pin.	0
	1	Upon OCD detection, the level of the signal output from PHYALM goes high.	
	0	Notification of OCD detection is not posted.	
D0: LCD		Used to set whether notification of LCD detection is to be output from the PHYALM pin.	0
	1	Upon LCD detection, the level of the signal output from PHYALM goes high.	
	0	Notification of LCD detection is not posted.	

Remark Bit D6 of this register can be written. Set this bit to 0.

(36) Alarm mask register 2 (AMR2)

This register is used to select the alarm or error (Line AIS, Path AIS, Line RDI, Path RDI) to be output from the PHYALM pin. Upon the detection of an alarm or error for which 1 has been set using this register, the level of the signal output from the PHYALM pin remains high until the cause of the alarm or error is cleared.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
AMR2	0	0	0	OOL	LAIS	PAIS	LRDI	PRDI	26H	00H	R/W

Field	Function		Default value
D4: OOL	Used to set whether notification of clock recovery PLL unlock is to be posted.		0
	1	Upon clock recovery PLL unlock, the level of the signal output from PHYALM goes high.	
	0	Notification of clock recovery PLL unlock is not posted.	
D3: LAIS	Used to set whether notification of Line AIS detection is to be output from the PHYALM pin.		0
	1	Upon Line AIS detection, the level of the signal output from PHYALM goes high.	
	0	Notification of Line AIS detection is not posted.	
D2: PAIS	Used to set whether notification of Path AIS detection is to be output from the PHYALM pin.		0
	1	Upon Path AIS detection, the level of the signal output from PHYALM goes high.	
	0	Notification of Path AIS detection is not posted.	
D1: LRDI	Used to set whether notification of Line RDI detection is to be output from the PHYALM pin.		0
	1	Upon Line RDI detection, the level of the signal output from PHYALM goes high.	
	0	Notification of Line RDI detection is not posted.	
D0: PRDI	Used to set whether notification of Path RDI detection is to be output from the PHYALM pin.		0
	1	Upon Path RDI detection, the level of the signal output from PHYALM goes high.	
	0	Notification of Path RDI detection is not posted.	

Remark When this register is read, 0 is returned for the high-order three bits. The high-order three bits cannot be written.

(37) Drop cell header pattern register (DCHPR)

This register is used to set which cells are to be discarded. The user can set the discarding of idle cells or unassigned cells. When both idle cells and unassigned cells are to be discarded, this can be set using the DCHPMR register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DCHPR	0	0	0	0	0	0	0	CLP	27H	01H	R/W

Field	Function		Default value
D0: CLP	Used for comparison with the CLP field of a receive cell.		1
	1	Idle cells are to be discarded. When all the bits of the area between the first and fourth bytes of a received cell's header, with the exception of the CLP field, are set to 0, and provided the CLP bit is set to 1, that cell is discarded.	
	0	Unassigned cells are to be discarded. When all the bits of the area between the first and fourth bytes of a received cell's header, with the exception of the CLP field, are set to 0, and provided the CLP bit is set to 0, that cell is discarded.	

The μPD98405 performs a pattern check on the header of a received cell before storing that cell into the receive FIFO. The CLP bit of this register corresponds to the CLP bit of the fourth byte of the header. When all the bits of the receive cell header area, with the exception of the CLP field, are set to 0, the CLP field of the cell is compared with the CLP bit of this register. When the values match, the cell is discarded. Because the default value of this register's CLP bit is 1, an idle cell (empty cell) having a header pattern of "00H, 00H, 00H, 01H" is discarded after initialization.

Remark The high-order seven bits of this register can be written. Set these bits to 0.

(38) Drop cell header pattern mask register (DCHPMR)

This register is used to set, when determining whether a cell is to be discarded, whether the CLP field of the receive cell header is to be compared with the CLP bit of the DCHPR register, or whether these values are to be ignored (masked).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DCHPMR	0	0	0	0	0	0	0	CLP	28H	00H	R/W

Field		Function	Default value
D0: CLP	Used to mask/unmask the CLP bit of the DCHPR register.		0
	1	Ignores the CLP field of the receive cell header and does not perform comparison with the CLP bit of the DCHPR register. The cell is discarded whenever all the bits of the area between the first and fourth bytes of the cell header are set to 0, with the exception of the CLP bit.	
	0	The CLP field of the receive cell header is checked, and compared with the CLP bit of the DCHPR register. The cell is discarded only when these values match.	

Setting the CLP bit of this register to 1 causes the μPD98405 to ignore the header of the CLP field. As a result, the μPD98405 discards both unassigned and idle cells.

Remark The high-order seven bits of this register can be written. Set these bits to 0.

(39) C11R data register (C11R)

This is an 8-bit register that is used to store the first C1 byte of the receive-side Section Overhead (SOH).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C11R									2AH	00H	R

(40) C12R data register (C12R)

This is an 8-bit register that is used to store the second C1 byte of the receive-side SOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C12R									2BH	00H	R

(41) C13R data register (C13R)

This is an 8-bit register that is used to store the third C1 byte of the receive-side SOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C13R									2CH	00H	R

(42) F1R data register (F1R)

This is an 8-bit register that is used to store the F1 byte data of the receive-side SOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F1R									2DH	00H	R

(43) K1R data register (K1R)

This is an 8-bit register that is used to store the K1 byte data of the receive-side Line Overhead (LOH).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K1R									2EH	00H	R

(44) K2R data register (K2R)

This is an 8-bit register that is used to store the K2 byte data of the receive-side LOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K2R									2FH	00H	R

(45) C2R data register (C2R)

This is an 8-bit register that is used to store the C2 byte data of the receive-side Path Overhead (POH).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C2R									30H	00H	R

(46) F2R data register (F2R)

This is an 8-bit register that is used to store the F2 byte data of the receive-side POH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F2R									31H	00H	R

(47) H4R data register (H4R)

This is an 8-bit register that is used to store the H4 byte data of the receive-side POH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H4R									32H	00H	R

(48) C11T data register (C11T)

This is an 8-bit register that is used to store the first C1 byte of the send-side SOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C11T									33H	01H	R/W

(49) C12T data register (C12T)

This is an 8-bit register that is used to store the second C1 byte of the send-side SOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C12T									34H	02H	R/W

(50) C13T data register (C13T)

This is an 8-bit register that is used to store the third C1 byte of the send-side SOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C13T									35H	03H	R/W

(51) F1T data register (F1T)

This is an 8-bit register that is used to store the F1 data of the send-side SOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F1T									36H	00H	R/W

(52) K1T data register (K1T)

This is an 8-bit register that is used to store the K1 data of the send-side LOH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K1T									37H	00H	R/W

(53) K2T data register (K2T)

This is a 5-bit register that is used to set the high-order five bits of the KA2 byte of the send-side LOH. Because the low-order three bits of the K2 byte are used for transmission of Line AIS and Line FERF, the low-order three bits set in this register are ignored.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K2T						X	X	X	38H	00H	R/W

(54) C2T data register (C2T)

This is an 8-bit register that is used to store the C2 byte data of the send-side POH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C2T									39H	13H	R/W

(55) F2T data register (F2T)

This is an 8-bit register that is used to store the F2 byte data of the send-side POH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F2T									3AH	00H	R/W

(56) H4T data register (H4T)

This is an 8-bit register that is used to store the H4 byte data of the send-side POH.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H4T									3BH	00H	R/W

CHAPTER 8 JTAG BOUNDARY SCAN

(This function is supported only when requested by the customer.)

The μPD98405 incorporates a JTAG boundary scan circuit.

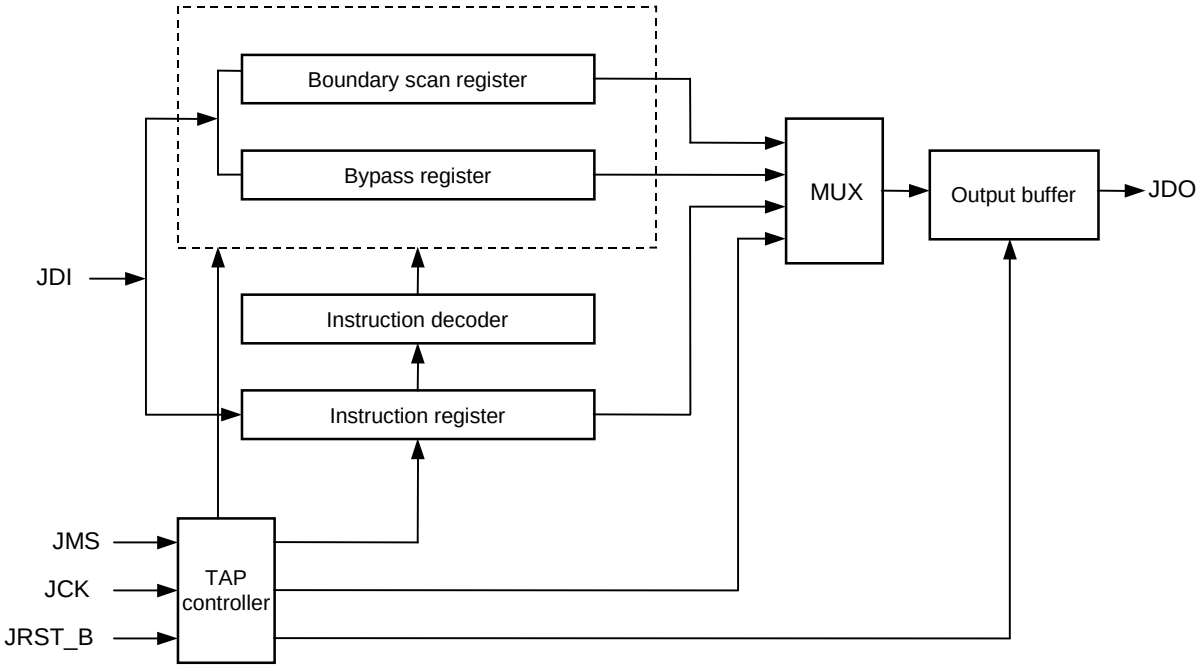
8.1 FEATURES

- Conforms to the IEEE1149.1 JTAG Boundary Scan Standard
- Three registers dedicated to boundary scan
  - Instruction register
  - Bypass register
  - Boundary scan register
- Three instructions supported
  - BYPASS instruction
  - EXTEST instruction
★ - SAMPLE/PRELOAD instruction
- Five pins dedicated to boundary scan
  - JCK (JTAG Clock)
  - JMS (JTAG Mode Select)
  - JDI (JTAG Data Input)
  - JDO (JTAG Data Output)
  - JRST_B (JTAG Reset)

8.2 INTERNAL CONFIGURATION OF BOUNDARY SCAN CIRCUIT

Figure 8-1 is a block diagram of the internal JTAG boundary scan circuit of the μPD98405.

Figure 8-1. Boundary Scan Circuit



8.2.1 Instruction Register

The instruction register is a shift register, configured using two bits, to which instructions received from the JDI pin are written. Register and instruction selection is determined based on this instruction.

8.2.2 TAP Controller

The operation state of the TAP controller is modified by latching the signal input to the JMS pin at the rising edge of the clock input to the JCK pin.

8.2.3 Bypass Register

The bypass register is a single-bit shift register, that connects the JDI and JDO pins, while the TAP controller is in the Shift-DR state. With the TAP controller in the Shift-DR state, and with the bypass register selected, data is shifted to the JDO pin at the rising edge of the clock input to the JCK pin.

When the bypass register is selected, the JTAG boundary scan circuit does not affect the operation of the μPD98405.

8.2.4 Boundary Scan Register

The boundary scan register is configured between the external pins and internal logic circuits of the μPD98405. When this register is selected, data is latched or loaded according to instructions received from the TAP controller.

While the TAP controller is in the Shift-DR state, if the boundary scan register is selected, data is output to the JDO pin, starting from the LSB, at the falling edge of the clock input to the JCK pin.

8.3 PIN FUNCTIONS

8.3.1 JCK Pin

The JCK pin is used to supply a clock signal to the JTAG boundary scan circuit (bypass register, instruction register, TAP controller). The configuration is such that this clock signal is prevented from being supplied to other internal circuits of the μPD98405.

8.3.2 JMS Pin

The input to the JMS pin is latched at the rising edge of the clock input to the JCK pin, to define the operation of the TAP controller.

8.3.3 JDI Pin

The JDI pin is used to input data to the registers of the JTAG boundary scan circuit.

8.3.4 JDO Pin

The JDO pin is used to output data from the registers of the JTAG boundary scan circuit. The output is modified at the falling edge of the clock being input to the JCK pin. Furthermore, the JDO pin can assume any of three states, as directed by the TAP controller.

8.3.5 JRST_B Pin

The JRST_B pin is used to asynchronously initialize the TAP controller. Upon the input of the reset signal, the normal operating mode of the μPD98405 is set, and the boundary register enters the non-operating state.

8.4 OPERATION

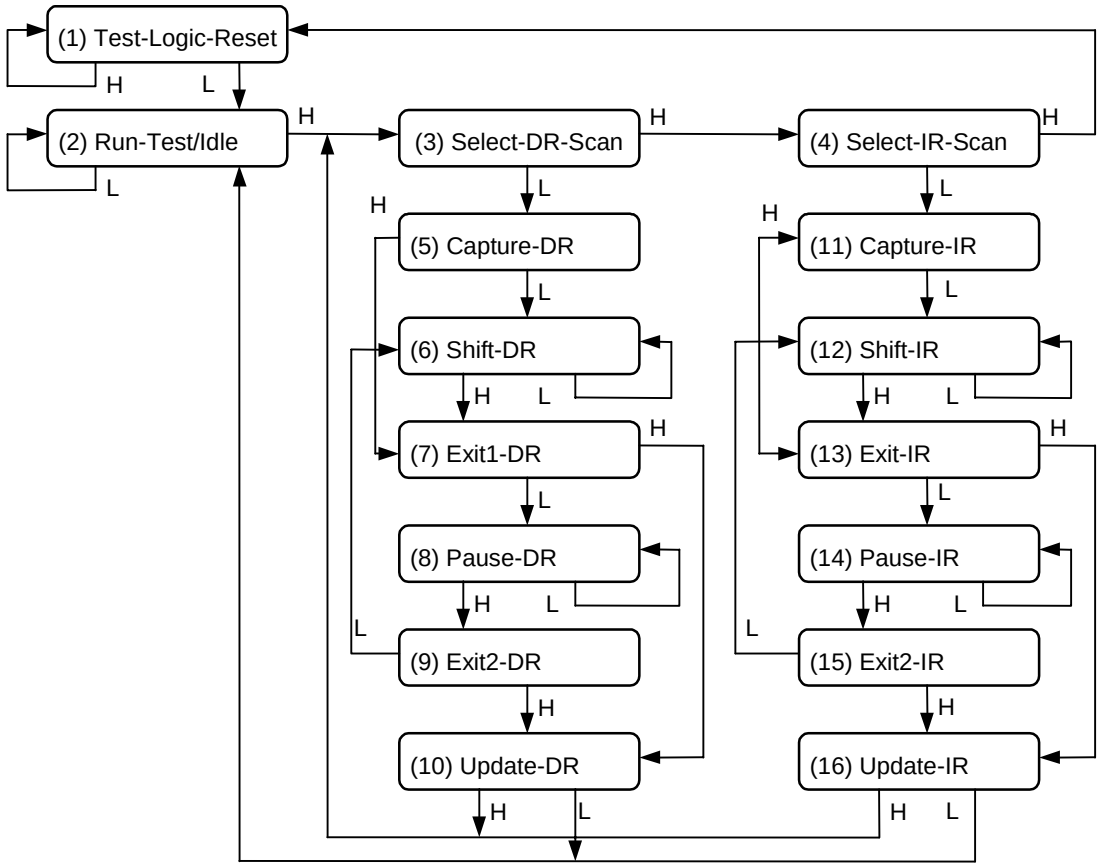
8.4.1 TAP Controller

The TAP controller is a circuit that can assume any of 16 states, according to the transition of the signals input to the JMS and JCK pins. The operation of the TAP controller conforms to IEEE standard 1149.1.

8.4.2 TAP Controller States

The states that the TAP controller can assume are shown in **Figure 8-2**. The TAP controller changes from one state to another, according to the state of the signal being input to the JMS pin at the rising edge of the clock input to the JCK pin. The operation of the instruction register, boundary scan register, and bypass register changes at either the rising or falling edge of the clock input to the JCK pin (see **Figure 8-3**).

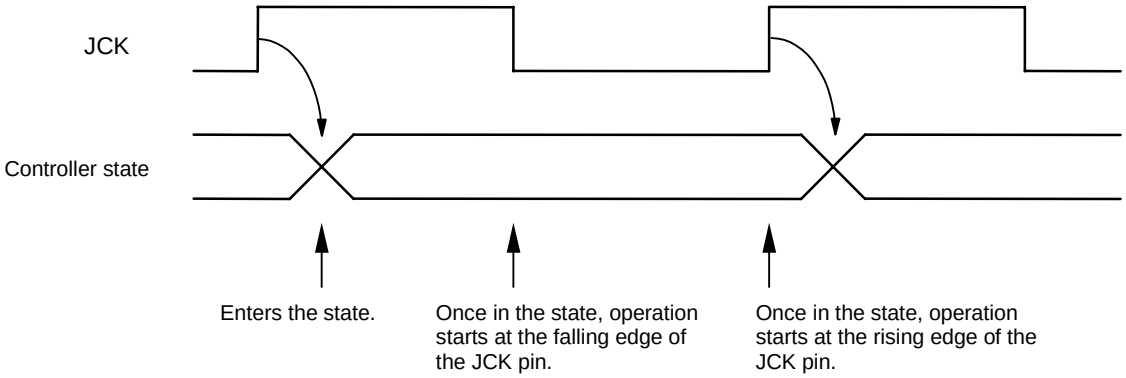
Figure 8-2. TAP Controller States



Remarks 1. In the figure, "H" and "L," next to the arrows indicating a state transition, correspond to the state of the JMS pin at the rising edge of the clock input to the JCK pin.

2. The figures in brackets correspond to the numbers of the state descriptions that follow.

Figure 8-3. Operation Timing in Controller State



(1) Test-Logic-Reset

The JTAG boundary scan circuit does not perform any processing for the μPD98405. Therefore, the circuit does not affect the system logic of the μPD98405. This is because, at initialization, the bypass instruction is stored into the instruction register and executed. Regardless of the state of the TAP controller, if the level of the signal being input to the JMS pin is held high while at least five rising edges of the signal input to the JCK pin are encountered, the Test-Logic-Reset state will be set. The TAP controller remains in this state for as long as the level of the signal being input to the JMS pin remains high.

The TAP controller must be placed in the Test-Logic-Reset state if, at the rising edge of the signal input to the JCK pin, a low-level signal is mistakenly input to the JMS pin (such as an external interface alarm). If the level of the signal input to the JMS pin is held high while the rising edge of the signal input to the JCK pin is encountered three times, the Test-Logic-Reset state is set again.

The test logic operation performed as a result of the above error does not affect the logic operations of the μPD98405.

Upon leaving the Test-Logic-Reset controller state, the TAP controller enters the Run-Test/Idle state. In this state, the current instruction is selected and set according to the operation of the bypass register, such that no processing is performed. Furthermore, the logic operation of the JTAG boundary scan circuit is deactivated in the Select-DR-Scan state and Select-IR-Scan state.

(2) Run-Test/Idle

The TAP controller assumes this state while scan processing (Select-DR-Scan state and Select-IR-Scan state) is not being performed. Once the TAP controller has entered Run-Test/Idle state, it remains in this state for as long as the level of the signal being input to the JMS pin remains low. Upon encountering a rising edge of the signal being input to the JCK pin, provided the level of the signal being input to the JMS pin is high, the TAP controller enters the Select-DR-Scan state.

All of the test data registers selected with the current instruction (boundary register, bypass register) maintain their previous statuses (idle). While the TAP controller is in this state, instruction conversion is not performed.

(3) Select-DR-Scan

Select-DR-Scan is a state that arises temporarily during boundary scan. The system maintains the previous states of the boundary scan register and bypass register, selected with the current instruction.

In this state, at the rising edge of the signal being input to the JCK pin, if the level of the JMS signal is held low, the TAP controller enters the Capture-DR state. Also, the scan sequence is started for the selected registers.

If, at the rising edge of the signal being input to the JCK pin, the level of the JMS signal is held high, the TAP controller enters the Select-IR-Scan state. While the TAP controller is in this state, instruction conversion is not performed.

(4) Select-IR-Scan

Select-IR-Scan is a state that arises temporarily during boundary scan. The system maintains the previous states of the boundary scan register and bypass register, selected with the current instruction.

In this state, at the rising edge of the signal being input to the JCK pin, if the level of the JMS signal is held low, the TAP controller enters the Capture-IR state. Also, the scan sequence is started for the selected registers.

At the rising edge of the signal being input to the JCK pin, if the level of the JMS signal is held high, the TAP controller returns to the Test-Logic-Reset state. While the TAP controller is in this state, instruction conversion is not performed.

(5) Capture-DR

While the TAP controller is in this state, data is parallel-loaded into the boundary scan register, selected with the current instruction, at the rising edge of the signal being input to the JCK pin (in this case, data is simultaneously loaded into the boundary scan registers from the input pins of each device). While the TAP controller is in this state, instruction conversion is not performed.

Whilst in the Capture-DR state, at the rising edge of the signal being input to the JCK pin, the state of the TAP controller changes as follows:

- When the level of the signal being input to the JMS pin is held high: The TAP controller enters the Exit1-DR state.
- When the level of the signal being input to the JMS pin is held low: The TAP controller enters the Shift-DR state.

(6) Shift-DR

While the TAP controller is in this state, JDI and JDO are connected according to the current instruction (in either the boundary scan register or the bypass register). The shift data is shifted, one level at a time, to the serial output at each rising edge of the signal input to the JCK pin.

When the boundary scan register or bypass register selected with the current instruction is not positioned in the serial path (when not in the Shift-DR state), the previous state is held. While the TAP controller is in this state, instruction conversion is not performed.

While the TAP controller is in this state, at a rising edge of the signal input to the JCK pin, the state of the TAP controller changes as follows:

- When the level of the signal being input to the JMS pin is held high: The TAP controller enters the Exit1-DR state.
- When the level of the signal being input to the JMS pin is held low: The TAP controller enters the Shift-DR state.

(7) Exit1-DR

Exit1-DR is a state that the controller enters temporarily. In this state, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held high, the TAP controller enters the Update-DR state. In this way, scan processing is terminated.

On the contrary, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held low, the TAP controller enters the Pause-DR state.

Regardless of whether the bypass register or boundary scan register is selected with the current instruction, the previous state is maintained. While the TAP controller is in this state, instruction conversion is not performed.

(8) Pause-DR

While the TAP controller is in the Pause-DR state, data shift between JDO and JDI, connected to either the bypass register or boundary scan register, is temporarily halted. These registers, selected with the current instruction, maintain their previous states.

While the level of the signal being input to the JMS pin is held low, the TAP controller remains in this state. At the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held high, the TAP controller enters the Exit2-DR state. While the TAP controller is in this state, instruction conversion is not performed.

(9) Exit2-DR

Exit2-DR is a state that the controller enters temporarily. In this state, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held high, the TAP controller enters the Update-DR state. In this way, scan processing is terminated.

On the contrary, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held low, the TAP controller enters the Shift-DR state.

Both the bypass register and boundary scan register, selected with the current instruction, maintain their previous states. While the TAP controller is in this state, instruction conversion is not performed.

(10) Update-DR

The boundary scan register is provided with a parallel output latch to prevent parallel output conversion (in that period shifted into the continuous shift register path) by some instructions (such as EXTEST).

While the TAP controller is in the Update-DR state, at the falling edge of the signal being input to the JCK pin, data from the shift register path is latched to the parallel output of this register.

That data that is held to latch the parallel output is modified while the controller is in this state (conversion is not performed while the controller is in any other state).

For the boundary scan register selected with the current instruction, all the shift registers maintain the previous state.

While the TAP controller is in this state, instruction conversion is not performed.

While the TAP controller is in this state, at the rising edge of the signal being input to the JCK pin, provided the level of the JMS signal is held high, the TAP controller enters the Select-DR-Scan state.

On the contrary, at the rising edge of the signal being input to the JCK pin, if the level of the JMS signal is held low, the TAP controller enters the Run-Test/Idle state.

(11) Capture-IR

While the TAP controller is in the Capture-IR state, at the rising edge of the signal being input to the JCK pin, the shift register loads a fixed logical value pattern (binary 01) into the instruction register.

Both the bypass register and boundary scan register, selected with the current instruction, maintain their previous states.

While the TAP controller is in this state, instruction conversion is not performed.

While the TAP controller is in the Capture-IR state, at the rising edge of the signal being input to the JCK pin, if the level of the JMS signal is held high, the TAP controller enters the Exit1-IR state.

Also, at the rising edge of the signal being input to the JCK pin, if the level of the JMS signal is held low, the TAP controller enters the Shift-IR state.

(12) Shift-IR

While the TAP controller is in this state, JDI and JDO are connected via the shift register within the instruction register. The shift data is shifted, one level at a time, to the serial output at each rising edge of the signal being input to the JCK pin.

The boundary scan register and bypass register selected with the current instruction maintain their previous states.

While the TAP controller is in this state, instruction conversion is not performed.

While the TAP controller is in this state, at a rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held high, the TAP controller enters the Exit1-IR state. If the level of the signal being input to the JMS pin is held low, the TAP controller remains in the Shift-IR state.

(13) Exit1-IR

Exit1-IR is a state that the controller enters temporarily. In this state, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held high, the TAP controller enters the Update-IR state. In this way, scan processing is terminated.

On the contrary, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held low, the TAP controller enters the Pause-IR state.

Both the bypass register and boundary scan register, selected with the current instruction, maintain their previous states.

While the TAP controller is in this state, instruction conversion is not performed.

(14) Pause-IR

While the TAP controller is in the Pause-IR state, shift processing by the instruction register is temporarily halted. The bypass register and boundary scan register, selected with the current instruction, maintain their previous states.

While the TAP controller is in this state, instruction conversion is not performed. Also, the instruction register maintains its current state.

While the level of the signal being input to the JMS pin is held low, the TAP controller remains in this state.

At the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held high, the TAP controller enters the Exit2-IR state.

(15) Exit2-IR

Exit2-IR is a state that the controller enters temporarily. In this state, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held high, the TAP controller enters the Update-IR state. In this way, scan processing is terminated.

On the contrary, at the rising edge of the signal being input to the JCK pin, if the level of the signal being input to the JMS pin is held low, the TAP controller enters the Shift-IR state.

Both the bypass register and boundary scan register, selected with the current instruction, maintain their previous states.

While the TAP controller is in this state, or while the instruction register remains in the same state, instruction conversion is not performed.

(16) Update-IR

While the TAP controller is in the Update-IR state, at the falling edge of the signal being input to the JCK pin, the instruction shifted into the instruction register is latched from the shift register path to the parallel output of this register. A new instruction, once latched, becomes the current instruction.

Both the bypass register and boundary scan register, selected with the current instruction, maintain their previous states.

While the TAP controller is in this state, at the rising edge of the signal being input to the JCK pin, provided the level of the JMS signal is held high, the TAP controller enters the Select-DR-Scan state.

On the contrary, at the rising edge of the signal being input to the JCK pin, if the level of the JMS signal is held low, the TAP controller enters the Run-Test/Idle state.

In both the Pause-DR state explained in (8) and the Pause-IR state explained in (14), data shift in the bypass register, boundary scan register, and instruction register is temporarily halted.

8.5 TAP CONTROLLER OPERATION

The operation of the TAP controller is explained below.

TAP controller state transition is performed upon the occurrence of either of the following:

(1) At the rising edge of the signal being input to the JCK pin

(2) Upon the input of a signal to the JRST_B pin.

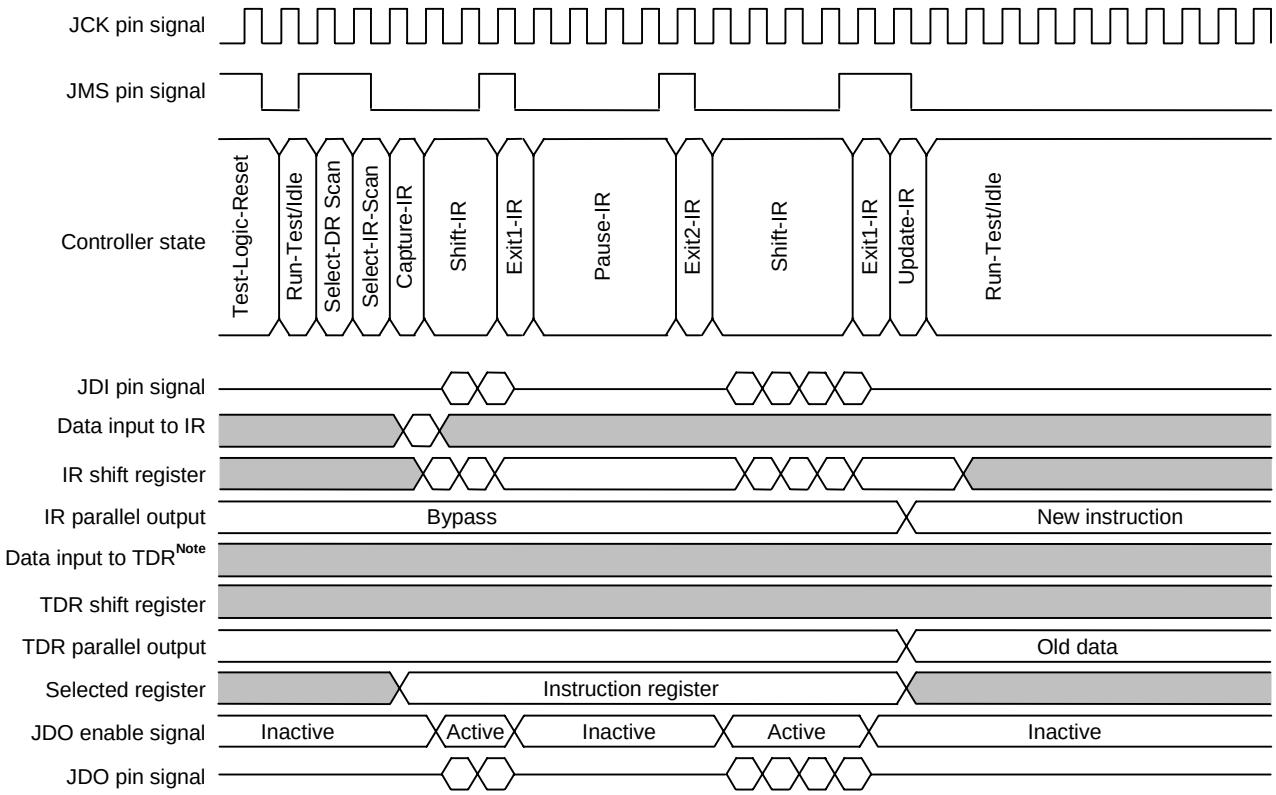
The TAP controller generates signals to control the operation of the bypass register, boundary scan register, and instruction register, as defined in the standard (see **Figures 8-4** and **8-5**).

The peripheral circuit that selects the output buffer of the JDO pin, and the register that performs output to the JDO pin, is controlled as shown in **Table 8-1**. After the TAP controller enters the state defined in Table 8-1, the JDO pin signal changes at the falling edge of the signal being input to the JCK pin.

Table 8-1. Operation in Each Controller State

Controller state	Register selected to drive JDO pin	JDO pin driver
Test-Logic-Reset	Undefined	High impedance
Run-Test/Idle		
Select-DR-Scan		
Select-IR-Scan		
Capture-IR		
Shift-IR	Instruction register	Active
Exit1-IR	Undefined	High impedance
Pause-IR		
Exit2-IR		
Update-IR		
Capture-DR		
Shift-DR	Data register (boundary scan register, bypass register)	Active
Exit1-DR	Undefined	High impedance
Pause-DR		
Exit2-DR		
Update-DR		

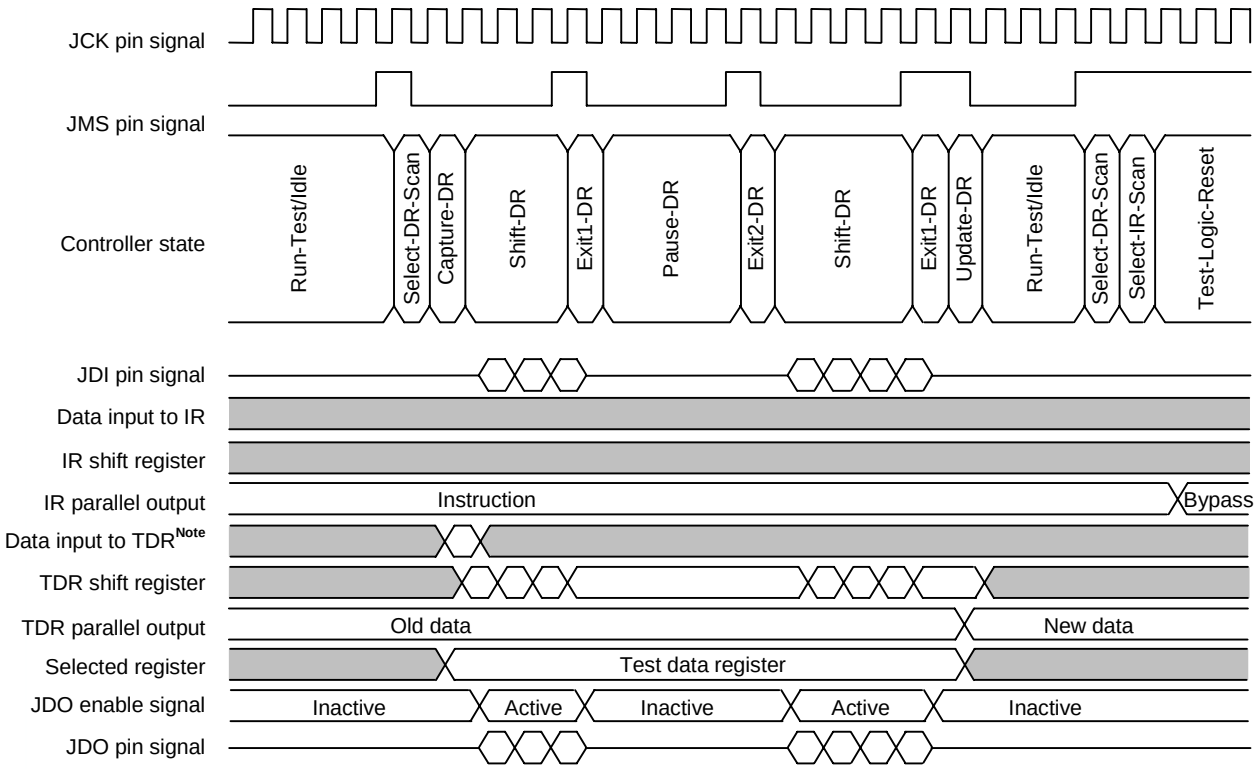
Figure 8-4. Test Logic Operation (Instruction Scan)



Note TDR (Test Data Register): Boundary scan register or bypass register

Remark : Don't care or undefined

Figure 8-5. Test Logic Operation (Data Scan)



Note TDR (Test Data Register): Boundary scan register or bypass register

Remark : Don't care or undefined

8.6 TAP CONTROLLER INITIALIZATION

TAP controller initialization is explained below.

(1) The TAP controller is not reset upon the occurrence of system input operation such as a system reset.
(2) If the level of the signal being input to the JMS pin is held high while at least five rising edges of the signal being input to the JCK pin are encountered, the TAP controller enters the Test-Logic-Reset state.
(3) Upon the occurrence of a JRST_B input, the TAP controller asynchronously enters the Test-Logic-Reset state.

★ The width of the low level input to the JRST_B pin should be at least one clock cycle of the SCLK input.

8.7 INSTRUCTION REGISTER

The use of this register is as defined below (see **Section 8.2**).

(1) To enable their conversion, the instructions that are shift-input into the instruction register are latched only while the TAP controller is in the Update-IR state or Test-Logic-Reset state.
(2) Between the serial input and serial output of the instruction register, data inversion is not performed.
(3) While the TAP controller is in the Capture-IR state, fixed binary "01" pattern data (where the LSB (Least Significant Bit) is 1) is loaded into this register cell.
(4) While the TAP controller is in the Test-Logic-Reset state, fixed binary "01" pattern data (where the LSB (Least Significant Bit) is 1) is set in this register.
(5) While the value in this register is being read, the data is output from the JDO pin, in order from the LSB to the MSB, every time a falling edge of the signal being input to the JCK pin is detected.

According to the data set in the instruction register, the JTAG boundary scan circuit of the μPD98405 can support only one of the three instructions listed below.

- BYPASS instruction
- EXTEST instruction
- ★ SAMPLE/PRELOAD instruction

Instruction register		Supported instruction
D1	D0	
0	0	EXTEST instruction
0	1	SAMPLE/PRELOAD instruction
1	0	Not used (BYPASS instruction)
1	1	BYPASS instruction

★

8.7.1 BYPASS Instruction

This instruction is specified by setting "11" or "10" as the instruction data. While the TAP controller is in the Shift-DR state, this instruction is used to enable selection of the bypass register (positioned between the JDI and JDO pins and used for serial access) only.

When this instruction is selected, the JTAG boundary scan circuit does not affect the operation of the μPD98405.

This instruction is selected while the TAP controller is in the Test-Logic-Reset state.

8.7.2 EXTEST Instruction

This instruction is specified by setting "00" as the instruction data. While the TAP controller is in the Shift-DR state, this instruction is used to enable selection of the boundary scan register for serial access between the JDI and JDO pins.

- When this instruction is selected:

  Based on the data shifted into the boundary scan register, the states of all the signals driven from the system output pins are all clearly defined. While the TAP controller is in the Update-DR state, conversion is performed only at the falling edge of the signal being input to the JCK pin.

  While the TAP controller is in the Capture-DR state, the states of all the signals input from the system input pins are loaded into the boundary scan register at a rising edge of the signal being input to the JCK pin.

★ 8.7.3 SAMPLE/PRELOAD Instruction

This instruction is specified by setting "01" as the instruction data. This instruction executes the SAMPLE function and PRELOAD function in one instruction.

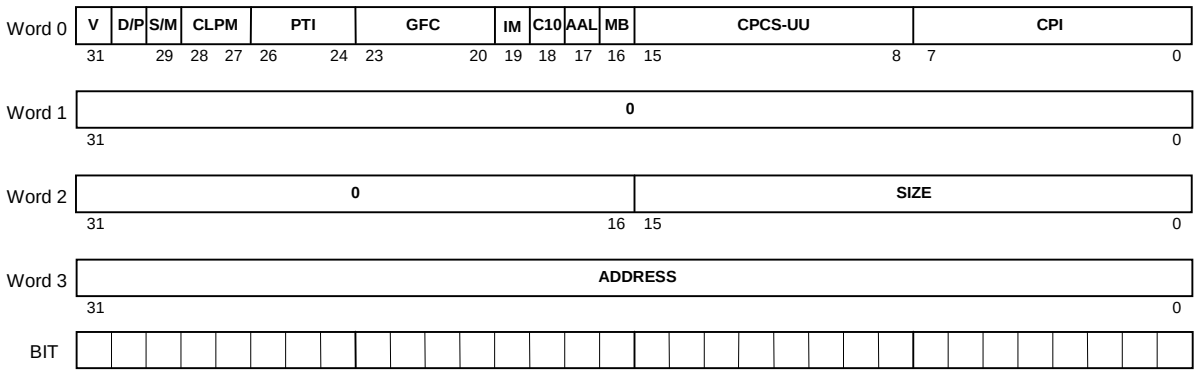
8.7.4 Boundary Scan Data Bit Setting

In response to customer requests, NEC has made available the BSDL (Boundary Scan Description Language) reference file for the μPD98405. To obtain this file, contact the NEC Semiconductor Technical Hotline.

[MEMO]

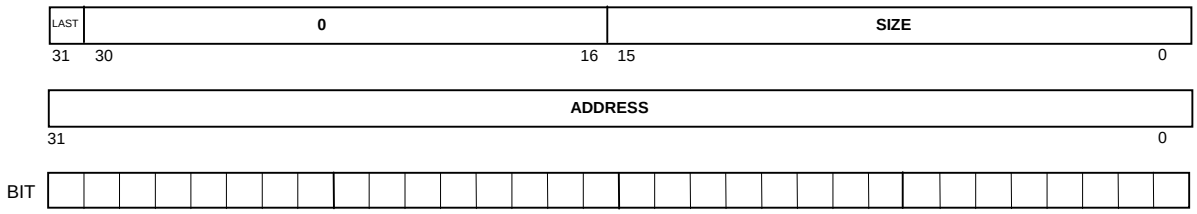
APPENDIX DATA FORMATS

(1) Transmit packet descriptor



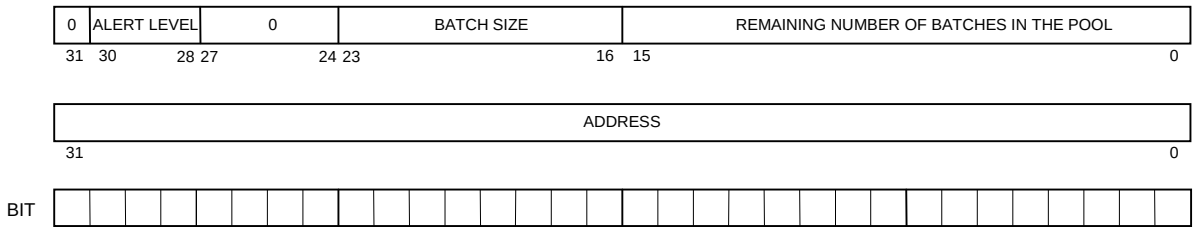
Field Name	Explanation
V D/P S/M	<table><tr><th>V</th><th>D/P</th><th>S/M</th><th>Function</th></tr><tr><td>0</td><td>-</td><td>-</td><td>Vacant packet descriptor</td></tr><tr><td>1</td><td>0</td><td>-</td><td>Link pointer</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Multi-buffer mode</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Single buffer mode</td></tr></table>
CLPM	<table><tr><td>00</td><td>Set CLP of all cells to 0</td></tr><tr><td>11</td><td>Set CLP of all cells to 1</td></tr><tr><td>01</td><td>Set CLP of last cell to 0, CLP of all other cells to 1</td></tr><tr><td>10</td><td>Setting prohibited</td></tr></table>
PTI	000 or 010: User data, 100 or 101: OAM F5 cell transmission
GFC	Arbitrary pattern
IM	1: Transmission indication mask, 0: Unmask
C10	1: CRC-10 operation enable, 0: CRC-10 operation disable
AAL	1: AAL-5 transmission, 0: Raw cell transmission
MB	1: Mailbox #3, 0: Mailbox #2
CPCS-UU CPI	Arbitrary pattern
SIZE	Packet size in byte units
ADDRESS	Data buffer/packet directory/address of next packet descriptor

(2) Buffer descriptor



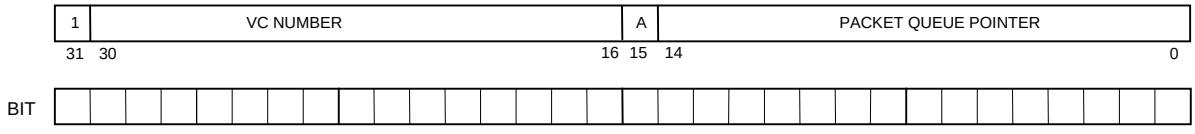
Field Name	Explanation
LAST	1: Last buffer descriptor, 0: Other than last buffer descriptor
SIZE	Packet size in byte units
ADDRESS	Address of data buffer

(3) Receive pool descriptor



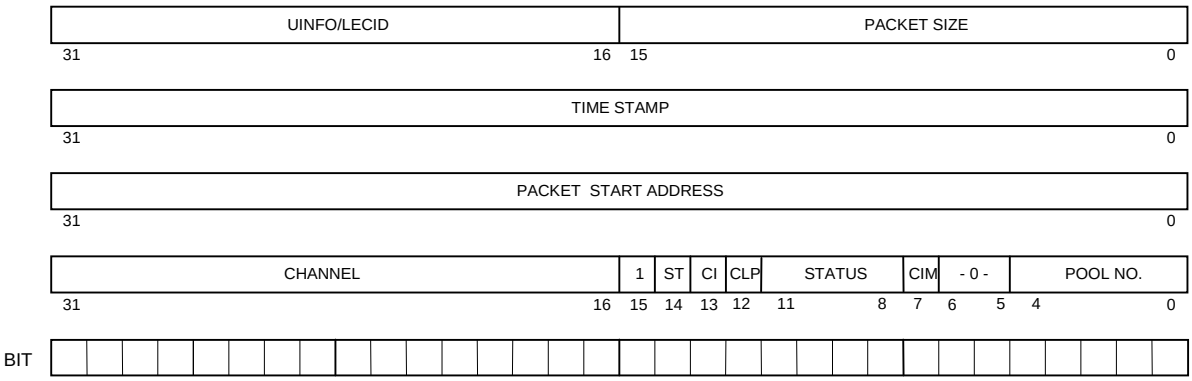
Field Name	Explanation
ALERT LEVEL	Remaining batch alert. n x 4
BATCH SIZE	Number of free buffers contained in one batch
REMAINING NO. OF BATCHES	Number of batches in the pool
ADDRESS	Batch start address

(4) Transmit indication



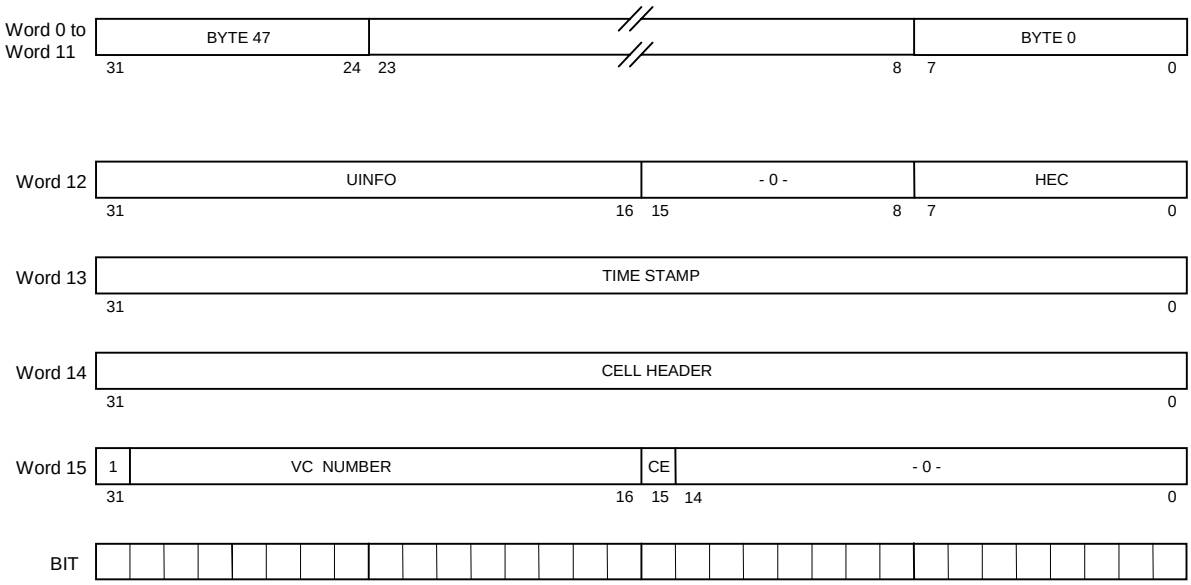
Field Name	Explanation
VC NUMBER	VC NUMBER used by this VC
A	0: Next packet descriptor is a vacant packet descriptor. 1: Next packet descriptor is a valid packet descriptor.
PACKET QUEUE POINTER	Low-order 15 bits of the start address of the next packet descriptor.

(5) Receive indication



Field Name	Explanation
UINFO/LECID	UINFO value in receive VC table, or receive LECID
PACKET SIZE	Receive packet size
TIME STAMP	TSR register value when packet is received
PACKET START ADDRESS	Start address of first batch
CHANNEL	Whether notification of the VPI/VCI reduction value for the VC that has received this packet, or the VC NUMBER, is posted according to the CIM.
ST	1: Value of STATUS field is other than 0, 0: Value of STATUS field is 0
CI	1: Congestion cell received, 0: No congestion cells
CLP	1: At least one cell for which CLP = 1 has been received, 0: CLP = 0 for all cells
STATUS	0000 Normal 0001 Free buffer underflow 0010 Receive FIFO overrun 0011 MAX. NO. OF SEGMENTS error 0100 CRC-32 error 0101 User abort 0110 Length error 0111 T1 error 1000 Deactivate_Channel command execution 1111 Early receive interrupt
CIM	1: CHANNEL field contains VPI/VCI reduction value. 0: CHANNEL field contains VC NUMBER.
POOL NO.	Number of stored pool

(6) Raw cell data



Field Name	Explanation
BYTE0-BYTE47	Segment data
UINFO	Arbitrary pattern set in VC table
HEC	Fifth byte of cell header
TIME STAMP	TSR register value at reception
CELL HEADER	First to fourth bytes of cell header
VC NUMBER	VC NUMBER used by this VC
CE	1: CRC-10 error occurrence, 0: No CRC-10 error

(7) Transmit VC table

Word 0

31	30	29	28	27	26	24	23	20	19	18	17	16	15	8	7	0
V	D/P	S/M	CLPM		PTI		GFC		IM	C10	AAL	MB	CPCS-UU			CPI

Word 1

31	30	29	28	27	24	23	0
L	Reserved		ABR	SHAPER NO.		VPI/VCI	

Word 2

31	0
Reserved	

Word 3

31	0
Reserved	

Word 4

31	0
Reserved	

Word 5

31	0
Reserved	

Word 6

31	2	1	0
TRANSMIT QUEUE READ POINTER			0

Word 7

31	15	14	0
Reserved		Rx VC TABLE POINTER	

Word 8

31	16	15	0
MCR		PCR	

Word 9

31	16	15	0
ICR		ACR	

Word 10

31	30	29	27	26	24	23	0
Reserved		ADTF0		CDF0		Reserved	

Word 11

31	0
Reserved	

Word 12

31	0
Reserved	

Word 13

31	29	28	17	16	15	14	13	12	0
MBL		Reserved		CD	Reserved		LIE	Reserved	

Word 14

31	16	15	0
Reserved		LOCAL LECID	

Word 15

31	30	16	15	14	0
A	BACKWARD POINTER		LST	FORWARD POINTER	

Field Name	Explanation
Word 0	Initially set to 0
L	Initially set to 1
ABR	1: ABR service, 0: CBR, VBR, and UBR services
SHAPER NO.	Shaper number
VPI/VCI	VPI/VCI field of cell header
TRANSMIT QUEUE READ POINTER	Pointer to head address of packet descriptor
Rx VC TABLE POINTER**Note**	Pointer to address of receive VC table
MCR**Note**	Minimum cell rate
PCR**Note**	Peak cell rate
ICR**Note**	Initial cell rate
ACR**Note**	Allowed cell rate
ADTF0**Note**	ACR decrease time factor ADTF (milliseconds) = $10*2^{ADTF0}$
CDF0**Note**	Cut-off decrease factor CDF0: 0 to 6 CDF = $1/2^{CDFO}$ CDF0: 7 CDF = 0
MBL	Maximum burst size for multi-cell transmission
CD	Close channel disable 1: Close_Channel command not accepted 0: Close_Channel command accepted
LIE	Transmit LECID insert enable 1: Enable, 2: Disable
LOCAL LECIED	Transmit LECID
A	Active bit 1: Active status, 0: Idle status
BACKWARD POIINTER	Pointer to previous VC in the shaper link list
LST	Last VC to be linked in the shaper link list
FORWARD POINTER	Pointer to the next VC in the shaper link list
Reserved	Initially set to 0

Note Set only for a VC used with the ABR service.

(8) Receive VC table

Word 0

Reserved	MB	POOL NO.	UINFO/ LECID
31 – 22	21	20 – 16	15 – 0

Word 1

Reserved	EIS	MAX. NUMBER OF SEGMENTS
31 – 14	13 – 11	10 – 0

Word 2

Reserved
31 – 0

Word 3

Reserved
31 – 0

Word 4

Reserved
31 – 0

Word 5

Reserved
31 – 0

Word 6

Reserved
31 – 0

Word 7

Reserved	T1D	RE	Tx VC TABLE POINTER
31 – 17	16	15	14 – 0

Word 8

Reserved
31 – 0

Word 9

Reserved
31 – 0

Word 10

Reserved
31 – 0

Word 11

Reserved
31 – 0

Word 12

0	ECI	ENI	ER enb	EER
31 – 19	18	17	16	15 – 0

Word 13

Reserved	CIM	Reserved	RIF0	RDF0
31 – 16	15	14 – 8	7 – 4	3 – 0

Word 14

Reserved

Reserved	ABR	MBL	MAC	A34	OD	A/R		RLI	DAF	LFE	LOCAL LECID
31 – 29	28	27 – 25	24	23	22	21	20	19	18	17	16 – 15	0

Word 15

0	BACKWARD POINTER	LST	FORWARD POINTER
31 – 30		16	15 – 14 – 0

Field Name	Explanation
MB	Mailbox No. 1: Mailbox #1, 0: Mailbox #0
POOL NO.	Pool No.
UINFO/LECID	User information/Receive LECID
EIS	Early interrupt size
MAX. NO. OF SEGMENTS	Max. no. of segments in 1 packet (Segment: 48-byte payload of receive cell)
T1D	T1 timer disable 1: Disable, 0: Enable
RE[Note]	Rate calculation based on RM cell reception, turn-around enable 1: Enable, 0: Disable
Tx VC TABLE POINTER[Note]	Pointer to transmit table address
ECI[Note]	Flag for setting CI bit of turn-around BRM cell
ENI[Note]	Flag for setting NI bit of turn-around BRM cell
ER enb[Note]	Flag for setting ER field of turn-around BRM cell
EER[Note]	Explicit rate When ER enb=1, set in the ER field of the turn-around BRM cell
CIM	Mode setting to determine whether to VPI/VCI value or VC NUMBER in the receive indication. 1: VPI/VCI value (reduced to 16 bits according to VRR register) 0: VC NUMBER
RIF0[Note]	Rate increase factor RIF = $1/2^{RIF0}$
RDF0[Note]	Rate decrease factor RDF = $1/2^{RDF0}$
ABR	1: ABR service, 0: CBR, VBR, UBR services
MBL	Maximum burst size in multi-cell transmission
MAC	Offset from packet initial value during MAC address filtering 00: 2 bytes (Ethernet LAN emulation data frame) 01: 4 bytes (Token-Ring LAN emulation data frame) 10: 6 bytes 11: 10 bytes
A34	AAL-3/4 packet receive assist function enable 1: Enable, 0: Disable
OD	OAM receive/discard selection 1: Discard OAM F5 cell, 0: Receive OAM F5 cell
A/R	AAL-5 receive/Raw cell receive 1: AAL-5 packet receive, 0: Raw cell receive
RLI	Notification of receive LECID to indication 1: Notification of receive LECID posted to indication 0: Notification of receive LECID not posted to indication

Field Name	Explanation
DAF	Destination address filtering enable 1: Enable, 0: Disable
LFE	Receive LECID filtering enable 1: Enable, 0: Disable
LOCAL LECID	LECID used for receive LECID filtering
BACKWARD POINTER	VC NUMBER of VC linked prior to current VC in T1 list
LST	Last VC to be linked in T1 list
FORWARD POINTER	VC NUMBER of VC linked subsequent to current VC in T1 list
Reserved	Initially set to 0

Note Set only for a VC used with the ABR service.

[MEMO]

Phase-out/Discontinued

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