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User's Manual

RENESAS

μPD612x Series

4-bit Single-Chip Microcontroller

For Remote Control Transmission

μPD6124A
μPD6125A
μPD6126A
μPD6600A
μPD61P24

Document No. U12678EJ3V0UM00 (3rd edition)
(O.D.No. IEU-800)
Date Published August 1997 N

NEC

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Date Published August 1997 N

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
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Major Revisions in This Edition

Page	Description
Entire	Deletion of Target Devices: μPD6123, 6124, 6127, 6129
Entire	Addition of Target Devices: μPD6124A, 6600A, 61P24
p. 2	Add Section **1.2 Ordering Information.**
p. 12	Add "Caution" in Section **3.4 Data Memory (RAM).**
 p. 13 p. 15, 16 p. 17, 18	Add the description of conditions after Reset in the following sections: **3.5 Data Pointer (R_0), 3.6 Accumulator (A), 3.8 Flags** **3.11 Timer, 3.13 S-IN Pin (D_0 bit of P_1)** **3.14 $K_{I/O}$ Pin (P_0), 3.16 I/O Pin (P_3, P_4)**
p. 14	Add **Table 3-1 Relationship between Port Register and Each Pin.**
p. 15	Add the explanation of Section **3.11 Timer.**
p. 16	Add **3.12 S-OUT Pin.**
p. 17, 18	Correct **Figure 3-8. S-IN Pin Configuration** and **Figure 3-10. K_I Pin Configuration.**
p. 21	Add Section **3.18 Low Voltage Detection (Reset) Circuit.**
p. 37, 38, 48	Add "Cautions" to the following instructions in Section **7.3 Branch Instructions.** (The same Cautions are added in the Branch Instruction of Section **7.8 Mnemonic ↔ Machine Language Correspondence Table.**) • JMP_0 Rr • JC Rr • JNC Rr • JF Rr • JNF Rr
p. 53	Add Section **8.2 μPD61P24.**
p. 67	Add **APPENDIX A. LIST OF μPD612x SERIES PRODUCTS".**
p. 69	Add **APPENDIX B. DEVELOPMENT TOOLS.**

The mark ★ shows major revised points.

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CHAPTER 1 OUTLINE

The μPD612x Series is an infrared remote control transmission processor which integrates a 4-bit ALU, program memory (ROM), data memory (RAM), infrared remote control transmission output timer, key scan I/O, and key input pin on a single chip.

★ Products in the μPD612x Series are the μPD6124A, 6125A, 6126A, 6600A and 61P24.

The command set is composed of an extremely simple 19 commands. These commands include the accumulator commands which are mainly composed of logical operations, input and output commands for each port, data transfer commands, branch commands, etc.

The μPD612x Series has a wide power supply voltage range, V_{DD} = 2.0 to 6.0 V, and has a CMOS structure, so low power consumption is realized.

In the μPD612x Series, a f_{osc} = 400 to 500 kHz ceramic oscillator is used as the operating clock and the operating clock can be stopped by executing the HALT command, which stops oscillation.

This series includes an exclusive output port for infrared remote control transmission and $f_{osc}/12$ (38 kHz) or $f_{osc}/8$ (57 kHz) carrier modulation outputs (when the f_{osc} = 455 kHz) can be program selected.

1.1 Features

- O Programmable infrared remote control transmitter
- O 19 instructions
- O Instruction execution time
  17.6 μs (when a 455 kHz ceramic oscillator is used)
- ★ O Program Memory (ROM) Capacity
  - μPD6600A : 512 × 10-bit (Mask ROM)
  - μPD6124A, 6125A, 6126A : 1002 × 10-bit (Mask ROM)
  - μPD61P24 : 1002 × 10-bit (One-time PROM)
- O Data Memory (RAM) Capacity : 32 × 5-bit
- O 9-bit programmable timer : 1 channel
- ★ O Input/Output Pins ($K_{I/O}$) : 8
- ★ O Input/Output Pins (I/O)
  - μPD6124A, 6600A, 61P24 : none
  - μPD6125A : 4
  - μPD6126A : 8
- O Input Pins (K_I) : 4
- ★ O Serial Input Pins (S-IN) : 1
- ★ O Transmitting Display Pin (S-OUT) : 1
- ★ O Transmission Carrier Frequency (REM)
  $f_{osc}/8$ or $f_{osc}/12$
- O Standby Operation (HALT/STOP Mode)
- O Low Power Consumption

★ ○ Low Voltage Operation

- μPD6124A, 61P24 : V_{DD} = 2.2 to 5.5 V
- μPD6125A, 6126A : V_{DD} = 2.0 to 6.0 V
- μPD6600A : V_{DD} = 2.2 to 3.6 V

★ 1.2 Ordering Information

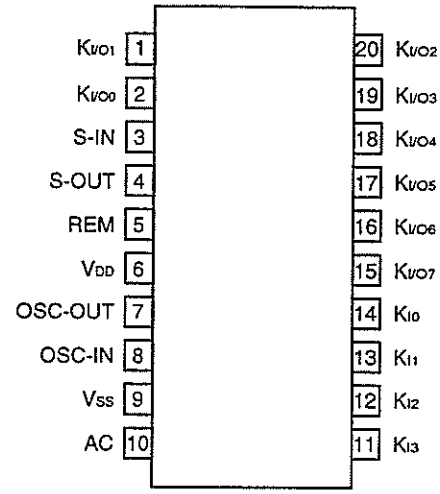
Ordering Information	Package
μPD6124ACS-xxx	20-pin Plastic Shrink DIP (300 mil)
μPD6124AGS-xxx	20-pin Plastic SOP (300 mil)
μPD6125ACA-xxx	24-pin Plastic Shrink DIP (300 mil)
μPD6125AG-xxx	24-pin Plastic SOP (300 mil)
μPD6126AG-xxx	28-pin Plastic SOP (375 mil)
μPD6600ACS-xxx	20-pin Plastic Shrink DIP (300 mil)
μPD6600AGS-xxx	20-pin Plastic SOP (300 mil)
μPD61P24CS	20-pin Plastic Shrink DIP (300 mil)
μPD61P24GS	20-pin Plastic SOP (300 mil)

★ 1.3 Pin Configuration (Top View)

(1) Normal Operation Mode

20-pin Plastic Shrink DIP (300 mil)
- μPD6124ACS-xxx
- μPD6600ACS-xxx
- μPD61P24CS

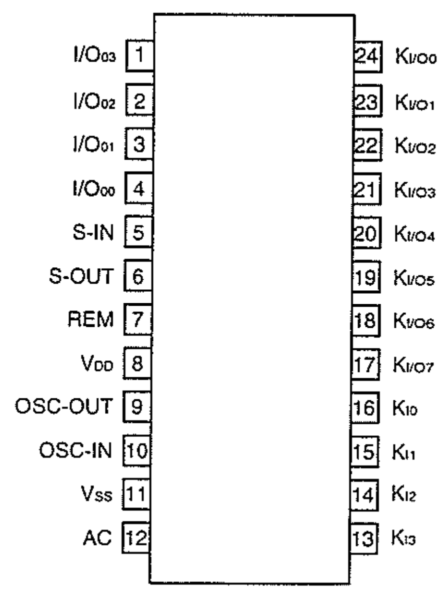
20-pin Plastic SOP (300 mil)
- μPD6124AGS-xxx
- μPD6600AGS-xxx
- μPD61P24GS



AC : All Clear
K_{I0} to K_{I3} : Key Input
$K_{I/O0}$ to $K_{I/O7}$: Key Input/Output
OSC-IN, OSC-OUT : System Clock Oscillation
REM : Carrier Modulation Output
S-IN : Serial Input
S-OUT : Transmitting Output Display
V_{DD} : Power Supply
V_{SS} : Ground

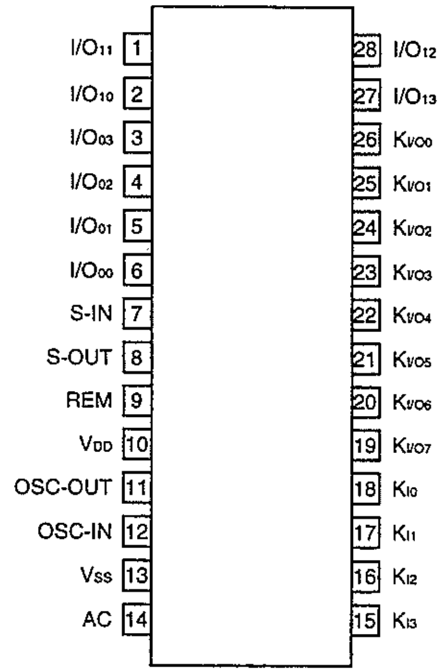
24-pin Plastic Shrink DIP (300 mil)
- μPD6125ACA-xxx

24-pin Plastic SOP (300 mil)
- μPD6125AG-xxx



AC : All Clear
I/O_{00} to I/O_{03} : Key Matrix Expansion Input/Output
K_{I0} to K_{I3} : Key Input
$K_{I/O0}$ to $K_{I/O7}$: Key Input/Output
OSC-IN, OSC-OUT : System Clock Oscillation
REM : Carrier Modulation Output
S-IN : Serial Input
S-OUT : Transmitting Output Display
V_{DD} : Power Supply
V_{SS} : Ground

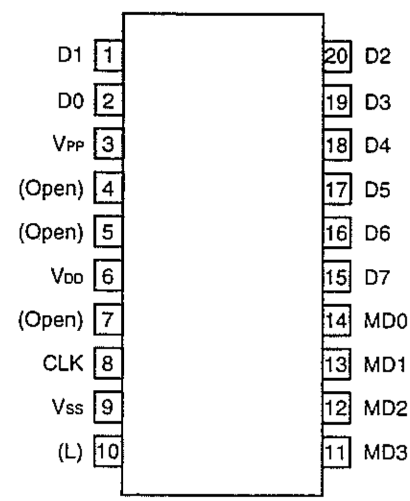
28-pin Plastic SOP (75 mil)
μPD6126AG-xxx



AC	: All Clear
I/O_{00} to I/O_{03}, I/O_{10} to I/O_{13}	: Key Matrix Expansion Input/Output
K_{I0} to K_{I3}	: Key Input
$K_{I/O0}$ to $K_{I/O7}$	: Key Input/Output
OSC-IN, OSC-OUT	: System Clock Oscillation
REM	: Carrier Modulation Output
S-IN	: Serial Input
S-OUT	: Transmitting Output Display
V_{DD}	: Power Supply
V_{SS}	: Ground

(2) PROM Programming Mode

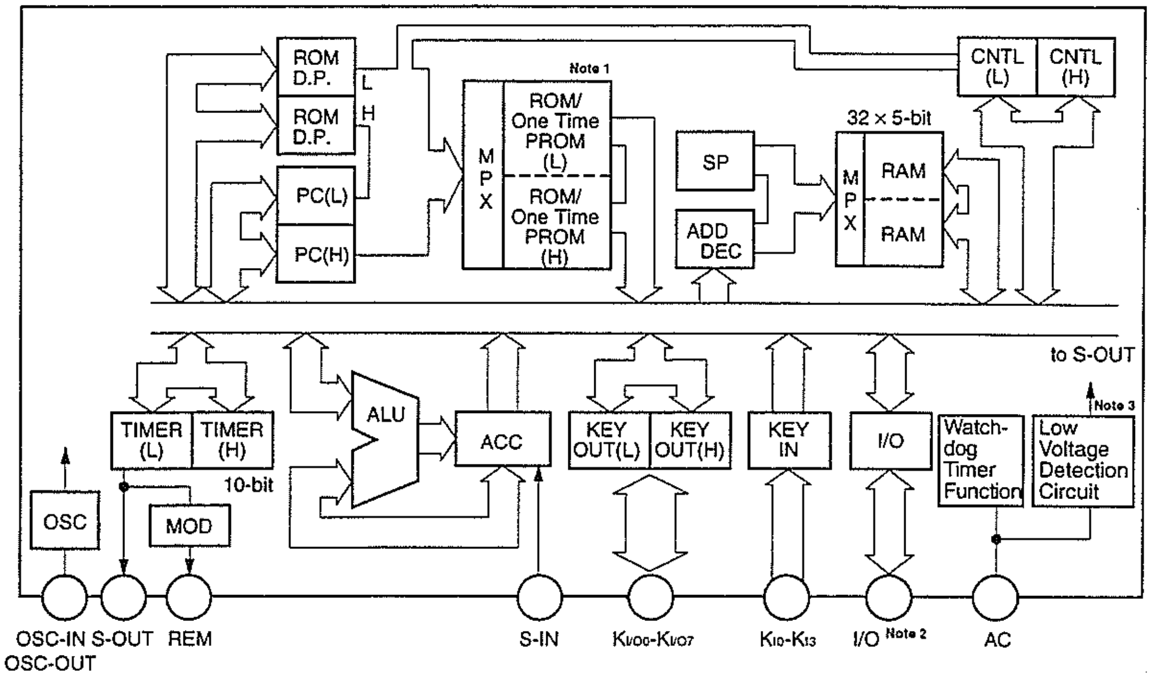
20-pin Plastic Shrink DIP (300 mil)
μPD61P24CS
20-pin Plastic SOP (300 mil)
μPD61P24GS



Caution Processing indicated in ( ) is processing for that pin when not used in the PROM programming mode.
L : Connect to GND independently via a resistor (470 Ω).
Open : Do not connect anything.

CLK	: Address Update Clock Input
D0 to D7	: Data Input/Output
MD0 to MD3	: Operating Mode Select
V_{DD}	: Power Supply
V_{PP}	: Program Voltage Impression
V_{SS}	: Ground

1.4 Programmable Remote Control Block Diagram



Notes 1. ROM (or PROM) capacity differs depending on the product.

μPD6600A : 512 × 10-bit

μPD6124A, 6125A, 6126A, 61P24 : 1002 × 10-bit

2. μPD6124A, 6600A, 61P24 : none

μPD6125A : I/O_{00} to I/O_{03}

μPD6126A : I/O_{00} to I/O_{03}, I/O_{10} to I/O_{13}

3. Only the μPD6124A and 6600A have low voltage detection circuits.

[MEMO]

(1) Normal Operation Mode

Pin Name	Input/Output	Function	After Reset
$K_{I/O0}$ to $K_{I/O7}$	Input/Output	Selects input or output by the control register. Can be used as a key scan output in the output mode. Pull down resistance is added in the input mode.	Input
I/O_{00} to I/O_{03} Note 1 I/O_{10} to I/O_{13} Note 2	Input/Output	Can be used as a key scan output in the output mode. Pull down resistance is added in the input mode.	Input
K_{I0} to K_{I3}	Input	Input pin with built-in pull down resistor.	Input
S-IN	Input	Reads S-IN data according to the accumulator's shift command. Specification of the S-IN data input mode is executed by the control register. Pull down resistance is added in the input mode. The S-IN pin enters the high impedance state when the input mode is canceled.	Input
REM	Output	Carrier Modulation Output Pin ··· $f_{osc}/8$, $f_{osc}/12$ Active High	Output
S-OUT	Output	An output which is synchronized with the REM pin output and is not carrier modulated can be obtained. Active Low	Output
AC	—	• System reset input pin. The system is reset by setting it on the low level. • Watchdog timer pin Operates as a watchdog timer by charging and discharging an external capacitor.	—
OSC-IN OSC-OUT	—	f_{osc} = 400 to 500 kHz Pin for the ceramic oscillator	—
V_{DD}	—	Power Supply	—
V_{SS}	—	GND	—

★ **Notes** 1. The μPD6124A, 6600A, and 61P24 do not have the I/O_{00} to I/O_{03} pins.

★ 2. The μPD6124A, 6125A, 6600A, and 61P24 do not have the I/O_{10} to I/O_{13} pins.

(2) PROM Programming Mode (μPD61P24 only)

Pin Name	Function
V_{PP}	Program Voltage (12.5 V) impression
CLK	Address update clock input
MD0 to MD3	Operating mode selection
D0 to D7	8-bit data input/output
V_{DD}	Power supply voltage (6 V) impression
Vss	GND

[MEMO]

CHAPTER 3 INTERNAL BLOCK FUNCTIONS

★ 3.1 Program Counter (PC) ······ 9-bit: μPD6600A
10-bit: μPD6124A, 6125A, 6126A, 61P24

This is a binary counter which holds program memory address information.

Figure 3-1. Program Counter Configuration

(a) μPD6600A

PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	PC

(b) μPD6124A, 6125A, 6126A, 61P24

PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	PC

Ordinarily, the program counter is incremented automatically each time a single instruction is executed, by an amount corresponding to the number of bytes of that instruction.

When the Jump command (JMP0, JC, JF) is executed, it shows the jump destination.

Immediate data or the contents of data memory are loaded in the PC in their entirety or partially.

When the call command (CALL0) is executed, the current contents of the PC are incremented (+1) ,and after the stack memory is cleared, the values required for the respective jump commands are loaded.

When the return command (RET) is executed, the contents of the stack memory are incremented by 2 and loaded in the PC.

The PC is cleared to 000H when there is a reset (all clear).

3.2 Stack Pointer (SP) ······ 2-bit

This is a 2-bit register which holds the top address information of the stack area. The stack area is used in common with data memory.

The SP is incremented when the call (CALL0) command is executed and decremented when the return (RET) command is executed.

It is cleared to 00B when there is a reset (all clear), and the topmost address of the data memory, FH is specified in data memory as the stack area.

The relationship between the stack pointer and the data memory area is shown in the following figure.

Data Memory		(SP)
		R_C — 11B
		R_D — 10B
		R_E — 01B
		R_F — 00B

If the stack pointer overflows or underflows, it is judged that the CPU is in the runaway state, and the internal reset signal is generated.

If the data memory is used as a stack, R_{1C} – R_{0C}, R_{1D} – R_{0D}, R_{1E} – R_{0E} and R_{1F} – R_{0F}, operate as pair registers.

Since a battery is ordinarily used as the power supply for infrared remote control transmitters, there is a possibility that the contents of the registers could change suddenly due to voltage fluctuations.

Since the stack pointer (SP) is the register that is used when the CALL0 and RET commands are executed, there is a possibility that the contents of the register could change suddenly just as with other registers or ports.

Each time processing ends, the data memory (RAM) or port can be initialized, but the stack pointer differs from other registers or ports, and since there is no instruction which sets a value in it, the stack pointer cannot be initialized while programming. The stack pointer is cleared to 00B only after an all clear is input and when there is a stack overflow or underflow.

When considering that initialization of the stack pointer is difficult, as described above, and the problems that would occur if the stack pointer deviates, we think that the CALL0 command should be used as little as possible in a remote control transmitter's program.

However, due to ROM capacity, there are some cases where the CALL0 command must be used, so if the CALL0 command is used, please carry out the following processing. That is to say, incorporate a program's initialization segment which checks whether or not the stack pointer is deviating or not, and if it is deviating, execute an all clear (make this the routine that is followed each time a processing task is completed).

The program for performing the previously mentioned processing is shown below.

Example:

```
INITL:   MOV    RF, #3FFH
         CALL0  SPTES Note
           :
SPTES:   MOV    A,R1F
         SCAF
         JC     ALLCR
         RET

ALLCR:   NOP
         CALL0  ALLCR
```

Note Write the program so that the address of the command "CALL0 SPTES" in the program example is an address other than $A_9\ A_8\ A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0$ = * * 11101111 (* is a 1 or 0).

In the initialization segment (INITL segment) input 3FFH to the RF register which stack pointer 00B points to and jump to SPTES by the CALL0 command.

Check the value of R1F in the subroutine SPTES. If the value of the stack pointer is 00B, the program counter's value will not be cleared by the CALL0 command, so 0FH will not be set in R1F.

Accordingly, if the value of R1F is not 0FH, judge that the value of the stack pointer is correct and return to the mail routine.

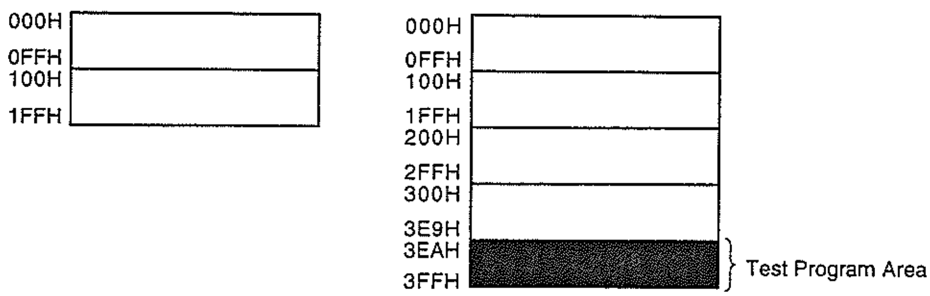
If the stack pointer is deviating, the value of the R1F register will become 0FH. Jump to ALLCR and perform discharge of the watchdog timer by repeating the NOP command a number of times. Make it so that an all clear occurs, or so that an all clear occurs by stack pointer overflow.

★ 3.3 Program Memory (ROM) ······512 steps × 10-bit : μPD6600A
1002 steps × 10-bit: μPD6124A, 6125A, 6126A, 61P24 Note

This ROM is configured at 10-bit per step and is addressed by the program counter.
Program memory is loaded with program or table data, etc.

Figure 3-2. Program Memory Map

(a) μPD6600A   (b) μPD6124A, 6125A, 6126A, 61P24 Note



Note The μPD61P24 is a one time PROM.

3.4 Data Memory (RAM) ...... 32 words × 5-bit

Data memory is static RAM configured in 32 words × 5-bit. It is used to store processing data. The data memory can be processed in 8-bit units. R_0 can be used as a data pointer.

The RAM value when the power is turned on is indefinite, and the previous data are preserved until a reset (R_0 is indefinite).

Figure 3-3. Data Memory Configuration

R_{1X} (H)	R_{0X} (L)		
R_{10}	R_{00}	R_0	
R_{11}	R_{01}	R_1	
R_{12}	R_{02}	R_2	
R_{13}	R_{03}	R_3	
R_{14}	R_{04}	R_4	
R_{15}	R_{05}	R_5	
R_{16}	R_{06}	R_6	
R_{17}	R_{07}	R_7	
R_{18}	R_{08}	R_8	
R_{19}	R_{09}	R_9	
R_{1A}	R_{0A}	R_A	
R_{1B}	R_{0B}	R_B	
R_{1C}	R_{0C}	R_C	SP-3
R_{1D}	R_{0D}	R_D	SP-2
R_{1E}	R_{0E}	R_E	SP-1
R_{1F}	R_{0F}	R_F	SP-0

★ **Caution** **RAM R_D, R_E and R_F are used in common with stack memory, so please avoid their use, particularly within CALL routines, as much as possible (this is a countermeasure for the CPU when it is in the runaway state due to the SP value being destroyed by noise, etc.).**
Also, if this memory is used as general purpose RAM, be sure to include a stack pointer check within the main routine.

3.5 Data Pointer (R_0)

R_0 (R_{10}, R_{00}) of the data memory has the function of data pointer for ROM. R_0 specifies the lower 8-bit of the ROM address and the higher 2-bit are specified by the control register.

By setting the ROM address in the data pointer and calling the contents of ROM, it is possible to execute table reference to ROM data easily.

★ It becomes indefinite when reset (all clear).

Figure 3-4. Data Pointer Configuration

Control Register (P1)		R_{10}				R_{00}				
AD_9 Note	AD_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	R_0

Note AD_9 = 0 in the μPD6600A

3.6 Accumulator (A) 4-bit

The accumulator has a 4-bit configuration, and each operation is executed centering on the accumulator.

★ Its value is indefinite when there is a reset (all clear).

Figure 3-5. Accumulator Configuration

A_3	A_2	A_1	A_0	A

3.7 Arithmetic Logic Unit (ALU) 4-bit

The arithmetic logic unit is a math circuit with a 4-bit configuration and executes simple processing centered around logical operations.

3.8 Flags

(1) Status Flag

When the condition of each pin is checked by the STTS command, if the status matches the conditions specified in the STTS command, the status flag (F) is set (1).

★ This flag becomes indefinite when there is a reset (all clear).

(2) Carry Flag

If a carry from the MSB of the accumulator occurs when the INC (increment) command or RL (rotate left) command is executed, the carry flag (C) is set (1).

Also, if the content of the accumulator is "FH" when the SCAF command is executed, the carry flag (C) is set (1).

★ This flag becomes indefinite when there is a reset (all clear).

3.9 Port (Pp)

The $K_{I/O}$, I/O, K_I, and control register are treated as port registers. The relationship between port registers and each pin are as shown below.

★ **Table 3-1. Relationship between Port Registers and Each Pin**

Pin Name	During Input Mode		During Output Mode		During Reset
	Read	Write	Read	Write	
$K_{I/O}$	Pin State	Output Latch	Pin State	Output Latch	Indefinite [Input/Output Mode, Output Latch]
K_I	Pin State	–	–	–	Input Mode
I/O_0 Note 1 I/O_1 Note 2	Pin State	Output Latch	Pin State	Output Latch	Input Mode, Output Latch is indefinite
S-IN	When D_0 of the P_1 register = 1, read the pin status by the R_L A command.				High Impedance (D_0 of P_1 register = 0)

P_{1X} (H)		P_{0X} (H)	
$K_{I/O7-4}$ P_{10}		$K_{I/O3-0}$ P_{00}	P_0
Control Register (H) P_{11}		Control Register (L) P_{01}	P_1
K_{I3-0} P_{12}		— P_{02}	P_2
— P_{13}	IN/OUT	I/O_0 Note 1 P_{03}	P_3
— P_{14}	IN/OUT	I/O_1 Note 2 P_{04}	P_4

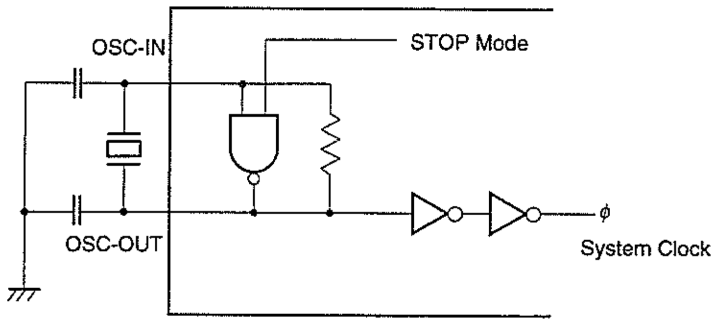
★ **Notes** 1. The μPD6124A, 6600A, and 61P24 do not contain the I/O_{00} to I/O_{03} pins.

★ 2. The μPD6124A, 6125A, 6600A, and 61P24 do not contain the I/O_{10} to I/O_{13} pins.

3.10 System Clock Generator Circuit

The system clock generator circuit is configured from a ceramic oscillator (400 to 500 kHz) circuit.

Figure 3-6. System Clock Generator Circuit



The system clock generator circuit stops the oscillator circuit when in the STOP mode (Oscillator Stop HALT Command) and the system clock stops.

3.11 Timer

The timer is a block which determines the transmission output pattern. It is configured from a 9-bit down counter and a 1-bit latch which determines whether or not a carrier is output, and thus has a total of 10-bit.

The 9-bit down counter synchronizes with the machine cycle after down counting starts, and decrements (−1) each ★ $8/f_{osc}$ (s). The down count stops when all bits of the 9-bit have become 0. When the down count stops, a signal is output which is interpreted to mean that timer operation has ended, and if the CPU's operating state is that it is waiting for timer operation to terminate (HALT TIMER), the wait state (HALT) is canceled and the CPU executes the next command. When a value is set in the down counter again by the next command, it counts down continuously without error (there is no influence even on the carrier output side of the REM pin).

Set the down count time based on the calculation of (set value (HEX) + 1) × $8/f_{osc}$. Setting of the value in the timer is done by the timer operation command.

The carrier for remote control transmission can also be output to the REM pin during down counter operation. Selection of whether to output the carrier or not is done by the MSB of the timer's register. if the carrier is output, this bit is set at "1" and if the carrier is not output, this bit is set at "0."

If the down counter's value reaches "0" in all its bits while the carrier is being output, carrier output halts. The REM pin's output goes low when the carrier is not being output.

★ A signal synchronized with the REM output is output to the S-OUT pin. However, the S-OUT pin waveform is low when the carrier is being output to the REM pin, and high when the carrier is not being output to the REM pin.

If the HALT command, which changes to the oscillator stop mode is executed during operation of the down counter, the mode changes to the oscillator stop mode after the down count terminates (after the counter's value becomes 0).

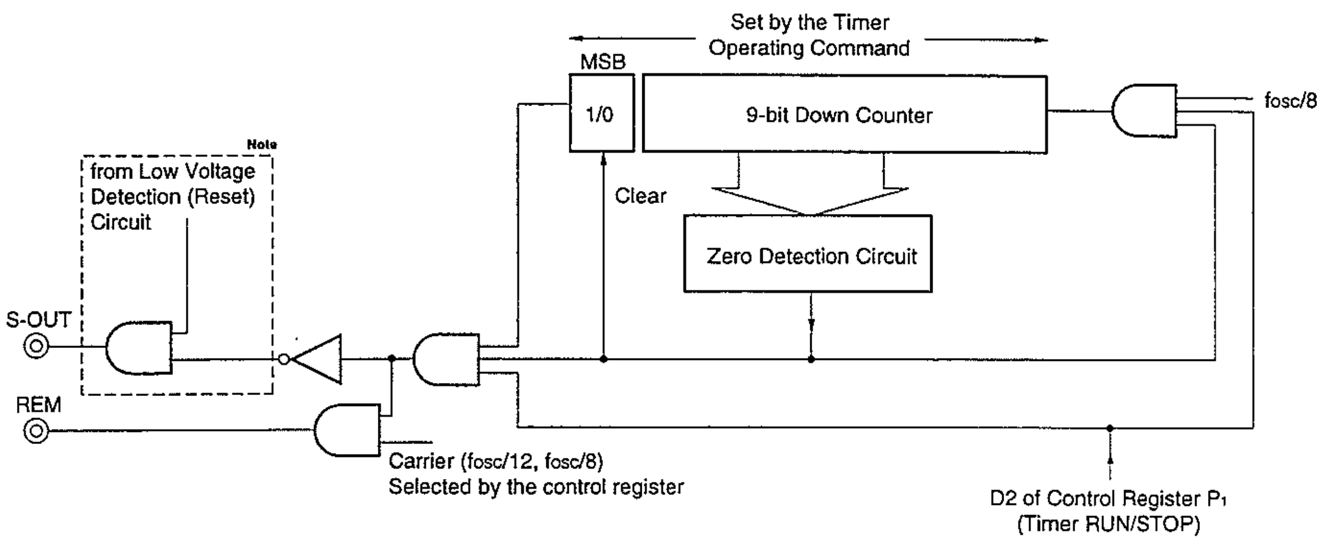
STOP/RUN control of the timer's operation is accomplished by the control register (P_1) (See 3.16, "Control Register (P_1)).

★ When there is a reset (all clear), the REM pin goes low and the S-OUT pin goes high. All 10-bit of the timer are also cleared to 000H.

★ **Cautions 1. The timer clock and carrier output are not synchronized, so the pulse width at the start and end of the carrier output may become short.**

★ **2. In a reset by the low voltage detection circuit (in the μPD6124A and 6600A only), the S-OUT pin goes low.**

★ **Figure 3-7. Timer Block Configuration**



Note There is no low voltage detection circuit in the μPD6125A, 6126A or 61P24.

★ 3.12 S-OUT Pin

This is a pin for communications display which outputs at the low level during REM pin carrier output.
The S-OUT pin is a CMOS output.
During reset, its output is at the high level.

3.13 S-IN Pin (D_0 bit of P_1)

Input of serial data is accomplished using the S-IN pin. If the control register (P_1) is set in the serial input mode, the S-IN pin can be connected as the LSB of the accumulator and at the same time, the S-IN pin can be pulled down to the V_{SS} level internally in the LSI Note. In this state, if the accumulator's Rotate Left command (RL A) is executed, the data in the accumulator's LSB is fetched to the S-IN pin.

If the control register's setting is released from the serial input mode, the impedance of the S-IN pin goes high and a continuity current cannot flow internally.

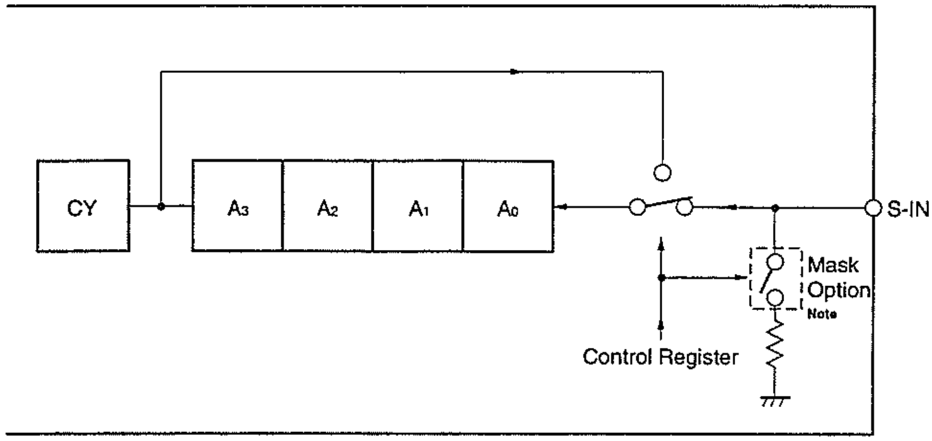
When the accumulator's rotate left command is executed, the data in the MSB is input in the LSB.

★ When there is a reset (all clear), the impedance of the S-IN pin goes high.

Note In the μPD61P24, the mask option is fixed so that the pull down resistor is ON.

Figure 3-8. S-IN Pin Configuration

★



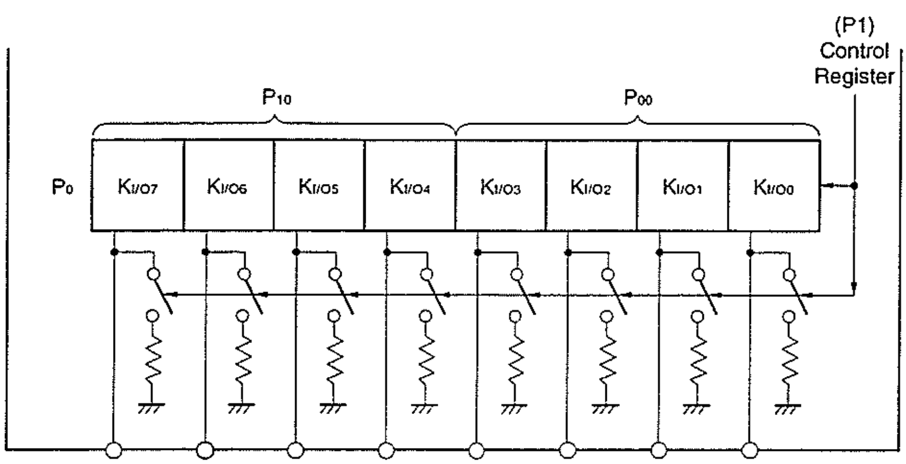
Note In the μPD61P24, the mask option is fixed so that the pull down resistor is ON.

3.14 KI/O Pin (P0)

This is an 8-bit input/output terminal for key scan output. If the control register (P_1) is set in the input mode, it can be used as an 8-bit input terminal. If it is set in the input mode, all the pins internally in the LSI are pulled down to the Vss level.

★ When there is a reset (all clear), the input/output mode and the value of the output latch become indefinite.

Figure 3-9. KI/O Pin Configuration



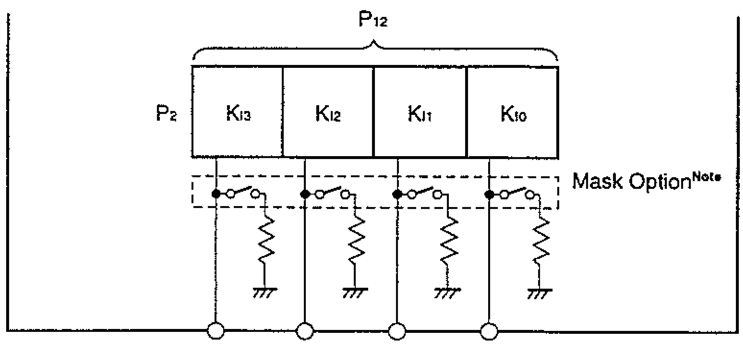
3.15 KI Pin (P_{12})

This is a 4-bit input pin for key input. All the pins can be pulled down to the Vss level in bit units through the mask option.

Note In the μPD61P24, the mask option is fixed so that the pull down resistor is ON.

Figure 3-10. KI Pin Configuration

★



Note In the μPD61P24, the mask option is fixed so that the pull down resistor is ON.

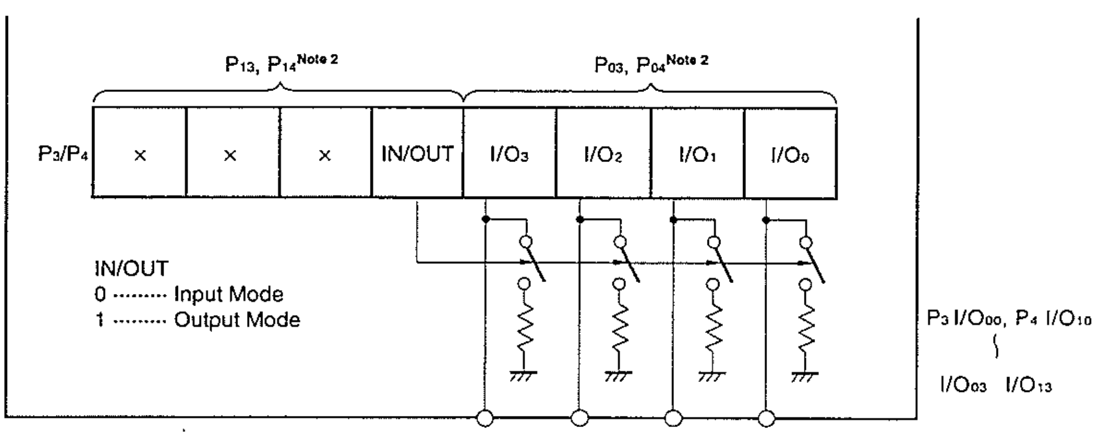
3.16 I/O Pin [Note 1] (P_3, P_4 [Note 2])

This is an input/output pin for key matrix expansion. Switching between the input mode and the output mode is executed by each LSB of P_{13} and P_{14}. [Note 2]

If set in the input mode, all the pins are pulled down to the Vss level internally in the LSI.

★ When there is a reset (all clear), this terminal switches to the input mode, and the value of the output latch is indefinite.

Figure 3-11. I/O Pin Configuration



Notes 1. The μPD6124A, 6600A and 61P24 do not have I/O terminals.

2. The μPD6125A does not have P4 (P_{04}, P_{14}).

3.17 Control Register (P_1)

The control register is configured from 10-bit. The contents of this register that can be controlled are as shown in Table 3-2.

Table 3-2. Control Register (P_1)

Bit		D_9	D_8	D_7	D_6	D_5[Note]	D_4	D_3	D_2	D_1	D_0
Name		Test Mode		—	HALT	D.P. AD_9	D.P. AD_8	MOD	Timer	$K_{I/O}$	RL Acc $A_0 \leftarrow$
Set Value	0	Always set to 0.			NOP	$AD_9 = 0$	$AD_8 = 0$	$f_{osc}/8$	STOP	IN	A_3
	1				OSC STOP	$AD_9 = 1$	$AD_8 = 1$	$f_{osc}/12$	RUN	OUT	S-IN

D_0 .... If the accumulator is shifted to the left, it specifies the data input in A_0.
0: A_3, 1: S-IN

D_1 .... Specifies the $K_{I/O}$ status.
0: Input Mode, 1: Output Mode

D_2 .... Specifies the timer status.
.... 0: Count Halt, 1: Count Run

D_3 .... Specifies the carrier frequency of the REM output.
0: $f_{osc}/8$, 1: $f_{osc}/12$

D_4, D_5 Note .... Specify the higher order 2-bit of the ROM data pointer.

D_6 .... Sets the oscillator circuit when the HALT command is executed.
0: Oscillation does not stop.
1: Oscillation stops. (STOP Mode)

D_7 .... Always set this pin to 0.

D_8, D_9 .... This is the test mode specification register. Always set it to 0.

★ **Note** In the case of the μPD6600A, always set D_5 to 0.

Remark D_0, D_8, and D_9 becomes 0 after reset, and the other bits are indefinite.

Caution **If the data memory is used for replacing the program counter contents or transferring ROM contents or immediate data, etc., this register is handled as 5-bit.**

Examples 1. MOV R1, #data

R_{11} to R_{01} are treated as pair registers and store 10-bit of data.

2. MOV R1, @R0

R_{10} to R_{00} are treated as pair registers and the ROM contents specified in the control register (P_{11}) and R_{10} to R_{00} are transferred to R_{11} to R_{01}.

However, if the accumulator is used, the lower 4-bit only are valid and the MSB (5th bit) always becomes "0." When the ROM data pointer is used, it specifies the higher 2-bit (AD_9, AD_8) in D_4 and D_5 of the control register.

Remark The correspondence table between the register, program counter, data pointer, timer and accumulator is as follows.

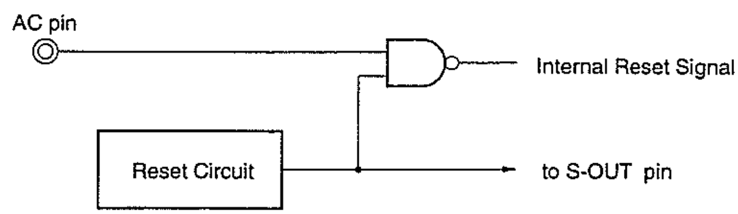
H					L					
R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0	Register
PC_9	PC_7	PC_6	PC_5	PC_4	PC_8	PC_3	PC_2	PC_1	PC_0	Program Counter
AD_9	AD_7	AD_6	AD_5	AD_4	AD_8	AD_3	AD_2	AD_1	AD_0	Data Pointer
t_1	t_9	t_8	t_7	t_6	t_0	t_5	t_4	t_3	t_2	Timer
"0"	A_3	A_2	A_1	A_0	"0"	A_3	A_2	A_1	A_0	Accumulator

★ 3.18 Low Voltage Detection (Reset) Circuit ····· μPD6124A, 6600A only

A low voltage detection (reset) circuit is incorporated to prevent a program from entering the runaway state.

When the power supply voltage V_{DD} is below 1 V, an internal reset signal is generated. Also, when in the reset state, the low level is output to the S-OUT pin.

★ **Figure 3-12. Low Voltage Detection (Reset) Circuit**



Caution The power supply voltage which can be put out by the low voltage detection circuit has a range of 1 to 2.2 V. Therefore, when the power supply voltage is 2 V or lower, it is possible that the program counter could enter the runaway state before the low voltage detection circuit operates.

[MEMO]

CHAPTER 4 STANDBY FUNCTION

In order to restrict power consumption while waiting for a program standby, two standby modes are provided in the μPD612x Series. Either the oscillation stop state (STOP Mode) or the oscillation continue state (HALT Mode) is decided by the value of the control register (D_6) when the HALT command is executed.

$D_6 = 0$ .... Oscillation Continue
$D_6 = 1$ .... Oscillation Stop

Conditions for canceling the standby mode are specified when the HALT command is executed.

When the standby mode canceling conditions is the state in (1), it is judged that cancellation of the standby is impossible, and it is initialized.

(1) Canceling standby of a pin which is set in the output mode

If multiple pins are specified, if even one of those pins is in the output mode, initialization is executed.

(2) Canceling standby in the case where the timer enters the timer wait HALT Mode while in the stop state

If the timer enters the timer wait HALT Mode, after it is detected that the timer's value is 0, standby is canceled. If the oscillation stop HALT command is executed during timer operation, execution is after the timer's value has become 0. [Note]

However, if the standby cancellation conditions match, standby is canceled even if the timer's value has not become 0.

Note If the timer's state is changed to clock stop (control register $D_2 = 0$) during timer countdown and the oscillation stop HALT command is executed, if the timer's value is not 0, it enters the HALT mode without oscillation stopping, so exercise caution.

4.1 HALT Instruction

The HALT instruction, is so structured that it can be confirmed whether or not there is an input at each input terminal.

D_3	D_2	D_1	D_0	Cancellation Condition	Remarks
0/1	0	0	0	S-IN	If RL ← A_3 is selected, the standby mode is always canceled.
	0	0	1	$K_{I/O}$	Valid only when in the IN Mode.
	0	1	0	K_I	
0	0	1	1	Timer	Canceled when it becomes 0.
0/1	1	0	0	I/O_0 [Note 1]	Valid only when in the IN Mode.
	1	0	1	I/O_1 [Note 2]	
1	1	1	0	K_I, I/O_0 [Note 1], I/O_1 [Note 2]	If even one I/O is in the OUT mode, it is judged as an error and initialization is performed.

↳ Cancellation Conditions "0" .. Low Level Detection
"1" .. High Level Detection

Notes 1. The μPD6124A, 6600A, and 61P24 do not have the I/O_{00} to I/O_{03} pins.
2. The μPD6124A, 6125A, 6600A, and 61P24 do not have the I/O_{10} to I/O_{13} pins.

The oscillation circuit can be stopped by the value of the control register (D_6) when the HALT command is executed. In the state where timer count is stopped, a HALT command causes an internal reset by the timer.

In cancellation when the oscillation circuit is stopped (when in the STOP Mode), cancellation is executed when the input's rise or fall is detected and oscillation started. In cancellation when the oscillation circuit is not stopped (when in the HALT Mode), the input level is judged by latching with the internal clock.

4.2 STATUS Instruction (STTS)

After standby is canceled, the STATUS instruction can be used to confirm the standby canceled condition. If the standby canceled condition matches the expected value, the status flag (F) is set to "1."

D_3	D_2	D_1	D_0	Standby Cancellation Condition
0/1	0	0	0	S-IN
	0	0	1	$K_{I/O}$
	0	1	0	K_I
0	0	1	1	Timer
0/1	1	0	0	I/O_0 Note 1
	1	0	1	I/O_1 Note 2
1	1	1	0	K_I, I/O_0 Note 1, I/O_1 Note 2

↳ Input Expected Value "0" ... Low Level
"1" ... High Level

Notes 1. The μPD6124A, 6600A, and 61P24 do not have the I/O_{00} to I/O_{03} pins.
2. The μPD6124A, 6125A, 6600A, and 61P24 do not have the I/O_{10} to I/O_{13} pins.

When the STATUS condition regarded as matching when the input level is the same as the expected value. After the standby mode is canceled, it is not judged as matching after the input level has inverted.

Caution "1" (high level detection) is specified as the expected value in the HALT and STTS commands. When either of these goes high during input of the setting conditions, the standby mode is canceled or the status flag (F) is set. If "0" is set (low level detection), detection occurs and operation begins when all the specified input conditions become 0.

[MEMO]

When the AC pin goes low, the all clear circuit operates and the CPU is reset internally, beginning with the program counter.

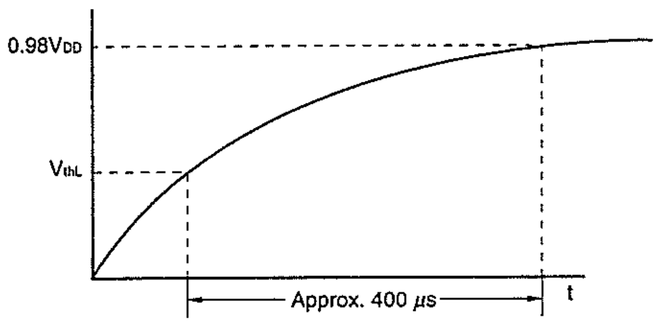
The capacitor added to the AC pin is charged and discharged through a resistor in the IC. The all clear circuit operates when the condenser's voltage becomes lower than the AC pin's low level and the threshold value.

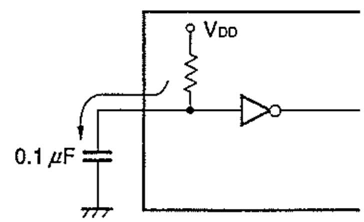
Charging and discharging of the capacitor is controlled through the program.

(1) Start Charging Command

Execute a HALT instruction immediately after the NOP instruction.

Charging Time When C = 0.1μF

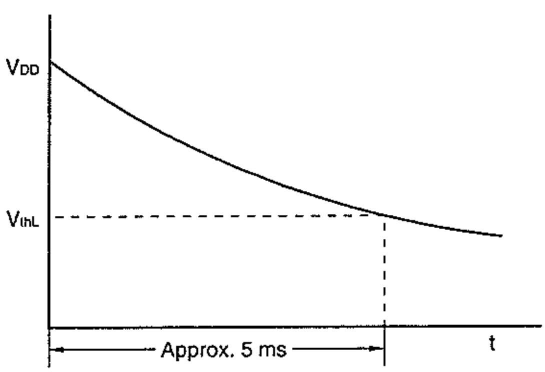


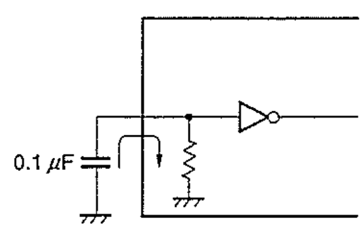


(2) Discharge Start Command

Start discharge by the NOP command.

Discharge Time When C = 0.1 μF



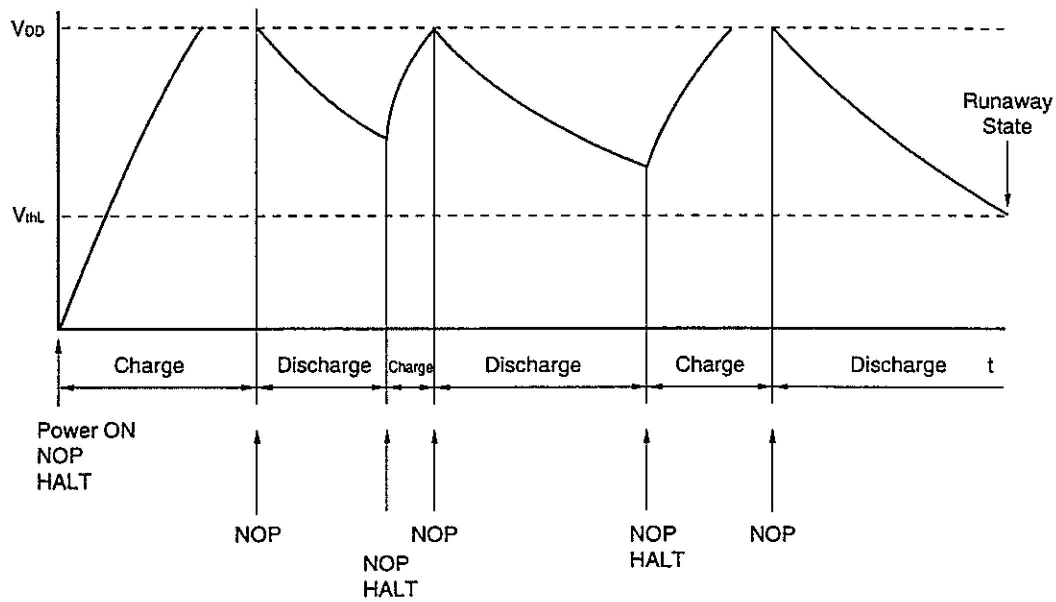


When discharge is repeated by the program and the capacitor's voltage becomes lower than V_{thL}, it is judged that the IC's operation is in the runaway state.

★ Therefore, carry out programming in such a way that the capacitor's charge will not drop below V_{thL}.

If the capacitor's value is made low, the time required for charging or discharging becomes shorter in proportion to the capacitor's value. Also, this circuit operates as a power on reset circuit when the power is turned on.

Operation Example



Caution **When the watchdog timer function is not being used, execute the NOP command immediately before the HALT command at the start of the program to set it in the charge mode (be sure to connect the capacitor).**

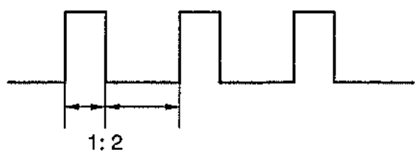
CHAPTER 6 REM OUTPUT

★ The transmission carrier frequency can be selected as either $f_{osc}/8$ or $f_{osc}/12$ by D_3 of the control register (P_1). The carrier duty can be selected as either 1/3 or 1/2 when the carrier frequency is $f_{osc}/12$. Note (However, when the carrier frequency is $f_{osc}/8$, the duty is fixed at 1/2.)

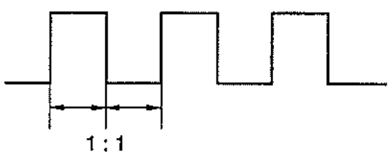
★ **Note** The mask option in the μPD61P24 is fixed so that the duty is 1/3.

Figure 6-1. Carrier Waveform

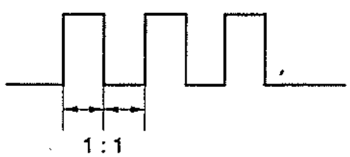
(1) D_3 = 1: $f_{osc}/12$
1/3 Duty



(2) D_3 = 1: $f_{osc}/12$
1/2 Duty

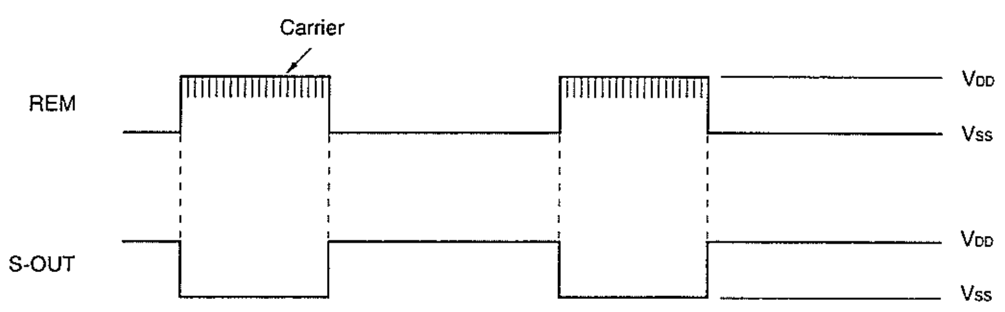


(3) D_3 = 0: $f_{osc}/8$
1/2 Duty



★ The S-OUT pin is a display pin which outputs at the low level during communications when the REM pin is outputting the carrier.

Figure 6-2. REM Pin and S-OUT Pin Output Example



[MEMO]

7.1 Accumulator Operating Instructions

- ANL A, Rr

① Instruction Code :

1 1 0 1	R_4 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

③ Function : (A) ← (A) ∧ (R_r) r = 00 to 0F 10 to 1F

Takes the logical product of the contents of the accumulator and the contents of the Rr register, and loads the results in the accumulator.

CARRY ← $A_3 \cdot R_3$

- ORL A, Rr

① Instruction Code :

1 1 1 0	R_4 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

③ Function : (A) ← (A) ∨ (R_r) r = 00 to 0F 10 to 1F

Takes the logical sum of the contents of the accumulator and the contents of the Rr register, and loads the results in the accumulator.

CARRY ← 0

- XRL A, Rr

① Instruction Code :

1 0 1 0	R_4 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

③ Function : (A) ← (A) $\veebar$ (R_r) r = 00 to 0F 10 to 1F

Takes the exclusive OR of the contents of the accumulator and the contents of the Rr register, and loads the results in the accumulator.

CARRY ← $A_3 \cdot R_3$

- INC A

① Instruction Code :

1 0 1 0	0 1	0 0 1 1

② Number of Cycles: 1

③ Function : (A) ← (A) + 1

Increments the contents of the accumulator (+1).

CARRY ← CARRY

- RL A

① Instruction Code :

1 1 1 1	0 1	0 0 1 1

② Number of Cycles: 1

③ Function : $(A_{n+1}) \leftarrow (A_n)$

$(A_0) \leftarrow (A_3)$ /S-IN

Rotates the contents of the accumulator one bit at a time to the left.

Data input to A_0 can be can be specified in the control register as the contents of A_3 or the serial input.

CARRY ← A_3

- ANL A, # data

① Instruction Code :

1 1 0 1	1 1	0 0 0 1

0	0 0 0 0	0	d_3 d_2 d_1 d_0

② Number of Cycles: 1

③ Function : $(A) \leftarrow (A) \wedge$ data

Takes the logical product of the contents of the accumulator and immediate data, and loads the results in the accumulator.

CARRY ← $A_3 \cdot d_3$

- ORL A, # data

① Instruction Code :

1 1 1 0	1 1	0 0 0 1

0	0 0 0 0	0	d_3 d_2 d_1 d_0

② Number of Cycles: 1

③ Function : $(A) \leftarrow (A) \vee$ data

Takes the logical sum of the contents of the accumulator and immediate data, and loads the results in the accumulator.

CARRY ← 0

- XRL A, # data

① Instruction Code :

1 0 1 0	1 1	0 0 0 1

0	0 0 0 0	0	d_3 d_2 d_1 d_0

② Number of Cycles: 1

③ Function : $(A) \leftarrow (A) \veebar$ data

Takes the exclusive OR of the contents of the accumulator and immediate data, and loads the results in the accumulator.

CARRY ← $A_3 \cdot d_3$

- ANL A, @R_0H/L

① Instruction Code :

1 1 0 1	0/1 1	0 0 0 0

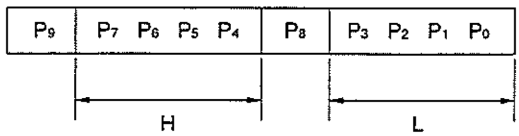
② Number of Cycles: 1

③ Function : $(A) \leftarrow (A) \wedge ((R_0H/L))$

Takes the logical product of the contents of the accumulator, control register P_{11} and the contents of program memory specified by pair register R_{10} to R_{00}, and loads the results in the accumulator.

If H is specified, P_7, P_6, P_5 and P_4 become valid and if L is specified, P_3, P_2, P_1 and P_0 become valid.

Remark Program Memory Configuration



Valid bits when the accumulator is operating

CARRY $\leftarrow A_3 \cdot P_7 (P_3)$

- ORL A, @R_0H/L

① Instruction Code :

1 1 1 0	0/1 1	0 0 0 0

② Number of Cycles: 1

③ Function : $(A) \leftarrow (A) \vee ((R_0H/L))$

Takes the logical sum of the contents of the accumulator, control register P_{11} and the contents of program memory specified by pair register R_{10} to R_{00}, and loads the results in the accumulator.

If H is specified, P_7, P_6, P_5 and P_4 become valid and if L is specified, P_3, P_2, P_1 and P_0 become valid.

CARRY $\leftarrow$ 0

- XRL A, @R_0H/L

① Instruction Code :

1 0 1 0	0/1 1	0 0 0 0

② Number of Cycles: 1

③ Function : $(A) \leftarrow (A) \veebar ((R_0H/L))$

Takes the exclusive OR of the contents of the accumulator, control register P_{11} and the contents of program memory specified by pair register R_{10} to R_{00}, and loads the results in the accumulator.

If H is specified, P_7, P_6, P_5 and P_4 become valid and if L is specified, P_3, P_2, P_1 and P_0 become valid.

CARRY $\leftarrow A_3 \cdot P_7 (P_3)$

7.2 Input and Output Instructions

- IN A, P_p

① Instruction Code :

1 1 1 1	P_4 1	1 P_2 P_1 P_0

② Number of Cycles: 1

③ Function : (A) ← (P_p) p = 00 to 02,10 to 12 (μPD6124A, 6600A, 61P24)
p = 00 to 03,10 to 13 (μPD6125A)
p = 00 to 04,10 to 14 (μPD6126A)

Loads (reads) the data in port P_p in (to) the accumulator.
CARRY ← 0

- OUT P_p, A

① Instruction Code :

0 0 1 0	P_4 1	1 P_2 P_1 P_0

② Number of Cycles: 1

★ ③ Function : (P_p) ← (A) p = 00 to 02,10 to 12 (μPD6124A, 6600A, 61P24)
p = 00 to 03,10 to 13 (μPD6125A)
p = 00 to 04,10 to 14 (μPD6126A)

Transfers the contents of the accumulator to port P_p and latches them.

- ANL A, P_p

① Instruction Code :

1 1 0 1	P_4 1	1 P_2 P_1 P_0

② Number of Cycles: 1

★ ③ Function : (A) ← (A) $\wedge$ (P_p) p = 00 to 02,10 to 12 (μPD6124A, 6600A, 61P24)
p = 00 to 03,10 to 13 (μPD6125A)
p = 00 to 04,10 to 14 (μPD6126A)

Takes the logical product of the contents of the accumulator and the contents of P_p and loads the results in the accumulator.
CARRY ← $A_3 \cdot D_3$

- ORL A, P_p

① Instruction Code :

1 1 1 0	P_4 1	1 P_2 P_1 P_0

② Number of Cycles: 1

★ ③ Function : (A) ← (A) $\vee$ (P_p) p = 00 to 02,10 to 12 (μPD6124A, 6600A, 61P24)
p = 00 to 03,10 to 13 (μPD6125A)
p = 00 to 04,10 to 14 (μPD6126A)

Takes the logical sum of the contents of the accumulator and the contents of Pp and loads the results in the accumulator.
CARRY ← 0

- XRL A, P_p

① Instruction Code :

1 0 1 0	P_4 1	1 P_2 P_1 P_0

② Number of Cycles: 1

★ ③ Function : (A) ← (A) ⊻ (P_p) p = 00 to 02,10 to 12 (μPD6124A, 6600A, 61P24)
p = 00 to 03,10 to 13 (μPD6125A)
p = 00 to 04,10 to 14 (μPD6126A)

Takes the exclusive OR of the contents of the accumulator and the contents of P_p and loads the results in the accumulator.

CARRY ← $A_3 \cdot D_3$

- OUT P_p, #data

① Instruction Code :

0 0 1 1	0 1	1 P_2 P_1 P_0

d_9	d_7 d_6 d_5 d_4	d_8	d_3 d_2 d_1 d_0

② Number of Cycles: 1

★ ③ Function : P_p ← data p = 0 to 2 (μPD6124A, 6600A, 61P24A)
p = 0 to 3 (μPD6125A)
p = 0 to 4 (μPD6126A)

Transfers immediate data to P_p. In this case, P_p operates as the pair P_{1p} to P_{0p}.

7.3 Branch Instructions

- JMP0 address

① Instruction Code :

0 1 0 0	0 1	0 0 0 1

a_9	a_7 a_6 a_5 a_4	a_8	a_3 a_2 a_1 a_0

② Number of Cycles: 1

③ Function : $(PC_{9-0}) \leftarrow a_{9-0}$

Replaces the 10-bit (PC_{9-0}) of the program counter with directly specified address a_9 to a_0.

In the μPD612x Series, JMP1 to JMP3 are kept for easing debugging operations. However, the ROM capacity in the μPD6124A, 6125A, 6126A, 6600A and 61P24 is 1002 steps or less, and as a result, in the actual product, JMP1, JMP2 and JMP3 cannot be used, so exercise caution.

When jumping to pages 1, 2 or 3 using the JMP1, JMP2 or JMP3 command, provided for debugging, if the table reference command (MOV R_r @RO) is executed in the page 1, 2 or 3 area, it refers to the contents of the specified address in page 0.

JMP 1	0 1 0 0	1 1	0 0 0 1
JMP 2	0 1 0 1	0 1	0 0 0 1
JMP 3	0 1 0 1	1 1	0 0 0 1

- JC address

① Instruction Code :

0 1 1 0	0 1	0 0 0 1

a_9	a_7 a_6 a_5 a_4	a_8	a_3 a_2 a_1 a_0

② Number of Cycles: 1

③ Function : $(PC_{9-0}) \leftarrow a_{9-0}$ If C = 1
$(PC) \leftarrow (PC) + 2$ If C = 0

Jumps to the address specified in a_9 to a_0 if "1" is set in the carry flag.

- JNC address

① Instruction Code :

0 1 1 0	1 1	0 0 0 1

a_9	a_7 a_6 a_5 a_4	a_8	a_3 a_2 a_1 a_0

② Number of Cycles: 1

③ Function : $(PC_{9-0}) \leftarrow a_{9-0}$ If C = 0
$(PC) \leftarrow (PC) + 2$ If C = 1

Jumps to the address specified in a_9 to a_0 if "0" is reset in the carry flag.

- JF address

① Instruction Code :

0 1 1 1	0 1	0 0 0 1

a_9	a_7 a_6 a_5 a_4	a_8	a_3 a_2 a_1 a_0

② Number of Cycles: 1

③ Function : $(PC_{9-0}) \leftarrow a_{9-0}$ If F = 1

$(PC) \leftarrow (PC) +2$ If F = 0

Jumps to the address specified in a_9 to a_0 if "1" is set in the status flag.

- JNF address

① Instruction Code :

0 1 1 1	1 1	0 0 0 1

a_9	a_7 a_6 a_5 a_4	a_8	a_3 a_2 a_1 a_0

② Number of Cycles: 1

③ Function : $(PC_{9-0}) \leftarrow a_{9-0}$ If F = 0

$(PC) \leftarrow (PC) +2$ If F = 1

Jumps to the address specified in a_9 to a_0 if "0" is reset in the status flag.

- JMP0 Rr

① Instruction Code :

0 1 0 0	0 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

★ ③ Function : $(PC_{9-0}) \leftarrow (R_{1r}\text{-}R_{0r})$ r = 1 to F

Replaces the 10-bit of the program counter ($PC_{9\text{-}0}$) with the contents of the pair register R_{1r} to R_{0r}.

When this command is executed, R_{1r} to R_{0r} become 10-bit.

However, after an accumulator operation command has been executed, R_9 and R_8 become "0," so exercise caution.

Ordinarily, the register operates in 4-bit units.

Example Before Execution

	R_{11}	R_{01}
R_{11} to R_{01}	R_9 R_7 R_6 R_5 R_4	R_8 R_3 R_2 R_1 R_0

Acc

0 0 0 0

ORL A, R_{11}

MOV R_{11}, A

→

0 R_7 R_6 R_5 R_4	R_{11} After execution

ORL A, R_{01}

MOV R_{01}, A

→

0 R_3 R_2 R_1 R_0	R_{01} After execution

★ Caution **JMP0 R_0 cannot be used.**

- JC R_r

  ① Instruction Code : | 0 1 1 0 | 0 0 | R_3 R_2 R_1 R_0 |

  ② Number of Cycles: 1

★ ③ Function : $(PC_{9-0}) \leftarrow (R_{1r}$ to $R_{0r})$ r = 1 to F If C = 1

  $(PC) \leftarrow (PC) +1$ If C = 0

  The contents of the program counter (PC_{9-0}) are replaced by the contents of the pair register R_{1r} to R_{0r} if the carry flag is set to "1."

★ **Caution JC R_0 cannot be used.**

- JNC R_r

  ① Instruction Code : | 0 1 1 0 | 1 0 | R_3 R_2 R_1 R_0 |

  ② Number of Cycles: 1

★ ③ Function : $(PC_{9-0}) \leftarrow (R_{1r}$ to $R_{0r})$ r = 1 to F If C = 0

  $(PC) \leftarrow (PC) +1$ If C = 1

  The contents of the program counter (PC_{9-0}) are replaced by the contents of the pair register R_{1r} to R_{0r} if the carry flag is reset to "0."

★ **Caution JNC R_0 cannot be used.**

- JF R_r

  ① Instruction Code : | 0 1 1 1 | 0 0 | R_3 R_2 R_1 R_0 |

  ② Number of Cycles: 1

★ ③ Function : $(PC_{9-0}) \leftarrow (R_{1r}$ to $R_{0r})$ r = 1 to F If F = 1

  $(PC) \leftarrow (PC) +1$ If F = 0

  The contents of the program counter (PC_{9-0}) are replaced by the contents of the pair register R_{1r} to R_{0r} if the status flag is set to "1."

★ **Caution JF R_0 cannot be used.**

- JNF Rr

  ① Instruction Code : | 0 1 1 1 | 1 0 | R_3 R_2 R_1 R_0 |

  ② Number of Cycles: 1

★ ③ Function : $(PC_{9-0}) \leftarrow (R_{1r}$ to $R_{0r})$ r = 1 to F If F = 0

  $(PC) \leftarrow (PC) +1$ If F = 1

  The contents of the program counter (PC_{9-0}) are replaced by the contents of the pair register R_{1r} to R_{0r} if the status flag is reset to "0."

★ **Caution JNF R_0 cannot be used.**

7.4 Subroutine Instructions

- CALL0 address

① Instruction Code :

0 0 1 1	0 1	0 0 1 0

0 1 0 0	0 1	0 0 0 1

a_9	a_7 a_6 a_5 a_4	a_8	a_3 a_2 a_1 a_0

② Number of Cycles: 2

③ Function : ((SP)) ← (PC) +1
(SP) ← (SP) +1
(PC_{9-0}) ← a_{9-0}

The contents of the program counter are incremented (+1) and that value is saved in the stack specified by the stack pointer. Next, the contents of the stack pointer are incremented (+1) and the subroutine in the address specified in a_9 to a_0 is called.

- RET

① Instruction Code :

0 1 0 0	0 1	0 0 1 0

② Number of Cycles: 1

③ Function : (SP) ← (SP) −1
(PC) ← ((SP)) +2

The contents of the stack pointer are decremented. Next the contents of the stack specified by this stack pointer are incremented (+2) and that value is returned to the program counter.

Caution **Subroutine instructions making the debugging operation easier, just like the JMP instructions of the branch instructions, so the CALL1, CALL2 and CALL3 commands are provided. However, in the actual product, commands other than CALL0 cannot be used.**
When jumping to page areas 1, 2 and 3 using the CALL1, CALL2 or CALL3 command, provided for debugging, if the table reference command (MOV R_r, @RO) is executed, it refers to the contents of the specified address in page 0.

7.5 Data Transfer Instructions

- MOV A, R_r

① Instruction Code :

1 1 1 1	R_4 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

③ Function : $(A) \leftarrow (R_r)$ r = 00 to 0F 10 to 1F

Transfers the contents of register R_r to the accumulator. If there are 5-bit data in the register, the MSB is disregarded.

CARRY ← 0

- MOV A, @R_0H

① Instruction Code :

1 1 1 1	0 1	0 0 0 0

② Number of Cycles: 1

③ Function : $(A) \leftarrow ((P_{11}, R_{10} \text{ to } R_{00}))$

Transfers the higher 4-bit of the program memory (P_7, P_6, P_5, P_4) specified in control register P_{11} and pair register R_{10} to R_{00}. P_9 is disregarded.

CARRY ← 0

- MOV A, @R_0L

① Instruction Code :

1 1 1 1	1 1	0 0 0 0

② Number of Cycles: 1

③ Function : $(A) \leftarrow ((P_{11}, R_{10} \text{ to } R_{00}))$

Transfers the lower 4-bit of the program memory (P_3, P_2, P_1, P_0) specified in control register P_{11} and pair register R_{10} to R_{00}. P_8 is disregarded.

Remark Program Memory Contents

	R_0H		R_0L
P_9	P_7 P_6 P_5 P_4	P_8	P_3 P_2 P_1 P_0

CARRY ← 0

- MOV A, #data

① Instruction Code :

1 1 1 1	1 1	0 0 0 1

0	0 0 0 0	0	d_3 d_2 d_1 d_0

② Number of Cycles: 1

③ Function : $(A) \leftarrow$ data

Transfers the immediate data to the accumulator.

CARRY ← 0

- MOV R_r, A

① Instruction Code :

0 0 1 0	R_4 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

③ Function : $(R_r) \leftarrow (A)$ r = 00 to 0F 10 to 1F

Transfers the contents of the accumulator to register R_r.

- MOVE R_r, #data

① Instruction Code :

0 0 1 1	0 0	R_3 R_2 R_1 R_0

d_9	d_7 d_6 d_5 d_4	d_8	d_3 d_2 d_1 d_0

② Number of Cycles: 1

③ Function : $(R_{1r}$ to $R_{0r}) \leftarrow$ data r = 0 to F data = 000H to 3FFH

Transfers immediate data to the register. When this command is used, each register operates as a pair register.

Combinations which become pairs are as shown below.

R_{10} to R_{00}

R_{11} to R_{01}

⋮

⋮

⋮

R_{1E} to R_{0E}

R_{1F} to R_{0F}

Higher Digit Lower Digit

When this command is executed, registers are treated as 10-bit, but if an accumulator operation command is executed, d_9 or d_8 becomes "0."

- MOV R_r, @R_0

① Instruction Code :

0 0 1 1	1 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

③ Function : $(R_{1r}$ to $R_{0r})$ ($(P_{11}$, R_{10} to $R_{00})$) r = 0 to F

Transfers the contents of the program memory specified in control register P11 and the contents of program memory specified in pair register R_{10} to R_{00} to pair register R_{1r} to R_{0r}. Program memory is configured in 10-bit and is in the following state after transfer to the register.

Program Memory

P_9	P_7 P_6 P_5 P_4	P_8	P_3 P_2 P_1 P_0

R_0

→

P_9	P_7 P_6 P_5 P_4	P_8	P_3 P_2 P_1 P_0
← R_{1r} →		← R_{0r} →	

The higher 2-bit of the program memory address are specified in the control register.

Caution When this command is executed, the register is treated as 5-bit, but in an accumulator operation command, only the lower 4-bit are valid, and if there is a transfer from the accumulator to the register, the MSB (5th bit) always becomes "0."
If this command is executed in page 1, 2 or 3 of the debugging area, the content at the specified address in the page 0 area are transferred.

7.6 Timer/Counter Operating Instructions

- MOV A, T_t

① Instruction Code : | 1 1 1 1 | t 1 | 1 1 1 1 |

② Number of Cycles: 1

③ Function : (A) ← (T_t) t = 0,1

Transfers the contents of timer T_t to the accumulator. T_1 corresponds to (t_9, t_8, t_7, t_6) and T_0 corresponds to (t_5, t_4, t_3, t_2).

t_9 t_8 t_7 t_6	t_5 t_4 t_3 t_2	t_1 t_0
T_1	T_0	Can be set by # data, @R_0.

CARRY ← 0

- MOV T, # data

① Instruction Code : | 0 0 1 1 | 0 1 | 1 1 1 1 |

t_1	t_9 t_8 t_7 t_6	t_0	t_5 t_4 t_3 t_2

② Number of Cycles: 1

③ Function : T ← data

Transfers immediate data to the timer register T_1 to T_0 to t_1, t_0.

Remark Timer operation stops at (set value (HEX) +1) × 8/f_{osc}.

- MOV T, @R_0

① Instruction Code : | 0 0 1 1 | 1 1 | 1 1 1 1 |

② Number of Cycles: 1

③ Function : (T_1 to T_0) ← ((P_{11}, R_{10} to R_{00}))

Transfers the contents of program memory specified in control register P_{11} and pair register R_{10} to R_{00} to timer register T_1 to T_0 to t_1, t_0. The higher 2-bit of program memory are specified in the control register.

Program Memory (R_0)

t_1	t_9 t_8 t_7 t_6	t_0	t_5 t_4 t_3 t_2

→ Timer

t_9 t_8 t_7 t_6	t_5 t_4 t_3 t_2	t_1 t_0
T_1	T_0	

- MOV T_t, A

① Instruction Code : | 0 0 1 0 | t 1 | 1 1 1 1 |

② Number of Cycles: 1

③ Function : $(T_t) \leftarrow (A)$ t=0,1

Transfers the contents of the accumulator to the timer register T_t. T_1 corresponds to (t_9, t_8, t_7, t_6) and T_0 corresponds to (t_5, t_4, t_3, t_2). If there is a transfer to T_t after this command is executed, t_1 becomes 0, and if there is a transfer to T_0 after this command is executed, t_0 becomes 0.

7.7 Others

- HALT #data

① Instruction Code :

0 0 0 1	0 1	0 0 0 1

0	0 0 0 0	0	d_3 d_2 d_1 d_0

② Number of Cycles: 1

③ Function : HALT ← data

Sets the CPU in the standby mode.

Standby mode cancellation conditions are specified by the immediate data.

- SCAF (Set Carry If Acc = F_H)

① Instruction Code :

1 1 0 1	0 1	0 0 1 1

② Number of Cycles: 1

③ Function : Carry ← If Acc = F_H

Sets the carry flag (C) to "1" if the contents of the accumulator are F_H.

The value of the accumulator is indefinite after the SCAF command is executed.

- STTS R_{0r}

① Instruction Code :

0 0 0 1	1 0	R_3 R_2 R_1 R_0

② Number of Cycles: 1

③ Function : STATUS ← (R_{0r}) r = 0 to F

Compares the status of S-IN, $K_{I/O}$, K_I, I/O and the timer with the contents of register R_{0r}, and if the set bit matches with at least one status, it sets the status flag (F) to "1."

- STTS #data

① Instruction Code :

0 0 0 1	1 1	0 0 0 1

0	0 0 0 0	0	d_3 d_2 d_1 d_0

② Number of Cycles: 1

③ Function : STATUS ← data

Compares the status of S-IN, $K_{I/O}$, K_I, I/O and the timer with the contents of immediate data, and if the set bit matches with at least one status, it sets the status flag (F) to "1."

- NOP
  - ① Instruction Code : | 0 0 0 0 | 0 0 | 0 0 0 0 |
  - ② Number of Cycles: 1
  - ③ Function : (PC) ← (PC) +1

    Watchdog timer capacitor operation
    Starts discharge.
    Charge within 5 ms. (However, when C = 0.1 μ or less)

    NOP + HALT
    Watchdog timer capacitor operation
    Starts charging.
    Carry out 23 steps or higher charging.

- Contents of Carry Flag (C)

  After the command is executed, the contents of the carry flag become as shown below.

XRL	→ $A_3 \cdot D_3$	INC A	→ CARRY
ORL	→ = 0	SCAF	→ CARRY
ANL	→ $A_3 \cdot D_3$	RL A	→ A_3
MOV A, X	→ = 0	IN A, P_p	→ 0

X: R_r, @R_0H/L, #data,T_t

7.8 Mnemonic ↔ Machine Language Correspondence Table

Accumulator Operation Instructions

R_r	—	R_{10}	R_{11}	R_{12}	- - -	R_{1F}	R_{00}	R_{01}	- - -	R_{0F}
ANL A,R_r		D00	D01	D02		D0F	D20	D21		D2F
ANL A,@R_0H	D10									
ANL A,@R_0L	D30									
ANL A,#data	D31									
ORL A,R_r		E00	E01	E02		E0F	E20	E21		E2F
ORL A,@R_0H	E10									
ORL A,@R_0L	E30									
ORL A,#data	E31									
XRL A,R_r		A00	A01	A02		A0F	A20	A21		A2F
XRL A,@R_0H	A10									
XRL A,@R_0L	A30									
XRL A,#data	A31									
INC A	A13									
RL A	F13									

Input/Output Instructions

P_p Note	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	P_{00}	P_{01}	P_{02}	P_{03}	P_{04}
IN A, P_p	F18	F19	F1A	F1B	F1C	F38	F39	F3A	F3B	F3C
OUT P_p, A	218	219	21A	21B	21C	238	239	23A	23B	23C
ANL A, P_p	D18	D19	D1A	D1B	D1C	D38	D39	D3A	D3B	D3C
ORL A, P_p	E18	E19	E1A	E1B	E1C	E38	E39	E3A	E3B	E3C
XRL A, P_p	A18	A19	A1A	A1B	A1C	A38	A39	A3A	A3B	A3C

Note μPD6124A, 6600A, 61P24: p = 00 to 02, 10 to 12
μPD6125A : p = 00 to 03, 10 to 13
μPD6126A : p = 00 to 04, 10 to 14

P_p Note	P_0	P_1	P_2	P_3	P_4
OUT P_p, #data	318	319	31A	31B	31C

P_{1p} to P_{0p} operate as a pair.

Note μPD6124A, 6600A, 61P24: p = 0 to 2
μPD6125A : p = 0 to 3
μPD6126A : p = 0 to 4

Data Transfer Instructions

R_r		R_{10}	R_{11}	R_{12}	R_{1F}	R_{00}	R_{01}	R_{0F}
MOV A,R_r		F00	F01	F02	F0F	F20	F21	F2F
MOV A,@R_0H	F10							
MOV A,@R_0L	F30							
MOV A,#data	F31							
MOV R_r, A		200	201	202	20F	220	221	22F

R_r		R_0	R_1	R_2	R_F
MOV R_r, #data		300	301	302	30F
MOV R_r,@R_0		320	321	322	32F

R_{1r} to R_{0r} operate as a pair register.

Branch Instructions

R_r	—	R_0	R_1	R_2	R_F
JMP0 addr	411				
★ JMP0 R_r Note	—	—	401	402	40F
JC addr	611				
JC R_r Note	—	—	601	602	60F
JNC addr	631				
JNC R_r Note	—	—	621	622	62F
JF addr	711				
JF R_r Note	—	—	701	702	70F
JNF addr	731				
JNF R_r Note	—	—	721	722	72F

← Pair Register

★ **Note** r = 1 – F
r = 0 cannot be used.

Subroutine Instructions

CALL0 addr	312	411
RET	412	

Timer/Counter Operating Instructions

T_i	T_{0-1}	T_1	T_0
MOV A, T_i	—	F1F	F3F
MOV T_i, A		21F	23F
MOV T,#data	31F		
MOV T,@R_0	33F		

Others

		R_{00}	R_{01}	R_{02}	R_{0F}
HALT #data	111				
STS R_{0r}		120	121	122	12F
STTS #data	131				
SCAF	D13				
NOP	000				

CHAPTER 8 MASK OPTION (PLA DATA)

8.1 μPD6124A, 6125A, 6126A, 6600A

The following items can be selected by switching the mask option.

(1) K_I, I/O_0, I/O_1, S-IN pull-down resistors present or not.
(2) Switching the carrier duty when the clock is $f_{osc}/12$ (1/2, 1/3)
(3) Runaway detection specification

Mask option data are registered after the object code.

Remarks The following items are already specified in the μPD6124A, 6125A, 6126A and 6600A.
(1) Pull down resistors at all pins of $K_{I/O}$.
(2) HALT cancellation sensing is specified for all bits of each port.
(3) The watchdog timer is valid.

Table 8-1. Switch Change Bit Deallocation (μPD6124A, 6125A, 6126A, 6600A) (1/2)

★ **(1) μPD6124A, 6600A**

<table>
<tr><th rowspan="2">Address</th><th rowspan="2">Correspondence</th><th colspan="7">MSB</th><th>LSB</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>K_I
Pull-down resistor</td><td>K_{I3}</td><td>K_{I2}</td><td>K_{I1}</td><td>K_{I0}</td><td colspan="4">0</td></tr>
<tr><td>1</td><td>Duty
S-IN</td><td>0</td><td>0</td><td>0</td><td>Duty
Change</td><td>0</td><td>0</td><td>S-IN Pull
Down
Resistor</td><td>0</td></tr>
<tr><td>2</td><td>Runaway detection</td><td>$K_{I/O}$
ALL</td><td>HALT
S-IN</td><td>HALT
$K_{I/O}$</td><td>HALT
K_I</td><td colspan="4">0</td></tr>
</table>

Table 8-1. Switch Change Bit Deallocation (μPD6124A, 6125A, 6126A, 6600A) (2/2)

(2) μPD6125A, 6126A

Address	Correspondence	MSB 7	6	5	4	3	2	1	0 LSB
0	K_I Pull-down resistor	K_{I0}	K_{I1}	K_{I2}	K_{I3}	0			
1	Duty S-IN	0	0	0	Duty change	0	0	S-IN Pull-down resistor	0
2	Runaway detection	$K_{I/O}$ ALL	HALT S-IN	HALT $K_{I/O}$	HALT K_I	HALT I/O_0	HALT I/O_1	I/O_0 ALL	I/O_1 ALL
3	I/O_0 Pull-down resistor	I/O_{00}	I/O_{01}	I/O_{02}	I/O_{03}	0			
4	I/O_1 Pull-down resistor Note	I/O_{10} Note	I/O_{11} Note	I/O_{12} Note	I/O_{13} Note	0			

Note In the μPD6125A, there are no I/O_{10} to I/O_{13} pins.

Switching for Data

(1) Pull-down resistor

When 0 ... None (OFF)
When 1 ... Yes (ON)

(2) Modulation duty (when $f_{osc}/12$)

When 0 ... 1/2 Duty
When 1 ... 1/3 Duty

(3) Runaway detection

① **$K_{I/O}$ ALL, I/O_0 ALL, I/O_1 ALL**

If the runaway detection $K_{I/O}$ ALL (I/O_0 ALL, I/O_1 ALL) switch is set to ON (set to 1) through the mask option, if there is an oscillator stop HALT (STOP Mode), the system is reset (AC pin changes to discharge mode) when the $K_{I/O}$ (I/O_0, I/O_1) terminal is in the input mode or even one pin of $K_{I/O}$ (I/O_0, I/O_1) is at the low level.
When 0 ... No reset function (OFF)
When 1 ... Reset function (ON)

Caution If these pins are used as the key source of a key matrix, be sure to turn the switch on with the mask option.

② **HALT Cancellation Condition Specification (S-IN, $K_{I/O}$, K_I)**

The system is reset if "mask option not used" specification condition exists when in the HALT mode state.

When 0 Used

When 1 Not Used

Caution For the "not used" cancellation condition HALT Mode, be sure to set "Not Used."

Remark When selecting the μPD6125A and 6126A, if "HALT #00E" (ready for K_I, I/O_0, I/O_1 key input) is used, set HALT S-IN, HALT $K_{I/O}$, HALT K_I, HALT I/O_0, HALT I/O_1 all on not used. "HALT #00E" can be used only in the case that the μPD6125A or 6126A is selected.

An example of setting of mask option data is shown below.

Examples 1. If the following items are selected with the μPD6124A or μPD6600A,

- Pull-down resistors on all K_I pins
- Carrier duty 1/3
- Pull-down resistor on S-IN
- $K_{I/O}$ ALL "H" reset function
- HALT K_I used
- HALT S-IN, HALT $K_{I/O}$ Not used

PLA data are as follows.

```
        PLA
KEY  :  DB    0F0H
DUTY :  DB    12H
HALT :  DB    0E0H
        END
```

2. If the following items are selected with the μPD6125A,

- Pull-down resistors on all K_I pins
- Carrier duty 1/3
- Pull-down resistor on S-IN
- $K_{I/O}$ ALL "H" reset function
- No I/O_0 ALL "H" reset function
- HALT S-IN, HALT $K_{I/O}$, HALT K_I, HALT I/O_0 not used [Note]
- Pull-down resistors on all I/O_0 pins

PLA data are as follows.

```
        PLA
KEY  :  DB   0F0H
DUTY:   DB   12H
HALT :  DB   0F8H Note
I/O0 :  DB   0F0H
        END
```

Note When the μPD6125A is selected, if "HALT #00E" (ready for K_I, I/O_0 key input) is used, set HALT S-IN, HALT $K_{I/O}$ HALT K_I and HALT I/O_0 all on Not Used.

3. If the following items are selected with the μPD6126A
   - Pull-down resistors on all K_I pins
   - Carrier duty 1/2
   - Pull-down resistor on S-IN
   - No $K_{I/O}$ ALL "H" reset function
   - I/O_0 ALL "H," I/O_1 ALL "H" reset function
   - HALT K_I used Note
   - HALT S-IN, HALT $K_{I/O}$, , HALT I/O_0, , HALT I/O_1 not used Note
   - Pull-down resistors on all I/O_0 pins.
   - Pull-down resistors on all I/O_1 pins.

   PLA data are as follows.

```
        PLA
KEY  :  DB   0F0H
DUTY:   DB   02H
HALT :  DB   6FH Note
I/O0 :  DB   0F0H
I/O1 :  DB   0F0H
        END
```

Note When the μPD6126A is selected, if "HALT #00E" (ready for K_I, I/O_0, I/O_1 key input) is used, set HALT S-IN, HALT $K_{I/O}$ HALT K_I and HALT I/O_0 and HALT I/O_1 all on Not Used.

★ 8.2 μPD61P24

For the μPD61P24, the following fixed mask options are provided.

(1) Pull down resistors on K_I and S-IN pins.

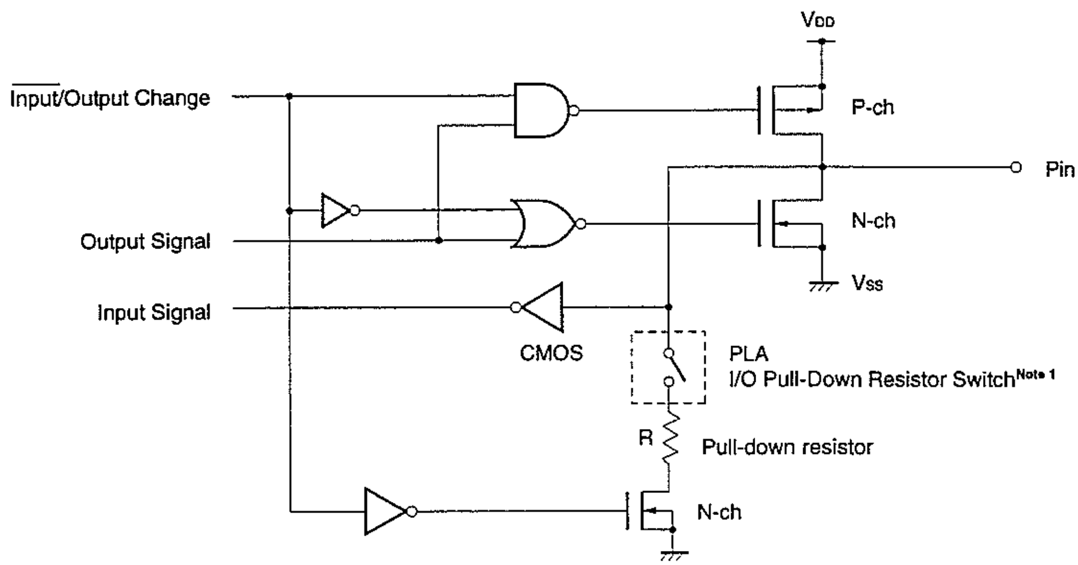
(2) Carrier duty when the clock speed is $f_{osc}/12$ is changed (1/3).

(3) Runaway check is included ($K_{I/O}$ ALL, HALT S-IN, HALT $K_{I/O}$)

★ **Table 8-2. Switch Change Bit Deallocation (μPD61P24)**

<table>
<tr><th rowspan="2">Address</th><th rowspan="2">Correspondence</th><th colspan="8">MSB LSB</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">K_I
Pull-down resistor</td><td>K_{I3}</td><td>K_{I2}</td><td>K_{I1}</td><td>K_{I0}</td><td colspan="4" rowspan="2">0</td></tr>
<tr><td>1
Provided</td><td>1
Provided</td><td>1
Provided</td><td>1
Provided</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">Duty
S-IN</td><td rowspan="2">0</td><td rowspan="2">0</td><td rowspan="2">0</td><td>Duty</td><td rowspan="2">0</td><td rowspan="2">0</td><td>S-IN
Pull-down
resistor</td><td rowspan="2">0</td></tr>
<tr><td>1
1/3 Duty</td><td>1
Provided</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">Runaway detection</td><td>$K_{I/O}$
ALL</td><td>HALT
S-IN</td><td>HALT
$K_{I/O}$</td><td>HALT
K_I</td><td colspan="4" rowspan="2">0</td></tr>
<tr><td>1
Detection</td><td>1
Not used</td><td>1
Not used</td><td>0
Detection</td></tr>
</table>

8.3 KI/O, I/O Pull-Down Resistor Configuration Diagram



If the I/O pin Note 2 pull-down resistor switch is set to ON (set to 1) through the mask option, the pull down resistor R is turned ON only when in the input mode.

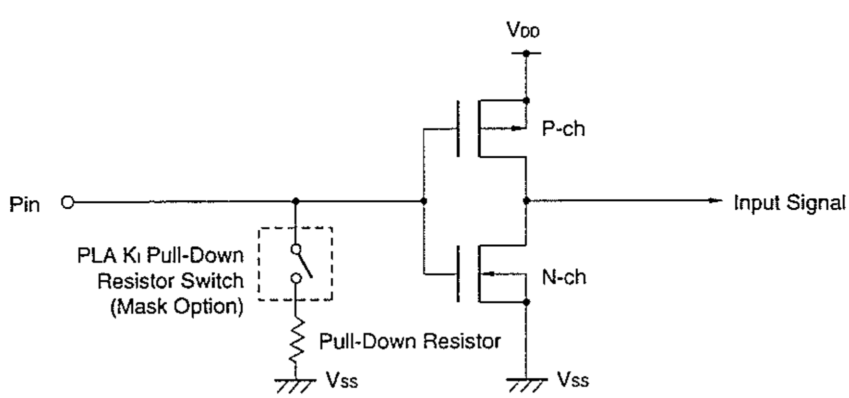
If the pin is used as a key switch, turn the pull-down resistor switch ON through the mask option.

If the KI/O pin is set in the input mode, the pull-down resistor R is turned ON.

Notes 1. There is no pull-down resistor switch on the KI/O pin.

2. There is no I/O port in the μPD6124A, 6600A or 61P24.

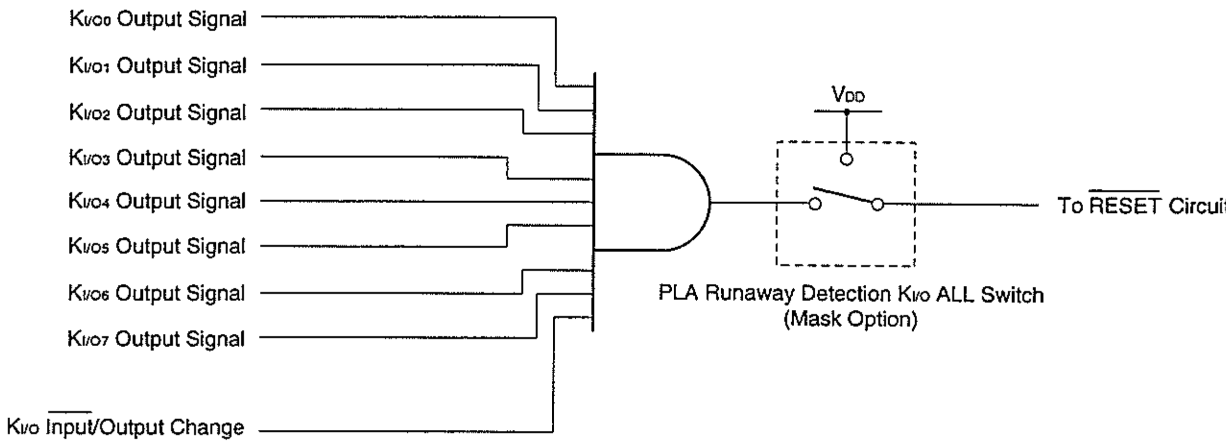
8.4 KI Pull-Down Resistor Configuration Diagram



If the KI pin's pull-down resistor switch is set to ON (set to 1) through the mask option, the pull-down resistor R is turned ON.

If the terminal is used as a key switch, turn the pull-down resistor switch ON through the mask option.

8.5 Runaway Detection $K_{I/O}$ ALL (I/O_0 ALL, I/O_1 ALL) Configuration Diagram

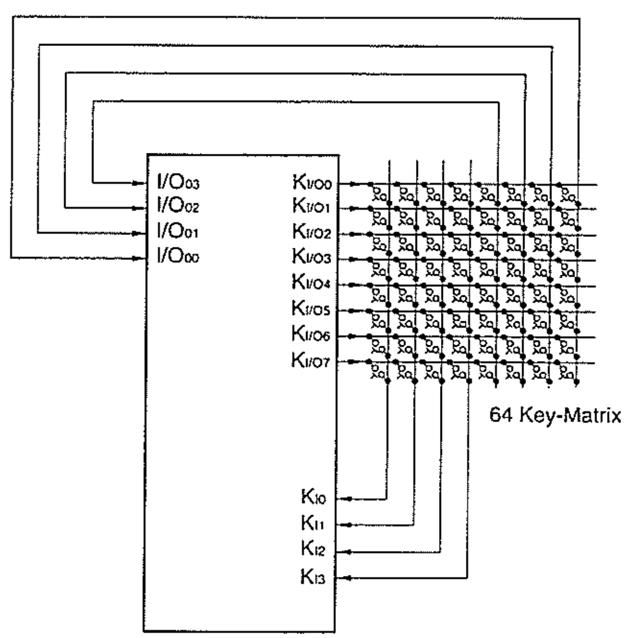


If the runaway detection $K_{I/O}$ ALL (I/O_0 ALL, I/O_1 ALL) switch is set to ON (set to 1) through the mask option, if there is an oscillator stop HALT (STOP Mode), the system is reset (AC pin changes to discharge mode) when the $K_{I/O}$ (I/O_0, I/O_1) terminal is in the input mode or even one pin of $K_{I/O}$ (I/O_0, I/O_1) is at the low level.

If this terminal is used as the key source of a key matrix, turn the switch ON through the mask option (same with I/O_0 ALL and I/O_1 ALL).

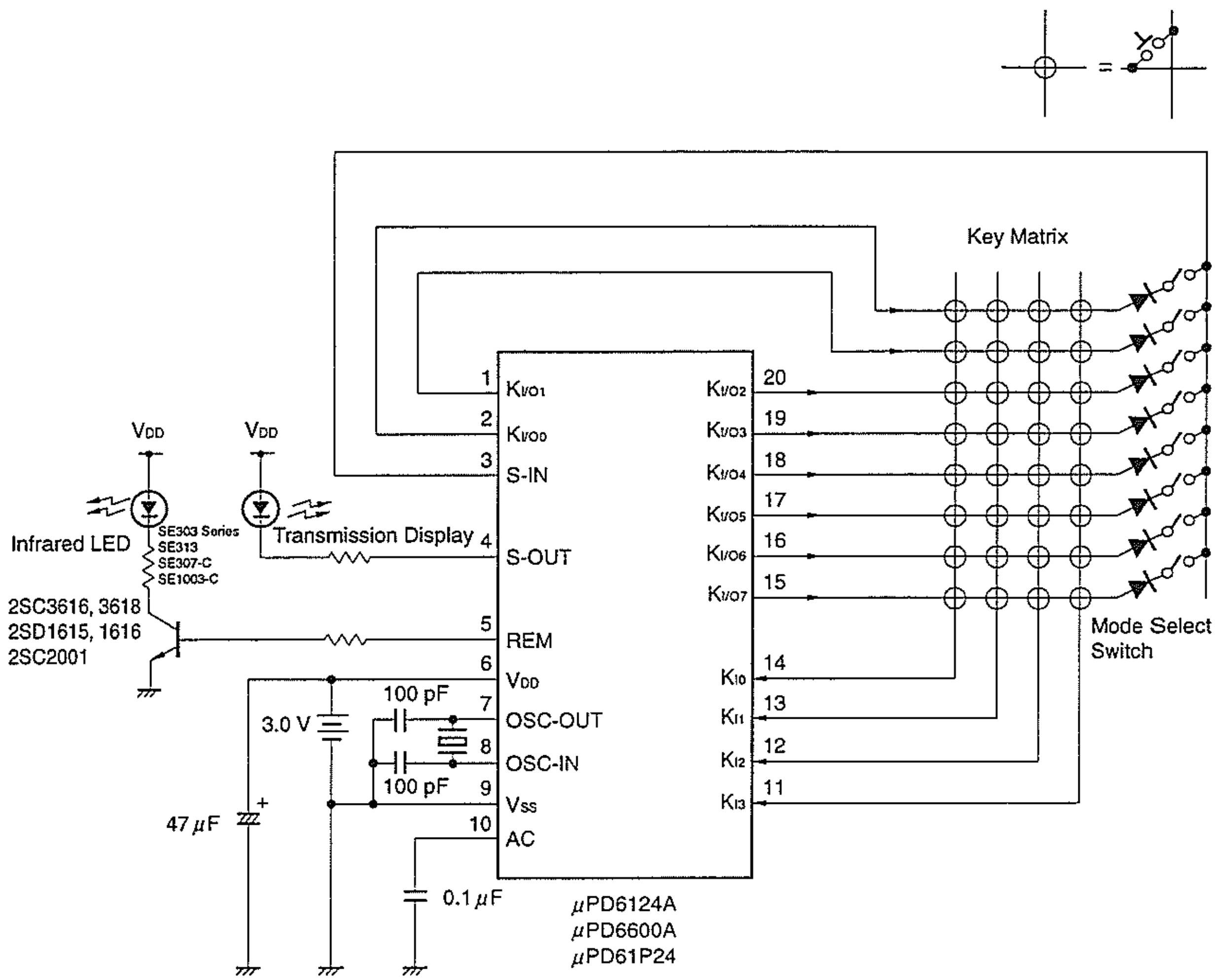
For example, if the circuit is configured as shown in the following figure, and $K_{I/O}$ is used as the source, during a ready for key input oscillation stop HALT (STOP Mode), ordinarily all the pins of $K_{I/O}$ are in the output mode and are set at the high level. At this time, if power supply fluctuations occur due to the influence of chattering, of the battery holder, etc., and $K_{I/O}$ switches to the input mode or $K_{I/O}$ output is inverted, inputs to the K_I and I/O pins do not enter and it becomes impossible to cancel HALT, or the IC seems from outward appearances not to be functioning at all. To avoid this state, either input the low level to the reset pin (AC pin) or disconnect and reconnect the battery, then carry out a power on reset.

If this runaway detection $K_{I/O}$ ALL switch is set to ON through the mask option, the device can be reset when there is a runaway condition such as described above.



[MEMO]

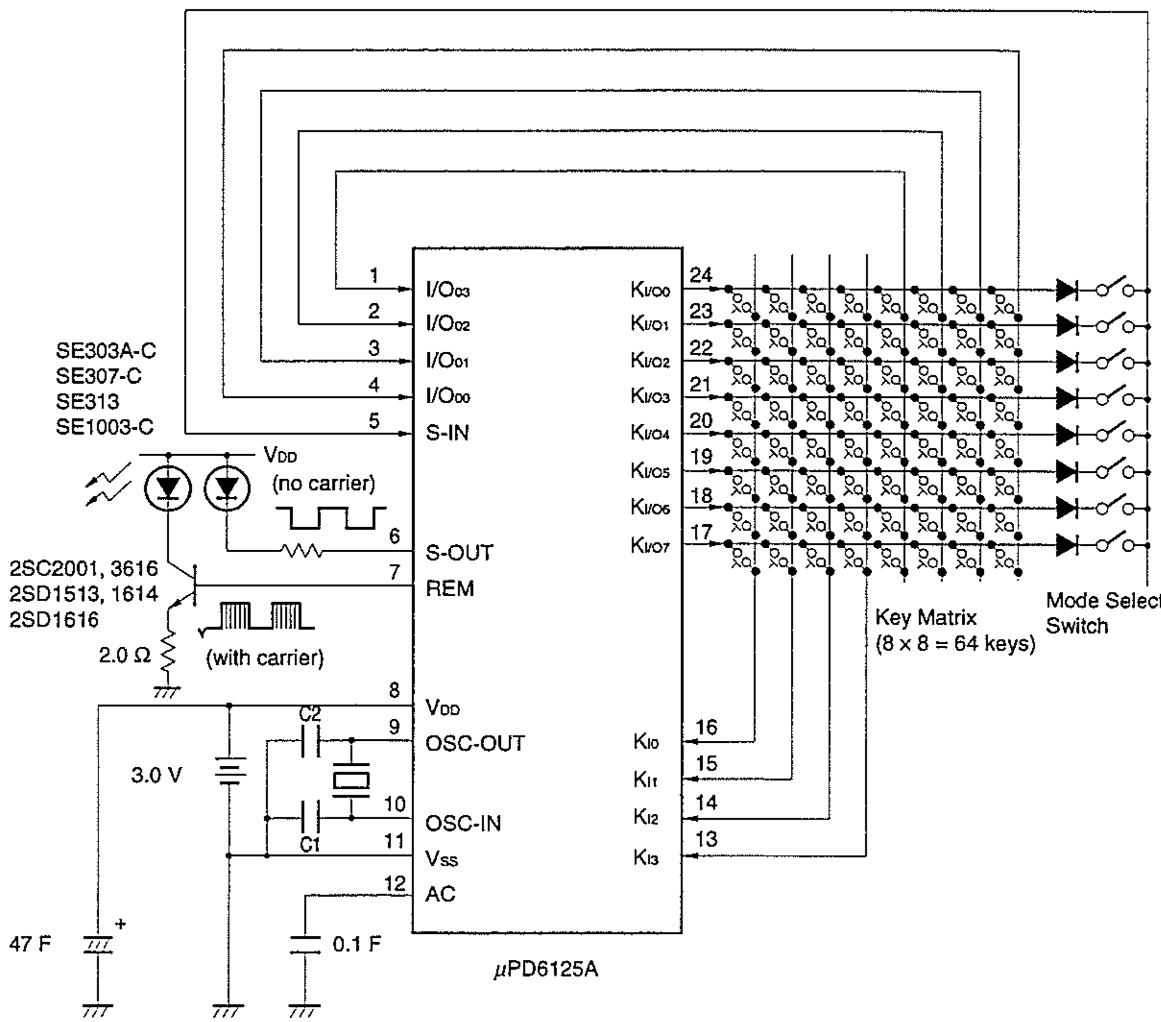
★ 9.1 μPD6124A, 6600A, 61P24



Caution **The value of the capacitor for starting the ceramic oscillator needs to be set after consideration of the voltage level it is going to be used at and the starting characteristics of the ceramic oscillator.**

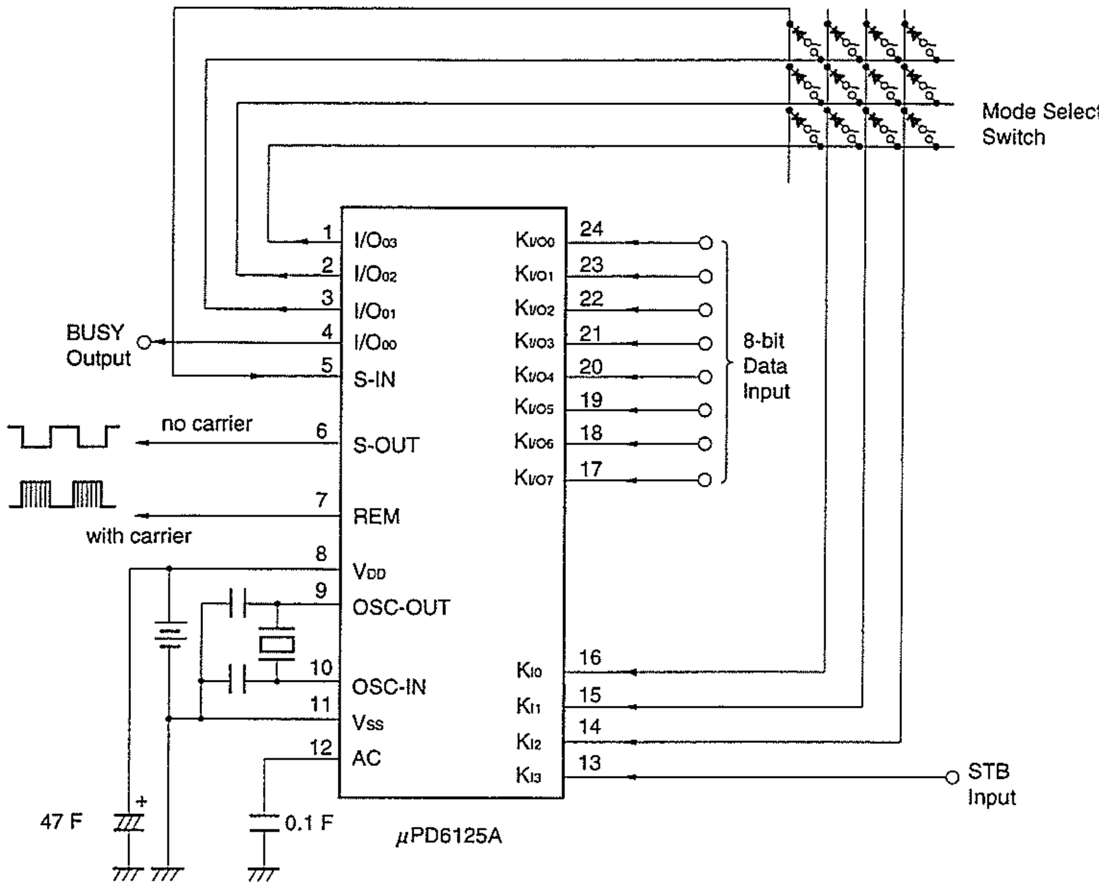
9.2 μPD6125A

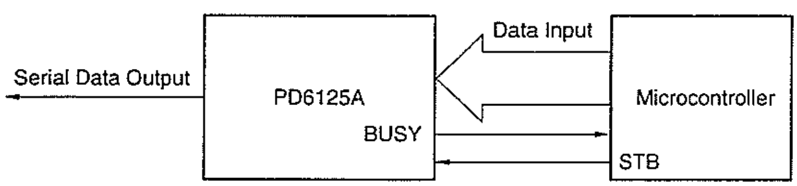
Application Circuit Example 1



Caution **The value of the capacitor for starting the ceramic oscillator needs to be set after consideration of the voltage level it is going to be used at and the starting characteristics of the ceramic oscillator.**

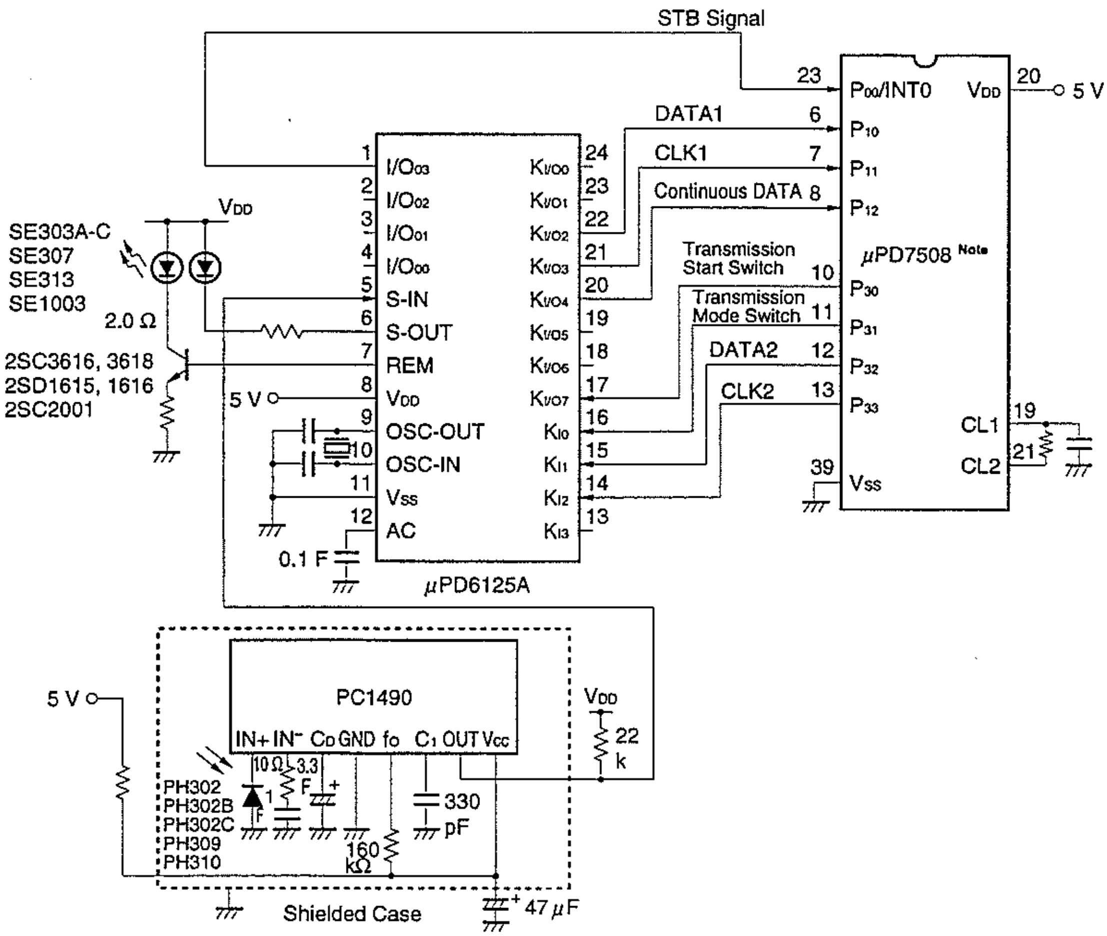
Application Circuit Example 2





Caution **The value of the capacitor for starting the ceramic oscillator needs to be set after consideration of the voltage level it is going to be used at and the starting characteristics of the ceramic oscillator.**

Application Circuit Example 3



Note Protective Device

Caution The value of the capacitor for starting the ceramic oscillator needs to be set after consideration of the voltage level it is going to be used at and the starting characteristics of the ceramic oscillator.

The µPD6125A can be used as the transmitter/receiver using the µPD7500 Series in the system computer.

In the case in the above diagram, ordinarily, the receiving mode is set and remote control reception is carried out through the µPC1490. When a signal is received, after sending the STB signal to the system computer, the received data are sent to the system computer by DATA1 and CLK1. If the received data are continuous code, they are sent to the system computer as continuous data.

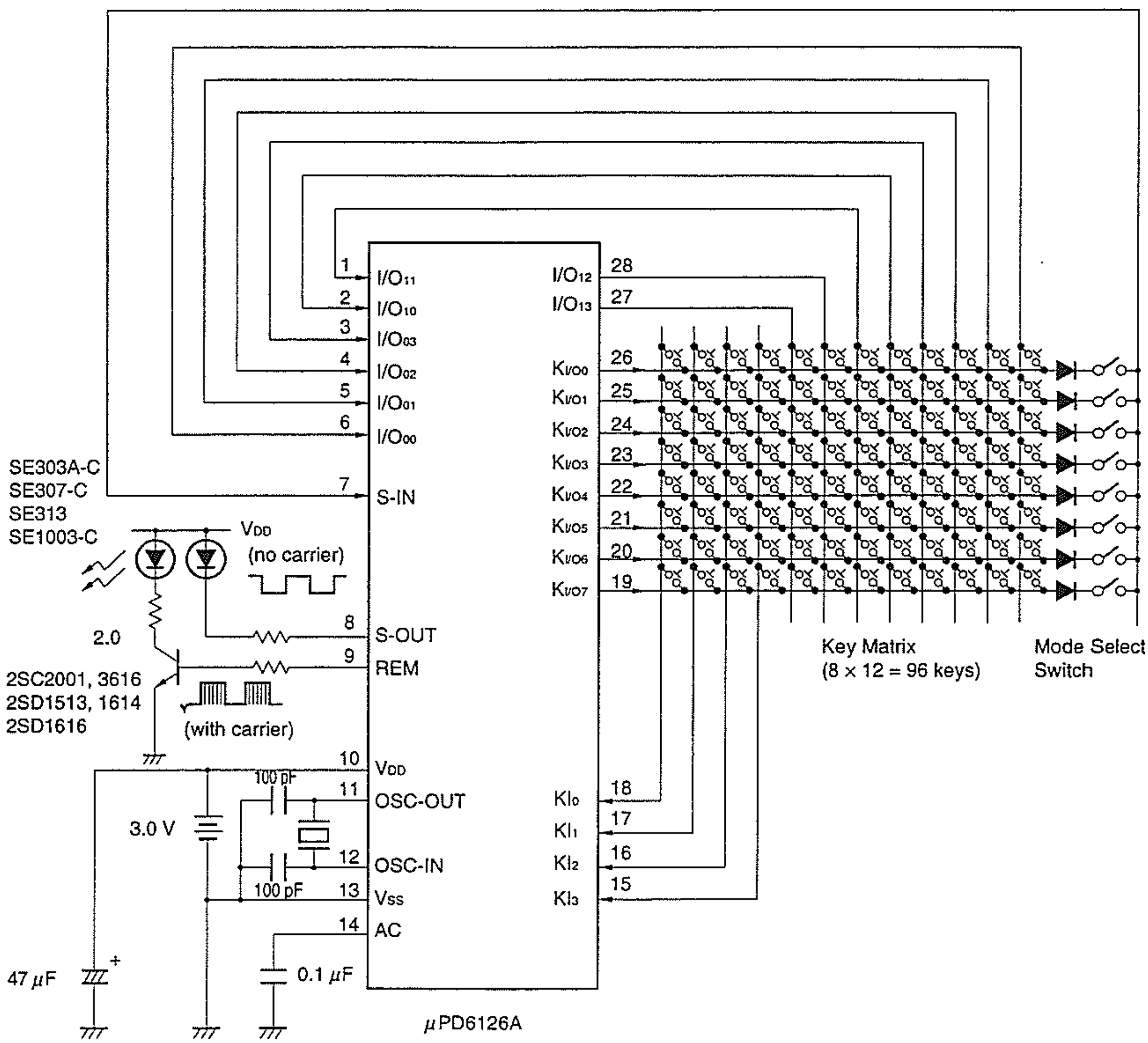
If the send mode switch is turned ON while in the receive mode, the µPD6125A changes to the send mode.

If the send mode switch is ON and the send start switch is OFF, the transmission data from the system computer are fetched by DATA2 and CLK2.

When the send mode switch is ON and the send start switch is ON, the data to be transmitted are sent from the REM pin.

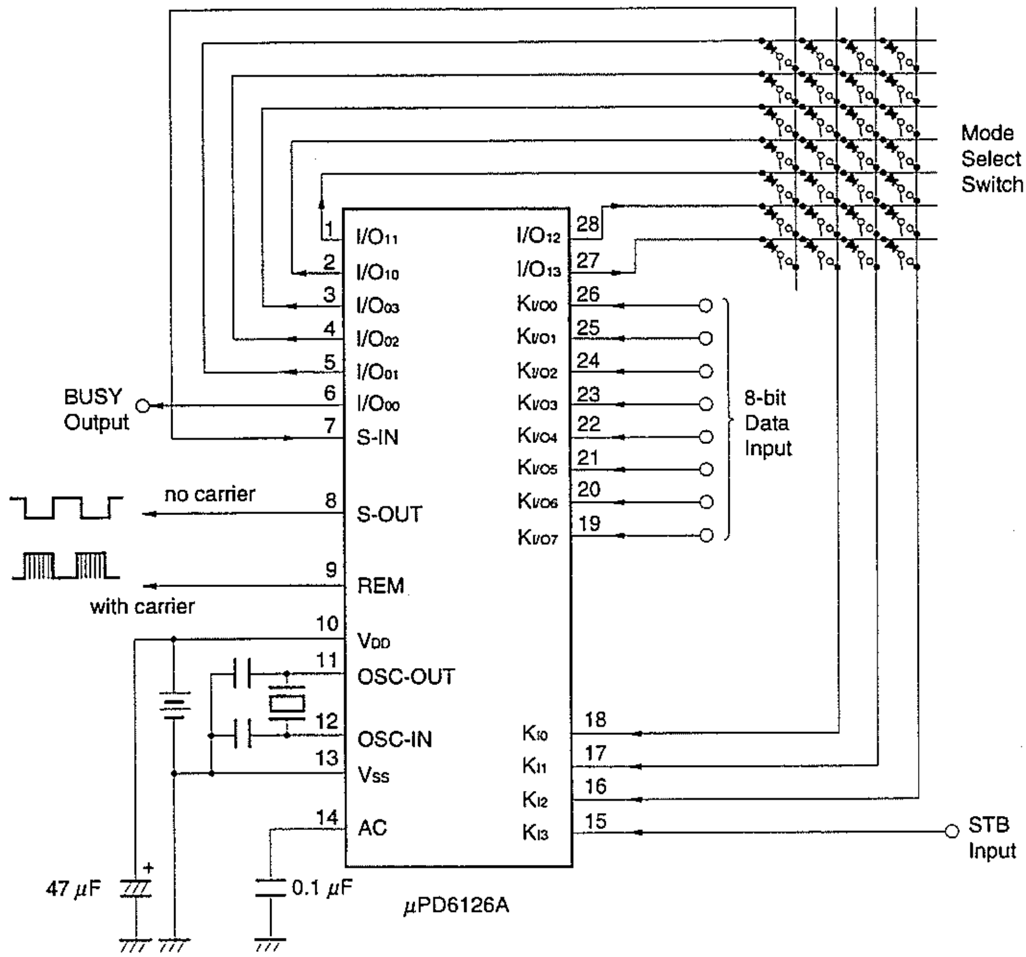
9.3 μPD6162A

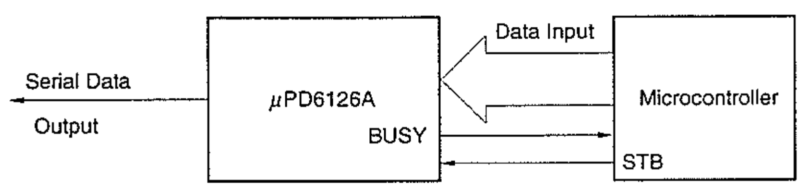
Application Circuit Example 1



Caution The value of the capacitor for starting the ceramic oscillator needs to be set after consideration of the voltage level it is going to be used at and the starting characteristics of the ceramic oscillator.

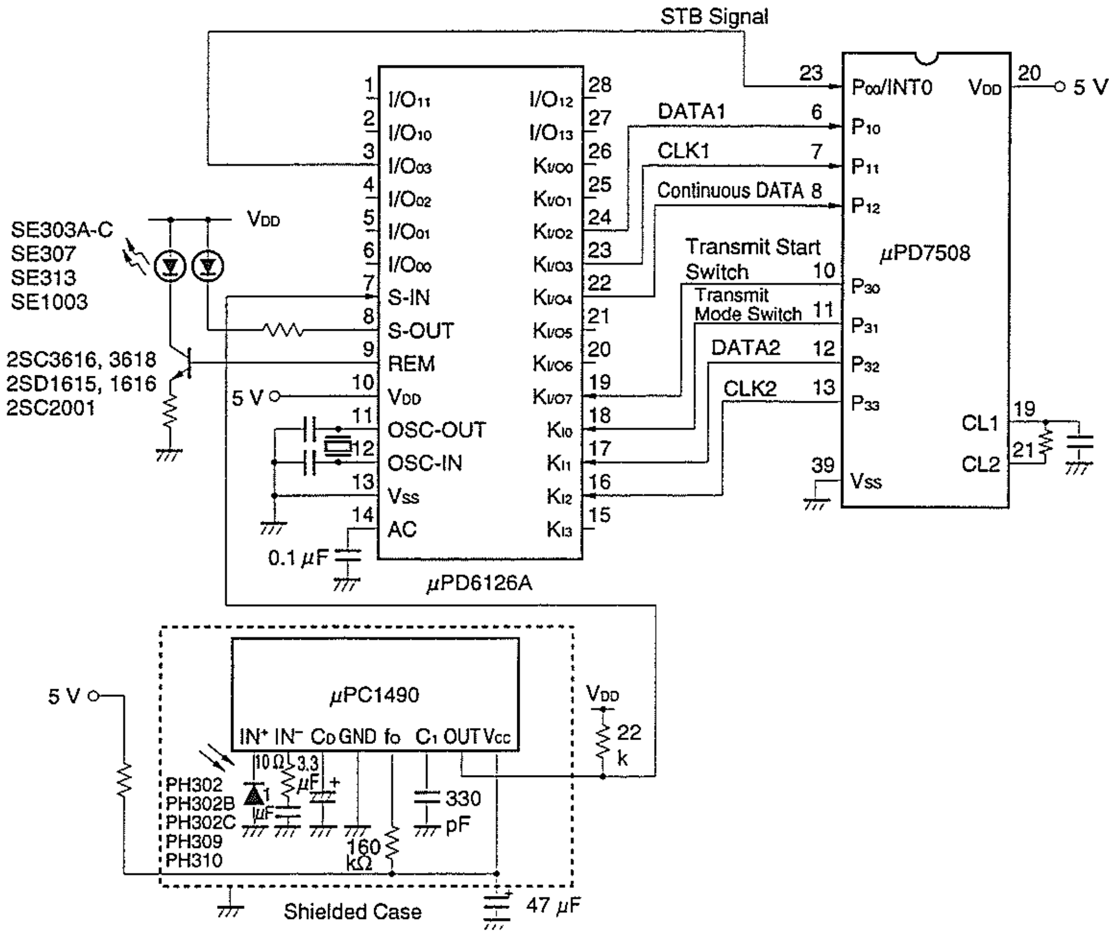
Application Circuit Example 2





Caution **The value of the capacitor for starting the ceramic oscillator needs to be set after consideration of the voltage level it is going to used at and the starting characteristics of the ceramic oscillator.**

Application Circuit Example 3



Note Protective Device

Caution The value of the capacitor for starting the ceramic oscillator needs to be set after consideration of the voltage level it is going to be used at and the starting characteristics of the ceramic oscillator.

The μPD6126A can be used as the transmitter/receiver using the μPD7500 Series in the system computer.

In the case in the above diagram, ordinarily, the receiving mode is set and remote control reception is carried out through the μPC1490. When a signal is received, after sending the STB signal to the system computer, the received data are sent to the system computer by DATA1 and CLK1. If the received data are continuous code, they are sent to the system computer as continuous data.

If the send mode switch is turned ON while in the receive mode, the μPD6126A changes to the send mode.

If the send mode switch is ON and the send start switch is OFF, the transmission data from the system computer are fetched by DATA2 and CLK2.

When the send mode switch is ON and the send start switch is ON, the data to be transmitted are sent from the REM pin.

9.4 Cautions in Wiring

When transmitting with an IR LED, it is conceivable that about 1A of current will flow at the peak. In that case, the power supply voltage tends to fluctuate, and noise with high frequency components is generated in the power line during switching.

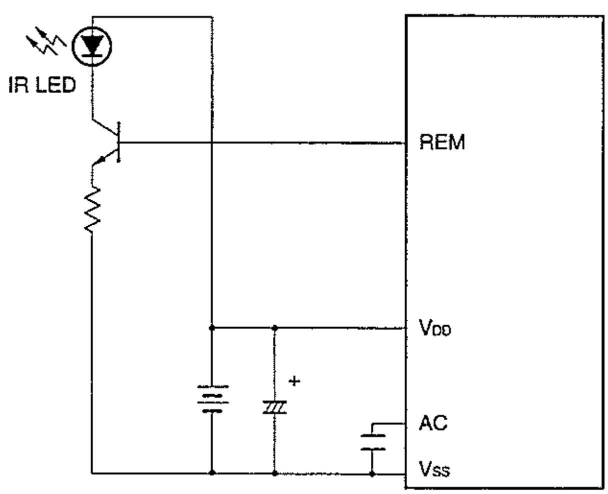
In order to minimize the effect of power supply system noise, use caution with wiring of V_{DD} and V_{SS}.

If V_{DD} or V_{SS} wiring is run to the IC power supply (V_{DD}, V_{SS}) via the IR LED power supply, switching noise to the IC will become greater. To minimize the effect of noise, run wiring so that the power line to V_{DD} and V_{SS} of the IC and the power line to the IR LED are isolated with the battery terminals at the center.

In the same way, run the wiring so that the AC pin is isolated from the power line for the IR LED.

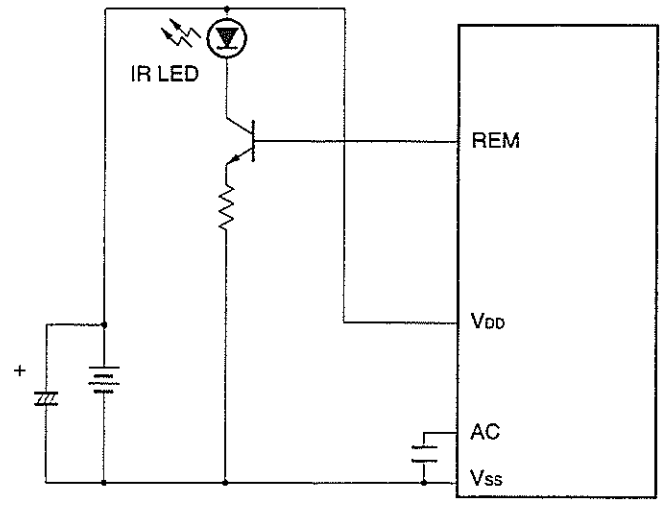
Also, the noise effect will be minimized if the ceramic oscillator is located as close to the IC as possible, and the power stabilization capacitor is located near the IC's power supply pins.

(Good Example)



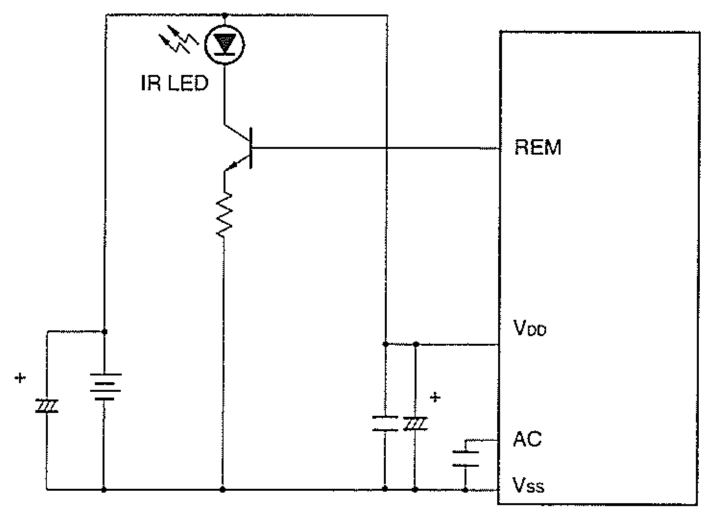
Since the IC side power supply line and the LED side power supply line are isolated by the battery and the capacitor, the noise effect becomes small.

(Bad Example)



Since the IC side power supply line is wired so that it passes by the IR LED as its power supply, the effect of switching noise on the IC is great.

(Improvement of the Bad Example)



If the power supply stabilization capacitor is placed right next to the IC's power supply pins, and if a by-pass capacitor is added for eliminating the high frequency components, the effect of noise can be minimized.

[MEMO]

★

APPENDIX A LIST OF μPD612x SERIES PRODUCTS

Item \ Product Name	μPD6124A	μPD6600A	μPD61P24	μPD6125A	μPD6126A
ROM Capacity	1002 × 10-bit (Mask ROM)	512 × 10-bit (Mask ROM)	1002 × 10-bit (One-Time PROM)	1002 × 10-bit (Mask ROM)	
RAM Capacity	32 × 5-bit				
Input/Output Pins	8-pin ($K_{I/O0-7}$)			12-pin ($K_{I/O0-7}$, I/O_{00-03})	16-pin ($K_{I/O0-7}$, I/O_{00-03}, I/O_{10-13})
S-IN Pin	Provided				
Power Consumption (f_{osc} = STOP) (MAX.)	2 μA		1 μA		
S-IN High Level Input Current (MAX.)	30 μA		15 μA		
Transmission Carrier Frequency	fosc/12, fosc/8				
Low Voltage Detection (Reset) Circuit	Provided		Not provided		
Mask Option	Provided		Not provided (fixed)	Provided	
Power Supply Voltage	V_{DD} = 2.2 to 5.5 V	V_{DD} = 2.2 to 3.6 V	V_{DD} = 2.2 to 5.5 V	V_{DD} = 2.0 to 6.0 V	
Package	• 20-pin Plastic SOP (300 mil) • 20-pin Plastic Shrink DIP (300 mil)			• 24-pin Plastic SOP (300 mil) • 24-pin Plastic Shrink DIP (300 mil)	• 28-pin Plastic SOP (375 mil)

[MEMO]

★ # APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided to develop programs for the μPD612x Series.

Name	Order Name
μPD612x Series Emulator	— Note 1
μPD612x Series Assembler	— Note 1
PROM Programmer	AF-9703 Notes 2, 3 AF-9704 Notes 2, 3 AF-9705 Note 3 AF-9706 Note 3
μPD61P24 Program Adapter	AF-9807B Note 3

Notes 1. Sold by IC Ltd.
Inquiries:
No. 6 Barnett Gotanda Bldg.
1-9-5 Higashi Gotanda, Shinagawa-ku, Tokyo 141
TEL 03 (3447) 3793
FAX 03 (3440) 5606
2. Out of production
3. Sold by Ando Denki Ltd.
Inquiries
4-19-7 Kamata, Ota-ku, Tokyo 144
TEL 0120-40-0211 (toll-free)

Caution **In the case of a writing program, after assembling the program, convert the HEX file to a ROM file using a PROM utility program "UPDROM" (See the AS612x Assembler User's Manual (EEU-601).)**

[MEMO]

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