Tsi310™ Evaluation Board User Manual

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Tsi310 Evaluation Board User Manual

This document describes how to test the key features of the Tsi310 using the Tsi310 Evaluation board. The following topics are discussed:

Revision History

80B6020_MA002_03, September 2009

This document was rebranded as IDT. It does not include any technical changes.

80B6020_MA002_02, June 2004

This document supports the following:

- Board part number Tsi310A-RDK1 v1.0; device part number Tsi310A-133CE
- Board part number Tsi310-RDK1 v1.0; device part number Tsi310-133CE

Please note that there are no technical differences between this document and the previous version of the evaluation board manual, document number 80B6020_MA002_01.

80B6020_MA002_01, February 2004

This document supports part numbers, Tsi310-133CE and Tsi310A-133CE. Please note that there are no technical differences between this document and the previous version of the evaluation board manual, document number 80B6000_MA002_02.

1. Features

The Tsi310 Evaluation board has the following features:

- Primary interface plugs into any standard 3.3V PCI option card slot
- Provides one secondary 3.3V PCI-X slot with operation up to 133.33 MHz, with optional unpopulated slot
- Interconnect complies with the specifications:
  - *PCI Local Bus Specification (Revision 2.2)*
  - *PCI-X Addendum to PCI Local Bus Specification (Revision 1.0a)*
  - *PCI-to-PCI Bridge Architecture Specification (Revision 1.1)*

2. Description

The Tsi310 Evaluation board is intended to operate in a “covers off” laboratory environment while installed in a host PC. The board consists of the following:

- One 64-bit PCI-X compatible card edge connector that connects to the primary side of the bridge device (see Figure 1)
- Two secondary 64-bit PCI-X compatible connectors available at the top of the evaluation board

For program debug and performance measurements, the evaluation board’s extended height provides access to jumpers and facilitates the use of a logic analyzer interface card for analysis of the PCI bus activity.

Power for the evaluation board is provided from the 64-bit PCI-X-compatible card edge. Power for the Tsi310 device is provided by an on-board regulator that develops 2.5V from the host +5V supply. Power-on status of the board is reported by LED DS1 on the 2.5V regulator output.

The on-board clock rate selection is provided by user-activated switch settings. The jumpers permit experimentation with various PCI conventional and PCI-X modes.

3. Jumper Settings

The following table shows the jumper settings for the evaluation board. The location of the board's jumpers, switches, and other devices is illustrated in Figures 1 and 2.

Table 1: Jumper Settings

Device Number	Description
R118	Controls PCI-X capability (PCIXCAP) presented to the primary bus. This is a solder-in part that is unpopulated by default. No resistor: 133 PCI-X 10K resistor: 66 PCI-X 0-ohm resistor: PCI Conventional
R80, R81	Control PRST1# PRSNT2# identify the power dissipation of the add-in card to the host system. These resistors are configured for the maximum power requirement of 25 watts.
J3	Secondary driver mode override: The Tsi310 automatically selects driver impedance based on bus mode. ON: Selects multi-point (conventional PCI, PCI-X66, and PCI-X100), point-to-point (PCI-X133). Note: This jumper is installed by default. OFF: Selects point-to-point (conventional PCI, PCI-X66, and PCI-X100), multi-point (PCI-X133).
J4	Primary driver mode control: The Tsi310 automatically selects driver impedance based on bus mode. ON: Selects multi-point (conventional PCI, PCI-X66, and PCI-X100), point-to-point (PCI-X133). Note: This jumper is installed by default. OFF: Selects point-to-point (conventional PCI, PCI-X66, and PCI-X100), multi-point (PCI-X133).
J5	Primary side M66EN pin: Has no function when the primary bus is operating in PCI-X mode. Populating this jumper grounds M66EN, thereby disabling 66 MHz operation. **Note:** This jumper is not installed.
J6	Controls selection of secondary bus PCI-X maximum frequency. This jumper is only applicable when secondary bus is operating in PCI-X mode and PCIXCAP indicates 133 MHz bus speed. When J6 is jumpered, the S_SEL100 signal is low indicating 133 MHz operation; otherwise, 100 MHz operation is selected. Users must ensure the selection of J6 matches S1-2 and S1-3 (clock frequency control) settings as described in Section 4 on page 9. **Note:** This jumper is installed by default.
J7	Internal arbitration enabled signal: Tests the capability of permitting external arbitration on the secondary bus by disabling the internal arbiter. An external arbiter chip is required when jumper is removed. **Note:** This jumper is installed by default, which means the arbiter is enabled.

Table 1: Jumper Settings *(Continued)*

Device Number	Description
J8	Pins 1 and 2 jumpered forces the secondary bus to PCI-X 66. Pins 2 and 3 jumpered forces the secondary bus into PCI conventional mode. **Note:** This jumper is installed in positions 2 and 3 by default.
J9	JTAG test interface for the Tsi310: The JTAG mechanical form factor is not standardized. This connector is normally not installed.
J10	Power consumption test interface for the Tsi310. **Note:** This jumper is not installed.

Figure 1: Jumper, Switch, and Connector Layout — Top View

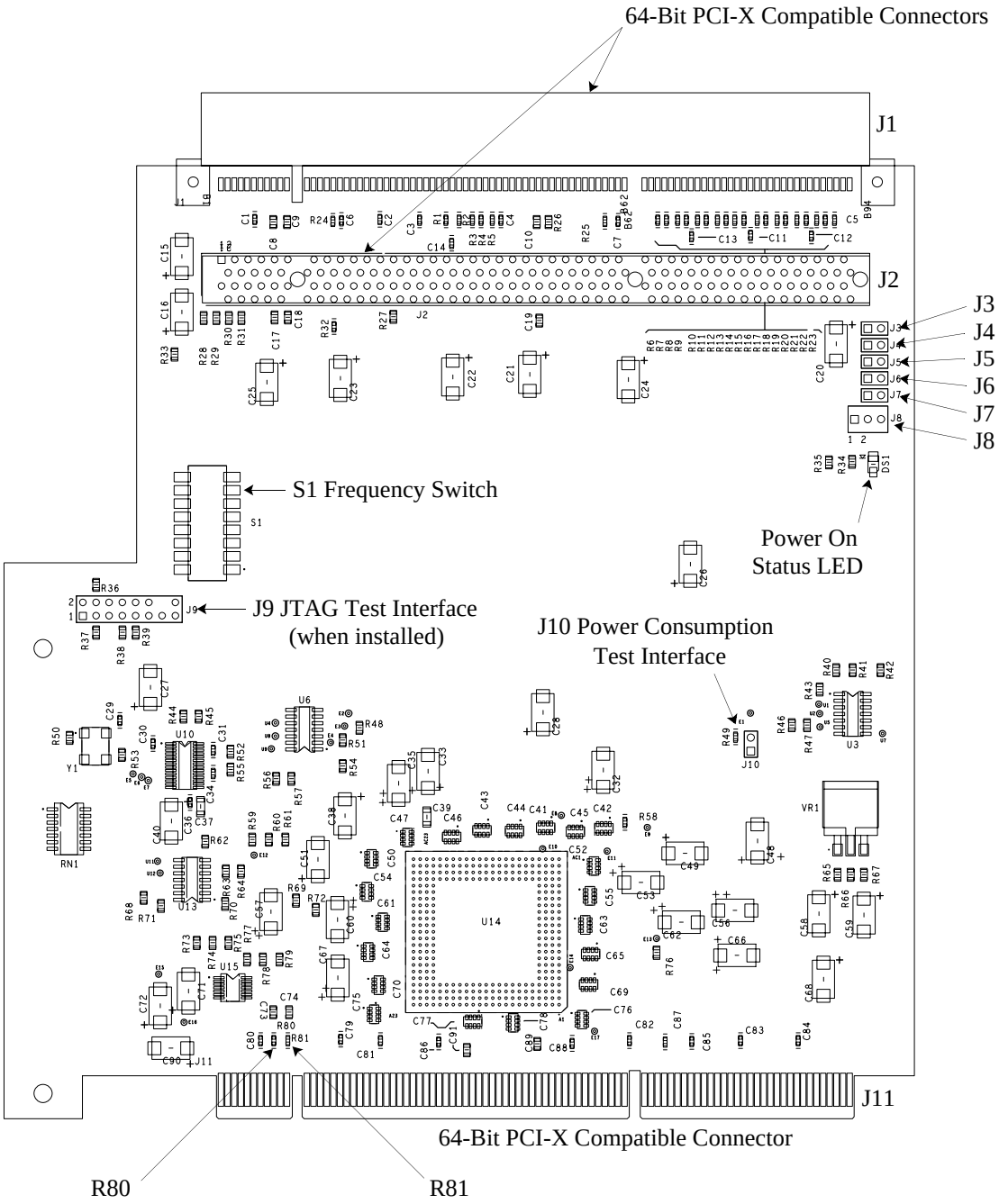
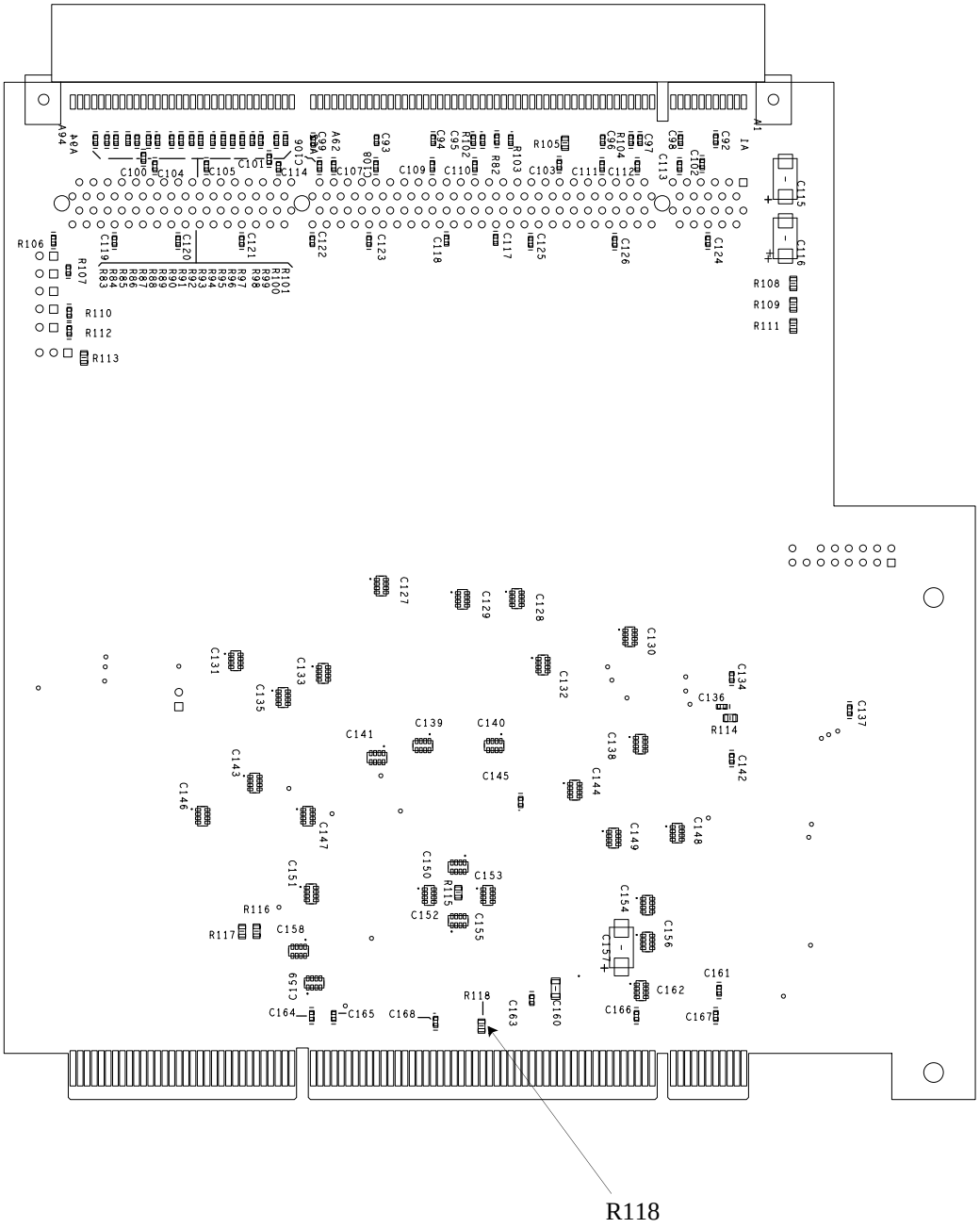


Figure 2: Jumper Layout — Bottom View



4. Switch Settings

The functions and settings of the switches are described in Tables 2 and 3; the location of the switches is displayed in Figure 1 on page 7.

Table 2: Switch S1 Functions and Default Settings

Switch S1 Element[a]	Default Setting[b]	Function
S1-1	off	Provides output enable for the C9531 clock generator.
S1-2, S1-3	on	Controls clock frequency generated by U5 (see Table 3) for the PCI-X Bridge secondary bus.
S1-4	off	Operates the spread-spectrum clock controls available from the C9531. The I_2C interface to the C9531 is not wired, which results in a 0.5% downspread (-0.5%, +0.0) of the generator clock output when spread-spectrum is selected. Default setting disables spread-spectrum operation.
S1-5 through S1-8	off	Not used.

a. The DIP switch on the evaluation board has a silk-screen label of “S1”. The notation used in the tables for the DIP switch is S1-x, where “S1” is the silk-screen reference locator, and “x” is the switch location on the DIP switch.

b. closed = on; open = off

Table 3: Secondary Clock Speed Generation Selection

Jumper/ Switch #	Signal Name	PCI Mode		PCI-X Mode		
		33 MHz[a]	66 MHz	66 MHz	100 MHz	133 MHz
Sw1-3	C9531AT Pin S0	0 (closed)	1 (open)	1 (open)	0 (closed)	1 (open)
Sw1-2	C9531AT Pin S1	0 (closed)	0 (closed)	0 (closed)	1 (open)	1 (open)
J6	S_SEL100	don’t care	don’t care	don’t care	not installed	installed
J8	PCIXCAP	2-3	2-3	1-2	not installed	not installed

a. The Tsi310 Evaluation board is shipped with this default configuration.

5. Schematic Diagrams

This section illustrates the schematic diagrams for the Tsi310 Evaluation board.

Figure 3: Schematic Diagram — Page 1

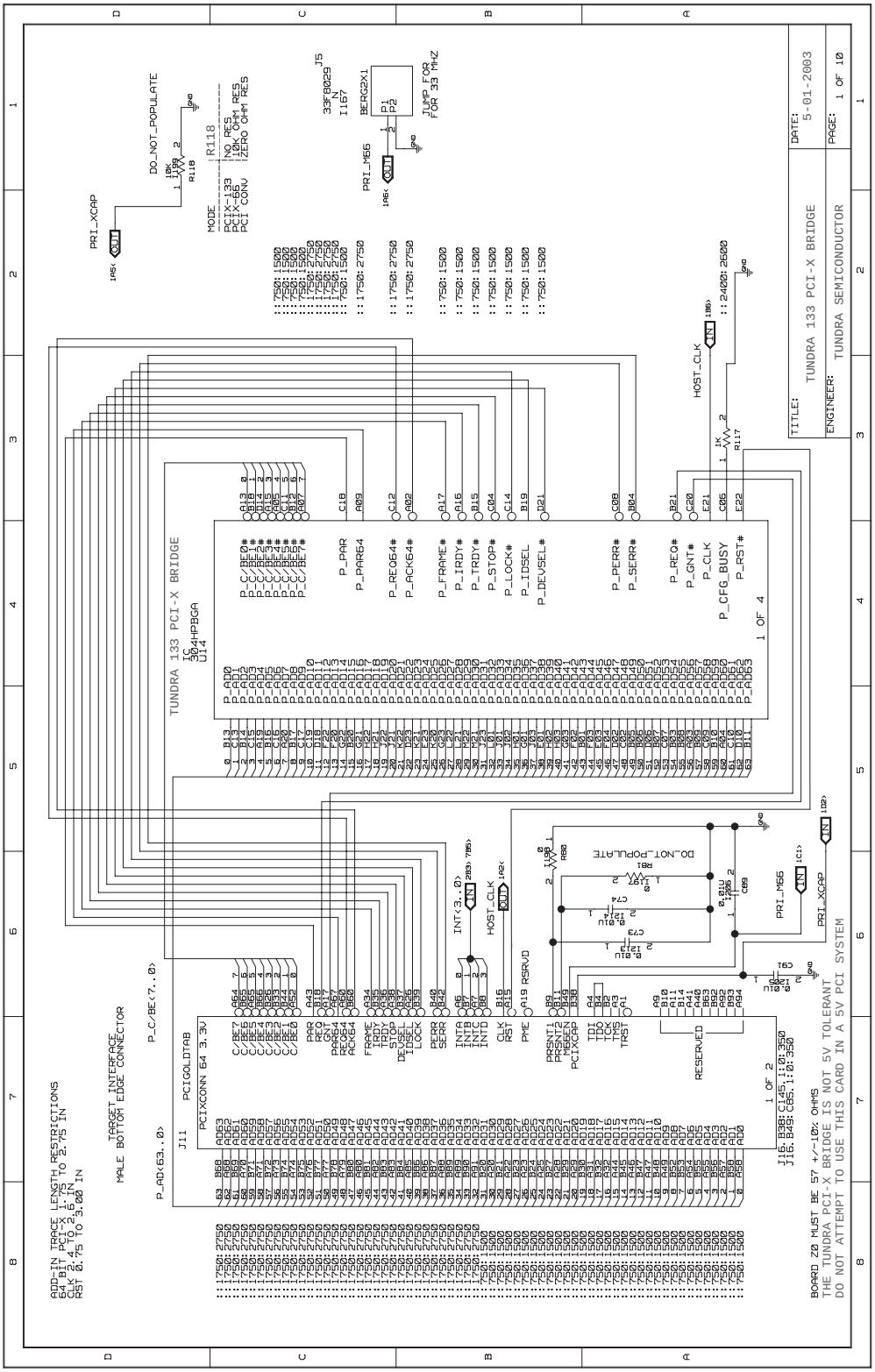


Figure 4: Schematic Diagram — Page 2

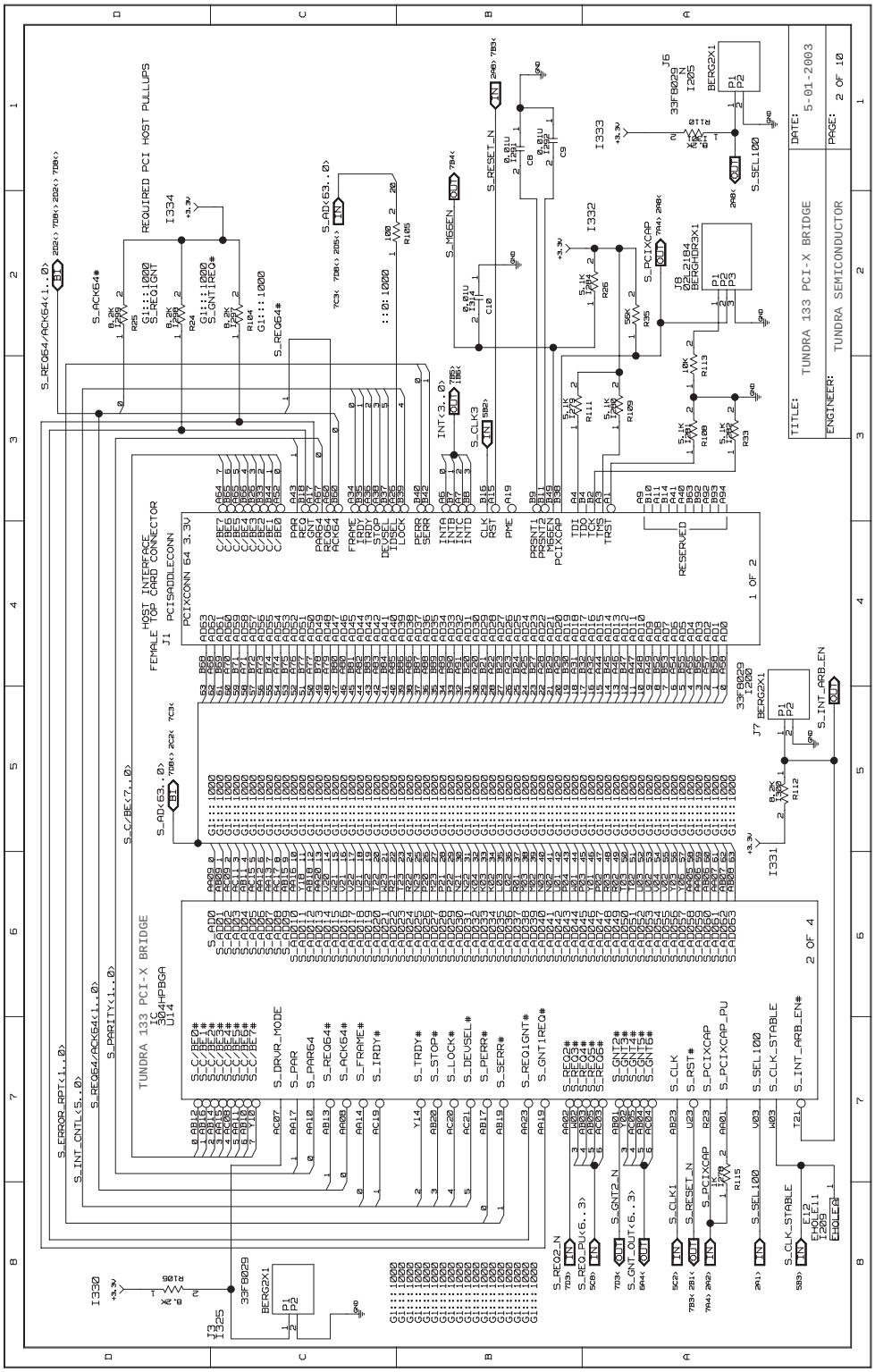


Figure 5: Schematic Diagram — Page 3

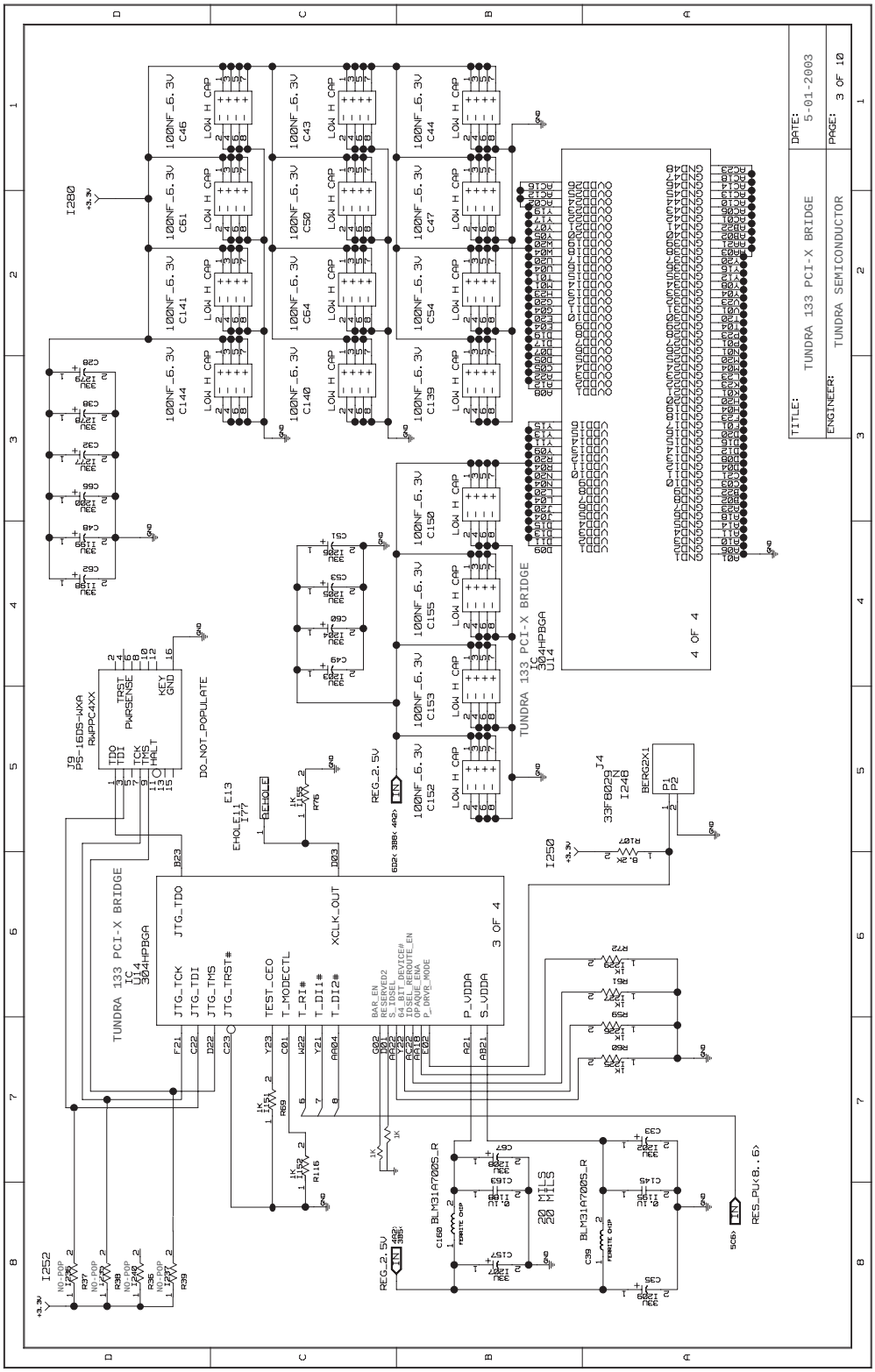


Figure 6: Schematic Diagram — Page 4

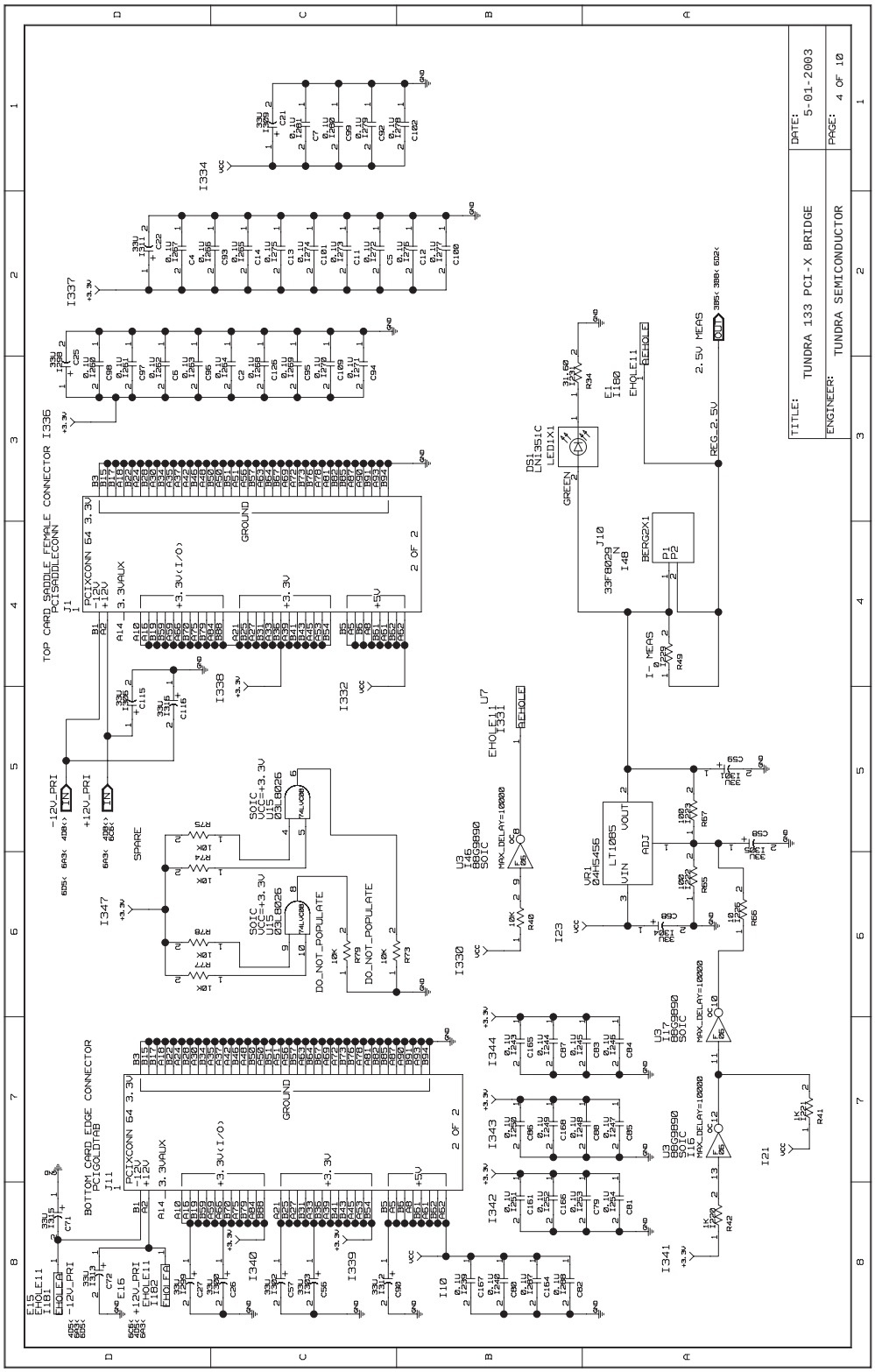


Figure 7: Schematic Diagram — Page 5

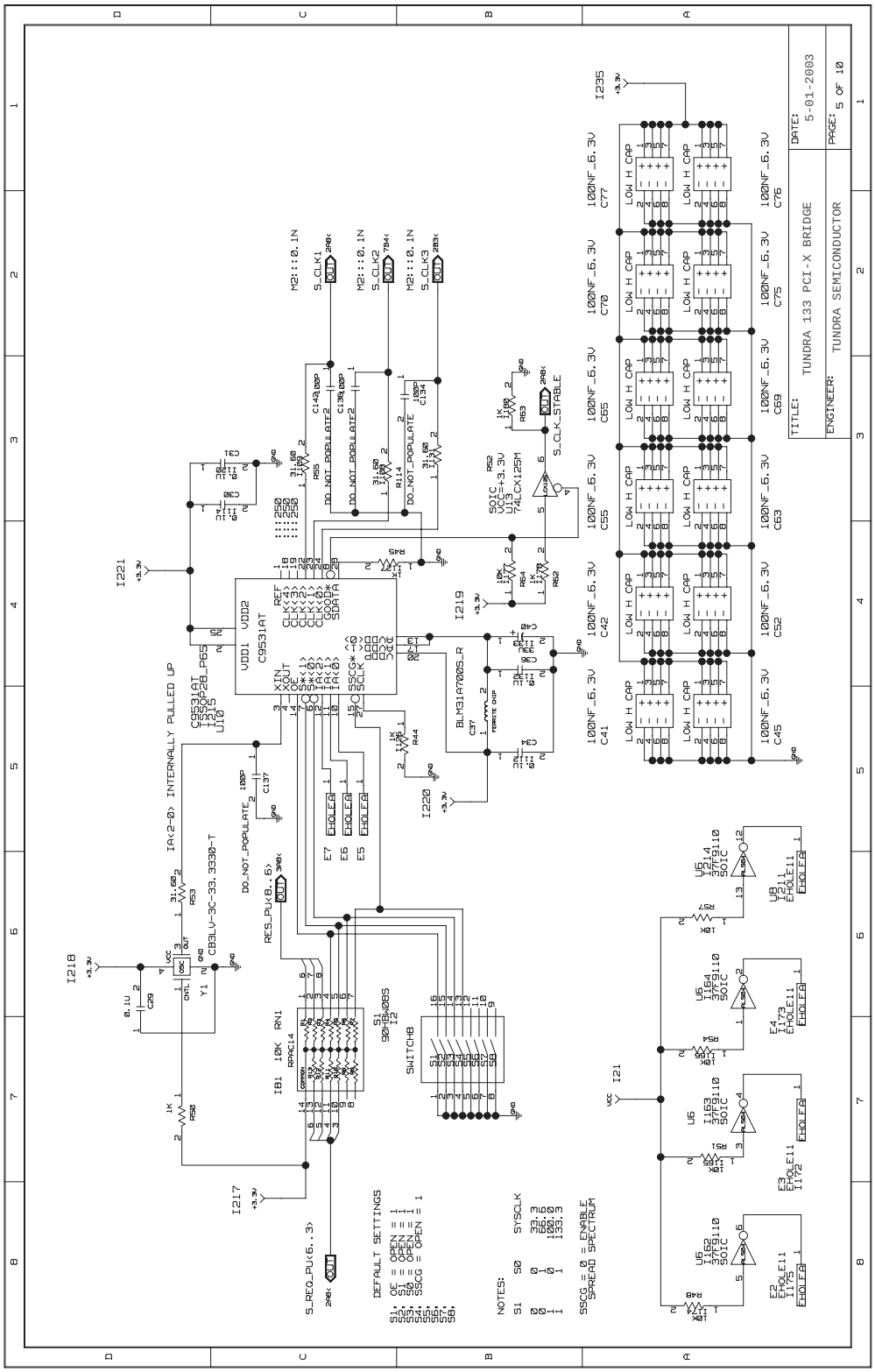


Figure 8: Schematic Diagram — Page 6

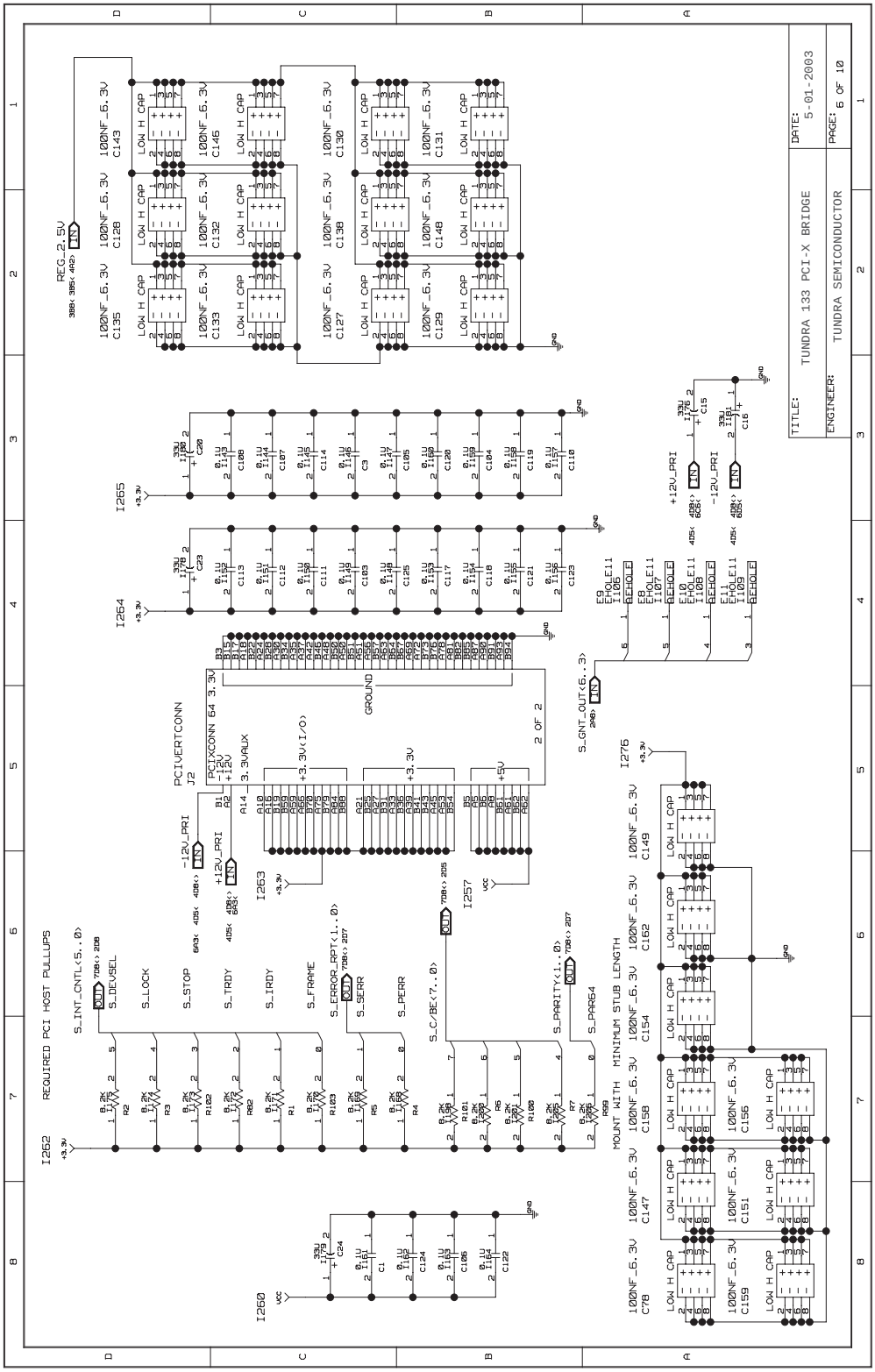


Figure 9: Schematic Diagram — Page 7

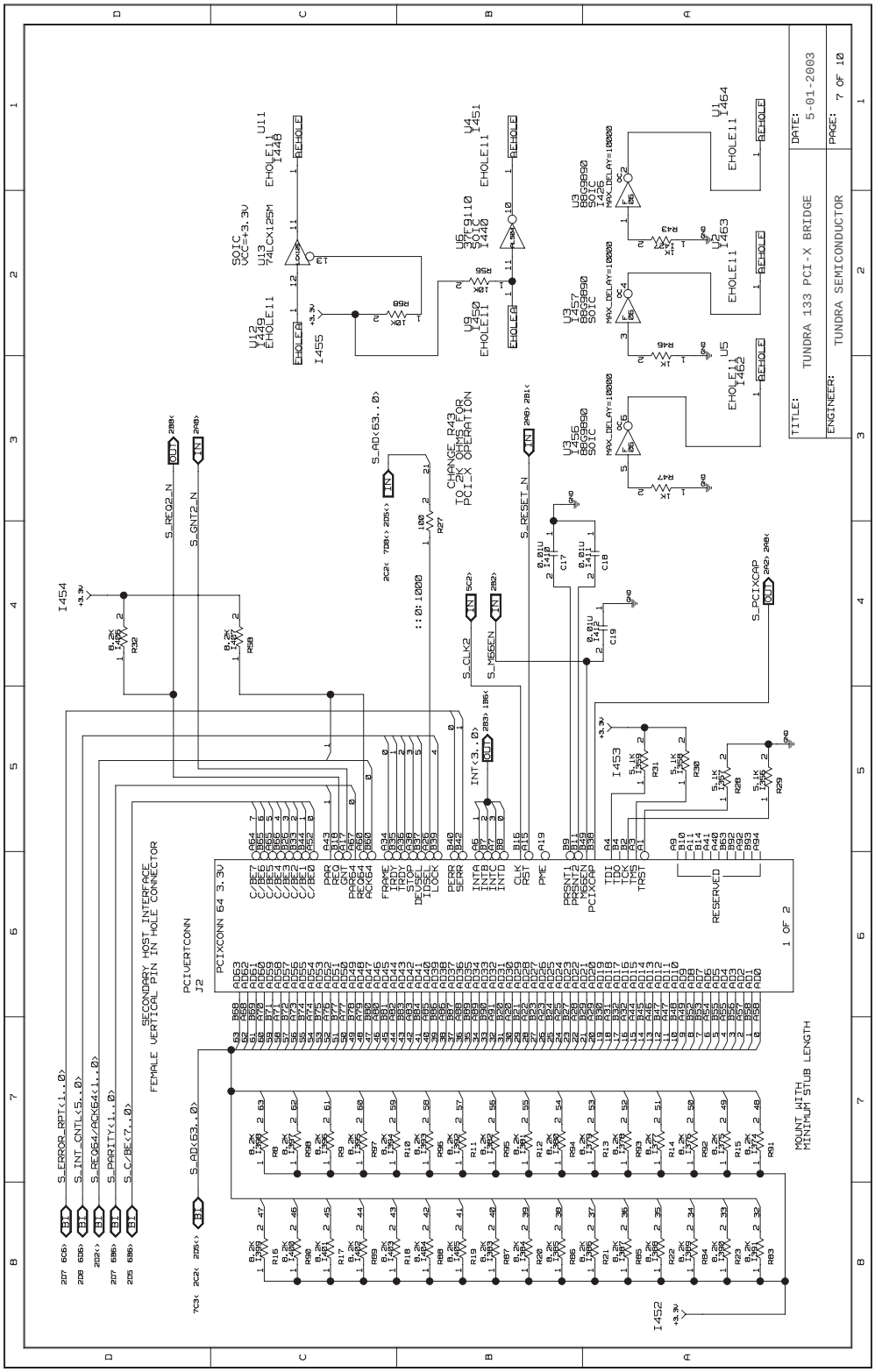


Figure 10: Schematic Diagram — Page 8

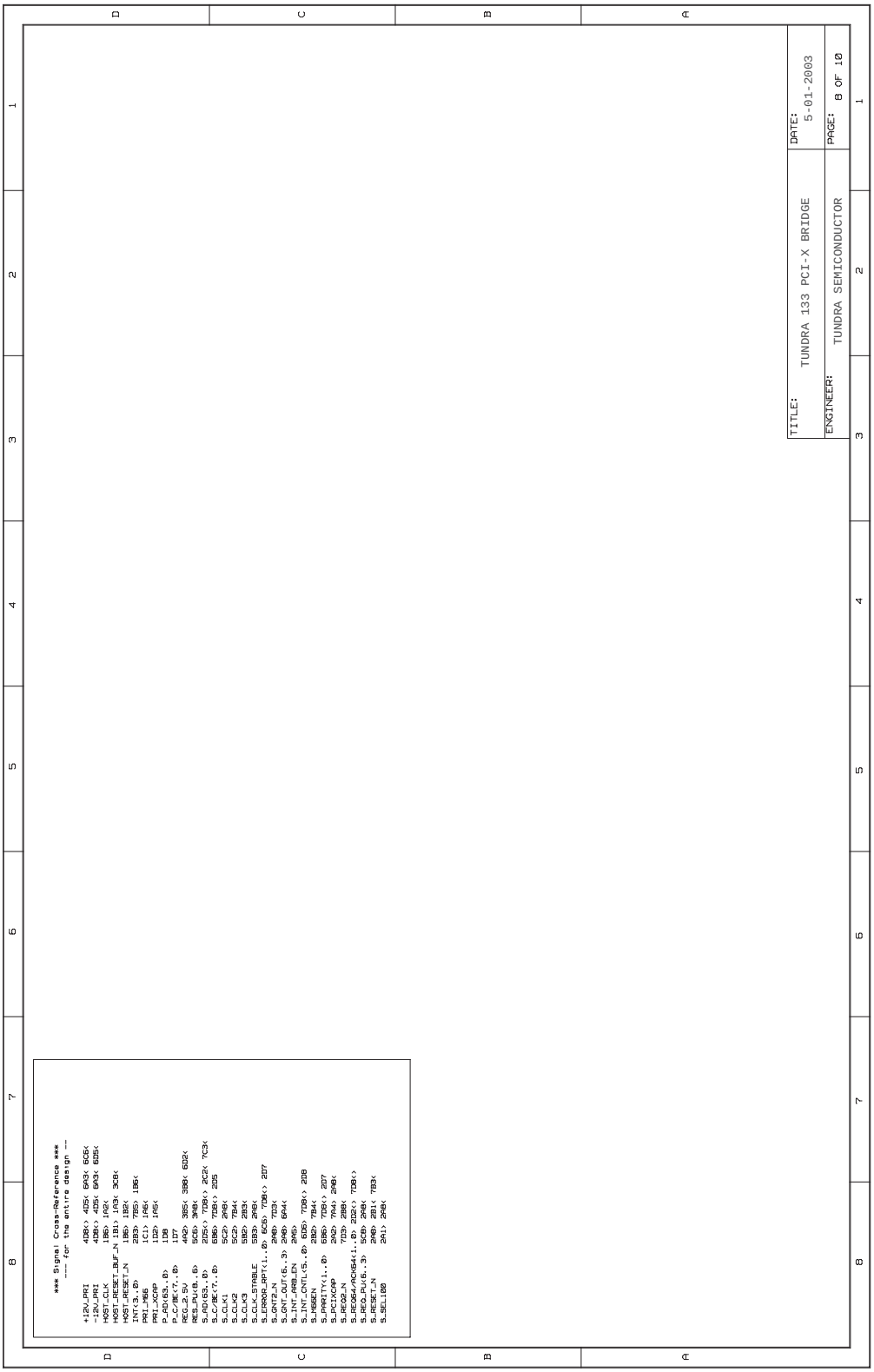


Figure 11: Schematic Diagram — Page 9

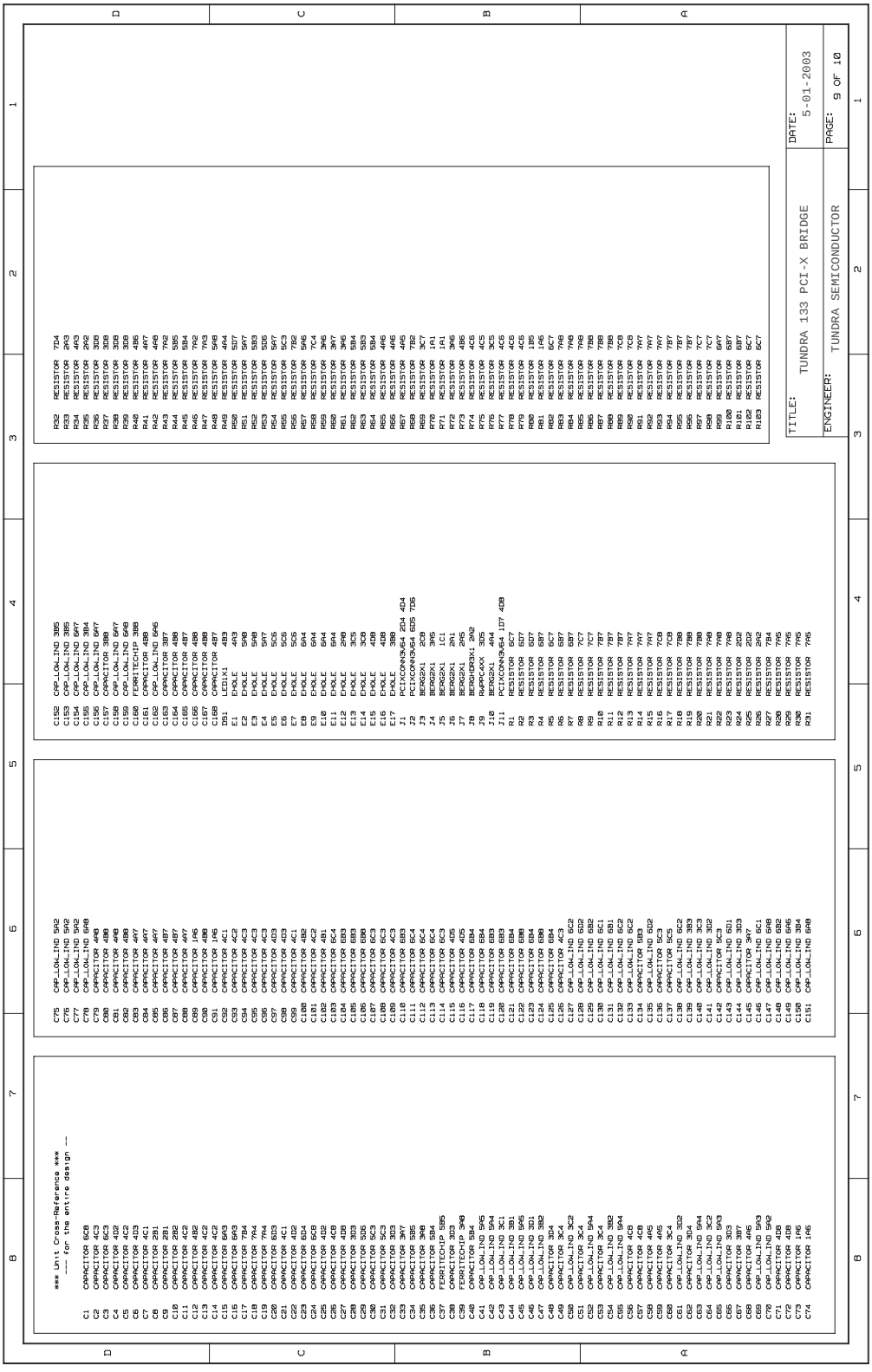
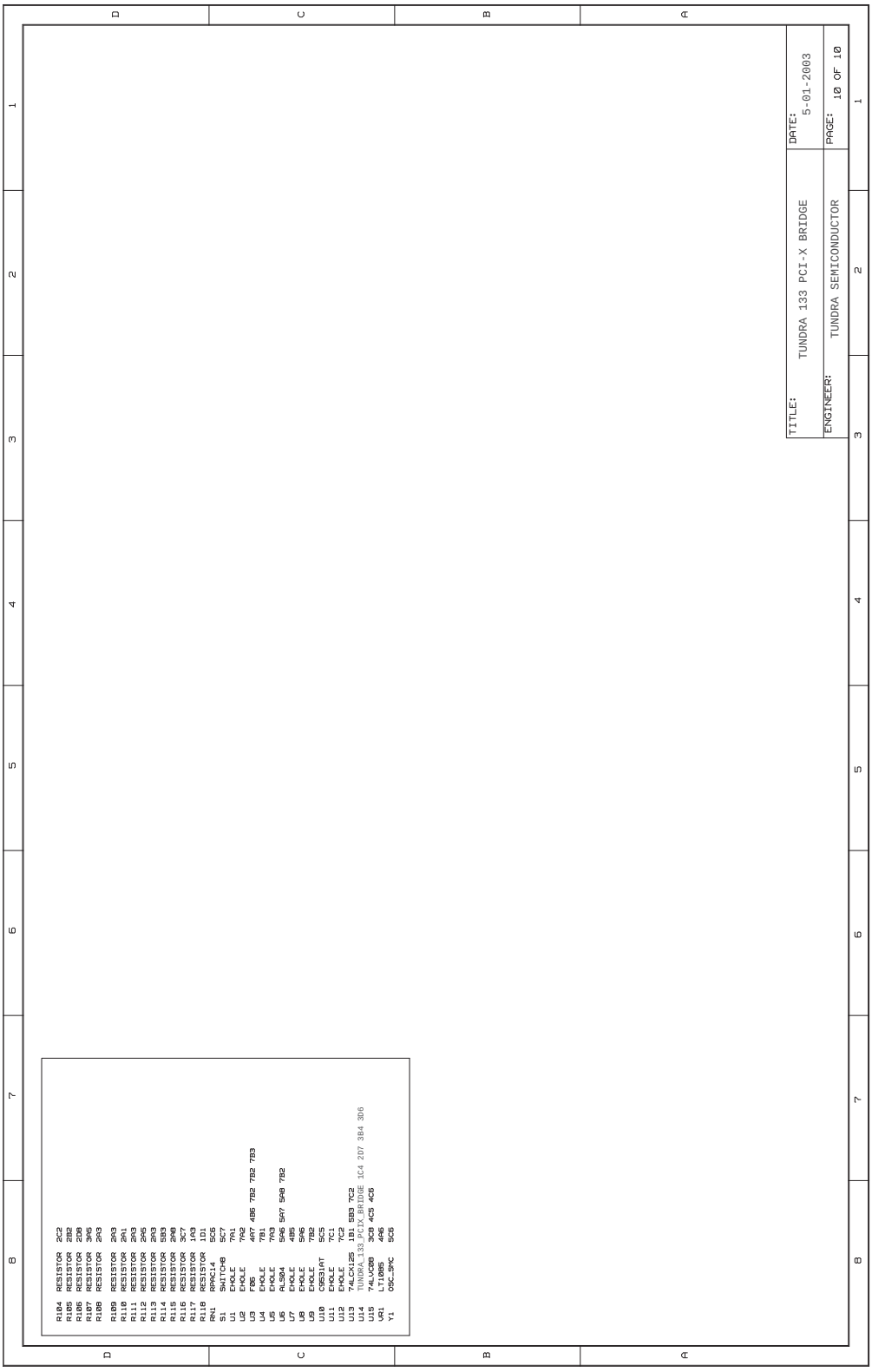


Figure 12: Schematic Diagram — Page 10



6. Unsupported Functions

The following table describes functions that are not supported by the Tsi310 Evaluation board.

Table 4: Unsupported Functions and Pins

Function	Connector Location	Comments
Power management support (PME)	Pin A19, edge card	Reserved and not wired.
Standby power (3.3VAUX)	Pin A14, edge card	Not connected to a standby power source.
-5VOLTS	-	Available from ATX power supply at ehole U20. Not required by PCI interface.
PRSNT1#, PRSNT2#	-	PRSNT1# is tied low by R80 at the edge card connector so the evaluation board is recognized as occupying a host slot in compliance with the PCI specification.
Hot plug	-	The evaluation board does not support hot plugging.

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