Verification Guide

PCB verification guide for Core VDD

RZ/A3UL PBGA 13.0sq

Renesas Electronics
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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

The purpose of this guide

This guide helps PCB design engineers to verify their design and achieve their design goal. To achieve the best SoC performance, Power Distribution Network (PDN) for core power supply is very important. Therefore, we recommend getting the PDN impedance lower than the target impedance for this SoC.

This guide describes a) PCB design restrictions, b) verification items and c) how to measure them.

It is indispensable to satisfy the PCB restrictions described in this guide in order to properly operate the core functions in user's system. Renesas recommends that customers satisfying the recommendation and restrictions in this guide.

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In this document, SoC refers to the RZ/A3UL (PBGA) device.

Table of Contents

1. Introduction

1.1 Overview

This document is provided as a PCB verification guide for PDN of the Core (VDD). The purpose of this guide is to help PCB design engineers design power supplies in their PCB design.

To secure the stable operation of SoC, power integrity verification is required and discussed in this guide.

The chapters of this guide are organized as follows:

- **Section 1** describes operating conditions and power name list of core.
- **Section 2** describes simulation setup for the power integrity verification at the system level. Provided by Renesas are SoC model and information. System level simulation prepared by customers should be performed using PCB models.
- **Section 3** describes recommended PCB configuration for power.
- **Section 4** describes verification items and method of Core PDN: verification item list, its target value (target impedance), and measurement method for PDN impedance.

1.2 Operating conditions

Please see RZ/A3UL User's Manual.

1.3 Power name

Power supply pins are listed in **Table 1.1**.

Table 1.1 Power supply

Pin name	Description
VDD	Power supply for CPU, GPU and peripheral circuits.
VSS	Ground pin (common with other power supplies)

2. Supplied Materials and Simulation Setup

This section shows necessary materials for power integrity verification. SoC models are provided by Renesas. Customer need to prepare PCB models.

2.1 Information and models provided by Renesas

(1) BGA pin assignments

(2) Power Distribution Network (PDN) model for target impedance confirmation
SoC PDN model of VDD: RZA3UL_PKG_PBGA13p0sq_VDD.s26p

(3) RZ/A3UL User's Manual

2.2 Models to be prepared by customer

PCB model of Core PDN for target impedance verification

2.3 Simulation setup

Please see **section 4.2**.

3. Recommended PCB configuration

3.1 Power supply configuration

3.1.1 VDD

Figure 3.1 shows a circuit diagram image of Core power supply and external parts.

Power supply impedance of your PCB must be lower than the target impedance of the Core power supply (VDD). Please refer to **section 4** concerning the target impedance and verification method.

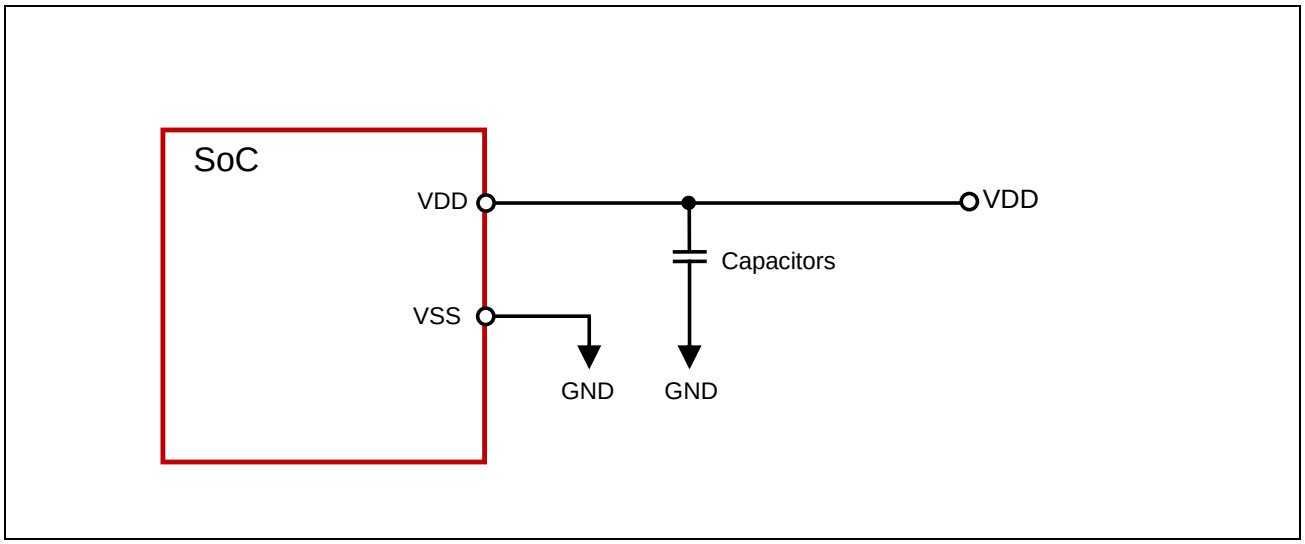

Figure 3.1 Circuit diagram of Core power supply (VDD) and external parts

4. Verification items and method of Core Power Distribution Network (PDN)

4.1 Verification items

The target impedances Ztarget(f) are shown in **Table 4.1**. Frequency range for Ztarget(f) is defined higher than 1MHz. Core PDN must be designed so that the voltage is kept in the range specified by SoC specification.

Table 4.1 Target impedance for SoC Core PDN

		Target impedance: Ztarget(f)		
Pin name	Frequency	Min	Max	Unit
VDD	1MHz to 100MHz	—	0.1	Ω

4.2 Verification method

Renesas has prepared a SoC Core PDN model to use for confirming the target impedance of SoC Core power supply for VDD. Please prepare a PCB PDN model of your design.

Please connect these two models as in **Figure 4.1**, and confirm impedance in every frequency to meet the target impedance of **Figure 4.2**.

Renesas recommend that all impedances are less than target impedance at every frequency as in **Figure 4.2**.

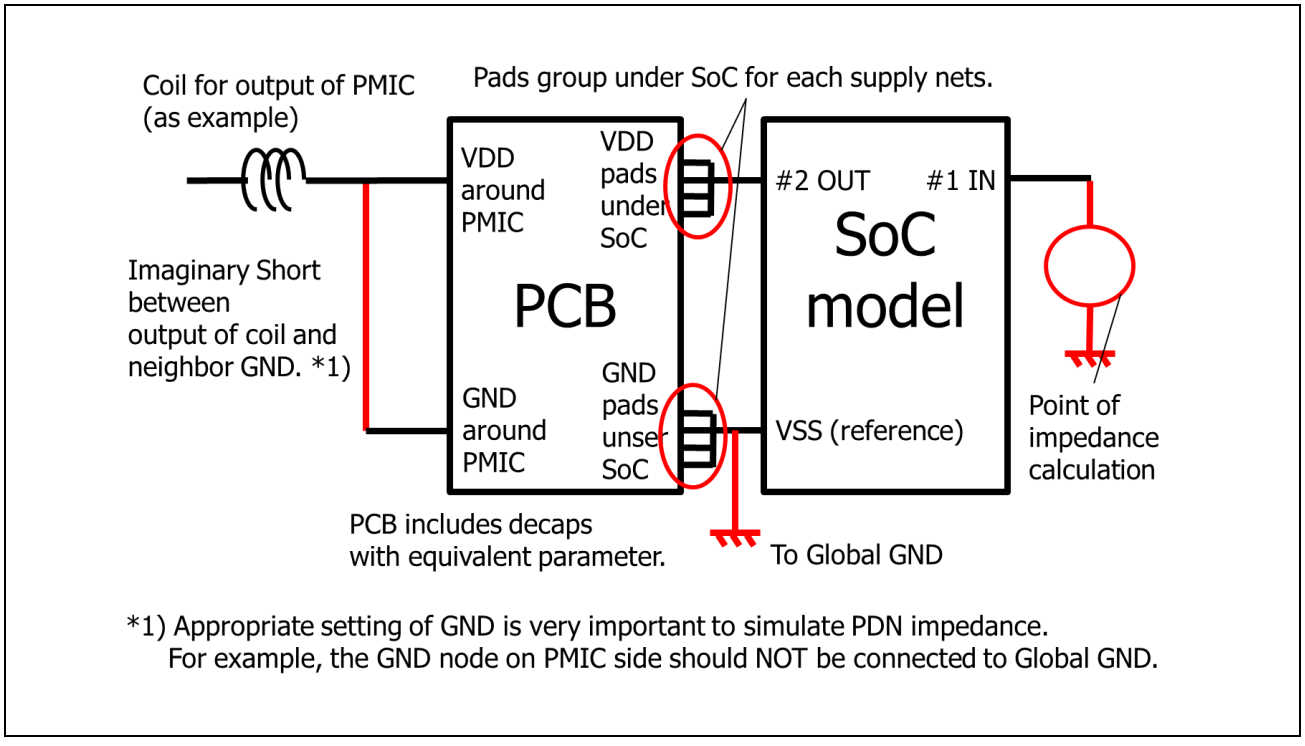

Figure 4.1 Circuit to calculate of power supply impedance

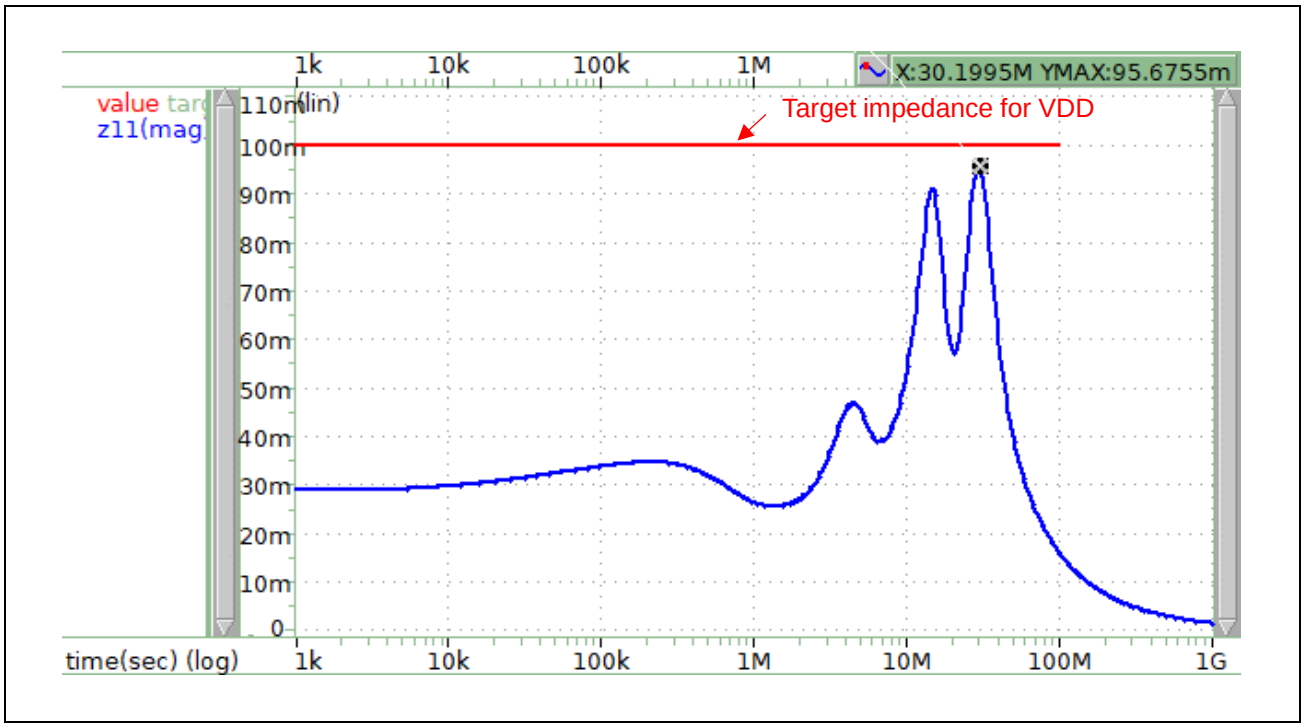

Figure 4.2 Target impedance of core power supply and impedance data of 13mm RZ/A3UL

Appendix A An example of capacitor selections

Table A.1 shows a actual example of capacitor selections for Renesas platform board.

Table A.1 A actual example of capacitor selections of 13mm RZ/A3UL platform board

Pin name	Value	Pics.
	0.01μF	2
	0.022μF	1
	0.047μF	3
	0.1μF	2
	1μF	1
	10μF	4
	47μF	5

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