User's Manual

32

RX63T Group

User's Manual: Hardware

RENESAS 32-Bit MCU
RX Family / RX600 Series

Renesas Electronics
www.renesas.com

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(2012.4)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Objective and Target Users

This manual was written to explain the hardware functions and electrical characteristics of this LSI to the target users, i.e. those who will be using this LSI in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.
This manual is organized in the following items: an overview of the product, descriptions of the CPU, system control functions, and peripheral functions, electrical characteristics of the device, and usage notes.

When designing an application system that includes this LSI, take all points to note into account.
Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

The following documents have been prepared for the RX63T Group. Before using any of the documents, please visit our web site to verify that you have the most up-to-date available version of the document.

Document Type	Contents	Document Title	Document No.
Data Sheet	Overview of hardware and electrical characteristics	RX63T Group Data sheet	—
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, and timing charts) and descriptions of operation	RX63T Group User's manual: Hardware	This User's manual
User's manual: Software	Detailed descriptions of the CPU and instruction set	RX Family Series User's manual: Software	R01US0032EJ
Application Note	Examples of applications and sample programs	—	—
Renesas Technical Update	Preliminary report on the specifications of a product, document, etc.	—	—

2. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

x.x.x ... Register

Address(es): xxxx xxxxxh

	b7	b6	b5	b4	b3	b2	b1	b0
	–	...	...	...	–	–	–	...
Value after reset:	x	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	...0	... Bit	0: ..... 1: Setting prohibited *3	R/W *1
b3 to b1	—	Reserved *2	The read value is 0. The write value should always be 0.	R/W
b4	...4	... Bit	0: 1:	R
b6, b5	...[1:0]	... Bit	0 0: ..... 0 1: ..... Settings other than above are prohibited. *3	R/(W) *
b7	—	Reserved	The read value is undefined. Writing to this bit has no effect.	R

(1) R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable. However, writing to this bit or field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit or field is readable. Writing to this bit or field has no effect.

(2) Reserved. Make sure to use the specified value when writing to this bit or field; otherwise, the correct operation is not guaranteed.

(3) Setting prohibited. The correct operation is not guaranteed if such a setting is performed.

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Contents

100-MHz 32-bit RX MCU, on-chip FPU, 165 DMIPS, Two 12-bit ADCs (three S/H circuits, double data registers, amplifier, comparator), one 10-bit ADC, simultaneous sampling on 7 channels using three ADCs, 100 MHz PWM (2 three-phase complementary channels + 4 single-phase complementary channels or 3 three-phase complementary channels + 1 single-phase complementary channel)

Features

■ 32-bit RX CPU core
- Max. operating frequency: 100 MHz
  Capable of 165 DMIPS in operation at 100 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- Two types of debugging interfaces: JTAG and FINE (two-line)

■ Low-power design and architecture
- Single 3.3-V supply or single 5-V supply; 3.3-V products can be used with a 5-V analog power supply
- Four low-power modes

■ On-chip main flash memory, no wait states
- 100-MHz operation, 10-ns read cycle (no wait states)
- Max. 512 Kbytes
- User code is programmable by USB, SCI, or JTAG.

■ On-chip data flash memory
- Max. 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM, no wait states
- Max. 48 Kbytes
- For instructions and operands

■ DMA
- DMA: Incorporates four channels
- DTC: A single unit can handle transfer on multiple channels.

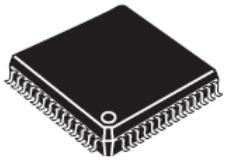
■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External crystal oscillator or internal PLL for operation at 4 to 12.5 MHz
- Internal 125-kHz LOCO
- Dedicated 125-kHz LOCO for the IWDT

■ Independent watchdog timer
- 125-kHz LOCO clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stop detection, frequency measurement, CRC, IWDT, self-diagnostic function for the A/D converter, etc.

■ External address space
- 4 CS areas (4 × 1 Mbyte)
- Multiplexed address data or separate address lines are selectable per area.
- 8- or 16-bit bus space is selectable per area.



PLQP0144KA-A 20 × 20mm, 0.5mm pitch
PLQP0120KA-A 16 × 16mm, 0.5mm pitch
PLQP0112JA-A 20 × 20mm, 0.65mm pitch
PLQP0100KB-A 14 × 14mm, 0.5mm pitch
PLQP0064KB-A 10 × 10mm, 0.5mm pitch
PLQP0048KB-A 7 × 7mm, 0.5mm pitch

■ Up to 11 communications interfaces
- USB 2.0 full-speed function interface (1 channel)
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (1 channel)
- SCI with multiple functionalities (5 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simple SPI, simple I^2C, and extended serial mode.
- I^2C bus interface for SMBus (2 channels)
- RSPI for high-speed transfer (2 channels)

■ Up to twenty 16-bit timers
- 16-bit MTU3: 100-MHz operation, input capture, output compare, three-phase complementary PWM waveform output (2 channels), phase-counting mode (8 channels); complementary PWM does not burden the CPU.
- 16-bit GPT: 100-MHz operation, input capture, output compare, 4-channel single-phase complementary PWM waveform output or 1-channel three-phase complementary + 1-channel single-phase complementary output, interlocking with comparator (counter operation, PWM negation control), detection of abnormal oscillation frequencies (useful for IEC60730 compliance)
  (8 channels); complementary PWM does not burden the CPU.
- 16-bit CMT (4 channels)

■ Generation of delays in PWM waveforms (for products with the product ID code 1)
- The timing with which signals on the 16-bit GPT PWM output pin rise and fall can be controlled with an accuracy of up to 312 ps (in operation at 100 MHz).

■ Two A/D converters for 1-MHz operation, total of 8 channels
- Simultaneous sampling on 7 channels is possible with three units.
- Self-diagnosis function (useful for IEC60730 compliance)
- Two 12-bit ADCs: three sample-and-hold circuits, double data registers, amplifier, comparator (8 channels)
- One 10-bit ADC (12 channels)

■ One A/D converter for 2-MHz operation, total of 20 channels
- One 10-bit ADC (20 channels)

■ 10-bit D/A converter: 2 channels

■ Digital Power Supply Controller-Dedicated Calculation Function (for products with product ID code 1)
- 16-bit fixed-point calculation function that handles compensatory calculations in the method of digital control for switched-mode power supplies.

■ Register write protection function can protect values in important registers against overwriting.

■ Up to 110 pins for GPIO
- Open drain, switchable driving ability

■ Operating temp. range
- –40°C to +85°C
- –40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.
Table 1.1 shows an outline of the maximum specifications, and the available peripheral modules and number of channels differ according to the number of pins on the package and the ROM capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/7)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision floating point (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 512 Kbytes, 384 Kbytes, 256 Kbytes, 64 Kbytes, 48 Kbytes, 32 Kbytes • 100 MHz, no-wait access • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. • Off-board programming: Programs can be modified using parallel programmer. (only in 144-, 120-, 112- and 100-pin versions)
	RAM	• Capacity: 48 Kbytes, 32 Kbytes, 24 Kbytes, 8 Kbytes • 100 MHz, no-wait access
	E^2 data flash	• Capacity: 32 Kbytes, 8 Kbytes • Programming/erasing: 100,000 times • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. Programming from the user program is possible.
MCU operating modes		[144-, 120-, 112- and 100-pin versions] Single-chip mode, on-chip ROM enabled extended mode, on-chip ROM disabled extended mode (switchable by software) [64- and 48-pin versions] Single-chip mode

Table 1.1 Outline of Specifications (2/7)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT • Main-clock oscillation stop detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), FlashIF clock (FCLK) and S12AD clock (PCLKD). The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Multi-function timer pulse unit 3 and general PWM timer run in synchronization with PCLKA: Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLKB): Up to 50 MHz Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz 10-bit A/D converter runs in synchronization with the AD clock (PCLKC): Up to 100 MHz 12-bit A/D converter runs in synchronization with the S12AD clock (PCLKD): Up to 50 MHz
Clock	Clock frequency accuracy measurement circuit (CAC)	The frequency of the following clocks can be measured; the main clock oscillator, PLL circuit, and IWDT-dedicated on-chip oscillator.
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: Up to 169 sources • External interrupts: Up to 8 (pins IRQ0 to IRQ7) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 1 Mbyte (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8- or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software interrupt activation register settings, external interrupts, and interrupt requests from peripheral functions

Table 1.1 Outline of Specifications (3/7)

Classification	Module/Function	Description
I/O ports	General I/O ports	• 144-pin LQFP I/O pins: 81 Input pins: 29 Open-drain outputs: 27 • 120-pin LQFP I/O pins: 72 Input pin: 21 Open-drain outputs: 26 • 112-pin LQFP I/O pins: 69 Input pins: 21 Open-drain outputs: 20 • 100-pin LQFP I/O pins: 57 Input pins: 21 Open-drain outputs: 16 • 64-pin LQFP I/O pins: 39 Input pins: 9 Open-drain outputs: 10 5-V tolerance: 39 • 48-pin LQFP I/O pins: 25 Input pins: 7 Open-drain outputs: 8 5-V tolerance: 25
Timers	Multi-function timer pulse unit 3 (MTU3)	• (16 bits × 8 channels) • Maximum of 16 pulse-input/output and 3 pulse-input possible • Select eight clocks from among ten count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (seven clocks for channel 1, four clocks for channel 5, and six clocks for channel 6 or 7) • 24 output compare/input capture registers • Counter-clearing operation (simultaneous clearing on compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous input and output to registers in synchronization with counter operations • Buffer operation specifiable • Capable of cascade-connected operation • Interrupts: 38 sources • Automatic transfer of register data • Pulse output modes Topple, PWM, complementary PWM, and reset-synchronous PWM modes • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins • Six pins for input from signal sources: POE0, POE4, POE8, POE10, POE11, and POE12 • Initiation on detection of short-circuited outputs (detection of PWM outputs having simultaneously become an active level.) • Initiation by comparator-detection, oscillation-stoppage detection, or software • Software control of the states of pins for output control can also be added.

Table 1.1 Outline of Specifications (4/7)

Classification	Module/Function	Description
Timers	General PWM timer (GPT)	• 16 bits x 8 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four count clocks (PCLKA/1, PCLKA/4, PCLKA/8, and PCLKA/16) for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Output of the internal comparator detection, software, and compare-match • The main clock can be used as a counter clock for measuring the timing of the edges of signals produced by frequency-dividing the dedicated clock signal for the IWDT (to detect abnormal oscillation). • A PWM delay with an accuracy of up to 1/32 times the period of the system clock (ICLK) can be generated to control the timing with which signals from the two PWM output pins from each of channels 0 to 3 rise and fall.
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256
Communication function	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Single port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus power mode are selectable • Supports the OTG (On-The-Go) • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIc, SCId)	• 5 channels (SCIc: 4 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format

Table 1.1 Outline of Specifications (5/7)

Classification	Module/Function	Description
Communication function	I^2C bus interfaces (RIIC)	• 2 channels Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps
	CAN module (CAN)	• 1 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interfaces (RSPI)	• 2 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • Max. transfer rate In master mode: [144-, 120-, 112- and 100-pin versions] 25 Mbps [64- and 48-pin versions] 12.5 Mbps In slave mode: 6.25 Mbps
12-bit A/D converter (S12ADB) [144-, 120-, 112- and 100-pin versions]		• 12 bits (4 channels x 2 unit) • 12-bit resolution • Conversion time 1.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 50 MHz, AVCC0 = 4.0 to 5.5 V) 2.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 25 MHz, AVCC0 = 3.0 to 3.6 V) • Operating modes Scan mode (single-cycle scan mode/continuous scan mode/group scan mode) Group A priority control (only for the group scan mode) • Sample-and-hold function A common sample-and-hold circuit for units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Double trigger mode (duplication of A/D converted data) • Input signal amplification function using programmable gain amplifier (three channels per unit) Amplification factors: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times, 5.0 times, 5.714 times, 6.667 times, 10.0 times, 13.333 times (total of 11 steps) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)

Table 1.1 Outline of Specifications (6/7)

Classification Module/Function	Description
12-bit A/D converter (S12ADB) [64- and 48-pin versions]	• 12 bits (8 channels x 1 unit) • 12-bit resolution • Conversion time 1.0 µs per channel (S12ADB clock: PCLKD (A/D conversion clock: ADCLK) = 50 MHz • Operating modes Scan mode (single scan mode / continuous scan mode / group scan mode) Group A priority control (group scan mode only) • Sample-and-hold function A common sample-and-hold circuit for units is included Separate sample-and-hold circuits are also included (three channels per unit) • Self-diagnosis function Three analog input voltages (VREFL0, VREFH0 × 1/2, VREFH0) can be generated internally by the self-diagnosis function. • Double trigger mode (double the results of A/D conversion) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)
10-bit A/D converter (ADA)	10 bits (20 channels × 1 unit) • 10-bit resolution • Conversion time 0.5 µs per channel (A/D conversion clock ADCLK = 100 MHz) • Two operating modes Single mode, scan mode • Scan mode Single-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for units is included • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • 8-bit precision output 2-bit right shifting for output of conversion results is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF)
D/A converter (DAa)	• 2 channels • 10-bit resolution • Output voltage: 0 V to VREF
CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Data operating circuit (DOC)	• Comparison, addition, and subtraction of 16-bit data
Digital power supply controller (DPC)	• Control parameters calculation unit of the digital switch-mode power supply systems. • Adopt robust control algorithm with high control stability • Results of measurement by the 10-bit A/D converter can be used in calculating the control parameters.
Operating frequency	Up to 100 MHz
Power supply voltage [144-, 120-, 112- and 100-pin versions]	• 3-V product VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V AVCC0 = AVCC = VREF = 3.0 to 3.6 V, or 4.0 to 5.5 V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 • 5-V product VCC = PLLVCC = 4.0 to 5.5 V VCC_USB = 3.0 to 3.6 V AVCC0 = AVCC = VREF = 4.0 to 5.5 V VREFH0 = 4.0 to AVCC0
Power supply voltage [64- and 48-pin versions]	VCC = 2.7 to 3.6 V, AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Table 1.1 Outline of Specifications (7/7)

Classification	Module/Function	Description
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C *1
Package		144-pin LQFP (PLQP0144KA-A (20 × 20, 0.5-mm pitch)) 120-pin LQFP (PLQP0120KA-A (16 × 16, 0.5-mm pitch)) 112-pin LQFP (PLQP0112JA-A (20 × 20, 0.65-mm pitch)) 100-pin LQFP (PLQP0100KB-A (14 × 14, 0.5-mm pitch)) 64-pin LQFP (PLQP0064KB-A (10 × 10, 0.5-mm pitch)) 48-pin LQFP (PLQP0048KB-A (07 × 07, 0.5-mm pitch))
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.2 Comparison of Functions for Different Packages

Functions			RX63T Group					
Package			**144 Pins**	**120 Pins**	**112 Pins**	**100 Pins**	**64 Pins**	**48 Pins**
External bus			16 bits				—	
External address space			1 Mbyte × 4 areas				—	
DMA	DMA controller (DMACA)		Ch. 0 to 3					
	Data transfer controller (DTCa)		Supported					
Interrupt controller (ICUb)	NMI pin		Supported					
	IRQ pin		Supported (x 8)				Supported (x 6)	
Timers	Multi-function timer pulse unit 3 (MTU3)*1		Ch. 0 to 7					
	General PWM timer (GPT)*1	Generation of delays in PWM, not supported	Ch. 0 to 7				Ch. 0 to 3	
		Generation of delays in PWM, supported	Ch. 0 to 3				—	
	Port output enable 3 (POE3)		Supported (POE pins × 6)			Supported (POE pins × 5)	Supported (POE pins × 4)	
	Compare match timer (CMT)		Ch. 0 to 3					
	Watchdog timer (WDTA)		Supported					
	Independent watchdog timer (IWDTa)		Supported					
Communication function	USB2.0 host/function module (USBa)		Ch. 0		—			
	Serial communications interfaces (SCIc)		Ch. 0 to 3			Ch. 0 to 2	Ch. 0, 1	
	Serial communications interfaces (SCId)		Ch. 12					
	I^2C bus interfaces (RIIC)		Ch. 0, 1		Ch. 0			
	Serial peripheral interfaces (RSPI)		Ch. 0, 1				Ch. 0	
	CAN module (CAN) (as an optional function)*1		Ch. 0				—	
12-bit A/D converter (S12ADB)			4 channels × 2 units				8 channels × 1 unit (AN000 to 007)	8 channels × 1 unit (AN000 to 004, 007)
	Three-channel simultaneous sampling function		2 units				1 unit	
	Programmable gain amplifier		3 channels × 2 units				—	
	Window comparator		3 channels × 2 units				3 channels × 1 unit	
10-bit A/D converter (ADA)			20 channels	12 channels			—	
D/A converter (DAa)			Ch. 0, 1				—	
Clock Frequency Accuracy Measurement Circuit			Supported					
Digital power supply controller (DPC)*2			Supported				Not supported	

Note 1. For the MTU3 and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. For details, see Table 1.3.

Note 2. Not provided for the product ID code O.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products (1/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TEADFB	R5F563TEADFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TEADFB	R5F563TEADFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFA	R5F563TEADFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFA	R5F563TEADFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFH	R5F563TEADFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFH	R5F563TEADFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFP	R5F563TEADFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFP	R5F563TEADFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCADFB	R5F563TCADFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFB	R5F563TCADFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFA	R5F563TCADFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFA	R5F563TCADFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFH	R5F563TCADFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFH	R5F563TCADFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFP	R5F563TCADFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFP	R5F563TCADFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBADFB	R5F563TBADFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFB	R5F563TBADFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFA	R5F563TBADFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFA	R5F563TBADFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFH	R5F563TBADFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFH	R5F563TBADFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFP	R5F563TBADFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFP	R5F563TBADFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEDDFB	R5F563TEDDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFA	R5F563TEDDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFH	R5F563TEDDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFP	R5F563TEDDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module not included		

Table 1.3 List of Products (2/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TCDDFB	R5F563TCDDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module not included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TCDDFA	R5F563TCDDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCDDFH	R5F563TCDDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCDDFP	R5F563TCDDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TBDDFB	R5F563TBDDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFA	R5F563TBDDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFH	R5F563TBDDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFP	R5F563TBDDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TEBDFB	R5F563TEBDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	
	R5F563TEBDFB	R5F563TEBDFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFA	R5F563TEBDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFA	R5F563TEBDFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFH	R5F563TEBDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFH	R5F563TEBDFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFP	R5F563TEBDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFP	R5F563TEBDFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCBDFB	R5F563TCBDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFB	R5F563TCBDFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFA	R5F563TCBDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFA	R5F563TCBDFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFH	R5F563TCBDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFH	R5F563TCBDFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFP	R5F563TCBDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFP	R5F563TCBDFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBBDFB	R5F563TBBDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFB	R5F563TBBDFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFA	R5F563TBBDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFA	R5F563TBBDFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFH	R5F563TBBDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFH	R5F563TBBDFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		

Table 1.3 List of Products (3/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TBBDFP	R5F563TBBDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TBBDFP	R5F563TBBDFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEEDFB	R5F563TEEDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFA	R5F563TEEDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFH	R5F563TEEDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFP	R5F563TEEDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TCEDFB	R5F563TCEDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFA	R5F563TCEDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFH	R5F563TCEDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFP	R5F563TCEDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TBEDFB	R5F563TBEDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFA	R5F563TBEDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFH	R5F563TBEDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFP	R5F563TBEDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563T6EDFM	R5F563T6EDFM#V0	PLQP0064KB-A	64 Kbytes	8 Kbytes	CAN module not included	VCC/ PLLVCC 2.7 to 3.6V AVCC0 3.0 to 3.6V	
	R5F563T5EDFM	R5F563T5EDFM#V0	PLQP0064KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EDFM	R5F563T4EDFM#V0	PLQP0064KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563T6EDFL	R5F563T6EDFL#V0	PLQP0048KB-A	64 Kbytes	8 Kbytes	CAN module not included		
	R5F563T5EDFL	R5F563T5EDFL#V0	PLQP0048KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EDFL	R5F563T4EDFL#V0	PLQP0048KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563TEAGFB	R5F563TEAGFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +105°C (G Version)*1
	R5F563TEAGFA	R5F563TEAGFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEAGFH	R5F563TEAGFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEAGFP	R5F563TEAGFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCAGFB	R5F563TCAGFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFA	R5F563TCAGFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFH	R5F563TCAGFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFP	R5F563TCAGFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBAGFB	R5F563TBAGFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		

Table 1.3 List of Products (4/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TBAGFA	R5F563TBAGFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +105°C (G Version)*1
	R5F563TBAGFH	R5F563TBAGFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBAGFP	R5F563TBAGFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEBGFB	R5F563TEBGFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	
	R5F563TEBGFA	R5F563TEBGFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBGFH	R5F563TEBGFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBGFP	R5F563TEBGFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCBGFB	R5F563TCBGFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFA	R5F563TCBGFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFH	R5F563TCBGFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFP	R5F563TCBGFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBBGFB	R5F563TBBGFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFA	R5F563TBBGFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFH	R5F563TBBGFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFP	R5F563TBBGFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563T6EGFM	R5F563T6EGFM#V0	PLQP0064KB-A	64 Kbytes	8 Kbytes	CAN module not included	VCC/ PLLVCC 2.7 to 3.6V AVCC0 3.0 to 3.6V	
	R5F563T5EGFM	R5F563T5EGFM#V0	PLQP0064KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EGFM	R5F563T4EGFM#V0	PLQP0064KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563T6EGFL	R5F563T6EGFL#V0	PLQP0048KB-A	64 Kbytes	8 Kbytes	CAN module not included		
	R5F563T5EGFL	R5F563T5EGFL#V0	PLQP0048KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EGFL	R5F563T4EGFL#V0	PLQP0048KB-A	32 Kbytes	8 Kbytes	CAN module not included		

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note: • The products with the product ID code 1 (ex. R5F563TEADFB#V1) are the revised version to the specification constraints of technical update TX-RX*-A84A / E described.

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

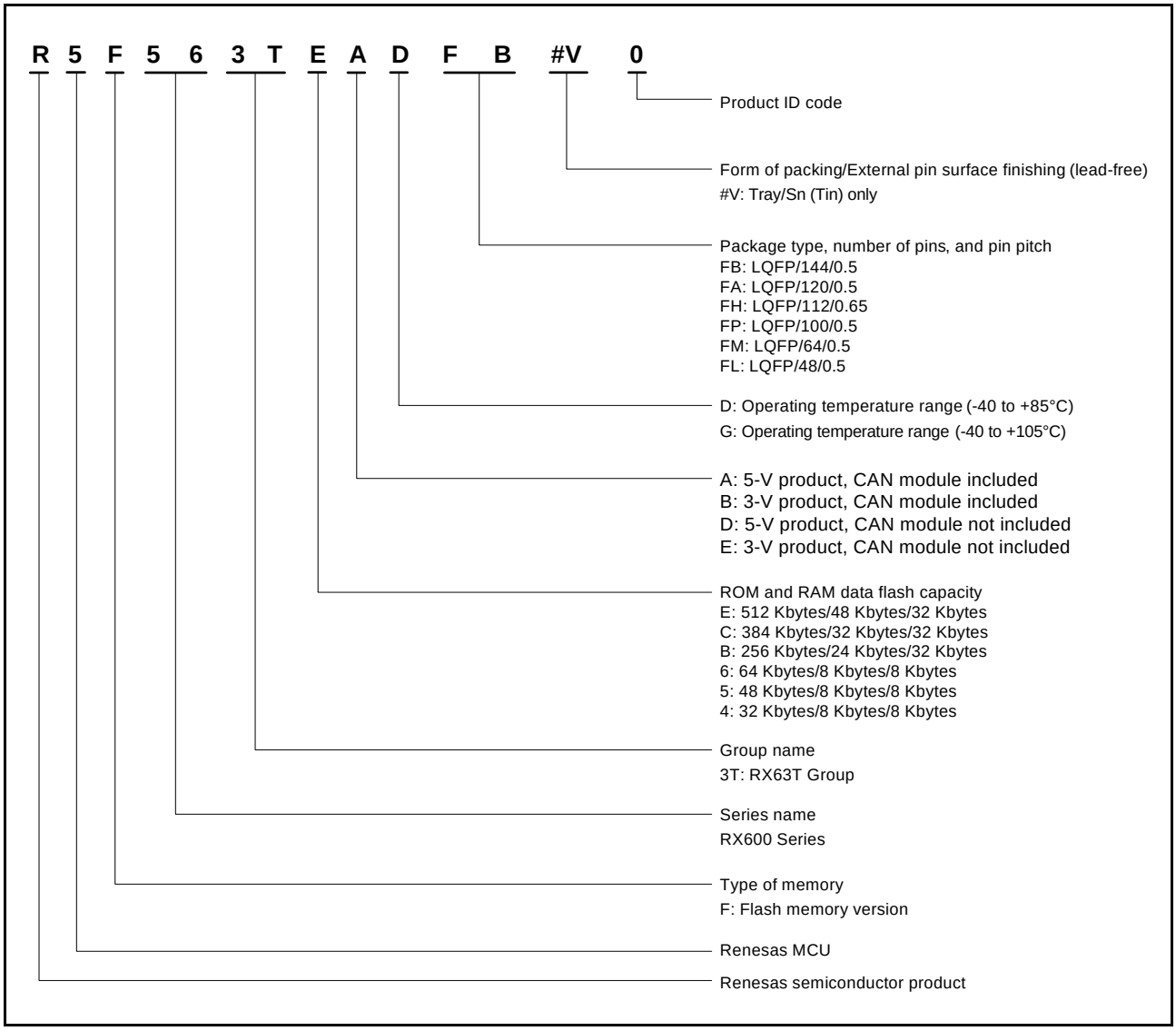
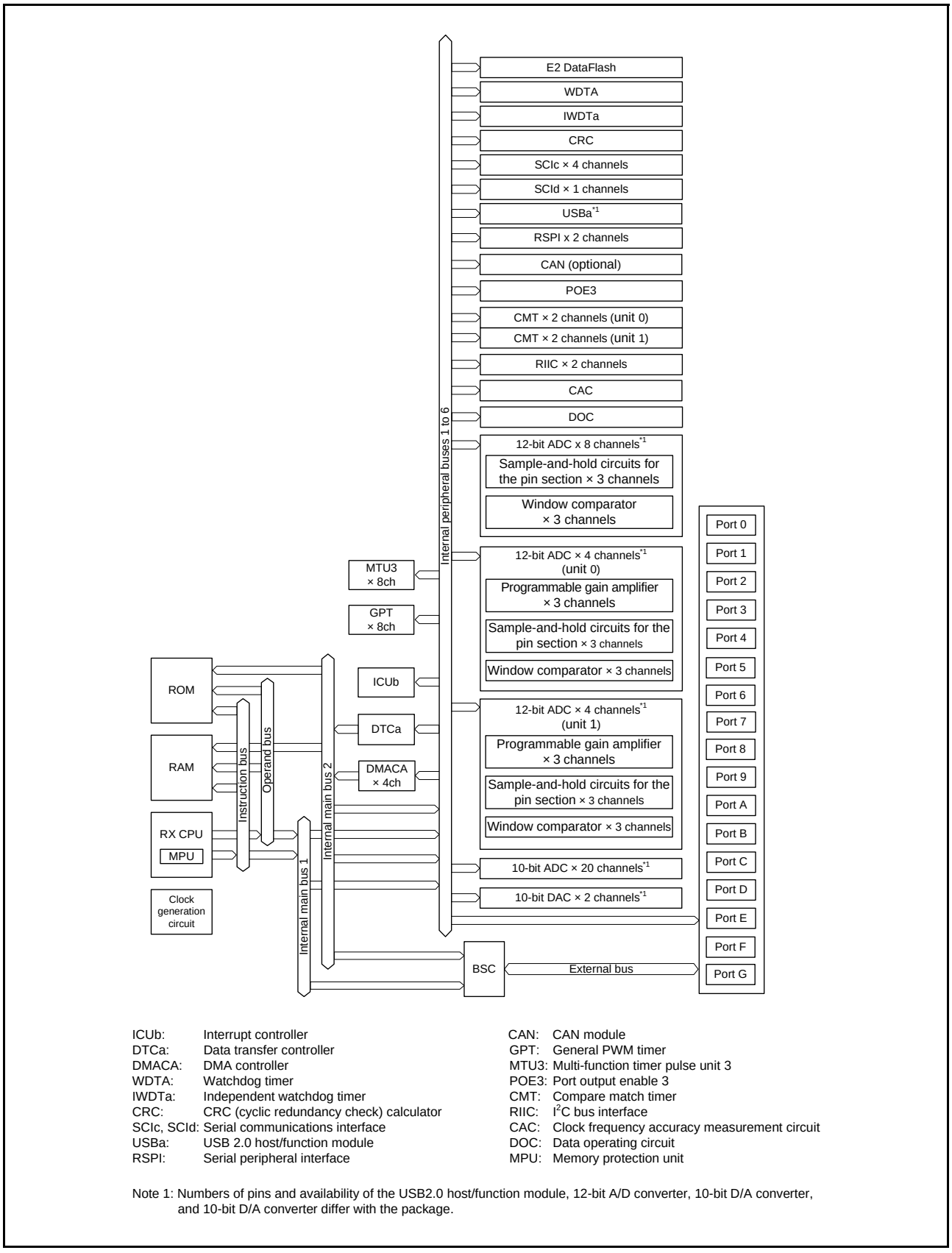


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
USBa: USB 2.0 host/function module
RSPI: Serial peripheral interface
CAN: CAN module
GPT: General PWM timer
MTU3: Multi-function timer pulse unit 3
POE3: Port output enable 3
CMT: Compare match timer
RIIC: I^2C bus interface
CAC: Clock frequency accuracy measurement circuit
DOC: Data operating circuit
MPU: Memory protection unit

Note 1: Numbers of pins and availability of the USB2.0 host/function module, 12-bit A/D converter, 10-bit D/A converter, and 10-bit D/A converter differ with the package.

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/5)

Classifications	Pin Name	I/O	Description
Power supply	VCC	—	Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VCL	—	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VSS	—	Ground pin. Connect it to the system power supply (0 V)
	PLLVCC	—	Power supply pin. Connect it to the system power supply.
	PLLVSS	—	Ground pin. Connect it to the system power supply (0 V)
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices
Clock frequency accuracy measurement	CACREF	Input	Input for the trigger signal in measuring accuracy of the clock frequency
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on these pins must not be changed during operation
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid
	TRDATA0 to TRDATA3	Output	These pins output the trace information
Address bus	A0 to A19	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS3#	Output	Select signals for CS areas

Table 1.4 Pin Functions (2/5)

Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pin
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/ PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock
Port output enable 3	POE0#, POE4# POE8#, POE10# POE11#, POE12#	Input	Input pins for request signals to place the MTU/GPT large-current pins in the high impedance state
General PWM timer	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins.
	GTETRG0	Input	External trigger input pin for the GPT0 to GPT3
	GTIOC4A, GTIOC4B	I/O	The GPT4.GTGRA and GPT4.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC5A, GTIOC5B	I/O	The GPT5.GTGRA and GPT5.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC6A, GTIOC6B	I/O	The GPT6.GTGRA and GPT6.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC7A, GTIOC7B	I/O	The GPT7.GTGRA and GPT7.GTGRB input capture input/output compare output/PWM output pins.
	GTETRG1	Input	External trigger input pin for the GPT4 to GPT7

Table 1.4 Pin Functions (3/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIc)	Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for clock signals.
	RXD0, RXD1, RXD2, RXD3	Input	Input pins for data reception.
	TXD0, TXD1, TXD2, TXD3	Output	Output pins for data transmission.
	CTS0#, CTS1#, CTS2#, CTS3#	Input	Transmit/receive start control input pins
	RTS0#, RTS1#, RTS2#, RTS3#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL0, SSCL1, SSCL2, SSCL3	I/O	Input/output pins for the I^2C clock
	SSDA0, SSDA1, SSDA2, SSDA3	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for the clock
	SMISO0, SMISO1, SMISO2, SMISO3	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI2, SMOSI3	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS2#, SS3#	Input	Input pins for chip select signals
Serial communications interface (SCId)	Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL12	I/O	Input/output pins for the I^2C clock
	SSDA12	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for transfer data
I^2C bus interface	SCL, SCL0, SCL1	I/O	Clock input/output pin. N-channel open drain can directly drive buses.
	SDA, SDA0, SDA1	I/O	Data input/output pin. N-channel open drain can directly drive buses.

Table 1.4 Pin Functions (4/5)

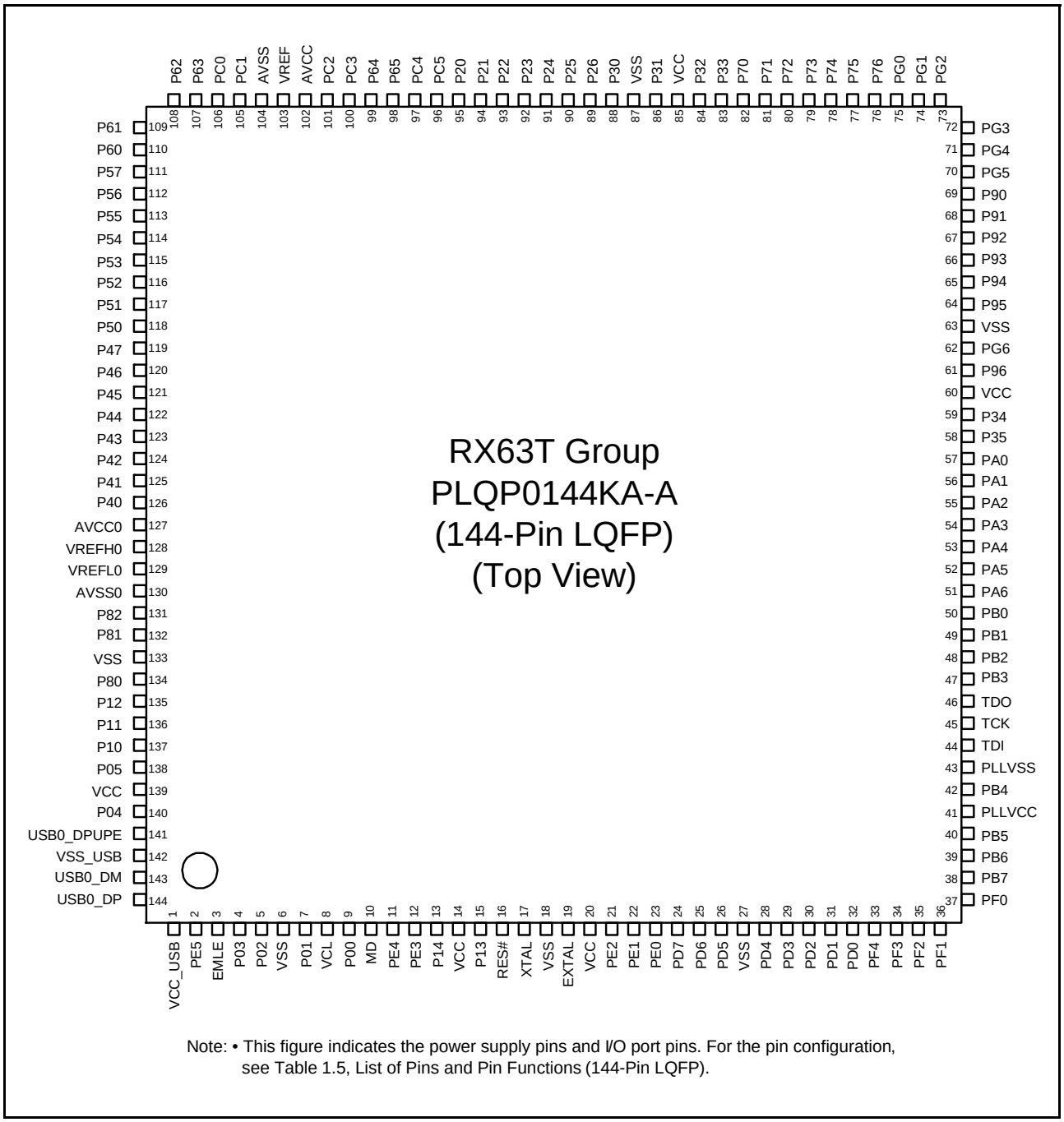
Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power supply pin for USB
	VSS_USB	Input	Ground pin for USB
	USB0_DP	I/O	USB internal transceiver D + input and output pins
	USB0_DM	I/O	USB internal transceiver D - input and output pins
	USB0_EXICEN	Output	Low power control signal for OTG chip
	USB0_VBUSEN	Output	Supply enable signal of VBUS (5 V) to OTG chip
	USB0_ID	Input	Mini AB connector ID input pin for use in OTG operation
	USB0_DPRPD	Output	D+ signal pull-down control pin for use during host operation
	USB0_DRPD	Output	D- signal pull-down control pin for use during host operation
	USB0_DPUPE	Output	D+ signal pull-up control pin for use during function operation
	USB0_VBUS	Input	Pin for monitoring USB cable connection
	USB0_OVRCURA, USB0_OVRCURB	Input	Pin for detecting external over current
CAN module	CRX1	Input	Input pins
	CTX1	Output	Output pins
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pins
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pins for slave selection
	SSLA1 to SSLA3 SSLB1 to SSLB3	Output	Output pins for slave selection
12-bit A/D converter	AN000 to AN007 AN100 to AN103	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
10-bit A/D converter	AN0 to AN19	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter
	ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the 10-bit A/D converter
Analog power supply	AVCC0	—	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	AVSS0	—	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	VREFH0	—	Reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	VREFL0	—	Reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	AVCC	—	Analog voltage supply pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply of the system if the A/D converter and the D/A converter are not to be used.
	AVSS	—	Ground pin for the 10-bit A/D converter and 10-bit D/A converter. Connect this pin to the power-supply ground for the system (0 V).
	VREF	—	Reference-voltage input pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply for the system if the A/D converter and the D/A converter are not to be used.

Table 1.4 Pin Functions (5/5)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P14	I/O	5-bit input/output pins
	P20 to P26	I/O	7-bit input/output pins
	P30 to P35	I/O	6-bit input/output pins
	P40 to P47	Input	8-bit input pins
	P50 to P57	Input	8-bit input pins
	P60 to P65	Input	6-bit input pins
	P70 to P76	I/O	7-bit input/output pins
	P80 to P82	I/O	3-bit input/output pins
	P90 to P96	I/O	7-bit input/output pins
	PA0 to PA6	I/O	7-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC5	Input	6-bit input pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0, PE1, PE3 to PE5	I/O	6-bit input/output pins
	PE2	Input	1-bit input pin
	PF0 to PF4	I/O	5-bit input/output pins
	PG0 to PG6	I/O	7-bit input/output pins

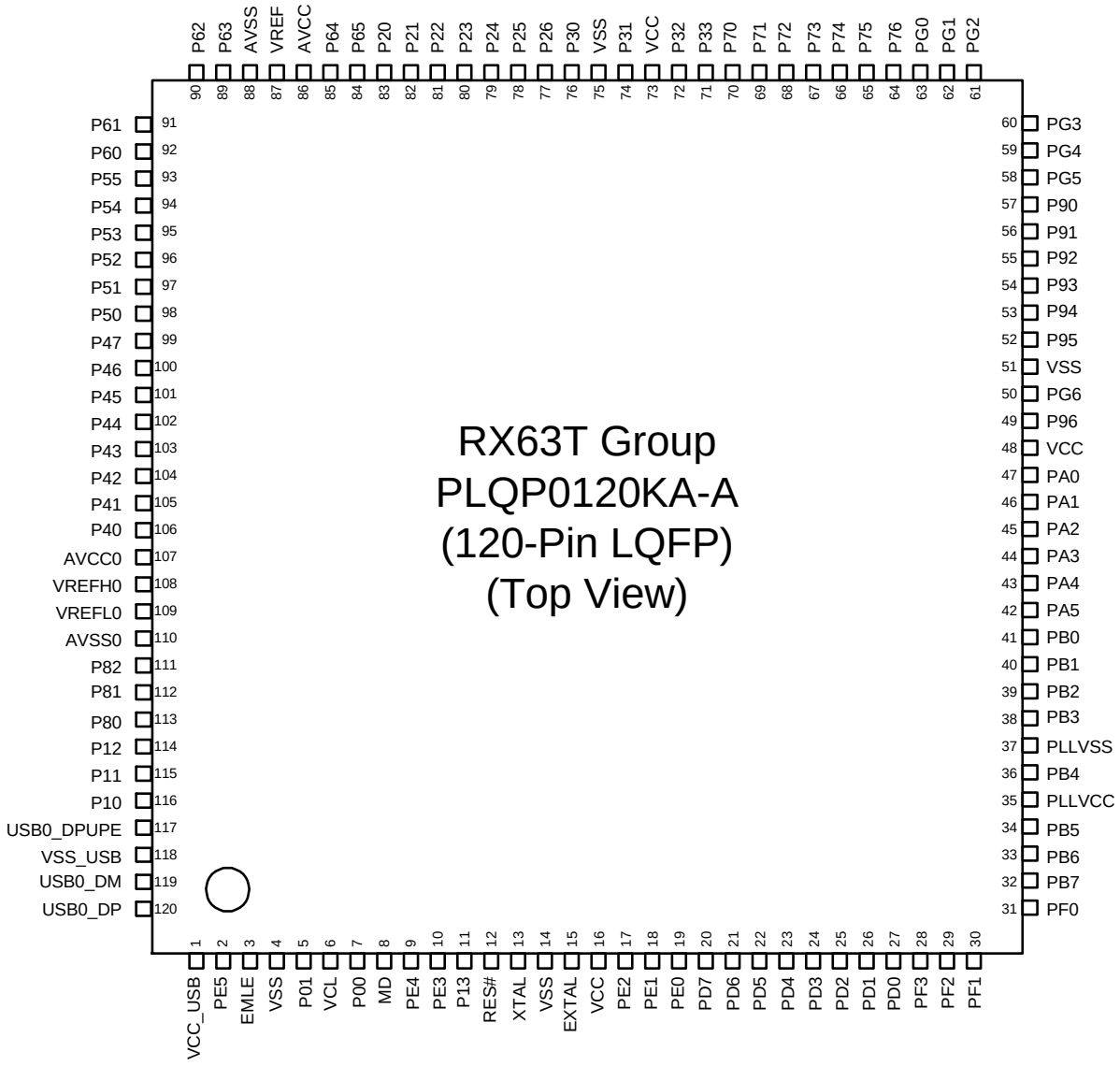
1.5 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.



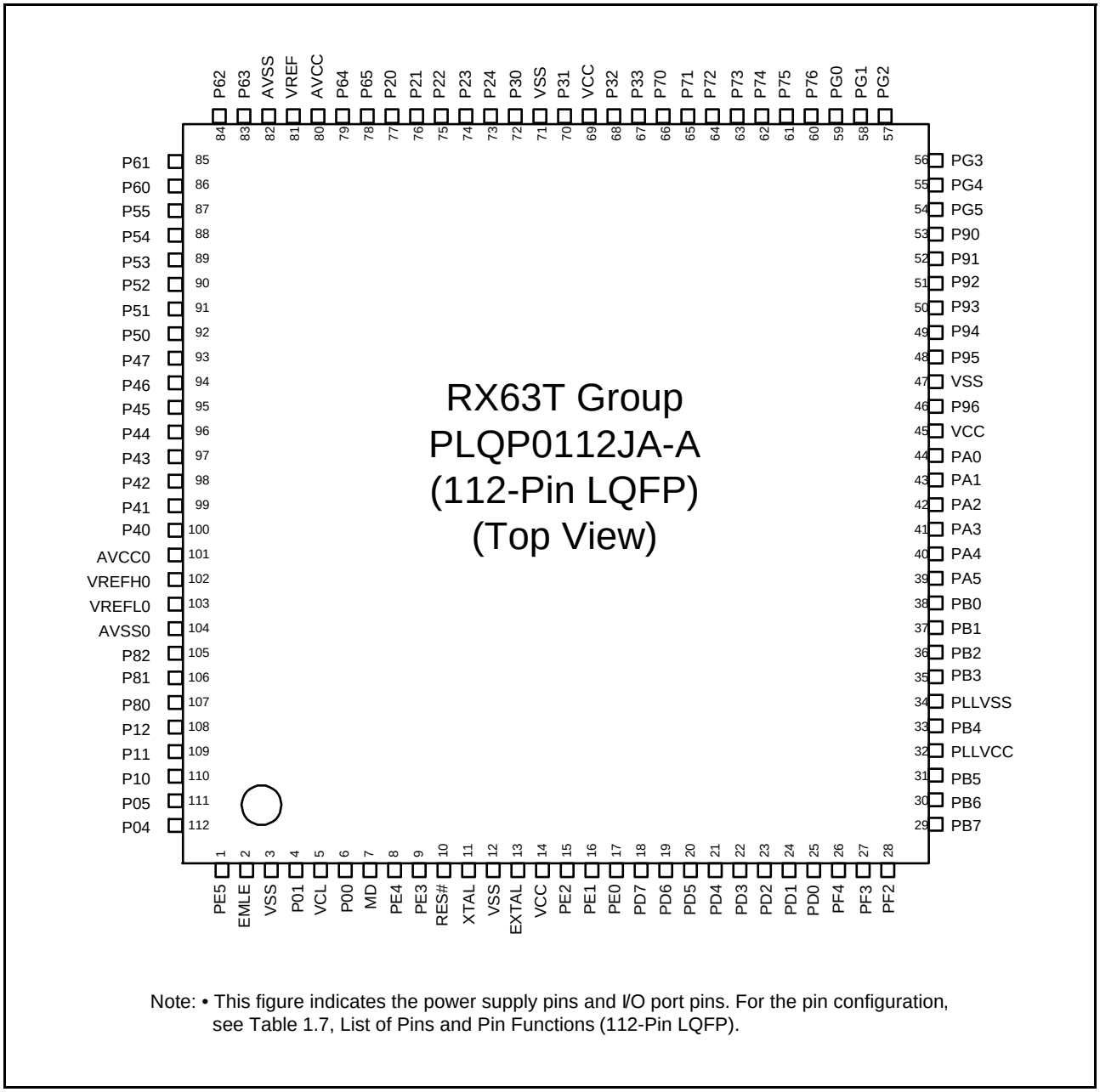
Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (144-Pin LQFP).

Figure 1.3 Pin Assignment (144-Pin LQFP)



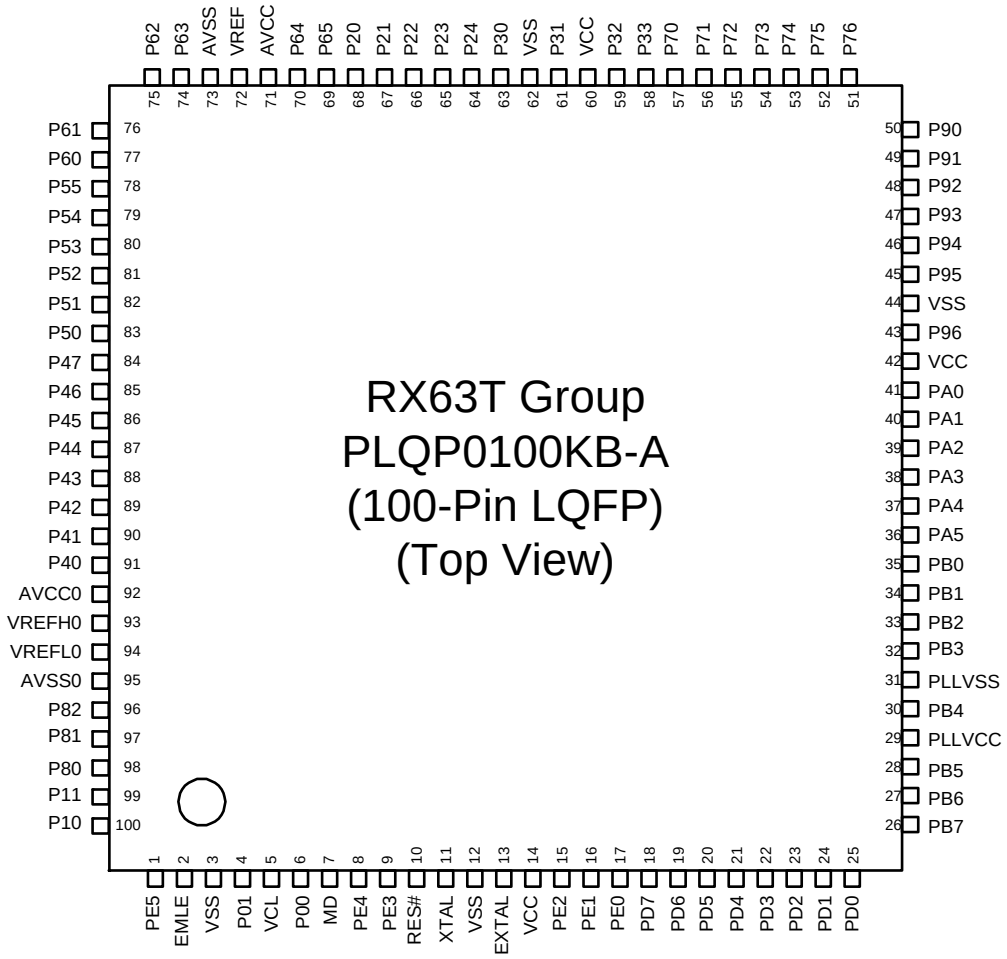
Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (120-Pin LQFP).

Figure 1.4 Pin Assignment (120-Pin LQFP)



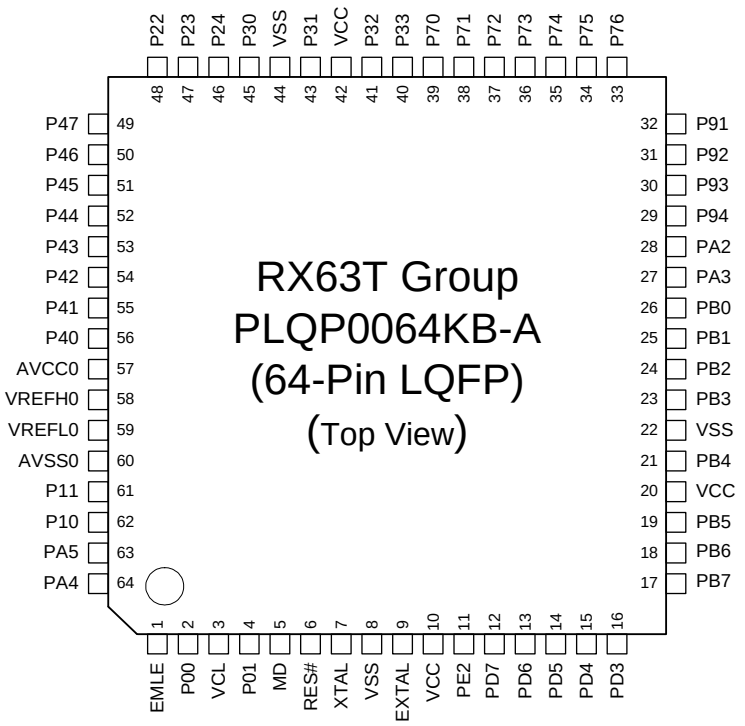
Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (112-Pin LQFP).

Figure 1.5 Pin Assignment (112-Pin LQFP)



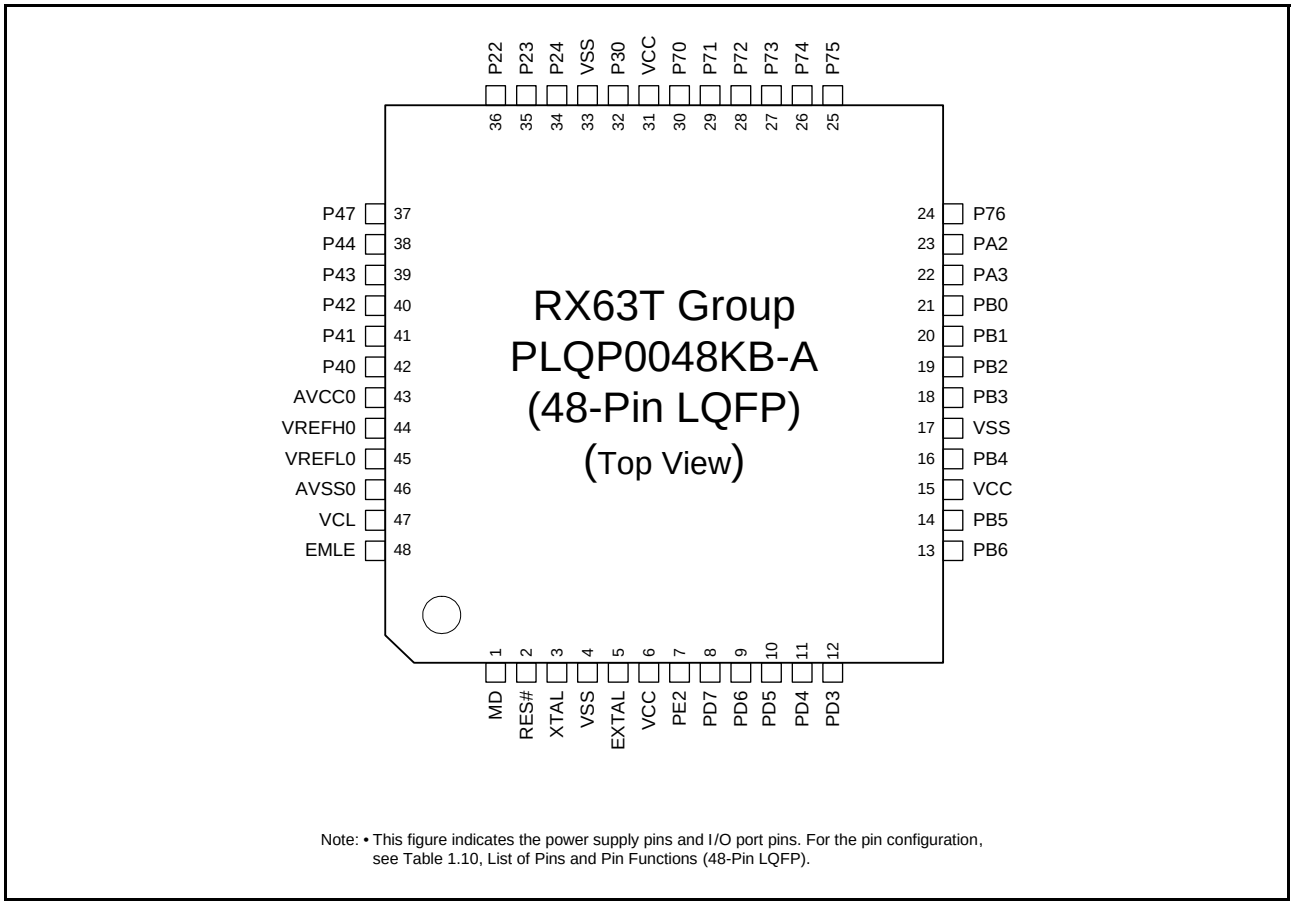
Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pins and Pin Functions (100-Pin LQFP).

Figure 1.6 Pin Assignment (100-Pin LQFP)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pins and Pin Functions (64-Pin LQFP).

Figure 1.7 Pin Assignment (64-Pin LQFP)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (48-Pin LQFP).

Figure 1.8 Pin Assignment (48-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	TRSYNC	P03			RXD2/SMISO2/SSCL2	IRQ7	
5	TRDATA3	P02			TXD2/SMOSI2/SSDA2		
6	VSS						
7		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
8	VCL						
9		P00	CS1#	CACREF			
10	MD/FINED						
11		PE4	A10	POE10#/MTCLKC		IRQ1	
12		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
13	TRDATA2	P14			SCK2		
14	VCC						
15		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
16	RES#						
17	XTAL						
18	VSS						
19	EXTAL						
20	VCC						
21		PE2		POE10#		NMI	
22		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
23		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
24		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
25		PD6		GTIOC0B	SSLA0/SSLB0		
26		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
27	VSS						
28		PD4		GTIOC1B	SCK1		
29		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
30		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
31		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
32		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
33		PF4	CS3#				
34		PF3			TXD1/SMOSI1/SSDA1		
35		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
36	TRST#	PF1					
37	TMS	PF0					
38		PB7	A19		SCK12		

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (2/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
39		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
40		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/ CTX1		
41	PLLVCC						
42		PB4	A16	POE8#/ GTETRG0		IRQ3-DS	
43	PLLVSS						
44	TDI				RXD1*1		
45	TCK/FINEC						
46	TDO				TXD1*1		
47		PB3	A15	MTIOC0A/CACREF	SCK0		
48		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
49		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
50		PB0	A14	MTIOC0D	MOSIA/MOSIB		
51	TRDATA1	PA6	CS3#		CTS3#/RTS3#/SS3#		
52		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
53		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/SMOSI0/ RSPCKA/RSPCKB		ADTRG0#
54		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
55		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
56		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SMOSI2/ SSLA2/SSLB2		
57		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
58	TRDATA0	P35			TXD3/SMOSI3/SSDA3		
59	TRCLK	P34		GTETRG1	RXD3/SMISO3/SSCL3	IRQ3	
60	VCC						
61		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
62		PG6	CS2#		SCK1		
63	VSS						
64		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
65		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
66		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
67		P92		MTIOC6D/GTIOC4B			
68		P91		MTIOC7C/GTIOC5B			
69		P90		MTIOC7D/GTIOC6B			
70		PG5		POE12#	SCK3		ADTRG#
71		PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (3/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
72		PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
73		PG2			SCK2	IRQ2	
74		PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
75		PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
76		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
77		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
78		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
79		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
80		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
81		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
82		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
83		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
84		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
85	VCC						
86		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
87	VSS						
88		P30	D10/[A10/D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
89		P26	CS0#		TXD1/SMOSI1/SSDA1/SDA1		
90		P25	CS1#		SCK1/SCL1		
91		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB	IRQ4	
92		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
93		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
94		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
95		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
96		PC5					AN19
97		PC4					AN18
98		P65	A0/BC0#				AN5
99		P64	A1				AN4
100		PC3					AN17
101		PC2					AN16
102	AVCC						
103	VREF						
104	AVSS						
105		PC1					AN15
106		PC0					AN14
107		P63	A2				AN3
108		P62	A3				AN2
109		P61	A4				AN1

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (4/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
110		P60	A5				AN0
111		P57					AN13
112		P56					AN12
113		P55					AN11/DA1
114		P54					AN10/ DA0
115		P53	A6				AN9
116		P52	A7				AN8
117		P51					AN7
118		P50					AN6
119		P47					AN103/ CVREFH
120		P46					AN102
121		P45					AN101
122		P44					AN100
123		P43					AN003/ CVREFL
124		P42					AN002
125		P41					AN001
126		P40					AN000
127	AVCC0						
128	VREFH0						
129	VREFL0						
130	AVSS0						
131		P82	WAIT#	MTIC5U	SCK12	IRQ3	
132		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
133	VSS						
134		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
135		P12	CS3#		USB0_DPRPD		
136		P11	ALE	MTCLKC		IRQ1-DS	
137		P10		MTCLKD		IRQ0-DS	
138		P05	CS2#/WAIT#				
139	VCC						
140		P04					
141					USB0_DPUPE		
142	VSS_USB						
143					USB0_DM		
144					USB0_DP		

Note 1. Available for use as SCI pin only in boot mode.

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (1/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	VSS						
5		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
6	VCL						
7		P00	CS1#	CACREF			
8	MD/FINED						
9		PE4	A10	POE10#/MTCLKC		IRQ1	
10		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
11		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
12	RES#						
13	XTAL						
14	VSS						
15	EXTAL						
16	VCC						
17		PE2		POE10#		NMI	
18		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
19		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
20	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
21	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
22	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
23	TCK/FINEC	PD4		GTIOC1B	SCK1		
24	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
25		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
26		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
27		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
28		PF3			TXD1/SMOSI1/SSDA1		
29		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
30		PF1					
31		PF0					
32		PB7	A19		SCK12		
33		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
34		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
35	PLLVCC						
36		PB4	A16	POE8#/GTETRG0		IRQ3-DS	

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (2/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
37	PLLVSS						
38		PB3	A15	MTIOC0A/CACREF	SCK0		
39		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
40		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
41		PB0	A14	MTIOC0D	MOSIA/MOSIB		
42		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
43		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
44		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
45		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
46		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
47		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
48	VCC						
49		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
50		PG6	CS2#		SCK1		
51	VSS						
52		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
53		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
54		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
55		P92		MTIOC6D/GTIOC4B			
56		P91		MTIOC7C/GTIOC5B			
57		P90		MTIOC7D/GTIOC6B			
58	TRCLK	PG5		POE12#	SCK3		ADTRG#
59	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
60	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
61	TRDATA1	PG2			SCK2	IRQ2	
62	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
63	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
64		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
65		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
66		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
67		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
68		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
69		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
70		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
71		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
72		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
73	VCC						
74		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (3/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
75	VSS						
76		P30	D10/[A10/D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
77		P26	CS0#		TXD1/SMOSI1/SSDA1/SDA1		
78		P25	CS1#		SCK1/SCL1		
79		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB	IRQ4	
80		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
81		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
82		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
83		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
84		P65	A0/BC0#				AN5
85		P64	A1				AN4
86	AVCC						
87	VREF						
88	AVSS						
89		P63	A2				AN3
90		P62	A3				AN2
91		P61	A4				AN1
92		P60	A5				AN0
93		P55					AN11/DA1
94		P54					AN10/DA0
95		P53	A6				AN9
96		P52	A7				AN8
97		P51					AN7
98		P50					AN6
99		P47					AN103/CVREFH
100		P46					AN102
101		P45					AN101
102		P44					AN100
103		P43					AN003/CVREFL
104		P42					AN002
105		P41					AN001
106		P40					AN000
107	AVCC0						
108	VREFH0						
109	VREFL0						
110	AVSS0						

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (4/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
111		P82	WAIT#	MTIC5U	SCK12	IRQ3	
112		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
113		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
114		P12	CS3#		USB0_DPRPD		
115		P11	ALE	MTCLKC		IRQ1-DS	
116		P10		MTCLKD		IRQ0-DS	
117					USB0_DPUPE		
118	VSS_USB						
119					USB0_DM		
120					USB0_DP		

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (1/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19		PD6		GTIOC0B	SSLA0/SSLB0		
20		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21		PD4		GTIOC1B	SCK1		
22		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26	TDI	PF4	CS3#		RXD1*1		
27	TCK/FINEC	PF3			TXD1/SMOSI1/SSDA1		
28	TDO	PF2	CS1#		RXD1/SMISO1/ SSCL1/TXD1*1	IRQ5	
29		PB7	A19		SCK12		
30		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
31		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
32	PLLVCC						
33		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
34	PLLVSS						
35		PB3	A15	MTIOC0A/CACREF	SCK0		
36		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
37		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
38		PB0	A14	MTIOC0D	MOSIA/MOSIB		
39		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
40		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
41		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
42		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
43		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
44		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
45	VCC						
46		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
47	VSS						
48		P95		MTIOC6B/ GTIOC4A	TXD1/SMOSI1/SSDA1		
49		P94		MTIOC7A/ GTIOC5A	CTS1#/RTS1#/SS1#		
50		P93		MTIOC7B/ GTIOC6A	CTS2#/RTS2#/SS2#		
51		P92		MTIOC6D/GTIOC4B			
52		P91		MTIOC7C/GTIOC5B			
53		P90		MTIOC7D/GTIOC6B			
54	TRCLK	PG5		POE12#	SCK3		ADTRG#
55	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
56	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
57	TRDATA1	PG2			SCK2	IRQ2	
58	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
59	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
60		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
61		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
62		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
63		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
64		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
65		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
66		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
67		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
68		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
69	VCC						
70		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
71	VSS						
72		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
73		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (3/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
74		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
75		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
76		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
77		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
78		P65	A0/BC0#				AN5
79		P64	A1				AN4
80	AVCC						
81	VREF						
82	AVSS						
83		P63	A2				AN3
84		P62	A3				AN2
85		P61	A4				AN1
86		P60	A5				AN0
87		P55					AN11/DA1
88		P54					AN10/DA0
89		P53	A6				AN9
90		P52	A7				AN8
91		P51					AN7
92		P50					AN6
93		P47					AN103/CVREFH
94		P46					AN102
95		P45					AN101
96		P44					AN100
97		P43					AN003/CVREFL
98		P42					AN002
99		P41					AN001
100		P40					AN000
101	AVCC0						
102	VREFH0						
103	VREFL0						
104	AVSS0						
105		P82	WAIT#	MTIC5U	SCK12	IRQ3	
106		P81	A8	MTIC5V	TXD12/SMOSI12/SSDA12/TXDX12/SIOX12		
107		P80	A9	MTIC5W	RXD12/SMISO12/SSCL12/RXDX12	IRQ5	
108		P12	CS3#				
109		P11	ALE	MTCLKC		IRQ1-DS	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (4/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
110		P10		MTCLKD		IRQ0-DS	
111	TRST#	P05	WAIT#/CS2#				
112	TMS	P04					

Note 1. Available for use as SCI pin only in boot mode.

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
20	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21	TCK/FINEC	PD4		GTIOC1B	SCK1		
22	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26		PB7	A19		SCK12		
27		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
28		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
29	PLLVCC						
30		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
31	PLLVSS						
32		PB3	A15	MTIOC0A/CACREF	SCK0		
33		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
34		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
35		PB0	A14	MTIOC0D	MOSIA/MOSIB		
36		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (3/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
71	AVCC						
72	VREF						
73	AVSS						
74		P63	A2				AN3
75		P62	A3				AN2
76		P61	A4				AN1
77		P60	A5				AN0
78		P55					AN11/DA1
79		P54					AN10/ DA0
80		P53	A6				AN9
81		P52	A7				AN8
82		P51					AN7
83		P50					AN6
84		P47					AN103/ CVREFH
85		P46					AN102
86		P45					AN101
87		P44					AN100
88		P43					AN003/ CVREFL
89		P42					AN002
90		P41					AN001
91		P40					AN000
92	AVCC0						
93	VREFH0						
94	VREFL0						
95	AVSS0						
96		P82	WAIT#	MTIC5U	SCK12	IRQ3	
97		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
98		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
99		P11	ALE	MTCLKC		IRQ1-DS	
100		P10		MTCLKD		IRQ0-DS	

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
1	EMLE							
2		P00		GTIOC3A	CTS0# RTS0# SS0#		IRQ2-DS	
3	VCL							
4		P01		GTIOC3B CACREF			IRQ4-DS	
5	MD FINED							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2	POE10#				NMI	
12	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
13	TMS	PD6		GTIOC0B				
14	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
15	TCK FINEC	PD4		GTIOC1B	SCK1			
16	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
17		PB7		GTIOC2B	SCK12			
18		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
19		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
20	VCC							
21		PB4	POE8#	GTETRG	CTS12# RTS12# SS12#		IRQ3-DS	
22	VSS							
23		PB3		MTIOC0A MTCLKA CACREF	SCK0			
24		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
25		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
26		PB0		MTIOC0D		MOSIA		

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (2/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
27		PA3		MTIOC2A		SSLA0		
28		PA2		MTIOC2B		SSLA1		
29		P94			TXD1 SMOSI1 SSDA1			
30		P93			RXD1 SMISO1 SSCL1		IRQ1	
31		P92			SCK1			
32		P91			CTS1# RTS1# SS1#			
33		P76		MTIOC4D GTIOC2B MTIOC7D				
34		P75		MTIOC4C GTIOC1B MTIOC7C				
35		P74		MTIOC3D GTIOC0B MTIOC6D				
36		P73		MTIOC4B GTIOC2A MTIOC7B				
37		P72		MTIOC4A GTIOC1A MTIOC7A				
38		P71		MTIOC3B GTIOC0A MTIOC6B				
39		P70	POE0#		CTS1# RTS1# SS1#		IRQ5-DS	
40		P33		MTIOC3A MTIOC6A		SSLA3		
41		P32		MTIOC3C MTIOC6C		SSLA2		
42	VCC							
43		P31		MTIOC0A		SSLA1		
44	VSS							
45		P30		MTIOC0B MTCLKD	TXD0 SMOSI0 SSDA0	SSLA0		
46		P24		MTIC5U MTCLKC	RXD0 SMISO0 SSCL0	RSPCKA		
47		P23		MTIC5V MTCLKB CACREF	SCK0	MOSIA		
48		P22		MTIC5W MTCLKA	CTS0# RTS0# SS0#	MISOA		
49		P47						AN007 CVREFH

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (3/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
50		P46						AN006
51		P45						AN005
52		P44						AN004
53		P43						AN003 CVREFL
54		P42						AN002
55		P41						AN001
56		P40						AN000
57	AVCC0							
58	VREFH0							
59	VREFL0							
60	AVSS0							
61		P11		MTCLKC			IRQ1-DS	
62		P10		MTCLKD			IRQ0-DS	
63		PA5		MTIOC1A		MISOA		
64		PA4		MTIOC1B		RSPCKA		ADTRG0#

Table 1.10 List of Pins and Pin Functions (48-Pin LQFP) (1/2)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications		Interrupt	S12ADB
					(SCIc, SCId)	(RSPI, RIIC)		
1	MD FINED							
2	RES#							
3	XTAL							
4	VSS							
5	EXTAL							
6	VCC							
7		PE2	POE10#				NMI	
8	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
9	TMS	PD6		GTIOC0B				
10	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
11	TCK FINEC	PD4		GTIOC1B	SCK1			
12	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
13		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
14		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
15	VCC							
16		PB4	POE8#	GTETRG	CTS12# RTS12# SS12#		IRQ3-DS	
17	VSS							
18		PB3		MTIOC0A MTCLKA CACREF	SCK0			
19		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
20		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
21		PB0		MTIOC0D		MOSIA		
22		PA3		MTIOC2A		SSLA0		
23		PA2		MTIOC2B		SSLA1		
24		P76		MTIOC4D GTIOC2B MTIOC7D				
25		P75		MTIOC4C GTIOC1B MTIOC7C				

Table 1.10 List of Pins and Pin Functions (48-Pin LQFP) (2/2)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications		Interrupt	S12ADB
					(SCIc, SCId)	(RSPI, RIIC)		
26		P74		MTIOC3D GTIOC0B MTIOC6D				
27		P73		MTIOC4B GTIOC2A MTIOC7B				
28		P72		MTIOC4A GTIOC1A MTIOC7A				
29		P71		MTIOC3B GTIOC0A MTIOC6B				
30		P70	POE0#		CTS1# RTS1# SS1#		IRQ5-DS	
31	VCC							
32		P30		MTIOC0B MTCLKD	TXD0 SMOSI0 SSDA0	SSLA0		
33	VSS							
34		P24		MTIC5U MTCLKC	RXD0 SMISO0 SSCL0	RSPCKA		
35		P23		MTIC5V MTCLKB CACREF	SCK0	MOSIA		
36		P22		MTIC5W MTCLKA	CTS0# RTS0# SS0#	MISOA		
37		P47						AN007 CVREFH
38		P44						AN004
39		P43						AN003 CVREFL
40		P42						AN002
41		P41						AN001
42		P40						AN000
43	AVCC0							
44	VREFH0							
45	VREFL0							
46	AVSS0							
47	VCL							
48	EMLE							

2. CPU

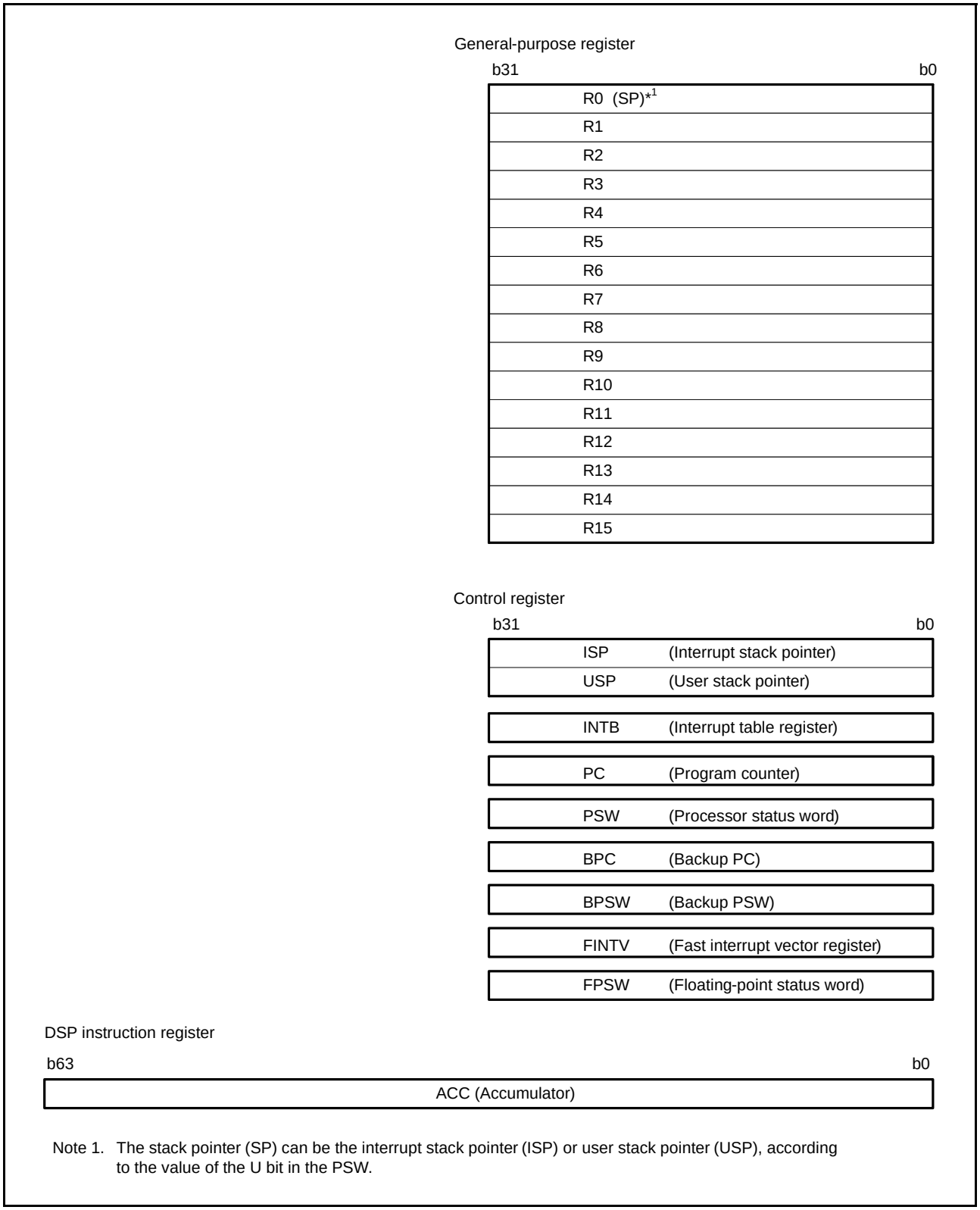
This MCU has the high-speed, high-performance RX CPU as its core.
A variable-length instruction format has been adopted for the RX CPU. Allocating the more frequently used instructions to the shorter instruction lengths facilitates the development of efficient programs that take up less memory.
The CPU has 73 basic instructions and 8 floating-point operation instructions, and nine DSP instructions, for a total of 90 instructions. It has 10 addressing modes and caters to register–register operations, register–memory operations, immediate–register operations, immediate–memory operations, memory–memory transfer, and bitwise operations. High-speed operation was realized by achieving execution in a single cycle not only for register–register operations, but also for other types of multiple instructions. The CPU includes an internal multiplier and an internal divider for high-speed multiplication and division.
The RX CPU has a five-stage pipeline for processing instructions. The stages are instruction fetching, instruction decoding, execution, memory access, and write-back. In cases where pipeline processing is drawn-out by memory access, subsequent operations may in fact be executed earlier. By adopting “out-of-order completion” of this kind, the execution of instructions is controlled to optimize numbers of clock cycles.

2.1 Features

- High instruction execution rate: One instruction in one clock cycle
- Address space: 4-Gbyte linear
- Register set of the CPU
  General purpose: Sixteen 32-bit registers
  Control: Nine 32-bit registers
  Accumulator: One 64-bit register
- Basic instructions: 73 (arithmetic/logic instructions, data-transfer instructions, branch instructions, bit-manipulation instructions, string-manipulation instructions, and system-manipulation instructions)
  Relative branch instructions to suit branch distances
  Variable-length instruction format (lengths from one to eight bytes)
  Short formats for frequently used instructions
- Floating-point operation instructions: 8
- DSP instructions: 9
  Supports 16-bit × 16-bit multiplication and multiply-and-accumulate operations.
  Rounds the data in the accumulator.
- Addressing modes: 10
- Five-stage pipeline
  Adoption of “out-of-order completion”
- Processor modes
  A supervisor mode and a user mode are supported.
- Floating-point operation unit
  Supports single-precision (32-bit) floating point
  Supports data types and exceptions in conformance with the IEEE754 standard
- Memory protection unit
- Data arrangement
  Selectable as little endian or big endian

2.2 Register Set of the CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

2.2.1 General-Purpose Registers (R0 to R15)

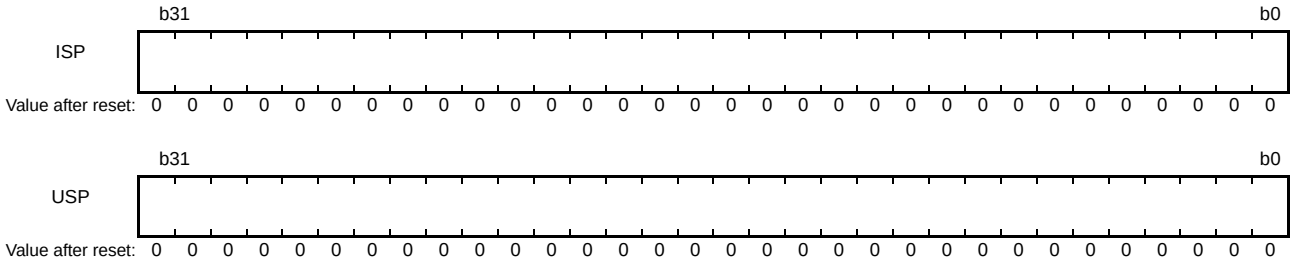
This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2.2 Control Registers

This CPU has the following nine control registers.

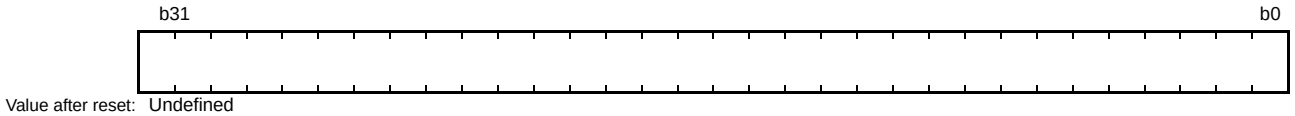
- Interrupt stack pointer (ISP)
- User stack pointer (USP)
- Interrupt table register (INTB)
- Program counter (PC)
- Processor status word (PSW)
- Backup PC (BPC)
- Backup PSW (BPSW)
- Fast interrupt vector register (FINTV)
- Floating-point status word (FPSW)

2.2.2.1 Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)



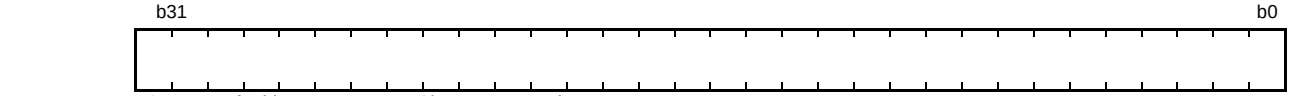
The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

2.2.2.2 Interrupt Table Register (INTB)



The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

2.2.2.3 Program Counter (PC)



Value after reset: Contents of addresses FFFFFFFCh to FFFFFFFFh

The program counter (PC) indicates the address of the instruction being executed.

2.2.2.4 Processor Status Word (PSW)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	IPL[3:0]				—	—	—	PM	—	—	U	I
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	O	S	Z	C
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C	Carry Flag	0: No carry has occurred. 1: A carry has occurred.	R/W
b1	Z	Zero Flag	0: Result is non-zero. 1: Result is 0.	R/W
b2	S	Sign Flag	0: Result is a positive value or 0. 1: Result is a negative value.	R/W
b3	O	Overflow Flag	0: No overflow has occurred. 1: An overflow has occurred.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	I*1	Interrupt Enable	0: Interrupt disabled. 1: Interrupt enabled.	R/W
b17	U*1	Stack Pointer Select	0: Interrupt stack pointer (ISP) is selected. 1: User stack pointer (USP) is selected.	R/W
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	PM*1,*2,*3	Processor Mode Select	0: Supervisor mode is selected. 1: User mode is selected.	R/W
b23 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b24	IPL[3:0]*1	Processor Interrupt Priority Level	b27 b24 0 0 0 0: Priority level 0 (lowest) 0 0 0 1: Priority level 1 0 0 1 0: Priority level 2 0 0 1 1: Priority level 3 0 1 0 0: Priority level 4 0 1 0 1: Priority level 5 0 1 1 0: Priority level 6 0 1 1 1: Priority level 7 1 0 0 0: Priority level 8 1 0 0 1: Priority level 9 1 0 1 0: Priority level 10 1 0 1 1: Priority level 11 1 1 0 0: Priority level 12 1 1 0 1: Priority level 13 1 1 1 0: Priority level 14 1 1 1 1: Priority level 15 (highest)	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In user mode, writing to the IPL[3:0], PM, U, and I bits by an MVTC or a POPC instruction is ignored. Writing to the IPL[3:0] bits by an MVTIPL instruction generates a privileged instruction exception.
Note 2. In supervisor mode, writing to the PM bit by an MVTC or a POPC instruction is ignored, but writing to the other bits is possible.
Note 3. Switching from supervisor mode to user mode requires execution of an RTE instruction after having set the PSW.PM bit saved on the stack to 1 or executing an RTFI instruction after having set the BPSW.PM bit to 1.

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

C Flag (Carry Flag)

This flag indicates whether a carry, borrow, or shift-out has occurred as the result of an operation.

Z Flag (Zero Flag)

This flag indicates that the result of an operation was 0.

S Flag (Sign Flag)

This flag indicates that the result of an operation was negative.

O Flag (Overflow Flag)

This flag indicates that an overflow occurred during an operation.

I Bit (Interrupt Enable)

This bit enables interrupt requests. When an exception is accepted, the value of this bit becomes 0.

U Bit (Stack Pointer Select)

This bit specifies the stack pointer as either the ISP or USP. When an exception request is accepted, this bit is set to 0. When the processor mode is switched from supervisor mode to user mode, this bit is set to 1.

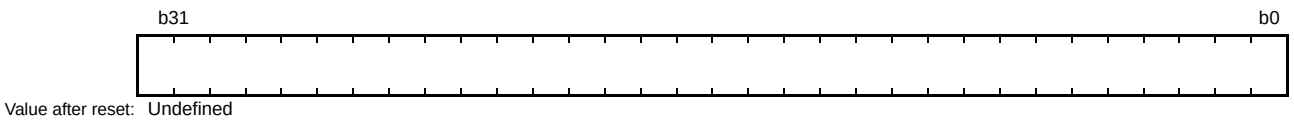
PM Bit (Processor Mode Select)

This bit specifies the processor mode. When an exception is accepted, the value of this bit becomes 0.

IPL[3:0] Bits (Processor Interrupt Priority Level)

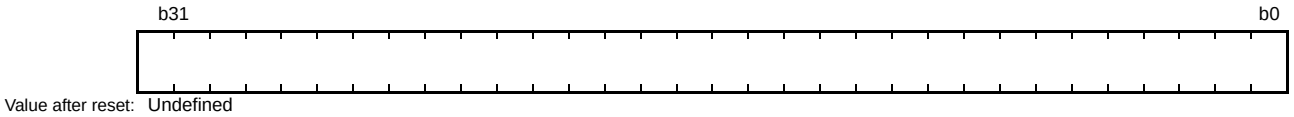
The IPL[3:0] bits specify the processor interrupt priority level as one of sixteen levels from zero to fifteen, wherein priority level zero is the lowest and priority level fifteen the highest. When the priority level of a requested interrupt is higher than the processor interrupt priority level, the interrupt is enabled. Setting the IPL[3:0] bits to level fifteen (Fh) disables all interrupt requests. The IPL[3:0] bits are set to level fifteen (Fh) when a non-maskable interrupt is generated. When interrupts in general are generated, the bits are set to the priority levels of accepted interrupts.

2.2.2.5 Backup PC (BPC)



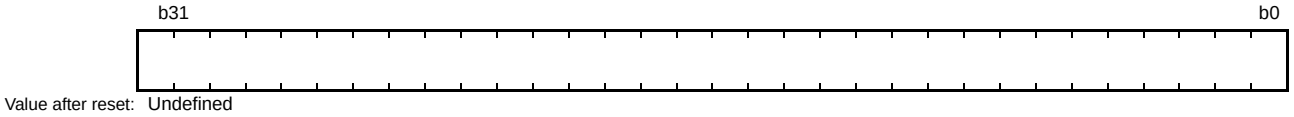
The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

2.2.2.6 Backup PSW (BPSW)



The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

2.2.2.7 Fast Interrupt Vector Register (FINTV)



The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.2.2.8 Floating-Point Status Word (FPSW)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FS	FX	FU	FZ	FO	FV	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	EX	EU	EZ	EO	EV	—	DN	CE	CX	CU	CZ	CO	CV	RM[1:0]	
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	RM[1:0]	Floating-Point Rounding-Mode Setting	b1 b0 0 0: Rounding towards the nearest value 0 1: Rounding towards 0 1 0: Rounding towards +∞ 1 1: Rounding towards –∞	R/W
b2	CV	Invalid Operation Cause Flag	0: No invalid operation has been encountered. 1: Invalid operation has been encountered.	R/(W) *1
b3	CO	Overflow Cause Flag	0: No overflow has occurred. 1: Overflow has occurred.	R/(W) *1
b4	CZ	Division-by-Zero Cause Flag	0: No division-by-zero has occurred. 1: Division-by-zero has occurred.	R/(W) *1
b5	CU	Underflow Cause Flag	0: No underflow has occurred. 1: Underflow has occurred.	R/(W) *1
b6	CX	Inexact Cause Flag	0: No inexact exception has been generated. 1: Inexact exception has been generated.	R/(W) *1
b7	CE	Unimplemented Processing Cause Flag	0: No unimplemented processing has been encountered. 1: Unimplemented process has been encountered.	R/(W) *1
b8	DN	0 Flush Bit of Denormalized Number	0: A denormalized number is handled as a denormalized number. 1: A denormalized number is handled as 0.*2	R/W

Bit	Symbol	Bit Name	Description	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	EV	Invalid Operation Exception Enable	0: Invalid operation exception is masked. 1: Invalid operation exception is enabled.	R/W
b11	EO	Overflow Exception Enable	0: Overflow exception is masked. 1: Overflow exception is enabled.	R/W
b12	EZ	Division-by-Zero Exception Enable	0: Division-by-zero exception is masked. 1: Division-by-zero exception is enabled.	R/W
b13	EU	Underflow Exception Enable	0: Underflow exception is masked. 1: Underflow exception is enabled.	R/W
b14	EX	Inexact Exception Enable	0: Inexact exception is masked. 1: Inexact exception is enabled.	R/W
b25 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26	FV*3	Invalid Operation Flag	0: No invalid operation has been encountered. 1: Invalid operation has been encountered.*8	R/W
b27	FO*4	Overflow Flag	0: No overflow has occurred. 1: Overflow has occurred.*8	R/W
b28	FZ*5	Division-by-Zero Flag	0: No division-by-zero has occurred. 1: Division-by-zero has occurred.*8	R/W
b29	FU*6	Underflow Flag	0: No underflow has occurred. 1: Underflow has occurred.*8	R/W
b30	FX*7	Inexact Flag	0: No inexact exception has been generated. 1: Inexact exception has been generated.*8	R/W
b31	FS	Floating-Point Error Summary Flag	This bit reflects the logical OR of the FU, FZ, FO, and FV flags.	R

Note 1. Writing 0 to the bit clears it. Writing 1 to the bit does not affect its value.
Note 2. Positive denormalized numbers are treated as +0, negative denormalized numbers as –0.
Note 3. When the EV bit is set to 0, the FV flag is enabled.
Note 4. When the EO bit is set to 0, the FO flag is enabled.
Note 5. When the EZ bit is set to 0, the FZ flag is enabled.
Note 6. When the EU bit is set to 0, the FU flag is enabled.
Note 7. When the EX bit is set to 0, the FX flag is enabled.
Note 8. Once the bit has been set to 1, this value is retained until it is cleared to 0 by software.

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

RM[1:0] Bits (Floating-Point Rounding-Mode Setting)

These bits specify the floating-point rounding-mode.

Explanation of Floating-Point Rounding Modes

- Rounding towards the nearest value (the default behavior): An inexact result is rounded to the available value that is closest to the result which would be obtained with an infinite number of digits. If two available values are equally close, rounding is to the even alternative.
- Rounding towards 0: An inexact result is rounded to the smallest available absolute value, i.e. in the direction of zero (simple truncation).
- Rounding towards +∞: An inexact result is rounded to the nearest available value in the direction of positive infinity.
- Rounding towards –∞: An inexact result is rounded to the nearest available value in the direction of negative infinity.

(1) Rounding to the nearest value is specified as the default mode and returns the most accurate value.
(2) Modes such as rounding towards 0, rounding towards +∞, and rounding towards –∞ are used to ensure precision when interval arithmetic is employed.

CV Flag (Invalid Operation Cause Flag), CO Flag (Overflow Cause Flag), CZ Flag (Division-by-Zero Cause Flag), CU Flag (Underflow Cause Flag), CX Flag (Inexact Cause Flag), and CE Flag (Unimplemented Processing Cause Flag)

Floating-point exceptions include the five specified in the IEEE754 standard, namely overflow, underflow, inexact, division-by-zero, and invalid operation. For a further floating-point exception that is generated upon detection of unimplemented processing, the corresponding flag (CE) is set to 1.

- The bit that has been set to 1 is cleared to 0 when the FPU instruction is executed.
- When 0 is written to the bit by the MVTC and POPC instructions, the bit is set to 0; the bit retains the previous value when 1 is written by the instruction.

DN Flag (0 Flush Bit of Denormalized Number)

When this bit is set to 0, a denormalized number is handled as a denormalized number. When this bit is set to 1, a denormalized number is handled as 0.

EV Bit (Invalid Operation Exception Enable), EO Bit (Overflow Exception Enable), EZ Bit (Division-by-Zero Exception Enable), EU Bit (Underflow Exception Enable), and EX Bit (Inexact Exception Enable)

When any of five floating-point exceptions specified in the IEEE754 standard is generated by the floating-point operation instruction, the bit decides whether the CPU will start handling the exception. When the bit is set to 0, the exception handling is masked; when the bit is set to 1, the exception handling is enabled.

FV Flag (Invalid Operation Flag), FO Flag (Overflow Flag), FZ Flag (Division-by-Zero Flag), FU Flag (Underflow Flag), and FX Flag (Inexact Flag)

While the exception handling enable bit (Ej) is 0 (exception handling is masked), if any of five floating-point exceptions specified in the IEEE754 standard is generated, the corresponding bit is set to 1.

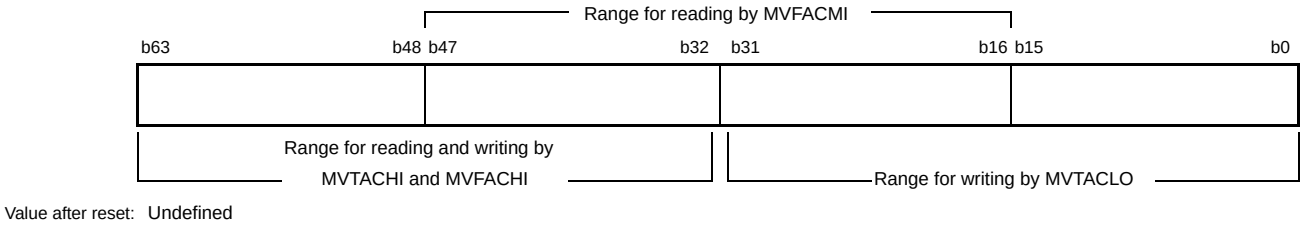
- When Ej is 1 (exception handling is enabled), the value of the flag remains.
- When the corresponding flag is set to 1, it remains 1 until it is cleared to 0 by software. (accumulation flag)

FS Flag (Floating-Point Error Summary Flag)

This bit reflects the logical OR of the FU, FZ, FO, and FV flags.

2.2.3 Register Associated with DSP Instructions

2.2.3.1 Accumulator (ACC)



Value after reset: Undefined

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

2.3 Processor Mode

The RX CPU supports two processor modes, supervisor and user. These processor modes enable the realization of a hierarchical CPU resource protection.
Each processor mode imposes a level on rights of access to the CPU resources and the instructions that can be executed. Supervisor mode carries greater rights than those of user mode.
The initial state after a reset is supervisor mode.

2.3.1 Supervisor Mode

In supervisor mode, all CPU resources are accessible and all instructions are available. However, writing to the processor mode select bit (PM) in the processor status word (PSW) by executing an MVTC or a POPC instruction will be ignored. For details on how to write to the PM bit, refer to section 2.2.2.4, Processor Status Word (PSW).

2.3.2 User Mode

In user mode, write access to the CPU resources listed below is restricted. The restriction applies to any instruction capable of write access.

- Some bits (bits IPL[3:0], PM, U, and I) in the processor status word (PSW)
- Interrupt stack pointer (ISP)
- Interrupt table register (INTB)
- Backup PSW (BPSW)
- Backup PC (BPC)
- Fast interrupt vector register (FINTV)

2.3.3 Privileged Instruction

Privileged instructions can only be executed in supervisor mode. Executing a privileged instruction in user mode produces a privileged instruction exception. Privileged instructions include the RTFI, MVTIPL, RTE, and WAIT instructions.

2.3.4 Switching Between Processor Modes

Manipulating the processor mode select bit (PM) in the processor status word (PSW) switches the processor mode. However, rewriting to the PM bit by executing an MVTC or a POPC instruction is prohibited. Switch the processor mode by following the procedures described below.

(1) Switching from user mode to supervisor mode

After an exception has been generated, the PSW.PM bit is set to 0 and the CPU switches to supervisor mode. The hardware pre-processing is executed in supervisor mode. The state of the processor mode before the exception was generated is retained in the copy of PSW.PM bit is saved on the stack.

(2) Switching from supervisor mode to user mode

Executing an RTE instruction when the value of the copy of the PSW.PM bit that has been preserved on the stack is 1 or an RTFI instruction when the value of the copy of the PSW.PM bit that has been preserved in the backup PSW (BPSW) is 1 causes a transition to user mode. In the transition to user mode, the value of the stack pointer designation bit (the U bit in the PSW) becomes 1.

2.4 Data Types

The RX CPU can handle four types of data: integer, floating-point, bit, and string.
For details, refer to RX Family User's Manual: Software.

2.5 Endian

For the RX CPU, instructions are little endian, but the treatment of data is selectable as little or big endian.

2.5.1 Switching the Endian

As arrangements of bytes, this MCU supports both big endian, where the higher-order byte (MSB) is at location 0, and little endian, where the lower-order byte (LSB) is at location 0.
For details on the endian setting, see section 3, Operating Modes [144-, 120-, 112- and 100-Pin Versions] or section 4, Operating Modes [64- and 48-Pin Versions].
Operations for access differ according to the endian setting and, depending on the instruction, whether 8-, 16- or 32-bit access has been selected. Operations for access in the various possible cases are described in Table 2.1 to Table 2.12.
In the tables,

LL indicates bits D7 to D0 of the general-purpose register,
LH indicates bits D15 to D8 of the general-purpose register,
HL indicates bits D23 to D16 of the general-purpose register, and
HH indicates bits D31 to D24 of the general-purpose register.

	D31 to D24	D23 to D16	D15 to D8	D7 to D0
General purpose register: Rm	HH	HL	LH	LL

Table 2.1 32-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to LL	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—
Address 2	Transfer to HL	Transfer to LH	Transfer to LL	—	—
Address 3	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL	—
Address 4	—	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL
Address 5	—	—	Transfer to HH	Transfer to HL	Transfer to LH
Address 6	—	—	—	Transfer to HH	Transfer to HL
Address 7	—	—	—	—	Transfer to HH

Table 2.2 32-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to HH	—	—	—	—
Address 1	Transfer to HL	Transfer to HH	—	—	—
Address 2	Transfer to LH	Transfer to HL	Transfer to HH	—	—
Address 3	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH	—
Address 4	—	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH
Address 5	—	—	Transfer to LL	Transfer to LH	Transfer to HL
Address 6	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	Transfer to LL

Table 2.3 32-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from LL	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—
Address 2	Transfer from HL	Transfer from LH	Transfer from LL	—	—
Address 3	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL	—
Address 4	—	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL
Address 5	—	—	Transfer from HH	Transfer from HL	Transfer from LH
Address 6	—	—	—	Transfer from HH	Transfer from HL
Address 7	—	—	—	—	Transfer from HH

Table 2.4 32-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from HH	—	—	—	—
Address 1	Transfer from HL	Transfer from HH	—	—	—
Address 2	Transfer from LH	Transfer from HL	Transfer from HH	—	—
Address 3	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH	—
Address 4	—	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH
Address 5	—	—	Transfer from LL	Transfer from LH	Transfer from HL
Address 6	—	—	—	Transfer from LL	Transfer from LH
Address 7	—	—	—	—	Transfer from LL

Table 2.5 16-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LL	—	—	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—	—	—
Address 2	—	Transfer to LH	Transfer to LL	—	—	—	—
Address 3	—	—	Transfer to LH	Transfer to LL	—	—	—
Address 4	—	—	—	Transfer to LH	Transfer to LL	—	—
Address 5	—	—	—	—	Transfer to LH	Transfer to LL	—
Address 6	—	—	—	—	—	Transfer to LH	Transfer to LL
Address 7	—	—	—	—	—	—	Transfer to LH

Table 2.6 16-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LH	—	—	—	—	—	—
Address 1	Transfer to LL	Transfer to LH	—	—	—	—	—
Address 2	—	Transfer to LL	Transfer to LH	—	—	—	—
Address 3	—	—	Transfer to LL	Transfer to LH	—	—	—
Address 4	—	—	—	Transfer to LL	Transfer to LH	—	—
Address 5	—	—	—	—	Transfer to LL	Transfer to LH	—
Address 6	—	—	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	—	—	Transfer to LL

Table 2.7 16-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LL	—	—	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—	—	—
Address 2	—	Transfer from LH	Transfer from LL	—	—	—	—
Address 3	—	—	Transfer from LH	Transfer from LL	—	—	—
Address 4	—	—	—	Transfer from LH	Transfer from LL	—	—
Address 5	—	—	—	—	Transfer from LH	Transfer from LL	—
Address 6	—	—	—	—	—	Transfer from LH	Transfer from LL
Address 7	—	—	—	—	—	—	Transfer from LH

Table 2.8 16-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LH	—	—	—	—	—	—
Address 1	Transfer from LL	Transfer from LH	—	—	—	—	—
Address 2	—	Transfer from LL	Transfer from LH	—	—	—	—
Address 3	—	—	Transfer from LL	Transfer from LH	—	—	—
Address 4	—	—	—	Transfer from LL	Transfer from LH	—	—
Address 5	—	—	—	—	Transfer from LL	Transfer from LH	—
Address 6	—	—	—	—	—	Transfer from LL	Transfer from LH
Address 7	—	—	—	—	—	—	Transfer from LH

Table 2.9 8-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.10 8-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.11 8-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

Table 2.12 8-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

2.5.2 Access to I/O Registers

The addresses of I/O registers are fixed, and this is regardless of whether the setting is for little endian or big endian. Accordingly, changes to the endian do not affect access to I/O registers. For the arrangements of I/O registers, refer to the descriptions of registers in the relevant sections.

2.5.3 Notes on Access to I/O Registers

Ensure that access to I/O registers is in accord with the following rules.

- With I/O registers for which a bus width of eight bits is indicated, use instructions having operands of the same width (eight bits). That is, access these registers by using instructions with .B as the size specifier (.size), or with .B or .UB as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 16 bits is indicated, use instructions having operands of the same width (16 bits). That is, access these registers by using instructions with .W as the size specifier (.size), or with .W or .UW as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 32 bits is indicated, use instructions having operands of the same width (32 bits). That is, access these registers by using instructions with .L as the size specifier (.size), or with .L size-extension specifier (.memex).

2.5.4 Data Arrangement

2.5.4.1 Data Arrangement in Registers

Figure 2.2 shows the relation between the sizes of registers and bit numbers.

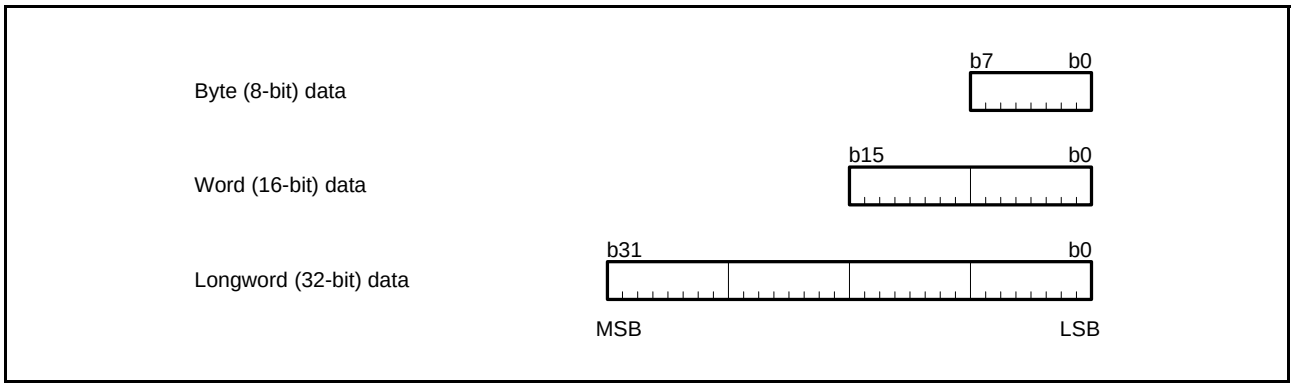


Figure 2.2 Data Arrangement in Registers

2.5.4.2 Data Arrangement in Memory

Data in memory have three sizes: byte (8-bit), word (16-bit), and longword (32-bit). The data arrangement is selectable as little endian or big endian. Figure 2.3 shows the arrangement of data in memory.

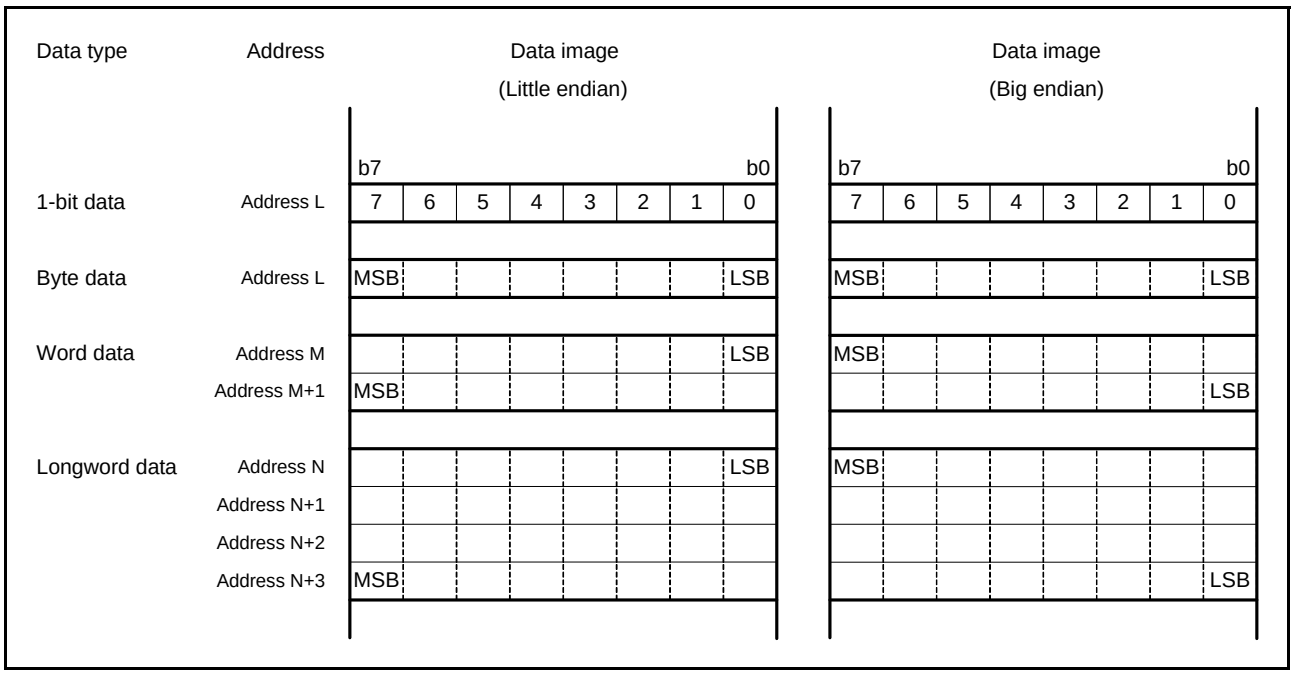


Figure 2.3 Data Arrangement in Memory

2.5.5 Notes on the Allocation of Instruction Codes

The allocation of instruction codes to an external space where the endian differs from that of the chip is prohibited. If the instruction codes are allocated to the external space, they must be allocated to areas where the endian setting is the same as that for the chip.

2.6 Vector Table

There are two types of vector table: fixed and relocatable. Each vector in the vector table consists of four bytes and specifies the address where the corresponding exception handling routine starts.

2.6.1 Fixed Vector Table

The fixed vector table is allocated to a fixed address range. The individual vectors for the privileged instruction exception, access exception, undefined instruction exception, floating-point exception, non-maskable interrupt, and reset are allocated to addresses in the range from FFFFFF80h to FFFFFFFFh. Figure 2.4 shows the fixed vector table.

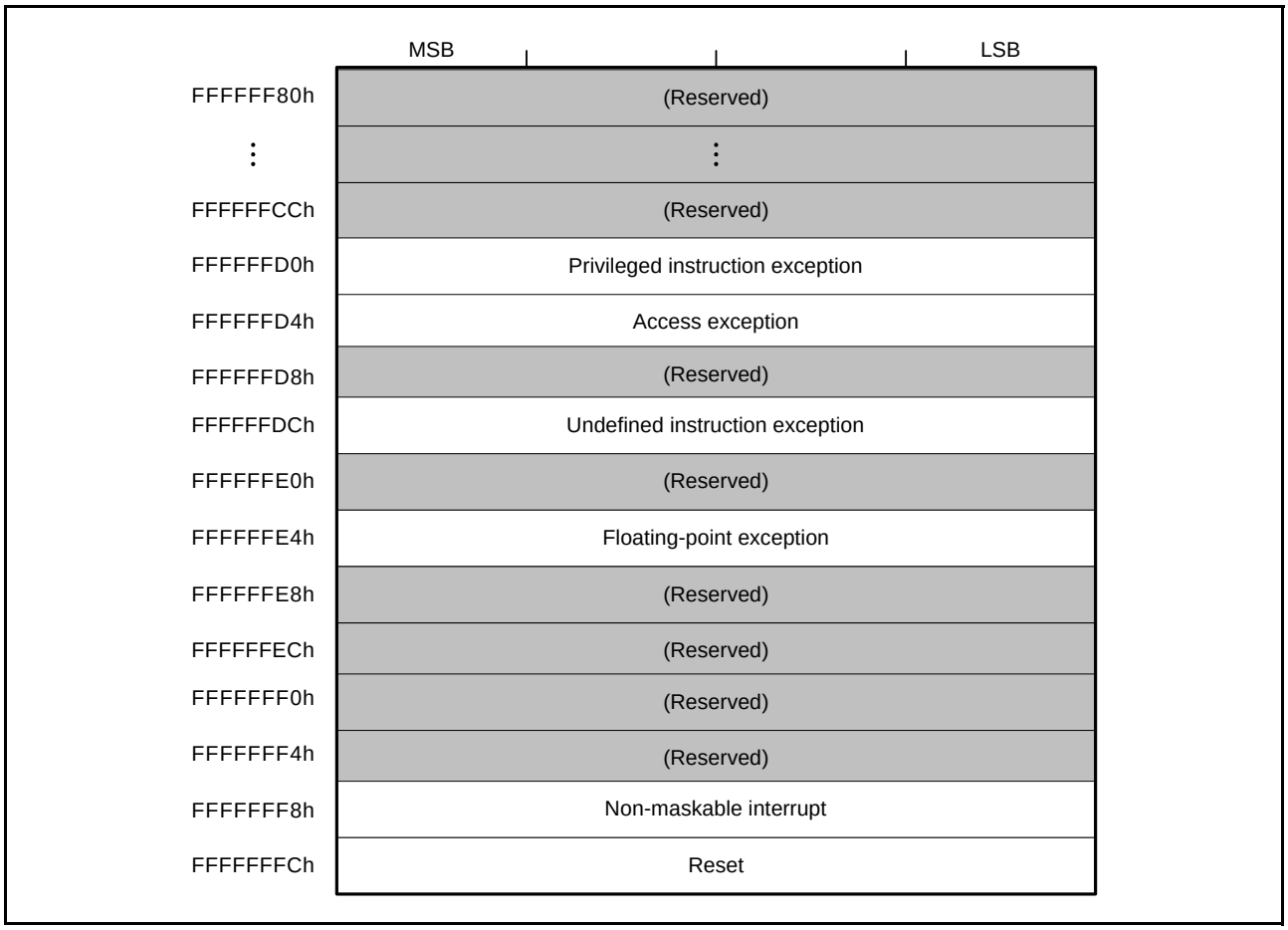


Figure 2.4 Fixed Vector Table

2.6.2 Relocatable Vector Table

The address where the relocatable vector table is placed can be adjusted. The table is a 1,024-byte region that contains all vectors for unconditional traps and interrupts and starts at the address (IntBase) specified in the interrupt table register (INTB). Figure 2.5 shows the relocatable vector table.

Each vector in the relocatable vector table has a vector number from 0 to 255. Each of the INT instructions, which act as the sources of unconditional traps, is allocated to the vector that has the same number as is specified as the operand of the instruction itself (from 0 to 255). The BRK instruction is allocated to the vector with number 0. Furthermore, vector numbers (from 0 to 255) are allocated to interrupt requests in a fixed way for each product. For more on interrupt vector numbers, see section 15.3.1, Interrupt Vector Table.

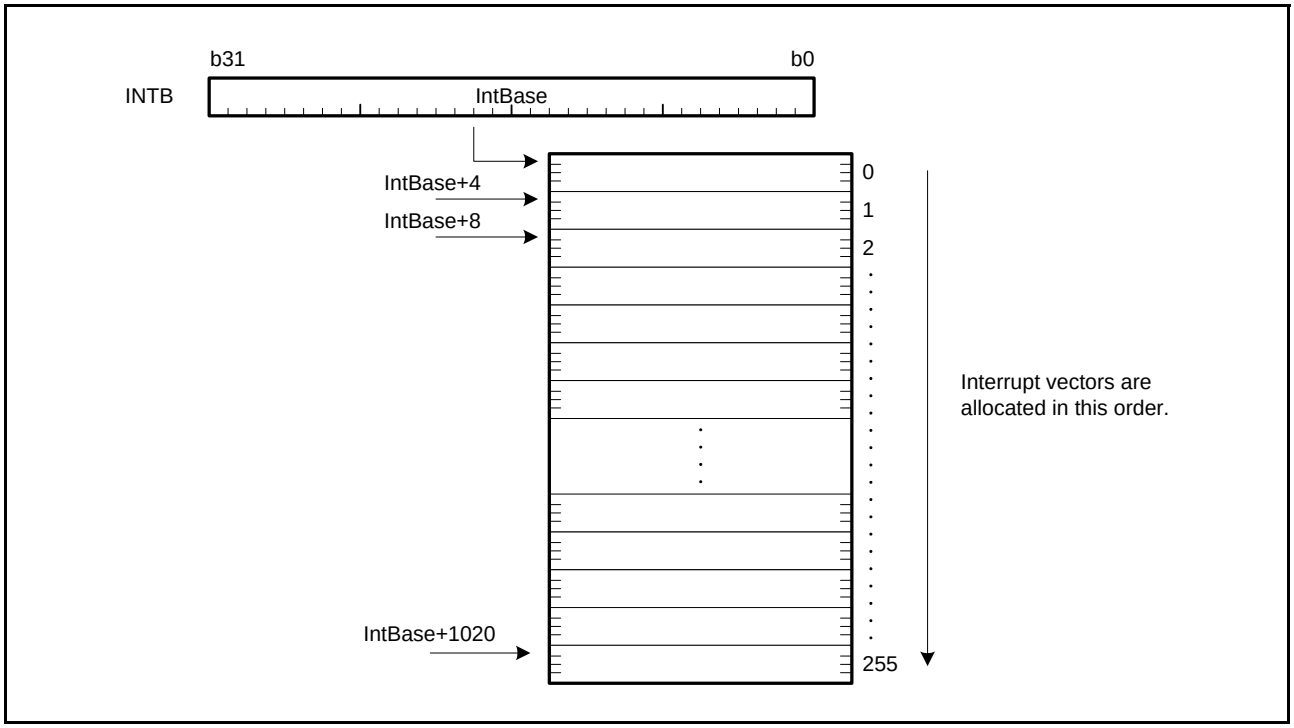


Figure 2.5 Relocatable Vector Table

2.7 Operation of Instructions

2.7.1 Data Prefetching by the RMPA Instruction and the String-Manipulation Instructions

The RMPA instruction and the string-manipulation instructions except the SSTR instruction (that is, SCMPU, SMOVB, SMOVF, SMOVU, SUNTIL, and SWHILE instructions) may prefetch data from the memory to speed up the read processing. Data is prefetched from the prefetching start position with three bytes as the upper limit. The prefetching start positions of each operation are shown below.

- RMPA instruction: The multiplicand address specified by R1, and the multiplier address specified by R2
- SCMPU instruction: The source address specified by R1 for comparison, and the destination address specified by R2 for comparison
- SUNTIL and SWHILE instructions: The destination address specified by R1 for comparison
- SMOVB, SMOVF, and SMOVU instructions: The source address specified by R2 for transfer

2.8 Pipeline

2.8.1 Overview

The RX CPU has 5-stage pipeline structure. The RX CPU instruction is converted into one or more micro-operations, which are then executed in pipeline processing. In the pipeline stage, the IF stage is executed in the unit of instructions, while the D and subsequent stages are executed in the unit of micro-operations.
The operation of pipeline and respective stages is described below.

(1) IF stage (instruction fetch stage)

In the IF stage, the CPU fetches instructions from the memory. As the RX CPU has four 8-byte instruction queues, it fetches instructions until the instruction queue is full, regardless of the completion of decoding in the D (decoding) stage.

(2) D stage (decoding stage)

The CPU decodes instructions in the D stage and converts them into micro-operations. The CPU reads the register information (RF) in this stage and executes a bypass process (BYP) if the result of the preceding instruction will be used in a subsequent instruction. The write of operation result to the register (RW) can be executed with the register reference by using the bypass process.

(3) E stage (execution stage)

Operations and address calculations (OP) are processed in the E stage.

(4) M stage (memory access stage)

Operand memory accesses (OA1, OA2) are processed in the M stage. This stage is used only when the memory is accessed, and is divided into two sub-stages, M1 and M2. The RX CPU enables respective memory accesses for M1 and M2.

- M1 stage (memory-access stage 1)
  Operand memory access (OA1) is processed.
  Store operation: The pipeline processing ends when a write request is received via the bus.
  Load operation: The operation proceeds to the M2 stage when a read request is received via the bus. If a request and load data are received at the same timing (no-wait memory access), the operation proceeds to the WB stage.
- M2 stage (memory-access stage 2)
  Operand memory access (OA2) is processed. The CPU waits for the load data in the M2 stage. When the load data is received, the operation proceeds to the WB stage.

(5) WB stage (write-back stage)

The operation result and the data read from memory are written to the register (RW) in the WB stage. The data read from memory and the other type of data, such as the operation result, can be written to the register in the same clock cycles.

Figure 2.6 shows the pipeline configuration and its operation.

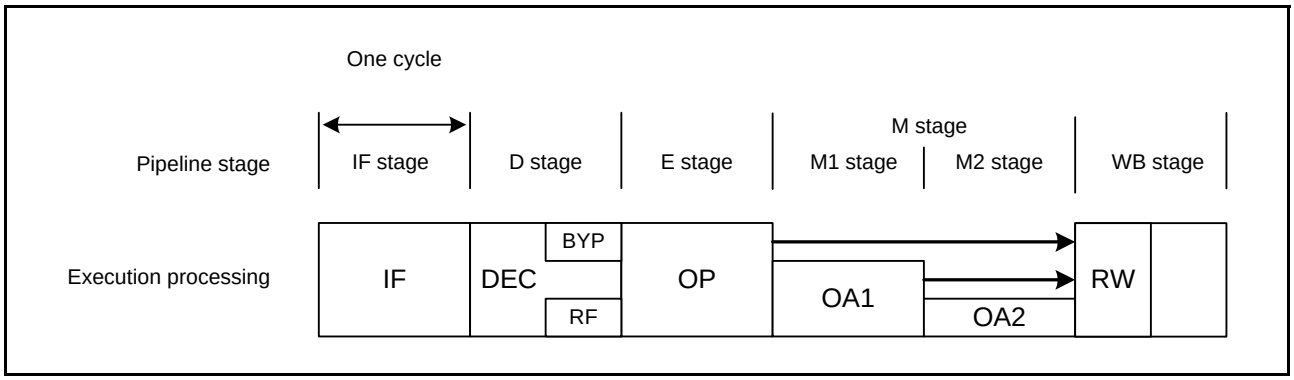


Figure 2.6 Pipeline Configuration and its Operation

2.8.2 Instructions and Pipeline Processing

The operands in the table below indicate the following meaning.

#IMM: Immediate
flag: bit, flag
Rs, Rs2, Rd, Rd2, Ri, Rb: General-purpose register
CR: Control register
dsp: displacement
pcdsp: displacement

2.8.2.1 Instructions Converted into Single Micro-Operation and Pipeline Processing

The table below lists the instructions that are converted into a single micro-operation. The number of cycles in the table indicates the number of cycles during no-wait memory access.

Table 2.13 Instructions that are Converted into a Single Micro-Operation

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Reference Figure	Number of Cycles
Arithmetic/logic instructions (register-register, immediate-register) Except EMUL, EMULU, RMPA, DIV, DIVU and SATR	• {ABS, NEG, NOT} “Rd”/“Rs, Rd” • {ADC, MAX, MIN, ROTL, ROTR, XOR} “#IMM, Rd”/“Rs, Rd” • ADD “#IMM, Rd”/“Rs, Rd”/“#IMM, Rs, Rd”/“Rs, Rs2, Rd” • {AND, MUL, OR, SUB} “#IMM, Rd”/“Rs, Rd”/“Rs, Rs2, Rd” • {CMP, TST} “#IMM, Rs”/“Rs, Rs2” • NOP • {ROLC, RORC, SAT} “Rd” • SBB “Rs, Rd” • {SHAR, SHLL, SHLR} “#IMM, Rd”/“Rs, Rd”/“#IMM, Rs, Rd”	Figure 2.7	1
Arithmetic/logic instructions (division)	• DIV “#IMM, Rd”/“Rs, Rd”	Figure 2.7	3 to 20*1
	• DIVU “#IMM, Rd”/“Rs, Rd”	Figure 2.7	2 to 18*1
Data transfer instructions (register-register, immediate-register)	• MOV “#IMM, Rd”/“Rs, Rd” • {MOVU, REVL, REVW} “Rs, Rd” • SC*Cnd* “Rd” • {STNZ, STZ} “#IMM, Rd”	Figure 2.7	1
Transfer instructions (load operation)	• {MOV, MOVU} “[Rs], Rd”/“dsp[Rs], Rd”/“[Rs+], Rd”/“[-Rs], Rd”/“[Ri, Rb], Rd” • POP “Rd”	Figure 2.8	Throughput: 1 Latency: 2*2
Transfer instructions (store operation)	• MOV “Rs, [Rd]”/“Rs, dsp[Rd]”/“Rs, [Rd+]”/“Rs, [-Rd]”/“Rs, [Ri, Rb]”/“#IMM, dsp[Rd]”/“#IMM, [Rd]” • PUSH “Rs” • PUSHC “CR” • SCCnd “[Rd]”/“dsp[Rd]”	Figure 2.9	1
Bit manipulation instructions (register)	• {BCLR, BNOT, BSET} “#IMM, Rd”/“Rs, Rd” • BM*Cnd* “#IMM, Rd” • BTST “#IMM, Rs”/“Rs, Rs2”	Figure 2.7	1
Branch instructions	• B*Cnd* “pcdsp” • {BRA, BSR} “pcdsp”/“Rs” • {JMP, JSR} “Rs”	Figure 2.18	Branch taken: 3 Branch not taken: 1
Floating-point operation instructions (register-register, immediate-register)	• FCMP “#IMM, Rd”/“Rs, Rs2”	Figure 2.7	1
System manipulation instructions	• {CLRPSW, SETPSW} “flag” • MVTC “#IMM, CR”/“Rs, CR” • MVFC “CR, Rd” • MVTIPL“#IMM”	—	1
DSP instructions	• {MACHI, MACLO, MULHI, MULLO} “Rs, Rs2” • {MVFACHI, MVFACMI} “Rd” • {MVTACHI, MVTACLO} “Rs” • RACW“#IMM”	Figure 2.7	1

Note 1. The number of cycles for the dividing instruction varies according to the divisor and dividend.
Note 2. For the number of cycles for throughput and latency, see section 2.8.3, Calculation of the Instruction Processing Time.

Figure 2.7 to Figure 2.9 show the operation of instructions that are converted into a basic single micro-operation.

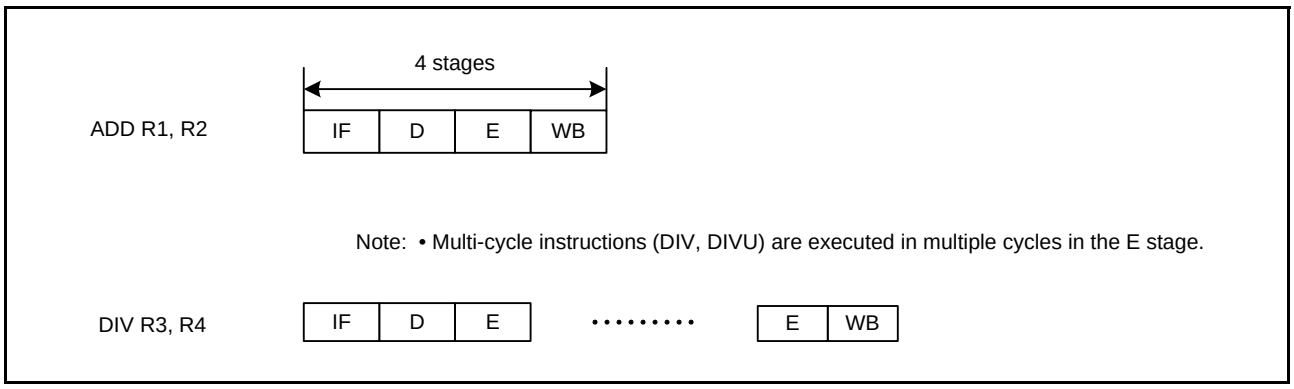


Figure 2.7 Operation for Register-Register, Immediate-Register

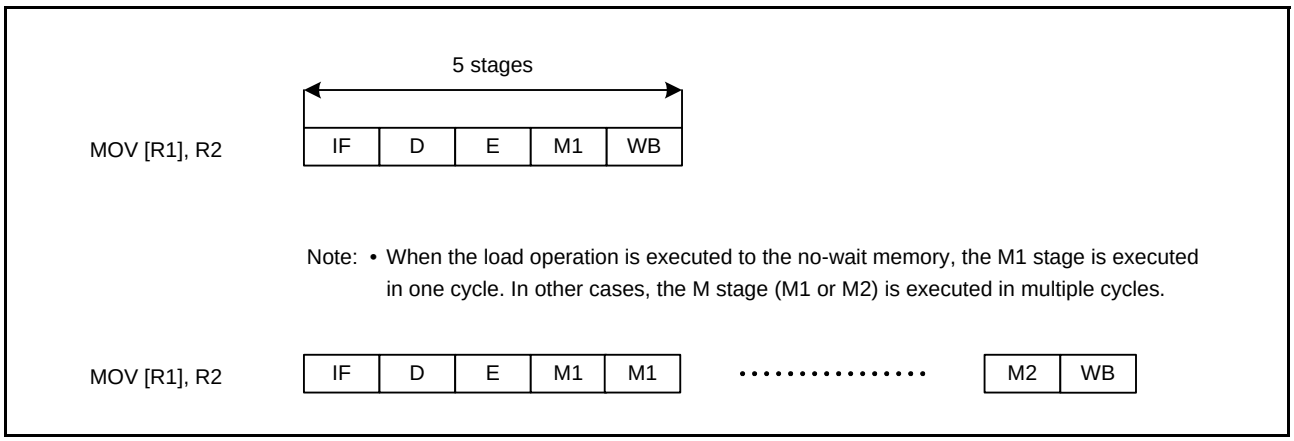


Figure 2.8 Load Operation

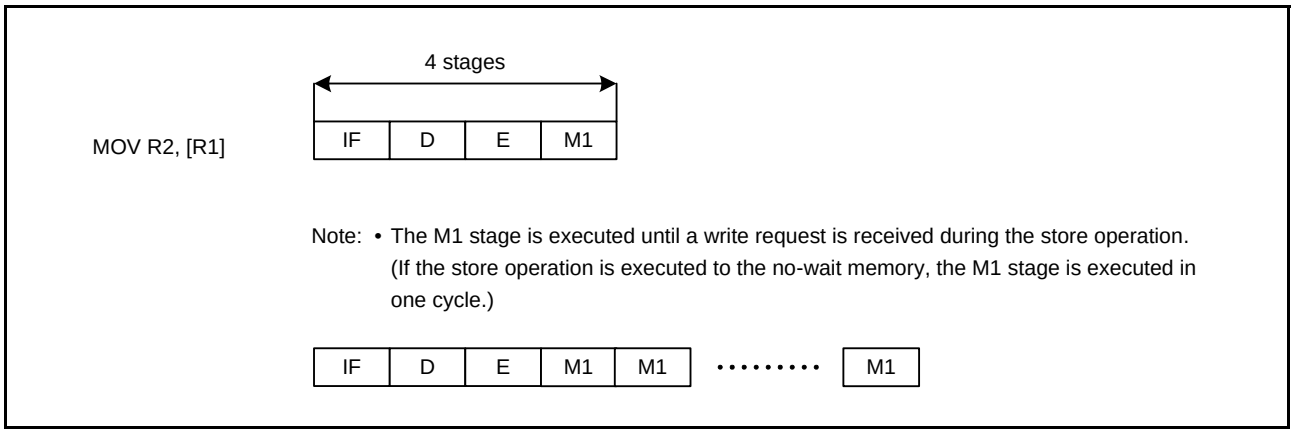


Figure 2.9 Store Operation

2.8.2.2 Instructions Converted into Multiple Micro-Operations and Pipeline Processing

The table below lists the instructions that are converted into multiple micro-operations. The number of cycles in the table indicates the number of cycles during no-wait memory access.

Table 2.14 Instructions that are Converted into Multiple Micro-Operations (1/2)

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Reference Figure	Number of Cycles
Arithmetic/logic instructions (memory source operand)	• {ADC, ADD, AND, MAX, MIN, MUL, OR, SBB, SUB, XOR} “[Rs], Rd”/“dsp[Rs], Rd” • {CMP, TST} “[Rs], Rs2”/“dsp[Rs], Rs2”	Figure 2.10	3
Arithmetic/logic instructions (division)	• DIV “[Rs],Rd / dsp[Rs],Rd”	—	5 to 22
	• DIVU“[Rs],Rd / dsp[Rs],Rd”	—	4 to 20
Arithmetic/logic instructions (multiplier: 32 × 32 → 64 bits) (register-register, register-immediate)	• {EMUL, EMULU} “#IMM, Rd”/“Rs, Rd”	Figure 2.12	2
Arithmetic/logic instructions (multiplier: 32 × 32 → 64 bits) (memory source operand)	• {EMUL, EMULU} “[Rs], Rd”/“dsp[Rs], Rd”	—	4
Arithmetic/logic instructions (multiply-and-accumulate operation)	• RMPA.B	—	6+7×floor(n/4)+4×(n%4) n: Number of processing bytes*1
	• RMPA.W	—	6+5×floor(n/2)+4×(n%2) n: Number of processing words*1
	• RMPA.L	—	6+4n n: Number of processing longwords*1
Arithmetic/logic instruction (64-bit signed saturation processing for the RMPA instruction)	• SATR	—	3
Data transfer instructions (memory-memory transfer)	• MOV “[Rs], [Rd]”/“dsp[Rs], [Rd]”/“[Rs], dsp[Rd]”/“dsp[Rs], dsp[Rd]” • PUSH “[Rs]”/“dsp[Rs]”	Figure 2.11	3
Bit manipulation instructions (memory source operand)	• {BCLR, BNOT, BSET} “#IMM, [Rd]”/“#IMM, dsp[Rd]”/“Rs, [Rd]”/“Rs, dsp[Rd]” • BMCnd “#IMM, [Rd]”/“#IMM, dsp[Rd]” • BTST “#IMM, [Rs]”/“#IMM, dsp[Rs]”/“Rs, [Rs2]”/“Rs, dsp[Rs2]	Figure 2.11	3
Transfer instruction (load operation)	• POPC “CR”	—	Throughput: 3 Latency: 4*2
Transfer instruction (save operation of multiple registers)	• PUSHM “Rs-Rs2”	—	n n: Number of registers*3
Transfer instructions (restore operation of multiple registers)	• POPM “Rs-Rs2”	—	Throughput: n Latency: n+1 n: Number of registers*2,*4
Transfer instruction (register-register)	• XCHG “Rs, Rd”	Figure 2.13	2
Transfer instructions (memory-register)	• XCHG “[Rs], Rd”/“dsp[Rs], Rd”	Figure 2.14	2
Branch instructions	• RTS	—	5
	• RTSD “#IMM”	—	5
	• RTSD “#IMM, Rd-Rd2”	—	Throughput: n<5?5:1+n Latency: n<4?5:2+n n: Number of registers*2

Table 2.14 Instructions that are Converted into Multiple Micro-Operations (2/2)

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Reference Figure	Number of Cycles
String manipulation instructions*5	• SCMPU	—	2+4×floor(n/4)+4×(n%4) n: Number of comparison bytes*1
	• SMOVB	—	n>3? 6+3×floor(n/4)+3×(n%4): 2+3n n: Number of transfer bytes*1
	• SMOVF, SMOVU	—	2+3×floor(n/4)+3×(n%4) n: Number of transfer bytes*1
	• SSTR.B	—	2+floor(n/4)+n%4 n: Number of transfer bytes*1
	• SSTR.W	—	2+floor(n/2)+n%2 n: Number of transfer words*1
	• SSTR.L	—	2+n n: Number of transfer longwords
	• SUNTIL.B, SWHILE.B	—	3+3×floor(n/4)+3×(n%4) n: Number of comparison bytes*1
	• SUNTIL.W, SWHILE.W	—	3+3×floor(n/2)+3×(n%2) n: Number of comparison words*1
	• SUNTIL.L, SWHILE.L	—	3+3×n n: Number of comparison longwords
Floating-point operation instructions (register-register, immediate-register)	• {FADD, FSUB} “#IMM, Rd”/“Rs, Rd”	Figure 2.15	4
	• FMUL “#IMM, Rd”/“Rs, Rd”	—	3
	• FDIV “#IMM, Rd”/“Rs, Rd”	—	16
	• {FTOI, ROUND, ITOF} “Rs, Rd”	—	2
Floating-point operation instructions (memory source operand)	• {FADD, FSUB} “[Rs], Rd”/“dsp[Rs], Rd”	—	6
	• FCMP “[Rs], Rs2”/“dsp[Rs], Rs2”	—	3
	• FMUL “[Rs], Rd”/“dsp[Rs], Rd”	—	5
	• FDIV “[Rs], Rd”/“dsp[Rs], Rd”	—	18
	• {FTOI, ROUND, ITOF} “[Rs], Rd”/ “dsp[Rs], Rd”	—	4
System manipulation instructions	• RTE	—	6
	• RTFI	—	3

?: Conditional operator

Note 1. floor (x): Max. integer that is smaller than x
Note 2. For the number of cycles for throughput and latency, see section 2.8.3, Calculation of the Instruction Processing Time.
Note 3. The PUSHM instruction is converted into multiple store operations. The pipeline processing is the same as the one for the store operations of the MOV instruction, where the operation is repeated for the number of specified registers.
Note 4. The POPM instruction is converted into multiple load operations. The pipeline processing is the same as the one for the load operations of the MOV instruction, where the operation is repeated for the number of specified registers.
Note 5. Each of the SCMPU, SMOVU, SWHILE, and SUNTIL instructions ends the execution regardless of the specified cycles, if the end condition is satisfied during execution.

Figure 2.10 to Figure 2.17 show the operation of instructions that are converted into basic multiple micro-operations.
Note: • mop: Micro-operation, stall: Pipeline stall

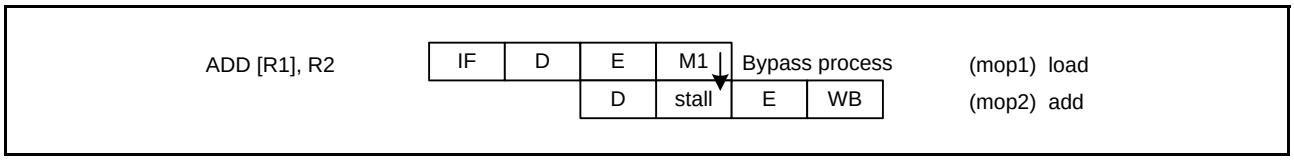


Figure 2.10 Arithmetic/Logic Instruction (Memory Source Operand)

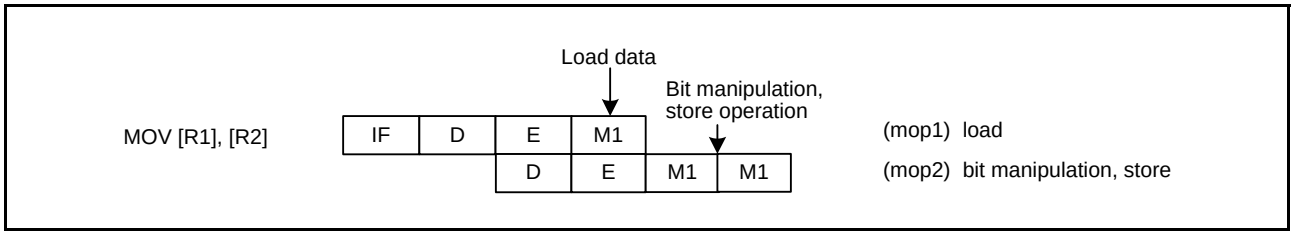


Figure 2.11 MOV Instruction (Memory-Memory), Bit Manipulation Instruction (Memory Source Operand)

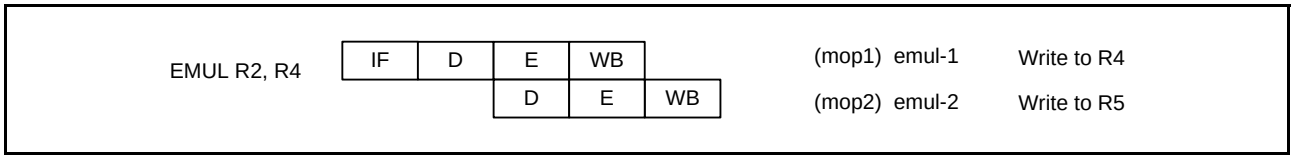


Figure 2.12 EMUL, EMULU Instructions (Register- Register, Register-Immediate)

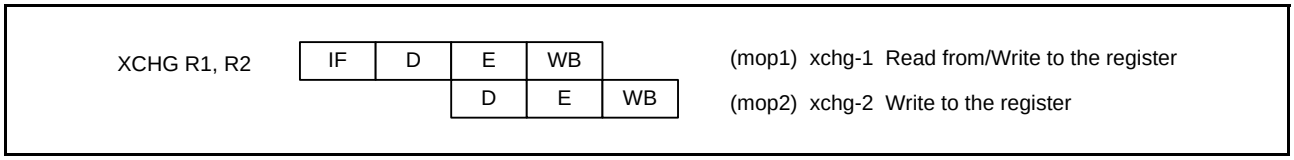


Figure 2.13 XCHG Instruction (Registers)

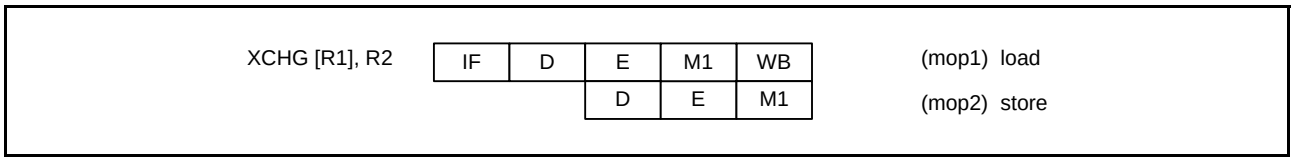


Figure 2.14 XCHG Instruction (Memory Source Operand)

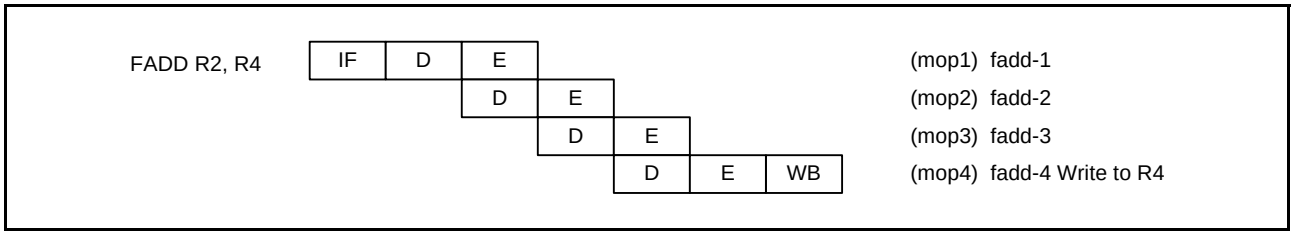


Figure 2.15 Floating-Point Operation Instruction (Register-Register, Immediate-Register)

2.8.2.3 Pipeline Basic Operation

In the ideal pipeline processing, each stage is executed in one cycle, though all instructions may not be pipelined in due to the processing in each stage and the branch execution.
The CPU controls the pipeline stage with the IF stage in the unit of instructions, while the D and subsequent stages in the unit of micro-operations.
The figures below show the pipeline processing of typical cases.
Note: • mop: Micro-operation, stall: Pipeline stall

(1) Pipeline Flow with Stalls

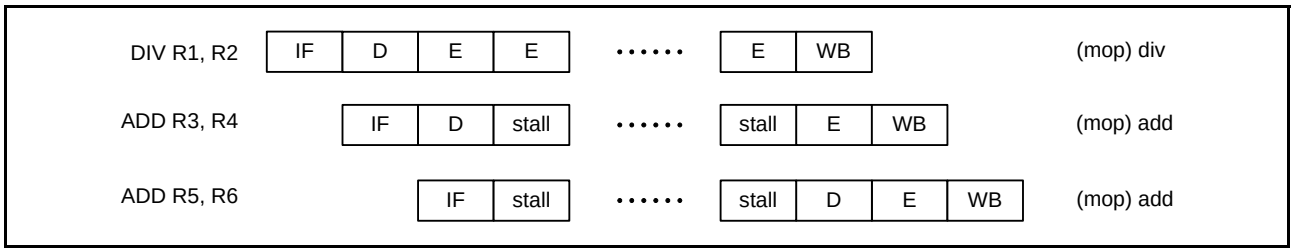


Figure 2.16 When an Instruction which Requires Multiple Cycles is Executed in the E Stage

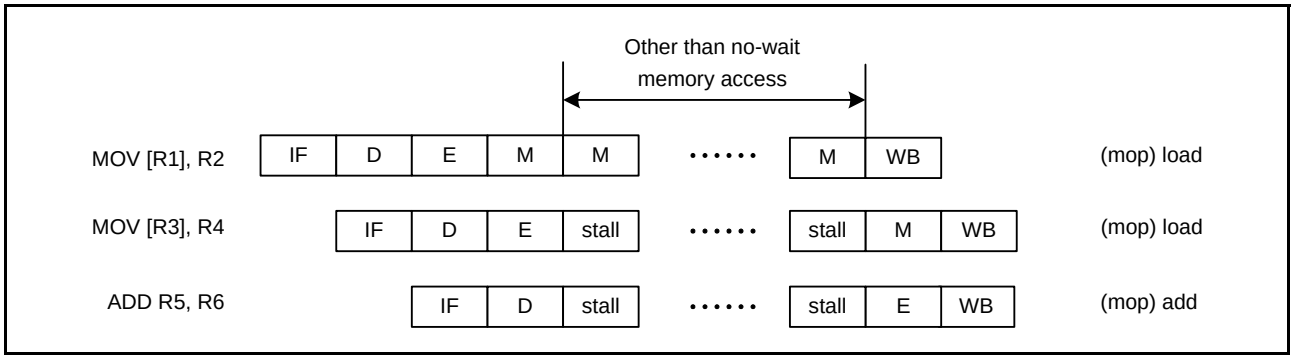


Figure 2.17 When an Instruction which Requires more than One Cycle for its Operand Access is Executed

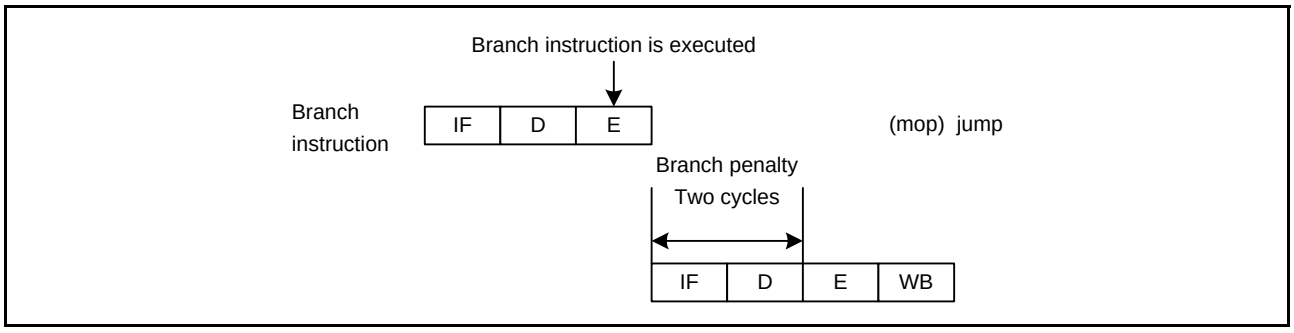


Figure 2.18 When a Branch Instruction is Executed (an Unconditional Branch Instruction is Executed or the Condition is Satisfied for a Conditional Branch Instruction)

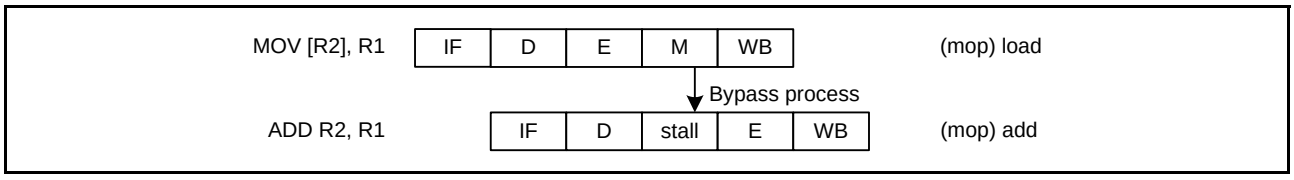


Figure 2.19 When the Subsequent Instruction Uses an Operand Read from the Memory

(2) Pipeline Flow with no Stall

(a) Bypass process

Even when the result of the preceding instruction will be used in a subsequent instruction, the operation processing between registers is pipelined in by the bypass process.

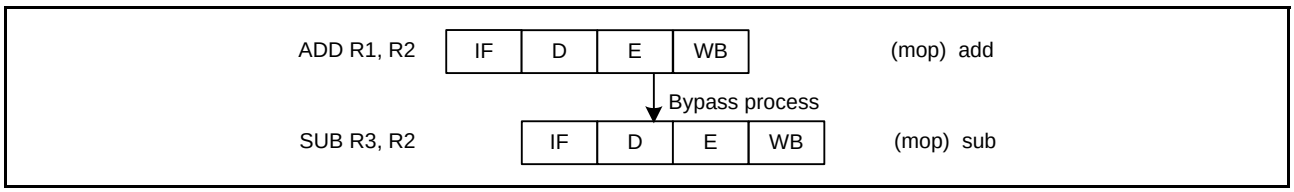


Figure 2.20 Bypass Process

(b) When WB stages for the memory load and for the operation are overlapped

Even when the WB stages for the memory load and for the operation are overlapped, the operation processing is pipelined in, because the load data and the operation result can be written to the register at the same timing.

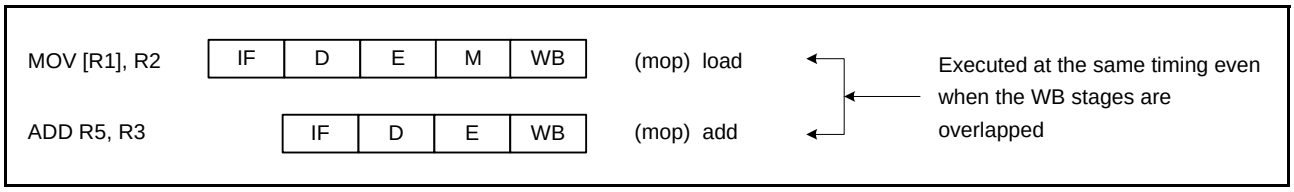


Figure 2.21 When WB Stages for the Memory Load and for the Operation are Overlapped

(c) When subsequent instruction writes to the same register before the end of memory load

Even when the subsequent instruction writes to the same register before the end of memory load, the operation processing is pipelined in, because the WB stage for the memory load is canceled.

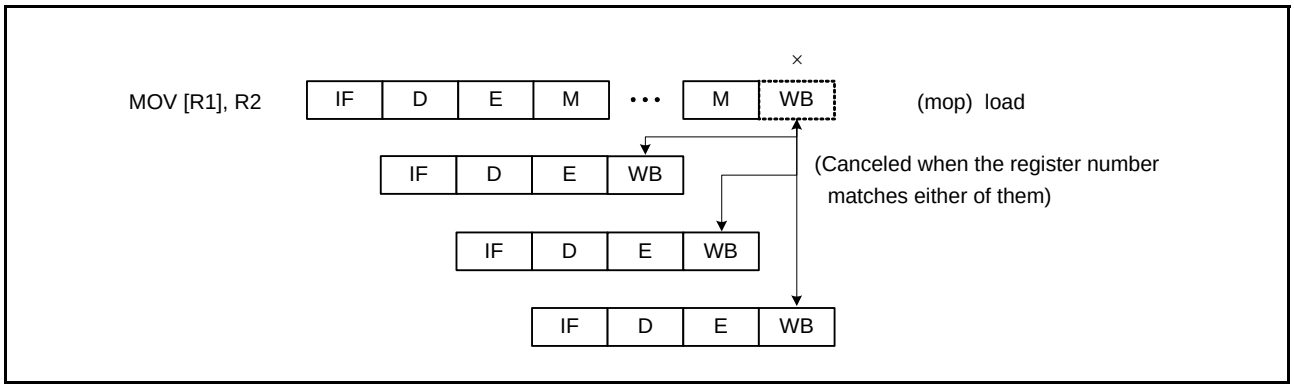


Figure 2.22 When Subsequent Instruction Writes to the Same Register before the End of Memory Load

(d) When the load data is not used by the subsequent instruction

When the load data is not used by the subsequent instruction, the subsequent operations are in fact executed earlier and the operation processing ends (out-of-order completion).

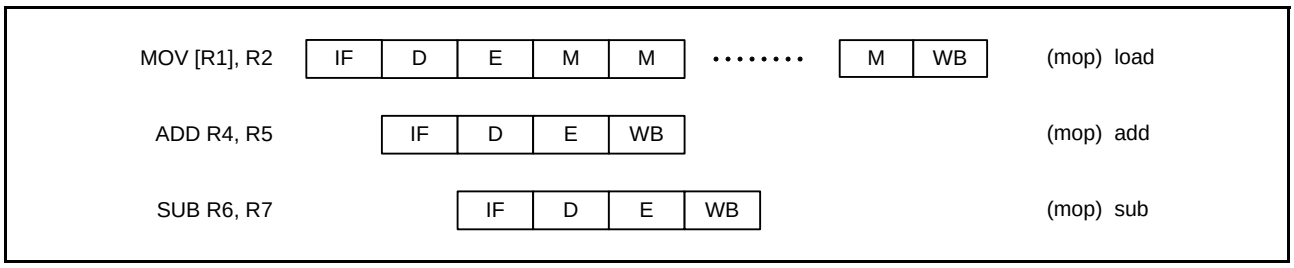


Figure 2.23 When Load Data is not Used by the Subsequent Instruction

2.8.3 Calculation of the Instruction Processing Time

Though the instruction processing time of the CPU varies according to the pipeline processing, the approximate time can be calculated in the following methods.

- Count the number of cycles (see Table 2.13 and Table 2.14)
- When the load data is used by the subsequent instruction, the number of cycles described as “latency” is counted as the number of cycles for the memory load instruction. For the cycles other than the memory load instruction, the number of cycles described as “throughput” is counted.
- If the instruction fetch stall is generated, the number of cycles increments.
- Depending on the system configuration, multiple cycles are required for the memory access.

2.8.4 Numbers of Cycles for Response to Interrupts

Table 2.15 lists numbers of cycles taken by processing for response to interrupts.

Table 2.15 Numbers of Cycles for Response to Interrupts

Type of Interrupt Request/Details of Processing	Fast Interrupt	Other Interrupts
ICU Judgment of priority order	2 cycles	
CPU Number of cycles from notification to acceptance of the interrupt request	N cycles (varies with the instruction being executed at the time the interrupt was received)	
CPU Pre-processing by hardware Saving the current PC and PSW values in RAM (or in control registers in the case of the fast interrupt) Reading of the vector Branching to the start of the exception handling routine	4 cycles	6 cycles

Times calculated from the values in Table 2.15 will be applicable when access to memory from the CPU is processed with no waiting. The RAM and ROM in products of this MCU allow such access. Numbers of cycles for response to interrupts can be minimized by placing program code (and vectors) in ROM and the stack in RAM. Furthermore, place the addresses where the exception handling routine start on 8-byte boundaries.

For information on the number of cycles from notification to acceptance of the interrupt request, indicated by N in the table above, see Table 2.13, Instructions that are Converted into a Single Micro-Operation, and Table 2.14, Instructions that are Converted into Multiple Micro-Operations.

The timing of interrupt acceptance depends on the state of the pipelines. For more information on this, see section 14.3.1, Acceptance Timing and Saved PC Value.

3. Operating Modes [144-, 120-, 112- and 100-Pin Versions]

3.1 Operating Mode Types and Selection

There are two types of operating-mode selection: one is be selected by the level on pins at the time of release from the reset state, and the other is selected by software after release from the reset state.
Table 3.1 shows the relationship between levels on the mode-setting pins (MD, P00) on release from the reset state and the operating mode selected at that time. For details on each of the operating modes, see section 3.3, Details of Operating Modes. Operation starts with the on-chip ROM (ROM, E2 DataFlash) enabled and the external bus disabled, regardless of the mode in which operation started. Set the SYSCR0.EXBE bit to 1 (external bus enabled) to enable the external bus.

Table 3.1 Selection of Operating Modes by the Mode-Setting Pins

Mode-Setting Pin			SYSCR0 Initial State	
MD*1	P00*2	Operating Mode	ROME	EXBE
High	—	Single-chip mode	1 (On-chip ROM enabled)	0 (External bus disabled)
Low	Low	Boot mode		
	High	USB boot mode		
		User boot mode		

Note 1. Do not change the level on the MD pin while the MCU is operating.
Note 2. The P00 pin can also be used as a general port pin.

Table 3.2 gives a list of the operating mode settings that can be made with system control register 0 (SYSCR0). For details on each of the operating modes, see section 3.3, Details of Operating Modes.

Table 3.2 Selection of Operating Modes by Register Setting

SYSCR0		
ROME	EXBE	Operating Mode
0 (On-chip ROM disabled)*1	0 (external bus disabled)	Single-chip mode, user boot mode
1 (On-chip ROM enabled)	0 (external bus disabled)	
0 (On-chip ROM disabled)*1	1 (external bus enabled)	On-chip ROM disabled extended mode
1 (On-chip ROM enabled)	1 (external bus enabled)	On-chip ROM enabled extended mode

Note 1. Once the ROME bit is set to 0, it cannot be reverted to 1.

The endian is selectable in single-chip mode and user boot mode. Endian is set in the given operating mode by using the endian selection bits (MDE[2:0]) in the register indicated in Table 3.3. For the correspondence between the setting and endian, see Table 3.4.

Table 3.3 Endian Setting

Operating Mode	Endian Setting Method
Single-chip mode	Endian is set in the endian selection register (MDES) in the option-setting memory.
User boot mode/USB boot mode	Endian is set in the endian selection register (MDEB) in the option-setting memory.

Table 3.4 Selection of Endian

Setting of the MDE[2:0] Bits	Selected Endian
000b	Big endian
111b	Little endian

3.2 Register Descriptions

3.2.1 Mode Monitor Register (MDMONR)

Address(es): 0008 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MD
Value after reset:	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit Name	Description	R/W
b0	MD	MD Pin Status Flag	0: The MD pin is low. 1: The MD pin is high.	R
b7 to b1	—	Reserved	These bits are read as 0.	R
b8	—	Reserved	The read value is undefined.	R
b15 to b9	—	Reserved	These bits are read as 0.	R

Note 1. This affects the level on the MD pin at the time of release from the reset state.

3.2.2 Mode Status Register (MDSR)

Address(es): 0008 0002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	UBTS	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0/1*1	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 1.	R
b4 to b1	—	Reserved	These bits are read as 0.	R
b5	UBTS	User Boot Mode Startup Flag	0: Started with single-chip mode. 1: Started with user boot mode.	R
b15 to b6	—	Reserved	These bits are read as 0.	R

Note 1. Depends on the operating mode at startup.

3.2.3 System Control Register 0 (SYSCR0)

Address(es): 0008 0006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	EXBE	ROME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	ROME	On-Chip ROM Enable	0: The on-chip ROM is disabled. 1: The on-chip ROM is enabled.	R/W
b1	EXBE	External Bus Enable	0: The external bus is disabled. 1: The external bus is enabled.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	SYSCR0 Key Code	These bits control permission and prohibition of writing to the SYSCR0 register. To modify the SYSCR0 register, write 5Ah to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W)*1

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Write data is not retained.

ROME Bit (On-Chip ROM Enable)

The ROME bit enables or disables the on-chip ROM (ROM, E2 DataFlash).
Once cleared to 0, it cannot be reverted to 1.
A 0 should not be written to this bit while a program is being executed from the on-chip ROM. After writing a 0 to this bit, be sure to disable the on-chip ROM by changing the ROME bit to 0 before proceeding with further processing.

EXBE Bit (External Bus Enable)

The EXBE bit enables or disables the external bus.
Do not write 0 to this bit while a program is running from an external address space. Write 0 to this bit after access to the external bus is completed. Furthermore, when an external address space is included in the range of transfer by the DMAC, prohibit DMA transfer before writing 0 to this bit.
After writing to the EXBE bit, confirm that its value has actually changed before proceeding with further processing.
When the EXBE bit is set to 1, the related I/O port settings must also be changed as required. For details, see section 21, Multi-Function Pin Controller (MPC).

KEY[7:0] Bits (SYSCR0 Key Code)

The KEY[7:0] bits enable or disable modifying SYSCR0.
When writing a value to the ROME or EXBE bit, write 5Ah to the KEY[7:0] bits simultaneously. If SYSCR0 is modified with a KEY[7:0] value other than 5Ah, the ROME and EXBE values remain unchanged.

3.2.4 System Control Register 1 (SYSCR1)

Address(es): 0008 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RAME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RAME	RAM Enable	0: The on-chip RAM is disabled. 1: The on-chip RAM is enabled.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RAME Bit (RAM Enable)

The RAME bit enables or disables the on-chip RAM.

The RAME bit is initialized to 1 after a reset is released.

A 0 should not be written to this bit during access to the on-chip RAM. When accessing the on-chip RAM immediately after changing the RAME bit from 0 (on-chip RAM disabled) to 1 (on-chip RAM enabled), make sure that the RAME bit is 1 before the access.

3.3 Details of Operating Modes

3.3.1 Single-Chip Mode

In single-chip mode, the external bus is disabled (SYSCR0.EXBE bit = 0) so that all I/O port pins are available for use as input or output port pins, inputs or outputs for peripheral functions, or as interrupt inputs.
If the high level is on the MD pin at the time of release from the reset state, the chip starts in single-chip mode. The on-chip ROM is enabled (SYSCR0.ROME bit = 1) at this time. The on-chip ROM can be disabled by software (by clearing the SYSCR0.ROME bit to 0), but it cannot be reenabled (by setting the SYSCR0.ROME bit to 1) once this is done.
Setting the SYSCR0.EXBE bit to 1 (enabling the external bus) causes a transition to on-chip ROM enabled extended mode or to on-chip ROM disabled extended mode, making the external bus available.

3.3.2 On-Chip ROM Enabled Extended Mode

In this mode, the on-chip ROM is enabled (SYSCR0.ROME bit = 1) and the external bus extension is enabled (SYSCR0.EXBE bit = 1). This mode allows some I/O ports to be used as data bus input/output, address bus output, or bus control signal input/output. For details, see section 21, Multi-Function Pin Controller (MPC).
After the chip has started up in single-chip mode, setting the SYSCR0.EXBE bit to 1 (external bus enabled) causes it to make the transition to on-chip ROM enabled extended mode.
Writing 0 to the SYSCR0.EXBE bit (external bus disabled) causes a transition to single-chip mode (on-chip ROM enabled).
Writing 0 to the SYSCR0.ROME bit (on-chip ROM disabled) causes a transition to on-chip ROM disabled extended mode.

3.3.3 On-Chip ROM Disabled Extended Mode

In this mode, the on-chip ROM is disabled (SYSCR0.ROME bit = 0) and the external bus extension is enabled (SYSCR0.EXBE bit = 1). This mode allows some I/O ports to be used as data bus input/output, address bus output, or bus control signal input/output. For details, see section 21, Multi-Function Pin Controller (MPC).
After the chip has started up in single-chip mode, setting the SYSCR0.EXBE bit to 1 (external bus enabled) and setting the SYSCR0.ROME bit to 0 (on-chip ROM disabled) causes it to make the transition to on-chip ROM disabled extended mode.
In this mode, the on-chip ROM cannot be enabled by setting the SYSCR0.ROME bit to 1.
Writing 0 to the SYSCR0.EXBE bit (external bus disabled) causes a transition to single-chip mode (on-chip ROM disabled).

3.3.4 Boot Mode

In this mode, the on-chip flash memory modifying program (boot program) stored in a dedicated area within the MCU operates. The on-chip flash memory (ROM, E2 DataFlash) can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (SCI1). For details, see section 41, Flash Memory.
The chip starts up in boot mode if the low level is on both the MD and P00 pins on release from the reset state.

3.3.5 USB Boot Mode

In this mode, the on-chip flash memory modifying program (USB boot program) stored in the user boot area at the time of shipping operates. On-chip flash memory (ROM, E2 DataFlash) can be modified from outside the MCU by using the USB. For details, see section 41, Flash Memory.
The chip starts up in USB boot mode if the low level is on the MD pin, and the high level is on the P00 pin on release from the reset state.

3.3.6 User Boot Mode

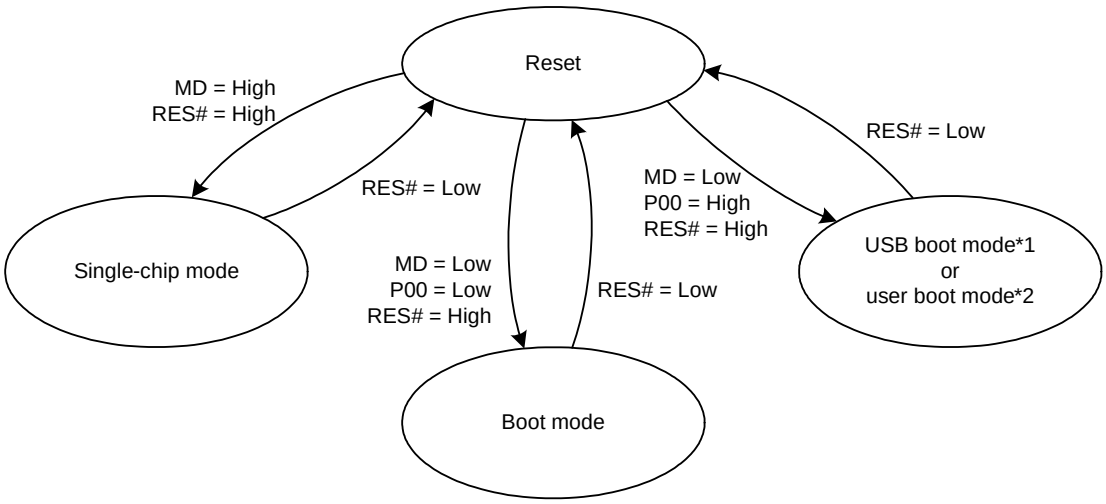
In user boot mode, an on-chip flash memory modifying program (user boot program) created by the user operates. After release from the reset state, the chip starts up in a state equivalent to single-chip mode.
After programming the prescribed values for UB code A and the UB code B, the chip starts up in user boot mode if the low level is on the MD pin and the high level is on the P00 pin on release from the reset state. For UB code A and UB code b, see section 8, Option-Setting Memory.
After the chip has started up in user boot mode, setting the SYSCR0.EXBE bit to 1 (external bus enabled) causes it to make the transition to on-chip ROM enabled extended mode.
At the time of shipping, USB boot program is stored in the user boot area. To store user boot program, erase the USB boot program. For details, see section 41, Flash Memory.

Note 1. In user mode, do not make a transition to software standby mode or deep software standby mode.
Note 2. The setting in the OFS0/OFS1 registers is ineffective in user boot mode, and the value becomes FFFF FFFFh.

3.4 Transitions of Operating Modes

3.4.1 Operating Mode Transitions Determined by the Mode-Setting Pins

Figure 3.1 shows operating mode transitions determined by the settings of the MD pin and the P00 pin.



Note 1. At the time of shipping, the user boot area holds a USB boot program. The product starts up in USB boot mode unless the USB boot program has been erased. It cannot start up in USB boot mode once the USB boot program has been erased.

Note 2. To start the chip in user boot mode, settings for the UB code A and UB code B in the option setting memory are required along with the levels set on the mode-setting pins.

Figure 3.1 Mode-Setting Pin Level and Operating Mode

3.4.2 Operating Mode Transitions According to Register Setting

Figure 3.2 shows operating mode transitions according to the setting of the ROME and EXBE bits in SYSCR0.

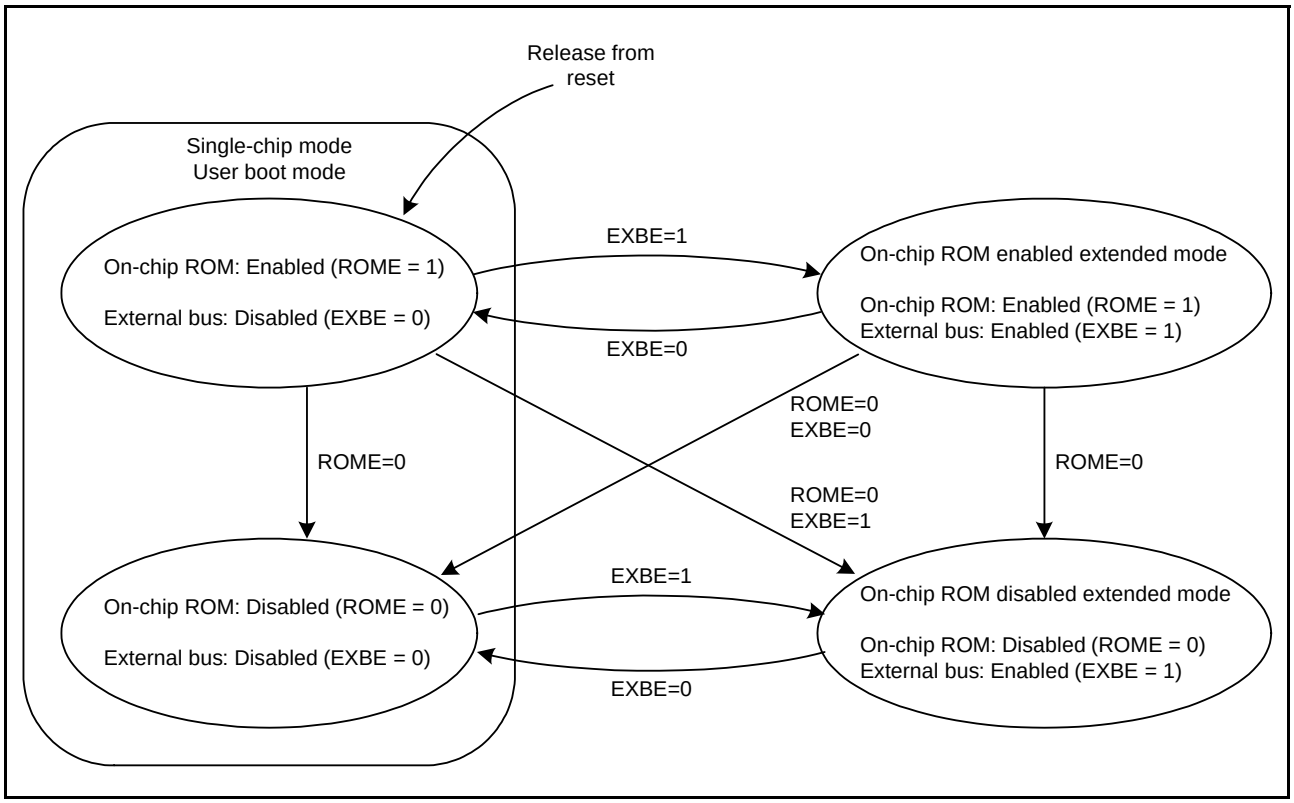


Figure 3.2 Setting of SYSCR0.ROME and EXBE Bits and Operating Modes

4. Operating Modes [64- and 48-Pin Versions]

4.1 Operating Mode Types and Selection

There are two types of operating-mode selection: one is be selected by the level on pins at the time of release from the reset state, and the other is selected by software after release from the reset state.
Table 4.1 shows the relationship between levels on the mode-setting pins (MD) on release from the reset state and the operating mode selected at that time. For details on each of the operating modes, see section 4.3, Details of Operating Modes. Operation starts with the on-chip ROM (ROM, E2 DataFlash) enabled and the external bus disabled, regardless of the mode in which operation started.

Table 4.1 Selection of Operating Modes by the Mode-Setting Pins

Mode-Setting Pin		SYSCR0 Initial State
MD*1	Operating Mode	ROME
High	Single-chip mode	1 (On-chip ROM enabled)
Low	Boot mode	

Note 1. Do not change the level on the MD pin while the MCU is operating.

Table 4.2 gives a list of the operating mode settings that can be made with system control register 0 (SYSCR0). For details on each of the operating modes, see section 4.3, Details of Operating Modes.

Table 4.2 Selection of Operating Modes by Register Setting

SYSCR0	
ROME	Operating Mode
0 (On-chip ROM disabled)*1	Single-chip mode
1 (On-chip ROM enabled)	

Note 1. Once the ROME bit is set to 0, it cannot be reverted to 1.

The endian is selectable in single-chip mode and user boot mode. Endian is set in the given operating mode by using the endian selection bits (MDE[2:0]) in the register indicated in Table 4.3. For the correspondence between the setting and endian, see Table 4.4.

Table 4.3 Endian Setting

Operating Mode	Endian Setting Method
Single-chip mode	Endian is set in the endian selection register (MDES) in the option-setting memory.

Table 4.4 Selection of Endian

Setting of the MDE[2:0] Bits	Selected Endian
000b	Big endian
111b	Little endian

4.2 Register Descriptions

4.2.1 Mode Monitor Register (MDMONR)

Address(es): 0008 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MD
Value after reset:	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0	0/1*1

Note 1. This affects the level on the MD pin at the time of release from the reset state.

Bit	Symbol	Bit Name	Description	R/W
b0	MD	MD Pin Status Flag	0: The MD pin is low. 1: The MD pin is high.	R
b7 to b1	—	Reserved	These bits are read as 0.	R
b8	—	Reserved	The read value is undefined.	R
b15 to b9	—	Reserved	These bits are read as 0.	R

4.2.2 System Control Register 0 (SYSCR0)

Address(es): 0008 0006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	ROME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	ROME	On-Chip ROM Enable	0: The on-chip ROM is disabled. 1: The on-chip ROM is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	SYSCR0 Key Code	These bits control permission and prohibition of writing to the SYSCR0 register. To modify the SYSCR0 register, write 5Ah to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W)*1

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Write data is not retained.

ROME Bit (On-Chip ROM Enable)

The ROME bit enables or disables the on-chip ROM (ROM, E2 DataFlash).

Once cleared to 0, it cannot be reverted to 1.

A 0 should not be written to this bit while a program is being executed from the on-chip ROM. After writing a 0 to this bit, be sure to disable the on-chip ROM by changing the ROME bit to 0 before proceeding with further processing.

4.2.3 System Control Register 1 (SYSCR1)

Address(es): 0008 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RAME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RAME	RAM Enable	0: The on-chip RAM is disabled. 1: The on-chip RAM is enabled.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RAME Bit (RAM Enable)

The RAME bit enables or disables the on-chip RAM.

A 0 should not be written to this bit during access to the on-chip RAM. When accessing the on-chip RAM immediately after changing the RAME bit from 0 (on-chip RAM disabled) to 1 (on-chip RAM enabled), make sure that the RAME bit is 1 before the access.

4.3 Details of Operating Modes

4.3.1 Single-Chip Mode

In this mode, the on-chip ROM is enabled or disabled, and all I/O ports can be used as input/output ports.
The on-chip ROM is enabled when this MCU is started. While the on-chip ROM is enabled (SYSCR0.ROME bit = 1), it can be disabled by clearing the SYSCR0.ROME bit to 0. While the on-chip ROM is disabled (SYSCR0.ROME bit = 0), it cannot be enabled by setting the SYSCR0.ROME bit to 1.

4.3.2 Boot Mode

In this mode, the on-chip flash memory modifying program (boot program) stored in a dedicated area within the MCU operates. The on-chip flash memory (ROM, E2 DataFlash) can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (SCI1). For details, see section 41, Flash Memory.

4.4 Transitions of Operating Modes

4.4.1 Operating Mode Transitions Determined by the Mode-Setting Pins

Figure 4.1 shows operating mode transitions determined by the settings of the MD pin.

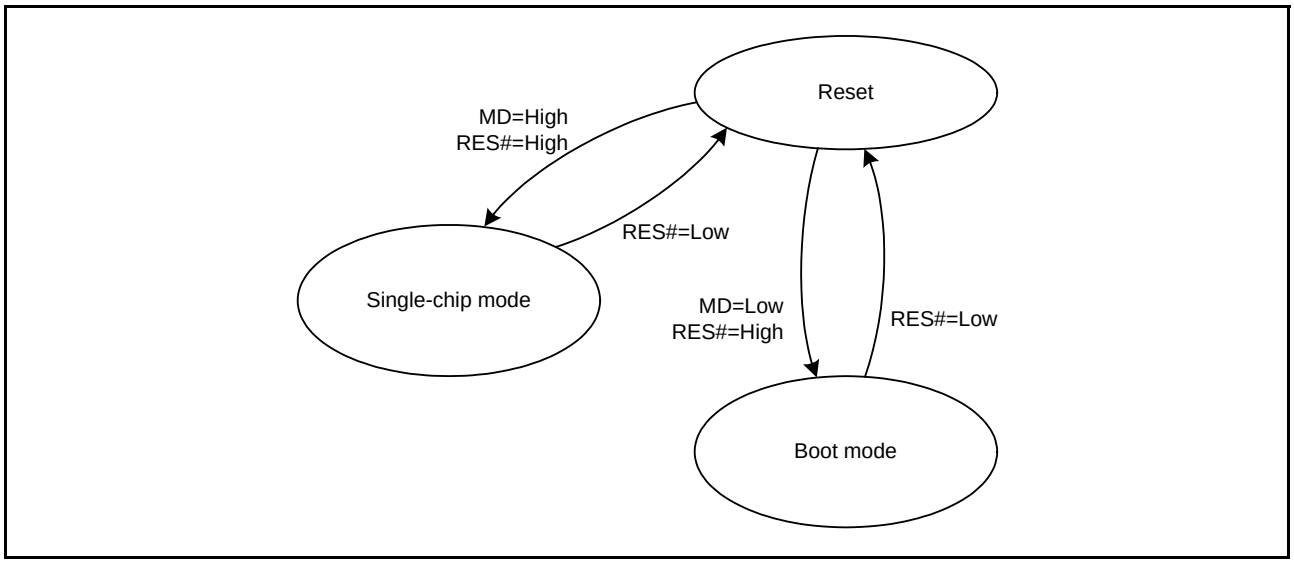


Figure 4.1 Mode-Setting Pin Level and Operating Mode

4.4.2 Operating Mode Transitions According to Register Setting

Figure 4.2 shows operating mode transitions according to the setting of the ROME and EXBE bits in SYSCR0.ROME bit. Operating modes can shift in the direction of arrow.

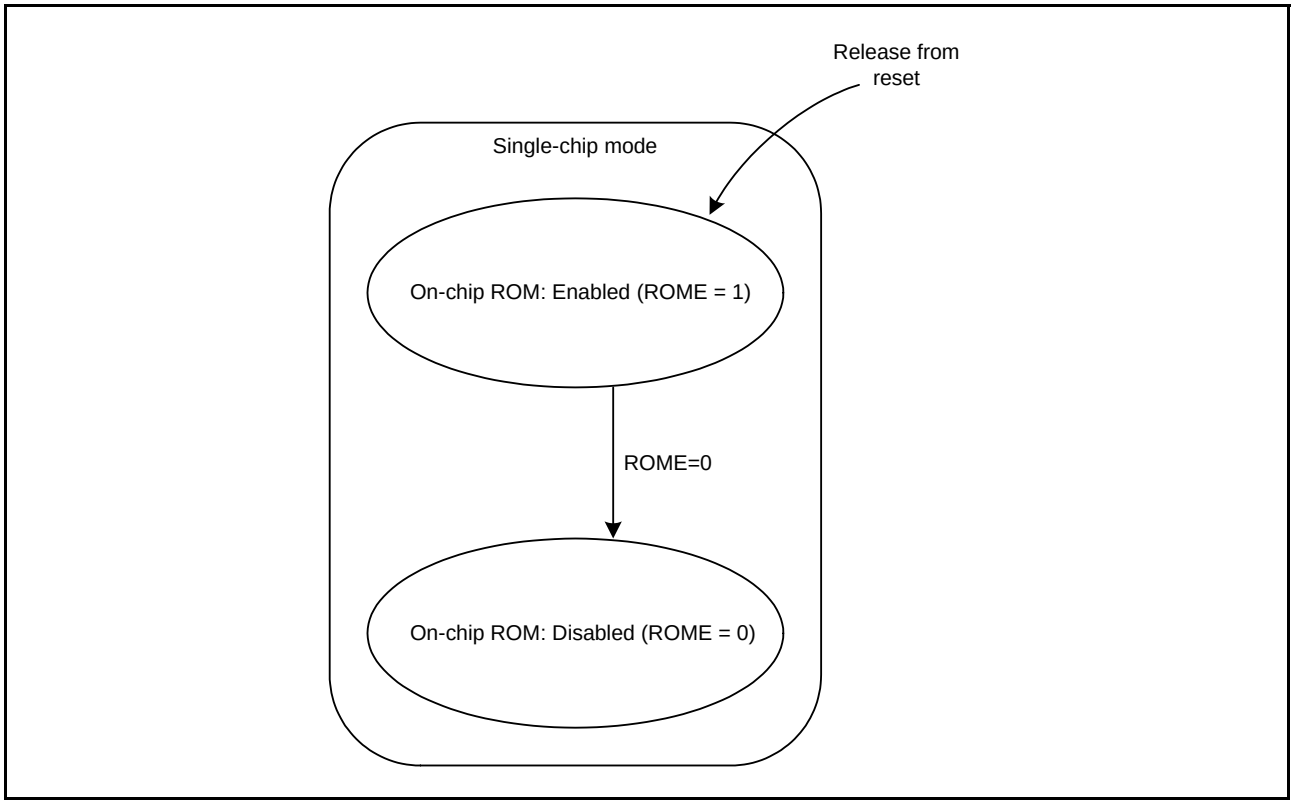
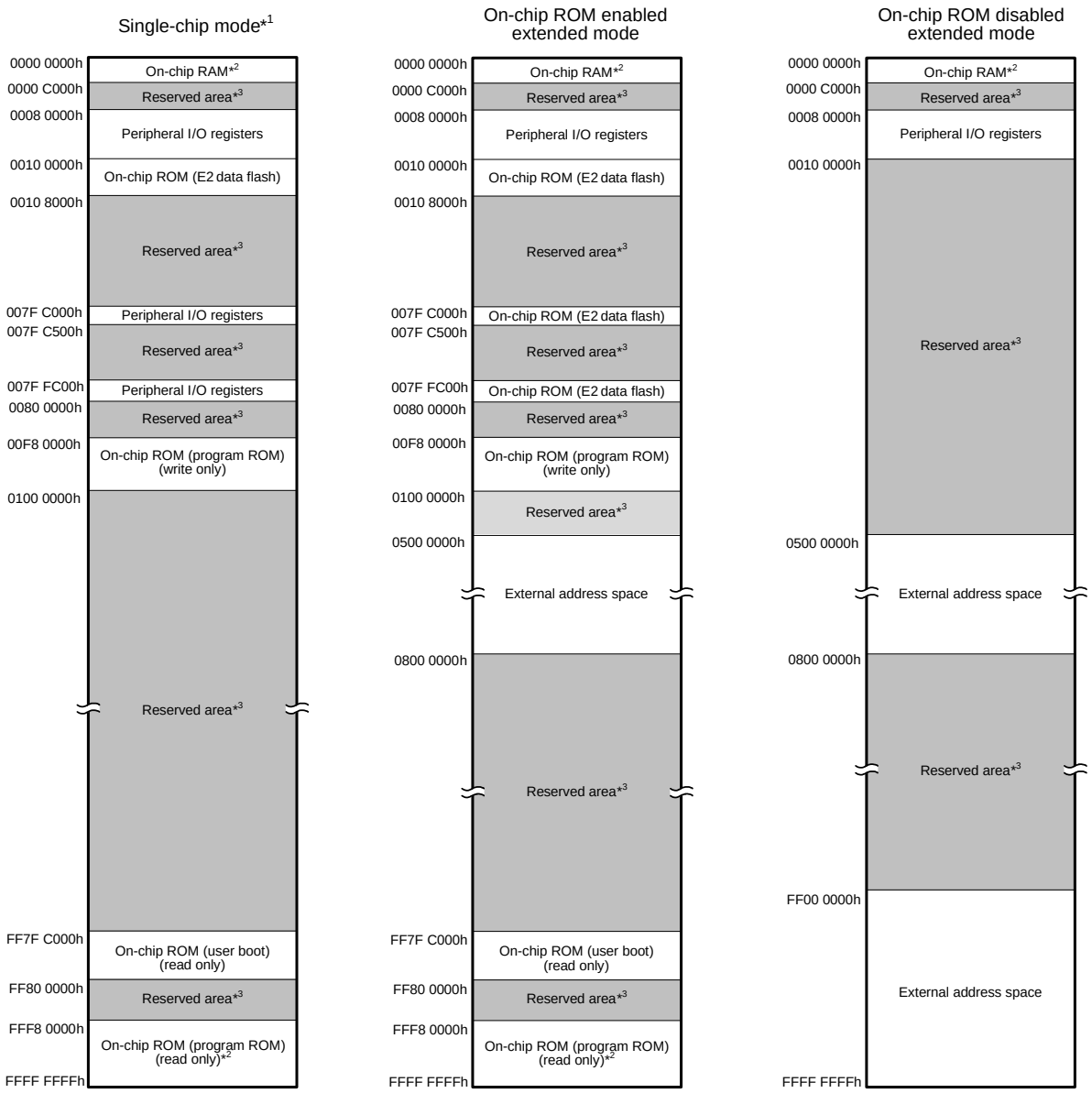


Figure 4.2 Mode-Setting Pin Level and Operating Mode

5. Address Space

5.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 5.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)		E2 DataFlash (bytes)	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	48 K	0000 0000h to 0000 BFFFh	32 K	0010 0000h to 0010 8000h
384 K	FFFA 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh		
256 K	FFFC 0000h to FFFF FFFFh	24 K	0000 0000h to 0000 5FFFh		
64 K	FFFF 0000h to FFFF FFFFh	8 K	0000 0000h to 0000 1FFFh	8 K	0010 0000h to 0010 2000h
48 K	FFFF 4000h to FFFF FFFFh				
32 K	FFFF 8000h to FFFF FFFFh				

Note:•See Table 1.3, List of Products, for the product type name.

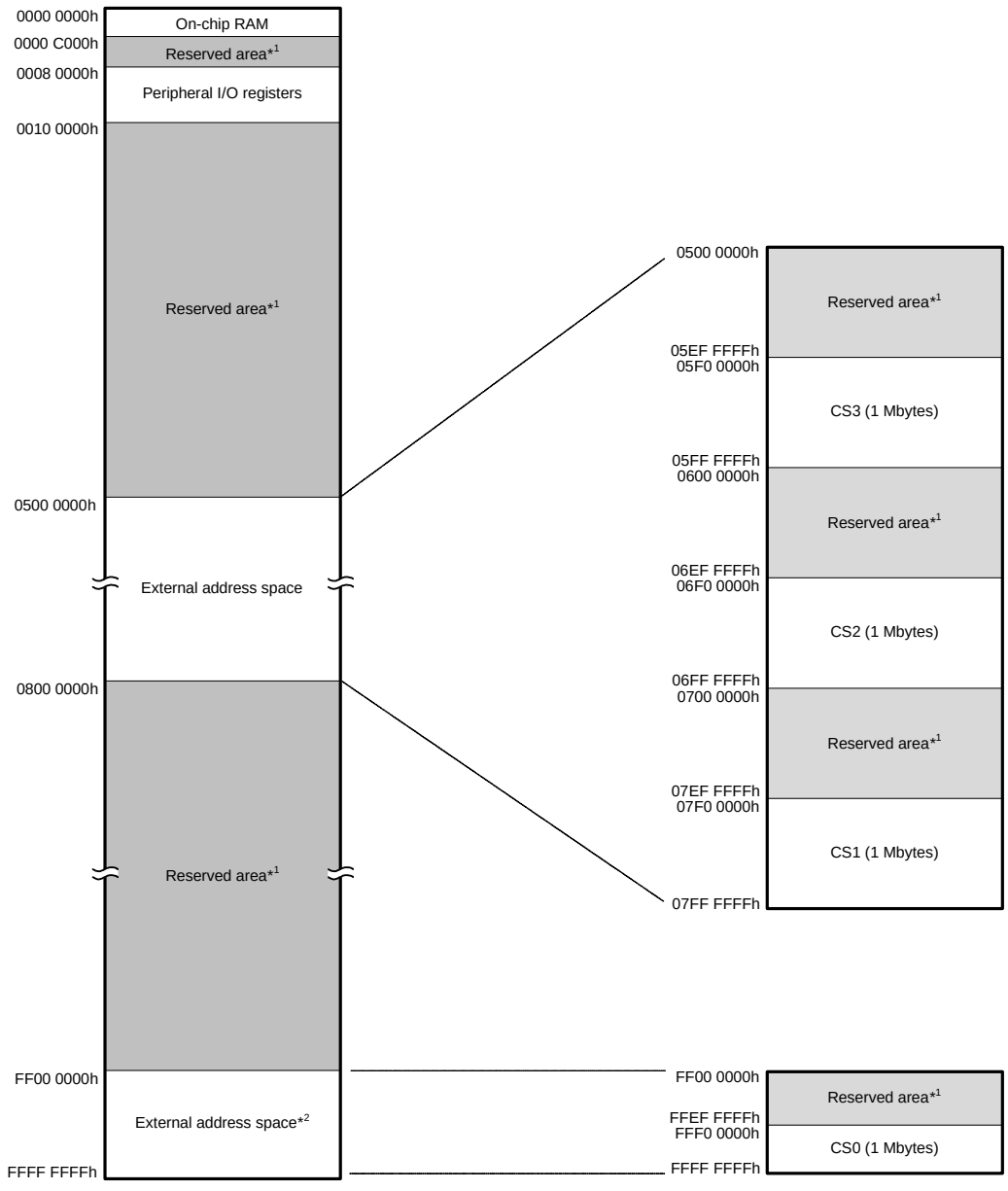
Note 3. Reserved areas should not be accessed.
Note 4. For details on the FCU, see section 41, Flash Memory.

Figure 5.1 Memory Map in Each Operating Mode

5.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 5.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 0800 0000h is as shown in Figure 5.1, Memory Map in Each Operating Mode.

Figure 5.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

6. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 6.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 6.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 6.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Note on Sleep Mode and Mode Transition

During sleep mode or a mode transition, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 6.1, List of I/O Registers (Address Order)).

6.1 I/O Register Addresses (Address Order)

Table 6.1 List of I/O Registers (Address Order) (1/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes	118, 126	
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK			118	Not present in versions with 64 or 48 pins.
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK			119, 126	
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK			120, 127	
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption	264	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK			265	
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK			266	
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK			268	
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit	231	
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK			233	Not present in versions with 64 or 48 pins.
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK			234	
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK			235	
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK			236	
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK			237	Not present in versions with 64 or 48 pins.
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK			238	
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK			239	
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK			240	
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK			241	
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK			242	
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Low Power Consumption	269	
0008 00A6h	SYSTEM	PLL Wait Control Register	PLLWTCR	8	8	3 ICLK			270	
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets	195	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK			196	
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA	214	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK			214	
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK			215	
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK			215	
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function	292	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses	371	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK			371	
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK			372	
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK			372	
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK			373	
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACA	429	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK			429	
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			430	
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			431	
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			433	
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			433	
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK			435	
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK			438	
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			438	

Table 6.1 List of I/O Registers (Address Order) (2/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACA	439	
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			440	
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			441	
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK			429	
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK			429	
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			430	
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			431	
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			432	
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			433	
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK			435	
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			438	
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK			439	
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK			440	
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			441	
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK			429	
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK			429	
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			430	
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			431	
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			432	
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			433	
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK			435	
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			438	
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK			439	
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK			440	
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			441	
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK			429	
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK			429	
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			430	
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			431	
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			432	
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			433	
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK			435	
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			438	
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK			439	
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK			440	
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			441	
0008 2200h	DMAC	DMACA Module Activation Register	DMAST	8	8	2 ICLK			442	
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2ICLK		DTCa	470	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2ICLK			471	
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2ICLK			471	
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2ICLK			472	
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2ICLK			473	
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1, 2 BCLK		Buses	363	Not present in versions with 64 or 48 pins.
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1, 2 BCLK			365	Not present in versions with 64 or 48 pins.
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1, 2 BCLK			368	Not present in versions with 64 or 48 pins.
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1, 2 BCLK			363	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (3/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1, 2 BCLK		Buses	365	Not present in versions with 64 or 48 pins.
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1, 2 BCLK			368	Not present in versions with 64 or 48 pins.
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1, 2 BCLK			363	Not present in versions with 64 or 48 pins.
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK			365	Not present in versions with 64 or 48 pins.
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK			368	Not present in versions with 64 or 48 pins.
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK			363	Not present in versions with 64 or 48 pins.
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK			365	Not present in versions with 64 or 48 pins.
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK			368	Not present in versions with 64 or 48 pins.
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK			357	Not present in versions with 64 or 48 pins.
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK			358	Not present in versions with 64 or 48 pins.
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK			357	Not present in versions with 64 or 48 pins.
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK			358	Not present in versions with 64 or 48 pins.
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK			357	Not present in versions with 64 or 48 pins.
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK			358	Not present in versions with 64 or 48 pins.
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK			357	Not present in versions with 64 or 48 pins.
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK			358	Not present in versions with 64 or 48 pins.
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK			360	Not present in versions with 64 or 48 pins.
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU	409	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK			410	
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK			409	
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK			410	
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK			409	
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK			410	
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK			409	
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK			410	
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK			409	
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK			410	
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK			409	
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK			410	
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK			409	
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK			410	
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK			409	
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK			410	

Table 6.1 List of I/O Registers (Address Order) (4/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK		MPU	411	
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK			412	
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK			413	
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK			414	
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK			415	
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK			416	
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK			416	
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK			417	
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK			418	
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK			420	
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK		ICUb	303	
0008 7015h	ICU	Interrupt Request Register 021	IR021	8	8	2 ICLK			303	
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK			303	
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK			303	
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK			303	
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK			303	
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK			303	
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK			303	
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 7023h	ICU	Interrupt Request Register 035	IR035	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 7024h	ICU	Interrupt Request Register 036	IR036	8	8	2 ICLK			303	
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8	2 ICLK			303	
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK			303	
0008 7027h	ICU	Interrupt Request Register 039	IR039	8	8	2 ICLK			303	
0008 7028h	ICU	Interrupt Request Register 040	IR040	8	8	2 ICLK			303	
0008 7029h	ICU	Interrupt Request Register 041	IR041	8	8	2 ICLK			303	
0008 702Ah	ICU	Interrupt Request Register 042	IR042	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 702Bh	ICU	Interrupt Request Register 043	IR043	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (5/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8	2 ICLK		ICUb	303	Not present in versions with 64 or 48 pins.
0008 7034h	ICU	Interrupt Request Register 052	IR052	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7035h	ICU	Interrupt Request Register 053	IR053	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7036h	ICU	Interrupt Request Register 054	IR054	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7037h	ICU	Interrupt Request Register 055	IR055	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7038h	ICU	Interrupt Request Register 056	IR056	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK			303	
0008 703Ah	ICU	Interrupt Request Register 058	IR058	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK			303	
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK			303	
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK			303	
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK			303	
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK			303	
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK			303	
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK			303	
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK			303	
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK			303	
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			303	
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			303	
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			303	

Table 6.1 List of I/O Registers (Address Order) (6/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK		ICUb	303	
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			303	
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			303	
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			303	
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			303	
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			303	
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			303	
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			303	
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			303	
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			303	
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			303	
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			303	
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			303	
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			303	
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			303	
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			303	
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			303	
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			303	
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			303	
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			303	
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			303	
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			303	
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			303	
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			303	
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			303	
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			303	
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			303	
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK			303	
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			303	
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			303	
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			303	
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			303	
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			303	
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			303	
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			303	
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			303	
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			303	
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			303	
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			303	
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			303	
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK			303	
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK			303	
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			303	
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK			303	
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK			303	
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (7/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK		ICUb	303	Not present in versions with 64 or 48 pins.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK			303	Not present in versions with 112, 100, 64 or 48 pins.
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK			303	
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK			303	
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK			303	
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK			303	
0008 70C6h	ICU	Interrupt Request Register 198	IR198	8	8	2 ICLK			303	
0008 70C7h	ICU	Interrupt Request Register 199	IR199	8	8	2 ICLK			303	
0008 70C8h	ICU	Interrupt Request Register 200	IR200	8	8	2 ICLK			303	
0008 70C9h	ICU	Interrupt Request Register 201	IR201	8	8	2 ICLK			303	
0008 70D6h	ICU	Interrupt Request Register 214	IR214	8	8	2 ICLK			303	

Table 6.1 List of I/O Registers (Address Order) (8/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 70D7h	ICU	Interrupt Request Register 215	IR215	8	8	2 ICLK		ICUb	303	
0008 70D8h	ICU	Interrupt Request Register 216	IR216	8	8	2 ICLK			303	
0008 70D9h	ICU	Interrupt Request Register 217	IR217	8	8	2 ICLK			303	
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK			303	
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK			303	
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK			303	Not present in versions with 64 or 48 pins.
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK			303	Not present in versions with 100, 64 or 48 pins.
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK			303	Not present in versions with 100, 64 or 48 pins.
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK			303	Not present in versions with 100, 64 or 48 pins.
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK			303	
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK			303	
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK			303	
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK			303	
0008 70E6h	ICU	Interrupt Request Register 230	IR230	8	8	2 ICLK			303	
0008 70E7h	ICU	Interrupt Request Register 231	IR231	8	8	2 ICLK			303	
0008 70E8h	ICU	Interrupt Request Register 232	IR232	8	8	2 ICLK			303	
0008 70E9h	ICU	Interrupt Request Register 233	IR233	8	8	2 ICLK			303	
0008 70EAh	ICU	Interrupt Request Register 234	IR234	8	8	2 ICLK			303	
0008 70EBh	ICU	Interrupt Request Register 235	IR235	8	8	2 ICLK			303	
0008 70ECh	ICU	Interrupt Request Register 236	IR236	8	8	2 ICLK			303	
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK			303	
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK			303	
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK			303	
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK			303	
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK			303	
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK			303	
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK			303	
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK			303	
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK			303	
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK			303	
0008 70FAh	ICU	Interrupt Request Register 250	IR250	8	8	2 ICLK			303	
0008 70FBh	ICU	Interrupt Request Register 251	IR251	8	8	2 ICLK			303	
0008 70FCh	ICU	Interrupt Request Register 252	IR252	8	8	2 ICLK			303	
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK			307	
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK			307	
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK			307	
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8	2 ICLK			307	
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8	2 ICLK			307	
0008 7121h	ICU	DTC Activation Enable Register 033	DTCER033	8	8	2 ICLK			307	Not present in versions with 112, 100, 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (9/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 7122h	ICU	DTC Activation Enable Register 034	DTCER034	8	8	2 ICLK		ICUb	307	Not present in versions with 112, 100, 64 or 48 pins.
0008 7127h	ICU	DTC Activation Enable Register 039	DTCER039	8	8	2 ICLK			307	
0008 7128h	ICU	DTC Activation Enable Register 040	DTCER040	8	8	2 ICLK			307	
0008 712Ah	ICU	DTC Activation Enable Register 042	DTCER042	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 712Bh	ICU	DTC Activation Enable Register 043	DTCER043	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7131h	ICU	DTC Activation Enable Register 049	DTCER049	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7132h	ICU	DTC Activation Enable Register 050	DTCER050	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7133h	ICU	DTC Activation Enable Register 051	DTCER051	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7134h	ICU	DTC Activation Enable Register 052	DTCER052	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7135h	ICU	DTC Activation Enable Register 053	DTCER053	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7136h	ICU	DTC Activation Enable Register 054	DTCER054	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7137h	ICU	DTC Activation Enable Register 055	DTCER055	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7138h	ICU	DTC Activation Enable Register 056	DTCER056	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 713Ah	ICU	DTC Activation Enable Register 058	DTCER058	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 713Bh	ICU	DTC Activation Enable Register 059	DTCER059	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 713Ch	ICU	DTC Activation Enable Register 060	DTCER060	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 713Dh	ICU	DTC Activation Enable Register 061	DTCER061	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 713Eh	ICU	DTC Activation Enable Register 062	DTCER062	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK			307	
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK			307	
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK			307	
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK			307	
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK			307	
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK			307	
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7162h	ICU	DTC Activation Enable Register 098	DTCER098	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK			307	
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK			307	

Table 6.1 List of I/O Registers (Address Order) (10/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 7168h	ICU	DTC Activation Enable Register 104	DTCER104	8	8	2 ICLK		ICUb	307	Not present in versions with 64 or 48 pins.
0008 7169h	ICU	DTC Activation Enable Register 105	DTCER105	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK			307	
0008 717Fh	ICU	DTC Activation Enable Register 127	DTCER127	8	8	2 ICLK			307	
0008 7180h	ICU	DTC Activation Enable Register 128	DTCER128	8	8	2 ICLK			307	
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK			307	
0008 7185h	ICU	DTC Activation Enable Register 133	DTCER133	8	8	2 ICLK			307	
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK			307	
0008 7189h	ICU	DTC Activation Enable Register 137	DTCER137	8	8	2 ICLK			307	
0008 718Ah	ICU	DTC Activation Enable Register 138	DTCER138	8	8	2 ICLK			307	
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8	2 ICLK			307	
0008 718Eh	ICU	DTC Activation Enable Register 142	DTCER142	8	8	2 ICLK			307	
0008 718Fh	ICU	DTC Activation Enable Register 143	DTCER143	8	8	2 ICLK			307	
0008 7190h	ICU	DTC Activation Enable Register 144	DTCER144	8	8	2 ICLK			307	
0008 7192h	ICU	DTC Activation Enable Register 146	DTCER146	8	8	2 ICLK			307	
0008 7193h	ICU	DTC Activation Enable Register 147	DTCER147	8	8	2 ICLK			307	
0008 7194h	ICU	DTC Activation Enable Register 148	DTCER148	8	8	2 ICLK			307	
0008 7195h	ICU	DTC Activation Enable Register 149	DTCER149	8	8	2 ICLK			307	
0008 7196h	ICU	DTC Activation Enable Register 150	DTCER150	8	8	2 ICLK			307	
0008 7197h	ICU	DTC Activation Enable Register 151	DTCER151	8	8	2 ICLK			307	
0008 7198h	ICU	DTC Activation Enable Register 152	DTCER152	8	8	2 ICLK			307	
0008 7199h	ICU	DTC Activation Enable Register 153	DTCER153	8	8	2 ICLK			307	
0008 719Ah	ICU	DTC Activation Enable Register 154	DTCER154	8	8	2 ICLK			307	
0008 719Bh	ICU	DTC Activation Enable Register 155	DTCER155	8	8	2 ICLK			307	
0008 719Ch	ICU	DTC Activation Enable Register 156	DTCER156	8	8	2 ICLK			307	
0008 719Dh	ICU	DTC Activation Enable Register 157	DTCER157	8	8	2 ICLK			307	
0008 71A1h	ICU	DTC Activation Enable Register 161	DTCER161	8	8	2 ICLK			307	
0008 71A2h	ICU	DTC Activation Enable Register 162	DTCER162	8	8	2 ICLK			307	
0008 71A3h	ICU	DTC Activation Enable Register 163	DTCER163	8	8	2 ICLK			307	
0008 71A4h	ICU	DTC Activation Enable Register 164	DTCER164	8	8	2 ICLK			307	
0008 71A5h	ICU	DTC Activation Enable Register 165	DTCER165	8	8	2 ICLK			307	
0008 71ABh	ICU	DTC Activation Enable Register 171	DTCER171	8	8	2 ICLK			307	
0008 71ACh	ICU	DTC Activation Enable Register 172	DTCER172	8	8	2 ICLK			307	
0008 71ADh	ICU	DTC Activation Enable Register 173	DTCER173	8	8	2 ICLK			307	
0008 71AEh	ICU	DTC Activation Enable Register 174	DTCER174	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71AFh	ICU	DTC Activation Enable Register 175	DTCER175	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B0h	ICU	DTC Activation Enable Register 176	DTCER176	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B1h	ICU	DTC Activation Enable Register 177	DTCER177	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B2h	ICU	DTC Activation Enable Register 178	DTCER178	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B3h	ICU	DTC Activation Enable Register 179	DTCER179	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B4h	ICU	DTC Activation Enable Register 180	DTCER180	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (11/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 71B5h	ICU	DTC Activation Enable Register 181	DTCER181	8	8	2 ICLK		ICUb	307	Not present in versions with 64 or 48 pins.
0008 71B6h	ICU	DTC Activation Enable Register 182	DTCER182	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B7h	ICU	DTC Activation Enable Register 183	DTCER183	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B8h	ICU	DTC Activation Enable Register 184	DTCER184	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71B9h	ICU	DTC Activation Enable Register 185	DTCER185	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71BAh	ICU	DTC Activation Enable Register 186	DTCER186	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71BBh	ICU	DTC Activation Enable Register 187	DTCER187	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71BCh	ICU	DTC Activation Enable Register 188	DTCER188	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71BDh	ICU	DTC Activation Enable Register 189	DTCER189	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71BFh	ICU	DTC Activation Enable Register 191	DTCER191	8	8	2 ICLK			307	Not present in versions with 112, 100, 64 or 48 pins.
0008 71C0h	ICU	DTC Activation Enable Register 192	DTCER192	8	8	2 ICLK			307	Not present in versions with 112, 100, 64 or 48 pins.
0008 71C3h	ICU	DTC Activation Enable Register 195	DTCER195	8	8	2 ICLK			307	
0008 71C4h	ICU	DTC Activation Enable Register 196	DTCER196	8	8	2 ICLK			307	
0008 71C6h	ICU	DTC Activation Enable Register 198	DTCER198	8	8	2 ICLK			307	
0008 71C7h	ICU	DTC Activation Enable Register 199	DTCER199	8	8	2 ICLK			307	
0008 71C8h	ICU	DTC Activation Enable Register 200	DTCER200	8	8	2 ICLK			307	
0008 71C9h	ICU	DTC Activation Enable Register 201	DTCER201	8	8	2 ICLK			307	
0008 71D6h	ICU	DTC Activation Enable Register 214	DTCER214	8	8	2 ICLK			307	
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8	2 ICLK			307	
0008 71D9h	ICU	DTC Activation Enable Register 217	DTCER217	8	8	2 ICLK			307	
0008 71DAh	ICU	DTC Activation Enable Register 218	DTCER218	8	8	2 ICLK			307	
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71DDh	ICU	DTC Activation Enable Register 221	DTCER221	8	8	2 ICLK			307	Not present in versions with 64 or 48 pins.
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK			307	Not present in versions with 100, 64 or 48 pins.
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK			307	Not present in versions with 100, 64 or 48 pins.
0008 71E2h	ICU	DTC Activation Enable Register 226	DTCER226	8	8	2 ICLK			307	
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8	2 ICLK			307	
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8	2 ICLK			307	
0008 71E5h	ICU	DTC Activation Enable Register 229	DTCER229	8	8	2 ICLK			307	
0008 71E6h	ICU	DTC Activation Enable Register 230	DTCER230	8	8	2 ICLK			307	
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8	2 ICLK			307	
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8	2 ICLK			307	
0008 71E9h	ICU	DTC Activation Enable Register 233	DTCER233	8	8	2 ICLK			307	

Table 6.1 List of I/O Registers (Address Order) (12/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 71EAh	ICU	DTC Activation Enable Register 234	DTCER234	8	8	2 ICLK		ICUb	307	
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8	2 ICLK			307	
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8	2 ICLK			307	
0008 71EEh	ICU	DTC Activation Enable Register 238	DTCER238	8	8	2 ICLK			307	
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK			307	
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK			307	
0008 71F1h	ICU	DTC Activation Enable Register 241	DTCER241	8	8	2 ICLK			307	
0008 71F2h	ICU	DTC Activation Enable Register 242	DTCER242	8	8	2 ICLK			307	
0008 71F4h	ICU	DTC Activation Enable Register 244	DTCER244	8	8	2 ICLK			307	
0008 71F5h	ICU	DTC Activation Enable Register 245	DTCER245	8	8	2 ICLK			307	
0008 71F6h	ICU	DTC Activation Enable Register 246	DTCER246	8	8	2 ICLK			307	
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK			307	
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK			307	
0008 71FAh	ICU	DTC Activation Enable Register 250	DTCER250	8	8	2 ICLK			307	
0008 71FBh	ICU	DTC Activation Enable Register 251	DTCER251	8	8	2 ICLK			307	
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK			304	
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK			304	
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK			304	
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK			304	
0008 7206h	ICU	Interrupt Request Enable Register 06	IER06	8	8	2 ICLK			304	Not present in versions with 64 or 48 pins.
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK			304	
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK			304	
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK			304	Not present in versions with 112, 100, 64 or 48 pins.
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK			304	
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK			304	Not present in versions with 64 or 48 pins.
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK			304	
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK			304	
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK			304	
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK			304	
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8	2 ICLK			304	
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8	2 ICLK			304	
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8	2 ICLK			304	
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK			304	
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK			304	Not present in versions with 64 or 48 pins.
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK			304	Not present in versions with 64 or 48 pins.
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8	2 ICLK			304	
0008 7219h	ICU	Interrupt Request Enable Register 19	IER19	8	8	2 ICLK			304	
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8	2 ICLK			304	
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK			304	
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK			304	
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK			304	
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK			304	
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK			304	
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK			307	
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK			306	

Table 6.1 List of I/O Registers (Address Order) (13/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK		ICUb	305	
0008 7301h	ICU	Interrupt Source Priority Register 001	IPR001	8	8	2 ICLK			305	
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8	2 ICLK			305	
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK			305	
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK			305	
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK			305	
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK			305	
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK			305	
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK			305	Not present in versions with 112, 100, 64 or 48 pins.
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK			305	Not present in versions with 112, 100, 64 or 48 pins.
0008 7323h	ICU	Interrupt Source Priority Register 035	IPR035	8	8	2 ICLK			305	Not present in versions with 112, 100, 64 or 48 pins.
0008 7324h	ICU	Interrupt Source Priority Register 036	IPR036	8	8	2 ICLK			305	
0008 7327h	ICU	Interrupt Source Priority Register 039	IPR039	8	8	2 ICLK			305	
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8	2 ICLK			305	
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8	2 ICLK			305	
0008 732Ah	ICU	Interrupt Source Priority Register 042	IPR042	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 732B	ICU	Interrupt Source Priority Register 043	IPR043	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 732C	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 732Dh	ICU	Interrupt Source Priority Register 045	IPR045	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7331h	ICU	Interrupt Source Priority Register 049	IPR049	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7334h	ICU	Interrupt Source Priority Register 052	IPR052	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7336h	ICU	Interrupt Source Priority Register 054	IPR054	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7337h	ICU	Interrupt Source Priority Register 055	IPR055	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7338h	ICU	Interrupt Source Priority Register 056	IPR056	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK			305	
0008 733Ah	ICU	Interrupt Source Priority Register 058	IPR058	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 733Dh	ICU	Interrupt Source Priority Register 061	IPR061	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 733Eh	ICU	Interrupt Source Priority Register 062	IPR062	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK			305	

Table 6.1 List of I/O Registers (Address Order) (14/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK		ICUb	305	
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK			305	
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK			305	
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK			305	
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK			305	
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 735Ah	ICU	Interrupt Source Priority Register 090	IPR090	8	8	2 ICLK			305	Not present in versions with 112, 100, 64 or 48 pins.
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK			305	
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK			305	
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK			305	
0008 737Ah	ICU	Interrupt Source Priority Register 122	IPR122	8	8	2 ICLK			305	
0008 737Eh	ICU	Interrupt Source Priority Register 126	IPR126	8	8	2 ICLK			305	
0008 7382h	ICU	Interrupt Source Priority Register 130	IPR130	8	8	2 ICLK			305	
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK			305	
0008 7387h	ICU	Interrupt Source Priority Register 135	IPR135	8	8	2 ICLK			305	
0008 7389h	ICU	Interrupt Source Priority Register 137	IPR137	8	8	2 ICLK			305	
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK			305	
0008 738Dh	ICU	Interrupt Source Priority Register 141	IPR141	8	8	2 ICLK			305	
0008 7391h	ICU	Interrupt Source Priority Register 145	IPR145	8	8	2 ICLK			305	
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK			305	
0008 7396h	ICU	Interrupt Source Priority Register 150	IPR150	8	8	2 ICLK			305	
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK			305	
0008 739Ah	ICU	Interrupt Source Priority Register 154	IPR154	8	8	2 ICLK			305	
0008 739Eh	ICU	Interrupt Source Priority Register 158	IPR158	8	8	2 ICLK			305	
0008 73A1h	ICU	Interrupt Source Priority Register 161	IPR161	8	8	2 ICLK			305	
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK			305	
0008 73A5h	ICU	Interrupt Source Priority Register 165	IPR165	8	8	2 ICLK			305	
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			305	
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			305	
0008 73ACh	ICU	Interrupt Source Priority Register 172	IPR172	8	8	2 ICLK			305	
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK			305	
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (15/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK		ICUb	305	Not present in versions with 64 or 48 pins.
0008 73B9h	ICU	Interrupt Source Priority Register 185	IPR185	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 73BCh	ICU	Interrupt Source Priority Register 188	IPR188	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 73BEh	ICU	Interrupt Source Priority Register 190	IPR190	8	8	2 ICLK			305	Not present in versions with 112, 100, 64 or 48 pins.
0008 73C2h	ICU	Interrupt Source Priority Register 194	IPR194	8	8	2 ICLK			305	
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8	2 ICLK			305	
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8	2 ICLK			305	
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8	2 ICLK			305	
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8	2 ICLK			305	
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK			305	
0008 73D9h	ICU	Interrupt Source Priority Register 217	IPR217	8	8	2 ICLK			305	
0008 73DCh	ICU	Interrupt Source Priority Register 220	IPR220	8	8	2 ICLK			305	Not present in versions with 64 or 48 pins.
0008 73DFh	ICU	Interrupt Source Priority Register 223	IPR223	8	8	2 ICLK			305	Not present in versions with 100, 64 or 48 pins.
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK			305	
0008 73E5h	ICU	Interrupt Source Priority Register 229	IPR229	8	8	2 ICLK			305	
0008 73E8h	ICU	Interrupt Source Priority Register 232	IPR232	8	8	2 ICLK			305	
0008 73EBh	ICU	Interrupt Source Priority Register 235	IPR235	8	8	2 ICLK			305	
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK			305	
0008 73F1h	ICU	Interrupt Source Priority Register 241	IPR241	8	8	2 ICLK			305	
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK			305	
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK			305	
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK			305	
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK			308	
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK			308	
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK			308	
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK			308	
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK			309	
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK			309	
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK			309	
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK			309	
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK			309	
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK			309	
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK			309	Not present in versions with 64 or 48 pins.
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK			309	Not present in versions with 64 or 48 pins.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK			310	
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			311	
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			312	
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			314	
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			315	
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			316	
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			316	

Table 6.1 List of I/O Registers (Address Order) (16/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK		ICUb	317	
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	991	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		992	
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		993	
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		993	
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		992	
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		993	
0008 800Ch	CMT1	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		993	
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		991	
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		992	
0008 8014h	CMT2	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		993	
0008 8016h	CMT2	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		993	
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		992	
0008 801Ah	CMT3	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		993	
0008 801Ch	CMT3	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		993	
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA	999	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		1000	
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		1003	
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		1004	
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa	1014	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		1015	
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		1018	
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK		1019	
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK		1019	
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa	1620	Not present in versions with 64 or 48 pins.
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK		1620	Not present in versions with 64 or 48 pins.
0008 80C4h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK		1621	Not present in versions with 64 or 48 pins.
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK		1622	Not present in versions with 64 or 48 pins.
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK		1623	Not present in versions with 64 or 48 pins.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC	1454	
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK		1454	
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK		1455	
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	1255	
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		1257	
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		1260	
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		1261	
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		1263	
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		1265	
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		1267	
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		1268	
0008 8308h	RIIC0	I^2C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK		1269	
0008 8309h	RIIC0	I^2C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK		1272	
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK		1275	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK		1281	
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK		1276	
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK		1281	

Table 6.1 List of I/O Registers (Address Order) (17/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIIC	1275	
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK		1276	
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK		1275	
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK		1276	
0008 8310h	RIIC0	I²C Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK		1277	
0008 8311h	RIIC0	I²C Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK		1278	
0008 8312h	RIIC0	I²C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK		1280	
0008 8313h	RIIC0	I²C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK		1280	
0008 8320h	RIIC1	I²C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK		1255	Not present in versions with 112, 100, 64, or 48 pins.
0008 8321h	RIIC1	I²C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		1257	Not present in versions with 112, 100, 64, or 48 pins.
0008 8322h	RIIC1	I²C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		1260	Not present in versions with 112, 100, 64, or 48 pins.
0008 8323h	RIIC1	I²C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		1261	Not present in versions with 112, 100, 64, or 48 pins.
0008 8324h	RIIC1	I²C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		1263	Not present in versions with 112, 100, 64, or 48 pins.
0008 8325h	RIIC1	I²C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		1265	Not present in versions with 112, 100, 64, or 48 pins.
0008 8326h	RIIC1	I²C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		1267	Not present in versions with 112, 100, 64, or 48 pins.
0008 8327h	RIIC1	I²C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		1268	Not present in versions with 112, 100, 64, or 48 pins.
0008 8328h	RIIC1	I²C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK		1269	Not present in versions with 112, 100, 64, or 48 pins.
0008 8329h	RIIC1	I²C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK		1272	Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK		1275	Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK		1281	Not present in versions with 112, 100, 64, or 48 pins.
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK		1276	Not present in versions with 112, 100, 64, or 48 pins.
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK		1281	Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK		1275	Not present in versions with 112, 100, 64, or 48 pins.
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK		1276	Not present in versions with 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (18/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIIC	1275	Not present in versions with 112, 100, 64, or 48 pins.
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK		1276	Not present in versions with 112, 100, 64, or 48 pins.
0008 8330h	RIIC1	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK		1277	Not present in versions with 112, 100, 64, or 48 pins.
0008 8331h	RIIC1	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK		1278	Not present in versions with 112, 100, 64, or 48 pins.
0008 8332h	RIIC1	I2C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK		1280	Not present in versions with 112, 100, 64, or 48 pins.
0008 8333h	RIIC1	I2C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK		1280	Not present in versions with 112, 100, 64, or 48 pins.
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK	RSPI	1380	
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		1382	
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		1383	
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		1384	
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		1386	
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		1390	
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		1391	
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK		1392	
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		1393	
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		1395	
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		1396	
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		1396	
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		1397	
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		1398	
0008 83A0h	RSPI1	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK		1380	Not present in versions with 64 or 48 pins.
0008 83A1h	RSPI1	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		1382	Not present in versions with 64 or 48 pins.
0008 83A2h	RSPI1	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		1383	Not present in versions with 64 or 48 pins.
0008 83A3h	RSPI1	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		1384	Not present in versions with 64 or 48 pins.
0008 83A4h	RSPI1	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		1386	Not present in versions with 64 or 48 pins.
0008 83A8h	RSPI1	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		1390	Not present in versions with 64 or 48 pins.
0008 83A9h	RSPI1	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		1391	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (19/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 83AAh	RSPI1	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK	RSPI	1392	Not present in versions with 64 or 48 pins.
0008 83ABh	RSPI1	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		1393	Not present in versions with 64 or 48 pins.
0008 83ACh	RSPI1	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		1395	Not present in versions with 64 or 48 pins.
0008 83ADh	RSPI1	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		1396	Not present in versions with 64 or 48 pins.
0008 83AEh	RSPI1	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		1396	Not present in versions with 64 or 48 pins.
0008 83AFh	RSPI1	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		1397	Not present in versions with 64 or 48 pins.
0008 83B0h	RSPI1	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 83B2h	RSPI1	RSPI Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 83B4h	RSPI1	RSPI Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 83B6h	RSPI1	RSPI Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 83B8h	RSPI1	RSPI Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 83BAh	RSPI1	RSPI Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 83BCh	RSPI1	RSPI Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 83BEh	RSPI1	RSPI Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		1398	Not present in versions with 64 or 48 pins.
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12ADB	1470	
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		1474	
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2, 3 PCLKB	2 ICLK		1476	
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		1477	
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		1478	
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		1480	
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		1475	
0008 9018h	S12AD	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		1466	
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		1469	
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK		1466	
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		1466	
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		1466	
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		1466	
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 144, 120, 112, or 100 pins.

Table 6.1 List of I/O Registers (Address Order) (20/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	S12ADB	1466	Not present in versions with 144, 120, 112, or 100 pins.
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		1485	
0008 9066h	S12AD	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		1486	
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		1485	
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		1485	
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		1485	
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 144, 120, 112, or 100 pins.
0008 9077h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 144, 120, 112, or 100 pins.
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 144, 120, 112, or 100 pins.
0008 9079h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 144, 120, 112, or 100 pins.
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		1487	
0008 9084h	S12AD	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		1466	
0008 9086h	S12AD	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		1466	
0008 908Ah	S12AD	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		1495	Not present in versions with 64 or 48 pins.
0008 90E0h	S12AD	Comparator Operating Mode Selection Register 0	ADCMPMD0	16	16	2, 3 PCLKB	2 ICLK		1489	
0008 90E2h	S12AD	Comparator Operating-Mode Selection Register 1	ADCMPMD1	16	16	2, 3 PCLKB	2 ICLK		1490	
0008 90E4h	S12AD	Comparator Filter-Mode Register	ADCMPNR0	16	16	2, 3 PCLKB	2 ICLK		1492	
0008 90E8h	S12AD	Comparator Detection Flag Register	ADCMPFR	8	8	2, 3 PCLKB	2 ICLK		1493	
0008 90EAh	S12AD	Comparator Interrupt Selection Register	ADCMPSEL	16	16	2, 3 PCLKB	2 ICLK		1494	
0008 90FCh	S12AD	A/D Group Scan Priority Control Register	ADGSPMR	16	16	2, 3 PCLKB	2 ICLK		1496	Not present in versions with 64 or 48 pins.
0008 9100h	S12AD1	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK		1470	Not present in versions with 64 or 48 pins.
0008 9104h	S12AD1	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		1474	Not present in versions with 64 or 48 pins.
0008 9108h	S12AD1	A/D-Converted Value Addition Mode Select Register (ADADS)	ADADS	16	16	2, 3 PCLKB	2 ICLK		1476	Not present in versions with 64 or 48 pins.
0008 910Ch	S12AD1	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		1477	Not present in versions with 64 or 48 pins.
0008 910Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		1478	Not present in versions with 64 or 48 pins.
0008 9110h	S12AD1	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		1480	Not present in versions with 64 or 48 pins.
0008 9114h	S12AD1	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		1475	Not present in versions with 64 or 48 pins.
0008 9118h	S12AD1	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 64 or 48 pins.
0008 911Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		1469	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (21/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 9120h	S12AD1	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADB	1466	Not present in versions with 64 or 48 pins.
0008 9122h	S12AD1	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 64 or 48 pins.
0008 9124h	S12AD1	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 64 or 48 pins.
0008 9126h	S12AD1	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 64 or 48 pins.
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 64 or 48 pins.
0008 9166h	S12AD1	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		1486	Not present in versions with 64 or 48 pins.
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 64 or 48 pins.
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 64 or 48 pins.
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		1485	Not present in versions with 64 or 48 pins.
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		1487	Not present in versions with 64 or 48 pins.
0008 9184h	S12AD1	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 64 or 48 pins.
0008 9186h	S12AD1	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		1466	Not present in versions with 64 or 48 pins.
0008 918Ah	S12AD1	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		1495	Not present in versions with 64 or 48 pins.
0008 91E0h	S12AD1	Comparator Operating Mode Selection Register 0	ADCMPMD0	16	16	2, 3 PCLKB	2 ICLK		1489	Not present in versions with 64 or 48 pins.
0008 91E2h	S12AD1	Comparator Operating-Mode Selection Register 1	ADCMPMD1	16	16	2, 3 PCLKB	2 ICLK		1490	Not present in versions with 64 or 48 pins.
0008 91E4h	S12AD1	Comparator Filter-Mode Register	ADCMPNR0	16	16	2, 3 PCLKB	2 ICLK		1492	Not present in versions with 64 or 48 pins.
0008 91E8h	S12AD1	Comparator Detection Flag Register	ADCMPFR	8	8	2, 3 PCLKB	2 ICLK		1493	Not present in versions with 64 or 48 pins.
0008 91EAh	S12AD1	Comparator Interrupt Selection Register	ADCMPSEL	16	16	2, 3 PCLKB	2 ICLK		1494	Not present in versions with 64 or 48 pins.
0008 9800h	AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	AD	1590	Not present in versions with 64 or 48 pins.
0008 9804h	AD	A/D Channel Select Register 0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK		1592	Not present in versions with 64 or 48 pins.
0008 9806h	AD	A/D Channel Select Register 1	ADANSA1	16	16	2, 3 PCLKB	2 ICLK		1593	Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 9808h	AD	A/D-Converted Value Addition Mode Select Register0	ADADS0	16	16	2, 3 PCLKB	2 ICLK		1594	Not present in versions with 64 or 48 pins.
0008 980Ah	AD	A/D-Converted Value Addition Mode Select Register1	ADADS1	16	16	2, 3 PCLKB	2 ICLK		1595	Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 980Ch	AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		1597	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (22/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 980Eh	AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK	AD	1598	Not present in versions with 64 or 48 pins.
0008 9810h	AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		1600	Not present in versions with 64 or 48 pins.
0008 981Eh	AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		1588	Not present in versions with 64 or 48 pins.
0008 9820h	AD	A/D Data Register A	ADDRA	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9822h	AD	A/D Data Register B	ADDRB	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9824h	AD	A/D Data Register C	ADDRC	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9826h	AD	A/D Data Register D	ADDRD	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9828h	AD	A/D Data Register E	ADDRE	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 982Ah	AD	A/D Data Register F	ADDRF	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 982Ch	AD	A/D Data Register G	ADDRG	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 982Eh	AD	A/D Data Register H	ADDRH	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9830h	AD	A/D Data Register I	ADDRI	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9832h	AD	A/D Data Register J	ADDRJ	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9834h	AD	A/D Data Register K	ADDRK	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9836h	AD	A/D Data Register L	ADDRL	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 64 or 48 pins.
0008 9838h	AD	A/D Data Register M	ADDRM	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ah	AD	A/D Data Register N	ADDRN	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ch	AD	A/D Data Register O	ADDRO	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Eh	AD	A/D Data Register P	ADDRP	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9840h	AD	A/D Data Register Q	ADDRQ	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9842h	AD	A/D Data Register R	ADDRR	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9844h	AD	A/D Data Register S	ADDRS	16	16	2, 3 PCLKB	2 ICLK		1586	Not present in versions with 120, 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (23/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 9846h	AD	A/D Data Register T	ADDRT	16	16	2, 3 PCLKB	2 ICLK	AD	1586	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9860h	AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 9861h	AD	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK		1604	Not present in versions with 64 or 48 pins.
0008 9873h	AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 9874h	AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 9875h	AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 9876h	AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 9877h	AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 9878h	AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 9879h	AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK		1603	Not present in versions with 64 or 48 pins.
0008 987Dh	AD	Digital Power Supply Control Circuit Output Register	ADDPCONR	8	8	2, 3 PCLKB	2 ICLK		1604	Not present in versions with 64, or 48 pins.
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	1141	
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		1153	
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		1144	
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		1140	
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		1148	
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		1140	
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		1152	
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		1161	
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		1163	
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		1164	
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		1165	
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		1166	
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		1168	
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		1169	
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK		1141	
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		1153	
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		1144	
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		1140	
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		1148	
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		1140	
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		1152	
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		1161	
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		1163	
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		1164	
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		1165	
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		1166	
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		1168	
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		1169	

Table 6.1 List of I/O Registers (Address Order) (24/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 A040h	SCI2	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	1141	Not present in versions with 64 or 48 pins.
0008 A041h	SCI2	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		1153	Not present in versions with 64 or 48 pins.
0008 A042h	SCI2	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		1144	Not present in versions with 64 or 48 pins.
0008 A043h	SCI2	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		1140	Not present in versions with 64 or 48 pins.
0008 A044h	SCI2	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		1148	Not present in versions with 64 or 48 pins.
0008 A045h	SCI2	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		1140	Not present in versions with 64 or 48 pins.
0008 A046h	SCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		1152	Not present in versions with 64 or 48 pins.
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		1161	Not present in versions with 64 or 48 pins.
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		1163	Not present in versions with 64 or 48 pins.
0008 A049h	SCI2	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		1164	Not present in versions with 64 or 48 pins.
0008 A04Ah	SCI2	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		1165	Not present in versions with 64 or 48 pins.
0008 A04Bh	SCI2	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		1166	Not present in versions with 64 or 48 pins.
0008 A04Ch	SCI2	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		1168	Not present in versions with 64 or 48 pins.
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		1169	Not present in versions with 64 or 48 pins.
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK		1141	Not present in versions with 100, 64, or 48 pins.
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		1153	Not present in versions with 100, 64, or 48 pins.
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		1144	Not present in versions with 100, 64, or 48 pins.
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		1140	Not present in versions with 100, 64, or 48 pins.
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		1148	Not present in versions with 100, 64, or 48 pins.
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		1140	Not present in versions with 100, 64, or 48 pins.
0008 A066h	SCI3	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		1152	Not present in versions with 100, 64, or 48 pins.
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		1161	Not present in versions with 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (25/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 A068h	SCI3	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	1163	Not present in versions with 100, 64, or 48 pins.
0008 A069h	SCI3	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		1164	Not present in versions with 100, 64, or 48 pins.
0008 A06Ah	SCI3	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		1165	Not present in versions with 100, 64, or 48 pins.
0008 A06Bh	SCI3	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		1166	Not present in versions with 100, 64, or 48 pins.
0008 A06Ch	SCI3	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		1168	Not present in versions with 100, 64, or 48 pins.
0008 A06Dh	SCI3	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		1169	Not present in versions with 100, 64, or 48 pins.
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK	CAC	252	
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK		253	
0008 B002h	CAC	CAC Control Register 2)	CACR2	8	8	2, 3 PCLKB	2 ICLK		254	
0008 B003h	CAC	CAC Interrupt Control Register	CAICR	8	8	2, 3 PCLKB	2 ICLK		255	
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2, 3 PCLKB	2 ICLK		256	
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2, 3 PCLKB	2 ICLK		257	
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2, 3 PCLKB	2 ICLK		257	
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK		257	
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2, 3 PCLKB	2 ICLK	DOC	1628	
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2, 3 PCLKB	2 ICLK		1629	
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2, 3 PCLKB	2 ICLK		1629	
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	1141	
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		1153	
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		1144	
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		1140	
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		1148	
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		1140	
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		1152	
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		1161	
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		1163	
0008 B309h	SCI12	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		1164	
0008 B30Ah	SCI12	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		1165	
0008 B30Bh	SCI12	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		1166	
0008 B30Ch	SCI12	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		1168	
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		1169	
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2, 3 PCLKB	2 ICLK		1170	
0008 B321h	SCI12	Control Register 0	CR0	8	8	2, 3 PCLKB	2 ICLK		1171	
0008 B322h	SCI12	Control Register 1	CR1	8	8	2, 3 PCLKB	2 ICLK		1171	
0008 B323h	SCI12	Control Register 2	CR2	8	8	2, 3 PCLKB	2 ICLK		1172	
0008 B324h	SCI12	Control Register 3	CR3	8	8	2, 3 PCLKB	2 ICLK		1173	
0008 B325h	SCI12	Port Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK		1173	
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2, 3 PCLKB	2 ICLK		1174	
0008 B327h	SCI12	Status Register	STR	8	8	2, 3 PCLKB	2 ICLK		1175	
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2, 3 PCLKB	2 ICLK		1176	
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2, 3 PCLKB	2 ICLK		1176	
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2, 3 PCLKB	2 ICLK		1177	

Table 6.1 List of I/O Registers (Address Order) (26/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	1177	
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK		1177	
0008 B32Dh	SCI12	Primary Control Field 1 Data Register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK		1177	
0008 B32Eh	SCI12	Secondary Control Field 1 Data Register	CF1CR	8	8	2, 3 PCLKB	2 ICLK		1178	
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2, 3 PCLKB	2 ICLK		1178	
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK		1179	
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2, 3 PCLKB	2 ICLK		1179	
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2, 3 PCLKB	2 ICLK		1180	
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2, 3 PCLKB	2 ICLK		1180	
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	503	Not present in versions with 48 pins.
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	Not present in versions with 48 pins.
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	Not present in versions with 64 or 48 pins.
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	Not present in versions with 48 pins.
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	Not present in versions with 64 or 48 pins.
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	Not present in versions with 100, 64, or 48 pins.
0008 C010h	PORTG	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		503	Not present in versions with 100, 64, or 48 pins.
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	Not present in versions with 48 pins.
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	Not present in versions with 48 pins.
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	Not present in versions with 64 or 48 pins.
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	Not present in versions with 48 pins.
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	Not present in versions with 64 or 48 pins.
0008 C02Fh	PORTF	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		504	Not present in versions with 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (27/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C030h	PORTG	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	504	Not present in versions with 100, 64, or 48 pins.
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 48 pins.
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 48 pins.
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 64 or 48 pins.
0008 C046h	PORT6	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 64 or 48 pins.
0008 C047h	PORT7	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C048h	PORT8	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 64 or 48 pins.
0008 C049h	PORT9	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 48 pins.
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	
0008 C04Fh	PORTF	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 100, 64, or 48 pins.
0008 C050h	PORTG	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		505	Not present in versions with 100, 64, or 48 pins.
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	Not present in versions with 48 pins.
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	Not present in versions with 48 pins.
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	Not present in versions with 64 or 48 pins.
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	Not present in versions with 48 pins.
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	Not present in versions with 100, 64, or 48 pins.
0008 C070h	PORTG	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		506	Not present in versions with 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (28/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	507	Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	Not present in versions with 64 or 48 pins.
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		508	Not present in versions with 112 or 100 pins.
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	Not present in versions with 144, 120, 112, or 100 pins.
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		508	Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	Not present in versions with 64 or 48 pins.
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	Not present in versions with 144, 120, 112, 100 or 48 pins.
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		508	Not present in versions with 48 pins.
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	Not present in versions with 64 or 48 pins.
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		508	Not present in versions with 64 or 48 pins.
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		508	
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		508	
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	Not present in versions with 100, 64, or 48 pins.
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		507	Not present in versions with 100, 64, or 48 pins.
0008 C0A1h	PORTG	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		508	Not present in versions with 100, 64, or 48 pins.
0008 C0F2h	PORT	Driving Ability Control Register 1	DSCR1	8	8	2, 3 PCLKB	2 ICLK		509	Not present in versions with 64 or 48 pins.
0008 C0F3h	PORT	Driving Ability Control Register 2	DSCR2	8	8	2, 3 PCLKB	2 ICLK		510	Not present in versions with 64 or 48 pins.
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC	543	Not present in versions with 64 or 48 pins.
0008 C102h	MPC	CS Output Pin Select Register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK		544	Not present in versions with 64 or 48 pins.
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8	2, 3 PCLKB	2 ICLK		545	Not present in versions with 64 or 48 pins.
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8	2, 3 PCLKB	2 ICLK		545	Not present in versions with 64 or 48 pins.
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8	2, 3 PCLKB	2 ICLK		546	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (29/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8	2, 3 PCLKB	2 ICLK	MPC	546	Not present in versions with 64 or 48 pins.
0008 C114h	MPC	USB0 Control Register	PFUSB0	8	8	2, 3 PCLKB	2 ICLK		547	Not present in versions with 112, 100, 64, or 48 pins.
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2, 3 PCLKB	2 ICLK			
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2, 3 PCLKB	2 ICLK		522	Not present in versions with 48 pins.
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2, 3 PCLKB	2 ICLK		522	Not present in versions with 48 pins.
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2, 3 PCLKB	2 ICLK		522	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2, 3 PCLKB	2 ICLK		522	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2, 3 PCLKB	2 ICLK		524	Not present in versions with 48 pins.
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2, 3 PCLKB	2 ICLK		524	Not present in versions with 48 pins.
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2, 3 PCLKB	2 ICLK		524	Not present in versions with 100, 64, or 48 pins.
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2, 3 PCLKB	2 ICLK		524	Not present in versions with 112, 100, 64, or 48 pins.
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2, 3 PCLKB	2 ICLK		524	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2, 3 PCLKB	2 ICLK		525	Not present in versions with 64 or 48 pins.
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2, 3 PCLKB	2 ICLK		525	Not present in versions with 64 or 48 pins.
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2, 3 PCLKB	2 ICLK		525	
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2, 3 PCLKB	2 ICLK		525	
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2, 3 PCLKB	2 ICLK		525	
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2, 3 PCLKB	2 ICLK		525	Not present in versions with 112, 100, 64, or 48 pins.
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2, 3 PCLKB	2 ICLK		525	Not present in versions with 112, 100, 64, or 48 pins.
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2, 3 PCLKB	2 ICLK		527	
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2, 3 PCLKB	2 ICLK		527	Not present in versions with 48 pins.
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2, 3 PCLKB	2 ICLK		527	Not present in versions with 48 pins.
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2, 3 PCLKB	2 ICLK		527	Not present in versions with 48 pins.
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2, 3 PCLKB	2 ICLK		527	Not present in versions with 120, 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (30/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C15Dh	MPC	P35 Pin Function Control Register	P35PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	527	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2, 3 PCLKB	2 ICLK		529	
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2, 3 PCLKB	2 ICLK		529	
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2, 3 PCLKB	2 ICLK		529	
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2, 3 PCLKB	2 ICLK		529	
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2, 3 PCLKB	2 ICLK		529	
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 48 pins.
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 48 pins.
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2, 3 PCLKB	2 ICLK		529	
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C16Eh	MPC	P56 Pin Function Control Register	P56PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C16Fh	MPC	P57 Pin Function Control Register	P57PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C170h	MPC	P60 Pin Function Control Register	P60PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C171h	MPC	P61 Pin Function Control Register	P61PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C172h	MPC	P62 Pin Function Control Register	P62PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C173h	MPC	P63 Pin Function Control Register	P63PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2, 3 PCLKB	2 ICLK		529	Not present in versions with 64 or 48 pins.
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2, 3 PCLKB	2 ICLK		530	
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2, 3 PCLKB	2 ICLK		530	
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2, 3 PCLKB	2 ICLK		530	
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2, 3 PCLKB	2 ICLK		530	
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2, 3 PCLKB	2 ICLK		530	
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2, 3 PCLKB	2 ICLK		530	
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2, 3 PCLKB	2 ICLK		530	

Table 6.1 List of I/O Registers (Address Order) (31/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	531	Not present in versions with 64 or 48 pins.
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2, 3 PCLKB	2 ICLK		531	Not present in versions with 64 or 48 pins.
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2, 3 PCLKB	2 ICLK		531	Not present in versions with 64 or 48 pins.
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2, 3 PCLKB	2 ICLK		532	Not present in versions with 64 or 48 pins.
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2, 3 PCLKB	2 ICLK		532	Not present in versions with 48 pins.
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2, 3 PCLKB	2 ICLK		532	Not present in versions with 48 pins.
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2, 3 PCLKB	2 ICLK		532	Not present in versions with 48 pins.
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2, 3 PCLKB	2 ICLK		532	Not present in versions with 48 pins.
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2, 3 PCLKB	2 ICLK		532	Not present in versions with 64 or 48 pins.
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2, 3 PCLKB	2 ICLK		532	Not present in versions with 64 or 48 pins.
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK		533	Not present in versions with 64 or 48 pins.
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK		533	Not present in versions with 64 or 48 pins.
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK		533	
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK		533	
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK		533	Not present in versions with 48 pins.
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK		533	Not present in versions with 48 pins.
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK		533	Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK		535	
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK		535	
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK		535	
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK		535	
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK		535	
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK		535	
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK		535	
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK		535	Not present in versions with 48 pins.
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 120, 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (32/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	537	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 64 or 48 pins.
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 64 or 48 pins.
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK		537	Not present in versions with 64 or 48 pins.
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK		537	
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK		537	
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK		537	
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK		537	
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK		537	
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK		539	Not present in versions with 64 or 48 pins.
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK		539	Not present in versions with 64 or 48 pins.
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK		539	
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK		539	Not present in versions with 64 or 48 pins.
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK		539	Not present in versions with 64 or 48 pins.
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK		539	Not present in versions with 64 or 48 pins.
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK		541	Not present in versions with 100, 64, or 48 pins.
0008 C1BBh	MPC	PF3 Pin Function Control Register	PF3PFS	8	8	2, 3 PCLKB	2 ICLK		541	Not present in versions with 100, 64, or 48 pins.
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2, 3 PCLKB	2 ICLK		542	Not present in versions with 100, 64, or 48 pins.
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2, 3 PCLKB	2 ICLK		542	Not present in versions with 100, 64, or 48 pins.
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2, 3 PCLKB	2 ICLK		542	Not present in versions with 100, 64, or 48 pins.
0008 C1C3h	MPC	PG3 Pin Function Control Register	PG3PFS	8	8	2, 3 PCLKB	2 ICLK		542	Not present in versions with 100, 64, or 48 pins.
0008 C1C4h	MPC	PG4 Pin Function Control Register	PG4PFS	8	8	2, 3 PCLKB	2 ICLK		542	Not present in versions with 100, 64, or 48 pins.
0008 C1C5h	MPC	PG5 Pin Function Control Register	PG5PFS	8	8	2, 3 PCLKB	2 ICLK		542	Not present in versions with 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (33/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C1C6h	MPC	PG6 Pin Function Control Register	PG6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	542	Not present in versions with 112, 100, 64, or 48 pins.
0008 C1D0h	MPC	USB0_DPUPE Pin Function Control Register	UDPUPEPFS	8	8	2, 3 PCLKB	2 ICLK		543	Not present in versions with 112, 100, 64, or 48 pins.
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	272	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK		273	
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK		274	
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK		275	
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK		276	
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK		277	
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	278	
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets	193	
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK		195	
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit	243	
0008 C296h	FLASH	Flash P/E Protection Register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM	1661	
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA	216	
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK		217	
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK		218	
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK		220	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	278	
0008 C300h	ICU	Group 0 Interrupt Source Register	GRP00	32	32	1, 2 PCLKB	2 ICLK	ICUb	318	Not present in versions with 64 or 48 pins.
0008 C330h	ICU	Group 12 Interrupt Source Register	GRP12	32	32	1, 2 PCLKB	2 ICLK		318	
0008 C340h	ICU	Group 0 Interrupt Enable Register	GEN00	32	32	1, 2 PCLKB	2 ICLK		320	Not present in versions with 64 or 48 pins.
0008 C370h	ICU	Group 12 Interrupt Enable Register	GEN12	32	32	1, 2 PCLKB	2 ICLK		320	
0008 C380h	ICU	Group 0 Interrupt Clear Register	GCR00	32	32	1, 2 PCLKB	2 ICLK		322	Not present in versions with 64 or 48 pins.
0008 C4C0h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK	POE3	787	
0008 C4C2h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK		790	
0008 C4C4h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK		789	Not present in versions with 64 or 48 pins.
0008 C4C6h	POE	Output Level Control/Status Register 2	OCSR2	16	8, 16	2, 3 PCLKB	2 ICLK		791	Not present in versions with 64 or 48 pins.
0008 C4C8h	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK		796	
0008 C4CAh	POE	Software Port Output Enable Register	SPOER	8	8	2, 3 PCLKB	2 ICLK		801	
0008 C4CBh	POE	Port Output Enable Control Register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK		804	
0008 C4CCh	POE	Port Output Enable Control Register 2	POECR2	16	16	2, 3 PCLKB	2 ICLK		805	
0008 C4CEh	POE	Port Output Enable Control Register 3	POECR3	16	16	2, 3 PCLKB	2 ICLK		807	
0008 C4D0h	POE	Port Output Enable Control Register 4	POECR4	16	16	2, 3 PCLKB	2 ICLK		809	
0008 C4D2h	POE	Port Output Enable Control Register 5	POECR5	16	16	2, 3 PCLKB	2 ICLK		812	
0008 C4D4h	POE	Port Output Enable Control Register 6	POECR6	16	16	2, 3 PCLKB	2 ICLK		814	
0008 C4D6h	POE	Input Level Control/Status Register 4	ICSR4	16	8, 16	2, 3 PCLKB	2 ICLK		798	
0008 C4D8h	POE	Input Level Control/Status Register 5	ICSR5	16	8, 16	2, 3 PCLKB	2 ICLK		799	
0008 C4DAh	POE	Active Level Setting Register 1	ALR1	16	8, 16	2, 3 PCLKB	2 ICLK		792	
0008 C4DCh	POE	Input Level Control/Status Register 6	ICSR6	16	16	2, 3 PCLKB	2 ICLK		820	

Table 6.1 List of I/O Registers (Address Order) (34/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0008 C4DEh	POE	Active Level Setting Register 2	ALR2	16	8, 16	2, 3 PCLKB	2 ICLK	POE3	794	Not present in versions with 64 or 48 pins.
0008 C4E0h	POE	Input Level Control/Status Register 7	ICSR7	16	8, 16	2, 3 PCLKB	2 ICLK		817	Not present in versions with 64 or 48 pins.
0008 C4E2h	POE	Port Output Enable Control Register 7	POECR7	16	16	2, 3 PCLKB	2 ICLK		818	Not present in versions with 64 or 48 pins.
0008 C4E4h	POE	Port Output Enable Control Register 8	POECR8	16	16	2, 3 PCLKB	2 ICLK		817	Not present in versions with 64 or 48 pins.
0009 1200h to 0009 13FFh	CAN1	Mailbox Register 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN	1334	Not present in versions with 64 or 48 pins.
0009 1400h to 0009 141Ch	CAN1	Mask Register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK		1331	Not present in versions with 64 or 48 pins.
0009 1420h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK		1332	Not present in versions with 64 or 48 pins.
0009 1424h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK		1332	Not present in versions with 64 or 48 pins.
0009 1428h	CAN1	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		1333	Not present in versions with 64 or 48 pins.
0009 142Ch	CAN1	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK		1338	Not present in versions with 64 or 48 pins.
0009 1820h to 0009 183Fh	CAN1	Message Control Register 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK		1339	Not present in versions with 64 or 48 pins.
0009 1840h	CAN1	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK		1325	Not present in versions with 64 or 48 pins.
0009 1842h	CAN1	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK		1348	Not present in versions with 64 or 48 pins.
0009 1844h	CAN1	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		1329	Not present in versions with 64 or 48 pins.
0009 1848h	CAN1	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK		1342	Not present in versions with 64 or 48 pins.
0009 1849h	CAN1	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK		1345	Not present in versions with 64 or 48 pins.
0009 184Ah	CAN1	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK		1345	Not present in versions with 64 or 48 pins.
0009 184Bh	CAN1	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK		1347	Not present in versions with 64 or 48 pins.
0009 184Ch	CAN1	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK		1354	Not present in versions with 64 or 48 pins.
0009 184Dh	CAN1	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK		1355	Not present in versions with 64 or 48 pins.
0009 184Eh	CAN1	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK		1357	Not present in versions with 64 or 48 pins.
0009 184Fh	CAN1	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK		1358	Not present in versions with 64 or 48 pins.
0009 1850h	CAN1	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK		1358	Not present in versions with 64 or 48 pins.
0009 1851h	CAN1	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK		1352	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (35/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN	1351	Not present in versions with 64 or 48 pins.
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK		1350	Not present in versions with 64 or 48 pins.
0009 1854h	CAN1	Time Stamp Register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK		1360	Not present in versions with 64 or 48 pins.
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK		1353	Not present in versions with 64 or 48 pins.
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK		1360	Not present in versions with 64 or 48 pins.
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2, 3 ICLK	USBa	1031	Not present in versions with 112, 100, 64, or 48 pins.
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more			1033	Not present in versions with 112, 100, 64, or 48 pins.
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more			1034	Not present in versions with 112, 100, 64, or 48 pins.
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		1037	Not present in versions with 112, 100, 64, or 48 pins.
000A 0018h	USB0	D0FIFO Port Registe	D0FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		1037	Not present in versions with 112, 100, 64, or 48 pins.
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		1037	Not present in versions with 112, 100, 64, or 48 pins.
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		1039	Not present in versions with 112, 100, 64, or 48 pins.
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		1039	Not present in versions with 112, 100, 64, or 48 pins.
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		1039	Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		1043	Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		1039	Not present in versions with 112, 100, 64, or 48 pins.
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		1043	Not present in versions with 112, 100, 64, or 48 pins.
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1045	Not present in versions with 112, 100, 64, or 48 pins.
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1046	Not present in versions with 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (36/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1	USBa	1047	Not present in versions with 112, 100, 64, or 48 pins.
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1048	Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1049	Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1050	Not present in versions with 112, 100, 64, or 48 pins.
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1051	Not present in versions with 112, 100, 64, or 48 pins.
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1054	Not present in versions with 112, 100, 64, or 48 pins.
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1057	Not present in versions with 112, 100, 64, or 48 pins.
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1058	Not present in versions with 112, 100, 64, or 48 pins.
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1059	Not present in versions with 112, 100, 64, or 48 pins.
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1060	Not present in versions with 112, 100, 64, or 48 pins.
000A 004Eh	USB0	Device State Change Register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1061	Not present in versions with 112, 100, 64, or 48 pins.
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1062	Not present in versions with 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (37/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1	USBa	1063	Not present in versions with 112, 100, 64, or 48 pins.
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1064	Not present in versions with 112, 100, 64, or 48 pins.
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1065	Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1066	Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1067	Not present in versions with 112, 100, 64, or 48 pins.
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1068	Not present in versions with 112, 100, 64, or 48 pins.
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1069	Not present in versions with 112, 100, 64, or 48 pins.
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1073	Not present in versions with 112, 100, 64, or 48 pins.
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1074	Not present in versions with 112, 100, 64, or 48 pins.
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1076	Not present in versions with 112, 100, 64, or 48 pins.
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1077	Not present in versions with 112, 100, 64, or 48 pins.
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (38/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1	USBa	1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1078	Not present in versions with 112, 100, 64, or 48 pins.
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1086	Not present in versions with 112, 100, 64, or 48 pins.
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1087	Not present in versions with 112, 100, 64, or 48 pins.
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1086	Not present in versions with 112, 100, 64, or 48 pins.
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1087	Not present in versions with 112, 100, 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (39/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1	USBa	1086	Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1087	Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1086	Not present in versions with 112, 100, 64, or 48 pins.
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1087	Not present in versions with 112, 100, 64, or 48 pins.
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1086	Not present in versions with 112, 100, 64, or 48 pins.
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*1		1087	Not present in versions with 112, 100, 64, or 48 pins.
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	559	
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		559	
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		563	
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		563	
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		566	
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		566	
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		585	
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		585	
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	2, 3 ICLK		605	
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	2, 3 ICLK		612	
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK		607	
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4, 5 PCLKA	2, 3 ICLK		607	
000C 1210h	MTU3	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		596	
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		596	
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		613	
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4, 5 PCLKA	2, 3 ICLK		614	
000C 1218h	MTU3	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	4, 5 PCLKA	2, 3 ICLK		614	
000C 1224h	MTU3	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		597	

Table 6.1 List of I/O Registers (Address Order) (40/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 1228h	MTU4	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	597	
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 122Ch	MTU3	Timer Status Register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		589	
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		589	
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK		625	
000C 1231h	MTU	Timer Interrupt Skipping Counters 1A	TITCNT1A	8	8	4, 5 PCLKA	2, 3 ICLK		628	
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4, 5 PCLKA	2, 3 ICLK		615	
000C 1234h	MTU	Timer dead time enable register A	TDERA	8	8	4, 5 PCLKA	2, 3 ICLK		615	
000C 1236h	MTU	Timer output level buffer register A	TOLBRA	8	8	4, 5 PCLKA	2, 3 ICLK		615	
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK		594	
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		594	
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4, 5 PCLKA	2, 3 ICLK		624	
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4, 5 PCLKA	2, 3 ICLK		630	
000C 123Ch	MTU	Timer Interrupt Skipping Counters 2A	TITCNT2A	8	8	4, 5 PCLKA	2, 3 ICLK		632	
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK		619	
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		623	
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK		623	
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		623	
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK		623	
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4, 5 PCLKA	2, 3 ICLK		617	
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4, 5 PCLKA	2, 3 ICLK		565	
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8, 16	4, 5 PCLKA	2, 3 ICLK		598	
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4, 5 PCLKA	2, 3 ICLK		600	
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4, 5 PCLKA	2, 3 ICLK		602	
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4, 5 PCLKA	2, 3 ICLK		604	
000C 1300h	MTU0	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		559	
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		563	
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		566	
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		585	
000C 1305h	MTU0	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		589	
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		596	
000C 1308h	MTU0	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1320h	MTU0	Timer General Register E	TGRE	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4, 5 PCLKA	2, 3 ICLK		585	
000C 1325h	MTU0	Timer Status Register 2	TSR2	8	8	4, 5 PCLKA	2, 3 ICLK		589	
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		594	
000C 1380h	MTU1	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		559	
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		563	
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		566	

Table 6.1 List of I/O Registers (Address Order) (41/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	585	
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		589	
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		596	
000C 1388h	MTU1	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	2, 3 ICLK		595	
000C 1400h	MTU2	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		559	
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		563	
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		585	
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		589	
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		596	
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A00h	MTU6	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		559	
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		559	
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		563	
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		563	
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		566	
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		566	
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		585	
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		585	
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4, 5 PCLKA	2, 3 ICLK		605	
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		607	
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4, 5 PCLKA	2, 3 ICLK		609	
000C 1A10h	MTU6	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		596	
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		596	
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		613	
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRB	16	16	4, 5 PCLKA	2, 3 ICLK		614	
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		613	
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	4, 5 PCLKA	2, 3 ICLK		614	
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		589	
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		589	
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		625	
000C 1A31h	MTU	Timer Interrupt Skipping Counters 1B	TITCNT1B	8	8	4, 5 PCLKA	2, 3 ICLK		628	
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	4, 5 PCLKA	2, 3 ICLK		615	
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	4, 5 PCLKA	2, 3 ICLK		615	
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	4, 5 PCLKA	2, 3 ICLK		611	
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK		594	
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		594	
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	4, 5 PCLKA	2, 3 ICLK		624	

Table 6.1 List of I/O Registers (Address Order) (42/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	4, 5 PCLKA	2, 3 ICLK	MTU3	630	
000C 1A3Ch	MTU	Timer Interrupt Skipping Counters 2B	TITCNT2B	8	8	4, 5 PCLKA	2, 3 ICLK		632	
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK		619	
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		623	
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK		623	
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		623	
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK		623	
000C 1A50h	MTU	Timer Synchronous Clear Register	TSYCR	8	8	4, 5 PCLKA	2, 3 ICLK		596	
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4, 5 PCLKA	2, 3 ICLK		617	
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4, 5 PCLKA	2, 3 ICLK		565	
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4, 5 PCLKA	2, 3 ICLK		598	
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4, 5 PCLKA	2, 3 ICLK		600	
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4, 5 PCLKA	2, 3 ICLK		604	
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4, 5 PCLKA	2, 3 ICLK		596	
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4, 5 PCLKA	2, 3 ICLK		559	
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4, 5 PCLKA	2, 3 ICLK		596	
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4, 5 PCLKA	2, 3 ICLK		559	
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4, 5 PCLKA	2, 3 ICLK		596	
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4, 5 PCLKA	2, 3 ICLK		597	
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4, 5 PCLKA	2, 3 ICLK		559	
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4, 5 PCLKA	2, 3 ICLK		566	
000C 1CB0h	MTU5	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		589	
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		585	
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4, 5 PCLKA	2, 3 ICLK		598	
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4, 5 PCLKA	2, 3 ICLK		584	
000C 2000h	GPT	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	841	
000C 2004h	GPT	General PWM Timer Hardware Source Start Control Register	GTHSCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		843	
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		845	
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		847	
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		851	
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		855	
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		856	
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		858	
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		859	
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		861	
000C 2080h	GPT	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		862	
000C 2082h	GPT	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		864	
000C 2084h	GPT	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK			

Table 6.1 List of I/O Registers (Address Order) (43/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2086h	GPT	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	865	
000C 2088h	GPT	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 208Ah	GPT	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 208Ch	GPT	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 208Eh	GPT	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 2090h	GPT	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 2092h	GPT	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 2094h	GPT	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 2096h	GPT	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 2098h	GPT	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 209Ah	GPT	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 209Ch	GPT	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 209Eh	GPT	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 20A0h	GPT	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 20A2h	GPT	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 20A4h	GPT	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 20A6h	GPT	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	
000C 20A8h	GPT	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		866	
000C 20AAh	GPT	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		866	
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		872	
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	
000C 210Ah	GPT0	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		877	
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 211Ch	GPT0	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 211Eh	GPT0	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2120h	GPT0	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 2124h	GPT0	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 2126h	GPT0	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 2128h	GPT0	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 212Ch	GPT0	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 212Eh	GPT0	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	

Table 6.1 List of I/O Registers (Address Order) (44/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2130h	GPT0	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	885	
000C 2134h	GPT0	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 2136h	GPT0	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	
000C 2138h	GPT0	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 213Ah	GPT0	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 213Ch	GPT0	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 213Eh	GPT0	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 2140h	GPT0	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		891	
000C 2142h	GPT0	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		892	
000C 2180h	GPT1	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	
000C 2182h	GPT1	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	
000C 2184h	GPT1	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		872	
000C 2186h	GPT1	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	
000C 2188h	GPT1	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	
000C 218Ah	GPT1	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		877	
000C 218Ch	GPT1	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	
000C 218Eh	GPT1	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	
000C 2190h	GPT1	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2192h	GPT1	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2194h	GPT1	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2196h	GPT1	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2198h	GPT1	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 219Ah	GPT1	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 219Ch	GPT1	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 219Eh	GPT1	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 21A0h	GPT1	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 21A8h	GPT1	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 21B0h	GPT1	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	

Table 6.1 List of I/O Registers (Address Order) (45/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	890	
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		891	
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		892	
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		872	
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		877	
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		891	

Table 6.1 List of I/O Registers (Address Order) (46/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	892	
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		872	
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		877	
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		891	
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		892	
000C 2318h	GPT0	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		896	Not present in versions with 64, or 48 pins.
000C 231Ah	GPT0	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		896	Not present in versions with 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (47/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 231Ch	GPT1	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	896	Not present in versions with 64, or 48 pins.
000C 231Eh	GPT1	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		896	Not present in versions with 64, or 48 pins.
000C 2320h	GPT2	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		896	Not present in versions with 64, or 48 pins.
000C 2322h	GPT2	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		896	Not present in versions with 64, or 48 pins.
000C 2324h	GPT3	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		896	Not present in versions with 64, or 48 pins.
000C 2326h	GPT3	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		896	Not present in versions with 64, or 48 pins.
000C 2328h	GPT0	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 232Ah	GPT0	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 232Ch	GPT1	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 232Eh	GPT1	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 2330h	GPT2	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 2332h	GPT2	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 2334h	GPT3	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 2336h	GPT3	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		897	Not present in versions with 64, or 48 pins.
000C 2800h	GPTB	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		841	Not present in versions with 64, or 48 pins.
000C 2804h	GPTB	General PWM Timer Hardware Source Start Control Register	GTHSCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		843	Not present in versions with 64, or 48 pins.
000C 2806h	GPTB	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		845	Not present in versions with 64, or 48 pins.
000C 2808h	GPTB	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		847	Not present in versions with 64, or 48 pins.
000C 280Ah	GPTB	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		851	Not present in versions with 64, or 48 pins.
000C 280Ch	GPTB	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		855	Not present in versions with 64, or 48 pins.
000C 280Eh	GPTB	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		856	Not present in versions with 64, or 48 pins.
000C 2810h	GPTB	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		858	Not present in versions with 64, or 48 pins.
000C 2814h	GPTB	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		859	Not present in versions with 64, or 48 pins.
000C 2818h	GPTB	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		861	Not present in versions with 64, or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (48/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2880h	GPTB	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	862	Not present in versions with 64, or 48 pins.
000C 2882h	GPTB	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		864	Not present in versions with 64, or 48 pins.
000C 2884h	GPTB	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64, or 48 pins.
000C 2886h	GPTB	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64, or 48 pins.
000C 2888h	GPTB	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64, or 48 pins.
000C 288Ah	GPTB	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64, or 48 pins.
000C 288Ch	GPTB	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 288Eh	GPTB	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 2890h	GPTB	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 2892h	GPTB	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 2894h	GPTB	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 2896h	GPTB	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 2898h	GPTB	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 289Ah	GPTB	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 289Ch	GPTB	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 289Eh	GPTB	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 28A0h	GPTB	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 28A2h	GPTB	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 28A4h	GPTB	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 28A6h	GPTB	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		865	Not present in versions with 64 or 48 pins.
000C 28A8h	GPTB	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		866	Not present in versions with 64 or 48 pins.
000C 28AAh	GPTB	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		866	Not present in versions with 64 or 48 pins.
000C 2900h	GPT4	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	Not present in versions with 64 or 48 pins.
000C 2902h	GPT4	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (49/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2904h	GPT4	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	872	Not present in versions with 64 or 48 pins.
000C 2906h	GPT4	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	Not present in versions with 64 or 48 pins.
000C 2908h	GPT4	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	Not present in versions with 64 or 48 pins.
000C 290Ah	GPT4	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		877	Not present in versions with 64 or 48 pins.
000C 290Ch	GPT4	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	Not present in versions with 64 or 48 pins.
000C 290Eh	GPT4	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	Not present in versions with 64 or 48 pins.
000C 2910h	GPT4	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2912h	GPT4	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2914h	GPT4	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2916h	GPT4	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2918h	GPT4	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 291Ah	GPT4	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 291Ch	GPT4	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 291Eh	GPT4	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2920h	GPT4	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2924h	GPT4	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2926h	GPT4	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2928h	GPT4	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 292Ch	GPT4	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 292Eh	GPT4	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2930h	GPT4	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2934h	GPT4	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2936h	GPT4	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	Not present in versions with 64 or 48 pins.
000C 2938h	GPT4	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (50/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 293Ah	GPT4	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	890	Not present in versions with 64 or 48 pins.
000C 293Ch	GPT4	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 293Eh	GPT4	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2940h	GPT4	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		891	Not present in versions with 64 or 48 pins.
000C 2942h	GPT4	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		892	Not present in versions with 64 or 48 pins.
000C 2980h	GPT5	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	Not present in versions with 64 or 48 pins.
000C 2982h	GPT5	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	Not present in versions with 64 or 48 pins.
000C 2984h	GPT5	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		872	Not present in versions with 64 or 48 pins.
000C 2986h	GPT5	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	Not present in versions with 64 or 48 pins.
000C 2988h	GPT5	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	Not present in versions with 64 or 48 pins.
000C 298Ah	GPT5	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		877	Not present in versions with 64 or 48 pins.
000C 298Ch	GPT5	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	Not present in versions with 64 or 48 pins.
000C 298Eh	GPT5	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	Not present in versions with 64 or 48 pins.
000C 2990h	GPT5	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2992h	GPT5	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2994h	GPT5	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2996h	GPT5	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2998h	GPT5	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 299Ah	GPT5	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 299Ch	GPT5	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 299Eh	GPT5	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 29A0h	GPT5	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 29A4h	GPT5	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 29A6h	GPT5	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (51/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 29A8h	GPT5	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	885	Not present in versions with 64 or 48 pins.
000C 29ACh	GPT5	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 29AEh	GPT5	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 29B0h	GPT5	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 29B4h	GPT5	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 29B6h	GPT5	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	Not present in versions with 64 or 48 pins.
000C 29B8h	GPT5	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 29BAh	GPT5	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 29BCh	GPT5	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 29BEh	GPT5	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 29C0h	GPT5	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		891	Not present in versions with 64 or 48 pins.
000C 29C2h	GPT5	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		892	Not present in versions with 64 or 48 pins.
000C 2A00h	GPT6	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	Not present in versions with 64 or 48 pins.
000C 2A02h	GPT6	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	Not present in versions with 64 or 48 pins.
000C 2A04h	GPT6	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		872	Not present in versions with 64 or 48 pins.
000C 2A06h	GPT6	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	Not present in versions with 64 or 48 pins.
000C 2A08h	GPT6	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	Not present in versions with 64 or 48 pins.
000C 2A0Ah	GPT6	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		877	Not present in versions with 64 or 48 pins.
000C 2A0Ch	GPT6	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	Not present in versions with 64 or 48 pins.
000C 2A0Eh	GPT6	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	Not present in versions with 64 or 48 pins.
000C 2A10h	GPT6	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A12h	GPT6	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A14h	GPT6	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A16h	GPT6	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (52/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2A18h	GPT6	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	883	Not present in versions with 64 or 48 pins.
000C 2A1Ah	GPT6	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A1Ch	GPT6	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A1Eh	GPT6	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A20h	GPT6	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2A24h	GPT6	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2A26h	GPT6	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2A28h	GPT6	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2A2Ch	GPT6	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2A2Eh	GPT6	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2A30h	GPT6	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2A34h	GPT6	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2A36h	GPT6	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	Not present in versions with 64 or 48 pins.
000C 2A38h	GPT6	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2A3Ah	GPT6	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2A3Ch	GPT6	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2A3Eh	GPT6	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2A40h	GPT6	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		891	Not present in versions with 64 or 48 pins.
000C 2A42h	GPT6	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		892	Not present in versions with 64 or 48 pins.
000C 2A80h	GPT7	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		867	Not present in versions with 64 or 48 pins.
000C 2A82h	GPT7	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		870	Not present in versions with 64 or 48 pins.
000C 2A84h	GPT7	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		872	Not present in versions with 64 or 48 pins.
000C 2A86h	GPT7	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		874	Not present in versions with 64 or 48 pins.
000C 2A88h	GPT7	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		876	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (53/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2A8Ah	GPT7	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	877	Not present in versions with 64 or 48 pins.
000C 2A8Ch	GPT7	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		879	Not present in versions with 64 or 48 pins.
000C 2A8Eh	GPT7	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		882	Not present in versions with 64 or 48 pins.
000C 2A90h	GPT7	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A92h	GPT7	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A94h	GPT7	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A96h	GPT7	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A98h	GPT7	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A9Ah	GPT7	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A9Ch	GPT7	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2A9Eh	GPT7	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		883	Not present in versions with 64 or 48 pins.
000C 2AA0h	GPT7	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2AA4h	GPT7	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2AA6h	GPT7	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2AA8h	GPT7	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2AACh	GPT7	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2AAEh	GPT7	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		884	Not present in versions with 64 or 48 pins.
000C 2AB0h	GPT7	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2AB4h	GPT7	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		885	Not present in versions with 64 or 48 pins.
000C 2AB6h	GPT7	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		889	Not present in versions with 64 or 48 pins.
000C 2AB8h	GPT7	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2ABAh	GPT7	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2ABCh	GPT7	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.
000C 2ABEh	GPT7	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		890	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (54/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C 2AC0h	GPT7	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	891	Not present in versions with 64 or 48 pins.
000C 2AC2h	GPT7	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		892	Not present in versions with 64 or 48 pins.
000C3002h	DPC	Software Start Setting Register 0	SOFTSTART0	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	1635	Not present in versions with 64 or 48 pins.
000C3006h	DPC	Software Start Setting Register 1	SOFTSTART1	16	16	3 to 5 PCLKA	2, 3 ICLK		1635	Not present in versions with 64 or 48 pins.
000C300Ah	DPC	Software Start Setting Register 2	SOFTSTART2	16	16	3 to 5 PCLKA	2, 3 ICLK		1635	Not present in versions with 64 or 48 pins.
000C300Eh	DPC	Software Start Setting Register 3	SOFTSTART3	16	16	3 to 5 PCLKA	2, 3 ICLK		1635	Not present in versions with 64 or 48 pins.
000C3012h	DPC	Reference Value Setting Register 0	VOTARGET0	16	16	3 to 5 PCLKA	2, 3 ICLK		1636	Not present in versions with 64 or 48 pins.
000C3016h	DPC	Reference Value Setting Register 1	VOTARGET1	16	16	3 to 5 PCLKA	2, 3 ICLK		1636	Not present in versions with 64 or 48 pins.
000C301Ah	DPC	Reference Value Setting Register 2	VOTARGET2	16	16	3 to 5 PCLKA	2, 3 ICLK		1636	Not present in versions with 64 or 48 pins.
000C301Eh	DPC	Reference Value Setting Register 3	VOTARGET3	16	16	3 to 5 PCLKA	2, 3 ICLK		1636	Not present in versions with 64 or 48 pins.
000C3022h	DPC	Reference Value Select Register	REFSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		1636	Not present in versions with 64 or 48 pins.
000C3026h	DPC	PWM Channel Setting Register	CHLSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		1637	Not present in versions with 64 or 48 pins.
000C302Ah	DPC	Control Enable Setting Register	ENABLE	16	16	3 to 5 PCLKA	2, 3 ICLK		1637	Not present in versions with 64 or 48 pins.
000C302Eh	DPC	Control Calculation Parameter Setting Register KP0	PARAMKP0	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3032h	DPC	Control Calculation Parameter Setting Register KI0	PARAMKI0	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3036h	DPC	Control Calculation Parameter Setting Register KQ0	PARAMKQ0	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C303Ah	DPC	Control Calculation Parameter Setting Register KF0	PARAMKF0	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C303Eh	DPC	Control Calculation Parameter Setting Register KP1	PARAMKP1	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3042h	DPC	Control Calculation Parameter Setting Register KI1	PARAMKI1	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3046h	DPC	Control Calculation Parameter Setting Register KQ1	PARAMKQ1	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C304Ah	DPC	Control Calculation Parameter Setting Register KF1	PARAMKF1	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C304Eh	DPC	Control Calculation Parameter Setting Register KP2	PARAMKP2	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3052h	DPC	Control Calculation Parameter Setting Register KI2	PARAMKI2	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3056h	DPC	Control Calculation Parameter Setting Register KQ2	PARAMKQ2	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (55/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C305Ah	DPC	Control Calculation Parameter Setting Register KF2	PARAMKF2	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	1638	Not present in versions with 64 or 48 pins.
000C305Eh	DPC	Control Calculation Parameter Setting Register KP3	PARAMKP3	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3062h	DPC	Control Calculation Parameter Setting Register KI3	PARAMKI3	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3066h	DPC	Control Calculation Parameter Setting Register KQ3	PARAMKQ3	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C306Ah	DPC	Control Calculation Parameter Setting Register KF3	PARAMKF3	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C306Ch	DPC	Control Calculation Result Higher-Order Bits Store Register 0	RESULTU0	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C306Eh	DPC	Control Calculation Result Lower-Order Bits Store Register 0	RESULTL0	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3070h	DPC	Control Calculation Result Higher-Order Bits Store Register 1	RESULTU1	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3072h	DPC	Control Calculation Result Lower-Order Bits Store Register 1	RESULTL1	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3074h	DPC	Control Calculation Result Higher-Order Bits Store Register 2	RESULTU2	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3076h	DPC	Control Calculation Result Lower-Order Bits Store Register 2	RESULTL2	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C3078h	DPC	Control Calculation Result Higher-Order Bits Store Register 3	RESULTU3	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C307Ah	DPC	Control Calculation Result Lower-Order Bits Store Register 3	RESULTL3	16	16	3 to 5 PCLKA	2, 3 ICLK		1638	Not present in versions with 64 or 48 pins.
000C307Eh	DPC	Input Code Monitor Enable Register	TMONEN	16	16	3 to 5 PCLKA	2, 3 ICLK		1639	Not present in versions with 64 or 48 pins.
000C3082h	DPC	Maximum Input Code Monitor Register 0	TMONMAX0	16	16	3 to 5 PCLKA	2, 3 ICLK		1639	Not present in versions with 64 or 48 pins.
000C3086h	DPC	Minimum Input Code Monitor Register 0	TMONMIN0	16	16	3 to 5 PCLKA	2, 3 ICLK		1640	Not present in versions with 64 or 48 pins.
000C308Ah	DPC	Maximum Input Code Monitor Register 1	TMONMAX1	16	16	3 to 5 PCLKA	2, 3 ICLK		1639	Not present in versions with 64 or 48 pins.
000C308Eh	DPC	Minimum Input Code Monitor Register 1	TMONMIN1	16	16	3 to 5 PCLKA	2, 3 ICLK		1640	Not present in versions with 64 or 48 pins.
000C3092h	DPC	Maximum Input Code Monitor Register 2	TMONMAX2	16	16	3 to 5 PCLKA	2, 3 ICLK		1639	Not present in versions with 64 or 48 pins.
000C3096h	DPC	Minimum Input Code Monitor Register 2	TMONMIN2	16	16	3 to 5 PCLKA	2, 3 ICLK		1640	Not present in versions with 64 or 48 pins.
000C309Ah	DPC	Maximum Input Code Monitor Register 3	TMONMAX3	16	16	3 to 5 PCLKA	2, 3 ICLK		1639	Not present in versions with 64 or 48 pins.
000C309Eh	DPC	Minimum Input Code Monitor Register 3	TMONMIN3	16	16	3 to 5 PCLKA	2, 3 ICLK		1640	Not present in versions with 64 or 48 pins.
000C30A2h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 0	ERRVTH0	16	16	3 to 5 PCLKA	2, 3 ICLK		1640	Not present in versions with 64 or 48 pins.
000C30A6h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 1	ERRVTH1	16	16	3 to 5 PCLKA	2, 3 ICLK		1640	Not present in versions with 64 or 48 pins.

Table 6.1 List of I/O Registers (Address Order) (56/56)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Reference Page	Remarks
						ICLK ≥ PCLK	ICLK < PCLK			
000C30AAh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 2	ERRVTH2	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	1640	Not present in versions with 64 or 48 pins.
000C30AEh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 3	ERRVTH3	16	16	3 to 5 PCLKA	2, 3 ICLK		1640	Not present in versions with 64 or 48 pins.
000C30B2h	DPC	PWM Shut-Down at Overvoltage Output Error Setting Register	ERRDWN	16	16	3 to 5 PCLKA	2, 3 ICLK		1641	Not present in versions with 64 or 48 pins.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	1662	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK		1663	
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK		1666	
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	ROM	1667	
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	1668	
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK		1669	
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK		1670	
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK		1671	
007F FFB0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2, 3 FCLK	2, 3 ICLK	ROM	1672	
007F FFB1h	FLASH	Flash Status Register 1	FSTATR1	8	8	2, 3 FCLK	2, 3 ICLK		1674	
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	1675	
007F FFB4h	FLASH	Flash Protection Register	FPROTR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	1677	
007F FFB6h	FLASH	Flash Reset Register	FRESETR	16	16	2, 3 FCLK	2, 3 ICLK		1678	
007F FFBAh	FLASH	FCU Command Register	FCMDR	16	16	2, 3 FCLK	2, 3 ICLK		1679	
007F FFC8h	FLASH	FCU Processing Switching Register	FCPSR	16	16	2, 3 FCLK	2, 3 ICLK		1680	
007F FFCAh	FLASH	E2 DataFlash Blank Check Control Register	DFLBCCNT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	1680	
007F FFCCh	FLASH	Flash P/E Status Register	FPESTAT	16	16	2, 3 FCLK	2, 3 ICLK	ROM	1681	
007F FFCEh	FLASH	E2 DataFlash Blank Check Status Register	DFLBCSTAT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	1681	
007F FFE8h	FLASH	Peripheral Clock Notification Register	PCKAR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	1682	

Note: • This table shows the maximum specifications of I/O registers. The I/O registers of individual products correspond to the list of functions given as Table 1.2. For details, refer to Table 1.2, Comparison of Functions for Different Packages.
Note 1. When the register is accessed while the USB is operating, a delay may be generated in accessing.
Note 2. Odd addresses are not accessible in 16-bit units. Obtain 16-bit access to the two registers by access to the address of TMOCNTL.
Note 3. Pins USB0 and RIIC1 are not present in 112-pin products.
Note 4. Pins USB0, RIIC1, and SCI3 are not present in 100-pin products.
Note 5. Pins GPT4 to GPT7, USB0, RSPI1, RIIC1, SCI2, SCI3, CAN1, AD, and S12AD1 are not present in 64- and 48-pin products.

7. Resets

7.1 Overview

The nine types of reset are as follows: RES# pin reset, power-on reset, voltage-monitoring 0 reset, voltage-monitoring 1 reset, voltage-monitoring 2 reset, deep software standby reset, independent watchdog timer reset, watchdog timer reset, and software reset.

Table 7.1 lists the reset names and sources.

Table 7.1 Reset Names and Sources

Reset Name	Source
RES# pin reset	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage detection: VPOR)*1
Voltage-monitoring 0 reset	VCC falls (voltage detection: Vdet0)*1
Voltage-monitoring 1 reset	VCC falls (voltage detection: Vdet1)*1
Voltage-monitoring 2 reset	VCC falls (voltage detection: Vdet2)*1
Deep software standby reset	Deep software standby mode is canceled by an interrupt.
Independent watchdog timer reset	The independent watchdog timer underflows, or a refresh error occurs.
Watchdog timer reset	The watchdog timer underflows, or a refresh error occurs.
Software reset	Register setting

Note 1. For details on details on the voltages to be monitored (VPOR, Vdet0, Vdet1, and Vdet2), see section 9, Voltage Detection Circuit (LVDA), section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] and section 43, Electrical Characteristics [64- and 48-Pin Versions].

The internal state and pins are initialized by a reset.

Table 7.2 lists the reset targets to be initialized.

Table 7.2 Targets to be Initialized by Each Reset Source

Targets to be Initialized	Reset Source								
	RES# Pin Reset	Power-On Reset	Voltage-Monitoring 0 Reset	Independent Watchdog Timer Reset	Watchdog Timer Reset	Voltage-Monitoring 1 Reset	Voltage-Monitoring 2 Reset	Deep Software Standby Reset	Software Reset
Power-on reset detect flag (RSTSR0.PORF)	○	—	—	—	—	—	—	—	—
Cold start/warm start determination flag (RSTSR1.CWSF)	—	○	—	—	—	—	—	—	—
Voltage-monitoring 0 reset detect flag (RSTSR0.LVD0RF)	○	○	—	—	—	—	—	—	—
Independent watchdog timer reset detect flag (RSTSR2.IWDTRF)	○	○	○	—	—	—	—	○	—
Registers related to the independent watchdog timer (IWDTRR, IWDTCR, IWDTSR, IWDTRCR, IWDTCSTPR, ILOCOCR)	○	○	○	—	—	—	—	○	—
Watchdog timer reset detect flag (RSTSR2.WDTRF)	○	○	○	○	—	—	—	○	—
Registers related to the watchdog timer (WDTRR, WDTCR, WDTSR, WDTRCR)	○	○	○	○	—	—	—	○	—
Voltage-monitoring 1 reset detect flag (RSTSR0.LVD1RF)	○	○	○	○	○	—	—	—	—
Registers related to the voltage monitor function 1 (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL)	○	○	○	○	○	—	—	—	—
(LVD1CR1, LVD1SR)	○	○	○	○	○	—	—	○	—
Voltage-monitoring 2 reset detect flag (RSTSR0.LVD2RF)	○	○	○	○	○	○	—	—	—
Registers related to the voltage monitor function 2 RSTSR0.LVD2RF, LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	○	○	○	○	○	○	—	—	—
(LVD2CR1, LVD2SR)	○	○	○	○	○	○	—	○	—
Deep software standby reset detect flag (RSTSR0.DPSRSTF)	○	○	○	○	○	○	○	—	—
Software reset detect flag (RSTSR2.SWRF)	○	○	○	○	○	○	○	○	—
Register related to main clock oscillator (MOFCR)	○	○	○	○	○	○	○	—	○
Pin state	○	○	○	○	○	○	○	—	○
Registers related to the low power-consumption function (DPSBYCR, DPSIER0, 2, DPSIFR0, 2, DPSIEGR0, 2)	○	○	○	○	○	○	○	—	○
Registers other than the above, CPU, and internal state	○	○	○	○	○	○	○	○	○

○: Targets to be initialized, —: No change occurs.

When a reset is canceled, the reset exception handling starts. For details on the reset exception handling, see section 14, Exception Handling.
Table 7.3 lists the pin related to the reset.

Table 7.3 Pin Related to Reset

Pin Name	I/O	Function
RES#	Input	Reset pin

7.2 Register Descriptions

7.2.1 Reset Status Register 0 (RSTSR0)

Address(es): 0008 C290h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	0*1	0	0	0	0*1	0*1	0*1	0*1

Bit	Symbol	Bit Name	Description	R/W
b0	PORF	Power-On Reset Detect Flag	0: Power-on reset not detected. 1: Power-on reset detected.	R(/W) *2
b1	LVD0RF	Voltage-Monitoring 0 Reset Detect Flag	0: Voltage-monitoring 0 reset not detected. 1: Voltage-monitoring 0 reset detected.	R(/W) *2
b2	LVD1RF	Voltage-Monitoring 1 Reset Detect Flag	0: Voltage-monitoring 1 reset not detected. 1: Voltage-monitoring 1 reset detected.	R(/W) *2
b3	LVD2RF	Voltage-Monitoring 2 Reset Detect Flag	0: Voltage-monitoring 2 reset not detected. 1: Voltage-monitoring 2 reset detected.	R(/W) *2
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSRSTF	Deep Software Standby Reset Flag	0: Deep software standby mode cancelation not requested by an interrupt. 1: Deep software standby mode cancelation requested by an interrupt.	R(/W) *2

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag.

PORF Flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset has occurred.
[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When PORF is read as 1 and then 0 is written to PORF.

LVD0RF Flag (Voltage-Monitoring 0 Reset Detect Flag)

The LVD0RF flag indicates that VCC voltage has fallen below Vdet0.
[Setting condition]

- When Vdet0-level VCC voltage is detected.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When LVD0RF is read as 1 and then 0 is written to LVD0RF.

LVD1RF Flag (Voltage-Monitoring 1 Reset Detect Flag)

The LVD1RF flag indicates that VCC voltage has fallen below Vdet1.
[Setting condition]

- When Vdet1-level VCC voltage is detected.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When LVD1RF is read as 1 and then 0 is written to LVD1RF.

LVD2RF Flag (Voltage-Monitoring 2 Reset Detect Flag)

The LVD2RF flag indicates that VCC voltage has fallen below Vdet2.
[Setting condition]

- When Vdet2-level VCC voltage is detected.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When LVD2RF is read as 1 and then 0 is written to LVD2RF.

DPSRSTF Flag (Deep Software Standby Reset Flag)

The DPSRSTF flag indicates that deep software standby mode has been canceled by an interrupt and that an internal reset (deep software standby reset) occurred.
[Setting condition]

- When deep software standby mode is canceled by an interrupt.
  For details, see section 12, Low Power Consumption.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When DPSRSTF is read as 1 and then 0 is written to DPSRSTF.

7.2.2 Reset Status Register 1 (RSTSR1)

Address(es): 0008 C291h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit Name	Description	R/W
b0	CWSF	Cold/Warm Start Determination Flag	0: Cold start 1: Warm start	R(/W) *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR1 determines whether a power-on reset has caused the reset processing (cold start) or a reset signal input during operation has caused the reset processing (warm start).

CWSF Flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing: cold start or warm start.
The CWSF flag is initialized by a power-on reset. It is not initialized by a RES# pin reset.
[Setting condition]

- When 1 is written through programming; it is not set to 0 even when 0 is written.

[Clearing condition]

- When a reset listed in Table 7.2 occurs.

7.2.3 Reset Status Register 2 (RSTSR2)

Address(es): 0008 00C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	0	0	0	0	0	0*1	0*1	0*1

Bit	Symbol	Bit Name	Description	R/W
b0	IWDTRF	Independent Watchdog Timer Reset Detect Flag	0: Independent watchdog timer reset not detected. 1: Independent watchdog timer reset detected.	R(/W) *2
b1	WDTRF	Watchdog Timer Reset Detect Flag	0: Watchdog timer reset not detected. 1: Watchdog timer reset detected.	R(/W) *2
b2	SWRF	Software Reset Detect Flag	0: Software reset not detected. 1: Software reset detected.	R(/W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag.

IWDTRF Flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset has occurred.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When IWDTRF is read as 1 and then 0 is written to IWDTRF.

WDTRF Flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset has occurred.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When WDTRF is read as 1 and then 0 is written to WDTRF.

SWRF Flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset has occurred.

[Setting condition]

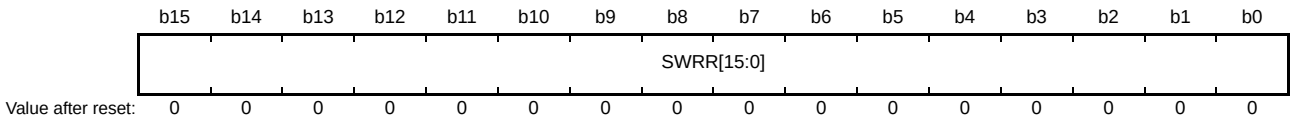
- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 7.2 occurs.
- When SWRF is read as 1 and then 0 is written to SWRF.

7.2.4 Software Reset Register (SWRR)

Address(es): 0008 00C2h



Bit	Symbol	Bit Name	Description	R/W
b15 to b0	SWRR[15:0]	Software Reset	Writing A501h resets the LSI. These bits are read as 0000h.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

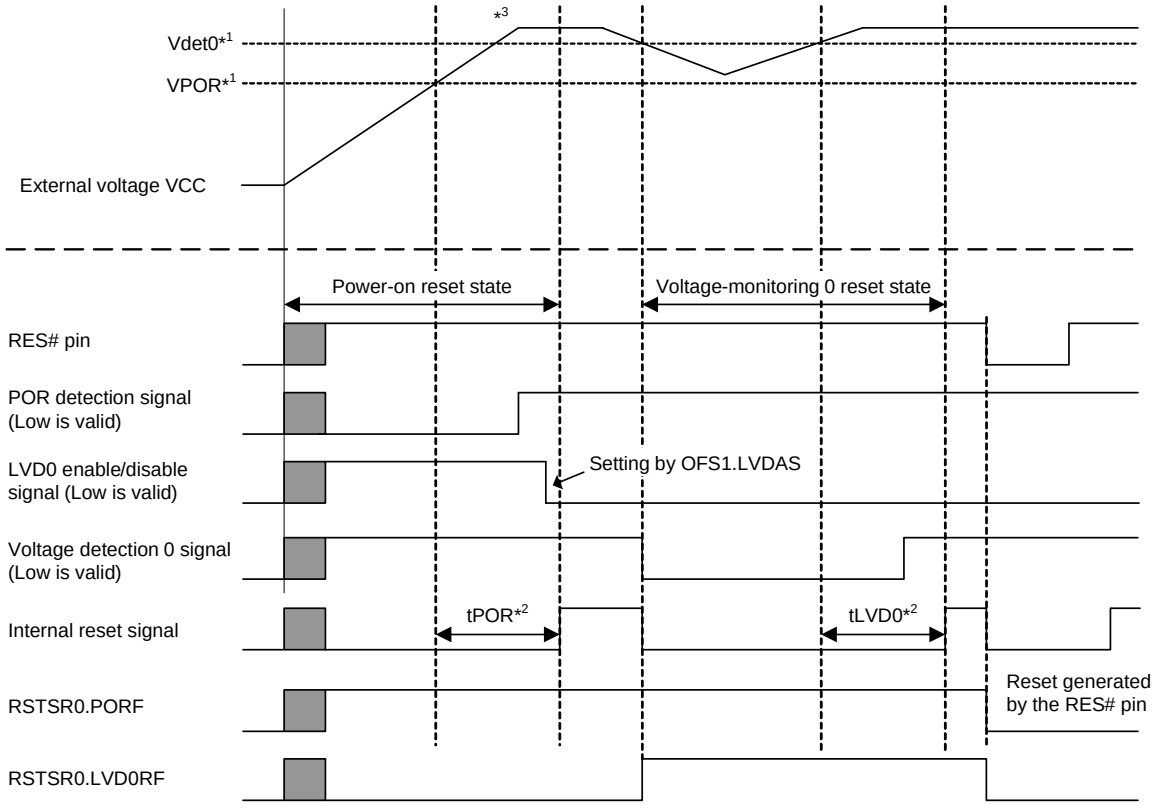
7.3 Operation

7.3.1 RES# Pin Reset

This is a reset generated by the RES# pin.
When the RES# pin is driven low, all the processing in progress is aborted and this MCU enters a reset state.
In order to unfailingly reset this MCU, the RES# pin should be held low for the specified power supply stabilization time at a power-on.
When the RES# pin is driven high from low, the internal reset is canceled after the post-RES# cancelation wait time (tRESWT) has elapsed, and then the CPU starts the reset exception handling.
For details, see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] and section 43, Electrical Characteristics [64- and 48-Pin Versions].

7.3.2 Power-On Reset and Voltage Monitoring 0 Reset

The power-on reset is an internal reset generated by the power-on reset circuit. If the RES# pin is in a high level state when power is supplied, a power-on reset is generated. After VCC has exceeded VPOR and the specified period (power-on reset time) has elapsed, the internal reset is canceled and the CPU starts the reset exception handling. The power-on reset time is a stabilization period of the external power supply and this MCU circuit. After a power-on reset has been generated, the PORF flag in RSTSR0 is set to 1. The PORF flag is initialized by a RES# pin reset.
The voltage monitoring 0 reset is an internal reset generated by the voltage monitoring circuit. If the voltage detection 0 level selection (LVDAS) bit in the option function select register 1 (OFS1) is 0 (voltage monitoring 0 reset is enabled after a reset) and VCC falls below Vdet0, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates voltage monitoring 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitoring 0 reset is to be used.
Release from the voltage monitoring 0 reset state occurs when VCC rises above Vdet0 and the LVD0 reset time (tLVD0) elapses.
Figure 7.1 shows operations during a power-on reset and voltage monitoring 0 reset.
For details on voltage monitoring 0 reset, refer to section 9, Voltage Detection Circuit (LVDA).



Note: • For details on the electrical characteristics, see section 41, Electrical Characteristics (Required Specifications) and section 42, Electrical Characteristics [64- and 48-Pin Versions].

Note 1. Vdet0 shows a voltage monitoring 0 reset detection level, and VPOR shows a power-on reset detection level.

Note 2. tPOR shows a time for power-on reset, and tLVD0 shows a time for voltage monitoring 0 reset.

Note 3. At a power-on, VCC should be risen to the minimum guaranteed voltage before the POR reset is released

Figure 7.1 Operation Examples During a Power-On Reset and Voltage Monitoring 0 Reset

7.3.3 Voltage Monitoring 1 Reset and Voltage Monitoring 2 Reset

The voltage monitoring 1 reset and voltage monitoring 2 reset are internal resets generated by the voltage monitoring circuit.

When the voltage monitoring 1 interrupt/reset enable bit (LVD1RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the voltage monitoring 1 circuit mode select bit (LVD1RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in the voltage monitoring 1 circuit control register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage-detection circuit generates a voltage monitoring 1 reset if VCC falls to or below Vdet1.

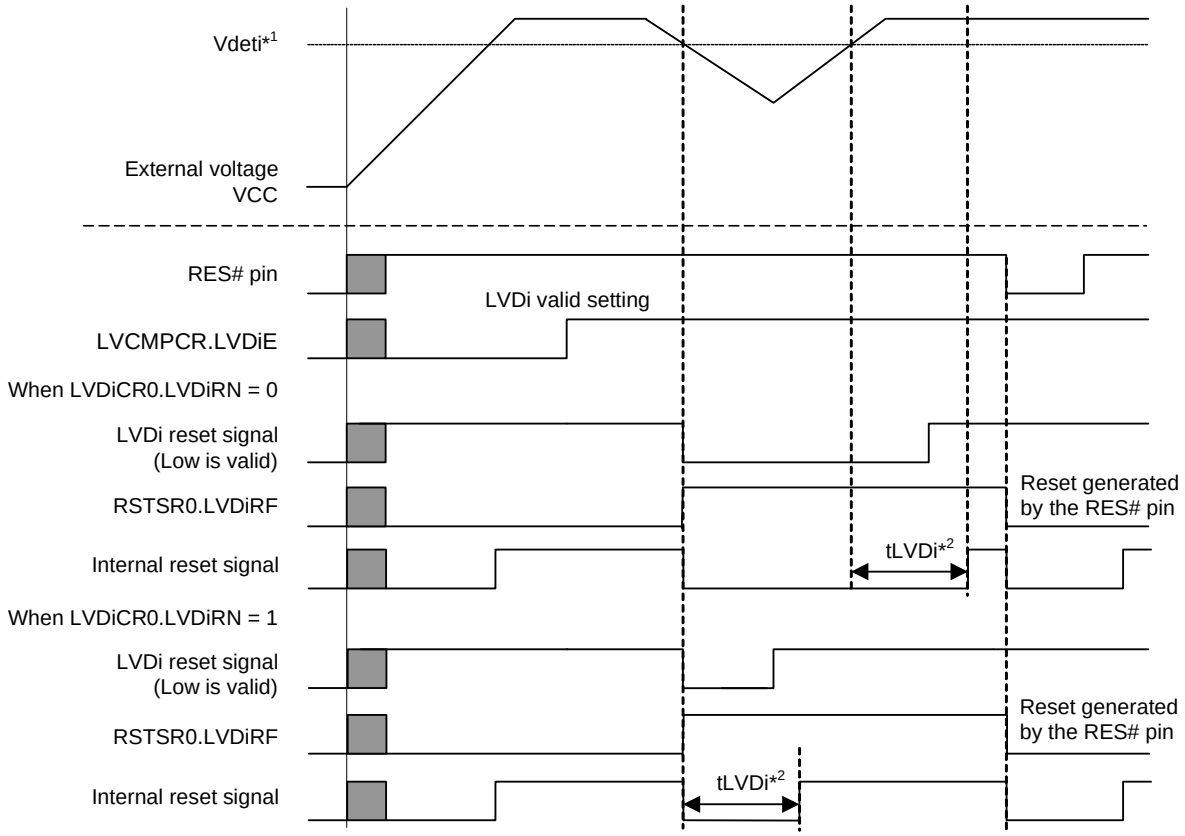
Likewise, when the voltage monitoring 2 interrupt/reset enable bit (LVD2RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the voltage monitoring 2 circuit mode select bit (LVD2RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in voltage monitoring 2 circuit control register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitoring 2 reset if VCC falls to or below Vdet2.

Timing for release from the voltage monitoring 1 reset state is selectable with the voltage monitoring 1 reset negate select bit (LVD1RN) in the LVD1CR0. When the LVD1CR0.LVD1RN bit is 0 and VCC has fallen to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling once the LVD1 reset time (tLVD1) has elapsed after VCC has risen above Vdet1. When the LVD1CR0.LVD1RN bit is 1 and VCC has fallen to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling once the LVD1 reset time (tLVD1) has elapsed.

Likewise, timing for release from the voltage monitoring 2 reset state is selectable by setting the voltage monitoring 2 reset negate select bit (LVD2RN) in LDV2CR0 register. Detection levels Vdet1 and Vdet2 can be changed by settings in the voltage detection select register (LDVLVLR).

Figure 6.2 shows examples of operations during voltage monitoring 1 and 2 resets.

For details on the voltage monitoring 1 reset and voltage monitoring 2 reset, refer to section 9, Voltage Detection Circuit (LVDA).



Note: • For details on the electrical characteristics, see section 41, Electrical Characteristics (Required Specifications) and section 42, Electrical Characteristics [64- and 48-Pin Versions].

Note 1. Vdeti shows a detection level of voltage monitoring 1 reset and voltage monitoring 2 reset.

Note 2. tLVDi shows a time for voltage monitoring 1 reset and voltage monitoring 2 reset. (i = 1, 2)

Figure 7.2 Operation Examples During Voltage Monitoring 1 Reset and Voltage Monitoring 2 Reset

7.3.4 Deep Software Standby Reset

This is an internal reset generated when deep software standby mode is canceled by an interrupt.
When a deep software standby mode cancelation source is generated, a deep software standby reset is generated. The deep software standby reset is canceled after tDSBY (return time after deep software standby mode cancelation) has elapsed. At the same time, deep software standby mode is also canceled.
When tDSBYWT (wait time after deep software standby mode cancelation) has elapsed after deep software standby mode has been canceled, the internal reset is canceled and the CPU starts the reset exception handling.
For details of the deep software standby reset, see section 12, Low Power Consumption.

7.3.5 Independent Watchdog Timer Reset

Independent watchdog timer reset is an internal reset generated by the independent watchdog timer.
Output of the independent watchdog timer reset from the independent watchdog timer can be selected by settings in the IWDT reset control register (IWDTRCR) or option function select register 0 (OFS0).
When output of the independent watchdog timer reset is selected, an independent watchdog timer reset is generated if the independent watchdog timer underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) has elapsed after the independent watchdog timer reset has been generated, the internal reset is canceled and the CPU starts the reset exception handling.
For details on the independent watchdog timer reset, see section 27, Independent Watchdog Timer (IWDTa).

7.3.6 Watchdog Timer Reset

The watchdog-timer reset is an internal reset from the watchdog timer.
Output of the watchdog timer reset from the watchdog timer can be selected by settings in the WDT reset control register (WDTRCR) or option function select register 0 (OFS0).
When output of the watchdog timer reset is selected, a watchdog timer reset is generated if the watchdog timer underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) has elapsed after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.
For details on the watchdog timer reset, see section 26, Watchdog Timer (WDTA).

7.3.7 Software Reset

The software reset is an internal reset generated by the software reset circuit.
When A501h is written to the software reset register (SWRR), a software reset is generated. When the internal reset time (tRESW2) has elapsed after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

7.3.8 Determination of Cold/Warm Start

By reading the CWSF flag in RSTSR1, the type of reset processing caused can be identified; that is, whether a power-on reset has caused the reset processing (cold start) or a reset signal input during operation has caused the reset processing (warm start).

The CWSF flag in RSTSR1 is set to 0 when a power-on reset occurs (cold start); otherwise the flag is not set to 0. The flag is set to 1 when 1 is written to it through programming; it is not set to 0 even when 0 is written.

Figure 7.3 shows an example of cold/warm start determination operation.

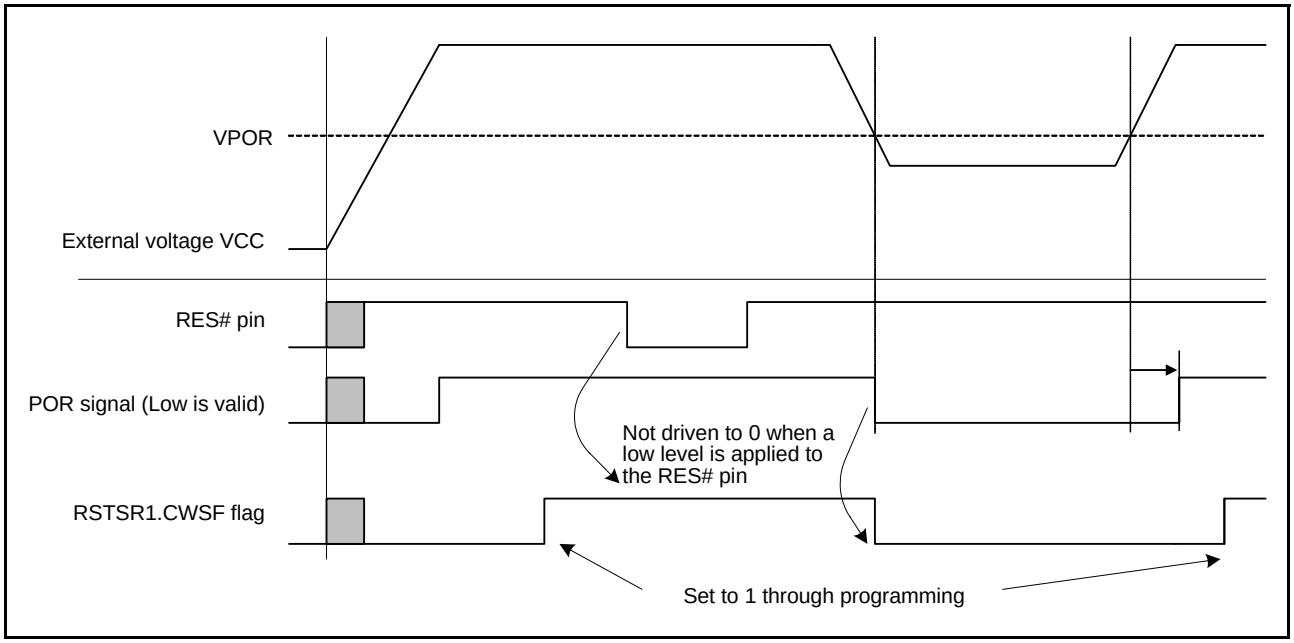


Figure 7.3 Example of Cold/Warm Start Determination Operation

7.3.9 Determination of Reset Generation Source

Reading RSTSR0 and RSTSR2 determines which reset was used to execute the reset exception handling. Figure 7.4 shows an example of the flow to identify a reset generation source.

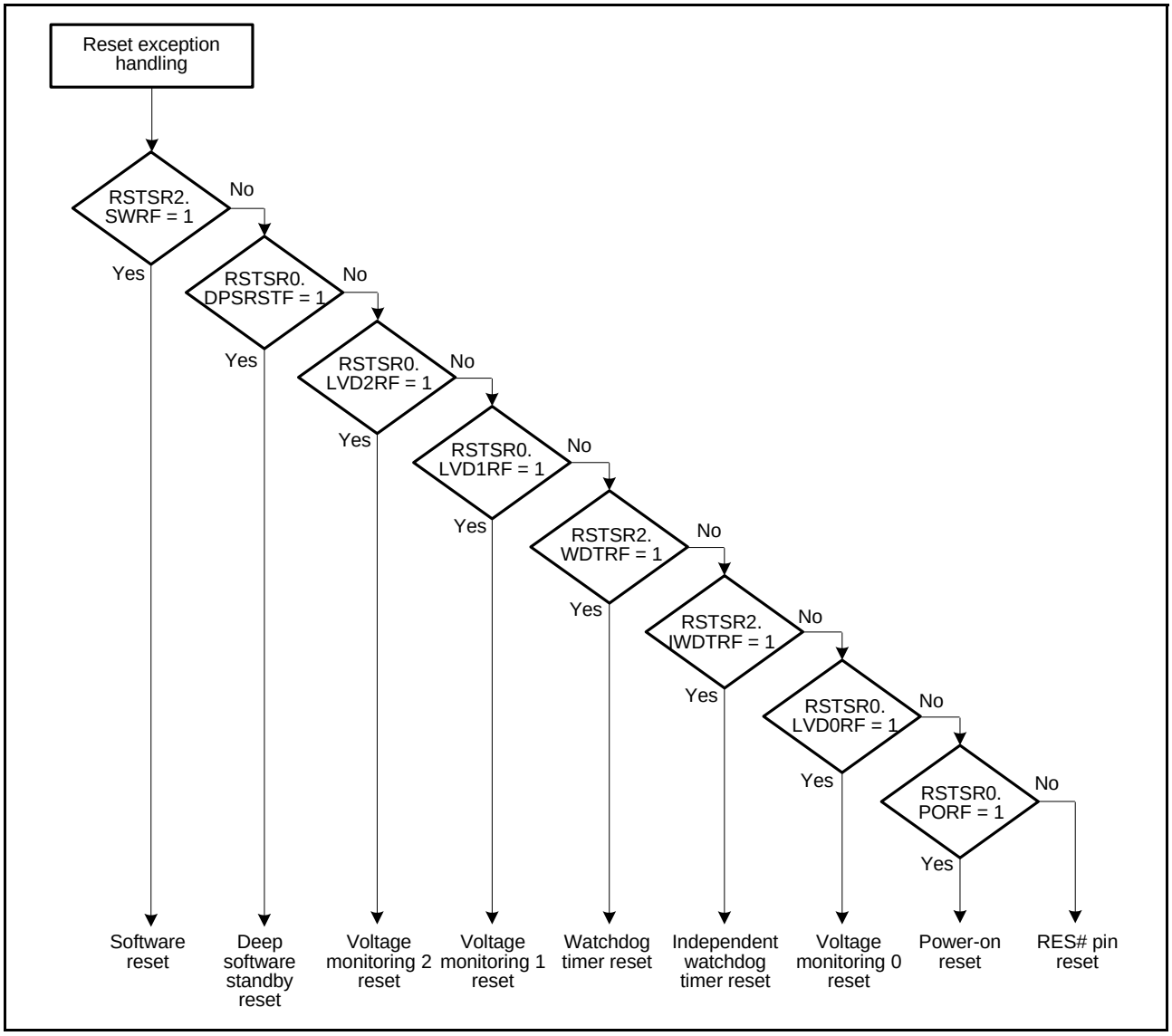


Figure 7.4 Example of Reset Generation Source Determination Flow

8. Option-Setting Memory

8.1 Overview

Option-setting memory refers to a set of registers that are provided for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the ROM.
Figure 8.1 shows the option-setting memory area.

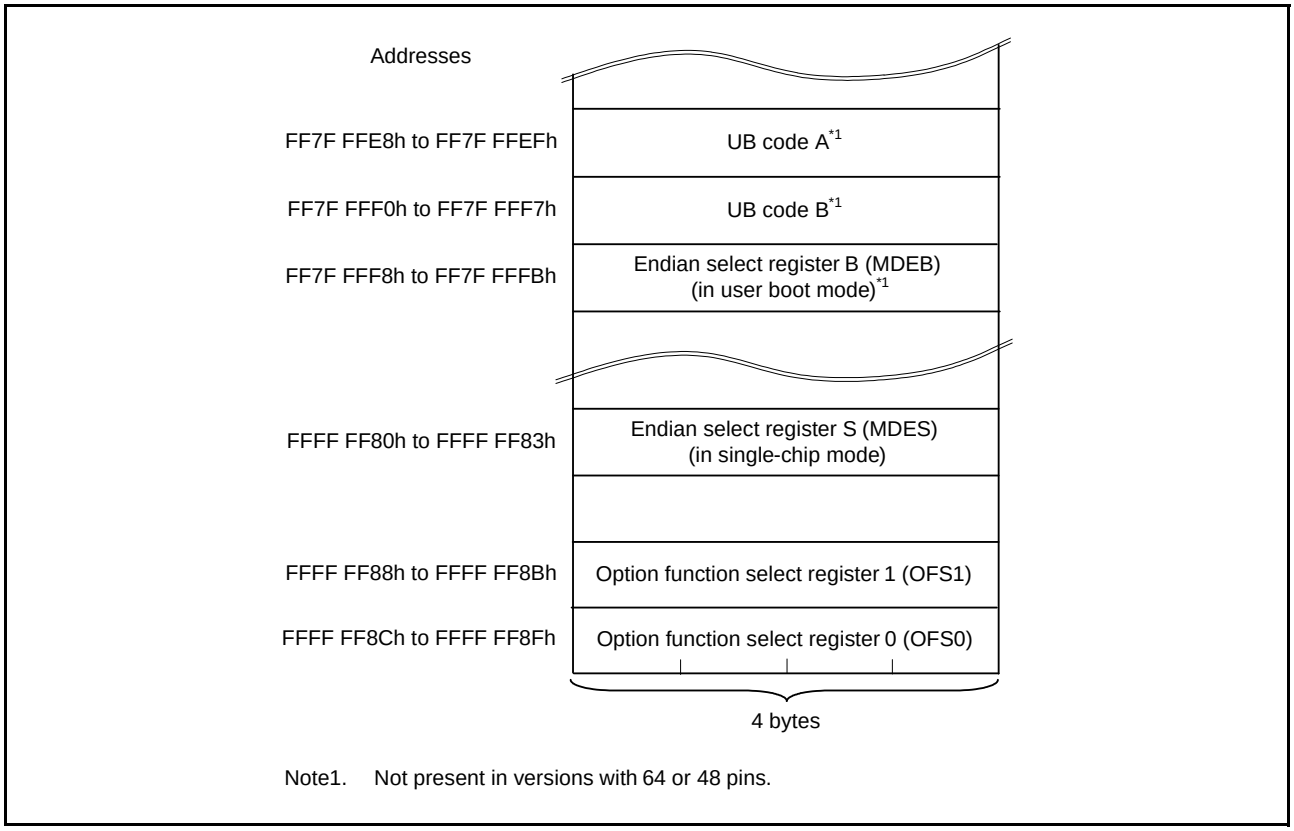


Figure 8.1 Option-Setting Memory Area

8.2 Register Descriptions

8.2.1 Option Function Select Register 0 (OFS0)

Address(es): FFFF FF8Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
Value after reset:	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IWDTSLCSTP	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
Value after reset:	The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	When reading, this bit returns to the value written by the user. The write value should be 1.	R
b1	IWDTSTRT	IWDT Start Mode Select	0: IWDT is automatically activated in auto-start mode after a reset 1: IWDT is halted after a reset	R
b3, b2	IWDTTOPS[1:0]	IWDT Timeout Period Select	b3 b2 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	R
b7 to b4	IWDTCKS[3:0]	IWDT Clock Frequency Division Ratio Select	b7 b4 0 0 0 0: x 1 (Cycle period: 131 ms) 0 0 1 0: x 1/16 (Cycle period: 2.10 s) 0 0 1 1: x 1/32 (Cycle period: 4.19 s) 0 1 0 0: x 1/64 (Cycle period: 8.39 s) 1 1 1 1: x 1/128 (Cycle period: 16.8 s) 0 1 0 1: x 1/256 (Cycle period: 33.6 s) Settings other than above are prohibited.	R
b9, b8	IWDTRPES[1:0]	IWDT Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting)	R
b11, b10	IWDTRPSS[1:0]	IWDT Window Start Position Select	b11 b10 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting)	R
b12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select	0: Non-maskable interrupt request is enabled 1: Reset is enabled	R
b13	—	Reserved	When reading, this bit returns to the value written by the user. The write value should be 1.	R
b14	IWDTSLCSTP	IWDT Sleep Mode Count Stop Control	0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode	R
b16, b15	—	Reserved	When reading, these bits return to the value written by the user. The write value should be 1.	R
b17	WDTSTRT	WDT Start Mode Select	0: WDT is automatically activated in auto-start mode after a reset 1: WDT is stopped after a reset	R

Bit	Symbol	Bit Name	Description	R/W
b19, b18	WDTTOPS[1:0]	WDT Timeout Period Select	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	R
b23 to b20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select	b23 b20 0 0 0 1: PCLK/4 0 1 0 0: PCLK/64 1 1 1 1: PCLK/128 0 1 1 0: PCLK/512 0 1 1 1: PCLK/2048 1 0 0 0: PCLK/8192 Settings other than above are prohibited.	R
b25, b24	WDTRPES[1:0]	WDT Window End Position Select	b25 b24 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting)	R
b27, b26	WDTRPSS[1:0]	WDT Window Start Position Select	b27 b26 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting)	R
b28	WDTRSTIRQS	WDT Reset Interrupt Request Select	0: Non-maskable interrupt request is enabled 1: Reset is enabled	R
b31 to b29	—	Reserved	When reading, these bits return to the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. It is set to the written value after written by the user.

The OFS0 register is allocated in the ROM. Set this register at the same time as writing the program. After writing to the OFS0 register once, do not write to it again.
When erasing the block including the OFS0 register, the OFS0 register value becomes FFFF FFFFh.
The setting in the OFS0 register is ineffective in user boot mode, and the value becomes FFFF FFFFh.

IWDTSTRT Bit (IWDT Start Mode Select)

This bit selects the mode in which the IWDT is activated after a reset (stopped state or activated in auto-start mode). When activated in auto-start mode, the OFS0 register setting for the IWDT is effective.

IWDTTOPS[1:0] Bits (IWDT Timeout Period Select)

These bits select the timeout period, i.e. the time it takes for the down-counter to underflow, as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set by the IWDTCKS[3:0] bits. The time (number of LOCO clock cycles for the IWDT) it takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] bits and IWDTTOPS[1:0] bits.
For details, see section 27, Independent Watchdog Timer (IWDTa).

IWDTCKS[3:0] Bits (IWDT Clock Frequency Division Ratio Select)

These bits select, from 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256, the division ratio of the prescaler to divide the frequency of the LOCO clock for the IWDT. Using the setting of these bits together with the IWDTTOPS[1:0] bit setting, the IWDT counting period can be set from 1024 to 4194304 LOCO clock cycles for the IWDT.
For details, see section 27, Independent Watchdog Timer (IWDTa).

IWDTRPES[1:0] Bits (IWDT Window End Position Select)

These bits select the position of the end of the window for the down-counter as 0%, 25%, 50%, or 75% of the value being counted by the counter. The value of the window end position must be smaller than the value of the window start position (window start position > window end position). If the value for the window end position is greater than the value for the

window start position, only the value for the window start position is effective.
The counter values corresponding to the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting of the IWDTTOPS[1:0] bits.
For details, refer to section 27, Independent Watchdog Timer (IWDTa).

IWDTRPSS[1:0] Bits (IWDT Window Start Position Select)

These bits select the position where the window for the down-counter starts as 25%, 50%, 75%, or 100% of the value being counted (the point at which counting starts is 100% and the point at which an underflow occurs is 0%). The interval between the positions where the window starts and ends becomes the period in which refreshing is possible, and refreshing is not possible outside this period.
For details, refer to section 27, Independent Watchdog Timer (IWDTa).

IWDTRSTIRQS Bit (IWDT Reset Interrupt Request Select)

The setting of this bit selects the operation on an underflow of the down-counter or generation of a refresh error. Either an independent watchdog timer reset or a non-maskable interrupt request is selectable.
For details, refer to section 27, Independent Watchdog Timer (IWDTa).

IWDTSLCSTP Bit (IWDT Sleep Mode Count Stop Control)

This bit selects to stop counting when entering sleep, software standby, deep software standby, or all-module clock stop mode.
For details, see section 27, Independent Watchdog Timer (IWDTa).

WDTSTRT Bit (WDT Start Mode Select)

This bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto-start mode). When activated in auto-start mode, the OFS0 register setting for the WDT is effective.

WDTTOPS[1:0] Bits (WDT Timeout Period Select)

These bits select the timeout period, i.e. the time it takes for the down-counter to underflow, as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set by the WDTCKS[3:0] bits. The time (number of PCLK cycles) it takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] bits and WDTTOPS[1:0] bits.
For details, see section 26, Watchdog Timer (WDTA).

WDTCKS[3:0] Bits (WDT Clock Frequency Division Ratio Select)

These bits select, from 1/4, 1/64, 1/128, 1/512, 1/2048, and 1/8192, the division ratio of the prescaler to divide the frequency of PCLK. Using the setting of these bits together with the WDTTOPS[1:0] bit setting, the WDT counting period can be set from 4096 to 134217728 PCLK cycles.
For details, see section 26, Watchdog Timer (WDTA).

WDTRPES[1:0] Bits (WDT Window End Position Select)

These bits select the position of the end of the window on the down-counter as 0%, 25%, 50%, or 75% of the value being counted by the counter. The value of the window end position must be smaller than the value of the window start position (window start position > window end position). If the value for the window end position is greater than the value for the window start position, only the value for the window start position is effective.
The counter values corresponding to the settings for the start and end positions of the window in the WDTRPSS[1:0] and WDTRPES[1:0] bits vary with the setting of the WDTTOPS[1:0] bits.
For details, refer to section 26, Watchdog Timer (WDTA).

WDTRPSS[1:0] Bits (WDT Window Start Position Select)

These bits select the position where the window for the down-counter starts as 25%, 50%, 75%, or 100% of the value being counted (the point at which counting starts is 100% and the point at which an underflow occurs is 0%). The interval between the positions where the window starts and ends becomes the period in which refreshing is possible, and refreshing is not possible outside this period.
For details, refer to section 26, Watchdog Timer (WDTA).

WDTRSTIRQS Bit (WDT Reset Interrupt Request Select)

The setting of this bit selects the operation on an underflow of the down-counter or generation of a refresh error. Either a watchdog timer reset or a non-maskable interrupt request is selectable.
For details, refer to section 26, Watchdog Timer (WDTA).

8.2.2 Option Function Select Register 1 (OFS1)

Address(es): FFFF FF88h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	LVDAS	—	—
	The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	When reading, these bits return to the value written by the user. The write value should be 1.	R
b2	LVDAS	Voltage Detection 0 Circuit Start	0: Voltage monitor 0 reset is enabled after a reset 1: Voltage monitor 0 reset is disabled after a reset	R
b31 to b3	—	Reserved	When reading, these bits return to the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. It is set to the written value after written by the user.

The OFS1 register is allocated in the ROM. Set this register at the same time as writing the program. After writing, do not write additions to this register.
When erasing the block including the OFS1 register, the setting in the OFS1 register is ineffective, and the OFS1 register value becomes FFFF FFFFh.
The setting in the OFS1 register is ineffective in user boot mode, and the value becomes FFFF FFFFh.

LVDAS Bit (Voltage Detection 0 Circuit Start)

This bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

8.2.3 Endian Select Register B (MDEB), Endian Select Register S (MDES)

Address(es): FF7F FFF8h: MDEB (in user boot mode)
FFFF FF80h: MDES (in single-chip mode)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MDE[2:0]		
Value after reset:	The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MDE[2:0]	Endian Select	b2 b0 0 0 0: Big endian 1 1 1: Little endian Settings other than above are prohibited.	R
b31 to b3	—	Reserved	When reading, this bit returns to the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. It is set to the written value after written by the user.

The MDEn (n = B, S) register selects the endian for the CPU. In user boot mode, the endian select register B (MDEB) at address FF7F FFF8h is used to select the endian. In single-chip mode, the endian select register S (MDES) at address FFFF FF80h is used.
MDEn is allocated in the ROM. Set the register at the same time as writing the program. After writing to the register once, do not write to it again.
When erasing the block including the MDEn register, the MDEn register value becomes FFFF FFFFh.

MDE[2:0] Bits (Endian Select)

These bits select little endian or big endian for the CPU.
The endian is determined by the value at address FF7F FFF8h in the user boot area when operating in user boot mode, and by the value at address FFFF FF80h in the user area when operating in single-chip mode.

8.3 UB Codes

UB codes A and B are required if user boot mode is to be employed. When the USB boot mode is used continuously, these codes should not be changed. The MCU will start up in user boot mode on release from the reset state if the four conditions below are satisfied.

- UB code A is 55736572h and 426F6F74h.
- UB code B is FFFF FF00h and 0008 C040h.
- The low level is being input on the MD pin.
- The high level is being input on the P00 pin.

8.3.1 UB Code A

UB code A consists of two 32-bit words. Set UB code A to 55736572h and 426F6F74h. Do not set other values for the code.
Figure 8.2 shows the structure of UB code A in memory. Set UB code A in 32-bit units.

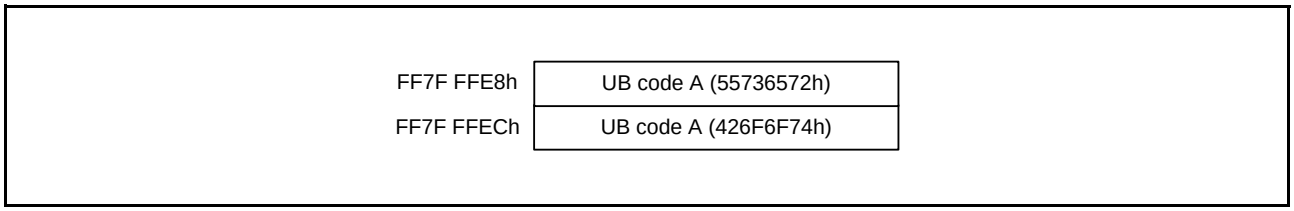


Figure 8.2 UB Code A Structure

8.3.2 UB Code B

UB code B consists of two words, i.e. 32 bits. Set UB code B to FFFF FF00h and 0008 C040h. Do not set other values for the code.
Figure 8.3 shows the structure of UB code B in memory. Set UB code B in 32-bit units.

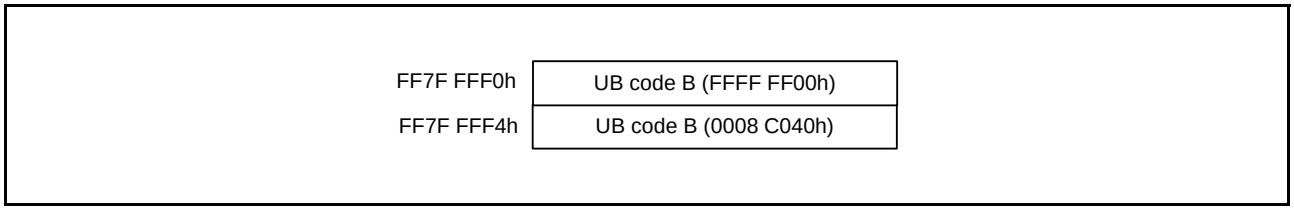


Figure 8.3 UB Code B Structure

8.4 Usage Note

8.4.1 Setting Example of Option-Setting Memory

Since the option-setting memory is allocated in the ROM, values cannot be written by executing instructions. Write appropriate values when writing the program. An example of the settings is shown below.

- To set ffff fff8h in the OFS0 register

```
.org    0ffff ff8ch
.lword  0ffffff8h
```

Note: • Programming formats vary depending on the compiler. Refer to the compiler manual for details.

9. Voltage Detection Circuit (LVDA)

The voltage detection circuit (LVDA) monitors the voltage level input to the VCC pin using a program.

9.1 Overview

In voltage detection 0, whether to enable or disable the reset of voltage monitoring 0 can be selected after the reset using the option function select register 1 (OFS1).
In voltage detection 1 and voltage detection 2, the detection voltage is set using the voltage detection level select register (LVDLVLR).
Reset of voltage monitoring 0, reset/interrupt of voltage monitoring 1, and reset/interrupt of voltage monitoring 2 can be used.

Table 9.1 lists the specifications of the voltage detection circuit. Figure 9.1 is a block diagram of the voltage detection circuit. Figure 9.2 is a block diagram of the voltage monitoring 1 interrupt/reset circuit. Figure 9.3 is a block diagram of the voltage monitoring 2 interrupt/reset circuit.

Table 9.1 Voltage Detection Circuit Specifications

Item		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2
	Detected event	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	One level fixed	Specify voltage using LVDLVLR.LVD1LVL[3:0] bits	Specify voltage using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flag	None	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	No interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable interrupt	Non-maskable interrupt
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enable/ Disable switching	Digital filter function not available	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)

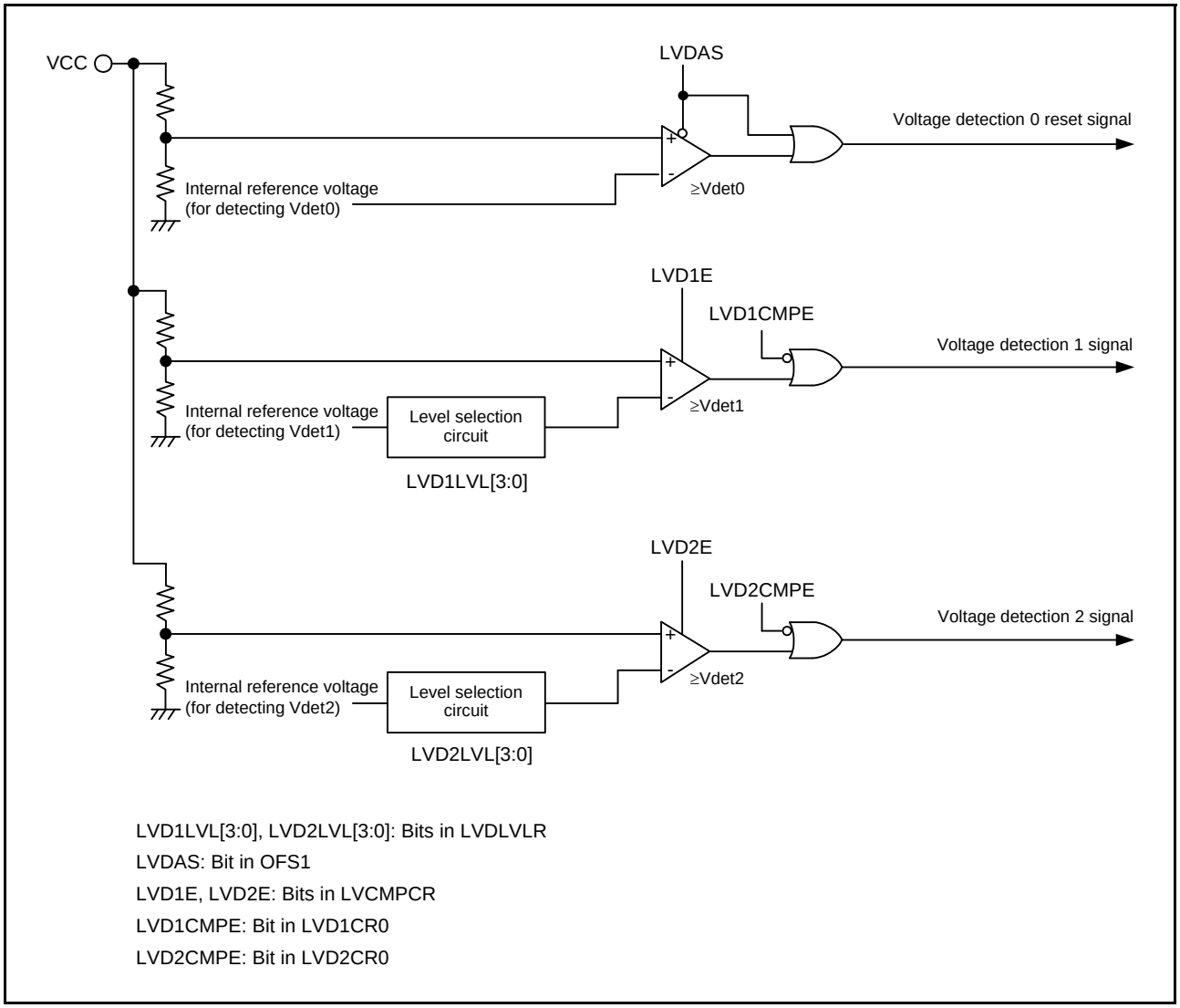


Figure 9.1 Block Diagram of Voltage Detection Circuit

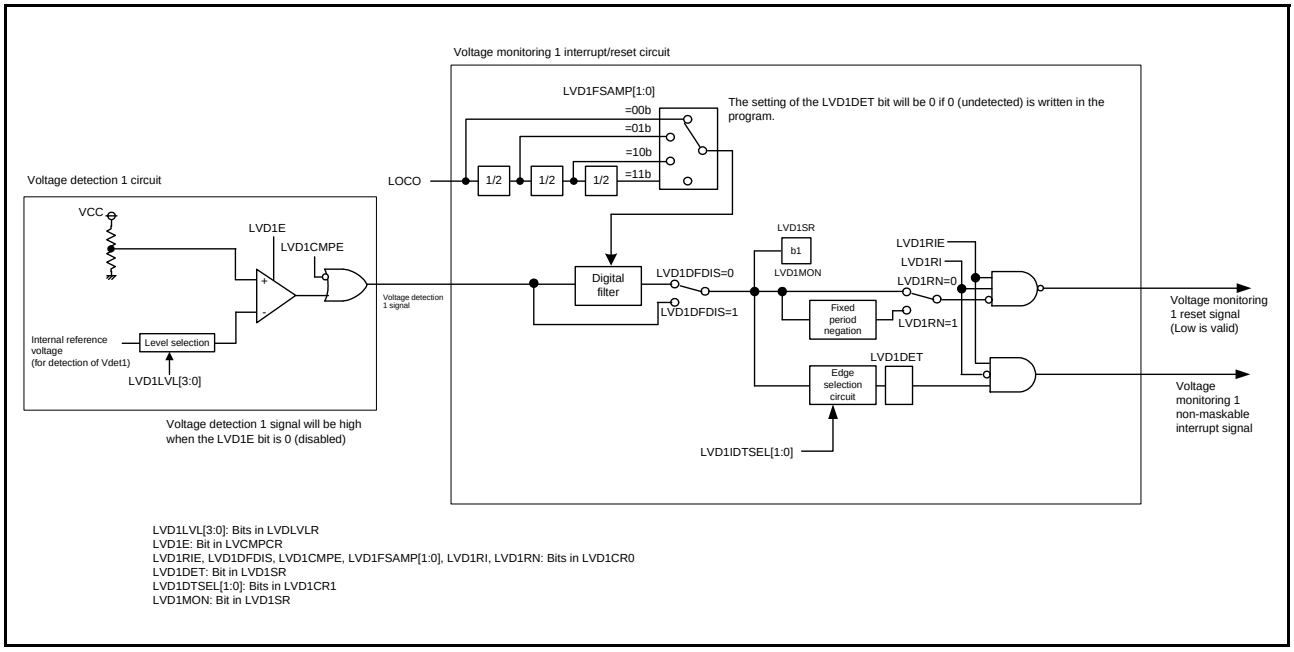


Figure 9.2 Block Diagram of Voltage Monitoring 1 Interrupt/Reset Circuit

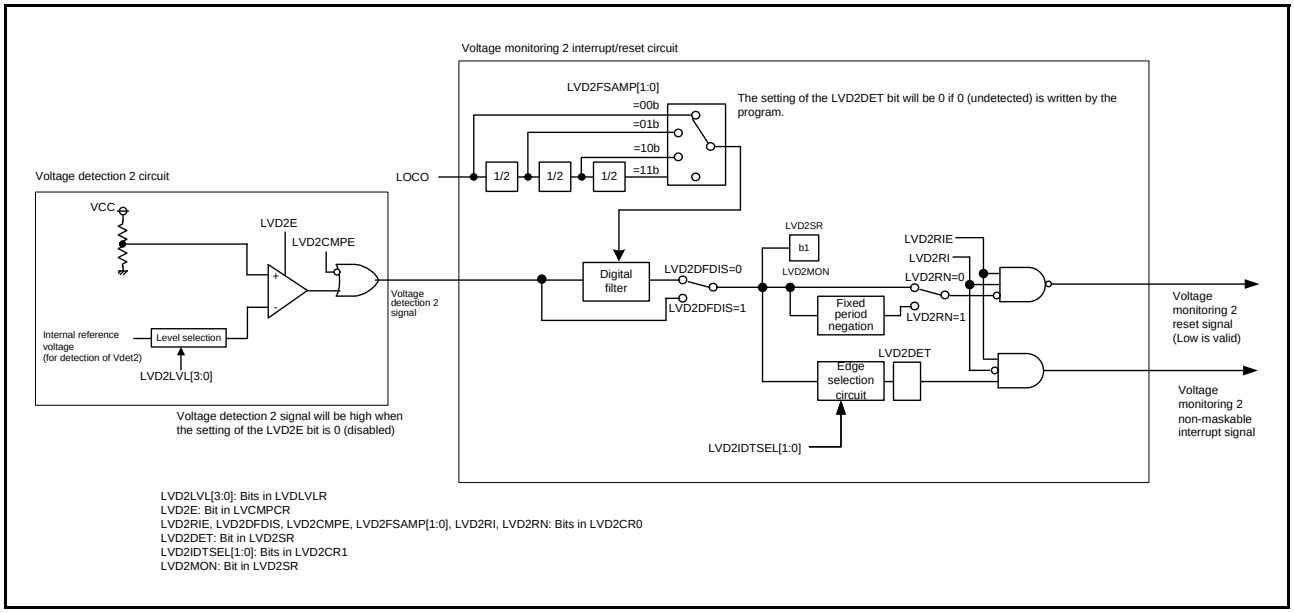


Figure 9.3 Block Diagram of Voltage Monitoring 2 Interrupt/Reset Circuit

9.2 Register Descriptions

9.2.1 Voltage Monitoring 1 Circuit Control Register 1 (LVD1CR1)

Address(es): 0008 00E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LVD1IDTSEL [1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	LVD1IDTSEL [1:0]	Voltage Monitoring 1 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ Vdet1 (rise) is detected 0 1: When VCC < Vdet1 (drop) is detected 1 0: When drop and rise are detected 1 1: Settings prohibited	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

9.2.2 Voltage Monitoring 1 Circuit Status Register (LVD1SR)

Address(es): 0008 00E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LVD1MON	LVD1DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	LVD1DET	Voltage Monitoring 1 Voltage Change Detection Flag	0: Not detected 1: Vdet1 passage detection	R(/W) *1
b1	LVD1MON	Voltage Monitoring 1 Signal Monitor Flag	0: VCC < Vdet1 1: VCC ≥ Vdet1 or LVD1MON is disabled	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes 2 peripheral module clock cycles for the bit to be read as 0.

LVD1DET Flag (Voltage Monitoring 1 Voltage Change Detection Flag)

The LVD1DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.LVD1CMPE bit is 1 (voltage monitoring 1 circuit comparison result output enabled).
When LVD1CR0 and LVD1CR1 have been modified, the LVD1DET flag may become 1.
The LVD1DET flag should be set to 0 after LVD1CR0.LVD1RIE is set to 0 (disabled). LVD1CR0.LVD1RIE can be set to 1 (enabled) after a period of two or more cycles of PCLKB has elapsed.
Depending on the number of cycles of PCLKB defined for access to read an I/O register, two or more cycles than PCLKB may have to be secured as waiting time.

LVD1MON Flag (Voltage Monitoring 1 Signal Monitor Flag)

The LVD1MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.LVD1CMPE bit is 1 (voltage monitoring 1 circuit comparison result output enabled).

9.2.3 Voltage Monitoring 2 Circuit Control Register 1 (LVD2CR1)

Address(es): 0008 00E2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LVD2IDTSEL [1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	LVD2IDTSEL [1:0]	Voltage Monitoring 2 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ Vdet2 (rise) is detected 0 1: When VCC < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Settings prohibited	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

9.2.4 Voltage Monitoring 2 Circuit Status Register (LVD2SR)

Address(es): 0008 00E3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LVD2MON	LVD2DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	LVD2DET	Voltage Monitoring 2 Voltage Change Detection Flag	0: Not detected 1: Vdet2 passage detection	R(/W) *1
b1	LVD2MON	Voltage Monitoring 2 Signal Monitor Flag	0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes 2 peripheral module clock cycles for the bit to be read as 0.

LVD2DET Flag (Voltage Monitoring 2 Voltage Change Detection Flag)

The LVD2DET flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.LVD2CMPE bit is 1 (voltage monitoring 2 circuit comparison result output enabled).
When LVD2CR0 and LVD2CR1 have been modified, the LVD2DET flag may become 1.
The LVD2DET flag should be set to 0 after LVD2CR0.LVD2RIE is set to 0 (disabled). LVD2CR0.LVD2RIE can be set to 1 (enabled) after a period of two or more cycles of PCLKB has elapsed.
Depending on the number of cycles of PCLKB defined for access to read an I/O register, two or more cycles of PCLKB may have to be secured as waiting time.

LVD2MON Flag (Voltage Monitoring 2 Signal Monitor Flag)

The LVD2MON flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.LVD2CMPE bit is 1 (voltage monitoring 2 circuit comparison result output enabled).

9.2.5 Voltage Monitoring Circuit Control Register (LVCMPCR)

Address(es): 0008 C297h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	LVD2E	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	LVD1E	Voltage Detection 1 Enable	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b6	LVD2E	Voltage Detection 2 Enable	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1E Bit (Voltage Detection 1 Enable)

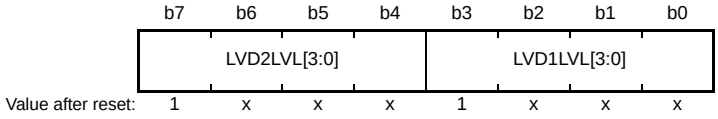
When using voltage detection 1 interrupt/reset or the LVD1SR.LVD1MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts once td(E-A) passes after the LVD1E bit value is changed from 0 to 1.

LVD2E Bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.LVD2MON bit, set the LVD2E bit to 1. The voltage detection 2 circuit starts once td(E-A) passes after the LVD2E bit value is changed from 0 to 1.

9.2.6 Voltage Detection Level Select Register (LVDLVLR)

Address(es): 0008 C298h



x: Undefined

[144-, 120-, 112- and 100-pin versions]

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	LVD1LVL[3:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage)	[3-V product] b3 b2 b1 b0 1 0 0 0: 2.90 V 1 0 0 1: 2.85 V 1 0 1 0: 2.88 V Do not set otherwise. [5-V product] b3 b2 b1 b0 1 0 0 0: 4.77 V 1 0 0 1: 4.23 V 1 0 1 0: 4.50 V Do not set otherwise.	R/W
b7 to b4	LVD2LVL[3:0]	Voltage Detection 2 Level Select (Standard voltage during drop in voltage)	[3-V product] b3 b2 b1 b0 1 0 0 0: 2.90 V 1 0 0 1: 2.85 V 1 0 1 0: 2.88 V Do not set otherwise. [5-V product] b3 b2 b1 b0 1 0 0 0: 4.77 V 1 0 0 1: 4.23 V 1 0 1 0: 4.50 V Do not set otherwise.	R/W

[64- and 48-pin versions]

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	LVD1LVL[3:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage)	b3 b2 b1 b0 1 0 1 0: 2.95 V Do not set otherwise.	R/W
b7 to b4	LVD2LVL[3:0]	Voltage Detection 2 Level Select (Standard voltage during drop in voltage)	b7 b6 b5 b4 1 0 1 0: 2.95 V Do not set otherwise.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The contents of the LVDLVLR register can only be changed if the LVCMPCR.LVD1E and LVCMPCR.LVD2E bits (voltage detection n circuit disable; n = 1, 2) are both 0.

9.2.7 Voltage Monitoring 1 Circuit Control Register 0 (LVD1CR0)

Address(es): 0008 C29Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD1RN	LVD1RI	LVD1FSAMP[1:0]		—	LVD1CMPE	LVD1DFDIS	LVD1RIE
Value after reset:	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	LVD1RIE	Voltage Monitoring 1 Interrupt/Reset Enable	0: Disabled 1: Enabled	R/W
b1	LVD1DFDIS	Voltage Monitoring 1 Digital Filter Disable Mode Select	0: Digital filter enabled 1: Digital filter disabled	R/W
b2	LVD1CMPE	Voltage Monitoring 1 Circuit Comparison Result Output Enable	0: Voltage monitoring 1 circuit comparison result output disabled. 1: Voltage monitoring 1 circuit comparison result output enabled.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b5, b4	LVD1FSAMP[1:0]	Sampling Clock Select	b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	R/W
b6	LVD1RI	Voltage Monitoring 1 Circuit Mode Select	0: Voltage monitoring 1 interrupt enabled when Vdet1 is crossed 1: Voltage monitoring 1 reset enabled when the voltage falls below Vdet1	R/W
b7	LVD1RN	Voltage Monitoring 1 Reset Negate Select	0: Negation follows a stabilization time (tLVD1) after VCC > Vdet1 is detected. 1: Negation follows a stabilization time (tLVD1) after assertion of the LVD1 reset.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1RIE Bit (Voltage Monitoring 1 Interrupt/Reset Enable)

The LVD1RIE bit is enabled when the LVCMPCR.LVD1E bit is set to 1 (enabling the voltage detection 1 circuit) and the LVD1CMPE bit is set to 1 (enabling output of the results of comparison by voltage monitor 1).
During programming or erasure of flash memory, please do not generate neither a voltage monitor 1 interrupt nor voltage monitor 1 reset.

LVD1DFDIS Bit (Voltage Monitoring 1 Digital Filter Disable Mode Select)

Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) if the LVD1DFDIS bit is 0 (enabling the digital filter circuit).
Set the LVD1DFDIS bit to 1 (digital filter circuit disabled) when using voltage monitoring 1 circuit in software standby mode or deep software standby mode.

LVD1FSAMP[1:0] Bits (Sampling Clock Select)

The LVD1FSAMP[1:0] bits can be modified only when the LVD1DFDIS bit is 1 (digital filter circuit disabled). The LVD1FSAMP[1:0] bits should not be modified when the LVD1DFDIS bit is 0 (digital filter circuit disabled).

LVD1RI Bit (Voltage Monitoring 1 Circuit Mode Select)

When the LVD1RI bit is 1 (voltage monitoring 1 reset enabled) or when the LVD2CR0.LVD2RI bit is 1 (voltage monitoring 2 reset enabled), a transition to deep software standby mode cannot be made, instead a transition to software standby mode is made. To enter deep software standby mode, set the LVD1RI bit to 0 (voltage monitoring 1 interrupt enabled) and the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt enabled).

LVD1RN Bit (Voltage Monitoring 1 Reset Negate Select)

If the LVD1RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Furthermore, if a transition to software standby or deep software standby is to be made, the only possible value for the LVD1RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the LVD1RN bit to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal) when this is the case.

9.2.8 Voltage Monitoring 2 Circuit Control Register 0 (LVD2CR0)

Address(es): 0008 C29Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD2RN	LVD2RI	LVD2FSAMP[1:0]		—	LVD2CMPE	LVD2DFDIS	LVD2RIE
Value after reset:	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	LVD2RIE	Voltage Monitoring 2 Interrupt/Reset Enable	0: Disabled 1: Enabled	R/W
b1	LVD2DFDIS	Voltage Monitoring 2 Digital Filter Disable Mode Select	0: Digital filter enabled 1: Digital filter disabled	R/W
b2	LVD2CMPE	Voltage Monitoring 2 Circuit Comparison Result Output Enable	0: Voltage monitoring 2 circuit comparison result output disabled. 1: Voltage monitoring 2 circuit comparison result output enabled.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b5, b4	LVD2FSAMP[1:0]	Sampling Clock Select	b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	R/W
b6	LVD2RI	Voltage Monitoring 2 Circuit Mode Select	0: Voltage monitoring 2 interrupt during Vdet2 passage 1: Voltage monitoring 2 reset enabled when the voltage falls below Vdet2	R/W
b7	LVD2RN	Voltage Monitoring 2 Reset Negate Select	0: Negation follows a stabilization time (tLVD2) after VCC > Vdet2 is detected. 1: Negation follows a stabilization time (tLVD2) after assertion of the LVD2 reset.	R/W

Note: • Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD2RIE Bit (Voltage Monitoring 2 Interrupt/Reset Enable)

The LVD2RIE bit is enabled when the LVCMPCR.LVD2E bit is set to 1 (enabling the voltage detection 2) and the LVD2CMPE bit is set to 1 (enabling output of the results of comparison by voltage monitor 2).

During programming or erasure of flash memory, please do not generate neither a voltage monitor 2 interrupt nor voltage monitor 2 reset.

LVD2DFDIS Bit (Voltage Monitoring 2 Digital Filter Disable Mode Select)

Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) if the LVD1DFDIS bit is 0 (enabling the digital filter circuit).

Set the LVD2DFDIS bit to 1 (digital filter circuit disabled) when using voltage monitoring 2 circuit in software standby mode or deep software standby mode.

LVD2FSAMP[1:0] Bits (Sampling Clock Select)

The LVD2FSAMP[1:0] bits can be modified only when the LVD2DFDIS bit is 1 (digital filter circuit disabled). The LVD2FSAMP[1:0] bits should not be modified when the LVD2DFDIS bit is 0 (digital filter circuit enabled).

LVD2RI Bit (Voltage Monitoring 2 Circuit Mode Select)

When the LVD2RI it is 1 (voltage monitoring 2 reset enabled) or when the LVD1CR0.LVD1RI bit is 1 (voltage monitoring 1 reset enabled), a transition to deep software standby mode cannot be made, instead a transition to software standby mode is made. To enter to deep software standby mode, set the LVD2RI bit to 0 (voltage monitoring 2 interrupt enabled) and the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt enabled).

LVD2RN Bit (Voltage Monitoring 2 Reset Negate Select)

If the LVD2RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Furthermore, if a transition to software standby or deep software standby is to be made, the only possible value for the LVD2RN bit is 0 (negation follows a stabilization time after VCC > Vdet2 is detected). Do not set the LVD2RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) when this is the case.

9.3 VCC Input Voltage Monitor

9.3.1 Monitoring Vdet0

Monitoring Vdet0 is not possible.

9.3.2 Monitoring Vdet1

Table 9.2 lists the procedures for setting up monitoring against Vdet1. After the settings are completed, results of comparison by voltage monitoring 1 can be monitored by using the LVD1SR.LVD1MON flag.

Table 9.2 Procedures for Setting up Monitoring against Vdet1

Step	When the Digital Filter is in Use	When the Digital Filter is Not in Use
1	Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	
2	Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits.	Set the LVD1CR0.LVD1DFDIS bit to 1 (disabling the digital filter).
3	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitor 1).	
4	Wait for at least one cycle of the LOCO.	—
5	Clear the LVD1CR0.LVD1DFDIS bit to 0 (enabling the digital filter).	—
6	Wait for at least 2n ? 3 cycles of the LOCO (where n = 1, 2, 4, 8, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	— (waiting is not required)
7	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).	

9.3.3 Monitoring Vdet2

Table 9.3 lists the procedures for setting up monitoring against Vdet2. After the settings are completed, results of comparison by voltage monitoring 2 can be monitored by using the LVD2SR.LVD2MON flag.

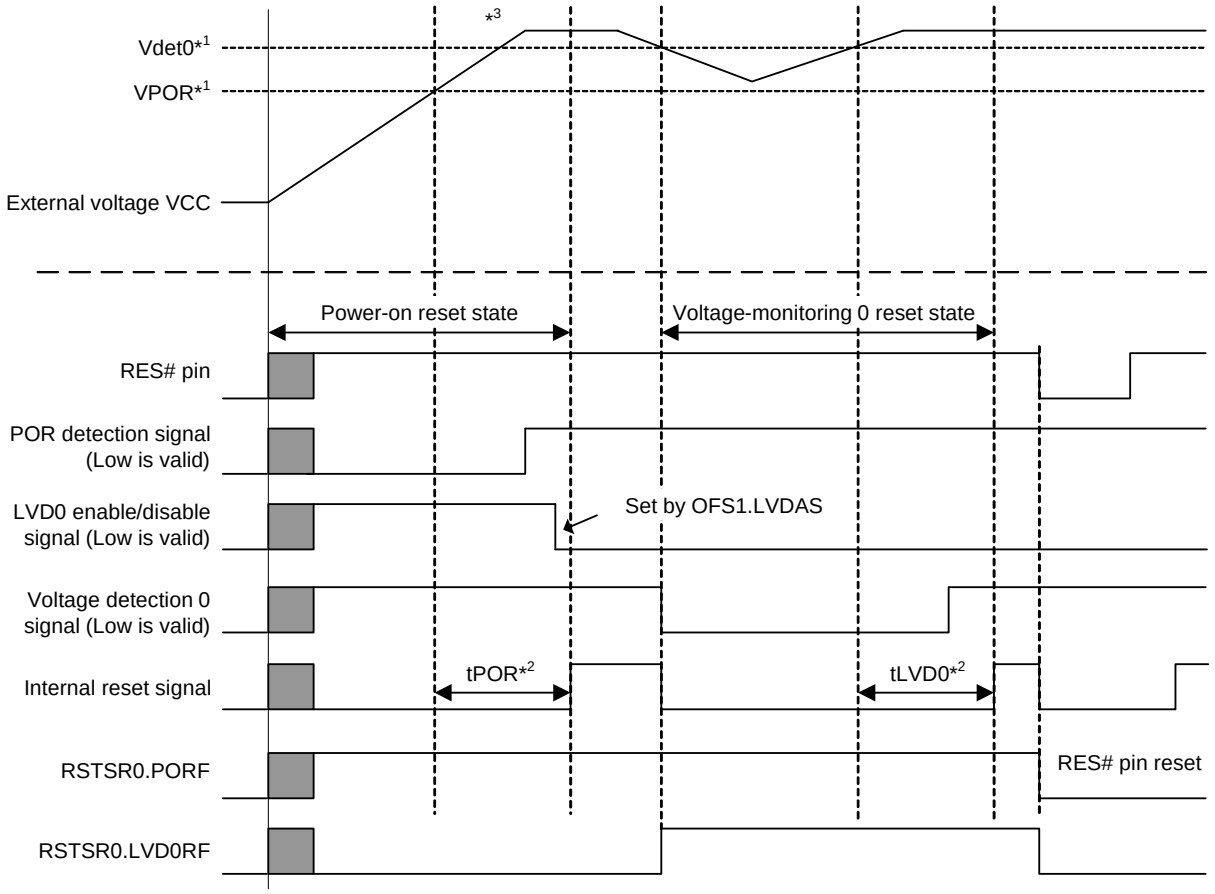
Table 9.3 Procedures for Setting up Monitoring against Vdet2

Step	When the Digital Filter is in Use	When the Digital Filter is Not in Use
1	Specify the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.	
2	Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits.	Set the LVD2CR0.LVD2DFDIS bit to 1 (disabling the digital filter).
3	Set the LVD2CR0.LVD2CMPE bit to 1 (enabling output of the results of comparison by voltage monitor 2).	
4	Wait for at least one cycle of the LOCO.	—
5	Clear the LVD2CR0.LVD2DFDIS bit to 0 (enabling the digital filter).	—
6	Wait for at least 2n ? 3 cycles of the LOCO (where n = 1, 2, 4, 8, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	— (waiting is not required)
7	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).	

9.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the voltage detection 0 circuit start bit (OFS1.LVDAS) to 0 (enabling the voltage monitor 0 reset after a reset).

Figure 9.4 shows an example of operations for a voltage monitoring 0 reset.



Note: • For details of the electrical characteristics, see section 41, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 42, Electrical Characteristics [64- and 48-Pin Versions].

Note 1. VPOR indicates the detection level for a power-on reset and Vdet0 indicates the detection level for a voltage monitor 0 reset.

Note 2. tPOR indicates the period of a power-on reset and tLVD0 indicates the period of a voltage monitor 0 reset.

Note 3. At the time the power-supply voltage rises, VCC must rise to at least the minimum guaranteed voltage before release from the POR reset state.

Figure 9.4 Example of Voltage Monitoring 0 Reset Operation

9.5 Interrupt and Reset from Voltage Monitor 1

Table 9.4 lists the procedures for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring operates. Table 9.5 shows the procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops. Figure 9.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 7.2 in section 7, Resets. Furthermore, set the LVD1CR0.LVD1DFDIS bit to 1 (disabling the digital filter) if you intend to use the voltage monitor 1 circuit in software standby or deep software standby mode.

Table 9.4 Procedures for Setting Bits Related to the Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset so that Voltage Monitoring Operates

	When the Digital Filter is in Use		When the Digital Filter is Not in Use	
Step	**Voltage Monitor 1 Interrupt**	**Voltage Monitor 1 Reset**	**Voltage Monitor 1 Interrupt**	**Voltage Monitor 1 Reset**
1*1	Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.			
2*2	Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits.		Set the LVD1CR0.LVD1DFDIS bit to 1 (disabling the digital filter).	
3 *1, *2	Clear the LVD1CR0.LVD1RI bit to 0 (selecting the voltage monitor 1 interrupt).	• Set the LVD1CR0.LVD1RI bit to 1 (selecting the voltage monitor 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.	Clear the LVD1CR0.LVD1RI bit to 0 (selecting the voltage monitor 1 interrupt).	• Set the LVD1CR0.LVD1RI bit to 1 (selecting the voltage monitor 1 reset). • Select the type of the reset negation by setting the LVD1CR0.LVD1RN bit.
4	Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits.	—	Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits.	—
5	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitor 1).			
6	Wait for at least one cycle of the LOCO.		—	
7	Clear the LVD1CR0.LVD1DFDIS bit to 0 (enabling the digital filter).		—	
8	Wait for at least 2n + 3 cycles of the LOCO (where n = 1, 2, 4, 8, and the sampling clock for the digital filter is the LOCO frequency-divided by n).		— (waiting is not required)	
9	Clear the LVD1SR.LVD1DET flag to 0.	—	Clear the LVD1SR.LVD1DET flag to 0.	—
10	Set the LVD1CR0.LVD1RIE bit to 1 (enabling the voltage monitor 1 interrupt or reset).			
11*1	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).			

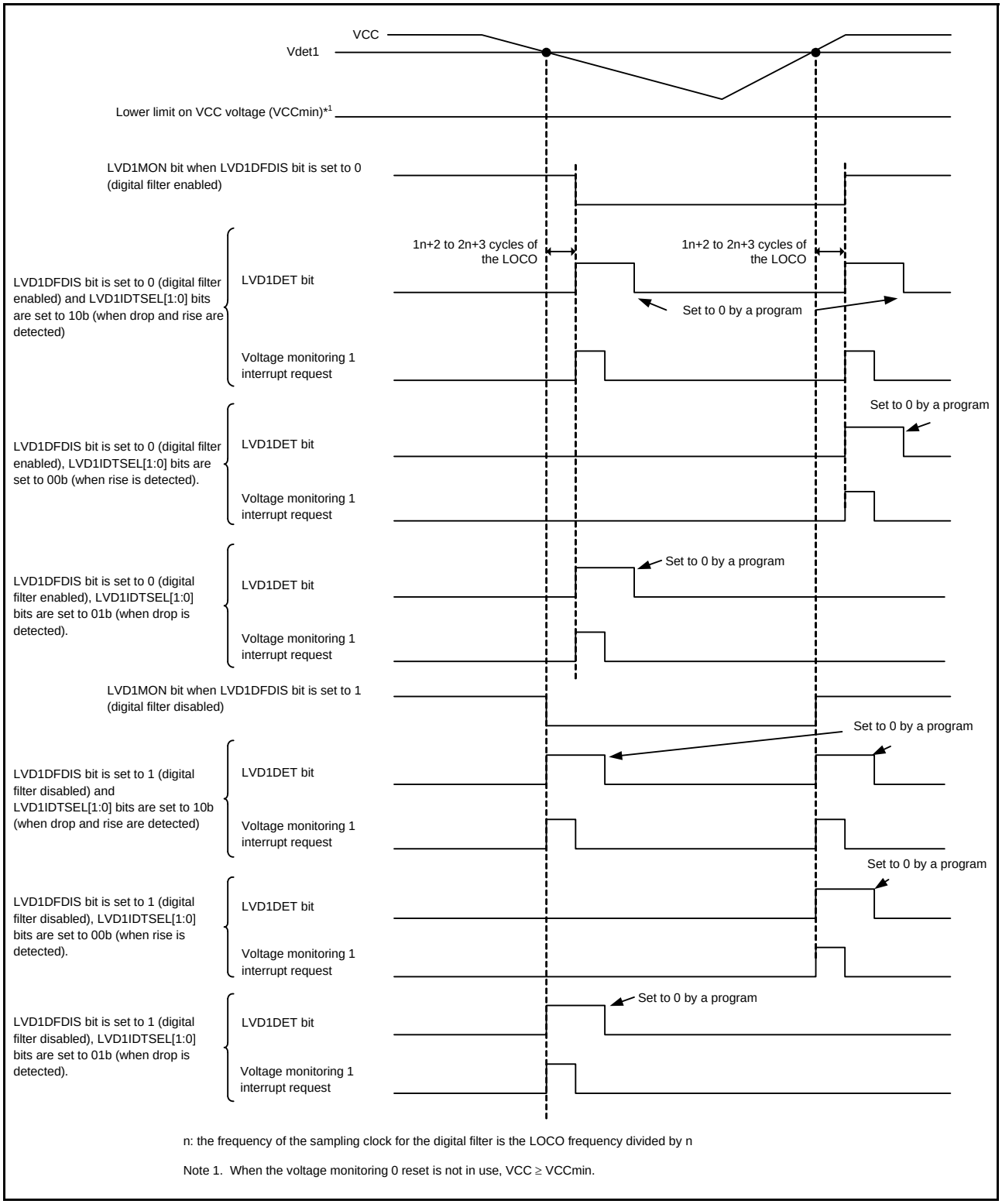
Note 1. Steps 1, 3, and 11 are not required if operation is with the setting to select the voltage monitor 1 interrupt (LVD1CR0.LVD1RI = 0) and operation can be restarted by simply changing the settings of the LVD1CR0.LVD1FSAMP[1:0] and LVD1DFDIS bits or of the LVD1CR1.LVD1IDTSEL[1:0] bits, or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitor 1 reset (LVD1CR0.LVD1RI = 1), proceed through all steps from 1 to 11.

Note 2. Executing steps 2 and 3 at the same time (with a single instruction) creates no problems.

Table 9.5 Procedures for Setting Bits Related to the Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset to Stop Voltage Monitoring

Step	Setting Bits Related to the Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset to Stop Voltage Monitoring
1*1	Clear the LVCMPCR.LVD1E bit to 0 (disabling the voltage detection 1 circuit).
2*1	Wait for at least one cycle of the LOCO.
3	Clear the LVD1CR0.LVD1RIE bit to 0 (disabling the voltage monitor 1 interrupt or reset).
4	Clear the LVD1CR0.LVD1CMPE bit to 0 (disabling output of the results of comparison by voltage monitor 1).
5	Modify settings of bits related to the voltage detection circuit other than the LVCMPCR.LVD1E, LVD1CR0.LVD1CMPE, and LVD1RIE bits.

Note 1. Steps 1 and 2 are not required when operation is with the setting to select the voltage monitor 1 interrupt (LVD1CR0.LVD1RI = 0) and, after it is stopped, operation is to be restarted by simply changing the settings of the LVD1CR0.LVD1FSAMP[1:0] and LVD1DFDIS bits or the LVD1CR1.LVD1IDTSEL[1:0] bits, or when restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitor 1 reset (LVD1CR0.LVD1RI = 1), proceed through all steps from 1 to 5.



n: the frequency of the sampling clock for the digital filter is the LOCO frequency divided by n

Note 1. When the voltage monitoring 0 reset is not in use, VCC ≥ VCCmin.

Figure 9.5 Example of Voltage Monitoring 1 Interrupt Operation

9.6 Interrupt and Reset from Voltage Monitor 2

Table 9.6 shows the procedures for setting bits related to the voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring operates.Table 9.7 shows the procedure for setting bits related to the voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring stops. Figure 9.6 shows an example of operations for a voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 7.2 in section 7, Resets.
Furthermore, set the LVD2CR0.LVD2DFDIS bit to 1 (disabling the digital filter) if you intend to use the voltage monitor 2 circuit in software standby or deep software standby mode.

Table 9.6 Procedures for Setting Bits Related to the Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset so that Voltage Monitoring Operates

	When the Digital Filter is in Use		When the Digital Filter is Not in Use	
Step	**Voltage Monitor 2 Interrupt**	**Voltage Monitor 2 Reset**	**Voltage Monitor 2 Interrupt**	**Voltage Monitor 2 Reset**
1*1	Specify the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.			
2*2	Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits.		Set the LVD2CR0.LVD2DFDIS bit to 1 (disabling the digital filter).	
3 *1,*2	Clear the LVD2CR0.LVD2RI bit to 0 (selecting the voltage monitor 2 interrupt).	• Set the LVD2CR0.LVD2RI bit to 1 (selecting the voltage monitor 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.	Clear the LVD2CR0.LVD2RI bit to 0 (selecting the voltage monitor 2 interrupt).	• Set the LVD2CR0.LVD2RI bit to 1 (selecting the voltage monitor 2 reset). • Select the type of the reset negation by setting the LVD2CR0.LVD2RN bit.
4	Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits.	—	Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits.	—
5	Set the LVD2CR0.LVD2CMPE bit to 1 (enabling output of the results of comparison by voltage monitor 2).			
6	Wait for at least one cycle of the LOCO.		—	
7	Clear the LVD2CR0.LVD2DFDIS bit to 0 (enabling the digital filter).		—	
8	Wait for at least 2n + 3 cycles of the LOCO (where n = 1, 2, 4, 8, and the sampling clock for the digital filter is the LOCO frequency-divided by n).		— (waiting is not required)	
9	Clear the LVD2SR.LVD2DET flag to 0.	—	Clear the LVD2SR.LVD2DET flag to 0.	—
10	Set the LVD2CR0.LVD2RIE bit to 1 (enabling the voltage monitor 2 interrupt or reset).			
11*1	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).			

Note 1. Steps 1, 3, and 11 are not required if operation is with the setting to select the voltage monitor 2 interrupt (LVD2CR0.LVD2RI = 0) and operation can be restarted by simply changing the settings of the LVD2CR0.LVD2FSAMP[1:0] and LVD2DFDIS bits or of the LVD2CR1.LVD2IDTSEL[1:0] bits, or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitor 2 reset (LVD2CR0.LVD2RI = 1), proceed through all steps from 1 to 11.
Note 2. Executing steps 2 and 3 at the same time (with a single instruction) creates no problems.

Table 9.7 Procedures for Setting Bits Related to the Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset to Stop Voltage Monitoring

Step	Setting Bits Related to the Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset to Stop Voltage Monitoring
1*1	Clear the LVCMPCR.LVD2E bit to 0 (disabling the voltage detection 2 circuit).
2*1	Wait for at least one cycle of the LOCO.
3	Clear the LVD2CR0.LVD2RIE bit to 0 (disabling the voltage monitor 2 interrupt or reset).
4	Clear the LVD2CR0.LVD2CMPE bit to 0 (disabling output of the results of comparison by voltage monitor 2).
5	Modify settings of bits related to the voltage detection circuit other than the LVCMPCR.LVD2E, LVD2CR0.LVD2CMPE, and LVD2RIE bits.

Note 1. Steps 1 and 2 are not required when operation is with the setting to select the voltage monitor 2 interrupt (LVD2CR0.LVD2RI = 0) and, after it is stopped, operation is to be restarted by simply changing the settings of the LVD2CR0.LVD2FSAMP[1:0] and LVD2DFDIS bits or the LVD2CR1.LVD2IDTSEL[1:0] bits, or when restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitor 2 reset (LVD1CR0.LVD1RI = 1), proceed through all steps from 1 to 5.

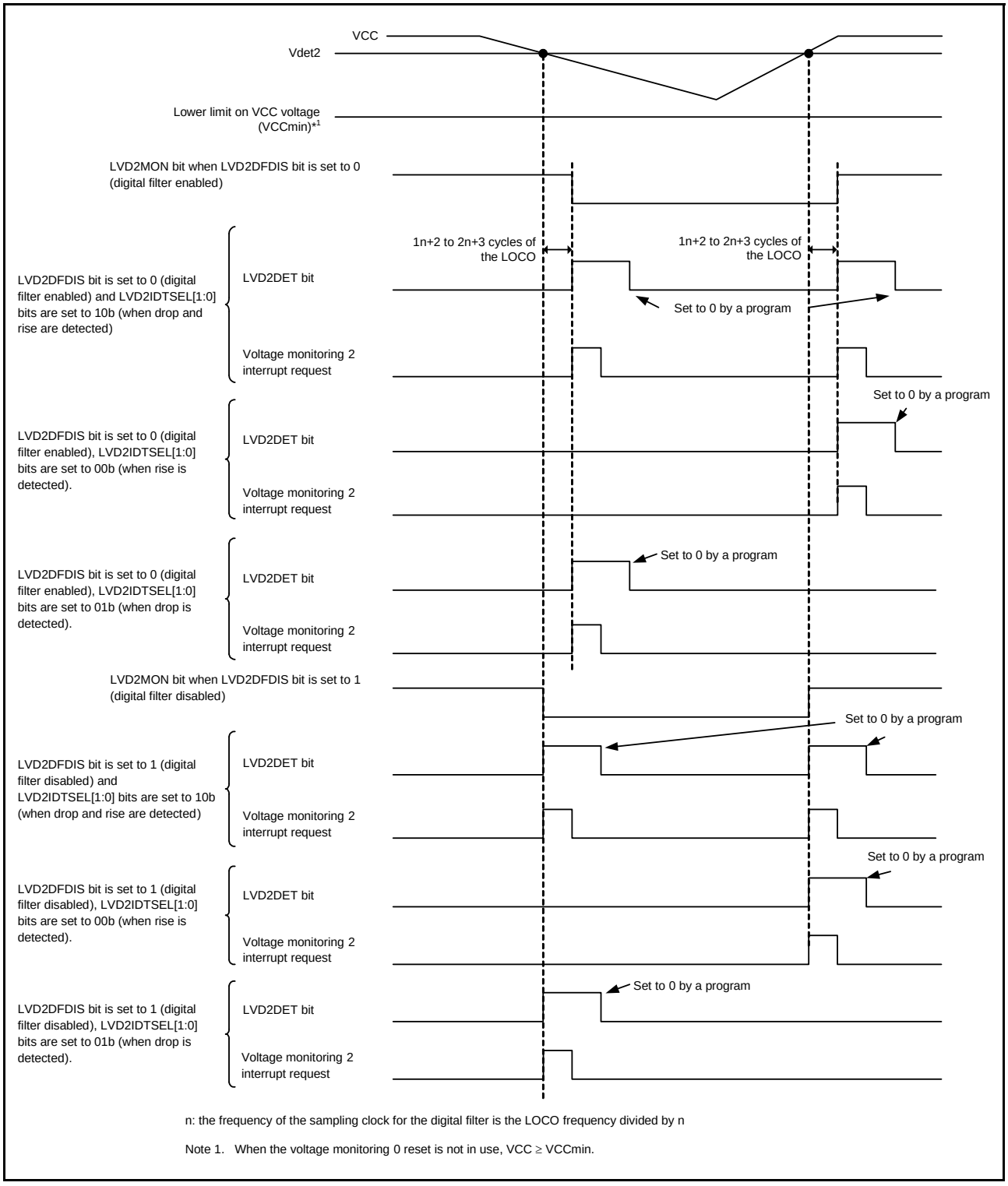


Figure 9.6 Example of Voltage Monitoring 2 Interrupt Operation

10. Clock Generation Circuit

10.1 Overview

This MCU incorporates a clock generation circuit.
Table 10.1 lists the specifications of the clock generation circuit. Figure 10.1 shows a block diagram of the clock generation circuit.

Table 10.1 Specifications of Clock Generation Circuit

Item	Specification
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the MTU3, GPT and DPC.*1 • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral module. • Generates the AD clock (PCLKC) to be supplied to the AD.*1 • Generates the S12AD clock (PCLKD) to be supplied to the S12AD.*1 • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the CAC clock (CACMCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG-dedicated clock (JTAGTCK) to be supplied to the JTAG.
Operating frequency	• ICLK: 100 MHz (max) • PCLKA: 100 MHz (max) • PCLKB: 50 MHz (max) • PCLKC: 100 MHz (max) • PCLKD: 50 MHz (max) • FCLK: 4 MHz to 50 MHz (for programming and erasing the ROM and E2 DataFlash) 50 MHz (max) (for reading from the E2 DataFlash) • BCLK: 50 MHz (max) • BCLK pin output: 50 MHz (max) • UCLK: 48 MHz (max) • CANMCLK: 14 MHz (max) • CACMCLK: Same as the clock from respective oscillators. • IWDTCLK: 125 kHz • JTAGTCK: 10 MHz (max)
Main clock oscillator	• Resonator frequency: [144-, 120-, 112- and 100-pin versions] 8 MHz to 12.5 MHz [64- and 48-pin versions] 4 MHz to 16 MHz • External clock input frequency: [144-, 120-, 112- and 100-pin versions] 14 MHz (max) [64- and 48-pin versions] 20 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU and GPT outputs can be forcedly driven to the high-impedance.
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: [144-, 120-, 112- and 100-pin versions] 8 MHz to 12.5 MHz [64- and 48-pin versions] 4 MHz to 16 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, 25, and 50 • VCO oscillation frequency: 104 MHz to 200 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz
External clock input (TCK) for JTAG	Input clock frequency: 10 MHz (max)
Control of output on the BCLK pin	• BCLK clock output or high-level output is selectable • BCLK or BCLK/2 is selectable

Note 1. In this MCU, PCLKB = PCLK.

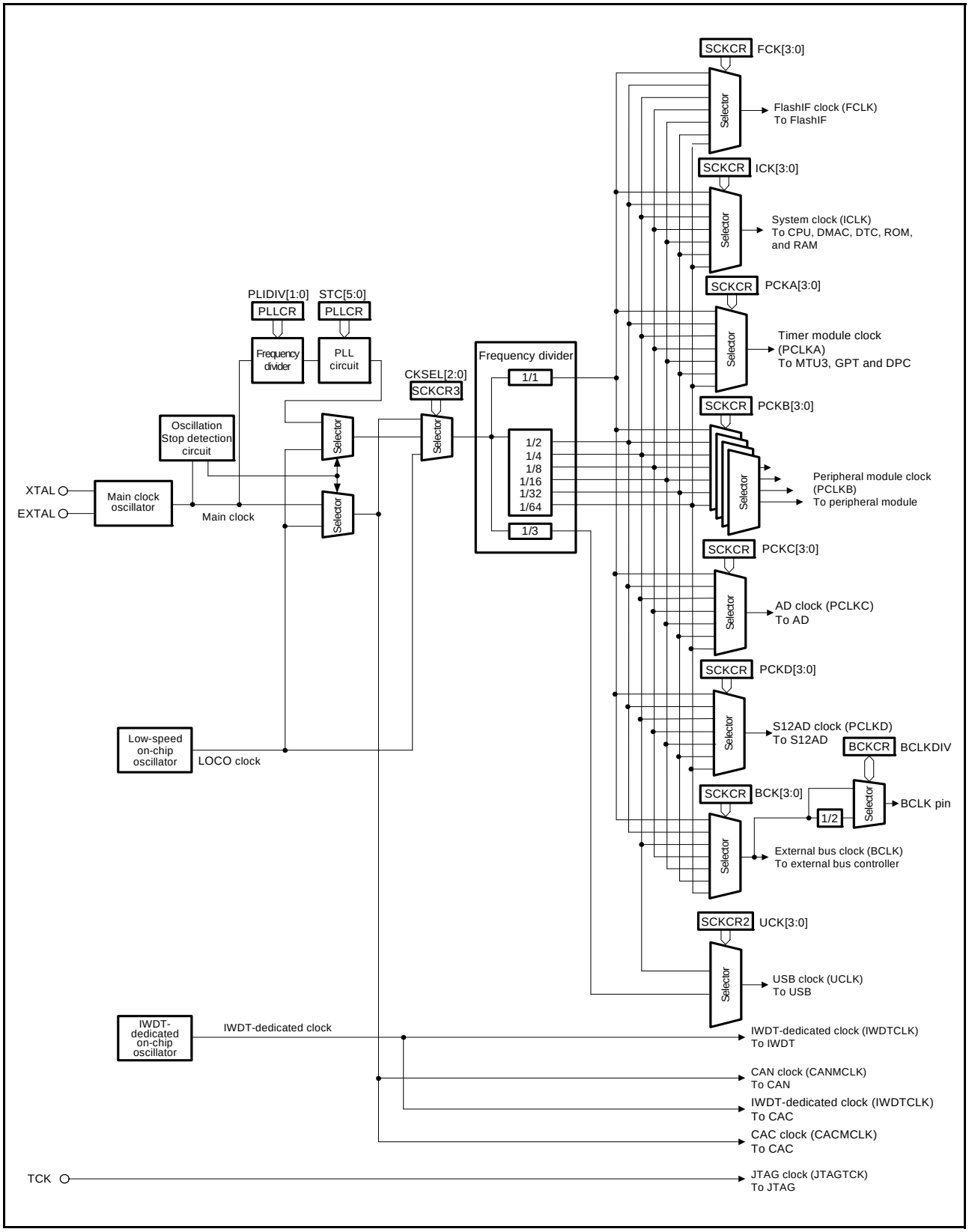


Figure 10.1 Block Diagram of Clock Generation Circuit

Table 10.2 lists the input/output pins of the clock generation circuit.

Table 10.2 Input/Output Pins of Clock Generation Circuit

Pin Name	I/O	Description
XTAL	Output	These pins are used to connect a crystal resonator. The EXTAL pin can also be used to input an external clock. For details, section 10.3.2, External Clock Input.
EXTAL	Input	
TCK	Input	This pin is used to input the clock for the JTAG.
BCLK	Output	This pin is used to supply external devices with the external bus clock (BCLK).

10.2 Register Descriptions

10.2.1 System Clock Control Register (SCKCR)

Address(es): 0008 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FCK[3:0]				ICK[3:0]				PSTOP1	—	—	—	BCK[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PCKA[3:0]				PCKB[3:0]				PCKC[3:0]				PCKD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	PCKD[3:0]	S12AD Clock (PCLKD) Select*1, *6, *10	b11 b8 0 0 0 0: × 1/1 0 0 0 1: × 1/2 0 0 1 0: × 1/4 0 0 1 1: × 1/8 0 1 0 0: × 1/16 0 1 0 1: × 1/32 0 1 1 0: × 1/64 Settings other than above are prohibited.	R/W
b7 to b4	PCKC[3:0]	AD Clock (PCLKC) Select*2, *6, *10, *11	b11 b8 0 0 0 0: × 1/1 0 0 0 1: × 1/2 0 0 1 0: × 1/4 0 0 1 1: × 1/8 0 1 0 0: × 1/16 0 1 0 1: × 1/32 0 1 1 0: × 1/64 Settings other than above are prohibited.	R/W
b11 to b8	PCKB[3:0]	Peripheral Module Clock B (PCLKB) Select*1 to *3, *5, *6, *10	b11 b8 0 0 0 0: × 1/1 0 0 0 1: × 1/2 0 0 1 0: × 1/4 0 0 1 1: × 1/8 0 1 0 0: × 1/16 0 1 0 1: × 1/32 0 1 1 0: × 1/64 Settings other than above are prohibited.	R/W
b15 to b12	PCKA[3:0]	Timer Module Clock (PCLKA) Select*4 to *6, *10	b15 b12 0 0 0 0: × 1/1 0 0 0 1: × 2 0 0 1 0: × 4 0 0 1 1: × 8 0 1 0 0: × 16 0 1 0 1: × 32 0 1 1 0: × 64 Settings other than those listed above are prohibited.	R/W
b19 to b16	BCK[3:0]	External Bus Clock (BCLK) Select*6 to *8, *10, *11	b19 b16 0 0 0 0: × 1/1 0 0 0 1: × 1/2 0 0 1 0: × 1/4 0 0 1 1: × 1/8 0 1 0 0: × 1/16 0 1 0 1: × 1/32 0 1 1 0: × 1/64 Settings other than above are prohibited.	R/W
b22 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b23	PSTOP1	BCLK Pin Output Control*8	0: BCLK pin output is enabled. 1: BCLK pin output is disabled. (Fixed high)	R/W
b27 to b24	ICK[3:0]	System Clock (ICLK) Select*3, *4,*6, *7, *9, *10	b27 b24 0 0 0 0: × 1/1 0 0 0 1: × 1/2 0 0 1 0: × 1/4 0 0 1 1: × 1/8 0 1 0 0: × 1/16 0 1 0 1: × 1/32 0 1 1 0: × 1/64 Settings other than above are prohibited.	R/W
b31 to b28	FCK[3:0]	FlashIF Clock (FCLK) Select*6, *9, *10	b31 b28 0 0 0 0: × 1/1 0 0 0 1: × 1/2 0 0 1 0: × 1/4 0 0 1 1: × 1/8 0 1 0 0: × 1/16 0 1 0 1: × 1/32 0 1 1 0: × 1/64 Settings other than above are prohibited.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKD = N:1, where N is an integer.
Note 2. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKC = N:1 or 1:N, where N is an integer.
Note 3. Make a setting such that the frequencies satisfy the relation ICLK:PCLKB = N:1 or 1:N, where N is an integer.
Note 4. Make a setting such that the frequencies satisfy the relation ICLK:PCLKA = N:1 or 1:N, where N is an integer.
Note 5. Make a setting such that the frequencies satisfy the relation PCLKA:PCLKB = N:1, where N is an integer.
Note 6. The setting for division by one is prohibited if the PLL is selected.
Note 7. Do not make a setting such that the ICLK runs at a lower frequency than the external bus clock.
Note 8. When operation of the external bus clock is selected, the PE5 I/O port pin function is not available because it is multiplexed on the same pin as the BCLK pin function.
Note 9. Make a setting such that the frequencies satisfy the relation ICLK:FCLK = N:1 or 1:N, where N is an integer.
Note 10. The setting for division by one or two is prohibited if the SCKCR3.CKSEL[2:0] bits are set to 010b (the main clock oscillator is selected)
Note 11. In 64- and 48-pin products, set the same value as the highest division ratio among the settings of the ICK[3:0] and PCKB[3:0] bits.

SCKCR should not be modified in the following cases:

- The ROM P/E mode entry bit 0 in the flash P/E mode entry register (FENTRYR.FENTRY0) is 1 (ROM P/E mode)
- Time period from WAIT instruction issuance for a transition to sleep mode, to return from sleep mode to normal operating mode

10.2.2 System Clock Control Register 2 (SCKCR2)

Address(es): 0008 0024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	UCK[3:0]				—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0001. The write value should be 0001.	R/W
b7 to b4	UCK[3:0]	USB Clock (UCLK) Select	b7 b4 0 0 0 1: × 1/2 0 0 1 0: × 1/3 0 0 1 1: × 1/4 Settings other than above are prohibited when USB is in use. When USB is not in use, these bits are read as 0001b. The write value should be 0001b.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

SCKCR2 should not be modified in the following cases:

- The ROM P/E mode entry bit 0 in the flash P/E mode entry register (FENTRYR.FENTRY0) is 1 (ROM P/E mode)
- Time period from WAIT instruction issuance for a transition to sleep mode, to return from sleep mode to normal operating mode

UCK[3:0] Bits (USB Clock (UCLK) Select)

These bits select the frequency of the USB clock (UCLK).
The duty ratio is 2:1 when × 1/3 is selected.

10.2.3 System Clock Control Register 3 (SCKCR3)

Address(es): 0008 0026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CKSEL[2:0]	Clock Source Select	b10 b8 0 0 0: LOCO 0 1 0: Main clock oscillator 1 0 0: PLL circuit Settings other than above are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

SCKCR3 should not be modified in the following cases:

- The ROM P/E mode entry bit 0 in the flash P/E mode entry register (FENTRYR.FENTRY0) is 1 (ROM P/E mode)
- Time period from WAIT instruction issuance for a transition to sleep mode, to return from sleep mode to normal operating mode

CKSEL[2:0] Bits (Clock Source Select)

These bits select the source of the system clock (ICLK), timer module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), S12AD clock (PCLKD), FlashIF clock (FCLK), external bus clock (BCLK), and USB clock (UCLK) from low-speed on-chip oscillator (LOCO), the main clock oscillator, and the PLL circuit.
Transitions to clock sources which are not in operation are prohibited.

10.2.4 PLL Control Register (PLLCR)

Address(es): 0008 0028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	STC[5:0]						—	—	—	—	—	—	PLIDIV[1:0]	
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select	b1 b0 0 0: × 1 0 1: × 1/2 1 0: × 1/4 1 1: Setting prohibited	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	STC[5:0]	Frequency Multiplication Factor Select	b13 b8 0 0 0 1 1 1: × 8 0 0 1 0 0 1: × 10 0 0 1 0 1 1: × 12 0 0 1 1 1 1: × 16 0 1 0 0 1 1: × 20 0 1 0 1 1 1: × 24 0 1 1 0 0 0: × 25 1 1 0 0 0 1: × 50 Settings other than above are prohibited.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Writing to the PLLCR is prohibited when the PLLCR2.PLLEN bit is 0 (the PLL operates).

PLIDIV[1:0] Bits (PLL Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL clock source.

Set these bits so that the frequency of PLL input signal is within the range of 8 to 12.5 MHz in 144-, 120-, 112-, and 100-pin products, and 4 to 16 MHz in 64- and 48-pin products.

STC[5:0] Bits (Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL circuit.

Set these bits so that the output frequency is within the range of the VCO oscillation frequency for the PLL (104 MHz to 200 MHz).

10.2.5 PLL Control Register 2 (PLLCR2)

Address(es): 0008 002Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PLLEN
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	PLLEN	PLL Stop Control	0: PLL is operating. 1: PLL is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Only set this register after setting the PLL wait control register according to the procedure in section 12, Low Power Consumption.

PLLEN Bit (PLL Stop Control)

This bit runs or stops the PLL circuit.
After the setting of the PLLEN bit has been changed so that the PLL operates, only start using the PLL clock after the PLL clock oscillation stabilization waiting time (tPLLWT1 or tPLLWT2) has elapsed.
That is, a fixed time for stabilization is required after the setting for PLL operation. A fixed time is also required for oscillation to stop after the setting to stop PLL operation. Accordingly, take note of the following limitations when starting and stopping PLL operation.

- When restarting the PLL after it has been stopped, allow at least five cycles of the PLL clock as an interval over which it is still stopped.
- Ensure that oscillation by the PLL is stable when making the setting to stop the PLL.
- Regardless of whether or not it is selected as the system clock, ensure that oscillation by the PLL is stable before executing a WAIT instruction to place the chip on software standby or deep software standby.
- When a transition to software standby or deep software standby is to follow the setting to stop the PLL, wait for at least two cycles of the PLL clock before executing the WAIT instruction.

Writing of 1 to the PLLEN bit (stopping the PLL) is prohibited while the PLL clock is selected by the clock source select bits in system clock control register 3 (SCKCR3.CKSEL[2:0]).

10.2.6 External Bus Clock Control Register (BCKCR)

Address(es): 0008 0030h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCLKDIV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCLKDIV	BCLK Pin Output Select	0: BCLK 1: 1/2 BCLK	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

BCKCR should not be modified in the following cases:

- The ROM P/E mode entry bit 0 in the flash P/E mode entry register (FENTRYR.FENTRY0) is 1 (ROM P/E mode)
- Time period from WAIT instruction issuance for a transition to sleep mode, to return from sleep mode to normal operating mode

BCLKDIV Bit (BCLK Pin Output Select)

This bit selects the clock signal for output from the BCLK pin.
Either the BCLK clock with the frequency selected by the BCK[3:0] bits in SCKCR or the BCLK clock divided by 2 can be selected.

10.2.7 Main Clock Oscillator Control Register (MOSCCR)

Address(es): 0008 0032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	MOSTP	Main Clock Oscillator Stop	0: Main clock oscillator is operating. 1: Main clock oscillator is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Only set this register after setting the main clock oscillator wait control register according to the procedure in section 12, Low Power Consumption.

MOSTP Bit (Main Clock Oscillator Stop)

This bit runs or stops the main clock oscillator.

The main clock oscillator is operated or stopped by the MOSTP bit and main clock oscillator forced oscillation bit in the main clock oscillator forced oscillation control register (MOFCR.MOFXIN). The main clock oscillator can be started by setting the MOSTP bit to operating or by setting the MOFXIN bit to forced oscillation. When the MOFXIN bit is set to forced oscillation, the oscillator operates even in deep software standby mode.

When changing the value of the MOSTP bit or MOFCR.MOFXIN bit, execute subsequent instructions after reading the bit and checking that its value has actually been updated (refer to (2) Notes on writing to I/O registers, in section 6, I/O Registers).

When a crystal oscillator is connected to supply the main clock signal, after changing the MOSTP bit or MOFCR.MOFXIN bit so that the main clock oscillator operates, only use the main clock after the main clock oscillation stabilization waiting time (crystal; tMAINOSCWT) has elapsed.

When an external clock is connected to supply the main clock signal, after changing the MOSTP bit or MOFCR.MOFXIN bit so that the main clock oscillator operates, only use the main clock after the EXTAL external clock input waiting time (tEXWT) has elapsed.

For the main clock oscillator, a fixed time is required for oscillation to become stable after the settings for operation have been made. Furthermore, a fixed time is required for oscillation to actually stop after the settings to stop oscillation have been made. Accordingly, take note of the following limitations when starting and stopping PLL operation.

- When restarting the main clock after it has been stopped, allow at least five cycles of the main clock as an interval over which it is still stopped.
- Ensure that oscillation by the main clock oscillator is stable when making the setting to stop the main clock oscillator.
- Regardless of whether or not it is selected as the system clock, ensure that oscillation by the main clock oscillator is stable before executing a WAIT instruction to place the chip on software standby or deep software standby.
- When a transition to software standby or deep software standby is to follow the setting to stop the main clock oscillator, wait for at least two cycles of the main clock before executing the WAIT instruction.

Writing of 1 to the MOSTP bit (stopping the main clock oscillator) is prohibited while the main clock oscillator or PLL is selected by the clock source select bits in system clock control register 3 (SCKCR3.CKSEL[2:0]).

10.2.8 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

Address(es): 0008 0034h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LCSTP	LOCO Stop	0: LOCO is operating. 1: LOCO is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

LCSTP Bit (LOCO Stop)

This bit runs or stops the LOCO.

After the setting of the LCSTP bit has been changed so that the LOCO operates, only start using the LOCO after the LOCO clock oscillation stabilization waiting time (tLOCOWT) has elapsed.

That is, a fixed time for stabilization of oscillation is required after the setting for LOCO operation. A fixed time is also required for oscillation to stop after the setting to stop the oscillator. Accordingly, take note of the following limitations when starting and stopping the oscillator.

- When restarting the LOCO after it has been stopped, allow at least five cycles of the LOCO as an interval over which it is still stopped.
- Ensure that oscillation by the LOCO is stable when making the setting to stop the LOCO.
- Regardless of whether or not it is selected as the system clock, ensure that oscillation by the LOCO is stable before executing a WAIT instruction to place the chip on software standby or deep software standby.
- When a transition to software standby or deep software standby is to follow the setting to stop the LOCO, wait for at least three cycles of the LOCO after the setting to stop the LOCO and before executing the WAIT instruction.

Writing of 1 to the LCSTP bit (stopping the LOCO) is prohibited while the LOCO is selected by the clock source select bits in system clock control register 3 (SCKCR3.CKSEL[2:0]).

Writing of 1 to the LCSTP bit (stopping the LOCO) is prohibited if detection of oscillation stopping is enabled by the oscillation-stop detection-enable bit in the oscillation stop detection control register (OSTDCR.OSTDE).

10.2.9 IWDT-Dedicated On-Chip Oscillator Control Register (ILOCOCR)

Address(es): 0008 0035h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ILCSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	ILCSTP	IWDT-Dedicated On-Chip Oscillator	0: IWDT-Dedicated On-Chip Oscillator is operating. 1: IWDT-Dedicated On-Chip Oscillator is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

When the IWDT start mode select bit in the option function select register 0 (OFS0.IWDTSTRT) is 0 (IWDT operating), the setting of this register is invalid; it is valid only when the OFS0.IWDTSTRT bit is set to 1 (IWDT stopped). The ILCSTP bit cannot be changed from 0 (IWDT-dedicated on-chip oscillator operating) to 1 (IWDT-dedicated on-chip oscillator stopped) while ILOCOCR is valid.

ILCSTP Bit (IWDT-Dedicated On-Chip Oscillator Stop)

This bit runs or stops the IWDT-dedicated on-chip oscillator.

After the setting of the ILCSTP bit has been changed so that the IWDT-dedicated on-chip oscillator operates, supply of the clock within the LSI only starts after a time of waiting for stabilization of the LOCO (tLOCOWT) has elapsed. If the IWDT-dedicated clock is to be used, only start using the oscillator after this waiting time (tLOCOWT) has elapsed. Ensure that oscillation by the IWDT-dedicated on-chip oscillator is stable before executing a WAIT instruction to place the chip on software standby or deep software standby.

10.2.10 Oscillation Stop Detection Control Register (OSTDCR)

Address(es): 0008 0040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	0: The oscillation stop detection interrupt is disabled. Oscillation stop detection is not notified to the POE. 1: The oscillation stop detection interrupt is enabled. Oscillation stop detection is notified to the POE.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	0: Oscillation stop detection function is disabled. 1: Oscillation stop detection function is enabled.	R/W

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

OSTDIE Bit (Oscillation Stop Detection Interrupt Enable)

If the oscillation-stop detection flag in the oscillation-stop detection status register (OSTDSR.OSTDF) requires clearing, do this after clearing the OSTDIE bit to 0. Wait for at least two cycles of PCLKB before again setting the OSTDIE bit to 1. According to the number of cycles for access to read out a given I/O register, waiting time longer than two cycles of PCLKB may have to be secured.

OSTDE Bit (Oscillation Stop Detection Function Enable)

This bit enables or disables the oscillation stop detection function.

When the OSTDE bit is 1 (oscillation stop detection function enabled), the LOCO stop bit (LOCOCR.LCSTP) is cleared to 0 and the LOCO operation is started. The LOCO cannot be stopped while the oscillation stop detection function is enabled; writing 1 to the LOCOCR.LCSTP bit (LOCO stopped) is invalid.

When the oscillation stop detection flag in the oscillation stop detection status register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

When the OSTDE bit is 1, a transition cannot be made to software standby mode or deep software standby mode. To make a transition to software standby mode or deep software standby mode, execute the WAIT instruction with the OSTDE bit being 0.

10.2.11 Oscillation Stop Detection Status Register (OSTDSR)

Address(es): 0008 0041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OSTDF	Oscillation Stop Detection Flag	0: The main clock oscillation stop has not been detected. 1: The main clock oscillation stop has been detected.	R(/W) *1
b7 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

Note: • Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes 3 system clock cycles for the bit to be read as 0.

OSTDF Flag (Oscillation Stop Detection Flag)

This bit is a flag to indicate the main clock status. When the OSTDF flag is 1, it indicates that the main clock oscillation stop has been detected.

Once the main clock oscillation stop is detected, the OSTDF bit is not cleared to 0 even though the main clock oscillation is restarted. The OSTDF bit is cleared to 0 by reading 1 from the bit and then writing 0. At least 3 ICLK cycles of wait time is necessary between writing 0 to OSTDF and reading OSTDF as 0. If the OSTDF bit is cleared to 0 while the main clock oscillation is stopped, the OSTDF bit becomes 0 and then returns to 1.

When the main clock oscillator or PLL is selected by the clock source select bits in system clock control register 3 (SCKCR3.CKSEL[2:0]) (010b or 100b), the OSTDF bit cannot be modified to 0. The OSTDF bit should be set to 0 after switching the clock source to other sources than the main clock oscillator and PLL.

[Setting condition]

- The main clock oscillation is stopped with the OSTDCR.OSTDE being 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKCR3.CKSEL[2:0] bits are neither 010b nor 100b.

10.2.12 Main Clock Oscillator Forced Oscillation Control Register (MOFCR)

Address(es): 0008 C293h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOFXIN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MOFXIN	Main Clock Oscillator Forced Oscillation	0: Oscillator is not controlled by this bit. 1: The main clock oscillator is forcedly oscillated.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

MOFXIN Bit (Main Clock Oscillator Forced Oscillation)

This bit controls forced oscillation of the main clock oscillator.

When changing the value of the MOSCCR.MOSTP bit or MOFXIN bit, execute subsequent instructions after reading the bit and checking that its value has actually been updated (refer to (2) Notes on writing to I/O registers, in section 6, I/O Registers).

10.3 Main Clock Oscillator

There are two ways of supplying the clock signal to the main clock oscillator: connecting an oscillator or the input of an external clock signal.

10.3.1 Connecting a Crystal Resonator

Figure 10.2 shows an example of connecting a crystal resonator.

A damping resistor Rd should be added, if necessary. Since the resistor values vary depending on the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If use of an external feedback resistor (Rf) is directed by the resonator manufacturer, insert an Rf between EXTAL and XTAL by following the instruction.

When connecting a resonator to supply the clock, the frequency of the resonator should be in the frequency range of the resonator for the main clock oscillator described in Table 10.1.

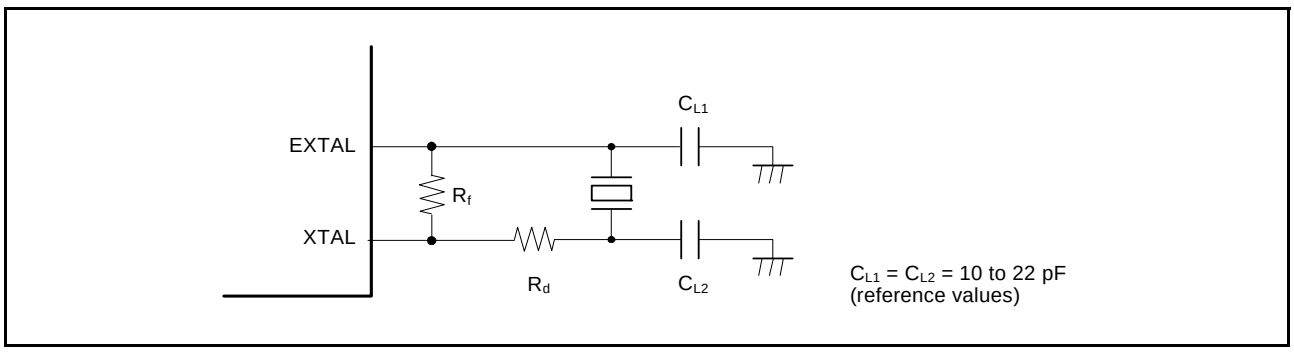


Figure 10.2 Example of Crystal Resonator Connection

Table 10.3 Damping Resistance (Reference Values)

Frequency (MHz)	8	10	12.5
Rd (Ω)	200	100	0

Figure 10.3 shows an equivalent circuit of the crystal resonator. Use a crystal resonator that has the characteristics shown in Table 10.4.

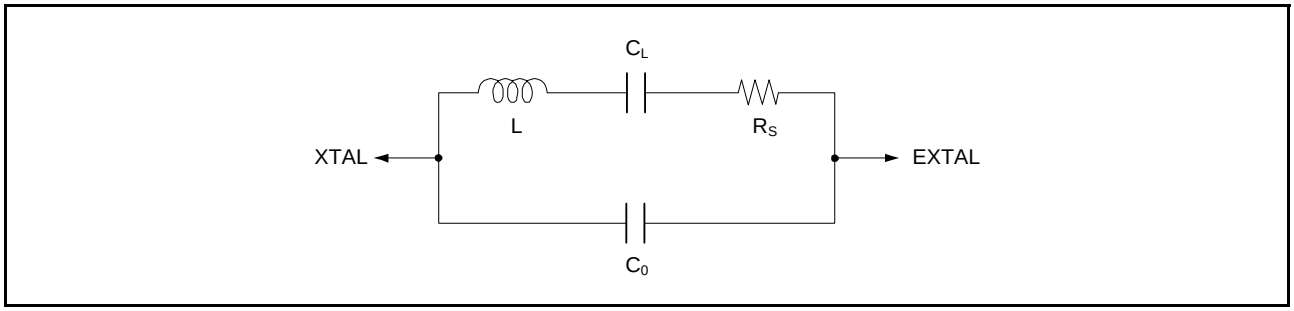


Figure 10.3 Equivalent Circuit of Crystal Resonator

Table 10.4 Crystal Resonator Characteristics (Reference Values)

Frequency (MHz)	8	10	12.5
R_S max (Ω)	80	70	60
C_0 max (pF)		7	

10.3.2 External Clock Input

Figure 10.4 shows examples of connection of external clock input. To leave the XTAL pin open, make the parasitic capacitance less than 5 pF.

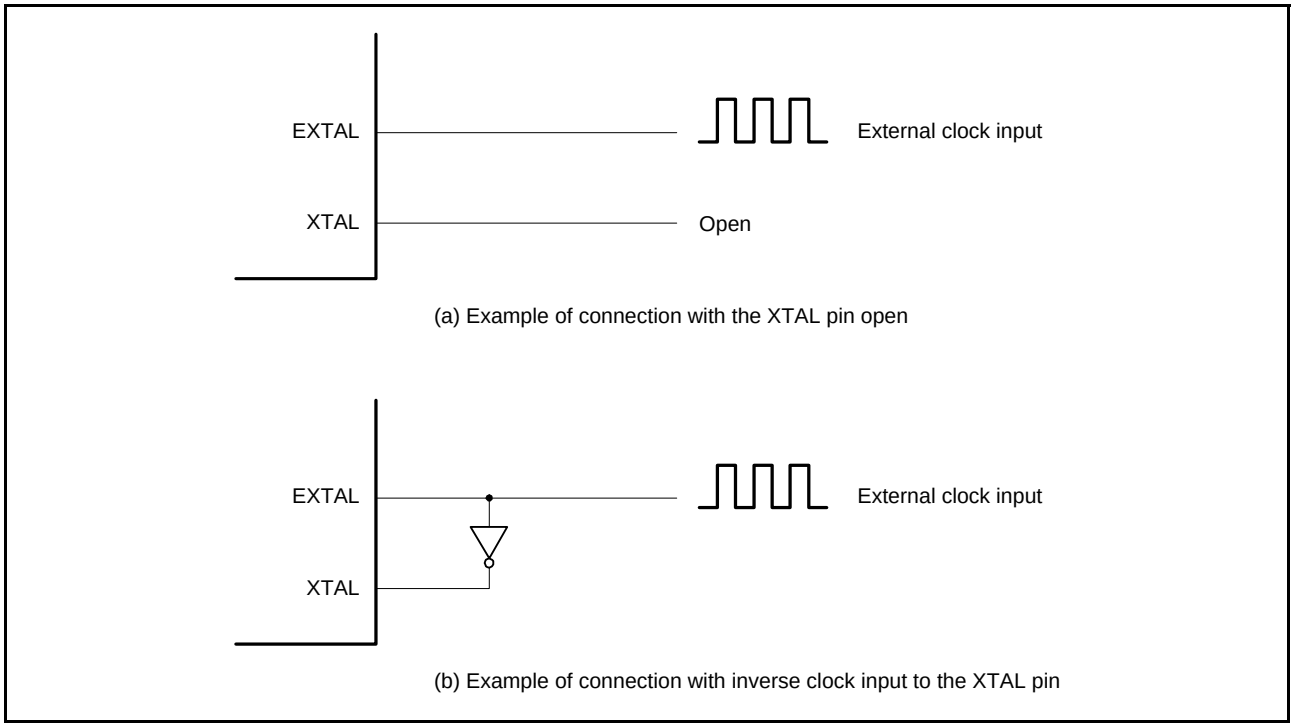


Figure 10.4 Equivalent Circuit for Crystal Resonator

10.3.3 Notes on the External Clock Input

The frequency of the external clock input can only be changed while the main clock oscillator is stopped. Do not change the frequency of the external clock input while the setting of the main clock oscillator stop bit (MOSCCR.MOSTP) is 0 (making the main clock oscillator run) or that of the main clock oscillator forced oscillation bit (MOFCR.MOFXIN) is 1 (forcing the main clock oscillator to run).

10.4 Oscillation Stop Detection Function

10.4.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function is used to detect the main clock oscillator stop and to supply LOCO clock pulses from the low-speed on-chip oscillator as the system clock source instead of the main clock or PLL clock.
An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the MTU output can be forcedly driven to the high-impedance on the detection. For details, see section 22, Multi-Function Timer Pulse Unit 3 (MTU3) and section 23, Port Output Enable 3 (POE3).
In this MCU, the main clock oscillation stop is detected when the input clock remains to be 0 or 1 for a certain period, for example, due to a malfunction of the main clock oscillator (see Table 42.28 Oscillation Stop Detection Circuit Characteristics or Table 43.19 Oscillation Stop Detection Circuit Characteristics).
When an oscillation stop is detected, the main clock or PLL clock selected by the clock source select bits (SCKCR3.CKSEL[2:0]) is switched to the LOCO clock by the corresponding selectors in the former stage. Therefore, if an oscillation stop is detected with the main clock or PLL clock selected as the system clock source, the system clock source is switched to the LOCO clock without a change of CKSEL[2:0].
Switching between the main clock and LOCO clock or between the PLL clock and LOCO clock is controlled by the oscillation stop detection flag (OSTDSR.OSTDF). The clock source is switched to the LOCO clock when the OSTDF flag is 1, and is switched to the main clock or PLL clock again when the OSTDF flag is cleared to 0. At this time, if the main clock or PLL clock is selected with the CKSEL[2:0] bits, the OSTDF flag cannot be cleared to 0. To switch the clock source to the main clock or PLL clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock or PLL clock and clear the OSTDF flag to 0. After that, check that the OSTDF flag is not 1, and then set the CKSEL[2:0] bits to the main clock or PLL clock after the specified oscillation settling time has elapsed.
After a reset is released, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation settling time has elapsed.
The oscillation stop detection function is provided against the main clock stop by an external cause. Therefore, the oscillation stop detection function should be disabled before the main clock oscillator is stopped by the software or a transition is made to software standby mode or deep software standby mode.
The clocks that are switched to the LOCO clock by the oscillation stop detection are: the main clock, PLL clock, CAN clock (CANMCLK), and CAC main clock (CACMCLK), which are provided as the system clock sources.
The system clock (ICLK) frequency during the low-speed clock operation is specified by the LOCO oscillation frequency and the division ratio set by the system clock select bits (SCKCR.ICK[3:0])

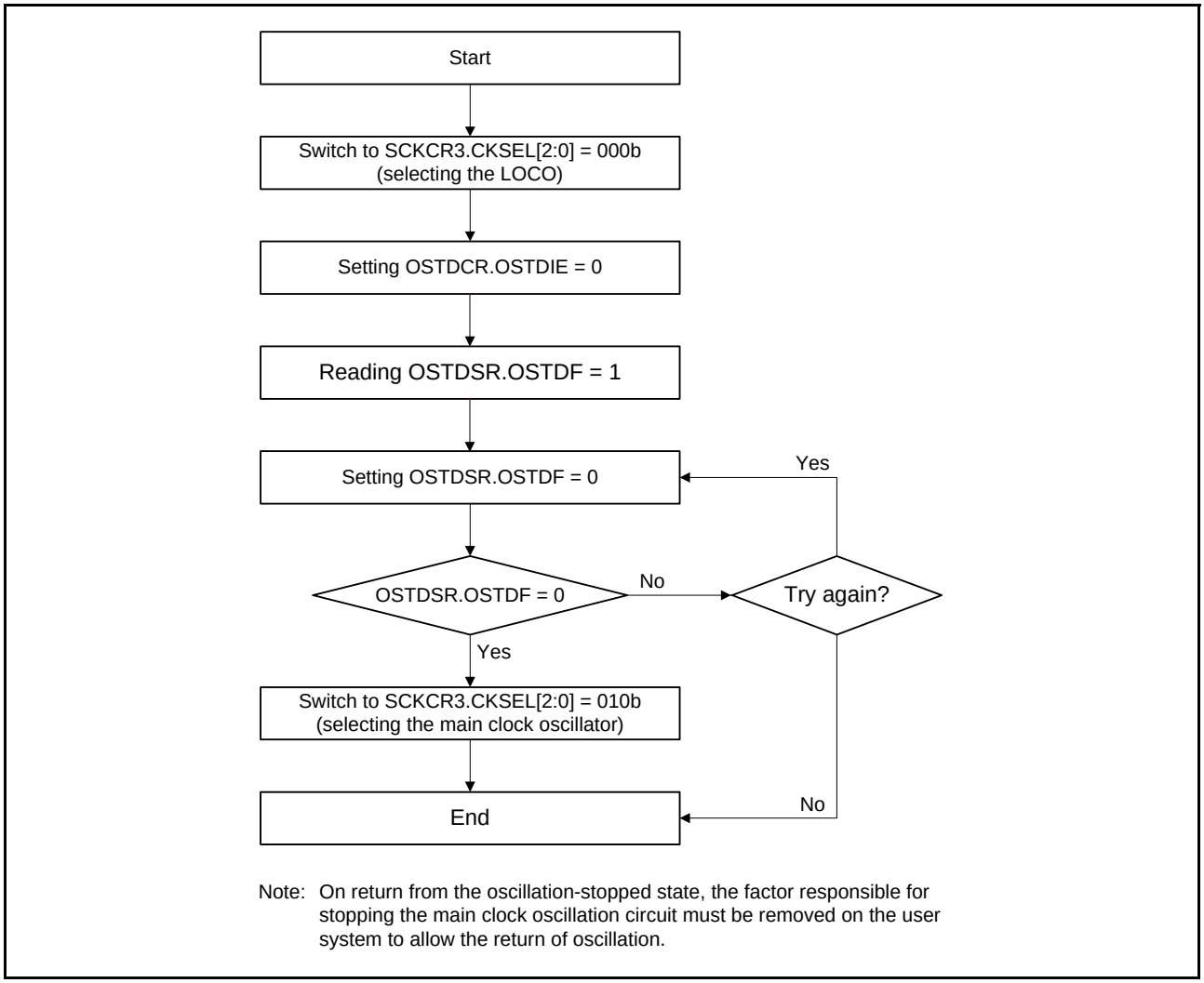


Figure 10.5 Flow of Recovery from Detection of Oscillator Stop

10.4.2 Oscillation Stop Detection Interrupts

An oscillation-stop detection interrupt (OSTDI) will be generated if the oscillation-stop detection flag (OSTDSR.OSTDF) becomes 1 while the oscillation-stop detection interrupt enable bit in the oscillation stop detection control register (OSTDCR.OSTDIE) is 1 (enabling interrupt generation on oscillation stop detection). At this time, the main clock oscillator stop is notified to the port output enable 23 (POE3). On accepting the notification of the oscillation stop, the POE3 sets the OSTST high-impedance flag in input level control/status register 3 (ICSR3.OSTSTF) to 1. After the oscillation stop is detected, wait for at least 10 cycles of PCLK before writing to this ICSR3.OSTSTF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the oscillation-stop detection interrupt enable bit in the oscillation stop detection control register (OSTDCR.OSTDIE). Wait for at least two cycles of PCLKB clock before again setting the OSTDCR.OSTDIE bit to 1. According to the number of cycles for access to read out a given I/O register, waiting time longer than two cycles of PCLKB may have to be secured.

The oscillation stop detection interrupt is a non-maskable interrupt. Since non-maskable interrupts are disabled in the initial state after a reset release, enable the non-maskable interrupts by the software before using oscillation stop detection interrupts. For details, see section 15, Interrupt controller (ICUb).

10.5 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

10.6 Internal Clock

Clock sources of internal clock signals are the main clock, LOCO clock, PLL clock, dedicated clock for the IWDT, and the external clock for JTAG. The internal clocks listed below are produced from these sources.

(1) Operating clock of the CPU, DMAC, DTC, ROM, and RAM: System clock (ICLK)
(2) Operating clock for the timer modules: Timer-module clock (PCLKA)
(3) Operating clock of peripheral modules: Peripheral module clock (PCLKB)
(4) Operating clock for the AD: AD clock (PCLKC)
(5) Operating clock for the S12AD: S12AD clock (PCLKD)
(6) Operating clock of the FlashIF: FlashIF clock (FCLK)
(7) Clock for the external bus controller and external pin output: External bus clock (BCLK)
(8) Operating clock for the USB: USB clock (UCLK)
(9) Operating clock for the CAN: CAN clock (CANMCLK)
(10) Operating clock for the CAC module: CAC clock (CACMCLK)
(11) Operating clock for the IWDT: IWDT-dedicated clock (IWDTCLK)
(12) Operating clock for the JTAG: JTAG clock (JTAGTCK)

Frequencies of the internal clocks are set by the combination of the divisors selected by the FCK[3:0], ICK[3:0], BCK[3:0], PCKA[3:0], PCKB[3:0], PCKC[3:0], and PCKD[3:0] bits in SCKCR, the UCK[3:0] bits in SCKCR2, the clock source selected by the CKSEL[2:0] bits in SCKCR3, and the bits that select the frequency of the PLL circuit (STC[5:0] and PLIDIV[1:0] in PLLCR). If the value of any of these bits is changed, subsequent operation will be at the frequency determined by the new value.

10.6.1 System Clock

The system clock (ICLK) is used as the operating clock of the CPU, DMAC, DTC, ROM, and RAM.
The ICLK frequency is specified by the ICK[3:0] bits in SCKCR, the CKSEL[2:0] bits in SCKCR3, and the STC[5:0] and PLIDIV[1:0] bits in PLLCR.

10.6.2 Timer-Module Clock

The timer-module clock (PCLKA) refers to the clock for the timer modules.
The settings of the SCKCR.PCKA[3:0], SCKCR3.CKSEL[2:0], PLLCR.STC[5:0], and PLIDIV[1:0] bits determine the frequency of the PCLKA.

10.6.3 Peripheral Module Clock

The peripheral module clock (PCLKB) is the operating clocks for use by peripheral modules.
The PCLKB frequencies are specified by the PCKB[3:0] bits in SCKCR, the CKSEL[2:0] bits in SCKCR3, and the STC[5:0] and PLIDIV[1:0] bits in PLLCR.

10.6.4 AD Clock

The AD clock (PCLKC) refers to the clock for the AD.
The settings of the SCKCR.PCKC[3:0], SCKCR3.CKSEL[2:0], PLLCR.STC[5:0], and PLIDIV[1:0] bits determine the frequency of the PCLKC.

10.6.5 S12AD Clock

The S12AD clock (PCLKD) refers to the clock for the S12AD.
The settings of the SCKCR.PCKD[3:0], SCKCR3.CKSEL[2:0], PLLCR.STC[5:0], and PLIDIV[1:0] bits determine the frequency of the PCLKD.

10.6.6 FlashIF Clock

The flash-interface clock (FCLK) is used as the operating clock for the flash-memory interfaces. That is, FCLK is used for programming and erasure of the ROM and E2 DataFlash, and reading from the E2 DataFlash.
The FCLK frequency is specified by the FCK[3:0] bits in SCKCR, the CKSEL[2:0] bits in SCKCR3, and the STC[5:0] and PLIDIV[1:0] bits in PLLCR.

10.6.7 External Bus Clock

The external bus clock (BCLK) is an operating clock for the external bus controller. It is also output externally from the BCLK pin for the external connection bus. When the external bus is enabled, PE5 that is function-multiplexed with the BCLK pin cannot be used as an I/O port.
BCLK can be output from the BCLK pin by setting the SCKCR.PSTOP1 bit to 0 and setting the external bus enable bit in the system control register 0 (SYSCR0.EXBE) to 1. Make sure that modification of the SYSCR0.EXBE bit to 1 must always be performed while the PSTOP1 bit in SCKCR is 1.
When the BCKCR.BCLKDIV bit is set to 1, the BCLK clock divided by 2 is output from the BCLK pin.
The BCLK frequency is specified by the BCK[3:0] bits in SCKCR, the CKSEL[2:0] bits in SCKCR3, and the STC[5:0] and PLIDIV[1:0] bits in PLLCR.

10.6.8 USB Clock

The USB clock (UCLK) is an operating clock for the USB.
The UCLK frequency is specified by the UCK[3:0] bits in SCKCR2, the CKSEL[2:0] bits in SCKCR3, and the STC[5:0] and PLIDIV[1:0] bits in PLLCR.
A 48-MHz clock must be supplied to the USB module. When the USB module is used, setting must be made so that UCLK is 48 MHz.

10.6.9 CAN Clock

The CAN clock (CANMCLK) is an operating clock for the CAN.
CANMCLK is generated by the main clock oscillator.

10.6.10 CAC Clock

The CAC clock (CACMCLK) is an operating clock for the CAC.
CACMCLK is generated by the main clock oscillator.

10.6.11 IWDT-Dedicated Clock

The IWDT-dedicated low-speed clock (IWDTCLK) is the operating clock for the IWDT.
IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

10.6.12 JTAG Clock

The JTAG-dedicated clock (JTAGTCK) is the operating clock for the JTAG.
JTAGTCK is generated by the external clock for JTAG (TCK).

10.7 Pin Settings When an Oscillator is Connected

(1) Main clock

Clear the main clock oscillator stop bit (MOSTP in MOSCCR) to 0 so that the clock runs, or set the main clock oscillator forced oscillation bit (MOFXIN in MOFCR) to 1 so that it is forcibly made to oscillate.

10.8 Usage Notes

10.8.1 Notes on Clock Generation Circuit

(1) The frequencies of the system clock (ICLK), timer module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), S12AD clock (PCLKD), FlashIF clock (FCLK), and external bus clock (BCLK) supplied to each module change according to the settings of SCKCR. Each frequency should meet the following:
Select each frequency that is within the operation guaranteed range of clock cycle time (tcyc) specified in AC characteristics of electrical characteristics.
The frequencies must not exceed the ranges listed in Table 10.1.
The peripheral modules operate on the PCLKB. Note therefore that the operating speed of modules such as the timer and SCI varies before and after the frequency is changed.

(2) The following relation is required between the frequencies of the system clock (ICLK) and external bus clock (BCLK).
ICLK ≥ BCLK

(3) Do not change the clock frequency during external bus access. Furthermore, when access via the external bus is to start after a change to the clock frequency, only start access via the bus after confirming that the change to the frequencies has been completed.

(4) To secure the processing after the clock frequency is changed, modify the pertinent clock control register to change the frequency, and then read the value from the register, and then perform the subsequent processing.

10.8.2 Notes on Resonator

Since various resonator characteristics relate closely to the user's board design, adequate evaluation is required on the user side before use, referencing the resonator connection example shown in this section. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, the circuit constants should be determined in full consultation with the resonator manufacturer. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

10.8.3 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 10.6 to prevent electromagnetic induction from interfering with correct oscillation.

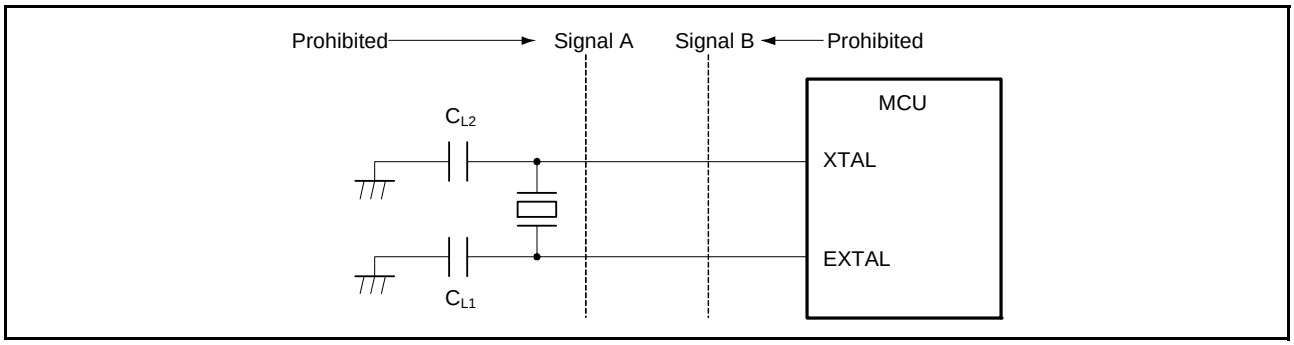


Figure 10.6 Notes on Board Design for Oscillation Circuit (Applies to the Sub-Clock Oscillator, in Case of the Main Clock Oscillator)

11. Clock Frequency Accuracy Measurement Circuit (CAC)

The clock frequency accuracy measurement circuit (CAC) monitors the clock frequency based on a reference signal input to the LSI externally or another clock source, and generates interrupts when the setting range is exceeded.

11.1 Overview

Table 11.1 shows the specifications of the CAC and Figure 11.1 shows a block diagram of the CAC.

Table 11.1 Specifications of CAC

Item	Description
Clock frequency measurement	The frequency of the following clocks can be measured. • Clock output from main clock oscillator (CACMCLK) • IWDT-dedicated lock (IWDTCLK) • Peripheral module clock (PCLK)
Selectable function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Power consumption reduction function	Module stop state can be set.

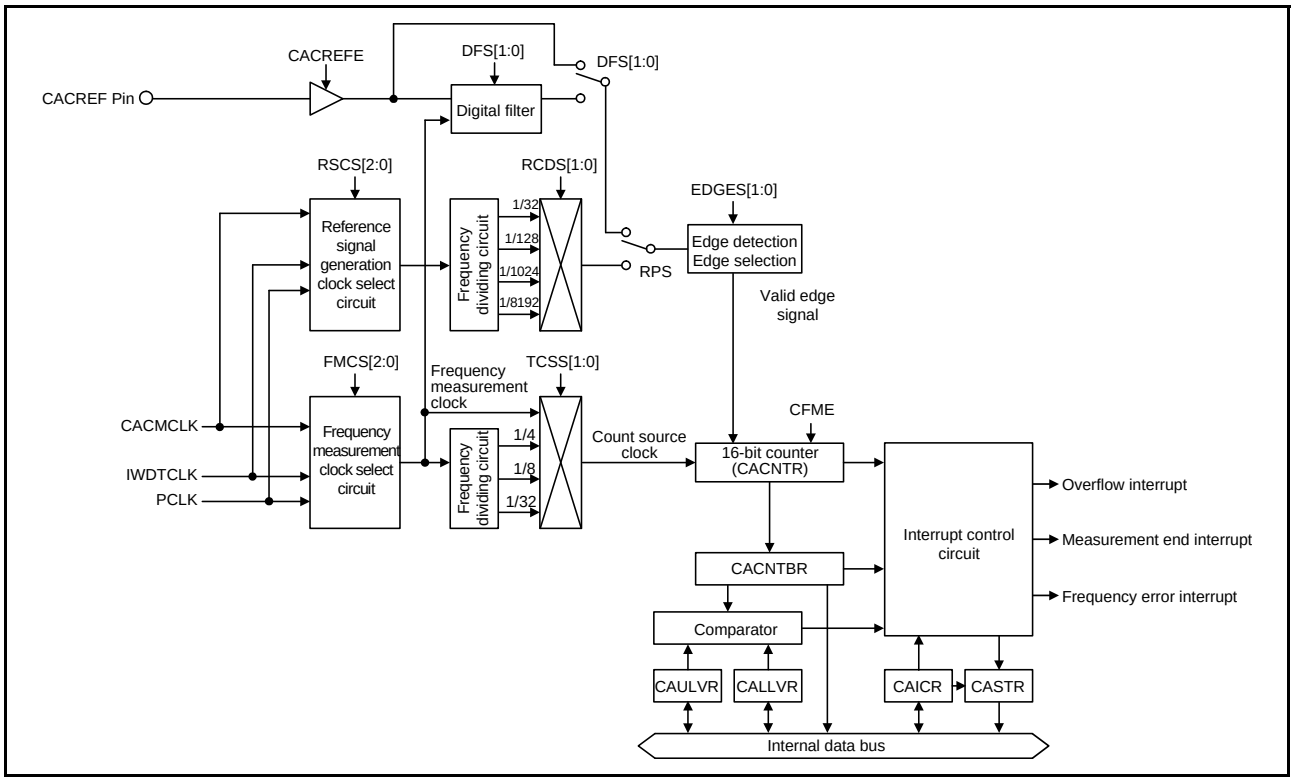


Figure 11.1 Block Diagram of CAC

Table 11.2 shows the pin configuration of the CAC.

Table 11.2 Pin Configuration of CAC

Pin Name	I/O	Function
CACREF	Input	Clock frequency accuracy measurement circuit input pin

11.2 Register Descriptions

11.2.1 CAC Control Register 0 (CACR0)

Address: 0008 B000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CFME	Clock Frequency Measurement Enable	0: Clock frequency measurement is disabled. 1: Clock frequency measurement is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CFME Bit (Clock Frequency Measurement Enable)

When the CFME bit is 1, clock frequency measurement is enabled.

After a new value is written to the CFME bit, reflecting the value in the internal circuitry takes a certain amount of time. The bit can be read to determine whether or not the new value is reflected. Note that overwriting the CFME bit when the previous value is not reflected in the internal circuitry has no effect.

11.2.2 CAC Control Register 1 (CACR1)

Address: 0008 B001h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: CACREF pin input is disabled. 1: CACREF pin input is enabled.	R/W
b3 to b1	FMCS[2:0]	Frequency Measurement Clock Select	b3 b1 0 0 0: Output clock of main clock oscillator (CACMCLK) 0 0 1: Setting prohibited 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock (PCLK) 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
b5, b4	TCSS[1:0]	Timer Count Clock Source Select	b5 b4 0 0: No division 0 1: × 1/4 clock 1 0: × 1/8 clock 1 1: × 1/32 clock	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

Note 1. CACR1 should be set when the CFME bit in CACR0 is 0.

CACREFE Bit (CACREF Pin Input Enable)

When the CACREFE bit is 1, the CACREF pin input is enabled.

FMCS[2:0] Bits (Frequency Measurement Clock Select)

The FMCS[2:0] bits select the clock whose frequency is to be measured.

TCSS[1:0] Bits (Timer Count Clock Source Select)

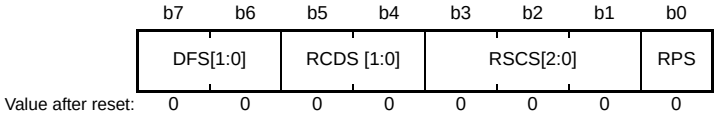
The TCSS[1:0] bits select the count clock source for the clock frequency accuracy measurement circuit.

EDGES[1:0] Bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

11.2.3 CAC Control Register 2 (CACR2)

Address: 0008 B002h



Bit	Symbol	Bit Name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internally generated signal	R/W
b3 to b1	RSCS[2:0]	Reference Signal Generation Clock Select	b3 b1 0 0 0: Output clock of main clock oscillator (CACMCLK) 0 0 1: Setting prohibited 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock (PCLK) 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
b5, b4	RCDS [1:0]	Reference Signal Generation Clock Frequency Division Ratio Select	b5 b4 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
b7, b6	DFS[1:0]	Digital Filter Selection	b7 b6 0 0: Digital filtering is disabled. 0 1: The sampling clock for the digital filter is the frequency measuring clock. 1 0: The sampling clock for the digital filter is the frequency measuring clock divided by four. 1 1: The sampling clock for the digital filter is the frequency measuring clock divided by 16.	R/W

Note 1. CACR2 should be set when the CFME bit in CACR0 is 0.

RPS Bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internally generated signal as the reference signal.

RSCS[2:0] Bits (Reference Signal Generation Clock Select)

The RSCS[2:0] bits select the clock source for generating the reference signal.

RCDS[1:0] Bits (Reference Signal Generation Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the frequency division ratio of the reference signal generation clock.

DFS[1:0] Bits (Digital Filter Selection)

The setting of the DFS[1:0] bits enables or disables the digital filter and selects its sampling clock.

11.2.4 CAC Interrupt Control Register (CAICR)

Address: 0008 B003h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FERRIE	Frequency Error Interrupt Enable	0: Frequency error interrupt is disabled. 1: Frequency error interrupt is enabled.	R/W
b1	MENDIE	Measurement End Interrupt Enable	0: Measurement end interrupt is disabled. 1: Measurement end interrupt is enabled.	R/W
b2	OVFIE	Overflow Interrupt Enable	0: Overflow interrupt is disabled. 1: Overflow interrupt is enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	FERRFCL	FERRF Clear	0: No effect on operations 1: Clears the FERRF flag In reading, the value read from this bit is 0.	R/W
b5	MENDFCL	MENDF Clear	0: No effect on operations 1: Clears the FERRF flag In reading, the value read from this bit is 0.	R/W
b6	OVFFCL	OVFF Clear	0: No effect on operations 1: Clears the FERRF flag In reading, the value read from this bit is 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

FERRIE Bit (Frequency Error Interrupt Enable)

When the FERRIE bit is 1, a frequency error interrupt is enabled.

MENDIE Bit (Measurement End Interrupt Enable)

When the MENDIE bit is 1, a measurement end interrupt is enabled.

OVFIE Bit (Overflow Interrupt Enable)

When the OVFIE bit is 1, an overflow interrupt is enabled.

FERRFCL Bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the FERRF flag.

MENDFCL Bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the MENDF flag.

OVFFCL Bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the OVFF flag.

11.2.5 CAC Status Register (CASTR)

Address: 0008 B004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FERRF	Frequency Error Flag	0: The clock frequency is within the range corresponding to the settings. 1: The clock frequency has deviated beyond the range corresponding to the settings (frequency error).	R
b1	MENDF	Measurement End Flag	0: Measurement is in progress. 1: Measurement has ended.	R
b2	OVFF	Overflow Flag	0: The counter has not overflowed. 1: The counter has overflowed.	R
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FERRF Flag (Frequency Error Flag)

This bit indicates deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- Clock frequency has deviated from the set value.

[Clearing condition]

- Writing of 1 to the FERRFCL bit

MENDF Flag (Measurement End Flag)

This bit indicates the end of measurement.

[Setting condition]

- End of measurement

[Clearing condition]

- Writing of 1 to the MENDFCL bit

OVFF Flag (Overflow Flag)

- This bit indicates that the counter has overflowed.
- [Setting condition]
- Overflow of the counter
- [Clearing condition]
- Writing of 1 to the OVFFCL bit

11.2.6 CAC Upper-Limit Value Setting Register (CAULVR)

Address: 0008 B006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR is a 16-bit readable/writable register that stores the upper-limit value of the frequency.
This register should be set when the CFME bit in CACR0 is 0.
The counter value held in CACNTBR can vary with the difference between the phases of the digital filter and edge-detection circuit on the one hand and the signal on the CACREF pin on the other, so ensure that this setting allows an adequate margin.

11.2.7 CAC Lower-Limit Value Setting Register (CALLVR)

Address: 0008 B008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR is a 16-bit readable/writable register that stores the lower-limit value of the frequency.
This register should be set when the CFME bit in CACR0 is 0.
The counter value held in CACNTBR can vary with the difference between the phases of the digital filter and edge-detection circuit on the one hand and the signal on the CACREF pin on the other, so ensure that this setting allows an adequate margin.

11.2.8 CAC Counter Buffer Register (CACNTBR)

Address: 0008 B00Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR is a 16-bit read-only register that retains the counter value at the time a valid reference signal edge is input.

11.3 Operation

11.3.1 Measuring Clock Frequency Based on CACREF Pin Input

Figure 11.2 shows an operating example of the clock frequency accuracy measurement circuit based on the CACREF pin input.
The clock frequency accuracy measurement circuit operates as shown below when measuring the clock frequency.

(1) Writing 1 to the CFME bit in CACR0 while the RPS bit in CACR2 is 0 and the CACREFE bit in CACR1 is 1 enables clock-frequency measurement based on the CACREF pin input.
(2) After 1 is written to the CFME bit, the timer starts up-counting when the valid edge selected by the EDGES[1:0] bits in CACR1 is input from the CACREF pin.
(3) When the next valid edge is input, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are satisfied, only the MENDF flag in CASTR is set to 1 because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt will occur.
(4) When the next valid edge is input, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt will occur. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt will occur.
(5) When the next valid edge is input, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt will occur. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt will occur.
(6) While the CFME bit in CACR0 is 1, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

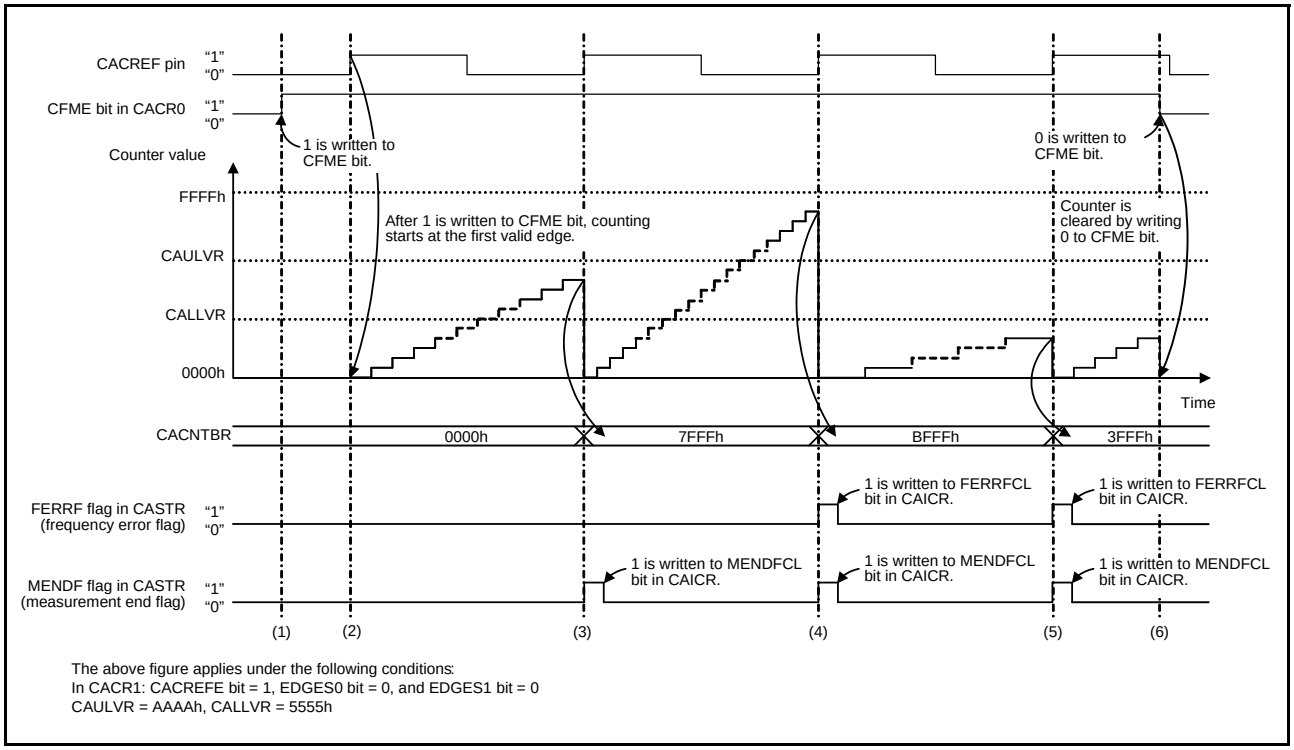


Figure 11.2 Operating Example of Clock Frequency Accuracy Measurement Circuit Based on CACREF Pin Input

11.3.2 Measuring Clock Frequency Based on Another Clock Source

Figure 11.3 shows an operating example of the clock frequency accuracy measurement circuit based on another clock source.

The clock frequency accuracy measurement circuit operates as shown below when measuring the clock frequency.

(1) When 1 is written to the CFME bit in CACR0 with the RPS bit in CACR2 set to 1, clock frequency measurement based on another clock source is enabled.

(2) After 1 is written to the CFME bit, the timer starts up-counting when the valid edge selected by the EDGES[1:0] bits in CACR1 is input based on the clock source selected by the RSCS[2:0] bits in CACR2.

(3) When the next valid edge is input, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are satisfied, only the MENDF flag in CASTR is set to 1 because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt will occur.

(4) When the next valid edge is input, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt will occur. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt will occur.

(5) When the next valid edge is input, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt will occur. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt will occur.

(6) While the CFME bit in CACR0 is 1, the counter value is retained in CACNTBR and compared with the values of CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

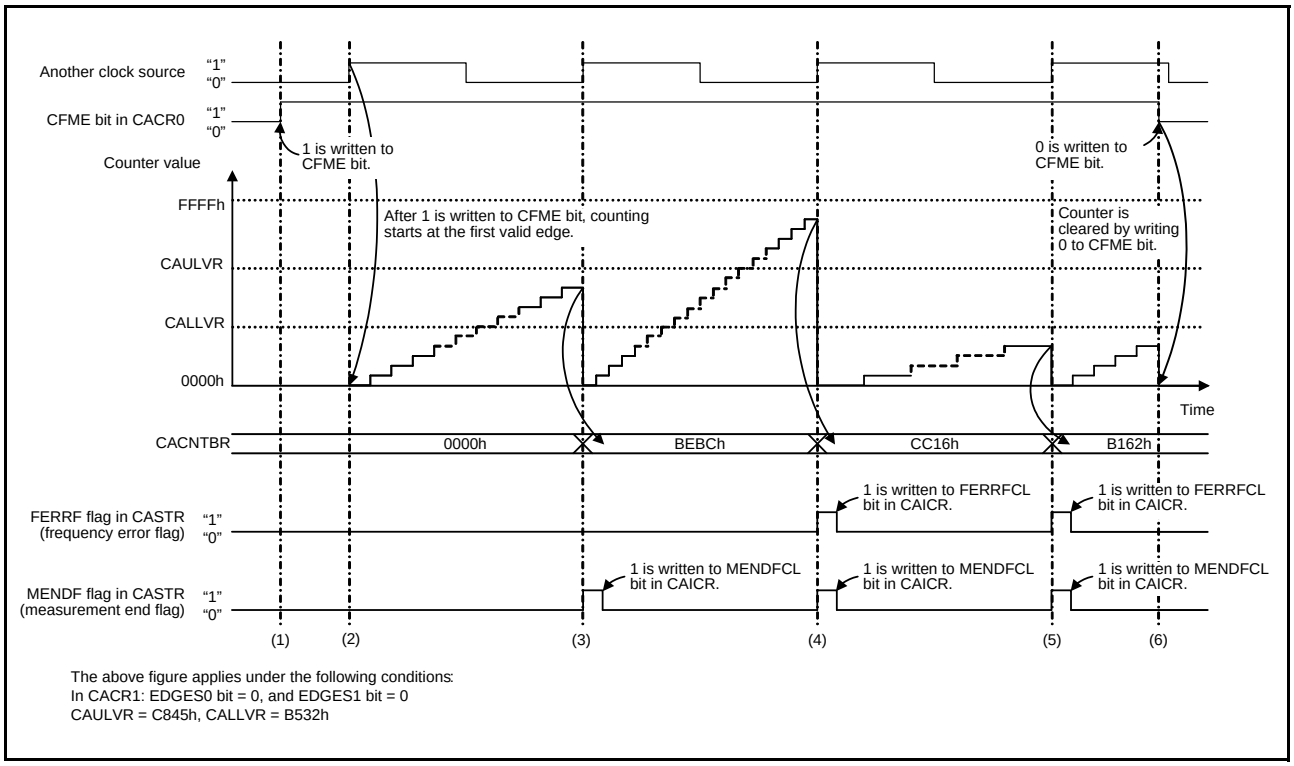


Figure 11.3 Operating Example of Clock Frequency Accuracy Measurement Circuit Based on Another Clock Source

11.3.3 Digital Filtering of Signals on the CACREF Pin

The CACREF pin has a digital filter. Levels on the target pin for sampling are conveyed to the internal circuitry after matching three times at the selected sampling interval and the same level continues to be conveyed internally until the level on the pin again matches three times.
Enabling and disabling of the digital filter and its sampling clock are selectable.
The counter value held in CACNTBR may be in error by up to one cycle of the sampling clock due to the difference between the phases of the digital filter and the signal on the CACREF pin.
When a frequency dividing clock is selected as a count source clock, the counter value error is obtained by the following formula.
Counter value error = (One cycle of the count source clock) / (One cycle of the sampling clock)

11.4 Interrupt Requests

The clock frequency accuracy measurement circuit issues three types of interrupt request: frequency error interrupt, measurement end interrupt, and overflow interrupt. When an interrupt source is generated, the corresponding status flag is set to 1. Table 11.3 shows details on the interrupt requests of the clock frequency accuracy measurement circuit.

Table 11.3 Interrupt Requests of Clock Frequency Accuracy Measurement Circuit

Interrupt Request	Interrupt Enable Bit	Status Flag	Interrupt Source
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR to CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR.
Measurement end interrupt	CAICR.MENDIE	CASTR. MENDF	A valid edge is input from the CACREF pin. Note however that a measurement end interrupt does not occur at the first valid edge after writing 1 to the CFME bit in CACR0.
Overflow interrupt	CAICR.OVFIE	CASTR. OVFF	The counter has overflowed.

11.5 Usage Notes

11.5.1 Module Stop Function Setting

CAC operation can be disabled or enabled using the module stop control register C (MSTPCRC). The initial setting is for the CAC to be halted. Register access is enabled by canceling the module stop state. For details, see section 12, Low Power Consumption.

12. Low Power Consumption

12.1 Overview

This MCU has several functions for reducing power consumption, including switching of clock signals to reduce power consumption, BCLK output control, stopping modules, and transitions to low power consumption states.
Table 12.1 lists the specifications of low power consumption functions, and Table 12.2 lists the conditions to shift to low power consumption modes, states of the CPU and peripheral modules, and the method for canceling each mode.
After a reset, this MCU enters the normal program execution state, but modules except for the DMACA, DTC, and on-chip RAM do not operate.

Table 12.1 Specifications of Low Power Consumption Functions

Item	Specification
Reducing power consumption by switching clock signals	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).*1
BCLK output control function	BCLK output or high-level output can be selected.*1
Module-stop function	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode

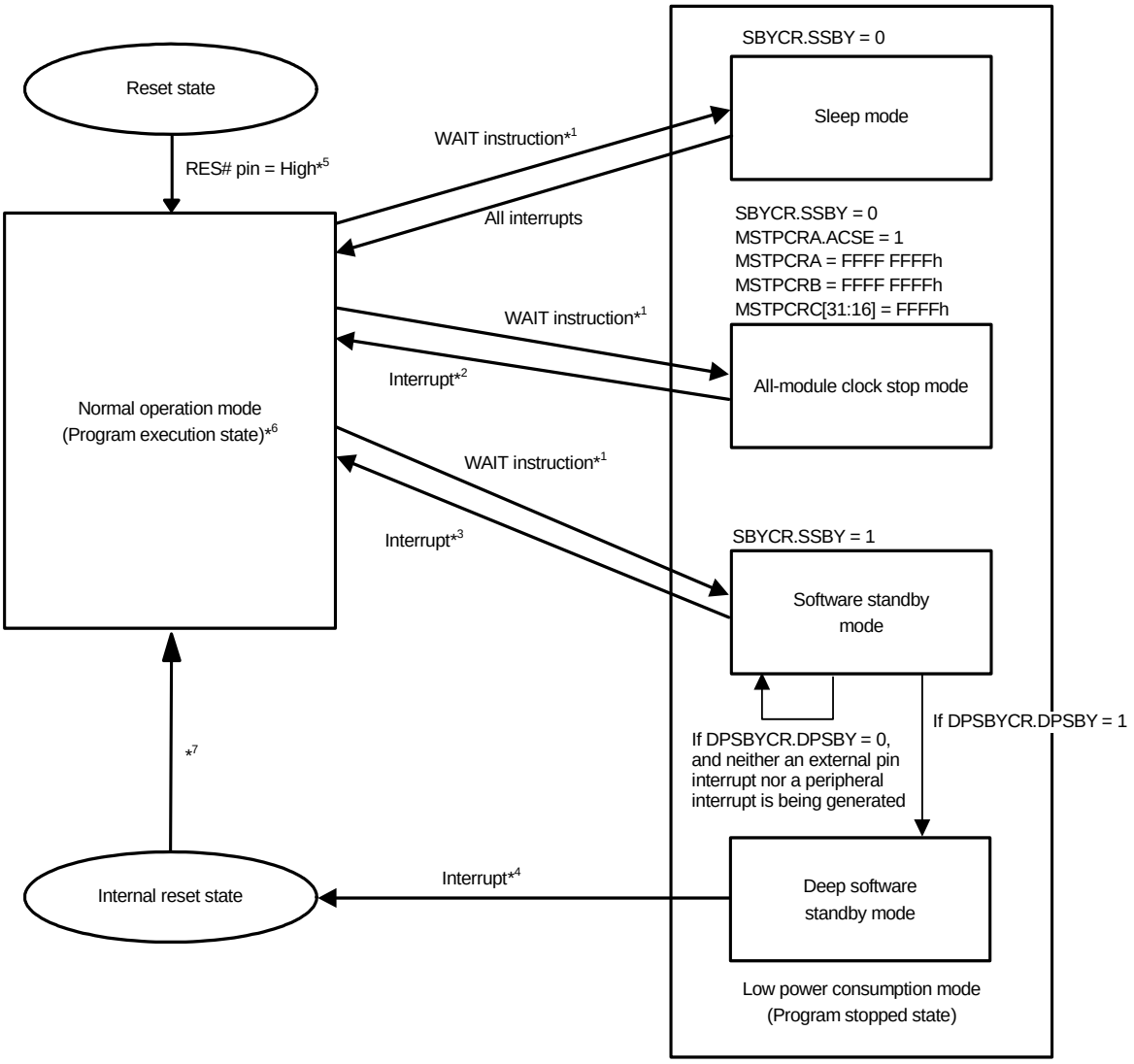
Note 1. For details, see section 10, Clock Generation Circuit.

Table 12.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Entering and Exiting Low Power Consumption Modes and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction	Control register + instruction	Control register + instruction
Canceling method other than reset	Interrupt	Interrupt*1	Interrupt*2	Interrupt*3
State after cancellation*4	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (reset processing)
Main clock oscillator	Operating possible	Operating possible	Operating possible*5	Operating possible*5
Low-speed on-chip oscillator	Operating possible	Operating possible	Stopped	Stopped
Dedicated on-chip oscillator for the IWDT	Operating possible*6	Operating possible*6	Operating possible*6	Stopped (Undefined)*6
PLL	Operating possible	Operating possible	Stopped	Stopped
CPU	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
On-chip RAM0 (0000 0000h to 0000 BFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
Flash memory	Operating	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)
USB 2.0 function module (USB)	Operating possible	Stopped*7	Stopped*7	Stopped (Undefined)
Watchdog timer (WDT)	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
Independent watchdog timer (IWDT)	Operating possible*6	Operating possible*6	Operating possible*6	Stopped (Undefined)*6
Port output enable (POE)	Operating possible	Operating possible*8	Stopped (Retained)	Stopped (Undefined)
Voltage detection circuit (LVD)	Operating possible	Operating possible	Operating possible	Operating possible*9
Power-on reset circuit	Operating	Operating	Operating	Operating
Peripheral modules	Operating possible	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
I/O ports	Operating	Retained*10	Retained*11	Retained*11

“Operating possible” means that operating or stopped can be controlled by the control register setting.
“Stopped (Retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (Undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Note 1. “Interrupts” here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (IWDT, USB suspend/resume, voltage monitoring 1, voltage monitoring 2, and oscillator-stopped detection interrupts).
Note 2. “Interrupts” here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (IWDT, USB suspend/resume, voltage monitoring 1, and voltage monitoring 2 interrupts).
Note 3. “Interrupts” here indicates a certain external pin interrupt source pin (the NMI, IRQ0-DS to IRQ7-DS) or any of peripheral interrupts (voltage monitoring 1, and voltage monitoring 2 interrupts). However, these interrupts are enabled only when the corresponding bit in the deep standby interrupt enable registers i (DPSIERi) (i = 0 or 2) is set to 1. Pins that have “-DS” appended to their names can be used as triggers for release from deep software standby.
Note 4. This does not include release initiated by a RES# pin reset, power-on reset, voltage monitoring reset, or independent watchdog-timer reset. The transition is to the reset state when release is initiated by one of these reset sources.
Note 5. Operation or stopping can be selected by the main clock oscillator forced oscillation bit (MOFXIN) in the main clock oscillator forced oscillation control register (MOFCR).
Note 6. Operation or stopping is selected by the setting of the IWDT sleep mode count stop control bit (IWDTSLCSTP) in the option function select register 0 (OFS0) in IWDT auto start mode. If the OFS0.IWDTSLCSTP bit is 0 (disabling stopping of the counter when a transition to low power consumption mode is made), the transition is to software standby mode rather than deep software standby mode. In any mode other than IWDT auto start mode, operation or stopping is selected by the setting of the sleep mode counter stop control bit (SLCSTP) in the IWDT counter stop control register (IWDTCSTPR). If the IWDTCSTPR.SLCSTP bit is 0 (disabling stopping of the counter when a transition to low power consumption mode is made), the transition is to software standby mode rather than deep software standby mode.
Note 7. Detection of USB resumption is possible.
Note 8. When a source condition for POE interrupts is satisfied while POE interrupts are enabled and the chip is in all-module clock stop mode, the flag for the source condition is retained but return from all-module clock stop mode does not proceed. If a different source initiates return from all-module clock stop mode in this situation, the POE interrupt is generated after that.
Note 9. If the voltage monitoring 1 circuit mode selection bit in the voltage monitoring 1 circuit control register 0 (LVD1CR0.LVD1RI) or the voltage monitoring 2 circuit mode selection bit in the voltage monitoring 2 circuit control register 0 (LVD2CR0.LVD2RI) is 1, the transition is to software standby mode rather than deep software standby mode.
Note 10. If pin PE5 is being used for the BCLK signal, operation continues with as-is output of BCLK. High impedance control is applied to the corresponding pin when a condition for this control is satisfied while the POE module is operating.
Note 11. Retention of levels or placement in the high-impedance state is selectable for the address bus and bus control signals (CS0# to CS3#, RD#, WR0# to WR1#, WR#, BC0# to BC1#, and ALE) by the output port enable bit (OPE) in the standby control register (SBYCR).



Note 1. When an interrupt that acts as a trigger for release is received during the transition to the program-stopped state after the execution of a WAIT instruction, the transition to the program stopped state does not proceed and interrupt exception processing is executed instead.

Note 2. "Interrupts" here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (IWDT, USB suspend/resume, voltage-monitoring 1, voltage-monitoring 2, and oscillator-stopped detection interrupts).

Note 3. "Interrupts" here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (IWDT, USB suspend/resume, voltage-monitoring 1, and voltage-monitoring 2 interrupts).

Note 4. "Interrupts" here indicates a certain external pin interrupt source pin (the NMI or IRQ0-DS to IRQ7-DS) or any of peripheral interrupts (voltage-monitoring 1, and voltage-monitoring 2 interrupts). However, these interrupts are enabled only when the corresponding bit in the deep standby interrupt enable registers i (DPSIERi) (i = 0 or 2) is set to 1.

Note 5. The LOCO is the source of the operating clock following a transition from the reset state to normal operating mode.

Note 6. The transition to normal operating mode is made due to an interrupt from sleep mode, all-module clock-stop mode, or software standby mode.

Note 7. When an interrupt request as indicated in Note 4 above is generated, an internal reset (deep software standby reset) is generated over a fixed period. Release from deep software standby mode accompanies release from the internal reset state. The transition from deep software standby mode is to normal operating mode, and reset exception processing starts with the LOCO as the source of the operating clock.

When a RES# pin reset, power-on reset, voltage-monitoring 0 reset, voltage-monitoring 1 reset, voltage-monitoring 2 reset, watchdog timer reset, independent watchdog timer reset, or software reset is generated in any state, a transition to the reset state is made. The voltage-monitoring 1 reset and voltage-monitoring 2 reset cannot be used to cancel deep software standby mode.

Figure 12.1 Mode Transitions

12.2 Register Descriptions

12.2.1 Standby Control Register (SBYCR)

Address(es): 0008 000Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	OPE	Output Port Enable	0: In software standby mode or deep software standby mode, the address bus and bus control signals are set to the high-impedance state. 1: In software standby mode or deep software standby mode, the address bus and bus control signals retain the output state.	R/W
b15	SSBY	Software Standby	0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

OPE Bit (Output Port Enable)

The OPE bit specifies whether to retain the output of the address bus and bus control signals (CS0# to CS3#, RD#, WR0# to WR1#, WR#, BC0# to BC1#, and ALE) in software standby mode or deep software standby mode, or to set the output to the high-impedance state.

SSBY Bit (Software Standby)

The SSBY bit specifies the transition destination after the WAIT instruction is executed.

When the SSBY bit is set to 1, the MCU enters software standby mode after execution of the WAIT instruction. When the MCU returns to normal mode after an interrupt has initiated release from software standby mode, the SSBY bit remains 1. Write 0 to this bit to clear it.

When the oscillation stop detection function enable bit (OSTDCR.OSTDE) is 1, setting of the SSBY bit is invalid. Even if the SSBY bit is 1, the MCU will enter sleep mode or all module clock stop mode on execution of the WAIT instruction.

12.2.2 Module Stop Control Register A (MSTPCRA)

Address(es): 0008 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ACSE	—	MSTPA 29	MSTPA 28	MSTPA 27	—	—	MSTPA 24	MSTPA 23	—	—	—	MSTPA 19	—	MSTPA 17	MSTPA 16
Value after reset:	0	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPA 15	MSTPA 14	—	—	—	—	MSTPA 9	—	MSTPA 7	MSTPA 6	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b6	MSTPA6	General PWM Timer (Unit 1) Module Stop	Target module: GPTB (GPT4 to GPT7) 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b7	MSTPA7	General PWM Timer (Unit 0) Module Stop	Target module: GPT (GPT0 to GPT3) 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b8	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b9	MSTPA9	Multifunction Timer Pulse Unit 3 Module Stop	Target module: MTU3 (MTU0 to MTU7) 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b13 to b10	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14	MSTPA14	Compare Match Timer (Unit 1) Module Stop	Target module: CMT unit 1 (CMT2, CMT3) 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b15	MSTPA15	Compare Match Timer (Unit 0) Module Stop	Target module: CMT unit 0 (CMT0, CMT1) 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b16	MSTPA16	12-bit A/D Converter (Unit 1) Module Stop	Target module: S12AD1 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b17	MSTPA17	12-bit A/D Converter (Unit 0) Module Stop	Target module: S12AD 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b18	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b19	MSTPA19	D/A Converter Module Stop	Target module: DA 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b22 to b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b23	MSTPA23	10-bit A/D Converter Module Stop	Target module: AD 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b24	MSTPA24	12-bit A/D Converter Control Section Module Stop	Target module: S12AD Control Section, S12AD1 Control Section 0: The module stop state is canceled 1: Transition to the module stop state is made	R/W
b26, b25	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b27	MSTPA27	Module Stop A27	Writing to and reading from this bit is enabled. When a transition to all-module clock stop mode is made, be sure that 1 has been written to this bit.	R/W
b28	MSTPA28	DMA Controller/Data Transfer Controller Module Stop	Target module: DMAC/DTC 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W

Bit	Symbol	Bit Name	Description	R/W
b29	MSTPA29	Module Stop A29	Writing to and reading from this bit is enabled. When a transition to all-module clock stop mode is made, be sure that 1 has been written to this bit.	R/W
b30	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b31	ACSE	All-Module Clock Stop Mode Enable	0: All-module clock stop mode is disabled 1: All-module clock stop mode is enabled	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

ACSE Bit (All-Module Clock Stop Mode Enable)

The ACSE bit enables or disables a transition to all-module clock stop mode.

With the ACSE bit set to 1, when the CPU executes the WAIT instruction with the SBYCR.SSBY bit, MSTPCRA, MSTPCRB, and MSTPCRC satisfying specified conditions, the MCU enters all-module clock stop mode. For details, see section 12.5.2, All-Module Clock Stop Mode.

When the MSTPCRA.ACSE bit = 0 while the SBYCR.SSBY = 0, a transition to sleep mode is made after the WAIT instruction is executed.

12.2.3 Module Stop Control Register B (MSTPCRB)

Address(es): 0008 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPB31	MSTPB30	MSTPB29	MSTPB28	—	—	—	—	MSTPB23	—	MSTPB21	MSTPB20	MSTPB19	—	MSTPB17	MSTPB16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	MSTPB6	—	MSTPB4	—	—	MSTPB1	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 1. The write value should be 0.	R/W
b1	MSTPB1	CAN Module 1 Module Stop*1	Target module: CAN1 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b3, b2	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b4	MSTPB4	Serial Communication Interface SCId Module Stop	Target module: SCId (SCI12) 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b5	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b6	MSTPB6	Data Operation Circuit Module Stop	Target module: DOC 0: The module stop state is canceled 1: Transition to the module stop state is made	R/W
b15 to b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b16	MSTPB16	Serial Peripheral Interface 1 Module Stop	Target module: RSPI1 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b17	MSTPB17	Serial Peripheral Interface 0 Module Stop	Target module: RSPI0 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b18	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Bit	Symbol	Bit Name	Description	R/W
b19	MSTPB19	Universal Serial Bus Interface (Port 0) Module Stop*2	Target module: USB0 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b20	MSTPB20	I^2C Bus Interface 1 Module Stop	Target module: RIIC1 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b21	MSTPB21	I^2C Bus Interface 0 Module Stop	Target module: RIIC0 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b22	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b23	MSTPB23	CRC Calculator Module Stop	Target module: CRC 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b27 to b24	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b28	MSTPB28	Serial Communication Interface 3 Module Stop	Target module: SCI3 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b29	MSTPB29	Serial Communication Interface 2 Module Stop	Target module: SCI2 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b30	MSTPB30	Serial Communication Interface 1 Module Stop	Target module: SCI1 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W
b31	MSTPB31	Serial Communication Interface 0 Module Stop	Target module: SCI0 0: The module-stop state is canceled 1: Transition to the module-stop state is made	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. The MSTPBi bit should be rewritten while the oscillation of the clock controlled by MSTPBi is stabilized. For entering software standby mode after rewriting the MSTPBi bit, wait for two CAN clock (CANCLK) cycles after rewriting, and execute the WAIT instruction (i = 0 to 2).

Note 2. For entering software standby mode after rewriting the MSTPB19 bit, wait for two USB clock (UCLK) cycles after rewriting, and execute the WAIT instruction.

12.2.4 Module Stop Control Register C (MSTPCRC)

Address(es): 0008 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPC31	—	—	—	—	—	—	—	—	—	—	—	MSTPC19	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTPC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPC0	RAM0 Module Stop*1	Target module: RAM0 (0000 0000h to 0000 BFFFh) 0: RAM0 operating 1: RAM0 stopped	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b19	MSTPC19	Clock Frequency Accuracy Measurement Circuit Module Stop	Target module: CAC 0: The module stop state is canceled 1: Transition to the module stop state is made	R/W
b30 to b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	MSTPC31	Digital Power Supply Control Circuit Module Stop	Target module: DPC 0: Module stop state is canceled 1: Transition to the module stop state is made	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. The MSTPC0 bit should not be set to 1 during access to the corresponding on-chip RAM. The corresponding on-chip RAM should not be accessed while the MSTPC0 bit is set to 1.

12.2.5 Main Clock Oscillator Wait Control Register (MOSCWTCR)

Address(es): 0008 00A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MSTS[4:0]				
Value after reset:	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	MSTS[4:0]	Main Clock Oscillator Wait Time Select	b4 b0 0 0 0 0 0: Waiting time = 2 cycles 0 0 0 0 1: Waiting time = 4 cycles 0 0 0 1 0: Waiting time = 8 cycles 0 0 0 1 1: Waiting time = 16 cycles 0 0 1 0 0: Waiting time = 32 cycles 0 0 1 0 1: Waiting time = 64 cycles 0 0 1 1 0: Waiting time = 512 cycles 0 0 1 1 1: Waiting time = 1024 cycles 0 1 0 0 0: Waiting time = 2048 cycles 0 1 0 0 1: Waiting time = 4096 cycles 0 1 0 1 0: Waiting time = 16384 cycles 0 1 0 1 1: Waiting time = 32768 cycles 0 1 1 0 0: Waiting time = 65536 cycles 0 1 1 0 1: Waiting time = 131072 cycles 0 1 1 1 0: Waiting time = 262144 cycles 0 1 1 1 1: Waiting time = 524288 cycles Settings other than above are prohibited.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

MOSCWTCR is used to control the oscillation settling time of the main clock oscillator.
Supply of the main clock signal within the MCU starts after counting of the number of cycles of the main clock specified in the MOSCWTCR register plus 16384.
Set the MSTS[4:0] bits so that the waiting time is at least as long as the main clock oscillator stabilization time ($t_{MAINOSC}$). Only use the main clock after the main clock oscillation settling time ($t_{MAINOSCWT}$) has elapsed. Regarding the main clock oscillation settling time, refer to Table 42.9 or Table 43.7.
The waiting time is not required when the main clock is externally input.
MOSCWTCR can only be rewritten when the MOSCCR.MOSTP bit is 1; do not rewrite MOSCWTCR with other settings.

Example: When oscillation is at 12 MHz and the crystal resonator is to be used after 10 ms (= 10000 µs) of stabilization time

To satisfy the relation waiting time ≥ $t_{MAINOSC} \times f_{MAIN}$ = 10000 [µs] × 12 [MHz] = 120000 [cycles], set the MSTS[4:0] bits to 01101b (131072 cycles).
At this time, when the main clock stabilization time is calculated from the formula in Table 42.9 or Table 43.7,

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

$$= 10000[\mu s] + \frac{131072[cycles] + 16384}{12[MHz]}$$

$$= 22288[\mu s]$$

22288 µs are required from the time the main clock starts oscillating until it is usable.

12.2.6 PLL Wait Control Register (PLLWTCR)

Address(es): 0008 00A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PSTS[4:0]				
Value after reset:	0	0	0	0	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSTS[4:0]	PLL Wait Time Select	b4 b0 0 0 0 0 0: Waiting time = 16 cycles 0 0 0 0 1: Waiting time = 32 cycles 0 0 0 1 0: Waiting time = 64 cycles 0 0 0 1 1: Waiting time = 512 cycles 0 0 1 0 0: Waiting time = 1024 cycles 0 0 1 0 1: Waiting time = 2048 cycles 0 0 1 1 0: Waiting time = 4096 cycles 0 0 1 1 1: Waiting time = 16384 cycles 0 1 0 0 0: Waiting time = 32768 cycles 0 1 0 0 1: Waiting time = 65536 cycles 0 1 0 1 0: Waiting time = 131072 cycles 0 1 0 1 1: Waiting time = 262144 cycles 0 1 1 0 0: Waiting time = 524288 cycles 0 1 1 0 1: Waiting time = 1048576 cycles 0 1 1 1 0: Waiting time = 2097152 cycles 0 1 1 1 1: Waiting time = 4194304 cycles Settings other than above are prohibited.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

PLLWTCR is used to select the oscillation settling time of the PLL.

Supply of the PLL clock signal within the MCU starts after counting of the number of cycles of the PLL clock specified in the PLLWTCR register + 131072.

Set the PSTS[4:0] bits so that the waiting time is greater than the PLL clock stabilization time (t_{PLL1} or t_{PLL2}). Only use the PLL clock after waiting for the PLL clock oscillation stabilization waiting time (t_{PLLWT1} or t_{PLLWT2}) to elapse after oscillation of the PLL has started. See Table 42.9 or Table 43.7 for the PLL clock oscillation stabilization waiting time.

PLLWTCR can only be rewritten when the PLLCR2.PLLEN bit is 1 (PLL stopped); do not rewrite PLLWTCR with other settings.

Example: When oscillation is at 12 MHz, the crystal resonator is to be used after 10 ms (= 10000 µs) of stabilization time, and the PLL is to oscillate at 200 MHz

- When the PLL starts operating after oscillation of the main clock has become stable

To satisfy the relation waiting time ≥ $t_{PLL} \times f_{PLL}$ = 500 [µs] × 200 [MHz] = 100000 [cycles], set the PSTS[4:0] bits to 01010b (131072 cycles).
At this time, when the PLL clock stabilization time is calculated from the formula in Table 42.9 or Table 43.7,

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$= 500[\mu s] + \frac{131072[cycles] + 131072}{200[MHz]}$$

$$= 1810.72[\mu s]$$

1811 µs of waiting are required from the time the PLL clock starts oscillating until it is usable.

- When the PLL starts operating before oscillation of the main clock has become stable

To satisfy the relation waiting time ≥ ($t_{MAINOSC} + t_{PLL1)} \times t_{PLL}$ = (10000 [µs] + 500 [µs]) x 200 [MHz] = 2100000 [cycles], set the PSTS[4:0] bits to 01111b (4194304 cycles).
At this time, when the PLL clock stabilization time is calculated from the formula in Table 42.9 or Table 43.7,

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}}$$

$$= t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$= 10000[\mu s] + 500[\mu s] + \frac{4194304[cycles] + 131072}{200[MHz]}$$

$$= 32126.88[\mu s]$$

about 32.13 ms of waiting are required from the time the PLL clock starts oscillating until it is usable.

12.2.7 Deep Standby Control Register (DPSBYCR)

Address(es): 0008 C280h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSBY	IOKEEP	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b5 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	IOKEEP	I/O Port Retention	0: Deep software standby mode and I/O port retention are canceled simultaneously. 1: The I/O port state is retained even after deep software standby mode is canceled. Then, writing 0 to the IOKEEP bit cancels the I/O port retention.	R/W
b7	DPSBY	Deep Software Standby	SSBY b7 0 0: Transition to sleep mode or all-module clock stop mode is made after the WAIT instruction is executed 0 1: Transition to sleep mode or all-module clock stop mode is made after the WAIT instruction is executed 1 0: Transition to software standby mode is made after the WAIT instruction is executed 1 1: Transition to deep software standby mode is made after the WAIT instruction is executed	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSBYCR is not initialized by the internal reset signal that is the source to cancel the deep software standby mode. For details, see Table 7.2, Targets to be Initialized by Each Reset Source.

IOKEEP Bit (I/O Port Retention)

In deep software standby mode, I/O ports keep retaining the same states from software standby mode. The IOKEEP bit specifies whether to keep retaining the I/O port states from deep software standby mode even after deep software standby mode is canceled, or to cancel retaining the I/O port states.

DPSBY Bit (Deep Software Standby)

The DPSBY bit controls transitions to deep software standby mode.

When the WAIT instruction is executed while the SBYCR.SSBY and DPSBY bits are both 1, the MCU enters deep software standby mode through software standby mode.

The DPSBY bit remains 1 when deep software standby mode is canceled by certain pins which are sources of external pin interrupts (NMI, IRQ0-DS to IRQ7-DS) or a peripheral interrupt (voltage monitoring 1 or voltage monitoring 2). Write 0 to this bit to clear it.

The setting of the DPSBY bit becomes invalid when the IWDT is in auto-start mode and the OFS0.IWDTSLCSTP is 0 (counting continues) or the IWDT is in register start mode and the SLCSTP bit in IWDTCSTPR is 0.

Instead, even when the SBYCR.SSBY bit is 1 and the DPSBY bit 1, the transition after the execution of a WAIT instruction is to software standby mode.

The setting of the DPSBY bit becomes invalid when voltage monitoring 1 reset is enabled by the voltage monitoring 1 circuit mode select bit (LVD1CR0.LVD1RI = 1) or when a voltage monitoring 2 reset is selected by the voltage monitoring 2 circuit mode bit (LVD2CR0.LVD2RI = 1). In this case, even when the SBYCR.SSBY bit is 1 and the DPSBY bit is 1, the transition after the execution of a WAIT instruction is to software standby mode.

12.2.8 Deep Standby Interrupt Enable Register 0 (DPSIER0)

Address(es): 0008 C282h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	DIRQ3E	DIRQ2E	DIRQ1E	DIRQ0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DIRQ0E	IRQ0-DS Pin Enable	0: Canceling deep software standby mode by the IRQ0-DS pin is disabled 1: Canceling deep software standby mode by the IRQ0-DS pin is enabled	R/W
b1	DIRQ1E	IRQ1-DS Pin Enable	0: Canceling deep software standby mode by the IRQ1-DS pin is disabled 1: Canceling deep software standby mode by the IRQ1-DS pin is enabled	R/W
b2	DIRQ2E	IRQ2-DS Pin Enable	0: Canceling deep software standby mode by the IRQ2-DS pin is disabled 1: Canceling deep software standby mode by the IRQ2-DS pin is enabled	R/W
b3	DIRQ3E	IRQ3-DS Pin Enable	0: Canceling deep software standby mode by the IRQ3-DS pin is disabled 1: Canceling deep software standby mode by the IRQ3-DS pin is enabled	R/W
b4	DIRQ4E	IRQ4-DS Pin Enable	0: Canceling deep software standby mode by the IRQ4-DS pin is disabled 1: Canceling deep software standby mode by the IRQ4-DS pin is enabled	R/W
b5	DIRQ5E	IRQ5-DS Pin Enable	0: Canceling deep software standby mode by the IRQ5-DS pin is disabled 1: Canceling deep software standby mode by the IRQ5-DS pin is enabled	R/W
b6	DIRQ6E	IRQ6-DS Pin Enable	0: Canceling deep software standby mode by the IRQ6-DS pin is disabled 1: Canceling deep software standby mode by the IRQ6-DS pin is enabled	R/W
b7	DIRQ7E	IRQ7-DS Pin Enable	0: Canceling deep software standby mode by the IRQ7-DS pin is disabled 1: Canceling deep software standby mode by the IRQ7-DS pin is enabled	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER0 is not initialized by the internal reset signal used as deep software standby mode canceling source. For details, see Table 7.2, Targets to be Initialized by Each Reset Source.

After the setting of DPSIER0 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR0 being set to 1. Therefore, DPSIFR0 should be cleared to 0 before a transition to deep software standby mode.

Even when DPSIER0 is 0, a rising edge may be internally generated at a transition to deep software standby mode with a specific pin state, resulting in DPSIFR0 being set to 1. However, when DPSIEGR0 is 0, the rising edge is not detected, resulting in DPSIFR0 not being set to 1.

12.2.9 Deep Standby Interrupt Enable Register 2 (DPSIER2)

Address(es): 0008 C284h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIE	—	—	DLVD2IE	DLVD1IE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DLVD1IE	LVD1 Deep Standby Cancel Signal Enable	0: Canceling deep software standby mode by the voltage monitoring 1 signal is disabled 1: Canceling deep software standby mode by the voltage monitoring 1 signal is enabled	R/W
b1	DLVD2IE	LVD2 Deep Standby Cancel Signal Enable	0: Canceling deep software standby mode by the voltage monitoring 2 signal is disabled 1: Canceling deep software standby mode by the voltage monitoring 2 signal is enabled	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DNMIE	NMI Pin Enable	0: Canceling deep software standby mode by the NMI pin is disabled 1: Canceling deep software standby mode by the NMI pin is enabled	R/W*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. 1 can be written only once. Once 1 is written to this bit, subsequent write accesses are disabled.

DPSIER2 is not initialized by the internal reset signal used as deep software standby mode canceling source. For details, see Table 7.2, Targets to be Initialized by Each Reset Source.

After the setting of DPSIER2 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR2 being set to 1. Therefore, DPSIFR2 should be cleared to 0 before a transition to deep software standby mode.

Even when DPSIER2 is 0, a rising edge may be internally generated at a transition to deep software standby mode with a specific pin state, resulting in DPSIFR2 being set to 1. However, when DPSIEGR2 is 0, the rising edge is not detected, resulting in DPSIFR2 not being set to 1.

12.2.10 Deep Standby Interrupt Flag Register 0 (DPSIFR0)

Address(es): 0008 C286h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	DIRQ3F	DIRQ2F	DIRQ1F	DIRQ0F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DIRQ0F	IRQ0-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ0-DS pin is generated 1: A cancel request by the IRQ0-DS pin is generated	R(/W) *1
b1	DIRQ1F	IRQ1-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ1-DS pin is generated 1: A cancel request by the IRQ1-DS pin is generated	R(/W) *1
b2	DIRQ2F	IRQ2-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ2-DS pin is generated 1: A cancel request by the IRQ2-DS pin is generated	R(/W) *1
b3	DIRQ3F	IRQ3-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ3-DS pin is generated 1: A cancel request by the IRQ3-DS pin is generated	R(/W) *1
b4	DIRQ4F	IRQ4-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ4-DS pin is generated 1: A cancel request by the IRQ4-DS pin is generated	R(/W) *1
b5	DIRQ5F	IRQ5-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ5-DS pin is generated 1: A cancel request by the IRQ5-DS pin is generated	R(/W) *1
b6	DIRQ6F	IRQ6-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ6-DS pin is generated 1: A cancel request by the IRQ6-DS pin is generated	R(/W) *1
b7	DIRQ7F	IRQ7-DS Deep Standby Cancel Flag	0: No cancel request by the IRQ7-DS pin is generated 1: A cancel request by the IRQ7-DS pin is generated	R(/W) *1

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Each flag is set to 1 when a cancel request specified by DPSIEGR0 is generated.
Each flag may be set to 1 when a cancel request is generated in any mode (not even deep software standby mode) or when the setting of DPSIER0 is modified. Therefore, a transition to deep software standby mode should be made after DPSIFR0 is cleared to 00h.
To clear DPSIFR0 to 00h after modifying DPSIER0, wait for at least six PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0.
DPSIFR0 is not initialized by the internal reset signal used as deep software standby mode canceling source. For details, see Table 7.2, Targets to be Initialized by Each Reset Source.

DIRQnF Flags (IRQn Deep Standby Cancel Flag) (n = 0 to 7)

These flags indicate that a cancel request by the IRQn-DS pin has been generated.
[Setting condition]

- A cancel request by the IRQn-DS pin specified by DPSIEGR0 is generated

[Clearing condition]

- Each bit is read as 1 and then written by 0

12.2.11 Deep Standby Interrupt Flag Register 2 (DPSIFR2)

Address(es): 0008 C288h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIF	—	—	DLVD2IF	DLVD1IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DLVD1IF	LVD1 Deep Standby Cancel Flag	0: No cancel request by the voltage monitor 1 signal is generated 1: A cancel request by the voltage monitor 1 signal is generated	R(/W) *1
b1	DLVD2IF	LVD2 Deep Standby Cancel Flag	0: No cancel request by the voltage monitor 2 signal is generated 1: A cancel request by the voltage monitor 2 signal is generated	R(/W) *1
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DNMIF	NMI Deep Standby Cancel Flag	0: No cancel request by the NMI pin is generated 1: A cancel request by the NMI pin is generated	R(/W) *1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Each flag is set to 1 when a cancel request specified by DPSIEGR2 is generated.
Each flag may be set to 1 when a cancel request is generated in any mode (not even deep software standby mode) or when the setting of DPSIER2 is modified. Therefore, a transition to deep software standby mode should be made after DPSIFR2 is cleared to 00h.
To clear DPSIFR2 to 00h after modifying DPSIER2, wait for at least six PCLKB cycles, read DPSIFR2, and then write 0 to DPSIFR2. Six or more PCLKB cycles can be secured, for example, by reading DPSIER2.
DPSIFR2 is not initialized by the internal reset signal used as deep software standby mode canceling source. For details, see Table 7.2, Targets to be Initialized by Each Reset Source.

DLVDmIF Flag (LVDm Deep Standby Cancel Flag) (m = 1 or 2)

This flag indicates that a cancel request by the voltage monitor m signal has been generated.
[Setting condition]

- A cancel request is generated by the voltage monitoring m signal that is selected in DPSIEGR2

[Clearing condition]

- This bit is read as 1 and then written by 0

DNMIF Flag (NMI Deep Standby Cancel Flag)

This flag indicates that a cancel request by the NMI pin has been generated.
[Setting condition]

- A cancel request by the NMI pin specified by DPSIEGR2 is generated

[Clearing condition]

- This bit is read as 1 and then written by 0

12.2.12 Deep Standby Interrupt Edge Register 0 (DPSIEGR0)

Address(es): 0008 C28Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	DIRQ3EG	DIRQ2EG	DIRQ1EG	DIRQ0EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DIRQ0EG	IRQ0-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b1	DIRQ1EG	IRQ1-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b2	DIRQ2EG	IRQ2-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b3	DIRQ3EG	IRQ3-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b4	DIRQ4EG	IRQ4-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b5	DIRQ5EG	IRQ5-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b6	DIRQ6EG	IRQ6-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b7	DIRQ7EG	IRQ7-DS Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR0 is not initialized by the internal reset signal that is the source to cancel the deep software standby mode. For details, see Table 7.2, Targets to be Initialized by Each Reset Source.

12.2.13 Deep Standby Interrupt Edge Register 2 (DPSIEGR2)

Address(es): 0008 C28Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DLVD1EG	LVD1 Edge Select	0: A cancel request is generated when VCC < Vdet1 (fall) is detected 1: A cancel request is generated when VCC ≥ Vdet1 (rise) is detected	R/W
b1	DLVD2EG	LVD2 Edge Select	0: A cancel request is generated when VCC < Vdet2 (fall) is detected 1: A cancel request is generated when VCC ≥ Vdet2 (rise) is detected	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DNMIEG	NMI Edge Select	0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: • Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR2 is not initialized by the internal reset signal that is the source to cancel the deep software standby mode. For details, see Table 7.2, Targets to be Initialized by Each Reset Source.

12.2.14 Deep Standby Backup Register (DPSBKRy) (y = 0 to 31)

Address(es): 0008 C2A0h to 0008 C2BFh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

DPSBKRy is a 32-byte readable/writable register to store data during deep software standby mode.
The value of this register is retained even in deep software standby mode where on-chip RAM data is not retained.
DPSBKRy is not initialized, and the register value is undefined immediately after power-on.

12.3 Reducing Power Consumption by Switching Clock Signals

When the SCKCR.FCK[3:0], ICK[3:0], BCK[3:0], PCKA[3:0], PCKB[3:0], PCKC[3:0] and, PCKD[3:0], bits are set, the clock frequency changes. The CPU, DMAC, DTC, ROM, and RAM operate on the operating clock specified by the ICK[3:0] bits.
The MTU3, GPT, and DPC operates on the operating clock specified by the PCKA[3:0] bits.
Peripheral modules operate on the operating clock specified by the PCKB[3:0] bits.
The AD operates on the operating clock specified by the PCKC[3:0] bits.
The S12AD operates on the operating clock specified by the PCKD[3:0] bits.
The flash memory interface operates on the operating clock specified by the FCK[3:0] bits.
The external bus operates on the operating clock specified by the BCK[3:0] bits. For details, see section 10, Clock Generation Circuit.

12.4 Module-Stop Function

The module-stop function can be set for each on-chip peripheral module.
When the MSTPmi bit (m = A to C, i = 31 to 0) in MSTPCRA to MSTPCRC is set to 1, the specified module-stops operating and enters the module-stop state, but the CPU continues to operate independently. Clearing the MSTPmi bit to 0 cancels the module-stop state, allowing the module to restart operating at the end of the bus cycle. The internal states of modules are retained in the module-stop state.
After a reset is canceled, all modules other than the DMAC, DTC, and on-chip RAM are placed in the module-stop state. Though read/write access cannot be made to the registers of the module that are in the module-stop state, some registers may be written to directly after the setting to the module-stop state. Therefore, care should be paid.

12.5 Low Power Consumption Modes

12.5.1 Sleep Mode

12.5.1.1 Transition to Sleep Mode

When the WAIT instruction is executed while the SBYCR.SSBY bit is 0, the CPU enters sleep mode. In sleep mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop.
When the WDT is used, the WDT stops counting when sleep mode is entered.
Counting by the IWDT stops if a transition to sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to sleep mode is made while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 1.
Furthermore, counting by the IWDT continues if a transition to sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low-power-consumption modes). In the same way, counting by the IWDT continues if a transition to sleep mode is made while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 0.
To use sleep mode, make the following settings and then execute a WAIT instruction.

(1) Clear the PSW.I bit*1 of the CPU to 0.
(2) Set the interrupt destination to be used for recovery from sleep mode to the CPU.
(3) Set the priority*2 of the interrupt to be used for recovery from sleep mode to a level higher than the setting of the PSW.IPL[3:0] bits*1 of the CPU.
(4) Set the IERm.IENj bit*2 for the interrupt to 1.
(5) For the last I/O register to which writing proceeded, read the register to confirm that the value written has been reflected.
(6) Execute the WAIT instruction (this automatically sets the I bit*1 in the PSW of the CPU to 1).

Note 1. For details, see section 2, CPU.
Note 2. For details, see section 15, Interrupt controller (ICUb).

12.5.1.2 Canceling Sleep Mode

Sleep mode is canceled by any interrupt, a RES# pin reset, a power-on reset, a voltage monitoring reset, or a reset caused by an IWDT underflow.

- Canceling by an interrupt
  When an interrupt occurs, sleep mode is canceled and the interrupt exception handling starts. If a maskable interrupt has been masked by the CPU (the priority level*1 of the interrupt has been set to a value lower than that of the PSW.IPL[3:0] bits*2 of the CPU), sleep mode is not canceled.
- Canceling by a RES# pin reset
  When the RES# pin is driven low, the MCU enters the reset state. When the RES# pin is driven high after the reset signal is input for a predetermined time period, the CPU starts the reset exception handling.
- Canceling by a power-on reset
  Sleep mode is canceled by a power-on reset.
- Canceling by a voltage monitoring reset
  Sleep mode is canceled by a voltage monitoring reset from the voltage detection circuit.
- Canceling by an independent watchdog timer reset
  Sleep mode is canceled by an internal reset generated by an IWDT underflow. However, when such conditions are set that stop IWDT counting in sleep mode (OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1), the IWDT is stopped and sleep mode cannot be canceled by the independent watchdog timer reset.

Note 1. For details, see section 15, Interrupt controller (ICUb).
Note 2. For details, see section 2, CPU.

12.5.2 All-Module Clock Stop Mode

12.5.2.1 Transition to All-Module Clock Stop Mode

After setting the MSTPCRA.ACSE bit to 1 and placing modules controlled by MSTPCRA, MSTPCRB, and MSTPCRC registers in the module-stop state (MSTPCRA = FFFF FFFFh, MSTPCRB = FFFF FFFFh, MSTPCRC[31:16] = FFFFh), executing a WAIT instruction while the SBYCR.SSBY bit is 0 stops the bus controller, I/O ports, and all modules except for the POE*4, IWDT, power-on reset circuit, voltage detection circuit at the end of the current bus cycle, and the chip enters all-module clock stop mode*1.

When the WDT is used, the WDT stops counting when all-module clock stop mode is entered.

Counting by the IWDT stops if a transition to all-module clock-stop mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to all-module clock-stop mode is made while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 1.

Furthermore, counting by the IWDT continues if a transition to all-module clock-stop mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low-power-consumption modes). In the same way, counting by the IWDT continues if a transition to all-module clock-stop mode is made while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 0.

To use all-module clock-stop mode, make the following settings and then execute a WAIT instruction.

(1) Clear the PSW.I bit*2 of the CPU to 0.
(2) Set the interrupt destination to be used for recovery from all-module clock stop mode to the CPU.
(3) Set the priority*3 of the interrupt to be used for recovery from all-module clock stop mode to a level higher than the setting of the PSW.IPL[3:0] bits*2 of the CPU.
(4) Set the IERm.IENj bit*3 for the interrupt to be used for recovery from all-module clock stop mode to 1.
(5) Read the last I/O register to have been written and confirm that its value reflects the value written.
(6) Execute a WAIT instruction (executing a WAIT instruction causes automatic setting of the PSW.I bit*2 of the CPU to 1).

Note 1. Transitions to all-module clock stop mode are not to be made in some states of DTC or DMAC operations. Before setting the MSTPCRA.MSTPA28 bit to 1, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC so that the DTC and DMACA are not activated.
Note 2. For details, see section 2, CPU.
Note 3. For details, see section 15, Interrupt controller (ICUb).
Note 4. When a source condition for POE interrupts is satisfied while POE interrupts are enabled and the chip is in all-module clock stop mode, the flag for the source condition is retained but return from all-module clock stop mode does not proceed. If a different source initiates return from all-module clock stop mode in this situation, the POE interrupt is generated after that.

12.5.2.2 Canceling All-Module Clock Stop Mode

Release from all-module clock-stop mode is initiated by an external pin interrupt (the NMI or IRQ0 to IRQ7), a peripheral interrupt (IWDT*1, USB suspend/resume, voltage monitoring 1, voltage monitoring 2, or oscillator-stopped detection interrupt), a RES# pin reset, a power-on reset, a voltage monitoring reset, or an independent watchdog timer reset, and the transition to the normal program execution state proceeds via exception processing for the given interrupt or reset.

However, note that in cases where a maskable interrupt has been masked by the CPU (priority level*2 of the interrupt has been set to a value lower than that of the PSW.IPL[3:0] bits*3 of the CPU) or a maskable interrupt has been set up as a trigger to activate the DTC or DMAC, the interrupt will not cancel all-module clock stop mode.

Note 1. If a condition for the independent watchdog timer to stop counting applied (OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1) at the time of a transition to all-module clock-stop mode, using a reset from the independent watchdog timer to release the chip from all-module clock-stop mode is impossible because the independent watchdog timer is stopped.

Note 2. For details, see section 15, Interrupt controller (ICUb).

Note 3. For details, see section 2, CPU.

12.5.3 Software Standby Mode

12.5.3.1 Transition to Software Standby Mode

When a WAIT instruction is executed with the SBYCR.SSBY bit set to 1 and the DPSBYCR.DPSBY bit cleared to 0, a transition to software standby mode is made. In this mode, the CPU, on-chip peripheral functions, and all the oscillator functions stop. However, the contents of the CPU internal registers, on-chip RAM data, on-chip peripheral functions, and the states of the I/O ports are retained. Whether the address bus and bus control signals are placed in the high-impedance or the output state is retained can be specified by the SBYCR.OPE bit. Software standby mode allows significant reduction in power consumption because the oscillator stops in this mode.
Clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0 before executing the WAIT instruction.
When the WDT is used, the WDT stops counting when software standby mode is entered because the oscillator stops. Counting by the IWDT stops if a transition to software standby mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to software standby mode is made while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 1. Furthermore, counting by the IWDT continues if a transition to software standby mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low-power-consumption modes). In the same way, counting by the IWDT continues if a transition to software standby mode is made while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 0.
When the oscillation stop detection function is enabled (OSTDCR.OSTDE = 1), software standby mode cannot be entered. To make a transition to software standby mode, issue a WAIT instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE = 0).
To use software standby mode, make the following settings and then execute a WAIT instruction.

(1) Clear the PSW.I bit*1 of the CPU to 0.
(2) Set the interrupt destination to be used for recovery from software standby mode to the CPU.
(3) Set the priority*2 of the interrupt to be used for recovery from software standby mode to a level higher than the setting of the PSW.IPL[3:0] bits*1 of the CPU.
(4) Set the IERm.IENj bit*2 for the interrupt to be used for recovery from software standby mode to 1.
(5) For the last I/O register to which writing proceeded, read the register to confirm that the value written has been reflected.
(6) Execute a WAIT instruction (executing a WAIT instruction causes automatic setting of the PSW.I bit*1 of the CPU to 1).

Note 1. For details, see section 2, CPU.
Note 2. For details, see section 15, Interrupt controller (ICUb).

12.5.3.2 Canceling Software Standby Mode

Release from software standby mode is initiated by an external pin interrupt (the NMI or IRQ0 to IRQ7), peripheral interrupts (IWDT, USB suspend/resume, voltage monitoring 1, and voltage monitoring 2 interrupts), an RES# pin reset, a power-on reset, a voltage monitoring reset, or an independent watchdog timer reset. When an interrupt initiates release from software standby, the oscillators which were operating before the transition to software standby are restarted. After the oscillation of all these oscillators has been stabilized, operation returns from software standby mode.

- Canceling by an interrupt
  When an interrupt request from the NMI, IRQ0 to IRQ7, IWDT, USB suspend/resume, voltage monitoring 1, or voltage monitoring 2 interrupt is generated, each oscillator which was operating before a transition to software standby mode resumes oscillation. After the time set by the MOSCWTCR.MSTS[4:0] or PLLWTCR.PSTS[4:0] bits has elapsed, the chip is released from software standby and starts interrupt exception processing.

- Canceling by a RES# pin reset
  Clock oscillation starts when the low level is applied to the RES# pin. Clock supply for the MCU starts at the same time. Keep the level on the RES# pin low over the time required for oscillation of the clocks to become stable. Reset exception processing starts when the high level is applied to the RES# pin.
- Canceling by a power-on reset
  Release from software standby mode proceeds after a fall in the power-supply voltage leads to the generation of a power-on reset.
- Canceling by a voltage monitoring reset
  Release from software standby mode proceeds after a fall in the power-supply voltage leads to the generation of a voltage monitoring reset.
- Canceling by an independent watchdog timer reset
  An internal reset due to an underflow of the IWDT leads to release from software standby mode.
  However, if a condition for the independent watchdog timer to stop counting applied (OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1) at the time of a transition to software standby, using a reset from the independent watchdog timer to release the chip from software standby is impossible because the independent watchdog timer is stopped.

12.5.3.3 Example of Software Standby Mode Application

Figure 12.2 shows an example where a transition to software standby mode is made at the falling edge of the IRQn pin, and software standby mode is canceled at the rising edge of the IRQn pin (n = 0 to 7).
In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits (i = 0 to 7) of the ICU set to 01b (falling edge), and then the IRQCRi.IRQMD[1:0] bits (i = 0 to 7) are set to 10b (rising edge). After that, the SBYCR.SSBY bit is set to 1 and the WAIT instruction is executed. Thus a transition to software standby mode is made. After that, software standby mode is canceled at the rising edge of the IRQn pin.
To return from software standby mode, settings of the interrupt controller (ICU) are also necessary. For details, see section 15, Interrupt controller (ICUb).

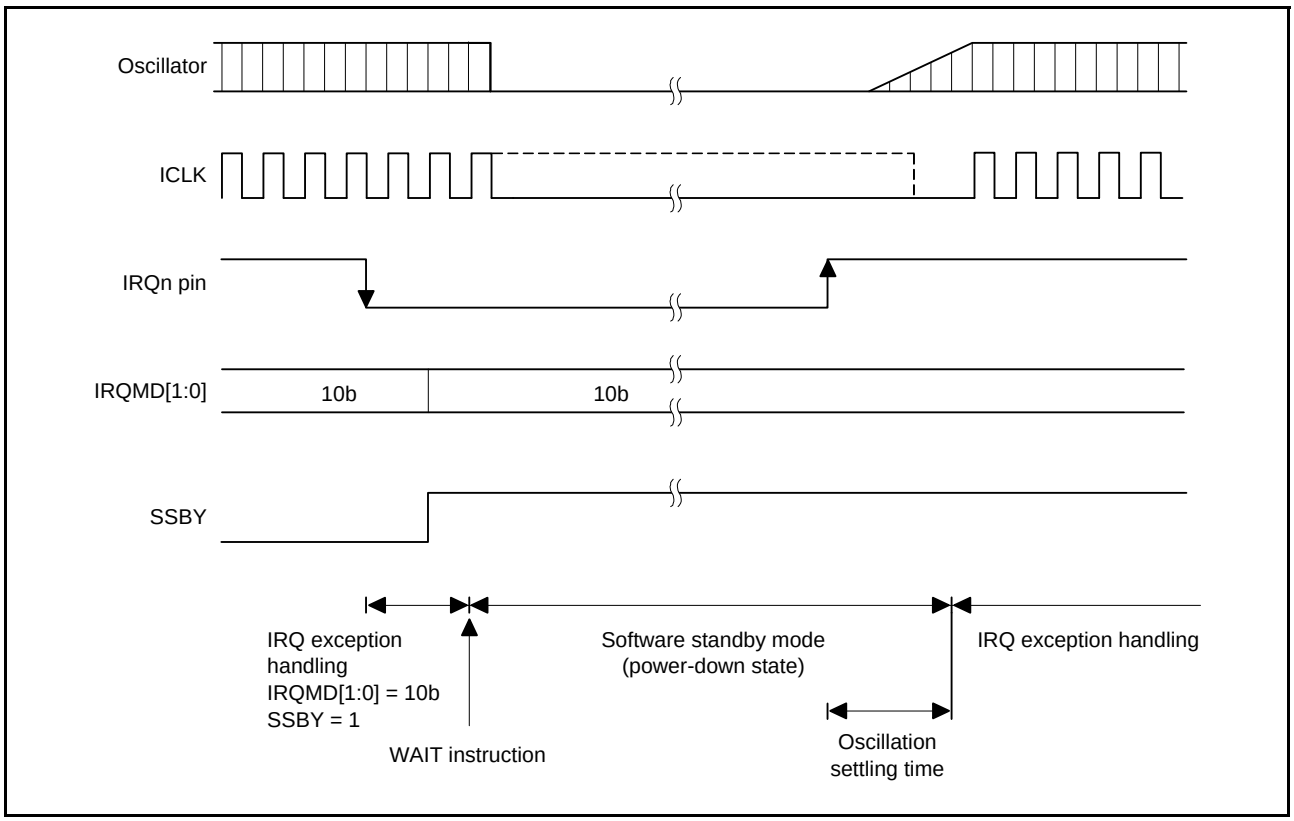


Figure 12.2 Example of Software Standby Mode Application

12.5.4 Deep Software Standby Mode

12.5.4.1 Transition to Deep Software Standby Mode

When the WAIT instruction is executed with the SBYCR.SSBY bit set to 1, a transition to software standby mode*1 is made. At this time, when the DPSBYCR.DPSBY bit is set to 1, a transition to deep software standby mode is made. On deep software standby mode, the CPU, internal peripheral modules, on-chip RAM, and all functions of the oscillators are stopped; furthermore, since the internal supply of power for these modules is stopped, power consumption is markedly reduced. At this time, the contents of all the registers of the CPU and internal peripheral modules become undefined. All data in the on-chip RAM become undefined.

When the WDT is in use, since the oscillators and power supply to the WDT are stopped by the transition to deep software standby mode, counting also stops.

Power supply to the IWDT-dedicated low-speed clock and the IWDT is stopped and counting by the IWDT stops if a transition to deep software standby mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, power supply to the IWDT-dedicated low-speed clock and the IWDT is stopped and counting by the IWDT stops if a transition to deep software standby mode is made while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 1.

Furthermore, counting by the IWDT continues if a transition to software standby mode is made but not to deep software standby mode while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low-power-consumption modes). In the same way, counting by the IWDT continues if a transition to software standby mode is made but not to deep software standby mode while the IWDT is being used in register start mode and the SLCSTP bit in IWDTCSTPR is 0.

When the voltage monitoring 1 reset function (LVD1CR0.LVD1RI = 1) or voltage monitoring 2 reset function (LVD2CR0.LVD2RI = 1) is selected for the voltage detection circuit, a transition to deep software standby mode cannot be made, but to software standby.

The I/O port states remain unchanged from software standby mode.

Note 1. Conditions on the DTC, DMAC, and IWDT for transition to software standby mode should be met before the WAIT instruction is executed. For details, see section 12.5.3, Software Standby Mode.

12.5.4.2 Canceling Deep Software Standby Mode

Release from deep software standby mode is initiated by any of the external pin interrupt source pins (the NMI or IRQ0-DS to IRQ7-DS), peripheral interrupts (voltage monitoring 1 and voltage monitoring 2 interrupts), an RES# pin reset, a power-on reset, or a voltage monitoring 0 reset.

(1) Canceling by an external interrupt pin or internal interrupt signal
Cancellation of deep software standby mode is controlled by DPSIERn (n = 0 or 2) and DPSIFRn (n = 0 or 2). When a deep software standby canceling interrupt is generated, the corresponding flag in DPSIFRn (n = 0 or 2) is set to 1. At this time, if the canceling source is enabled in DPSIERn (n = 0 or 2), deep software standby mode is canceled. Rising edge or falling edge can be selected by DPSIEGRn (n = 0 or 2). The interrupts for which an edge can be selected are the NMI, IRQ0-DS to IRQ7-DS, voltage monitoring 1, and voltage monitoring 2 interrupts.
When a deep software standby mode canceling source is generated, the internal power supply and LOCO clock oscillation begin, and then the internal reset (deep software standby reset) is generated for the entire MCU.
A stable LOCO clock is then supplied to the entire MCU and deep software standby reset is canceled. At the same time, deep software standby mode is canceled and the reset exception handling starts.
When deep software standby mode is canceled by an external interrupt pin or internal interrupt signal, the RSTSR0.DPSRSTF flag is set to 1.

(2) Canceling by a RES# pin reset
Deep software standby mode is canceled when the low level is applied to the RES# pin.
At this time, the RES# pin should be held low according to the specifications described in section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions]. Reset exception processing starts when the high level is applied to the RES# pin.

(3) Canceling by a power-on reset
Release from deep software standby mode proceeds after a fall in the power-supply voltage leads to the generation of a power-on reset.

(4) Canceling by a voltage monitoring 0 reset
Release from deep software standby mode proceeds after a fall in the power-supply voltage leads to the generation of a voltage monitoring 0 reset.

12.5.4.3 Pin States when Deep Software Standby Mode is Canceled

In deep software standby mode, the I/O ports retain the same states from software standby mode. The inside of the MCU is initialized by an internal reset generated when deep software standby mode is canceled. Upon cancellation of deep software standby mode, the reset exception handling starts immediately. The following shows the states of I/O ports at this time.
Whether to initialize the I/O ports or to retain the I/O port states at the time of software standby mode can be selected by the DPSBYCR.IOKEEP bit.

- When the DPSBYCR.IOKEEP bit = 0
  I/O ports are initialized by an internal reset generated when deep software standby mode is canceled.
- When the DPSBYCR.IOKEEP bit = 1
  Although the inside of the MCU is initialized by an internal reset generated when deep software standby mode is canceled, I/O ports retain their states from software standby mode regardless of the MCU internal state. At this time, the I/O port states remain unchanged from software standby mode even if settings of I/O ports or peripheral modules are made. Then, the retained I/O port states are released by clearing the DPSBYCR.IOKEEP bit to 0, and the MCU operates according to the internal state.

The DPSBYCR.IOKEEP bit is not initialized by an internal reset generated when deep software standby mode is canceled.

12.5.4.4 Example of Deep Software Standby Mode Application

Figure 12.3 shows an example where a transition to deep software standby mode is made at the falling edge of the IRQn-DS pin, and deep software standby mode is canceled at the rising edge of the IRQn-DS pin.
In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 01b (falling edge). Then, after the DPSIEGRy.DIRQnEG (y = 0, n = 0 to 7) bit is set to 1 (rising edge) and the SBYCR.SSBY bit and DPSBYCR.DPSBY bit are both set to 1, the WAIT instruction is executed. Thus a transition to deep software standby mode is made.
After that, deep software standby mode is canceled at the rising edge of the IRQ-DS pin.

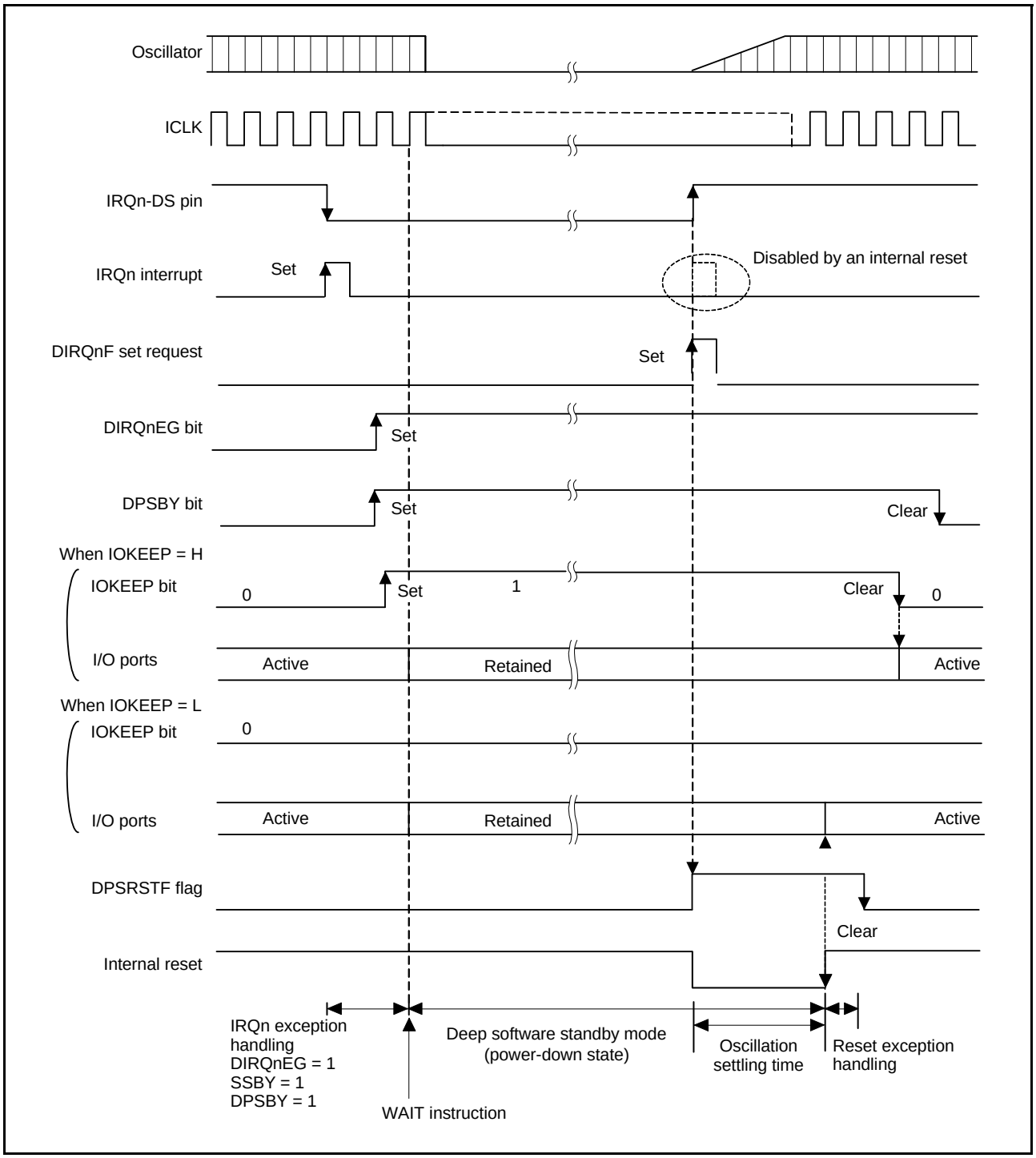


Figure 12.3 Example of Deep Software Standby Mode Application

12.5.4.5 Flowchart to Use Deep Software Standby Mode

Figure 12.4 shows an example of a flowchart to use deep software standby mode.
In this example, the RSTSR0.DPSRSTF flag of the reset function is read after the reset exception handling to determine whether a reset was generated by the RES# pin or by the cancellation of deep software standby mode.
In the case of a reset by the RES# pin, a transition to deep software standby mode is made after the required register settings have been made.
In the case of a reset by the cancellation of deep software standby mode, the DPSBYCR.IOKEEP bit is cleared to 0 after the I/O port settings have been made.

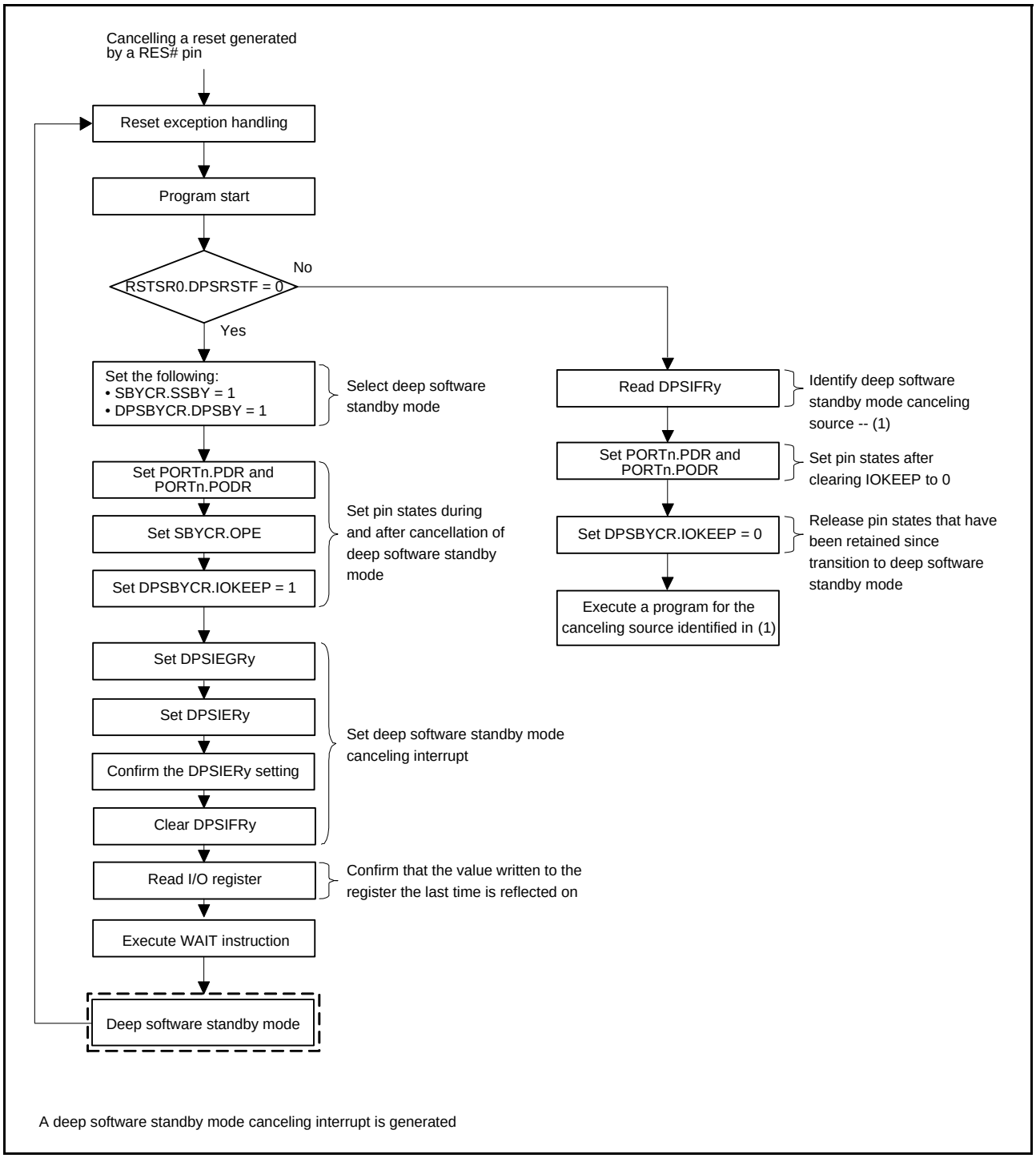


Figure 12.4 Example of Flowchart to Use Deep Software Standby Mode

12.6 Usage Notes

12.6.1 I/O Port States

I/O port states are retained in software standby mode and deep software standby mode. Therefore, the supply current is not reduced while output signals are held high.

12.6.2 Module-Stop State of DMAC and DTC

Before setting the MSTPCRA.MSTPA28 bit to 1, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0 so that the DMAC and DTC are not activated.
For details, see section 18, DMA Controller (DMACA) and section 19, Data Transfer Controller (DTCa).

12.6.3 On-Chip Peripheral Module Interrupts

Interrupts do not operate in the module-stop state. Therefore, if the module-stop state is made after an interrupt request is generated, a CPU interrupt source or a DMAC or DTC startup source cannot be cleared. For this reason, disable interrupts before entering the module-stop state.

12.6.4 Write Access to MSTPCRA, MSTPCRB, and MSTPCRC

Write accesses to MSTPCRA, MSTPCRB, and MSTPCRC should be made only by the CPU.

12.6.5 Input Buffer Control by DIRQnE Bit (n = 0 to 7)

Setting the DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 7) bit to 1 enables the input buffer of the IRQ0-DS to IRQ7-DS pins. Therefore, note that, although inputs to these pins are sent to the DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 7) bits, they are not sent to the interrupt controller, peripheral modules, and I/O ports.

12.6.6 Timing of Wait Instructions

The WAIT instruction is executed before completion of the preceding register write. The WAIT instruction may be executed before the change to the setting of an I/O register is reflected, in which case operation may not be as intended. To avoid this, always execute the WAIT instruction after confirming that the last write to the register has completed.

12.6.7 Rewrite the Register by DMAC and DTC in Sleep Mode

The WDT stops in sleep mode. Do not set up the DMACA and DTC to rewrite any registers related to the WDT while the chip is in sleep mode.
According to the settings of the OFS0.IWDTSLCSTP bit and IWDTCSTPR.SLCSTP bit, the IWDT may also stop in sleep mode. If that is the case, do not set up the DMAC and DTC to rewrite any registers related to the IWDT in sleep mode.

12.6.8 Points for Caution on Return from Software Standby

When interrupts IRQ0 to IRQ7 are not set as triggers for release from software standby, the corresponding input buffers become invalid on software standby, so the input signal within the MCU is fixed to the high level. Accordingly, depending on the state of the pin, a transition to software standby may set the interrupt status flag (ICU.IRi.IR) to 1. When placing the chip on software standby, execute the WAIT instruction after setting the IERi.IENj bits to prohibit whichever of interrupts IRQ0 to IRQ7 are not to be used as triggers for release from standby. Moreover, after return from software standby, clear the interrupt status flags.

13. Register Write Protection Function

The register write protection function protects important registers from being overwritten for in case a program runs out of control. The registers to be protected are set with the protect register (PRCR).

Table 13.1 lists the association between the PRCR bits and the registers to be protected.

Table 13.1 Association between PRCR Bits and Registers to be Protected

PRCR Bit	Register to be Protected
PRC0	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, LOCOCR, ILOCOCR, OSTDCR, OSTDSR
PRC1	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2 • Registers related to clock generation circuit: MOFCR • Software reset register: SWRR
PRC3	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

13.1 Register Descriptions

13.1.1 Protect Register (PRCR)

Address(es): 0008 03FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the clock generation circuit. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to operating modes, low power consumption, and software reset. 0: Write disabled 1: Write enabled	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD. 0: Write disabled 1: Write enabled	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control permission and prohibition of writing to the PRCR register. To modify the PRCR register, write A5h to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W)*1

Note 1. Write data is not retained.

PRCi Bits (Protect Bit i) (i = 0, 1, 3)

These bits enable or disable writing to the corresponding registers to be protected.

Setting the PRCi bits to 1 and 0 enables and disables writing to the corresponding registers to be protected, respectively.

14. Exception Handling

14.1 Exception Events

During execution of a program by the CPU, the occurrence of a certain event may cause execution of that program to be suspended and execution of another program to be started. Such kinds of events are called exception events.
The RX CPU supports seven types of exceptions. The types of exception events are shown in Figure 14.1.
The occurrence of an exception causes the processor mode to shift to supervisor mode.

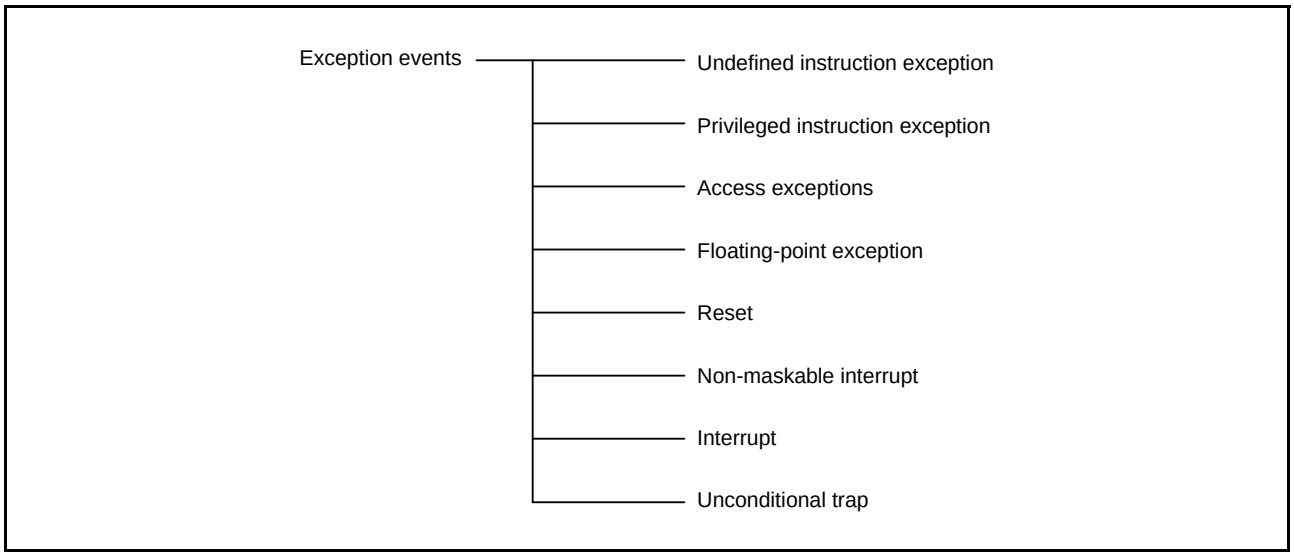


Figure 14.1 Types of Exception Events

14.1.1 Undefined Instruction Exception

An undefined instruction exception occurs when execution of an undefined instruction (an instruction not implemented) is detected.

14.1.2 Privileged Instruction Exception

A privileged instruction exception occurs when execution of a privileged instruction is detected in user mode. Privileged instructions can be executed only in supervisor mode.

14.1.3 Access Exceptions

An access exception occurs when an error is detected in access to memory by the CPU. If the memory-protection unit detects an instruction memory-protection error, an instruction-access exception occurs, and if the unit detects a data memory protection error, an operand-access exception occurs.

14.1.4 Floating-Point Exception

Floating-point exceptions include the five exception events (overflow, underflow, inexact, division-by-zero, and invalid operation) specified in the IEEE754 standard and another floating-point exception that is generated on detection of unimplemented processing. The exception handling of floating-point exceptions is prohibited when the EX, EU, EZ, EO, or EV bit in FPSW is 0.

14.1.5 Reset

A reset is generated by input of a reset signal to the CPU. This has the highest priority of any exception and is always accepted.

14.1.6 Non-Maskable Interrupt

The non-maskable interrupt is generated by input of a non-maskable interrupt signal to the CPU and is only used when a fatal fault is considered to have occurred in the system. Never use the non-maskable interrupt with an attempt to return to the program that was being executed at the time of interrupt generation after the exception handling routine is ended.

14.1.7 Interrupt

Interrupts are generated by the input of interrupt signals to the CPU. A fast interrupt can be selected as the interrupt with the highest priority. In the case of the fast interrupt, hardware pre-processing and hardware post-processing are handled fast. The priority level of the fast interrupt is 15 (the highest). The exception handling of interrupts is masked when the I bit in PSW is 0.

14.1.8 Unconditional Trap

An unconditional trap is generated when the INT or BRK instruction is executed.

14.2 Exception Handling Procedure

In the exception handling, part of the processing is handled automatically by hardware and part of it is handled by a program (exception handling routine) that has been written by the user. Figure 14.2 shows the processing procedure when an exception other than a reset is accepted.

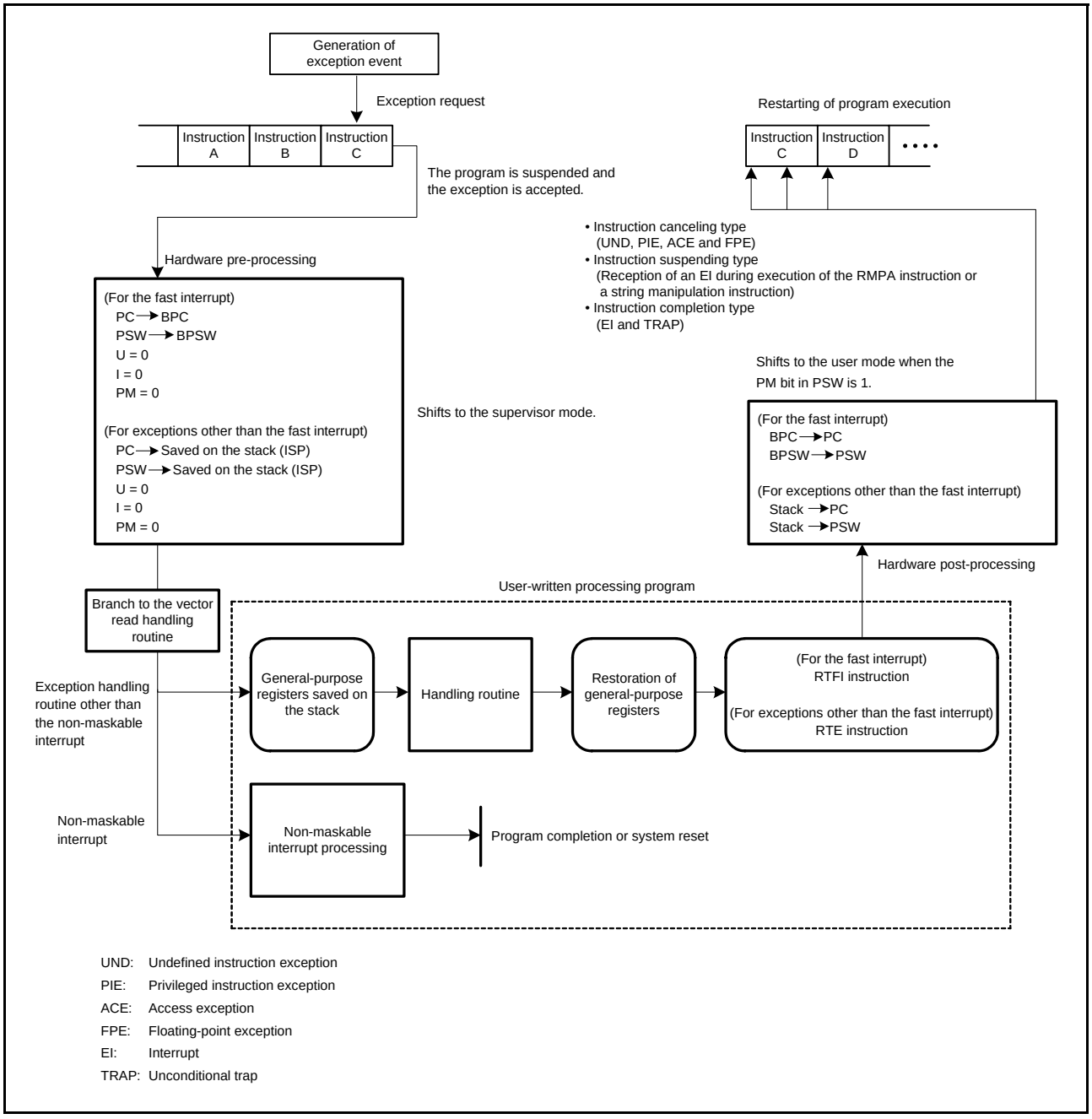


Figure 14.2 Outline of Exception Handling Procedure

When an exception is accepted, hardware processing by the RX CPU is followed by access to the vector to acquire the address of the branch destination. In the vector, a vector address is allocated to each exception, and the branch destination address of the exception handling routine is written to each vector address.

Hardware pre-processing by the RX CPU handles saving of the contents of the program counter (PC) and processor status word (PSW). In the case of a fast interrupt, the contents are saved in the backup PC (BPC) and the backup PSW (BPSW), respectively. In the case of exceptions other than a fast interrupt, the contents are saved in the stack area.

General purpose registers and control registers other than the PC and PSW that are to be used within the exception

handling routine must be saved on the stack by a user program at the start of the exception handling routine.
On completion of processing by an exception handling routine, registers saved on the stack are restored and the RTE instruction is executed to restore execution from the exception handling routine to the original program. For return from a fast interrupt, the RTFI instruction is used instead. In the case of a non-maskable interrupt, however, finish the program or reset the system without returning to the original program.
Hardware post-processing by the RX CPU handles restoration of the contents of PC and PSW. In the case of a fast interrupt, the values of BPC and BPSW are restored to PC and PSW, respectively. In the case of exceptions other than a fast interrupt, the values are restored from the stack to PC and PSW.

14.3 Acceptance of Exception Events

When an exception occurs, the CPU suspends the execution of the program and processing branches to the exception handling routine.

14.3.1 Acceptance Timing and Saved PC Value

Table 14.1 lists the timing of acceptance and the program counter (PC) value to be saved for each exception event.

Table 14.1 Acceptance Timing and Saved PC Value

Exception Event		Type of Handling	Acceptance Timing	Value Saved in BPC or on the Stack
Undefined instruction exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Privileged instruction exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Access exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Floating-point exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Reset		Instruction abandonment type	Any machine cycle	None
Non-maskable interrupt	During execution of the RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions	Instruction suspending type	During instruction execution	PC value of the instruction being executed
	Other than above	Instruction completion type	At the next break between instructions	PC value of the next instruction
Interrupt	During execution of the RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions	Instruction suspending type	During instruction execution	PC value of the instruction being executed
	Other than above	Instruction completion type	At the next break between instructions	PC value of the next instruction
Unconditional trap		Instruction completion type	At the next break between instructions	PC value of the next instruction

14.3.2 Vector and Site for Saving the Values in the PC and PSW

The vector for each type of exception and the site for saving the values of the program counter (PC) and processor status word (PSW) are listed in Table 14.2.

Table 14.2 Vector and Site for Saving the Values in the PC and PSW

Exception		Vector	Site for Saving the Values in the PC and PSW
Undefined instruction exception		Fixed vector table	Stack
Privileged instruction exception		Fixed vector table	Stack
Access exception		Fixed vector table	Stack
Floating-point exception		Fixed vector table	Stack
Reset		Fixed vector table	Nowhere
Non-maskable interrupt		Fixed vector table	Stack
Interrupt	Fast interrupt	FINTV	BPC and BPSW
	Other than above	Relocatable vector table (INTB)	Stack
Unconditional trap		Relocatable vector table (INTB)	Stack

14.4 Hardware Processing for Accepting and Returning from Exceptions

This section describes the hardware processing for accepting and returning from exceptions other than a reset.

(1) Hardware Pre-Processing for Accepting an Exception

(a) Saving PSW

- For a fast interrupt
  PSW → BPSW
- For exceptions other than a fast interrupt
  PSW → Stack

Note: • The values in FPSW are not saved by hardware pre-processing. Therefore, if floating-point instructions are to be used within an exception handling routine, the user must save these values on the stack within the exception handling routine.

(b) Updating PM, U, and I Bits in PSW

I: Set to 0
U: Set to 0
PM: Set to 0

(c) Saving PC

- For a fast interrupt
  PC → BPC
- For exceptions other than a fast interrupt
  PC → Stack

(d) Setting Branch Destination Address of Exception Handling Routine in PC

Processing is shifted to the exception handling routine by acquiring the vector corresponding to the exception and then branching accordingly.

(2) Hardware Post-Processing for Execution of RTE and RTFI Instructions

(a) Restoring PSW

- For a fast interrupt
  BPSW → PSW
- For exceptions other than a fast interrupt
  Stack → PSW

(b) Restoring PC

- For a fast interrupt
  BPC → PC
- For exceptions other than a fast interrupt
  Stack → PC

14.5 Hardware Pre-Processing

The hardware pre-processing from reception of each exception request to execution of the associated exception handling routine are explained below.

14.5.1 Undefined Instruction Exception

1. The value of the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from address FFFF FFDCh.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.2 Privileged Instruction Exception

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from address FFFF FFD0h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.3 Access Exceptions

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from address FFFFFFD4h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.4 Floating-Point Exception

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from address FFFF FFE4h.

5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.5 Reset

1. The control registers are initialized.
2. The vector is fetched from address FFFF FFFCh.
3. The fetched vector is set to the PC.

14.5.6 Non-Maskable Interrupt

1. The value of the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. If the interrupt was generated during the execution of an RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, or SWHILE instruction, the value of the program counter (PC) for that instruction is saved on the stack (ISP). For other instructions, the PC value of the next instruction is saved.
4. The processor interrupt priority level bits (IPL[3:0]) in PSW are set to Fh.
5. The vector is fetched from address FFFF FFF8h.
6. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.7 Interrupt

1. The value of the processor status word (PSW) is saved on the stack (ISP) or, for the fast interrupt, in the backup PSW (BPSW).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. If the interrupt was generated during the execution of an RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, or SWHILE instruction, the value of the program counter (PC) for that instruction is saved. For other instructions, the PC value of the next instruction is saved. Saving of the PC is in the backup PC (BPC) for fast interrupts.
4. The processor interrupt priority level bits (IPL[3:0]) in PSW indicate the interrupt priority level of the interrupt.
5. The vector for an interrupt source other than the fast interrupt is fetched from the relocatable vector table. For the fast interrupt, the address is fetched from the fast interrupt vector register (FINTV).
6. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.8 Unconditional Trap

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) for the next instruction is saved on the stack (ISP).
4. For the INT instruction, the value at the vector corresponding to the INT instruction number is fetched from the relocatable vector table.
   For the BRK instruction, the value at the vector from the start address is fetched from the relocatable vector table.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.6 Return from Exception Handling Routine

Executing the instruction listed in Table 14.3 at the end of the corresponding exception handling routine restores the values of the program counter (PC) and processor status word (PSW) that were saved on the stack or in the control registers (BPC and BPSW) immediately before the exception handling sequence.

Table 14.3 Return from Exception Handling Routine

Exception		Instruction for Return
Undefined instruction exception		RTE
Privileged instruction exception		RTE
Access exception		RTE
Floating-point exception		RTE
Reset		Return is impossible
Non-maskable interrupt		Return is impossible
Interrupt	Fast interrupt	RTFI
	Other than above	RTE
Unconditional trap		RTE

14.7 Priority of Exception Events

The priority of exception events is listed in Table 14.4. When multiple exceptions are generated at the same time, the exception with the highest priority is accepted first.

Table 14.4 Priority of Exception Events

Priority		Exception Event
High	1	Reset
↑	2	Non-maskable interrupt
	3	Interrupt
	4	Instruction access exception
	5	Undefined instruction exception Privileged instruction exception
	6	Unconditional trap
	7	Operand access exception
Low	8	Floating-point exception

15. Interrupt controller (ICUb)

15.1 Overview

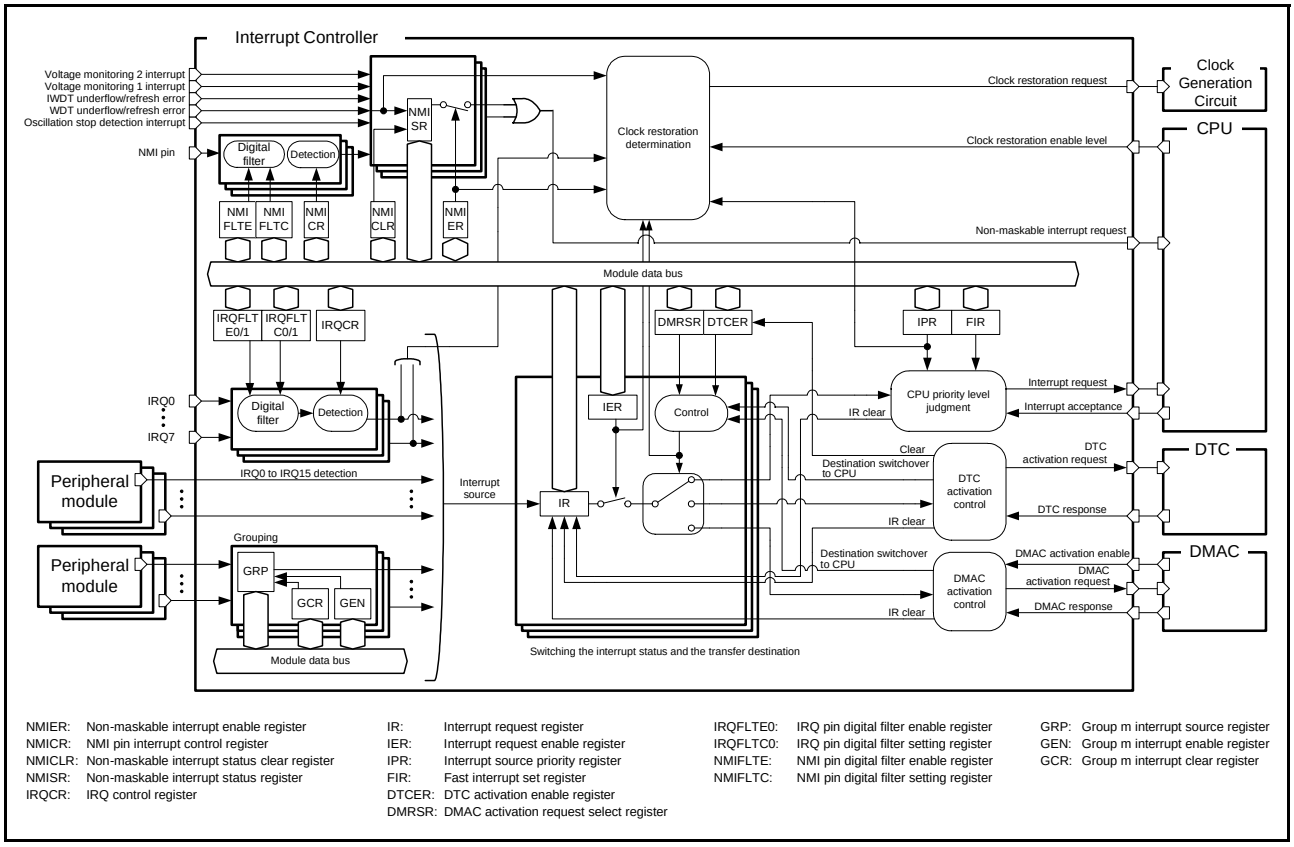
The interrupt controller receives interrupt signals from the peripheral modules and external pins, sends interrupts to the CPU, and activates the DTC and DMAC.

Table 15.1 lists the specifications of the interrupt controller, and Figure 15.1 shows a block diagram of the interrupt controller.

Table 15.1 Specifications of Interrupt Controller

Item		Description
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules. • Interrupt grouping: Multiple interrupt requests can be allocated to a single interrupt vector. Number of groups for edge detection interrupts: 1 (group 0) Number of groups for level detection interrupts: 1 (group 12)
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 (max) • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source. • Digital filter function: supported
	Software interrupt	• Interrupt generated by writing to a register • One interrupt source
	Interrupt priority	Specified by registers.
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC/DMAC control	The DTC and DMAC can be activated by interrupt sources.*1
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped
	WDT underflow/ refresh error	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/ refresh error	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Voltage-monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)
	Voltage-monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)
Return from power-down modes		• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • All-module clock stop mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or USB resume interrupts. • Software standby mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or USB resume interrupts.

Note 1. For the DTC and DMAC activation sources, refer to Table 15.3, Interrupt Vector Table.



NMIER: Non-maskable interrupt enable register
NMICR: NMI pin interrupt control register
NMICLR: Non-maskable interrupt status clear register
NMISR: Non-maskable interrupt status register
IRQCR: IRQ control register

IR: Interrupt request register
IER: Interrupt request enable register
IPR: Interrupt source priority register
FIR: Fast interrupt set register
DTCER: DTC activation enable register
DMRSR: DMAC activation request select register

IRQFLTE0: IRQ pin digital filter enable register
IRQFLTC0: IRQ pin digital filter setting register
NMIFLTE: NMI pin digital filter enable register
NMIFLTC: NMI pin digital filter setting register

GRP: Group m interrupt source register
GEN: Group m interrupt enable register
GCR: Group m interrupt clear register

Figure 15.1 Block Diagram of Interrupt Controller

Table 15.2 lists the input/output pins of the interrupt controller.

Table 15.2 Pin Configuration of Interrupt Controller

Pin Name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0 to IRQ7	Input	External interrupt request pins

15.2 Register Descriptions

15.2.1 Interrupt Request Register n (IRn) (n = interrupt vector number)

Address(es): 0008 7010h to 0008 70FCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IR	Interrupt Status Flag	0: No interrupt request is generated 1: An interrupt request is generated	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. For an edge detection interrupt, only 0 can be written to this bit; do not write 1.
For a level detection interrupt, neither 0 nor 1 can be written.

IRn is provided for each interrupt source, where “n” indicates the interrupt vector number.
For the correspondence between interrupt sources and interrupt vector numbers, see Table 15.3, Interrupt Vector Table.

IR Flag (Interrupt Status Flag)

This bit is the status flag of an individual interrupt request. This flag is set to 1 when the corresponding interrupt request is generated. To detect an interrupt request, the interrupt request output should be enabled by the corresponding peripheral module interrupt enable bit.
There are two interrupt request detection methods: edge detection and level detection. For interrupts from peripheral modules, either edge detection or level detection is determined per interrupt source. For interrupts from IRQi pins, edge detection or level detection is selected by the setting of the IRQMD[1:0] bits in the corresponding IRQCRi (i = 0 to 7).
For detection of the various interrupt sources, see Table 15.3, Interrupt Vector Table.
Grouped interrupt requests are detected using group m interrupt source register (GRPm; m = group number). The interrupt request detected by GRPm is further detected as a level detection interrupt request by the IR flag corresponding to the group. For details of the interrupt grouping function, see section 15.4, Peripheral Module Interrupt Request Grouping.
For grouped interrupt requests, see Table 15.4, Group m Interrupt Requests (1/2).

(1) Edge detection

[Setting condition]

- The flag is set to 1 in response to the generation of an interrupt request from the corresponding peripheral module or IRQi pin. For interrupt generation by the various peripheral modules, refer to the sections describing the modules.

[Clearing conditions]

- The flag is cleared to 0 when the interrupt request destination accepts the interrupt request.
- The IR flag is cleared to 0 by writing 0 to it. Note, however, that writing 0 to the IR flag is prohibited if the destination of the interrupt request is the DTC or DMAC.

(2) Level detection

[Setting conditions]

- The flag remains set to 1 while an interrupt request is being sent from the corresponding peripheral module or IRQi pin. For interrupt generation by the various peripheral modules, refer to the sections describing the modules.
- For grouped interrupt requests, the flag is set to 1 when both the interrupt request enable bit j in group m interrupt enable register (GENm.ENj; m = group number and j = bit number) and interrupt status flag in group m interrupt source register (GRPm.ISj) are 1.

[Clearing conditions]

- The flag is cleared to 0 when the source of the interrupt request is cleared (it is not cleared when the interrupt request destination accepts the interrupt request). For clearing interrupts from the various peripheral modules, refer to the sections describing the modules.
- For grouped interrupt requests, the flag is cleared to 0 when either the GENm.ENj bit or GRPm.ISj flag is 0.

When level detection has been selected for an IRQi pin, the interrupt request is withdrawn by driving the IRQi pin high. Do not write 0 or 1 to the IR flag while level detection is selected.

15.2.2 Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh)

Address(es): 0008 7202h to 0008 721Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IEN0	Interrupt Request Enable 0	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b1	IEN1	Interrupt Request Enable 1		R/W
b2	IEN2	Interrupt Request Enable 2		R/W
b3	IEN3	Interrupt Request Enable 3		R/W
b4	IEN4	Interrupt Request Enable 4		R/W
b5	IEN5	Interrupt Request Enable 5		R/W
b6	IEN6	Interrupt Request Enable 6		R/W
b7	IEN7	Interrupt Request Enable 7		R/W

Note: • Write 0 to the bit that corresponds to the vector number for reservation. These bits are read as 0.

IENj Bits (Interrupt Request Enable j) (j = 7 to 0)

When an IENj bit is 1, the corresponding interrupt request will be output to the destination selected for the request.
When an IENj bit is 0, the corresponding interrupt request will not be output to the destination selected for the request.
The setting of an IENj bit does not affect the IRn.IR flag. Even if the corresponding IENj bit is 0, the IR flag value changes according to the descriptions in section 15.2.1, Interrupt Request Register n (IRn) (n = interrupt vector number).
The IERm.IENj bit is set for each request source (vector number).
For the correspondence between interrupt sources and IERm.IENj bits, see Table 15.3, Interrupt Vector Table.
For the procedure for setting IERm.IENj bits during the selection of destinations for interrupt requests, refer to section 15.5.3, Selecting Interrupt Request Destinations.

15.2.3 Interrupt Source Priority Register n (IPRn) (n = 000 to 250)

Address(es): 0008 7300h to 0008 73FAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	IPR[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IPR[3:0]	Interrupt Priority Level Select	b3 b0 0 0 0 0: Level 0 (interrupt disabled)*1 0 0 0 1: Level 1 0 0 1 0: Level 2 0 0 1 1: Level 3 0 1 0 0: Level 4 0 1 0 1: Level 5 0 1 1 0: Level 6 0 1 1 1: Level 7 1 0 0 0: Level 8 1 0 0 1: Level 9 1 0 1 0: Level 10 1 0 1 1: Level 11 1 1 0 0: Level 12 1 1 0 1: Level 13 1 1 1 0: Level 14 1 1 1 1: Level 15 (highest)	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the interrupt is specified as a fast interrupt, it can be issued even if the priority level is level 0.

For the correspondence between interrupt sources and IPRn registers, see Table 15.3, Interrupt Vector Table.

IPR[3:0] Bits (Interrupt Priority Level Select)

These bits specify the priority level of the corresponding interrupt source.

Priority levels specified by the IPR[3:0] bits are used only to determine the priority of interrupt requests to be transferred to the CPU, and do not affect activation requests to the DTC and DMAC.

The CPU accepts only interrupt requests higher than the priority level specified by the IPL[3:0] bits in PSW, and handles accepted interrupts.

If two or more interrupt requests are generated at the same time, their priority levels are compared with the value of the IPR[3:0] bits. If interrupt requests of the same priority level are generated at the same time, an interrupt source with a smaller vector number takes precedence.

These bits should be written to while an interrupt request is disabled (IERm.IENj bit = 0).

15.2.4 Fast Interrupt Set Register (FIR)

Address(es): 0008 72F0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIEN	—	—	—	—	—	—	—	FVCT[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	FVCT[7:0]	Fast Interrupt Vector Number	Specify the vector number of an interrupt source to be a fast interrupt.	R/W
b14 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	FIEN	Fast Interrupt Enable	0: Fast interrupt is disabled 1: Fast interrupt is enabled	R/W

The fast interrupt function based on the FIR register setting is applicable only to interrupts to the CPU. It will not affect any transfer request to the DTC or DMAC.
Before writing to this register, be sure to disable interrupt requests (IERm.IENj bit = 0).

FVCT[7:0] Bits (Fast Interrupt Vector Number)

The FVCT[7:0] bits specify the vector number of an interrupt source that uses the fast interrupt function.

FIEN Bit (Fast Interrupt Enable)

This bit enables the fast interrupt.
Setting this bit to 1 makes the interrupt request of the vector number specified by the FVCT[7:0] bits a fast interrupt. When an interrupt request of the vector number specified by the FVCT[7:0] bits is generated and the interrupt request destination is the CPU while the FIEN bit is 1, the interrupt request is output to the CPU as a fast interrupt regardless of the setting of the IPRn register. When using the fast interrupt for returning from the software standby mode, see section 15.7.3, Return from Software Standby Mode.
If the setting of the IERm.IENj (m = 02h to 1Fh, j = 7 to 0) bit has disabled interrupt requests from the interrupt source with the vector number in this register, fast interrupt requests are not output to the CPU.
For settable vector numbers, see Table 15.3, Interrupt Vector Table.
Do not write any reserved vector numbers to the FVCT[7:0] bits.

For details on the fast interrupt, see section 14, Exception Handling, and section 15.5.6, Fast Interrupt.

15.2.5 Software Interrupt Activation Register (SWINTR)

Address(es): 0008 72E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SWINT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWINT	Software Interrupt Activation	This bit is read as 0. Writing 1 issues a software interrupt request. Writing 0 to this bit has no effect.	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written.

SWINT Bit (Software Interrupt Activation)

When 1 is written to the SWINT bit, the interrupt request register 027 (IR027) is set to 1.
If 1 is written to the SWINT bit when the DTC activation enable register 027 (DTCER027) is set to 0, an interrupt to the CPU is generated.
If 1 is written to the SWINT bit when the DTC activation enable register 027 (DTCER027) is set to 1, a DTC activation request is issued.

15.2.6 DTC Activation Enable Register n (DTCERn) (n = interrupt vector number)

Address(es): 0008 711Bh to 0008 71FBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DTCE	DTC Activation Enable	0: DTC activation is disabled 1: DTC activation is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

An interrupt source that has been selected as a source for DMAC activation should not be specified as a source for DTC activation. See Table 15.3, Interrupt Vector Table, for the interrupt sources that are selectable as sources for DTC activation.

DTCE Bit (DTC Activation Enable)

When the DTCE bit is set to 1, the corresponding interrupt source is selected as the source for the DTC activation.

[Setting condition]

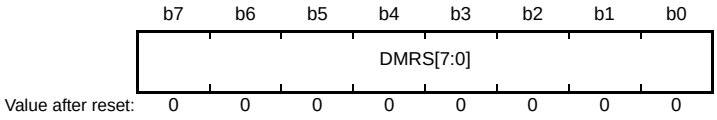
- When 1 is written to the DTCE bit

[Clearing conditions]

- When the specified number of transfers is completed (for the chain transfer, the number of transfers for the last chain transfer is completed)
- When 0 is written to the DTCE bit

15.2.7 DMAC Activation Request Select Register m (DMRSRm) (m = DMAC channel number)

Address(es): DMRSR0 0008 7400h, DMRSR1 0008 7404h
DMRSR2 0008 7408h, DMRSR3 0008 740Ch



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	DMRS[7:0]	DMAC Activation Source Select	These bits specify the vector number for the DMAC activation request.	R/W

To specify the same interrupt source for multiple DMRSRm registers is disabled. The interrupt source that has been selected for the DMRSRm activation should not be specified as the source for the DTC activation. Otherwise, the correct operation is not guaranteed.

DMRS[7:0] Bits (DMAC Activation Source Select)

The vector number of the interrupt source for DMAC activation is specified in 8 bits. Do not set the vector numbers that are not assigned for the DMAC activation.

For the correspondence between interrupt sources and interrupt vector numbers, see Table 15.3, Interrupt Vector Table.

Write to the DMRSRm register while the DMA transfer enable bit of the DMA transfer enable register (DMACm.DMCNT.DTE) is cleared to 0.

15.2.8 IRQ Control Register i (IRQCRi) (i = 0 to 7)

Address(es): 0008 7500h to 0008 7507h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	IRQMD[1:0]		—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3, b2	IRQMD[1:0]	IRQ Detection Sense Select	b3 b2 0 0: Low level 0 1: Falling edge 1 0: Rising edge 1 1: Rising and falling edges	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only change the settings of this register while the corresponding interrupt request enable bit is prohibiting the interrupt request (IENj bit in IERm is 0). After changing the setting, clear the IR flag in IRn before setting the interrupt enable bit. However, when the change is to the low level, the IR flag does not require clearing.

IRQMD[1:0] Bits (IRQ Detection Sense Select)

These bits select the detection sensing method of external pin interrupt sources IRQ0 to IRQ7.
For the external pin interrupt detection setting, see section 15.5.8, External Pin Interrupts.

15.2.9 IRQ Pin Digital Filter Enable Register 0 (IRQFLTE0)

Address(es): 0008 7510h

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FLTEN0	IRQ0 Digital Filter Enable	0: Digital filter is disabled. 1: Digital filter is enabled.	R/W
b1	FLTEN1	IRQ1 Digital Filter Enable		R/W
b2	FLTEN2	IRQ2 Digital Filter Enable		R/W
b3	FLTEN3	IRQ3 Digital Filter Enable		R/W
b4	FLTEN4	IRQ4 Digital Filter Enable		R/W
b5	FLTEN5	IRQ5 Digital Filter Enable		R/W
b6	FLTEN6	IRQ6 Digital Filter Enable		R/W
b7	FLTEN7	IRQ7 Digital Filter Enable		R/W

FLTENi Bits (IRQi Digital Filter Enable) (i = 0 to 7)

These bits enable the digital filter used for the external pin interrupt sources IRQ0 to IRQ7.

The digital filter is enabled when the FLTENi bit is 1, and disabled when the FLTENi bit is 0.

The IRQi pin level is sampled at the sampling clock cycle specified with the IRQFLTC0.FCLKSELi[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.

For details of the digital filter, see section 15.5.7, Digital Filter.

15.2.10 IRQ Pin Digital Filter Setting Register 0 (IRQFLTC0)

Address(es): 0008 7514h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FCLKSEL7[1:0]		FCLKSEL6[1:0]		FCLKSEL5[1:0]		FCLKSEL4[1:0]		FCLKSEL3[1:0]		FCLKSEL2[1:0]		FCLKSEL1[1:0]		FCLKSEL0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	FCLKSEL0[1:0]	IRQ0 Digital Filter Sampling Clock	0 0: PCLK 0 1: PCLK/8 1 0: PCLK/32 1 1: PCLK/64	R/W
b3, b2	FCLKSEL1[1:0]	IRQ1 Digital Filter Sampling Clock		R/W
b5, b4	FCLKSEL2[1:0]	IRQ2 Digital Filter Sampling Clock		R/W
b7, b6	FCLKSEL3[1:0]	IRQ3 Digital Filter Sampling Clock		R/W
b9, b8	FCLKSEL4[1:0]	IRQ4 Digital Filter Sampling Clock		R/W
b11, b10	FCLKSEL5[1:0]	IRQ5 Digital Filter Sampling Clock		R/W
b13, b12	FCLKSEL6[1:0]	IRQ6 Digital Filter Sampling Clock		R/W
b15, b14	FCLKSEL7[1:0]	IRQ7 Digital Filter Sampling Clock		R/W

FCLKSELi[1:0] Bits (IRQi Digital Filter Sampling Clock) (i = 0 to 7)

These bits select the cycle of the digital filter sampling clock for the external pin interrupt request pins IRQ0 to IRQ7. The sampling clock cycle can be selected from among the PCLK (every cycle), PCLK/8 (once every eight cycles), PCLK/32 (once every 32 cycles), and PCLK/64 (once every 64 cycles).

For details of the digital filter, see section 15.5.7, Digital Filter.

15.2.11 Non-Maskable Interrupt Status Register (NMISR)

Address(es): 0008 7580h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD2ST	LVD1ST	IWDTST	WDTST	OSTST	NMIST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMIST	NMI Status Flag	0: NMI pin interrupt is not requested. 1: NMI pin interrupt is requested.	R
b1	OSTST	Oscillation Stop Detection Interrupt Status Flag	0: Oscillation stop detection interrupt is not requested. 1: Oscillation stop detection interrupt is requested.	R
b2	WDTST	WDT Underflow/Refresh Error Status Flag	0: WDT underflow/refresh error interrupt is not requested. 1: WDT underflow/refresh error interrupt is requested.	R
b3	IWDTST	IWDT Underflow/Refresh Error Status Flag	0: IWDT underflow/refresh error interrupt is not requested. 1: IWDT underflow/refresh error interrupt is requested.	R
b4	LVD1ST	Voltage-Monitoring 1 Interrupt Status Flag	0: Voltage-monitoring 1 interrupt is not requested. 1: Voltage-monitoring 1 interrupt is requested.	R
b5	LVD2ST	Voltage-Monitoring 2 Interrupt Status Flag	0: Voltage-monitoring 2 interrupt is not requested. 1: Voltage-monitoring 2 interrupt is requested.	R
b7, b6	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

The NMISR register monitors the status of a non-maskable interrupt source. Writing to the NMISR register is ignored. The setting in the non-maskable interrupt enable register (NMIER) does not affect the status flags in NMISR.
Before the end of the non-maskable interrupt handler, read the NMISR register and confirm the generation status of other non-maskable interrupts. Be sure to confirm that all of the bits in the NMISR register are set to 0 before the end of the handler.

NMIST Flag (NMI Status Flag)

This flag indicates the NMI pin interrupt request.
The NMIST flag is read-only, and cleared by the NMICLR.NMICLR bit.
[Setting condition]

- When an edge specified by the NMICR.NMIMD bit is input to the NMI pin

[Clearing condition]

- When 1 is written to the NMICLR.NMICLR bit

OSTST Flag (Oscillation Stop Detection Interrupt Status Flag)

This flag indicates the oscillation stop detection interrupt request.
The OSTST flag is read-only, and cleared by the NMICLR.OSTCLR bit.
[Setting condition]

- When the oscillation stop detection interrupt is generated

[Clearing condition]

- When 1 is written to the NMICLR.OSTCLR bit

WDTST Flag (WDT Underflow/Refresh Error Status Flag)

This flag indicates the WDT underflow/refresh error interrupt request.
The WDTST flag is read-only, and cleared by the NMICLR.WDTCLR bit.
[Setting condition]

- When the WDT underflow/refresh error interrupt is generated

[Clearing condition]

- When 1 is written to the NMICLR.WDTCLR bit

IWDTST Flag (IWDT Underflow/Refresh Error Status Flag)

This flag indicates the IWDT underflow/refresh error interrupt request.
The IWDTST flag is read-only, and cleared by the NMICLR.IWDTCLR bit.
[Setting condition]

- When the IWDT underflow/refresh error interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.IWDTCLR bit

LVD1ST Flag (Voltage-Monitoring 1 Interrupt Status Flag)

This flag indicates the request for voltage-monitoring 1 interrupt.
The LVD1ST flag is read-only, and cleared by the NMICLR.LVD1CLR bit.
[Setting condition]

- When the voltage-monitoring 1 interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.LVD1CLR bit

LVD2ST Flag (Voltage-Monitoring 2 Interrupt Status Flag)

This flag indicates the request for voltage-monitoring 2 interrupt.
The LVD2ST flag is read-only, and cleared by the NMICLR.LVD2CLR bit.
[Setting condition]

- When the voltage-monitoring 2 interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.LVD2CLR bit

15.2.12 Non-Maskable Interrupt Enable Register (NMIER)

Address(es): 0008 7581h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD2EN	LVD1EN	IWDTEN	WDTEN	OSTEN	NMIEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMIEN	NMI Pin Interrupt Enable	0: NMI pin interrupt is disabled 1: NMI pin interrupt is enabled	R/(W) *1
b1	OSTEN	Oscillation Stop Detection Interrupt Enable	0: Oscillation stop detection interrupt is disabled 1: Oscillation stop detection interrupt is enabled	R/(W) *1
b2	WDTEN	WDT Underflow/Refresh Error Enable	0: WDT underflow/refresh error interrupt is disabled 1: WDT underflow/refresh error interrupt is enabled	R/(W) *1
b3	IWDTEN	IWDT Underflow/Refresh Error Enable	0: IWDT underflow/refresh error interrupt is disabled 1: IWDT underflow/refresh error interrupt is enabled	R/(W) *1
b4	LVD1EN	Voltage-Monitoring 1 Interrupt Enable	0: Voltage-monitoring 1 interrupt is disabled 1: Voltage-monitoring 1 interrupt is enabled	R/(W) *1
b5	LVD2EN	Voltage-Monitoring 2 Interrupt Enable	0: Voltage-monitoring 2 interrupt is disabled 1: Voltage-monitoring 2 interrupt is enabled	R/(W) *1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

NMIEN Bit (NMI Pin Interrupt Enable)

This bit enables the NMI pin interrupt.
A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.
Writing 0 to this bit is disabled.

OSTEN Bit (Oscillation Stop Detection Interrupt Enable)

This bit enables the oscillation stop detection interrupt.
A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.
Writing 0 to this bit is disabled.

WDTEN Bit (WDT Underflow/Refresh Error Enable)

This bit enables the WDT underflow/refresh error interrupt.
A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.
Writing 0 to this bit is disabled.

IWDTEN Bit (IWDT Underflow/Refresh Error Enable)

This bit enables the IWDT underflow/refresh error interrupt.
A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.
Writing 0 to this bit is disabled.

LVD1EN Bit (Voltage-Monitoring 1 Interrupt Enable)

This bit enables the voltage-monitoring 1 interrupt.
A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.
Writing 0 to this bit is disabled.

LVD2EN Bit (Voltage-Monitoring 2 Interrupt Enable)

This bit enables the voltage-monitoring 2 interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

15.2.13 Non-Maskable Interrupt Status Clear Register (NMICLR)

Address(es): 0008 7582h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD2CLR	LVD1CLR	IWDTCLR	WDTCLR	OSTCLR	NMICLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMICLR	NMI Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.NMIST flag. Writing 0 to this bit has no effect.	R/(W) *1
b1	OSTCLR	OST Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.OSTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b2	WDTCLR	WDT Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.WDTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b3	IWDTCLR	IWDT Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.IWDTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b4	LVD1CLR	LVD1 Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.LVD1ST flag. Writing 0 to this bit has no effect.	R/(W) *1
b5	LVD2CLR	LVD2 Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.LVD2ST flag. Writing 0 to this bit has no effect.	R/(W) *1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written to this bit.

NMICLR Bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag.

This bit is read as 0.

OSTCLR Bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag.

This bit is read as 0.

WDTCLR Bit (WDT Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag.

This bit is read as 0.

IWDTCLR Bit (IWDT Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag.

This bit is read as 0.

LVD1CLR Bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag.

This bit is read as 0.

LVD2CLR Bit (LVD2 Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag.
This bit is read as 0.

15.2.14 NMI Pin Interrupt Control Register (NMICR)

Address(es): 0008 7583h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	NMIMD	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Change the setting of the NMICR register before the NMI pin interrupt is enabled (before setting the NMIER.NMIEN bit to 1).

15.2.15 NMI Pin Digital Filter Enable Register (NMIFLTE)

Address(es): 0008 7590h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	NFLTEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFLTEN	NMI Digital Filter Enable	0: Digital filter is disabled. 1: Digital filter is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFLTEN Bit (NMI Digital Filter Enable)

This bit enables the digital filter used for the NMI pin interrupt.
The digital filter is enabled when the NFLTEN bit is 1, and disabled when the NFLTEN bit is 0.
The NMI pin level is sampled at the sampling clock cycle specified with the NMIFLTC.NFCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.
For details of the digital filter, see section 15.5.7, Digital Filter.

15.2.16 NMI Pin Digital Filter Setting Register (NMIFLTC)

Address(es): 0008 7594h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	NFCLKSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock	b1 b0 0 0: PCLK 0 1: PCLK/8 1 0: PCLK/32 1 1: PCLK/64	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFCLKSEL[1:0] Bits (NMI Digital Filter Sampling Clock)

These bits select the cycle of the digital filter sampling clock for the NMI pin interrupt.

The sampling clock cycle can be selected from among the PCLK (every cycle), PCLK/8 (once every eight cycles), PCLK/32 (once every 32 cycles), and PCLK/64 (once every 64 cycles).

For details of the digital filter, see section 15.5.7, Digital Filter.

15.2.17 Group m Interrupt Source Register (GRPm) (m: group number)

- GRP00

Address(es): GRP00 0008 C300h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IS1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0 and cannot be modified.	R
b1	IS1	Interrupt Status Flag 1	0: Interrupt is not requested. 1: Interrupt is requested.	R
b31 to b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

- GRP12

Address(es): GRP12 0008 C330h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	IS6	IS5	IS4	IS3	IS2	IS1	IS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IS0	Interrupt Status Flag 0	0: Interrupt is not requested. 1: Interrupt is requested.	R
b1	IS1	Interrupt Status Flag 1		R
b2	IS2	Interrupt Status Flag 2		R
b3	IS3	Interrupt Status Flag 3		R
b4	IS4	Interrupt Status Flag 4		R
b5	IS5	Interrupt Status Flag 5		R
b6	IS6	Interrupt Status Flag 6		R
b31 to b7	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

GRPm is provided for each group, where m indicates the group number (m: 00 or 12).
For details of the grouping function, see section 15.4.1, Interrupt Request Groups. For correspondence between the interrupt request allocated to each group and the bit number in the GRPm register, see Table 15.3, Interrupt Vector Table. For correspondence between grouped interrupt sources and interrupt vector numbers, see Table 15.3, Interrupt Vector Table.

ISj Flag (Interrupt Status Flag j) (j = bit number)

This bit is the status flag of the peripheral module interrupt request allocated to the jth bit in group m. This flag is set to 1 when the interrupt request is generated and is enabled by the interrupt request enable bit j in group m interrupt enable register (GENm.ENj; m = group number and j = bit number).
When both the GENm.ENj bit and ISj flag bit for any of the interrupt sources in a group are 1, the interrupt status flag in interrupt request register n (IRn.IR; n = interrupt vector number) corresponding to the group is set to 1.
Group 0 comprises edge detection interrupt requests and group 12 comprises level detection interrupt requests.

(1) Group 0

[Setting condition]

- The ISj flag is set to 1 when the corresponding peripheral module interrupt request is generated and GENm.ENj is 1.

[Clearing condition]

- The ISj flag is cleared to 0 by writing 1 to the interrupt source clear bit in group m interrupt clear register (GCRm.CLRj).

(2) Group 12

[Setting condition]

- The ISj flag remains 1 while the corresponding peripheral module interrupt request is being sent and GENm.ENj is 1.

[Clearing conditions]

- The ISj flag is cleared to 0 when the source of the interrupt request is cleared.
- The ISj flag is cleared to 0 when GENm.ENj is 0.

Writing to the ISj flag is disabled.

15.2.18 Group m Interrupt Enable Register (GENm) (m = group number)

- GEN00

Address(es): GEN00 0008 C340h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	EN1	Interrupt request enable 1	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- GEN12

Address(es): GEN12 0008 C370h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	EN6	EN5	EN4	EN3	EN2	EN1	EN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EN0	Interrupt request enable 0	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b1	EN1	Interrupt request enable 1		R/W
b2	EN2	Interrupt request enable 2		R/W
b3	EN3	Interrupt request enable 3		R/W
b4	EN4	Interrupt request enable 4		R/W
b5	EN5	Interrupt request enable 5		R/W
b6	EN6	Interrupt request enable 6		R/W
b31 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

For details of the grouping function, see section 15.4.1, Interrupt Request Groups.
GENm is provided for each group, where m indicates the group number (m: 00 or 12).

ENj Bits (Interrupt Request Enable j) (j = bit number)

- Group 00

When an ENj bit is 1, interrupt request detection by the corresponding GRPm.ISj flag (m = group number and j = bit number) is enabled. When an interrupt is detected, the GRPm.ISj flag is set to 1.
When an ENj bit is 0, interrupt request detection is disabled.
Writing 0 to the ENj bit does not affect the corresponding GRPm.ISj flag.

- Group 12

When an ENj bit is 1, interrupt request detection by the corresponding GRPm.ISj flag (m = group number and j = bit number) is enabled. When an interrupt is detected, the GRPm.ISj flag is set to 1.
When an ENj bit is 0, interrupt request detection is disabled.
Writing 0 to the ENj bit does not affect the corresponding GRPm.ISj flag.

15.2.19 Group m Interrupt Clear Register (GCRm) (m = group number)

- GCR00

Address(es): GCR00 0008 C380h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLR1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b1	CLR1	Interrupt source clear 1	These bits are read as 0. Writing 1 to this bit clears the interrupt status flag bit (GRPm.ISj) of the same group and bit. Writing 0 is invalid.	R(/W) *1
b31 to b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

Note 1. Only 1 can be written.

For details of the grouping function, see section 15.4.1, Interrupt Request Groups.
GCRm is provided for each group, where m indicates the group number (m: 00).

CLRj Bits (Interrupt Source Clear j) (j = bit number)

Writing 1 to this bit clears the corresponding GRPm.ISj flag (m = group number and j = bit number) to 0.

15.3 Vector Table

There are two types of interrupts detected by the interrupt controller: maskable interrupts and non-maskable interrupts. When the CPU accepts an interrupt or non-maskable interrupt, it acquires a four-byte vector address from the vector table.

15.3.1 Interrupt Vector Table

The interrupt vector table is placed in the 1024-byte range (4 bytes x 256 sources) beginning at the address specified in the interrupt table register (INTB) of the CPU. Write a value to the INTB register before enabling interrupts. The value written to the INTB register should be a multiple of 4.
Furthermore, the execution of an INT or BRK instruction leads to an unconditional trap.
The vectors for unconditional traps are in the same area as the vector table for interrupts given as Table 14.3. BRK instructions have vector number 0 while INT instructions have the vector numbers given as the operands (0 to 255).
Table 15.3 lists details of the interrupt vectors. Details of the headings in Table 15.3 are listed below.

Item	Description
Source of interrupt request generation	Name of the source for generation of the interrupt request
Name	Name of the interrupt
Vector no.	Vector number for the interrupt
Vector address offset	Value of the offset from the base address for the vector table.
Form of interrupt detection	“Edge” or “level” as the method for detection of the interrupt
CPU interrupt	“○” in this column indicates usability as a CPU interrupt.
DTC activation	“○” in this column indicates usability as a request for DTC activation.
DMAC activation	“○” in this column indicates usability as a request for DMAC activation.
sstb return	“○” in this column indicates usability as a request for return from software-standby mode.
sacs return	“○” in this column indicates usability as a request for return from all-module clock-stop mode.
IER	Name of the interrupt request enable register (IER) and bit corresponding to the vector number
IPR	Name of the interrupt source priority register (IPR) corresponding to the interrupt source
DTCER	Name of the DTC activation enable register (DTCER) corresponding to the DTC activation source

Table 15.3 Interrupt Vector Table (1/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
—	Dedicated for unconditional traps	0	0000h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	1	0004h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	2	0008h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	3	000Ch	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	4	0010h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	5	0014h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	6	0018h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	7	001Ch	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	8	0020h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	9	0024h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	10	0028h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	11	002Ch	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	12	0030h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	13	0034h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	14	0038h	—	×	×	×	×	×	—	—	—	
—	Dedicated for unconditional traps	15	003Ch	—	×	×	×	×	×	—	—	—	
BSC	BUSERR	16	0040h	Level	○	×	×	×	×	IER02.IEN0	IPR000	—	
—	Reserved	17	0044h	—	×	×	×	×	×	—	—	—	
—	Reserved	18	0048h	—	×	×	×	×	×	—	—	—	
—	Reserved	19	004Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	20	0050h	—	×	×	×	×	×	—	—	—	
FCU	FIFERR	21	0054h	Level	○	×	×	×	×	IER02.IEN5	IPR001	—	
—	Reserved	22	0058h	—	×	×	×	×	×	—	—	—	
FCU	FRDYI	23	005Ch	Edge	○	×	×	×	×	IER02.IEN7	IPR002	—	
—	Reserved	24	0060h	—	×	×	×	×	×	—	—	—	
—	Reserved	25	0064h	—	×	×	×	×	×	—	—	—	
—	Reserved	26	0068h	—	×	×	×	×	×	—	—	—	
ICU	SWINT	27	006Ch	Edge	○	○	×	×	×	IER03.IEN3	IPR003	DTCER027	
CMT0	CMI0	28	0070h	Edge	○	○	○	×	×	IER03.IEN4	IPR004	DTCER028	
CMT1	CMI1	29	0074h	Edge	○	○	○	×	×	IER03.IEN5	IPR005	DTCER029	
CMT2	CMI2	30	0078h	Edge	○	○	○	×	×	IER03.IEN6	IPR006	DTCER030	
CMT3	CMI3	31	007Ch	Edge	○	○	○	×	×	IER03.IEN7	IPR007	DTCER031	
—	Reserved	32	0080h	—	×	×	×	×	×	—	—	—	

Table 15.3 Interrupt Vector Table (2/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
USB0	D0FIFO0	33	0084h	Edge	○	○	○	×	×	IER04.IEN1	IPR033	DTCER033	Not present in versions with 112, 100, 64, or 48 pins.
	D1FIFO0	34	0088h	Edge	○	○	○	×	×	IER04.IEN2	IPR034	DTCER034	Not present in versions with 112, 100, 64, or 48 pins.
	USBI0	35	008Ch	Edge	○	×	×	×	×	IER04.IEN3	IPR035	—	Not present in versions with 112, 100, 64, or 48 pins.
CAC	FERRF	36	0090h	Level	○	×	×	×	×	IER04.IEN4	IPR036	—	
	MENDF	37	0094h	Level	○	×	×	×	×	IER04.IEN5		—	
	OVFF	38	0098h	Level	○	×	×	×	×	IER04.IEN6		—	
RSPI0	SPRI0	39	009Ch	Edge	○	○	○	×	×	IER04.IEN7	IPR039	DTCER039	
	SPTI0	40	00A0h	Edge	○	○	○	×	×	IER05.IEN0	IPR040	DTCER040	
	SPII0	41	00A4h	Level	○	×	×	×	×	IER05.IEN1	IPR041	—	
RSPI1	SPRI1	42	00A8h	Edge	○	○	○	×	×	IER05.IEN2	IPR042	DTCER042	Not present in versions with 64 or 48 pins.
	SPTI1	43	00ACh	Edge	○	○	○	×	×	IER05.IEN3	IPR043	DTCER043	Not present in versions with 64 or 48 pins.
	SPII1	44	00B0h	Level	○	×	×	×	×	IER05.IEN4	IPR044	—	Not present in versions with 64 or 48 pins.
CAN1	RXF1	45	00B4h	Edge	○	×	×	×	×	IER05.IEN5	IPR045	—	Not present in versions with 64 or 48 pins.
	TXF1	46	00B8h	Edge	○	×	×	×	×	IER05.IEN6		—	Not present in versions with 64 or 48 pins.
	RXM1	47	00BCh	Edge	○	×	×	×	×	IER05.IEN7		—	Not present in versions with 64 or 48 pins.
	TXM1	48	00C0h	Edge	○	×	×	×	×	IER06.IEN0		—	Not present in versions with 64 or 48 pins.
GPT7	GTCIA7	49	00C4h	Edge	○	○	○	×	×	IER06.IEN1	IPR049	DTCER049	Not present in versions with 64 or 48 pins.
	GTCIB7	50	00C8h	Edge	○	○	○	×	×	IER06.IEN2		DTCER050	Not present in versions with 64 or 48 pins.
	GTCIC7	51	00CCh	Edge	○	○	○	×	×	IER06.IEN3		DTCER051	Not present in versions with 64 or 48 pins.
	GTCIE7	52	00D0h	Edge	○	○	○	×	×	IER06.IEN4	IPR052	DTCER052	Not present in versions with 64 or 48 pins.
	GTCIV7	53	00D4h	Edge	○	○	○	×	×	IER06.IEN5		DTCER053	Not present in versions with 64 or 48 pins.
Comparator	CMP4	54	00D8h	Edge	○	○	○	×	×	IER06.IEN6	IPR054	DTCER054	Not present in versions with 64 or 48 pins.
	CMP5	55	00DCh	Edge	○	○	○	×	×	IER06.IEN7	IPR055	DTCER055	Not present in versions with 64 or 48 pins.
	CMP6	56	00E0h	Edge	○	○	○	×	×	IER07.IEN0	IPR056	DTCER056	Not present in versions with 64 or 48 pins.
DOC	DOPCF	57	00E4h	Level	○	×	×	×	×	IER07.IEN1	IPR057	—	

Table 15.3 Interrupt Vector Table (3/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
DPC	RBI0	58	00FCh	Edge	○	○	○	×	×	IER07.IEN2	IPR058	DTCER058	Not present in versions with 64 or 48 pins.
	RBI1	59	00FCh	Edge	○	○	○	×	×	IER07.IEN3	IPR059	DTCER059	Not present in versions with 64 or 48 pins.
	RBI2	60	00FCh	Edge	○	○	○	×	×	IER07.IEN4	IPR060	DTCER060	Not present in versions with 64 or 48 pins.
	RBI3	61	00FCh	Edge	○	○	○	×	×	IER07.IEN5	IPR061	DTCER061	Not present in versions with 64 or 48 pins.
	RBI4	62	00FCh	Edge	○	○	○	×	×	IER07.IEN6	IPR062	DTCER062	Not present in versions with 64 or 48 pins.
—	Reserved	63	00FCh	—	×	×	×	×	×	—	—	—	
ICU	IRQ0	64	0100h	Edge/Level	○	○	○	○	○	IER08.IEN0	IPR064	DTCER064	
	IRQ1	65	0104h	Edge/Level	○	○	○	○	○	IER08.IEN1	IPR065	DTCER065	
	IRQ2	66	0108h	Edge/Level	○	○	○	○	○	IER08.IEN2	IPR066	DTCER066	
	IRQ3	67	010Ch	Edge/Level	○	○	○	○	○	IER08.IEN3	IPR067	DTCER067	
	IRQ4	68	0110h	Edge/Level	○	○	○	○	○	IER08.IEN4	IPR068	DTCER068	
	IRQ5	69	0114h	Edge/Level	○	○	○	○	○	IER08.IEN5	IPR069	DTCER069	
	IRQ6	70	0118h	Edge/Level	○	○	○	○	○	IER08.IEN6	IPR070	DTCER070	Not present in versions with 64 or 48 pins.
	IRQ7	71	011Ch	Edge/Level	○	○	○	○	○	IER08.IEN7	IPR071	DTCER071	Not present in versions with 64 or 48 pins.
—	Reserved	72	0120h	—	×	×	×	×	×	—	—	—	
—	Reserved	73	0124h	—	×	×	×	×	×	—	—	—	
—	Reserved	74	0128h	—	×	×	×	×	×	—	—	—	
—	Reserved	75	012Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	76	0130h	—	×	×	×	×	×	—	—	—	
—	Reserved	77	0134h	—	×	×	×	×	×	—	—	—	
—	Reserved	78	0138h	—	×	×	×	×	×	—	—	—	
—	Reserved	79	013Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	80	0140h	—	×	×	×	×	×	—	—	—	
—	Reserved	81	0144h	—	×	×	×	×	×	—	—	—	
—	Reserved	82	0148h	—	×	×	×	×	×	—	—	—	
—	Reserved	83	014Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	84	0150h	—	×	×	×	×	×	—	—	—	
—	Reserved	85	0154h	—	×	×	×	×	×	—	—	—	
—	Reserved	86	0158h	—	×	×	×	×	×	—	—	—	
—	Reserved	87	015Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	88	0160h	—	×	×	×	×	×	—	—	—	
—	Reserved	89	0164h	—	×	×	×	×	×	—	—	—	
USB	USBR0	90	0168h	Level	○	×	×	○	○	IER0B.IEN2	IPR090	—	Not present in versions with 112, 100, 64, or 48 pins.
—	Reserved	91	016Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	92	0170h	—	×	×	×	×	×	—	—	—	
—	Reserved	93	0174h	—	×	×	×	×	×	—	—	—	
—	Reserved	94	0178h	—	×	×	×	×	×	—	—	—	
—	Reserved	95	017Ch	—	×	×	×	×	×	—	—	—	

Table 15.3 Interrupt Vector Table (4/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
—	Reserved	96	0180h	—	×	×	×	×	×	—	—	—	
—	Reserved	97	0184h	—	×	×	×	×	×	—	—	—	
AD	ADI0	98	0188h	Edge	○	○	○	×	×	IER0C.IEN2	IPR098	DTCER098	Not present in versions with 64 or 48 pins.
—	Reserved	99	018Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	100	0190h	—	×	×	×	×	×	—	—	—	
—	Reserved	101	0194h	—	×	×	×	×	×	—	—	—	
S12AD	S12ADI	102	0198h	Edge	○	○	○	×	×	IER0C.IEN6	IPR102	DTCER102	
	S12GBADI	103	019Ch	Edge	○	○	○	×	×	IER0C.IEN7	IPR103	DTCER103	
S12AD1	S12ADI1	104	01A0h	Edge	○	○	○	×	×	IER0D.IEN0	IPR104	DTCER104	Not present in versions with 64 or 48 pins.
	S12GBADI1	105	01A4h	Edge	○	○	○	×	×	IER0D.IEN1	IPR105	DTCER105	Not present in versions with 64 or 48 pins.
ICU*2	GROUP0	106	01A8h	Level	○	×	×	×	×	IER0D.IEN2	IPR106	—	Not present in versions with 64 or 48 pins.
—	Reserved	107	01ACh	—	×	×	×	×	×	—	—	—	
—	Reserved	108	01B0h	—	×	×	×	×	×	—	—	—	
—	Reserved	109	01B4h	—	×	×	×	×	×	—	—	—	
—	Reserved	110	01B8h	—	×	×	×	×	×	—	—	—	
—	Reserved	111	01BCh	—	×	×	×	×	×	—	—	—	
—	Reserved	112	01C0h	—	×	×	×	×	×	—	—	—	
—	Reserved	113	01C4h	—	×	×	×	×	×	—	—	—	
ICU	GROUP12	114	01C8h	Level	○	×	×	×	×	IER0E.IEN2	IPR114	—	
—	Reserved	115	01CCh	—	×	×	×	×	×	—	—	—	
—	Reserved	116	01D0h	—	×	×	×	×	×	—	—	—	
—	Reserved	117	01D4h	—	×	×	×	×	×	—	—	—	
—	Reserved	118	01D8h	—	×	×	×	×	×	—	—	—	
—	Reserved	119	01DCh	—	×	×	×	×	×	—	—	—	
—	Reserved	120	01E0h	—	×	×	×	×	×	—	—	—	
—	Reserved	121	01E4h	—	×	×	×	×	×	—	—	—	
SCI12	SCIX0	122	01E8h	Level	○	×	×	×	×	IER0F.IEN2	IPR122	—	
	SCIX1	123	01ECh	Level	○	×	×	×	×	IER0F.IEN3		—	
	SCIX2	124	01F0h	Level	○	×	×	×	×	IER0F.IEN4		—	
	SCIX3	125	01F4h	Level	○	×	×	×	×	IER0F.IEN5		—	
MTU0	TGIA0	126	01F8h	Edge	○	○	○	×	×	IER0F.IEN6	IPR126	DTCER126	
	TGIB0	127	01FCh	Edge	○	○	○	×	×	IER0F.IEN7		DTCER127	
	TGIC0	128	0200h	Edge	○	○	○	×	×	IER10.IEN0		DTCER128	
	TGID0	129	0204h	Edge	○	○	○	×	×	IER10.IEN1		DTCER129	
	TCIV0	130	0208h	Edge	○	×	×	×	×	IER10.IEN2	IPR130	—	
	TGIE0	131	020Ch	Edge	○	×	×	×	×	IER10.IEN3		—	
	TGIF0	132	0210h	Edge	○	×	×	×	×	IER10.IEN4		—	
MTU1	TGIA1	133	0214h	Edge	○	○	○	×	×	IER10.IEN5	IPR133	DTCER133	
	TGIB1	134	0218h	Edge	○	○	○	×	×	IER10.IEN6		DTCER134	
	TCIV1	135	021Ch	Edge	○	×	×	×	×	IER10.IEN7	IPR135	—	
	TCIU1	136	0220h	Edge	○	×	×	×	×	IER11.IEN0		—	

Table 15.3 Interrupt Vector Table (5/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
MTU2	TGIA2	137	0224h	Edge	○	○	○	×	×	IER11.IEN1	IPR137	DTCER137	
	TGIB2	138	0228h	Edge	○	○	○	×	×	IER11.IEN2		DTCER138	
	TCIV2	139	022Ch	Edge	○	×	×	×	×	IER11.IEN3	IPR139	—	
	TCIU2	140	0230h	Edge	○	×	×	×	×	IER11.IEN4		—	
MTU3	TGIA3	141	0234h	Edge	○	○	○	×	×	IER11.IEN5	IPR141	DTCER141	
	TGIB3	142	0238h	Edge	○	○	○	×	×	IER11.IEN6		DTCER142	
	TGIC3	143	023Ch	Edge	○	○	○	×	×	IER11.IEN7		DTCER143	
	TGID3	144	0240h	Edge	○	○	○	×	×	IER12.IEN0		DTCER144	
	TCIV3	145	0244h	Edge	○	×	×	×	×	IER12.IEN1	IPR145	—	
MTU4	TGIA4	146	0248h	Edge	○	○	○	×	×	IER12.IEN2	IPR146	DTCER146	
	TGIB4	147	024Ch	Edge	○	○	○	×	×	IER12.IEN3		DTCER147	
	TGIC4	148	0250h	Edge	○	○	○	×	×	IER12.IEN4		DTCER148	
	TGID4	149	0254h	Edge	○	○	○	×	×	IER12.IEN5		DTCER149	
	TCIV4	150	0258h	Edge	○	○	○	×	×	IER12.IEN6	IPR150	DTCER150	
MTU5	TGIU5	151	025Ch	Edge	○	○	○	×	×	IER12.IEN7	IPR151	DTCER151	
	TGIV5	152	0260h	Edge	○	○	○	×	×	IER13.IEN0		DTCER152	
	TGIW5	153	0264h	Edge	○	○	○	×	×	IER13.IEN1		DTCER153	
MTU6	TGIA6	154	0268h	Edge	○	○	○	×	×	IER13.IEN2	IPR154	DTCER154	
	TGIB6	155	026Ch	Edge	○	○	○	×	×	IER13.IEN3		DTCER155	
	TGIC6	156	0270h	Edge	○	○	○	×	×	IER13.IEN4		DTCER156	
	TGID6	157	0274h	Edge	○	○	○	×	×	IER13.IEN5		DTCER157	
	TCIV6	158	0278h	Edge	○	×	×	×	×	IER13.IEN6	IPR158	—	
—	Reserved	159	027Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	160	0280h	—	×	×	×	×	×	—	—	—	
MTU7	TGIA7	161	0284h	Edge	○	○	○	×	×	IER14.IEN1	IPR161	DTCER161	
	TGIB7	162	0288h	Edge	○	○	○	×	×	IER14.IEN2		DTCER162	
	TGIC7	163	028Ch	Edge	○	○	○	×	×	IER14.IEN3	IPR163	DTCER163	
	TGID7	164	0290h	Edge	○	○	○	×	×	IER14.IEN4		DTCER164	
	TCIV7	165	0294h	Edge	○	○	○	×	×	IER14.IEN5	IPR165	DTCER165	
POE	OEI1	166	0298h	Level	○	×	×	×	×	IER14.IEN6	IPR166	—	
	OEI2	167	029Ch	Level	○	×	×	×	×	IER14.IEN7		—	Not present in versions with 64 or 48 pins.
	OEI3	168	02A0h	Level	○	×	×	×	×	IER15.IEN0		—	
	OEI4	169	02A4h	Level	○	×	×	×	×	IER15.IEN1		—	
	OEI5	170	02A8h	Level	○	×	×	×	×	IER15.IEN2		—	Not present in versions with 64 or 48 pins.
Comparator	CMP0	171	02ACh	Edge	○	○	○	×	×	IER15.IEN3	IPR171	DTCER171	
	CMP1	172	02B0h	Edge	○	○	○	×	×	IER15.IEN4	IPR172	DTCER172	
	CMP2	173	02B4h	Edge	○	○	○	×	×	IER15.IEN5	IPR173	DTCER173	

Table 15.3 Interrupt Vector Table (6/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
GPT4	GTCIA4	174	02B8h	Edge	○	○	○	×	×	IER15.IEN6	IPR174	DTCER174	Not present in versions with 64 or 48 pins.
	GTCIB4	175	02BCh	Edge	○	○	○	×	×	IER15.IEN7		DTCER175	Not present in versions with 64 or 48 pins.
	GTCIC4	176	02C0h	Edge	○	○	○	×	×	IER16.IEN0		DTCER176	Not present in versions with 64 or 48 pins.
	GTCIE4	177	02C4h	Edge	○	○	○	×	×	IER16.IEN1	IPR177	DTCER177	Not present in versions with 64 or 48 pins.
	GTCIV4	178	02C8h	Edge	○	○	○	×	×	IER16.IEN2		DTCER178	Not present in versions with 64 or 48 pins.
	LOCOI4	179	02CCh	Edge	○	○	○	×	×	IER16.IEN3		DTCER179	Not present in versions with 64 or 48 pins.
GPT5	GTCIA5	180	02D0h	Edge	○	○	○	×	×	IER16.IEN4	IPR180	DTCER180	Not present in versions with 64 or 48 pins.
	GTCIB5	181	02D4h	Edge	○	○	○	×	×	IER16.IEN5		DTCER181	Not present in versions with 64 or 48 pins.
	GTCIC5	182	02D8h	Edge	○	○	○	×	×	IER16.IEN6		DTCER182	Not present in versions with 64 or 48 pins.
	GTCIE5	183	02DCh	Edge	○	○	○	×	×	IER16.IEN7	IPR183	DTCER183	Not present in versions with 64 or 48 pins.
	GTCIV5	184	02E0h	Edge	○	○	○	×	×	IER17.IEN0		DTCER184	Not present in versions with 64 or 48 pins.
GPT6	GTCIA6	185	02E4h	Edge	○	○	○	×	×	IER17.IEN1	IPR185	DTCER185	Not present in versions with 64 or 48 pins.
	GTCIB6	186	02E8h	Edge	○	○	○	×	×	IER17.IEN2		DTCER186	Not present in versions with 64 or 48 pins.
	GTCIC6	187	02ECh	Edge	○	○	○	×	×	IER17.IEN3		DTCER187	Not present in versions with 64 or 48 pins.
	GTCIE6	188	02F0h	Edge	○	○	○	×	×	IER17.IEN4	IPR188	DTCER188	Not present in versions with 64 or 48 pins.
	GTCIV6	189	02F4h	Edge	○	○	○	×	×	IER17.IEN5		DTCER189	Not present in versions with 64 or 48 pins.
RIIC1	EEI1	190	02F8h	Level	○	×	×	×	×	IER17.IEN6	IPR190	—	Not present in versions with 112, 100, 64, or 48 pins.
	RXI1	191	02FCh	Edge	○	○	○	×	×	IER17.IEN7		DTCER191	Not present in versions with 112, 100, 64, or 48 pins.
	TXI1	192	0300h	Edge	○	○	○	×	×	IER18.IEN0		DTCER192	Not present in versions with 112, 100, 64, or 48 pins.
	TEI1	193	0304h	Level	○	×	×	×	×	IER18.IEN1		—	Not present in versions with 112, 100, 64, or 48 pins.
RIIC0	EEI0	194	0308h	Level	○	×	×	×	×	IER18.IEN2	IPR194	—	
	RXI0	195	030Ch	Edge	○	○	○	×	×	IER18.IEN3		DTCER195	
	TXI0	196	0310h	Edge	○	○	○	×	×	IER18.IEN4		DTCER196	
	TEI0	197	0314h	Level	○	×	×	×	×	IER18.IEN5		—	

Table 15.3 Interrupt Vector Table (7/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
DMAC	DMAC0I	198	0318h	Edge	○	○	×	×	×	IER18.IEN6	IPR198	DTCER198	
	DMAC1I	199	031Ch	Edge	○	○	×	×	×	IER18.IEN7	IPR199	DTCER199	
	DMAC2I	200	0320h	Edge	○	○	×	×	×	IER19.IEN0	IPR200	DTCER200	
	DMAC3I	201	0324h	Edge	○	○	×	×	×	IER19.IEN1	IPR201	DTCER201	
—	Reserved	202	0328h	—	×	×	×	×	×	—	—	—	
	Reserved	203	032Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	204	0330h	—	×	×	×	×	×	—	—	—	
—	Reserved	205	0334h	—	×	×	×	×	×	—	—	—	
—	Reserved	206	0338h	—	×	×	×	×	×	—	—	—	
—	Reserved	207	033Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	208	0340h	—	×	×	×	×	×	—	—	—	
—	Reserved	209	0344h	—	×	×	×	×	×	—	—	—	
—	Reserved	210	0348h	—	×	×	×	×	×	—	—	—	
—	Reserved	211	034Ch	—	×	×	×	×	×	—	—	—	
—	Reserved	212	0350h	—	×	×	×	×	×	—	—	—	
—	Reserved	213	0354h	—	×	×	×	×	×	—	—	—	
SCI0	RXI0	214	0358h	Edge	○	○	○	×	×	IER1A.IEN6	IPR214	DTCER214	
	TXI0	215	035Ch	Edge	○	○	○	×	×	IER1A.IEN7		DTCER215	
	TEI0	216	0360h	Level	○	×	×	×	×	IER1B.IEN0		—	
SCI1	RXI1	217	0364h	Edge	○	○	○	×	×	IER1B.IEN1	IPR217	DTCER217	
	TXI1	218	0368h	Edge	○	○	○	×	×	IER1B.IEN2		DTCER218	
	TEI1	219	036Ch	Level	○	×	×	×	×	IER1B.IEN3		—	
SCI2	RXI2	220	0370h	Edge	○	○	○	×	×	IER1B.IEN4	IPR220	DTCER220	Not present in versions with 64 or 48 pins.
	TXI2	221	0374h	Edge	○	○	○	×	×	IER1B.IEN5		DTCER221	Not present in versions with 64 or 48 pins.
	TEI2	222	0378h	Level	○	×	×	×	×	IER1B.IEN6		—	Not present in versions with 64 or 48 pins.
SCI3	RXI3	223	037Ch	Edge	○	○	○	×	×	IER1B.IEN7	IPR223	DTCER223	Not present in versions with 100, 64, or 48 pins.
	TXI3	224	0380h	Edge	○	○	○	×	×	IER1C.IEN0		DTCER224	Not present in versions with 100, 64, or 48 pins.
	TEI3	225	0384h	Level	○	×	×	×	×	IER1C.IEN1		—	Not present in versions with 100, 64, or 48 pins.
GPT0	GTCIA0	226	0388h	Edge	○	○	○	×	×	IER1C.IEN2	IPR226	DTCER226	
	GTCIB0	227	038Ch	Edge	○	○	○	×	×	IER1C.IEN3		DTCER227	
	GTCIC0	228	0390h	Edge	○	○	○	×	×	IER1C.IEN4		DTCER228	
	GTCIE0	229	0394h	Edge	○	○	○	×	×	IER1C.IEN5	IPR229	DTCER229	
	GTCIV0	230	0398h	Edge	○	○	○	×	×	IER1C.IEN6		DTCER230	
	LOCOI0	231	039Ch	Edge	○	○	○	×	×	IER1C.IEN7		DTCER231	
GPT1	GTCIA1	232	03A0h	Edge	○	○	○	×	×	IER1D.IEN0	IPR232	DTCER232	
	GTCIB1	233	03A4h	Edge	○	○	○	×	×	IER1D.IEN1		DTCER233	
	GTCIC1	234	03A8h	Edge	○	○	○	×	×	IER1D.IEN2		DTCER234	
	GTCIE1	235	03ACh	Edge	○	○	○	×	×	IER1D.IEN3	IPR235	DTCER235	
	GTCIV1	236	03B0h	Edge	○	○	○	×	×	IER1D.IEN4		DTCER236	

Table 15.3 Interrupt Vector Table (8/8)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	sacs Return	IER	IPR	DTCER	Remarks
—	Reserved	237	03B4h	—	×	×	×	×	×	—	—	—	
GPT2	GTCIA2	238	03B8h	Edge	○	○	○	×	×	IER1D.IEN6	IPR238	DTCER238	
	GTCIB2	239	03BCh	Edge	○	○	○	×	×	IER1D.IEN7		DTCER239	
	GTCIC2	240	03C0h	Edge	○	○	○	×	×	IER1E.IEN0		DTCER240	
	GTCIE2	241	03C4h	Edge	○	○	○	×	×	IER1E.IEN1	IPR241	DTCER241	
	GTCIV2	242	03C8h	Edge	○	○	○	×	×	IER1E.IEN2		DTCER242	
—	Reserved	243	03CCh	—	×	×	×	×	×	—	—	—	
GPT3	GTCIA3	244	03D0h	Edge	○	○	○	×	×	IER1E.IEN4	IPR244	DTCER244	
	GTCIB3	245	03D4h	Edge	○	○	○	×	×	IER1E.IEN5		DTCER245	
	GTCIC3	246	03D8h	Edge	○	○	○	×	×	IER1E.IEN6		DTCER246	
	GTCIE3	247	03DCh	Edge	○	○	○	×	×	IER1E.IEN7	IPR247	DTCER247	
	GTCIV3	248	03E0h	Edge	○	○	○	×	×	IER1F.IEN0		DTCER248	
—	Reserved	249	03E4h	—	×	×	×	×	×	—	—	—	
SCI12	RXI12	250	03E8h	Edge	○	○	○	×	×	IER1F.IEN2	IPR250	DTCER250	
	TXI12	251	03ECh	Edge	○	○	○	×	×	IER1F.IEN3		DTCER251	
	TEI12	252	03F0h	Level	○	×	×	×	×	IER1F.IEN4		—	
—	Reserved	253	03F4h	—	×	×	×	×	×	—	—	—	
—	Reserved	254	03F8h	—	×	×	×	×	×	—	—	—	
—	Reserved	255	03FCh	—	×	×	×	×	×	—	—	—	

Note: • This table lists the interrupt vectors for the maximum specification. The interrupt vectors for individual products correspond to the functions listed in Table 1.2. For details, see Table 1.2, Comparison of Functions for Different Packages.
Note 1. An interrupt source with a smaller vector number takes precedence.
Note 2. For the allocation of interrupt requests to the various interrupt groups, see Table 15.4, Group m Interrupt Requests (1/2).
Note 3. USB0 and RIIC1 are not included in 112-pin products.
Note 4. USB0, RIIC1, and SCI3 are not included in 100-pin products.
Note 5. GPT4 to GPT7, USB0, RSPI1, RIIC1, SCI2, SCI3, CAN1, AD, and S12AD1 are not included in 64- and 48-pin products.

15.3.2 Fast Interrupt Vector Table

The address of the entry in the interrupt vector table that corresponds to the vector number of the fast interrupt is placed in the fast interrupt vector register (FINTV) of the CPU.

15.3.3 Non-maskable Interrupt Vector Table

The non-maskable interrupt vector table is at FFFF FFF8h.

15.4 Peripheral Module Interrupt Request Grouping

15.4.1 Interrupt Request Groups

A maximum of 7 interrupt signals from peripheral modules are divided into groups and the interrupt signals in each group can be handled collectively as a single interrupt request.
Group 0 comprises edge detection interrupt requests and group 12 comprises level detection interrupt requests.
When an interrupt request is detected and GENm.ENj bit (m = group number and j = bit number) is 1, the GRPm.ISj flag is set to 1.
When a GENm.ENj flag in group m is 1, the IRn.IR flag (n = interrupt vector number) corresponding to the group is set to 1.

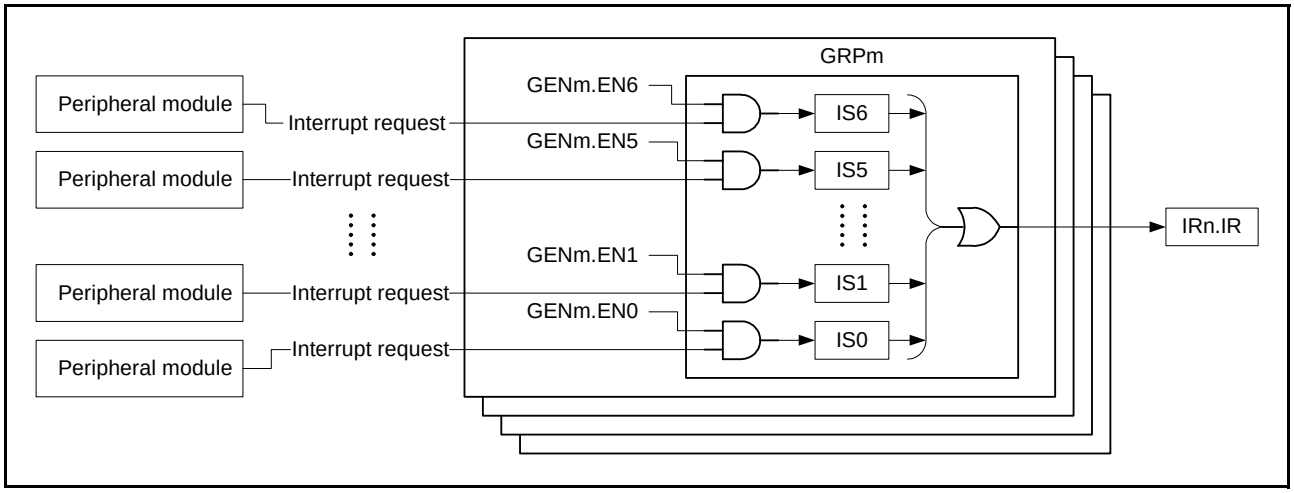


Figure 15.2 Interrupt Request Grouping

(1) Edge Detection Interrupt Requests

Group 0 comprises edge detection interrupt requests.
When an interrupt request is detected and GENm.ENj bit (m = group number and j = bit number) is 1, the GRPm.ISj flag bit is set to 1. The interrupt request is not detected when GENm.ENj bit is 0.
The GRPm.ISj flag is cleared to 0 by writing 1 to the GCRm.CLRj bit.
The GRPm.ISj flag remains 1 if the GENm.ENj bit is cleared to 0 when the GRPm.ISj flag is 1.
For operation examples, see section 15.5.1.3, Edge Detection Group Interrupts and Interrupt Status Flags.

(2) Level Detection Interrupt Requests

Group 12 comprises level detection interrupt requests.
When an interrupt request is detected and GENm.ENj bit (m = group number and j = bit number) is 1, the GRPm.ISj flag bit is set to 1. When the interrupt request is detected as 0, the GRPm.ISj flag is also cleared to 0.
When the GENm.ENj bit is 0, the interrupt request is not detected and the GRPm.ISj flag is cleared to 0.
For operation examples, see section 15.5.1.4, Level Detection Group Interrupts and Interrupt Status Flags.

(3) List of Interrupt Requests for Each Group

Table 15.4 lists the interrupt requests by group.

Table 15.4 Group m Interrupt Requests (1/2)

Group	Interrupt Request Source Interrupt Request	Name	GENm.ENj Bit	GRPm.ISj Flag	GCRm.CLRj Flag	Vector No. (IRn.IR)
Group 0	CAN1	ERS1 (error interrupt)	GEN00.EN1	GRP00.IS1	GCR00.CLR1	106

Table 15.4 Group m Interrupt Requests (2/2)

Group	Interrupt Request Source Interrupt Request	Name	GENm.ENj Bit	GRPm.ISj Flag	Vector No. (IRn.IR)
Group 12	SCI0	ERI0 (SCI0 reception error)	GEN12.EN0	GRP12.IS0	114
	SCI1	ERI1 (SCI1 reception error)	GEN12.EN1	GRP12.IS1	
	SCI2	ERI2 (SCI2 reception error)	GEN12.EN2	GRP12.IS2	
	SCI3	ERI3 (SCI3 reception error)	GEN12.EN3	GRP12.IS3	
	SCI12	ERI12 (SCI12 reception error)	GEN12.EN4	GRP12.IS4	
	RSPI0	SPEI0 (error interrupt)	GEN12.EN5	GRP12.IS5	
	RSPI1	SPEI1 (error interrupt)	GEN12.EN6	GRP12.IS6	

15.5 Interrupt Operation

The interrupt controller performs the following processing.

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations (CPU interrupt, DTC activation, or DMAC activation)
- Determining priority

15.5.1 Detecting Interrupts

Interrupt requests are detected in either of two ways: the detection of edges of the interrupt signal or the detection of a level of the interrupt signal.

Edge detection or level detection is selected for the IRQi pins (i = 0 to 7) as external interrupt requests by the setting of the IRQMD[1:0] bits in IRQCRi.

For interrupts from peripheral modules, either edge detection or level detection is determined per interrupt source.

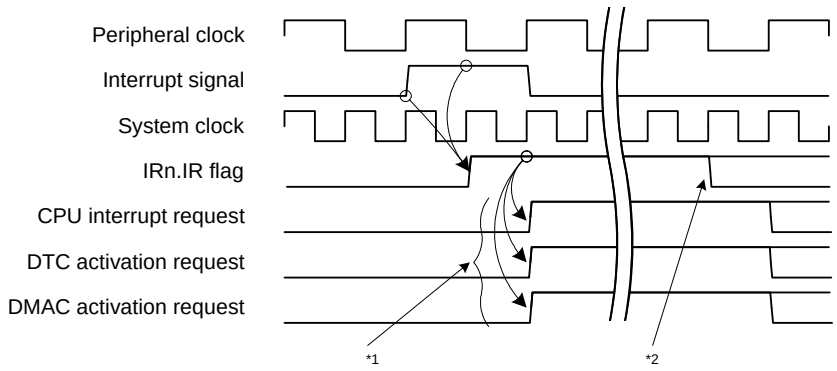
For the correspondence between interrupt sources and methods of detection, see Table 15.3, Interrupt Vector Table.

Grouped interrupt requests are classified into two groups; edge detection interrupt request group and level detection interrupt request group, and retained in the GRPm register (m = group number, 0 or 12). In both groups, the IRn.IR flag operates as the level interrupt. For details of the interrupt grouping function, see section 15.4, Peripheral Module Interrupt Request Grouping. For grouped interrupt requests, see Table 15.4, Group m Interrupt Requests.

15.5.1.1 Operation of Status Flags for Edge-Detected Interrupts

Figure 15.3 shows the operation of the IR flag in IRn in the case of edge detection of an interrupt from a peripheral module or on an external pin.

The IR flag in IRn is set to 1 immediately after the transition of the interrupt signal due to generation of the interrupt. If the CPU is the request destination for the interrupt, the IR flag is automatically cleared to 0 on acceptance of the interrupt. If the DMAC or DTC is the request destination for the interrupt, the IRn.IR flag operation differs according to the DMAC/DTC transfer settings and transfer count. For details, see Table 15.5, Operation at DMAC/DTC Activation.



Note 1. One of the following requests is issued: CPU interrupt request, DTC activation request, and DMAC activation request. For details of the setting, see section 15.5.3, Selecting Interrupt Request Destinations.
Note 2. When the CPU interrupt request is specified, this flag is set to 0 on acceptance of a CPU interrupt. For the timing of 0 setting at the DTC activation or DMAC activation, see Table 15.5 Operation at DMAC/DTC Activation.

Figure 15.3 IRn.IR Flag Operation for Edge Detection Interrupts

Figure 15.4 to Figure 15.7 show the interrupt signals of the interrupt controller. Note that the timings of the interrupts with interrupt vector numbers 64 to 95 are different from those of other interrupts. For the IRQ pin interrupts with interrupt vector numbers 64 to 71, “internal delay + 2 PCLK cycles” of delay is added after the IRQ pin input. For the interrupts with interrupt vector numbers 80 to 95, “2 PCLK cycles” of delay is added.

If an interrupt signal is generated every clock cycle, the subsequent interrupts cannot be detected; secure two or more clock cycles of the system clock or peripheral clock, whichever is slower, between issuance of continuous interrupt requests.

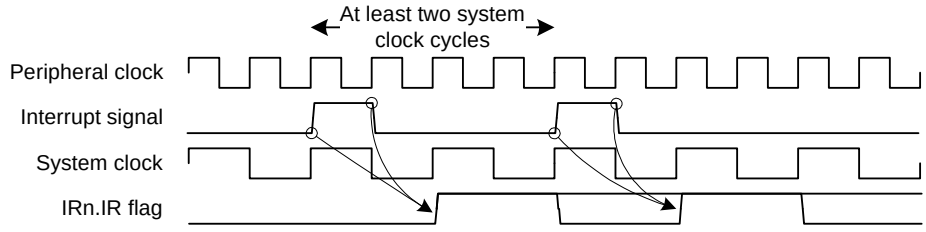


Figure 15.4 Interval Required between Issuance of Continuous Interrupt Requests (when the Frequency of System Clock is Slower than that of the Peripheral Clock)

While the IRn.IR flag is 1 after an interrupt request is generated, the interrupt request that is generated again will be ignored.*1
Figure 15.5 shows the timing for IRn.IR flag re-setting.

Note 1. When the transmission or reception interrupt of the SCI, RSPI, or RIIC is generated with the IRn.IR flag being 1, the interrupt request is retained. After the IRn.IR flag is cleared to 0, the IRn.IR flag is set to 1 again by the retained request. For details, see descriptions of the interrupts in section 29, Serial Communications Interface (SCIc, SCId), section 30, I2C Bus Interface (RIIC), and section 32, Serial Peripheral Interface (RSPI).

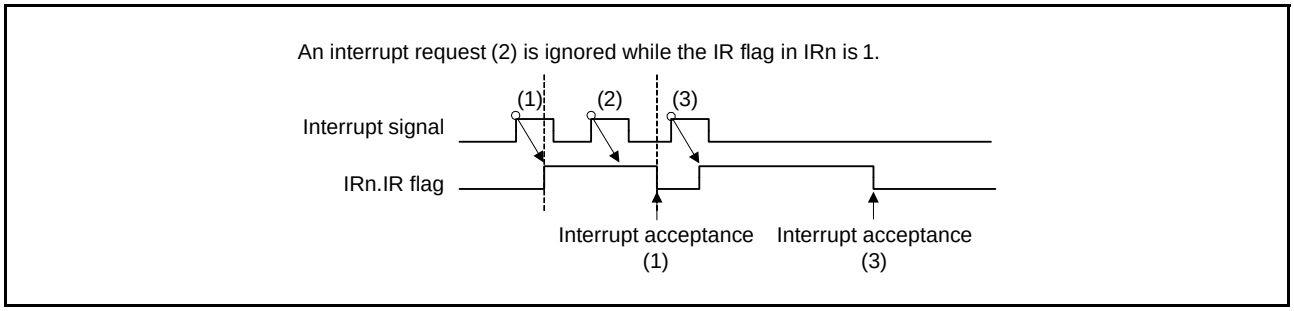


Figure 15.5 Timing for IRn.IR Flag Re-Setting

If an interrupt is disabled after the IRn.IR flag is set to 1 (output of the interrupt request is disabled by the interrupt enable bit of the relevant peripheral module), the IRn.IR flag is not affected but retains its state. Figure 15.6 shows operation when the interrupt is disabled.

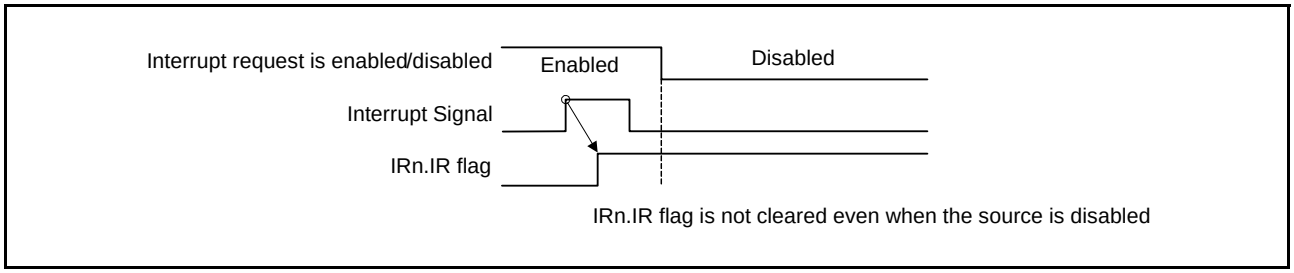


Figure 15.6 Relationship between IRn.IR Flag Operation and Disabling of Interrupt Request

15.5.1.2 Operation of Status Flags for Level-Detected Interrupts

Figure 15.7 shows the operation of the interrupt status flag (IR flag) in IRn in the case of level detection of an interrupt from a peripheral module or an external pin.

The IR flag in IRn remains set to 1 as long as the interrupt signal is asserted. To clear the IRn.IR flag to 0, clear the interrupt request in the source generating the interrupt. Confirm that the interrupt request flag in the source generating the interrupt has been cleared to 0 and that the IRn.IR flag has been cleared to 0, and then complete the interrupt handling.

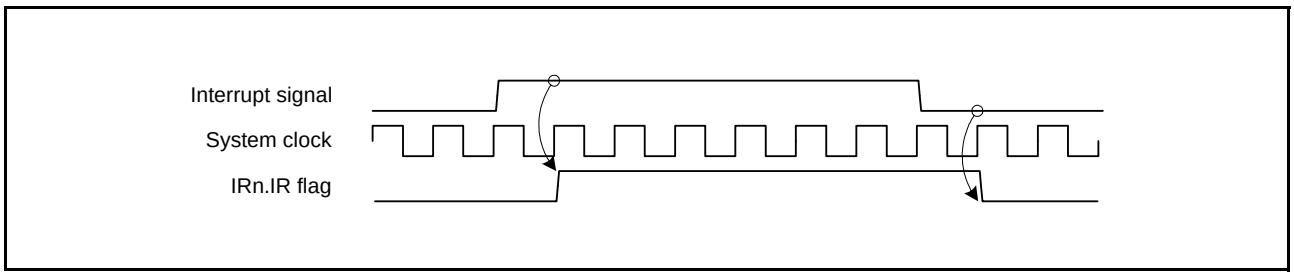


Figure 15.7 IRn.IR Flag Operation for Level Detection Interrupts

Figure 15.8 shows the procedure for handling level detection interrupts.

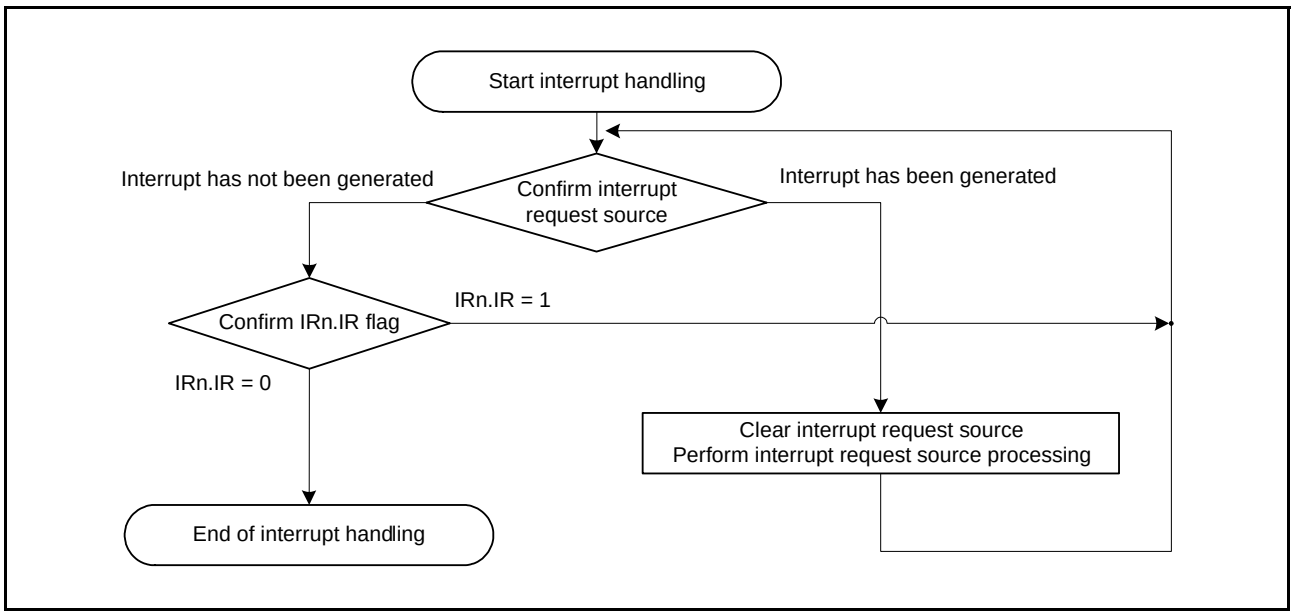


Figure 15.8 Procedure for Handling Level Detection Interrupts

15.5.1.3 Edge Detection Group Interrupts and Interrupt Status Flags

Edge detection interrupt requests are grouped into group 0. The IRn.IR flag corresponding to the groups operates assuming the interrupt requests as level detection interrupts.

Figure 15.9 shows an operation example in which an edge detection interrupt request is generated and Figure 15.10 shows an operation example in which multiple edge detection interrupt requests allocated to a group are generated.

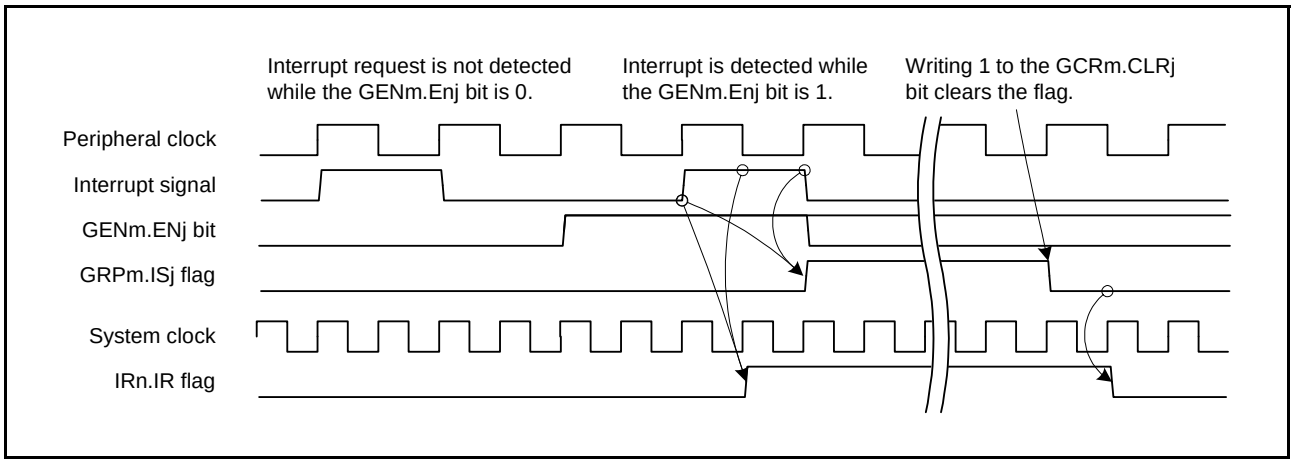


Figure 15.9 Operation Example in Which an Edge Detection Group Interrupt Request is Generated

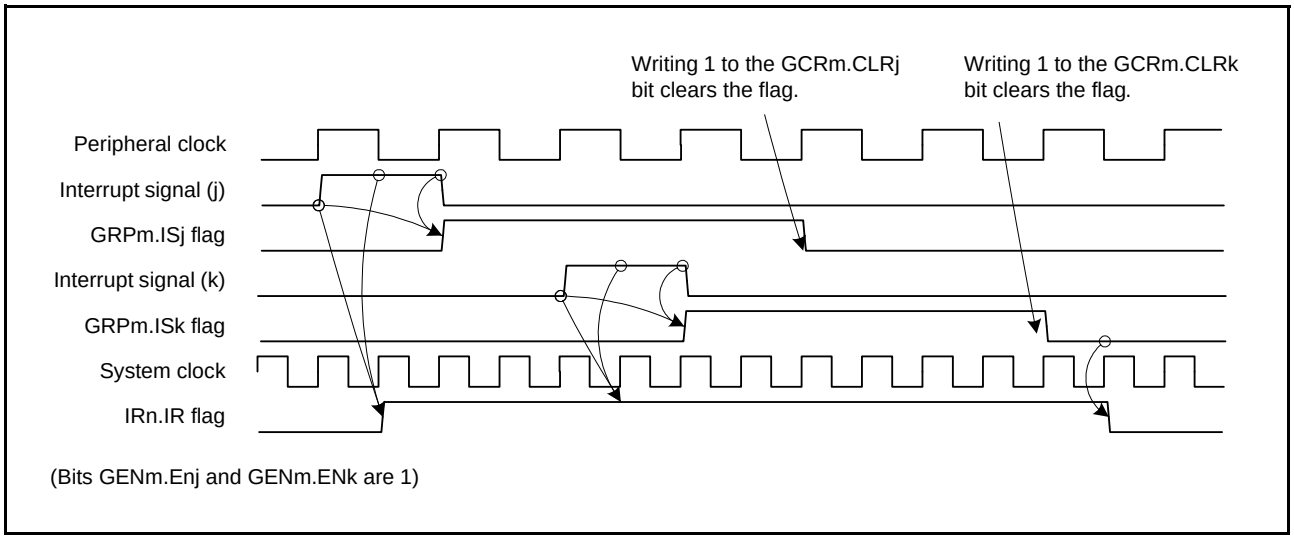


Figure 15.10 Operation Example in Which Multiple Edge Detection Interrupt Requests allocated to a Group are Generated

As for the interrupt handling of edge detection group 0, follow the procedure shown in Figure 15.11.

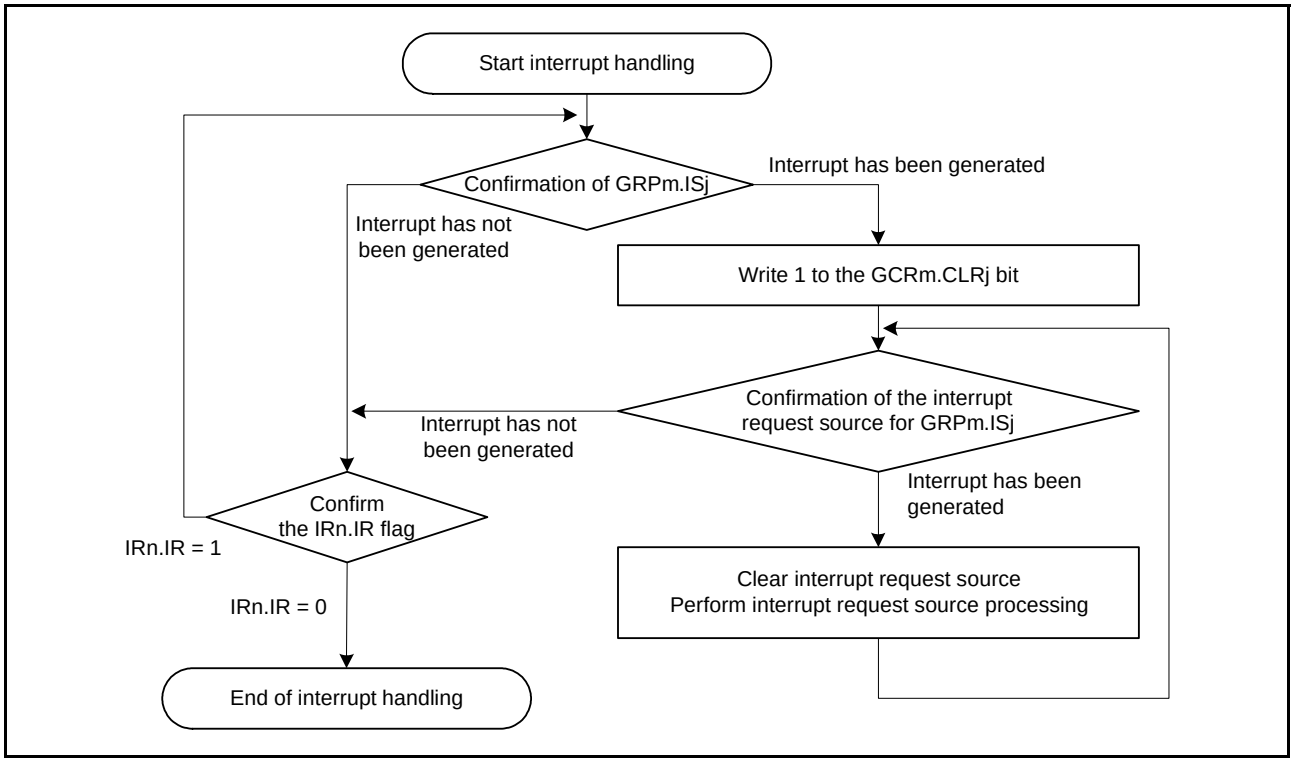


Figure 15.11 Procedure for Interrupt Handling of Edge Detection Group 0

15.5.1.4 Level Detection Group Interrupts and Interrupt Status Flags

Level detection interrupt requests are grouped into group 12. The IRn.IR flag corresponding to the group operates assuming the interrupt requests as level detection interrupts.

Figure 15.12 shows an operation example in which a level detection interrupt request is generated and Figure 15.13 shows an operation example in which multiple level detection interrupt requests of a group are generated.

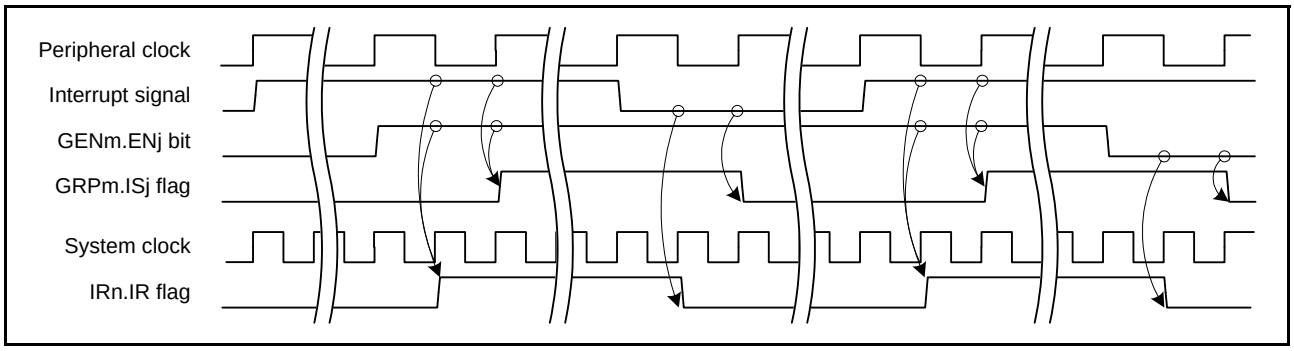


Figure 15.12 Operation Example in Which a Level Detection Group Interrupt Request is Generated

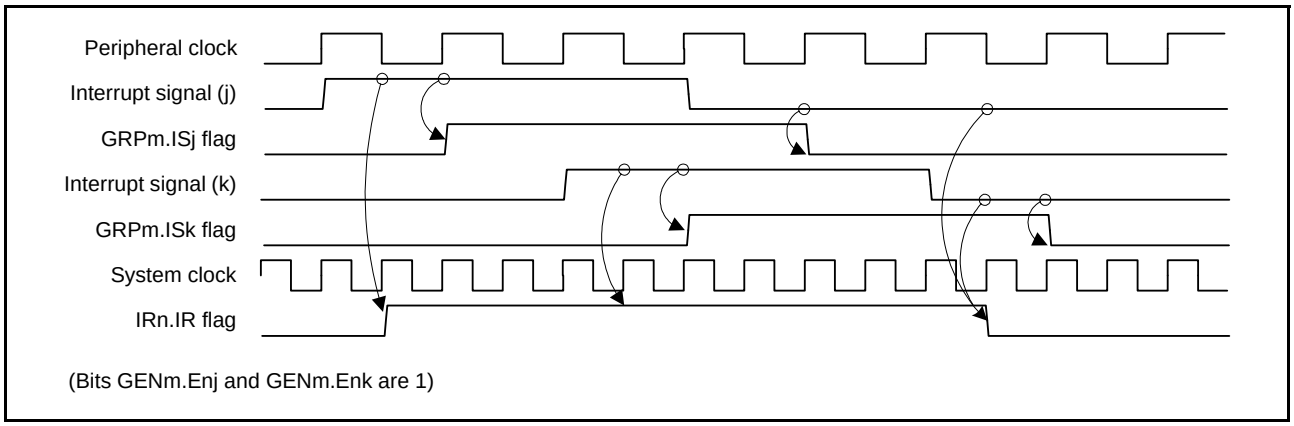


Figure 15.13 Operation Example in Which Multiple Level Detection Interrupt Requests of a Group are Generated

As for the interrupt handling of a level detection group, follow the procedure shown in Figure 15.14.

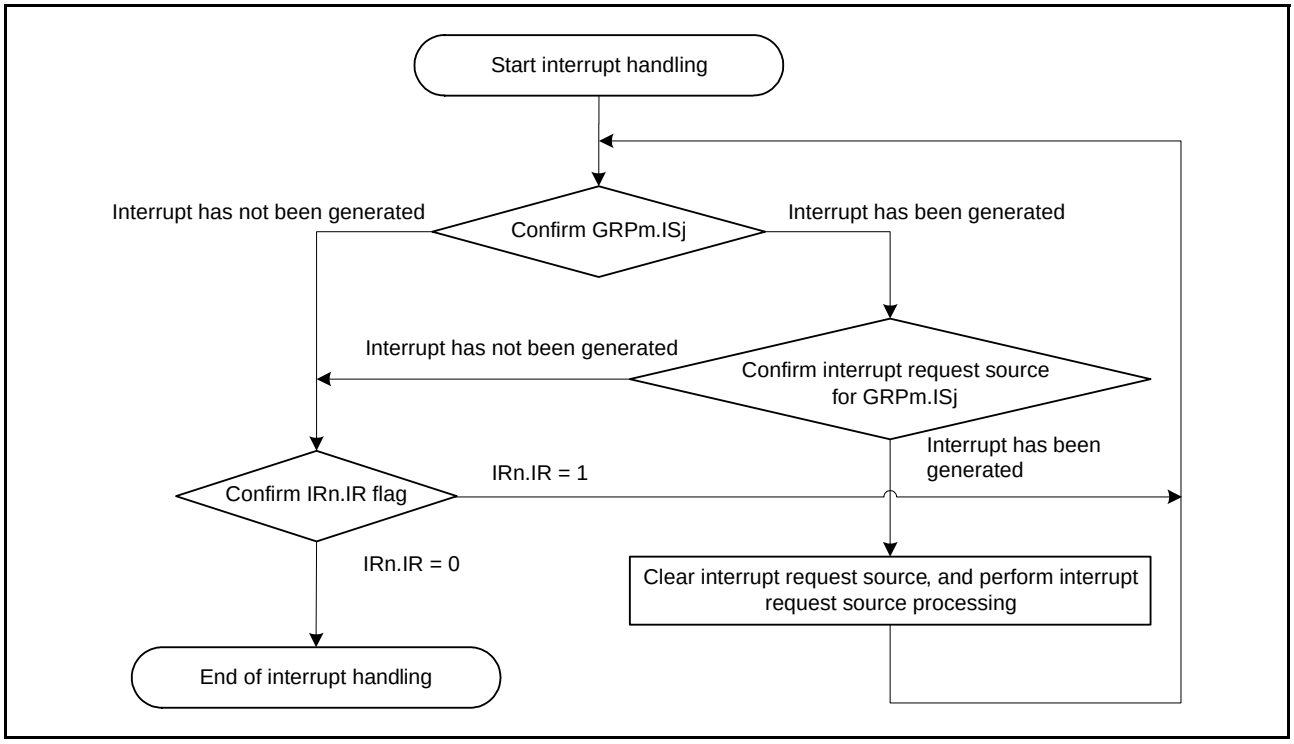


Figure 15.14 Procedure for Interrupt Handling of a Level Detection Group

15.5.2 Enabling and Disabling Interrupt Sources

Enabling requests from a given interrupt source requires the following settings.

1. In the case of interrupt requests from peripheral modules, setting the interrupt enable bit for the peripheral module to permit the output of interrupt requests from the source
2. For grouped interrupt requests, enabling the interrupts by the GENm.ENj bits
3. Enabling of the interrupt by the IERm.IENj bit

When an interrupt request that is enabled at the corresponding source is generated, the corresponding IRn.IR flag is set to 1. When a grouped interrupt request is generated, the corresponding GRPm.ISj flag is set to 1 and the IRn.IR flag corresponding to the group is set to 1.
Setting the IERm.IENj bit to enable an interrupt request allows the interrupt request for which the corresponding IRn.IR is 1 to be output to the interrupt request destination. Setting the IERm.IENj bit to disable an interrupt request suspends the output of the interrupt request for which the corresponding IRn.IR is 1.
The IRn.IR flag is not affected by the IERm.IENj bit.

Use the following procedure to disable interrupt requests.

1. Set the IERm.IENj bit to disable interrupt requests.
2. For grouped interrupt requests, set the GENm.ENj bit to disable.
3. Set the peripheral module interrupt output enable bit to disable the output. Read the last written register and confirm that writing is completed.
4. Check the IRn.IR flag, and clear the IRn.IR flag if necessary.*1
   For grouped interrupt requests, check the GRPm.ISj flag or clear the GRPm.ISj flag to 0.

Note 1. To disable the transmission or reception interrupt of the SCI, RSPI, or RIIC from the enabled state, clear the IRn.IR flag to 0 using the above procedure. For details, see descriptions of the interrupts in section 29, Serial Communications Interface (SCIc, SCId), section 30, I^2C Bus Interface (RIIC), and section 32, Serial Peripheral Interface (RSPI).

15.5.3 Selecting Interrupt Request Destinations

Possible settings for the request destination of each interrupt are fixed. That is, settings for request destination other than those indicated in Table 15.3, Interrupt Vector Table, are not possible. Do not make an interrupt request destination setting that is not indicated by a O in Table 15.3.
If the DMAC or DTC is selected as the destination for requests from an IRQ pin, be sure to set the IRQMD[1:0] bits in IRQCRi for that interrupt to select edge detection.
The following describes how to specify the destinations of interrupt requests.

(1) DMAC Activation

Make the following settings for each source while the IERm.IENj bit is 0.

1. Specify the vector number of the desired interrupt in the DMAC activation request select register (DMRSRm) for the required channel of the DMAC.*1
2. Set the activation source for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
3. Set the DMAC activation enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.

After making the above settings, set the IERm.IENj bit to 1.
In addition, set the DMAC operation enable bit (DMAST.DMST) to 1. The order of making settings for each interrupt and enabling the DMAC operation enable bit does not matter.
For the DMAC setting procedure, refer to section 18.3.7, Activating the DMAC in section 18, DMA Controller (DMACA).

(2) DTC Activation

Make the following settings for each source while the IERm.IENj bit is 0.

1. Set the DTC activation enable bit in the DTC activation enable register (DTCERn.DTCE) for the pertinent source to 1.*1

After making the above settings, set the IERm.IENj bit to 1.
In addition, set the DTC module activation bit (DTCST.DTCST) to 1. The order of making settings for each interrupt and enabling the DTC module activation bit does not matter.
For the DTC setting procedure, refer to section 19.5, DTC Setting Procedure, in section 19, Data Transfer Controller (DTCa).

Note 1. Do not set a DTC activation enable bit (DTCERn.DTCE) and a DMAC activation request select register (DMRSRm) to select the same source. Do not select the same source in more than one DMRSRm register.

(3) CPU Interrupt Request

If the interrupt request destination is neither the DMAC nor the DTC, the interrupt request is sent to the CPU. Set the IERm.IENj bit to 1 while neither the DMAC activation settings nor the DTC activation settings described above are in place.

Table 15.5 shows operation when the DTC or the DMAC is the request destination.

Table 15.5 Operation at DMAC/DTC Activation

Interrupt Request Destination	DISEL	Remaining Number of Transfer Operations	Operation per Request	IR*1	Interrupt Request Destination after Transfer
DMAC	1	≠ 0	DMA transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DMAC
		= 0	DMA transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The DMACm.DMCNT.DTE bit is cleared and the CPU becomes the destination.
	0	≠ 0	DMA transfer	Cleared at the start of DMAC transfer	DMAC
		= 0	DMA transfer*2	Cleared at the start of DMAC transfer*2	The DMACm.DMCNT.DTE bit is cleared and the CPU becomes the destination.
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The DTCER.DTCE bit is cleared and the CPU becomes the destination.
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer information	DTC
		= 0	DTC transfer → CPU interrupt *2	Cleared on interrupt acceptance by the CPU*2	The DTCER.DTCE bit is cleared and the CPU becomes the destination.

DISEL for the DMAC is set by the DMACm.DMCSL.DISEL bit; DISEL for the DTC is set by the DTC.MRB.DISEL bit.

Note 1. When the IRn.IR flag is 1, an interrupt request (DTC or DMAC activation request) that is generated again will be ignored.

Note 2. When the DISEL bit is 0, operation with the remaining number of transfer operations being 0 differs according to whether the source is for DTC or DMAC.

Note 3. For chain transfer, DTC transfer continues until the last chain transfer ends. Whether a CPU interrupt is generated at the end of chain transfer, the IRn.IR flag clear timing, and the interrupt request destination after transfer are determined by the state of DISEL and the remaining transfer count at the end of chain transfer. For the chain transfer, see Table 19.3, Chain Transfer Conditions in section 19, Data Transfer Controller (DTCa).

The request destination for an interrupt should be changed while the IERm.IENj bit is 0.

When a source is to be changed to an interrupt request or the DMA activation source is to be changed while a transfer is not complete (i.e. while the DMACm.DMCNT.DTE bit has not been cleared) after the settings described under (1) DMAC Activation have been made, follow the procedure below.

1. For both the source to be withdrawn and the source that will have a new target for activation, clear the IENj bits in IERm to 0.
2. Check the state of transfer by the DMAC. If transfer is in progress, wait for its completion.
3. Make the settings described under (1) DMAC Activation.

When a source is to be changed to an interrupt request or the DTC transfer information is to be changed while a transfer is not complete (i.e. while the DTCERn.DTCE bit has not been cleared) after the settings described under (2) DTC Activation have been made, follow the procedure below.

1. For both the source to be withdrawn and the source that will have a new target for activation, clear the IENj bits in IERm to 0.
2. Check the state of transfer by the DTC. If transfer is in progress, wait for its completion.
3. Make the settings described under (2) DTC Activation.

15.5.4 Determining Priority

Interrupt priority is determined for each interrupt request destination.
The priority for each interrupt request destination is determined as follows.

(1) Determining Priority when the CPU is the Request Destination of the Interrupt Signal

A source selected for the fast interrupt has the highest priority. After that, an interrupt source with a larger value of the interrupt priority level select bits (IPR[3:0]) in IPRn takes priority. If interrupts with the same priority level are generated by multiple sources, the source with the smallest vector number takes precedence.

(2) Determining Priority when the DTC is the Request Destination of the Interrupt Signal

The IPR[3:0] bits in IPRn have no effect. An interrupt source with a smaller vector number takes precedence.

(3) Determining Priority when the DMAC is the Request Destination of the Interrupt Signal

The IPR[3:0] bits in IPRn have no effect. Regarding the order of priority of DMAC channels, see section 18, DMA Controller (DMACA).

15.5.5 Multiple Interrupt

Multiple interrupt is enabled by setting the PSW.I bit to 1 within the processing routine for the interrupt accepted.
The PSW.IPL[3:0] bits indicate the priority level of the accepted interrupt request. At this time, if an interrupt request with higher priority level than the value shown in the PSW.IPL[3:0] bits is generated, such interrupt request is accepted (multiple interrupt occurred).

15.5.6 Fast Interrupt

The fast interrupt is a facility for faster interrupt response by the CPU, to only one assigned interrupt source among interrupt sources.
The fast interrupt, which has the highest interrupt priority level of 15, takes precedence over other level-15 priority interrupt sources regardless of the value set in the IPRn.IPR[3:0] bits. However, if the value of the PSW.IPL[3:0] bits is 1111b (priority level 15), the fast interrupt is not accepted.
An interrupt source can be assigned to the fast interrupt by writing the vector number of the source to the FIR.FVCT[7:0] bits and set the FIR.FIEn bit to 1 (fast interrupt enabled).
For details on the fast interrupt, see section 14, Exception Handling.

15.5.7 Digital Filter

The digital filter function is provided for the external interrupt request IRQi pins (i = 0 to 7) and NMI pin interrupt.
The digital filter samples input signals at the filter sampling clock (PCLK) and removes the pulses of which length is less than three sampling cycles.
To use the digital filter for the IRQi pin, set the sampling clock cycle (PCLK, PCLK/8, PCLK/32, or PCLK/64) with the IRQFLTC0.FCLKSELi[1:0] bits (i = 0 to 7) and set the IRQFLTEn.FLTENi bit to 1 (digital filter enabled).
To use the digital filter for the NMI pin, set the sampling clock cycle (PCLK, PCLK/8, PCLK/32, or PCLK/64) with the NMIFLTC.NFCLKSEL[1:0] bits and set the NMIFLTE.NFLTEN bit to 1 (digital filter enabled).
Figure 15.15 shows an example of digital filter operation.

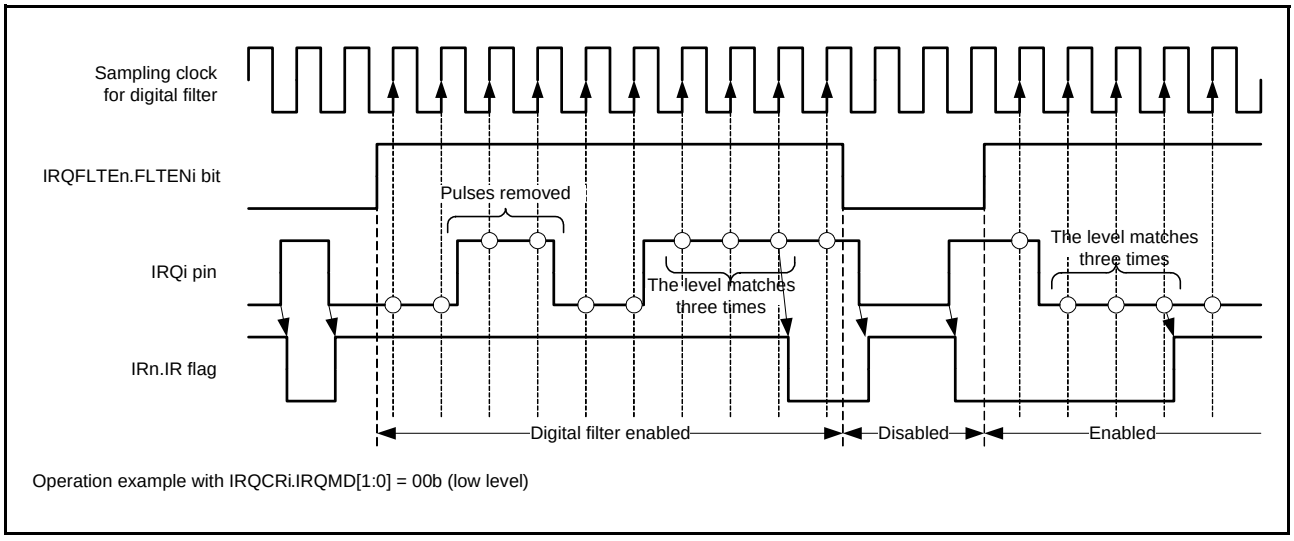


Figure 15.15 Digital Filter Operation Example

Before software standby mode is entered, set the IRQFLTEn.FLTENi and NMIFLTE.NFLTEN bits to 0 (digital filter disabled). To use the digital filter again after return from software standby mode, set the IRQFLTEn.FLTENi or NMIFLTE.NFLTEN bit to 1 (digital filter enabled).

15.5.8 External Pin Interrupts

The procedure for using the signal on an external pin as an interrupt is as follows.

1. Clear the IERm.IENj bit to 0 (interrupt request disabled).
2. Clear the IRQFLTE0.FLTENi[1:0] bits (i = 0 to 7) to 0 (digital filter disabled).
3. Set the digital filter sampling clock with the IRQFLTC0.FCLKSELi[1:0] bits.
4. Make or confirm the I/O port settings.
5. Set the method of detection for the interrupt in the IRQCRi.IRQMD[1:0] bits.
6. Clear the corresponding IRn.IR flag to 0 (if edge detection is in use).
7. Set the IRQFLTE0.FLTENi bit to 1 (digital filter enabled).
8. If the interrupt is to be used for DMAC activation, set the DMRSRm.DMRS[7:0] bits. If the interrupt is to be used for DTC activation, set the DTCERn.DTCE bit. The interrupt will be a CPU interrupt if neither of these settings is made.
9. Set the IERm.IENj bit to 1 (interrupt request enabled).

15.6 Non-maskable Interrupt Operation

There are six types of non-maskable interrupt: the NMI pin interrupt, oscillation stop detection interrupt, WDT underflow/refresh error, IWDT underflow/refresh error, voltage-monitoring 1 interrupt, and voltage-monitoring 2 interrupt. Non-maskable interrupts are only usable as interrupts for the CPU; that is, they are not capable of DTC or DMAC activation. Non-maskable interrupts take precedence over all interrupts, including the fast interrupt.
Non-maskable interrupt requests are accepted regardless of the states of the I (interrupt enable) bit and IPL[3:0] (processor interrupt priority level) bits in the PSW of the CPU. The current states of the non-maskable interrupts can be checked in the non-maskable interrupt status register (NMISR).
Confirm that all bits in the NMISR have returned to 0 from within the handler for the non-maskable interrupt.
Non-maskable interrupts are disabled by default. If a system is to use non-maskable interrupts, the following procedure must be followed at the beginning of program processing.

Non-maskable interrupt usage procedure:

1. Set the stack pointer (SP).
2. To use the NMI pin, clear the NMIFLTE.NFLTEN bit to 0 (digital filter disabled).
3. To use the NMI pin, set the digital filter sampling clock with the NMIFLTC.NFCLKSEL[1:0] bits.
4. To use the NMI pin, set the NMI pin detection sense with the NMICR.NMIMD bit.
5. To use the NMI pin, write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
6. To use the NMI pin, set the NMIFLTE.NFLTEN bit to 1 (digital filter enabled).
7. Enable the non-maskable interrupt by writing 1 to the corresponding bit in the non-maskable interrupt enable register (NMIER).

After 1 is written to each interrupt enable bit in the NMIER register, subsequent write access to the respective bits is ignored. Interrupt sources that have once been enabled cannot be disabled. They are disabled only by a reset.
For the flow of non-maskable interrupt processing, see section 14, Exception Handling.

Writing 1 to the NMICLR.NMICLR bit clears the NMI status flag (NMISR.NMIST) to 0.
Writing 1 to the NMICLR.OSTCLR bit clears the oscillation stop detection interrupt status flag (NMISR.OSTST) to 0.
Writing 1 to the NMICLR.WDTCLR bit clears the WDT underflow/refresh error status flag (NMISR.WDTST) to 0.

Writing 1 to the NMICLR.IWDTCLR bit clears the IWDT underflow/refresh error status flag (NMISR.IWDTST) to 0.
Writing 1 to the NMICLR.LVD1CLR bit clears the voltage-monitoring 1 interrupt status flag (NMISR.LVD1ST) to 0.
Writing 1 to the NMICLR.LVD2CLR bit clears the voltage-monitoring 2 interrupt status flag (NMISR.LVD2ST) to 0.

15.7 Return from Power-Down States

The interrupt sources that can be used to return operation from sleep mode, all-module clock stop mode, or software standby mode are listed in Table 15.3, Interrupt Vector Table.
For details, refer to section 12, Low Power Consumption. The following describes how to use an interrupt to return operation from each power-down mode.

15.7.1 Return from Sleep Mode

If the interrupt controller is to return operation from sleep mode in response to an interrupt or non-maskable interrupt (except for the WDT underflow/refresh error interrupt), make the following settings for the interrupt.

- Interrupts

1. Select the CPU as the interrupt request destination.
2. Use the IENj bit in IERm to enable the given interrupt request.
3. Set a priority level higher than that set by the IPL[3:0] bits in the PSW of CPU.
4. Use the ENj bit in GENm to enable the given grouped interrupt requests.

- Non-maskable interrupts

Use the NMIER register to enable the given interrupt request.

15.7.2 Return from All-Module Clock Stop Mode

If the interrupt controller is to return operation from all-module clock stop mode in response to an interrupt or non-maskable interrupt (except for the WDT underflow/refresh error interrupt), make the following settings for the interrupt.

- Interrupts

1. Select the interrupt source that enables the return from the all-module clock stop mode.
2. Select the CPU as the interrupt request destination.
3. Use the IENj bit in IERm to enable the given interrupt request.
4. Set a priority level higher than that set by the IPL[3:0] bits in the PSW of CPU.

- Non-maskable interrupts

Use the NMIER register to enable the given interrupt request.

15.7.3 Return from Software Standby Mode

The interrupt controller can return operation from a non-maskable interrupt (except for the WDT underflow/refresh error interrupt) or an interrupt that enables the return from the software standby mode.
The conditions for the return are listed below.

- Interrupts

1. Select the interrupt source that enables the return from the software standby mode.
2. Select the CPU as the interrupt request destination.
3. Use the IENj bit in IERm to enable the given interrupt request.
4. Set a priority level higher than that set by the IPL[3:0] bits in the PSW of CPU.
   (For the interrupt source specified as a fast interrupt, as well as setting the fast interrupt set register (FIR), the interrupt priority level (IPRn) should be set above the level set by IPL in the PSW of the CPU.)

Interrupt requests through the IRQ pins that do not satisfy the above conditions are not detected while the clock is stopped in software standby mode.

- Non-maskable interrupts

Use the NMIER register to enable the given interrupt request.

Use the following procedure to make a transition to/from software standby mode.

1. Before software standby mode is entered, disable the digital filter for the interrupt source as a return target (IRQFLTEn.FLTENi = 0, NMIFLTE.NFLTEN = 0).
2. To use the digital filter again after return from software standby mode, enable the digital filter (IRQFLTEn.FLTENi = 1, NMIFLTE.NFLTEN = 1).

15.8 Usage Note

15.8.1 Note on WAIT Instruction Used with Non-Maskable Interrupt

Confirm that all status flags in register NMISR are 0 whenever a WAIT instruction is to be issued.

15.8.2 Note on Using the MTU3 Interrupt

If conditions *1, *2, or *3 apply when the status flag in the timer status register (TSR) is to be cleared to 0, and a flag setting request is generated to set the corresponding flag to 1 before 0 has been written to the flag after 1 was read from the flag, the corresponding flag will not be cleared and will thus retain the value 1.

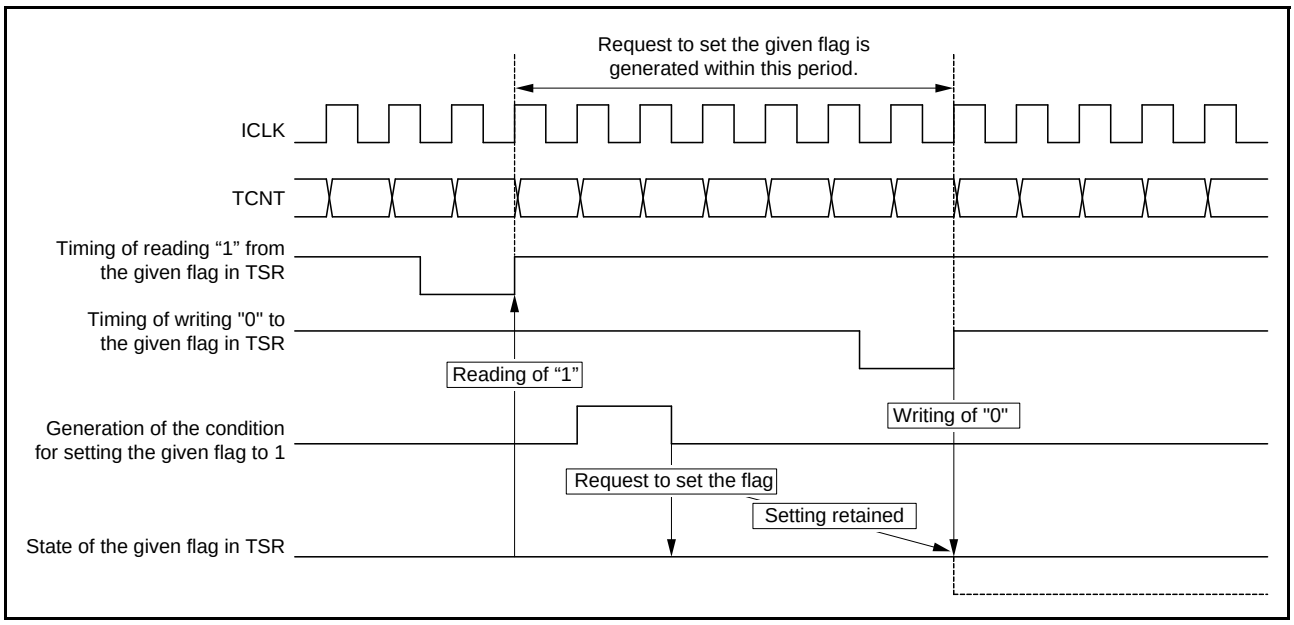


Figure 15.16 State of the Status Flag in the TSR Register

*1: TGFm flag (input capture/output compare flag m) (m = A to F)
[Setting conditions]
• TCNT = TGRm while the TGRm register is functioning as an output compare register or compare register
• Transfer of the value in TCNT to the TGRm register in response to the input capture signal while the TGRm register is functioning as an input capture register

[Clearing condition]
• After the TGFm flag is read while TGFm = 1, writing of “0” to the TGFm flag

*2: TCFj flag (overflow/underflow flag) (j = V, U)
[Setting conditions]
• Overflow of the TCNT (FFFFh → 0000h)
• Underflow of the TCNT (0000h → FFFFh)

[Clearing condition]
• After the TCFj flag is read while TCFj = 1, writing of “0” to the TCFj flag

*3: CMFn5 compare match/input capture flag n (n = U, V, W)
[Setting conditions]
• MTU5.TCNTn = MTU5.TGRn while the MTU5.TGRn is functioning as a compare match register
• Transfer of the value in MTU5.TCNTn to MTU5.TGRn in response to the input capture signal while the MTU5.TGRn

is functioning as an input capture register
• Transfer of the value in MTU5.TCNTn to MTU5.TGRn in response to the input capture signal while the MTU5.TGRn is in use for measuring the pulse width of an externally input signal

[Clearing condition]
• After the CMFn5 flag is read while CMFn5 = 1, writing of “0” to the CMFn5 flag

The interrupt request is ignored as long as the corresponding flag in the TSR register is 1. Therefore, to re-enable the interrupt, clear the corresponding flag and then execute the procedure in the flowchart for software to avoid problems (Figure 15.17).

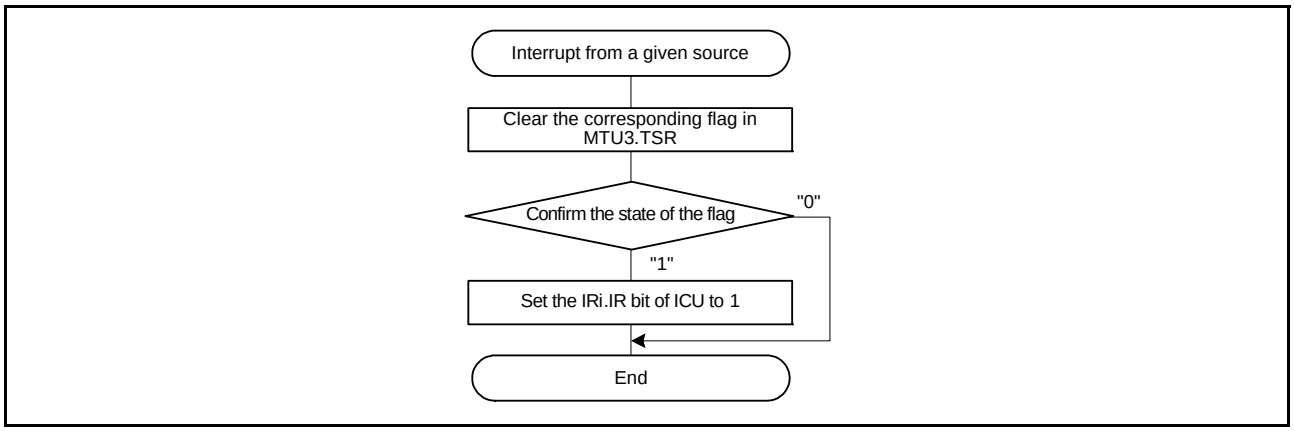


Figure 15.17 Flowchart for Software to Avoid Problems

16. Buses

16.1 Overview

Table 16.1 lists the bus specifications, Figure 16.1 shows the bus configuration, and Table 16.2 lists the addresses assigned for each bus.

Table 16.1 Bus Specifications

Bus Type		Description
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	• Connected to RAM
	Memory bus 2	• Connected to ROM
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USB) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3, GPT, and DPC) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	Reserved area
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)

P/E: Programming/Erasure

BCLK (external-bus clock): 50 MHz (max.) The CSC (CS area controller) operate in synchronization with the BCLK.

BCLK pin output: The frequency is the same as the BCLK as default. 1/2 BCLK can be supplied by setting the BCLK pin output select bit (BCKCR.BCLKDIV) in the external bus clock control register. For details, see section 10, Clock Generation Circuit.

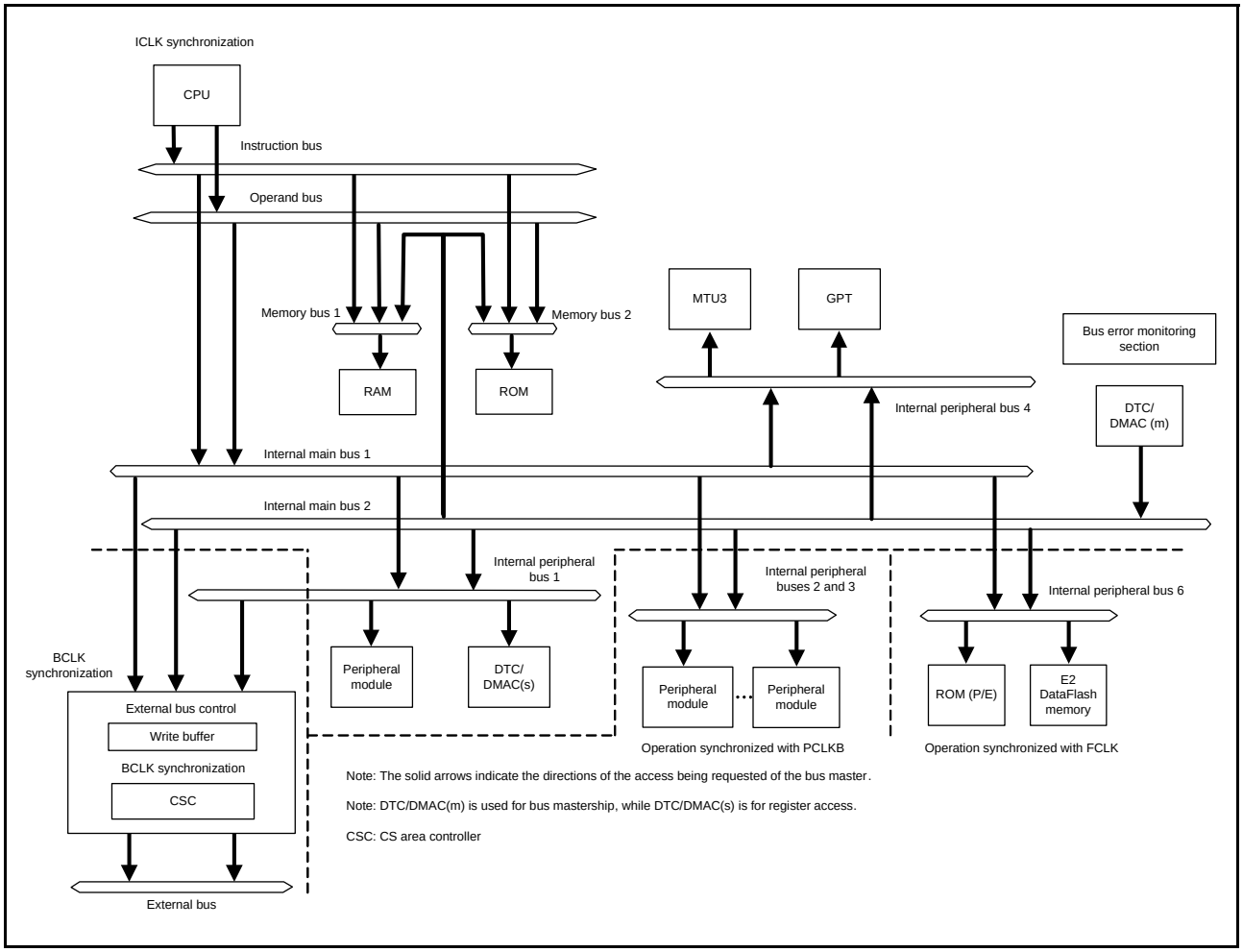


Figure 16.1 Bus Configuration

Table 16.2 Addresses Assigned for Each Bus

Address	Bus		Area	
	On-Chip ROM Enabled	On-Chip ROM Disabled	On-Chip ROM Enabled	On-Chip ROM Disabled
0000 0000h to 0000 BFFFh	Memory bus 1		RAM	
0000 C000h to 0007 FFFFh			Reserved area	
0008 0000h to 0008 7FFFh	Internal peripheral bus 1		Peripheral I/O registers	
0008 8000h to 0009 FFFFh	Internal peripheral bus 2			
000A 0000h to 000B FFFFh	Internal peripheral bus 3			
000C 0000h to 000D FFFFh	Internal peripheral bus 4			
000E 0000h to 000F FFFFh	Reserved area			
0010 0000h to 00FF FFFFh	Internal peripheral bus 6	Reserved area	E2 DataFlash memory, ROM (P/E)	Reserved area
0100 0000h to 04FF FFFFh	External bus		Reserved area	
0500 0000h to 07FF FFFFh			External address space (CS1 to CS3)	
0800 0000h to 0FFF FFFFh			Reserved area	
1000 0000h to 7FFF FFFFh	Reserved area		Reserved area	
8000 0000h to FEFF FFFFh	Memory bus 2	Reserved area	ROM	Reserved area
FF00 0000h to FFFF FFFFh		External bus		External address space (CS0)

16.2 Description of Buses

16.2.1 CPU Buses

The CPU buses consist of the instruction and operand buses, which are connected to internal main bus 1. As the names suggest, the instruction bus is used to fetch instructions for the CPU, while the operand bus is used for operand access. Connection of the instruction and operand buses to on-chip RAM and on-chip ROM provides the CPU with direct access to these areas, i.e. access is not via internal main bus 1. However, only reading is possible in direct access to on-chip ROM by the CPU; programming and erasure are handled via an internal peripheral bus.

Bus requests for instruction fetching and operand access are arbitrated through internal main bus 1. The order of priority is operand access then instruction fetching.

If instruction fetching and operand access are requested for different buses (memory bus 1, memory bus 2, and internal main bus 1), the bus-access operations can proceed simultaneously. For example, parallel access to on-chip ROM and on-chip RAM or to on-chip ROM and external space is possible.

16.2.2 Memory Buses

The memory buses consist of memory bus 1 and memory bus 2. On-chip RAM is connected to memory bus 1 and on-chip ROM is connected to memory bus 2. Requests for bus mastership from the CPU buses (instruction fetching and operand) and internal main bus 2 are arbitrated through memory buses 1 and 2.

The priority order of CPU bus and internal main bus 2 can be set using the memory bus 1 (on-chip RAM) priority control bits (BPRA[1:0]) and memory bus 2 (on-chip ROM) priority control bits (BPRO[1:0]) in the bus priority control register (BUSPRI) for the corresponding memory buses. When the priority order is fixed, internal main bus 2 has priority over the CPU bus (operand over instruction fetching). When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

16.2.3 Internal Main Buses

The internal main buses consist of a bus for use by the CPU (internal main bus 1) and a bus for use by the other bus-master modules, i.e. the DTC, and DMAC DMAC (internal main bus 2).
Bus requests for instruction fetching and operand access are arbitrated through internal main bus 1. The order of priority is operand access then instruction fetching.
Requests for bus mastership from the DTC, and DMAC are arbitrated by internal main bus 2. The order of priority is DMAC, and then DTC as listed in Table 16.3.
Between the DTC and DMAC, only the one that accepted the activation request issues the bus mastership request. The priority order of activation requests between the DTC and DMAC is DMAC0, DMAC1, DMAC2, DMAC3, and then DTC, regardless of the BUSPRI setting.
If the CPU and another bus master are requesting access to different buses (on-chip memory and internal peripheral buses 1 to 6, and external bus), the respective bus-access operations can proceed simultaneously.
However, when the CPU executes the XCHG instruction, requests for bus access from masters other than the CPU are not accepted until data transfer for the XCHG instruction is completed regardless of the bus priority control register (BUSPRI) setting. Furthermore, requests for bus access from masters other than the DTC are not accepted during reading and writing-back of transfer control information for the DTC.

Table 16.3 Order of Priority for Bus Masters

Priority	Bus Master
High	DMAC
↑	DTC
Low	CPU

16.2.4 Internal Peripheral Buses

Connection of peripheral modules to the internal peripheral buses is as described in Table 16.4.

Table 16.4 Connection of Peripheral Modules to the Internal Peripheral Buses

Type of Bus	Peripheral Modules
Internal peripheral bus 1	DTC, DMAC, interrupt controller, and bus error monitoring section
Internal peripheral bus 2	Peripheral modules other than those connected to internal peripheral buses 1, 3, 4, and 5
Internal peripheral bus 3	USB
Internal peripheral bus 4	MTU3, GPT, and DPC
Internal peripheral bus 5	Reserved area
Internal peripheral bus 6	ROM (P/E)/E2 DataFlash memory

Requests for bus mastership from the CPU (internal main bus 1) and other bus masters (internal main bus 2) are arbitrated through internal peripheral buses 1 to 6.
The priority order of two internal main buses can be set using the bus priority control register (BUSPRI). The priority order can be set with the internal peripheral bus 1 priority control bits (BUSPRI.BPIB[1:0]), internal peripheral bus 2 and 3 priority control bits (BUSPRI.BPGB[1:0]), internal peripheral bus 4 priority control bits (BUSPRI.BPHB[1:0]), and internal peripheral bus 6 priority control bits (BUSPRI.BPFB[1:0]) for the corresponding internal peripheral buses.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1. When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.
The order of accepting requests may change depending on the BUSPRI setting (Refer to Figure 16.2).

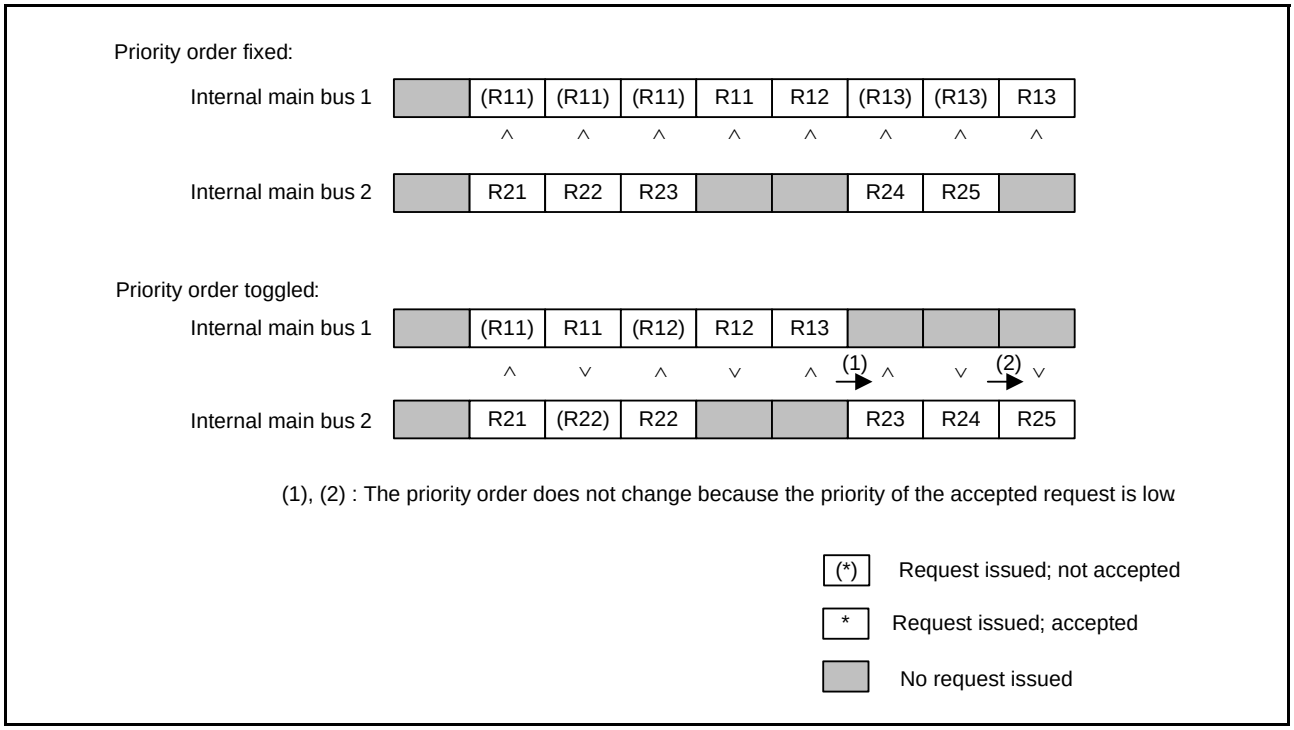


Figure 16.2 Priority Order between Internal Peripheral Bus Accesses

16.2.5 Write Buffer Function (Internal Peripheral Bus)

The internal peripheral bus has the write buffer function, which allows the next round of bus access to start, before the current write access is completed, in write access. However, if the following round of bus access is from the same bus master but to the different internal peripheral bus, it is suspended until the bus operations already in progress are completed. When read access to the internal memory is scheduled after the write access to the internal peripheral bus from the CPU, the following round of bus access can be started before the current bus operation is completed and thus the order of accesses may be changed (Refer to Figure 16.3).

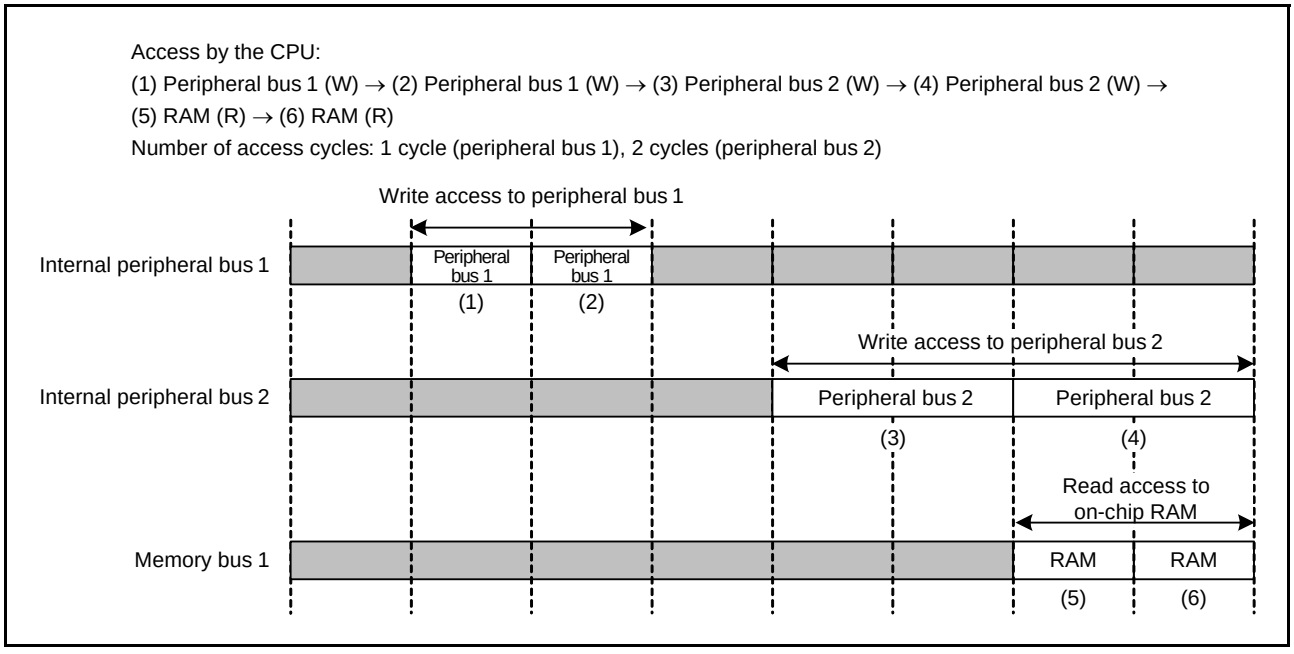


Figure 16.3 Write Buffer Function

16.2.6 External Bus

Table 16.5 lists the specifications of the external bus.
The external bus controller arbitrates requests for bus mastership from internal main bus 1, and internal main bus 2. The priority order of these two buses can be set using the external bus priority control bits (BPEB[1:0]) in the bus priority control register (BUSPRI). When the priority order is fixed, the order is internal main bus 2, and then internal main bus 1. When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted, between internal main bus 1 and internal main bus 2.
The order of accepting requests may change depending on the BUSPRI setting (Refer to Figure 16.4).

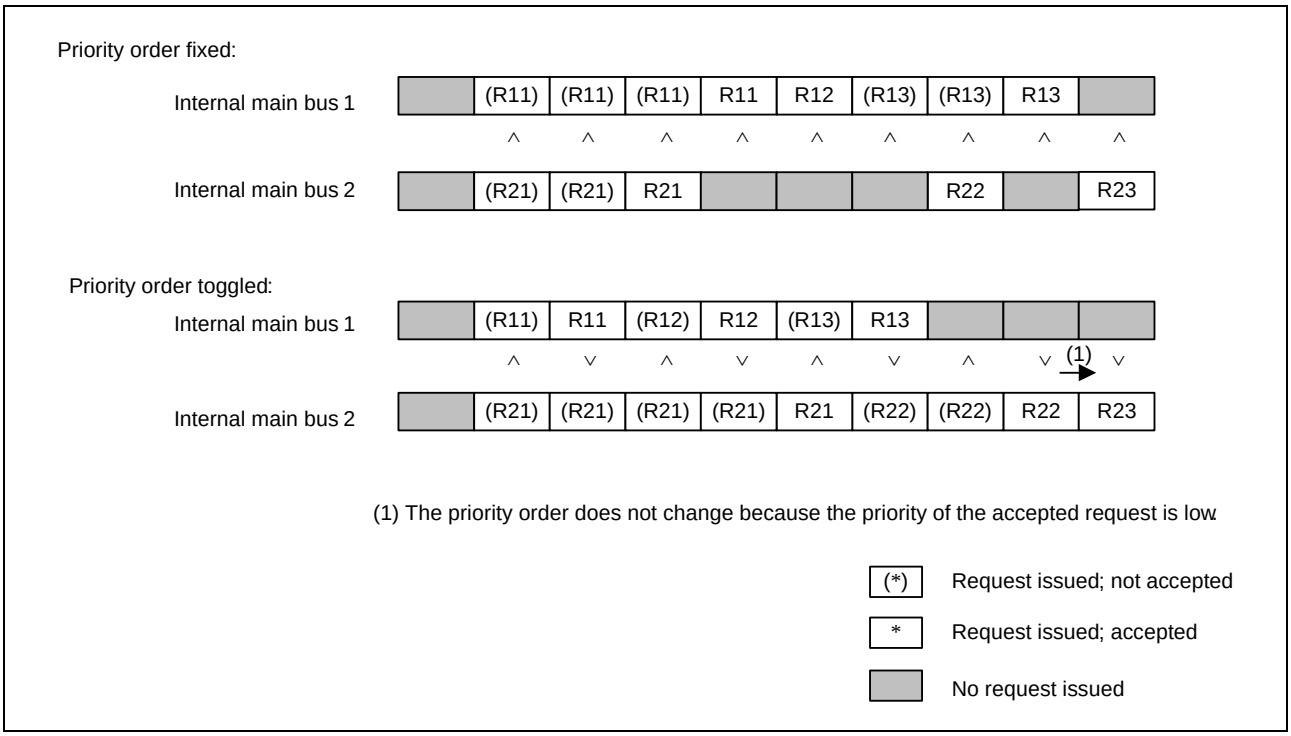


Figure 16.4 Priority Order of Internal Peripheral Bus Accesses

Table 16.5 Specifications of the External Bus

Item	Description
External address space	• An external address space is divided into four CS areas (CS0 to CS3) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. Separate bus: An 8, or 16-bit bus space is selectable. Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.
CS area controller	• Recovery cycles can be inserted. Read recovery: Up to 15 cycles Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. Timing of assertion and negation for chip-select signals (CS0# to CS3#) The timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, WR1#) The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
Write buffer function	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.
Frequency	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).

Table 16.6 lists the input/output pins of the external bus.

Table 16.6 Pin Configuration of the External Bus

Pin Name	I/O	Description
A19 to A0*1	Output	Address output pins
D15 to D0	I/O	Data input/output pins D15 to D0 pins are enabled when the 16-bit bus space is specified. D7 to D0 pins are enabled when the 8-bit bus space is specified.
BC0#*1	Output	A strobe signal; (the BC0# signal being at the low level) during access to an external address space in single write strobe mode indicates that D7 to D0 are valid. When an 8-bit bus space is specified, this output pin is always held low regardless of write access mode.
BC1#	Output	A strobe signal; (the BC1# signal being at the low level) during access to an external address space in single write strobe mode indicates that D15 to D8 are valid. This pin is not used when the 8-bit bus space is specified.
CS0#	Output	A chip select signal for area 0 (CS0)
CS1#	Output	A chip select signal for area 1 (CS1)
CS2#	Output	A chip select signal for area 2 (CS2)
CS3#	Output	A chip select signal for area 3 (CS3)
RD#	Output	A strobe signal indicating that reading from an external address space (CS0 to CS7) is in progress
WR0#/WR#*2	Output	WR0# signal is a strobe signal indicates that (the WR0# signal being at the low level) writing to an external address space is in progress in byte strobe mode, and D7 to D0 are valid. WR# signal is a strobe signal that indicates writing to an external address space is in progress in single write strobe mode. When an 8-bit bus space is specified, this output pin is held low during a write access regardless of write access mode.
WR1#	Output	A strobe signal; (the WR1# signal being at the low level) during writing to an external address space in byte strobe mode indicates that D15 to D8 are valid. This signal is invalid in single write strobe mode. This pin is not used when the 8-bit bus space is specified.
ALE	Output	Address latch signal when address/data multiplexed bus is selected.
WAIT#	Input	A wait request signal when accessing the external address space (CS0 to CS3) (Low: Wait request)

Note 1. The A0 and BC0# pin functions share the same pin, and either becomes effective according to the area, with the function being A0 in byte strobe mode and BC0# in single write strobe mode. Note that setting the 8-bit external bus width is prohibited in single write strobe mode. For information on other multiplexed pin functions, see section 20, I/O Ports.

Note 2. The WR0# signal and WR# signal are identical. The WR0# signal is particularly referred to as WR# in single write strobe mode.

16.2.7 Parallel Operation

Parallel operation is possible when different bus-master modules are requesting access to different slave modules. For example, if the CPU is fetching an instruction from on-chip ROM and an operand from on-chip RAM, the DMAC is able to handle transfer between a peripheral bus and the external bus at the same time.
An example of parallel operations is shown in Figure 16.5. In this example, the CPU is able to employ the instruction and operand buses for simultaneous access to on-chip ROM and on-chip RAM, respectively. Furthermore, the DMACA simultaneously employs internal main bus 2 for access to a peripheral bus or the external bus during access to on-chip RAM and ROM by the CPU.

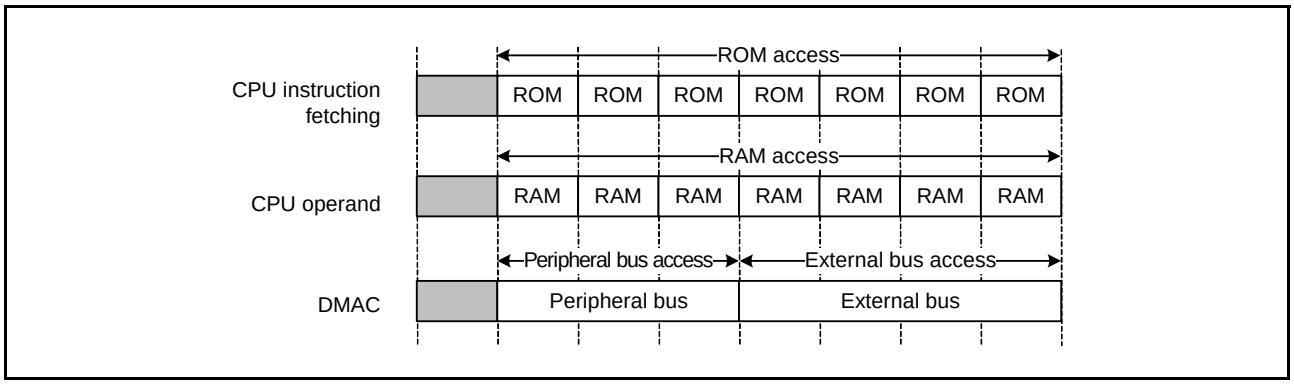


Figure 16.5 Example of Parallel Operations

16.2.8 Bus Settings

(1) Set the mode of the external bus in the CSn mode register (CSnMOD), CSn wait-control register 1 (CSnWCR1), CSn wait-control register 2 (CSnWCR2), CSn control register (CSnCR), CSn recovery-cycle setting register (CSnREC), CS recovery cycle insertion enable register (CSRECEN), bus error monitoring enable register (BEREN), and bus priority control register (BUSPRI).
(2) Make settings for pins in the CS output enable register (PFCSE), CS output pin selection register 0 (PFCSS0), address output enable register 0 (PFAOE0), address output enable register 1 (PFAOE1), external-bus control register 0 (PFBCR0), and external-bus control register 1 (PFBCR1).
(3) Set up pins to be used as input port pins.

Set the external-bus enable bit (EXBE) in the system control register 0 (SYSCR0) to 1 (enabling the external bus).

16.2.9 Restrictions

(1) Prohibition of Access that Spans Areas of Address Space

Single access that spans two areas of the address space is prohibited, and operation of such an access is not guaranteed. Setting must be made so that two areas are not accessed at the same time by a single word or longword access.

(2) Restrictions in Relation to RMPA and String-Manipulation Instructions

(a) Although the external space has a per-area ending-switching facility (only for data), the allocation of data to be handled by RMPA or string-manipulation instructions to an area where the endian differs from that of the chip is prohibited, and operation is not guaranteed if this restriction is not observed. If data to be handled by RMPA or string-manipulation instructions are allocated to the external space, they must be allocated to areas where the endian setting is the same as that for the chip.
(b) The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(3) Restriction on Endian

When the endian setting for each area is different from that for the chip, no instruction code can be allocated in the area. The instruction code should be allocated to the external space whose endian setting is the same as that for the chip.

16.3 Register Descriptions

16.3.1 CSn Control Register (CSnCR) (n = 0 to 3)

Address(es): CS0CR 0008 3802h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Address(es): CS1CR 0008 3812h, CS2CR 0008 3822h, CS3CR 0008 3832h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EXENB	Operation Enable	0: Operation is disabled 1: Operation is enabled	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	BSIZE[1:0]	External Bus Width Select	b5 b4 0 0: A 16-bit bus space is selected 0 1: Setting prohibited 1 0: An 8-bit bus space is selected 1 1: Setting prohibited	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	EMODE	Endian Mode	0: Endian of area n is the same as the endian of operating mode. 1: Endian of area n is not the endian of operating mode. (n = 0 to 3)	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	MPXEN	Address/Data Multiplexed I/O Interface Select	0: Separate bus interface is selected for area n. 1: Address/data multiplexed I/O interface is selected for area n. (n = 0 to 3)	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not write to the CSnCR register while access to the CSn area is in progress.

EXENB Bit (Operation Enable)

This bit enables or disables operation of the respective CS areas.

After this MCU is reset, operation is enabled (EXENB = 1) only for area 0; operation in other areas is disabled (EXENB = 0).

An attempt at access to an area for which operation has been disabled does not lead to access via the external bus. However, if the illegal address access detection enable bit in the bus error monitoring enable register has been set to enable detection (BEREN.IGAEN = 1), such an attempt will lead to an illegal-access error.

BSIZE[1:0] Bits (External Bus Width Select)

These bits specify the data bus width of each area.

The data bus width of area 0 (CS0) after a reset depends on the setting of the bus width in operating mode.

EMODE Bit (Endian Mode)

This bit specifies the endian of each area.

When the endian setting for each area is different from that for the chip, no instruction code can be allocated in the area.

The instruction code should be allocated to the external space whose endian setting is the same as that for the chip.

16.3.2 CSn Recovery Cycle Register (CSnREC) (n = 0 to 3)

Address(es): CS0REC 0008 380Ah, CS1REC 0008 381Ah, CS2REC 0008 382Ah, CS3REC 0008 383Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	WRCV[3:0]				—	—	—	—	RRCV[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	RRCV[3:0]	Read Recovery	b3 b0 0 0 0 0: No recovery cycle is inserted. 0 0 0 1: 1 recovery cycle is inserted. 0 0 1 0: 2 recovery cycles are inserted. 0 0 1 1: 3 recovery cycles are inserted. 0 1 0 0: 4 recovery cycles are inserted. 0 1 0 1: 5 recovery cycles are inserted. 0 1 1 0: 6 recovery cycles are inserted. 0 1 1 1: 7 recovery cycles are inserted. 1 0 0 0: 8 recovery cycles are inserted. 1 0 0 1: 9 recovery cycles are inserted. 1 0 1 0: 10 recovery cycles are inserted. 1 0 1 1: 11 recovery cycles are inserted. 1 1 0 0: 12 recovery cycles are inserted. 1 1 0 1: 13 recovery cycles are inserted. 1 1 1 0: 14 recovery cycles are inserted. 1 1 1 1: 15 recovery cycles are inserted.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	WRCV[3:0]	Write Recovery	b11 b8 0 0 0 0: No recovery cycle is inserted. 0 0 0 1: 1 recovery cycle is inserted. 0 0 1 0: 2 recovery cycles are inserted. 0 0 1 1: 3 recovery cycles are inserted. 0 1 0 0: 4 recovery cycles are inserted. 0 1 0 1: 5 recovery cycles are inserted. 0 1 1 0: 6 recovery cycles are inserted. 0 1 1 1: 7 recovery cycles are inserted. 1 0 0 0: 8 recovery cycles are inserted. 1 0 0 1: 9 recovery cycles are inserted. 1 0 1 0: 10 recovery cycles are inserted. 1 0 1 1: 11 recovery cycles are inserted. 1 1 0 0: 12 recovery cycles are inserted. 1 1 0 1: 13 recovery cycles are inserted. 1 1 1 0: 14 recovery cycles are inserted. 1 1 1 1: 15 recovery cycles are inserted.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not write to the CSnREC register while access to the CSn area is in progress.
When the preceding bus access is a separate bus access, CSnREC is valid when the recovery cycle insertion is enabled with the separate bus recovery cycle insertion enable bit (RCVENj (j = 0 to 7)) in CSRECEN. When the preceding bus access is an address/data multiplexed bus access, CSnREC is valid when the recovery cycle insertion is enabled with the multiplexed bus recovery cycle insertion enable bit (RCVENMj) in CSRECEN.

RRCV[3:0] Bits (Read Recovery)

These bits specify the number of recovery cycles to be inserted after a read access to the external bus.
When the recovery cycle insertion is enabled and a value except 0000b is written to these bits, one to 15 recovery cycles are inserted in the following cases.

- After a read access to the external bus, a read access is made to the external bus in the same area.
- After a read access to the external bus, a read access is made to the external bus in a different area.
- After a read access to the external bus, a write access is made to the external bus in the same area.
- After a read access to the external bus, a write access is made to the external bus in a different area.

WRCV[3:0] Bits (Write Recovery)

These bits specify the number of recovery cycles to be inserted after a write access to the external bus.
When the recovery cycle insertion is enabled and a value except 0000b is written to these bits, one to 15 recovery cycles are inserted in the following cases.

- After a write access to the external bus, a read access is made to the external bus in the same area.
- After a write access to the external bus, a read access is made to the external bus in a different area.
- After a write access to the external bus, a write access is made to the external bus in the same area.
- After a write access to the external bus, a write access is made to the external bus in a different area.

16.3.3 CS Recovery Cycle Insertion Enable Register (CSRECEN)

Address(es): 0008 3880h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCVENM7	RCVENM6	RCVENM5	RCVENM4	RCVENM3	RCVENM2	RCVENM1	RCVENM0	RCVEN7	RCVEN6	RCVEN5	RCVEN4	RCVEN3	RCVEN2	RCVEN1	RCVEN0
Value after reset:	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	RCVEN0	Separate Bus Recovery Cycle Insertion Enable	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b1	RCVEN1	Separate Bus Recovery Cycle Insertion Enable	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b2	RCVEN2	Separate Bus Recovery Cycle Insertion Enable 2	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b3	RCVEN3	Separate Bus Recovery Cycle Insertion Enable 3	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b4	RCVEN4	Separate Bus Recovery Cycle Insertion Enable 4	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b5	RCVEN5	Separate Bus Recovery Cycle Insertion Enable 5	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b6	RCVEN6	Separate Bus Recovery Cycle Insertion Enable 6	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b7	RCVEN7	Separate Bus Recovery Cycle Insertion Enable 7	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b8	RCVENM0	Multiplexed Bus Recovery Cycle Insertion Enable 0	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b9	RCVENM1	Multiplexed Bus Recovery Cycle Insertion Enable 1	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b10	RCVENM2	Multiplexed Bus Recovery Cycle Insertion Enable 2	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b11	RCVENM3	Multiplexed Bus Recovery Cycle Insertion Enable 3	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b12	RCVENM4	Multiplexed Bus Recovery Cycle Insertion Enable 4	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b13	RCVENM5	Multiplexed Bus Recovery Cycle Insertion Enable 5	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b14	RCVENM6	Multiplexed Bus Recovery Cycle Insertion Enable 6	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
b15	RCVENM7	Multiplexed Bus Recovery Cycle Insertion Enable 7	0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W

Do not write to the CSRECEN register while access to the CSn area is in progress.

RCVEN0 Bit (Separate Bus Recovery Cycle Insertion Enable 0)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a read access is made to the external bus in the same area.

RCVEN1 Bit (Separate Bus Recovery Cycle Insertion Enable 1)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a read access is made to the external bus in a different area.

RCVEN2 Bit (Separate Bus Recovery Cycle Insertion Enable 2)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a write access is made to the external bus in the same area.

RCVEN3 Bit (Separate Bus Recovery Cycle Insertion Enable 3)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a write access is made to the external bus in a different area.

RCVEN4 Bit (Separate Bus Recovery Cycle Insertion Enable 4)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a read access is made to the external bus in the same area.

RCVEN5 Bit (Separate Bus Recovery Cycle Insertion Enable 5)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a read access is made to the external bus in a different area.

RCVEN6 Bit (Separate Bus Recovery Cycle Insertion Enable 6)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a write access is made to the external bus in the same area.

RCVEN7 Bit (Separate Bus Recovery Cycle Insertion Enable 7)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a write access is made to the external bus in a different area.

RCVENM0 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 0)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a read access is made to the external bus in the same area.

RCVENM1 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 1)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a read access is made to the external bus in a different area.

RCVENM2 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 2)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a write access is made to the external bus in the same area.

RCVENM3 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 3)

This bit enables or disables the insertion of read recovery cycles when, after a read access to the external bus, a write access is made to the external bus in a different area.

RCVENM4 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 4)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a read access is made to the external bus in the same area.

RCVENM5 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 5)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a read access is made to the external bus in a different area.

RCVENM6 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 6)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a write access is made to the external bus in the same area.

RCVENM7 Bit (Multiplexed Bus Recovery Cycle Insertion Enable 7)

This bit enables or disables the insertion of write recovery cycles when, after a write access to the external bus, a write access is made to the external bus in a different area.

Table 16.7 Insertion of Recovery Cycles

Access Type	External Address Space	Insertion of Recovery Cycles	Corresponding Bits (Separate/Multiplexed)
Read access after read access	Same area	Recovery cycles specified by the RRCV[3:0] bits are inserted.	RCVEN0/RCVENM0
	Different area	Recovery cycles specified by the RRCV[3:0] bits are inserted.	RCVEN1/RCVENM1
Read access after write access	Same area	Recovery cycles specified by the RRCV[3:0] bits are inserted.	RCVEN2/RCVENM2
	Different area	Recovery cycles specified by the RRCV[3:0] bits are inserted.	RCVEN3/RCVENM3
Write access after read access	Same area	Recovery cycles specified by the WRCV[3:0] bits are inserted.	RCVEN4/RCVENM4
	Different area	Recovery cycles specified by the WRCV[3:0] bits are inserted.	RCVEN5/RCVENM5
Write access after write access	Same area	Recovery cycles specified by the WRCV[3:0] bits are inserted.	RCVEN6/RCVENM6
	Different area	Recovery cycles specified by the WRCV[3:0] bits are inserted.	RCVEN7/RCVENM7

16.3.4 CSn Mode Register (CSnMOD) (n = 0 to 3)

Address(es): CS0MOD 0008 3002h, CS1MOD 0008 3012h, CS2MOD 0008 3022h, CS3MOD 0008 3032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRMOD	—	—	—	—	—	PWENB	PRENB	—	—	—	—	EWENB	—	—	WRMOD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WRMOD	Write Access Mode Select	0: Byte strobe mode 1: Single write strobe mode	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	EWENB	External Wait Enable	0: External wait is disabled 1: External wait is enabled	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PRENB	Page Read Access Enable	0: Page read access is disabled 1: Page read access is enabled	R/W
b9	PWENB	Page Write Access Enable	0: Page write access is disabled 1: Page write access is enabled	R/W
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	PRMOD	Page Read Access Mode Select	0: Normal access compatible mode 1: External data read continuous assertion mode	R/W

Do not write to the CSnMOD register while access to the CSn area is in progress.

WRMOD Bit (Write Access Mode Select)

This bit selects a write access operating mode.

Writing 0 to this bit selects byte strobe mode where data write operation is controlled by the WRn# (n = 0 or 1) signal corresponding to the respective byte positions.

Writing 1 to this bit selects single write strobe mode where data write operation is controlled by the BCn# (n = 0 or 1) signal and the WR# signal corresponding to respective byte positions. Note that setting the external bus width of 8 bits is prohibited in single write strobe mode.

Table 16.8 Control Signals for Write Access Mode

Mode	Pin Name			
Write Access Mode	**WR1#**	**WR0#/WR#**	**BC1#**	**BC0#**
Byte strobe mode	○	○ (WR0#)	×	×
Single write strobe mode	×	○ (WR#)	○	○

○: Enabled, ×: Disabled

EWENB Bit (External Wait Enable)

This bit enables or disables external wait.

Writing 1 to this bit selects external wait and allows control of the number of waits in each cycle with the WAIT# signal. In this state, wait cycles are inserted while the WAIT# signal is at the low level.

Writing 0 to this bit disables the WAIT# signal.

PRENB Bit (Page Read Access Enable)

This bit enables or disables page read accesses.

Note: • When the address/data multiplexed I/O interface is selected with the MPXEN bit in CSnCR, this bit should not be set to enable page read accesses. Page read accesses are not supported in the address/data multiplexed I/O interface.

PWENB Bit (Page Write Access Enable)

This bit enables or disables page write accesses.

Note: • When the address/data multiplexed I/O interface is selected with the MPXEN bit in CSnCR, this bit should not be set to enable page read accesses. Page read accesses are not supported in the address/data multiplexed I/O interface.

PRMOD Bit (Page Read Access Mode Select)

This bit selects a page read access operating mode.

Writing 0 to this bit selects normal access compatible mode where the RD# signal is negated and RD assert wait is inserted each time a piece of data is read. However, when there is no RD assert wait, the RD# signal is negated only in the final transfer of the external bus access.

Writing 1 to this bit selects external data read continuous assertion mode where RD assert wait is inserted and the RD# signal is continuously asserted during this time period.

16.3.5 CSn Wait Control Register 1 (CSnWCR1) (n = 0 to 3)

Address(es): CS0WCR1 0008 3004h, CS1WCR1 0008 3014h, CS2WCR1 0008 3024h, CS3WCR1 0008 3034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	CSRWAIT[4:0]					—	—	—	CSWWAIT[4:0]				
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CSPRWAIT[2:0]			—	—	—	—	—	CSPWWAIT[2:0]		
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	CSPWWAIT[2:0]	Page Write Cycle Wait Select*1	b2 b0 0 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CSPRWAIT[2:0]	Page Read Cycle Wait Select*2	b10 b8 0 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b20 to b16	CSWWAIT[4:0]	Normal Write Cycle Wait Select	b20 b16 0 0 0 0 0: No wait is inserted. 0 0 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 0 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 0 0 1 1: Wait with a length of 3 clock cycles are inserted. 0 0 1 0 0: Wait with a length of 4 clock cycles are inserted. 0 0 1 0 1: Wait with a length of 5 clock cycles are inserted. 0 0 1 1 0: Wait with a length of 6 clock cycles are inserted. 0 0 1 1 1: Wait with a length of 7 clock cycles are inserted. 0 1 0 0 0: Wait with a length of 8 clock cycles are inserted. 0 1 0 0 1: Wait with a length of 9 clock cycles are inserted. 0 1 0 1 0: Wait with a length of 10 clock cycles are inserted. 0 1 0 1 1: Wait with a length of 11 clock cycles are inserted. 0 1 1 0 0: Wait with a length of 12 clock cycles are inserted. 0 1 1 0 1: Wait with a length of 13 clock cycles are inserted. 0 1 1 1 0: Wait with a length of 14 clock cycles are inserted. 0 1 1 1 1: Wait with a length of 15 clock cycles are inserted. 1 0 0 0 0: Wait with a length of 16 clock cycles are inserted. 1 0 0 0 1: Wait with a length of 17 clock cycles are inserted. 1 0 0 1 0: Wait with a length of 18 clock cycles are inserted. 1 0 0 1 1: Wait with a length of 19 clock cycles are inserted. 1 0 1 0 0: Wait with a length of 20 clock cycles are inserted. 1 0 1 0 1: Wait with a length of 21 clock cycles are inserted. 1 0 1 1 0: Wait with a length of 22 clock cycles are inserted. 1 0 1 1 1: Wait with a length of 23 clock cycles are inserted. 1 1 0 0 0: Wait with a length of 24 clock cycles are inserted. 1 1 0 0 1: Wait with a length of 25 clock cycles are inserted. 1 1 0 1 0: Wait with a length of 26 clock cycles are inserted. 1 1 0 1 1: Wait with a length of 27 clock cycles are inserted. 1 1 1 0 0: Wait with a length of 28 clock cycles are inserted. 1 1 1 0 1: Wait with a length of 29 clock cycles are inserted. 1 1 1 1 0: Wait with a length of 30 clock cycles are inserted. 1 1 1 1 1: Wait with a length of 31 clock cycles are inserted.	R/W
b23 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28 to b24	CSRWAIT[4:0]	Normal Read Cycle Wait Select	b28 b24 0 0 0 0 0: No wait is inserted. 0 0 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 0 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 0 0 1 1: Wait with a length of 3 clock cycles are inserted. 0 0 1 0 0: Wait with a length of 4 clock cycles are inserted. 0 0 1 0 1: Wait with a length of 5 clock cycles are inserted. 0 0 1 1 0: Wait with a length of 6 clock cycles are inserted. 0 0 1 1 1: Wait with a length of 7 clock cycles are inserted. 0 1 0 0 0: Wait with a length of 8 clock cycles are inserted. 0 1 0 0 1: Wait with a length of 9 clock cycles are inserted. 0 1 0 1 0: Wait with a length of 10 clock cycles are inserted. 0 1 0 1 1: Wait with a length of 11 clock cycles are inserted. 0 1 1 0 0: Wait with a length of 12 clock cycles are inserted. 0 1 1 0 1: Wait with a length of 13 clock cycles are inserted. 0 1 1 1 0: Wait with a length of 14 clock cycles are inserted. 0 1 1 1 1: Wait with a length of 15 clock cycles are inserted. 1 0 0 0 0: Wait with a length of 16 clock cycles are inserted. 1 0 0 0 1: Wait with a length of 17 clock cycles are inserted. 1 0 0 1 0: Wait with a length of 18 clock cycles are inserted. 1 0 0 1 1: Wait with a length of 19 clock cycles are inserted. 1 0 1 0 0: Wait with a length of 20 clock cycles are inserted. 1 0 1 0 1: Wait with a length of 21 clock cycles are inserted. 1 0 1 1 0: Wait with a length of 22 clock cycles are inserted. 1 0 1 1 1: Wait with a length of 23 clock cycles are inserted. 1 1 0 0 0: Wait with a length of 24 clock cycles are inserted. 1 1 0 0 1: Wait with a length of 25 clock cycles are inserted. 1 1 0 1 0: Wait with a length of 26 clock cycles are inserted. 1 1 0 1 1: Wait with a length of 27 clock cycles are inserted. 1 1 1 0 0: Wait with a length of 28 clock cycles are inserted. 1 1 1 0 1: Wait with a length of 29 clock cycles are inserted. 1 1 1 1 0: Wait with a length of 30 clock cycles are inserted. 1 1 1 1 1: Wait with a length of 31 clock cycles are inserted.	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The CSPWWAIT[2:0] value is valid only when the PWENB bit in CSnMOD is set to 1.
Note 2. The CSPRWAIT[2:0] value is valid only when the PRENB bit in CSnMOD is set to 1.

Do not write to the CSnWCR1 register while access to the CSn area is in progress.
Set each of these bits within a range of the restrictions described in section 16.5.7 (1) Limitations on Using Separate Bus Interface or section 16.5.7 (2) Limitations on Using Address/Data Multiplexed Bus Interface, according to the bus interface used.

CSPWWAIT[2:0] Bits (Page Write Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the second and subsequent accesses during a page write cycle.
This setting is enabled when the PWENB bit in CSnMOD is set to 1.

Note: • Be sure to satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

CSPRWAIT[2:0] Bits (Page Read Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the second and subsequent accesses during a page read cycle.
This setting is enabled when the PRENB bit in CSnMOD is set to 1.

Note: • Be sure to satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSPRWAIT[2:0] value.

CSWWAIT[4:0] Bits (Normal Write Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the first access during a normal write cycle or page write cycle.

Note: • Be sure to satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSRWAIT[4:0] Bits (Normal Read Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the first access during a normal read cycle or page read cycle.

Note: • Be sure to satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

16.3.6 CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 3)

Address(es): CS0WCR2 0008 3008h, CS1WCR2 0008 3018h, CS2WCR2 0008 3028h, CS3WCR2 0008 3038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	CSON[2:0]			—	WDON[2:0]			—	WRON[2:0]			—	RDON[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AWAIT[1:0]		—	WDOFF[2:0]			—	CSWOFF[2:0]			—	CSROFF[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	CSROFF[2:0]	Read-Access CS Extension Cycle Select	b2 b0 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	CSWOFF[2:0]	Write-Access CS Extension Cycle Select	b6 b4 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10 to b8	WDOFF[2:0]	Write Data Output Extension Cycle Select	b10 b8 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	AWAIT[1:0]	Address Cycle Wait Select	b13 b12 0 0: No wait is inserted. 0 1: Wait with a length of 1 clock cycle is inserted. 1 0: Wait with a length of 2 clock cycles are inserted. 1 1: Wait with a length of 3 clock cycles are inserted.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	RDON[2:0]	RD Assert Wait Select	b18 b16 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b19	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b22 to b20	WRON[2:0]	WR Assert Wait Select	b22 b20 0 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b26 to b24	WDON[2:0]	Write Data Output Wait Select	b26 b24 0 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b30 to b28	CSON[2:0]	CS Assert Wait Select	b30 b28 0 0 0: No wait is inserted. 0 0 1: Wait with a length of 1 clock cycle is inserted. 0 1 0: Wait with a length of 2 clock cycles are inserted. 0 1 1: Wait with a length of 3 clock cycles are inserted. 1 0 0: Wait with a length of 4 clock cycles are inserted. 1 0 1: Wait with a length of 5 clock cycles are inserted. 1 1 0: Wait with a length of 6 clock cycles are inserted. 1 1 1: Wait with a length of 7 clock cycles are inserted.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Do not write to the CSnWCR2 register while access to the CSn area is in progress.
Set each of these bits within a range of the restrictions described in section 16.5.7 (1) Limitations on Using Separate Bus Interface or section 16.5.7 (2) Limitations on Using Address/Data Multiplexed Bus Interface, according to the bus interface used.

CSROFF[2:0] Bits (Read-Access CS Extension Cycle Select)

These bits specify the number of wait cycles to be inserted in a time period from the end of a wait cycle (RD# signal negated) until the CSn# signal (n = 0 to 3) is negated in read access mode.

CSWOFF[2:0] Bits (Write-Access CS Extension Cycle Select)

These bits specify the number of wait cycles to be inserted in a time period from the end of a wait cycle (WRn# signal (n = 0 or 1) negated) until the CSn# signal (n = 0 to 3) is negated in write access mode.

Note: • Be sure to satisfy WDOFF[2:0] value ≤ CSWOFF[2:0] value.

WDOFF[2:0] Bits (Write Data Output Extension Cycle Select)

These bits specify the number of wait cycles to be inserted in a time period from the end of a wait cycle (WRn# signal (n = 0 or 1) negated) until the write data output is completed in write access mode.

Note: • Be sure to satisfy WDOFF[2:0] value ≤ CSWOFF[2:0] value.

AWAIT[1:0] Bits (Address Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into an address output cycle with the address/data multiplexed I/O interface.

Note: • CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value
For read access, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1CSRWAIT[4:0] value.
For write access, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WRON[2:0] value ≤

CSnWCR1.CSWWAIT[4:0] value and CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

RDON[2:0] Bits (RD Assert Wait Select)

These bits specify the number of wait cycles to be inserted before the RD# signal is asserted.

Note: • For normal read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.
For page read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤CSnWCR1.CSPRWAIT[4:0]value.

Note: • When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

WRON[2:0] Bits (WR Assert Wait Select)

These bits specify the number of wait cycles to be inserted before the WRn# signal (n = 0 or 1) is asserted.

Note: • For normal write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.
For page write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

Note: • When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

WDON[2:0] Bits (Write Data Output Wait Select)

These bits specify the number of wait cycles to be inserted before the write data is output.

Note: • For normal write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.
For page write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

Note: • When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSON[2:0] Bits (CS Assert Wait Select)

These bits specify the number of wait cycles to be inserted before the CSn# signal (n = 0 to 3) is asserted.

Note: • For normal read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.
For page read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤CSnWCR1.CSPRWAIT[4:0]value.
For normal write access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.
For page write access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

Note: • When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value.

16.3.7 Bus Error Status Clear Register (BERCLR)

Address(es): 0008 1300h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	STSCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STSCLR	Status Clear	0: Invalid 1: Bus error status register cleared	(W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only writing 1 is effective; i.e. writing 0 has no effect.

STSCLR Bit (Status Clear)

Writing 1 to this bit clears the bus error status registers 1 and 2 (BERSR1 and BERSR2).
Writing 0 has no effect. It is read as 0.

16.3.8 Bus Error Monitoring Enable Register (BEREN)

Address(es): 0008 1304h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TOEN	IGAEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IGAEN	Illegal Address Access Detection Enable	0: Illegal address access detection is disabled. 1: Illegal address access detection is enabled.	R/W
b1	TOEN	Timeout Detection Enable*1,*2	0: Bus timeout detection is disabled. 1: Bus timeout detection is enabled.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When detection is disabled (the TOEN bit is cleared to 0), bus access can cause the bus to freeze.
Note 2. Do not clear the TOEN bit to 0 (bus timeout detection disabled) while timeout errors are being detected.

16.3.9 Bus Error Status Register 1 (BERSR1)

Address(es): 0008 1308h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MST[2:0]			—	—	TO	IA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IA	Illegal Address Access	0: Illegal address access not made 1: Illegal address access made	R
b1	TO	Timeout	0: Timeout not generated 1: Timeout generated	R
b3, b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b6 to b4	MST[2:0]	Bus Master Code	b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

MST[2:0] Bits (Bus Master Code)

These bits indicate the bus master that accessed a bus when a bus error occurred.

16.3.10 Bus Error Status Register 2 (BERSR2)

Address(es): 0008 130Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADDR[12:0]													—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15 to b3	ADDR[12:0]	Bus Error Occurrence Address	The upper 13 bits of an address that was accessed when a bus error occurred (in units of 512 Kbytes).	R

16.3.11 Bus Priority Control Register (BUSPRI)

Address(es): 0008 1310h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BPEB[1:0]		BPFB[1:0]		BPHB[1:0]		BPGB[1:0]		BPIB[1:0]		BPRO[1:0]		BPRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BPRA[1:0]	Memory Bus 1 (On-Chip RAM) Priority Control	b1 b0 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b3, b2	BPRO[1:0]	Memory Bus 2 (On-Chip ROM) Priority Control	b3 b2 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b5, b4	BPIB[1:0]	Internal Peripheral Bus 1 Priority Control	b5 b4 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b7, b6	BPGB[1:0]	Internal Peripheral Bus 2 and 3 Priority Control	b7 b6 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b9, b8	BPHB[1:0]	Internal Peripheral Bus 4 and 5 Priority Control	b9 b8 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b11, b10	BPFB[1:0]	Internal Peripheral Bus 6 Priority Control	b11 b10 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b13, b12	BPEB[1:0]	External Bus Priority Control	b13 b12 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits can be written to only once while the DTC and DMAC are written to more than one time, the operation is not guaranteed.

BPRA[1:0] Bits (Memory Bus 1 (On-Chip RAM) Priority Control)

These bits specify the priority order for memory bus 1 (on-chip RAM).

When the priority order is fixed, internal main bus 2 has priority over the CPU bus.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPRO[1:0] Bits (Memory Bus 2 (On-Chip ROM) Priority Control)

These bits specify the priority order for memory bus 2 (on-chip ROM).

When the priority order is fixed, internal main bus 2 has priority over the CPU bus.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPIB[1:0] Bits (Internal Peripheral Bus 1 Priority Control)

These bits specify the priority order for internal peripheral bus 1.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPGB[1:0] Bits (Internal Peripheral Bus 2 and 3 Priority Control)

These bits specify the priority order for internal peripheral buses 2 and 3.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPHB[1:0] Bits (Internal Peripheral Bus 4 and 5 Priority Control)

These bits specify the priority order for internal peripheral buses 4 and 5.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPFB[1:0] Bits (Internal Peripheral Bus 6 Priority Control)

These bits specify the priority order for internal peripheral bus 6.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPEB[1:0] Bits (External Bus Priority Control)

These bits specify the priority order for the external bus.
When the priority order is fixed, the order is internal main bus 2, and then internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted, between internal main bus 1 and internal main bus 2.

16.4 Endian and Data Alignment

The external bus has a data-alignment function to control which byte of the data bus (D15 to D8, or D7 to D0) is used according to the bus specifications of the area to be accessed (8-bit, or 16-bit bus space), data size, and endian format when accessing the external address space (the CS).

16.4.1 Data Alignment Control for CS Area

(1) 16-Bit Bus Space

When a 16-bit width is selected for a bus space by the BSIZE[1:0] bits in CSnCR, the address buses A23 to A1 are enabled to output address signals in units of 16 bits, and the address bus A0 is disabled (always output the low level). When byte strobe mode is selected (the WRMOD bit = 0 in CSnMOD), the WR0# and WR1# pins are enabled. and BC1# pins are not used.

When single write strobe mode is selected (the WRMOD bit = 1 in CSnMOD), only the WR0# pin is enabled and always outputs the low level during write access, regardless of the data size. Here, the WR1# pin is invalid (always output the high level). The valid byte position is indicated by the BC0# and BC1# pins.

Data Size	Access Address	Number of Access	Bus Cycle	Unit of Data	Address		WR1#/BC1# (D15–D8)	WR0#/BC0# (D7–D0)
							RD#	
							Data Bus	
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n		7 0	
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+2		7 0	
16 bits	4n	One	First	16 bits	4n		15 8	7 0
	4n+1	Two	First	8 bits	4n		7 0	
			Second	8 bits	4n+2			15 8
	4n+2	One	First	16 bits	4n+2		15 8	7 0
	4n+3	Two	First	8 bits	4n+2		7 0	
			Second	8 bits	4n+4			15 8
32 bits	4n	Two	First	16 bits	4n		15 8	7 0
			Second	16 bits	4n+2	(p)	31 24	23 16
	4n+1	Three	First	8 bits	4n		7 0	
			Second	16 bits	4n+2		23 16	15 8
			Third	8 bits	4n+4			31 24
	4n+2	Two	First	16 bits	4n+2		15 8	7 0
			Second	16 bits	4n+4		31 24	23 16
	4n+3	Three	First	8 bits	4n+2		7 0	
			Second	16 bits	4n+4		23 16	15 8
			Third	8 bits	4n+6			31 24

(p): Page access (only when page access is enabled with the PRENB and PWENB bits in CSnMOD)

Figure 16.6 Data Alignment (Little Endian) in 16-Bit Bus Space

Data Size	Access Address	Number of Access	Bus Cycle	Unit of Data	Address	WR1#/BC1# / WR0#/BC0# / RD# Data Bus D15 D8 D7 D0
8 bits	4n	One	First	8 bits	4n	7 0
	4n+1	One	First	8 bits	4n	7 0
	4n+2	One	First	8 bits	4n+2	7 0
	4n+3	One	First	8 bits	4n+2	7 0
16 bits	4n	One	First	16 bits	4n	15 8 7 0
	4n+1	Two	First	8 bits	4n	15 8
			Second	8 bits	4n+2	7 0
	4n+2	One	First	16 bits	4n+2	15 8 7 0
	4n+3	Two	First	8 bits	4n+2	15 8
			Second	8 bits	4n+4	7 0
32 bits	4n	Two	First	16 bits	4n	31 24 23 16
			Second	16 bits	4n+2 (p)	15 8 7 0
	4n+1	Three	First	8 bits	4n	31 24
			Second	16 bits	4n+2	23 16 15 8
			Third	8 bits	4n+4	7 0
	4n+2	Two	First	16 bits	4n+2	31 24 23 16
			Second	16 bits	4n+4	15 8 7 0
	4n+3	Three	First	8 bits	4n+2	31 24
			Second	16 bits	4n+4	23 16 15 8
			Third	8 bits	4n+6	7 0

(p): Page access (only when page access is enabled with the PRENB and PWENB bits in CSnMOD)

Figure 16.7 Data Alignment (Big Endian) in 16-Bit Bus Space

(2) 8-Bit Bus Space

When an 8-bit bus space is selected by the BSIZE[1:0] bits in CSnCR, the address buses A19 to A0 are enabled to output address signals in byte units.

In 8-bit bus space, only the WR0# pin is valid regardless of write access mode, and always outputs the low level during write access. The WR1#, BC0#,and BC1# pins are not used.

Page access can occur in access to data in 16- or 32-bit units. Specifically, page access can occur when an access does not spread over a 32-bit boundary. The situations in which page access occurs are indicated by the letter (p) in Figure 16.8 and Figure 16.9.

In 8-bit bus space, the valid positions of data external to the chip are D7 to D0 and WR0# is used as the control signal, regardless of the endian mode.

Data Size	Access Address	Number of Access	Bus Cycle	Unit of Data	Address		WR1#/BC1# WR0#/BC0# RD# Data Bus D15 D8 D7 D0
8 bits	4n	One	First	8 bits	4n		7 0
	4n+1	One	First	8 bits	4n+1		7 0
	4n+2	One	First	8 bits	4n+2		7 0
	4n+3	One	First	8 bits	4n+3		7 0
16 bits	4n	Two	First	8 bits	4n		7 0
			Second	8 bits	4n+1	(p)	15 8
	4n+1	Two	First	8 bits	4n+1		7 0
			Second	8 bits	4n+2	(p)	15 8
	4n+2	Two	First	8 bits	4n+2		7 0
			Second	8 bits	4n+3	(p)	15 8
	4n+3	Two	First	8 bits	4n+3		7 0
			Second	8 bits	4n+4		15 8
32 bits	4n	Four	First	8 bits	4n		7 0
			Second	8 bits	4n+1	(p)	15 8
			Third	8 bits	4n+2	(p)	23 16
			Fourth	8 bits	4n+3	(p)	31 24
	4n+1	Four	First	8 bits	4n+1		7 0
			Second	8 bits	4n+2	(p)	15 8
			Third	8 bits	4n+3	(p)	23 16
			Fourth	8 bits	4n+4		31 24
	4n+2	Four	First	8 bits	4n+2		7 0
			Second	8 bits	4n+3	(p)	15 8
			Third	8 bits	4n+4		23 16
			Fourth	8 bits	4n+5	(p)	31 24
	4n+3	Four	First	8 bits	4n+3		7 0
			Second	8 bits	4n+4		15 8
			Third	8 bits	4n+5	(p)	23 16
			Fourth	8 bits	4n+6	(p)	31 24

(p): Page access (only when page access is enabled with the PRENB and PWENB bits in CSnMOD)

Figure 16.8 Data Alignment (Little Endian) in 8-Bit Bus Space

Data Size	Access Address	Number of Access	Bus Cycle	Unit of Data	Address		WR1#/BC1# RD# Data Bus D15 D8	WR0#/BC0# Data Bus D7 D0
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			15 8
			Second	8 bits	4n+1	(p)		7 0
	4n+1	Two	First	8 bits	4n+1			15 8
			Second	8 bits	4n+2	(p)		7 0
	4n+2	Two	First	8 bits	4n+2			15 8
			Second	8 bits	4n+3	(p)		7 0
	4n+3	Two	First	8 bits	4n+3			15 8
			Second	8 bits	4n+4			7 0
32 bits	4n	Four	First	8 bits	4n			31 24
			Second	8 bits	4n+1	(p)		23 16
			Third	8 bits	4n+2	(p)		15 8
			Fourth	8 bits	4n+3	(p)		7 0
	4n+1	Four	First	8 bits	4n+1			31 24
			Second	8 bits	4n+2	(p)		23 16
			Third	8 bits	4n+3	(p)		15 8
			Fourth	8 bits	4n+4			7 0
	4n+2	Four	First	8 bits	4n+2			31 24
			Second	8 bits	4n+3	(p)		23 16
			Third	8 bits	4n+4			15 8
			Fourth	8 bits	4n+5	(p)		7 0
	4n+3	Four	First	8 bits	4n+3			31 24
			Second	8 bits	4n+4			23 16
			Third	8 bits	4n+5	(p)		15 8
			Fourth	8 bits	4n+6	(p)		7 0

(p): Page access (only when page access is enabled with the PRENB and PWENB bits in CSnMOD)

Figure 16.9 Data Alignment (Big Endian) in 8-Bit Bus Space

16.5 Operation of CS Area Controller

16.5.1 Separate Bus

The various periods in the timing charts are described below.
The CS area controller (CSC) operates in synchronization with the external bus clock (BCLK). The operation cycles, such as wait cycles specified with the CSC register, are counted on BCLK. In the following description, frequencies of BCLK and BCLK pin output are the same, unless otherwise noted.
Access via the external bus starts at the same point as the output of a rising edge on the BCLK pin. However, if the external bus clock (BCLK) and the output on the BCLK pin are at different frequencies so that a single request from a bus master for transfer leads to two or more rounds of access via the external bus, the wait settings may cause the start of access for the second and subsequent rounds to coincide with the falling edge of the output on the BCLK pin (see Figure 16.15 to Figure 16.19). If recovery cycles are inserted for bus access, the setting for the number of recovery cycles may also cause the start of access for the second and subsequent rounds to coincide with the falling edge of the output on the BCLK pin (see Figure 16.37 and Figure 16.39).

(a) Tw1 to Twn (Clock Cycles of Waiting for a Normal Read Cycle or Normal Write Cycle)

The period Tw1 to Twn is made up of the number of clock cycles between the start of access via the external bus clock and one cycle before the strobe signal is valid. The number of cycles are selectable within the range from zero to 31. Within this period, the timing of CSn#, RD#, and WRn# assertion (placing the signals at the low level) is determined by the respective wait settings. Specifically, the periods of waiting are controlled by the CS assert wait select bits (CSON), the RD assert wait select bits (RDON), the WR assert wait select bits (WRON), and the write data output wait select bits (WDON) in CSn wait control register 2 (CSnWCR2). The number of clock cycles for each of these periods of waiting is selectable as a value from zero to seven counted from the start of external bus access. Selectable numbers of cycles are also within the overall number of clock cycles of waiting for reading or writing.

(b) Tend (Clock Cycle where the Strobe Signal is Valid)

Tend is the next clock cycle after completion of the period of waiting for a normal cycle of reading or writing or for a cycle of page reading or page writing. If each wait select bit for a normal cycle of reading or writing or for a cycle of page reading or page writing is zero, the clock cycle where bus access starts is the clock cycle where the strobe signal is valid. The RD# and WRn# signals are negated in the next clock cycle after the cycle where the strobe signal is valid. In the case of read access, the clock cycle where the strobe signal is valid becomes the clock cycle where the data to be read are sampled.
If an external wait is enabled, the wait signal is sampled at the time of the cycle where the strobe signal is valid. The bus cycle is extended if the wait signal is at the low level. The bus cycle is completed in the next clock cycle if the wait signal is at the high level. Tend indicates the cycle where sampling of the wait signal starts.
After the first cycle where the strobe signal is valid during page access, second and subsequent page access operations (point (e) below) start in the next cycle except in cases of write access where a setting (other than zero) for write-data output extension clock cycles (point (d) below) has been made. If the setting for the RD or WR assertion wait is a value other than zero, the RD# and WRn# signals are negated in the next clock cycle. If the setting is zero, assertion continues. Furthermore, the CSn# signal continues to be asserted rather than being negated.

(c) Tn1 to Tnm (Clock Cycles of CS Extension)

In the case of normal access, Tn1 to Tnm represent the clock cycles of the period following the cycle where the strobe signal is valid (Tend) up to negation of the CSn# signal. For read or write access, the timing of negation can be controlled by the read-access CS extension cycle select bits (CSROFF) and the write-access CS extension cycle select bits (CSWOFF) in the CSn wait control register 2 (CSnWCR2), respectively.
The number of cycles are counted from the cycle following the cycle where the strobe signal is valid.
In the case of page access, Tn1 to Tnm represent the clock cycles of the period for the cycle following the last cycle where the strobe signal is valid up to negation of the CSn# signal.

For write access, setting the write data output extension cycle select bits (WDOFF) controls extension of the period where the address and output data are valid.

(d) Tdw1 to Tdwn (Write-Data Output Extension Clock Cycles)

For write access, if the setting for write-data output extension wait is a value other than zero, clock cycles of write-data output extension are inserted from the cycle that follows the cycle where the strobe signal is valid (Tend).
In the case of normal access, this is inserted within the period of clock cycles of CS extension (point (c) above).
In the case of page access, this is inserted within the period of the cycle where the strobe signal is valid and subsequent page access or within the period of clock cycles of CS extension (point (c) above). Valid address and data output are extended over this period, and the WRn# signal is negated.

(e) Tpw1 to Tpwn (Page-Read Cycle Wait or Page-Write Cycle Wait)

For the second and subsequent bus cycles during page access, the values for a page-read cycle wait or page-write cycle wait are used instead of the settings for a normal read or write cycle wait. Setting the WR assert wait select bits becomes enabled in the same way as for the first round of access. How the setting for RD assertion controls operation depends on the setting for page-read access mode (the PRMOD bit in CSnMOD) as described below.

CSnMOD.PRMOD = 0: A wait until RD assertion is inserted in the same way as for the first round of access, and the RD# signal is negated.
CSnMOD.PRMOD = 1: Although a wait until RD assertion is inserted in the same way as for normal-access compatibility mode, the RD# signal continues to be asserted over this period.

(f) Tr1 to Trn (Recovery Cycles)

Recovery cycles can be inserted from the point where a bus cycle is completed (CSn# signal negation). The number of recovery cycles can be controlled by the setting of the read recovery (RRCV) or write recovery (WRCV) bits in the CSn recovery cycle register (CSnREC). Both numbers of recovery cycles are counted from the end of a bus cycle (CSn# negation) and can be selected from 0 to 15 cycles. For details on recovery cycles, see section 16.5.4, Insertion of Recovery Cycles.

(1) Normal Access

When the PRENB and PWENB bits in CSnMOD are set to 0 to disable page-read and page-write access, respectively, all bus accesses will take the form of normal read and write operations.
Even when the PRENB and PWENB bits in CSnMOD are set to 1 to enable page-read and page-write access, respectively, bus access other than page access will take the form of normal read and write operations.
Figure 16.10 to Figure 16.12 show the normal access operations.

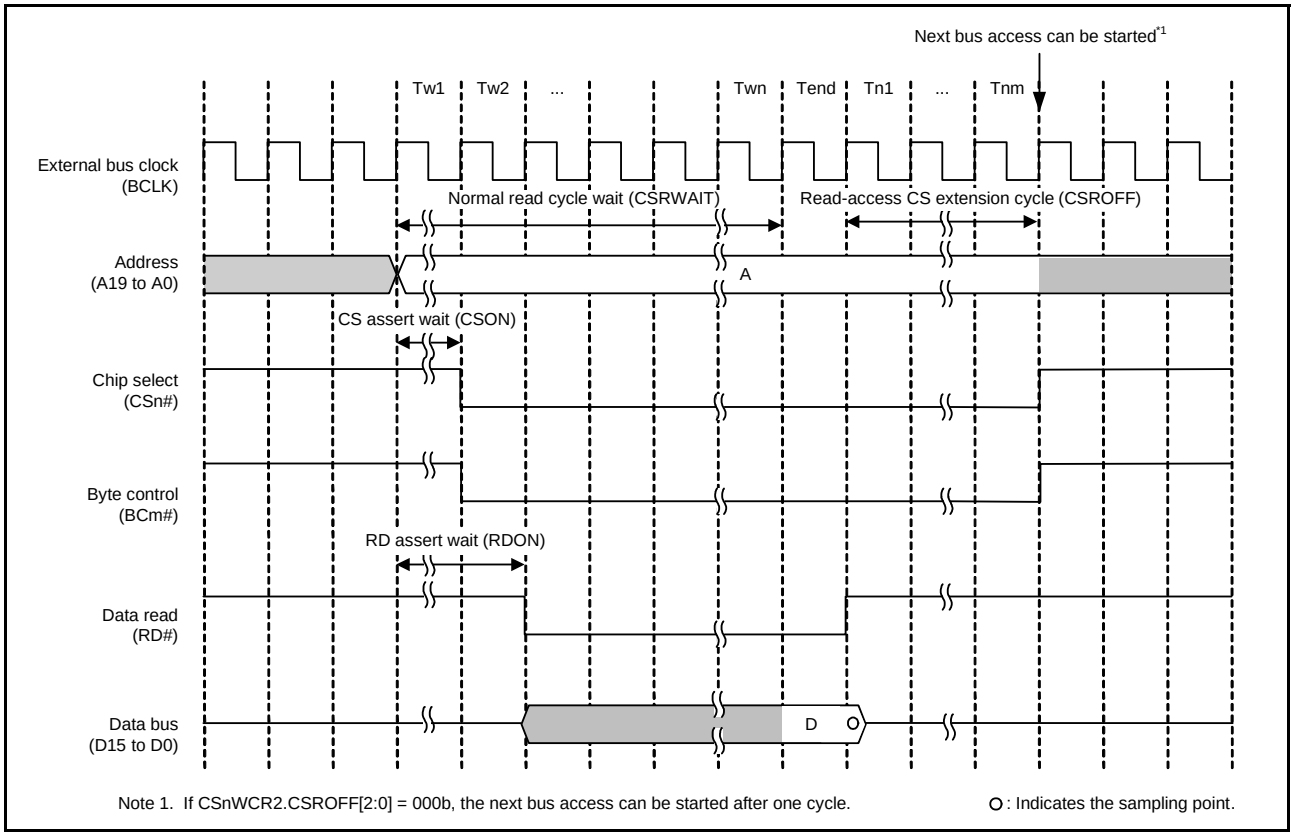


Figure 16.10 Bus Timing (Normal-Read Operation) (n = 0 to 3, m = 0, 1)

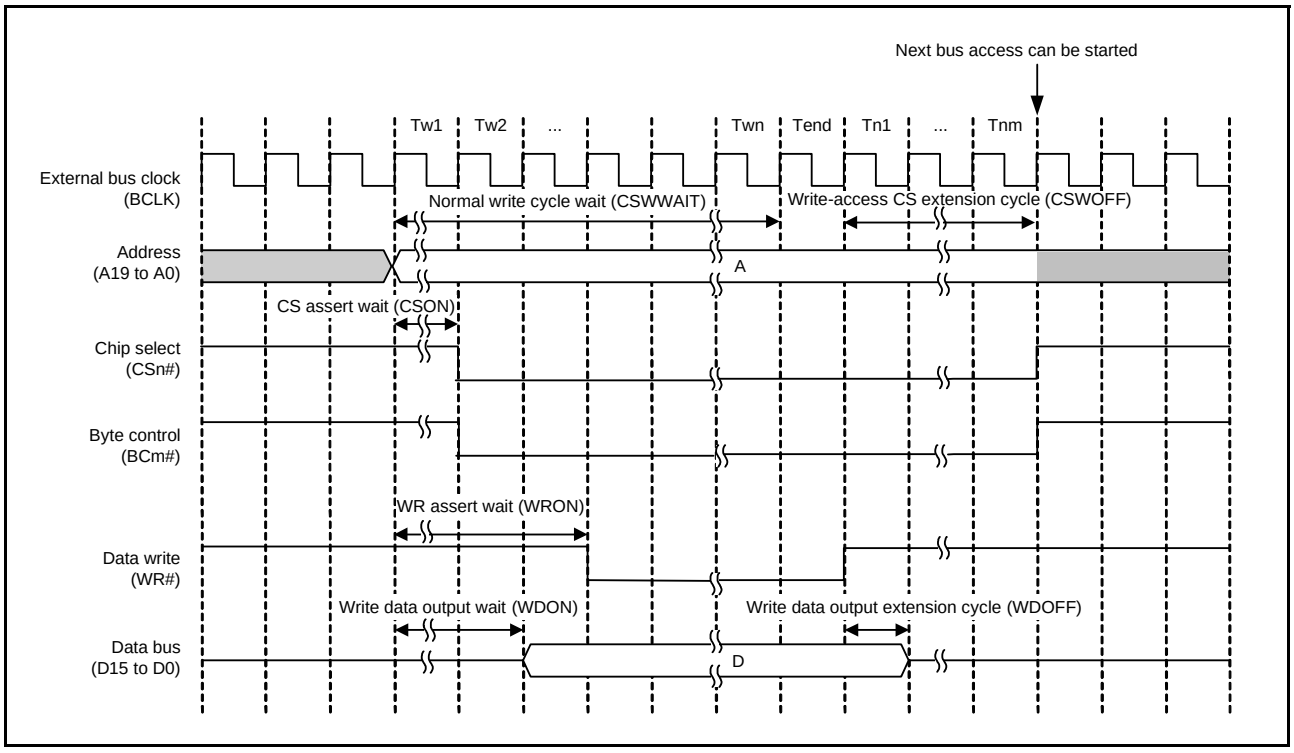


Figure 16.11 Bus Timing (Normal-Write Operation, Single Write Strobe Mode) (n = 0 to 3, m = 0, 1)

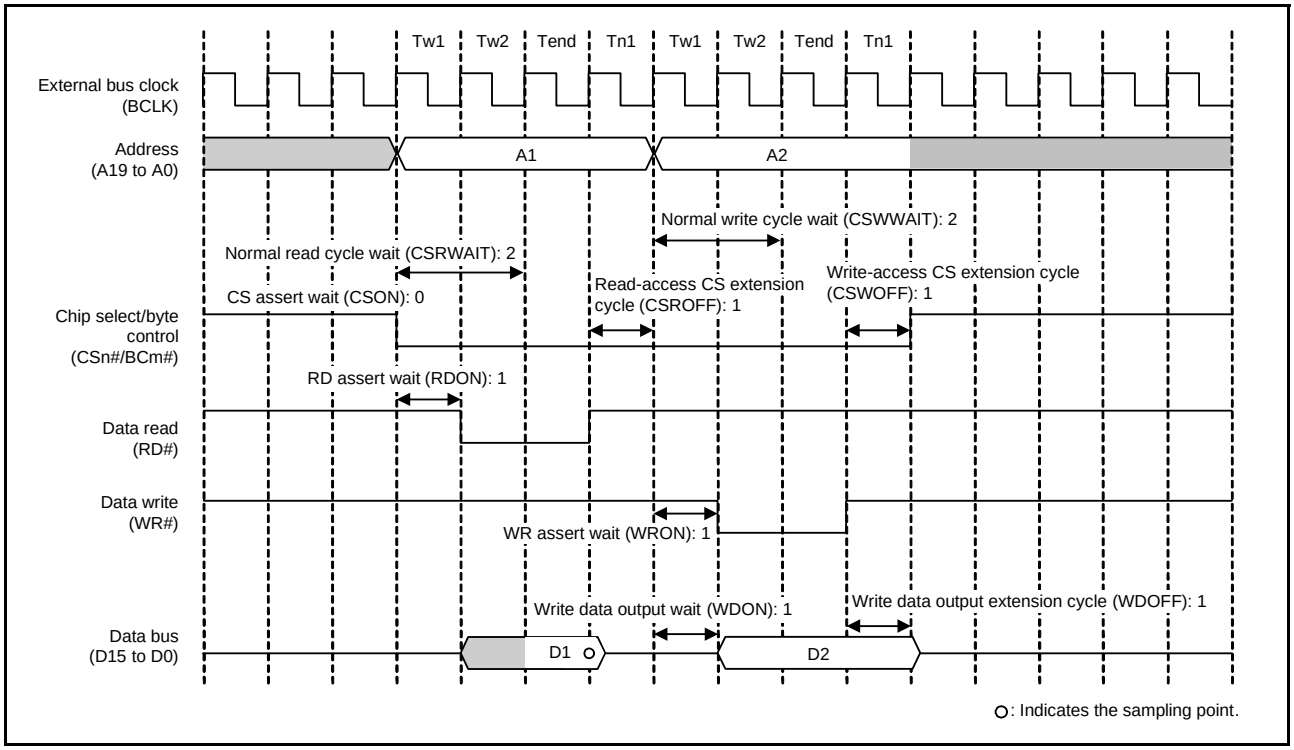


Figure 16.12 Example of Normal Access Operation (Read/Write) (n = 0 to 3, m = 0, 1)

When two or more rounds of external bus access are required in response to a single request for transfer from a bus master, normal access operations (steps (a) to (d) above) are repeated. Figure 16.13 and Figure 16.14 show examples of operations when two rounds of bus access are generated in response to a single request for transfer. If the recovery cycle insertion condition is satisfied, recovery cycles (step (f) above) are also inserted in the second and subsequent external bus accesses (see Figure 16.35).

The values of the wait control registers are example settings. In practice, set the register bits according to the specifications of connected devices.

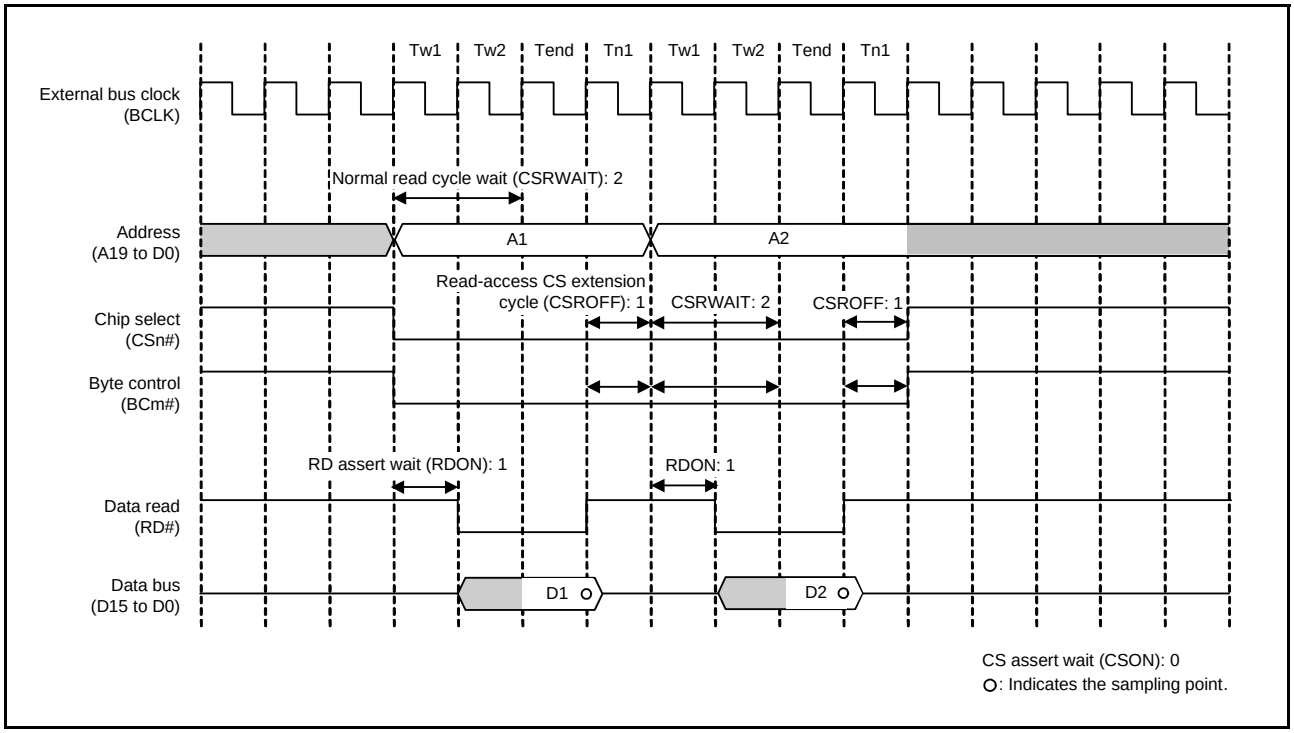


Figure 16.13 Example of Normal-Read Operation (when Two Rounds of Bus Access are Generated in Response to a Single Request for Transfer) (n = 0 to 3, m = 0, 1)

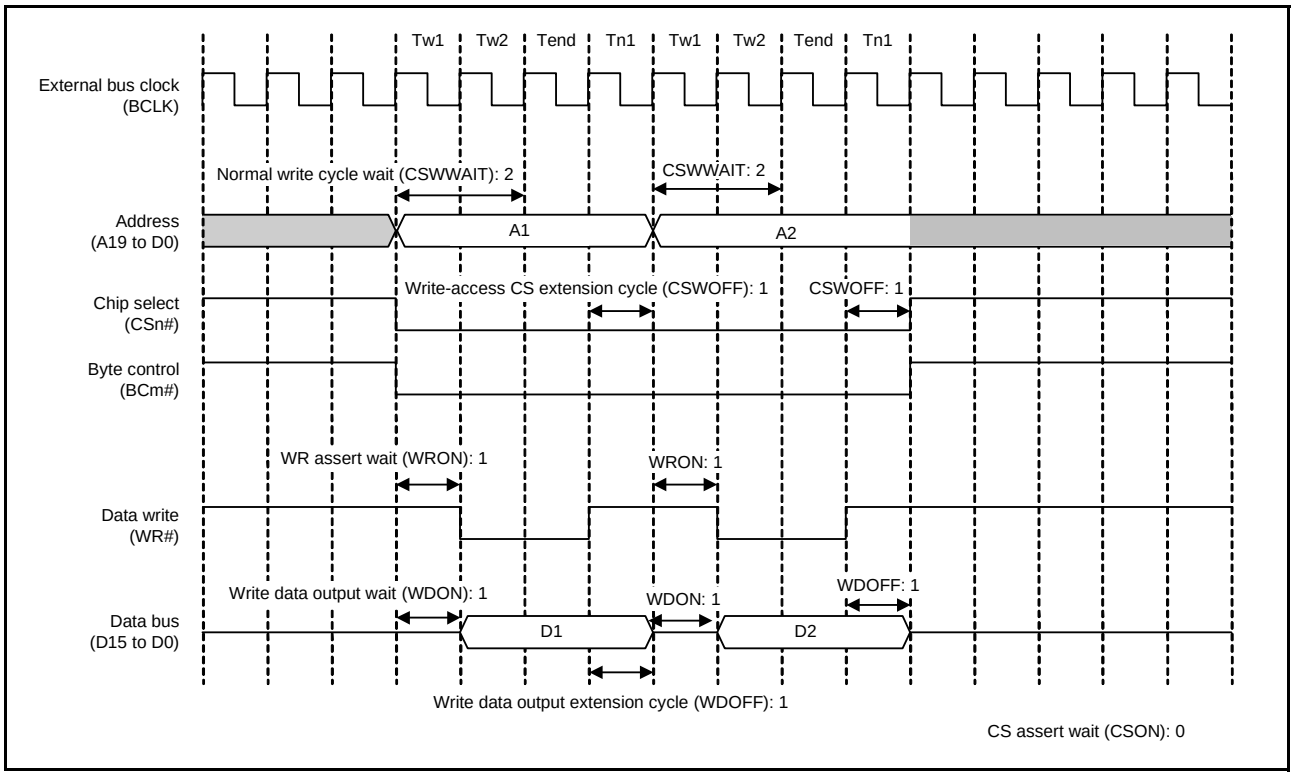


Figure 16.14 Example of Normal-Write Operation (when Two Rounds of Bus Access are Generated in Response to a Single Request for Transfer, in Single Write Strobe Mode) (n = 0 to 3, m = 0, 1)

Figure 16.15 to Figure 16.19 show examples of normal accesses made with the 1/2 BCLK selected with the BCLK pin output select bit.

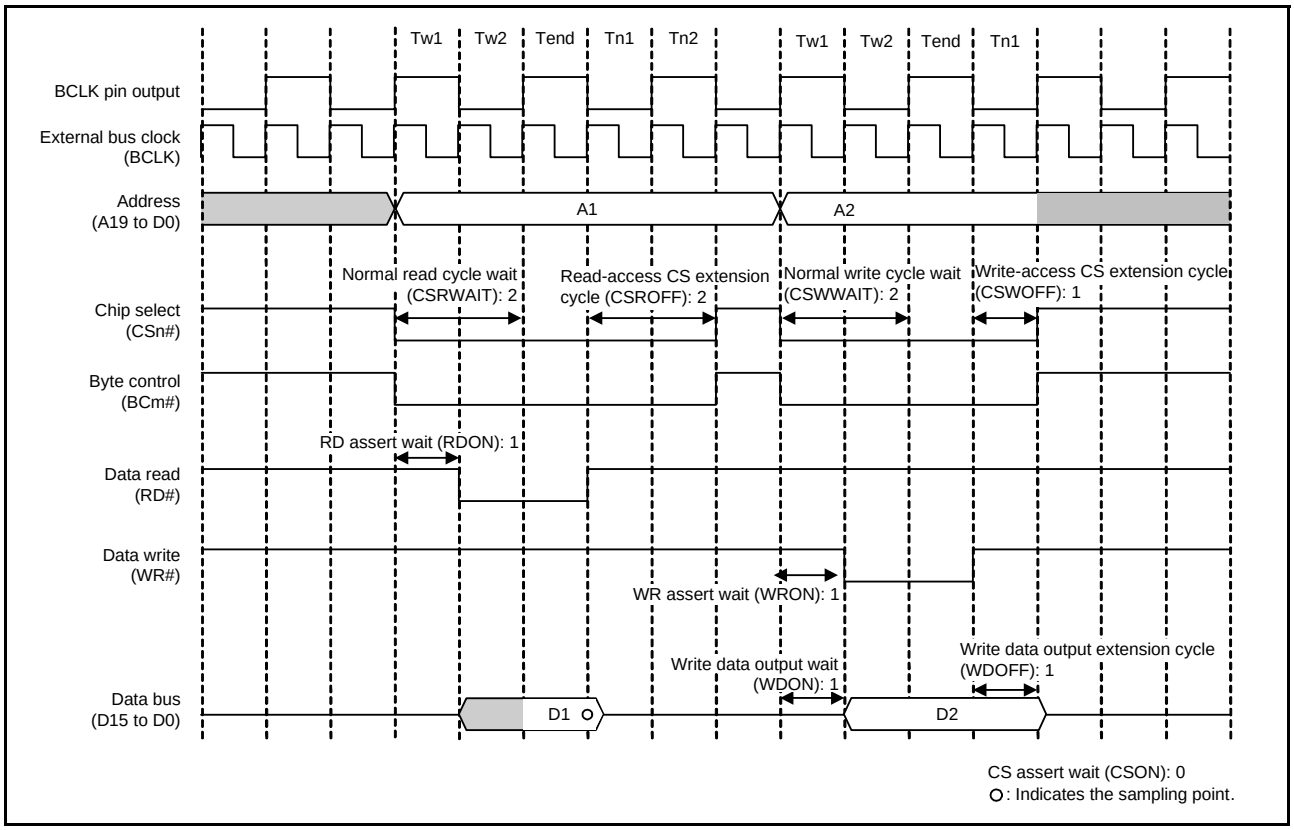


Figure 16.15 Example of Normal Access (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit) (n = 0 to 3, m = 0, 1)

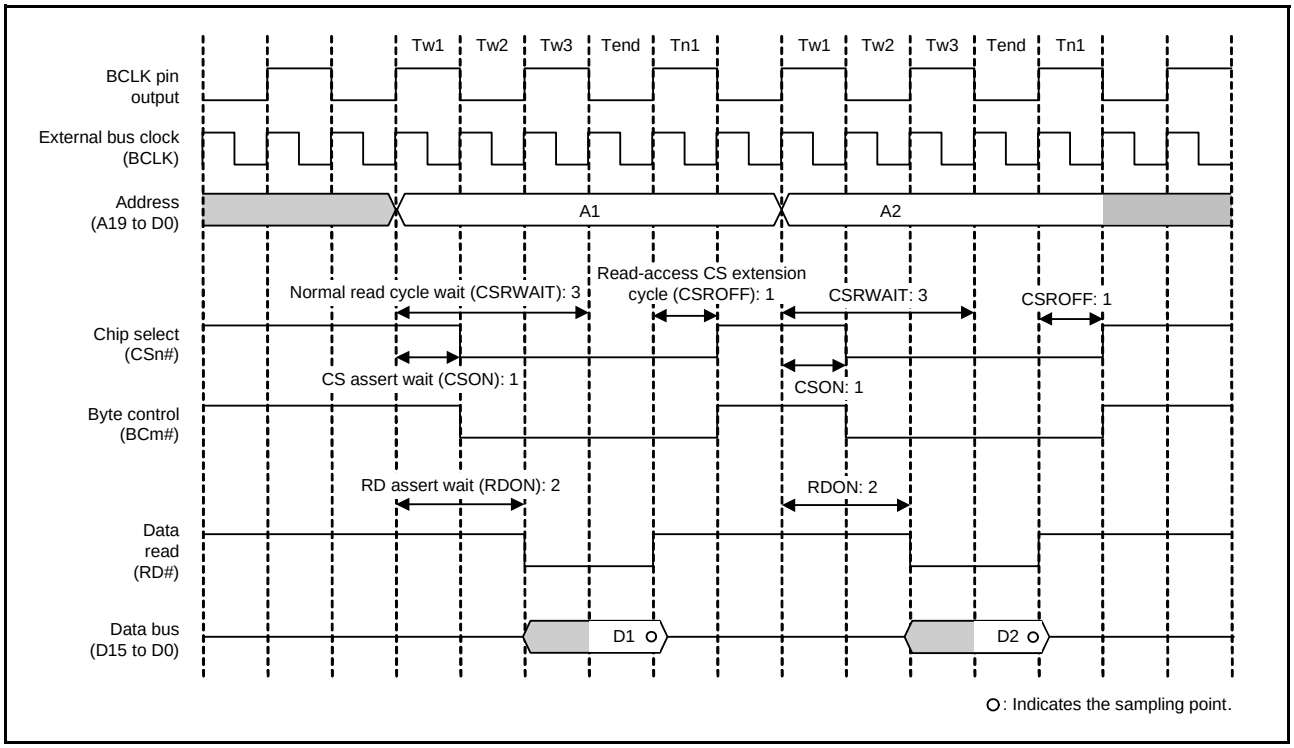


Figure 16.16 Example of Normal-Read Operation (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit) (n = 0 to 3, m = 0, 1)

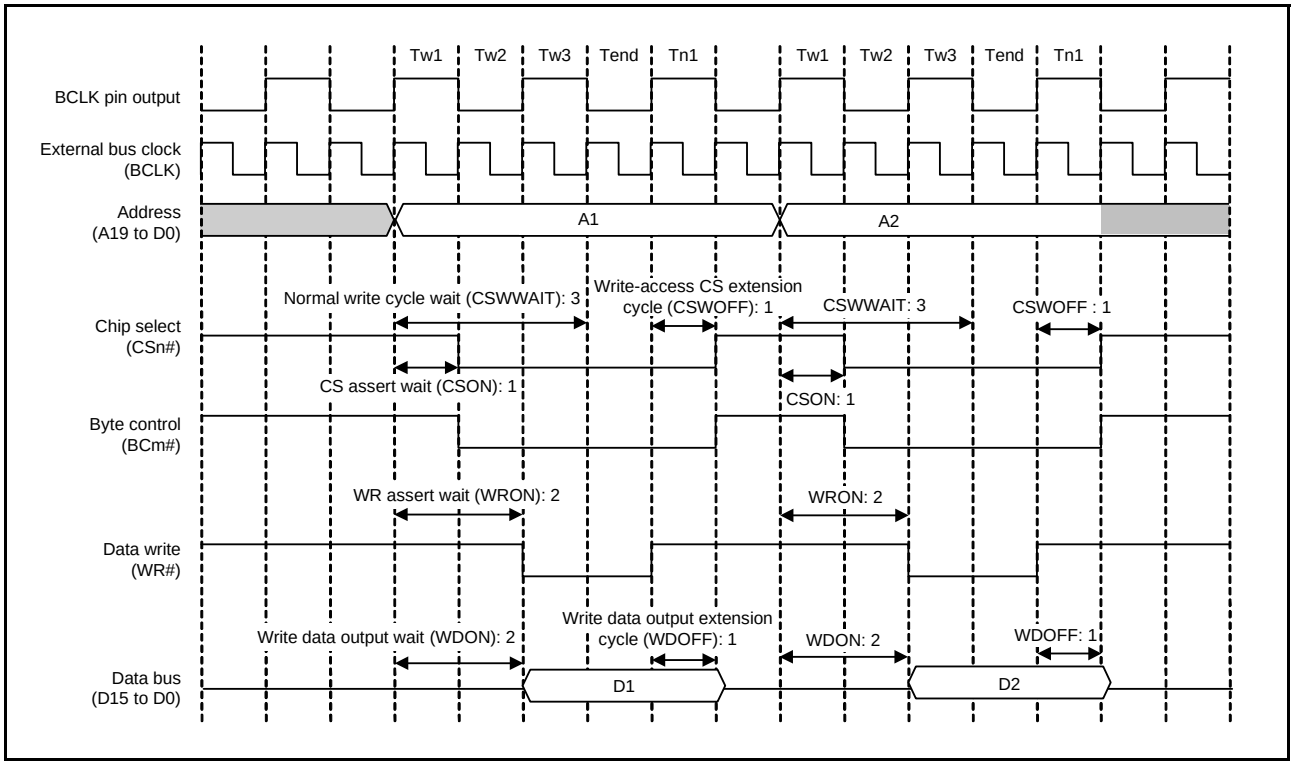


Figure 16.17 Example of Normal-Write Operation (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit) (n = 0 to 3, m = 0, 1)

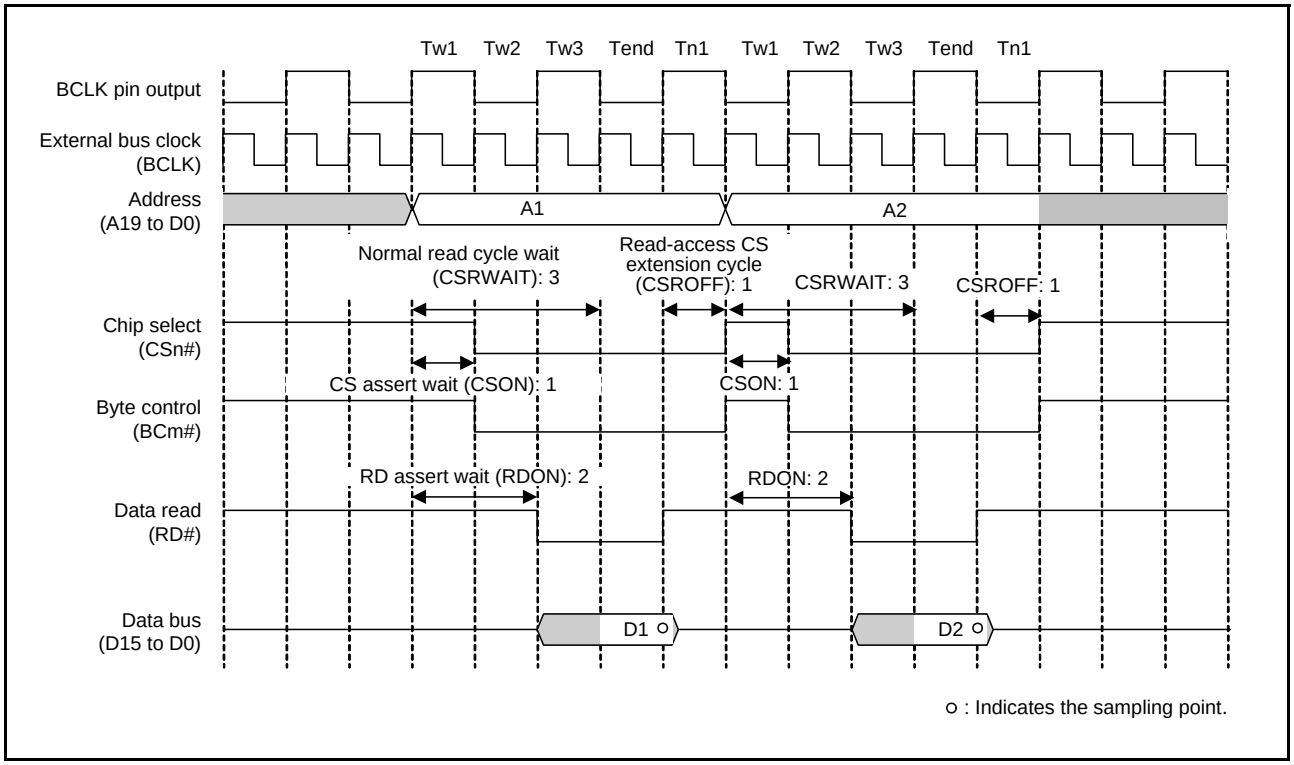


Figure 16.18 Example of Normal-Read Operation (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit and Two Rounds of Bus Access are Generated in Response to a Single Request for Transfer) (n = 0 to 3, m = 0, 1)

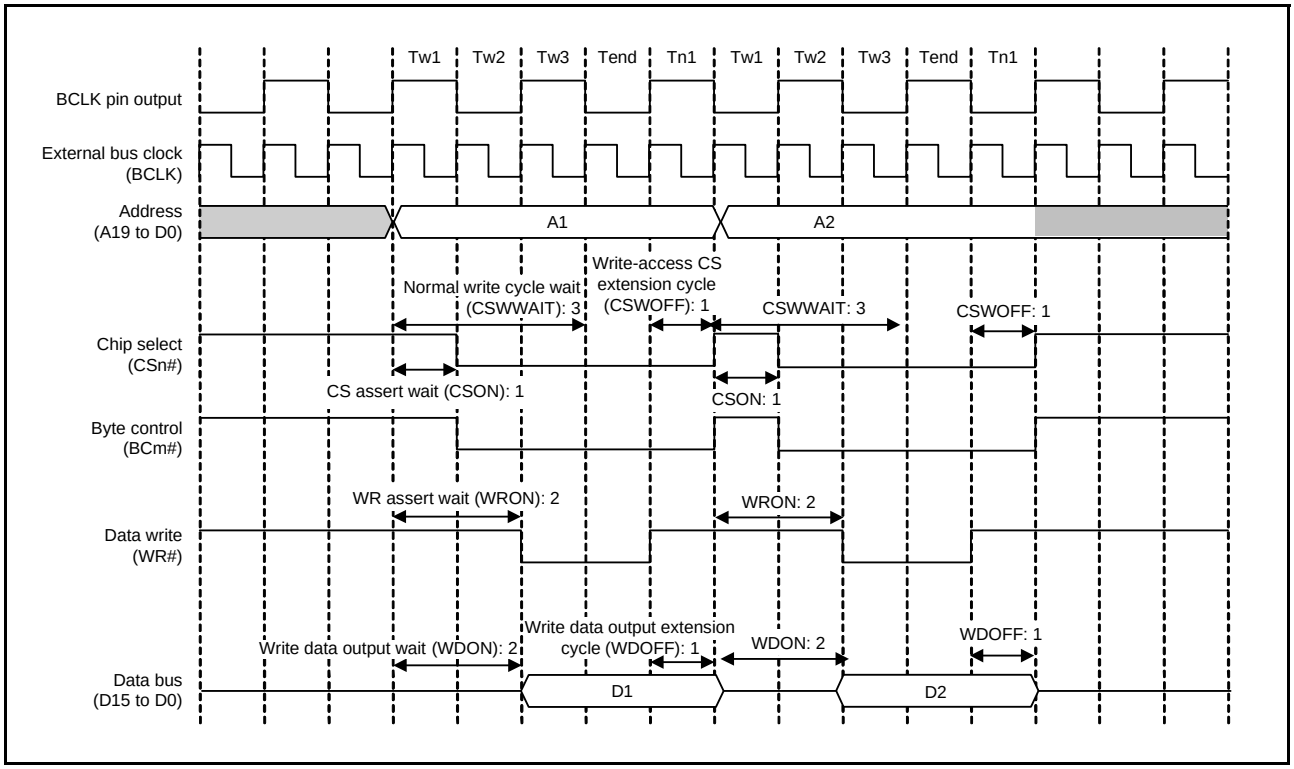


Figure 16.19 Example of Normal-Write Operation (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit and Two Rounds of Bus Access are Generated in Response to a Single Request for Transfer) (n = 0 to 3, m = 0, 1)

(2) Page Access

When the PRENB and PWENB bits in CSnMOD are set to 1 to enable page-read and page-write access, respectively, the bus access for page access operations becomes page reading and writing. Specifically, page access can occur when two or more rounds of external bus access are required for a single transfer request from the bus master. However, normal access is made when the split accesses are not aligned or the access spreads over the 32-bit boundary. See Figure 16.6 to Figure 16.9 for the conditions under which page access occurs.

Figure 16.20 and Figure 16.21 show examples of page access operations.

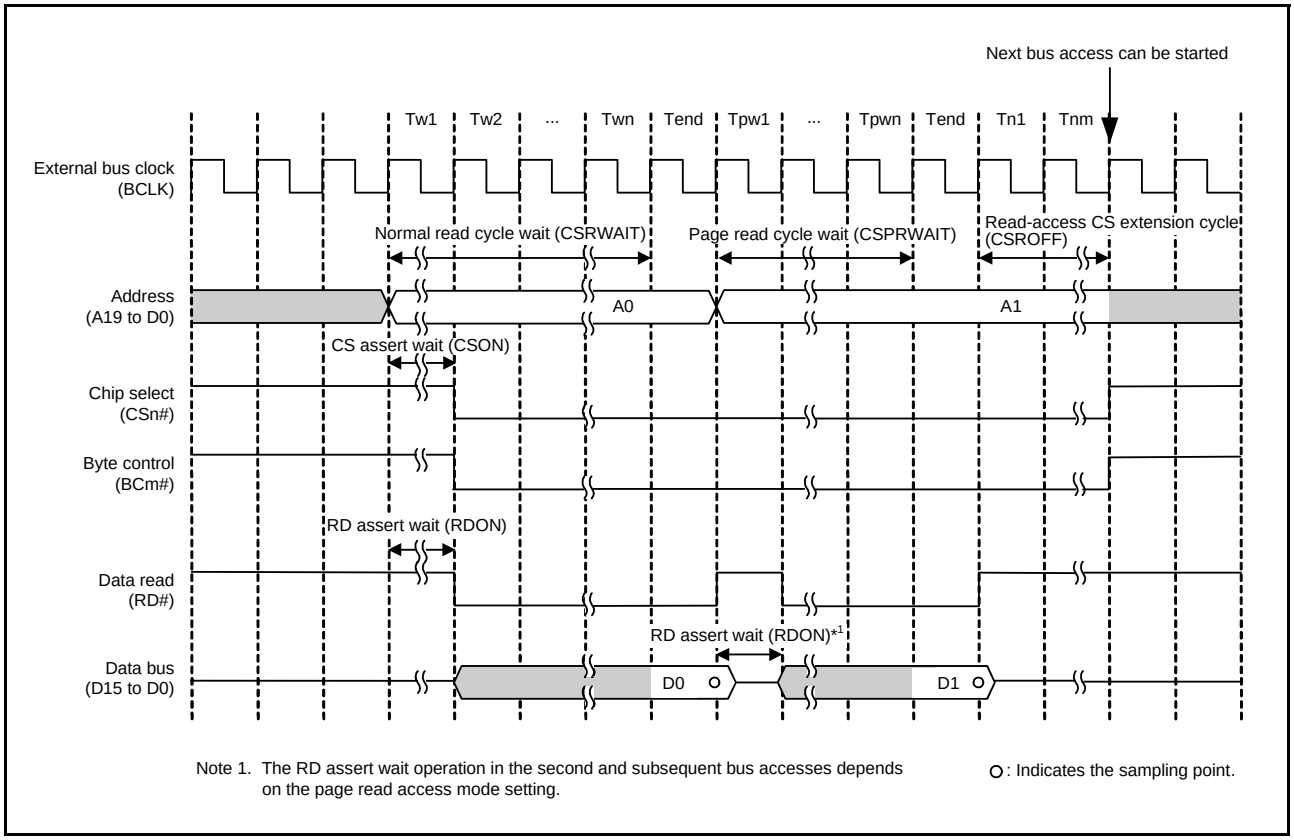


Figure 16.20 Page-Read Access Timing (n = 0 to 3, m = 0, 1)

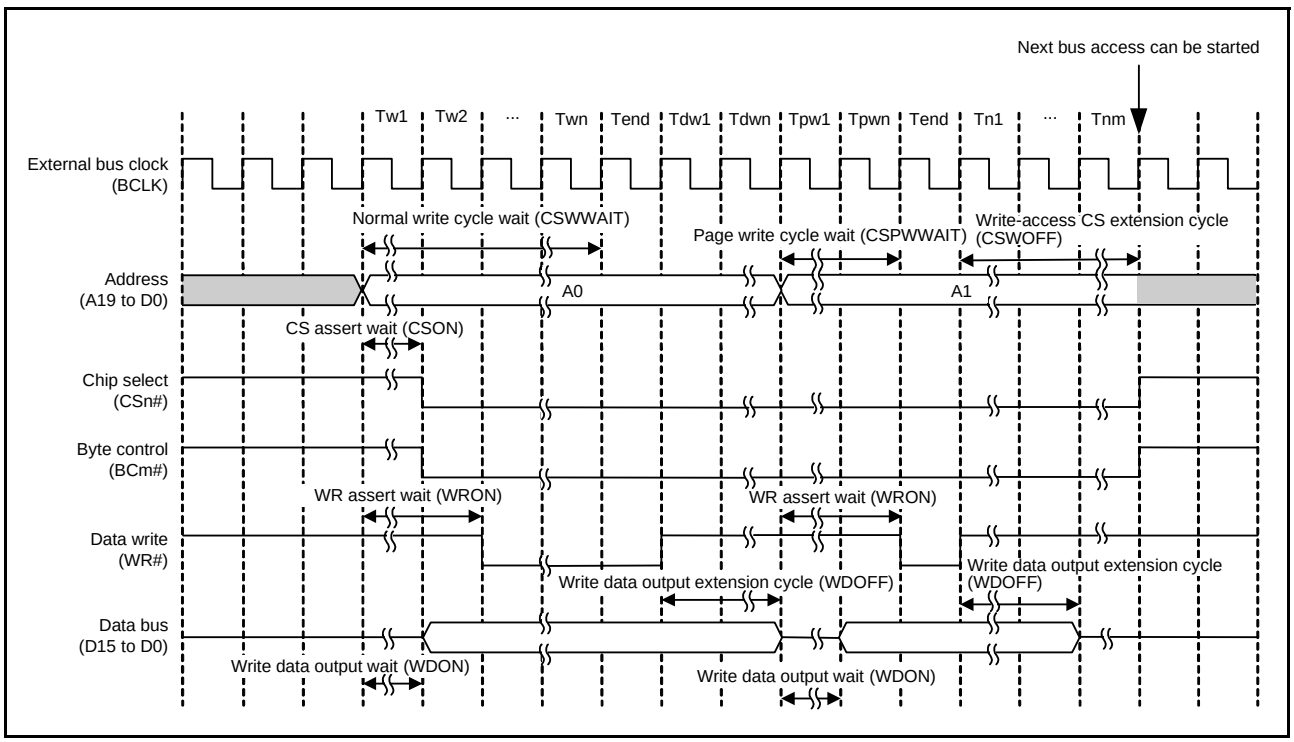


Figure 16.21 Page-Write Access Timing (n = 0 to 3, m = 0, 1)

Figure 16.22 and Figure 16.23 show examples of operations for access to a 16-bit bus space in 32 bits. The values of the wait control registers are example settings. In practice, the register settings will correspond to the specifications of connected devices.

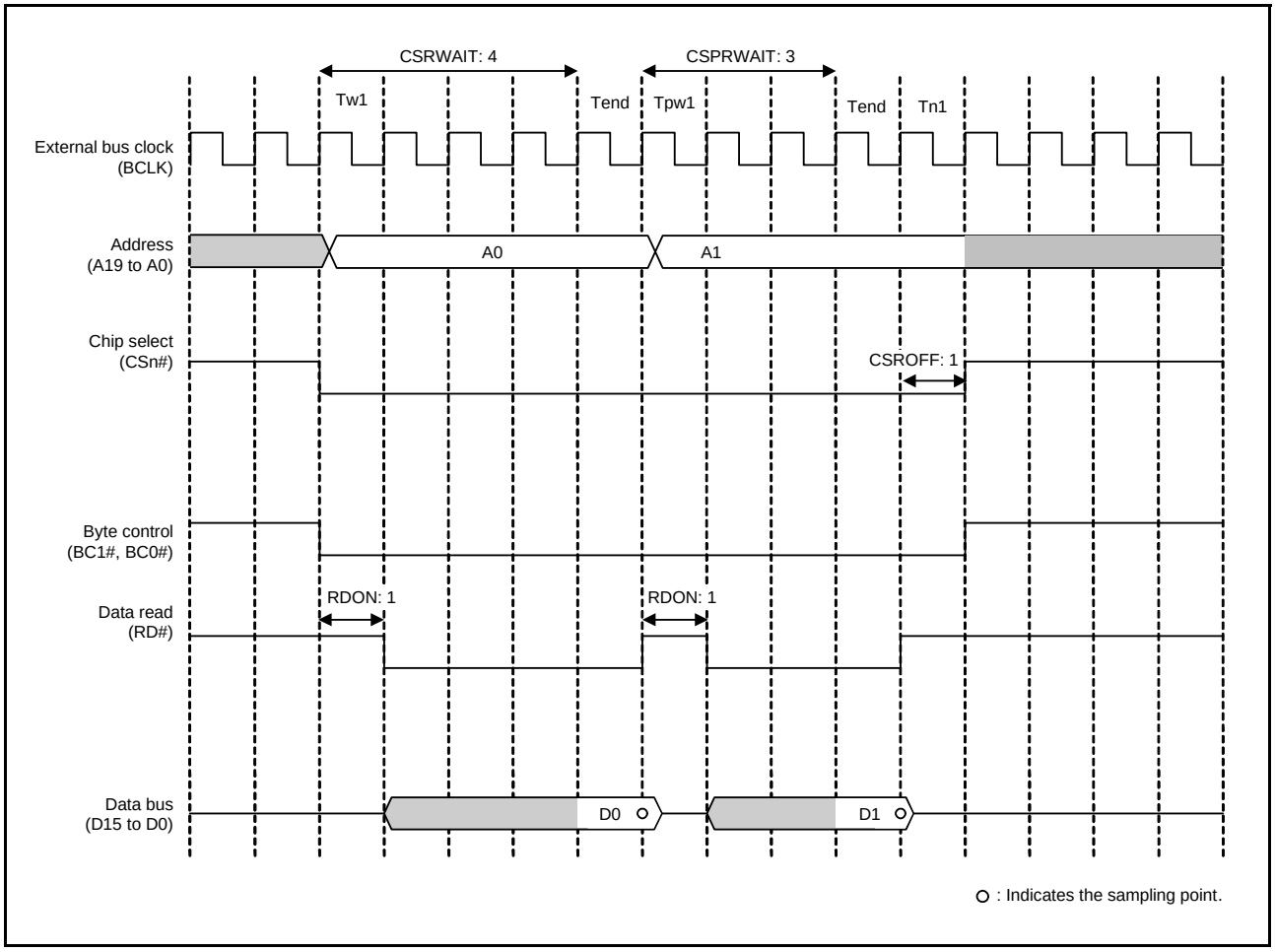


Figure 16.22 Example of Page-Read Access Operation (when 16-Bit Bus Space is Accessed in 32 Bits) (n = 0 to3)

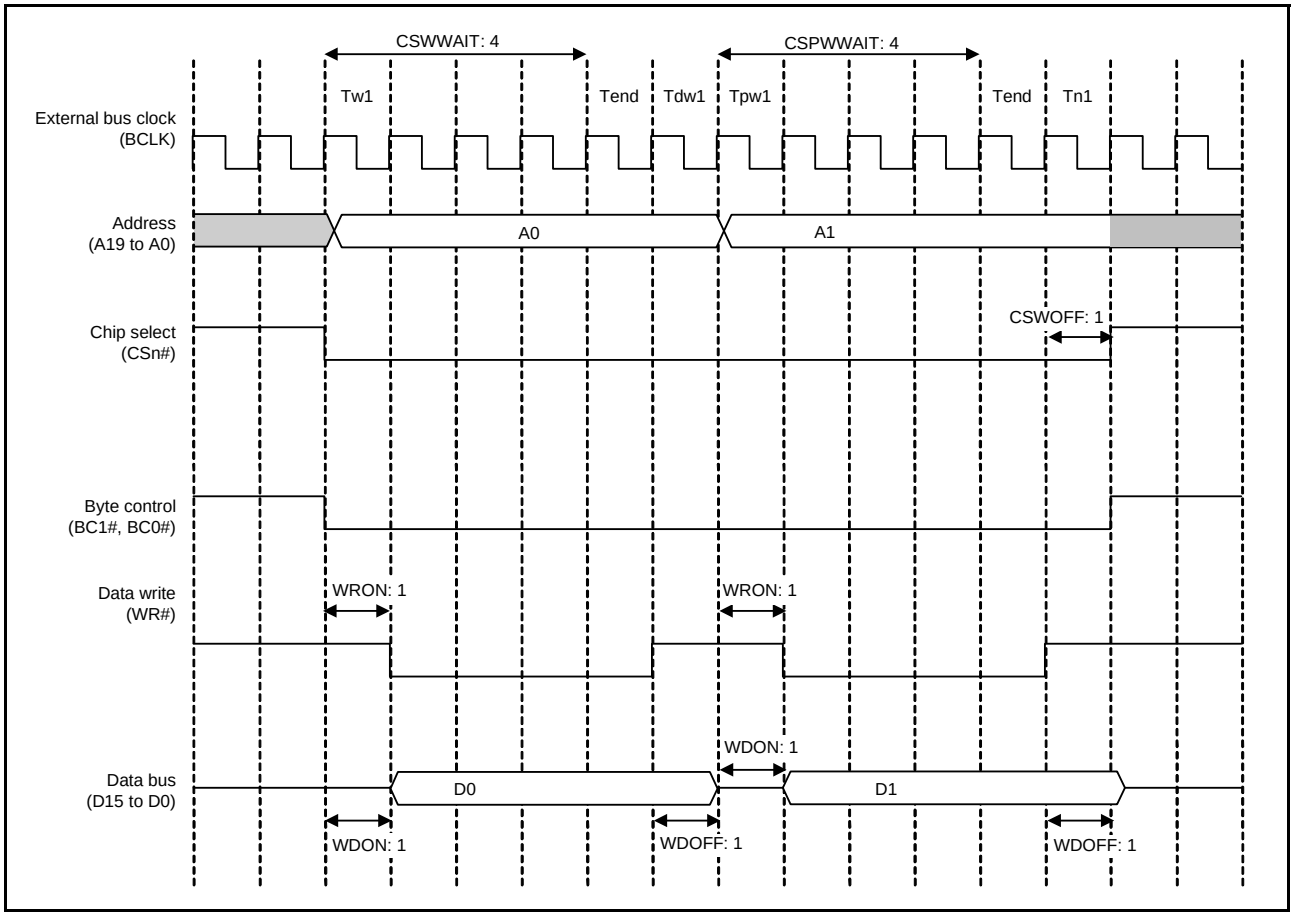


Figure 16.23 Example of Page-Write Access Operation (when 16-Bit Bus Space is Accessed in 32 Bits, in Single Write Strobe Mode) (n = 0 to 3)

Figure 16.24 and Figure 16.25 show examples of page access operations performed with the 1/2 BCLK selected with the BCLK pin output select bit.

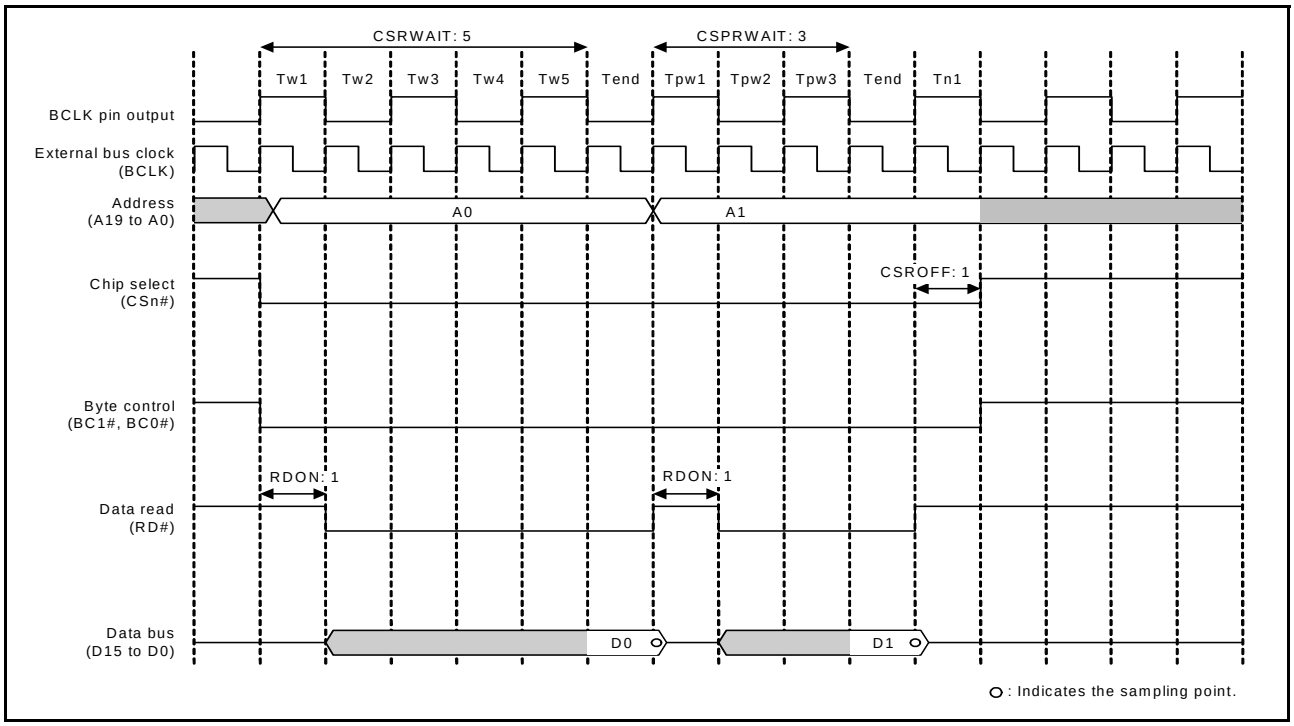


Figure 16.24 Example of Page Read Access Operation (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit and Two Rounds of Bus Access are Generated in Response to a Single Request for Transfer) (n = 0 to 3)

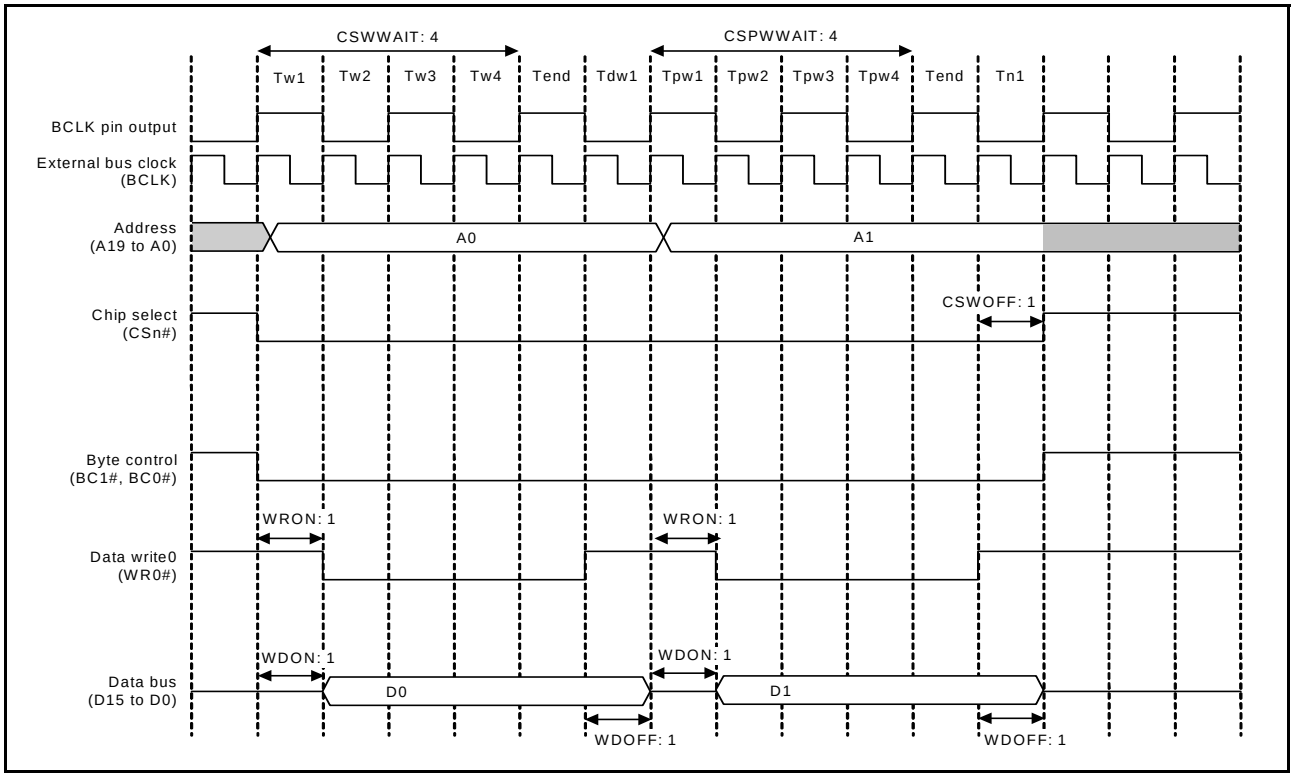


Figure 16.25 Example of Page Write Access Operation (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit and Two Rounds of Bus Access are Generated in Response to a Single Request for Transfer, in Single Write Strobe Mode) (n = 0 to 3)

16.5.2 Address/Data Multiplexed Bus

When the address/data multiplexed I/O interface select bit (MPXEN) in CSnCR is set to 1, addresses and data can be multiplexing input/output to/from the D15 to D0 pins in the corresponding area. Using this function enables direct connection of this MCU to peripheral MCUs requiring address/data multiplexing. When 8-bit width is selected with the BSIZE[1:0] bits in CSnCR, D7 to D0 are multiplexed with A7 to A0. When 16-bit width is selected, D15 to D0 are multiplexed with A15 to A0. In the address/data multiplexed I/O space, accesses are controlled with the ALE, RD#, WRn#, and BCn# signals.
Byte strobe mode or single-write strobe mode is selectable in the same way as for a separate bus. However, with regard to the BCn# signals within the address cycle, the byte-control signal is output for the data being read or written.
During the address/data multiplexed I/O space access, after the number of wait cycles specified by the address cycle wait select bits (AWAIT[1:0]) in CSnWCR2 is inserted in the address output cycle, data access is performed.

- Ta1 to Tan (Address Cycle Wait)

The period Ta1 to Tan is valid only when the address/data multiplexed I/O space is specified. This period is made up of the number of clock cycles between the start of external bus access and one cycle before the address latch (ALE) signal is negated. The number of cycles are selectable within the range from zero to three. Addresses are output until the next cycle of ALE signal negation (address cycle). The timing of ALE signal is the same as that of CS# assertion. After the address cycle, a data cycle is started. CSnWCR1 and CSnWCR2 should be set so that an address cycle and a data cycle do not overlap.

Page access to the address/data multiplexed I/O space is invalid. When the PRENB or PWENB bit in CSnMOD is set to 1 to enable page-read or page-write access, these settings are ignored and normal read or write operation is performed.

Figure 16.26 to Figure 16.28 show examples of operations with the address/data multiplexed I/O interface.

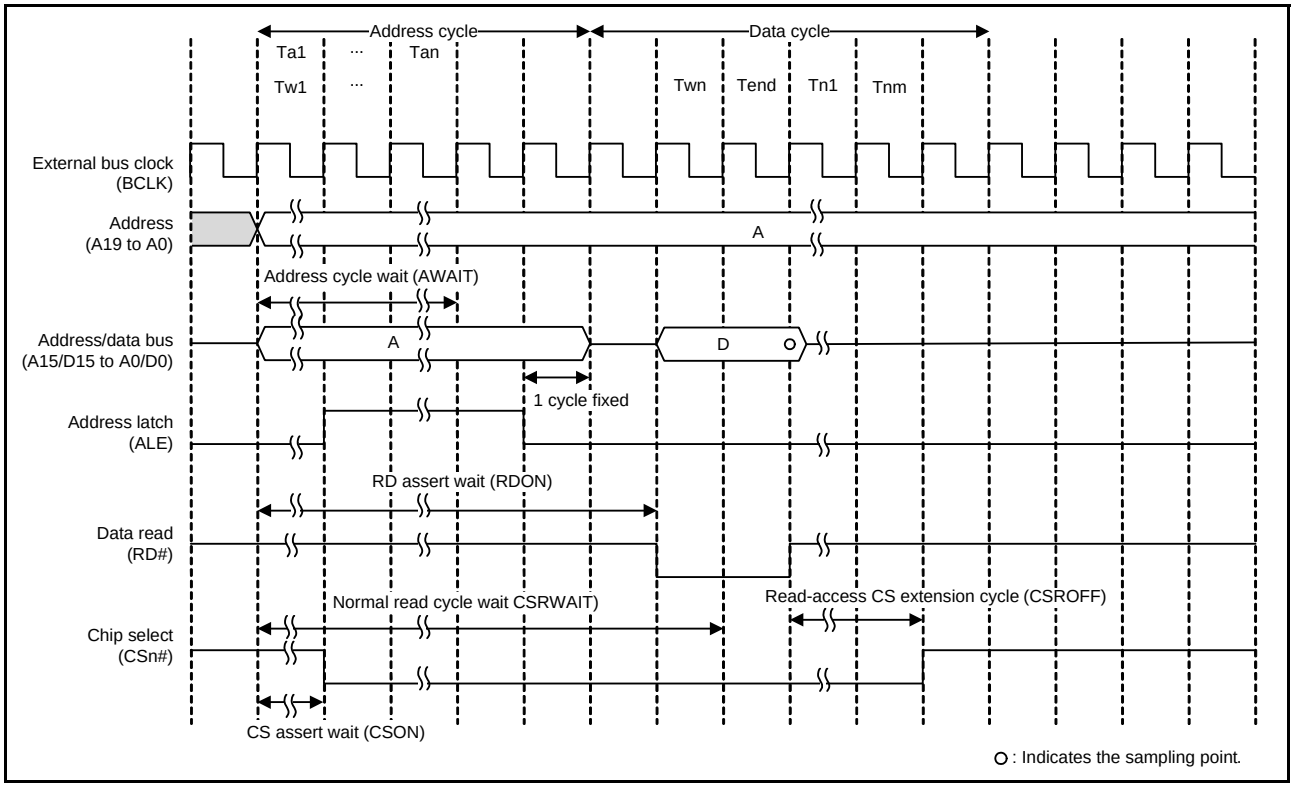


Figure 16.26 Example of Read Access Operation (with Address/Data Multiplexed I/O Interface)

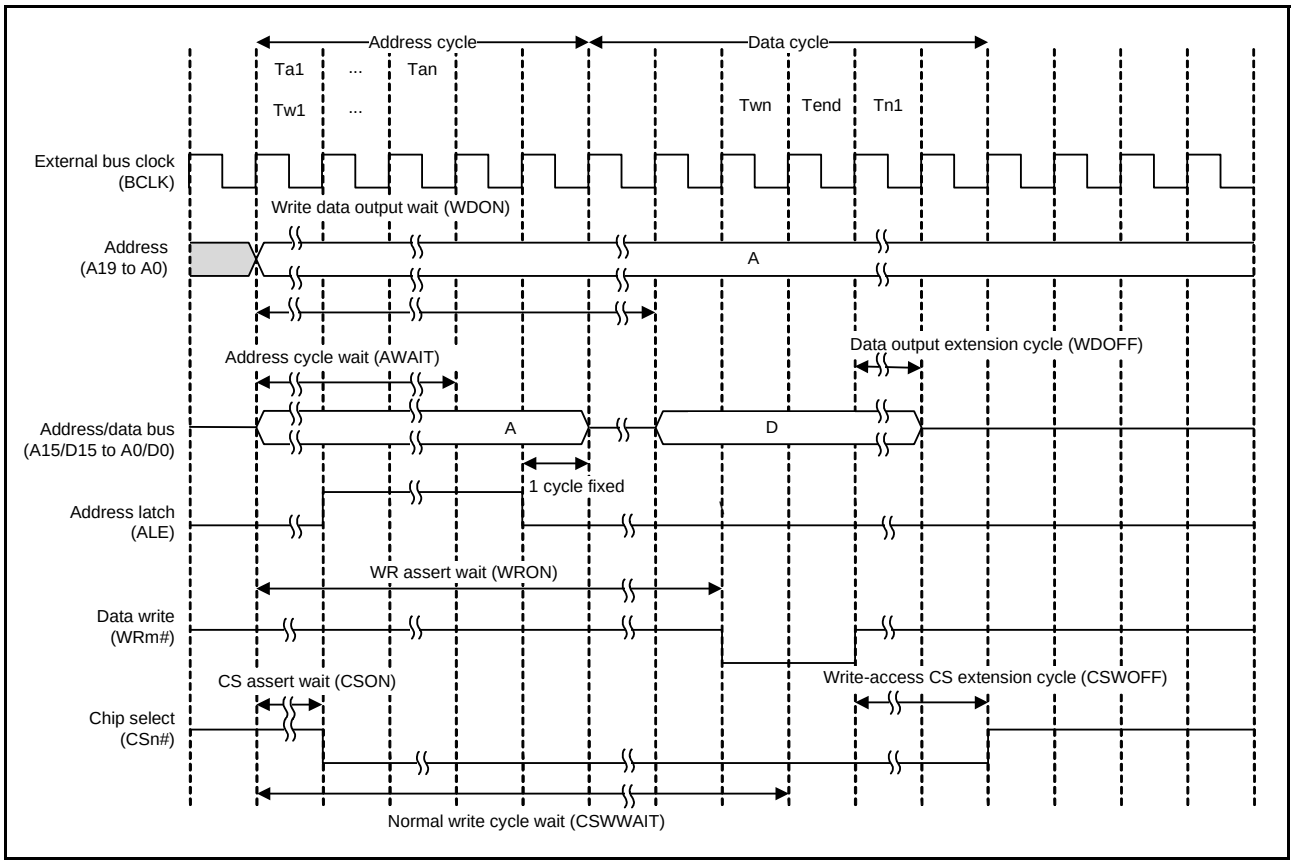


Figure 16.27 Example of Write Access Operation (with Address/Data Multiplexed I/O Interface; m = 0, 1)

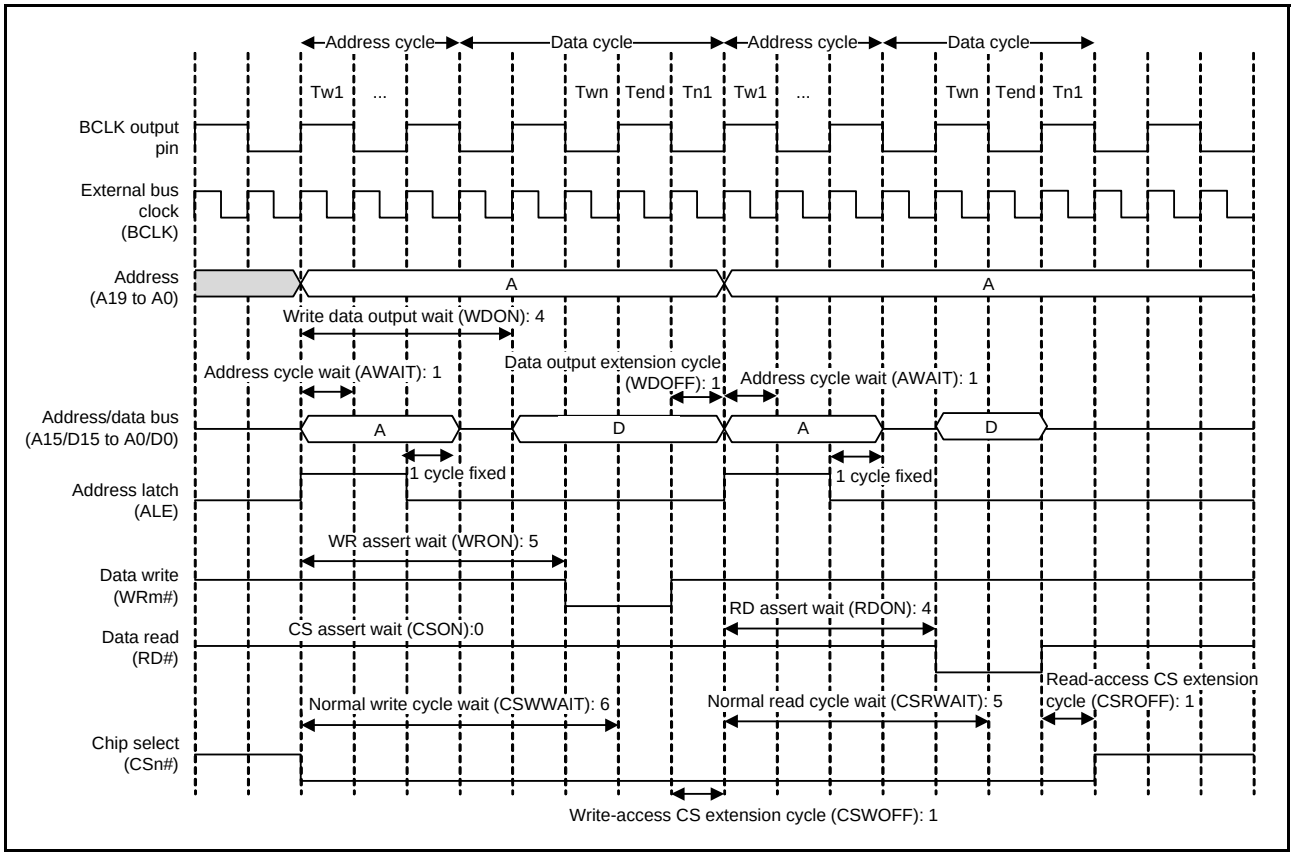


Figure 16.28 Example of Bus Timing (with Address/Data Multiplexed I/O Interface; m = 0, 1)

When two or more rounds of external bus access are required in response to a single transfer request, an address cycle and a data cycle are repeated in the second and subsequent external bus accesses in the same way as the first access operation. For details, see Figure 16.29 and Figure 16.30.

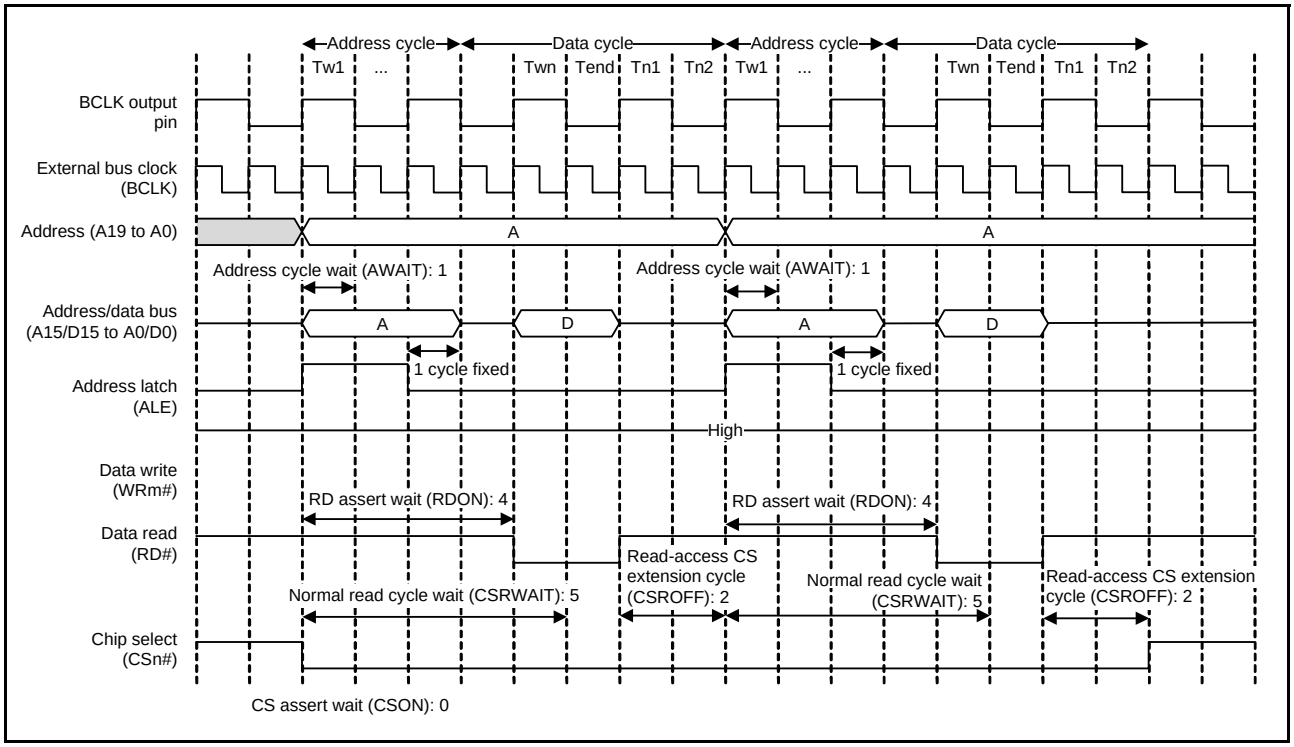


Figure 16.29 Example of Operation When a Read Access is Split (with Address/Data Multiplexed I/O Interface; m = 0, 1)

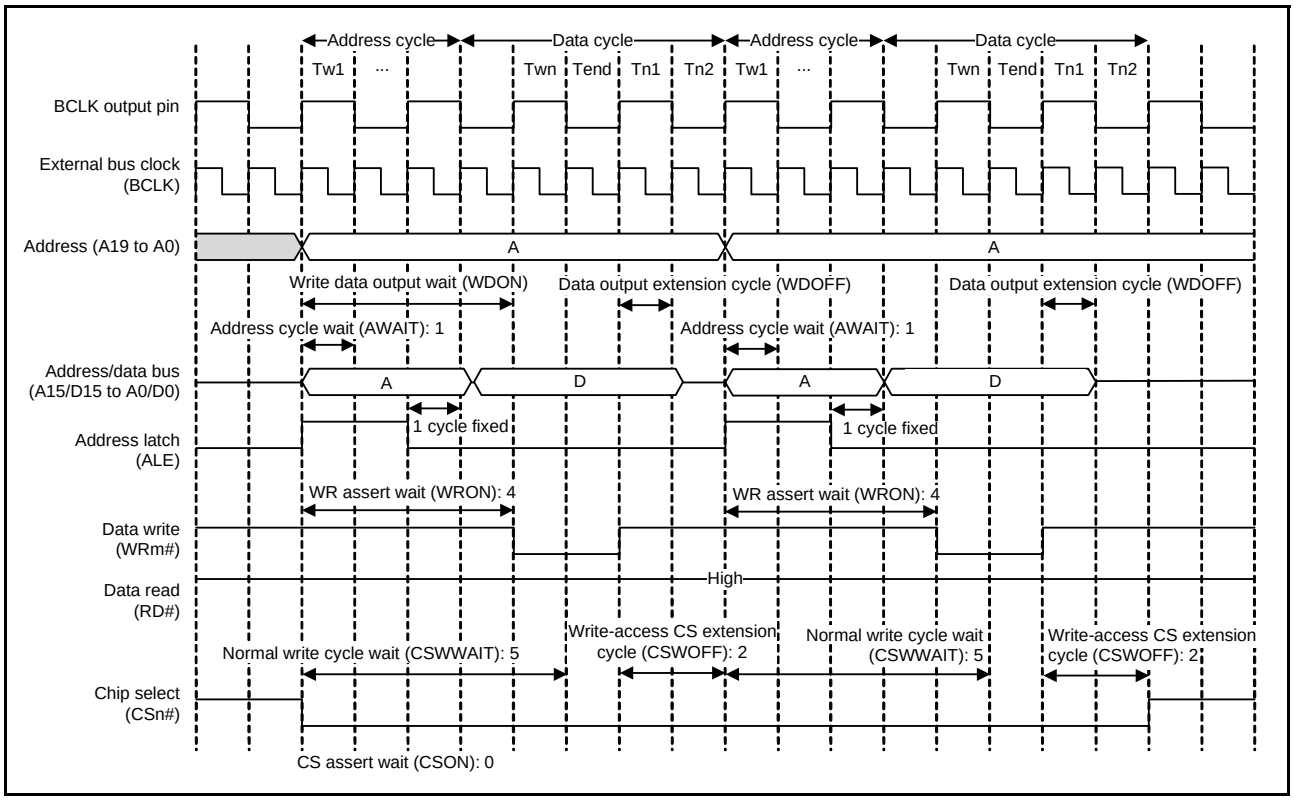


Figure 16.30 Example of Operation When a Write Access is Split (with Address/Data Multiplexed I/O Interface; m = 0, 1)

16.5.3 External Wait Function

Wait cycles can be extended by the WAIT# signal over the length of normal access cycle wait (specified by the CSRWAIT[4:0] and CSWWAIT[4:0] bits in CSnWCR1) and page access cycle wait (specified by the CSPRWAIT[2:0] and CSPWWAIT[2:0] bits in CSnWCR1).
When external wait is enabled (the EWENB bit = 1 in CSnMOD), wait cycles are inserted while the WAIT# signal is held low. When external wait is disabled (the EWENB bit = 0 in CSnMOD), the WAIT# signal has no effect.
All wait cycles specified in CSnWCR1 are inserted independently of the WAIT# signal.

(1) Normal Access

Sampling of the WAIT# signal begins upon completion of the wait cycle (Tend) specified in CSnWCR1. The bus cycle is extended while the WAIT# signal is held low. The wait cycle ends (Tend) at the next cycle after the WAIT# signal becomes high.

(2) Page Access

The first access operation is the same as the normal access operation. Sampling of the WAIT# signal begins upon completion of the wait cycle (Tend) specified in the CSnWCR1 register. The bus cycle is extended while the WAIT# signal is held low. The wait cycle ends (Tend) at the next cycle after the WAIT# signal becomes high.
With respect to the second and subsequent accesses, sampling of the WAIT# signal begins upon completion of the wait cycle of the page access (Tend). The wait cycle of the page access is extended while the WAIT# signal is held low, and ends (Tend) at the next cycle after the WAIT# signal becomes high.
Figure 16.31 and Figure 16.32 show examples of external wait insertion timing with the separate bus interface.

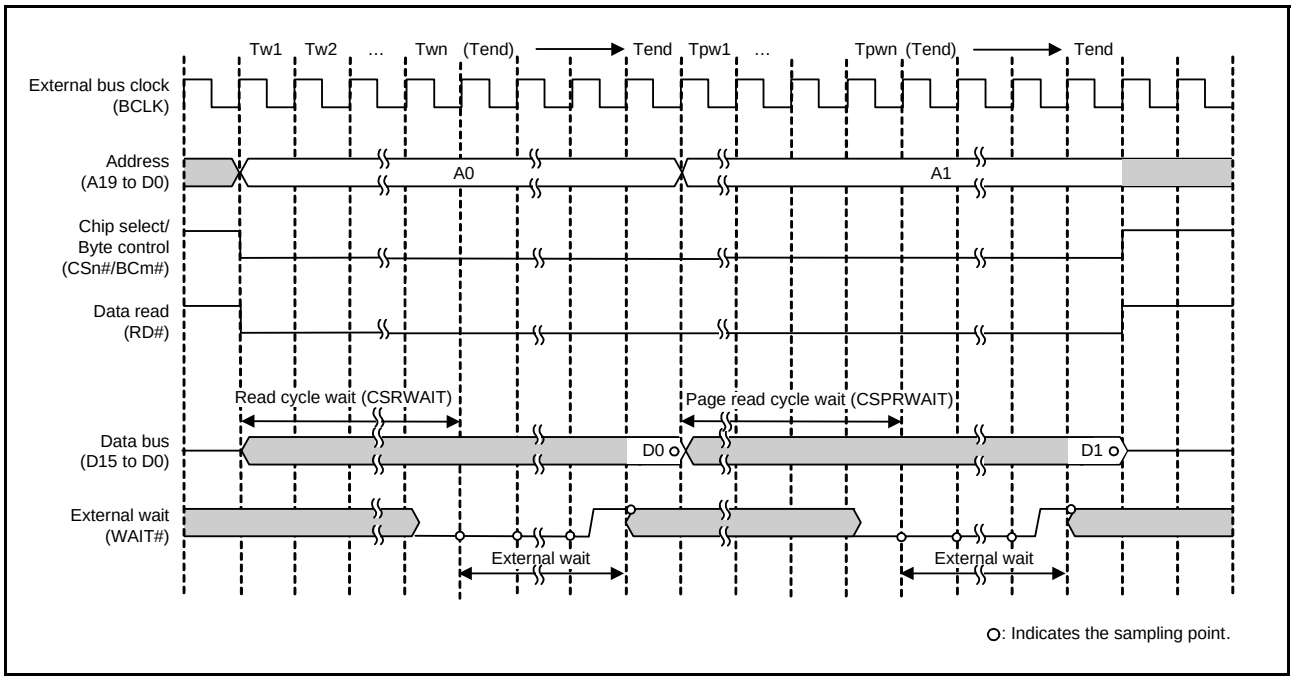


Figure 16.31 Example of External Wait Timing (Page-Read Access to 16-Bit Bus Space) (n = 0 to 3, m = 0, 1)

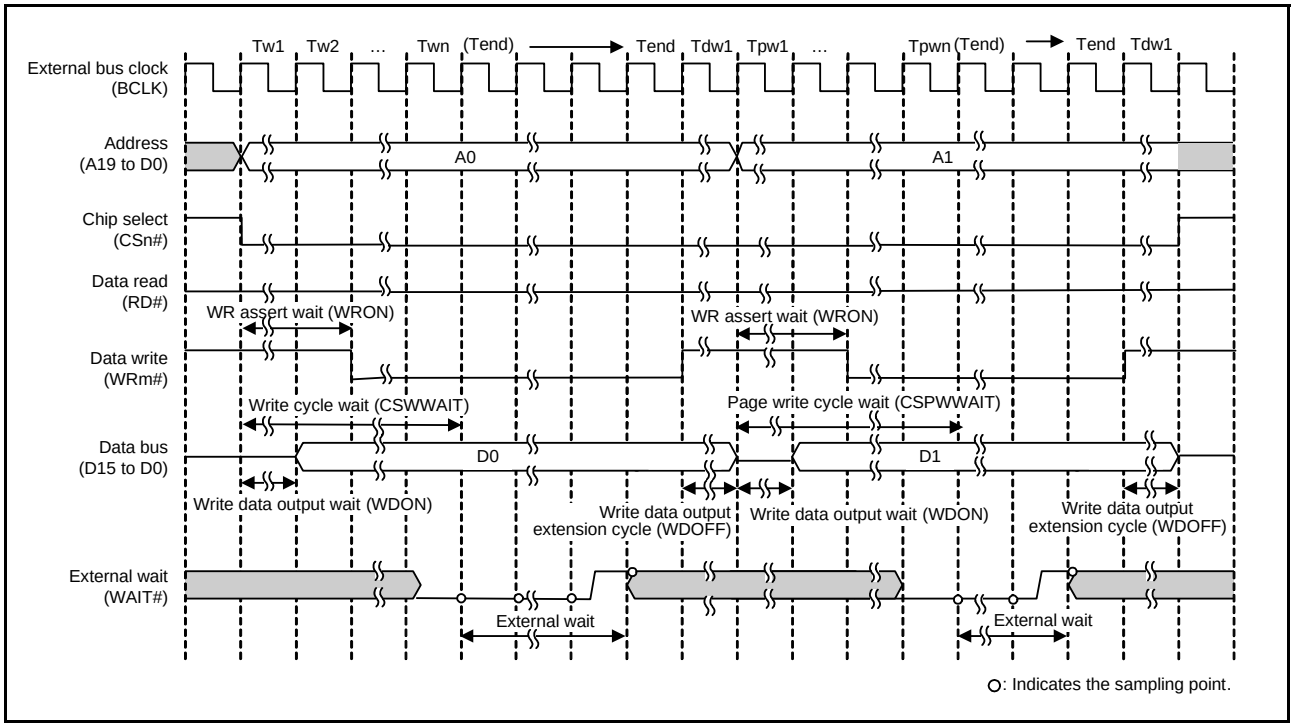


Figure 16.32 Example of External Wait Timing (Page-Write Access to 16-Bit Bus Space, in Byte Strobe Mode) (n = 0 to 3, m = 0, 1)

(3) Address/Data Multiplexed I/O Interface

In a data cycle with the address/data multiplexed I/O interface, programmed waits and pin waits using the WAIT pin can be inserted in the same way as that with the separate bus interface.

Address cycles are not affected by the wait control settings. Figure 16.33 shows an example of external wait insertion timing with the address/data multiplexed I/O interface.

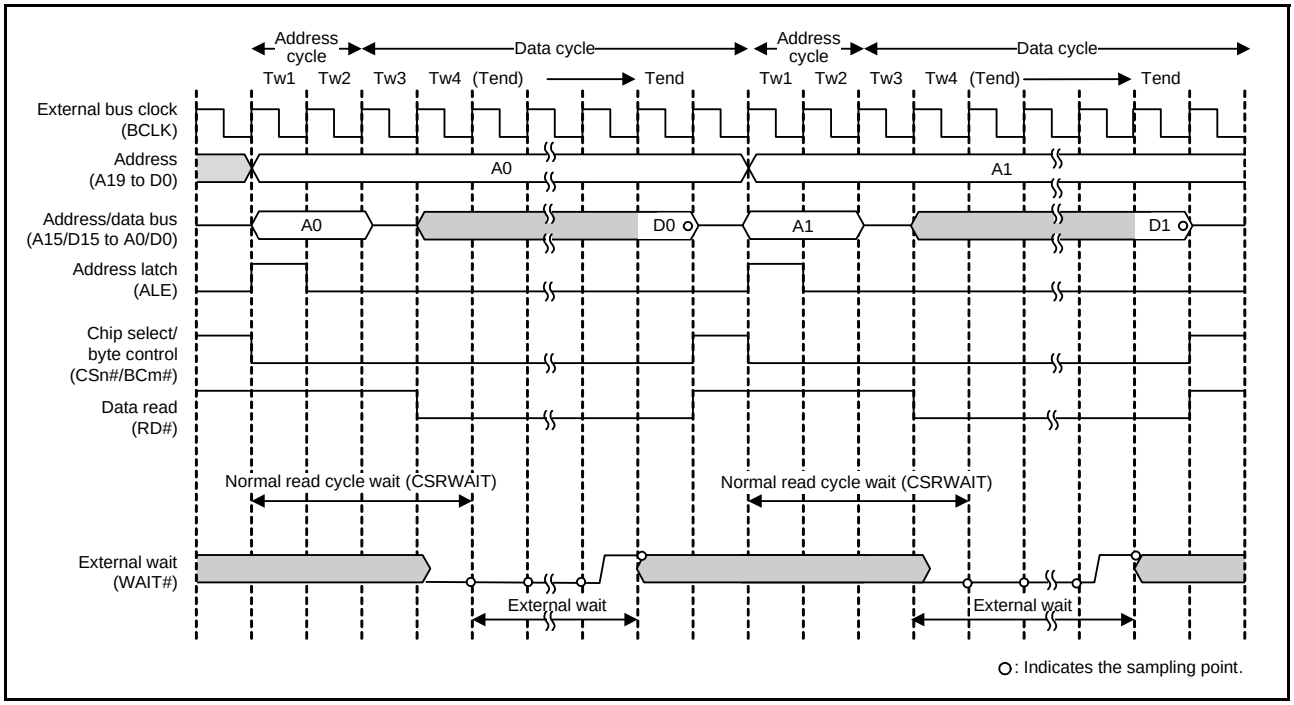


Figure 16.33 Example of External Wait Insertion Timing (with Address/Data Multiplexed I/O Interface; m = 0, 1)

16.5.4 Insertion of Recovery Cycles

Recovery cycles can be inserted between consecutive rounds of external bus access by setting the recovery cycle insertion enable bit in CSRECEN to 1.
The number of recovery cycles to be inserted after read cycles and write cycles can be separately set for each area using CSnREC. When the preceding bus cycle is a write access, the number of write recovery cycles should be set with the WRCV[3:0] bits for the area. When the preceding bus cycle is a read access, the number of read recovery cycles should be set with the RRCV[3:0] bits for the area. For example, when CS1 read access occurs after CS0 read access, the number of recovery cycles to be inserted between them is set by the RRCV[3:0] bits in CS0REC.
Recovery cycles can be inserted on any of the following eight conditions. The recovery cycle insertion can be enabled or disabled with the RCVENj (j = 0 to 7) in CSRECEN when the preceding bus access is a separate bus access, and with RCVENMj (j = 0 to 7) when the preceding bus access is an address/data multiplexed bus access.

- After a read access to the external bus, a read access is made to the external bus in the same area.
- After a read access to the external bus, a read access is made to the external bus in a different area.
- After a read access to the external bus, a write access is made to the external bus in the same area.
- After a read access to the external bus, a write access is made to the external bus in a different area.
- After a write access to the external bus, a read access is made to the external bus in the same area.
- After a write access to the external bus, a read access is made to the external bus in a different area.
- After a write access to the external bus, a write access is made to the external bus in the same area.
- After a write access to the external bus, a write access is made to the external bus in a different area.

The recovery cycle starts at the end of the preceding bus cycle, i.e. when the CSn# signal (n = 0 to 3) is negated. A high-level period of the CSn# signal is inserted for the specified recovery cycle period starting from this point.
The CSn# signal for the next round of bus access is asserted immediately after the end of recovery cycles in the fastest case. Even if the next request for access to an external address space is generated during the recovery period, the next round of access over the external bus will start immediately after the end of recovery cycles.
When two or more external bus access cycles are required for a single transfer request from a bus master and the recovery cycle insertion condition is satisfied, recovery cycles are also inserted between these bus access cycles. However, when page read access is enabled (CSnMOD.PRENB = 1) or page write access is enabled (CSnMOD.PWENB = 1), recovery cycles are not inserted except after the last bus access cycle of the transfer even if the recovery cycle insertion condition is satisfied (Figure 16.36). Similarly, during normal accesses with page access enabled, recovery cycles are not inserted between bus access cycles but inserted only after the last bus access cycle of the transfer. Similarly, during normal accesses with page access enabled, with the separate bus interface, recovery cycles are not inserted between bus access cycles but inserted only after the last bus access cycle of the transfer. With the address/data multiplexed I/O interface, when the recovery cycle insertion condition is satisfied, recovery cycles are inserted between bus access cycles regardless of the page access enable setting.

Figure 16.34 to Figure 16.36 show examples of recovery cycle insertion with the separate bus interface.

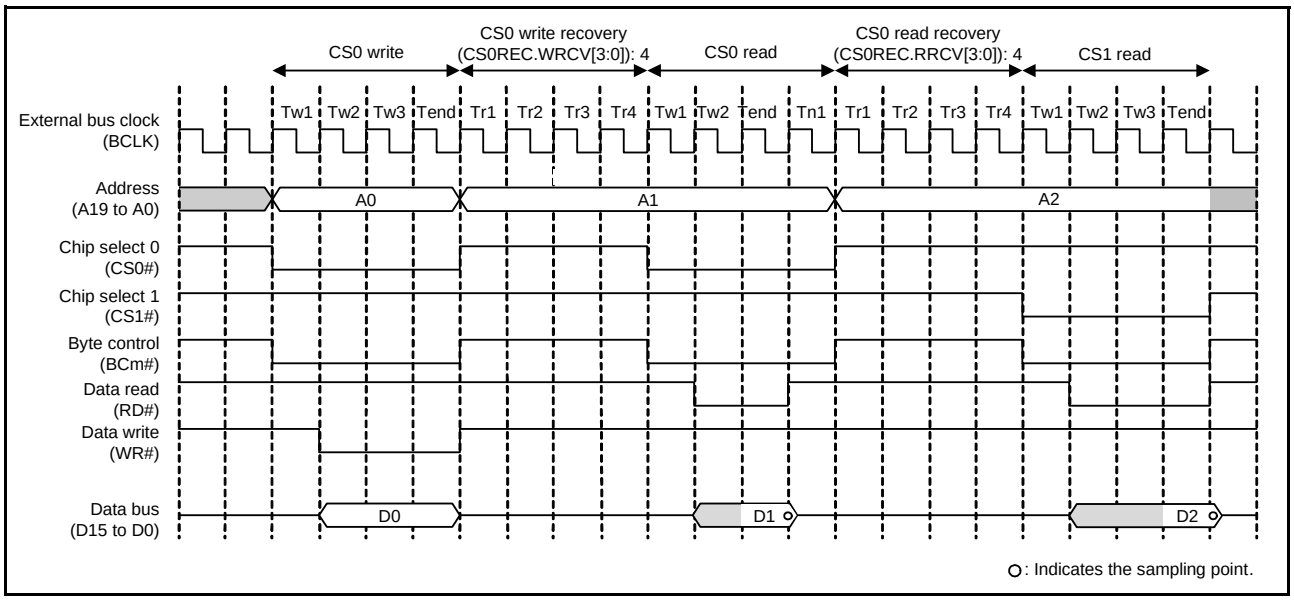


Figure 16.34 Example of Recovery Cycle Insertion (with Separate Bus Interface) (m = 0, 1)

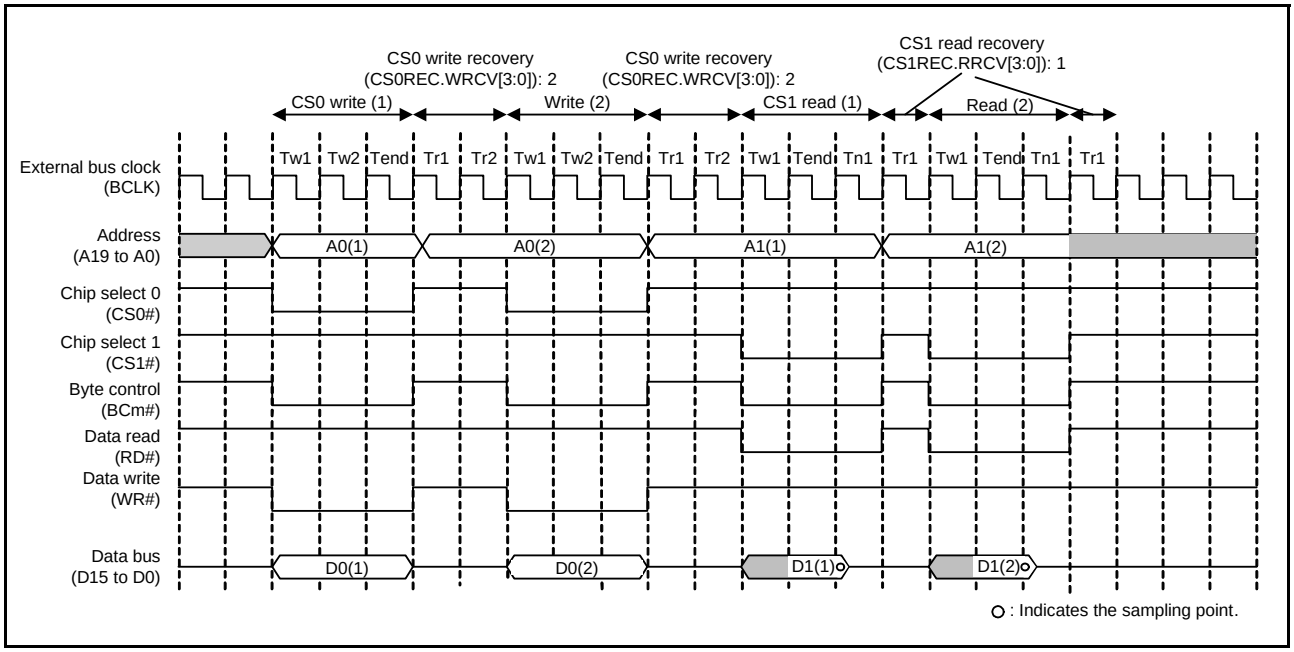


Figure 16.35 Example of Recovery Cycle Insertion When a Bus Access is Split (with Separate Bus Interface, Normal Access) (m = 0, 1)

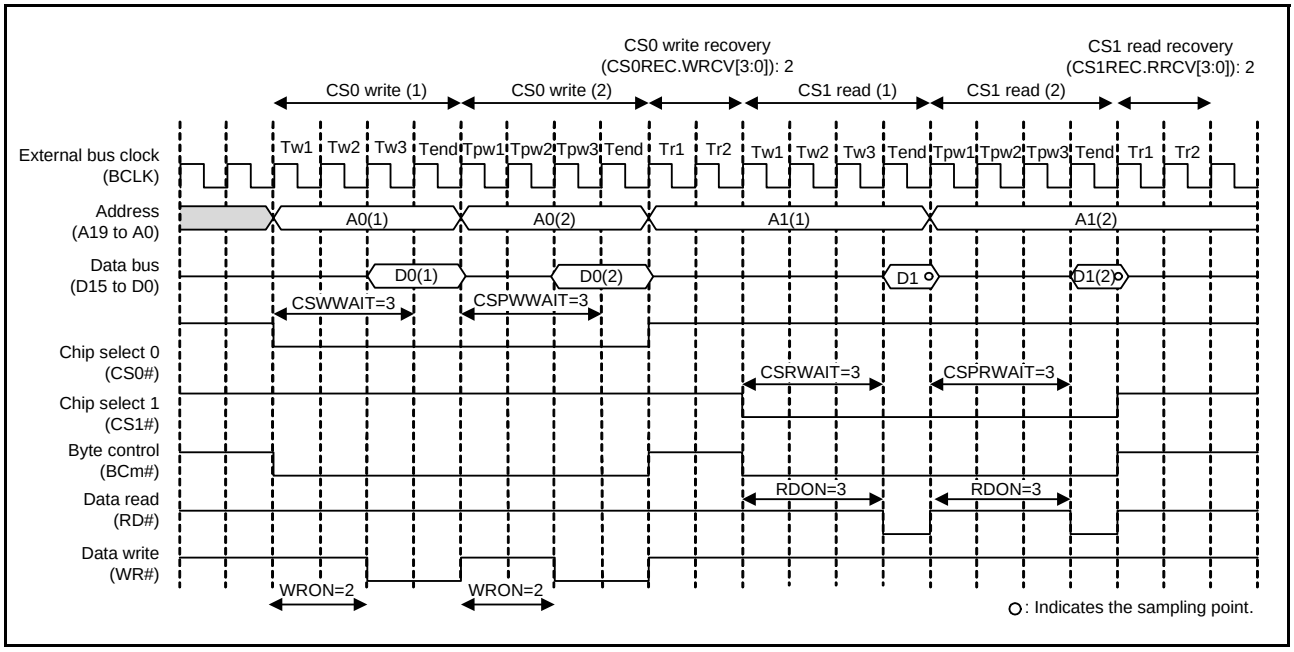


Figure 16.36 Example of Recovery Cycle Insertion When a Bus Access is Split (with Separate Bus Interface, Page Access) (m = 0, 1)

Figure 16.37 and Figure 16.38 show examples of operations when the BCLK pin output selection bits are set for frequency-division of BCLK by 2.

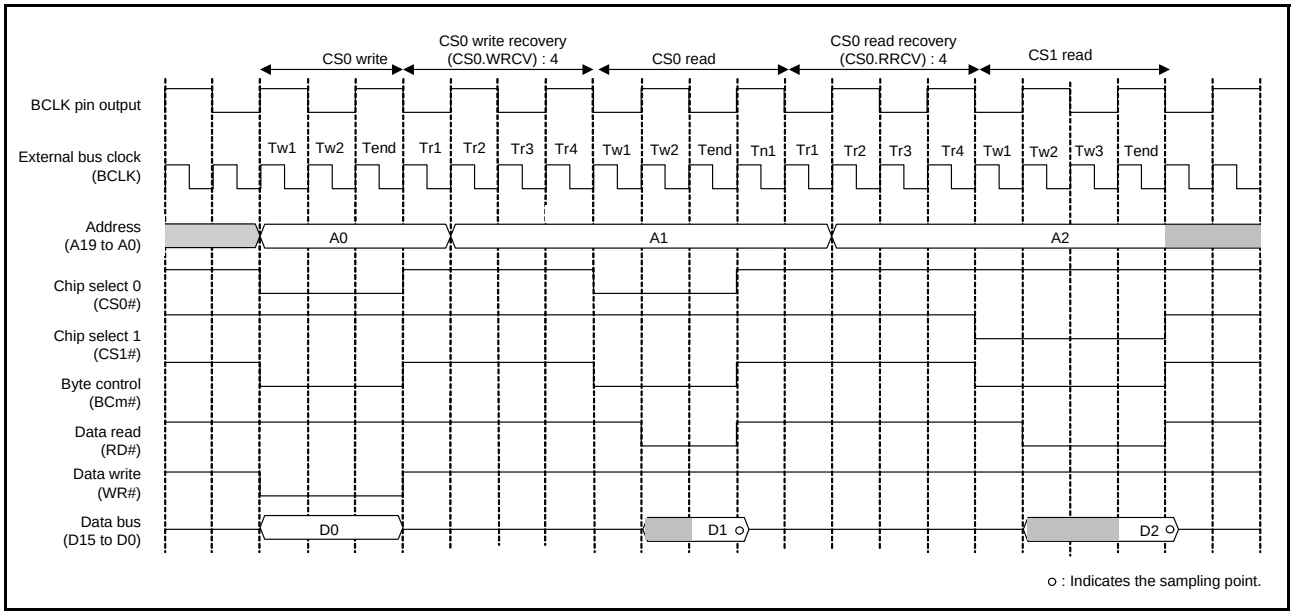


Figure 16.37 Example of Operation for Recovery Cycles when the BCLK Pin Output Selection Bits Are Set for Frequency-Division of BCLK by 2 (For the Case of Normal Access Through a Separate Bus Interface; m = 0, 1)

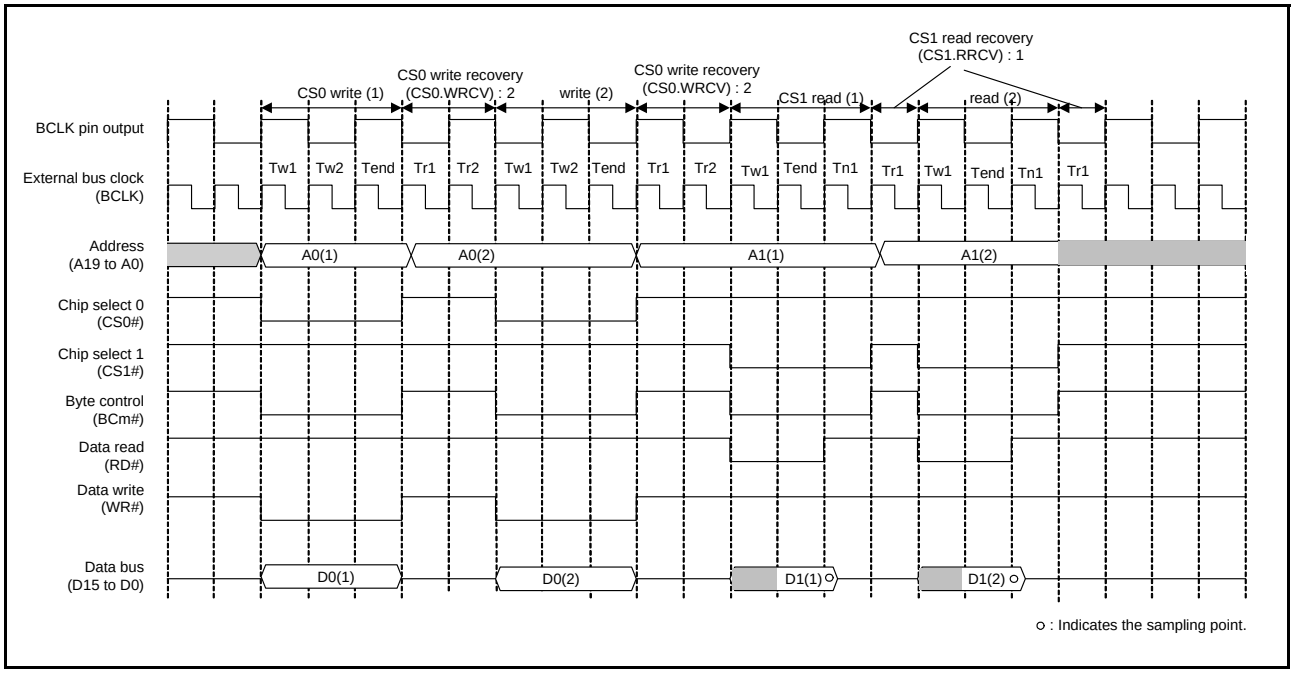


Figure 16.38 Example of Operation for Recovery Cycles when the BCLK Pin Output Selection Bits Are Set for Frequency-Division of BCLK by 2 (For the Case where Bus Access is Divided up; m = 0, 1)

With the address/data multiplexed I/O interface, recovery cycles are inserted in the same way as that with the separate bus interface. Figure 16.39 and Figure 16.40 show examples of recovery cycle insertion with the address/data multiplexed I/O interface.

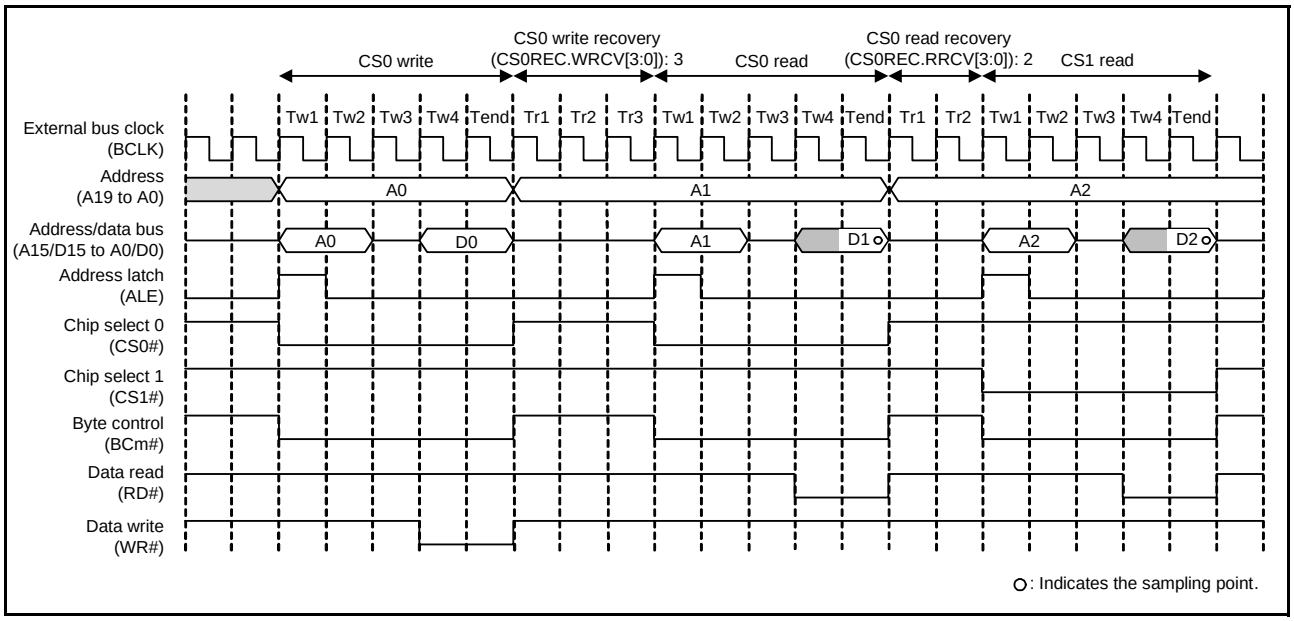


Figure 16.39 Example of Recovery Cycle Insertion (with Address/Data Multiplexed I/O Interface; m = 0, 1)

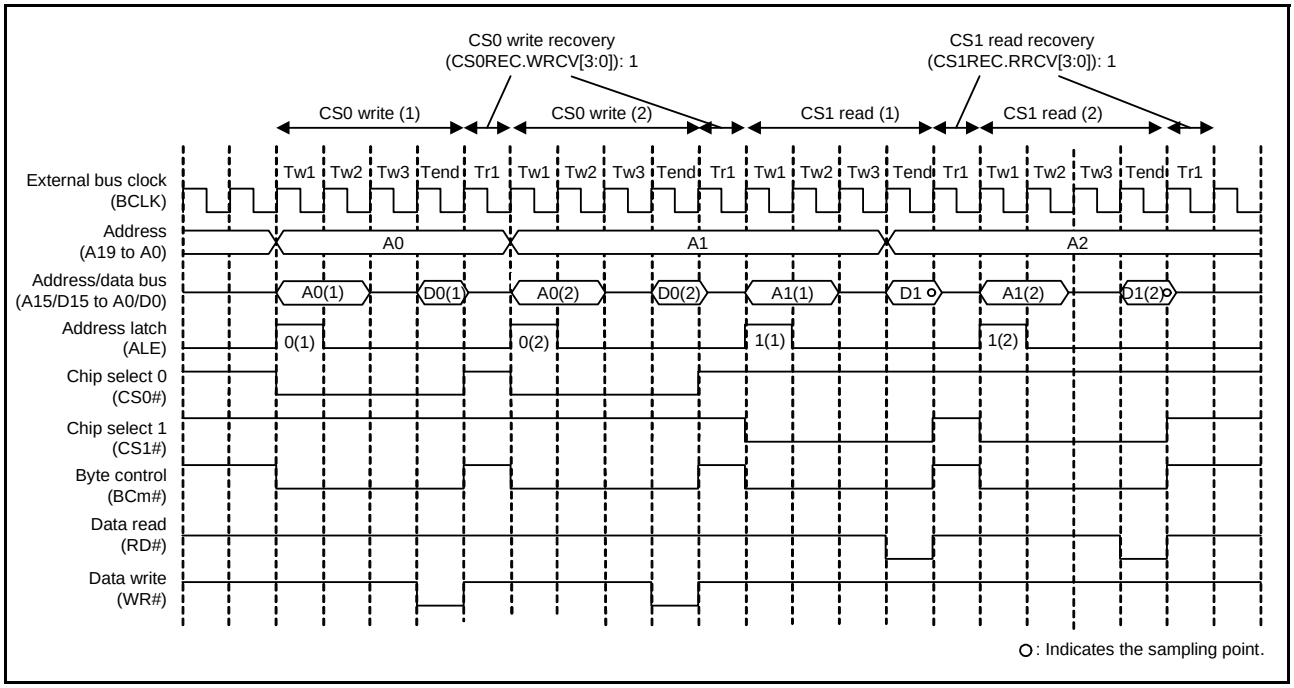


Figure 16.40 Example of Recovery Cycle Insertion When a Bus Access is Split (with Address/Data Multiplexed I/O Interface; m = 0, 1)

16.5.5 No Access State

When no external address space is accessed, CSn#, BCn#, WRn#, and RDn# signals are high, ALE signal is low, and D15 to D0 are in the high-impedance state.

16.5.6 Write Buffer Function (External Bus)

The internal main bus is released by writing data to the write buffer before the write access is completed, which allows the next round of bus access to start. However, if the following round of bus access is to an external address space or to a register of the external bus controller, it is suspended until the external bus operations already in progress are completed. Figure 16.41 shows an example of operation when the write-buffer function is in use. When this function is in use, if the next operation after an external write is internal access, the internal access (access to on-chip memory or a peripheral module) is executed in parallel with the external write, i.e. without waiting for completion of the latter operation.

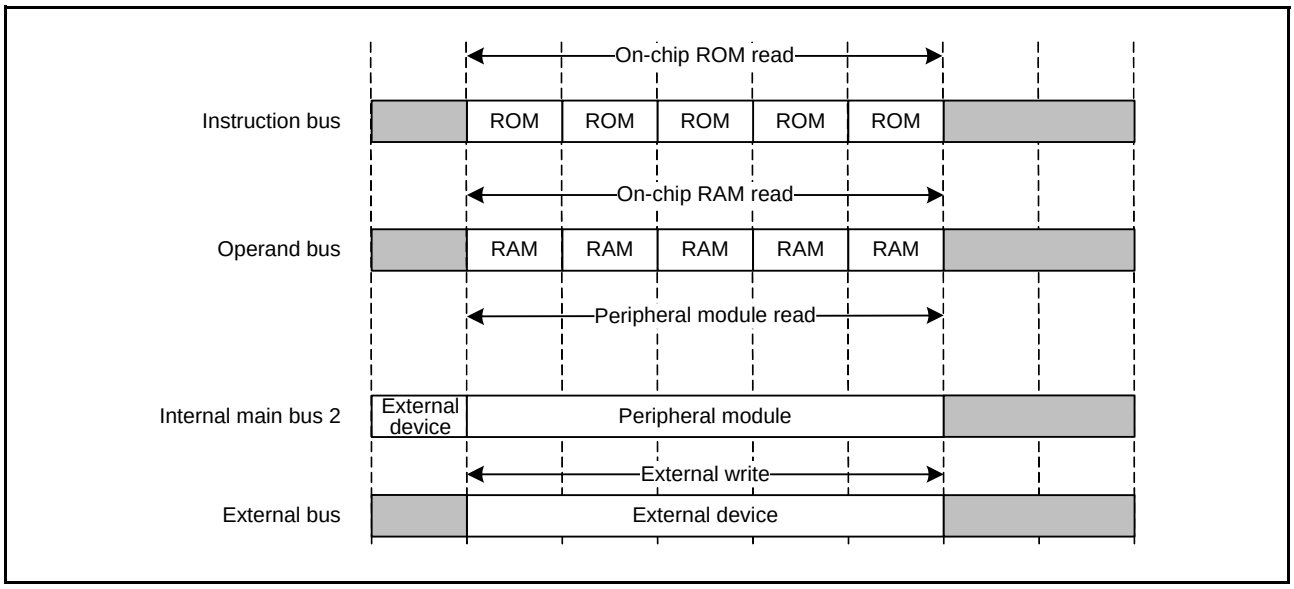


Figure 16.41 Example of Operation when the Write-Buffer Function is in Use

16.5.7 Limitations

(1) Limitations on Using Separate Bus Interface

- Limitations that apply to various bits of CSn wait control register 1 (CSnWCR1) and CSn wait control register 2 (CSnWCR2) at the times of normal and page accesses are listed in Table 16.9.
  Even if the setting of the page-read access enable bit in the CSn mode register or the page-write access enable bit in the CSn mode register selects permission (CSnMOD.PRENB = 1 or CSnMOD.PWENB = 1), the first round of access for page access and the access that does not fall within the scope of page access are normal access operation, and thus limitations on normal access must be satisfied.

Table 16.9 Limitations at the Time of Normal and Page Access

Limitations at the Time of Normal Access		Limitations at the Time of Page Access	
Reading	**Writing**	**Reading**	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON	CSON[2:0] ≤ CSPRWAIT RDON[2:0] ≤ CSPRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSPWWAIT WRON[2:0] ≤ CSPWWAIT WDON[2:0] ≤ CSPWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON

- When two or more external bus access cycles are required for a single transfer request from a bus master and the recovery cycle insertion condition is satisfied with page read access enabled (CSnMOD.PRENB = 1) or page write access enabled (CSnMOD.PWENB = 1), recovery cycles are not inserted between bus access cycles but inserted only after the last bus access cycle of the transfer.

(2) Limitations on Using Address/Data Multiplexed Bus Interface

- In the address/data multiplexed I/O space, page accesses are invalid. If a page access setting is specified, the setting is ignored and the normal read or write operation is performed.

Table 16.10 Limitations at the Time of Normal and Page Access

Limitations at the Time of Normal Access	
Reading	**Writing**
CSON[2:0] ≤ CSRWAIT	CSON[2:0] ≤ CSWWAIT
RDON[2:0] ≤ CSRWAIT	WRON[2:0] ≤ CSWWAIT
CSON[2:0] ≤ RDON	WDON[2:0] ≤ CSWWAIT
AWAIT[1:0]+2≤RDON	WDOFF[2:0] ≤ CSWOFF
CSON[2:0]≤AWAIT	WDON[2:0] ≤ WRON
	CSON[2:0] ≤ WRON
	AWAIT[1:0]+2≤WRON
	AWAIT[1:0]+2≤WDON
	CSON[2:0]≤AWAIT

(3) Limitation when a Pin is Multiplexed between A0 and BC0# Functions

When the A0 and BC0# pin functions share the same pin, setting the single write strobe mode is prohibited in the 8-bit bus space; otherwise the operation is not guaranteed.

(4) Limitations when 1/2 BCLK is Selected with BCLK Pin Output Select Bit

When 1/2 BCLK is selected through the BCLK pin output select bit, the external bus access cycle starts at the rising edge of the BCLK pin output. However, when two or more external bus access cycles are generated for a single transfer request from a bus master, the second or subsequent external bus access cycle may start at the falling edge of the BCLK pin output depending on the wait cycle settings. Make appropriate register settings according to the specifications of the device to be connected.

(5) Prohibition of Access that Spans Areas of Address Space

Single access that spans several areas of the address space is prohibited, and operation of such an access is not guaranteed. Setting must be made so that two areas are not accessed at the same time by a single word or longword access.

(6) Restrictions on RMPA and String-Manipulation Instructions

- Although the external space has a per-area ending-switching facility (only for data), the allocation of data to be handled by RMPA or string-manipulation instructions to an area where the endian differs from that of the chip is prohibited, and operation is not guaranteed if this restriction is not observed. If data to be handled by RMPA or string-manipulation instructions are allocated to the external space, they must be allocated to areas where the endian setting is the same as that for the chip.
- The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(7) Restriction on Instruction Code

When the endian setting for each area is different from that for the chip, no instruction code can be allocated in the area. The instruction code should be allocated to the external space whose endian setting is the same as that for the chip.

16.6 Bus Error Monitoring Section

The bus error monitoring section monitors the individual areas for bus errors, and when a bus error occurs, the error is indicated to the bus master.

16.6.1 Types of Bus Error

There are two types of bus error: illegal address access and timeout.
Illegal address access is the detection of illegal access to an area, and time-out is the detection of a bus-access operation not being completed within 768 cycles.

16.6.1.1 Illegal Address Access

When the illegal address access detection enable bit (IGAEN) in the bus error monitoring enable register (BEREN) is set to 1, access of the following types leads to illegal address access errors.

- Access to areas of external space for which operation has been disabled (CSnCR.EXENB = 0)
- With respect to areas other than those described above, access to illegal address ranges
  The address ranges where access will lead to illegal address access errors are indicated in Table 16.11.

16.6.1.2 Timeout

When the timeout detection enable bit (TOEN) in the bus error monitoring enable register (BEREN) is set to 1, bus access that is not completed within 768 cycles leads to a timeout error.

- CS areas (CS0 to CS3): Bus access is not completed (the WAIT# signal is not negated) within 768 external bus clock (BCLK) cycles from the start of the access.
  Once a timeout error occurs, accesses from the bus master are rejected for 256 BCLK cycles. If multiple external bus accesses are generated with a single request from the bus master during the transfer, the bus accesses cannot be stopped by a timeout. At this time, timeout errors may occur repeatedly.
- Internal peripheral buses (2 and 3): Bus access is not completed within 768 peripheral module clock (PCLKB) cycles from the start of the access.
  Once a timeout error occurs, accesses from the bus master are rejected for 256 PCLKB cycles.
- Internal peripheral bus 4: Bus access is not completed within 768 peripheral module clock (PCLKA) cycles from the start of the access.
  Once a timeout error occurs, accesses from the bus master are rejected for 256 PCLKA cycles.
- Internal peripheral bus 6: Bus access is not completed within 768 FlashIF clock (FCLK) cycles from the start of the access.
  Once a timeout error occurs, accesses from the bus master are rejected for 256 FCLK cycles.

16.6.2 Operations When a Bus Error Occurs

When a bus error occurs, the error is indicated to the CPU. Operation is not guaranteed when a bus error occurs.

- Bus error indication to the CPU
  An interrupt is generated. The IERn register in the ICU can specify whether to generate an interrupt in the case of a bus error.

16.6.3 Conditions Leading to Bus Errors

Table 16.11 lists the types of bus errors for each area in the respective address space.

If an illegal address access error or timeout is detected when no bus error has occurred (bus error status register n (BERSRn; n = 1 or 2) is cleared), the detected error is reflected on the BERSRn. Once a bus error occurs, no subsequent bus errors are reflected on the register unless the register is cleared.

If bus errors are simultaneously caused by two or more bus masters, error information of only one bus master is reflected. Once a bus error occurs, the status is retained until BERSRn is cleared.

Table 16.11 Types of Bus Errors

	Type of Area		Type of Error			
			Illegal Address Access		Timeout	
	On-chip ROM Mode		On-chip ROM Mode		On-chip ROM Mode	
Address	Enabled	Disabled	Enabled	Disabled	Enabled	Disabled
0000 0000h to 0007 FFFFh	Memory bus 1		—		—	
0008 0000h to 0008 7FFFh	Internal peripheral bus 1		—		—	
0008 8000h to 0009 FFFFh	Internal peripheral bus 2		Δ		—	
000A 0000h to 000B FFFFh	Internal peripheral bus 3		Δ		—	
000C 0000h to 000D FFFFh	Internal peripheral bus 4		Δ		—	
000E 0000h to 000F FFFFh	Reserved area		—		—	
0010 0000h to 00FF FFFFh	Internal peripheral bus 6	Reserved area	Δ	○	—	—
0100 0000h to 04FF FFFFh	Reserved area		○		—	
0500 0000h to 07FF FFFFh	External bus (CS1 to CS3)		[IA]		[TO]	
0800 0000h to 0FFF FFFFh	Reserved area		—		—	—
1000 0000h to 7FFF FFFFh	Reserved area		○		—	—
8000 0000h to FEFF FFFFh	Memory bus 2	Reserved area	—	○	—	—
FF00 0000h to FF7F FFFFh		External bus (CS0)	—	[IA]	—	[TO]
FF80 0000h to FFFF FFFFh			—		—	

—: A bus error does not result.

Δ: A bus error may or may not result.

○: A bus error results.

[IA]: Access to this area leads to detection of a bus error if operation for this area is disabled (CSnCR.EXENB = 0; n = 0 to 7).

[TO]: Bus access not being completed within 768 cycles leads to detection of a bus error.

Note: • The capacity of the on-chip RAM, DataFlash, and on-chip ROM differs depending on the product. For details, see section 40, RAM, section 41, Flash Memory.

17. Memory-Protection Unit (MPU)

17.1 Overview

The RX CPU incorporates a memory-protection unit that checks the addresses of CPU access to the overall address space (0000 0000h to FFFF FFFFh).

Access-control information can be set for up to eight regions, and permission for access to each region is in accord with this information. The default response to the detection of access to a region where permission has not been set is the generation of a memory-protection error.

The supported access-control information for the individual regions consists of permission to read, permission to write, and permission to execute. This access-control information is effective when the processor mode of the CPU is user mode. Memory protection is not applied when the CPU is in supervisor mode.

Table 17.1 lists the specifications of the memory-protection unit, and Figure 17.1 shows a block diagram of the memory-protection unit.

Table 17.1 Specifications of Memory Protection

Specifictaions	Description
Region to be covered by memory protection and processor mode	0000 0000h to FFFF FFFFh (in user mode) No memory protection in supervisor mode
Number of regions	8
Page size (smallest unit of protection)	16 bytes
Specifying addresses of individual regions	Setting the page numbers where regions start and end
Setting to make memory protection effective or ineffective in individual regions	A V (valid) bit in each region-n end page number register (REPAGEn) makes the settings effective or ineffective for the corresponding region (n = 0 to 7).
Access-control information settings for individual regions	Instruction execution: Permission to execute Operand access: Permission to read, permission to write
Start of memory-protection operations	After the memory-protection unit has been enabled, access monitoring start-ing up with the transition to user mode.
Memory-protection error processing	Generation of access exceptions
Addresses where memory-protection errors are generated	Address in instruction execution: The PC value is preserved on the stack. Address in operand access: The address is stored in the data memory-protection error address register (MPDEA).
Determining the reasons for memory-protection errors	The memory-protection error status register (MPESTS) holds indicators of the reason.
Background region setting	Access-control information can be set for the background region (the whole address space).
Processing where regions overlap	The access-control information for access to an overlap between regions is the logical OR of the attributes for the given regions, and permission is given priority.

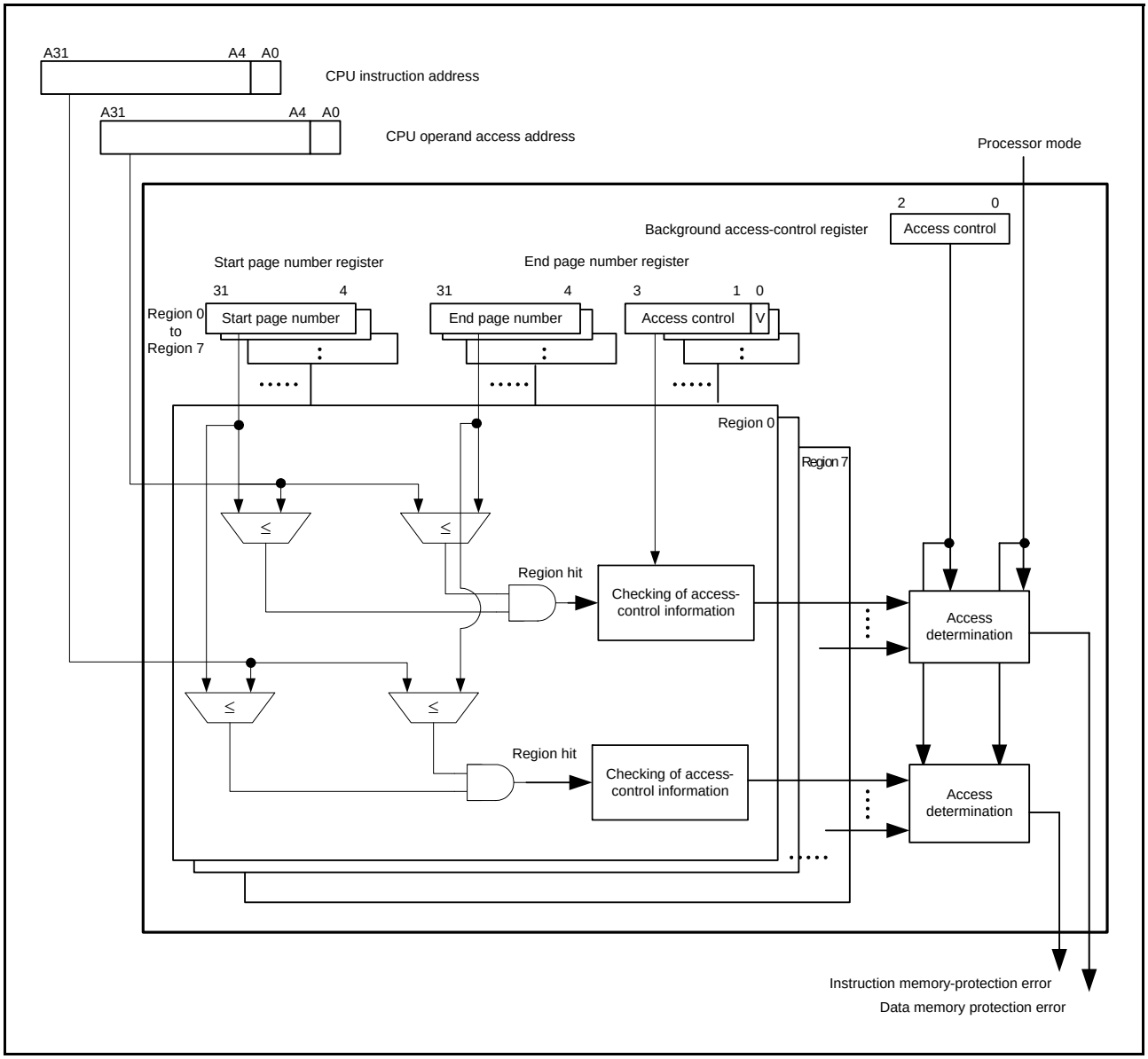


Figure 17.1 Block Diagram of the Memory-Protection Unit

17.1.1 Types of Access Control

There are three types of access control information: permission for instruction execution, permission to read operands, and permission to write operands. Violations of these types of access control are only detected when programs are running in user mode. Violations are not detected when programs are running in supervisor mode.

17.1.2 Regions for Access Control

Up to eight regions for access control are definable. Settings of the range of memory for each access-control region are made in the corresponding region-n start page number register (RSPAGEn) and region-n end page number register (REPAGEn), where n = 0 to 7.
The minimum unit for control of access is the “page”, by which the address space is divided into 16-byte units. The 28 higher-order bits ([31:4]) of the address [31:0] bits correspond to the page number.
The REPAGEn register specifies the access-control information for each area and whether the area is enabled or not.

17.1.3 Background Region

“Background region” refers to the whole address space (0000 0000h to FFFF FFFFh). Access-control information for the background region is set in the background-region access-control register (MPBAC). In contrast to the access-control information for the eight individual regions, protection information for the background region is effective as long as memory protection is enabled (the MPEN bit in the MPEN register is 1).

17.1.4 Overlap between Regions

In cases of overlap between multiple regions, the access-control information becomes the logical OR of the access-control bits for the overlapping regions (including the background region), with permission given priority.

17.1.5 Instructions and Data that Span Regions

Operations in response to the detection of memory-protection errors when instructions or data span regions for which different access-control settings have been made are undefined. Ensure that instructions and data do not span regions for which different access-control settings have been made.

17.2 Register Descriptions

17.2.1 Region-n Start Page Number Register (RSPAGEn) (n = 0 to 7)

Addresses: RSPAGE0 0008 6400h, RSPAGE1 0008 6408h, RSPAGE2 0008 6410h, RSPAGE3 0008 6418h
RSPAGE4 0008 6420h, RSPAGE5 0008 6428h, RSPAGE6 0008 6430h, RSPAGE7 0008 6438h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RSPN[27:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSPN[27:0]												—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b31 to b4	RSPN[27:0]	Region-Start Page Number	Page number where the region starts, for use in region determination	R/W

RSPN[27:0] Bits (Region-Start Page Number)

These bits specify the page number where the region starts.

17.2.2 Region-n End Page Number Register (REPAGEn) (n = 0 to 7)

Addresses: REPAGE0 0008 6404h, REPAGE1 0008 640Ch, REPAGE2 0008 6414h, REPAGE3 0008 641Ch
REPAGE4 0008 6424h, REPAGE5 0008 642Ch, REPAGE6 0008 6434h, REPAGE7 0008 643Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	REPN[27:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REPN[27:0]												UAC[2:0]			V
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b0	V	Valid Bit	0: Region setting invalid 1: Region setting valid	R/W
b3 to b1	UAC[2:0]	Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R/W
b31 to b4	REPN[27:0]	Region-End Page Number	Page number where the region ends, for use in region determination	R/W

V Bit (Valid Bit)

This bit enables or disables the settings for the corresponding region.
This bit is cleared to 0 when the region invalidation operation register (MPOPI) invalidates all access-controlled areas.

UAC[2:0] Bits (Access Control Bits in User Mode)

These bits specify the access control in user mode.

REPN[27:0] Bits (Region-End Page Number)

These bits specify the page number where the region ends.
Specify a value that is greater than or equal to the page number where the corresponding region starts. The page specified by the region-end page number is part of the target region for memory protection.

17.2.3 Memory-Protection Enable Register (MPEN)

Address: 0008 6500h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MPEN	Memory-Protection Enable	1: The memory protection is enabled. 0: The memory protection is disabled.	R/W
b31 to b1	—	Reserved	The read value is 0. The write value should always be 0	R/W

MPEN Bit (Memory-Protection Enable)

This bit enables or disables the memory protection.

After 1 has been written to this bit, address checking for memory protection by the CPU starts on the execution of a branch instruction (RTE and RTFI) that shifts operation to the user mode.

17.2.4 Background Access Control Register (MPBAC)

Address: 0008 6504h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UBAC[2:0]			—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b3 to b1	UBAC[2:0]	Background Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R/W
b31 to b4	—	Reserved	The read value is 0. The write value should always be 0.	R/W

UBAC[2:0] Bits (Background Access Control Bits in User Mode)

These bits specify the background access control in user mode.

17.2.5 Memory-Protection Error Status-Clearing Register (MPECLR)

Address: 0008 6508h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLR	Error Status-Clearing	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: The DRW, DA, and IA bits in the MPESTS are cleared to 0.	R/W
b31 to b1	—	Reserved	The read value is 0. The write value should always be 0.	R/W

CLR Bit (Error Status-Clearing)

This bit clears the data read/write bit (DRW), the data memory-protection error generated bit (DA), and the instruction memory-protection error generated bit (IA) in the memory-protection error status register (MPESTS) to 0.

17.2.6 Memory-Protection Error Status Register (MPESTS)

Address: 0008 650Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRW	DA	IA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IA	Instruction Memory-Protection Error Generated Bit	0: No instruction memory-protection error was generated. 1: Instruction memory-protection error was generated.	R
b1	DA	Data Memory-Protection Error Generated Bit	0: No data memory-protection error was generated. 1: Data memory-protection error was generated.	R
b2	DRW	Data Read/Write Bit	0: Data were read. 1: Data were written.	R
b31 to b3	—	Reserved	The read value is 0. The write value should always be 0.	R/W

IA Bit (Instruction Memory-Protection Error Generated Bit)

This bit indicates the state of memory-protection error generation by instruction execution.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

DA Bit (Data Memory-Protection Error Generated Bit)

This bit indicates the state of memory-protection error generation by operand access.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

DRW Bit (Data Read/Write Bit)

For a memory-protection error produced by operand access, this bit indicates the read/write attribute of the access operation. This bit is only valid when the data memory-protection error generated bit (DA) is 1.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

17.2.7 Data Memory-Protection Error Address Register (MPDEA)

Address: 0008 6514h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DEA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b31 to b0	DEA[31:0]	Data Memory-Protection Error Address	Data memory-protection error address	R

DEA[31:0] Bits (Data Memory-Protection Error Address)

These bits retain the address for which operand access generated a memory-protection error.

17.2.8 Region Search Address Register (MPSA)

Address: 0008 6520h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b31 to b0	SA[31:0]	Region Search Address	Address for region searching	R/W

SA[31:0] Bits (Region Search Address)

These bits specify the address for use in comparison with region-start addresses in the region-n start page number registers (RSPAGEn) and region-end addresses in the region-n end page number registers (REPAGEn).

17.2.9 Region Search Operation Register (MPOPS)

Address: 0008 6524h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	S
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	S	Region Search Operation	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: A region-search operation proceeds.	R/W
b15 to b1	—	Reserved	The read value is 0. The write value should always be 0.	R/W

S Bit (Region Search Operation)

Setting this bit to 1 makes the memory-protection unit perform a region-search operation. The address specified in the region search address register (MPSA) is compared with the address information for individual regions to search for a hitting region.

The result of searching is stored in the data-hit region bits (HITD[7:0]) of the data-hit region register (MHITD). Moreover, the logical OR of the respective access control bits for hitting regions is stored in the data-hit region access control bits (UHACD[2:0]) in user mode.

17.2.10 Region Invalidation Operation Register (MPOPI)

Address: 0008 6526h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INV	Region Invalidate Start	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: All access-controlled areas are invalidated.	R/W
b15 to b1	—	Reserved	The read value is 0. The write value should always be 0.	R/W

INV Bit (Region Invalidate Start)

Setting this bit to 1 clears the valid (V) bits in all of the region-n end page number registers (REPAGEn) to 0. After a V bit is cleared to 0, all settings other than background access-control settings are invalid.

17.2.11 Instruction-Hit Region Register (MHITI)

Address: 0008 6528h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	HITI[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UHACI[2:0]			—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b3 to b1	UHACI[2:0]	Instruction-Hit Region Access Control Bits in User Mode	b3 0: Reading prohibited 1: Read permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution is permitted.	R
b15 to b4	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b23 to b16	HITI[7:0]	Instruction-Hit Region	When the instruction memory-protection error generated (IA) bit in the MPESTS = 1, [b23:b16] = 0000 0000b indicates that attempted access to the background region led to an instruction memory-protection error. Other than above b23 0: Instruction memory-protection error was not generated in region 7. 1: Instruction memory-protection error was generated in region 7. b22 0: Instruction memory-protection error was not generated in region 6. 1: Instruction memory-protection error was generated in region 6. b21 0: Instruction memory-protection error was not generated in region 5. 1: Instruction memory-protection error was generated in region 5. b20 0: Instruction memory-protection error was not generated in region 4. 1: Instruction memory-protection error was generated in region 4. b19 0: Instruction memory-protection error was not generated in region 3. 1: Instruction memory-protection error was generated in region 3. b18 0: Instruction memory-protection error was not generated in region 2. 1: Instruction memory-protection error was generated in region 2. b17 0: Instruction memory-protection error was not generated in region 1. 1: Instruction memory-protection error was generated in region 1. b16 0: Instruction memory-protection error was not generated in region 0. 1: Instruction memory-protection error was generated in region 0.	R
b31 to b24	—	Reserved	The read value is 0. The write value should always be 0.	R/W

UHACI[2:0] Bits (Instruction-Hit Region Access Control Bits in User Mode)

These bits hold the user-mode access control bits (REPAGEn.UAC[2:0]) for the region where the instruction memory-protection error was generated.

If the error was generated in an overlap between regions, the value stored here is the logical OR of the user-mode access control bits for the corresponding regions (including the background region).

HITI[7:0] Bits (Instruction-Hit Region)

These bits indicate the region where an instruction memory-protection error was generated. These bits are set to 0000 0000b in response to the generation of an instruction memory-protection error in the background region.

17.2.12 Data-Hit Region Register (MHITD)

Address: 0008 652Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	HITD[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UHACD[2:0]			—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b3 to b1	UHACD[2:0]	Data-Hit Region Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R
b15 to b4	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b23 to b16	HITD[7:0]	Data-Hit Region	When the data memory-protection error generated (DA) bit = 1, [b23:b16] = 0000 0000b indicates that attempted access to the background region led to a data memory-protection error. Other than above b23 0: Neither a data memory-protection error nor a search hit was generated in region 7. 1: A data memory-protection error or search hit was generated in region 7. b22 0: Neither a data memory-protection error nor a search hit was generated in region 6. 1: A data memory-protection error or search hit was generated in region 6. b21 0: Neither a data memory-protection error nor a search hit was generated in region 5. 1: A data memory-protection error or search hit was generated in region 5. b20 0: Neither a data memory-protection error nor a search hit was generated in region 4. 1: A data memory-protection error or search hit was generated in region 4. b19 0: Neither a data memory-protection error nor a search hit was generated in region 3. 1: A data memory-protection error or search hit was generated in region 3. b18 0: Neither a data memory-protection error nor a search hit was generated in region 2. 1: A data memory-protection error or search hit was generated in region 2. b17 0: Neither a data memory-protection error nor a search hit was generated in region 1. 1: A data memory-protection error or search hit was generated in region 1. b16 0: Neither a data memory-protection error nor a search hit was generated in region 0. 1: A data memory-protection error or search hit was generated in region 0.	R
b31 to b24	—	Reserved	The read value is 0. The write value should always be 0.	R/W

UHACD[2:0] Bits (Data-Hit Region Access Control Bits in User Mode)

These bits hold the user-mode access control bits (REPAGEn.UAC[2:0]) that have been set for the region where a data memory-protection error was generated or the region that produced a hit in region searching.
When an error is generated in an overlap between regions or a hit was generated in region searching, the value stored here is the logical OR of the user-mode access control bits for the corresponding regions (including the background region).

HITD[7:0] Bits (Data-Hit Region)

These bits indicate the region where a data memory-protection error was generated or the region that produced a hit in a region search. These bits are set to 0000 0000b for a data memory-protection error generated in the background region.

Note: When access to a register of memory protection unit in user mode generates a data memory-protection error, the value in this register is cleared to 0000 0000h.

17.3 Functions

17.3.1 Memory Protection

Memory protection means monitoring, in accord with the access-control information that has been set for the individual access-control regions and the background region, whether or not access by programs running in user mode violates the access-control settings. The memory-protection unit notifies the CPU of access-control violations (or memory-protection errors) when they are detected, causing the CPU to start access-exception processing.
Memory protection is enabled by setting the memory-protection enable (MPEN) bit in the memory-protection enable (MPEN) register to 1.
An instruction memory-protection error is generated on detection of an instruction-execution violation and a data memory-protection error is generated on detection of an operand-access reading or writing violation. Operand access that leads to a data memory-protection error is not actually executed.

17.3.2 Region Search

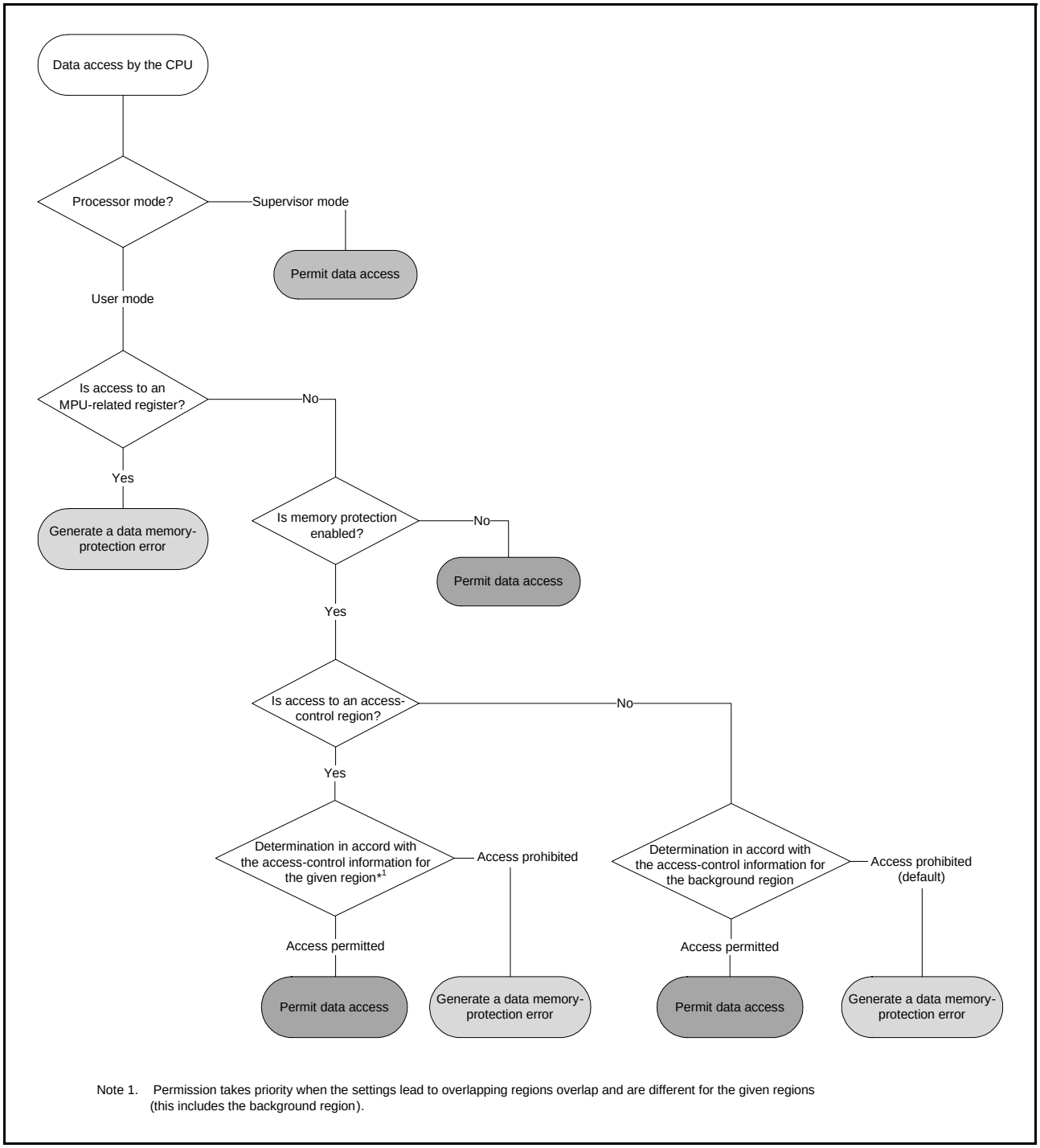
Region search means enquiry as to which of the eight specified access regions was “hit” and how the access-control information (permission to execute, to read, and to write) is set.
When the region search operation (S) bit in the region-search operation (MPOP) register is set to 1, the address specified in the region search address (MPSA) register is compared with the addresses for the individual regions. After a region search is executed, the data-hit region register (MHITD) indicates the logical OR of the access-control information for the region which was “hit” and for the other regions.

17.3.3 Protection of Registers Related to the Memory-Protection Unit

Registers related to the memory-protection unit are not accessible through means of access other than operand access by the CPU. Attempted access to registers related to the memory-protection unit in user mode through operand access by the CPU leads to a data memory-protection error regardless of whether or not memory protection is in effect at the given location.

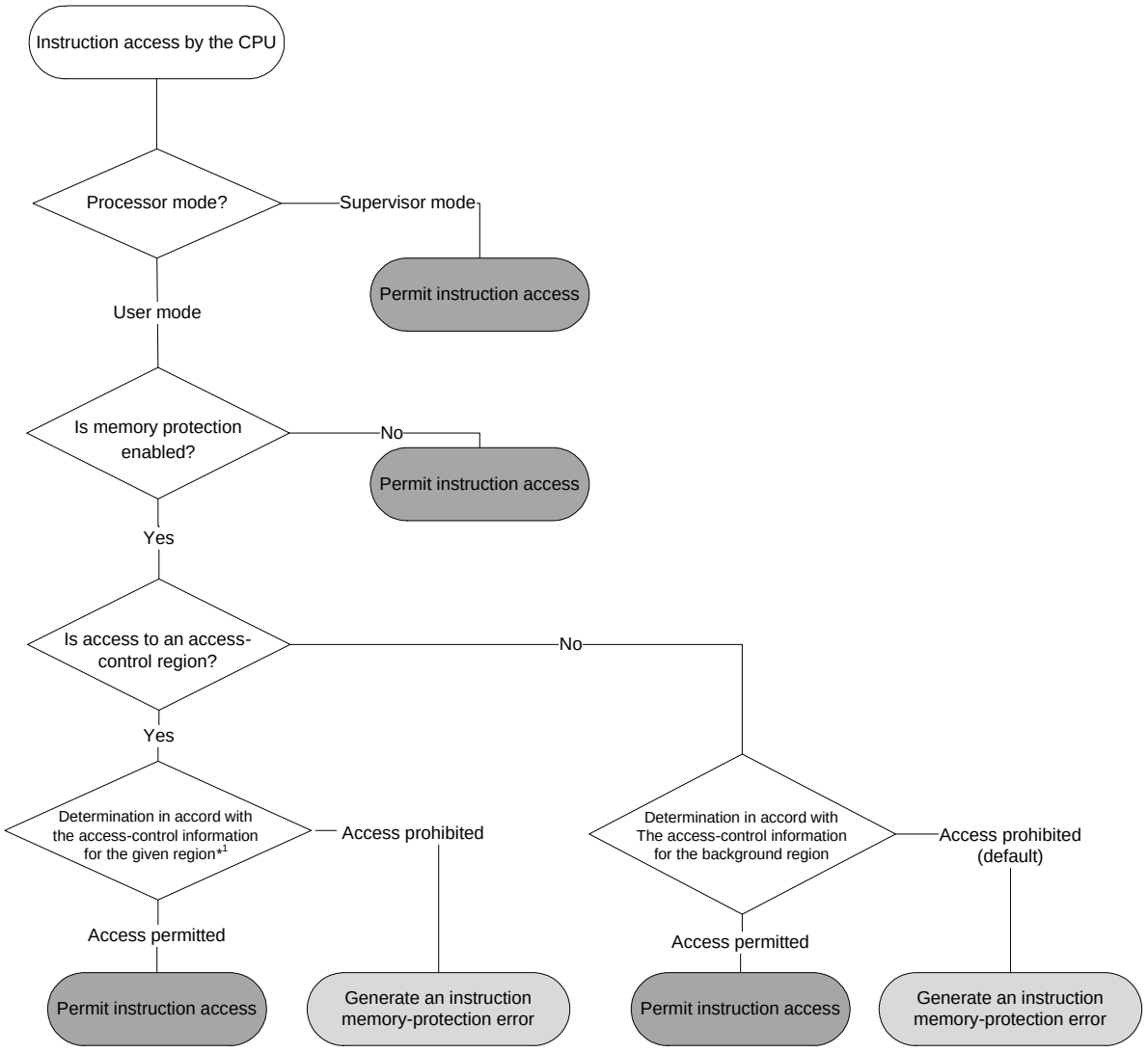
17.3.4 Flow for Determination of Access by the Memory-Protection Function

Figure 17.2 shows the flow of determination in the case of data access and Figure 17.3 shows the flow of determination in the case of instruction access.



Note 1. Permission takes priority when the settings lead to overlapping regions overlap and are different for the given regions (this includes the background region).

Figure 17.2 Flow of Determination for Data Access



Note 1. Permission takes priority when the settings lead to overlapping regions overlap and are not the same for the given regions (this includes the background region).

Figure 17.3 Flow of Determination for Instruction Access

17.4 Procedures for Using Memory Protection

17.4.1 Setting Access-Control Information

Access-control information for the various regions is set in supervisor mode.
Settings for up to eight access-control regions are made in the region-n start page number registers (RSPAGEn) and region-n end page number registers (REPAGEn), where n = 0 to 7.
Settings for the background access-control region are made in the background access-control register (MPBAC).

17.4.2 Enabling Memory Protection

Setting the memory-protection enable (MPEN) bit in the memory-protection enable (MPEN) register to 1 while operation is in supervisor mode enables memory protection.

17.4.3 Transition to User Mode

After updating the registers related to the memory-protection unit, be sure to read the registers for which writing was performed and check that the settings have been made as the final step before the transition to user mode.
Either of the methods below can be used for the transition from supervisor mode to user mode.

- Set the processor mode setting (PM) bit in the copy of the processor status word (PSW) saved in the stack area to 1 (the setting for user mode) and then execute an RTE instruction.
- Set the PM bit in the backup processor status word (BPSW) to 1 and then execute an RTFI instruction.

Note: Using an MVTC or POPC instruction to write to the PSW.PM bit is invalid. Use an RTE or RTFI instruction to update the value of the PSW.PM bit.

The memory-protection unit starts checking instruction-execution access and operand access by the CPU on the transition to user mode.

17.4.4 Processing in Response to Memory-Protection Errors

The CPU starts access-exception processing on detection of a violation of protection set up by the access-control information (i.e. a memory-protection error). For details on CPU operations in access-exception processing, refer to section 14., Exception Handling.
To determine whether an instruction memory-protection error or data memory-protection error has been generated, check the values of the instruction memory-protection error generated (IA) and data memory-protection error generated (DA) bits in the memory-protection error status (MPESTS) register from within the exception-processing routine.
After confirming the type of error, clear the memory-protection error status (MPESTS) register by writing 1 to the status clearing (CLR) bit in the memory-protection error status clearing (MPECLR) register.

(1) When a data memory-protection error is generated

Access-exception processing by the CPU saves the address of the instruction that led to the memory-protection error on the stack. Furthermore, the address of the operand for which access led to a memory-protection error is stored in the data memory-protection error address register (MPDEA) and the region information for the region where the memory-protection error was generated is stored in the data-hit region register (MHITD).

- Violations of access control in access to valid regions 0 to 7

The data-hit region bits (MHITD.HITD[7:0]) with the same region number as the region where the error occurred is set to 1. In user mode, the logical “or” of the region access-control information for the location where the error occurred is set in the data-hit region access-control bits (MHITD.UHACD[2:0]).

- Violations of access control for the background region, besides access to valid regions 0 to 7

The data-hit region bits (MHITD.HITD[7:0]) are set to 0000 0000b. In user mode, the access-control information for the background region is set in the data-hit region access-control bits (MHITD.UHACD[2:0]).

Referring to this information can pinpoint the sources of errors.

(2) When an instruction memory-protection error is generated

Access-exception processing by the CPU saves the address of the instruction that led to the memory-protection error on the stack. Furthermore, the region information for the region where the memory-protection error was generated is stored in the instruction-hit region register (MHITI).

- Violations of access control in access to valid regions 0 to 7

The instruction-hit region bit (MHITD.HITI[7:0]) with the same region number as the region where the error occurred is set to 1. In user mode, the logical “or” of the region access-control information for the location where the error occurred is set in the instruction-hit region access-control bits (MHITI.UHACI[2:0]).

- Violations of access control for the background region, besides access to valid regions 0 to 7

The instruction-hit region bits (MHITI.HITI[7:0]) are set to 0000 0000b. In user mode, the access-control information for the background region is set in the instruction-hit region access-control bits (MHITI.UHACI[2:0]).

Referring to this information can pinpoint the sources of errors.

18. DMA Controller (DMACA)

This MCU incorporates a 4-channel direct memory access controller (DMAC).
The DMAC is a module to transfer data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

18.1 Overview

Table 18.1 lists the specifications of the DMAC, and Figure 18.1 shows a block diagram of the DMAC.

Table 18.1 Specifications of DMAC

Item		Description
Number of channels		4 (DMACm (m = 0 to 3))
Transfer space		512 Mbytes (0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas)
Maximum transfer volume		1 Mbyte (Maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)
DMA request source		• Activation source selectable for each channel Software trigger Interrupt requests from peripheral modules or trigger input to external interrupt input pins*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: Highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024
	Block transfer mode	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Power consumption reduction function		Module-stop state can be set.

Note 1. For details on DMAC activation sources, see Table 15.3, Interrupt Vector Table in section 15, Interrupt controller (ICUb).

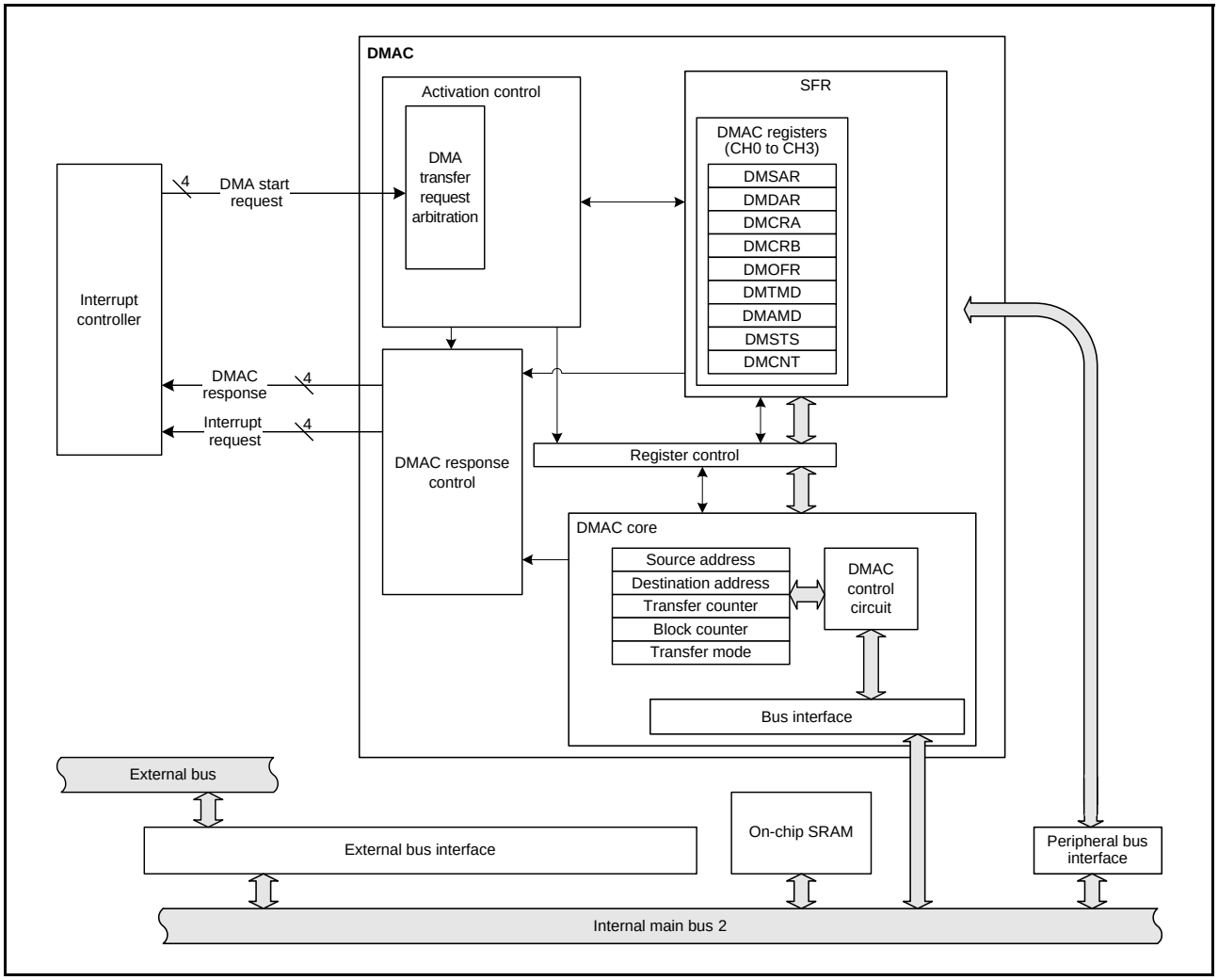


Figure 18.1 Block Diagram of DMAC

18.2 Register Descriptions

18.2.1 DMA Source Address Register (DMSAR)

Address(es): DMAC0.DMSAR 0008 2000h, DMAC1.DMSAR 0008 2040h
DMAC2.DMSAR 0008 2080h, DMAC3.DMSAR 0008 20C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting Range	R/W
b31 to b0	Specifies the transfer source start address.	0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	R/W

Set DMSAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).
Setting bits 31 to 29 is invalid; a value of bit 28 is extended to bits 31 to 29. Reading DMSAR returns the extended value.

18.2.2 DMA Destination Address Register (DMDAR)

Address(es): DMAC0.DMDAR 0008 2004h, DMAC1.DMDAR 0008 2044h
DMAC2.DMDAR 0008 2084h, DMAC3.DMDAR 0008 20C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

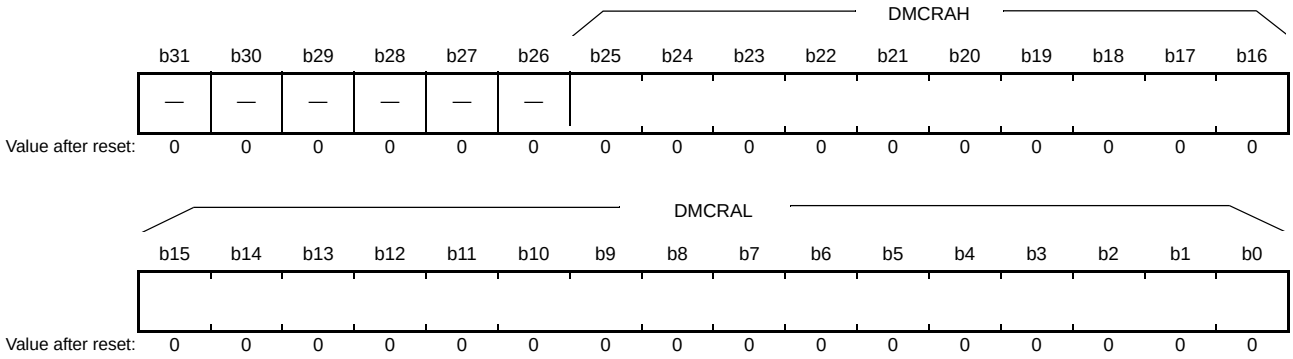
Bit	Description	Setting Range	R/W
b31 to b0	Specifies the transfer destination start address.	0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	R/W

Set DMDAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).
Setting bits 31 to 29 is invalid; a value of bit 28 is extended to bits 31 to 29. Reading DMDAR returns the extended value.

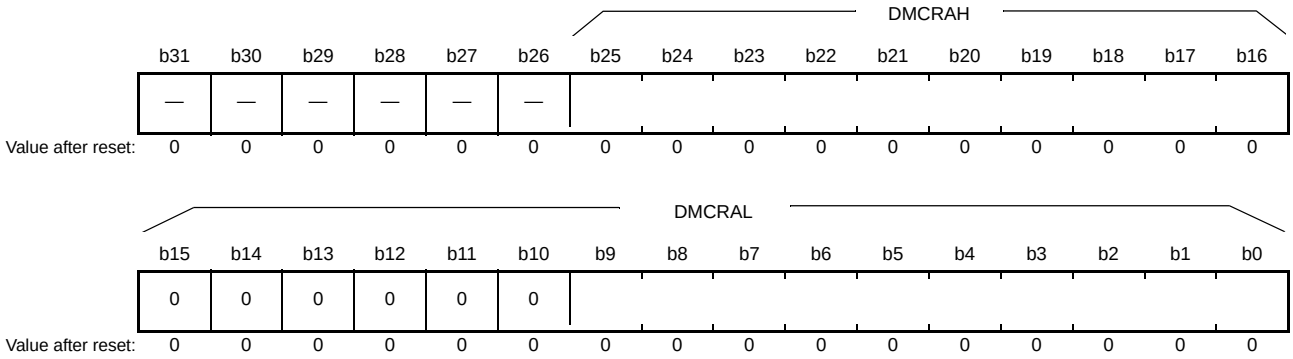
18.2.3 DMA Transfer Count Register (DMCRA)

Address(es): DMAC0.DMCRA 0008 2008h, DMAC1.DMCRA 0008 2048h
DMAC2.DMCRA 0008 2088h, DMAC3.DMCRA 0008 20C8h

- Normal transfer mode



- Repeat transfer mode, block transfer mode



Symbol	Bit Name	Description	R/W
DMCRAL	Lower bits of transfer count	Specifies the number of transfer operations	R/W
DMCRAH	Upper bits of transfer count		R/W

Note: • Set the same value for DMCRAH and DMCRAL in repeat transfer mode and block transfer mode.

(1) Normal Transfer Mode (MD[1:0] Bits in DMACm.DMTMD = 00b)

DMCRAL functions as a 16-bit transfer counter. The number of transfer operations is one when the setting is 0001h, and 65535 when it is FFFFh.

The value is decremented by one each time data is transferred.

When the setting is 0000h, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running mode).

DMCRAH is not used in normal transfer mode. Write 0000h to DMCRAH.

(2) Repeat Transfer Mode (MD[1:0] Bits in DMACm.DMTMD = 01b)

DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter.
The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In repeat transfer mode, a value in the range of 000h to 3FFh (1 to 1024) can be set for DMCRAH and DMCRAL.
Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.
The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which the value in DMCRAH is loaded into DMCRAL.

(3) Block Transfer Mode (MD[1:0] Bits in DMACm.DMTMD = 10b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.
The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In block transfer mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.
Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.
The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which the value in DMCRAH is loaded into DMCRAL.

18.2.4 DMA Block Transfer Count Register (DMCRB)

Address(es): DMAC0.DMCRB 0008 200Ch, DMAC1.DMCRB 0008 204Ch
DMAC2.DMCRB 0008 208Ch, DMAC3.DMCRB 0008 20CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting Range	R/W
b9 to b0	Specifies the number of block transfer operations or repeat transfer operations.	001h to 3FFh (1 to 1023) 000h (1024)	R/W
b15 to b10	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMCRB specifies the number of block transfer operations and repeat transfer operations in block and repeat transfer mode, respectively.
The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h.
In repeat transfer mode, the value is decremented by one when the final data of one repeat size is transferred.
In block transfer mode, the value is decremented by one when the final data of one block size is transferred.
In normal transfer mode, DMCRB is not used. The setting is invalid.

18.2.5 DMA Transfer Mode Register (DMTMD)

Address(es): DMAC0.DMTMD 0008 2010h, DMAC1.DMTMD 0008 2050h
DMAC2.DMTMD 0008 2090h, DMAC3.DMTMD 0008 20D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		DTS[1:0]		—	—	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DCTG[1:0]	DMA Request Source Select	b1 b0 0 0: Software 0 1: Interrupts*1 from peripheral modules or external interrupt input pins 1 0: Setting prohibited 1 1: Setting prohibited	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SZ[1:0]	Transfer Data Size Select	b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	DTS[1:0]	Repeat Area Select	b13 b12 0 0: The destination is specified as the repeat area or block area. 0 1: The source is specified as the repeat area or block area. 1 0: The repeat area or block area is not specified. 1 1: Setting prohibited	R/W
b15, b14	MD[1:0]	Transfer Mode Select	b15 b14 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Setting prohibited	R/W

Note 1. DMAC activation source is selected using the DMRSRm registers of the ICU. For details on DMAC activation sources, see Table 15.3, Interrupt Vector Table in section 15, Interrupt controller (ICUb).

DTS[1:0] Bits (Repeat Area Select)

DTS[1:0] select either the source or destination as the repeat area in repeat or block transfer mode. In normal transfer mode, setting these bits is invalid.

18.2.6 DMA Interrupt Setting Register (DMINT)

Address(es): DMAC0.DMINT 0008 2013h, DMAC1.DMINT 0008 2053h
DMAC2.DMINT 0008 2093h, DMAC3.DMINT 0008 20D3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable	0: Disables an interrupt request for an extended repeat area overflow on the destination address 1: Enables an interrupt request for an extended repeat area overflow on the destination address	R/W
b1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable	0: Disables an interrupt request for an extended repeat area overflow on the source address 1: Enables an interrupt request for an extended repeat area overflow on the source address	R/W
b2	RPTIE	Repeat Size End Interrupt Enable	0: Disables the repeat size end interrupt request. 1: Enables the repeat size end interrupt request.	R/W
b3	ESIE	Transfer Escape End Interrupt Enable	0: Disables the transfer escape end interrupt request. 1: Enables the transfer escape end interrupt request.	R/W
b4	DTIE	Transfer End Interrupt Enable	0: Disables the transfer end interrupt request. 1: Enables the transfer end interrupt request.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DARIE Bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the destination address occurs while this bit is set to 1, the DTE bit in DMCNT is cleared to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that an interrupt by an extended repeat area overflow on the destination address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DTE bit in DMACm.DMCNT of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the destination address, this bit is ignored.

SARIE Bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the source address occurs while this bit is set to 1, the DTE bit in DMCNT is cleared to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that an interrupt by an extended repeat area overflow on the source address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DTE bit in DMACm.DMCNT of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the source address, this bit is ignored.

RPTIE Bit (Repeat Size End Interrupt Enable)

When this bit is set to 1 in repeat transfer mode, the DTE bit in DMCNT is cleared to 0 after completion of a 1-repeat size data transfer. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (= repeat area or block area is not specified).

When this bit is set to 1 in block transfer mode, the DTE bit in DMCNT is cleared to 0 after completion of a 1-block data transfer in the same way as repeat transfer mode. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (= repeat area or block area is not specified).

ESIE Bit (Transfer Escape End Interrupt Enable)

This bit enables or disables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that are generated during DMA transfer.

The transfer escape end interrupt is generated when the ESIF flag in DMSTS is set to 1 with this bit set to 1. The transfer escape end interrupt is cleared by clearing this bit or the ESIF flag in DMSTS to 0.

DTIE Bit (Transfer End Interrupt Enable)

This bit enables or disables the transfer end interrupt request to be generated on completion of a specified number of data transfers.

The transfer end interrupt is generated when the DTIF bit in DMSTS is set to 1 with this bit set to 1. The transfer end interrupt is cleared by clearing this bit or the DTIF bit in DMSTS to 0.

18.2.7 DMA Address Mode Register (DMAMD)

Address(es): DMAC0.DMAMD 0008 2014h, DMAC1.DMAMD 0008 2054h
DMAC2.DMAMD 0008 2094h, DMAC3.DMAMD 0008 20D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SM[1:0]		—	SARA[4:0]					DM[1:0]		—	DARA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	DARA[4:0]	Destination Address Extended Repeat Area	Specifies the extended repeat area on the destination address. For details on the settings, see Table 18.2.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	DM[1:0]	Destination Address Update Mode	b7 b6 0 0: Destination address is fixed. 0 1: Offset addition*1 1 0: Destination address is incremented. 1 1: Destination address is decremented.	R/W
b12 to b8	SARA[4:0]	Source Address Extended Repeat Area	Specifies the extended repeat area on the source address. For details on the settings, see Table 18.2.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15, b14	SM[1:0]	Source Address Update Mode	b15 b14 0 0: Destination address is fixed. 0 1: Offset addition*1 1 0: Destination address is incremented. 1 1: Destination address is decremented.	R/W

Note 1. Offset addition can be specified only for DMAC0.

DARA[4:0] Bits (Destination Address Extended Repeat Area)

These bits specify the extended repeat area on the destination address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer destination, do not specify the extended repeat area on the destination address. When repeat transfer or block transfer is selected, or when DMACm.DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat area or block area), write 00000b in the DARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DARIE bit in DMINT set to 1. Table 18.2 lists the settings and the corresponding extended repeat areas.

DM[1:0] Bits (Destination Address Update Mode)

These bits select the mode of updating the destination address.

When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is decremented by 1, 2, and 4, respectively.

When offset addition is selected, the offset specified by the DMAC0.DMOFR register is added to the address.

Offset addition can be specified only for DMAC0.

SARA[4:0] Bits (Source Address Extended Repeat Area)

These bits specify the extended repeat area on the source address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer source, do not specify the extended repeat area on the source address. When repeat transfer or block transfer is selected, or when DMACm.DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat area or block area), write 00000b in the SARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the SARIE bit in DMINT set to 1. Table 18.2 lists the settings and the corresponding extended repeat areas.

SM Bit (Source Address Update Mode)

These bits select the mode of updating the source address.

When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is decremented by 1, 2, and 4, respectively.

When offset addition is selected, the offset specified by the DMAC0.DMOFR register is added to the address. Offset addition can be specified only for DMAC0.

Table 18.2 SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas

SARA4 to SARA0 or DARA4 to DARA0	Extended Repeat Area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 Kbyte specified as extended repeat area by the lower 10 bits of the address
01011b	2 Kbytes specified as extended repeat area by the lower 11 bits of the address
01100b	4 Kbytes specified as extended repeat area by the lower 12 bits of the address
01101b	8 Kbytes specified as extended repeat area by the lower 13 bits of the address
01110b	16 Kbytes specified as extended repeat area by the lower 14 bits of the address
01111b	32 Kbytes specified as extended repeat area by the lower 15 bits of the address
10000b	64 Kbytes specified as extended repeat area by the lower 16 bits of the address
10001b	128 Kbytes specified as extended repeat area by the lower 17 bits of the address
10010b	256 Kbytes specified as extended repeat area by the lower 18 bits of the address
10011b	512 Kbytes specified as extended repeat area by the lower 19 bits of the address
10100b	1 Mbyte specified as extended repeat area by the lower 20 bits of the address
10101b	2 Mbytes specified as extended repeat area by the lower 21 bits of the address
10110b	4 Mbytes specified as extended repeat area by the lower 22 bits of the address
10111b	8 Mbytes specified as extended repeat area by the lower 23 bits of the address
11000b	16 Mbytes specified as extended repeat area by the lower 24 bits of the address
11001b	32 Mbytes specified as extended repeat area by the lower 25 bits of the address
11010b	64 Mbytes specified as extended repeat area by the lower 26 bits of the address
11011b	128 Mbytes specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited.

18.2.8 DMA Offset Register (DMOFR)

Address(es): DMAC0.DMOFR 0008 2018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting Range	R/W
b31 to b0	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination.	0000 0000h to 00FF FFFFh (0 bytes to (16 M – 1) bytes) FF00 0000h to FFFF FFFFh (–16 Mbytes to –1 byte)	R/W

Write to this register while the DMAC operation is stopped or DMA transfer is disabled (not during data transfer). Setting bits 31 to 25 is invalid; a value of bit 24 is extended to bits 31 to 25. Reading DMOFR returns the extended value.

18.2.9 DMA Transfer Enable Register (DMCNT)

Address(es): DMAC0.DMCNT 0008 201Ch, DMAC1.DMCNT 0008 205Ch
DMAC2.DMCNT 0008 209Ch, DMAC3.DMCNT 0008 20DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DTE	DMA Transfer Enable	0: Disables DMA transfer. 1: Enables DMA transfer.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTE Bit (DMA Transfer Enable)

When the DMST bit in DMAST is set to 1 (DMAC activation is enabled) and this bit is set to 1 (DMA transfer is enabled), DMA transfer can be started for the corresponding channel.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When 0 is written to this bit.
- When the specified total volume of data transfer is completed.
- When DMA transfer is stopped by the repeat size end interrupt.
- When DMA transfer is stopped by the extended repeat area overflow interrupt.

18.2.10 DMA Software Start Register (DMREQ)

Address(es): DMAC0.DMREQ 0008 201Dh, DMAC1.DMREQ 0008 205Dh
DMAC2.DMREQ 0008 209Dh, DMAC3.DMREQ 0008 20DDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CLRS	—	—	—	SWREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWREQ	DMA Software Start	0: DMA transfer is not requested. 1: DMA transfer is requested.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	CLRS	DMA Software Start Bit Auto Clear Select	0: SWREQ bit is cleared after DMA transfer is started by software. 1: SWREQ bit is not cleared after DMA transfer is started by software.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SWREQ Bit (DMA Software Start)

When 1 is written to this bit, a DMA transfer request is generated. After DMA transfer is started in response to the request, this bit is cleared to 0 if the CLRS bit is set to 0. This bit is not cleared to 0 while the CLRS bit is set to 1. In this case, a DMA transfer request can be issued again after completion of a transfer.
Note that, however, setting this bit is valid and DMA transfer by software is enabled only when the DCTG[1:0] bits in DMTMD are set to 00b (DMA activation source is software).
Setting this bit is invalid when the DCTG[1:0] bits in DMTMD are set to a value other than 00b.
To start DMA transfer by software with the CLRS bit being 0, ensure that the SWREQ bit is 0, and then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started while the CLRS bit is set to 0 (the SWREQ bit is cleared after DMA transfer is started by software).
- When 0 is written to this bit.

CLRS Bit (DMA Software Start Bit Auto Clear Select)

This bit specifies whether to clear the SWREQ bit to 0 after DMA transfer is started in response to the DMA transfer request generated by setting the SWREQ bit to 1. With this bit set to 0, the SWREQ bit is cleared to 0 after DMA transfer is started. With this bit set to 1, the SWREQ bit is not cleared to 0. In this case, a DMA transfer request can be issued again after completion of a transfer.

18.2.11 DMA Status Register (DMSTS)

Address(es): DMAC0.DMSTS 0008 201Eh, DMAC1.DMSTS 0008 205Eh
DMAC2.DMSTS 0008 209Eh, DMAC3.DMSTS 0008 20DEh

	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ESIF	Transfer Escape End Interrupt Flag	0: A transfer escape end interrupt has not been generated. 1: A transfer escape end interrupt has been generated.	R/W*1
b3 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b4	DTIF	Transfer End Interrupt Flag	0: A transfer end interrupt has not been generated. 1: A transfer end interrupt has been generated.	R/W*1
b6, b5	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	ACT	DMA Active Flag	0: DMAC operation is suspended. 1: DMAC is operating.	R

Note 1. Only 0 can be written to clear the flag.

ESIF Flag (Transfer Escape End Interrupt Flag)

This flag indicates that the transfer escape end interrupt has been generated.

[Setting conditions]

- When 1-repeat size data transfer is completed in repeat transfer mode with the RPTIE bit in DMINT set to 1.
- When 1-block data transfer is completed in block transfer mode with the RPTIE bit in DMINT set to 1.
- When an extended repeat area overflow on the source address occurs while the SARIE bit in DMINT is set to 1 and the SARA[4:0] bits in DMAMD are set to a value other than 00000b (extended repeat area is specified on the transfer source address)
- When an extended repeat area overflow on the destination address occurs while the DARIE bit in DMINT is set to 1 and the DARA[4:0] bits in DMAMD are set to a value other than 00000b (extended repeat area is specified on the transfer destination address)

[Clearing conditions]

- When 0 is written to this bit.
- When 1 is written to the DTE bit in DMCNT.

DTIF Flag (Transfer End Interrupt Flag)

This flag indicates that the transfer end interrupt has been generated.

[Setting conditions]

- When the specified number of unit-transfers are completed in normal transfer mode (the value of DMCRAL becoming 0 on completion of transfer)
- When the specified number of repeat transfer operations are completed in repeat transfer mode (the value of DMCRB becoming 0 on completion of transfer))
- When the specified number of blocks have been transferred in block transfer mode (the value of DMCRB becoming 0 on completion of transfer)

[Clearing conditions]

- When 0 is written to this bit
- When 1 is written to the DTE bit in DMCNT

ACT Flag (DMA Active Flag)

This flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts data transfer operation

[Clearing condition]

- When data transfer in response to one transfer request is completed

18.2.12 DMA Activation Source Flag Control Register (DMCSL)

Address(es): DMAC0.DMCSL 0008 201Fh, DMAC1.DMCSL 0008 205Fh
DMAC2.DMCSL 0008 209Fh, DMAC3.DMCSL 0008 20DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DISEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DISEL	Interrupt Select	0: At the beginning of transfer, clear the interrupt flag of the activation source to 0. 1: At the end of transfer, the interrupt flag of the activation source issues an interrupt to the CPU.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DISEL Bit (Interrupt Select)

This bit selects whether the interrupt flag of the activation source of the DMAC is cleared to 0 or issues an interrupt to the CPU, at the beginning of transfer.

When DMTMD.DCTG[1:0] = 00b (activation by software), the setting of the DISEL bit does not affect the operation.

18.2.13 DMACA Module Activation Register (DMAST)

Address(es): 0008 2200h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DMST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DMST	DMAC Operation Enable	0: DMAC activation is disabled. 1: DMAC activation is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMST Bit (DMAC Operation Enable)

When this bit is set to 1, DMAC activation is enabled for all channels.

When 1 is written to the DMACm.DMCNT.DTE bit (DMA transfer is enabled) of multiple channels and then this bit is set to 1 (DMAC activation is enabled), the corresponding multiple channels can be placed in the transfer request acceptable state at the same time.

When the DMST bit is cleared to 0 during DMA transfer, DMA transfer is suspended after completion of the current data transfer corresponding to a single transfer request. DMA transfer is resumed by setting the DMST bit to 1 again.

[Setting condition]

- When 1 is written to this bit

[Clearing condition]

- When 0 is written to this bit

18.3 Operation

18.3.1 Transfer Mode

(1) Normal Transfer Mode

In normal transfer mode, one data is transferred by one transfer request. A maximum of 65535 can be set as the number of transfer operations using the DMCRAL of DMACm. When these bits are set to 0000h, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running mode). Setting DMCRB of DMACm is invalid in normal transfer mode. Except in free running mode, a transfer end interrupt request can be generated after completion of the specified number of transfer operations.
Table 18.3 summarizes the register update operation in normal transfer mode, and Figure 18.2 shows the operation in normal transfer mode.

Table 18.3 Register Update Operation in Normal Transfer Mode

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request
DMACm.DMSAR	Transfer source address	Increment/decrement/fixed/offset addition*1
DMACm.DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition*1
DMACm.DMCRAL	Transfer count	Decremented by one/not updated (in free running mode)
DMACm.DMCRAH	—	Not updated (Not used in normal transfer mode)
DMACm.DMCRB	—	Not updated (Not used in normal transfer mode)

Note 1. Offset addition can be specified only for DMAC0.

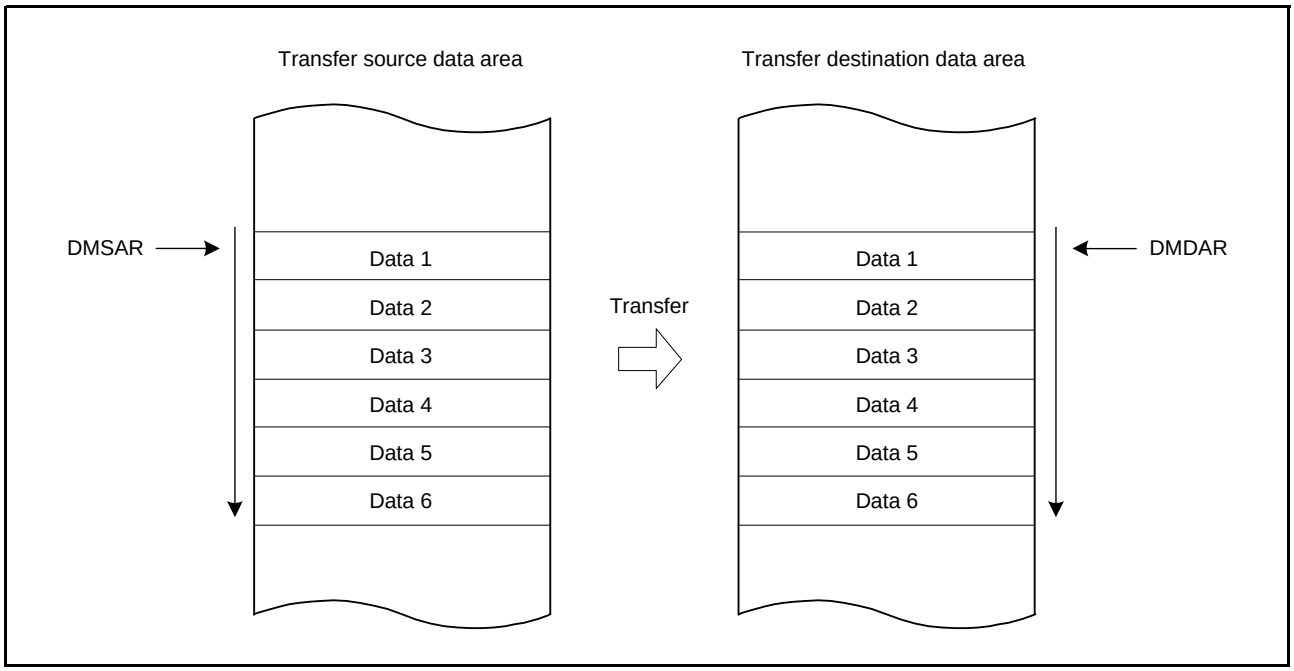


Figure 18.2 Operation in Normal Transfer Mode

(2) Repeat Transfer Mode

In repeat transfer mode, one data is transferred by one transfer request.
A maximum of 1K data can be set as a total repeat transfer size using DMCRA of the DMACm.
A maximum of 1K can be set as the number of repeat transfer operations using DMCRB of the DMACm; therefore, a maximum of 1M data (1K data × 1K count of repeat transfer operations) can be set as a total data transfer size.
Either the transfer source or transfer destination can be specified as a repeat area. When transfer of the repeat size data is completed, the address of the specified repeat area (DMSAR or DMDAR of the DMACm) returns to the transfer start address. When data of the specified repeat size has all been transferred in repeat transfer mode, DMA transfer can be stopped and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm in the repeat size end interrupt handling.
A transfer end interrupt request can be generated after completion of the specified number of repeat transfer operations.
Table 18.4 summarizes the register update operation in repeat transfer mode, and Figure 18.3 shows the operation in repeat transfer mode.

Table 18.4 Register Update Operation in Repeat Transfer Mode

		Update Operation after Completion of a Transfer by One Transfer Request	
Register	**Function**	**When DMACm.DMCRAL is not 1**	**When DMACm.DMCRAL is 1 (Transfer of the Last Data in Repeat Size)**
DMACm.DMSAR	Transfer source address	Increment/decrement/fixed/offset addition*1	• DMACm.DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition*1 • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition*1
DMACm.DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition*1	• DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition*1 • DMACm.DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition*1
DMACm.DMCRAH	Repeat size	Not updated	Not updated
DMACm.DMCRAL	Transfer count	Decremented by one	DMACm.DMCRAH
DMACm.DMCRB	Count of repeat transfer operations	Not updated	Decremented by one

Note 1. Offset addition can be specified only for DMAC0.

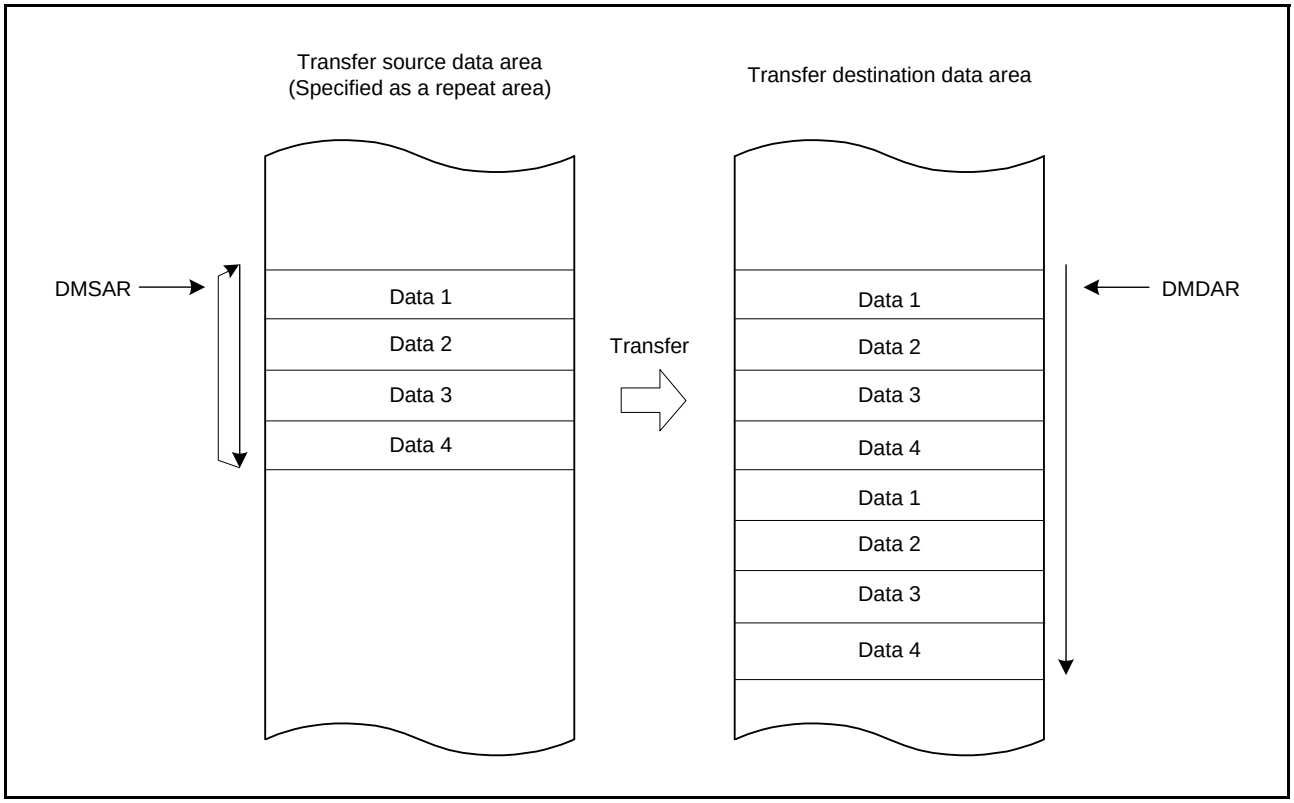


Figure 18.3 Operation in Repeat Transfer Mode

(3) Block Transfer Mode

In block transfer mode, a single block data is transferred by one transfer request.
A maximum of 1K data can be set as a total block transfer size using DMCRA of the DMACm.
A maximum of 1K can be set as the number of block transfer operations using DMCRB of the DMACm; therefore, a maximum of 1M data (1K data × 1K count of block transfer operations) can be set as a total data transfer size.
Either the transfer source or transfer destination can be specified as a block area. When transfer of a single block data is completed, the address of the specified block area (DMSAR or DMDAR of the DMACm) returns to the transfer start address. When a single block data has all been transferred in block transfer mode, DMA transfer can be stopped and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm in the repeat size end interrupt handling.
Transfer end interrupt request can be generated after completion of the specified number of block transfer operations.
Table 18.5 summarizes the register update operation in block transfer mode, and Figure 18.4 shows the operation in block transfer mode.

Table 18.5 Register Update Operation in Block Transfer Mode

Register	Function	Update Operation after Completion of Single-Block Transfer by One Transfer Request
DMACm.DMSAR	Transfer source address	• DMACm.DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition*1 • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition*1
DMACm.DMDAR	Transfer destination address	• DMACm.DMTMD.DTS[1:0] = 00 b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01 b Increment/decrement/fixed/offset addition*1 • DMACm.DMTMD.DTS[1:0] = 10 b Increment/decrement/fixed/offset addition*1
DMACm.DMCRAH	Block size	Not updated
DMACm.DMCRAL	Transfer count	DMACm.DMCRAH
DMACm.DMCRB	Count of block transfer operations	Decremented by one

Note 1. Offset addition can be specified only for DMAC0.

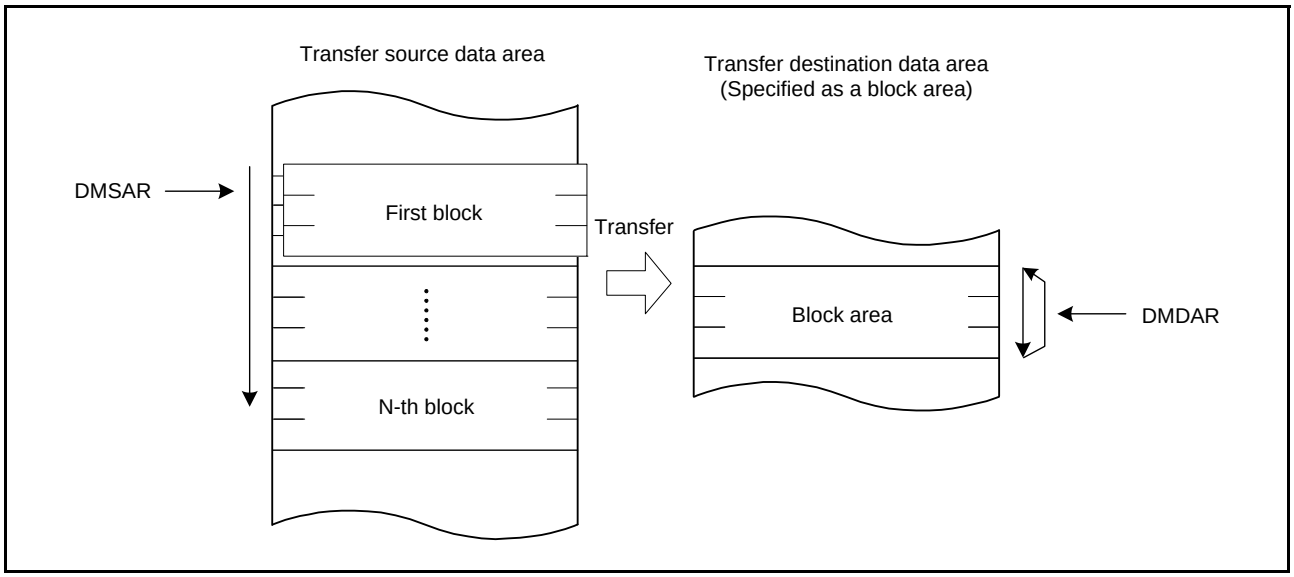


Figure 18.4 Operation in Block Transfer Mode

18.3.2 Extended Repeat Area Function

The DMAC supports a function to specify the extended repeat areas on the transfer source and destination addresses. With the extended repeat areas set, the address registers repeatedly indicate the addresses of the specified extended repeat areas.

The extended repeat areas can be specified separately to the transfer source address register (DMSAR) and transfer destination address register (DMDAR) of DMACm.

The extended repeat area on the source address is specified by the SARA[4:0] bits in DMAMD of DMACm. The extended repeat area on the destination address is specified by the DARA[4:0] bits in DMAMD of DMACm. The size can be specified separately for the source and destination sides.

However, the area (of transfer source or transfer destination) which is specified as the repeat area or block area should not be specified as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an interrupt by an extended repeat area overflow can be requested. When an overflow occurs in the extended repeat area on the transfer source while the SARIE bit in DMINT of DMACm is set to 1, the ESIF flag in DMSTS of DMACm is set to 1 and the DTE bit in DMCNT of DMACm is cleared to 0 to stop DMA transfer. At this time, if the ESIE bit in DMINT of DMACm is set to 1, an interrupt by an extended repeat area overflow is requested. When the DARIE bit in DMINT of DMACm is set to 1, the destination address register becomes a target to apply the function. DMA transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm in the interrupt handling.

Figure 18.5 shows an example of the extended repeat area operation.

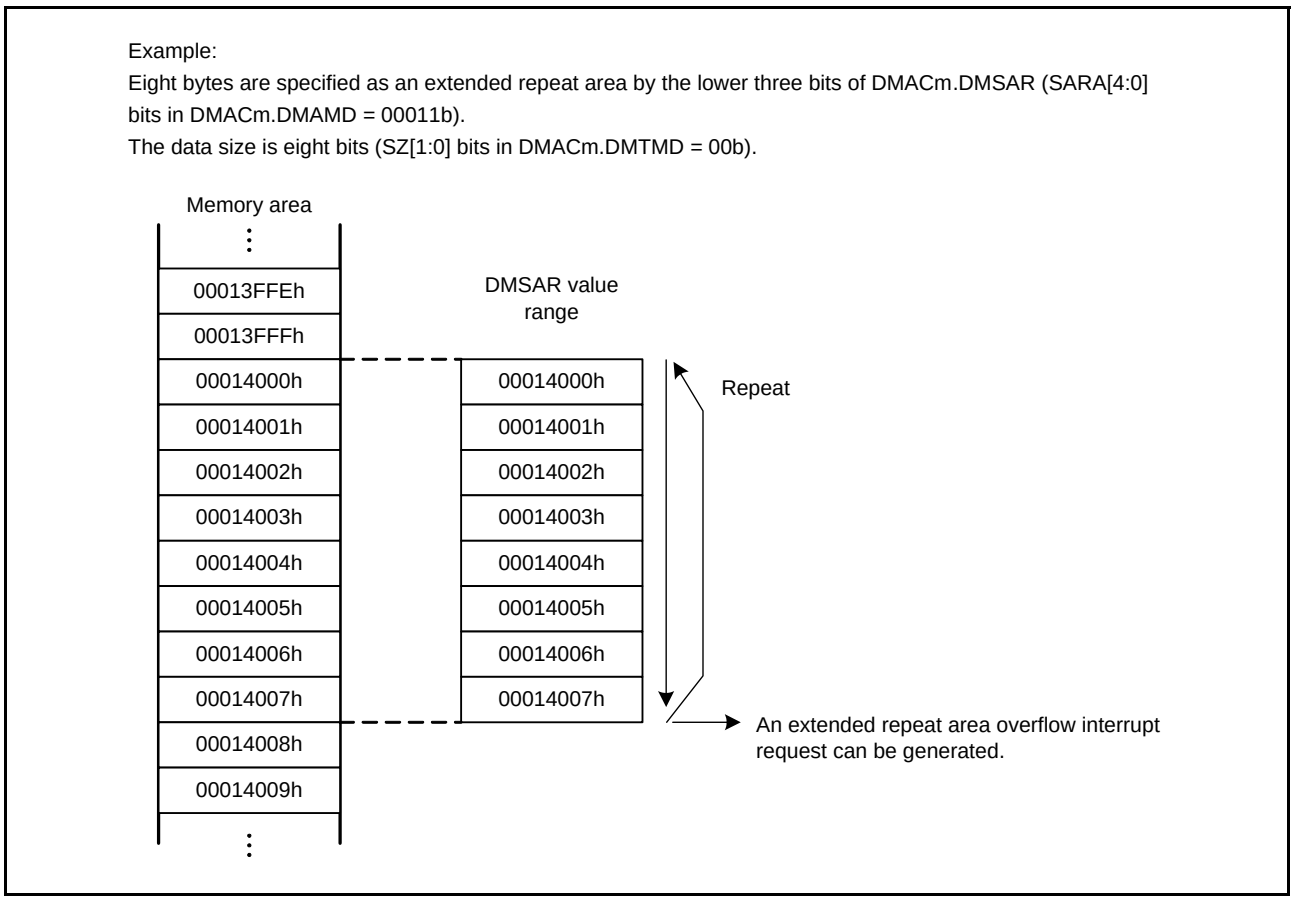


Figure 18.5 Example of Extended Repeat Area Operation

When an interrupt by an extended repeat area overflow is used in block transfer mode, the following should be taken into consideration.
When a transfer is stopped by an interrupt by an extended repeat area overflow, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the interrupt by the overflow is suspended until transfer of the block is completed, and the transfer overruns.

Figure 18.6 shows an example when the extended repeat area function is used in block transfer mode.

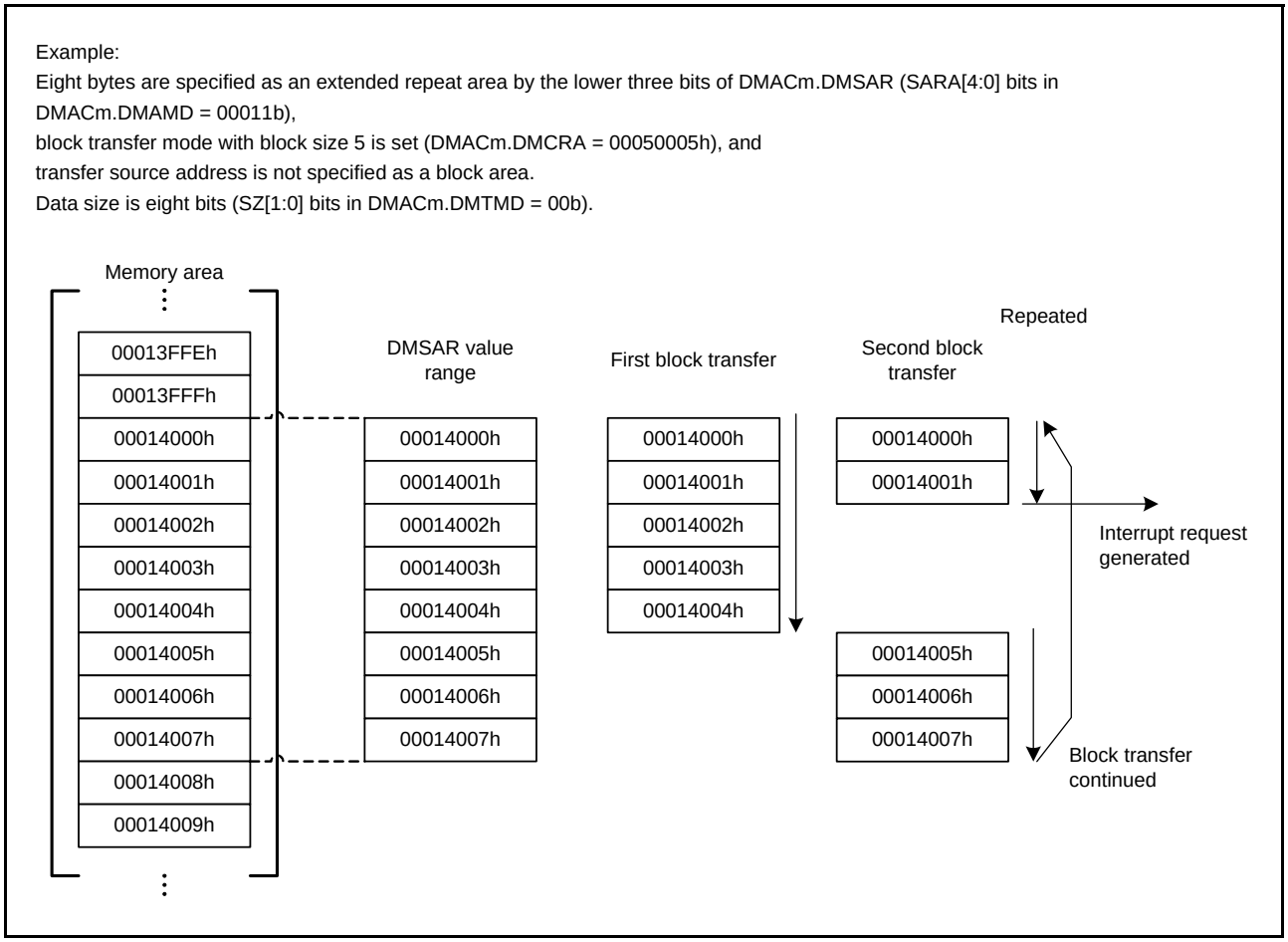


Figure 18.6 Example of Extended Repeat Area Function in Block Transfer Mode

18.3.3 Address Update Function using Offset

The source and destination addresses can be updated by fixing, increment, decrement, or offset addition. When the offset addition is selected, the offset specified by the DMA offset register (DMOFR of DMAC0) is added to the address every time the DMAC performs one data transfer. This function realizes a data transfer where addresses are allocated to separated areas.

Offset subtraction can also be realized by setting a negative value in DMOFR of DMAC0. In this case, the negative value must be 2's complement.

Address update function using offset can be specified only for the DMAC0 channel.

Table 18.6 shows the address update method in each address update mode.

Table 18.6 Address Update Method in Each Address Update Mode

Address Update Mode	Settings of DMACm.DMAMD.SM[1:0] and DMACm.DMAMD.DM[1:0] for Address Update Modes	Address Update Method (for Different SZ[1:0] Settings in DMTMD of DMACm)		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMACm.DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

Note 1. When setting a negative value in the DMA offset register, the value must be 2's complement. The 2's complement is obtained by the following formula.
2's complement of a negative offset value =~ (offset) + 1 (~: bit inversion)

(1) Basic Transfer Using Offset Addition

Figure 18.7 shows an example of address updating using offset addition.

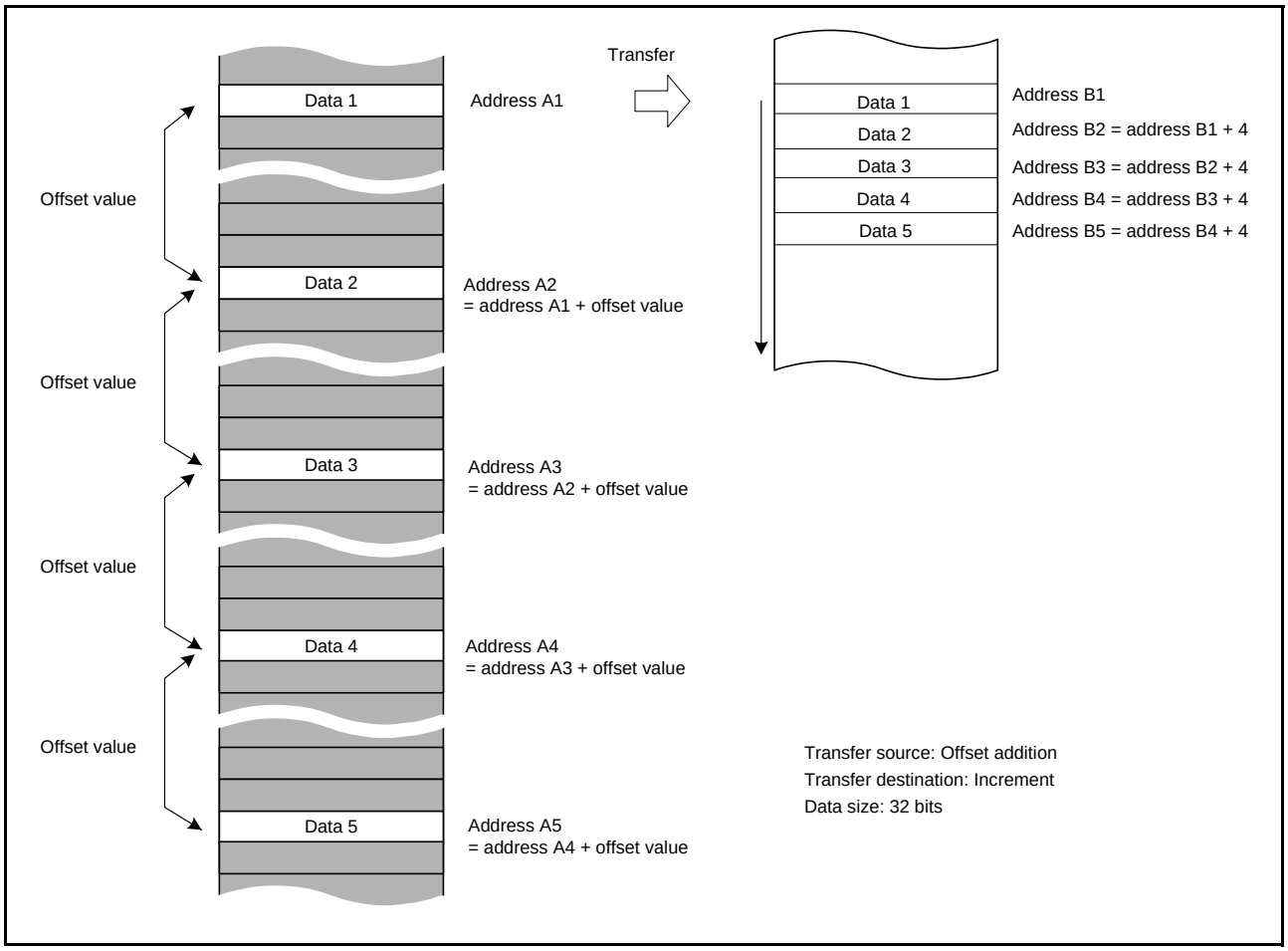


Figure 18.7 Example of Address Updating by Offset Addition

In Figure 18.7, the transfer data is 32 bits long, and offset addition and increment are set as the transfer source address update mode and transfer destination address update mode, respectively. The second and subsequent data is each read from the transfer source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to the continuous locations on the destination.

(2) Example of XY Conversion Using Offset Addition

Figure 18.8 shows the XY conversion using offset addition in repeat transfer mode.
Settings are as follows:

- DMAC0.DMAMD: Transfer source address update mode: Offset addition
- DMAC0.DMAMD: Transfer destination address update mode: Destination address is incremented.
- DMAC0.DMTMD: Transfer data size select: 32 bits
- DMAC0.DMTMD: Transfer mode select: Repeat transfer
- DMAC0.DMTMD: Repeat area select: The source is specified as the repeat area.
- DMAC0.DMOFR: Offset address: 10h
- DMAC0.DMCRA: Repeat size: 4h
- DMAC0.DMINT: The repeat size end interrupt is enabled.

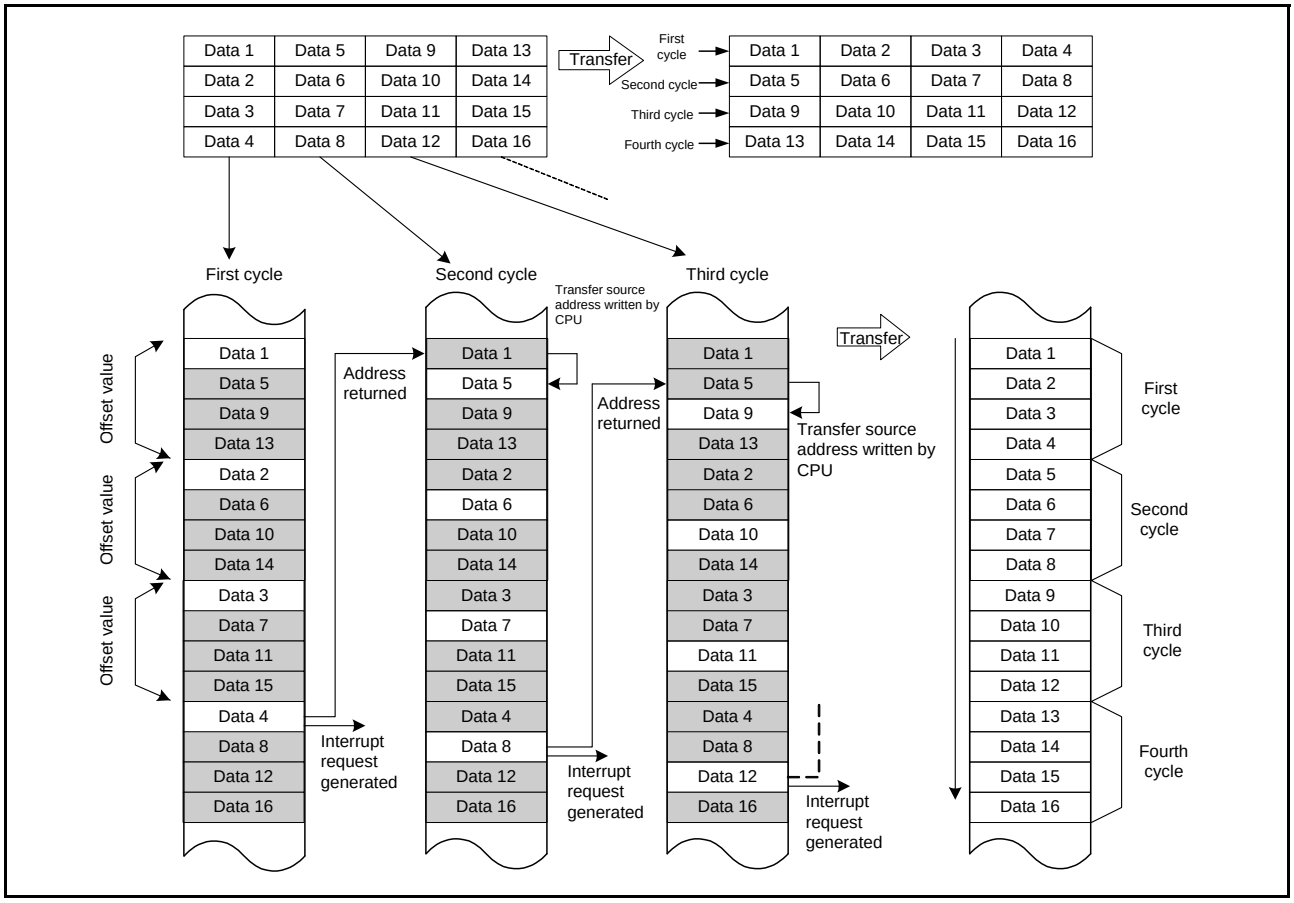


Figure 18.8 XY Conversion Operation Using Offset Addition in Repeat Transfer Mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to the destination continuous addresses. When data 4 is transferred, which means that the repeat size of transfers is completed, the transfer source address returns to the transfer start address (address of data 1 on the transfer source) and a repeat size end interrupt is requested. While this interrupt stops the transfer temporarily, perform the following.

- DMAC0.DMSAR: Rewrite the DMA transfer source address to the address of data 5 (with the above example, the data 1 address + 4).
- DMAC0.DMCNT: Set the DTE bit to 1.

The DMA transfer is resumed from the state when the DMA transfer is stopped. After that, the operations described above are repeated until the transfer source data is transposed to the destination area (XY conversion).

Figure 18.9 shows a flowchart of the XY conversion.

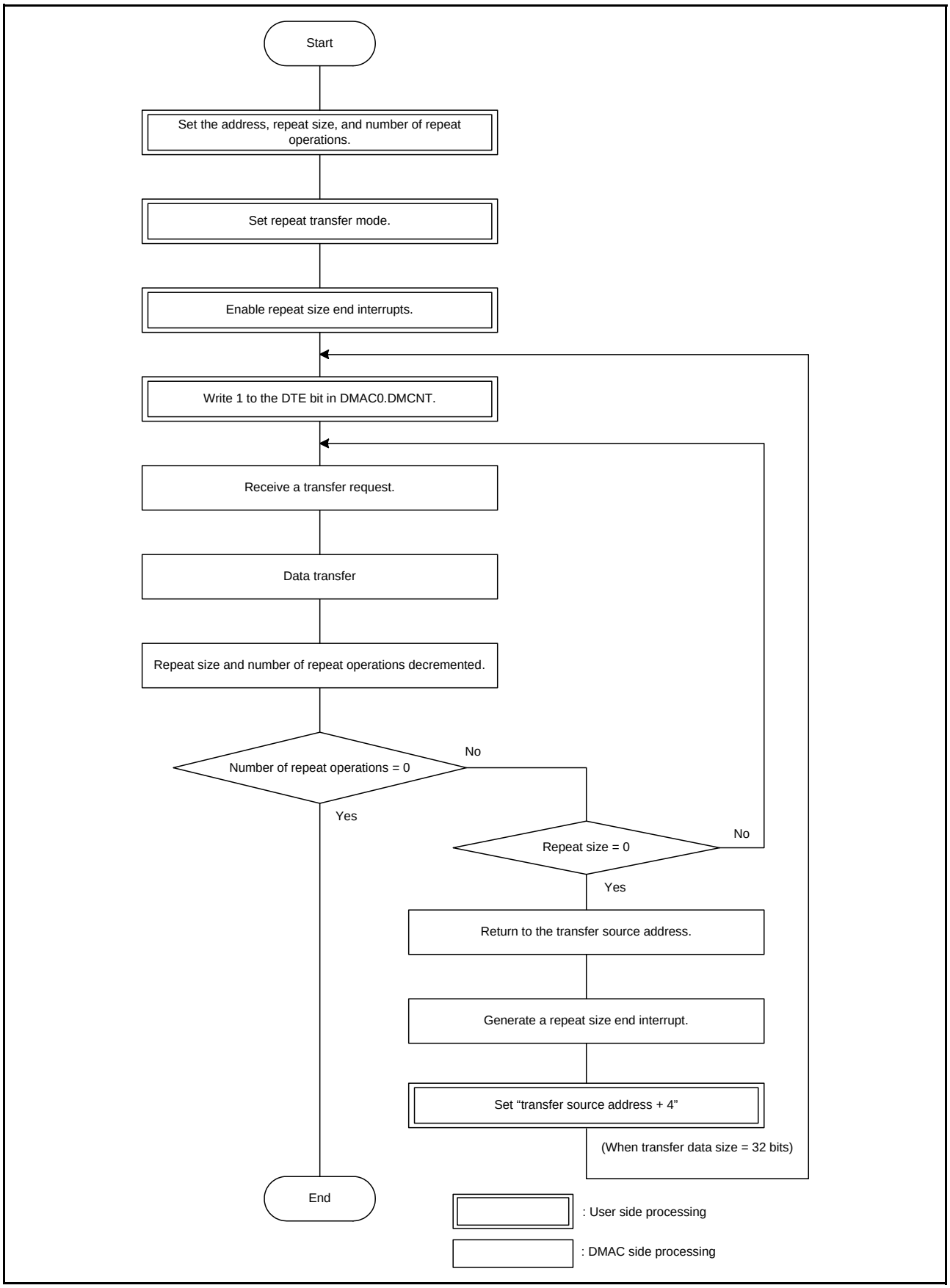


Figure 18.9 XY Conversion Flowchart Using Offset Addition in Repeat Transfer Mode

18.3.4 Activation Sources

Software, the interrupt requests from the peripheral modules, and the external interrupt requests can be specified as the DMAC activation sources. Setting the DCTG[1:0] bits in DMTMD of DMACm selects the activation source.

(1) DMAC Activation by Software

Setting the DCTG[1:0] bits in DMTMD of DMACm to 00b enables the DMAC activation by software.
To start DMA transfer by software, set the DCTG[1:0] bits in DMTMD of DMACm to 00b, and then set the DTE bit in DMCNT of DMACm to 1 (DMA transfer is enabled) and the SWREQ bit in DMREQ of DMACm to 1 (DMA transfer is requested) with the DMST bit in DMAST set to 1 (DMAC activation enabled).
When the DMAC is activated by software while the CLRS bit in DMREQ of DMACm is 0, the SWREQ bit in DMREQ of DMACm is cleared to 0 after data transfer is started in response to a DMA transfer request.
When the DMAC is activated by software while the CLRS bit is 1, the SWREQ bit is not cleared to 0 after data transfer is started. In this case, a DMA transfer request is issued again after completion of a transfer.

(2) DMAC Activation by Interrupt Requests from On-Chip Peripheral Modules or External Interrupt Requests

Interrupt requests from the on-chip peripheral modules and external interrupt requests can be specified as the DMAC activation sources. The activation source can be selected separately for each channel using the DMRSRm registers (m = 0 to 3) of the ICU.
The DMAC is activated when an interrupt request from the on-chip peripheral module or an external interrupt request is generated while the DCTG[1:0] bits in DMTMD of DMACm are set to 01b (interrupts from the peripheral modules and the external interrupt pins are selected), the DTE bit in DMCNT of DMACm is set to 1 (DMA transfer is enabled), and the DMST bit in DMAST is set to 1 (DMAC activation is enabled).

For interrupt requests specified as DMAC activation sources, see Table 15.3, Interrupt Vector Table, in section 15, Interrupt controller (ICUb).

18.3.5 Operation Timing

Figure 18.10 and Figure 18.11 show DMAC operation timing examples.

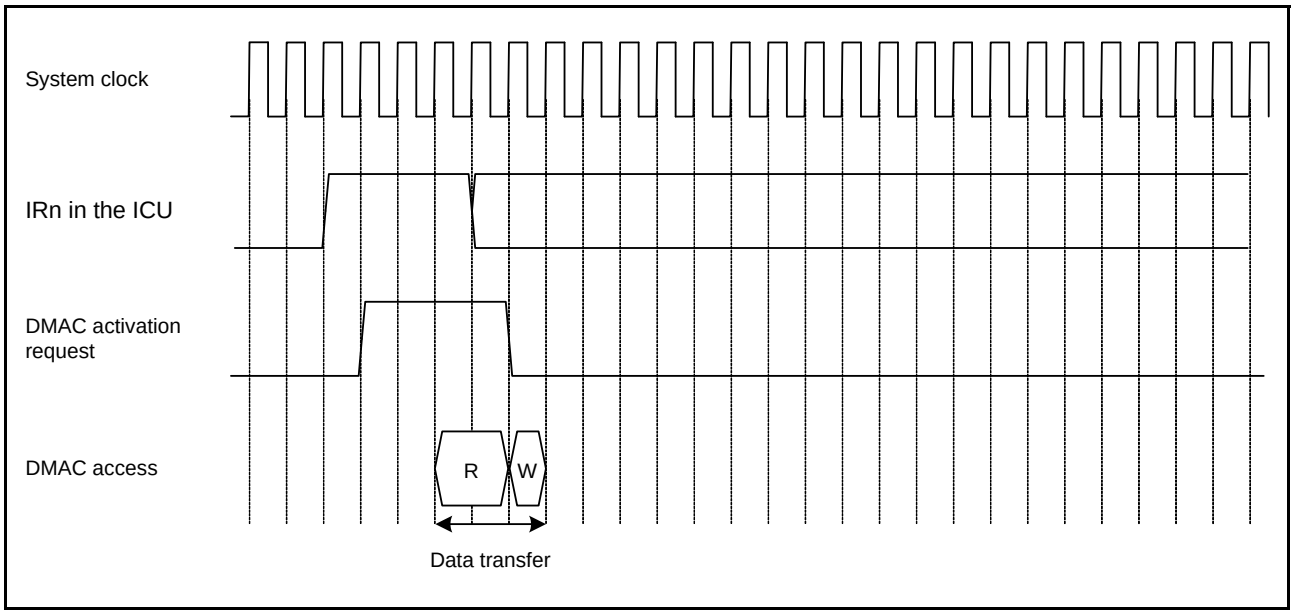


Figure 18.10 DMAC Operation Timing Example (1) (DMA Activation by Interrupt from Peripheral Module/ External Interrupt Input Pin, Normal Transfer Mode, Repeat Transfer Mode)

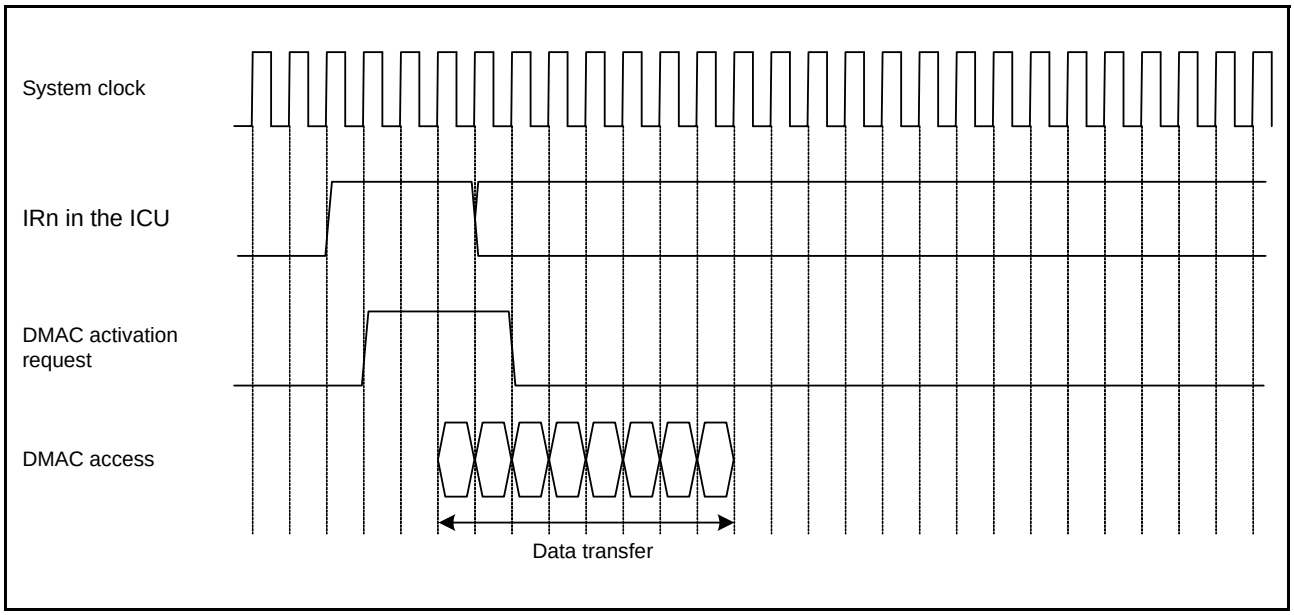


Figure 18.11 DMAC Operation Timing Example (2) (DMA Activation by Interrupt from Peripheral Module/ External Interrupt Input Pin, Block Transfer Mode, Block Size = 4)

18.3.6 DMAC Execution Cycles

Table 18.7 lists execution cycles in one DMAC data transfer operation.

Table 18.7 DMAC Execution Cycles

Transfer Mode	Data Transfer (Read)	Data Transfer (Write)
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle is applied.

P: Block size (DMCRAH register setting)
Cr: Data read destination access cycle
Cw: Data write destination access cycle

Cr and Cw depend on the access destination. For the number of cycles for each access destination, see section 40, RAM, section 41, Flash Memory, section 6, I/O Registers, and section 16.2.6, External Bus.
The unit for +1 in “Data Transfer (Read)” column is one system clock cycle (ICLK).
For the operation example, see section 18.3.5, Operation Timing.

18.3.7 Activating the DMAC

Figure 18.12 shows the register setting procedure.

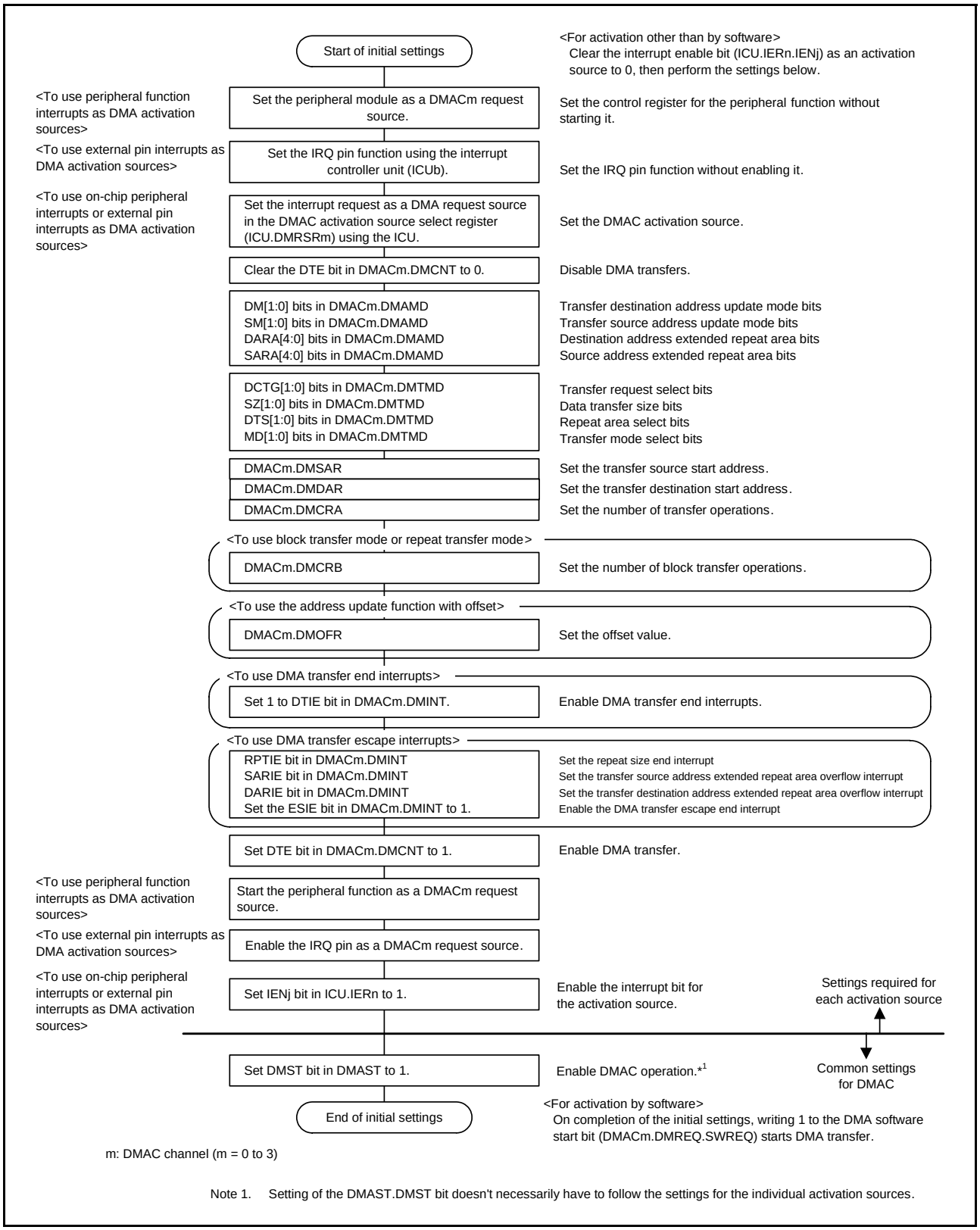


Figure 18.12 Register Setting Procedure

18.3.8 Starting DMA Transfer

Setting the DTE bit in DMCNT of DMACm to 1 (DMA transfer enabled) and setting the DMST bit in DMAST to 1 (DMAC start enabled) enable DMA transfer of channel m (m = 0 to 3).
Another activation request cannot be accepted during the transfer of other DMAC channel or DTC. When the proceeding transfer is completed, channel arbitration is performed where a DMA transfer request of the highest priority channel is accepted and DMA transfer of the channel starts. When DMA transfer starts, the ACT bit in DMSTS of DMACm is set to 1 (the DMAC is in the active state).

18.3.9 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated differs according to the other settings and the transfer state. The registers to be updated are DMSAR, DMDAR, DMCRA, DMCRB, DMCNT, and DMSTS of DMACm.

(1) DMA Source Address Register (DMACm.DMSAR)

When data has been transferred in response to one transfer request, the contents of DMSAR are updated to the address to be accessed by the next transfer request.
For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(2) DMA Destination Address Register (DMACm.DMDAR)

When data has been transferred in response to one transfer request, the contents of DMDAR are updated to the address to be accessed by the next transfer request.
For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(3) DMA Transfer Count Register (DMACm.DMCRA)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.
For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(4) DMA Block Transfer Count Register (DMACm.DMCRB)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.
For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(5) DMA Transfer Enable Bit (DMACm.DMCNT.DTE)

Although the DMACm.DMCNT.DTE bit enables or disables data transfer by the register write access, it is automatically cleared to 0 by the DMAC according to the DMA transfer state.
The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is completed
- When DMA transfer is stopped by the repeat size end interrupt
- When DMA transfer is stopped by the extended repeat area overflow interrupt

Writing to the registers for the channels when the corresponding DMACm.DMCNT.DTE bit is set to 1 is prohibited (except for DMACm.DMCNT). In this case, writing must be performed after the bit is cleared to 0.

(6) DMA Active Flag (DMACm.DMSTS.ACT)

The ACT bit in DMSTS of DMACm indicates whether the DMACm is in the idle or active state.
This flag is set to 1 when the DMAC starts data transfer, and is cleared to 0 when data transfer in response to one transfer request is completed.
Even when DMA transfer is stopped by writing 0 to the DTE bit in DMCNT of DMACm during DMA transfer, this flag remains 1 until DMA transfer is completed.

(7) Transfer End Interrupt Flag (DMACm.DMSTS.DTIF)

The DTIF flag in DMSTS of DMACm is set to 1 after DMA transfer of the total transfer size of data is completed.
When both this flag and the DTIE bit in DMINT of DMACm are set to 1, a transfer end interrupt is requested.
This flag is set to 1 when the DMA transfer bus cycle is completed and the ACT flag in DMSTS of DMACm is cleared to 0 indicating the DMA transfer end.
This flag is automatically cleared to 0 when the DTE bit in DMCNT of DMACm is set to 1 during the interrupt handling.

(8) Transfer Escape End Interrupt Flag (DMACm.DMSTS.ESIF)

The ESIF flag in DMSTS of DMACm is set to 1 when a repeat size end interrupt or extended repeat area overflow interrupt is requested. When this bit and the ESIE bit in DMINT of DMACm are set to 1, a transfer escape end interrupt is requested.
This flag is set to 1 when the bus cycle of the DMA transfer having caused the interrupt request is completed and the ACT flag in DMSTS of DMACm is cleared to 0 indicating the DMA transfer end.
This flag is automatically cleared to 0 when the DTE bit in DMCNT of DMACm is set to 1 during an interrupt handling.
Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 15, Interrupt controller (ICUb).

18.3.10 Channel Priority

When multiple DMA transfer requests are present, the DMAC determines the priority of channels that have DMA transfer requests.
The channel priority is fixed as channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest).
When a DMA transfer request is generated during data transfer, channel arbitration is started after the final data has been transferred, and DMA transfer of the higher-priority channel starts.

18.4 Ending DMA Transfer

The operation for ending DMA transfer depends on the transfer end conditions. When DMA transfer ends, the DTE bit in DMCNT and the ACT flag in DMSTS of DMACm are changed from 1 to 0, indicating that DMA transfer has ended.

18.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In Normal Transfer Mode (DMACm.DMTMD.MD[1:0] = 00b)

When the value of DMCRAL of DMACm changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DTE bit in DMCNT of DMACm is cleared to 0 and the DTIF bit in DMSTS of DMACm is set to 1 at the same time. If the DTIE bit in DMINT of DMACm is 1 at this time, a transfer end interrupt request is issued to the CPU or the DTC.

(2) In Repeat Transfer Mode (DMACm.DMTMD.MD[1:0] = 01b)

When the value of DMCRB of DMACm changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DTE bit in DMCNT of DMACm is cleared to 0 and the DTIF bit in DMSTS of DMACm is set to 1 at the same time. If the DTIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC.

(3) In Block Transfer Mode (DMACm.DMTMD.MD[1:0] = 10b)

When the value of DMCRB of DMACm changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DTE bit in DMCNT of DMACm is cleared to 0 and the DTIF bit in DMSTS of DMACm is set to 1 at the same time. If the DTIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC.
Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 15, Interrupt controller (ICUb).

18.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, a repeat size end interrupt is requested when transfer of a 1-repeat size of data is completed while the RPTIE bit in DMINT of DMACm is set to 1. When the interrupt is requested to complete DMA transfer, the DTE bit in DMCNT of DMACm is cleared to 0 and the ESIF flag in DMSTS of DMACm is set to 1. If the ESIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC. Here, the transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm.
A repeat size end interrupt can be requested also in block transfer mode. In block transfer mode, the interrupt is requested in the same way as in repeat transfer mode when transfer of a 1-block size data is completed.
Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 15, Interrupt controller (ICUb).

18.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the SARIE or DARIE bit in DMINT of DMACm is set to 1, an interrupt by an extended repeat area overflow is requested. When the interrupt is requested, the DMA transfer is terminated, the DTE bit in DMCNT of DMACm is cleared to 0, and the ESIF flag in DMSTS of DMACm is set to 1. If the ESIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC.
Even if an interrupt by an extended repeat area overflow is requested during a read cycle, the following write cycle is performed.
In block transfer mode, even if an interrupt by an extended repeat area overflow is requested during a 1-block transfer, the remaining data in the block is transferred; transfer is terminated after a block transfer.
Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 15, Interrupt controller (ICUb).

18.5 Interrupts

Each DMAC channel can output an interrupt request to the CPU or the DTC after transfer in response to one request is completed. When the transfer destination is the on-chip peripheral bus, an interrupt request is generated upon completion of data write to the write buffer not to the actual transfer destination.

Table 18.8 lists the relation among the interrupt sources, the interrupt status flags, and the interrupt enable bits. Figure 18.13 shows the schematic logic diagram of interrupt outputs. Figure 18.14 shows the DMAC interrupt handling routine to resume or terminate DMA transfer.

Table 18.8 Relation among Interrupt Sources, Interrupt Status Flags, and Interrupt Enable Bits

Interrupt Sources		Interrupt Enable Bits	Interrupt Status Flags	Request Output Enable Bits
Transfer end		—	DMACm.DMSTS.DTIF	DMACm.DMINT.DTIE
Escape transfer end	Repeat size end	DMACm.DMINT.RPTIE	DMACm.DMSTS.ESIF	DMACm.DMINT.ESIE
	Source address extended repeat area overflow	DMACm.DMINT.SARIE		
	Destination address extended repeat area overflow	DMACm.DMINT.DARIE		

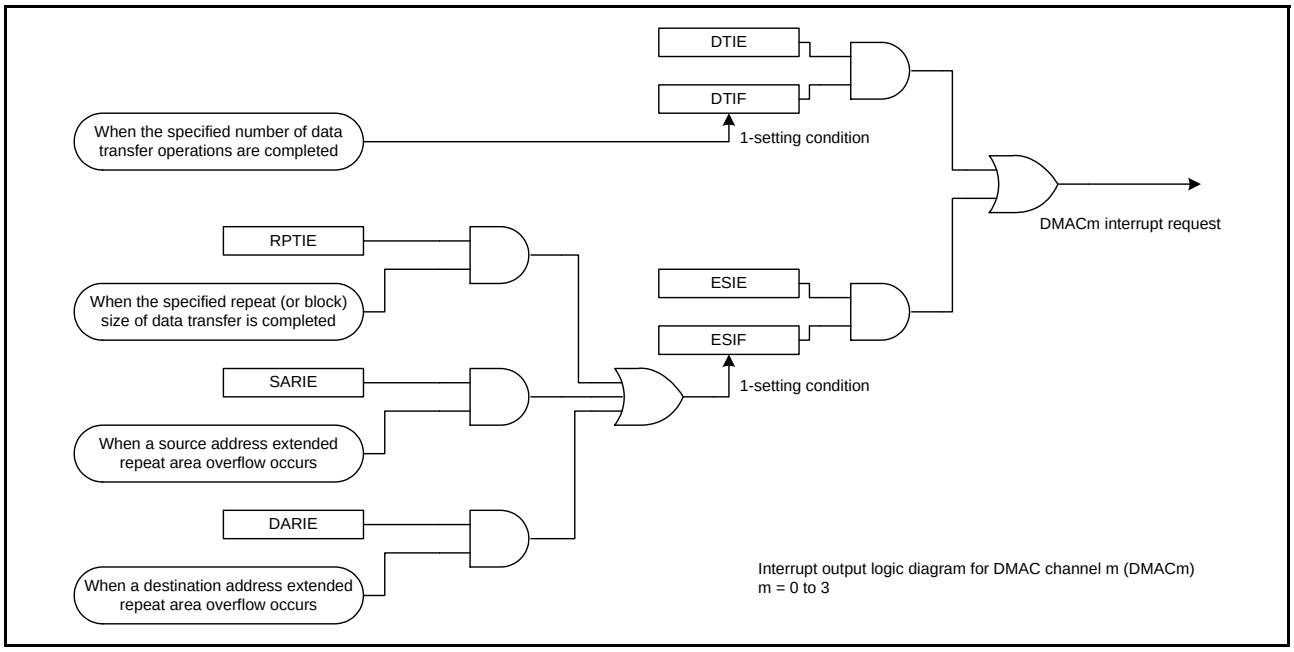


Figure 18.13 Schematic Logic Diagram of Interrupt Outputs

Specifically, the different procedures are used for canceling an interrupt to restart DMA transfer in the following two cases: (1) discontinuing or terminating DMA transfer and (2) continuing DMA transfer.

(1) When Discontinuing or Terminating DMA Transfer

Write 0 to the DTIF bit in DMSTS of DMACm to clear a transfer end interrupt, and to the ESIF bit in DMSTS of DMACm to clear a repeat size interrupt and an extended repeat area overflow interrupt. The DMACm remains in the stop state. When starting another DMA transfer after that, set the appropriate registers, and set the DTE bit in DMCNT of DMACm to 1 (DMA transfer enabled).

(2) When Continuing DMA Transfer

Write 1 to the DTE bit in DMCNT of DMACm. The ESIF bit in DMSTS of DMACm is automatically cleared to 0 (interrupt source cleared), and DMA transfer is resumed.

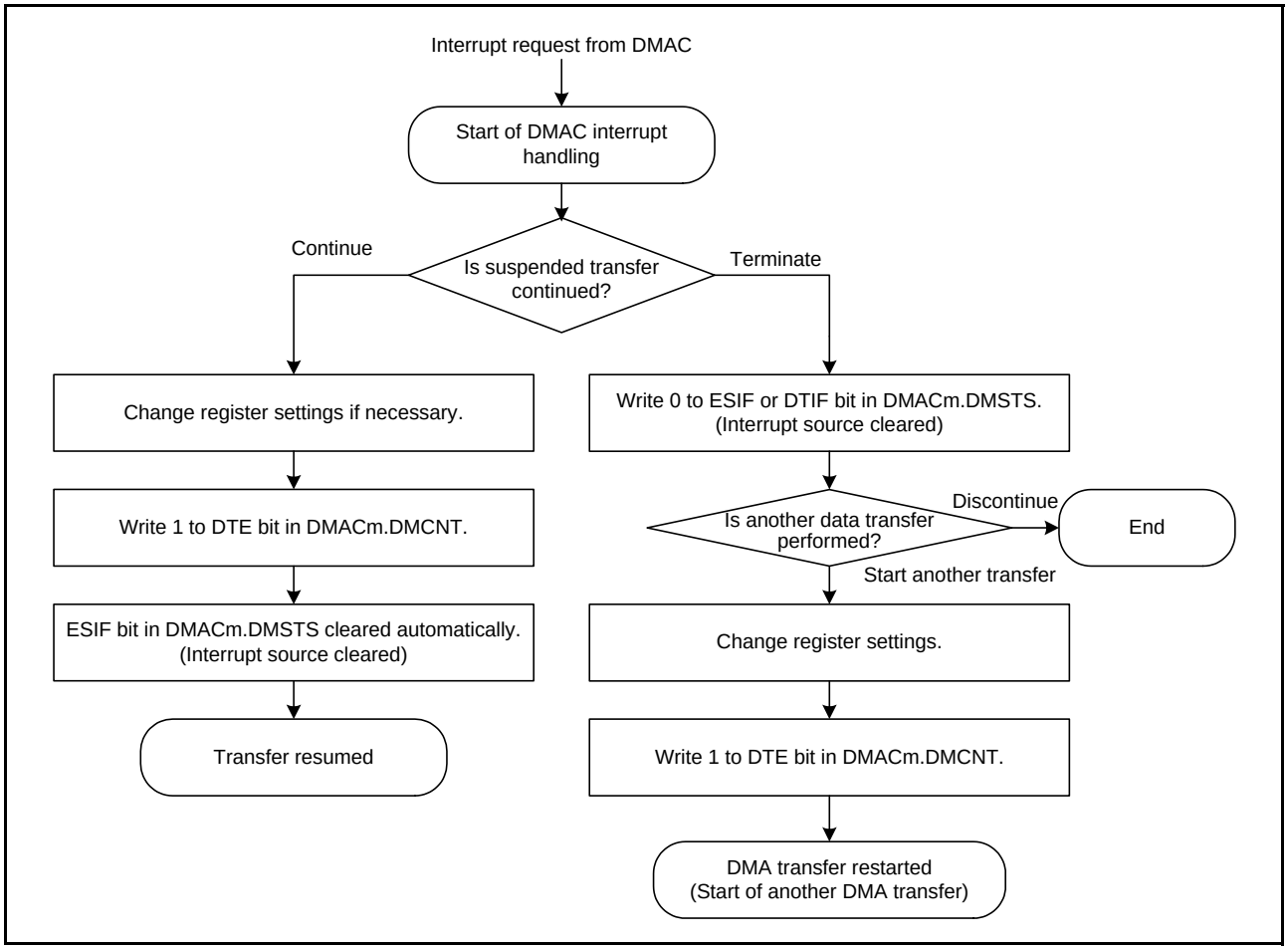


Figure 18.14 DMAC Interrupt Handling Routine to Resume/Terminate DMA Transfer

18.6 Low-Power Consumption Function

Before transition to the module-stop state, all-module clock stop mode, software standby mode, or deep software standby mode, clear the DMST bit in DMAST to 0 (the DMAC suspended), and then perform the following.

(1) Module-Stop Function

Writing 1 to the MSTPA28 bit (transition to the module-stop state) in MSTPCRA enables the module-stop function of the DMAC. If DMA transfer is in progress at the time a 1 is written to the MSTPA28 bit, the transition to the module-stop state proceeds after DMA transfer has ended. While the MSTPA28 bit is 1, accessing the DMAC registers are prohibited.
Writing 0 to the MSTPA28 bit releases the DMAC from the module-stop state.

(2) All-Module Clock Stop Mode

Make settings in accord with the procedure under section 12.5.2.1, Transition to All-Module Clock Stop Mode, in section 12, Low Power Consumption.
If DMA transfer operations are in progress at the time the WAIT instruction is executed, the transition to all-module clock stop mode follows the completion of DMA transfer.
The DMAC is released from the module-stop state by writing 0 to the MSTPCRA.MSTPA28 bit following recovery from all-module clock stop mode.

(3) Software Standby and Deep Software Standby Modes

Make settings in accord with the procedure under section 12.5.3.1, Transition to Software Standby Mode or section 12.5.4.1, Transition to Deep Software Standby Mode, in section 12, Low Power Consumption.
If DMA transfer operations are in progress at the time the WAIT instruction is executed, the transition to software standby or deep software standby follows the completion of DMA transfer.

(4) Note on Low-Power Consumption Function

For the WAIT instruction and the register setting procedure, see section 12.6.6, Timing of Wait Instructions in section 12, Low Power Consumption.
To perform DMA transfer after returning from low-power consumption mode, set the DMST bit in DMAST to 1 again.
To use a request that is generated in all-module clock-stop mode and software standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination in accordance with the description in section 15.5.3, Selecting Interrupt Request Destinations in section 15, Interrupt controller (ICUb), and then execute the WAIT instruction.

18.7 Usage Notes

18.7.1 DMA Transfer to External Devices

In DMA transfer to an external device, the ACT bit in DMSTS of DMACm may be cleared to 0 (DMAC transfer suspended) during the period from the beginning of the final data write to the end of the external bus access.

18.7.2 DMA Transfer to Peripheral Modules

In DMA transfer to a peripheral module, the ACT bit in DMSTS of DMACm may be cleared to 0 (DMAC transfer suspended) during the period from the beginning of the final data write to the end of the peripheral bus access.

18.7.3 Access to the Registers during DMA Transfer

The DMSAR, DMDAR, DMCRA, DMCRB, DMTMD, DMINT, DMAMD, DMOFR, and DMCSL registers of DMACm must not be accessed while the ACT bit in DMSTS of the same channel is set to 1 (DMAC active state) or the DTE bit in DMCNT of the same channel is set to 1 (DMA transfer enabled).

18.7.4 DMA Transfer to Reserved Areas

DMA transfer to the reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on the reserved areas, see section 5, Address Space.

18.7.5 Interrupt Request by the DMA Activation Source Flag Control Register (DMCSL) at the End of Each Transfer

While the DMACm.DMCSL.DISEL bit is 1, an interrupt is issued to the CPU at the end of each transfer that has been activated by one DMA request. Unlike the transfer end interrupt that the DMAC outputs or the escape end interrupt, the interrupt of this type is issued to the CPU at the end of DMA transfer without clearing the interrupt flag of the DMAC activation source to 0 by changing the interrupt request destination to the CPU. In this case, since the interrupt flag is not cleared to 0 at the end of DMAC transfer, it should be cleared to 0 by the CPU interrupt routine.
The interrupt flag is cleared when the CPU interrupt is accepted.
For the change of the settings on the interrupt flag or the interrupt request destination, see section 15, Interrupt controller (ICUb). For the DMACm.DMCSL.DISEL bit setting, see section 18.2.12, DMA Activation Source Flag Control Register (DMCSL).

18.7.6 Setting of DMAC Activation Request Select Register of the Interrupt Controller (ICU.DMRSRm)

The DMAC activation request select register (ICU.DMRSRm) should be set while the DMA transfer enable bit (DMACm.DMCNT.DTE) is cleared to 0 (DMA transfer is disabled). Moreover, the DTC activation enable register (ICU.DTCERm) that corresponds to the same vector number that has been set by the ICU.DMRSRm register should not be set to 1. For details on the ICU.DTCERn and ICU.DMRSRm, see section 15, Interrupt controller (ICUb).

18.7.7 Suspending or Restarting DMA Activation

To suspend a DMA activation request, write 0 to the interrupt enable bit for the activation source (ICU.IERn.IENj bit). To restart the DMA transfer, write 1 to the ICU.IERn.IENj bit with the setting shown in section 18.3.7, Activating the DMAC.

19. Data Transfer Controller (DTCa)

This MCU incorporates a data transfer controller (DTC).
The DTC is activated by an interrupt request to control data transfer.

19.1 Overview

Table 19.1 lists the specifications of the DTC, and Figure 19.1 shows a block diagram of the DTC.

Table 19.1 DTC Specifications

Item	Description
Transfer mode	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. The maximum repeat size is 256. • Block transfer mode A single activation leads to the transfer of a single block. The maximum block size is 256 data.
Transfer channel	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh excepting reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh excepting reserved areas)
Data transfer units	• Length of a single data: 8, 16, or 32 bits • Number of data for a single block: 1 to 256 data
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Read skip	Transfer data read skip can be specified.
Write-back skip	When “fixed” is selected for transfer source address or transfer destination address, write-back skip execution is provided.
Lower power consumption function	Module-stop state can be specified.

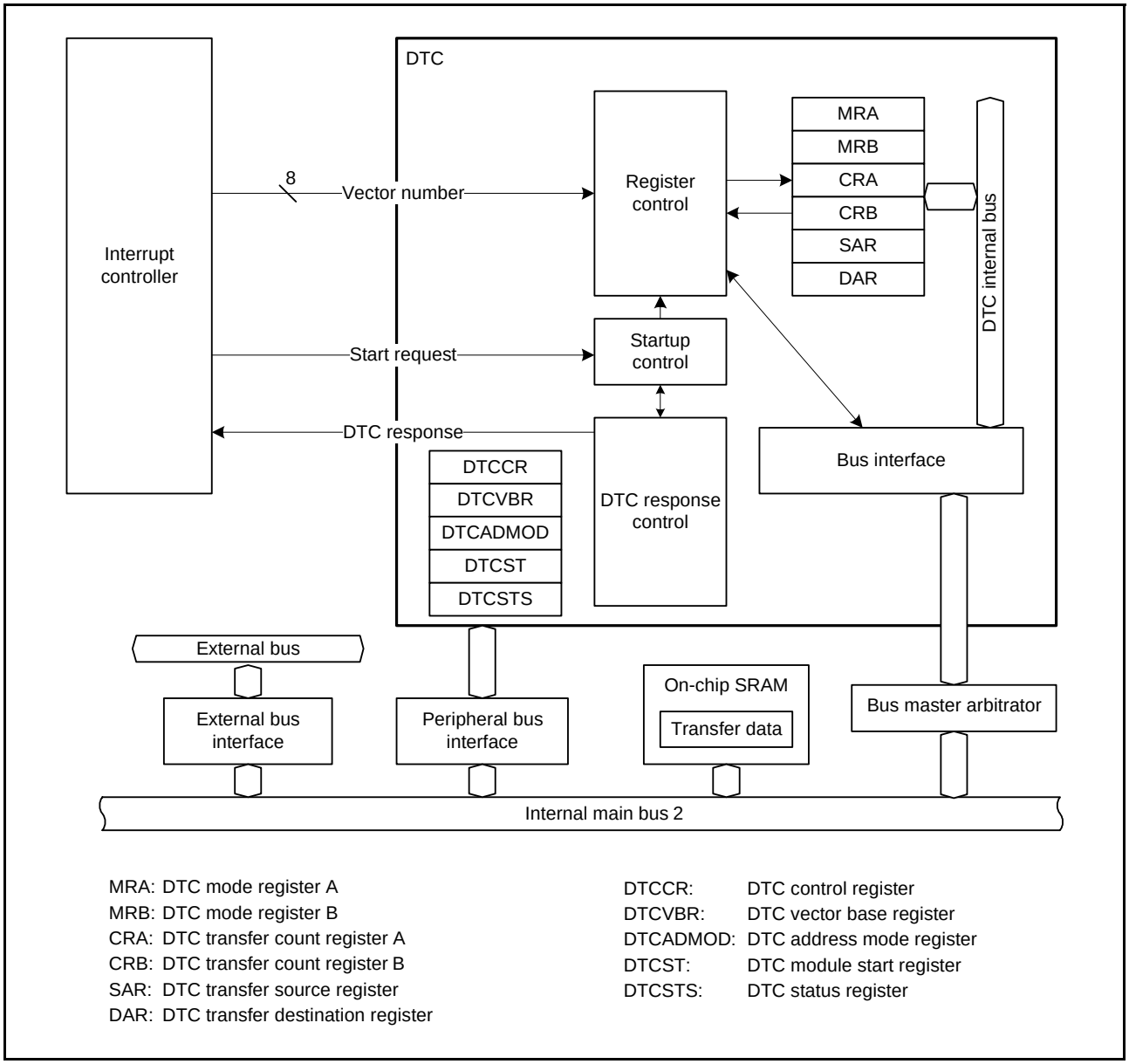


Figure 19.1 Block Diagram of DTC

19.2 Register Descriptions

Registers MRA, MRB, SAR, DAR, CRA, and CRB are DTC internal registers, which cannot be directly accessed from the CPU. Values to be set in the DTC internal registers are placed in the RAM area as transfer information data. When an activation request is generated, the DTC reads the transfer information data from the RAM area and set them in the internal registers. After the data transfer ends, the internal register contents are written back to the RAM area as transfer information data.

19.2.1 DTC Mode Register A (MRA)

Address(es): (inaccessible directly from the CPU)

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—
b3, b2	SM[1:0]	Transfer Source Address Addressing Mode	b3 b2 0 0: Address in the SAR register is fixed (Write-back to SAR is skipped) 0 1: Address in the SAR register is fixed (Write-back to SAR is skipped) 1 0: SAR value is incremented after data transfer (+1 when SZ[1:0] bits = 00b, +2 when SZ[1:0] bits = 01b, +4 when SZ[1:0] bits = 10b) 1 1: SAR value is decremented after data transfer (–1 when SZ[1:0] bits = 00b, –2 when SZ[1:0] bits = 01b, –4 when SZ[1:0] bits = 10b)	—
b5, b4	SZ[1:0]	DTC Data Transfer Size	b5 b4 0 0: 8-bit (byte) transfer 0 1: 16-bit (word) transfer 1 0: 32-bit (longword) transfer 1 1: Setting prohibited	—
b7, b6	MD[1:0]	DTC Transfer Mode Select	b7 b6 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited	—

MRA cannot be accessed directly from the CPU.

19.2.2 DTC Mode Register B (MRB)

Address(es): (inaccessible directly from the CPU)

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—
b3, b2	DM[1:0]	Transfer Destination Address Addressing Mode	b3 b2 0 0: Address in the DAR register is fixed (Write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (Write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer (+1 when SZ[1:0] bits in MRA = 00b, +2 when SZ[1:0] bits = 01b, +4 when SZ[1:0] bits = 10b) 1 1: DAR value is decremented after data transfer (–1 when SZ[1:0] bits in MRA = 00b, –2 when SZ[1:0] bits = 01b, –4 when SZ[1:0] bits = 10b)	—
b4	DTS	DTC Transfer Mode Select	0: Transfer destination side is repeat area or block area 1: Transfer source side is repeat area or block area	—
b5	DISEL	DTC Interrupt Select	0: An interrupt request to the CPU is generated when specified data transfer is completed 1: An interrupt request to the CPU is generated each time DTC data transfer is performed	—
b6	CHNS	DTC Chain Transfer Select	0: Chain transfer is performed continuously 1: Chain transfer is performed only when the transfer counter is changed from 1 to 0 or 1 to CRAH	—
b7	CHNE	DTC Chain Transfer Enable	0: Chain transfer is disabled 1: Chain transfer is enabled	—

MRB cannot be accessed directly from the CPU.

DTS Bit (DTC Transfer Mode Select)

The DTS bit specifies the side (transfer source or destination) to be a repeat area or block area in repeat transfer mode or block transfer mode.

CHNS Bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition.

When the CHNE bit is 0, setting of the CHNS bit is ignored. For details on the conditions to select the chain transfer, see Table 19.3, Chain Transfer Conditions.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the startup source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE Bit (DTC Chain Transfer Enable)

The CHNE bit enables or disables chain transfer.

The chain transfer condition is selected by the CHNS bit.

For details of chain transfer, see section 19.4.6, Chain Transfer.

19.2.3 DTC Transfer Source Register (SAR)

Address(es): (inaccessible directly from the CPU)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

In full-address mode, 32 bits are valid.
In short-address mode, lower 24 bits are valid and upper 8 bits (b31 to b24) are ignored. The address of this register is extended by the value specified by b23.
SAR cannot be accessed directly from the CPU.

19.2.4 DTC Transfer Destination Register (DAR)

Address(es): (inaccessible directly from the CPU)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

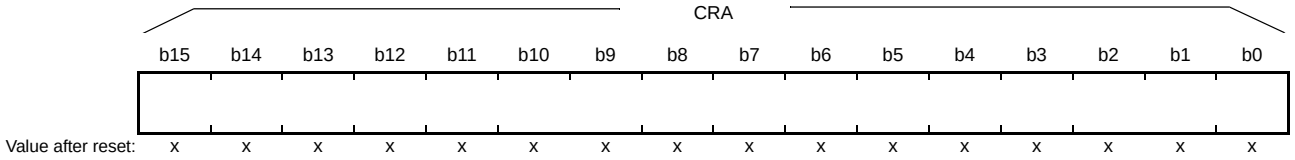
x: Undefined

In full-address mode, 32 bits are valid.
In short-address mode, lower 24 bits are valid and upper 8 bits (b31 to b24) are ignored. The address of this register is extended by the value specified by b23.
DAR cannot be accessed directly from the CPU.

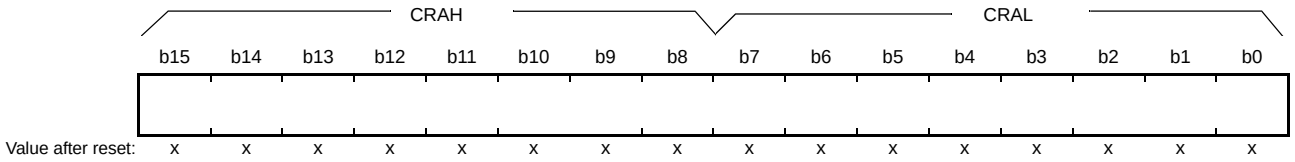
19.2.5 DTC Transfer Count Register A (CRA)

Address(es): (inaccessible directly from the CPU)

- Normal transfer mode



- Repeat transfer mode/block transfer mode



x: Undefined

Note: • The function depends on transfer mode.

Symbol	Register Name	Description	R/W
CRAL	Transfer Counter A Lower Register	Set transfer count.	—
CRAH	Transfer Counter A Upper Register		—

Note: • Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

CRA cannot be accessed directly from the CPU.

(1) Normal transfer mode (MD[1:0] bits in MRA = 00b)

CRA functions as a 16-bit transfer counter in normal transfer mode.
The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively.
The CRA value is decremented (–1) at each data transfer.

(2) Repeat transfer mode (MD[1:0] bits in MRA = 01b)

The CRAH register retains transfer count and the CRAL register functions as an 8-bit transfer counter.
The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.
The CRAL value is decremented (–1) at each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MD[1:0] bits in MRA = 10b)

The CRAH register retains block size and the CRAL register functions as an 8-bit block size counter.
The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.
The CRAL value is decremented (–1) at each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

19.2.6 DTC Transfer Count Register B (CRB)

Address(es): (inaccessible directly from the CPU)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

CRB is used to set the block transfer count for block transfer mode.
The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRB value is decremented (–1) when the final data of a single block size is transferred.
When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.
CRB cannot be accessed directly from the CPU.

19.2.7 DTC Control Register (DTCCR)

Address(es): 0008 2400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	RRS	DTC Transfer Data Read Skip Enable	0: Transfer data read is not skipped 1: Transfer data read is skipped when vector numbers match.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RRS Bit (DTC Transfer Data Read Skip Enable)

The DTC vector number is always compared with the vector number in the previous startup process.
When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transferred data. However, when the previous transfer was chain transfer, the transferred data is always read regardless of the value of RRS bit.
Furthermore, when the transfer counter (CRA register) became 0 during the previous normal transfer and when the transfer counter (CRB register) became 0 during the previous block transfer, the transferred data is always read regardless of the value of RRS bit.

19.2.8 DTC Vector Base Register (DTCVBR)

Address(es): 0008 2404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Description	R/W
b9 to b0	DTC vector address (the lower 10 bits)	These bits are read as 0. The write value should be 0.	R
b31 to b10	DTC vector base address (the upper 22 bits)	The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified by b27.	R/W

DTCVBR is used to set the base address for calculating the DTC vector table address.
It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1K-byte units.

19.2.9 DTC Address Mode Register (DTCADMOD)

Address(es): 0008 2408h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SHORT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SHORT	Short-Address Mode	0: Full-address mode 1: Short-address mode	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCADMOD is used to specify the area accessible by the DTC.

SHORT Bit (Short-Address Mode)

Full-address mode allows the DTC to access to a 4-Gbyte space (0000 0000h to FFFF FFFFh).
Short-address mode allows the DTC to access to a 16-Mbyte space (0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh).

19.2.10 DTC Module Start Register (DTCST)

Address(es): 0008 240Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DTCST	DTC Module Start	0: DTC module-stop 1: DTC module-stop	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCST Bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is cleared to 0, transfer requests are no longer accepted.

If this bit is cleared to 0 during data transfer, the accepted transfer request is active until the processing is completed.

Before making transition to the module-stop state, all-module clock-stop mode, software standby mode, or deep software standby mode, the DTCST bit must be set to 0.

For details on transitions to the module-stop state, all-module clock-stop mode, software standby mode, and deep software standby mode, refer to section 19.8, Low-Power Consumption Function, and section 12, Low Power Consumption.

19.2.11 DTC Status Register (DTCSTS)

Address(es): 0008 240Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	VECN[7:0]	DTC-Activating Vector Number Monitoring	These bits indicate the vector number for the activating source when DTC transfer is in progress. The value is only valid if DTC transfer is in progress (the value of the ACT flag is 1).	R
b14 to b8	—	Reserved	These bits are read as 0. Writing to this bit has no effect.	R
b15	ACT	DTC Active Flag	0: DTC transfer operation is not in progress. 1: DTC transfer operation is in progress.	R

VECN[7:0] Bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, these bits indicate the vector number corresponding to the activating source for the transfer.

When the DTCSTS register is read, the value read from the VECN[7:0] bits is valid if the value of the ACT flag was 1 (indicating DTC transfer in progress) and invalid if the value of the ACT flag was 0 (indicating no current DTC transfer).

For the correspondence between the DTC startup sources and the vector addresses, see Table 15.3, Interrupt Vector Table in section 15, Interrupt controller (ICUb).

ACT Bit (DTC Active Flag)

This bit indicates the state of DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request

[Clearing condition]

- When transfer by the DTC is completed in response to a transfer request.

19.3 Sources of Activation

The DTC is activated by an interrupt request. Setting the DTCERn.DTCE bit (where n is the interrupt vector number of the given interrupt) of the ICU to 1 selects the corresponding interrupt as an activation source for the DTC.
For the correspondence between the DTC startup sources and the vector addresses, see Table 15.3, Interrupt Vector Table in section 15, Interrupt controller (ICUb). For startup by software, see section 15.2.5, Software Interrupt Activation Register (SWINTR).
Once the DTC has accepted a startup request, it does not accept another startup request until transfer for that single request is completed, regardless of the priority of the requests. When multiple startup requests are generated during DMAC/DTC transfer, a request with the highest priority on completion of the transfer is accepted. When multiple startup requests are generated while the DTC module start (DTCST) bit in DTCST is 0, a request with the highest priority at the moment when the bit is subsequently set to 1 is accepted.

The following operations are performed for each single round of data transfer (or the last of the consecutive transfers in the case of a chained transfer).

- On completion of a specified round of data transfer, the DTCERn.DTCE bit is cleared to 0 and an interrupt is requested to the CPU.
- If the MRB.DISEL bit is 1, an interrupt is requested to the CPU on completion of data transfer.
- For the other transfers, the interrupt status flag of the startup source is cleared to 0 at the start of data transfer.

19.3.1 Allocating Transfer Data and DTC Vector Table

The DTC reads the start address of the transfer data corresponding to each startup source from the vector table and reads the transfer data starting at that address.
The vector table should be located so that the lower 12 bits of the base address (start address) are 0. Use the DTC vector base register (DTCVBR) to set the base address of the DTC vector table.
Transfer data is allocated in the RAM area. In the RAM area, the start address of the transfer data (n) with vector number n should be 4n added to the base address in the vector table.
Transfer data can be allocated in short-address mode (3 longwords) or full-address mode (4 longwords). Use the SHORT bit in DTCADMOD to select short-address mode (SHORT bit = 1) or full-address mode (SHORT bit = 0).
Figure 19.2 shows the relationship between the DTC vector table and transfer data.
Figure 19.3 shows the allocation of transfer data in the RAM area. The lower addresses vary according to the endian of the corresponding allocation area. For details, see section 19.9.2, Allocating Transfer Data.

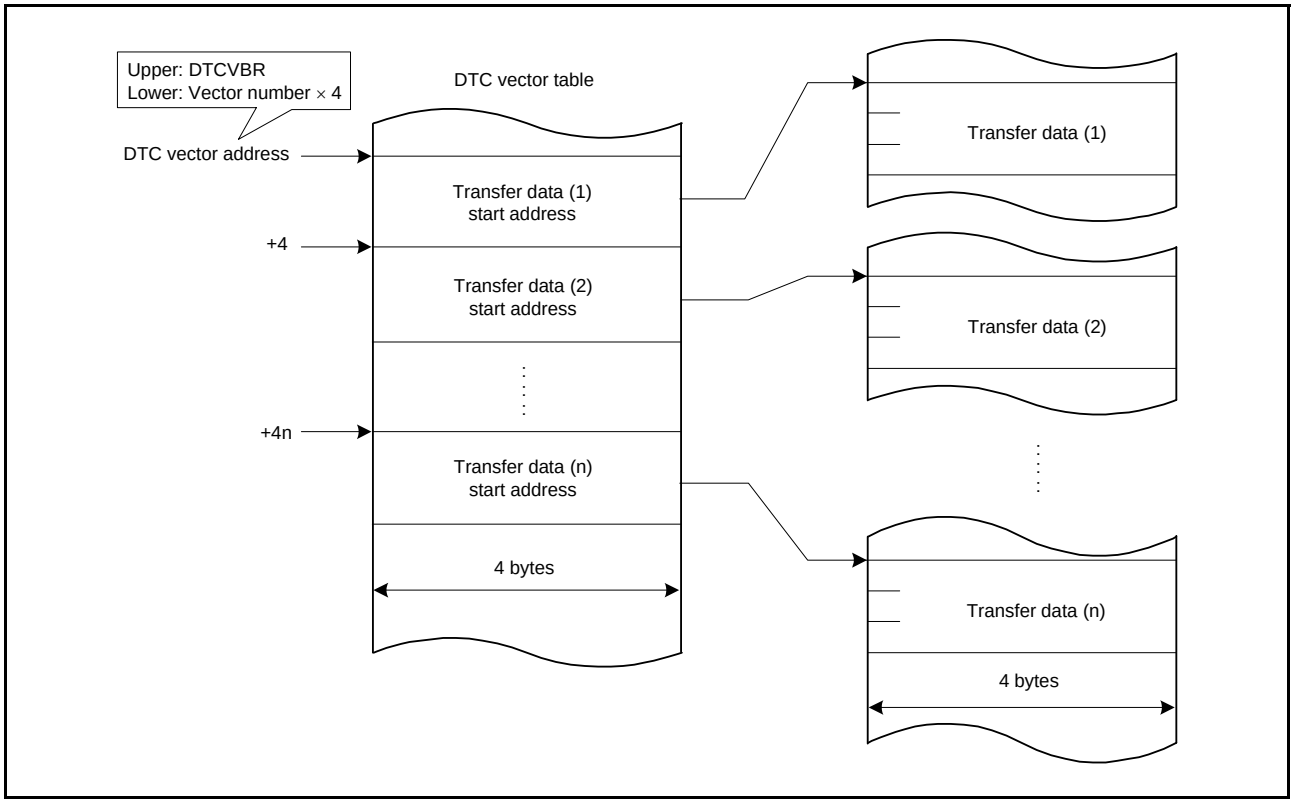


Figure 19.2 DTC Vector Table and Transfer Data

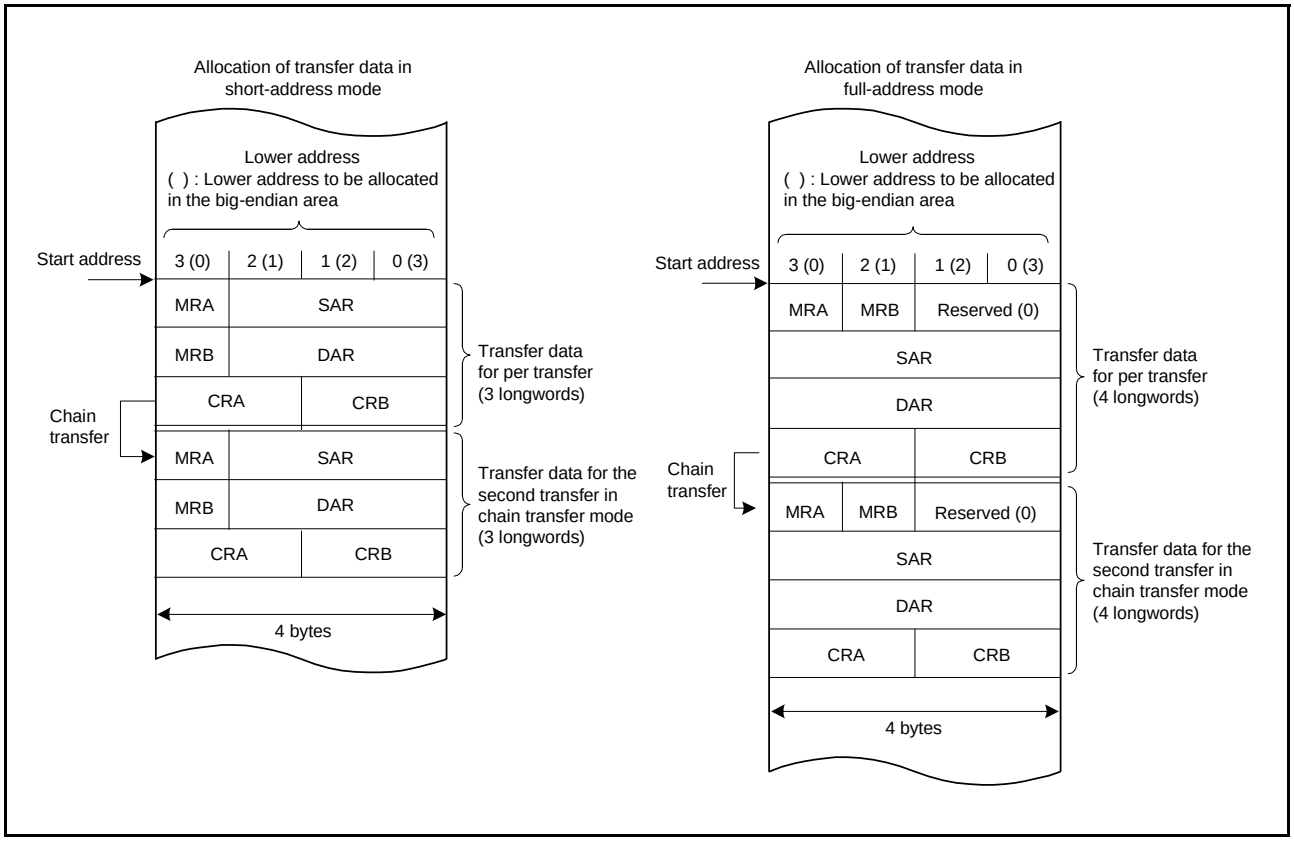


Figure 19.3 Allocation of Transfer Data in the RAM Area

19.4 Operation

The DTC transfers data in accordance with the transfer data. Storage of the transfer data in the RAM area is required before DTC operation.

When the DTC is activated, it reads the DTC vector corresponding to the vector number. Then the DTC reads transfer data from the transfer data store address pointed by the DTC vector, transfers data, and then writes back the transfer data after the data transfer. Storing transfer data in the RAM area allows data transfer of arbitrary number of channels.

There are three transfer modes: normal transfer mode, repeat transfer mode, and block transfer mode.

The DTC specifies a transfer source address in SAR and a transfer destination address in DAR. The values of these registers are incremented, decremented, or address-fixed independently after data transfer.

Table 19.2 lists transfer modes of the DTC.

Table 19.2 Transfer Modes of the DTC

Transfer Mode	Data Size Transferred on a Single Transfer Request	Increment/Decrement of Memory Address	Settable Transfer Count
Normal transfer mode	1 byte/word/longword	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte/word/longword	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes/words/longwords)	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set transfer source or transfer destination in the repeat area.
Note 2. Set transfer source or transfer destination in the block area.
Note 3. After data transfer of the specified count, the initial state is restored and the operation is continued (repeated).

Setting the CHNE bit in MRB to 1 allows multiple transfers (chain transfer) on a single startup source. Setting the CHNS bit in MRB also enables chain transfer when specified data transfer is completed.

Figure 19.4 shows the operation flowchart of the DTC. Table 19.3 lists chain transfer conditions.

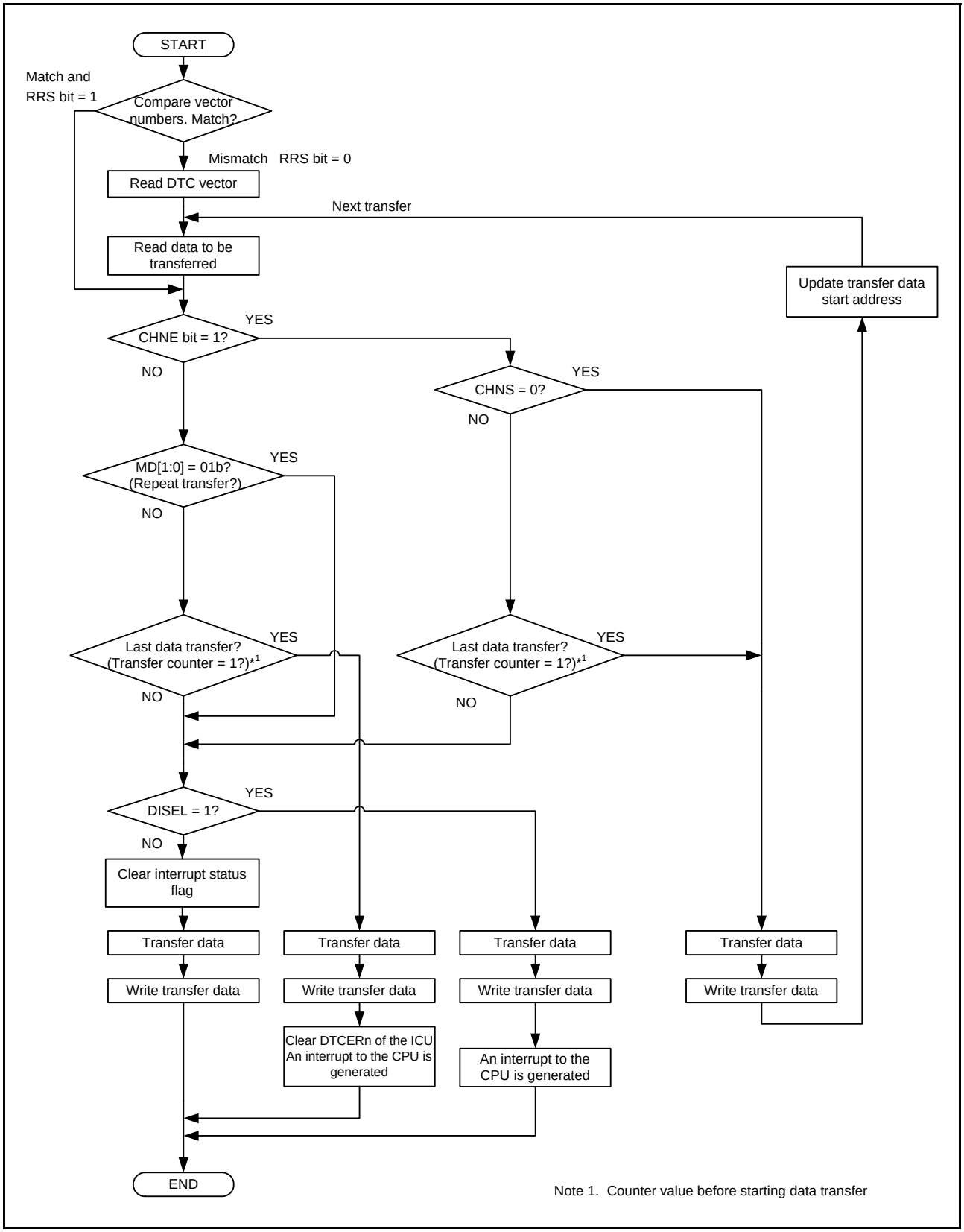


Figure 19.4 Operation Flowchart of the DTC

Table 19.3 Chain Transfer Conditions

First Transfer				Second Transfer*3				
CHNE Bit	CHNS Bit	DISEL Bit	Transfer Counter*1,*2	CHNE Bit	CHNS Bit	DISEL Bit	Transfer Counter*1,*2	DTC Transfer
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counters used depend on transfer modes as follows:
Normal transfer mode: CRA register
Repeat transfer mode: CRAL register
Block transfer mode: CRB register

Note 2. On completion of data transfer, the counters operate as follows:
1 → 0: in normal and block transfer modes
1 → CRAH: in repeat transfer mode
(1 → *) in the table indicates both of the two operations above.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The condition combination of “second transfer and CHNE bit = 1” is omitted.

19.4.1 Transfer Data Read Skip Function

Vector address read and transfer data read can be skipped by the setting of the RRS bit in DTCCR.

When a DTC startup request is generated, the current DTC vector number is always compared with the DTC vector number in the previous startup process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the vector address and transfer data. However, when the previous transfer was chain transfer, the vector address and transfer data are always read. Furthermore, when the transfer counter (CRA register) became 0 during the previous normal transfer and when the transfer counter (CRB register) became 0 during the previous block transfer, transfer data is always read regardless of the value of RRS bit. Figure 19.13 shows an example of transfer data read skip.

To update the vector table and transfer data, set the RRS bit to 0, update the vector table and transfer data, and then set the RRS bit to 1. When the RRS bit is set to 0, the retained vector number is discarded and the vector table and transfer data that are updated in the following startup process are read.

19.4.2 Transfer Data Write-Back Skip Function

When the SM[1:0] bits in MRA or the DM[1:0] bits in MRB are set to “address fixed”, a part of transfer data is not written back. This function is performed independently of the setting of short-address mode or full-address mode. Table 19.4 lists transfer data write-back skip conditions and applicable registers.
The CRA and CRB registers are always written back independently of the setting of short-address mode or full-address mode. Furthermore, in full-address mode, write-back of the MRA and MRB registers are always skipped.

Table 19.4 Transfer Data Write-Back Skip Conditions and Applicable Registers

SM[1:0] Bits in MRA		DM[1:0] Bits in MRB		SAR Register	DAR Register
b3	b2	b3	b2		
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

19.4.3 Normal Transfer Mode

This mode allows 1-byte, 1-word, or 1-longword data transfer on a single startup source. The transfer count can be set to 1 to 65536.
Transfer source addresses and transfer destination addresses can be set to increment, decrement, or fixed independently.
This mode enables an interrupt request to the CPU to be generated at the end of specified-count transfer.
Table 19.5 lists register functions in normal transfer mode, and Figure 19.5 shows the memory map of normal transfer mode.

Table 19.5 Register Functions in Normal Transfer Mode

Register	Description	Value Written Back by Writing Transfer Data
SAR	Transfer source address	Increment/decrement/fixed*1
DAR	Transfer destination address	Increment/decrement/fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

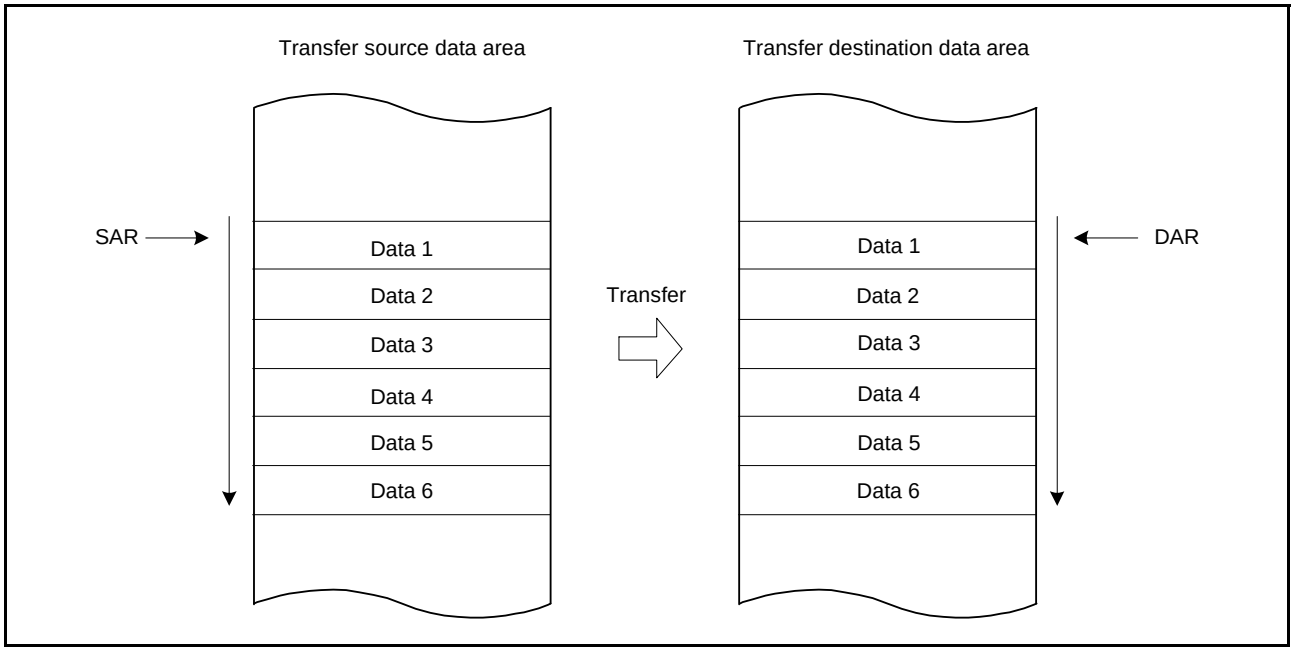


Figure 19.5 Memory Map of Normal Transfer Mode

19.4.4 Repeat Transfer Mode

This mode allows 1-byte, 1-word, or 1-longword data transfer on a single startup source.

Specify either transfer source or transfer destination for the repeat area by the DTS bit in MRB. The transfer count can be set to 1 to 256. When the specified-count transfer is completed, the initial value of the address register specified in the transfer counter and the repeat area is restored and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL is decreased to 00h in repeat transfer mode, the CRAL value is updated to the value set in CRAH. Thus the transfer counter does not become 00h, which inhibits generation of interrupt request to the CPU when the DISEL bit in MRB is set to 0 (an interrupt request to the CPU is generated when specified data transfer is completed).

Table 19.6 lists the register functions in repeat transfer mode, and Figure 19.6 shows the memory map of repeat transfer mode.

Table 19.6 Register Functions in Repeat Transfer Mode

Register	Description	Value Written Back by Writing Transfer Data	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment/decrement/fixed*1	(When the DTS bit in MRB is 0) Increment/decrement/fixed*1 (When the DTS bit in MRB is 1) SAR register initial value
DAR	Transfer destination address	Increment/decrement/fixed*1	(When the DTS bit in MRB is 0) DAR register initial value (When the DTS bit in MRB is 1) Increment/decrement/fixed*1
CRAH	Retains transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

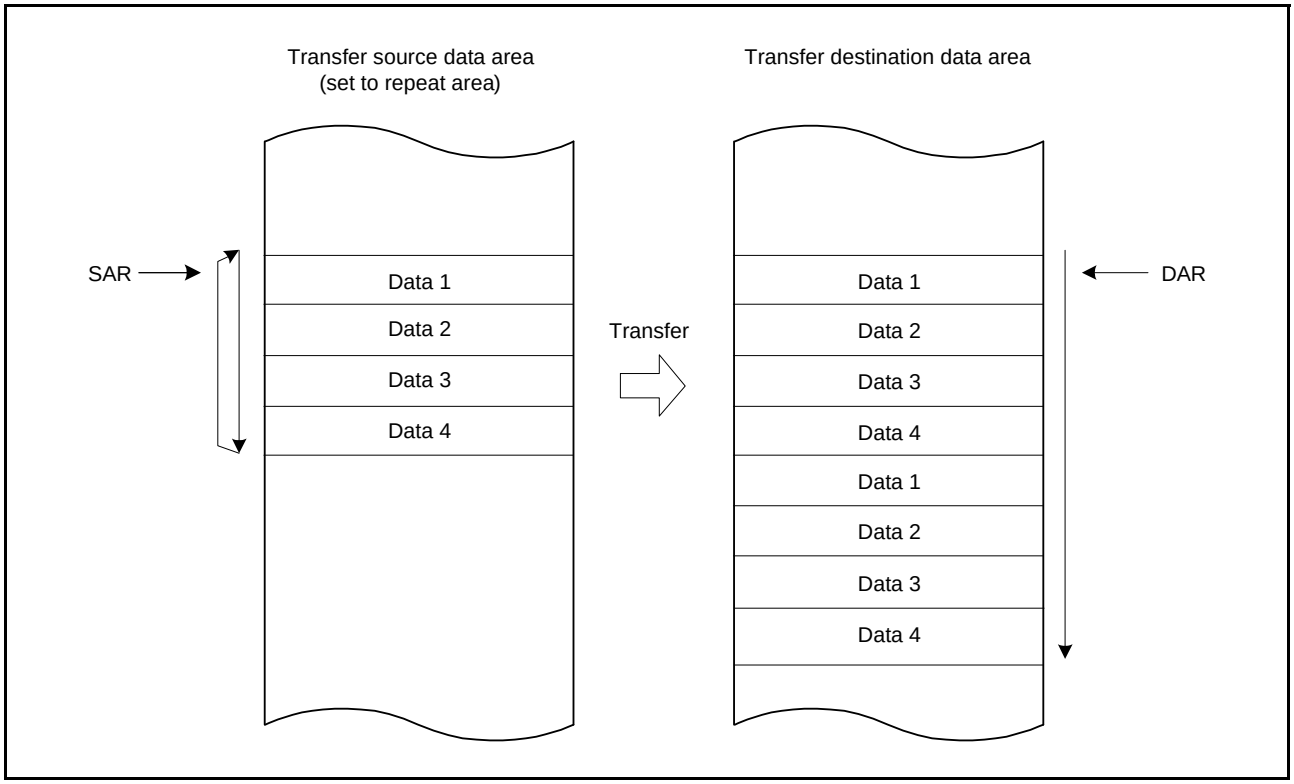


Figure 19.6 Memory Map of Repeat Transfer Mode (Transfer Source: Repeat Area)

19.4.5 Block Transfer Mode

This mode allows single-block data transfer on a single startup source.
Specify either transfer source or transfer destination for the block area by the DTS bit in MRB. The block size can be set to 1 to 256 bytes (or 1 to 256 words or 1 to 256 longwords).
When transfer of the specified one block is completed, the initial values of the block size counter CRAL and the address register (SAR when the DTS bit = 1 or DAR when the DTS bit = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.
The transfer count (block count) can be set to 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of specified-count block transfer.
Table 19.7 lists register functions in block transfer mode, and Figure 19.7 shows the memory map of block transfer mode.

Table 19.7 Register Functions in Block Transfer Mode

Register	Description	Value Written Back by Writing Transfer Data
SAR	Transfer source address	(When DTS bit in MRB is 0) Increment/decrement/fixed*1 (When DTS bit in MRB is 1) SAR register initial value
DAR	Transfer destination address	(When DTS bit in MRB is 0) DAR register initial value (When DTS bit in MRB is 1) Increment/decrement/fixed*1
CRAH	Retains block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

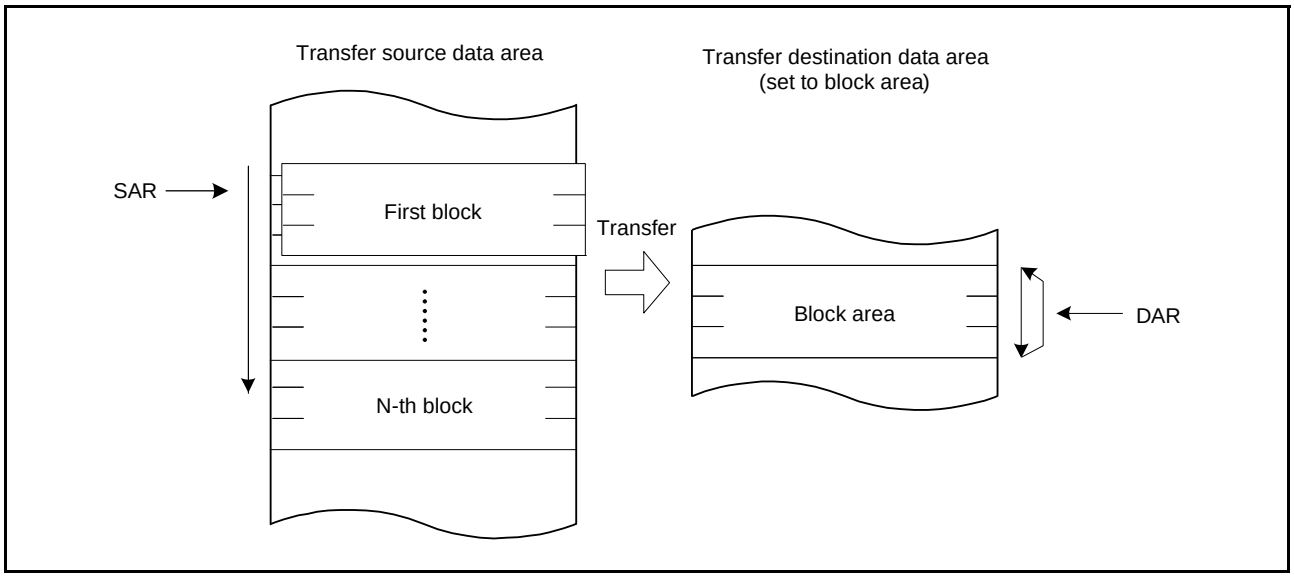


Figure 19.7 Memory Map of Block Transfer Mode (Transfer Destination: Block Area)

19.4.6 Chain Transfer

Setting the CHNE bit in MRB to 1 allows chain transfer to be performed continuously on a single startup source.
If the CHNE bit in MRB is set to 1, and the CHNS bit in MRB is set to 0, an interrupt request to the CPU is not generated by completion of specified number of rounds of transfer or by setting the DISEL bit in MRB to 1 (an interrupt request to the CPU is generated each time DTC data transfer is performed), and data transfer has no effect on the interrupt status flag that has started up the transfer.
The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define data transfer.
Figure 19.8 shows chain transfer operation.

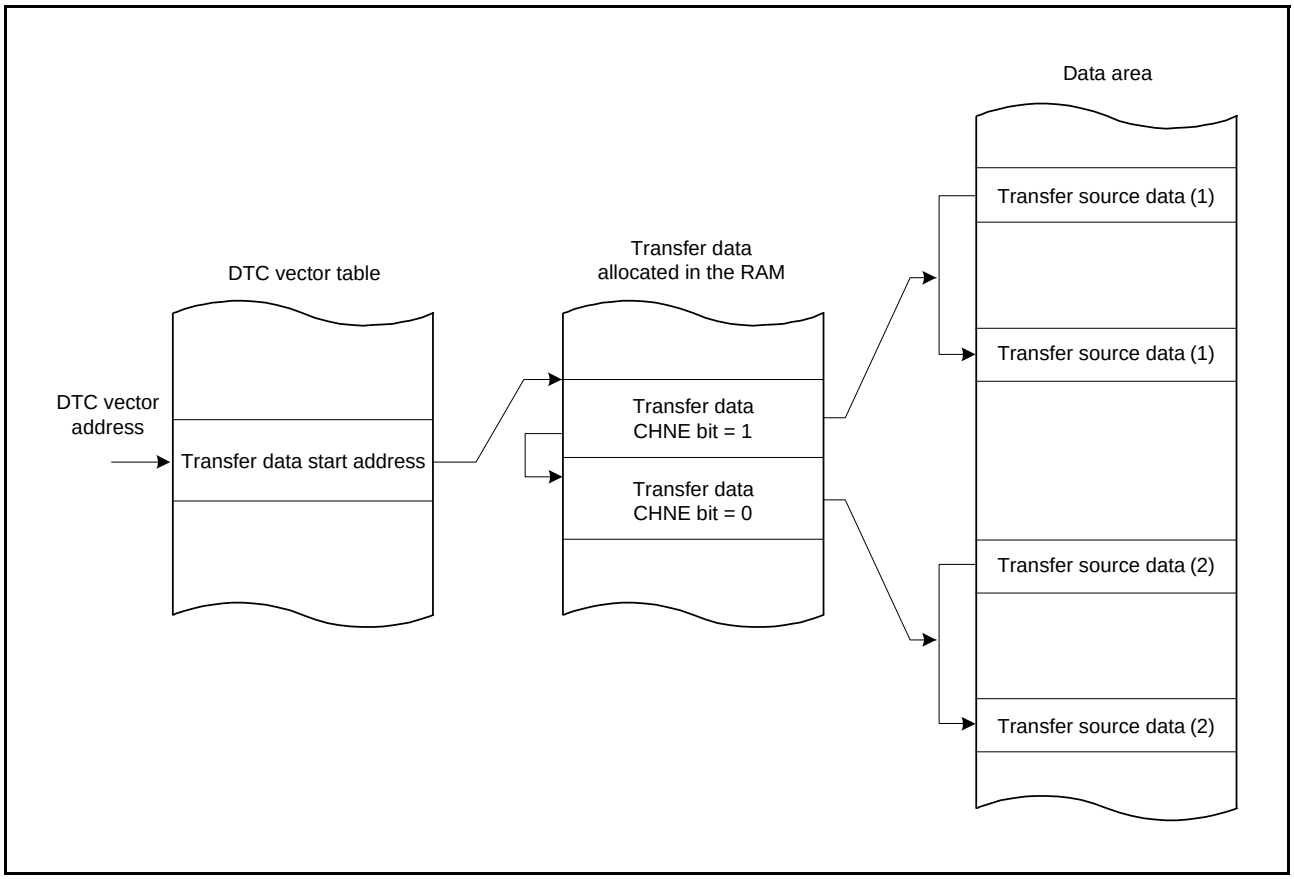


Figure 19.8 Chain Transfer Operation

Writing 1 to the CHNE and CHNS bits in MRB enables chain transfer to be performed only after completion of specified data transfer. In repeat transfer mode, chain transfer is performed after completion of specified data transfer.
For details on chain transfer conditions, see Table 19.3, Chain Transfer Conditions.

19.4.7 Operation Timing

Figure 19.9 to Figure 19.13 show examples of DTC operation timing.

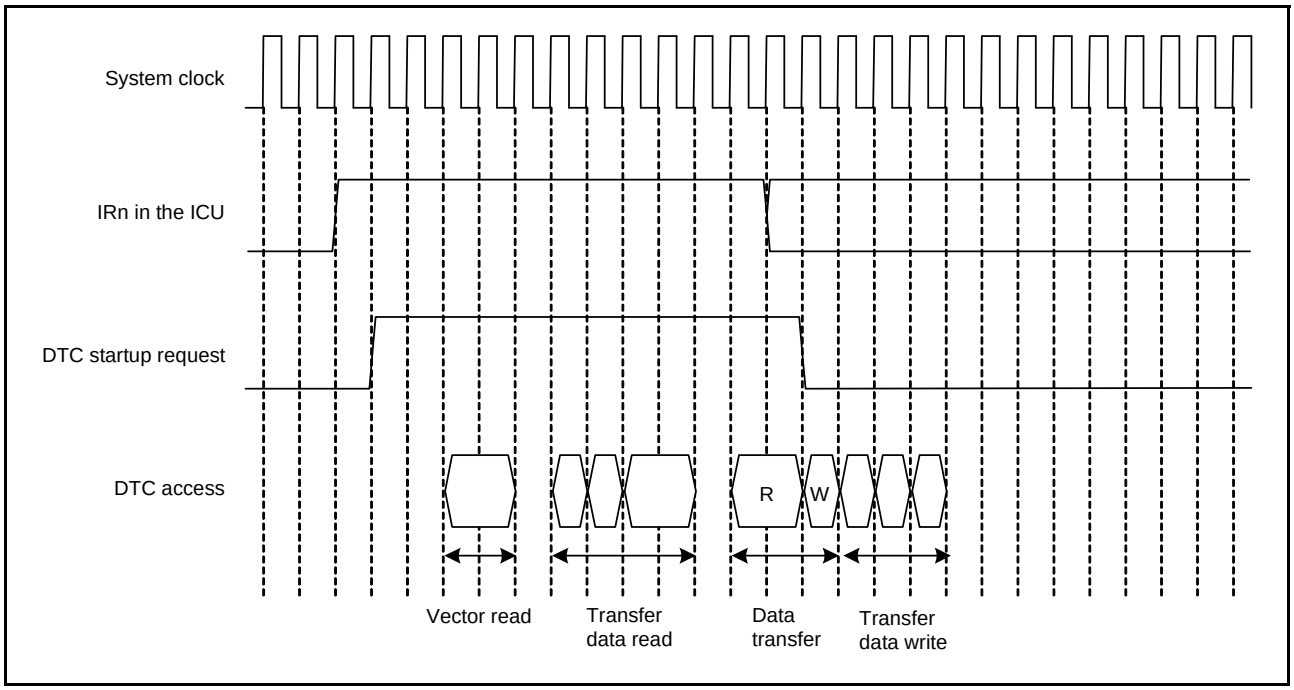


Figure 19.9 Example (1) of DTC Operation Timing (Short-Address Mode, Normal Transfer Mode, Repeat Transfer Mode)

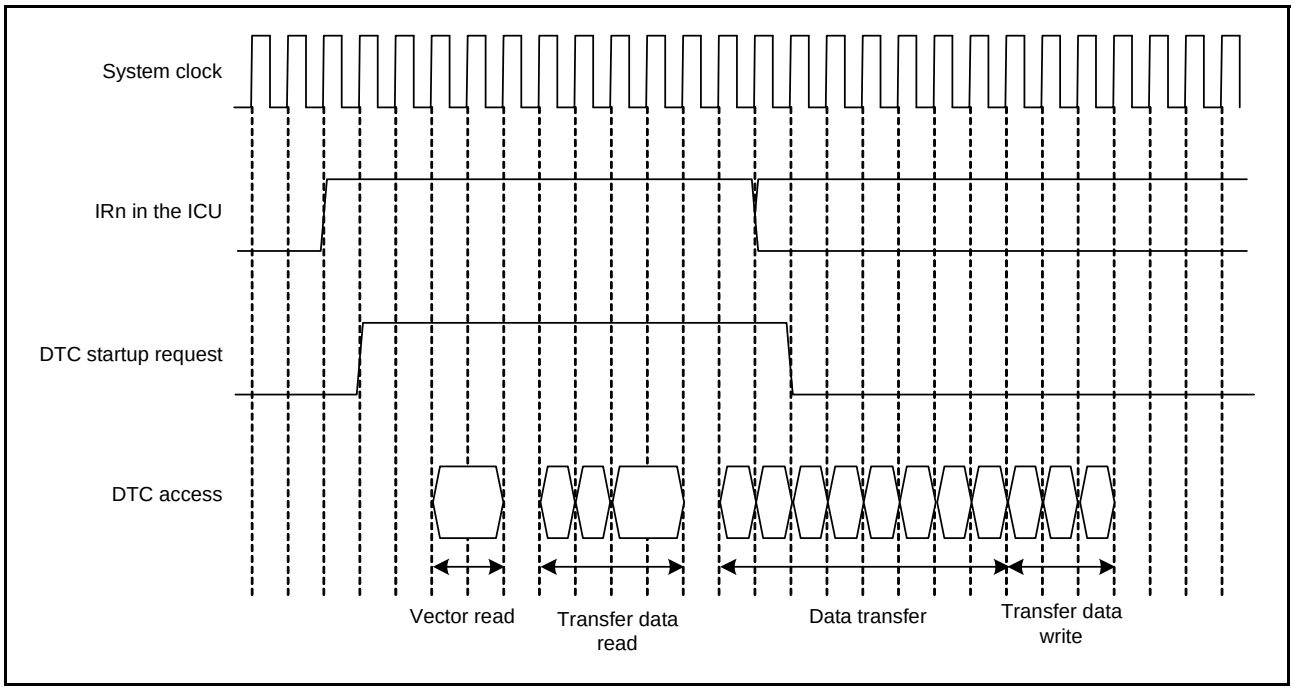


Figure 19.10 Example (2) of DTC Operation Timing (Short-Address Mode, Block Transfer Mode, Block Size = 4)

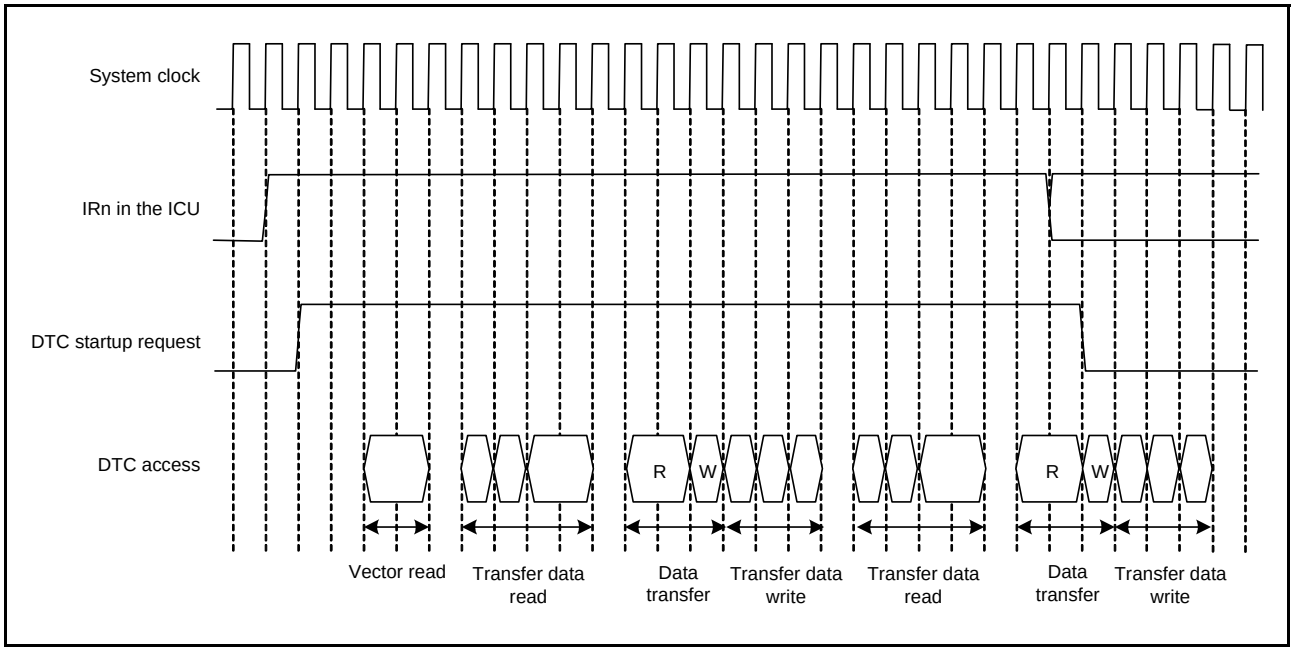


Figure 19.11 Example (3) of DTC Operation Timing (Short-Address Mode, Chain Transfer)

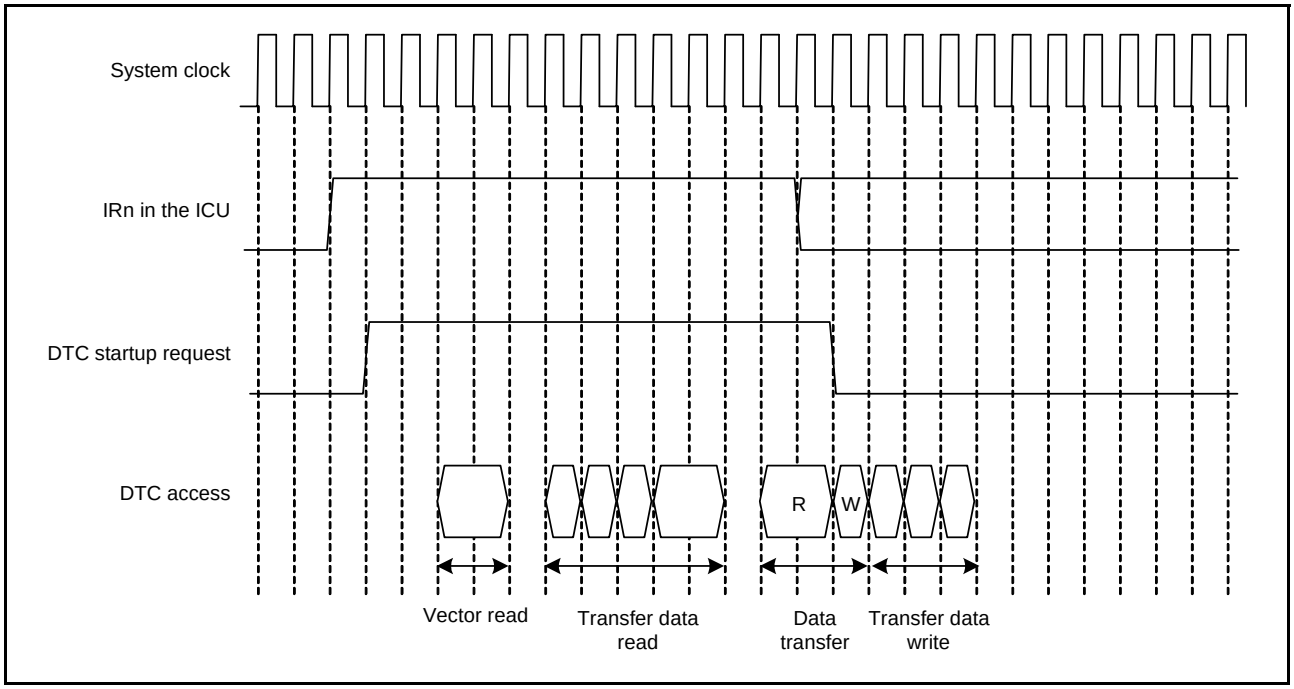


Figure 19.12 Example (4) of DTC Operation Timing (Full-Address Mode, Normal Transfer Mode, Repeat Transfer Mode)

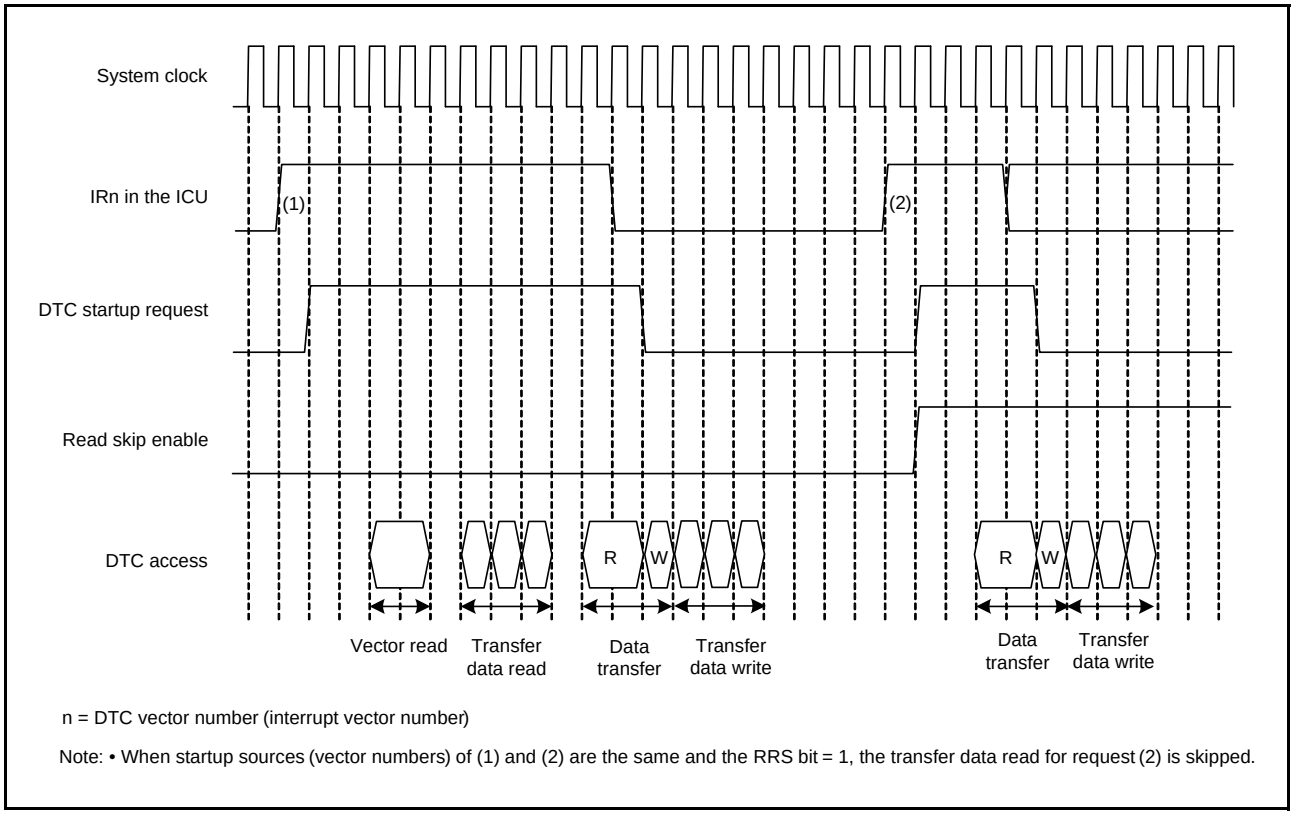


Figure 19.13 Example of Operation when Transfer Information Skip is Executed (Vector, Transfer Information, and Transfer Destination Data on the On-Chip RAM, and Transfer Source Data on the Peripheral Module)

19.4.8 Execution Cycles of the DTC

Table 19.8 lists the execution cycles of single data transfer of the DTC.
For the order of the execution states, refer to section 19.4.7, Operation Timing.

Table 19.8 Execution Cycles of the DTC

Transfer Mode	Vector Read		Transfer Data Read			Transfer Data Write			Data Transfer		Internal Operation	
									Read	Write		
Normal	Cv+1	0*1	4×Ci+1*2	3×Ci+1*3	0*1	3×Ci*4	2×Ci*5	Ci*6	Cr+1	Cw	2	0*1
Repeat									Cr+1	Cw		
Block*7									P×Cr	P×Cw		

Note 1. When transfer data read is skipped
Note 2. In full-address mode
Note 3. In short-address mode
Note 4. When neither SAR nor DAR is set to address-fixed mode
Note 5. When SAR or DAR is set to address-fixed mode
Note 6. When SAR and DAR are set to address-fixed mode
Note 7. When the block size is 2 or larger. If the block size is 1, the cycle number for normal transfer is applied.

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer data storage destination
Ci: Cycles for access to transfer data storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
(The unit is system clocks (ICLK) for “+1” in the Vector Read, Transfer Data Read, and Data Transfer Read columns and “2” in the Internal Operation ?column.)
(Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 40, RAM, section 41, Flash Memory, section 6, I/O Registers, and section 16.2.6, External Bus.)

19.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer data read and transfer data write. While transfer data is not read or written, bus arbitration is made according to the priority determined by the bus master arbitrator.
For bus arbitration, see section 16, Buses.

19.5 DTC Setting Procedure

Before using the DTC, set the DTC vector base register (DTCVBR).
Figure 19.14 shows the procedure to set the DTC.

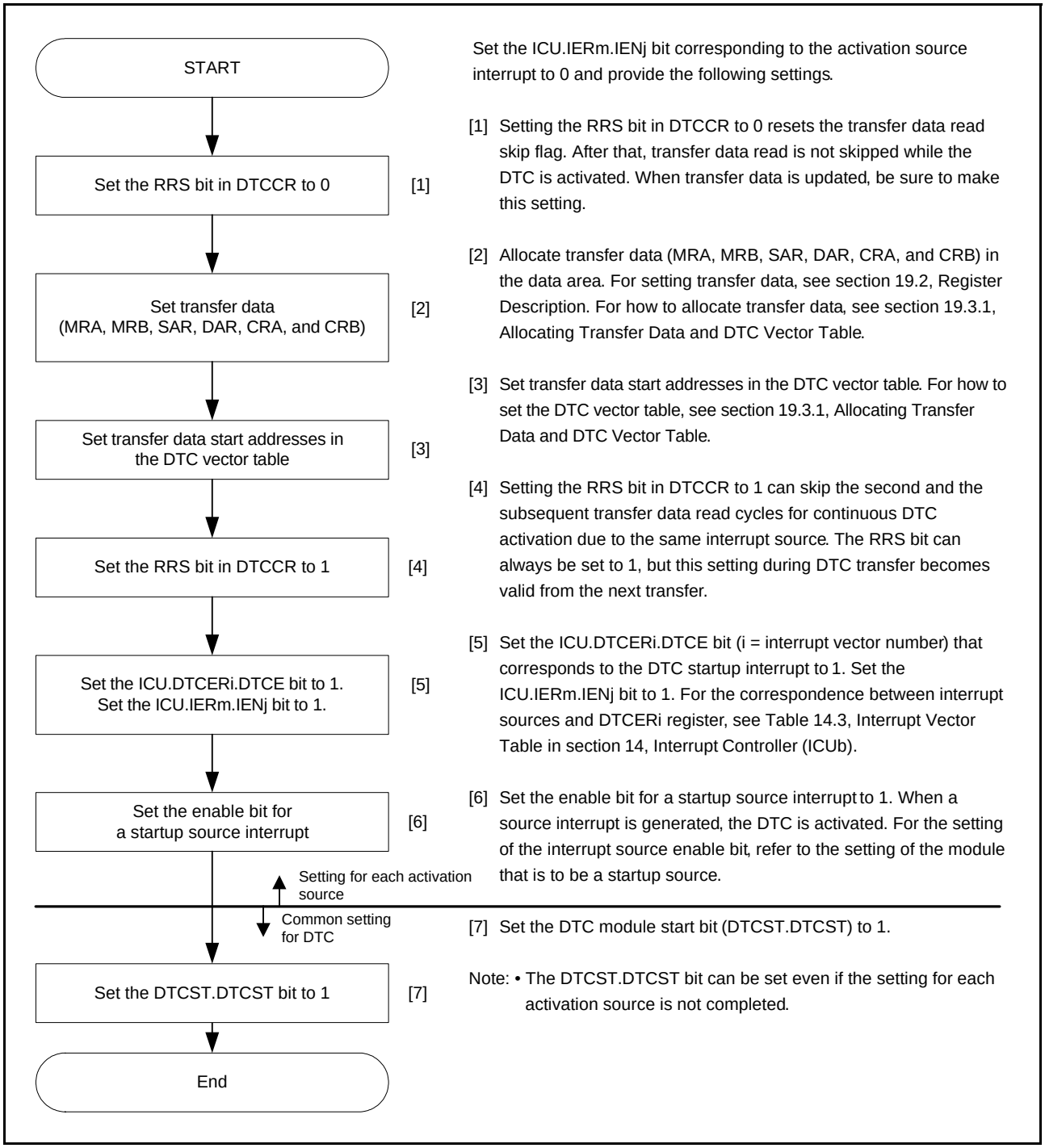


Figure 19.14 Procedure to Set the DTC

19.6 Examples of DTC Usage

19.6.1 Normal Transfer

As an example of DTC usage, its employment in the transfer of 128 bytes of data by an SCI is described below.

(1) Transfer Data Set

In the MRA register, select a fixed source address (MRA.SM[1:0] = 00b), normal transfer mode (MRA.MD[1:0] = 00b), and byte-sized transfer (MRA.SZ[1:0] = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] = 10b) and single data transfer by a single interrupt (MRB.CHNE bit = 0 and MRB.DISEL bit = 0). The MRB.DTS bit can be set to any value. Set the address of the RDR register in the SCIm (m = 0 to 12) in the SAR register, the start address of the RAM area for data storage in the DAR register, and 128 (0080h) in the CRA register. The CRB register can be set to any value.

(2) DTC Vector Table

The address where the transfer-control information for use with the RXI starts is set in the vector table for the DTC.

(3) ICU Set and DTC Module Activation

Set the corresponding ICU.DTCERi.DTCE bit to 1 and the ICU.IERi.IENj bit to 1.
Set the DTCST.DTCST bit to 1.

(4) SCI Set

Enable the receive end interrupt (RXI) by setting the SCR.RIE bit in the SCIm to 1. If a reception error occurs during the SCI receive operation, further reception is not performed. Accordingly, make settings so that the CPU can accept receive error interrupts.

(5) DTC Transfer

Every time the reception of 1 byte by the SCI is completed, an RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCIm to RAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt Handling

After 128 rounds of data transfer have been completed and the value in the CRA register becomes 0, an RXI interrupt request is generated for the CPU. Processing for completion is performed in the processing routine for this interrupt.

19.6.2 Chain Transfer when Counter = 0

The second data transfer is performed only when the counter = 0. Repeat transfer of a transfer count of 256 or more is enabled by the re-setting for the first data transfer.
The following shows an example of configuring a 128-Kbyte input buffer, where the input buffer is set so that its lower address starts with 0000h. Figure 19.15 shows a chain transfer when the counter = 0.

1. Set normal transfer mode for input data for the first data transfer. Set the following:
   Transfer source address: Fixed, CRA = 0000h (65,536 times), CHNE bit = 1 (chain transfer enabled) in MRB, CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0) in MRB, and DISEL bit = 0 (an interrupt request to the CPU is generated when specified data transfer is completed) in MRB.
2. Prepare the upper 8-bit address of the start address at every 65,536 times of the transfer destination address for the first data transfer in another area (such as ROM). For example, when setting the input buffer to 200000h to 21FFFFh, prepare 21h and 20h.
3. For the second data transfer, set repeat transfer mode (source side: repeat area) for re-setting the transfer destination address of the first data transfer. Specify the upper 8 bits of DAR in the first transfer data area for the transfer destination. At this time, set CHNE bit = 0 (chain transfer disabled) in MRB and DISEL bit = 0 (an interrupt request to the CPU is generated when specified data transfer is completed) in MRB. When setting the input buffer mentioned above to 200000h to 21FFFFh, set the transfer counter to 2.
4. The first data transfer is performed by an interrupt 65,536 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer source address of the first data transfer to 21h. The transfer counter (lower 16 bits) of the transfer destination address of the first data transfer is 0000h.
5. In succession, the first data transfer is performed by an interrupt 65,536 times specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer source address of the first data transfer to 20h. The transfer counter (lower 16 bits) of the transfer destination address of the first data transfer is 0000h.
6. Steps 4 and 5 above are repeated infinitely. Since the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

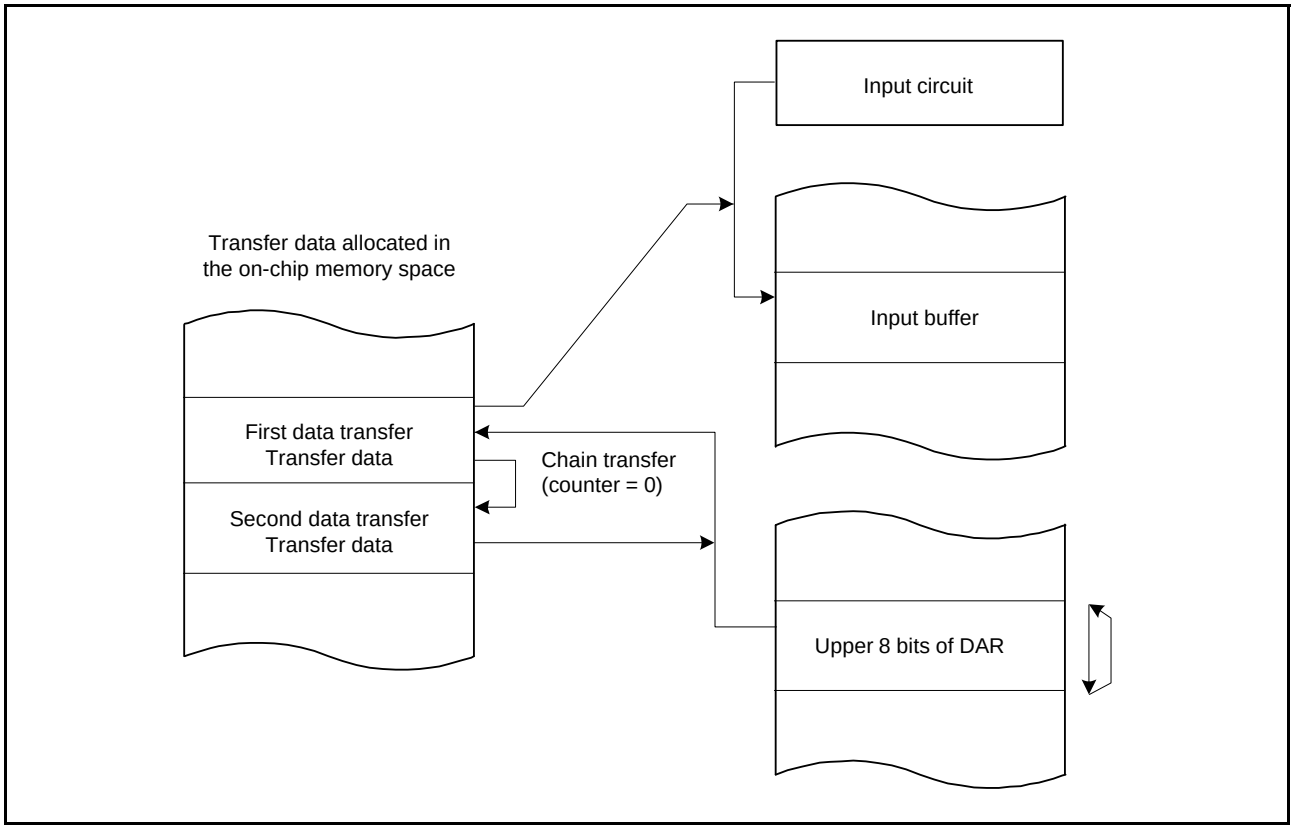


Figure 19.15 Chain Transfer when Counter = 0

19.7 Interrupt Source

When the DTC has finished data transfer of specified count or when data transfer with the DISEL bit in MRB set to 1 (an interrupt request to the CPU is generated each time DTC data transfer is performed) has been completed, an interrupt to the CPU is generated by the DTC startup source. Such interrupts to the CPU are controlled according to the PSW.I bit (interrupt enable) of the CPU, the PSW.IPL[3:0] bits (processor interrupt priority level), and the priority level of the interrupt controller.

19.8 Low-Power Consumption Function

Before transition to the module-stop state, all-module clock stop mode, software standby mode, or deep software standby mode, clear the DTCST bit in DTCST to 0 (the DTC suspended), and then perform the following.

(1) Module-Stop Function

Writing 1 to the MSTPA28 bit (transition to the module-stop state) in MSTPCRA enables the module-stop function of the DTC. If DTC transfer is in progress at the time a 1 is written to the MSTPA28 bit, the transition to the module-stop state proceeds after DTC transfer has ended. While the MSTPA28 bit is 1, accessing the DTC registers are prohibited. Writing 0 to the MSTPA28 bit releases the DTC from the module-stop state.

(2) All-Module Clock-Stop Mode

Make settings in accord with the procedure under section 12.5.2.1, Transition to All-Module Clock Stop Mode, in section 12, Low Power Consumption.
If DTC transfer operations are in progress at the time the WAIT instruction is executed, the transition to all-module clock stop mode follows the completion of DTC transfer.
The DTC is released from the module-stop state by writing 0 to the MSTPCRA.MSTPA28 bit following recovery from all-module clock stop mode.

(3) Software Standby and Deep Software Standby Modes

Make settings in accord with the procedure under section 12.5.3.1, Transition to Software Standby Mode, or section 12.5.4.1, Transition to Deep Software Standby Mode, in section 12, Low Power Consumption.
If DTC transfer operations are in progress at the time the WAIT instruction is executed, the transition to software standby or deep software standby follows the completion of DTC transfer.

(4) Notes on Low-Power Consumption Function

For the WAIT instruction and the register setting procedure, section 12.6.6, Timing of Wait Instructions in section 12, Low Power Consumption.
To perform DTC transfer after returning from low-power consumption mode, set the DTCST bit in DTCST to 1 again.
To use a request that is generated in all-module clock stop mode and software standby mode as an interrupt request to the CPU but not as a DTC startup request, specify the CPU as the interrupt request destination in accordance with the description in section 15.5.3, Selecting Interrupt Request Destinations in section 15, Interrupt controller (ICUb), and then execute the WAIT instruction.

19.9 Usage Notes

19.9.1 Transfer Data Start Address/Source Address/Destination Address

Be sure to set multiples of 4 for the transfer data start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

19.9.2 Allocating Transfer Data

Allocate transfer data in the memory area according to the endian of the area as shown in Figure 19.16.
For example, when writing CRA and CRB setting data with 16 bits in big endian, write the CRA setting data to lower address 0 and the CRB setting data to lower address 2. In little endian, write the CRB setting data to lower address 0 and the CRA setting data to lower address 2. When writing CRA and CRB setting data with 32 bits, place the CRA setting data at the MSB side and the CRB setting data at the LSB side regardless of endian, and then write the data to lower address 0.

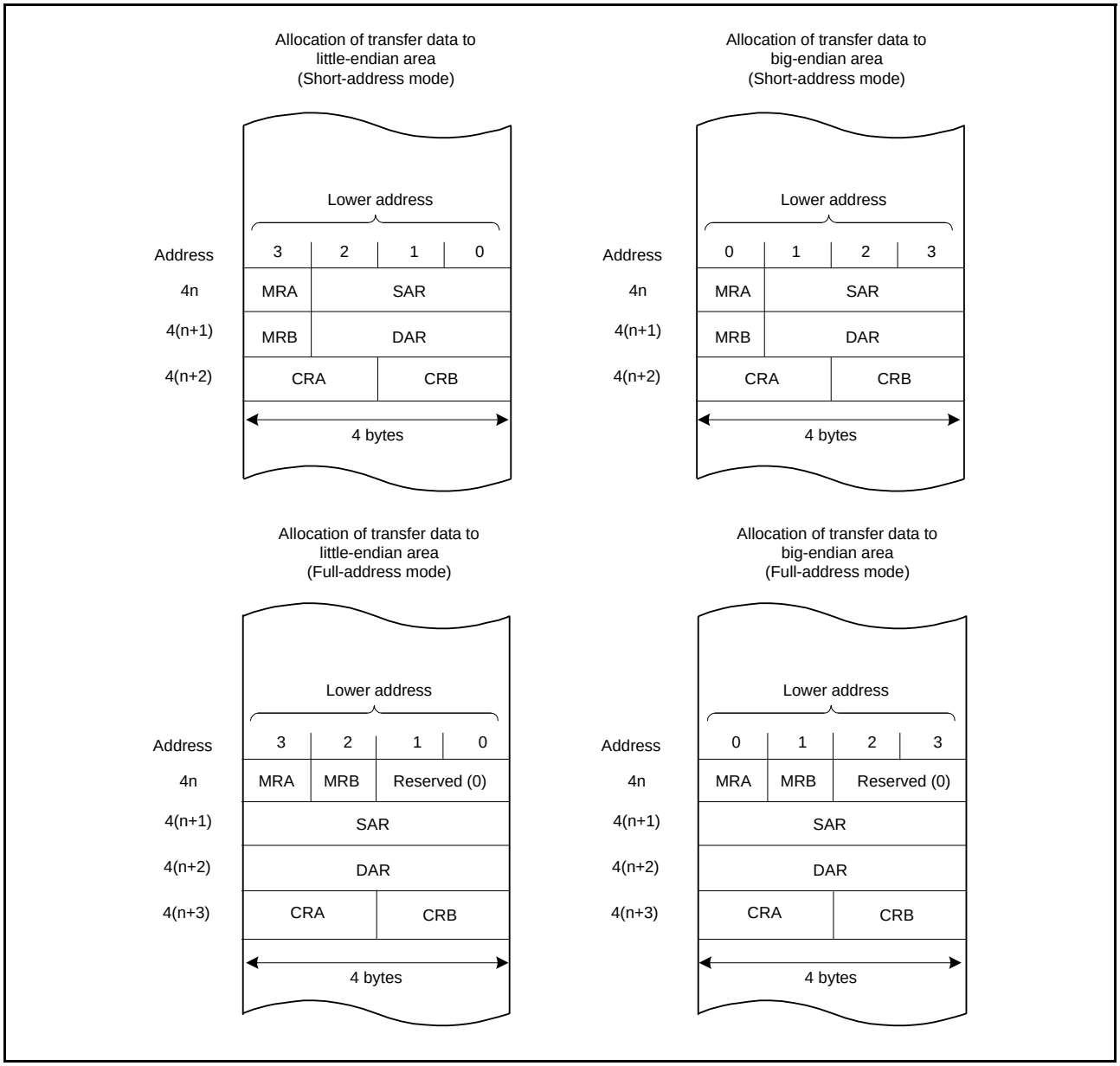


Figure 19.16 Allocation of Transfer Data

19.9.3 Setting the DTC Activation Enable Register (ICU.DTCERn) of the Interrupt controller

The DMAC should not be activated by setting the DMAC activation request select register (ICU.DMRSRn (n = number of DMAC channel)) to the same vector number that has been specified by setting the ICU.DTCERn register to 1 (DTC transfer enable). For details on the ICU.DTCERn and ICU.DMRSRn registers (n = number of DMACA channel), refer to section 15, Interrupt controller (ICUb).

20. I/O Ports

20.1 Overview

The I/O ports of this MCU function as a programmable I/O port, an I/O pin of a peripheral module, an input pin for an interrupt, or a bus control pin.

Each pin is also configurable as an I/O pin of a peripheral module or an input pin for an interrupt. All pins function as input pins immediately after a reset, and pin functions are switched by register settings. The setting of each pin is specified by the registers for the corresponding I/O port and peripheral modules.

Each port has the port direction register (PDR) that selects input or output direction, the port output data register (PODR) that holds data for output, the port input data register (PIDR) that indicates the pin states, the open drain control register y (ODRy, y = 0, 1) that selects the output type of each pin, the driving ability control register (DSCRy, y = 1, 2) that selects the driving ability, and the port mode register (PMR) that specifies the pin function of each port.

For details on the PMR register, see section 21, Multi-Function Pin Controller (MPC).

The configuration of the I/O ports differs depending on the package. Table 20.1 lists the specifications of I/O ports, and Table 20.2 lists the port functions.

Table 20.1 Specifications of I/O Ports

Port	Package		Package		Package		Package		Package		Package	
	144 Pins	Number of Pin	120 Pins	Number of Pin	112 Pins	Number of Pin	100 Pins	Number of Pin	64 Pins	Number of Pin	48 Pins	Number of Pin
PORT0	P00 to P05	6	P00, P01	2	P00, P01, P04, P05	4	P00, P01	2	P00, P01	2	Not provided	0
PORT1	P10 to P14	5	P10 to P13	4	P10 to P12	3	P10, P11	2	P10, P11	2	Not provided	0
PORT2	P20 to P26	7	P20 to P26	7	P20 to P24	5	P20 to P24	5	P22 to P24	3	P22 to P24	3
PORT3	P30 to P35	6	P30 to P33	4	P30 to P33	4	P30 to P33	4	P30 to P33	4	P30	1
PORT4	P40 to P47	8	P40 to P47	8	P40 to P47	8	P40 to P47	8	P40 to P47	8	P40 to P44, P47	6
PORT5	P50 to P57	8	P50 to P55	6	P50 to P55	6	P50 to P55	6	Not provided	0	Not provided	0
PORT6	P60 to P65	6	P60 to P65	6	P60 to P65	6	P60 to P65	6	Not provided	0	Not provided	0
PORT7	P70 to P76	7	P70 to P76	7	P70 to P76	7	P70 to P76	7	P70 to P76	7	P70 to P76	7
PORT8	P80 to P82	3	P80 to P82	3	P80 to P82	3	P80 to P82	3	Not provided	0	Not provided	0
PORT9	P90 to P96	7	P90 to P96	7	P90 to P96	7	P90 to P96	7	P91 to P94	4	Not provided	0
PORTA	PA0 to PA6	7	PA0 to PA5	6	PA0 to PA5	6	PA0 to PA5	6	PA2 to PA5	4	PA2, PA3	2
PORTB	PB0 to PB7	8	PB0 to PB7	8	PB0 to PB7	8	PB0 to PB7	8	PB0 to PB7	8	PB0 to PB6	7
PORTC	PC0 to PC5	6	Not provided	0	Not provided	0	Not provided	0	Not provided	0	Not provided	0
PORTD	PD0 to PD7	8	PD0 to PD7	8	PD0 to PD7	8	PD0 to PD7	8	PD3 to PD7	5	PD3 to PD7	5
PORTE	PE0 to PE5	6	PE0 to PE5	6	PE0 to PE5	6	PE0 to PE5	6	PE2	1	PE2	1
PORTF	PF0 to PF4	5	PF0 to PF3	4	PF2 to PF4	3	Not provided	0	Not provided	0	Not provided	0
PORTG	PG0 to PG6	7	PG0 to PG6	7	PG0 to PG5	6	Not provided	0	Not provided	0	Not provided	0
	Total of Pins	110	Total of Pins	93	Total of Pins	90	Total of Pins	78	Total of Pins	48	Total of Pins	32

Table 20.2 Port Functions [144-, 120-, 112- and 100-Pin Versions] (1/2)

Port	Pin	Open Drain Output	Driving Ability Switching	Large-Current Output Pin
PORT0	P00, P01	—	○	—
	P02, P03	○	—	—
	P04	—	—	—
	P05	—	○	—
PORT1	P10	—	—	—
	P11, P12	—	○	—
	P13, P14	—	—	—
PORT2	P20, P21	—	○	—
	P22, P23	○	○	—
	P24, P25	—	○	—
	P26	○	○	—
PORT3	P30 to P33	—	○	—
	P34, P35	○	—	—
PORT4	P40 to P47 (input)			
PORT5	P50, P51 (input)			
	P52, P53 (input)		○	
	P54 to P57 (input)			
PORT6	P60 to P65 (input)		○	
PORT7	P70	—	○	—
	P71 to P76	—	Fixed to high driving ability output	○
PORT8	P80, P81	○	○	—
	P82	—	—	—
PORT9	P90 to P94	—	Fixed to high driving ability output	○
	P95	○	Fixed to high driving ability output	○
	P96	○	○	—
PORTA	PA0	—	○	—
	PA1, PA2	○	○	—
	PA3	—	○	—
	PA4, PA5	○	○	—
	PA6	—	○	—
PORTB	PB0	—	○	—
	PB1, PB2	○	—	—
	PB3, PB4	—	○	—
	PB5, PB6	○	○	—
	PB7	—	○	—
PORTC	PC0 to PC5 (input)			
PORTD	PD0 to PD2	—	○	—
	PD3	○	—	—
	PD4	—	—	—
	PD5	○	—	—
	PD6, PD7	—	○	—
PORTE	PE0, PE1	—	○	—
	PE2 (input)			
	PE3 to PE5	—	○	—

Table 20.2 Port Functions [144-, 120-, 112- and 100-Pin Versions] (2/2)

Port	Pin	Open Drain Output	Driving Ability Switching	Large-Current Output Pin
PORTF	PF0, PF1	—	—	—
	PF2	○	○	—
	PF3	○	—	—
	PF4	—	○	—
PORTG	PG0, PG1	○	—	—
	PG2	—	—	—
	PG3, PG4	○	—	—
	PG5	—	—	—
	PG6	—	○	—

Open drain output is only available when an SCIn function where n = 0 to 3 or 12 is selected.
Switching of driving ability is available for other signals on pins that also function as general I/O pins.

Table 20.3 Port Functions [64- and 48-Pin Versions]

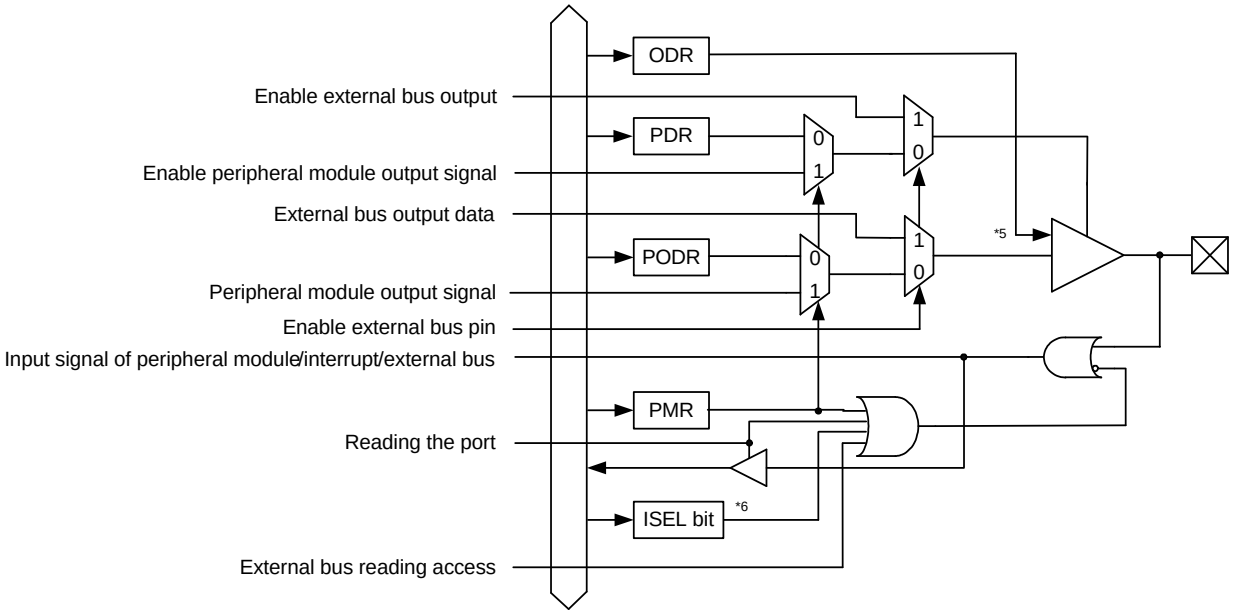
Port	Pin	Open Drain Output	5-V Tolerant
PORT0	P00, P01	—	○
PORT1	P10, P11	—	○
PORT2	P22, P23	—	○
	P24	○	○
PORT3	P30	○	○
	P31 to P34	—	○
PORT4	P40 to P47	—	—
PORT7	P70 to P76	—	○
PORT9	P91, P92	—	○
	P93, P94	○	○
PORTA	PA2 to PA5	—	○
PORTB	PB0, PB3, PB4, PB7	—	○
	PB1, PB2, PB5, PB6	○	○
PORTD	PD3, PD5	○	○
	PD4, PD6, PD7	—	○
PORTE	PE2	—	—

Specifying input pull-up, open-drain output, switching of driving ability, or 5-V tolerance is available for other signals on pins that also function as general I/O pins.

20.2 I/O Port Configuration

20.2.1 144-, 120-, 112, and 100-Pin Versions

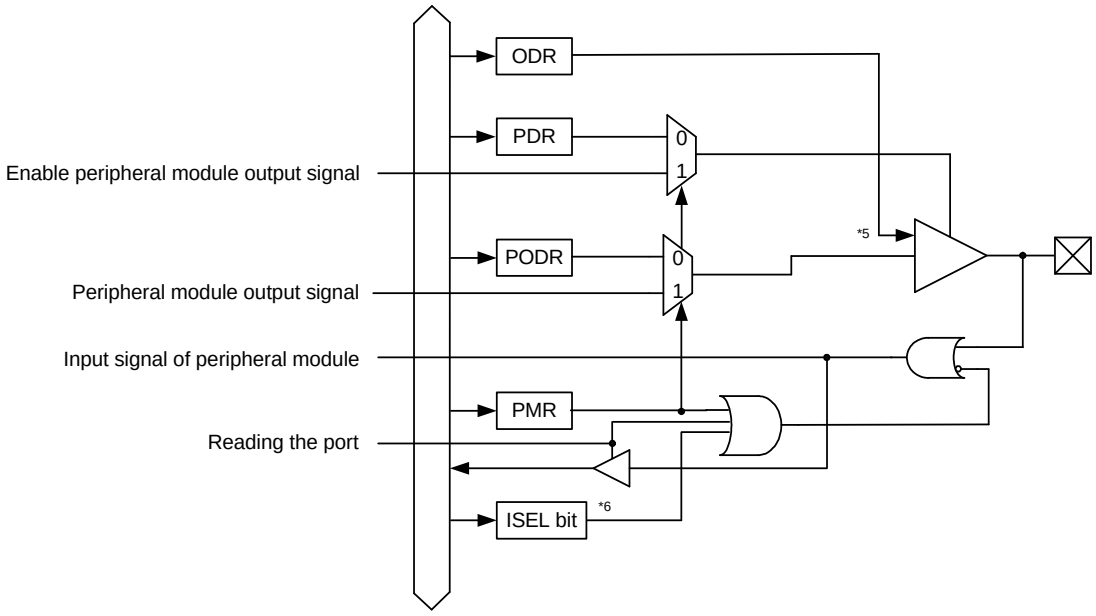
Port 0: P00, P01, P05*2
Port 1: P11, P12*4
Port 2: P20 to P24, P25*3, P26*3
Port 3: P30 to P33
Port 7: P70 to P76
Port 8: P80 to P82
Port 9: P96
Port A: A6*1
Port B: PB0, PB3 to PB7
Port D: PD0 to PD2
Port E: PE0, PE1, PE3 to PE5
Port F: PF2*4, PF4*2
Port G: PG6*4



Note 1. Not provided on the 120-pin, 112-pin, and 100-pin products
Note 2. Not provided on the 120-pin and 100-pin products
Note 3. Not provided on the 112-pin and 100-pin products
Note 4. Not provided on the 100-pin product
Note 5. Control signal for N-channel open drain. This is only present for pins capable of open drain output.
Note 6. An external interrupt function is multiplexed on this pin.

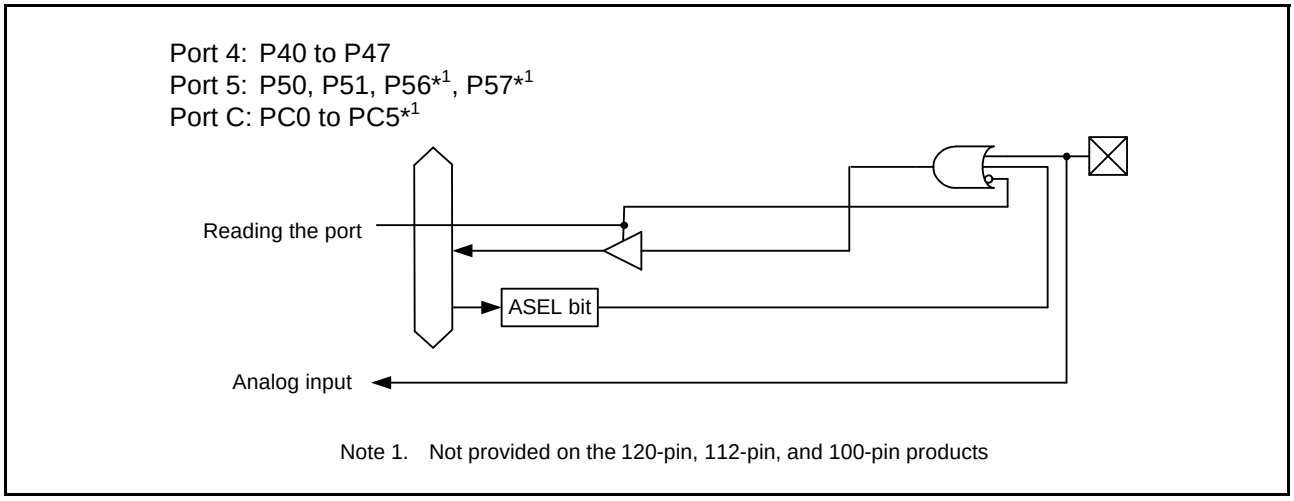
Figure 20.1 I/O Port Configuration (1)

Port 0: P02 *1, P03 *1, P04*2
Port 1: P10, P13*3, P14*1
Port 3: P34*1, P35*1
Port 9: P90 to P95
Port A: PA0 to PA5
Port B: PB1, PB2
Port D: PD3 to PD7
Port F: PF0*3, PF1*3, PF3*4
Port G: PG0 to PG5*4



Note 1. Not provided on the 120-pin, 112-pin, and 100-pin products
Note 2. Not provided on the 120-pin and 100-pin products
Note 3. Not provided on the 112-pin and 100-pin products
Note 4. Not provided on the 100-pin product
Note 5. Control signal for N-channel open drain
This is only present for pins capable of open drain output
Note 6. An external interrupt function is multiplexed on this pin.

Figure 20.2 I/O Port Configuration (2)



Note 1. Not provided on the 120-pin, 112-pin, and 100-pin products

Figure 20.3 I/O Port Configuration (3)

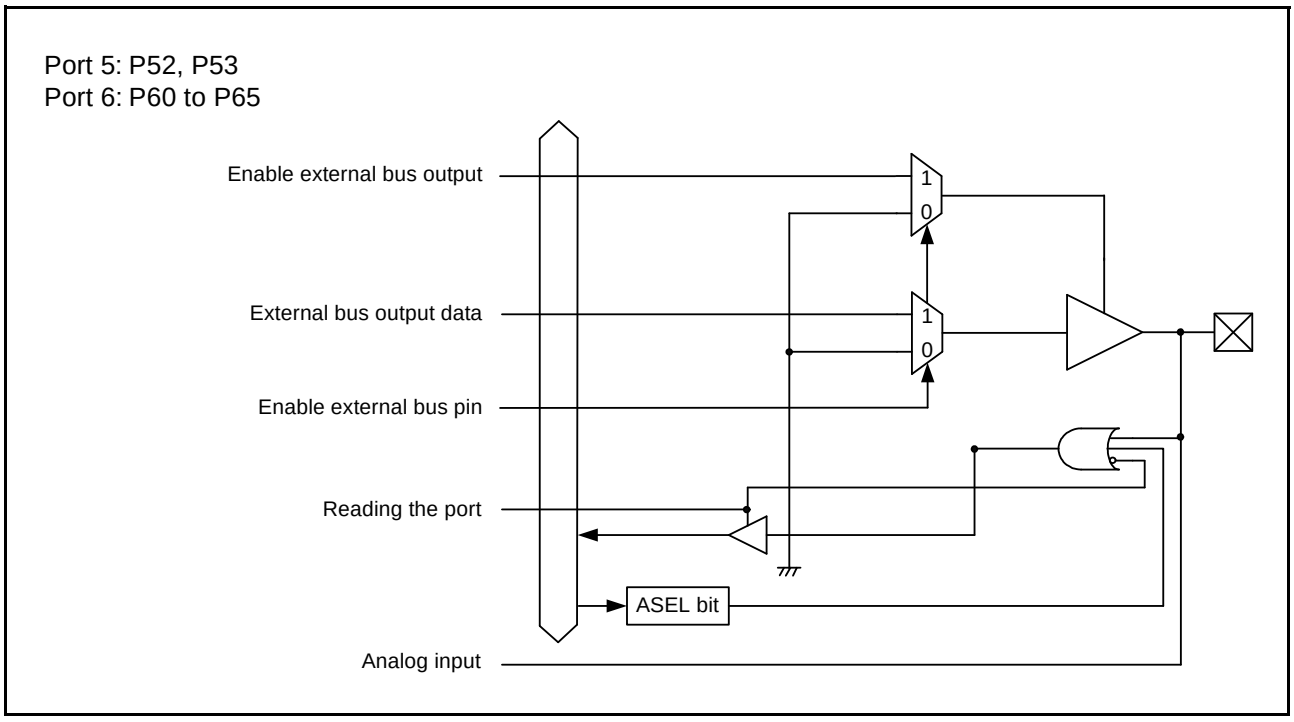


Figure 20.4 I/O Port Configuration (4)

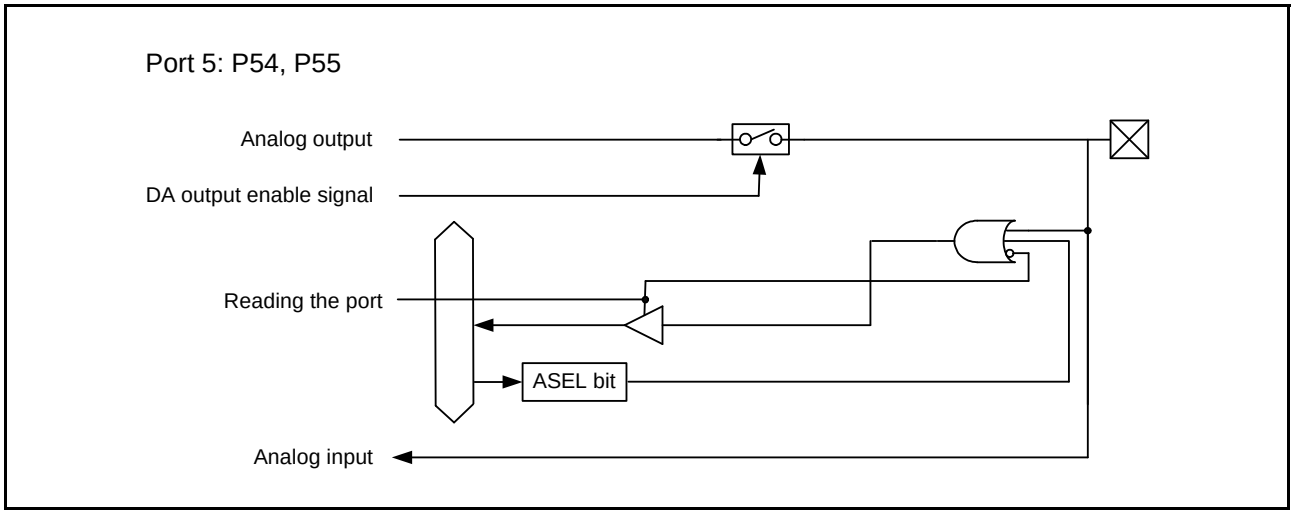


Figure 20.5 I/O Port Configuration (5)

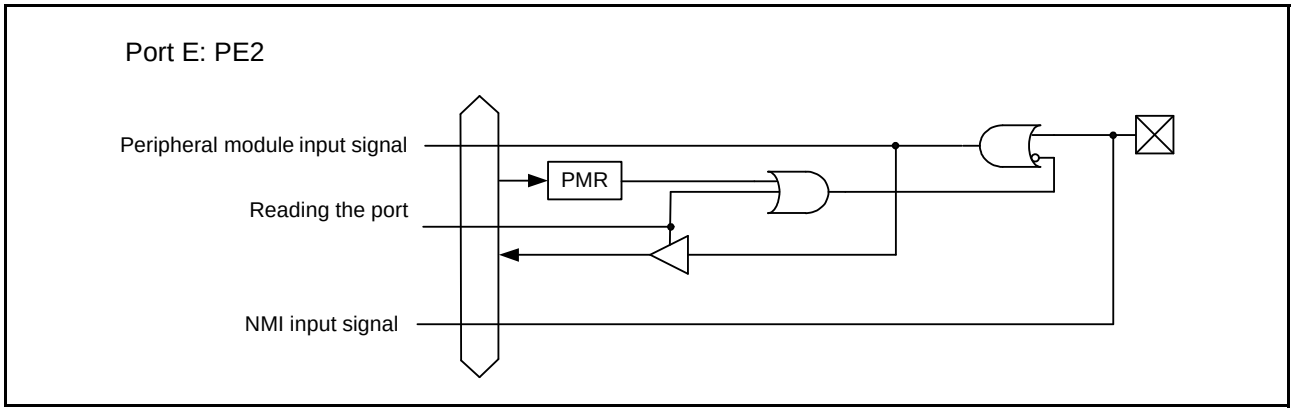
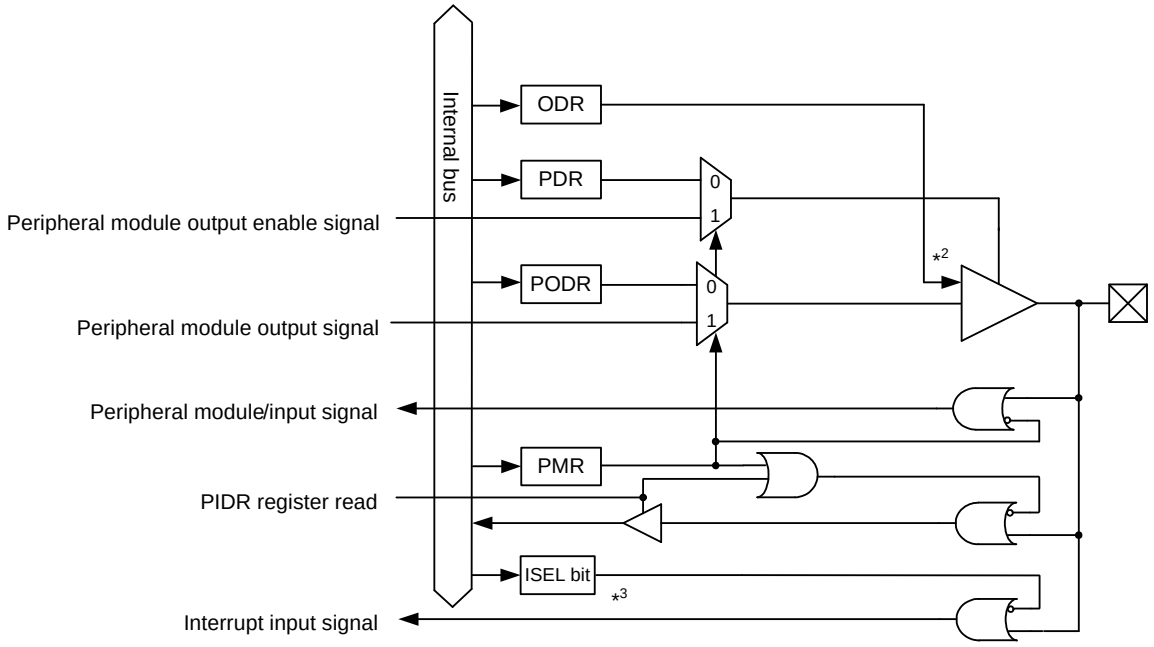


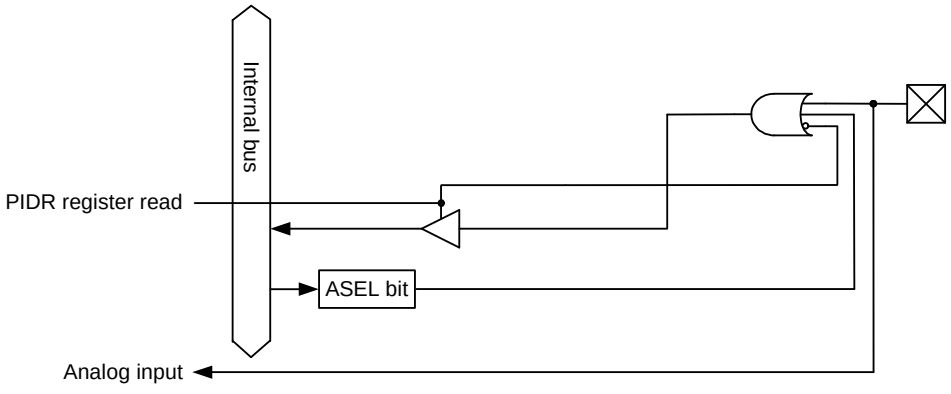
Figure 20.6 I/O Port Configuration (6)

20.2.2 64- and 48-Pin Versions

Port 0: P00*1, P01*1
Port 1: P10*1, P11*1
Port 2: P22 to P24
Port 3: P30, P31 to P33*1
Port 7: P70 to P76
Port 9: P91 to P94*1
Port A: PA2, PA3, PA4*1, PA5*1
Port B: PB0 to PB6, PB7*1
Port D: PD3 to PD7



Port 4: P40 to 44, P45*1, P46*1, P47



Note 1. Not provided on 48-pin LQFP.
Note 2. Control signal (pin with open drain function) for N-channel open drain
Note 3. Pin with external interrupt function

Figure 20.7 I/O Port Configuration (1)

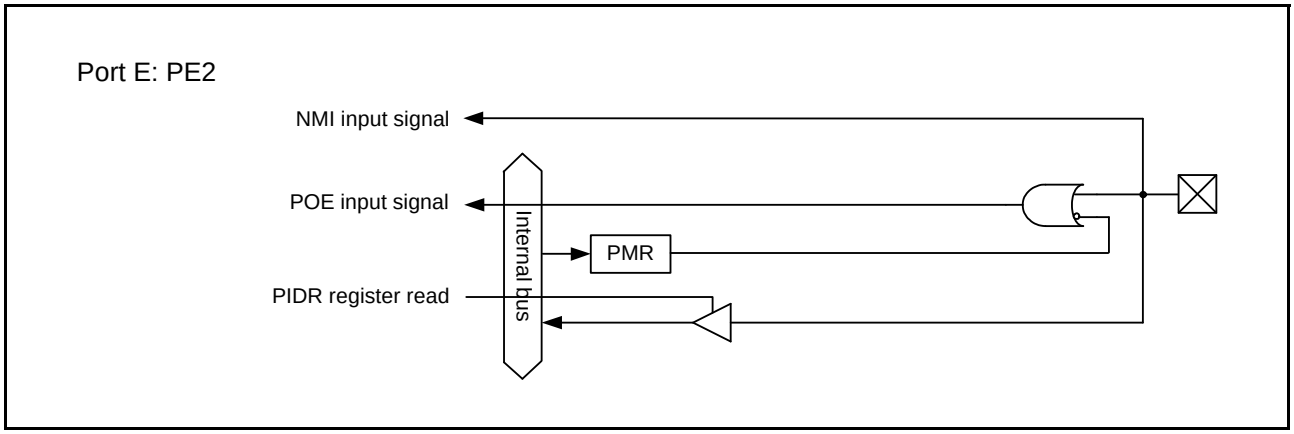


Figure 20.8 I/O Port Configuration (2)

20.3 Register Descriptions

20.3.1 Port Direction Register (PDR)

Address(es): PORT0.PDR 0008 C000h, PORT1.PDR 0008 C001h, PORT2.PDR 0008 C002h, PORT3.PDR 0008 C003h, PORT7.PDR 0008 C007h, PORT8.PDR 0008 C008h, PORT9.PDR 0008 C009h, PORTA.PDR 0008 C00Ah, PORTB.PDR 0008 C00Bh, PORTD.PDR 0008 C00Dh, PORTE.PDR 0008 C00Eh, PORTF.PDR 0008 C00Fh, PORTG.PDR 0008 C010h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 I/O Select	0: Input (Functions as an input pin.) 1: Output (Functions as an output pin.)	R/W
b1	B1	Pm1 I/O Select		R/W
b2	B2	Pm2 I/O Select		R/W
b3	B3	Pm3 I/O Select		R/W
b4	B4	Pm4 I/O Select		R/W
b5	B5	Pm5 I/O Select		R/W
b6	B6	Pm6 I/O Select		R/W
b7	B7	Pm7 I/O Select		R/W

m = 0 to 3, 7 to 9, A, B, D to G

PDR is a register which is used to select the input or output direction for individual pins of the corresponding port when the pins are configured as the general I/O pins.
Each bit of PORTm.PDR corresponds to each pin of port m; I/O direction can be specified in 1-bit units.
The B2 bit in PORTE.PDR is reserved, because the PE2 pin is input only. The bit corresponding to a pin that does not exist is also reserved. A reserved bit is read as 0. The write value should be 0.

20.3.2 Port Output Data Register (PODR)

Address(es): PORT0.PODR 0008 C020h, PORT1.PODR 0008 C021h, PORT2.PODR 0008 C022h, PORT3.PODR 0008 C023h, PORT7.PODR 0008 C027h, PORT8.PODR 0008 C028h, PORT9.PODR 0008 C029h, PORTA.PODR 0008 C02Ah, PORTB.PODR 0008 C02Bh, PORTD.PODR 0008 C02Dh, PORTE.PODR 0008 C02Eh, PORTF.PODR 0008 C02Fh, PORTG.PODR 0008 C030h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Output Data Store	0: Low output 1: High output	R/W
b1	B1	Pm1 Output Data Store		R/W
b2	B2	Pm2 Output Data Store		R/W
b3	B3	Pm3 Output Data Store		R/W
b4	B4	Pm4 Output Data Store		R/W
b5	B5	Pm5 Output Data Store		R/W
b6	B6	Pm6 Output Data Store		R/W
b7	B7	Pm7 Output Data Store		R/W

m = 0 to 3, 7 to 9, A, B, D to G

PODR is a register which holds the data to be output from the pins used for general I/O.
The B2 bit in PORTE.PODR is reserved, because the PE2 pin is input only. Data is not output from the corresponding pins even if these bits are set. The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

20.3.3 Port Input Data Register (PIDR)

Address(es): PORT0.PIDR 0008 C040h, PORT1.PIDR 0008 C041h, PORT2.PIDR 0008 C042h, PORT3.PIDR 0008 C043h, PORT4.PIDR 0008 C044h, PORT5.PIDR 0008 C045h, PORT6.PIDR 0008 C046h, PORT7.PIDR 0008 C047h, PORT8.PIDR 0008 C048h, PORT9.PIDR 0008 C049h, PORTA.PIDR 0008 C04Ah, PORTB.PIDR 0008 C04Bh, PORTC.PIDR 0008 C04Ch, PORTD.PIDR 0008 C04Dh, PORTE.PIDR 0008 C04Eh, PORTF.PIDR 0008 C04Fh, PORTG.PIDR 0008 C050h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0	0: Low input 1: High input	R
b1	B1	Pm1		R
b2	B2	Pm2		R
b3	B3	Pm3		R
b4	B4	Pm4		R
b5	B5	Pm5		R
b6	B6	Pm6		R
b7	B7	Pm7		R

m = 0 to 9, A to G

PIDR is a register which reflects individual pin states of the port.

The pin states of port m can be read with the PORTm.PIDR, regardless of the values of PORTm.PDR and PORTm.PMR.

The states of pins of ports 4 to 6 and C can only be read when the ASEL bit is 0.

The NMI pin state is reflected in the PE2 bit.

The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as undefined, and cannot be modified.

20.3.4 Port Mode Register (PMR)

Address(es): PORT0.PMR 0008 C060h, PORT1.PMR 0008 C061h, PORT2.PMR 0008 C062h, PORT3.PMR 0008 C063h, PORT7.PMR 0008 C067h, PORT8.PMR 0008 C068h, PORT9.PMR 0008 C069h, PORTA.PMR 0008 C06Ah, PORTB.PMR 0008 C06Bh, PORTD.PMR 0008 C06Dh, PORTE.PMR 0008 C06Eh, PORTF.PMR 0008 C06Fh, PORTG.PMR 0008 C070h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Pin Mode Control	0: Uses the pin as a general I/O pin. 1: Uses the pin as an I/O port for peripheral functions.	R/W
b1	B1	Pm1 Pin Mode Control		R/W
b2	B2	Pm2 Pin Mode Control		R/W
b3	B3	Pm3 Pin Mode Control		R/W
b4	B4	Pm4 Pin Mode Control		R/W
b5	B5	Pm5 Pin Mode Control		R/W
b6	B6	Pm6 Pin Mode Control		R/W
b7	B7	Pm7 Pin Mode Control		R/W

m = 0 to 3, 7 to 9, A, B, D to G

Each bit of PORTm.PMR corresponds to each pin of port m; pin function can be specified in 1-bit units.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

20.3.5 Open Drain Control Register 0 (ODR0)

Address(es): PORT0.ODR0 0008 C080h, PORT2.ODR0 0008 C084h, PORT3.ODR0 0008 C086h, PORT8.ODR0 0008 C090h, PORT9.ODR0 0008 C092h, PORTA.ODR0 0008 C094h, PORTB.ODR0 0008 C096h, PORTD.ODR0 0008 C09Ah, PORTF.ODR0 0008 C09Eh, PORTG.ODR0 0008 C0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	B6	—	B4	—	B2	—	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Output Type Select (m = 3, 8, G)	These bits select the method of output when the selected pin function is for SCIn where n = 0 to 3 or 12. 0: CMOS output 1: N-channel open-drain output	R/W
b1	—	Reserved		R/W
b2	B2	Pm1 Output Type Select (m = 8, A, B, G)		R/W
b3	—	Reserved		R/W
b4	B4	Pm2 Output Type Select (m = 0, 2, A, B, F)		R/W
b5	—	Reserved		R/W
b6	B6	Pm3 Output Type Select (m = 0, 2, 9, D, F, G)		R/W
b7	—	Reserved		R/W

The odd bits in the ODR0 register (b1, b3, b5, and b7) are reserved.

The bit corresponding to a pin that does not exist is also reserved. A reserved bit is read as 0. The write value should be 0.

20.3.6 Open Drain Control Register 1 (ODR1)

Address(es): PORT2.ODR1 0008 C085h, PORT3.ODR1 0008 C087h, PORT9.ODR1 0008 C093h, PORTA.ODR1 0008 C095h, PORTB.ODR1 0008 C097h, PORTD.ODR1 0008 C09Bh, PORTG.ODR1 0008 C0A1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	B4	—	B2	—	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm4 Output Type Select (m = 2, 3, A, G)	These bits select the method of output when the selected pin function is for SCIn where n = 0 to 3 or 12. 0: CMOS output 1: N-channel open-drain output	R/W
b1	—	Reserved		R/W
b2	B2	Pm5 Output Type Select (m = 3, 9, A, B, D)		R/W
b3	—	Reserved		R/W
b4	B4	Pm6 Output Type Select (m = 2, 9, B)		R/W
b7 to b5	—	Reserved		R/W

The bits b1, b3, and b5 to b7 in the ODR1 register are reserved.

The bit corresponding to a pin that does not exist is also reserved. A reserved bit is read as 0. The write value should be 0.

20.3.7 Driving Ability Control Register 1 (DSCR1)

Address(es): DSCR1 0008 C0F2h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	0: Normal drive output 1: High-drive output	R/W
b1	B1	BCLK (PE5) Pin Driving Ability Control		R/W
b2	B2	CS0 (PD1, P26), CS1 (P25, PF2), CS2 (PD2, PG6, P05), CS3 (P12, PF4, PA6) WR1/BC1 (PE0), ALE (P11) Pins Driving Ability Control		R/W
b3	B3	CS1 (P00), RD (P01), WR0/WR (PE1), BC0 (P65: multiplexed with A0) Pins Driving Ability Control		R/W
b4	B4	A7 (P52), A6 (P53), A5 (P60), A4 (P61), A3 (P62), A2 (P63), A1 (P64), A0 (P65) Pins Driving Ability Control		R/W
b5	B5	A19 (PB7), A18 (PB6), A17 (PB5), A16 (PB4), A15 (PB3), A14 (PB0), A13 (P96), A12 (PD0), A11 (PE3), A10 (PE4), A9 (P80), A8 (P81) Pins Driving Ability Control		R/W
b6	B6	D7 (P33), D6 (P70) Pins Driving Ability Control		R/W
b7	B7	D15 (P20), D14 (P21), D13 (P22), D12 (P23), D11 (P24), D10 (P30), D9 (P31), D8 (P32) Pins Driving Ability Control		R/W

DSCR1 controls switching of port driving ability.

Driving ability of the corresponding pin is changed whether or not it is being used for an external expansion signal.

The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

20.3.8 Driving Ability Control Register 2 (DSCR2)

Address(es): DSCR2 0008 C0F3h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved		R/W
b6	B6	RSPI Pins (MISOn, SSLn0 to SSLn3) Driving Ability Control MISOn: P22, PA5, PD1 SSLn0: P30, PA3, PD6 SSLn1: P31, PA2, PD7 SSLn2: P32, PA1, PE0 SSLn3: P33, PA0, PE1	0: Normal drive output 1: High-drive output	R/W
b7	B7	RSPI Pins (RSPCKn, MOSIn) Driving Ability Control RSPCKn: P24, PA4, PD0 MOSIn: P23, PB0, PD2	0: Normal drive output 1: High-drive output	R/W

n = A, B

DSCR2 controls switching of the driving ability for port pins on which RSPI pin functions are multiplexed.
Driving ability of the corresponding pin is changed whether or not the RSPI pin function is in use.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

20.4 Handling of Unused Pins

Table 20.4 lists handling of unused pins.

Table 20.4 Handling of Unused Pins

Pin	Handling Description
EMLE	Connect to VSS through resistor (pull-down)
MD	(Used as a mode pin)
RES#	Connect to VCC through resistor (pull-up)
USB0_DP	Keep the pin open
USB0_DM	
USB0_DPUPE	
PE2/NMI	Connect to VCC through resistor (pull-up)
XTAL	Keep the pin open
EXTAL	Connect to VSS through resistor (pull-down)
Ports 0 to 3, 7 to 9, A, B, C, D to G	Set PORTn.PMR to the initial value (input buffer disabled), and set the PmnPFS.ISEL bit to the initial value. • If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to VCC (pulled up) via a resistor or to VSS (pulled down) via a resistor.*1 • If the direction setting is for output (PORTn.PDR = 1), the pin is released.*1, *2
Port 4	Connect to AVCC0 through resistor (pull-up) or connect to AVSS0 through resistor (pull-down) per pin
Ports 5, 6, and C	Connect to AVCC through resistor (pull-up) or connect to AVSS through resistor (pull-down) per pin
VREFH0	Connect to AVCC0
VREFL0	Connect to AVSS0
VREF	Connect to AVCC

Note 1. Clear the PORTn.PMR bit, the PmnPFS.ISEL bit and the PmnPFS.ASEL bit to 0.
Note 2. In the case of release when the setting is for output, the port is an input over the period from release from the reset state to the pin becoming an output. Since the voltage on the pin is undefined while it is an input, this may lead to an increase in the current drawn.

20.5 Usage Notes

20.5.1 Products with Fewer than 144 Pins

Note that bits that correspond to port m on the 144-pin product but do not exist on a product with fewer pins are read as undefined.

21. Multi-Function Pin Controller (MPC)

21.1 Overview

The multi-function pin controller (MPC) selects and assigns input/output of peripheral functions and interrupt input signals from multiple ports. The MPC also assigns the port of external bus related signals.

Table 21.1 lists the functions assigned to each multiplexed pin. The symbols ○ and × in the table indicate whether the pin is available or unavailable for the package. Selecting a single function for multiple pins is prohibited.

Table 21.1 Functions Assigned to Each Multiplexed Pin (1/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package					
				144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
Interrupt		NMI (input)	PE2	○	○	○	○	○	○
Interrupt	IRQ0	IRQ0-DS (input)	P10	○	○	○	○	○	×
		IRQ0 (input)	PB5	×	×	×	×	○	○
			PE5	○	○	○	○	×	×
			PG0	○	○	○	×	×	×
	IRQ1	IRQ1-DS (input)	P11	○	○	○	○	○	×
		IRQ1 (input)	P93	×	×	×	×	○	×
			PE4	○	○	○	○	×	×
			PG1	○	○	○	×	×	×
	IRQ2	IRQ2-DS (input)	P00	×	×	×	×	○	×
			PE3	○	○	○	○	×	×
		IRQ2 (input)	PB6	○	○	○	○	×	×
			PG2	○	○	○	×	×	×
	IRQ3	IRQ3-DS (input)	PB4	○	○	○	○	○	○
		IRQ3 (input)	P34	○	×	×	×	×	×
			P82	○	○	○	○	○	○
	IRQ4	IRQ4-DS (input)	P01	×	×	×	×	○	×
			P96	○	○	○	○	×	×
		IRQ4 (input)	P24	○	○	○	○	×	×
			PB1	○	○	○	○	×	×
	IRQ5	IRQ5-DS (input)	P70	○	○	○	○	○	○
		IRQ5 (input)	P80	○	○	○	○	×	×
			PF2	○	○	○	×	×	×
	IRQ6	IRQ6-DS (input)	P21	○	○	○	○	×	×
		IRQ6 (input)	PD5	○	○	○	○	×	×
			PG4	○	○	○	×	×	×
	IRQ7	IRQ7-DS (input)	P20	○	○	○	○	×	×
		IRQ7(input)	P03	○	×	×	×	×	×
			PE0	○	○	○	○	×	×
Multi-function timer pulse unit 3	MTU0	MTIOC0A (input/output)	P31	○	○	○	○	○	×
			PB3	○	○	○	○	○	○
		MTIOC0B (input/output)	P30	○	○	○	○	○	○
			PB2	○	○	○	○	○	○
		MTIOC0C (input/output)	PB1	○	○	○	○	○	○
		MTIOC0D (input/output)	PB0	○	○	○	○	○	○
	MTU1	MTIOC1A (input/output)	PA5	○	○	○	○	○	×
		MTIOC1B (input/output)	PA4	○	○	○	○	○	×
	MTU2	MTIOC2A (input/output)	PA3	○	○	○	○	○	○
		MTIOC2B (input/output)	PA2	○	○	○	○	○	○
	MTU3	MTIOC3A (input/output)	P33	○	○	○	○	○	×
		MTIOC3B (input/output)	P71	○	○	○	○	○	○
		MTIOC3C (input/output)	P32	○	○	○	○	○	×
		MTIOC3D (input/output)	P74	○	○	○	○	○	○

Table 21.1 Functions Assigned to Each Multiplexed Pin (2/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package					
				144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
Multi-function timer pulse unit 3	MTU4	MTIOC4A (input/output)	P72	○	○	○	○	○	○
		MTIOC4B (input/output)	P73	○	○	○	○	○	○
		MTIOC4C (input/output)	P75	○	○	○	○	○	○
		MTIOC4D (input/output)	P76	○	○	○	○	○	○
	MTU5	MTIC5U (input)	P24	×	×	×	×	○	○
			P82	○	○	○	○	×	×
		MTIC5V (input)	P23	×	×	×	×	○	○
			P81	○	○	○	○	×	×
		MTIC5W (input)	P22	×	×	×	×	○	○
			P80	○	○	○	○	×	×
	MTU6	MTIOC6A (input/output)	P33	×	×	×	×	○	×
			PA1	○	○	○	○	×	×
		MTIOC6B (input/output)	P71	×	×	×	×	○	○
			P95	○	○	○	○	×	×
		MTIOC6C (input/output)	P32	×	×	×	×	○	×
			PA0	○	○	○	○	×	×
		MTIOC6D (input/output)	P74	×	×	×	×	○	○
			P92	○	○	○	○	×	×
	MTU7	MTIOC7A (input/output)	P72	×	×	×	×	○	○
			P94	○	○	○	○	×	×
		MTIOC7B (input/output)	P73	×	×	×	×	○	○
			P93	○	○	○	○	×	×
		MTIOC7C (input/output)	P75	×	×	×	×	○	○
			P91	○	○	○	○	×	×
		MTIOC7D (input/output)	P76	×	×	×	×	○	○
			P90	○	○	○	○	×	×
	MTU	MTCLKA (input)	P21	○	○	○	○	×	×
			P22	×	×	×	×	○	○
			P33	○	○	○	○	×	×
			PB3	×	×	×	×	○	○
		MTCLKB (input)	P20	○	○	○	○	×	×
			P23	×	×	×	×	○	○
			P32	○	○	○	○	×	×
			PB2	×	×	×	×	○	○
		MTCLKC (input)	P11	○	○	○	○	○	×
			P24	×	×	×	×	○	○
			P31	○	○	○	○	×	×
			PE4	○	○	○	○	×	×
		MTCLKD (input)	P10	○	○	○	○	○	×
			P30	○	○	○	○	○	○
			PE3	○	○	○	○	×	×

Table 21.1 Functions Assigned to Each Multiplexed Pin (3/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package					
				144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
Port output enable 3	POE0	POE0# (input)	P70	○	○	○	○	○	○
	POE4	POE4# (input)	P96	○	○	○	○	×	×
	POE8	POE8# (input)	PB4	○	○	○	○	○	○
	POE10	POE10# (input)	PE4	○	○	○	○	×	×
			PE2	○	○	○	○	○	○
	POE11	POE11# (input)	PE3	○	○	○	○	×	×
			PB5	×	×	×	×	○	○
	POE12	POE12# (input)	PG5	○	○	○	×	×	×
General PWM timer	GPT0	GTIOC0A (input/output)	P71	○	○	○	○	○	○
			PD7	○	○	○	○	○	○
		GTIOC0B (input/output)	P74	○	○	○	○	○	○
			PD6	○	○	○	○	○	○
	GPT1	GTIOC1A (input/output)	P72	○	○	○	○	○	○
			PD5	○	○	○	○	○	○
		GTIOC1B (input/output)	P75	○	○	○	○	○	○
			PD4	○	○	○	○	○	○
	GPT2	GTIOC2A (input/output)	P73	○	○	○	○	○	○
			PD3	○	○	○	○	○	○
		GTIOC2B (input/output)	P76	○	○	○	○	○	○
			PB6	×	×	×	×	○	○
			PB7	×	×	×	×	○	×
			PD2	○	○	○	○	×	×
	GPT3	GTIOC3A (input/output)	P00	×	×	×	×	○	×
			PD1	○	○	○	○	×	×
		GTIOC3B (input/output)	P01	×	×	×	×	○	×
			PD0	○	○	○	○	×	×
	GPT4	GTIOC4A (input/output)	P95	○	○	○	○	×	×
		GTIOC4B (input/output)	P92	○	○	○	○	×	×
General PWM timer	GPT5	GTIOC5A (input/output)	P94	○	○	○	○	×	×
		GTIOC5B (input/output)	P91	○	○	○	○	×	×
	GPT6	GTIOC6A (input/output)	P93	○	○	○	○	×	×
			PG3	○	○	○	×	×	×
		GTIOC6B (input/output)	P90	○	○	○	○	×	○
			PG4	○	○	○	×	×	×
	GPT7	GTIOC7A (input/output)	PG0	○	○	○	×	×	×
		GTIOC7B (input/output)	PG1	○	○	○	×	×	×
	GPT	GTETRG0	PB4	○	○	○	○	○	○
		GTETRG1	P34	○	×	×	×	×	×

Table 21.1 Functions Assigned to Each Multiplexed Pin (4/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package					
				144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
Serial communications interface	SCI0	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P22	○	○	○	○	×	×
			P24	×	×	×	×	○	○
			PA5	○	○	○	○	×	×
			PB1	○	○	○	○	○	○
		TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P23	○	○	○	○	×	×
			P30	×	×	×	×	○	○
			PA4	○	○	○	○	×	×
			PB2	○	○	○	○	○	○
		SCK0 (input/output)	P23	×	×	×	×	○	○
			P30	○	○	○	○	×	×
			PA3	○	○	○	○	×	×
			PB3	○	○	○	○	○	○
		CTS0# (input)/ RTS0# (output)/ SS0# (input)	P00	×	×	×	×	○	×
			P01	○	○	○	○	×	×
			P22	×	×	×	×	○	○
			P24	○	○	○	○	×	×
			PD7	○	○	○	○	○	○
	SCI1	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P93	×	×	×	×	○	×
			P96	○	○	○	○	×	×
			PD5	○	○	○	○	○	○
			PF2	○	○	○	×	×	×
		TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P26	○	○	×	×	×	×
			P94	×	×	×	×	○	×
			P95	○	○	○	○	×	×
			PD3	○	○	○	○	○	○
			PF3	○	○	○	×	×	×
		SCK1 (input/output)	P25	○	○	×	×	×	×
			P92	×	×	×	×	○	×
			PD4	○	○	○	○	○	○
			PG6	○	○	×	×	×	×
		CTS1# (input)/ RTS1# (output)/ SS1# (input)	P70	○	○	○	○	○	○
			P91	×	×	×	×	○	×
			P94	○	○	○	○	×	×

Table 21.1 Functions Assigned to Each Multiplexed Pin (5/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package 144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
Serial communications interface	SCI2	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P03	○	×	×	×	×	×
			PA2	○	○	○	○	×	×
			PG1	○	○	○	×	×	×
		TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P02	○	×	×	×	×	×
			PA1	○	○	○	○	×	×
			PG0	○	○	○	×	×	×
		SCK2 (input/output)	P14	○	×	×	×	×	×
			PA0	○	○	○	○	×	×
			PG2	○	○	○	×	×	×
		CTS2# (input)/ RTS2# (output)/ SS2# (input)	P13	○	○	×	×	×	×
			P93	○	○	○	○	×	×
	SCI3	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P34	○	×	×	×	×	×
			PG4	○	○	○	×	×	×
		TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P35	○	×	×	×	×	×
			PG3	○	○	○	×	×	×
		SCK3 (input/output)	PG5	○	○	○	×	×	×
		CTS3# (input)/ RTS3# (output)/ SS3# (input)	PA6	○	×	×	×	×	×
	SCI12	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P80	○	○	○	○	×	×
			PB6	○	○	○	○	○	○
		TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P81	○	○	○	○	×	×
			PB5	○	○	○	○	○	○
		SCK12 (input/output)	P82	○	○	○	○	×	×
			PB7	○	○	○	○	○	×
		CTS12# (input)/ RTS12# (output)/ SS12# (input)	PB4	×	×	×	×	○	○
			PE1	○	○	○	○	×	×
I²C bus interface	RIIC0	SCL0 (input/output)	PB1	○	○	○	○	○	○
		SDA0 (input/output)	PB2	○	○	○	○	○	○
	RIIC1	SCL1 (input/output)	P25	○	○	×	×	×	×
		SDA1 (input/output)	P26	○	○	×	×	×	×
USB 2.0 host/function module		USB0_DPUPE	–	○	○	×	×	×	×
		USB0_VBUSEN (output)	P13	○	○	×	×	×	×
		USB0_OVRCURA (input)	PE1	○	○	×	×	×	×
		USB0_VBUS (input)	PE5	○	○	×	×	×	×
		USB0_EXICEN (output)	PD1	○	○	×	×	×	×
		USB0_OVRCURB (input)	PE0	○	○	×	×	×	×
		USB0_ID (input)	PD2	○	○	×	×	×	×
		USB0_DRPD (output)	P01	○	○	×	×	×	×
		USB0_DPRPD (output)	P12	○	○	×	×	×	×

Table 21.1 Functions Assigned to Each Multiplexed Pin (6/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package					
				144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
CAN module		CRX1 (input)	PE0	○	○	○	○	×	×
		CRX1 (input)	P22	○	○	○	○	×	×
			PB6	○	○	○	○	×	×
		CTX1 (output)	P23	○	○	○	○	×	×
			PB5	○	○	○	○	×	×
			PD7	○	○	○	○	×	×
Serial peripheral interface	RSPI0	RSPCKA (input/output)	P24	○	○	○	○	○	○
			PA4	○	○	○	○	○	×
			PD0	○	○	○	○	×	×
		MOSIA (input/output)	P23	○	○	○	○	○	○
			PB0	○	○	○	○	○	○
			PD2	○	○	○	○	×	×
		MISOA (input/output)	P22	○	○	○	○	○	○
			PA5	○	○	○	○	○	×
			PD1	○	○	○	○	×	×
		SSLA0 (input/output)	P30	○	○	○	○	○	○
			PA3	○	○	○	○	○	○
			PD6	○	○	○	○	×	×
		SSLA1 (output)	P31	○	○	○	○	○	×
			PA2	○	○	○	○	○	○
			PD7	○	○	○	○	×	×
		SSLA2 (output)	P32	○	○	○	○	○	×
			PA1	○	○	○	○	×	×
			PE0	○	○	○	○	×	×
		SSLA3 (output)	P33	○	○	○	○	○	×
			PA0	○	○	○	○	×	×
			PE1	○	○	○	○	×	×

Table 21.1 Functions Assigned to Each Multiplexed Pin (7/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package					
				144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
Serial peripheral interface	RSPI1	RSPCKB (input/output)	P24	○	○	○	○	×	×
			PA4	○	○	○	○	×	×
			PD0	○	○	○	○	×	×
		MOSIB (input/output)	P23	○	○	○	○	×	×
			PB0	○	○	○	○	×	×
			PD2	○	○	○	○	×	×
		MISOB (input/output)	P22	○	○	○	○	×	×
			PA5	○	○	○	○	×	×
			PD1	○	○	○	○	×	×
		SSLB0 (input/output)	P30	○	○	○	○	×	×
			PA3	○	○	○	○	×	×
			PD6	○	○	○	○	×	×
		SSLB1 (output)	P31	○	○	○	○	×	×
			PA2	○	○	○	○	×	×
			PD7	○	○	○	○	×	×
		SSLB2 (output)	P32	○	○	○	○	×	×
			PA1	○	○	○	○	×	×
			PE0	○	○	○	○	×	×
		SSLB3 (output)	P33	○	○	○	○	×	×
			PA0	○	○	○	○	×	×
			PE1	○	○	○	○	×	×
12-bit A/D converter		AN000 (input)	P40	○	○	○	○	○	○
		AN001 (input)	P41	○	○	○	○	○	○
		AN002 (input)	P42	○	○	○	○	○	○
		AN003 (input)	P43	○	○	○	○	○	○
		AN004 (input)	P44	×	×	×	×	○	○
		AN005 (input)	P45	×	×	×	×	○	×
		AN006 (input)	P46	×	×	×	×	○	×
		AN007 (input)	P47	×	×	×	×	○	○
		AN100 (input)	P44	○	○	○	○	×	×
		AN101 (input)	P45	○	○	○	○	×	×
		AN102 (input)	P46	○	○	○	○	×	×
		AN103 (input)	P47	○	○	○	○	×	×
		ADTRG0# (input)	P20	○	○	○	○	×	×
			PA4	○	○	○	○	○	×
		ADTRG1# (input)	P21	○	○	○	○	×	×
			PA5	○	○	○	○	×	×

Table 21.1 Functions Assigned to Each Multiplexed Pin (8/8)

Module/Function	Channel	Pin Functions	Allocation Port	Package					
				144-pin	120-pin	112-pin	100-pin	64-pin	48-pin
10-bit A/D converter		AN0 (input)	P60	○	○	○	○	×	×
		AN1 (input)	P61	○	○	○	○	×	×
		AN2 (input)	P62	○	○	○	○	×	×
		AN3 (input)	P63	○	○	○	○	×	×
		AN4 (input)	P64	○	○	○	○	×	×
		AN5 (input)	P65	○	○	○	○	×	×
		AN6 (input)	P50	○	○	○	○	×	×
		AN7 (input)	P51	○	○	○	○	×	×
		AN8 (input)	P52	○	○	○	○	×	×
		AN9 (input)	P53	○	○	○	○	×	×
		AN10 (input)	P54	○	○	○	○	×	×
		AN11 (input)	P55	○	○	○	○	×	×
		AN12 (input)	P56	○	×	×	×	×	×
		AN13 (input)	P57	○	×	×	×	×	×
		AN14 (input)	PC0	○	×	×	×	×	×
		AN15 (input)	PC1	○	×	×	×	×	×
		AN16 (input)	PC2	○	×	×	×	×	×
		AN17 (input)	PC3	○	×	×	×	×	×
		AN18 (input)	PC4	○	×	×	×	×	×
		AN19 (input)	PC5	○	×	×	×	×	×
		ADTRG# (input)	P22	○	○	○	○	×	×
			PG5	○	○	○	×	×	×
D/A converter		DA0 (output)	P54	○	○	○	○	×	×
		DA1 (output)	P55	○	○	○	○	×	×
Clock Frequency Accuracy Measurement Circuit		CACREF (input)	P00	○	○	○	○	×	×
			P01	×	×	×	×	○	×
			P23	○	○	○	○	○	○
			PB3	○	○	○	○	○	○

21.2 Register Descriptions

The registers and bits of unsupported pins, depending on the package, are reserved. The write value to the reserved bits is the value after a reset.

21.2.1 Write-Protect Register (PWPR)

Address(es): 0008 C11Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PFS Register Write Enable	0: Writing to the PFS register is disabled 1: Writing to the PFS register is enabled	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled	R/W

PFSWE (PFS Register Write Enable)

Only when 1 is written to the PFSWE bit, writing to the PmnPFS and UDPUEPFS registers is allowed.

To set the PFSWE bit to 1, write 0 to the B0WI bit before setting the PFSWE bit to 1.

B0WI Bit (PFSWE Bit Write Disable)

Only when 0 is written to the B0WI bit, writing to the PFSWE bit is allowed.

21.2.2 P0n Pin Function Control Register (P0nPFS) (n = 0 to 3)

Address(es): P00PFS 0008 C140h, P01PFS 0008 C141h, P02PFS 0008 C142h, P03PFS 0008 C143h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.2.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The port mn pin function select register (PmnPFS) selects the pin function. Bits PSEL[4:0] select the peripheral function which is assigned to bits.
The ISEL bit is set when a pin is used as an IRQ input pin. This setting can be used with the combination of the peripheral function, though IRQn (external pin interrupt) of the same number should not be enabled by two or more pins.
The ASEL bit is set when a pin is used as an analog pin. The pin state cannot be read at this point, since the PmnPFS register is protected by the write-protect register (PWPR). Modify the register after releasing the protection.
The ISEL bit to which IRQn is not specified is reserved. The ASEL bit to which analog input/output is not specified is reserved.

Table 21.2 Register Settings for Input/Output Pin Function in 144-Pin LQFP

	Pin			
PSEL[4:0] Settings	**P00**	**P01**	**P02**	**P03**
00000b (initial value)	Hi-Z			
00101b	CACREF	—	—	—
01010b	—	CTS0# RTS0# SS0#	TXD2 SMOSI2 SSDA2	RXD2 SMISO2 SSCL2
10001b	—	USB0_DRPD	—	—

—: Do not specify this value.

Table 21.3 Register Settings for Input/Output Pin Function in 120-Pin LQFP

	Pin	
PSEL[4:0] Settings	**P00**	**P01**
00000b (initial value)	Hi-Z	
00101b	CACREF	—
01010b	—	CTS0# RTS0# SS0#
10001b	—	USB0_DRPD

—: Do not specify this value.

Table 21.4 Register Settings for Input/Output Pin Function in 112-Pin LQFP, 100-Pin LQFP

	Pin	
PSEL[4:0] Settings	**P00**	**P01**
00000b (initial value)	Hi-Z	
00101b	CACREF	—
01010b	—	CTS0# RTS0# SS0#

—: Do not specify this value.

Table 21.5 Register Settings for Input/Output Pin Function in 64-Pin LQFP

	Pin	
PSEL[3:0] Settings	**P00**	**P01**
0000b (initial value)	Hi-Z	
0101b	—	CACREF
0110b	GTIOC3A	GTIOC3B
1010b	CTS0# RTS0# SS0#	—

—: Do not specify this value.

21.2.3 P1n Pin Function Control Registers (P1nPFS) (n = 0 to 4)

Address(es): P10PFS 0008 C148h, P11PFS 0008 C149h, P12PFS 0008 C14Ah, P13PFS 0008 C14Bh, P14PFS 0008 C14Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.6.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.6 Register Settings for Input/Output Pin Function in 144-Pin LQFP

	Pin				
PSEL[4:0]Settings	**P10**	**P11**	**P12**	**P13**	**P14**
00000b (initial value)	Hi-Z				
00010b	MTCLKD	MTCLKC	—	—	—
01010b	—	—	—	CTS2# RTS2# SS2#	SCK2
10001b	—	—	USB0_DPRPD	USB0_VBUSEN	—

—: Do not specify this value.

Table 21.7 Register Settings for Input/Output Pin Function in 120-Pin LQFP

	Pin			
PSEL[4:0]Settings	**P10**	**P11**	**P12**	**P13**
00000b (initial value)	Hi-Z			
00010b	MTCLKD	MTCLKC	—	—
01010b	—	—	—	CTS2# RTS2# SS2#
10001b	—	—	USB0_DPRPD	USB0_VBUSEN

—: Do not specify this value.

Table 21.8 Register Settings for Input/Output Pin Function in 112-Pin LQFP, 100-Pin LQFP

	Pin	
PSEL[4:0]Settings	**P10**	**P11**
00000b (initial value)	Hi-Z	
00010b	MTCLKD	MTCLKC

—: Do not specify this value.

Table 21.9 Register Settings for Input/Output Pin Function in 64-Pin LQFP

	Pin	
PSEL[3:0] Settings	**P10**	**P11**
0000b (initial value)	Hi-Z	
0010b	MTCLKD	MTCLKC

21.2.4 P2n Pin Function Control Registers (P2nPFS) (n = 0 to 6)

Address(es): P20PFS 0008 C150h, P21PFS 0008 C151h, P22PFS 0008 C152h, P23PFS 0008 C153h, P24PFS 0008 C154h, P25PFS 0008 C155h, P26PFS 0008 C156h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.10.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.10 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP

	Pin						
PSEL[4:0] Settings	**P20**	**P21**	**P22**	**P23**	**P24**	**P25**	**P26**
00000b (initial value)	Hi-Z						
00010b	MTCLKB	MTCLKA	—	—	—	—	—
00101b	—	—	—	CACREF	—	—	—
01001b	ADTRG0#	ADTRG1#	ADTRG#	—	—	—	—
01010b	—	—	RXD0 SMISO0 SSCL0	TXD0 SMOSI0 SSDA0	CTS0# RTS0# SS0#	SCK1	TXD1 SMOSI1 SSDA1
01101b	—	—	MISOA	MOSIA	RSPCKA	—	—
01110b	—	—	MISOB	MOSIB	RSPCKB	—	—
01111b	—	—	—	—	—	SCL1	SDA1
10000b	—	—	CRX1	CTX1	—	—	—

—: Do not specify this value.

Table 21.11 Register Settings for Input/Output Pin Function in 112-Pin LQFP, 100-Pin LQFP

	Pin				
PSEL[4:0] Settings	**P20**	**P21**	**P22**	**P23**	**P24**
00000b (initial value)	Hi-Z				
00010b	MTCLKB	MTCLKA	—	—	—
00101b	—	—	—	CACREF	—
01001b	ADTRG0#	ADTRG1#	ADTRG#	—	—
01010b	—	—	RXD0 SMISO0 SSCL0	TXD0 SMOSI0 SSDA0	CTS0# RTS0# SS0#
01101b	—	—	MISOA	MOSIA	RSPCKA
01110b	—	—	MISOB	MOSIB	RSPCKB
10000b	—	—	CRX1	CTX1	—

—: Do not specify this value.

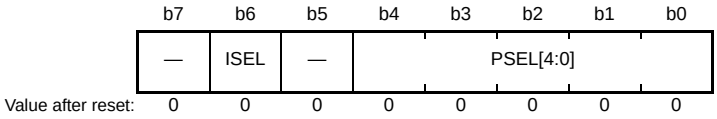
Table 21.12 Register Settings for Input/Output Pin Function in 64 and 48-Pin LQFPs

	Pin		
PSEL[3:0] Settings	**P22**	**P23**	**P24**
0000b (initial value)	Hi-Z		
0001b	MTIC5W	MTIC5V	MTIC5U
0010b	MTCLKA	MTCLKB	MTCLKC
0101b	—	CACREF	—
1010b	CTS0# RTS0# SS0#	SCK0	RXD0 SMISO SSCL0
1101b	MISOA	MOSIA	RSPCKA

—: Do not specify this value.

21.2.5 P3n Pin Function Control Registers (P3nPFS) (n = 0 to 5)

Address(es): P30PFS 0008 C158h, P31PFS 0008 C159h, P32PFS 0008 C15Ah, P33PFS 0008 C15Bh
P34PFS 0008 C15Ch, P35PFS 0008 C15Dh



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.13.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.13 Register Settings for Input/Output Pin Function in 144-Pin LQFP

	Pin					
PSEL[4:0] Settings	**P30**	**P31**	**P32**	**P33**	**P34**	**P35**
00000b (initial value)	Hi-Z					
00001b	MTIOC0B	MTIOC0A	MTIOC3C	MTIOC3A	—	—
00010b	MTCLKD	MTCLKC	MTCLKB	MTCLKA	—	—
00110b	—	—	—	—	GTETRG1	—
01010b	SCK0	—	—	—	RXD3 SMISO3 SSCL3	TXD3 SMOSI3 SSDA3
01101b	SSLA0	SSLA1	SSLA2	SSLA3		
01110b	SSLB0	SSLB1	SSLB2	SSLB3	—	—

—: Do not specify this value.

Table 21.14 Register Settings for Input/Output Pin Function in 120-Pin LQFP, 112-Pin LQFP, 100-Pin LQFP

	Pin			
PSEL[4:0] Settings	**P30**	**P31**	**P32**	**P33**
00000b (initial value)	Hi-Z			
00001b	MTIOC0B	MTIOC0A	MTIOC3C	MTIOC3A
00010b	MTCLKD	MTCLKC	MTCLKB	MTCLKA
01010b	SCK0	—	—	—
01101b	SSLA0	SSLA1	SSLA2	SSLA3
01110b	SSLB0	SSLB1	SSLB2	SSLB3

—: Do not specify this value.

Table 21.15 Register Settings for Input/Output Pin Function in 64-Pin LQFP

PSEL[3:0] Settings	Pin			
	P30	P31	P32	P33
0000b (initial value)	Hi-Z			
0001b	MTIOC0B	MTIOC0A	MTIOC3C	MTIOC3A
0010b	MTCLKD	—	MTIOC6C	MTIOC6A
1010b	TXD0 SMOSI0 SSDA0	—	—	—
1101b	SSLA0	SSLA1	SSLA2	SSLA3

—: Do not specify this value.

Table 21.16 Register Settings for Input/Output Pin Function in 48-Pin LQFP

PSEL[3:0] Settings	Pin
	P30
0000b (initial value)	Hi-Z
0001b	MTIOC0B
0010b	MTCLKD
1010b	TXD0 SMOSI0 SSDA0
1101b	SSLA0

—: Do not specify this value.

21.2.6 P4n Pin Function Control Registers (P4nPFS) (n = 0 to 7)

Address(es): P40PFS 0008 C160h, P41PFS 0008 C161h, P42PFS 0008 C162h, P43PFS 0008 C163h
P44PFS 0008 C164h, P45PFS 0008 C165h, P46PFS 0008 C166h, P47PFS 0008 C167h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ASEL	Analog Function Select	0: Used other than as analog pin. 1: Used as analog pin.	R/W

21.2.7 P5n Pin Function Control Registers (P5nPFS) (n = 0 to 7)

Address(es): P50PFS 0008 C168h, P51PFS 0008 C169h, P52PFS 0008 C16Ah, P54PFS 0008 C16Bh, P54PFS 0008 C16Ch,
P55PFS 0008 C16Dh, P56PFS 0008 C16Eh, P57PFS 0008 C16Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ASEL	Analog Function Select	0: Used other than as analog pin. 1: Used as analog pin. P54: DA0 [144-, 120-, 112- and 100-pin versions] P55: DA1 [144-, 120-, 112- and 100-pin versions]	R/W

21.2.8 P6n Pin Function Control Registers (P6nPFS) (n = 0 or 5)

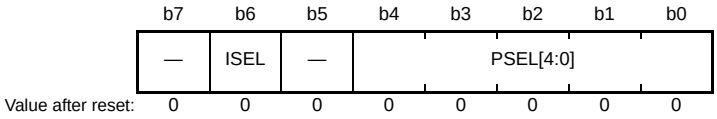
Address(es): P60PFS 0008 C170h, P61PFS 0008 C171h, P62PFS 0008 C172h, P63PFS 0008 C173h,
P64PFS 0008 C174h, P65PFS 0008 C175h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ASEL	Analog Function Select	0: Used other than as analog pin. 1: Used as analog pin.	R/W

21.2.9 P7n Pin Function Control Registers (P7nPFS) (n = 0 to 6)

Address(es): P70PFS 0008 C178h, P71PFS 0008 C179h, P72PFS 0008 C17Ah, P73PFS 0008 C17Bh
P74PFS 0008 C17Ch, P75PFS 0008 C17Dh, P76PFS 0008 C17Eh



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.17.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.17 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP, 112-Pin LQFP, 100-Pin LQFP

	Pin						
PSEL[4:0] Settings	**P70**	**P71**	**P72**	**P73**	**P74**	**P75**	**P76**
00000b (initial value)	Hi-Z						
00001b	—	MTIOC3B	MTIOC4A	MTIOC4B	MTIOC3D	MTIOC4C	MTIOC4D
00110b	—	GTIOC0A	GTIOC1A	GTIOC2A	GTIOC0B	GTIOC1B	GTIOC2B
00111b	POE0#	—	—	—	—	—	—
01010b	CTS1# RTS1# SS1#	—	—	—	—	—	—

—: Do not specify this value.

Table 21.18 Register Settings for Input/Output Pin Function in 64 and 48-Pin LQFPs

	Pin						
PSEL[3:0] Settings	**P70**	**P71**	**P72**	**P73**	**P74**	**P75**	**P76**
0000b (initial value)	Hi-Z						
0001b	—	MTIOC3B	MTIOC4A	MTIOC4B	MTIOC3D	MTIOC4C	MTIOC4D
0010b	—	MTIOC6B	MTIOC7A	MTIOC7B	MTIOC6D	MTIOC7C	MTIOC7D
0110b	—	GTIOC0A	GTIOC1A	GTIOC2A	GTIOC0B	GTIOC1B	GTIOC2B
0111b	POE0#	—	—	—	—	—	—
1010b	CTS1# RTS1# SS1#	—	—	—	—	—	—

—: Do not specify this value.

21.2.10 P8n Pin Function Control Registers (P8nPFS) (n = 0 to 2)

Address(es): P80PFS 0008 C180h, P81PFS 0008 C181h, P82PFS 0008 C182h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

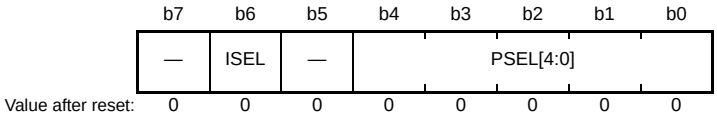
Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.19.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.19 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP, 112-Pin LQFP, 100-Pin LQFP

	Pin		
PSEL[4:0] Settings	**P80**	**P81**	**P82**
00000b (initial value)	Hi-Z		
00001b	MTIC5W	MTIC5V	MTIC5U
01100b	RXD12 SMISO12 SSCL12 RXDX12	TXD12 SMOSI12 SSDA12 TXDX12 SIOX12	SCK12

21.2.11 P9n Pin Function Control Registers (P9nPFS) (n = 0 to 6)

Address(es): P90PFS 0008 C188h, P91PFS 0008 C189h, P92PFS 0008 C18Ah, P93PFS 0008 C18Bh, P94PFS 0008 C18Ch, P95PFS 0008 C18Dh, P96PFS 0008 C18Eh



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.20.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.20 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP, 112-Pin LQFP, 100-Pin LQFP

	Pin						
PSEL[4:0] Settings	**P90**	**P91**	**P92**	**P93**	**P94**	**P95**	**P96**
00000b (initial value)	Hi-Z						
00001b	MTIOC7D	MTIOC7C	MTIOC6D	MTIOC7B	MTIOC7A	MTIOC6B	—
00110b	GTIOC6B	GTIOC5B	GTIOC4B	GTIOC6A	GTIOC5A	GTIOC4A	—
00111b	—	—	—	—	—	—	POE4#
01010b	—	—	—	CTS2# RTS2# SS2#	CTS1# RTS1# SS1#	TXD1 SMOSI1 SSDA1	RXD1 SMISO1 SSCL1

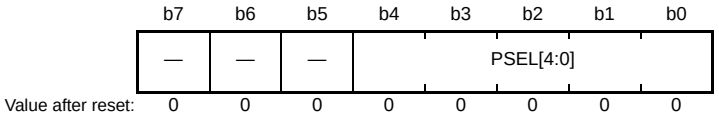
—: Do not specify this value.

Table 21.21 Register Settings for Input/Output Pin Function in 64-Pin LQFP

	Pin			
PSEL[3:0] Settings	**P91**	**P92**	**P93**	**P94**
0000b (initial value)	Hi-Z			
1010b	CTS1# RTS1# SS1#	SCK1	RXD1 SMISO1 SSCL1	TXD1 SMOSI1 SSDA1

21.2.12 PAn Pin Function Select Registers (PAnPFS) (n = 0 to 6)

Address(es): PA0PFS 0008 C190h, PA1PFS 0008 C191h, PA2PFS 0008 C192h, PA3PFS 0008 C193h
PA4PFS 0008 C194h, PA5PFS 0008 C195h, PA6PFS 0008 C196h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.22.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 21.22 Register Settings for Input/Output Pin Function in 144-Pin LQFP

	Pin						
PSEL[4:0] Settings	**PA0**	**PA1**	**PA2**	**PA3**	**PA4**	**PA5**	**PA6**
00000b (initial value)	Hi-Z						
00001b	MTIOC6C	MTIOC6A	MTIOC2B	MTIOC2A	MTIOC1B	MTIOC1A	—
01010b	SCK2	TXD2 SMOSI2 SSDA2	RXD2 MISO2 SSCL2	SCK0	TXD0 SMOSI0 SSDA0	RXD0 SMISO0 SSCL0	CTS3# RTS3# SS3#
01101b	SSLA3	SSLA2	SSLA1	SSLA0	RSPCKA	MISOA	—
01110b	SSLB3	SSLB2	SSLB1	SSLB0	RSPCKB	MISOB	—
01001b	—	—	—	—	ADTRG0#	ADTRG1#	—

—: Do not specify this value.

Table 21.23 Register Settings for Input/Output Pin Function in 120-Pin LQFP, 112-Pin LQFP, 100-Pin LQFP

	Pin					
PSEL[4:0] Settings	**PA0**	**PA1**	**PA2**	**PA3**	**PA4**	**PA5**
00000b (initial value)	Hi-Z					
00001b	MTIOC6C	MTIOC6A	MTIOC2B	MTIOC2A	MTIOC1B	MTIOC1A
01010b	SCK2	TXD2 SMOSI2 SSDA2	RXD2 MISO2 SSCL2	SCK0	TXD0 SMOSI0 SSDA0	RXD0 SMISO0 SSCL0
01101b	SSLA3	SSLA2	SSLA1	SSLA0	RSPCKA	MISOA
01110b	SSLB3	SSLB2	SSLB1	SSLB0	RSPCKB	MISOB
01001b	—	—	—	—	ADTRG0#	ADTRG1#

Table 21.24 Register Settings for Input/Output Pin Function in 64-Pin LQFP

	Pin			
PSEL[3:0] Settings	**PA2**	**PA3**	**PA4**	**PA5**
0000b (initial value)	Hi-Z			
0001b	MTIOC2B	MTIOC2A	MTIOC1B	MTIOC1A
1001b	—	—	ADTRG0#	—
1101b	SSLA1	SSLA0	RSPCKA	MISOA

—: Do not specify this value.

Table 21.25 Register Settings for Input/Output Pin Function in 48-Pin LQFP

	Pin	
PSEL[3:0] Settings	**PA2**	**PA3**
0000b (initial value)	Hi-Z	
0001b	MTIOC2B	MTIOC2A
1101b	SSLA1	SSLA0

21.2.13 PBn Pin Function Control Registers (PBnPFS) (n = 0 to 7)

Address(es): PB0PFS 0008 C198h, PB1PFS 0008 C199h, PB2PFS 0008 C19Ah, PB3PFS 0008 C19Bh
PB4PFS 0008 C19Ch, PB5PFS 0008 C19Dh, PB6PFS 0008 C19Eh, PB7PFS 0008 C19Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.26.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.26 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP, 112-Pin LQFP, 100-Pin LQFP

	Pin							
PSEL[4:0] Settings	**PB0**	**PB1**	**PB2**	**PB3**	**PB4**	**PB5**	**PB6**	**PB7**
00000b (initial value)	Hi-Z							
00001b	MTIOC0D	MTIOC0C	MTIOC0B	MTIOC0A	—	—	—	—
00101b	—	—	—	CACREF	—	—	—	—
00110b	—	—	—	—	GTETRG0	—	—	—
00111b	—	—	—	—	POE8#	—	—	—
01010b	—	RXD0 SMISO0 SSCL0	TXD0 SMOSI0 SSDA0	SCK0	—	—	—	—
01100b	—	—	—	—	—	TXD12 SMOSI12 SSDA12 TXDX12 SIOX12	RXD12 SMISO12 SSCL12 RXDX12	SCK12
01101b	MOSIA	—	—	—	—	—	—	—
01110b	MOSIB	—	—	—	—	—	—	—
10000b	—	—	—	—	—	CTX1	CRX1	—
01111b	—	SCL0	SDA0	—	—	—	—	—

—: Do not specify this value.

Table 21.27 Register Settings for Input/Output Pin Function in 64-Pin LQFP

	Pin							
PSEL[3:0] Settings	**PB0**	**PB1**	**PB2**	**PB3**	**PB4**	**PB5**	**PB6**	**PB7**
0000b (initial value)	Hi-Z							
0001b	MTIOC0D	MTIOC0C	MTIOC0B	MTIOC0A	—	—	—	—
0010b	—	—	MTCLKB	MTCLKA	—	—	—	—
0101b	—	—	—	CACREF	—	—	—	—
0110b	—	—	—	—	GTETRG	—	GTIOC2B	GTIOC2B
0111b	—	—	—	—	POE8#	POE11#	—	—
1010b	—	RXD0 SMISO0 SSCL0	TXD0 SMOSI0 SSDA0	SCK0	—	TXD12 SMOSI12 SSDA12 TXDX12 SIOX12	RXD12 SMISO12 SSCL12 RXDX12	SCK12
1100b	—	—	—	—	CTS12# RTS12# SS12#	—	—	—
1101b	MOSIA	—	—	—	—	—	—	—
1111b	—	SCL	SDA	—	—	—	—	—

—: Do not specify this value.

Table 21.28 Register Settings for Input/Output Pin Function in 48-Pin LQFP

	Pin						
PSEL[3:0] Settings	**PB0**	**PB1**	**PB2**	**PB3**	**PB4**	**PB5**	**PB6**
0000b (initial value)	Hi-Z						
0001b	MTIOC0D	MTIOC0C	MTIOC0B	MTIOC0A	—	—	—
0010b	—	—	MTCLKB	MTCLKA	—	—	—
0101b	—	—	—	CACREF	—	—	—
0110b	—	—	—	—	GTETRG	—	GTIOC2B
0111b	—	—	—	—	POE8#	POE11#	—
1010b	—	RXD0 SMISO0 SSCL0	TXD0 SMOSI0 SSDA0	SCK0	—	TXD12 SMOSI12 SSDA12 TXDX12 SIOX12	RXD12 SMISO12 SSCL12 RXDX12
1100b	—	—	—	—	CTS12# RTS12# SS12#	—	—
1101b	MOSIA	—	—	—	—	—	—
1111b	—	SCL	SDA	—	—	—	—

—: Do not specify this value.

21.2.14 PCn Pin Function Control Register (PCnPFSn) (n = 0 to 5)

Address(es): PC0PFS 0008 C1A0h, PC1PFS 0008 C1A1h, PC2PFS 0008 C1A2h, PC3PFS 0008 C1A3h
PC4PFS 0008 C1A4h, PC5PFS 0008 C1A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ASEL	Analog Input Function Select	0: Used other than as analog pin. 1: Used as analog pin.	R/W

21.2.15 PDn Pin Function Control Register (PDnPFS) (n = 0 to 7)

Address(es): PD0PFS 0008 C1A8h, PD1PFS 0008 C1A9h, PD2PFS 0008 C1AAh, PD3PFS 0008 C1ABh
PD4PFS 0008 C1ACh, PD5PFS 0008 C1ADh, PD6PFS 0008 C1AEh, PD7PFS 0008 C1AFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.29.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.29 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP

	Pin							
PSEL[4:0] Settings	**PD0**	**PD1**	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**
00000b (initial value)	Hi-Z							
00110b	GTIOC3B	GTIOC3A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC0B	GTIOC0A
01010b	—	—	—	TXD1 SMOSI1 SSDA1	SCK1	RXD1 SMISO1 SSCL1	—	CTS0# RTS0# SS0#
01101b	RSPCKA	MISOA	MOSIA	—	—	—	SSLA0	SSLA1
01110b	RSPCKB	MISOB	MOSIB	—	—	—	SSLB0	SSLB1
10000b	—	—	—	—	—	—	—	CTX1
10001b	—	USB0_EXICEN	USB0_ID	—	—	—	—	—

—: Do not specify this value.

Table 21.30 Register Settings for Input/Output Pin Function in 112-Pin LQFP and 100-Pin LQFP

PSEL[4:0] Settings	Pin							
	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
00000b (initial value)	Hi-Z							
00110b	GTIOC3B	GTIOC3A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC0B	GTIOC0A
01010b	—	—	—	TXD1 SMOSI1 SSDA1	SCK1	RXD1 SMISO1 SSCL1	—	CTS0# RTS0# SS0#
01101b	RSPCKA	MISOA	MOSIA	—	—	—	SSLA0	SSLA1
01110b	RSPCKB	MISOB	MOSIB	—	—	—	SSLB0	SSLB1
10000b	—	—	—	—	—	—	—	CTX1

—: Do not specify this value.

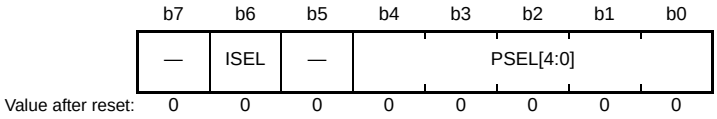
Table 21.31 Register Settings for Input/Output Pin Function in 64 and 48-Pin LQFPs

PSEL[3:0] Settings	**Pin**				
	PD3	**PD4**	**PD5**	**PD6**	**PD7**
0000b (initial value)	Hi-Z				
0110b	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC0B	GTIOC0A
1010b	TXD1 SMOSI1 SSDA1	SCK1	RXD1 SMISO1 SSCL1	—	CTS0# RTS0# SS0#

—: Do not specify this value.

21.2.16 PEn Pin Function Control Register (PEnPFS) (n = 0 to 5)

Address(es): PE0PFS 0008 C1B0h, PE1PFS 0008 C1B1h, PE2PFS 0008 C1B2h, PE3PFS 0008 C1B3h
PE4PFS 0008 C1B4h, PE5PFS 0008 C1B5h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.32.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.32 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP

	Pin					
PSEL[4:0] Settings	**PE0**	**PE1**	**PE2**	**PE3**	**PE4**	**PE5**
00000b (initial value)	Hi-Z					
00010b	—	—	—	MTICLKD	MTICLKC	—
00111b	—	—	POE10#	POE11#	POE10#	—
01100b	—	CTS12# RTS12# SS12#	—	—	—	—
01101b	SSLA2	SSLA3	—	—	—	—
01110b	SSLB2	SSLB3	—	—	—	—
10000b	CRX1	—	—	—	—	—
10001b	USB0_OVRCURB	USB0_OVRCURA	—	—	—	USB0_VBUS

—: Do not specify this value.

Table 21.33 Register Settings for Input/Output Pin Function in 112-Pin LQFP, 100-Pin LQFP

	Pin					
PSEL[4:0] Settings	**PE0**	**PE1**	**PE2**	**PE3**	**PE4**	**PE5**
00000b (initial value)	Hi-Z					
00010b	—	—	—	MTICLKD	MTICLKC	—
00111b	—	—	POE10#	POE11#	POE10#	—
01100b	—	CTS12# RTS12# SS12#	—	—	—	—
01101b	SSLA2	SSLA3	—	—	—	—
01110b	SSLB2	SSLB3	—	—	—	—
10000b	CRX1	—	—	—	—	—

—: Do not specify this value.

Table 21.34 Register Settings for Input/Output Pin Function in 64 and 48-Pin LQFPs

	Pin
PSEL[3:0] Settings	**PE2**
0000b (initial value)	Hi-Z
0111b	POE10#

21.2.17 PFn Pin Function Select Register (PFnPFS) (n = 2, 3)

Address(es): PF2PFS 0008 C1BAh, PF3PFS 0008 C1BBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

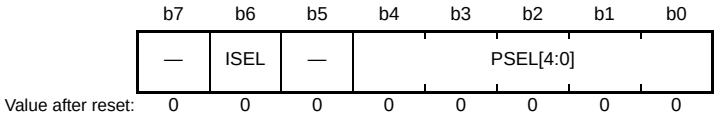
Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.35.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.35 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP, 112-Pin LQFP

PSEL[4:0] Settings	Pin	
	PF2	PF3
00000b (initial value)	Hi-Z	
01010b	RXD1 SMISO1 SSCL1	TXD1 SMOSI1 SSDA1

21.2.18 PGn Pin Function Control Register (PGnPFS) (n = 0 to 6)

Address(es): PG0PFS 0008 C1C0h, PG1PFS 0008 C1C1h, PG2PFS 0008 C1C2h, PG3PFS 0008 C1C3h, PG4PFS 0008 C1C4h, PG5PFS 0008 C1C5h, PG6PFS 0008 C1C6h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.36.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 21.36 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP

	Pin						
PSEL[4:0] Settings	**PG0**	**PG1**	**PG2**	**PG3**	**PG4**	**PG5**	**PG6**
00000b (initial value)	Hi-Z						
00110b	GTIOC7A	GTIOC7B	—	GTIOC6A	GTIOC6B	—	—
00111b	—	—	—		—	POE12#	—
01010b	TXD2 SMOSI2 SSDA2	RXD2 SMISO2 SSCL2	SCK2	TXD3 SMOSI3 SSDA3	RXD3 SMISO3 SSCL3	SCK3	SCK1
01001b	—	—	—	—	—	ADTRG#	—

—: Do not specify this value.

Table 21.37 Register Settings for Input/Output Pin Function in 112-Pin LQFP

	Pin					
PSEL[4:0] Settings	**PG0**	**PG1**	**PG2**	**PG3**	**PG4**	**PG5**
00000b (initial value)	Hi-Z					
00110b	GTIOC7A	GTIOC7B	—	GTIOC6A	GTIOC6B	—
00111b	—	—	—		—	POE12#
01010b	TXD2 SMOSI2 SSDA2	RXD2 SMISO2 SSCL2	SCK2	TXD3 SMOSI3 SSDA3	RXD3 SMISO3 SSCL3	SCK3
01001b	—	—	—	—	—	ADTRG#

—: Do not specify this value.

21.2.19 USB0_DPUPE Pin Function Control Register (UDPUPEPFS)

Address(es): UDPUEPFS 0008 C1D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 21.38.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 21.38 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP

	Pin
PSEL[4:0] Settings	**USB0_DPUPE**
00000b (initial value)	Hi-Z
10001b	USB0_DPUPE

21.2.20 CS Output Enable Register (PFCSE)

Address(es): 0008 C100h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CS3E	CS2E	CS1E	CS0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CS0E	CS0 Enable	0: CSn# output disabled 1: CSn# output enabled (n = 0 to 3)	R/W
b1	CS1E	CS1 Enable		R/W
b2	CS2E	CS2 Enable		R/W
b3	CS3E	CS3 Enable		R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CSnE Bits (CSn Enable) (n = 0 to 3)

These bits enable or disable the corresponding pins to output the CSn# signal.

To enable output of the CSn# signal, set the corresponding CSnE bit in PFCSE to 1.

21.2.21 CS Output Pin Select Register 0 (PFCSS0)

Address(es): 0008 C102h

	b7	b6	b5	b4	b3	b2	b1	b0
	CS3S[1:0]		CS2S[1:0]		CS1S[1:0]		—	CS0S
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CS0S	CS0# Output Pin Select	0: Set P26 as CS0# output pin 1: Set PD1 as CS0# output pin	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3, b2	CS1S[1:0]	CS1# Output Pin Select	b3 b2 0 0: Set P00 as CS1# output pin 0 1: Set P25 as CS1# output pin 1 x: Set PF2 as CS1# output pin	R/W
b5, b4	CS2S[1:0]	CS2# Output Pin Select	b5 b4 0 0: Set PD2 as CS2# output pin 0 1: Set PG6 as CS2# output pin 1 x: Set P05 as CS2# output pin	R/W
b7, b6	CS3S[1:0]	CS3# Output Pin Select	b7 b6 0 0: Set P12 as CS3# output pin 0 1: Set PF4 as CS3# output pin 1 x: Set PA6 as CS3# output pin	R/W

x: Don’t care

CS0S Bits (CS0# Output Pin Select)

CSnS[1:0] Bits (CSn# Output Pin Select) (n = 1 to 3)

When CSn# output is enabled (the PFCSE.CSnE bit = 1), the CSn# output pin is selected.

21.2.22 Address Output Enable Register 0 (PFAOE0)

Address(es): 0008 C104h

	b7	b6	b5	b4	b3	b2	b1	b0
	A15E	A14E	A13E	A12E	A11E	A10E	A9E	A8E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	A8E	Address A8 Output Enable	0: Disables A8 output. 1: Enables A8 output.	R/W
b1	A9E	Address A9 Output Enable	0: Disables A9 output. 1: Enables A9 output.	R/W
b2	A10E	Address A10 Output Enable	0: Disables A10 output. 1: Enables A10 output.	R/W
b3	A11E	Address A11 Output Enable	0: Disables A11 output. 1: Enables A11 output.	R/W
b4	A12E	Address A12 Output Enable	0: Disables A12 output. 1: Enables A12 output.	R/W
b5	A13E	Address A13 Output Enable	0: Disables A13 output. 1: Enables A13 output.	R/W
b6	A14E	Address A14 Output Enable	0: Disables A14 output. 1: Enables A14 output.	R/W
b7	A15E	Address A15 Output Enable	0: Disables A15 output. 1: Enables A15 output.	R/W

21.2.23 Address Output Enable Register 1 (PFAOE1)

Address(es): 0008 C105h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	A19E	A18E	A17E	A16E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	A16E	AddressA16 Output Enable	0: Disables A16 output. 1: Enables A16 output.	R/W
b1	A17E	AddressA17 Output Enable	0: Disables A17 output. 1: Enables A17 output.	R/W
b2	A18E	AddressA18 Output Enable	0: Disables A18 output. 1: Enables A18 output.	R/W
b3	A19E	AddressA19 Output Enable	0: Disables A19 output. 1: Enables A19 output.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

21.2.24 External Bus Control Register 0 (PFBCR0)

Address(es): 0008 C106h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	WR1BC1E	—	DHE	—	—	—	ADRLE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ADRLE	A0 to A7 Output Enable	0: Configures P65 to P60, P53, and P52 as the I/O port pins. 1: Configures P65 to P60, P53, and P52 as the external address bus A0 to A7.	R/W
b3 to b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DHE	D8 to D15 Output Enable	0: Configures P32 to P30 and P24 to P20 as the I/O port pins. 1: Configures P32 to P30 and P24 to P20 as the external data bus D8 to D15.	R/W
b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	WR1BC1E	WR1#/BC1# Output Enable	0: Configures PE0 as the I/O port pin. 1: Configures PE0 as the WR1# or BC1# pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

21.2.25 External Bus Control Register 1 (PFBCR1)

Address(es): 0008 C107h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ALEOE	WAITS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	WAITS[1:0]	WAIT Select	b1 b0 0 0: Configures PE0 as the WAIT# input pin. 0 1: Configures P82 as the WAIT# input pin. 1 x: Configures P05 as the WAIT# input pin.	R/W
b2	ALEOE	ALE Output Enable	0: Configures P11 as an I/O port pin. 1: Configures P11 as the ALE output pin.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

WAITS[1:0] Bits (WAIT Select Bits)

The port pin specified by the WAIT[1:0] bits becomes the WAIT# pin when the external bus is enabled. However, if the specified port pin is not to be used as the WAIT# pin, the external wait enable bit (EWENB) in the CSn mode register (CSnMOD) can be cleared (disabling external wait) to make the pin available for use as a general input port pin.
If the specified WAIT# pin is not to be used as the WAIT input or as a general input port pin, pull the level on the WAIT# pin up or down.

21.2.26 USB0 Control Register (PFUSB0)

Address(es): 0008 C114h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	PDHZS	PUPHZS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1-b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	PUPHZS	PUPHZ Select	0: USB0_DPUPE pin: high-level output or low-level output (external pull-up control signal) 1: USB0_DPUPE pin: high-level output or Hi-Z state (USB0_DP pin pull-up output)	R/W
b3	PDHZS	PDHZ Select	0: USB0_DPRPD pin: high-level output or low-level output USB0_DRPD pin: high-level output or low-level output (external pull-down control signal) 1: USB0_DPRPD pin: low-level output or Hi-Z state USB0_DRPD pin: low-level output or Hi-Z state (USB0_DP / USB0_DM pin pull-down output)	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

When the DPUPE pin function has been assigned to a pin by the setting of the USB0_DPUPE pin function control register (UDPUPEPFS), the function of the PUPHZS bit becomes effective.

PUPHZS Bit (PUPHZ Select)

This bit selects the output mode (external pull-up control/pin pull-up output) for the DPUPE pin of the USB0.
When the PUPHZS bit is set to 0, the control signal output mode for the external pull-up IC is selected and the high-active control signal is output from the DPUPE pin. When the DP pin of the USB0 is pulled up, the DPUPE pin is set to the high-level output state. When the pulled-up state of the DP pin is canceled, the DPUPE pin is set to the low-level output state.
When the PUPHZS bit is set to 1, the output mode where the DP pin is directly pulled-up is selected. When the DP pin is pulled up, the DPUPE pin is set to the high-level output state. When the pulled-up state of the DP pin is canceled, the DPUPE pin is set to the Hi-Z state.

PDHZS Bit (PDHZ Select)

This bit selects the output mode (external pull-down control or pin pull-down output) for the DPRPD and DRPD pins of the USB interface.
Setting the PDHZS bit to 0 selects a control signal output mode for use with an external pull-down IC in which the DPRPD and DRPD pins output an active-high control signal.
The DPRPD and DRPD pins output the high level when the DP and DM pins are to be pulled down and output the low level when the DP and DM pins are to be released from the pulled-down state.
Setting the PDHZS bit to 1 selects an output mode where the DP and DM pins are directly pulled down.
The DPRPD and DRPD pins output the low level when the DP and DM pins are being directly pulled down and are in the high-impedance state when the DP and DM pins are released from the pulled-down state.

21.3 How to Set the External Bus Interface

If the external bus interface is to be used, set the MPC registers according to Table 20.26 and then set the external bus enable bit (EXBE) in system control register 0 (SYSCR0) to 1.
Table 21.39 lists how to set up port pins to act as the external bus interface. For details on the relevant registers of the MPC, refer to 20.2, Register Descriptions.

Table 21.39 How to Set the External Bus Interface (1/2)

144-Pin Port	120-Pin Port	112-Pin Port	100-Pin Port	Output Signal	Settings of MPC Registers
PE1	PE1	PE1	PE1	WR0#/WR#	—
PE0	PE0	PE0	PE0	WR1#/BC1#	PFBCR0.WR1BC1E = 1
				WAIT#	PFBCR1.WAITS[1:0] = 00, PFBCR0.WR1BC1E = 0
P01	P01	P01	P01	RD#	—
PE5	PE5	PE5	PE5	BCLK	—
P11	P11	P11	P11	ALE	PFBCR1.ALEOE = 1
P82	P82	P82	P82	WAIT#	PFBCR1.WAITS[1:0] = 01
PD2	PD2	PD2	PD2	CS2#	PFCSE.CS2E = 1, PFCSS0.CS2S[1:0] = 00
PG6	PG6	—	—	CS2#	PFCSE.CS2E = 1, PFCSS0.CS2S[1:0] = 01
P05	—	P05	—	CS2#	PFCSE.CS2E = 1, PFCSS0.CS2S[1:0] = 10/11
				WAIT#	PFBCR1.WAITS[1:0] = 10/11, conditions other than the above
P12	P12	P12	—	CS3#	PFCSE.CS3E = 1, PFCSS0.CS3S[1:0] = 00
PF4	—	PF4	—	CS3#	PFCSE.CS3E = 1, PFCSS0.CS3S[1:0] = 01
PA6	—	—	—	CS3#	PFCSE.CS3E = 1, PFCSS0.CS3S[1:0] = 10/11
P00	P00	P00	P00	CS1#	PFCSE.CS1E = 1, PFCSS0.CS1S[1:0] = 00
P25	P25	—	—	CS1#	PFCSE.CS1E = 1, PFCSS0.CS1S[1:0] = 01
PF2	PF2	PF2	—	CS1#	PFCSE.CS1E = 1, PFCSS0.CS1S[1:0] = 10/11
P26	P26	—	—	CS0#	PFCSE.CS0E = 1, PFCSS0.CS0S = 0
PD1	PD1	PD1	PD1	CS0#	PFCSE.CS0E = 1, PFCSS0.CS0S = 1
P65	P65	P65	P65	A0/BC0#	PFBCR0.ADRLE = 1
P64	P64	P64	P64	A1	PFBCR0.ADRLE = 1
P63	P63	P63	P63	A2	PFBCR0.ADRLE = 1
P62	P62	P62	P62	A3	PFBCR0.ADRLE = 1
P61	P61	P61	P61	A4	PFBCR0.ADRLE = 1
P60	P60	P60	P60	A5	PFBCR0.ADRLE = 1
P53	P53	P53	P53	A6	PFBCR0.ADRLE = 1
P52	P52	P52	P52	A7	PFBCR0.ADRLE = 1
P81	P81	P81	P81	A8	PFAOE0.A8E = 1
P80	P80	P80	P80	A9	PFAOE0.A9E = 1
PE4	PE4	PE4	PE4	A10	PFAOE0.A10E = 1
PE3	PE3	PE3	PE3	A11	PFAOE0.A11E = 1
PD0	PD0	PD0	PD0	A12	PFAOE0.A12E = 1
P96	P96	P96	P96	A13	PFAOE0.A13E = 1
PB0	PB0	PB0	PB0	A14	PFAOE0.A14E = 1
PB3	PB3	PB3	PB3	A15	PFAOE0.A15E = 1
PB4	PB4	PB4	PB4	A16	PFAOE1.A16E = 1
PB5	PB5	PB5	PB5	A17	PFAOE1.A17E = 1
PB6	PB6	PB6	PB6	A18	PFAOE1.A18E = 1
PB7	PB7	PB7	PB7	A19	PFAOE1.A19E = 1

Table 21.39 How to Set the External Bus Interface (2/2)

144-Pin Port	120-Pin Port	112-Pin Port	100-Pin Port	Output Signal	Settings of MPC Registers
P76	P76	P76	P76	D0[A0/D0]	—
P75	P75	P75	P75	D1[A1/D1]	—
P74	P74	P74	P74	D2[A2/D2]	—
P73	P73	P73	P73	D3[A3/D3]	—
P72	P72	P72	P72	D4[A4/D4]	—
P71	P71	P71	P71	D5[A5/D5]	—
P70	P70	P70	P70	D6[A6/D6]	—
P33	P33	P33	P33	D7[A7/D7]	—
P32	P32	P32	P32	D8[A8/D8]	PFBCR0.DHE = 1
P31	P31	P31	P31	D9[A9/D9]	PFBCR0.DHE = 1
P30	P30	P30	P30	D10[A10/D10]	PFBCR0.DHE = 1
P24	P24	P24	P24	D11[A11/D11]	PFBCR0.DHE = 1
P23	P23	P23	P23	D12[A12/D12]	PFBCR0.DHE = 1
P22	P22	P22	P22	D13[A13/D13]	PFBCR0.DHE = 1
P21	P21	P21	P21	D14[A14/D14]	PFBCR0.DHE = 1
P20	P20	P20	P20	D15[A15/D15]	PFBCR0.DHE = 1

21.4 Usage Notes

21.4.1 Procedure for Specifying Input/Output Pin Function

Use the following procedure to specify the input/output pin functions.

(1) Clear the port mode register (PMR) to 0 to select the general input function.
(2) Specify the assignments of input/output signals for peripheral functions to the desired pins.
(3) Enable writing to the Pmn pin function control register (PmnPFS) through the write-protect register (PWPR) setting. (m = 0 to 9, A to G, n = 0 to 7)
(4) Specify the input/output function for the pin through the PSEL[4:0] bit settings in the PFS register.
(5) Clear the PFSWE bit in the PWPR register to 0 to disable writing to the PmnPFS register.
(6) Set the PMR to 1 as necessary to switch to the selected input/output function for the pin.
(7) One of the pins is always selected as the WAIT pin. For pins that are not in use as the input for the WAIT signal, disable WAIT input by setting CSnMOD.EWENB to 0.
(8) Of the pins on which the WAIT pin function is multiplexed, for that which is set as the WAIT input pin by the PFBCR1.WAITS[1:0] bits, the WAIT input is enabled even if it is set as a general port or peripheral function pin.

21.4.2 Notes on MPC Register Setting

(1) Settings of the Pmn pin function control register (PmnPFS) should be made only while the PMR register for the target pin is cleared to 0. If a port mn pin function select register is set while the PMR register is 1, unexpected edges may be input through the input pin or unexpected pulses are output through the output pin.
(2) Only the allowed values (functions) should be specified in the port mn pin function select registers. If a value that is not allowed for the register is specified, correct operation is not guaranteed.
(3) Do not assign a single function to multiple pins through the MPC settings.
(4) Points to note regarding the port mode register (PMR), port direction register (PDR), and Pmn pin function control register (PmnPFS) settings for pins that have multiplexed pin functions are listed in Table 21.40. The pin states are only readable when the ASEL bit is 0. If the value of the PSEL[4:0] bits is to be changed, do so while the corresponding PMR.Bj bit is 0.

Table 21.40 Register Settings

Item	PMR.Bn	PDR.Bn	PmnPFS			Point to Note
			ASEL	ISEL	PSEL[4:0]	
After a reset	0	0	0	0	00000b	Pins function as general input port pins after release from the reset state.
General input ports	0	0	0	0/1	x	Set the PmnPFS.ISEL bit to 1 if these are multiplexed with interrupt inputs.
General output ports	0	1	0	0	x	
Peripheral functions	1	x	0	0/1	Peripheral functions (see Table 21.2 to Table 21.38)	Set the PmnPFS.ISEL bit to 1 if these are multiplexed with interrupt inputs.
Interrupt inputs	0	0	0	1	x	
NMI	x	x	x	x*1	x	Register settings are not required.
Analog inputs	0	0	1	x	x	
External bus	0	x	0	0	x	Set the PMR.Bn bit to 0 and do not select the peripheral function.
JTAG interface	0	x	x	0	x	Set the PMR.Bn bit and the PmnPFS.ISEL bit to 0 and switch the input buffers off.
FINE interface	0	x	x	0	x	Set the PMR.Bn bit and the PmnPFS.ISEL bit to 0 and switch the input buffers off.

x: Setting not required.

0/1: Setting the PmnPFS.ISEL bit to 0 makes the pin incapable of functioning as an IRQ pin.
Setting the PmnPFS.ISEL bit to 1 makes the pin capable of functioning as an IRQ pin (if the IRQ is selected from the multiplexed functions).

Note 1. Even if the PmnPFS.ISEL bit is set to 1, the pin will not function as an IRQn input pin.

Note>• The pin state is readable when the PmnPFS.ASEL bit is 0.
• If the value of the PmnPFS.PSEL[4:0] bits is to be changed, do so while the PMR.Bn bit is 0.

21.4.3 Notes on the Use of Analog Functions

To use an analog function, set the pin function select bit (PmnPFS.ASEL) in the Pmn pin function control register to 1.

22. Multi-Function Timer Pulse Unit 3 (MTU3)

22.1 Overview

This MCU has on-chip multi-function timer pulse unit 3 (MTU3), which comprises eight 16-bit timer channels. Table 22.1 shows the specifications of the MTU and Table 22.2 shows the function list of the MTU. Figure 22.1 and Figure 22.2 show block diagrams of the MTU.

Table 22.1 Specifications of MTU

Item	Description
Pulse input/output	[144-, 120-, 112-, and 100-pin versions] 24 lines max. [64- and 48-pin versions] 24 lines max. (up to 16 lines can be simultaneously used) *1
Pulse input	3 lines
Count clock	Six to eight clocks for each channel (four clocks for channel 5)
Operating frequency	8 to 100 MHz
Available operations	[MTU0 to MTU4, MTU6, and MTU7] • Waveform output on compare match • Input capture function • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations [144-, 120-, 112-, and 100-pin versions] Up to 12-phase PWM output in combination with synchronous operation [64- and 48-pin versions] Up to 8-phase PWM output in combination with synchronous operation*1
	[MTU0 to MTU4, MTU6, and MTU7] • Buffer operation specifiable
	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3/MTU4 and MTU6/MTU7, output of positive and negative signals in three phases (for a total of six phases) in complementary-PWM and reset-PWM operation • In complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks and troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode
	[MTU3 and MTU4] • Through interlocking with channel 0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)
	[MTU1 and MTU2] • Independently specifiable phase-counting mode • Capable of cascade-connected operation
	[MTU5] • Capable of operation as a dead-time compensation counter
Interrupt-skipping function in complementary PWM mode	• In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped
Interrupt sources	38 sources
Buffer operation	Automatic transfer of register data (transfer from the buffer register to the timer register)
Trigger generation	A/D converter start triggers can be generated
	A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output
Power reduction	Module stop mode can be set

Note 1. In the 64- and 48-pin products, each pair of MTIOC3A and MTIOC6A, MTIOC3B and MTIOC6B, MTIOC3C and MTIOC6C, and MTIOC3D and MTIOC6D shares the same pin; one of each pair can be selected and used by the MPC. Similarly, each pair of MTIOC4A and MTIOC7A, MTIOC4B and MTIOC7B, MTIOC4C and MTIOC7C, and MTIOC4D and MTIOC7D shares the same pin; one of each pair can be selected and used by the MPC.

Table 22.2 MTU Functions (1/3)

Item		MTU0	MTU1	MTU2	MTU3	MTU4	MTU5	MTU6	MTU7
Count clock		PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64 MTCLKA MTCLKB MTCLKC MTCLKD	PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64 PCLKA/ 256 MTCLKA MTCLKB	PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64 PCLKA/ 1024 MTCLKA MTCLKB MTCLKC	PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64 PCLKA/ 256 PCLKA/ 1024 MTCLKA MTCLKB	PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64 PCLKA/ 256 PCLKA/ 1024 MTCLKA MTCLKB	PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64	PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64 PCLKA/ 256 PCLKA/ 1024	PCLKA/1 PCLKA/4 PCLKA/16 PCLKA/64 PCLKA/ 256 PCLKA/ 1024
External clock for phase counting mode		—	MTCLKA MTCLKB	MTCLKC MTCLKD	—	—	—	—	—
General registers (TGR)		TGRA TGRB TGRE	TGRA TGRB	TGRA TGRB	TGRA TGRB	TGRA TGRB	TGRU TGRV TGRW	TGRA TGRB	TGRA TGRB
General registers/ buffer registers		TGRC TGRD TGRF	—	—	TGRC TGRD TGRE	TGRC TGRD TGRE TGRF	—	TGRC TGRD TGRE	TGRC TGRD TGRE TGRF
I/O pins		MTIOC0A MTIOC0B MTIOC0C MTIOC0D	MTIOC1A MTIOC1B	MTIOC2A MTIOC2B	MTIOC3A MTIOC3B MTIOC3C MTIOC3D	MTIOC4A MTIOC4B MTIOC4C MTIOC4D	Input pins MTIC5U MTIC5V MTIC5W	MTIOC6A MTIOC6B MTIOC6C MTIOC6D	MTIOC7A MTIOC7B MTIOC7C MTIOC7D
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	Low output	√	√	√	√	√	—	√	√
	High output	√	√	√	√	√	—	√	√
	Toggle output	√	√	√	√	√	—	√	√
Input capture function		√	√	√	√	√	√	√	√
Synchronous operation		√	√	√	√	√	—	√	√
PWM mode 1		√	√	√	√	√	—	√	√
PWM mode 2		√	√	√	—	—	—	—	—
Complementary PWM mode		—	—	—	√	√	—	√	√
Reset-synchronized PWM mode		—	—	—	√	√	—	√	√
AC synchronous motor drive mode		√	—	—	√	√	—	—	—
Phase counting mode		—	√	√	—	—	—	—	—
Buffer operation		√	—	—	√	√	—	√	√
Dead time compensation counter function		—	—	—	—	—	√	—	—

Table 22.2 MTU Functions (2/3)

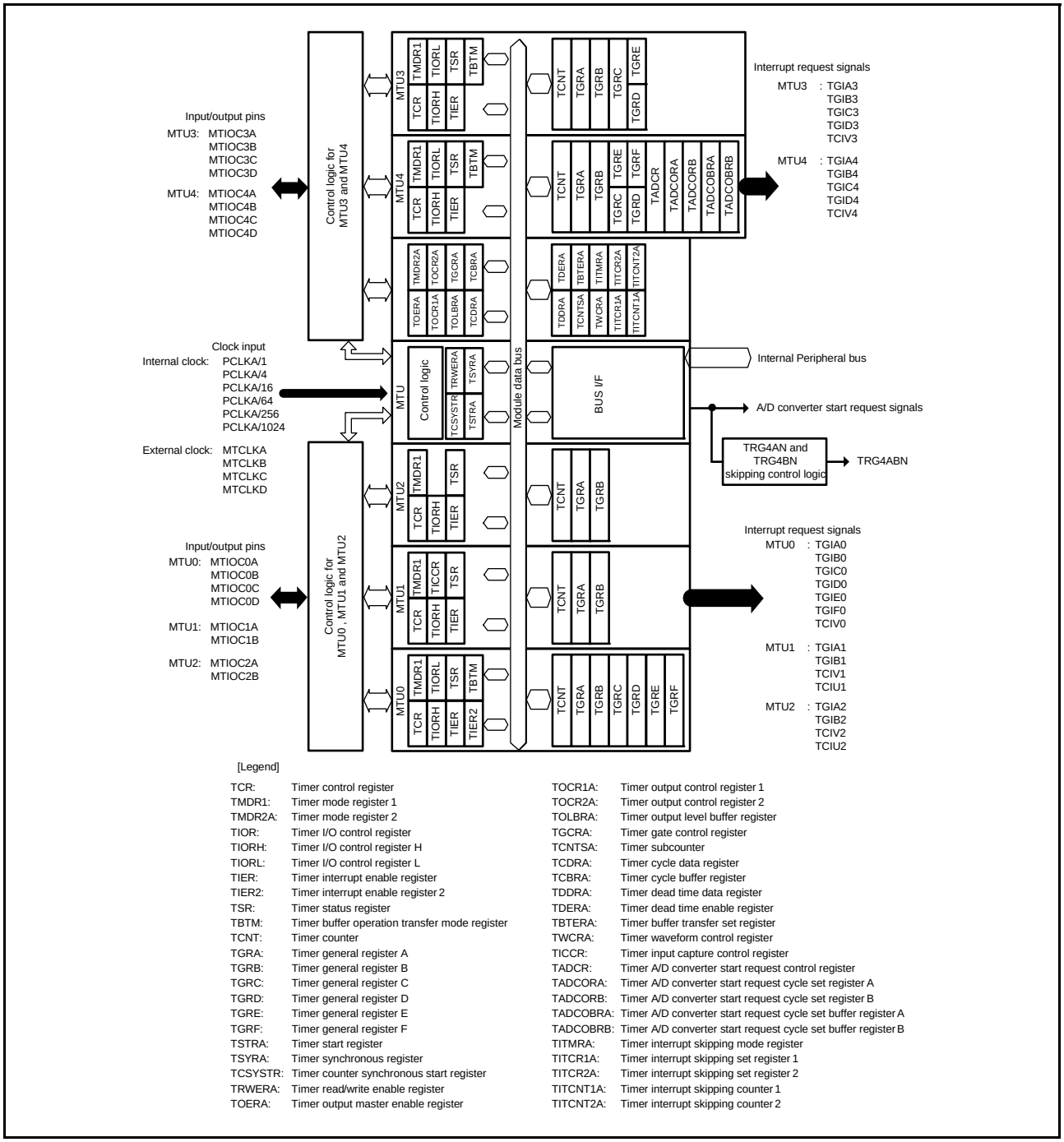
Item	MTU0	MTU1	MTU2	MTU3	MTU4	MTU5	MTU6	MTU7
Interrupt sources	7 sources • Compare match or input capture A • Compare match or input capture B • Compare match or input capture C • Compare match or input capture D • Compare match 0E • Compare match F • Overflow	4 sources • Compare match or input capture A • Compare match or input capture B • Overflow • Underflow	4 sources • Compare match or input capture A • Compare match or input capture B • Overflow • Underflow	5 sources • Compare match or input capture A • Compare match or input capture B • Compare match or input capture C • Compare match or input capture D • Overflow	5 sources • Compare match or input capture A • Compare match or input capture B • Compare match or input capture C • Compare match or input capture D • Overflow or underflow (only in comple-mentary PWM mode)	3 sources • Compare match or input capture U • Compare match or input capture V • Compare match or input capture W	5 sources • Compare match or input capture A • Compare match or input capture B • Compare match or input capture C • Compare match or input capture D • Overflow	5 sources • Compare match or input capture A • Compare match or input capture B • Compare match or input capture C • Compare match or input capture D • Overflow or underflow (only in comple-mentary PWM mode)
DTC activation	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture • Overflow or underflow (only in comple-mentary PWM mode)	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture • Overflow or underflow (only in comple-mentary PWM mode)
A/D converter start trigger	TGRA compare match or input capture TGRE compare match	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture TCNT underflow (trough) in compleme ntary PWM mode	—	TGRA compare match or input capture	TGRA compare match or input capture TCNT underflow (trough) in compleme ntary PWM mode

Table 22.2 MTU Functions (3/3)

Item	MTU0	MTU1	MTU2	MTU3	MTU4	MTU5	MTU6	MTU7
A/D converter start request delaying function	—	—	—	—	• A/D converter start request at a match between TADCORA and TCNT • A/D converter start request at a match between TADCORB and TCNT	—	—	• A/D converter start request at a match between TADCORA and TCNT • A/D converter start request at a match between TADCORB and TCNT
Interrupt skipping function 1	—	—	—	• Skips TGRA compare match interrupts	• Skips TCIV interrupts	—	• Skips TGRA compare match interrupts	• Skips TCIV interrupts
Interrupt skipping function 2	—	—	—	—	• Skips interrupts according to the count of compare matches between TADCORA and TCNT and TADCORB and TCNT	—	—	• Skips interrupts according to the count of compare matches between TADCORA and TCNT and TADCORB and TCNT
Module stop function	MSTPCRA.MSTPA9*1							

√: Possible —: Not possible

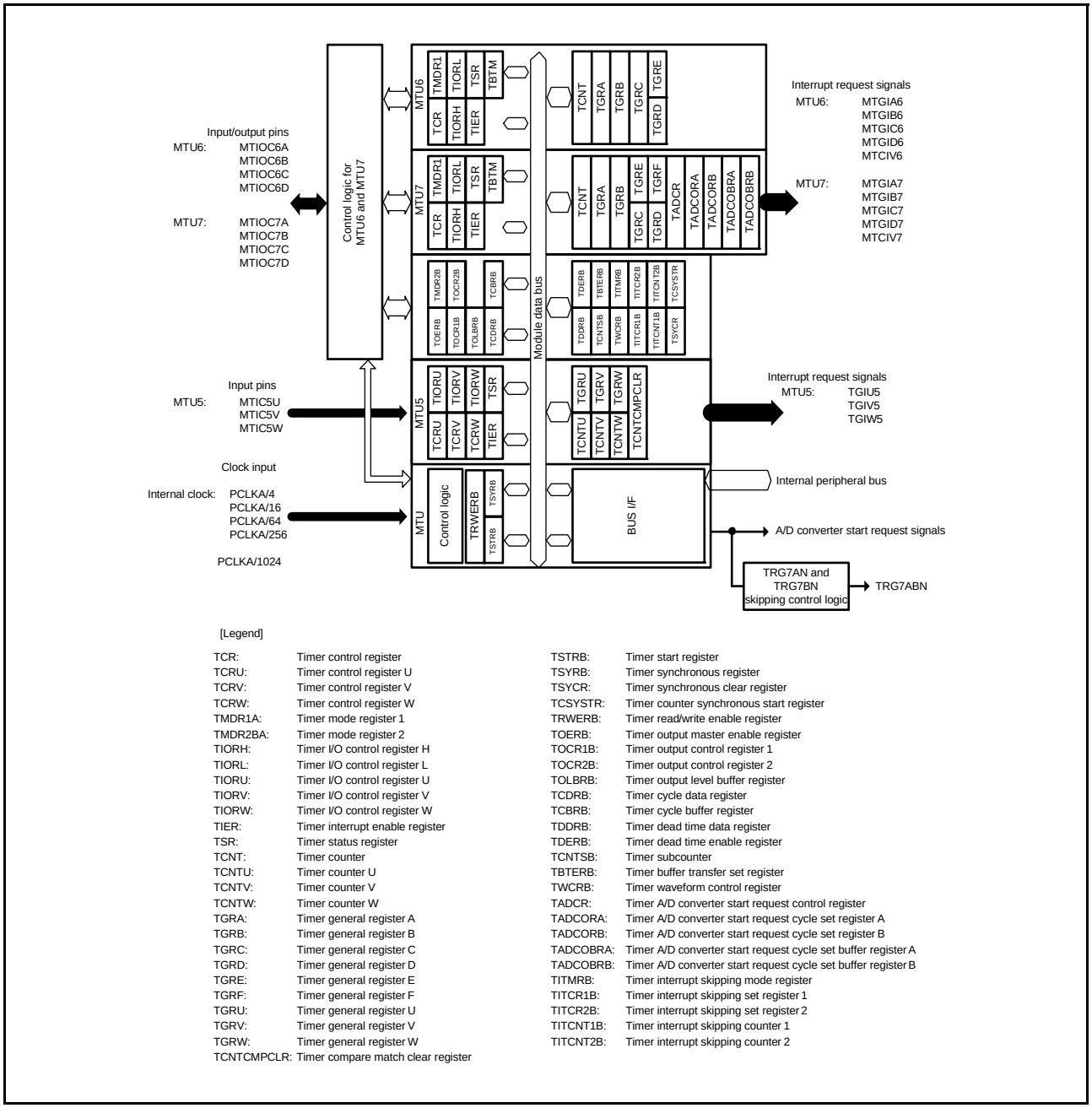
Note 1. For details on the module stop function, see section 12, Low Power Consumption.



[Legend]

TCR:	Timer control register	TOCR1A:	Timer output control register 1
TMDR1:	Timer mode register 1	TOCR2A:	Timer output control register 2
TMDR2A:	Timer mode register 2	TOLBRA:	Timer output level buffer register
TIOR:	Timer I/O control register	TGCRA:	Timer gate control register
TIORH:	Timer I/O control register H	TCNTSA:	Timer subcounter
TIORL:	Timer I/O control register L	TCDRA:	Timer cycle data register
TIER:	Timer interrupt enable register	TCBRA:	Timer cycle buffer register
TIER2:	Timer interrupt enable register 2	TDDRA:	Timer dead time data register
TSR:	Timer status register	TDERA:	Timer dead time enable register
TBTM:	Timer buffer operation transfer mode register	TBTERA:	Timer buffer transfer set register
TCNT:	Timer counter	TWCRA:	Timer waveform control register
TGRA:	Timer general register A	TICCR:	Timer input capture control register
TGRB:	Timer general register B	TADCR:	Timer A/D converter start request control register
TGRC:	Timer general register C	TADCORA:	Timer A/D converter start request cycle set register A
TGRD:	Timer general register D	TADCORB:	Timer A/D converter start request cycle set register B
TGRE:	Timer general register E	TADCOBRA:	Timer A/D converter start request cycle set buffer register A
TGRF:	Timer general register F	TADCOBRB:	Timer A/D converter start request cycle set buffer register B
TSTRA:	Timer start register	TITMRA:	Timer interrupt skipping mode register
TSYRA:	Timer synchronous register	TITCR1A:	Timer interrupt skipping set register 1
TCSYSTR:	Timer counter synchronous start register	TITCR2A:	Timer interrupt skipping set register 2
TRWERA:	Timer read/write enable register	TITCNT1A:	Timer interrupt skipping counter 1
TOERA:	Timer output master enable register	TITCNT2A:	Timer interrupt skipping counter 2

Figure 22.1 Block Diagram of MTU (MTU0 to MTU4)



[Legend]

TCR:	Timer control register	TSTRB:	Timer start register
TCRU:	Timer control register U	TSYRB:	Timer synchronous register
TCRV:	Timer control register V	TSYCR:	Timer synchronous clear register
TCRW:	Timer control register W	TCSYSTR:	Timer counter synchronous start register
TMDR1A:	Timer mode register 1	TRWERB:	Timer read/write enable register
TMDR2BA:	Timer mode register 2	TOERB:	Timer output master enable register
TIORH:	Timer I/O control register H	TOCR1B:	Timer output control register 1
TIORL:	Timer I/O control register L	TOCR2B:	Timer output control register 2
TIORU:	Timer I/O control register U	TOLBRB:	Timer output level buffer register
TIORV:	Timer I/O control register V	TCDRB:	Timer cycle data register
TIORW:	Timer I/O control register W	TCBRB:	Timer cycle buffer register
TIER:	Timer interrupt enable register	TDDRB:	Timer dead time data register
TSR:	Timer status register	TDERB:	Timer dead time enable register
TCNT:	Timer counter	TCNTSB:	Timer subcounter
TCNTU:	Timer counter U	TBTERB:	Timer buffer transfer set register
TCNTV:	Timer counter V	TWCRB:	Timer waveform control register
TCNTW:	Timer counter W	TADCR:	Timer A/D converter start request control register
TGRA:	Timer general register A	TADCORA:	Timer A/D converter start request cycle set register A
TGRB:	Timer general register B	TADCORB:	Timer A/D converter start request cycle set register B
TGRC:	Timer general register C	TADCOBRA:	Timer A/D converter start request cycle set buffer register A
TGRD:	Timer general register D	TADCOBRB:	Timer A/D converter start request cycle set buffer register B
TGRE:	Timer general register E	TITMRB:	Timer interrupt skipping mode register
TGRF:	Timer general register F	TITCR1B:	Timer interrupt skipping set register 1
TGRU:	Timer general register U	TITCR2B:	Timer interrupt skipping set register 2
TGRV:	Timer general register V	TITCNT1B:	Timer interrupt skipping counter 1
TGRW:	Timer general register W	TITCNT2B:	Timer interrupt skipping counter 2
TCNTCMPCLR:	Timer compare match clear register		

Figure 22.2 Block Diagram of MTU (MTU5 to MTU7)

Table 22.3 shows the pin configuration of the MTU.

Table 22.3 Pin Configuration

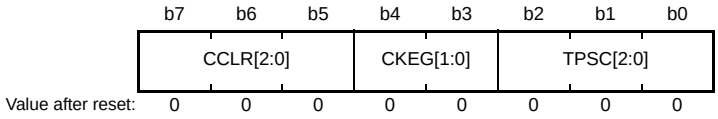
Channel	Pin Name	I/O	Function
MTU	MTCLKA	Input	External clock A input pin (MTU1 phase counting mode A phase input)
	MTCLKB	Input	External clock B input pin (MTU1 phase counting mode B phase input)
	MTCLKC	Input	External clock C input pin (MTU1 phase counting mode A phase input)
	MTCLKD	Input	External clock D input pin (MTU2 phase counting mode B phase input)
MTU0	MTIOC0A	I/O	MTU0 TGRA input capture input/output compare output/PWM output pin
	MTIOC0B	I/O	MTU0 TGRB input capture input/output compare output/PWM output pin
	MTIOC0C	I/O	MTU0 TGRC input capture input/output compare output/PWM output pin
	MTIOC0D	I/O	MTU0 TGRD input capture input/output compare output/PWM output pin
MTU1	MTIOC1A	I/O	MTU1 TGRA input capture input/output compare output/PWM output pin
	MTIOC1B	I/O	MTU1 TGRB input capture input/output compare output/PWM output pin
MTU2	MTIOC2A	I/O	MTU2 TGRA input capture input/output compare output/PWM output pin
	MTIOC2B	I/O	MTU2 TGRB input capture input/output compare output/PWM output pin
MTU3	MTIOC3A	I/O	MTU3 TGRA input capture input/output compare output/PWM output pin
	MTIOC3B	I/O	MTU3 TGRB input capture input/output compare output/PWM output pin
	MTIOC3C	I/O	MTU3 TGRC input capture input/output compare output/PWM output pin
	MTIOC3D	I/O	MTU3 TGRD input capture input/output compare output/PWM output pin
MTU4	MTIOC4A	I/O	MTU4 TGRA input capture input/output compare output/PWM output pin
	MTIOC4B	I/O	MTU4 TGRB input capture input/output compare output/PWM output pin
	MTIOC4C	I/O	MTU4 TGRC input capture input/output compare output/PWM output pin
	MTIOC4D	I/O	MTU4 TGRD input capture input/output compare output/PWM output pin
MTU5	MTIC5U	Input	MTU5 TGRU input capture input/external pulse input pin
	MTIC5V	Input	MTU5 TGRV input capture input/external pulse input pin
	MTIC5W	Input	MTU5 TGRW input capture input/external pulse input pin
MTU6	MTIOC6A	I/O	MTU6 TGRA input capture input/output compare output/PWM output pin
	MTIOC6B	I/O	MTU6 TGRB input capture input/output compare output/PWM output pin
	MTIOC6C	I/O	MTU6 TGRC input capture input/output compare output/PWM output pin
	MTIOC6D	I/O	MTU6 TGRD input capture input/output compare output/PWM output pin
MTU7	MTIOC7A	I/O	MTU7 TGRA input capture input/output compare output/PWM output pin
	MTIOC7B	I/O	MTU7 TGRB input capture input/output compare output/PWM output pin
	MTIOC7C	I/O	MTU7 TGRC input capture input/output compare output/PWM output pin
	MTIOC7D	I/O	MTU7 TGRD input capture input/output compare output/PWM output pin

22.2 Register Descriptions

22.2.1 Timer Control Register (TCR)

- MTU0, MTU1, MTU2, MTU3, MTU4, MTU6, MTU7

Address(es): MTU0.TCR 000C 1300h, MTU1.TCR 000C 1380h, MTU2.TCR 000C 1400h, MTU3.TCR 000C 1200h, MTU4.TCR 000C 1201h, MTU6.TCR 000C 1A00h, MTU7.TCR 000C 1A01h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC[2:0]	Time Prescaler Select	See Table 22.6 to Table 22.9.	R/W
b4, b3	CKEG[1:0]	Clock Edge Select	b4 b3 0 0: Count at rising edge 0 1: Count at falling edge 1 x: Count at both edges	R/W
b7 to b5	CCLR[2:0]	Counter Clear Source Select	See Table 22.4 and Table 22.5.	R/W

x: Don’t care

TCR controls the TCNT operation for each channel. The MTU has a total of ten TCR registers, one each for MTU0 to MTU4, MTU 6, and MTU7 and three (TCRU, TCRV, and TCRW) for MTU5. TCR values should be specified only while TCNT operation is stopped.

TPSC[2:0] Bits (Time Prescaler Select)

These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See Table 22.6 to Table 22.9 for details.

CKEG[1: 0] Bits (Clock Edge Select)

These bits select the input clock edge. When the input clock is counted at both edges, the input clock period is halved (e.g. PCLKA/4 at both edges = PCLKA/2 at rising edge). If phase counting mode is used on MTU1 and MTU2, the setting of these bits is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is PCLKA/4 or slower. When PCLKA/1 or the overflow/underflow in another channel is selected for the input clock, a value can be written to these bits but counter operation compiles with the initial value.

CCLR[2:0] Bits (Counter Clear Source Select)

These bits select the TCNT counter clearing source. See Table 22.4 and Table 22.5 for details.

- MTU5

Address(es): MTU5.TCRU 000C 1C84h, MTU5.TCRV 000C 1C94h, MTU5.TCRW 000C 1CA4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TPSC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TPSC[1:0]	Time Prescaler Select	See Table 22.10.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TPSC[1:0] Bits (Time Prescaler Select)

These bits select the TCNT counter clock. See Table 22.10 for details.

Table 22.4 CCLR[2:0] (MTU0, MTU3, MTU4, MTU6, and MTU7)

	Bit 7	Bit 6	Bit 5	
Channel	CCLR2	CCLR1	CCLR0	Description
MTU0 MTU3 MTU4 MTU6 MTU7	0	0	0	TCNT clearing disabled
	0	0	1	TCNT cleared by TGRA compare match/input capture
	0	1	0	TCNT cleared by TGRB compare match/input capture
	0	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation*1
	1	0	0	TCNT clearing disabled
	1	0	1	TCNT cleared by TGRC compare match/input capture*2
	1	1	0	TCNT cleared by TGRD compare match/input capture*2
	1	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation*1

Note 1. Synchronous operation is selected by setting the TSYRA.SYNC or TSYRB.SYNC bit to 1.
Note 2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority and compare match/input capture does not occur.

Table 22.5 CCLR[2:0] (MTU1 and MTU2)

	Bit 7	Bit 6		
Channel	Reserved*2	CCLR1	CCLR0	Description
MTU1 MTU2	0	0	0	TCNT clearing disabled
	0	0	1	TCNT cleared by TGRA compare match/input capture
	0	1	0	TCNT cleared by TGRB compare match/input capture
	0	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation*1

Note 1. Synchronous operation is selected by setting the TSYRA.SYNC and TSYRB.SYNC bits to 1.
Note 2. Bit 7 is reserved in MTU1 and MTU2. It is read as 0. The write value is ignored.

Table 22.6 TPSC[2:0] (MTU0)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
MTU0	0	0	0	Internal clock: counts on PCLKA/1
	0	0	1	Internal clock: counts on PCLKA/4
	0	1	0	Internal clock: counts on PCLKA/16
	0	1	1	Internal clock: counts on PCLKA/64
	1	0	0	External clock: counts on MTCLKA pin input
	1	0	1	External clock: counts on MTCLKB pin input
	1	1	0	External clock: counts on MTCLKC pin input
	1	1	1	External clock: counts on MTCLKD pin input

Table 22.7 TPSC[2:0] (MTU1)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
MTU1	0	0	0	Internal clock: counts on PCLKA/1
	0	0	1	Internal clock: counts on PCLKA/4
	0	1	0	Internal clock: counts on PCLKA/16
	0	1	1	Internal clock: counts on PCLKA/64
	1	0	0	External clock: counts on MTCLKA pin input
	1	0	1	External clock: counts on MTCLKB pin input
	1	1	0	Internal clock: counts on ICLK/256
	1	1	1	Counts on MTU2.TCNT overflow/underflow

Note: • This setting is ignored when MTU1 is in phase counting mode.

Table 22.8 TPSC[2:0] (MTU2)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
MTU2	0	0	0	Internal clock: counts on PCLKA/1
	0	0	1	Internal clock: counts on PCLKA/4
	0	1	0	Internal clock: counts on PCLKA/16
	0	1	1	Internal clock: counts on PCLKA/64
	1	0	0	External clock: counts on MTCLKA pin input
	1	0	1	External clock: counts on MTCLKB pin input
	1	1	0	External clock: counts on MTCLKC pin input
	1	1	1	Internal clock: counts on PCLKA/1024

Note: • This setting is ignored when MTU2 is in phase counting mode.

Table 22.9 TPSC[2:0] (MTU3, MTU4, MTU6, and MTU7)

	Bit 2	Bit 1	Bit 0	
Channel	**TPSC2**	**TPSC1**	**TPSC0**	**Description**
MTU3 MTU4 MTU6 MTU7	0	0	0	Internal clock: counts on PCLKA/1
	0	0	1	Internal clock: counts on PCLKA/4
	0	1	0	Internal clock: counts on PCLKA/16
	0	1	1	Internal clock: counts on PCLKA/64
	1	0	0	Internal clock: counts on PCLKA/256
	1	0	1	Internal clock: counts on PCLKA/1024
	1	1	0	External clock: counts on MTCLKA pin input*1
	1	1	1	External clock: counts on MTCLKB pin input*1

Note 1. This setting is not allowed in MTU6 and MTU7.

Table 22.10 TPSC[1:0] (MTU5)

	Bit 1	Bit 0	
Channel	**TPSC1**	**TPSC0**	**Description**
MTU5	0	0	Internal clock: counts on PCLKA/1
	0	1	Internal clock: counts on PCLKA/4
	1	0	Internal clock: counts on PCLKA/16
	1	1	Internal clock: counts on PCLKA/64

Note: • Bits 7 to 2 are reserved in MTU5. These bits are read as 0. The write value should be 0.

22.2.2 Timer Mode Register 1 (TMDR1)

- MTU0.TMDR1

Address(es): MTU0.TMDR1 000C 1301h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	BFE	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

- MTU1.TMDR1, MTU2.TMDR1

Address(es): MTU1.TMDR1 000C 1381h, MTU2.TMDR1 000C 1401h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

- MTU3.TMDR1, MTU4.TMDR1, MTU6.TMDR1, MTU7.TMDR1

Address(es): MTU3.TMDR1 000C 1202h, MTU4.TMDR1 000C 1203h,
MTU6.TMDR1 000C 1A02h, MTU7.TMDR1 000C 1A03h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	MD[3:0]	Mode Select	These bits specify the timer operating mode. See Table 22.11 for details.	R/W
b4	BFA	Buffer Operation A	0: TGRA and TGRC operate normally 1: TGRA and TGRC used together for buffer operation	R/W
b5	BFB	Buffer Operation B	0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation	R/W
b6	BFE	Buffer Operation E	0: MTU0.TGRE and MTU0.TGRF operate normally 1: MTU0.TGRE and MTU0.TGRF used together for buffer operation	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

TMDR1 specifies the operating mode of each channel. The MTU3 has a total of seven TMDR1 registers, one each for MTU0 to MTU4,MTU 6, and MTU7. TMDR1 values should be specified only while TCNT operation is stopped.

Table 22.11 Operating Mode Setting by MD[3:0] Bits

Bit 3	Bit 2	Bit 1	Bit 0	
MD3	MD2	MD1	MD0	Description
0	0	0	0	Normal mode
0	0	0	1	Setting prohibited
0	0	1	0	PWM mode 1
0	0	1	1	PWM mode 2*1
0	1	0	0	Phase counting mode 1*2
0	1	0	1	Phase counting mode 2*2
0	1	1	0	Phase counting mode 3*2
0	1	1	1	Phase counting mode 4*2
1	0	0	0	Reset-synchronized PWM mode *3
1	0	0	1	Setting prohibited
1	0	1	x	Setting prohibited
1	1	0	0	Setting prohibited
1	1	0	1	Complementary PWM mode 1 (transfer at crest) *3
1	1	1	0	Complementary PWM mode 2 (transfer at trough)*3
1	1	1	1	Complementary PWM mode 3 (transfer at crest and trough)*3

x: Don't care

Note 1. PWM mode 2 cannot be set for MTU3, MTU4, MTU6, and MTU7.

Note 2. Phase counting mode cannot be set for MTU0, MTU3, MTU4, MTU6, and MTU7.

Note 3. Reset-synchronized PWM mode and complementary PWM mode can only be set for MTU3 and MTU6.
When MTU3 or MTU6 is set to reset-synchronized PWM mode or complementary PWM mode, the MTU4 or MTU7 settings become ineffective and automatically conform to the MTU3 or MTU6 setting, respectively. MTU4 and MTU7 should be set to the initial values (normal operation).
Reset-synchronized PWM mode and complementary PWM mode cannot be set for MTU0, MTU1, and MTU2.

BFA Bit (Buffer Operation A)

This bit specifies whether to operate TGRA in the normal way or to use TGRA and TGRC together for buffer operation. When TGRC is used as a buffer register, TGRC input capture/output compare does not occur in the mode other than complementary PWM mode. In complementary PWM mode, TGRC compare match occurs. If a compare match occurs in MTU4 during Tb interval in complementary PWM mode, set the TGIEC bit in the timer interrupt enable register (MTU4.TIER) to 0.

In reset synchronized PWM mode or complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in the BFA bit of MTU3.TMDR1 (MTU6.TMDR1). The BFA bit of MTU4.TMDR1 (MTU7.TMDR1) should be set to 0.

In MTU1 and MTU2, which have no TGRC, this bit is reserved. It is read as 0. The write value should be 0.

For the Tb interval in complementary PWM mode, see Figure 22.41.

BFB Bit (Buffer Operation B)

This bit specifies whether to operate TGRB in the normal way or to use TGRB and TGRD together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare does not occur in the mode other than complementary PWM mode. In complementary PWM mode, TGRD compare match occurs.

If a compare match occurs in MTU4 during Tb interval in complementary PWM mode, set the TGIED bit in the timer interrupt enable register (MTU4.TIER) to 0.

In reset synchronized PWM mode or complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in the BFB bit of MTU3.TMDR1 (MTU6.TMDR1). The BFB bit of MTU4.TMDR1 (MTU7.TMDR1) should be set to 0.

In MTU1 and MTU2, which have no TGRD, this bit is reserved. It is read as 0. The write value should be 0.

For the Tb interval in complementary PWM mode, see Figure 22.41.

BFE Bit (Buffer Operation E)

This bit specifies whether to operate MTU0.TGRE and MTU0.TGRF in the normal way or to use them together for buffer operation. TGRF compare match occurs even when TGRF is used as a buffer register.
In MTU1 to MTU4, MTU6, and MTU7, this bit is reserved. It is read as 0. The write value should be 0.

22.2.3 Timer Mode Registers 2 (TMDR2A and TMDR2B)

Address(es): MTU.TMDR2A 000C 1270h, MTU.TMDR2B 000C 1A70h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DRS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DRS	Double Buffer Select	0: Double buffer function is disabled 1: Double buffer function is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TMDR2 specifies the double buffer function in complementary PWM mode 3 (transfer at the crest and trough of the counter value). The MTU3 has two TMDR2 registers, one each for MTU3 (TMDR2A) and MTU6 (TMDR2B). TMDR2A and TMDR2B values should be specified only while TCNT operation is stopped.

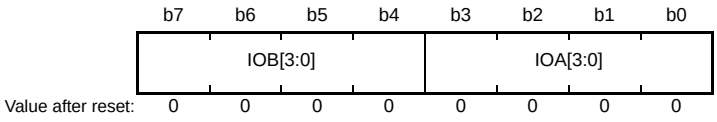
DRS Bit (Double Buffer Select)

This bit enables or disables the double buffer function in complementary PWM mode.

22.2.4 Timer I/O Control Register (TIOR)

- MTU0.TIORH, MTU1.TIOR, MTU2.TIOR, MTU3.TIORH, MTU4.TIORH, MTU6.TIORH, MTU7.TIOR

Address(es): MTU0.TIORH 000C 1302h, MTU1.TIOR 000C 1382h, MTU2.TIOR 000C 1402h, MTU3.TIORH 000C 1204h, MTU4.TIORH 000C 1206h, MTU6.TIORH 000C 1A04h, MTU7.TIORH 000C 1A06h

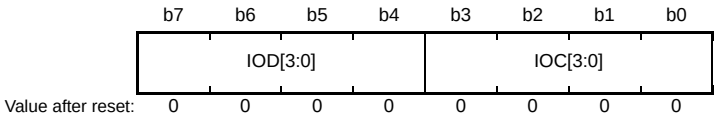


Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOA[3:0]	I/O Control A	See the following tables. *1 MTU0.TIORH: Table 22.24 MTU1.TIOR: Table 22.26 MTU2.TIOR: Table 22.27 MTU3.TIORH: Table 22.28 MTU4.TIORH: Table 22.30 MTU6.TIORH: Table 22.32 MTU7.TIORH: Table 22.34	R/W
b7 to b4	IOB[3:0]	I/O Control B	See the following tables. *1 MTU0.TIORH: Table 22.12 MTU1.TIOR: Table 22.14 MTU2.TIOR: Table 22.15 MTU3.TIORH: Table 22.16 MTU4.TIORH: Table 22.18 MTU5.TIORH: Table 22.20 MTU6.TIORH: Table 22.22	R/W

Note 1. The pin enters Hi-Z state by modification of the IOn[3:0] (n = A, B) values to 0000b or 0100b (output disabled) during low, high or toggle output at compare match.

- MTU0.TIORL, MTU3.TIORL, MTU4.TIORL, MTU6.TIORL, MTU7.TIORL

Address(es): MTU0.TIORL 000C 1303h, MTU3.TIORL 000C 1205h, MTU4.TIORL 000C 1207h, MTU6.TIORL 000C 1A05h, MTU7.TIORL 000C 1A07h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOC[3:0]	I/O Control C	See the following tables. *1 MTU0.TIORL: Table 22.25 MTU3.TIORL: Table 22.29 MTU4.TIORL: Table 22.31 MTU6.TIORL: Table 22.33 MTU7.TIORL: Table 22.35	R/W
b7 to b4	IOD[3:0]	I/O Control D	See the following tables. *1 MTU0.TIORL: Table 22.13 MTU3.TIORL: Table 22.17 MTU4.TIORL: Table 22.19 MTU6.TIORL: Table 22.21 MTU7.TIORL: Table 22.23	R/W

Note 1. The pin enters Hi-Z state by modification of the IOn[3:0] (n = C, D) values to 0000b or 0100b (output disabled) during low, high or toggle output at compare match.

- MTU5.TIORU, MTU5.TIORV, MTU5.TIORW

Address(es): MTU5.TIORU 000C 1C86h, MTU5.TIORV 000C 1C96h, MTU5.TIORW 000C 1CA6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IOC[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	IOC[4:0]	I/O Control C	See the following table. MTU5.TIORU, MTU5.TIORV, MTU5.TIORW: Table 22.36	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TIOR controls TGR. The MTU has a total of 15 TIOR registers, two each for MTU0, MTU3, MTU4, MTU6, and MTU7, one each for MTU1 and MTU2, and three (MTU5.TIORU/V/W) for MTU5. The TIOR register is set when the TMDR register is in normal mode, PWM mode, or phase counting mode.
Note that TIOR is affected by the TMDR1 setting.
The initial output specified by TIOR is valid when the counter is stopped (the CST bit in TSTRA and the CST bit in TSYRB are cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter is cleared to 0 is specified.
When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

Table 22.12 TIORH (MTU0)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOB3	**IOB2**	**IOB1**	**IOB0**	**MTU0.TGRB Function**	**MTIOC0B Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is count clock in MTU1. Input capture at MTU1.TCNT up-count/down-count.

x: Don't care

Table 22.13 TIORL (MTU0)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOD3	IOD2	IOD1	IOD0	MTU0.TGRD Function	MTIOC0D Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register *1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is count clock in MTU1. Input capture at MTU1.TCNT up-count/down-count.

x: Don't care

Note 1. When the MTU0.TMDR1.BFB is set to 1 and MTU0.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.14 TIOR (MTU1)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOB3	IOB2	IOB1	IOB0	MTU1.TGRB Function	MTIOC1B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Input capture at generation of MTU0.TGRC compare match/input capture.

x: Don't care

Table 22.15 TIOR (MTU2)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOB3	IOB2	IOB1	IOB0	MTU2.TGRB Function	MTIOC2B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.16 TIORH (MTU3)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOB3	**IOB2**	**IOB1**	**IOB0**	**MTU3.TGRB Function**	**MTIOC3B Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.17 TIORL (MTU3)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOD3	IOD2	IOD1	IOD0	MTU3.TGRD Function	MTIOC3D Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register *1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU3.TMDR1 is set to 1 and MTU3.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.18 TIORH (MTU4)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOB3	IOB2	IOB1	IOB0	MTU4.TGRB Function	MTIOC4B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.19 TIORL (MTU4)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOD3	IOD2	IOD1	IOD0	MTU4.TGRD Function	MTIOC4D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register *1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU4.TMDR1 is set to 1 and MTU4.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.20 TIORH (MTU6)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOB3	IOB2	IOB1	IOB0	MTU6.TGRB Function	MTIOC6B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.21 TIORL (MTU6)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOD3	IOD2	IOD1	IOD0	MTU6.TGRD Function	MTIOC6D Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register *1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU6.TMDR1 is set to 1 and MTU6.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.22 TIORH (MTU7)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOB3	IOB2	IOB1	IOB0	MTU7.TGRB Function	MTIOC7B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.23 TIORL (MTU7)

Bit 7	Bit 6	Bit 5	Bit 4		Description
IOD3	IOD2	IOD1	IOD0	MTU7.TGRD Function	MTIOC7D Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU7.TMDR1 is set to 1 and MTU7.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.24 TIORH (MTU0)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOA3	IOA2	IOA1	IOA0	MTU0.TGRA Function	MTIOC0A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is count clock in MTU1 Input capture at generation of MTU1.TCNT up-count/ down-count

x: Don't care

Table 22.25 TIORL (MTU0)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOC3	IOC2	IOC1	IOC0	MTU0.TGRC Function	MTIOC0C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register*1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is count clock in MTU1 Input capture at generation of MTU1.TCNT up-count/down-count

x: Don't care

Note 1. When the BFA bit in MTU0.TMDR1 is set to 1 and MTU0.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.26 TIOR (MTU1)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOA3	IOA2	IOA1	IOA0	MTU1.TGRA Function	MTIOC1A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Input capture at generation of MTU0.TGRA compare match/input capture.

x: Don't care

Table 22.27 TIOR (MTU2)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOA3	IOA2	IOA1	IOA0	MTU2.TGRA Function	MTIOC2A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.28 TIORH (MTU3)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOA3	IOA2	IOA1	IOA0	MTU3.TGRA Function	MTIOC3A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.29 TIORL (MTU3)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOC3	IOC2	IOC1	IOC0	MTU3.TGRC Function	MTIOC3C Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register *1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFA bit in MTU3.TMDR1 is set to 1 and MTU3.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.30 TIORH (MTU4)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOA3	IOA2	IOA1	IOA0	MTU4.TGRA Function	MTIOC4A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.31 TIORL (MTU4)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOC3	IOC2	IOC1	IOC0	MTU4.TGRC Function	MTIOC4C Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register *1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFA bit in MTU4.TMDR1 is set to 1 and MTU4.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.32 TIORH (MTU6)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOA3	IOA2	IOA1	IOA0	MTU6.TGRA Function	MTIOC6A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.33 TIORL (MTU6)

Bit 3	Bit 2	Bit 1	Bit 0	MTU6.TGRC Function	Description
IOC3	IOC2	IOC1	IOC0		MTIOC6C Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register *1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFA bit in MTU6.TMDR1 is set to 1 and MTU6.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.34 TIORH (MTU7)

Bit 3	Bit 2	Bit 1	Bit 0		Description
IOA3	IOA2	IOA1	IOA0	MTU7.TGRA Function	MTIOC7A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 22.35 TIORL (MTU7)

Bit 3	Bit 2	Bit 1	Bit 0	MTU7.TGRC Function	Description
IOC3	IOC2	IOC1	IOC0		MTIOC7C Pin Function
0	0	0	0	Output compare register *1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register *1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFA bit in MTU7.TMDR1 is set to 1 and MTU7.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 22.36 TIORU, TIORV, and TIORW (MTU5)

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	MTU5.TGRU, MTU5.TGRV, MTU5.TGRW Function	Description
IOC4	IOC3	IOC2	IOC1	IOC0		MTIC5U, MTIC5V, MTIC5W Pin Function
0	0	0	0	0	Compare match register	Compare match
0	0	0	0	1		Setting prohibited
0	0	0	1	x		Setting prohibited
0	0	1	x	x		Setting prohibited
0	1	x	x	x		Setting prohibited
1	0	0	0	0	Input capture register*1	Setting prohibited
1	0	0	0	1		Input capture at rising edge.
1	0	0	1	0		Input capture at falling edge.
1	0	0	1	1		Input capture at both edges.
1	0	1	x	x		Setting prohibited
1	1	0	0	0		Setting prohibited
1	1	0	0	1		Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode.
1	1	0	1	0		Measurement of low pulse width of external input signal. Capture at crest of complementary PWM mode.
1	1	0	1	1		Measurement of low pulse width of external input signal. Capture at crest and trough of complementary PWM mode.
1	1	1	0	0		Setting prohibited
1	1	1	0	1		Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode.
1	1	1	1	0		Measurement of high pulse width of external input signal. Capture at crest of complementary PWM mode.
1	1	1	1	1		Measurement of high pulse width of external input signal. Capture at crest and trough of complementary PWM mode.

x: Don't care

Note 1. Set the IOC[4:0] bits to 19h, 1Ah, 1Bh, 1Dh, 1Eh, or 1Fh only when using external pulse width measurement or only when using dead time compensation linked with MTU6 and MTU7. For details, refer to section 22.3.11, External Pulse Width Measurement and section 22.3.12, Dead Time Compensation.

22.2.5 Timer Compare Match Clear Register (TCNTCMPCLR)

Address(es): MTU5.TCNTCMPCLR 000C 1CB6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPCLR5U	CMPCLR5V	CMPCLR5W
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMPCLR5W	TCNT Compare Clear 5W	0: Disables MTU5.TCNTW to be cleared to 0000h at MTU5.TCNTW and MTU5.TGRW compare match or input capture 1: Enables MTU5.TCNTW to be cleared to 0000h at MTU5.TCNTW and MTU5.TGRW compare match or input capture	R/W
b1	CMPCLR5V	TCNT Compare Clear 5V	0: Disables MTU5.TCNTV to be cleared to 0000h at MTU5.TCNTV and MTU5.TGRV compare match or input capture 1: Enables MTU5.TCNTV to be cleared to 0000h at MTU5.TCNTV and MTU5.TGRV compare match or input capture	R/W
b2	CMPCLR5U	TCNT Compare Clear 5U	0: Disables MTU5.TCNTU to be cleared to 0000h at MTU5.TCNTU and MTU5.TGRU compare match or input capture 1: Enables MTU5.TCNTU to be cleared to 0000h at MTU5.TCNTU and MTU5.TGRU compare match or input capture	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TCNTCMPCLR specifies requests to clear MTU5.TCNTU, MTU5.TCNTV, and MTU5.TCNTW. The MTU has one TCNTCMPCLR (on MTU5).

22.2.6 Timer Interrupt Enable Register (TIER)

- TIER (MTU1, MTU2)

Address(es): MTU1.TIER 000C 1384h, MTU2.TIER 000C 1404h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

- TIER (MTU0, MTU3, MTU6)

Address(es): MTU0.TIER 000C 1304h, MTU3.TIER 000C 1208h, MTU6.TIER 000C 1A08h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

- TIER (MTU4, MTU7)

Address(es): MTU4.TIER 000C 1209h, MTU7.TIER 000C 1A09h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGIEA	TGR Interrupt Enable A	0: Interrupt requests (TGIA) disabled 1: Interrupt requests (TGIA) enabled	R/W
b1	TGIEB	TGR Interrupt Enable B	0: Interrupt requests (TGIB) disabled 1: Interrupt requests (TGIB) enabled	R/W
b2	TGIEC	TGR Interrupt Enable C	0: Interrupt requests (TGIC) disabled 1: Interrupt requests (TGIC) enabled	R/W
b3	TGIED	TGR Interrupt Enable D	0: Interrupt requests (TGID) disabled 1: Interrupt requests (TGID) enabled	R/W
b4	TCIEV	Overflow Interrupt Enable	0: Interrupt requests (TCIV) disabled 1: Interrupt requests (TCIV) enabled	R/W
b5	TCIEU	Underflow Interrupt Enable	0: Interrupt requests (TCIU) disabled 1: Interrupt requests (TCIU) enabled	R/W
b6	TTGE2	A/D Converter Start Request Enable 2	0: A/D converter start request generation by MTUn.TCNT underflow (trough) disabled 1: A/D converter start request generation by MTUn.TCNT underflow (trough) enabled	R/W
b7	TTGE	A/D Converter Start Request Enable	0: A/D converter start request generation disabled 1: A/D converter start request generation enabled	R/W

n = 4 or 7

TIER enables or disables interrupt requests in each channel. The MTU has a total of nine TIER registers, two for MTU0 and one each for MTU1 to MTU7.

TGIEA and TGIEB Bits (TGR Interrupt Enable A and B)

Each bit enables or disables interrupt requests (TGIn) (n = A, B).

TGIEC and TGIED Bits (TGR Interrupt Enable C and D)

Each bit enables or disables interrupt requests (TGIn) in MTU0, MTU3, MTU4, MTU6, and MTU7 (n = C, D).
In MTU1 and MTU2, these bits are reserved. They are always read as 0. The write value should be 0.

TCIEV Bit (Overflow Interrupt Enable)

This bit enables or disables interrupt requests (TCIV).

TCIEU Bit (Underflow Interrupt Enable)

This bit enables or disables interrupt requests (TCIU) in MTU1 and MTU2.
In MTU0, MTU3, MTU4, MTU6, and MTU7, this bit is reserved. It is always read as 0. The write value should be 0.

TTGE2 Bit (A/D Converter Start Request Enable 2)

This bit enables or disables generation of A/D converter start requests by MTUn.TCNT underflow (trough) in complementary PWM mode (n = 4, 7).
In MTU0 to MTU3 and MTU6, this bit is reserved. It is always read as 0. The write value should be 0.

TTGE Bit (A/D Converter Start Request Enable)

This bit enables or disables generation of A/D converter start requests by TGRA input capture/compare match.

- TIER2 (MTU0)

Address(es): MTU0.TIER2 000C 1324h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE2	—	—	—	—	—C	TGIEF	TGIEE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGIEE	TGR Interrupt Enable E	0: Interrupt requests (TGIE) disabled 1: Interrupt requests (TGIE) enabled	R/W
b1	TGIEF	TGR Interrupt Enable F	0: Interrupt requests (TGIF) disabled 1: Interrupt requests (TGIF) enabled	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TTGE2	A/D Converter Start Request Enable 2	0: A/D converter start request generation by compare match between MTU0.TCNT and MTU0.TGRE disabled 1: A/D converter start request generation by compare match between MTU0.TCNT and MTU0.TGRE enabled	R/W

TGIEE and TGIEF Bits (TGR Interrupt Enable E and F)

Each bit enables or disables interrupt requests by compare match between MTU0.TCNT and MTU0.TGRn (n = E or F).

TTGE2 Bit (A/D Converter Start Request Enable 2)

Each bit enables or disables interrupt requests by compare match between MTU0.TCNT and MTU0.TGRE.

- TIER (MTU5)

Address(es): MTU5.TIER 000C 1CB2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	TGIE5W	TGR Interrupt Enable 5W	0: Interrupt requests TGIW5 disabled 1: Interrupt requests TGIW5 enabled	R/W
b1	TGIE5V	TGR Interrupt Enable 5V	0: Interrupt requests TGIV5 disabled 1: Interrupt requests TGIV5 enabled	R/W
b2	TGIE5U	TGR Interrupt Enable 5U	0: Interrupt requests TGIU5 disabled 1: Interrupt requests TGIU5 enabled	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TGIE5n Bits (TGR Interrupt Enable 5n)

Each bit enables or disables interrupt requests (TGIn5) (n = U, V, W).

22.2.7 Timer Status Register (TSR)

- TSR (MTU0)

Address(es): MTU0.TSR 000C 1305h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Value after reset:	1	1	0	0	0	0	0	0

TSR (MTU1, MTU2)

Address(es): MTU1.TSR 000C 1385h, MTU2.TSR 000C 1405h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Value after reset:	1	1	0	0	0	0	0	0

- TSR (MTU3, MTU4, MTU6, MTU7)

Address(es): MTU3.TSR 000C 122Ch, MTU4.TSR 000C 122Dh, MTU6.TSR 000C 1A2Ch, MTU7.TSR 000C 1A2Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGFA	Input Capture/Output Compare Flag A	0: Neither TGRA input capture nor compare match generated 1: TGRA input capture or compare match generated	R/(W)*1
b1	TGFB	Input Capture/Output Compare Flag B	0: Neither TGRB input capture nor compare match generated 1: TGRB input capture or compare match generated	R/(W)*1
b2	TGFC	Input Capture/Output Compare Flag C	0: Neither TGRC input capture nor compare match generated 1: TGRC input capture or compare match generated	R/(W)*1
b3	TGFD	Input Capture/Output Compare Flag D	0: Neither TGRD input capture nor compare match generated 1: TGRD input capture or compare match generated	R/(W)*1
b4	TCFV	Overflow Flag	0: No TCNT overflow generated 1: TCNT overflow generated	R/(W)*1
b5	TCFU	Underflow flag	0: No TCNT underflow generated when MTU1 or MTU2 is in phase counting mode 1: TCNT underflow generated when MTU1 or MTU2 is in phase counting mode	R/(W)*1
b6	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b7	TCFD	Count Direction Flag	0: TCNT counts down 1: TCNT counts up	R

Note 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

TSR indicates the status of each channel. The MTU3 has a total of nine TSR registers, two for MTU0 and one each for MTU1 to MTU7.

TGFA Flag (Input Capture/Output Compare Flag A)

Status flag that indicates the occurrence of TGRA input capture or compare match. Only 0 can be written to clear the flag.

[Setting conditions]

- When TCNT = TGRA while TGRA is functioning as output compare register
- When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

[Clearing condition]

- When 0 is written to TGFA after reading TGFA = 1

TGFB Flag (Input Capture/Output Compare Flag B)

Status flag that indicates the occurrence of TGRB input capture or compare match in MTU0, MTU3, MTU4, MTU6, and MTU7. Only 0 can be written to clear the flag.

[Setting conditions]

- When TCNT = TGRB while TGRB is functioning as output compare register
- When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

[Clearing condition]

- When 0 is written to TGFB after reading TGFB = 1

TGFC Flag (Input Capture/Output Compare Flag C)

Status flag that indicates the occurrence of TGRC input capture or compare match in MTU0, MTU3, MTU4, MTU6, and MTU7. Only 0 can be written to clear the flag.

[Setting conditions]

- When TCNT = TGRC while TGRC is functioning as output compare register
- When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

[Clearing condition]

- When 0 is written to TGFC after reading TGFC = 1

In MTU1 and MTU2, this bit is reserved. It is read as 0. The write value should be 0.

TGFD Flag (Input Capture/Output Compare Flag D)

Status flag that indicates the occurrence of TGRD input capture or compare match in MTU0, MTU3, MTU4, MTU6, and MTU7. Only 0 can be written to clear the flag.

[Setting conditions]

- When TCNT = TGRD while TGRD is functioning as output compare register
- When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

[Clearing condition]

- When 0 is written to TGFD after reading TGFD = 1

In MTU1 and MTU2, this bit is reserved. It is read as 0. The write value should be 0.

TCFV Flag (Overflow Flag)

Status flag that indicates that TCNT overflow has occurred. Only 0 can be written to clear the flag.
[Setting conditions]

- When the TCNT value overflows (changes from FFFFh to 0000h)
- In MTU4 or MTU7, when the MTU4.TCNT or MTU7.TCNT value underflows (changes from 0001h to 0000h) in complementary PWM mode, this flag is also set.

[Clearing condition]

- When 0 is written to TCFV after reading TCFV = 1

TCFU Flag (Underflow Flag)

Status flag that indicates that TCNT underflow has occurred when MTU1 or MTU2 is set to phase counting mode. Only 0 can be written to clear the flag.
[Setting conditions]

- When the TCNT value underflows (changes from 0000h to FFFFh)

[Clearing condition]

- When 0 is written to TCFU after reading TCFU = 1

In MTU0, MTU3, MTU4, MTU6, and MTU7, this bit is reserved. It is read as 0. The write value should be 0.

TCFD Flag (Count Direction Flag)

Status flag that shows the direction in which TCNT counts in MTU1 to MTU4, MTU6, and MTU7.
In MTU0, this bit is reserved. It is read as 1. The write value should be 1.

- TSR2 (MTU0)

Address(es): MTU0.TSR2 000C 1325h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TGFF	TGFE
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGFE	Compare Match Flag E	0: No compare match between the MTU0.TCNT and MTU0.TGRE generated 1: Compare match between the MTU0.TCNT and MTU0.TGRE generated	R/(W)*1
b1	TGFF	Compare Match Flag F	0: No compare match between the MTU0.TCNT and MTU0.TGRF generated 1: Compare match between the MTU0.TCNT and MTU0.TGRF generated	R/(W)*1
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

TGFE Flag (Compare Match Flag E)

Status flag that indicates the occurrence of compare match between the MTU0.TCNT and MTU0.TGRE. Only 0 can be written to clear the flag.

[Setting condition]

- When MTU0.TCNT = MTU0.TGRE while TGRE is functioning as a compare register

[Clearing condition]

- When 0 is written to TGFE after reading TGFE = 1

TGFF Flag (Compare Match Flag F)

Status flag that indicates the occurrence of compare match between the MTU0.TCNT and MTU0.TGRF. Only 0 can be written to clear the flag.

[Setting condition]

- When MTU0.TCNT = MTU0.TGRF while TGRF is functioning as a compare register

[Clearing condition]

- When 0 is written to TGFF after reading TGFF = 1

- TSR (MTU5)

Address(es): MTU5.TSR 000C 1CB0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMFU5	CMFV5	CMFW5
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbo	Bit Name	Description	R/W
b0	CMFW5	Compare Match/Input Capture Flag W5	0: Neither MTU5.TGRW input capture nor compare match generated 1: MTU5.TGRW input capture or compare match generated	R/(W)*1
b1	CMFV5	Compare Match/Input Capture Flag V5	0: Neither MTU5.TGRV input capture nor compare match generated 1: MTU5.TGRV input capture or compare match generated	R/(W)*1
b2	CMFU5	Compare Match/Input Capture Flag U5	0: Neither MTU5.TGRU input capture nor compare match generated 1: MTU5.TGRU input capture or compare match generated	R/(W)*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

CMFn5 Flag (Compare Match/Input Capture Flag n5) (n = U, V, W)

Status flags that indicate the occurrence of MTU5.TGRn input capture or compare match. Only 0 can be written to clear the flag.

[Setting conditions]

- When MTU5.TCNTn = MTU5.TGRn while MTU5.TGRn is functioning as a compare match register
- When MTU5.TCNTn value is transferred to MTU5.TGRn by input capture signal while MTU5.TGRn is functioning as an input capture register
- When MTU5.TCNTn value is transferred to MTU5.TGRn while MTU5.TGRn is functioning as a register for measuring the pulse width of the external input signal.*1

[Clearing condition]

- When 0 is written to CMFn5 after reading CMFn5 = 1

Note 1. The transfer timing is specified by the IOC[4:0] bits in MTU5.TIORU, MTU5.TIORV, and MTU5.TIORW.

22.2.8 Timer Buffer Operation Transfer Mode Register (TBTM)

- MTU0.TBTM

Address(es): MTU0.TBTM 000C 1326h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TTSE	TTSB	TTSA
Value after reset:	0	0	0	0	0	0	0	0

- MTU3.TBTM, MTU4.TBTM, MTU6.TBTM, MTU7.TBTM

Address(es): MTU3.TBTM 000C 1238h, MTU4.TBTM 000C 1239h
MTU6.TBTM 000C 1A38h, MTU7.TBTM 000C 1A39h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TTSB	TTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TTSA	Timing Select A	0: When compare match A occurs in each channel, data is transferred from TGRC to TGRA 1: When TCNT is cleared in each channel, data is transferred from TGRC to TGRA	R/W
b1	TTSB	Timing Select B	0: When compare match B occurs in each channel, data is transferred from TGRD to TGRB 1: When TCNT is cleared in each channel, data is transferred from TGRD to TGRB	R/W
b2	TTSE	Timing Select E	0: When compare match E occurs in MTU0, data is transferred from MTU0.TGRF to MTU0.TGRE 1: When MTU0.TCNT is cleared in MTU0, data is transferred from MTU0.TGRF to MTU0.TGRE	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TBTM specifies the timing for transferring data from the buffer register to the timer general register in PWM mode. The MTU3 has a total of five TBTM registers, one each for MTU0, MTU3, MTU4, MTU6, and MTU7.

TTSA Bit (Timing Select A)

This bit specifies the timing for transferring data from TGRC to TGRA in each channel when they are used together for buffer operation. When a channel is not set to PWM mode, do not set the TTSA bit in the channel to 1.

TTSB Bit (Timing Select B)

This bit specifies the timing for transferring data from TGRD to TGRB in each channel when they are used together for buffer operation. When a channel is not set to PWM mode, do not set the TTSB bit in the channel to 1.

TTSE Bit (Timing Select E)

This bit specifies the timing for transferring data from MTU0.TGRF to MTU0.TGRE when they are used together for buffer operation.
In MTU3, MTU4, MTU6, and MTU7, this bit is reserved. It is read as 0 and the write value should be 0. When channel 0 is not set to PWM mode, do not set the TTSE bit in the channel to 1.

22.2.9 Timer Input Capture Control Register (TICCR)

Address(es): MTU1.TICCR 000C 1390h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	I2BE	I2AE	I1BE	I1AE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	I1AE	Input Capture Enable	0: Does not include the MTIOC1A pin in the MTU2.TGRA input capture conditions 1: Includes the MTIOC1A pin in the MTU2.TGRA input capture conditions	R/W
b1	I1BE	Input Capture Enable	0: Does not include the MTIOC1B pin in the MTU2.TGRB input capture conditions 1: Includes the MTIOC1B pin in the MTU2.TGRB input capture conditions	R/W
b2	I2AE	Input Capture Enable	0: Does not include the MTIOC2A pin in the MTU1.TGRA input capture conditions 1: Includes the MTIOC2A pin in the MTU1.TGRA input capture conditions	R/W
b3	I2BE	Input Capture Enable	0: Does not include the MTIOC2B pin in the MTU1.TGRB input capture conditions 1: Includes the MTIOC2B pin in the MTU1.TGRB input capture conditions	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TICCR specifies input capture conditions when MTU1.TCNT and MTU2.TCNT are cascaded. The MTU3 has one TICCR for MTU1.

22.2.10 Timer Synchronous Clear Register (TSYCR)

Address(es): MTU6.TSYCR 000C 1A50h

	b7	b6	b5	b4	b3	b2	b1	b0
	CE0A	CE0B	CE0C	CE0D	CE1A	CE1B	CE2A	CE2B
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CE2B	Clear Enable 2B	0: Disables counter clearing by the TGFB flag setting in MTU2.TSR 1: Enables counter clearing by the TGFB flag setting in MTU2.TSR	R/W
b1	CE2A	Clear Enable 2A	0: Disables counter clearing by the TGFA flag setting in MTU2.TSR 1: Enables counter clearing by the TGFA flag setting in MTU2.TSR	R/W
b2	CE1B	Clear Enable 1B	0: Disables counter clearing by the TGFB flag setting in MTU1.TSR 1: Enables counter clearing by the TGFB flag setting in MTU1.TSR	R/W
b3	CE1A	Clear Enable 1A	0: Disables counter clearing by the TGFA flag setting in MTU1.TSR 1: Enables counter clearing by the TGFA flag setting in MTU1.TSR	R/W
b4	CE0D	Clear Enable 0D	0: Disables counter clearing by the TGFD flag setting in MTU0.TSR 1: Enables counter clearing by the TGFD flag setting in MTU0.TSR	R/W
b5	CE0C	Clear Enable 0C	0: Disables counter clearing by the TGFC flag setting in MTU0.TSR 1: Enables counter clearing by the TGFC flag setting in MTU0.TSR	R/W
b6	CE0B	Clear Enable 0B	0: Disables counter clearing by the TGFB flag setting in MTU0.TSR 1: Enables counter clearing by the TGFB flag setting in MTU0.TSR	R/W
b7	CE0A	Clear Enable 0A	0: Disables counter clearing by the TGFA flag setting in MTU0.TSR 1: Enables counter clearing by the TGFA flag setting in MTU0.TSR	R/W

TSYCR specifies synchronous clear conditions for MTU6.TCNT and MTU7.TCNT. The MTU3 has one TSYCR for MTU1.

CEnm Bits (Clear Enable nm; n = 0, 1, 2; m = A, B, C, D)

These bits enable or disable clearing in response to setting of the TGFm flag in MTUn.TSR.

22.2.11 Timer Counter (TCNT)

Address(es): MTU0.TCNT 000C 1306h, MTU1.TCNT 000C 1386h, MTU2.TCNT 000C 1406h, MTU3.TCNT 000C 1210h, MTU4.TCNT 000C 1212h, MTU5.TCNTU 000C 1C80h, MTU5.TCNTV 000C 1C90h, MTU5.TCNTW 000C 1CA0h, MTU6.TCNT 000C 1A10h, MTU7.TCNT 000C 1A12h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note 1. TCNT must not be accessed in eight bits; it should always be accessed in 16 bits.

TCNT is a 16-bit readable/writable counter. The MTU3 has a total of ten TCNT counters, one each for MTU0 to MTU4, MTU6, and MTU7 and three (MTU5.TCNTU, TCNTUV, and TCNTUW) for MTU5.

TCNT is initialized to 0000h by a reset.

TCNT must not be accessed in eight bits; it should always be accessed in 16 bits.

22.2.12 Timer General Register (TGR)

Address(es): MTU0.TGRA 000C 1308h, MTU0.TGRB 000C 130Ah, MTU0.TGRC 000C 130Ch, MTU0.TGRD 000C 130Eh, MTU0.TGRE 000C 1320h, MTU0.TGRF 000C 1322h, MTU1.TGRA 000C 1388h, MTU1.TGRB 000C 138Ah, MTU2.TGRA 000C 1408h, MTU2.TGRB 000C 140Ah, MTU3.TGRA 000C 1218h, MTU3.TGRB 000C 121Ah, MTU3.TGRC 000C 1224h, MTU3.TGRD 000C 1226h, MTU3.TGRE 000C 1272h MTU4.TGRA 000C 121Ch, MTU4.TGRB 000C 121Eh, MTU4.TGRC 000C 1228h, MTU4.TGRD 000C 122Ah, MTU4.TGRE 000C 1274h, MTU4.TGRF 000C 1276h, MTU5.TGRU 000C 1C82h, MTU5.TGRV 000C 1C92h, MTU5.TGRW 000C 1CA2h, MTU6.TGRA 000C 1A18h, MTU6.TGRB 000C 1A1Ah, MTU6.TGRC 000C 1A24h, MTU6.TGRD 000C 1A26h, MTU6.TGRE 000C 1A72h, MTU7.TGRA 000C 1A1Ch, MTU7.TGRB 000C 1A1Eh, MTU7.TGRC 000C 1A28h, MTU7.TGRD 000C 1A2A, MTU7.TGRE 000C 1A74h, MTU7.TGRF 000C 1A76h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. TGR must not be accessed in eight bits; it should always be accessed in 16 bits. TGR is initialized to FFFFh.

TGR is a 16-bit readable/writable register. The MTU has a total of 35 TGR registers, six each for channel 0, two each for MTU1 and MTU2, five each for MTU3 and MTU6, six each for MTU4 and MTU7, and three for MTU5.

TGRA, TGRB, TGRC, and TGRD function as either output compare or input capture registers. TGRC and TGRD for MTU0, MTU3, MTU4, MTU6, and MTU7 can also be designated for operation as buffer registers. TGR buffer register combinations are TGRA and TGRC, and TGRB and TGRD.

MTU0.TGRE and MTU0.TGRF function as compare registers. When the MTU0.TCNT count matches the MTU0.TGRE value, an A/D converter start request can be issued. TGRF can also be designated for operation as a buffer register. TGR buffer register combination is TGRE and TGRF.

MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW function as compare match, input capture, or external pulse width measurement registers.

22.2.13 Timer Start Register (TSTR)

- TSTRA (MTU0 to MTU4)

Address(es): MTU.TSTRA 000C 1280h

	b7	b6	b5	b4	b3	b2	b1	b0
	CST4	CST3	—	—	—	CST2	CST1	CST0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST0	Counter Start 0	0: MTU0.TCNT count operation is stopped 1: MTU0.TCNT performs count operation	R/W
b1	CST1	Counter Start 1	0: MTU1.TCNT count operation is stopped 1: MTU1.TCNT performs count operation	R/W
b2	CST2	Counter Start 2	0: MTU2.TCNT count operation is stopped 1: MTU2.TCNT performs count operation	R/W
b5 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CST3	Counter Start 3	0: MTU3.TCNT count operation is stopped 1: MTU3.TCNT performs count operation	R/W
b7	CST4	Counter Start 4	0: MTU4.TCNT count operation is stopped 1: MTU4.TCNT performs count operation	R/W

Note 1. When 1 is written to a bit in TCSYSTR, the corresponding bit in TSTRA is also set to 1 automatically.

TSTRA starts or stops TCNT operation in MTU0 to MTU4.
TSTRB starts or stops TCNT operation in MTU6 and MTU7.
TSTR starts or stops TCNT operation in MTU5.
Before setting the operating mode in TMDR1 or setting the TCNT count clock in TCR, be sure to stop the TCNT counter.

CSTn Bits (Counter Start n; n = 0 to 4)

Each bit starts or stops TCNT in the corresponding channel.
If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops but the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

- TSTRB (MTU6, MTU7)

Address(es): MTU.TSTRB 000C 1A80h

	b7	b6	b5	b4	b3	b2	b1	b0
	CST7	CST6	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CST6	Counter Start 6	0: MTU6.TCNT count operation is stopped 1: MTU6.TCNT performs count operation	R/W
b7	CST7	Counter Start 7	0: MTU7.TCNT count operation is stopped 1: MTU7.TCNT performs count operation	R/W

Note 1. When 1 is written to a bit in TCSYSTR, the corresponding bit in TSTRB is also set to 1 automatically.

CSTn Bits (Counter Start n) (n = 6 or 7)

Each bit starts or stops TCNT in the corresponding channel.

If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops but the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

- TSTR (MTU5)

Address(es): MTU5.TSTR 000C 1CB4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CSTU5	CSTV5	CSTW5
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CSTW5	Counter Start W5	0: MTU5.TCNTW count operation is stopped 1: MTU5.TCNTW performs count operation	R/W
b1	CSTV5	Counter Start V5	0: MTU5.TCNTV count operation is stopped 1: MTU5.TCNTV performs count operation	R/W
b2	CSTU5	Counter Start U5	0: MTU5.TCNTU count operation is stopped 1: MTU5.TCNTU performs count operation	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

22.2.14 Timer Synchronous Register TSYRA (TSYRB)

- TSYRA (MTU0 to MTU4)

Address(es): MTU.TSYRA 000C 1281h

	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC4	SYNC3	—	—	—	SYNC2	SYNC1	SYNC0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SYNC0	Timer Synchronous Operation 0	0: MTU0.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU0.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b1	SYNC1	Timer Synchronous Operation 1	0: MTU1.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU1.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b2	SYNC2	Timer Synchronous Operation 2	0: MTU2.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU2.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b5 to b3	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b6	SYNC3	Timer Synchronous Operation 3	0: MTU3.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU3.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b7	SYNC4	Timer Synchronous Operation 4	0: MTU4.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU4.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W

TSYRA selects independent operation or synchronous operation of TCNT in MTU0 to MTU4.
TSYRB selects independent operation or synchronous operation of TCNT in MTU6 and MTU7.
A channel performs synchronous operation when the corresponding bit in TSYR is set to 1.

SYNCn Bits (Timer Synchronous Operation n; n = 0, 1, 2, 3, and 4)

Each bit selects whether operation is independent of or synchronized with other channels.
When synchronous operation is selected, the TCNT synchronous presetting of multiple channels and synchronous clearing by counter clearing on another channel are possible.
To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits TCR.CCLR[2:0].

- TSYRB (MTU6, MTU7)

Address(es): MTU.TSYRB 000C 1A81h

	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC7	SYNC6	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	SYNC6	Timer Synchronous Operation 6	0: MTU6.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU6.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b7	SYNC7	Timer Synchronous Operation 7	0: MTU7.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU7.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W

SYNCn Bits (Timer Synchronous Operation n; n = 6 or 7)

Each bit selects whether operation is independent of or synchronized with other channels.

When synchronous operation is selected, the TCNT synchronous presetting of multiple channels and synchronous clearing by counter clearing on another channel are possible.

To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits TCR.CCLR[2:0].

22.2.15 Timer Counter Synchronous Start Register (TCSYSTR)

Address(es): MTU.TCSYSTR 000C 1282h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCH0	SCH1	SCH2	SCH3	SCH4	—	SCH6	SCH7
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SCH7	Synchronous Start 7	0: Does not specify synchronous start for MTU7.TCNT 1: Specifies synchronous start for MTU7.TCNT	R/(W)*1
b1	SCH6	Synchronous Start 6	0: Does not specify synchronous start for MTU6.TCNT 1: Specifies synchronous start for MTU6.TCNT	R/(W)*1
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R
b3	SCH4	Synchronous Start 4	0: Does not specify synchronous start for MTU4.TCNT 1: Specifies synchronous start for MTU4.TCNT	R/(W)*1
b4	SCH3	Synchronous Start 3	0: Does not specify synchronous start for MTU3.TCNT 1: Specifies synchronous start for MTU3.TCNT	R/(W)*1
b5	SCH2	Synchronous Start 2	0: Does not specify synchronous start for MTU2.TCNT 1: Specifies synchronous start for MTU2.TCNT	R/(W)*1
b6	SCH1	Synchronous Start 1	0: Does not specify synchronous start for MTU1.TCNT 1: Specifies synchronous start for MTU1.TCNT	R/(W)*1
b7	SCH0	Synchronous Start 0	0: Does not specify synchronous start for MTU0.TCNT 1: Specifies synchronous start for MTU0.TCNT	R/(W)*1

Note 1. Only 1 can be written to this bit, and doing so sets the flag.
TCSYSTR is automatically cleared after 1 is written to.

TCSYSTR specifies synchronous start of the counters.

SCH7 Bit (Timer Start 7)

This bit controls synchronous start of MTU7.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST7 bit while SCH7 = 1

SCH6 Bit (Timer Start 6)

This bit controls synchronous start of MTU6.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST6 bit while SCH6 = 1

SCH4 Bit (Timer Start 4)

This bit controls synchronous start of MTU4.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST4 bit while SCH4 = 1

SCH3 Bit (Timer Start 3)

This bit controls synchronous start of MTU3.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST3 bit while SCH3 = 1

SCH2 Bit (Timer Start 2)

This bit controls synchronous start of MTU2.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST2 bit while SCH2 = 1

SCH1 Bit (Timer Start 1)

This bit controls synchronous start of MTU1.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST1 bit while SCH1 = 1

SCH0 Bit (Timer Start 0)

This bit controls synchronous start of MTU0.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST0 bit while SCH0 = 1

22.2.16 Timer Read/Write Enable Registers (TRWERA and TRWERB)

Address(es): MTU.TRWERA 000C 1284h, MTU.TRWERB 000C 1A84h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RWE
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RWE	Read/Write Enable	0: Read/write access to the registers is disabled 1: Read/write access to the registers is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TRWERA enables or disables access to the registers and counters that have write-protection capability against accidental modification in MTU3 and MTU4.
TRWERB enables or disables access to the registers and counters that have write-protection capability against accidental modification in MTU6 and MTU7.

RWE Bit (Read/Write Enable)

This bit enables or disables access to the registers that have write-protection capability against accidental modification.
[Clearing condition]

- When 0 is written to the RWE bit after reading RWE = 1

- Registers and Counters having Write-Protection Capability against Accidental Modification (TRWERA)
  22 registers: MTUn.TCR, MTUn.TMDR1, MTUn.TIORH, MTUn.TIORL, MTUn.TIER, MTUn.TGRA, MTUn.TGRB, TOERA, TOCR1A, TOCR2A, TGCRA, TCDRA, TDDRA, and MTUn.TCNT (n = 3 or 4)
- Registers and Counters having Write-Protection Capability against Accidental Modification (TRWERB)
  21 registers: MTUn.TCR, MTUn.TMDR1, MTUn.TIORH, MTUn.TIORL, MTUn.TIER, MTUn.TGRA, MTUn.TGRB, TOERB, TOCR1B, TOCR2B, TCDRB, TDDRB, and MTUn.TCNT (n = 6 or 7)

22.2.17 Timer Output Master Enable Register (TOER)

- TOERA

Address(es): MTU.TOERA 000C 120Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OE3B	Master Enable MTIOC3B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b1	OE4A	Master Enable MTIOC4A	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b2	OE4B	Master Enable MTIOC4B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b3	OE3D	Master Enable MTIOC3D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b4	OE4C	Master Enable MTIOC4C	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b5	OE4D	Master Enable MTIOC4D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. To output a non-active level from each pin when MTU output is disabled, make necessary settings for non-active level output from general I/O ports in the data direction registers (PDR), port output data registers (PODR), and port mode register (PMR) in advance. For details, refer to I/O Ports section.

TOERA enables or disables output settings for output pins MTIOC4D, MTIOC4C, MTIOC3D, MTIOC4B, MTIOC4A, and MTIOC3B.

TOERB enables or disables output settings for output pins MTIOC7D, MTIOC7C, MTIOC6D, MTIOC7B, MTIOC7A, and MTIOC6B.

These pins do not output correctly if the TOER bits have not been set. In MTU3, MTU4, MTU6, and MTU7, set TOER prior to setting TIOR.

Set MTU.TOERA after clearing the CST3 and CST4 bits in MTU.TSTRA to 0.

Set MTU.TOERB after clearing the CST0 and CST1 bits in MTU.TSTRB to 0 (see Figure 22.36 and Figure 22.39).

- TOERB

Address(es): MTU.TOERB 000C 1A0Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OE7D	OE7C	OE6D	OE7B	OE7A	OE6B
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OE6B	Master Enable MTIOC6B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b1	OE7A	Master Enable MTIOC7A	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b2	OE7B	Master Enable MTIOC7B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b3	OE6D	Master Enable MTIOC6D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b4	OE7C	Master Enable MTIOC7C	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b5	OE7D	Master Enable MTIOC7D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. To output a non-active level from each pin when MTU output is disabled, make necessary settings for non-active level output from general I/O ports in the data direction registers (PDR), port output data registers (PODR), and port mode register (PMR) in advance. For details, refer to I/O Ports section.

22.2.18 Timer Output Control Registers 1 (TOCR1A and TOCR1B)

Address(es): MTU.TOCR1A 000C 120Eh, MTU.TOCR1B 000C 1A0Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
Value after reset:	0	0	0	0	0*4	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSP	Output Level Select P*1, *3	See Table 22.37.	R/W
b1	OLSN	Output Level Select N*1, *3	See Table 22.38.	R/W
b2	TOCS	TOC Select	0: TOCR1j setting is selected (j = A or B) 1: TOCR2j setting is selected	R/W
b3	TOCL	TOC Register Write Protection*2	0: Write access to the TOCS, OLSN, and OLSP bits is enabled 1: Write access to the TOCS, OLSN, and OLSP bits is disabled	R/W
b5, b4	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b6	PSYE	PWM Synchronous Output Enable	0: Toggle output is disabled 1: Toggle output is enabled	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Clearing the TOCR1j.TOCS bit to 0 makes this bit setting valid.
Note 2. Setting the TOCR1j.TOCL bit to 1 prevents accidental modification when the CPU goes out of control.
Note 3. If dead-time is not generated, the negative-phase output is always the exact inverse of the positive-phase output. In this case, only the OLSP bit is valid.
Note 4. This bit can be set to 1 only once after a reset. After 1 is written, 0 cannot be written to the bit.

TOCR1A and TOCR1B enable or disable PWM-synchronized toggle output in complementary PWM mode and reset-synchronized PWM mode, and control inversion of PWM output level.

OLSP Bit (Output Level Select P)

This bit selects the positive-phase output level in reset-synchronized PWM mode and complementary PWM mode.

OLSN Bit (Output Level Select N)

This bit selects the negative-phase output level in reset-synchronized PWM mode and complementary PWM mode.

TOCS Bit (TOC Select)

This bit selects either the TOCR1j or TOCR2j (j = A or B) setting to be used for the output level in complementary PWM mode and reset-synchronized PWM mode.

TOCL Bit (TOC Register Write Protection)

This bit enables or disables write access to the TOCS, OLSN, and OLSP bits in TOCR1j (j = A or B).

PSYE Bit (PWM Synchronous Output Enable)

This bit enables or disables toggle output synchronized with the PWM cycle.

Table 22.37 Output Level Select Function

Bit 0			Function	
			Compare Match Output	
OLSP	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	Low	High
1	Low	High	High	Low

Table 22.38 Output Level Select Function

Bit 1			Function	
			Compare Match Output	
OLSN	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	High	Low
1	Low	High	Low	High

Note: • The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Figure 22.3 shows an example of output in complementary PWM mode (one phase) when OLSN = 1 and OLSP = 1.

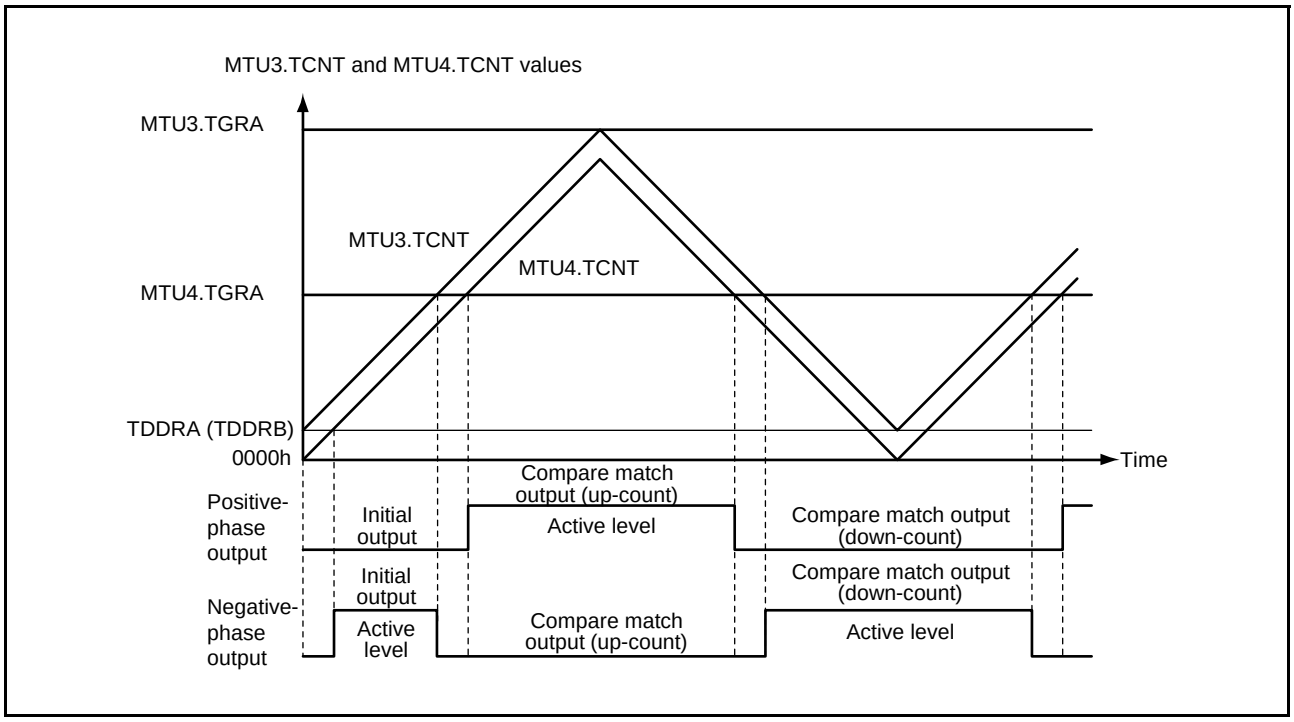


Figure 22.3 Example of Output in Complementary PWM Mode

22.2.19 Timer Output Control Registers 2 (TOCR2A and TOCR2B)

Address(es): MTU.TOCR2A 000C 120Fh, MTU.TOCR2B 000C 1A0Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P*1, *2	This bit selects the output level on MTIOC3B or MTIOC6B in reset-synchronized PWM mode and complementary PWM mode. See Table 22.39.	R/W
b1	OLS1N	Output Level Select 1N *1, *2	This bit selects the output level on MTIOC3D or MTIOC6D in reset-synchronized PWM mode and complementary PWM mode. See Table 22.40.	R/W
b2	OLS2P	Output Level Select 2P*1, *2	This bit selects the output level on MTIOC4A or MTIOC7Ain reset-synchronized PWM mode and complementary PWM mode. See Table 22.41.	R/W
b3	OLS2N	Output Level Select 2N *1, *2	This bit selects the output level on MTIOC4C or MTIOC7C in reset-synchronized PWM mode and complementary PWM mode. See Table 22.42.	R/W
b4	OLS3P	Output Level Select 3P*1, *2	This bit selects the output level on MTIOC4B or MTIOC7B in reset-synchronized PWM mode and complementary PWM mode. See Table 22.43.	R/W
b5	OLS3N	Output Level Select 3N*1, *2	This bit selects the output level on MTIOC4D or MTIOC7D in reset-synchronized PWM mode and complementary PWM mode. See Table 22.44.	R/W
b7, b6	BF[1:0]	TOLBR Buffer Transfer Timing Select	These bits select the timing for transferring data from TOLBRj to TOCR2j. See Table 22.45 for details.	R/W

j = A or B

Note 1. Setting the TOCR1j.TOCS bit to 1 makes this bit setting valid.

Note 2. If dead-time is not generated, the negative-phase output is always the exact inverse of the positive-phase output. In this case, only the OLSiP bits are valid (i = 1 to 3).

TOCR2A and TOCR2B control inversion of PWM output level in complementary PWM mode and reset-synchronized PWM mode.

Table 22.39 MTIOCmB Output Level Select Function

Bit 0	Function			
			Compare Match Output	
OLS1P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	Low	High
1	Low	High	High	Low

m = 3 or 6

Table 22.40 MTIOCmD Output Level Select Function

Bit 1	Function			
			Compare Match Output	
OLS1N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	High	Low
1	Low	High	Low	High

m = 3 or 6

Note: • The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 22.41 MTIOCmA Output Level Select Function

Bit 2	Function			
			Compare Match Output	
OLS2P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	Low	High
1	Low	High	High	Low

m = 4 or 7

Table 22.42 MTIOCmC Output Level Select Function

Bit 3	Function			
			Compare Match Output	
OLS2N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	High	Low
1	Low	High	Low	High

m = 4 or 7

Note: • The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 22.43 MTIOCmB Output Level Select Function

Bit 4	Function			
			Compare Match Output	
OLS3P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	Low	High
1	Low	High	High	Low

m = 4 or 7

Table 22.44 MTIOCmD Output Level Select Function

Bit 5	Function			
			Compare Match Output	
OLS3N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High	Low	High	Low
1	Low	High	Low	High

m = 4 or 7

Note: • The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 22.45 Setting of TOCR2j.BF[1:0] Bits

Bit 7	Bit 6	Description	
BF1	BF0	Complementary PWM Mode	Reset-Synchronized PWM Mode
0	0	Does not transfer data from the buffer register (TOLBRj) to TOCR2j.	Does not transfer data from the buffer register (TOLBRj) to TOCR2j.
0	1	Transfers data from the buffer register (TOLBRj) to TOCR2j at the crest of the MTUn.TCNT count.	Transfers data from the buffer register (TOLBRj) to TOCR2j when MTUm.TCNT or MTUn.TCNT is cleared.
1	0	Transfers data from the buffer register (TOLBRj) to TOCR2j at the trough of the MTUn.TCNT count.	Setting prohibited
1	1	Transfers data from the buffer register (TOLBRj) to TOCR2j at the crest and trough of the MTUn.TCNT count.	Setting prohibited

n = 4 or 7, m = 3 or 6, j = A or B

22.2.20 Timer Output Level Buffer Registers (TOLBRA and TOLBRB)

Address(es): MTU.TOLBRA 000C 1236h, MTU.TOLBRB 000C 1A36h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P	Specify the buffer value to be transferred to the OLS1P bit in TOCR2j.	R/W
b1	OLS1N	Output Level Select 1N	Specify the buffer value to be transferred to the OLS1N bit in TOCR2j.	R/W
b2	OLS2P	Output Level Select 2P	Specify the buffer value to be transferred to the OLS2P bit in TOCR2j.	R/W
b3	OLS2N	Output Level Select 2N	Specify the buffer value to be transferred to the OLS2N bit in TOCR2j.	R/W
b4	OLS3P	Output Level Select 3P	Specify the buffer value to be transferred to the OLS3P bit in TOCR2j.	R/W
b5	OLS3N	Output Level Select 3N	Specify the buffer value to be transferred to the OLS3N bit in TOCR2j.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

j = A or B

TOLBRA and TOLBRB are buffer registers for TOCR2A and TOCR2B and specify the PWM output level in complementary PWM mode and reset-synchronized PWM mode.

Figure 22.4 shows an example of the PWM output level setting procedure in buffer operation.

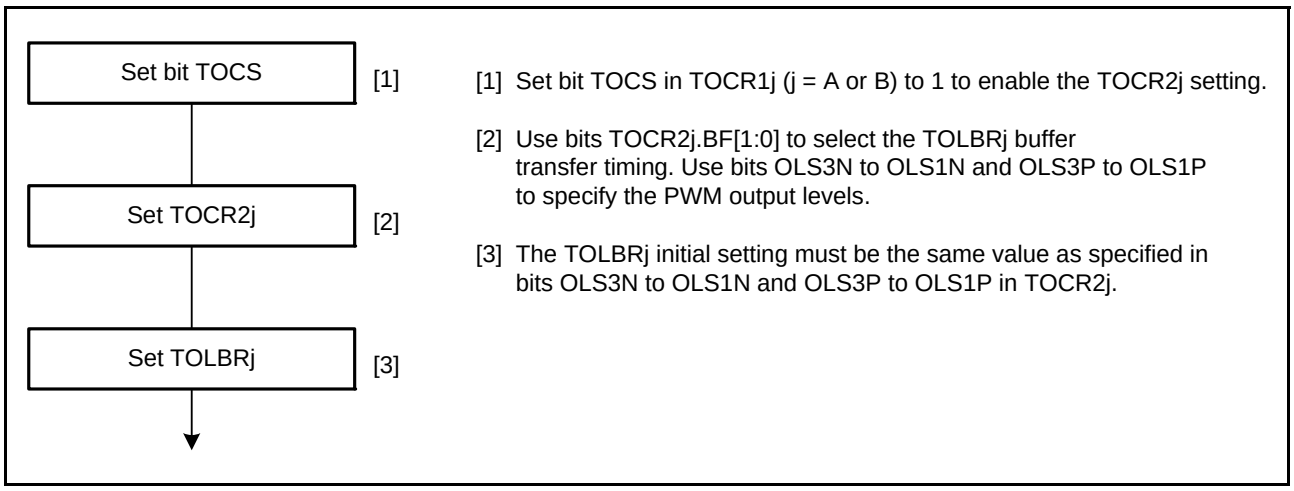


Figure 22.4 Example of PWM Output Level Setting Procedure in Buffer Operation

22.2.21 Timer Gate Control Register A (TGCRA)

Address(es): MTU.TGCRA 000C 120Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	BDC	N	P	FB	WF	VF	UF
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	UF	Output Phase Switch	These bits turn on or off the positive-phase/negative-phase output. The setting of these bits is valid only when the TGCR.FB bit s set to 1. In this case, the setting of b0 to b2 is used instead of the external input. See Table 22.46.	R/W
b1	VF			R/W
b2	WF			R/W
b3	FB	External Feedback Signal Enable	0: Output is switched by external input (input sources are TGRA, TGRB, and TGRC input capture signals in MTU0) 1: Output is switched by software (TGCRA's UF, VF, and WF settings)	R/W
b4	P	Positive-Phase Output (P) Control	0: Level output 1: Reset-synchronized PWM or complementary PWM output	R/W
b5	N	Negative-Phase Output (N) Control	0: Level output 1: Reset-synchronized PWM or complementary PWM output	R/W
b6	BDC	Brushless DC Motor	0: Ordinary output 1: Functions of this register are made effective	R/W
b7	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

TGCRA controls the output waveform necessary for brushless DC motor control in reset-synchronized PWM mode and complementary PWM mode. TGCRA register settings are ineffective for anything other than complementary PWM mode and reset-synchronized PWM mode.

UF, VF, and WF Bits (Output Phase Switch)

The setting of these bits are valid only when the TGCR.FB bit is set to 1. In this case, the setting of b0 to b2 is used instead of the external input. See Table 22.46.

FB Bit (External Feedback Signal Enable)

This bit selects whether the positive-/negative-phase output is switched automatically with the TGRA, TGRB, and TGRC input capture signals in MTU0 or by writing 0 or 1 to bits 2 to 0 in TGCRA.

P Bit (Positive-Phase Output (P) Control)

This bit selects the level output or the reset-synchronized PWM/complementary PWM output for the positive-phase output pins (MTIOC3B, MTIOC4A, and MTIOC4B pins).

N Bit (Negative-Phase Output (N) Control)

This bit selects the level output or the reset-synchronized PWM/complementary PWM output for the negative-phase output pins (MTIOC3D, MTIOC4C, and MTIOC4D pins).

BDC Bit (Brushless DC Motor)

This bit selects whether to make the functions of TGCRA effective or ineffective.

Table 22.46 Output Level Select Function

Bit 2	Bit 1	Bit 0	Function					
			MTIOC3B	MTIOC4A	MTIOC4B	MTIOC3D	MTIOC4C	MTIOC4D
WF	VF	UF	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase
0	0	0	OFF	OFF	OFF	OFF	OFF	OFF
0	0	1	ON	OFF	OFF	OFF	OFF	ON
0	1	0	OFF	ON	OFF	ON	OFF	OFF
0	1	1	OFF	ON	OFF	OFF	OFF	ON
1	0	0	OFF	OFF	ON	OFF	ON	OFF
1	0	1	ON	OFF	OFF	OFF	ON	OFF
1	1	0	OFF	OFF	ON	ON	OFF	OFF
1	1	1	OFF	OFF	OFF	OFF	OFF	OFF

22.2.22 Timer Subcounters (TCNTSA and TCNTSB)

Address(es): MTU.TCNTSA 000C 1220h, MTU.TCNTSB 000C 1A20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note 1. TCNTSA and TCNTSB must not be accessed in eight bits; it should always be accessed in 16 bits.

TCNTSA and TCNTSB are 16-bit read-only counters that are used only in complementary PWM mode.
The initial value of TCNTSA and TCNTSB after a reset is 0000h.

22.2.23 Timer Cycle Data Registers (TCDRA and TCDRB)

Address: MTU.TCDRA 000C 1214h, MTU.TCDRB 000C 1A14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. TCDRA and TCDRB must not be accessed in eight bits; it should always be accessed in 16 bits.

TCDRA and TCDRB are 16-bit readable/writable registers used only in complementary PWM mode. Set half the PWM carrier cycle as the TCDRA and TCDRB values. TCDRA and TCDRB are constantly compared with the TCNTSA and TCNTSB counters in complementary PWM mode. If the values are matched, the TCNTSA and TCNTSB counters switch direction from counting down to counting up. The initial value of TCDRA and TCDRB after a reset is FFFFh.

22.2.24 Timer Cycle Buffer Registers (TCBRA and TCBRB)

Address(es): MTU.TCBRA 000C 1222h, MTU.TCBRB 000C 1A22h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. TCBRA and TCBRB must not be accessed in eight bits; it should always be accessed in 16 bits.

TCBRA and TCBRB are 16-bit readable/writable registers, used only in complementary PWM mode, that function as buffer registers for TCDRA and TCDRB. The TCBRA and TCBRB values are transferred to TCDRA and TCDRB with the transfer timing set in TMDR1. The initial value of TCBRA and TCBRB after a reset is FFFFh.

22.2.25 Timer Dead Time Data Registers (TDDRA and TDDRB)

Address(es): MTU.TDDRA 000C 1216h, MTU.TDDRB 000C 1A16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. TDDRA and TDDRB must not be accessed in eight bits; it should always be accessed in 16 bits.

TDDRA and TDDRB are 16-bit readable/writable registers, used only in complementary PWM mode, that specify the MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) counter offset value. In complementary PWM mode, when the MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) counters are cleared and then restarted, the TDDRA (TDDRB) value is loaded into the MTU3.TCNT (MTU6.TCNT) counter and the count operation starts. The initial value of TDDRA and TDDRB after a reset is FFFFh.

22.2.26 Timer Dead Time Enable Registers (TDERA and TDERB)

Address(es): MTU3.TDERA 000C 1234h, MTU6.TDERB 000C 1A34h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDER
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	TDER	Dead Time Enable	0: No dead time is generated 1: Dead time is generated *1	R/(W)
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. TDDRA and TDDRB must be set to 1 or a larger value.

TDERA and TDERB control dead time generation in complementary PWM mode. The MTU3 has one TDER each for MTU3 and MTU6. TDERA and TDERB should be modified only while TCNT stops.

TDER Bit (Dead Time Enable)

This bit specifies whether to generate dead time.

[Clearing condition]

When 0 is written to TDER after reading TDER = 1

22.2.27 Timer Buffer Transfer Set Registers (TBTERA and TBTERB)

Address(es): MTU.TBTERA 000C 1232h, MTU.TBTERB 000C 1A32h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BTE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1 to b0	BTE[1:0]	Buffer Transfer Disable and Interrupt Skipping Link Setting	These bits enable or disable transfer from the buffer registers*1 used in complementary PWM mode to the temporary registers, and specify whether to link the transfer with interrupt skipping function 1. For details, see Table 22.47.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Applicable buffer registers (TBTERA):
MTU3.TGRC, MTU3.TGRD, MTU4.TGRC, MTU4.TGRD, and TCBRA
Applicable buffer registers (TBTERB):
MTU6.TGRC, MTU6.TGRD, MTU7.TGRC, MTU7.TGRD, and TCBRB

TBTERA and TBTERB enable or disable transfer from the buffer registers used in complementary PWM mode to the temporary registers, and specify whether to link the transfer with interrupt skipping 1 operation.

Table 22.47 Setting of TBTERA(TBTERB).BTE[1:0] Bits

Bit 1	Bit 0	
BTE1	**BTE0**	**Description**
0	0	Enables transfer from the buffer registers to the temporary registers*1 and does not link the transfer with interrupt skipping function 1.
0	1	Disables transfer from the buffer registers to the temporary registers.
1	0	Links transfer from the buffer registers to the temporary registers with interrupt skipping function 1.*2
1	1	Setting prohibited

Note 1. Data is transferred according to the MD3 to MD0 bit setting in TMDR1. For details, refer to section 22.3.8, Complementary PWM Mode .

Note 2. When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits are cleared to 0 in the timer interrupt skipping set register (TITCR1A (TITCR1B)) or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), be sure to disable link of buffer transfer with interrupt skipping (clear the BTE1 bit in the timer buffer transfer set register (TBTERA (TBTERB)) to 0). If link with interrupt skipping is enabled while interrupt skipping is disabled, buffer transfer will not be performed.

22.2.28 Timer Waveform Control Registers (TWCRA and TWCRB)

Address(es): MTU.TWCRA 000C 1260h, MTU.TWCRB 000C 1A60h

	b7	b6	b5	b4	b3	b2	b1	b0
	CCE	—	—	—	—	—	SCC	WRE
Value after reset:	0*2	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WRE	Waveform Retain Enable	0: Initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are output 1: Initial output is inhibited	R/(W)*3
b1	SCC *1, *3	Synchronous Clearing Control	(Only valid in register TWCRB) 0: Clearing of MTU6.TCNT and MTU7.TCNT in response to synchronous clearing for MTU0, MTU1, MTU2–MTU6, MTU7 is enabled. 1: Clearing of MTU6.TCNT and MTU7.TCNT in response to synchronous clearing for MTU0, MTU1, MTU2–MTU6, MTU7 is disabled.	R/(W)
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CCE*2	Compare Match Clear Enable	0: Counters are not cleared at MTU3.TGRA (MTU6.TGRA) compare match 1: Counters are cleared at MTU3.TGRA (MTU6.TGRA) compare match	R/(W)

Note 1. This bit is only valid in register TWCRB and is a reserved bit in register TWCRA.
Note 2. Do not write 1 when complementary PWM mode 1 is not selected.
Note 3. Do not set to 1 when complementary PWM mode is not selected.

TWCRA and TWCRB control the output waveform when synchronous counter clearing occurs in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) in complementary PWM mode and specifies whether to clear the counters at MTU3.TGRA (MTU6.TGRA) compare match.
The CCE bit and WRE bit in TWCRA and TWCRB should be modified only while TCNT stops.

WRE Bit (Waveform Retain Enable)

This bit selects the waveform output when synchronous counter clearing occurs in complementary PWM mode.
The initial output is inhibited with this function only when synchronous clearing occurs within the Tb interval at the trough in complementary PWM mode. When synchronous clearing occurs outside this interval, the initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are output regardless of the WRE bit setting. The initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are also output when synchronous clearing occurs in the Tb interval at the trough immediately after MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) start operation.
For the Tb interval at the trough in complementary PWM mode, see Figure 22.41.
[Setting condition]

- When 1 is written to WRE after reading WRE = 0.

SCC Bit (Synchronous Clearing Control) (Only valid in register TWCRB)

The setting of this bit selects whether MTU6.TCNT and MTU7.TCNT are or are not cleared when counter-synchronous clearing is generated for MTU0, MTU1, MTU2–MTU6, MTU7 in complementary PWM mode.
Make the complementary PWM mode settings for MTU6 and MTU7 when this function is in use. When writing a new value to the SCC bit while the counter is operating, do so in such a way that the values of the CCE and WRE bits are not changed.
Synchronous clearing from the MTU module only becomes disabled due to the setting of the SCC bit when synchronous clearing is generated outside the Tb interval in the trough. If synchronous clearing is generated within the Tb interval in the trough including immediately after the value at which MTU6.TCNT and MTU7.TCNT start, MTU6.TCNT and MTU7.TCNT are cleared.
Regarding the Tb interval in the trough in complementary PWM mode, see Figure 22.41.
[Setting condition]

- Writing of 1 to the SCC bit after reading it as 0

The corresponding bit in register TWCRA is reserved and is always read as 0. When writing to TWCRA, always write 0 to this bit.

CCE Bit (Compare Match Clear Enable)

This bit specifies whether to clear counters at MTU3.TGRA (MTU6.TGRA) compare match in complementary PWM mode.
[Setting condition]

- When 1 is written to CCE after reading CCE = 0

22.2.29 Timer A/D Converter Start Request Control Register (TADCR)

- TADCR (MTU4)

Address(es): MTU.TADCR 000C 1240h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
Value after reset:	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB4VE *2,*3,*4	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are linked	R/W
b1	ITB3AE *2,*3,*4	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are linked	R/W
b2	ITA4VE *2,*3,*4	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are linked	R/W
b3	ITA3AE *2,*3,*4	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are linked	R/W
b4	DT4BE*4	Down-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT down-count operation	R/W
b5	UT4BE	Up-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT up-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT up-count operation	R/W
b6	DT4AE*4	Down-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b7	UT4AE	Up-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT up-count operation 1: A/D converter up requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU4.TADCOBRA/B Transfer Timing Select	See Table 22.48 for details. These bits specify the transfer timing from MTU4.TADCOBRA and MTU4.TADCOBRB to MTU4.TADCORA and MTU4.TADCORB.	R/W

Note 1. MTU4.TADCR must not be accessed in eight bits; it should always be accessed in 16 bits.
Note 2. Set this bit to 0 when the interrupt-skipping function is disabled, when bits T3AEN and T4VEN in TITCR1A are set to 0, or when bits T3ACOR and T4VCOR in TITCR1A are set to 0.
Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.
Note 4. Set this bit to 0 in modes other than complementary PWM.

TADCR enables or disables A/D converter start requests and specifies whether to link A/D converter start requests with interrupt skipping function. The MTU3 has one TADCR each for MTU4 and MTU7.

Table 22.48 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU4)

Bit 15	Bit 14	Description			
BF1	BF0	Complementary PWM mode	Reset-synchronized PWM mode	PWM mode 1	Normal mode
0	0	Does not transfer data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB.	Does not transfer data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB.	Does not transfer data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB.	Does not transfer data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB.
0	1	Transfers data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB at the crest of the MTU4.TCNT count.	Transfers data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB when compare match occurs between MTU3.TCNT and MTU3.TGRA.	Transfers data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB when compare match occurs between MTU4.TCNT and MTU4.TGRA.	Transfers data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB when compare match occurs between MTU4.TCNT and MTU4.TGRA.
1	0	Transfers data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB at the trough of the MTU4.TCNT count.	Setting prohibited	Setting prohibited	Setting prohibited
1	1	Transfers data from cycle set buffer registers MTU4.TADCOBRA and TADCOBRB to cycle set registers MTU4.TADCORA and TADCORB at the crest and trough of the MTU4.TCNT count.	Setting prohibited	Setting prohibited	Setting prohibited

- TADCR (MTU7)

Address(es): 000C 1A40h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT7AE	DT7AE	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
Value after reset:	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB7VE *2,*3,*4	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are linked	R/W
b1	ITB6AE *2,*3,*4	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are linked	R/W
b2	ITA7VE *2,*3,*4	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are linked	R/W
b3	ITA6AE *2,*3,*4	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are linked	R/W
b4	DT7BE*4	Down-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT down-count operation	R/W
b5	UT7BE	Up-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT up-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT up-count operation	R/W
b6	DT7AE*4	Down-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b7	UT7AE	Up-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT up-count operation 1: A/D converter up requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU7.TADCOBRA/B Transfer Timing Select	See Table 22.49 for details. These bits specify the transfer timing from MTU7.TADCOBRA and MTU7.TADCOBRB to MTU7.TADCORA and MTU7.TADCORB.	R/W

Note 1. MTU7.TADCR must not be accessed in eight bits; it should always be accessed in 16 bits.
Note 2. Set this bit to 0 when the interrupt-skipping function is disabled, when bits T6AEN and T7AEN in TITCR1B are set to 0, or when bits T6ACOR and T7VCOR in TITCR1B are set to 0.
Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.
Note 4. Set this bit to 0 in modes other than complementary PWM.

Table 22.49 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU7)

Bit 15	Bit 14	Description			
BF1	BF0	Complementary PWM mode	Reset-synchronized PWM mode	PWM mode 1	Normal mode
0	0	Does not transfer data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB.	Does not transfer data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB.	Does not transfer data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB.	Does not transfer data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB.
0	1	Transfers data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB at the crest of the MTU7.TCNT count.	Transfers data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB when compare match occurs between MTU6.TCNT and MTU6.TGRA.	Transfers data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB when compare match occurs between MTU7.TCNT and MTU7.TGRA.	Transfers data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB when compare match occurs between MTU7.TCNT and MTU7.TGRA.
1	0	Transfers data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB at the trough of the MTU7.TCNT count.	Setting prohibited	Setting prohibited	Setting prohibited
1	1	Transfers data from cycle set buffer registers MTU7.TADCOBRA and TADCOBRB to cycle set registers MTU7.TADCORA and TADCORB at the crest and trough of the MTU7.TCNT count.	Setting prohibited	Setting prohibited	Setting prohibited

22.2.30 Timer A/D Converter Start Request Cycle Set Registers (TADCORA and TADCORB)

Address(es): MTU4.TADCORA 000C 1244h, MTU4.TADCORB 000C 1246h
MTU7.TADCORA 000C 1A44h, MTU7.TADCORB 000C 1A46h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. MTUn.TADCORA and MTUn.TADCORB (n =4 or 7) must not be accessed in eight bits; they should always be accessed in 16 bits.

Note 2. When the A/D converter start request delaying function linked with skipping function 1 (for details, see section 22.3.9 (4), A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1) is used, the value of this register should be 0002h to TCDRA setting - 2 in MTU4 and 0002h to TCDRB setting - 2 in MTU7.

Note 3. When interrupt skipping function 2 is used and the difference between the MTUn.TADCORA value and the MTUn.TADCORB value is small, the skipping count may not be counted correctly and the A/D converter start request may not be generated with the expected timing in some cases. The TADCORA and TADCORB values should satisfy the following conditions.

(1) When skipping function 2 is specified with the skipping count set to 0
- The difference between the MTUn.TADCORA and MTUn.TADCORB values should be equal to or greater than 4.
- The MTUn.TADCORA compare interval should be equal to or greater than 4 PCLKA cycles (the MTUn.TADCORA update value should be the previous value + 4 or greater, or previous value - 4 or smaller).
- The MTUn.TADCORB compare interval should be equal to or greater than 4 PCLKA cycles (the MTUn.TADCORB update value should be the previous value + 4 or greater, or previous value - 4 or smaller).

(2) When skipping function 2 is specified with the skipping count set to 1 or greater
- The difference between the MTUn.TADCORA and MTUn.TADCORB values should be equal to or greater than 2.
- The MTUn.TADCORB compare interval should be equal to or greater than 2 PCLKA cycles (the MTUn.TADCOR update value should be the previous value + 2 or greater, or previous value - 2 or smaller)

TADCORA and TADCORB are 16-bit readable/writable registers that issue a corresponding A/D converter start request when the MTUn.TCNT (n = 4 or 7) count reaches the value in TADCORA or TADCORB.
MTUn.TADCORA and TADCORB are initialized to FFFFh by a reset.

22.2.31 Timer A/D Converter Start Request Cycle Set Buffer Registers (TADCOBRA and TADCOBRB)

Address(es): MTU4.TADCOBRA 000C 1248h, MTU4.TADCOBRB 000C 124Ah
MTU7.TADCOBRA 000C 1A48h, MTU7.TADCOBRB 000C 1A4Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. TADCOBRA and TADCOBRB must not be accessed in eight bits; it should always be accessed in 16 bits.

TADCOBRA and TADCOBRB are 16-bit readable/writable registers whose values are transferred to TADCORA and TADCORB, respectively, when the crest or trough of the MTUn.TCNT count is reached.
TADCOBRA and TADCOBRB are initialized to FFFFh by a reset.

22.2.32 Timer Interrupt Skipping Mode Registers (TITMRA and TITMRB)

Address(es): MTU.TITMRA 000C 123Ah, MTU.TITMRB 000C 1A3Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TITM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TITM	Interrupt Skipping Function Select	Selects one of the two types of interrupt skipping functions shown in Table 22.50.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TITMRA and TITMRB are used to select either of two skipping functions for the TITMRA and TITMRB registers.

Table 22.50 Interrupt Skipping Function Selected through TITM Bit

Bit 0	
TITM	**Description**
0	Selects interrupt skipping function 1 *1
1	Selects interrupt skipping function 2 *2

Note 1. TITCR1A or TITCR1B enables interrupt skipping function 1.
Note 2. TITCR2A or TITCR2B enables interrupt skipping function 2.

22.2.33 Timer Interrupt Skipping Set Registers 1 (TITCR1A and TITCR1B)

- TITCR1A

Address(es): MTU.TITMRA 000C 1230h

	b7	b6	b5	b4	b3	b2	b1	b0
	T3AEN		T3ACOR[2:0]			T4VEN	T4VCOR[2:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T4VCOR[2:0]	TCIV4 Interrupt Skipping Count Setting	These bits specify the TCIV4 interrupt skipping count within the range from 0 to 7. *1 For details, see Table 22.51.	R/W
b3	T4VEN	T4VEN	0: TCIV4 interrupt skipping disabled 1: TCIV4 interrupt skipping enabled	R/W
b6 to b4	T3ACOR[2:0]	TGIA3 Interrupt Skipping Count Setting	These bits specify the TGIA3 interrupt skipping count within the range from 0 to 7. *1 For details, see Table 22.52.	R/W
b7	T3AEN	T3AEN	0: TGIA3 interrupt skipping disabled 1: TGIA3 interrupt skipping enabled	R/W

Note 1. When 0 is specified for the interrupt skipping count, no interrupt skipping will be performed.
Before changing the interrupt skipping count, be sure to clear the TITCR1A.T3AEN and TITCR1A.T4VEN bits to 0 to clear the skipping counter (TITCNT1A).

TITCR1A and TITCR1B enable or disable interrupt skipping and specify the interrupt skipping count. This setting is valid only while TITMRA or TITMRB is set to 0; when TITMRA or TITMRB is set to 1, the setting in the corresponding TITMRA or TITMRB register is cleared.

- TITCR1B

Address(es): MTU.TITCR1B 000C 1A30h

	b7	b6	b5	b4	b3	b2	b1	b0
	T6AEN	T6ACOR[2:0]			T7VEN	T7VCOR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T7VCOR[2:0]	TCIV7 Interrupt Skipping Count Setting	These bits specify the TCIV7 interrupt skipping count within the range from 0 to 7. *1 For details, see Table 22.53.	R/W
b3	T7VEN	T7VEN	0: TCIV7 interrupt skipping disabled 1: TCIV7 interrupt skipping enabled	R/W
b6 to b4	T6ACOR[2:0]	TGIA6 Interrupt Skipping Count Setting	These bits specify the TGIA6 interrupt skipping count within the range from 0 to 7. *1 For details, see Table 22.54.	R/W
b7	T6AEN	T6AEN	0: TGIA6 interrupt skipping disabled 1: TGIA6 interrupt skipping enabled	R/W

Note 1. When 0 is specified for the interrupt skipping count, no interrupt skipping will be performed.
Before changing the interrupt skipping count, be sure to clear the TITCR1B.T6AEN and TITCR1B.T7VEN bits to 0 to clear the skipping counter (TITCNT1B).

Table 22.51 Setting of Interrupt Skipping Count by T4VCOR[2:0] Bits

Bit 2	Bit 1	Bit 0	Description
T4VCOR2	T4VCOR1	T4VCOR0	
0	0	0	Does not skip TCIV4 interrupts.
0	0	1	Sets the TCIV4 interrupt skipping count to 1.
0	1	0	Sets the TCIV4 interrupt skipping count to 2.
0	1	1	Sets the TCIV4 interrupt skipping count to 3.
1	0	0	Sets the TCIV4 interrupt skipping count to 4.
1	0	1	Sets the TCIV4 interrupt skipping count to 5.
1	1	0	Sets the TCIV4 interrupt skipping count to 6.
1	1	1	Sets the TCIV4 interrupt skipping count to 7.

Table 22.52 Setting of Interrupt Skipping Count by T3ACOR[2:0] Bits

Bit 6	Bit 5	Bit 4	
T3ACOR2	T3ACOR1	T3ACOR0	Description
0	0	0	Does not skip TGIA3 interrupts.
0	0	1	Sets the TGIA3 interrupt skipping count to 1.
0	1	0	Sets the TGIA3 interrupt skipping count to 2.
0	1	1	Sets the TGIA3 interrupt skipping count to 3.
1	0	0	Sets the TGIA3 interrupt skipping count to 4.
1	0	1	Sets the TGIA3 interrupt skipping count to 5.
1	1	0	Sets the TGIA3 interrupt skipping count to 6.
1	1	1	Sets the TGIA3 interrupt skipping count to 7.

Table 22.53 Setting of Interrupt Skipping Count by T7VCOR[2:0] Bits

Bit 2	Bit 1	Bit 0	
T7VCOR2	T7VCOR1	T7VCOR0	Description
0	0	0	Does not skip TCIV7 interrupts.
0	0	1	Sets the TCIV7 interrupt skipping count to 1.
0	1	0	Sets the TCIV7 interrupt skipping count to 2.
0	1	1	Sets the TCIV7 interrupt skipping count to 3.
1	0	0	Sets the TCIV7 interrupt skipping count to 4.
1	0	1	Sets the TCIV7 interrupt skipping count to 5.
1	1	0	Sets the TCIV7 interrupt skipping count to 6.
1	1	1	Sets the TCIV7 interrupt skipping count to 7.

Table 22.54 Setting of Interrupt Skipping Count by T6ACOR[2:0] Bits

Bit 6	Bit 5	Bit 4	
T6ACOR2	**T6ACOR1**	**T6ACOR0**	**Description**
0	0	0	Does not skip TGIA6 interrupts.
0	0	1	Sets the TGIA6 interrupt skipping count to 1.
0	1	0	Sets the TGIA6 interrupt skipping count to 2.
0	1	1	Sets the TGIA6 interrupt skipping count to 3.
1	0	0	Sets the TGIA6 interrupt skipping count to 4.
1	0	1	Sets the TGIA6 interrupt skipping count to 5.
1	1	0	Sets the TGIA6 interrupt skipping count to 6.
1	1	1	Sets the TGIA6 interrupt skipping count to 7.

22.2.34 Timer Interrupt Skipping Counters 1 (TITCNT1A and TITCNT1B)

- TITCNT1A

Address(es): MTU.TITCNT1A 000C 1231h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	T3ACNT[2:0]			—	T4VCNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T4VCNT[2:0]	TCIV4 Interrupt Counter	While the T4VEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TCIV4 interrupt occurs.	R
b3	—	Reserved	This bit is always read as 0. Writing to this bit has no effect.	R
b6 to b4	T3ACNT[2:0]	TGIA3 Interrupt Counter	While the T3AEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TGIA3 interrupt occurs.	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. To clear the TITCNT1A, clear the TITCR1A.T3AEN and TITCR1A.T4VEN bits to 0.

TITCNT1A and TITCNT1B are 8-bit readable/writable counters. TITCNT1A and TITCNT1B retain their values even after stopping the count operation of MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT).

T4VCNT[2:0] Bits (TCIV4 Interrupt Counter)

[Clearing conditions]

- When the TITM bit in TITMRA is 1
- When the T4VEN bit in TITCR1A is cleared to 0
- When the T4VCOR[2:0] bits in TITCR1A are cleared to 000b
- When the T4VCNT[2:0] bits in TITCNT1A match the T4VCOR[2:0] bits in TITCR1A

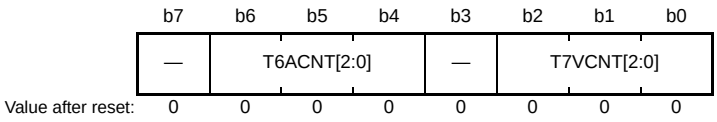
T3ACNT[2:0] Bits (TGIA3 Interrupt Counter)

[Clearing conditions]

- When the TITM bit in TITMRA is 1
- When the T3AEN bit in TITCR1A is cleared to 0
- When the T3ACOR[2:0] bits in TITCR1A are cleared to 000b
- When the T3ACNT[2:0] bits in TITCNT1A match the T3ACOR[2:0] bits in TITCR1A

- TITCNT1B

Address(es): MTU.TITCNT1B 000C 1A31h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T7VCNT[2:0]	TCIV7 Interrupt Counter	While the T7VEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TCIV7 interrupt occurs.	R
b3	—	Reserved	This bit is always read as 0. Writing to this bit has no effect.	R
b6 to b4	T6ACNT[2:0]	TGIA6 Interrupt Counter	While the T6AEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TGIA6 interrupt occurs.	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. To clear the TITCNT1B, clear the TITCR1B.T6AEN and TITCR1B.T7VEN bits to 0.

T7VCNT[2:0] Bits (TCIV7 Interrupt Counter)

[Clearing conditions]

- When the TITM bit in TITMRB is 1
- When the T7VEN bit in TITCR1B is cleared to 0
- When the T7VCOR[2:0] bits in TITCR1B are cleared to 000b
- When the T7VCNT[2:0] bits in TITCNT1B match the T7VCOR[2:0] bits in TITCR1B

T6ACNT[2:0] Bits (TGIA6 Interrupt Counter)

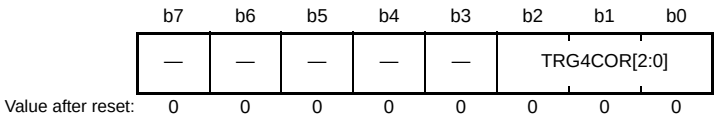
[Clearing conditions]

- When the TITM bit in TITMRB is 1
- When the T6AEN bit in TITCR1B is cleared to 0
- When the T6ACOR[2:0] bits in TITCR1B are cleared to 000b
- When the T6ACNT[2:0] bits in TITCNT1B match the T6ACOR[2:0] bits in TITCR1B

22.2.35 Timer Interrupt Skipping Set Registers 2 (TITCR2A and TITCR2B)

- TITCR2A

Address(es): MTU.TITCR2A 000C 123Bh



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG4COR[2:0]	TRG4AN/TRG4BN Interrupt Skipping Count Setting	These bits specify the TRG4AN/TRG4BN interrupt skipping count within the range from 0 to 7. For details, see Table 22.55.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TITCR2A and TITCR2B specify the interrupt skipping count for TRG4AN and TRG4BN (TRG7AN and TRG7BN). This setting is valid only while TITMRA or TITMRB is set to 1.

Table 22.55 Setting of Interrupt Skipping Count by TRG4COR[2:0] Bits

Bit 2	Bit 1	Bit 0	
TRG4COR2	TRG4COR1	TRG4COR0	Description
0	0	0	Does not skip TRG4AN and TRG4BN interrupts.
0	0	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 1.
0	1	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 2.
0	1	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 3.
1	0	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 4.
1	0	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 5.
1	1	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 6.
1	1	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 7.

- TITCR2B

Address(es): MTU.TITCR2B 000C 1A3Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG7COR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG7COR[2:0]	TRG7AN/TRG7BN Interrupt Skipping Count Setting	These bits specify the TRG7AN/TRG7BN interrupt skipping count within the range from 0 to 7. For details, see Table 22.56.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 22.56 Setting of Interrupt Skipping Count by TRG7COR[2:0] Bits

Bit 2	Bit 1	Bit 0	
TRG7COR2	TRG7COR1	TRG7COR0	Description
0	0	0	Does not skip TRG7AN and TRG7BN interrupts.
0	0	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 1.
0	1	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 2.
0	1	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 3.
1	0	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 4.
1	0	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 5.
1	1	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 6.
1	1	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 7.

22.2.36 Timer Interrupt Skipping Counters 2 (TITCNT2A and TITCNT2B)

- TITCNT2A

Address(es): MTU.TITCNT2A 000C 123Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG4CNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG4CNT[2:0]	TRG4AN/TRG4BN Interrupt Counter	These bits start counting from the value set in TRG4COR[2:0] and the count decrements every time TRG4AN or TRG4BN is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts become valid.	R
b7 to b3	—	Reserved	These bits are read as 0. Writing to this bit has no effect.	R

TITCNT2A and TITCNT2B start counting from the values set in the TRG4COR[2:0] and TRG7COR[2:0] bits and the count decrements every time TRG4AN or TRG4BN (TITCNT2A) is generated or TRG7AN or TRG7BN (TITCNT2B) is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts or the TRG7AN and TRG7BN interrupts become valid.

TRG4CNT[2:0] Bits (TRG4AN/TRG4BN Interrupt Counter)

These bits start counting from the value set in the TRG4COR[2:0] bits and the count decrements every time a TRG4AN or TRG4BN interrupt is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts become valid.

[Clearing conditions]

- When the TITM bit in TITMRA is 0
- When the TRG4COR[2:0] bits in TITCR2A are cleared to 000b
- When the count of TRG4AN and TRG4BN occurrence matches the TRG4COR[2:0] value in TITCR2A

- TITCNT2B

Address(es): MTU.TITCNT2B 000C 1A3Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG7CNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG7CNT[2:0]	TRG7AN/TRG7BN Interrupt Counter	These bits start counting from the value set in TRG7COR[2:0] and the count decrements every time TRG7AN or TRG7BN is generated. When the count reaches 0 and is reloaded, the TRG7AN and TRG7BN interrupts become valid.	R
b7 to b3	—	Reserved	These bits are read as 0. Writing to this bit has no effect.	R

TRG7CNT[2:0] Bits (TRG7AN/TRG7BN Interrupt Counter)

These bits start counting from the value set in the TRG7COR[2:0] bits and the count decrements every time a TRG7AN or TRG7BN interrupt is generated. When the count reaches 0 and is reloaded, the TRG7AN and TRG7BN interrupts become valid.

[Clearing conditions]

- When the TITM bit in TITMRB is 0
- When the TRG7COR[2:0] bits in TITCR2B are cleared to 000b
- When the count of TRG7AN and TRG7BN occurrence matches the TRG7COR[2:0] value in TITCR2B

22.2.37 Bus Master Interface

The timer counters (TCNT), general registers (TGR), timer subcounters (TCNTSA and TCNTSB), timer cycle buffer registers (TCBRA and TCBRB), timer dead time data registers (TDDRA and TDDRB), timer cycle data registers (TCDRA and TCDRB), timer A/D converter start request control registers (MTU4.TADCR and MTU7.TADCR), timer A/D converter start request cycle set registers (MTU4.TADCORA, MTU4.TADCORB, MTU7.TADCORA, and MTU7.TADCORB), and timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA, MTU4.TADCOBRB, MTU7.TADCOBRA, and MTU7.TADCOBRB) are 16-bit registers. A 16-bit data bus to the bus master enables 16-bit read/write access. 8-bit read/write is not allowed. Always access the registers in 16-bit units.
All registers other than the above registers are 8-bit registers. They can be read/written in 8-bit units.

22.3 Operation

22.3.1 Basic Functions

Each channel has TCNT and TGR. TCNT performs up-counting, and is also capable of free-running operation, periodic counting, and external event counting.
Each TGR can be used as an input capture register or an output compare register.

(1) Counter Operation

When one of bits CST0 to CST4 in TSTRA, bits CST6 and CST7 in TSTRB, and bits CSTU5, CSTV5, and CSTW5 in MTU5.TSTR is set to 1, TCNT for the corresponding channel begins counting. TCNT can operate as a free-running counter, periodic counter, for example.

(a) Example of Count Operation Setting Procedure

Figure 22.5 shows an example of the count operation setting procedure.

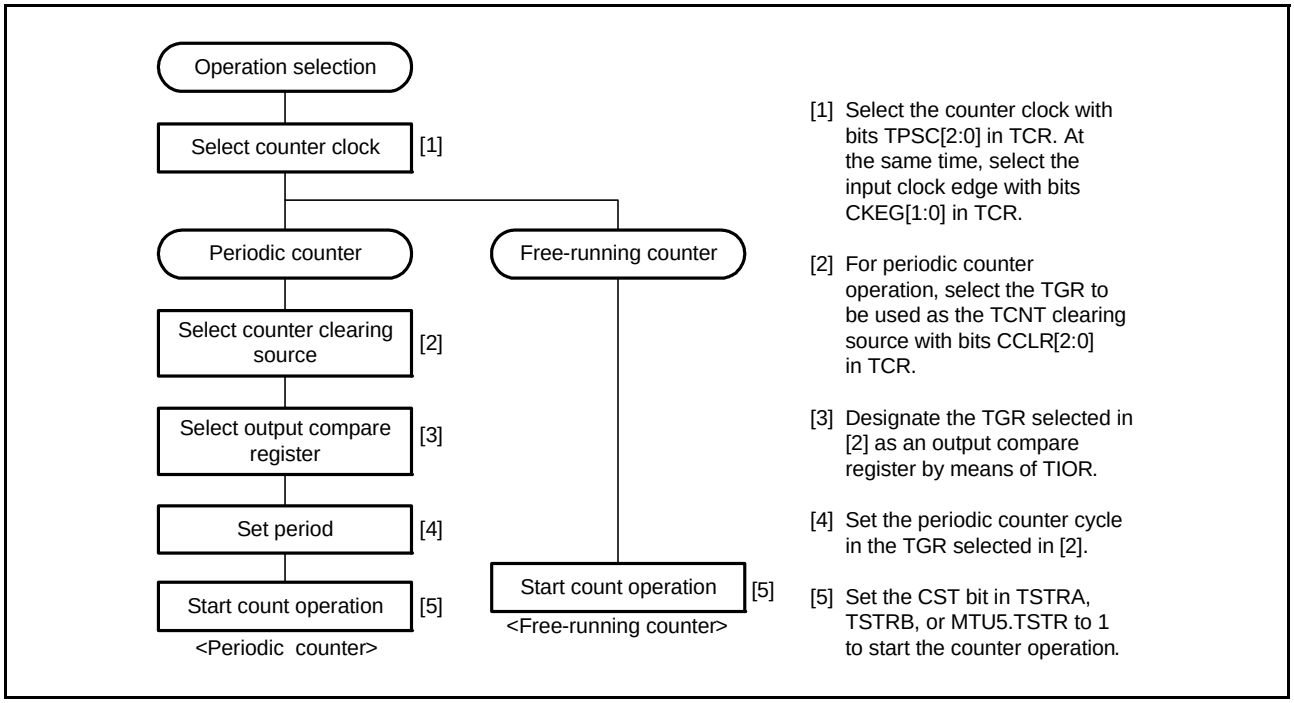


Figure 22.5 Example of Counter Operation Setting Procedure

(b) Free-Running Count Operation and Periodic Count Operation

Immediately after a reset, the MTU's TCNT counters are all designated as free-running counters. When the relevant bit in TSTRA, TSTRB, or MTU5.TSTR is set to 1, the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from FFFFh to 0000h), the TSR.TCFV flag is set to 1. If the corresponding TIER.TCIEV bit is 1 at this point, the MTU requests an interrupt. After an overflow, TCNT starts counting up again from 0000h.

Figure 22.6 illustrates free-running counter operation.

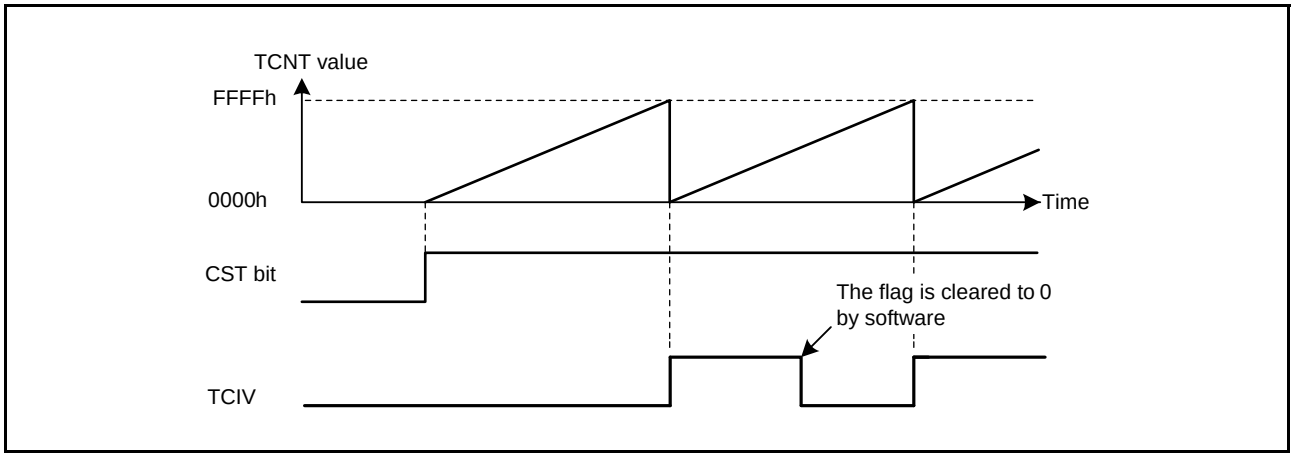


Figure 22.6 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, TCNT for the relevant channel performs periodic count operation. TGR for setting the cycle is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR[2:0] in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTRA, TSTRB or MTU5.TSTR is set to 1. When the count matches the value in TGR, the TSR.TGF flag is set to 1 and TCNT is cleared to 0000h.

If the value of the corresponding TIER.TGIE bit is 1 at this point, the MTU requests an interrupt. After a compare match, TCNT starts counting up again from 0000h.

Figure 22.7 illustrates periodic counter operation.

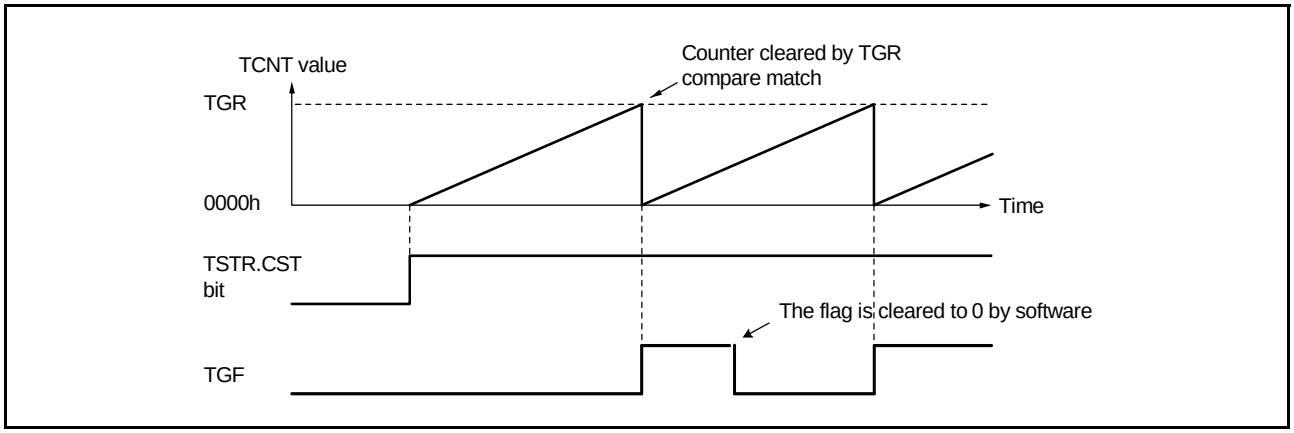


Figure 22.7 Periodic Counter Operation

(2) Waveform Output by Compare Match

The MTU can output low or high or toggles output from the corresponding output pin using compare match.

(a) Example of Procedure for Setting Waveform Output by Compare Match

Figure 22.8 shows an example of the procedure for setting waveform output by compare match

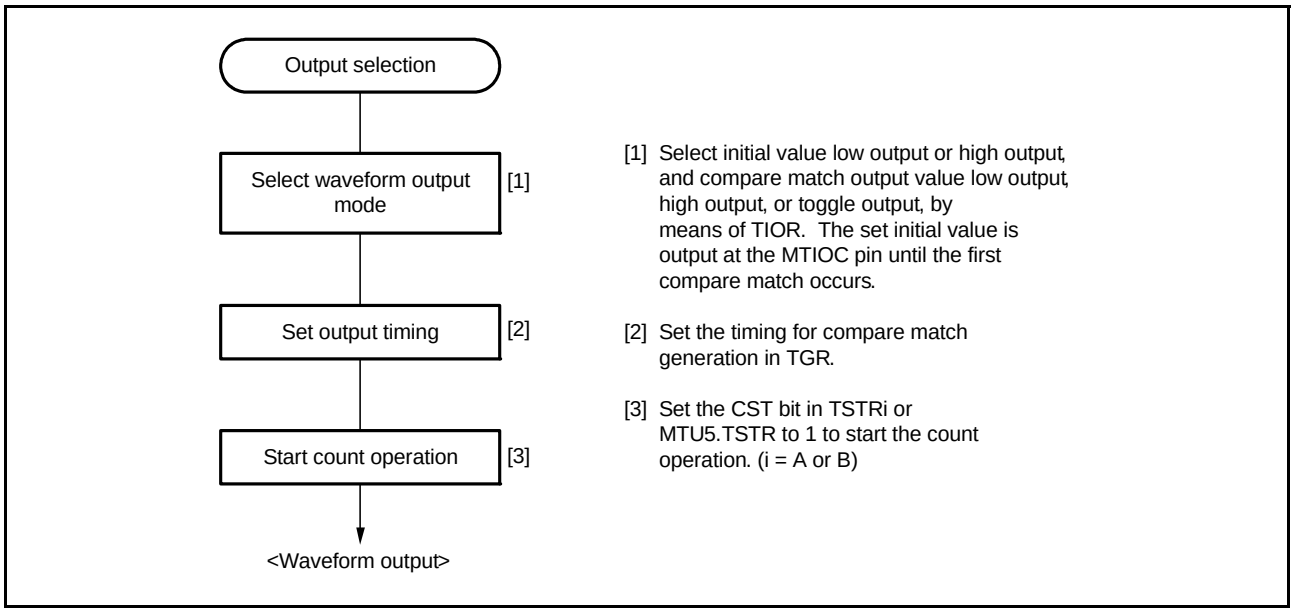


Figure 22.8 Example of Procedure for Setting Waveform Output by Compare Match

(b) Examples of Waveform Output Operation

Figure 22.9 shows an example of low output and high output.
In this example, TCNT has been designated as a free-running counter, and settings have been made so that high is output by compare match A and low is output by compare match B. When the pin level is the same as the specified level, the pin level does not change.

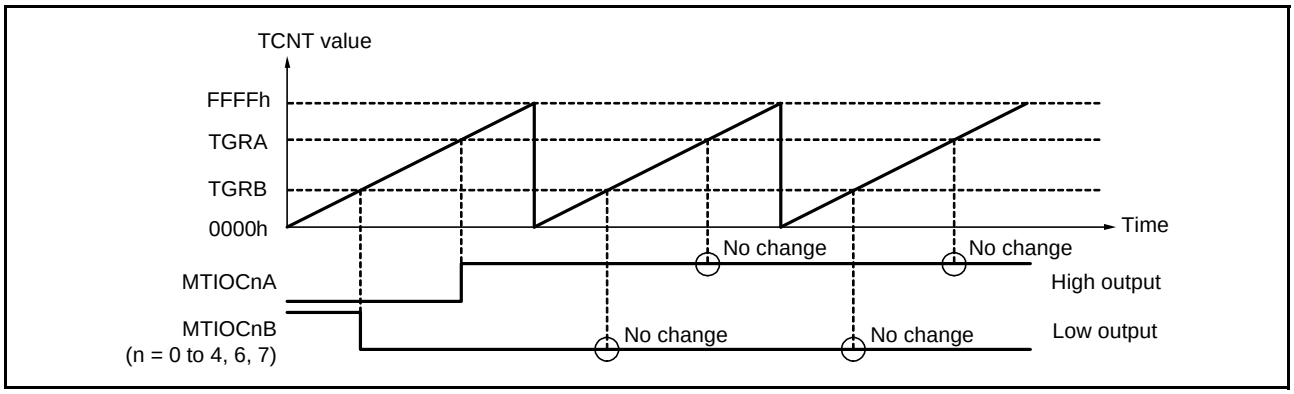


Figure 22.9 Example of low output and high output Operation

Figure 22.10 shows an example of toggle output.
In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made so that the output is toggled by both compare match A and compare match B.

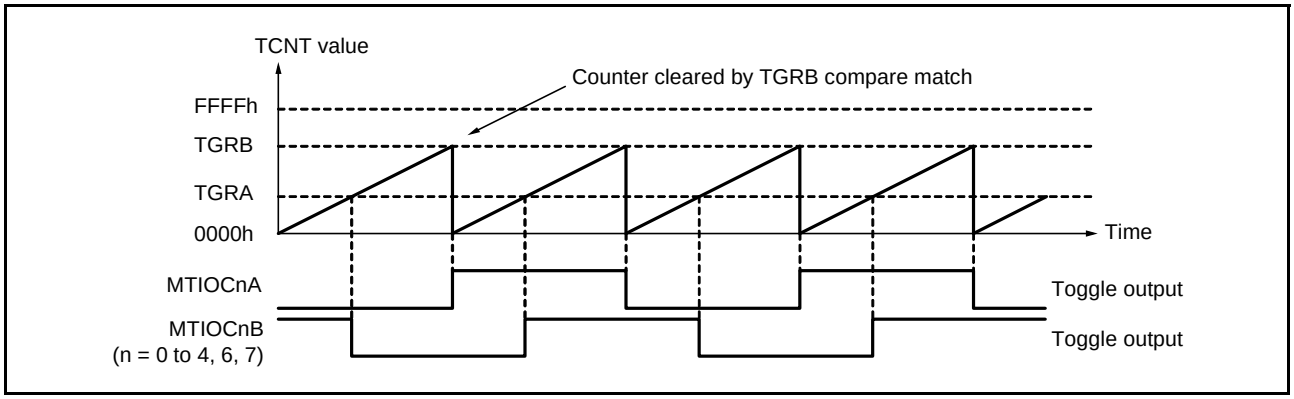


Figure 22.10 Example of Toggle Output Operation

(3) Input Capture Function

The TCNT value can be transferred to TGR on detection of the MTIOCnm pin input edge (n = 0 to 4, 6, 7; m = A to D). The rising edge, falling edge, or both edges can be selected as the detection edge. For MTU0 and MTU1, another channel's counter input clock or compare match signal can also be specified as the input capture source.

Note: • When another channel's counter input clock is used as the input capture input for MTU0 and MTU1, PCLKA/1 should not be selected as the counter input clock used for input capture input. Input capture will not be generated if PCLKA/1 is selected.

(a) Example of Input Capture Operation Setting Procedure

Figure 22.11 shows an example of the input capture operation setting procedure.

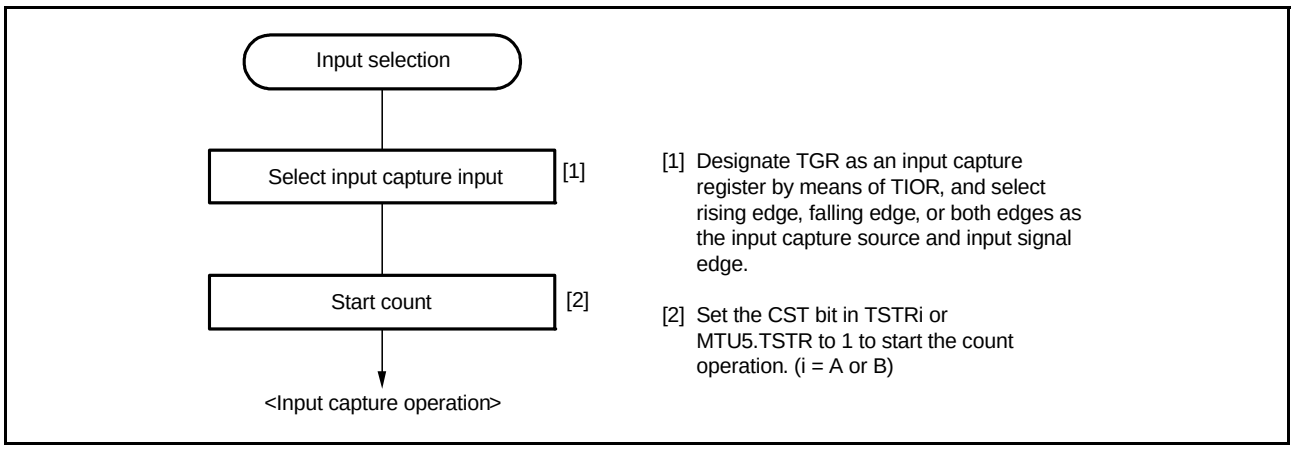


Figure 22.11 Example of Input Capture Operation Setting Procedure

(b) Example of Input Capture Operation

Figure 22.12 shows an example of input capture operation.
In this example, both rising and falling edges have been selected as the MTIOCnA pin input capture input edge, the falling edge has been selected as the MTIOCnB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT. (n = 0 to 4, 6, 7)

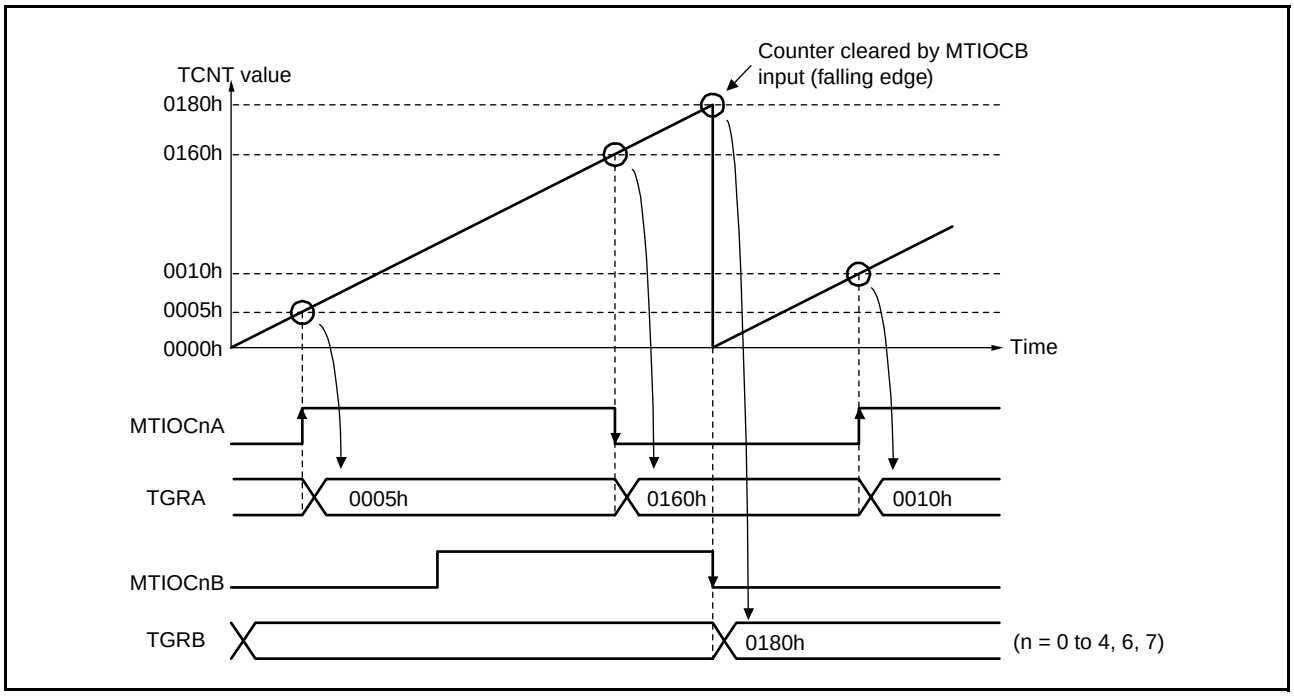


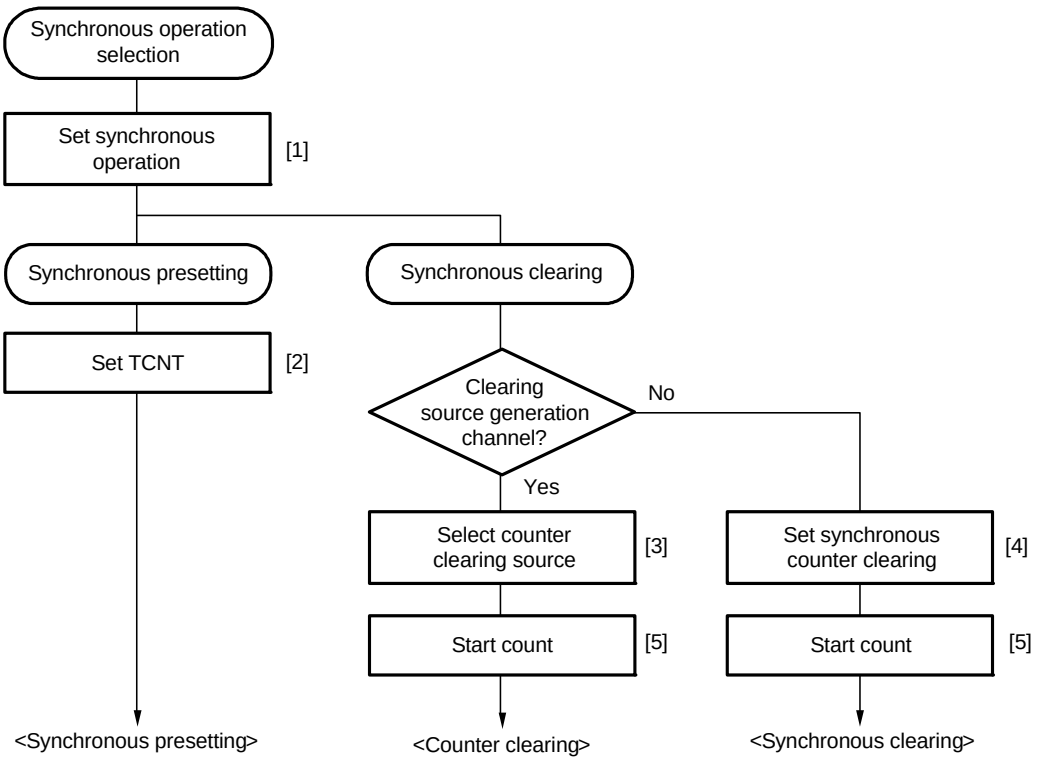
Figure 22.12 Example of Input Capture Operation

22.3.2 Synchronous Operation

In synchronous operation, the values in multiple TCNT counters can be modified simultaneously (synchronous presetting). In addition, multiple TCNT counters can be cleared simultaneously (synchronous clearing) by making the appropriate setting in TCR.
Synchronous operation increases the number of TGR registers assigned to a single time base.
MTU0 to MTU4, MTU6, and MTU7 can all be designated for synchronous operation. MTU5 cannot be used for synchronous operation.

(1) Example of Synchronous Operation Setting Procedure

Figure 22.13 shows an example of the synchronous operation setting procedure.



[1] Set to 1 the SYNC bits in TSYRj corresponding to the channels to be designated for synchronous operation (j = A or B)
[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.
[3] Use bits CCLR[2:0] in TCR to specify TCNT clearing by input capture/output compare, etc.
[4] Use bits CCLR[2:0] in TCR to designate synchronous clearing for the counter clearing source.
[5] Set to 1 the CST bits in TSTRj for the relevant channels, to start the count operation. (j = A or B)

Figure 22.13 Example of Synchronous Operation Setting Procedure

(2) Example of Synchronous Operation

Figure 22.14 shows an example of synchronous operation.
In this example, synchronous operation and PWM mode 1 have been designated for MTU0 to MTU 2, MTU0.TGRB compare match has been set as the counter clearing source in channel 0, and synchronous clearing has been set for the counter clearing source in MTU1 and MTU2.
Three-phase PWM waveforms are output from pins MTIOC0A, MTIOC1A, and MTIOC2A. At this time, synchronous presetting and synchronous clearing by MTU0.TGRB compare match are performed for the TCNT counters in MTU0 to MTU2, and the data set in MTU0.TGRB is used as the PWM cycle.
For details of PWM modes, see section 22.3.5, PWM Modes .

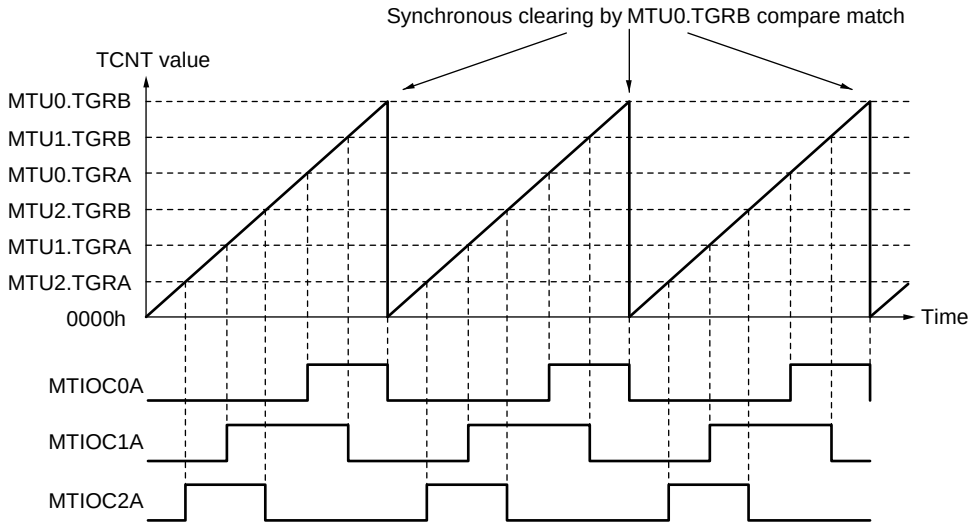


Figure 22.14 Example of Synchronous Operation

22.3.3 Buffer Operation

Buffer operation, provided for MTU0, MTU3, MTU4, MTU6, and MTU7, enables TGRC and TGRD to be used as buffer registers. In MTU0, TGRF can also be used as a buffer register.
Buffer operation differs depending on whether TGR has been designated as an input capture register or as a compare match register.

Note: • MTU0.TGRE cannot be designated as an input capture register and can only operate as a compare match register.

shows the register combinations used in buffer operation.

Table 22.57 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
MTU0	TGRA	TGRC
	TGRB	TGRD
	TGRE	TGRF
MTU3	TGRA	TGRC
	TGRB	TGRD
MTU4	TGRA	TGRC
	TGRB	TGRD
MTU6	TGRA	TGRC
	TGRB	TGRD
MTU7	TGRA	TGRC
	TGRB	TGRD

- When TGR is an output compare register

When a compare match occurs, the value in the buffer register for the corresponding channel is transferred to the timer general register.
This operation is illustrated in Figure 22.15.

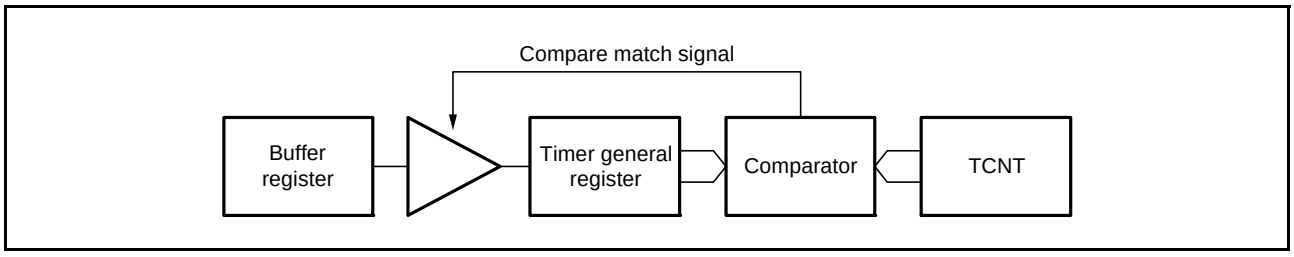


Figure 22.15 Compare Match Buffer Operation

- When TGR is an input capture register

When an input capture occurs, the value in TCNT is transferred to TGR and the value previously held in TGR is transferred to the buffer register.
This operation is illustrated in Figure 22.16.

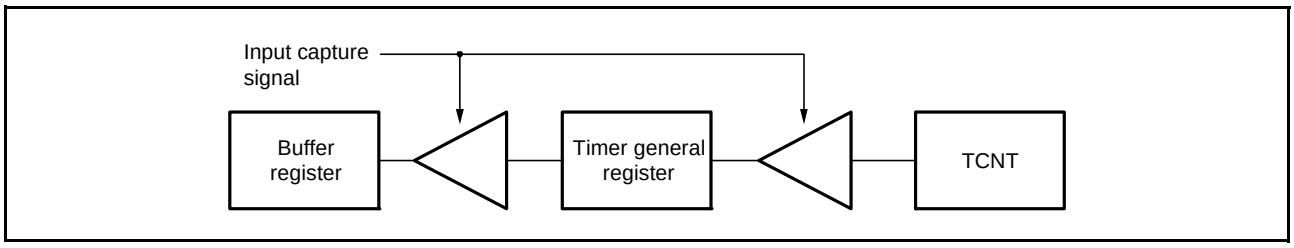


Figure 22.16 Input Capture Buffer Operation

(1) Example of Buffer Operation Setting Procedure

Figure 22.17 shows an example of the buffer operation setting procedure.

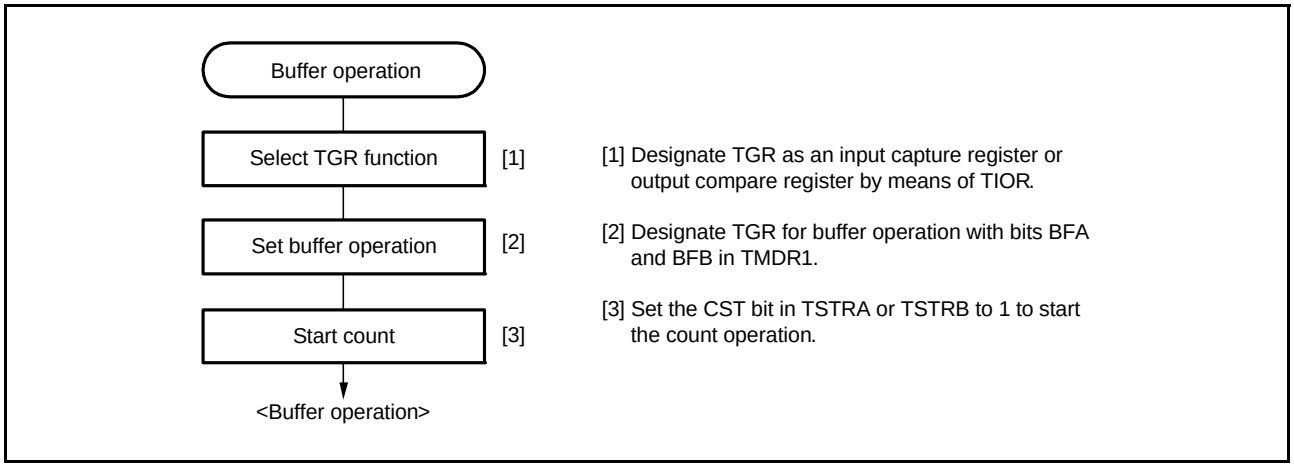


Figure 22.17 Example of Buffer Operation Setting Procedure

(2) Examples of Buffer Operation

(a) When TGR is an Output Compare Register

Figure 22.18 shows an operation example in which PWM mode 1 has been designated for MTU0, and buffer operation has been designated for TGRA and TGRC. The settings used in this example are TCNT clearing by compare match B, high output at compare match A, and low output at compare match B. In this example, the TTSA bit in TBTM is cleared to 0.

As buffer operation has been set, when compare match A occurs, the output changes and the value in buffer register TGRC is simultaneously transferred to timer general register TGRA. This operation is repeated each time compare match A occurs.

For details of PWM modes, see section 22.3.5, PWM Modes .

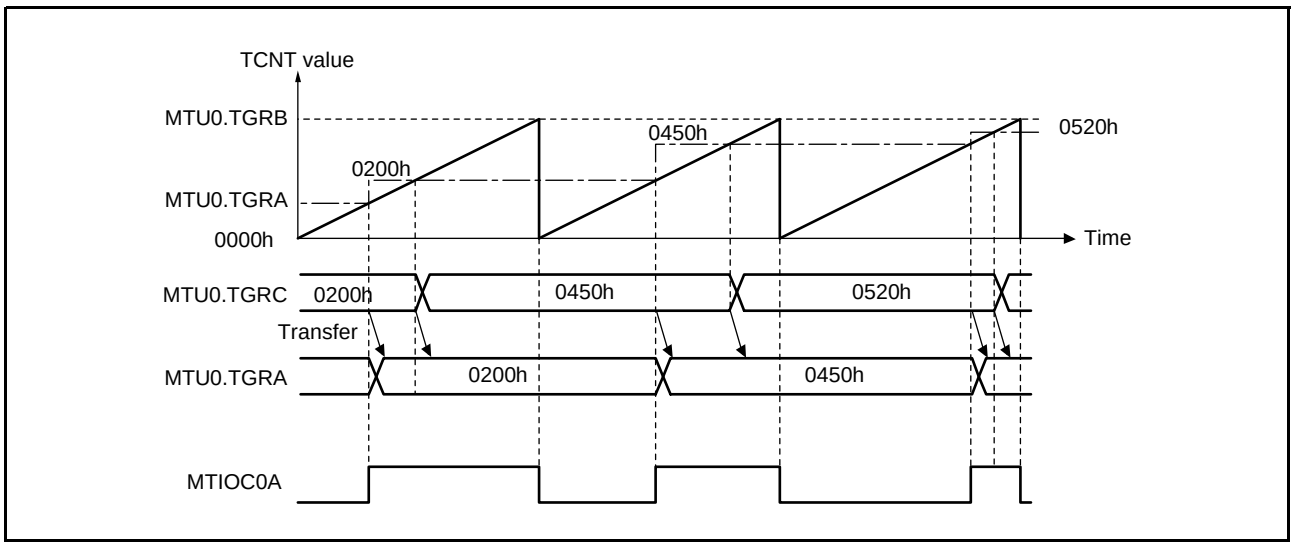


Figure 22.18 Example of Buffer Operation (1)

(b) When TGR is an Input Capture Register

Figure 22.19 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC.
Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the MTIOCnA pin input capture input edge. (n = 0 to 4, 6, 7)
As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

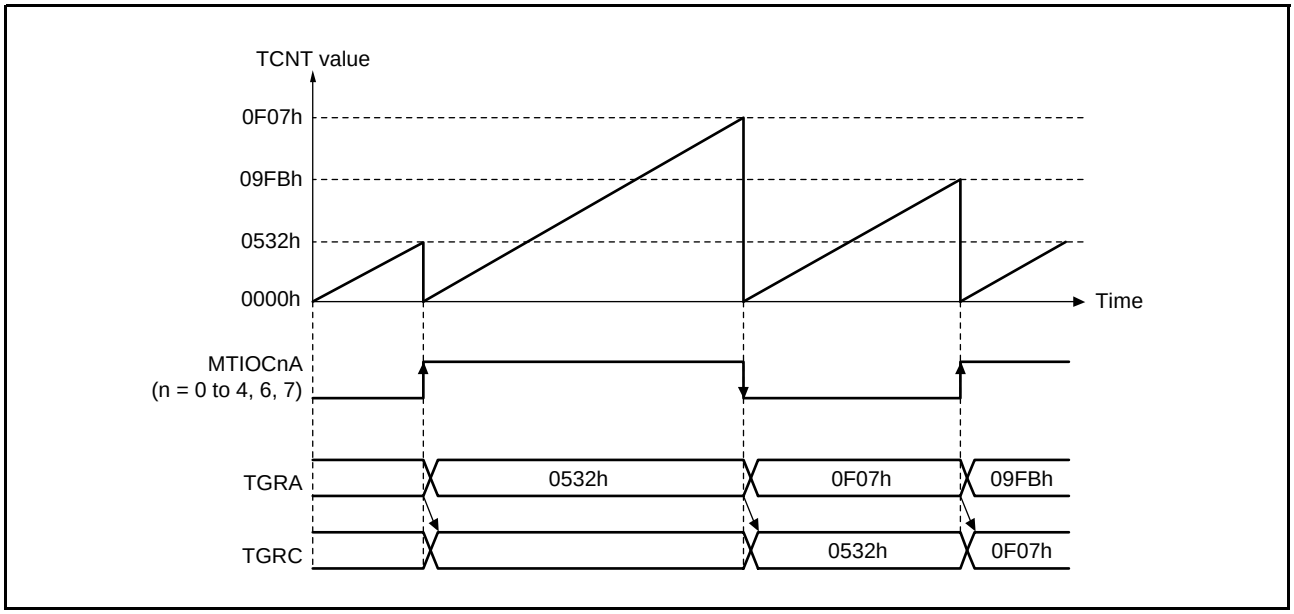


Figure 22.19 Example of Buffer Operation (2)

(3) Selecting Timing for Transfer from Buffer Registers to Timer General Registers in Buffer Operation

The timing for transfer from buffer registers to timer general registers can be selected in PWM mode 1 or 2 for MTU0 or in PWM mode 1 for MTU3, MTU4, MTU6, and MTU7 by setting the buffer operation transfer mode registers (MTUn.TBTM (n = 0, 3, 4, 6, or 7)). Either compare match (value after reset) or TCNT clearing can be selected for the transfer timing. TCNT clearing as transfer timing is one of the following cases.

- When TCNT overflows (FFFFh to 0000h)
- When 0000h is written to TCNT during counting
- When TCNT is cleared to 0000h under the condition specified in the CCLR[2:0] bits in TCR

Note: • TBTM must be modified only while TCNT stops.

Figure 22.20 shows an operation example in which PWM mode 1 is designated for MTU0 and buffer operation is designated for MTU0.TGRA and MTU0.TGRC. The settings used in this example are MTU0.TCNT clearing by compare match B, high output at compare match A, and low output at compare match B. The TTSA bit in MTU0.TBTM is set to 1.

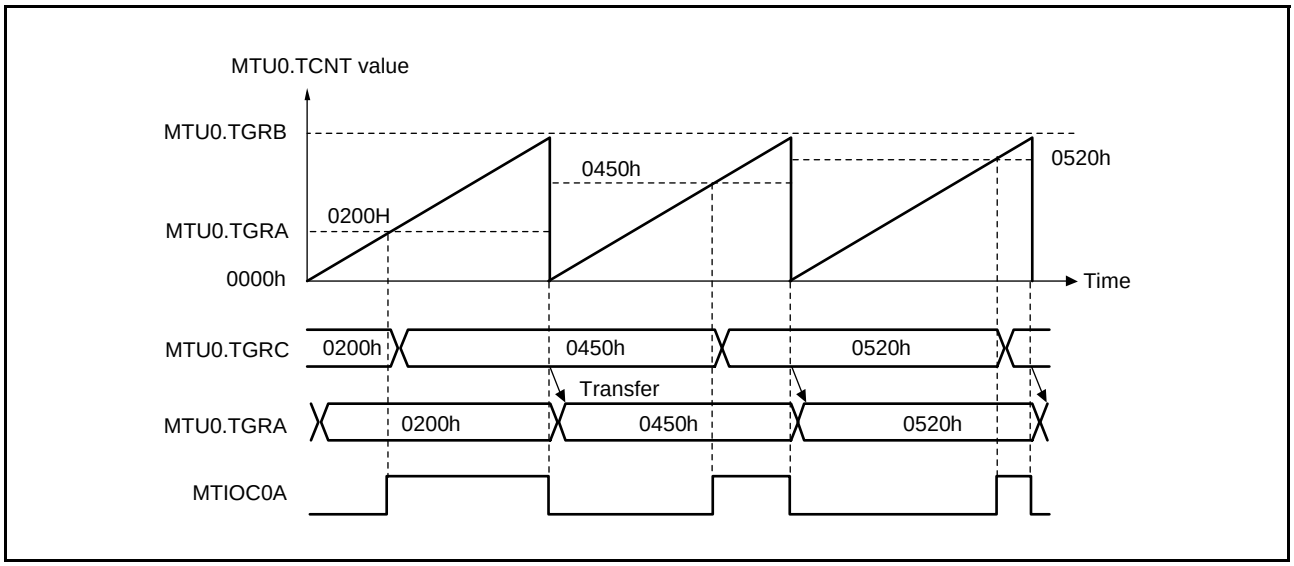


Figure 22.20 Example of Buffer Operation When MTU0.TCNT Clearing is Selected for MTU0.TGRC-to-MTU0.TGRA Transfer Timing

22.3.4 Cascaded Operation

In cascaded operation, two 16-bit counters in different channels are used together as a 32-bit counter.
This function works when overflow/underflow of MTU2.TCNT is selected as the counter clock for MTU1 through the TCR.TPSC[2:0] bits in TCR.
Underflow occurs only when the lower 16 bits of TCNT is in phase counting mode.
Table 22.58 shows the register combinations used in cascaded operation.

Note: • When phase counting mode is set for MTU1, the counter clock setting is invalid and the counters operate independently in phase counting mode.

Table 22.58 Cascaded Combinations

Combination	Upper 16 Bits	Lower 16 Bits
MTU1 and MTU2	MTU1.TCNT	MTU2.TCNT

For simultaneous input capture of MTU1.TCNT and MTU2.TCNT during cascaded operation, additional input capture input pins can be specified by the input capture control register (TICCR). The input-capture condition is of edges in the signal produced by taking the logical OR of the input level on the main input pin and the input level on the added input pin. Accordingly, if either is at the high level, a change in the level of the other will not produce an edge for detection. For details, see (4) Cascaded Operation Example (c). For input capture in cascade connection, refer to section 22.6.21, Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection.
Table 22.59 shows the TICCR setting and input capture input pins.

Table 22.59 TICCR Setting and Input Capture Input Pins

Target Input Capture	TICCR Setting	Input Capture Input Pin
Input capture from MTU1.TCNT to MTU1.TGRA	I2AE bit = 0 (initial value)	MTIOC1A
	I2AE bit = 1	MTIOC1A, MTIOC2A
Input capture from MTU1.TCNT to MTU1.TGRB	I2BE bit = 0 (initial value)	MTIOC1B
	I2BE bit = 1	MTIOC1B, MTIOC2B
Input capture from MTU2.TCNT to MTU2.TGRA	I1AE bit = 0 (initial value)	MTIOC2A
	I1AE bit = 1	MTIOC2A, MTIOC1A
Input capture from MTU2.TCNT to MTU2.TGRB	I1BE bit = 0 (initial value)	MTIOC2B
	I1BE bit = 1	MTIOC2B, MTIOC1B

(1) Example of Cascaded Operation Setting Procedure

Figure 22.21 shows an example of the cascaded operation setting procedure.

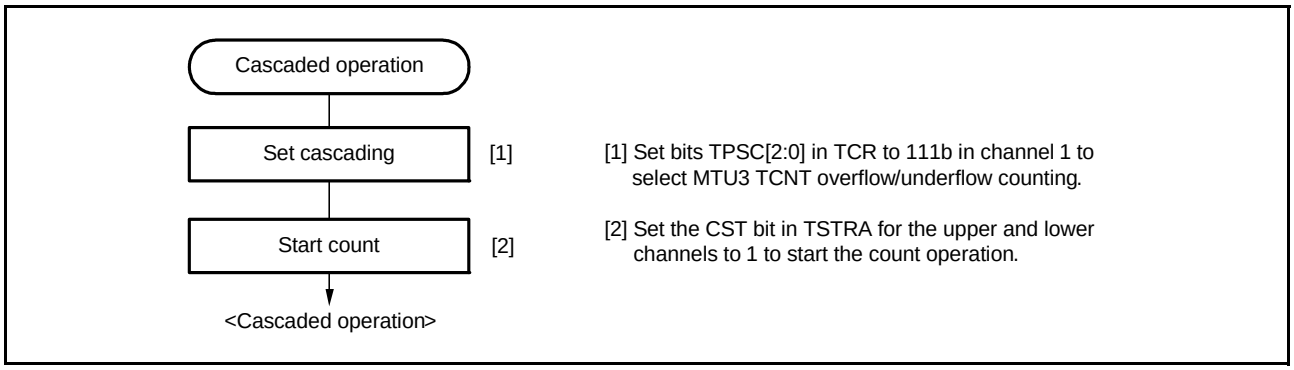


Figure 22.21 Cascaded Operation Setting Procedure

(2) Cascaded Operation Example (a)

Figure 22.22 illustrates the operation when MTU2.TCNT overflow/underflow counting has been set for MTU1.TCNT and phase counting mode has been designated for MTU2.
MTU1.TCNT is incremented by MTU2.TCNT overflow and decremented by MTU2.TCNT underflow.

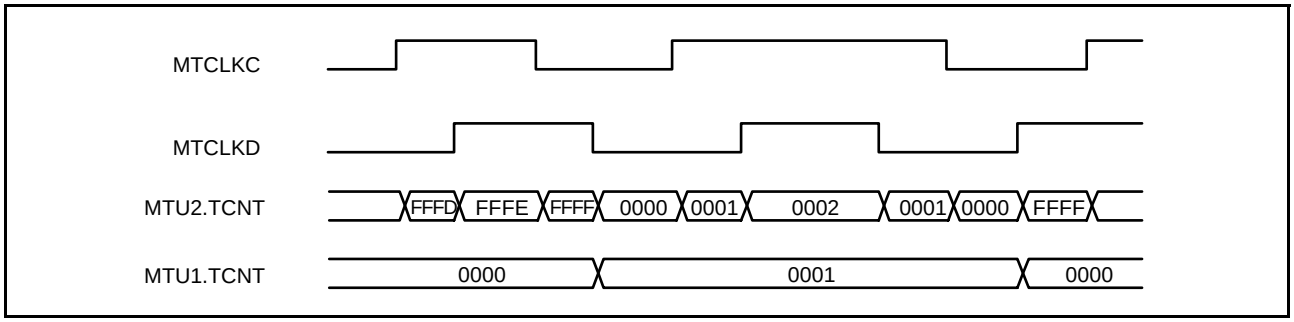


Figure 22.22 Cascaded Operation Example (a)

(3) Cascaded Operation Example (b)

Figure 22.23 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the I2AE bit in TICCR has been set to 1 to include the MTIOC2A pin in the MTU1.TGRA input capture conditions. In this example, the MTU1.TIOR.IOA[3:0] bits have selected the MTIOC1A rising edge for the input capture timing while the MTU2.TIOR.IOA[3:0] bits have selected the MTIOC2A rising edge for the input capture timing.
Under these conditions, the rising edge of both MTIOC1A and MTIOC2A is used for the MTU1.TGRA input capture condition. For the MTU2.TGRA input capture condition, the MTIOC2A rising edge is used.

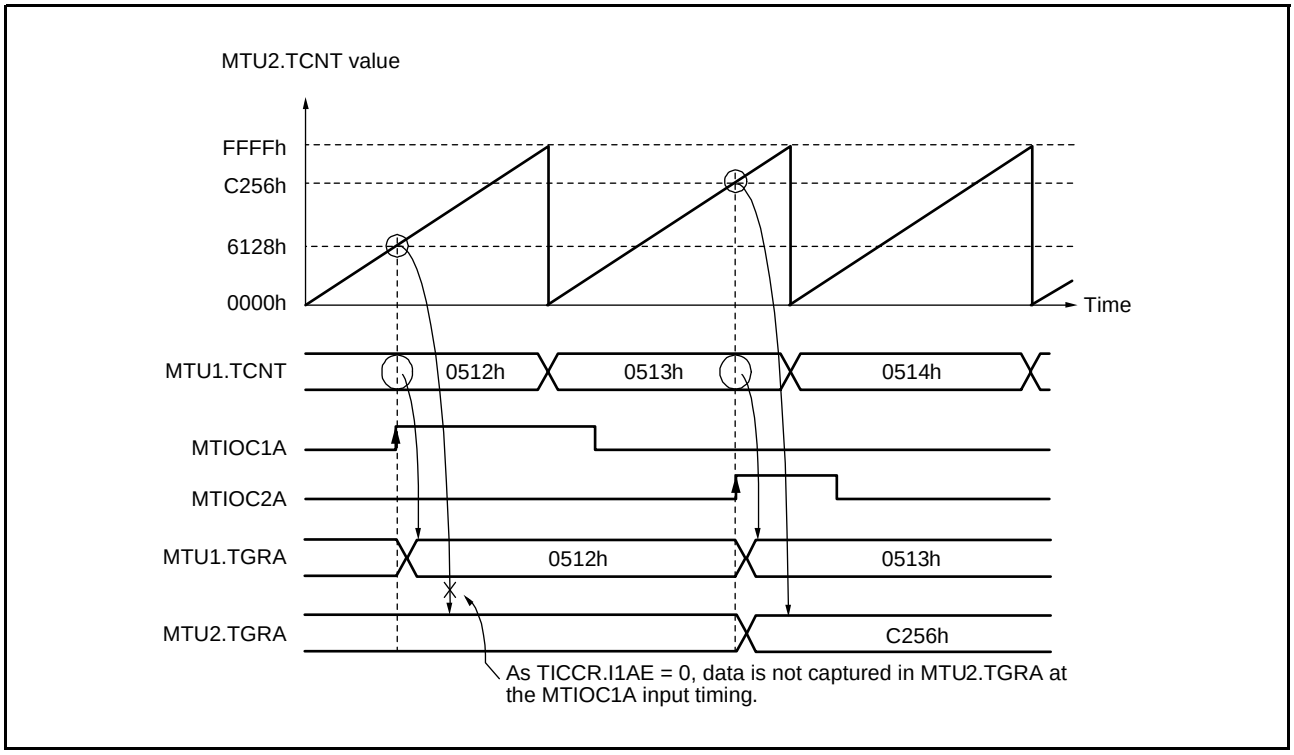


Figure 22.23 Cascaded Operation Example (b)

(4) Cascaded Operation Example (c)

Figure 22.24 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the TICCR.I2AE and I1AE bits have been set to 1 to include the MTIOC2A and MTIOC1A pins in the MTU1.TGRA and MTU2.TGRA input capture conditions, respectively. In this example, the IOA[3:0] bits in both MTU1.TIOR and MTU2.TIOR have selected both the rising and falling edges for the input capture timing. Under these conditions, the ORed result of MTIOC1A and MTIOC2A input is used for the MTU1.TGRA and MTU2.TGRA input capture conditions.

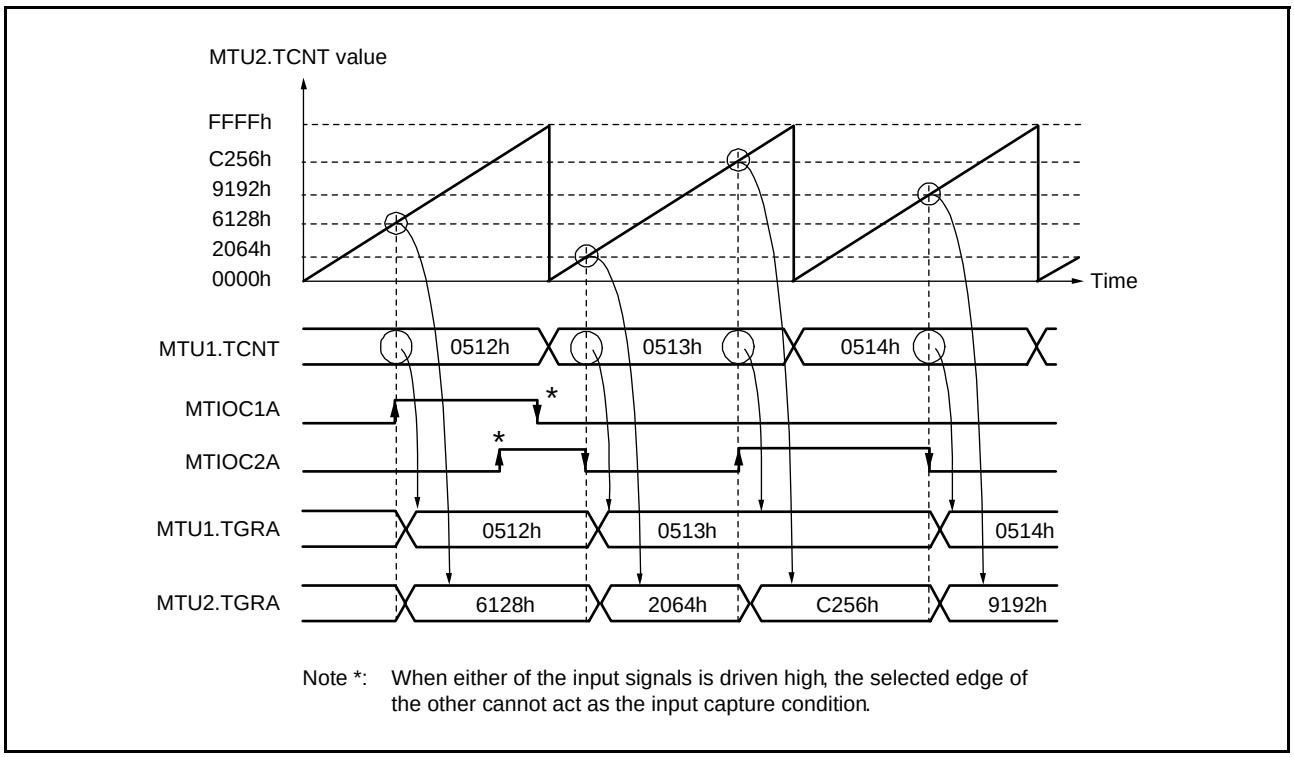


Figure 22.24 Cascaded Operation Example (c)

(5) Cascaded Operation Example (d)

Figure 22.25 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the TICCR.I2AE bit has been set to 1 to include the MTIOC2A pin in the MTU1.TGRA input capture conditions. In this example, the IOA[3:0] bits in MTU1.TIOR have selected occurrence of MTU0.TGRA compare match or input capture for the input capture timing while the IOA[3:0] bits in MTU2.TIOR have selected the MTIOC2A rising edge for the input capture timing.

Under these conditions, as MTU1.TIOR has selected occurrence of MTU0.TGRA compare match or input capture for the input capture timing, the MTIOC2A edge is not used for MTU1.TGRA input capture condition although the I2AE bit in TICCR has been set to 1.

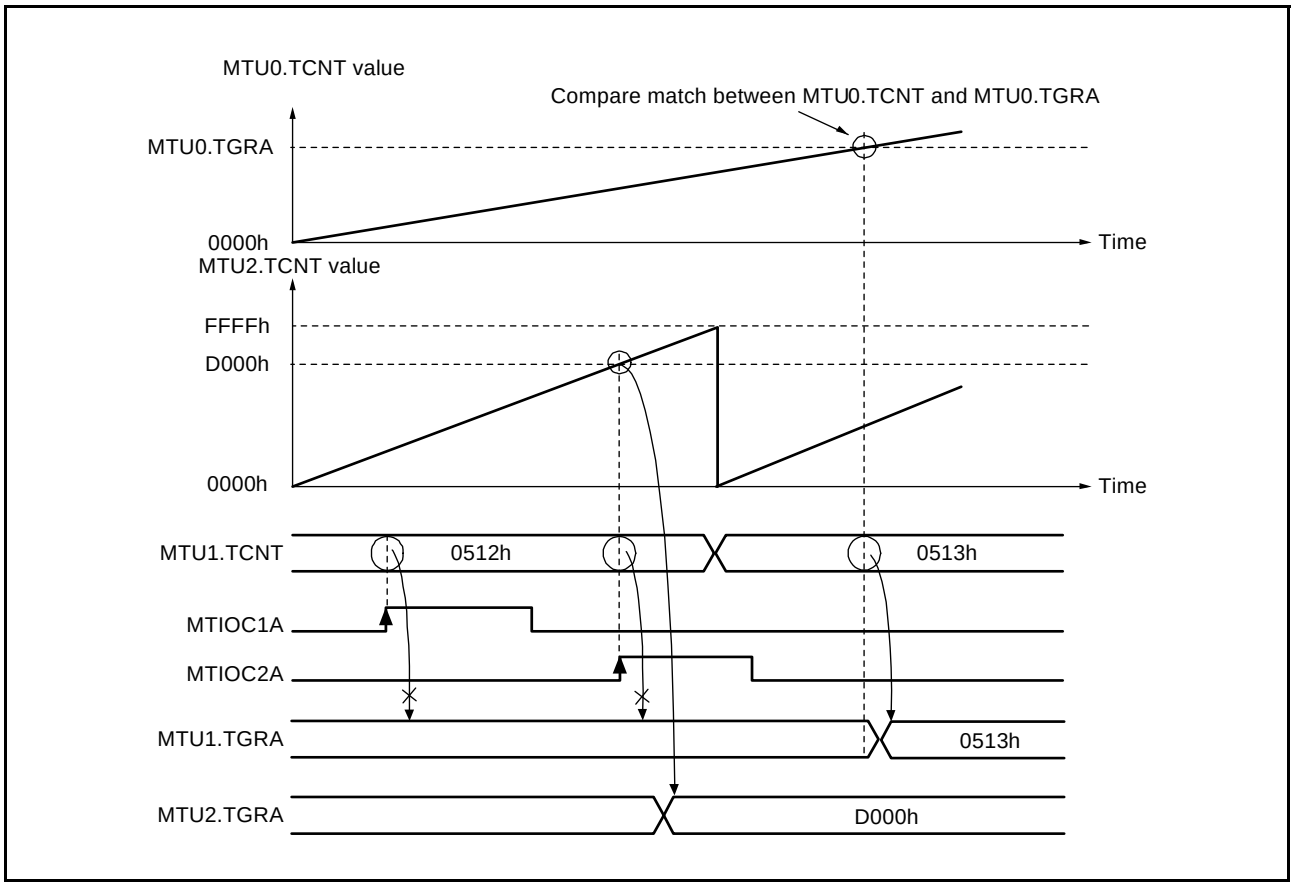


Figure 22.25 Cascaded Operation Example (d)

22.3.5 PWM Modes

PWM modes are provided to output PWM waveforms from the external pins. The output level can be selected as low, high, or toggle output in response to a compare match of each TGR.
PWM waveforms in the range of 0% to 100% duty cycle can be output according to the TGR settings.
By designating TGR compare match as the counter clearing source, the PWM cycle can be specified in that register.
Every channel can be set to PWM mode independently. Channels set to PWM mode can perform synchronous operation with each other or other channels set to any other mode.
There are two PWM modes as described below.

(a) PWM Mode 1

PWM waveforms are output from the MTIOCA and MTIOCC pins by pairing TGRA with TGRB and TGRC with TGRD. The levels specified by the TIOR.IOA[3:0] and IOC[3:0] bits are output from the MTIOCnA and MTIOCnC pins at compare matches A and C, and the level specified by the TIOR.IOB[3:0] and IOD[3:0] bits are output at compare matches B and D (n = 0 to 4, 6, 7). The initial output value is set in TGRA or TGRC. If the values set in paired TGRs are identical, the output value does not change even when a compare match occurs.
In PWM mode 1, up to 12 phases of PWM waveforms can be output.

Note: • In the 64- and 48-pin products, each pair of MTIOC3A and MTIOC6A, MTIOC3C and MTIOC6C, and MTIOC4A and MTIOC7A, MTIOC4C and MTIOC7C shares the same pin; one of each pair can be selected and used by the MPC.

(b) PWM Mode 2

PWM waveform output is generated using one TGR as the cycle register and the others as duty registers. The level specified in TIOR is output at compare matches. Upon counter clearing by a cycle register compare match, the initial value set in TIOR is output from each pin. If the values set in the cycle and duty registers are identical, the output value does not change even when a compare match occurs.

In PWM mode 2, up to eight phases of PWM waveforms can be output when using synchronous operation in combination.

The correspondence between PWM output pins and registers is shown in Table 22.60.

Table 22.60 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Register**	**PWM Mode 1**	**PWM Mode 2**
MTU0	TGRA	MTIOC0A	MTIOC0A
	TGRB		MTIOC0B
	TGRC	MTIOC0C	MTIOC0C
	TGRD		MTIOC0D
MTU1	TGRA	MTIOC1A	MTIOC1A
	TGRB		MTIOC1B
MTU2	TGRA	MTIOC2A	MTIOC2A
	TGRB		MTIOC2B
MTU3	TGRA	MTIOC3A	Setting prohibited
	TGRB		
	TGRC	MTIOC3C	
	TGRD		
MTU4	TGRA	MTIOC4A	
	TGRB		
	TGRC	MTIOC4C	
	TGRD		
MTU6	TGRA	MTIOC6A	
	TGRB		
	TGRC	MTIOC6C	
	TGRD		
MTU7	TGRA	MTIOC7A	
	TGRB		
	TGRC	MTIOC7C	
	TGRD		

Note 1. In PWM mode 2, PWM waveform output is not possible for the TGR register in which the PWM cycle is set.

(1) Example of PWM Mode Setting Procedure

Figure 22.26 shows an example of the PWM mode setting procedure.

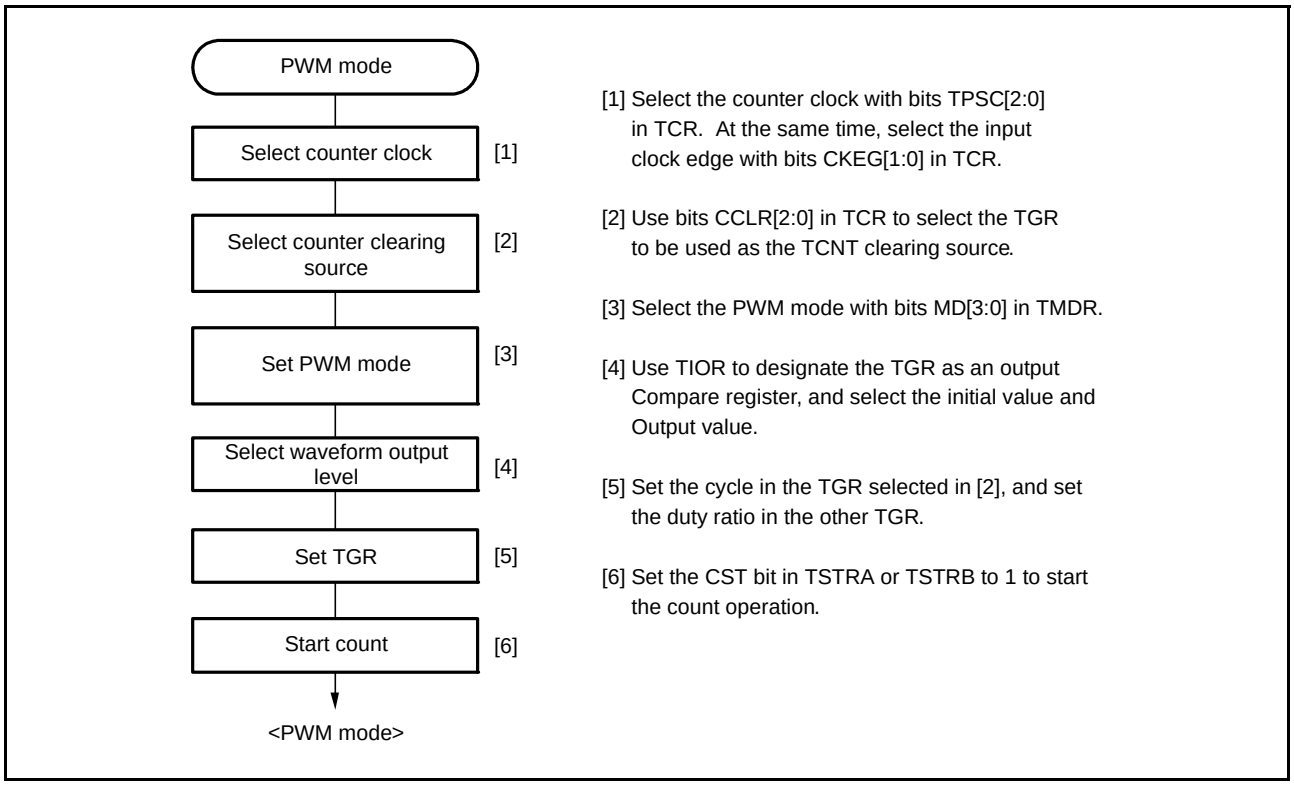


Figure 22.26 Example of PWM Mode Setting Procedure

(2) Examples of PWM Mode Operation

Figure 22.27 shows an example of operation in PWM mode 1.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set as the initial output value and output value for TGRA, and 1 is set as the output value for TGRB.

In this case, the value set in TGRA is used as the cycle, and the value set in TGRB is used as the duty ratio.

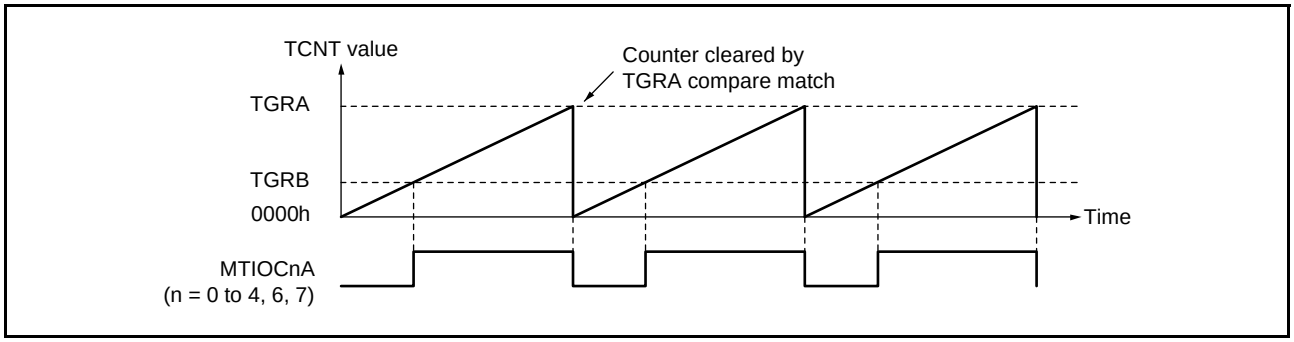


Figure 22.27 Example of PWM Mode 1 Operation

Figure 22.28 shows an example of operation in PWM mode 2.
In this example, synchronous operation is designated for MTU0 and MTU1, MTU1.TGRB compare match is set as the TCNT clearing source, and Low is set as the initial output value and High as the output value for the other TGR registers (MTU0.TGRA to MTU0.TGRD and MTU1.TGRA), outputting 5-phase PWM waveforms.
In this case, the value set in MTU1.TGRB is used as the cycle, and the values set in the other TGRs are used as the duty ratio.

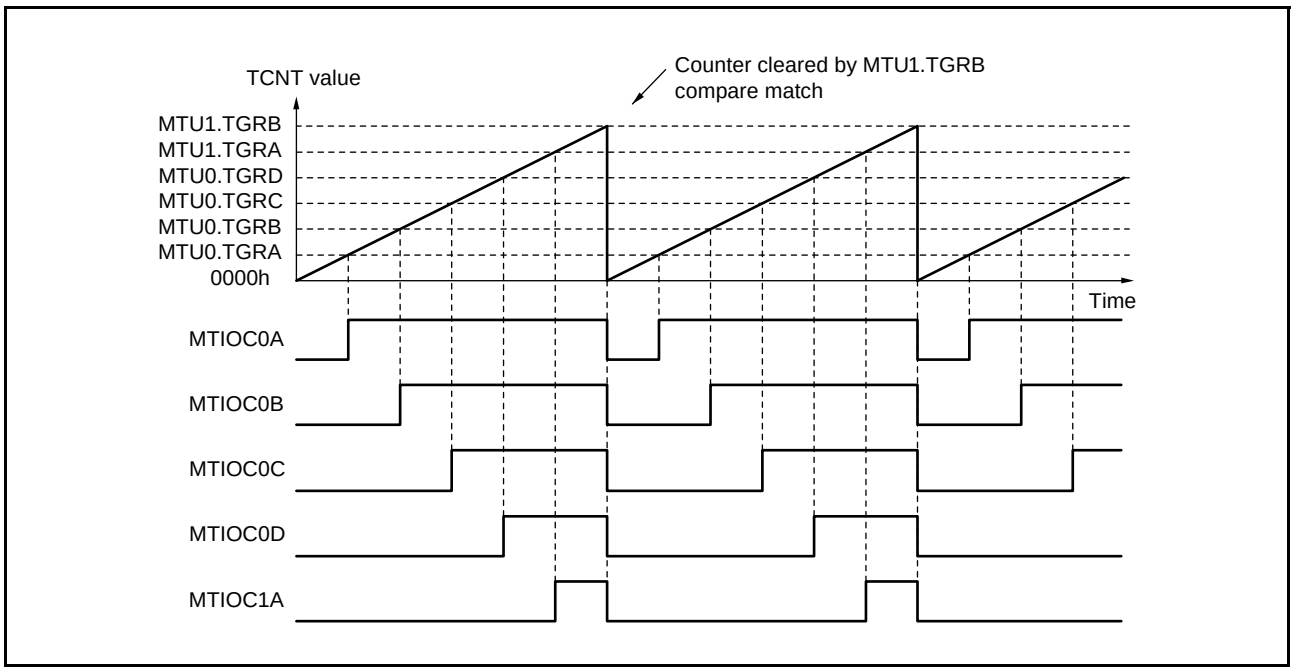


Figure 22.28 Example of PWM Mode 2 Operation

Figure 22.29 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

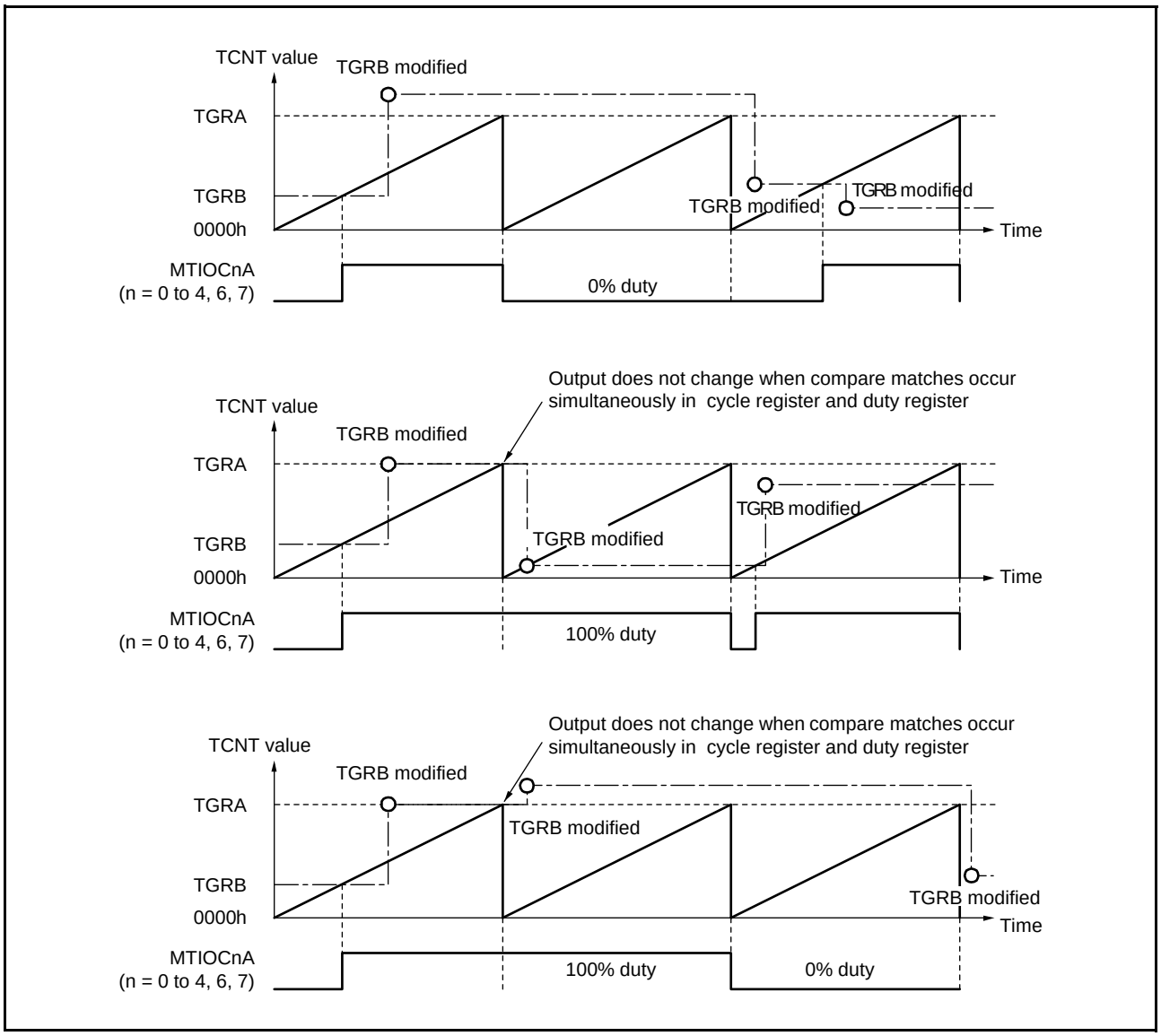


Figure 22.29 Examples of PWM Mode Operation (PWM Waveform Output with 0% Duty and 100% Duty)

22.3.6 Phase Counting Mode

In phase counting mode, the phase difference between two external input clocks is detected and TCNT is incremented or decremented accordingly. This mode can be set for MTU1 and MTU2.

When phase counting mode is specified, an external clock is selected as the counter input clock and TCNT operates as an up/down-counter regardless of the setting of bits TPSC[2:0] and bits CKEG[1:0] in TCR. However, the functions of bits CCLR[1:0] in TCR and of TIOR, TIER, and TGR are valid, and input capture/compare match and interrupt functions can be used.

This can be used for two-phase encoder pulse input.

If an overflow occurs while TCNT is counting up, the TCFV flag in TSR is set to 1. If an underflow occurs while TCNT is counting down, the TCFU flag is TSR is set to 1.

The TCFD flag in TSR is the count direction flag. Read the TCFD flag to check whether TCNT is counting up or down.

Table 22.61 shows the correspondence between external clock pins and channels.

Table 22.61 Clock Input Pins in Phase Counting Mode

	External Clock Input Pins	
Channel	**A-Phase**	**B-Phase**
When MTU1 is set to phase counting mode	MTCLKA	MTCLKB
When MTU2 is set to phase counting mode	MTCLKC	MTCLKD

(1) Example of Phase Counting Mode Setting Procedure

Figure 22.30 shows an example of the phase counting mode setting procedure.

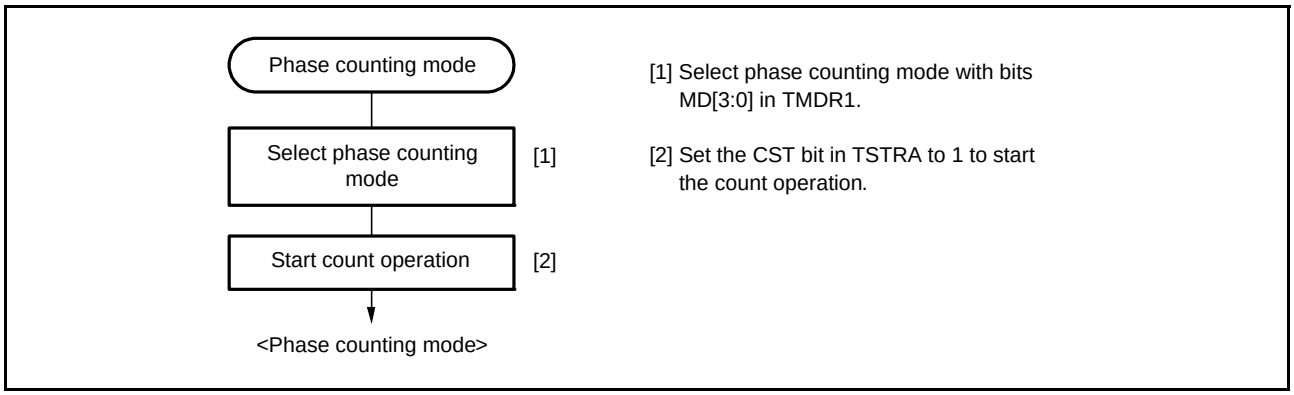


Figure 22.30 Example of Phase Counting Mode Setting Procedure

(2) Examples of Phase Counting Mode Operation

In phase counting mode, TCNT is incremented or decremented according to the phase difference between two external clocks. There are four modes according to the count conditions.

(a) Phase Counting Mode 1

Figure 22.31 shows an example of operation in phase counting mode 1, and Table 22.62 summarizes the TCNT up-/down-count conditions.

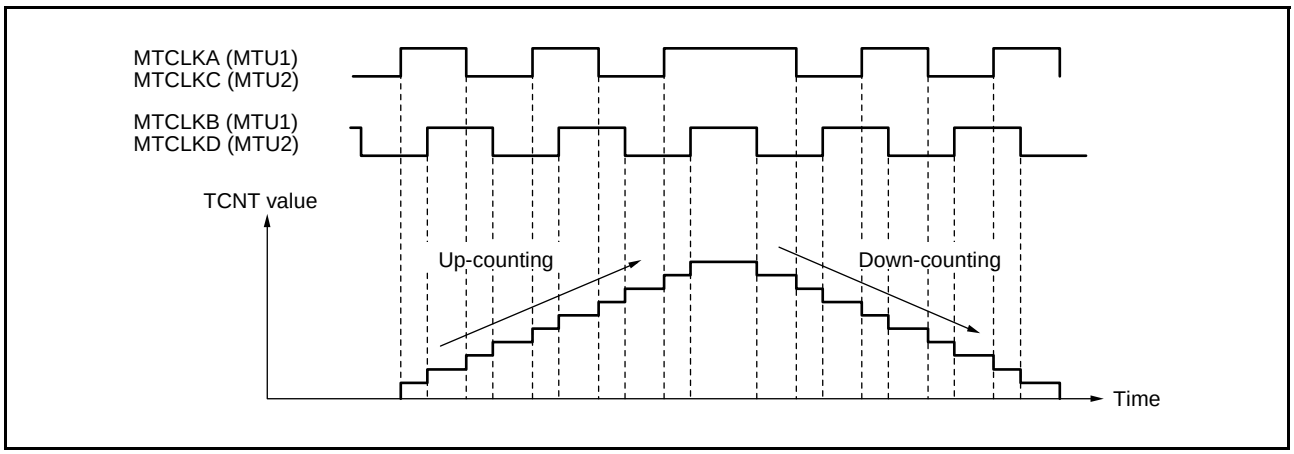


Figure 22.31 Example of Operation in Phase Counting Mode 1

Table 22.62 Up-/Down-Count Conditions in Phase Counting Mode 1

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Up-counting
Low	↓	
↑	Low	
↓	High	
High	↓	Down-counting
Low	↑	
↑	High	
↓	Low	

↑ : Rising edge

↓ : Falling edge

(b) Phase Counting Mode 2

Figure 22.32 shows an example of operation in phase counting mode 2, and Table 22.63 summarizes the TCNT up-/down-count conditions.

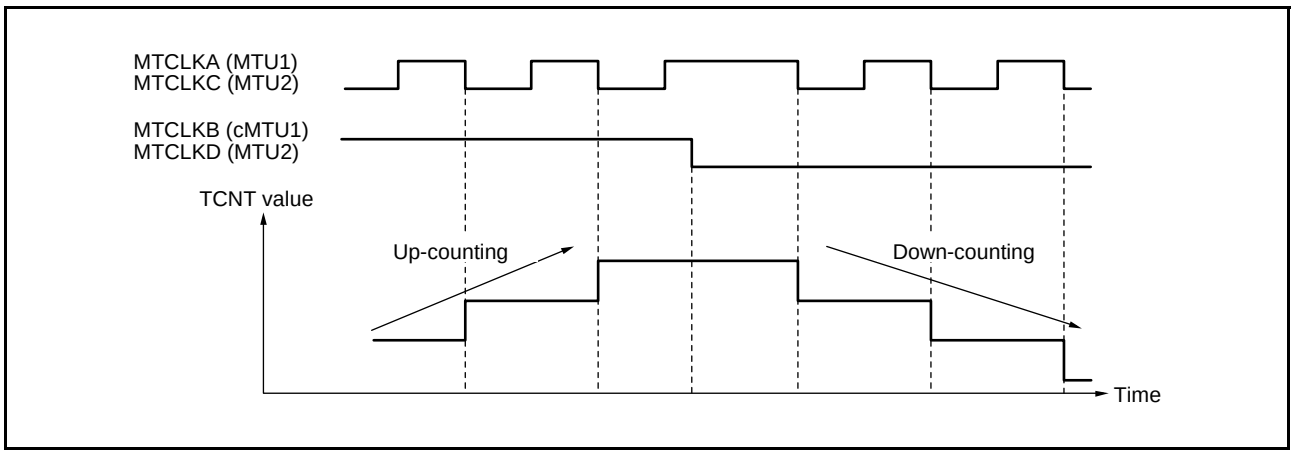


Figure 22.32 Example of Operation in Phase Counting Mode 2

Table 22.63 Up-/Down-Count Conditions in Phase Counting Mode 2

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Not counted (Don't care)
Low	↓	
↑	Low	
↓	High	Up-counting
High	↓	Not counted (Don't care)
Low	↑	
↑	High	
↓	Low	Down-counting

↑ : Rising edge

↓ : Falling edge

(c) Phase Counting Mode 3

Table 22.32 shows an example of operation in phase counting mode 3, and Table 22.64 summarizes the TCNT up-/down-count conditions.

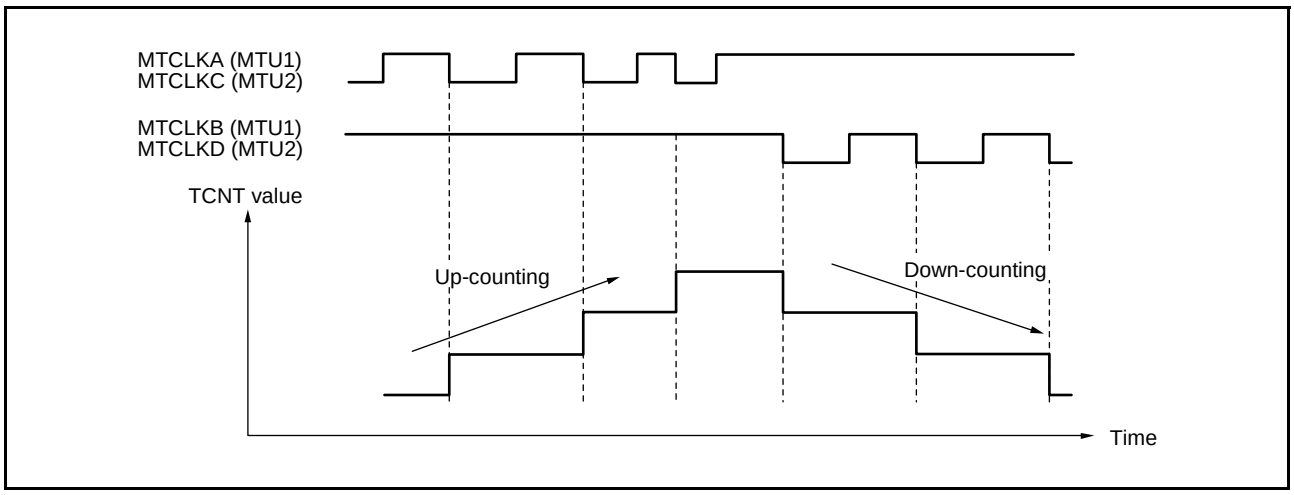


Figure 22.33 Example of Operation in Phase Counting Mode 3

Table 22.64 Up-/Down-Count Conditions in Phase Counting Mode 3

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Not counted (Don't care)
Low	↓	
↑	Low	
↓	High	Up-counting
High	↓	Down-counting
Low	↑	Not counted (Don't care)
↑	High	
↓	Low	

↑ : Rising edge

↓ : Falling edge

(d) Phase Counting Mode 4

Table 22.33 shows an example of operation in phase counting mode 4, and Table 22.65 summarizes the TCNT up-/down-count conditions.

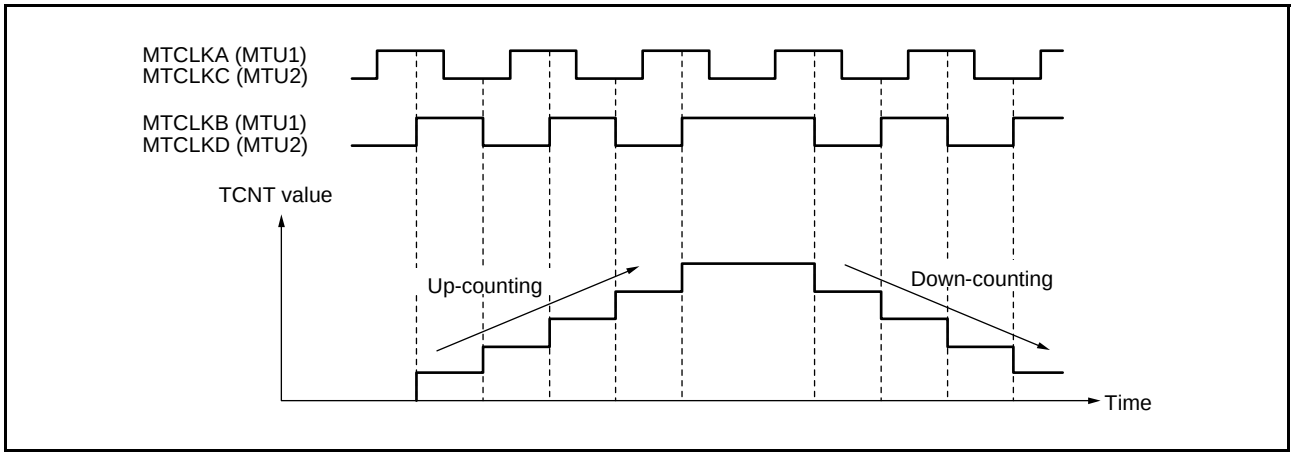


Figure 22.34 Example of Operation in Phase Counting Mode 4

Table 22.65 Up-/Down-Count Conditions in Phase Counting Mode 4

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Up-counting
Low	↓	
↑	Low	Not counted (Don't care)
↓	High	
High	↓	Down-counting
Low	↑	
↑	High	Not counted (Don't care)
↓	Low	

↑ : Rising edge

↓ : Falling edge

(3) Phase Counting Mode Application Example

Table 22.34 shows an example in which MTU1 is in phase counting mode, and MTU1 is coupled with MTU0 to input 2-phase encoder pulses of a servo motor in order to detect position or speed.

MTU1 is set to phase counting mode 1, and the encoder pulse A-phase and B-phase are input to MTCLKA and MTCLKB.

In MTU0, MTU0.TGRC compare match is specified as the TCNT clearing source and MTU0.TGRA and MTU0.TGRC are used for the compare match function and are set with the speed control cycle and position control cycle.

MTU0.TGRB is used for input capture, with MTU0.TGRB and MTU0.TGRD operating in buffer mode. The MTU1 counter input clock is designated as the MTU0.TGRB input capture source, and the widths of 2-phase encoder 4-multiplication pulses are detected.

MTU1.TGRA and MTU1.TGRB for MTU1 are designated for the input capture function and MTU0.TGRA and MTU0.TGRC compare matches in MTU0 are selected as the input capture sources to store the up/down-counter values for the control cycles.

This procedure enables the accurate detection of position and speed.

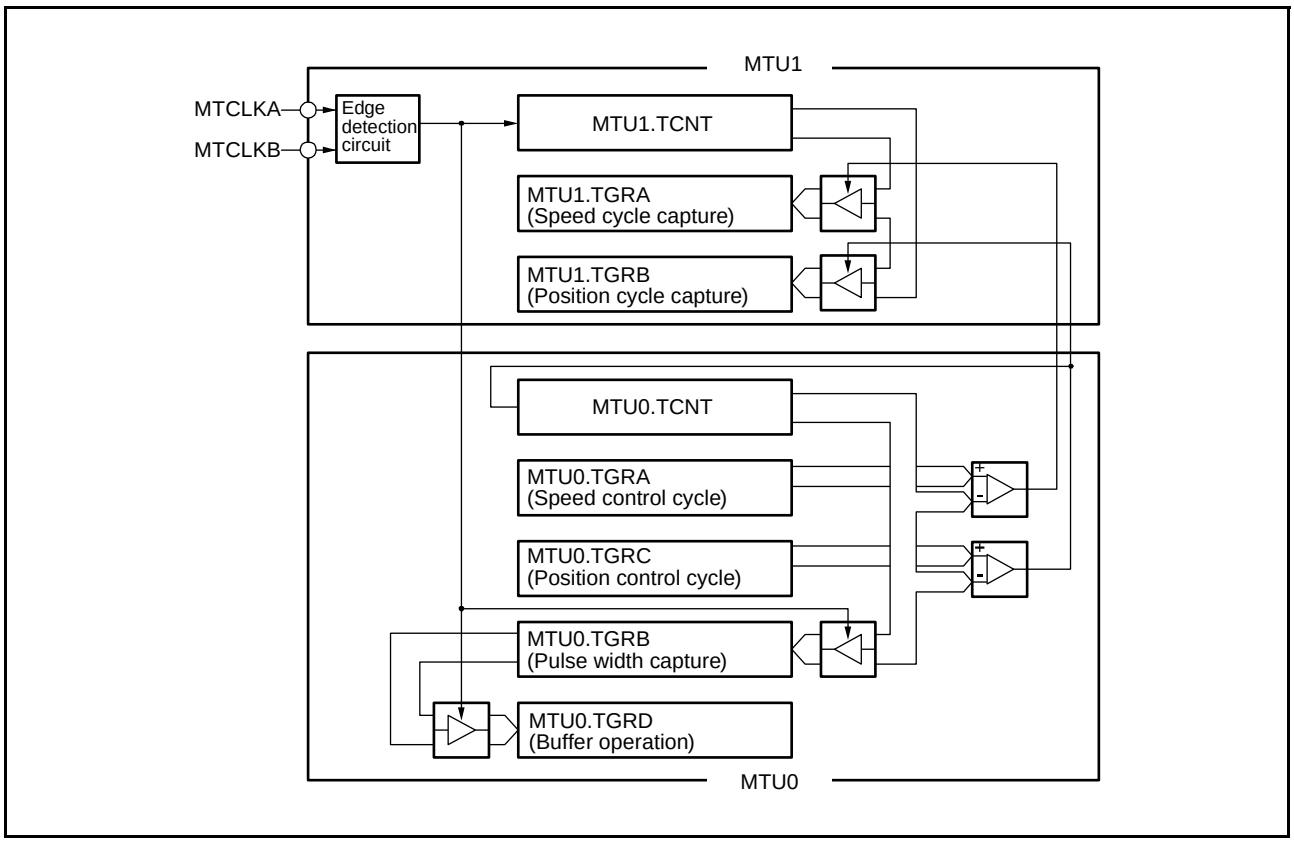


Figure 22.35 Phase Counting Mode Application Example

22.3.7 Reset-Synchronized PWM Mode

In the reset-synchronized PWM mode, three phases of positive and negative PWM waveforms (six phases in total) that share a common wave transition point can be output by combining MTU3 and MTU4 and MTU6 and MTU7.
When set for reset-synchronized PWM mode, the MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D pins function as PWM output pins and timer counters 3 and 6 (MTU3.TCNT and MTU6.TCNT) functions as an up-counter.
Table 22.66 shows the PWM output pins used. Table 22.67 shows the settings of the registers.

Table 22.66 Output Pins for Reset-Synchronized PWM Mode

Channel	Output Pin	Description
MTU3	MTIOC3B	PWM output pin 1
	MTIOC3D	PWM output pin 1' (negative-phase waveform of PWM output 1)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2' (negative-phase waveform of PWM output 2)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3' (negative-phase waveform of PWM output 3)
MTU6	MTIOC6B	PWM output pin 4
	MTIOC6D	PWM output pin 4' (negative-phase waveform of PWM output 4)
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5' (negative-phase waveform of PWM output 5)
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6' (negative-phase waveform of PWM output 6)

Table 22.67 Register Settings for Reset-Synchronized PWM Mode

Register	Setting
MTU3.TCNT	Initial setting (0000h)
MTU4.TCNT	Initial setting (0000h)
MTU3.TGRA	Set the count cycle for MTU3.TCNT
MTU3.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC3B and MTIOC3D pins
MTU4.TGRA	Set the transition point of the PWM waveform to be output from the MTIOC4A and MTIOC4C pins
MTU4.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC4B and MTIOC4D pins
MTU6.TCNT	Initial setting (0000h)
MTU7.TCNT	Initial setting (0000h)
MTU6.TGRA	Set the count cycle for MTU6.TCNT
MTU6.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC6B and MTIOC6D pins
MTU7.TGRA	Set the transition point of the PWM waveform to be output from the MTIOC7A and MTIOC7C pins
MTU7.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC7B and MTIOC7D pins

(1) Example of Procedure for Setting Reset-Synchronized PWM Mode

Figure 22.36 shows an example of procedure for setting the reset-synchronized PWM mode.

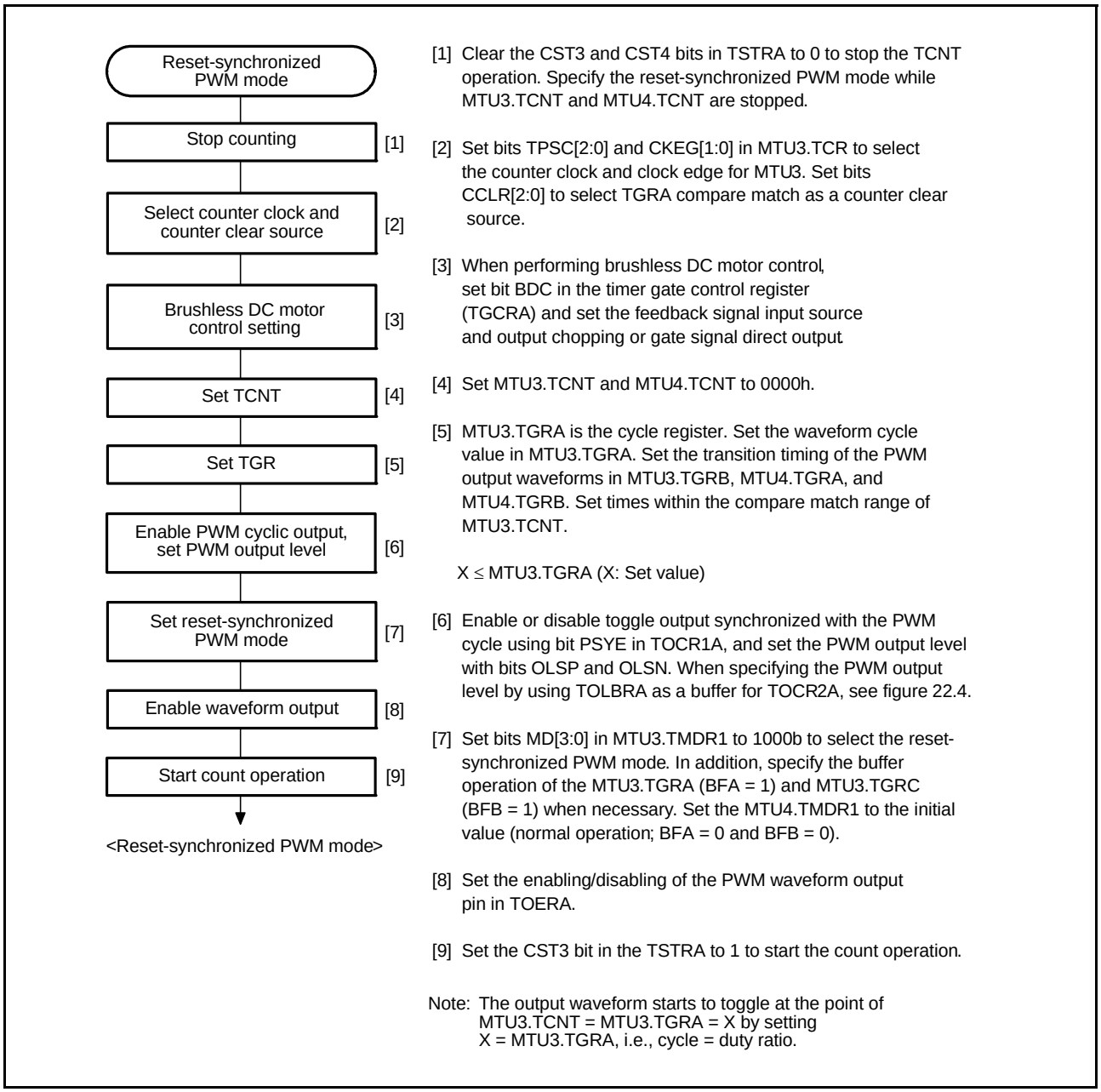


Figure 22.36 Procedure for Selecting Reset-Synchronized PWM Mode

(2) Example of Reset-Synchronized PWM Mode Operation

Figure 22.37 shows an example of operation in the reset-synchronized PWM mode.
MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) operate as up-counters. The counters are cleared when a compare match occurs between MTU3.TCNT (MTU6.TCNT) and MTU3.TGRA (MTU6.TGRA), and then begin incrementing from 0000h. The output from the PWM pins toggles every time a compare match occurs in MTU3.TGRB (MTU6.TGRB), MTU4.TGRA (MTU7.TGRA), and MTU4.TGRB (MTU7.TGRB) and the counters are cleared.

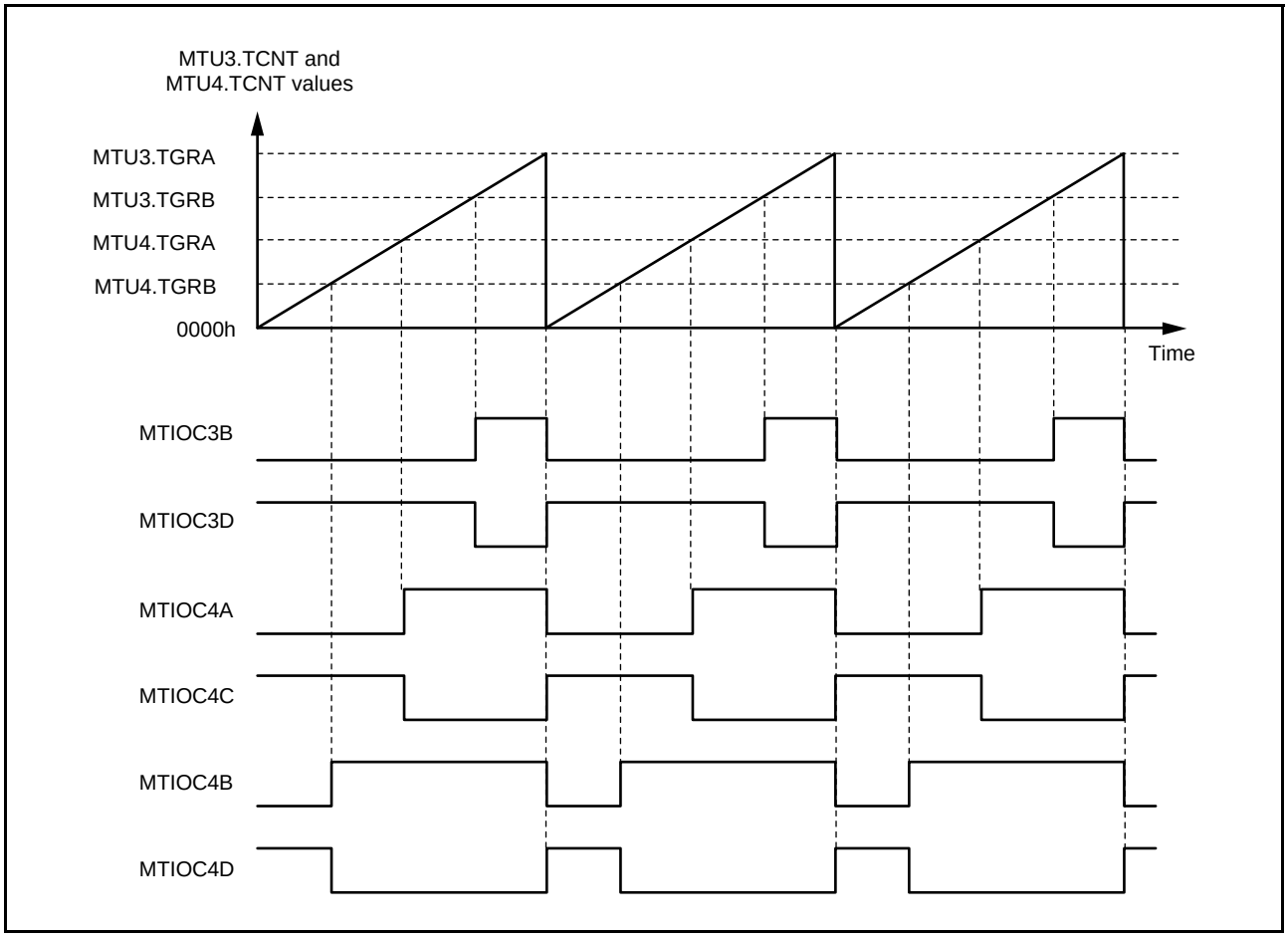


Figure 22.37 Example of Reset-Synchronized PWM Mode Operation (When TOCR1A's OLSN = 1 and OLSP = 1 in MTU3 and MTU4)

22.3.8 Complementary PWM Mode

In complementary PWM mode, dead time can be set in the PWM waveform to be output. Dead time is a period during which both upper and lower arm transistors are set to inactive level in order to prevent arm short-circuit.
By combining MTU3 and MTU4, three phases (six phases in total) of PWM waveforms can be output. Output of a waveform without dead time is also possible.
In complementary PWM mode, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D pins function as PWM output pins, and the MTIOC3A and MTIOC6A pins can be set for toggle output synchronized with the PWM cycle.
MTU3.TCNT, MTU4.TCNT, MTU6.TCNT, and MTU7.TCNT function as up/down-counters.
Table 22.67 shows the PWM output pins used. Table 22.69 shows the settings of the registers used.
A function to directly cut off the PWM output by using an external signal is supported as a port function.

Table 22.68 Output Pins for Complementary PWM Mode

Channel	Output Pin	Description
MTU3	MTIOC3A	Toggle output synchronized with PWM cycle (or I/O port)
	MTIOC3B	PWM output pin 1
	MTIOC3C	I/O port*1
	MTIOC3D	PWM output pin 1' (negative phase waveform of PWM output 1)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2' (negative phase waveform of PWM output 2)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3' (negative phase waveform of PWM output 3)
MTU6	MTIOC6A	Toggle output synchronized with PWM cycle (or I/O port)
	MTIOC6B	PWM output pin 4
	MTIOC6C	I/O port*1
	MTIOC6D	PWM output pin 4' (non-overlapping negative-phase waveform of PWM output 4; PWM output without non-overlapping interval is also available)
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5' (non-overlapping negative-phase waveform of PWM output 5; PWM output without non-overlapping interval is also available)
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6' (non-overlapping negative-phase waveform of PWM output 6; PWM output without non-overlapping interval is also available)

Note 1. Avoid setting the MTIOC3C and MTIOC6C pins as timer I/O pins in complementary PWM mode.

Table 22.69 Register Settings for Complementary PWM Mode

Channel	Counter/ Register	Description	Read/Write from CPU
MTU3	TCNT	Starts up-counting from the value set in the dead time register	Maskable by TRWERA setting *1
	TGRA	Set MTU3.TCNT upper limit value (1/2 carrier cycle + dead time)	Maskable by TRWERA setting *1
	TGRB	PWM output 1 compare register	Maskable by TRWERA setting*1
	TGRC	MTU3.TGRA buffer register	Always readable/writable
	TGRD	PWM output 1/MTU3.TGRB buffer register	Always readable/writable
	TGRE	MTU3.TGRB buffer register B (when double buffer function is used)	Always readable/writable
MTU4	TCNT	Starts up-counting after being initialized to 0000h	Maskable by TRWERA setting*1
	TGRA	PWM output 2 compare register	Maskable by TRWERA setting*1
	TGRB	PWM output 3 compare register	Maskable by TRWERA setting*1
	TGRC	PWM output 2/MTU4.TGRA buffer register	Always readable/writable
	TGRD	PWM output 3/MTU4.TGRB buffer register	Always readable/writable
	TGRE	MTU4.TGRA buffer register B (when double buffer function is used)	Always readable/writable
	TGRF	MTU4.TGRB buffer register B (when double buffer function is used)	Always readable/writable
MTU6	TCNT	Starts up-counting from the value set in the dead time register	Maskable by TRWERB setting*2
	TGRA	Set MTU6.TCNT upper limit value (1/2 carrier cycle + dead time)	Maskable by TRWERB setting *2
	TGRB	PWM output 4 compare register	Maskable by TRWERB setting*2
	TGRC	MTU6.TGRA buffer register	Always readable/writable
	TGRD	PWM output 4/MTU6.TGRB buffer register	Always readable/writable
	TGRE	MTU6.TGRB buffer register B (when double buffer function is used)	Always readable/writable
MTU7	TCNT	Starts up-counting after being initialized to 0000h	Maskable by TRWERB setting*2
	TGRA	PWM output 5 compare register	Maskable by TRWERB setting*2
	TGRB	PWM output 6 compare register	Maskable by TRWERB setting*2
	TGRC	PWM output 5/MTU7.TGRA buffer register	Always readable/writable
	TGRD	PWM output 6/MTU7.TGRB buffer register	Always readable/writable
	TGRE	MTU7.TGRA buffer register B (when double buffer function is used)	Always readable/writable
	TGRF	MTU7.TGRB buffer register B (when double buffer function is used)	Always readable/writable

Note 1. Access can be enabled or disabled according to the setting in TRWERA (timer read/write enable register A).
Note 2. Access can be enabled or disabled according to the setting in TRWERB (timer read/write enable register B).

Table 22.70 Register Settings for Complementary PWM Mode

Channel	Counter/ Register	Description	Read/Write from CPU
Timer dead time data register A (TDDRA)		Set MTU4.TCNT and MTU3.TCNT offset value (dead time value)	Maskable by TRWERA setting *1
Timer dead time data register B (TDDRB)		Set MTU7.TCNT and MTU6.TCNT offset value (dead time value)	Maskable by TRWERB setting *2
Timer cycle data register A (TCDRA)		Set MTU4.TCNT upper limit value (1/2 carrier cycle)	Maskable by TRWERA setting *1
Timer cycle data register B (TCDRB)		Set MTU7.TCNT upper limit value (1/2 carrier cycle)	Maskable by TRWERB setting *2
Timer cycle buffer register A (TCBRA)		TCDRA buffer register	Always readable/writable
Timer cycle buffer register B (TCBRB)		TCDRB buffer register	Always readable/writable
Subcounter A (TCNTSA)		Subcounter A for dead time generation	Read-only
Subcounter B (TCNTSB)		Subcounter B for dead time generation	Read-only
Temporary register 1A (TEMP1A)		PWM output 1/MTU3.TGRB temporary register A	Not readable/writable
Temporary register 1B (TEMP1B)		PWM output 1/MTU3.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 2A (TEMP2A)		PWM output 2/MTU4.TGRA temporary register A	Not readable/writable
Temporary register 2B (TEMP2B)		PWM output 2/MTU4.TGRA temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 3A (TEMP3A)		PWM output 3/MTU4.TGRB temporary register A	Not readable/writable
Temporary register 3B (TEMP3B)		PWM output 3/MTU4.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 4A (TEMP4A)		PWM output 4/MTU6.TGRB temporary register A	Not readable/writable
Temporary register 4B (TEMP4B)		PWM output 4/MTU6.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 5A (TEMP5A)		PWM output 5/MTU7.TGRA temporary register A	Not readable/writable
Temporary register 5B (TEMP5B)		PWM output 5/MTU7.TGRA temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 6A (TEMP6A)		PWM output 6/MTU7.TGRB temporary register A	Not readable/writable
Temporary register 6B (TEMP6B)		PWM output 6/MTU7.TGRB temporary register B (when double buffer function is used)	Not readable/writable

Note 1. Access can be enabled or disabled according to the setting in TRWERA (timer read/write enable register A).
Note 2. Access can be enabled or disabled according to the setting in TRWERB (timer read/write enable register B).

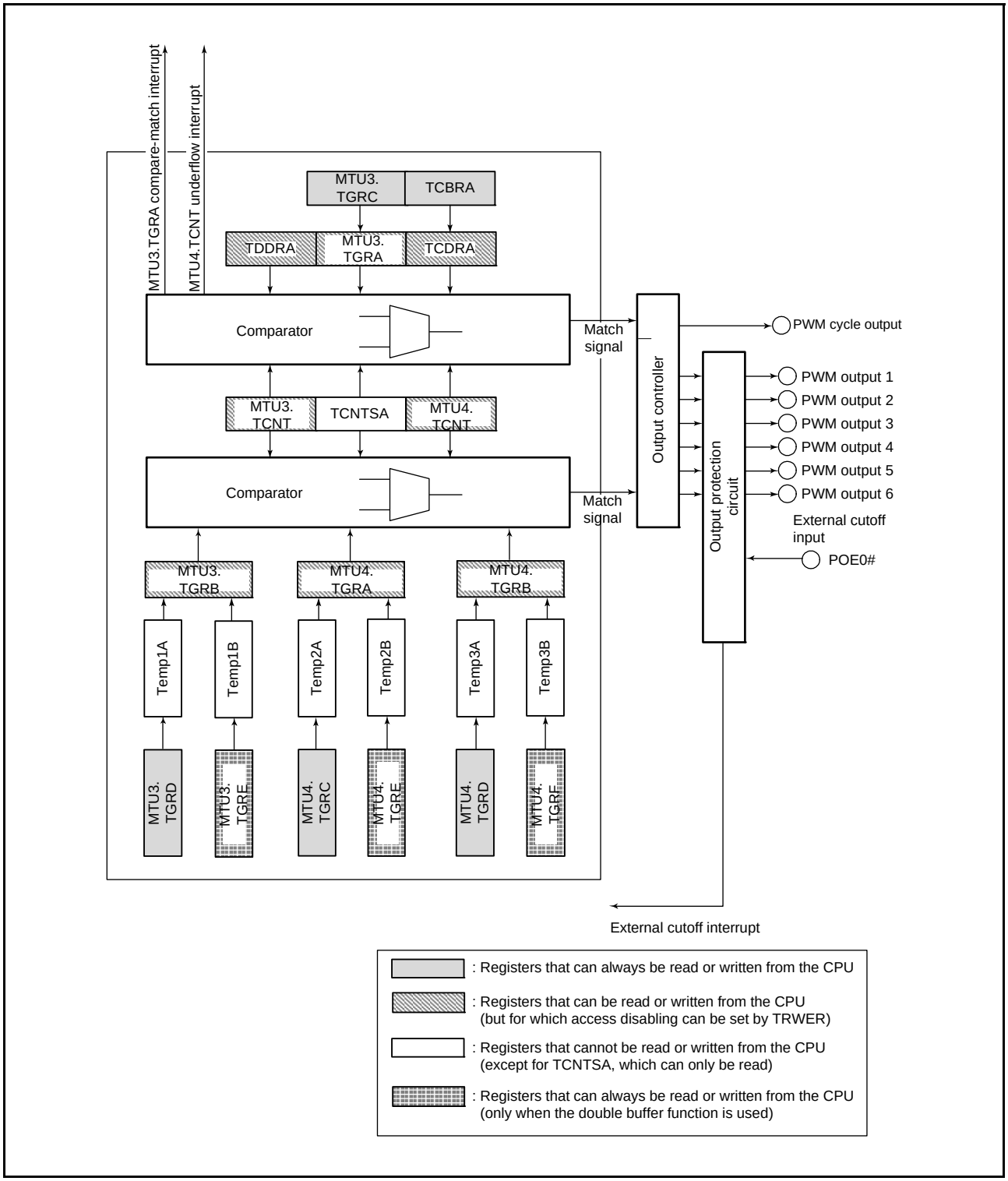


Figure 22.38 Block Diagram of MTU3 and MTU4 in Complementary PWM Mode

(1) Example of Complementary PWM Mode Setting Procedure

Figure 22.39 shows an example of the complementary PWM mode setting procedure.

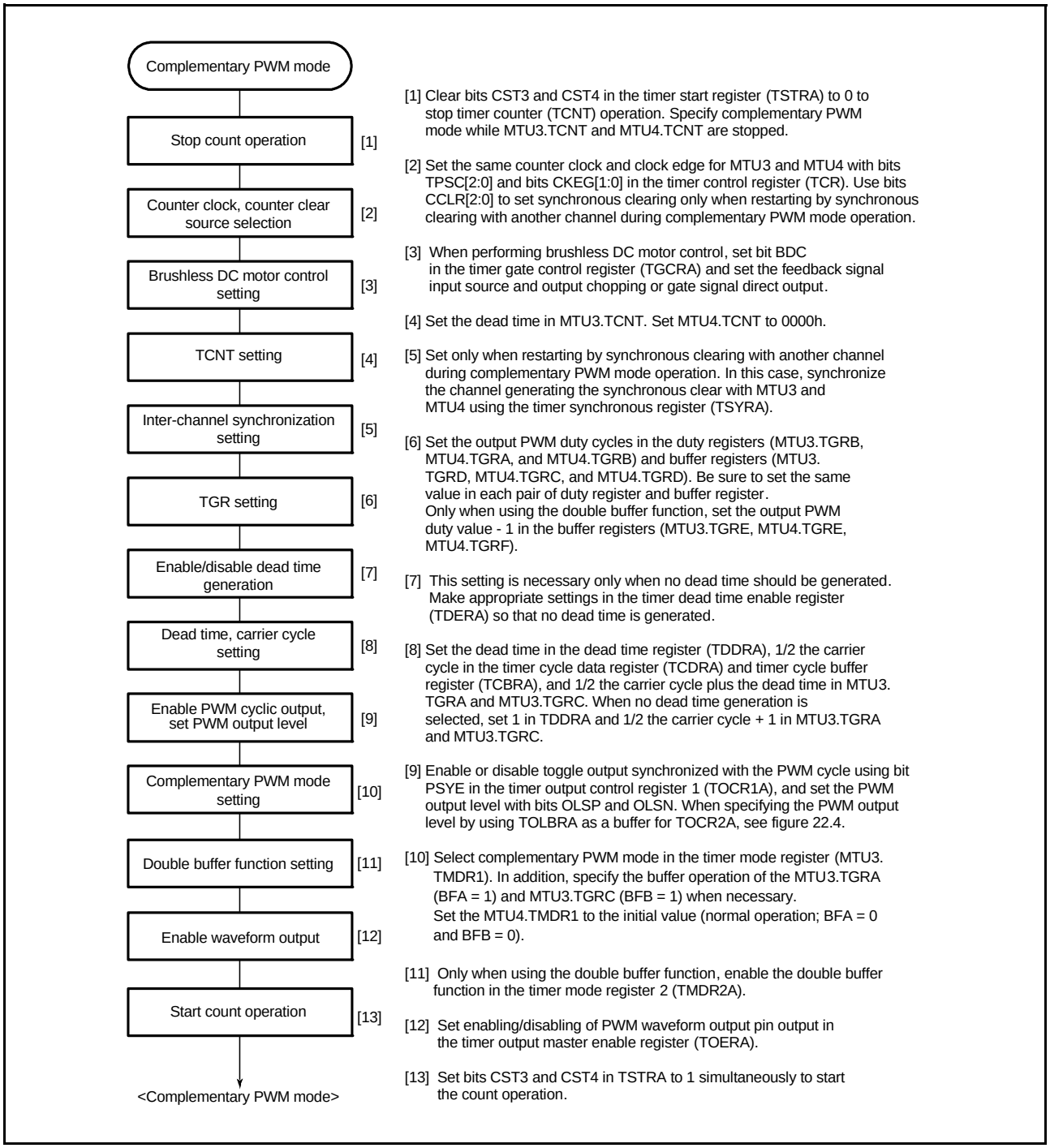


Figure 22.39 Example of Complementary PWM Mode Setting Procedure

(2) Outline of Complementary PWM Mode Operation

In complementary PWM mode, three phases (six phases in total) of PWM waveforms can be output. Figure 22.40 illustrates counter operation in complementary PWM mode (MTU3 and MTU4), and Figure 22.41 shows an example of operation in complementary PWM mode.

(a) Counter Operation

In complementary PWM mode, three counters—MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) —in each unit perform up-/down-count operations.
MTU3.TCNT (MTU6.TCNT) is automatically initialized to the value set in TDDRA (TDDRB) when complementary PWM mode is selected and the CST bit in TSTRA (TSTRB) is 0. When the CST bit is set to 1, MTU3.TCNT (MTU6.TCNT) counts up to the value set in MTU3.TGRA (MTU6.TGRA), then switches to down-counting when it matches MTU3.TGRA (MTU6.TGRA). When the MTU4.TCNT (MTU7.TCNT) value matches 0000h, MTU3.TCNT (MTU6.TCNT) switches to up-counting, and the operation is repeated in this way.
MTU4.TCNT (MTU7.TCNT) should be initialized to 0000h after a reset. When the CST bit is set to 1, MTU4.TCNT (MTU7.TCNT) counts up in synchronization with MTU3.TCNT (MTU6.TCNT), and switches to down-counting when MTU3.TCNT (MTU6.TCNT) matches MTU3.TGRA (MTU6.TGRA). On reaching 0000h, MTU4.TCNT (MTU7.TCNT) switches to up-counting, and the operation is repeated in this way. TCNTSA (TCNTSB) is a read-only counter. It does not need to be initialized after a reset.
In counting up by MTU3.TCNT and MTU4.TCNT (or MTU6.TCNT and MTU7.TCNT), MTU3.TCNT (or MTU6.TCNT) starts counting up when it matches TCDRA (or TCDRB) and switches to counting down when it matches MTU3.TGRA (or MTU6.TGRA). Furthermore, when MTU4.TCNT (or MTU7.TCNT) matches TDDRA (or TDDRB), TCNTSA (or TCNTSB) is set to the value in MTU3.TGRA (or MTU6.TGRA) and counting is stopped.
When MTU4.TCNT (MTU7.TCNT) matches TDDRA (TDDRB) during down-counting of MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT), TCNTSA (TCNTSB) starts up-counting, and when MTU4.TCNT (MTU7.TCNT) matches 0000h, the operation switches to down-counting. When MTU3.TCNT (MTU6.TCNT) matches TCDRA (TCDRB), TCNTSA (TCNTSB) is cleared to 0000h and stops counting.
TCNTSA (TCNTSB) is compared with the compare register and temporary register, in which the PWM duty is specified, only during the count operation.

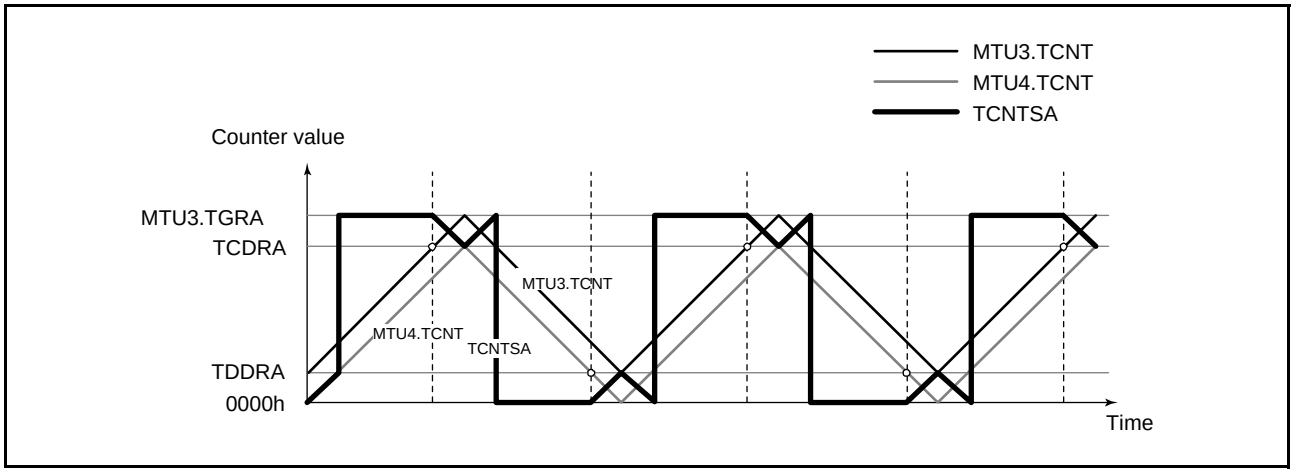


Figure 22.40 Counter Operation in Complementary PWM Mode

(b) Register Operation

In complementary PWM mode, nine registers (compare registers, buffer registers, and temporary registers) are used for each unit. Figure 22.41 shows an example of operation in complementary PWM mode (MTU3 and MTU4).
MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB (MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB) are constantly compared with the counters to generate PWM waveforms. When these registers match the counter, the value set in bits OLSN and OLSP in the timer output control register (TOCR1) is output.
MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD (MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD) are buffer registers for these compare registers.
When the double buffer function is used, MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF) are also used as buffer registers B. For details of double buffer operation, refer to section 22.3.8 (2) (s) Double Buffer Function in Complementary PWM Mode.
Data in a compare register can be changed by writing new data to the corresponding buffer register. The buffer registers can be read or written at any time.
When updating buffer register data, be sure to write to MTU4.TGRD (MTU7.TGRD) at the end of the update, to enable data to be transferred from the buffer registers to the temporary registers. At the same time, transfer from TCBRA (TCBRB) and MTU3.TGRC (MTU6.TGRC), which operate as buffer registers for the timer cycle registers, to temporary registers is also enabled. Data is transferred to all five temporary registers at the same time.
When transfer is enabled in the Ta interval, data written to a buffer register is transferred to the temporary register. Data is not transferred to the temporary register in the Tb1 and Tb2 intervals. Data enabled for transfer in this interval is transferred to the temporary register at the end of this interval.
The value transferred to a temporary register is transferred to the compare register at the end of the Tb1 interval (when TCNTSA (TCNTSB) matches MTU3.TGRA (MTU6.TGRA) at up-count), or at the end of the Tb2 interval (when TCNTSA (TCNTSB) matches 0000h at down-count). The timing for transfer from the temporary register to the compare register can be selected with the TMDR1.MD[3:0] bits. Figure 22.41 shows an example in which the trough is selected for the transfer timing.
In the Tb interval in which data is not transferred to the temporary register (Tb1 in Figure 22.41), the temporary register has the same function as the compare register and is compared with the counter. In this interval, therefore, there are two compare match registers for one output phase; the compare register contains the pre-change data and the temporary register contains new data. In this interval, three counters MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) and two registers (compare register and temporary register) are compared, and PWM output is controlled accordingly.

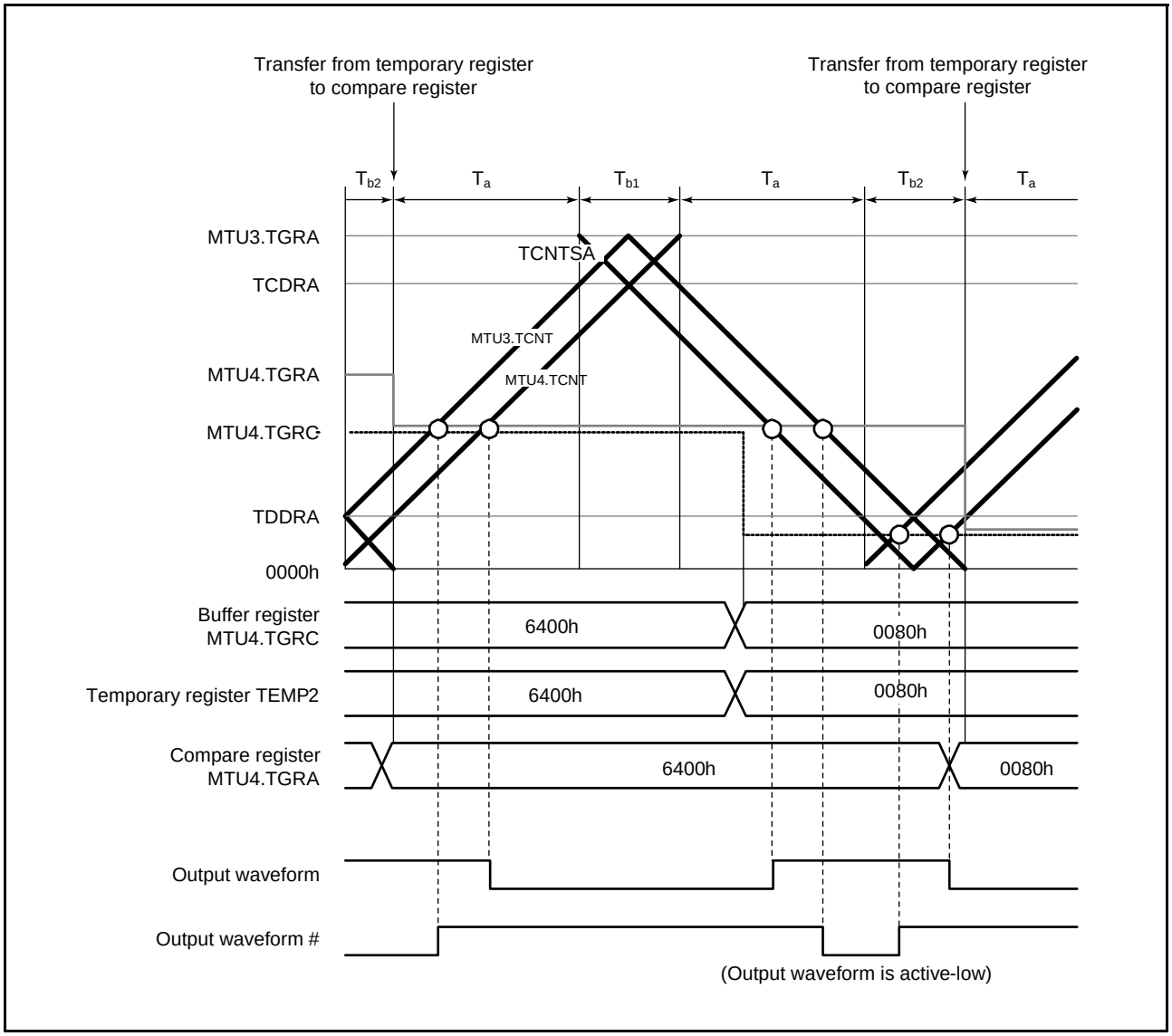


Figure 22.41 Example of Operation in Complementary PWM Mode (MTU3 and MTU4)

(c) Initial Setting

In complementary PWM mode, there are six registers that require initial setting. In addition, there is a register that specifies whether to generate dead time (it should be used only when dead time generation should be disabled).
Before setting complementary PWM mode with bits MD[3:0] in the timer mode register 1 (TMDR1), initial values should be set in the following registers.
MTU3.TGRC (MTU6.TGRC) operates as the buffer register for MTU3.TGRA (MTU6.TGRA), and should be set with 1/2 the PWM carrier cycle + dead time Td. The timer cycle buffer register (TCBRA or TCBRB) operates as the buffer register for the timer cycle data register (TCDRA or TCDRB), and should be set with 1/2 the PWM carrier cycle. Set dead time Td in the timer dead time data register (TDDRA or TDDRB).
When dead time is not needed, the TDER bit in the timer dead time enable register (TDERA or TDERB) should be cleared to 0, MTU3.TGRC and MTU3.TGRA (MTU6.TGRC and MTU6.TGRA) should be set to 1/2 the PWM carrier cycle + 1, and TDDRA (TDDRB) should be set to 1.
Set the respective initial PWM duty values in three buffer registers A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD (MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD)).
Set the respective (initial PWM duty – 1) values in three buffer registers B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)) only when the double buffer function is used.
The values set in the five buffer registers excluding TDDRA (TDDRB) are transferred to the corresponding compare registers as soon as complementary PWM mode is set.
Set MTU4.TCNT (MTU7.TCNT) to 0000h before setting complementary PWM mode.

Table 22.71 Registers and Counters Requiring Initial Setting

Register and Counter	Setting
MTU3.TGRC MTU6.TGRC	1/2 PWM carrier cycle + dead time Td (1/2 PWM carrier cycle + 1 when dead time generation is disabled by TDERA or TDERB)
TDDRA, TDDRB	Dead time Td (1 when dead time generation is disabled by TDERA or TDERB)
TCBRA, TCBRB	1/2 PWM carrier cycle
MTU3.TGRD, MTU4.TGRC, MTU4.TGRD MTU6.TGRD, MTU7.TGRC, MTU7.TGRD	Initial PWM duty ratio value for each phase
MTU3.TGRE, MTU4.TGRE, MTU4.TGRF MTU6.TGRE, MTU7.TGRE, MTU7.TGRF	Initial PWM duty ratio – 1 value for each phase (only when double buffer function is used)
MTU4.TCNT MTU7.TCNT	0000h

Note 1. The value set in MTU3.TGRC (MTU6.TGRC) should be the sum of 1/2 the PWM carrier cycle set in TCBRA (TCBRB) and dead time Td set in TDDRA (TDDRB). When dead time generation is disabled by TDERA (TDERB), TGRC should be set to 1/2 the PWM carrier cycle + 1.

(d) PWM Output Level Setting

In complementary PWM mode, the PWM pulse output level is set with bits OLSN and OLSP in timer output control register 1 (TOCR1A or TOCR1B) or bits OLS1P to OLS3P and OLS1N to OLS3N in timer output control register 2 (TOCR2A or TOCR2B).
The output level can be set for each of the three positive phases and three negative phases of 6-phase output.
Complementary PWM mode should be cleared before setting or changing output levels.

(e) Dead Time Setting

In complementary PWM mode, dead time can be set in the PWM waveform to be output.
Dead time is set in TDDRA and TDDRB. The value set in TDDRA is used as the MTU3.TCNT counter start value and generates a dead time between MTU3.TCNT and MTU4.TCNT.
The value set in TDDRB is used as the MTU6.TCNT counter start value and generates a dead time between MTU6.TCNT and MTU7.TCNT. Complementary PWM mode should be cleared before changing the contents of TDDRA (TDDRB).

(f) Dead Time Suppressing

Dead time generation is suppressed by clearing the TDER bit in the timer dead time enable register (TDERA or TDERB) to 0. TDERA (TDERB) can be cleared to 0 only when 0 is written to it after reading TDER = 1.
MTU3.TGRA and MTU4.TGRC (MTU6.TGRA and MTU7.TGRC) should be set to 1/2 PWM carrier cycle + 1 and the timer dead time data register (TDDRA or TDDRB) should be set to 1.
By the above settings, PWM waveforms without dead time can be obtained. Figure 22.42 shows an example of operation without dead time (MTU3 and MTU4).

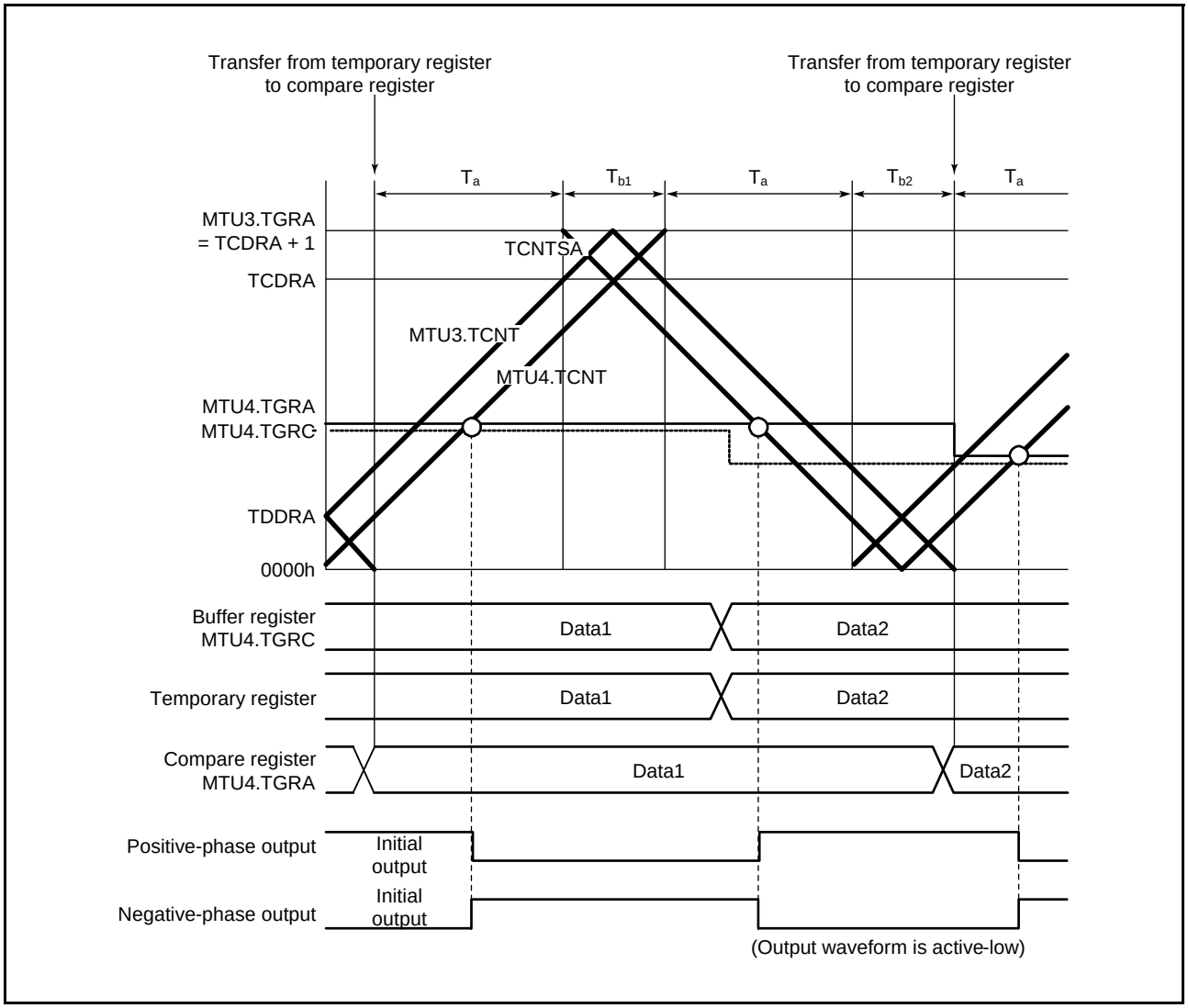


Figure 22.42 Example of Operation without Dead Time (MTU3 and MTU4)

(g) PWM Cycle Setting

In complementary PWM mode, the PWM pulse cycle is set in two registers—MTU3.TGRA (MTU6.TGRA), in which the MTU3.TCNT (MTU6.TCNT) upper limit value is set, and TCDRA (TCDRB), in which the MTU4.TCNT (MTU7.TCNT) upper limit value is set. The settings should be made so as to achieve the following relationship between these two registers:
With dead time: MTU3.TGRA (MTU6.TGRA) setting = TCDRA (TCDRB) setting + TDDRA (TDDRB) setting
Without dead time: MTU3.TGRA (MTU6.TGRA) setting = TCDRA (TCDRB) setting + 1
For the PWM output with dead time, the setting should be made so as to achieve the following relationship between these two registers:
TCDRA(TCDRB) setting > TDDRA(TDDRB) setting × 2 + 2

The MTU3.TGRA and TCDRA (MTU6.TGRA and TCDRB) settings are made by setting values in buffer registers MTU3.TGRC and TCBRA (MTU6.TGRC and TCBRB). When data is written to MTU4.TGRD (MTU7.TGRD) to enable transfers, the values set in MTU3.TGRC and TCBRA (MTU6.TGRC and TCBRB) are transferred simultaneously to the MTU3.TGRA and TCDRA (MTU6.TGRA and TCDRB) according to the transfer timing selected with the MTU3.TMDR1.MD[3:0] (MTU6.TMDR1.MD[3:0]) bits.
The new PWM cycle is reflected from the next cycle when data is updated at the crest, or from the current cycle when updated in the trough. Figure 22.43 illustrates the operation when the PWM cycle is updated at the crest.
See the following section, (h) Register Data Updating, for the method of updating the data in each buffer register.

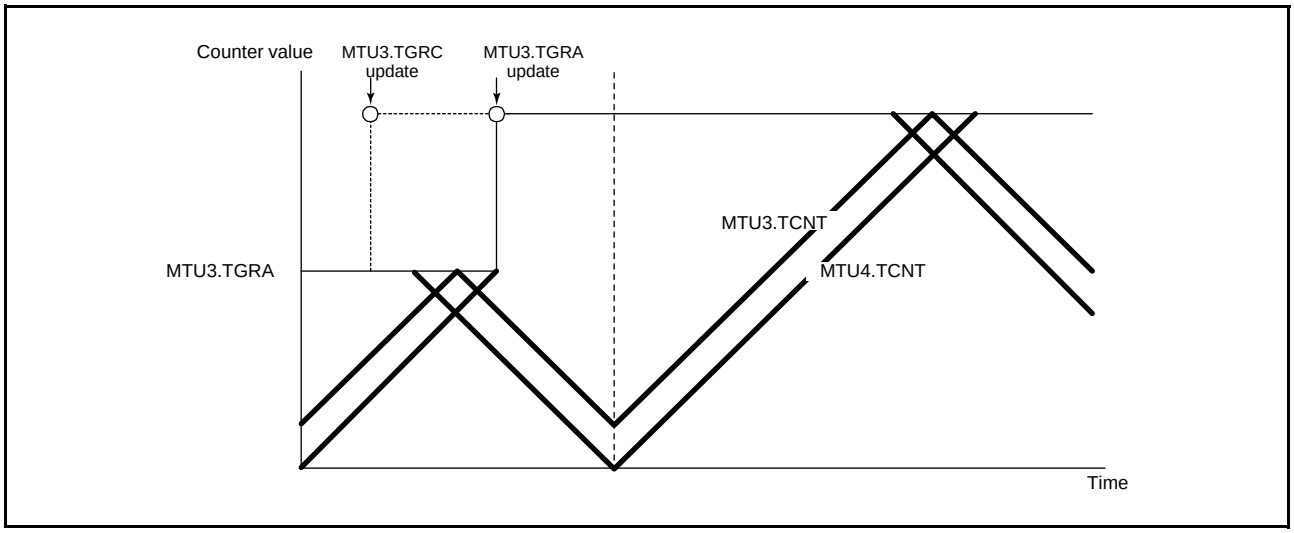


Figure 22.43 Example of PWM Cycle Updating (MTU3 and MTU4)

(h) Register Data Updating

In complementary PWM mode, the buffer register is used to update the data in a compare register. The update data can be written to the buffer register at any time. There are five registers (PWM duty and carrier cycle registers) that have buffer registers and can be updated during operation.

There is a temporary register between each of these registers and its buffer register. While subcounter TCNTSA (TCNTSB) is not counting, if buffer register data is updated, the temporary register value also changes. Data is not transferred from buffer registers to temporary registers while TCNTSA (TCNTSB) is counting; in this case, the value written to a buffer register is transferred after TCNTSA (TCNTSB) halts.

The temporary register value is transferred to the compare register at the data update timing set with bits MD[3:0] in the timer mode register 1 (TMDR1). Figure 22.44 shows an example of data updating in complementary PWM mode (MTU3 and MTU4). This example shows the mode in which data is updated at both the counter crest and trough.

When updating buffer register data, be sure to write to MTU4.TGRD (MTU7.TGRD) at the end of the update. Data is transferred from buffer registers to the temporary registers simultaneously for all five registers after the write to MTU4.TGRD (MTU7.TGRD).

Even when not updating all five registers or when not updating the MTU4.TGRD (MTU7.TGRD) data, be sure to write to MTU4.TGRD (MTU7.TGRD) after writing data to the registers to be updated. In this case, the data written to MTU4.TGRD (MTU7.TGRD) should be the same as the data prior to the write operation.

See section 22.3.8 (2) (s) Double Buffer Function in Complementary PWM Mode, for data updating when the double buffer function is used.

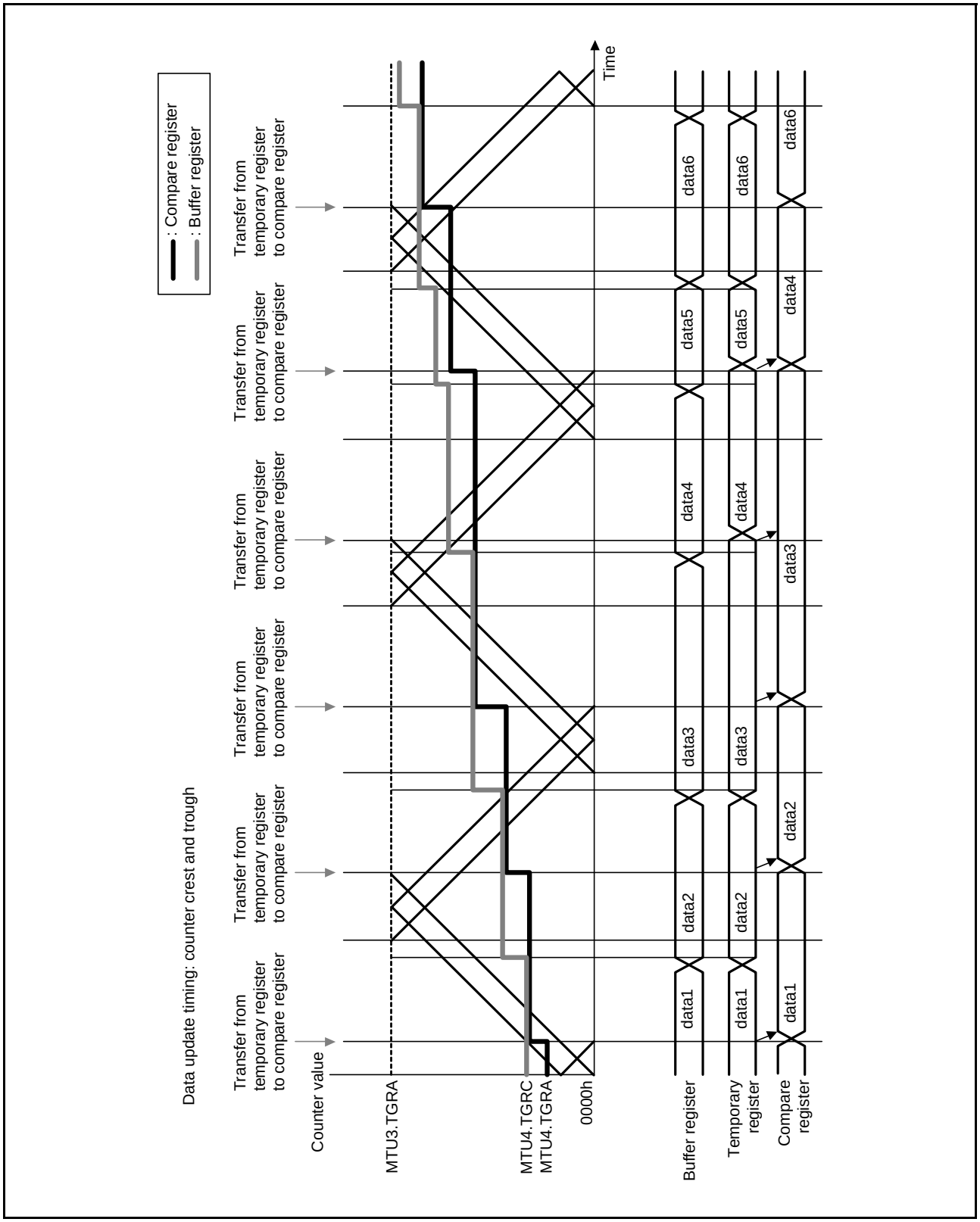


Figure 22.44 Example of Data Updating in Complementary PWM Mode (MTU3 and MTU4)

(i) Initial Output in Complementary PWM Mode

In complementary PWM mode, the initial output is determined by the setting of bits OLSN and OLSP in timer output control register 1 (TOCR1A or TOCR1B) or bits OLS1N to OLS3N and OLS1P to OLS3P in timer output control register 2 (TOCR2A or TOCR2B).

This initial output is the non-active level of the PWM pulse and continues from when complementary PWM mode is set with the timer mode register 1 (TMDR1) until MTU4.TCNT (MTU7.TCNT) exceeds the value set in the dead time register (TDDRA or TDDRB). Figure 22.45 shows an example of the initial output in complementary PWM mode. An example of the waveform when the initial PWM duty ratio value is smaller than the TDDRA (TDDRB) value is shown in Figure 22.46.

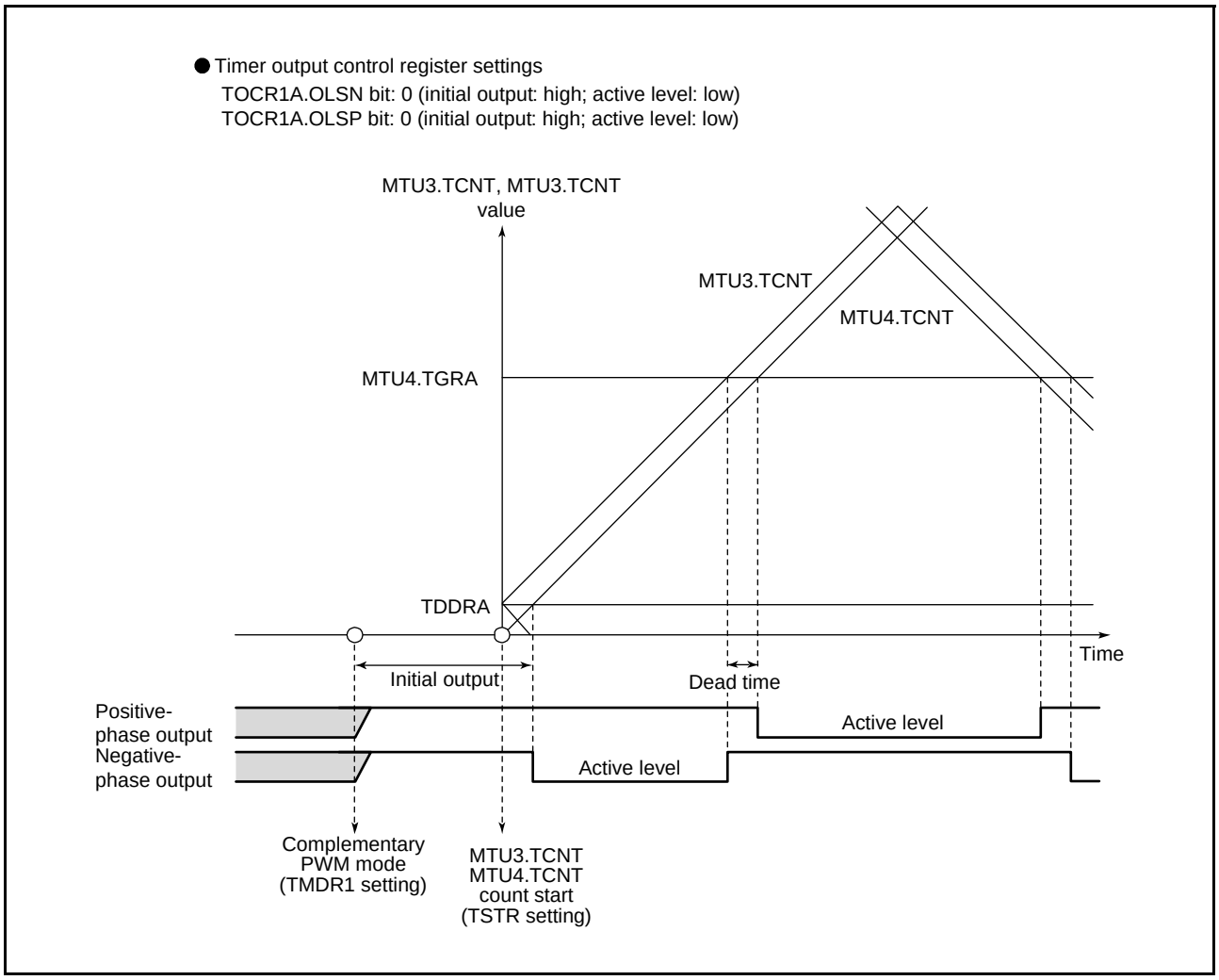


Figure 22.45 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (1))

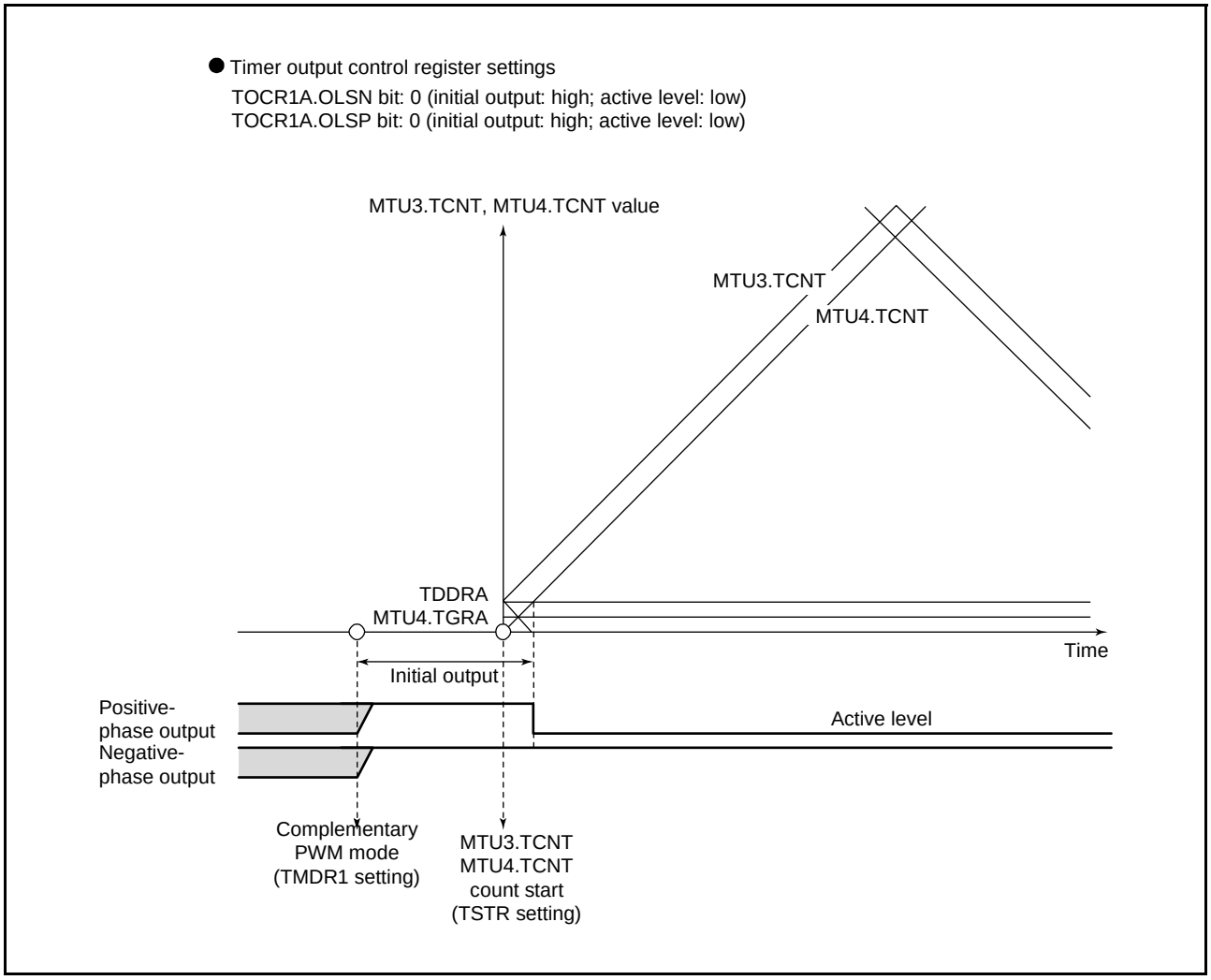


Figure 22.46 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (2)

(j) Method for Generating PWM Output in Complementary PWM Mode

In complementary PWM mode, three-phases (six phases in total) of PWM waveforms are output. Dead time can be set in the PWM waveform to be output.

A PWM waveform is generated by output of the level selected in the timer output control register in the event of a compare match between a counter and a compare register. While TCNTSA (TCNTSB) is counting, the compare register and temporary register values are simultaneously compared to create consecutive PWM pulses from 0 to 100%. The relative timing of turn-on and turn-off compare match occurrence may vary, but the compare match that turns off each phase takes precedence to secure the dead time and ensure that the positive-phase and negative-phase turn-on times do not overlap. Figure 22.47 to Figure 22.49 show examples of waveform generation in complementary PWM mode.

The positive-phase and negative-phase turn-off timing is generated by a compare match with the counter indicated by a solid line, and the turn-on timing is generated by a compare match with the counter indicated by a dotted line, which operates with a delay equal to the dead time behind the counter indicated by a solid line.

In the T1 period, compare match a that turns off the negative phase has the highest priority, and compare matches before a are ignored. In the T2 period, compare match c that turns off the positive phase has the highest priority, and compare matches before c are ignored.

In most cases, compare matches occur in the order a → b → c → d (or c → d → a' → b') as shown in Figure 22.47.

If compare matches deviate from the a → b → c → d order, since the time for which the negative phase is off is shorter than twice the dead time, the positive phase is not turned on. If compare matches deviate from the c → d → a' → b' order, since the time for which the positive phase is off is shorter than twice the dead time, the negative phase is not turned on.

As shown in Figure 22.48, if compare match c follows compare match a before compare match b, compare match b is ignored and the negative phase is turned on by compare match d. This is because turning off the positive phase has priority due to the occurrence of compare match c (positive-phase off timing) before compare match b (positive-phase on timing) (consequently, the waveform does not change because the positive phase goes from off to off).

Similarly, in the example in Figure 22.48, turning off the negative phase has priority due to the occurrence of compare match a' (negative-phase off timing) before compare match d (negative-phase on timing). As a result, the negative phase is not turned on.

Thus, in complementary PWM mode, compare matches at turn-off timings take precedence, and turn-on timing compare matches that occur before a turn-off timing compare match are ignored.

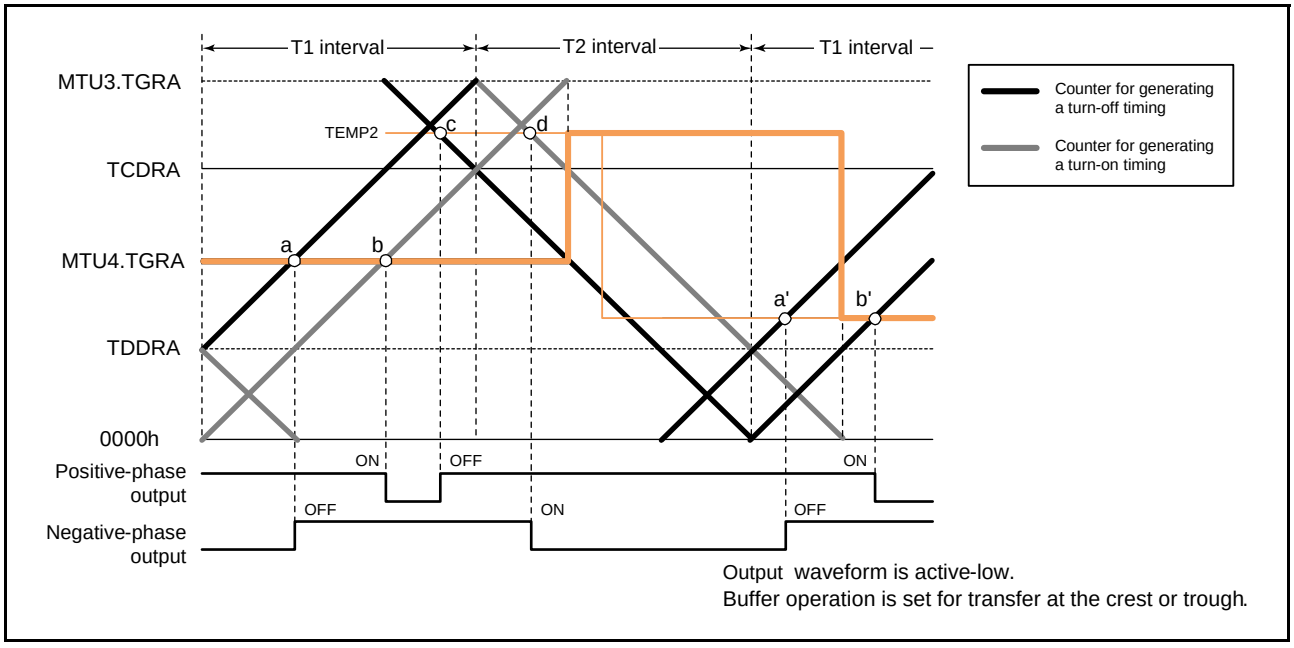


Figure 22.47 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1)

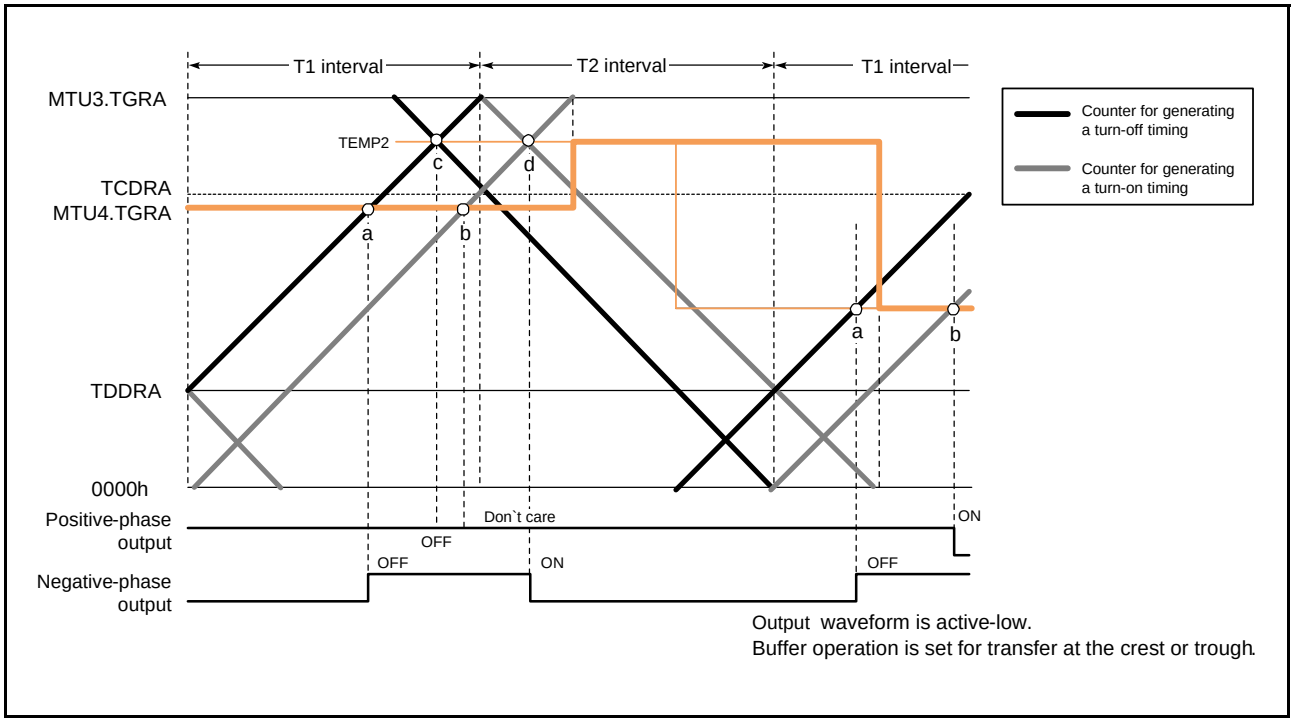


Figure 22.48 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2)

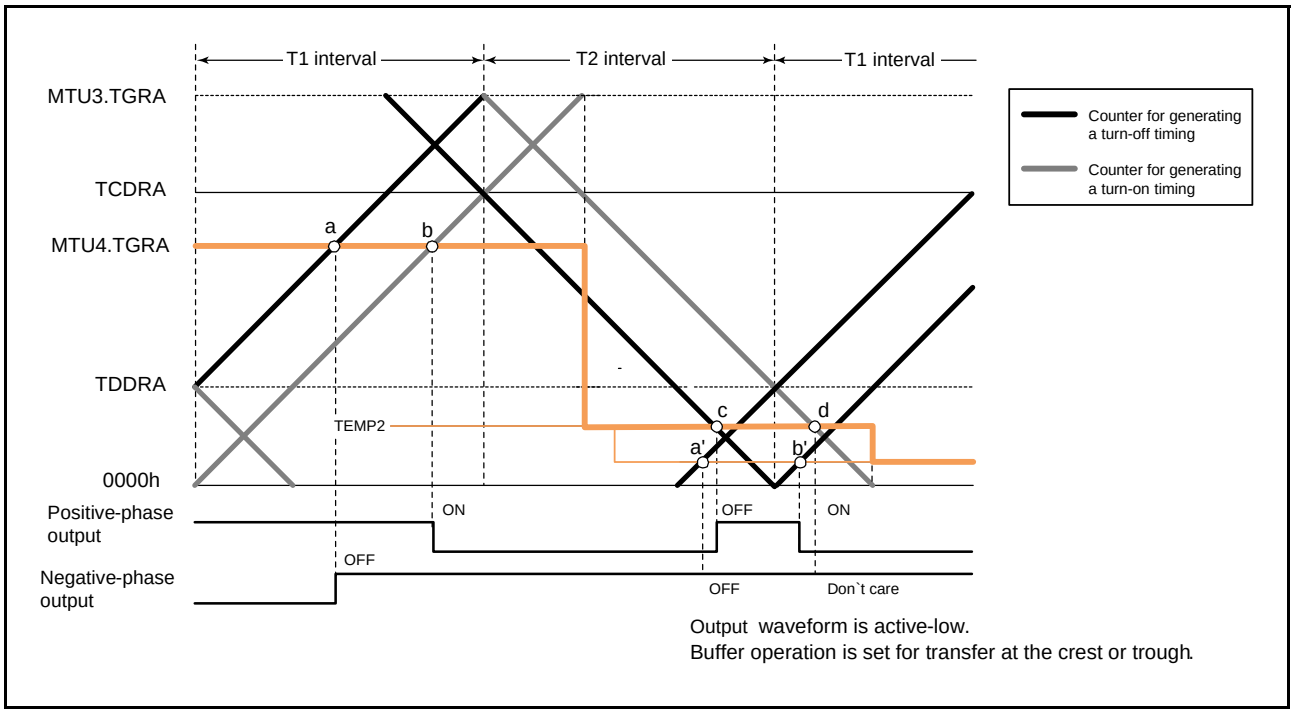


Figure 22.49 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3)

(k) 0% and 100% duty ratio Output in Complementary PWM Mode

In complementary PWM mode, 0% and 100% duty PWM waveforms can be output as required. Figure 22.50 to Figure 22.54 show output examples.

A 100% duty waveform is output when the compare register value is set to 0000h. The waveform in this case has a positive phase with a 100% on-state. A 0% duty waveform is output when the compare register value is set to the same value as MTU3.TGRA (MTU6.TGRA). The waveform in this case has a positive phase with a 100% off-state.

On and off compare matches occur simultaneously, but if a turn-on compare match and turn-off compare match for the same phase occur simultaneously, both compare matches are ignored and the waveform does not change.

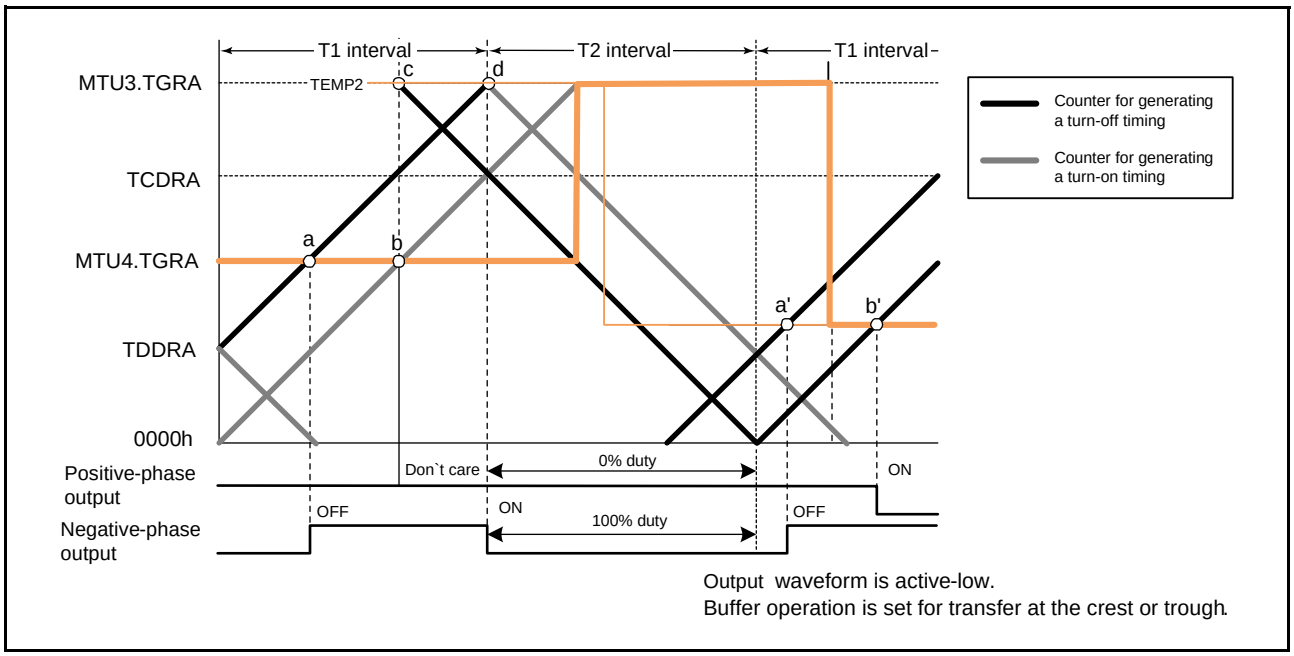


Figure 22.50 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1)

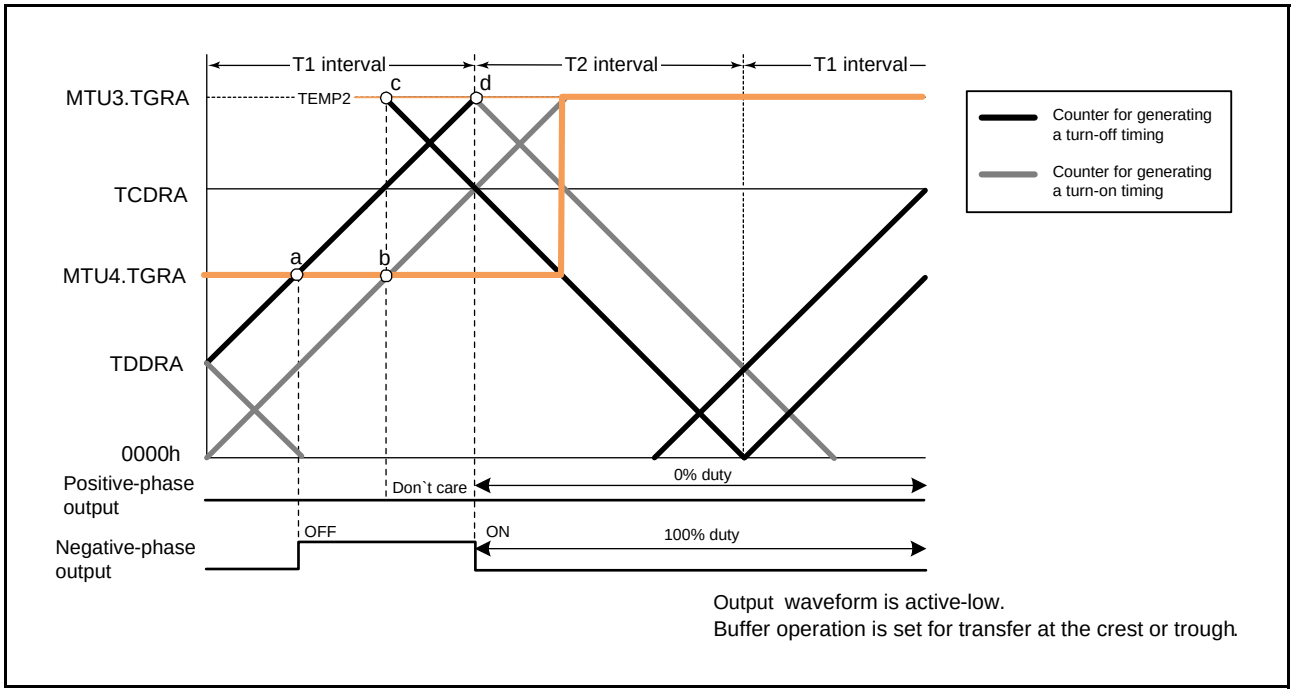


Figure 22.51 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2)

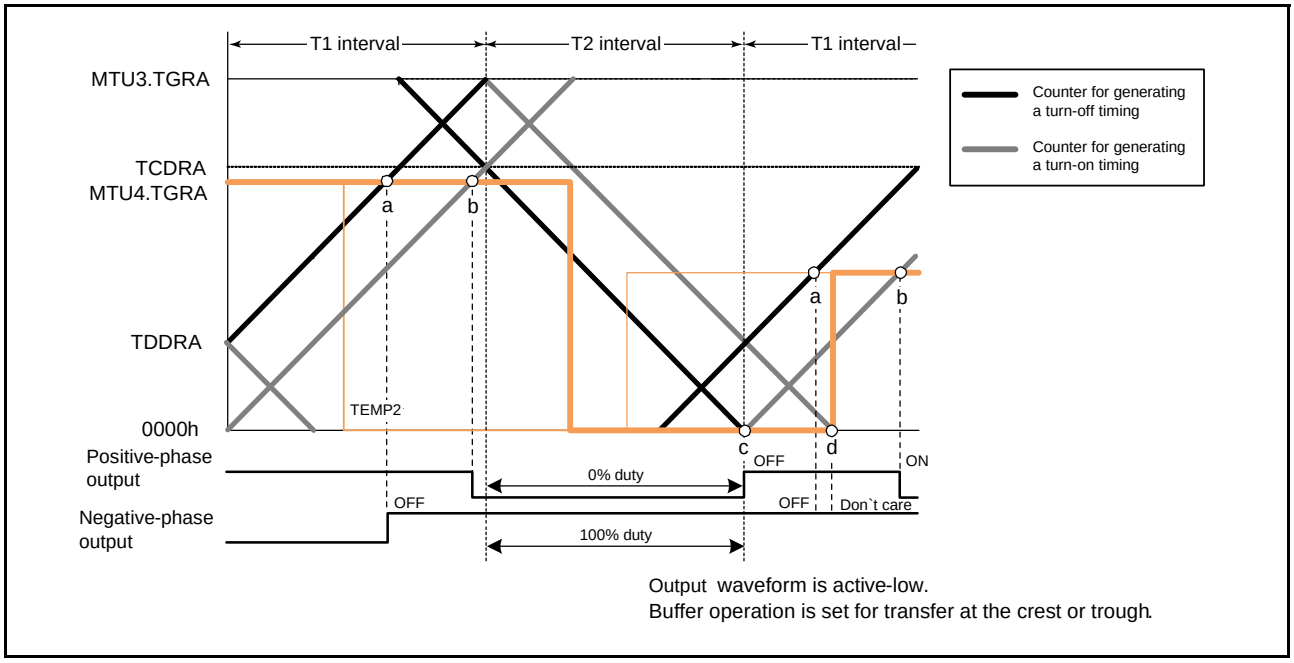


Figure 22.52 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3)

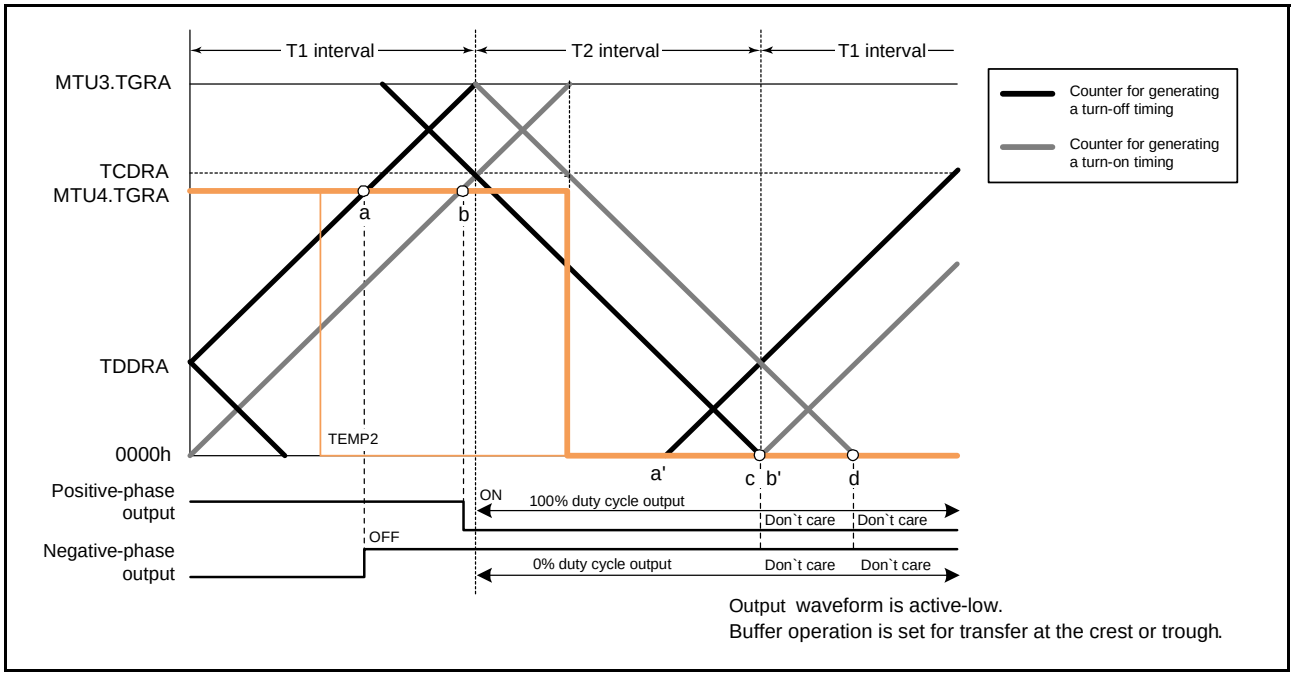


Figure 22.53 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (4)

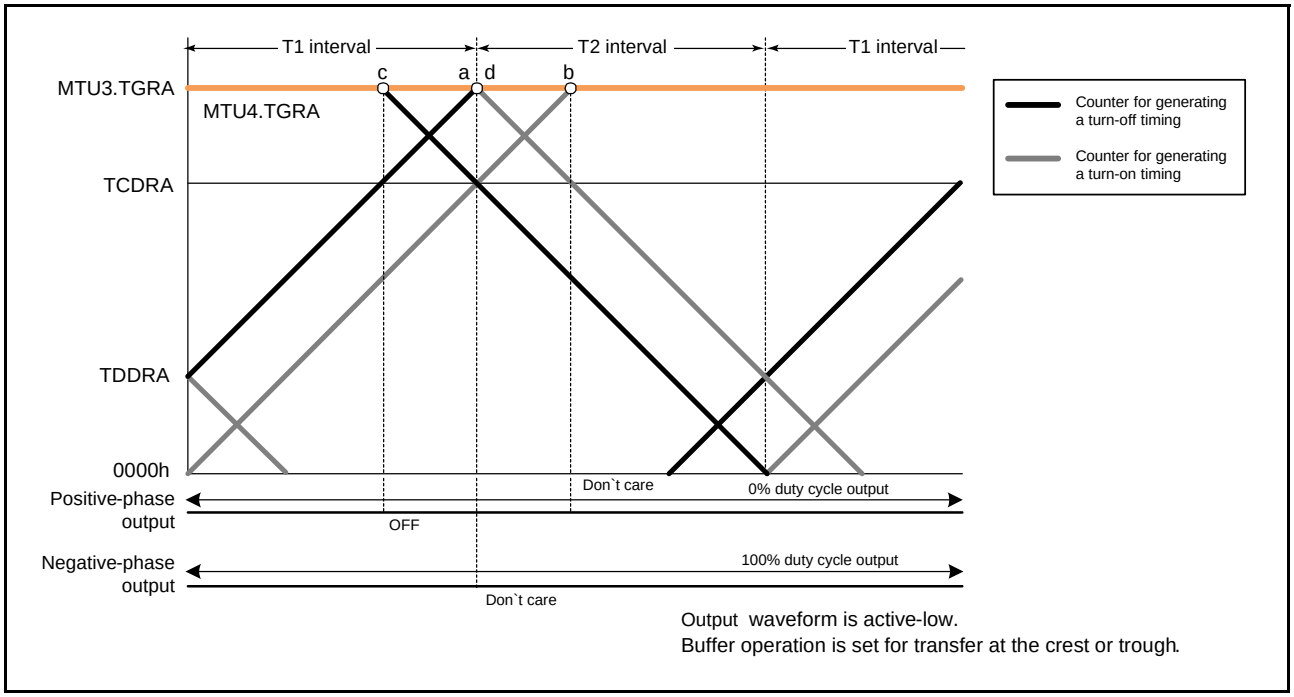


Figure 22.54 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (5)

(l) Toggle Output Synchronized with PWM Cycle

In complementary PWM mode, toggle output in synchronization with the PWM carrier cycle can be generated by setting the PSYE bit to 1 in the timer output control register 1 (TOCR1A or TOCR1B). An example of a toggle output waveform is shown in Figure 22.55.

This output is toggled by a compare match between MTU3.TCNT and MTU3.TGRA (MTU6.TCNT and MTU6.TGRA) and a compare match between MTU4.TCNT (MTU7.TCNT) and 0000h.

The MTIOC3A (MTIOC6A) pin is assigned for this toggle output. The initial output is High.

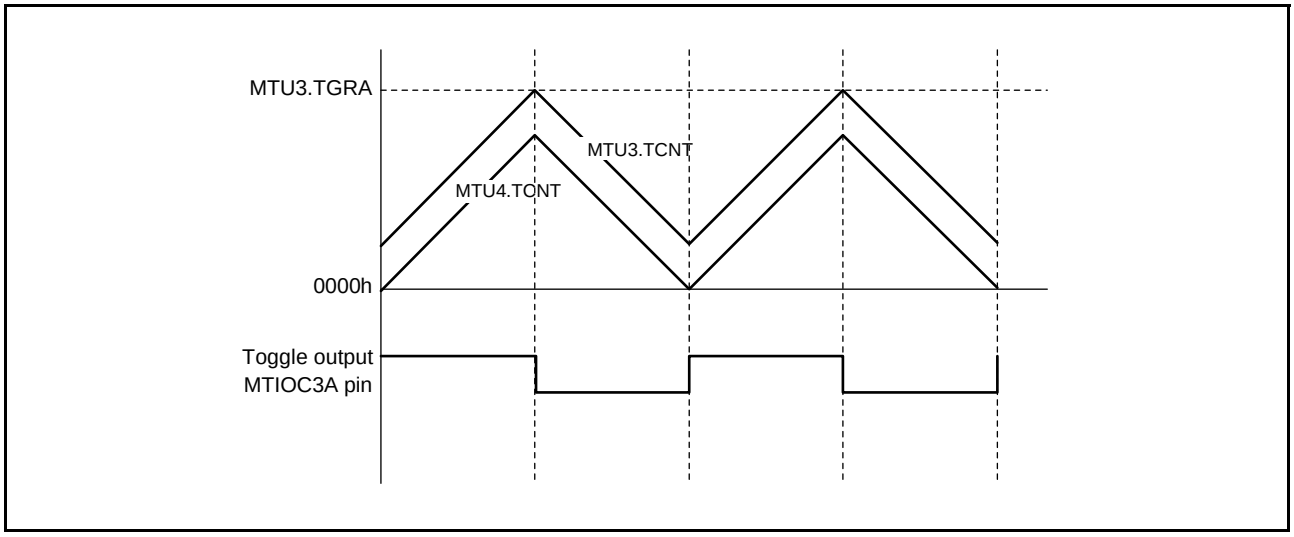


Figure 22.55 Example of Toggle Output Waveform Synchronized with PWM Output (MTU3 and MTU4)

(m) Counter Clearing by Another Channel

In complementary PWM mode, MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) can be cleared by another channel when a mode for synchronization with another channel is specified through the timer synchronous register (TSYRA or TSYRB)) and synchronous clearing is selected with bits CCLR[2:0] in the timer control register (TCR).

Figure 22.56 illustrates an example of this operation.

Use of this function enables a counter to be cleared and restarted through an external signal.

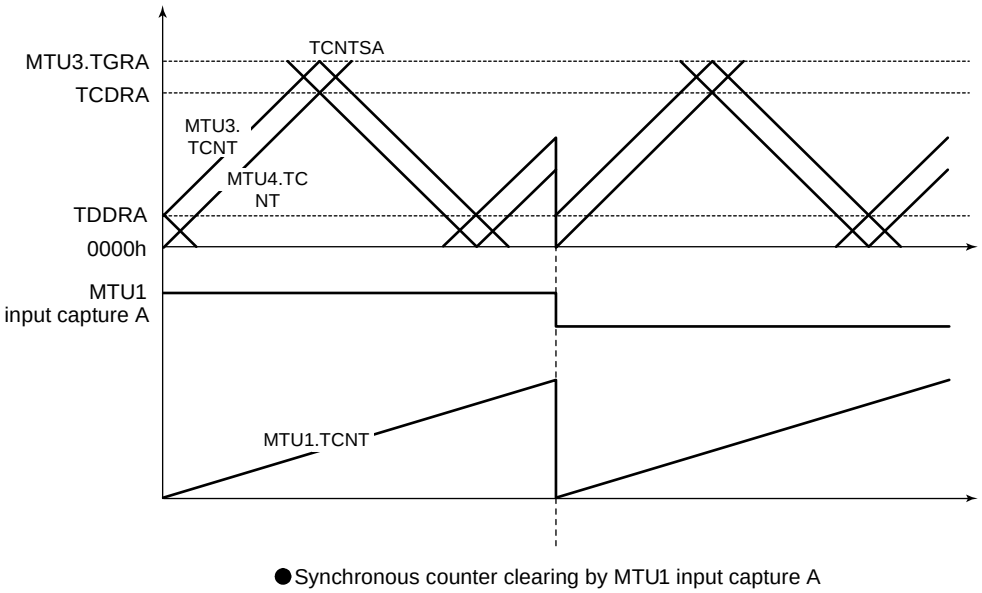


Figure 22.56 Counter Clearing Synchronized with Another Channel (MTU3 and MTU4)

(n) Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Setting the WRE bit in TWCRA (TWCRB) to 1 suppresses initial output when synchronous counter clearing occurs in the Tb interval at the trough in complementary PWM mode and controls abrupt change in duty cycle at synchronous counter clearing.

Initial output suppression through the WRE bit = 1 is applicable only when synchronous clearing occurs in the Tb interval at the trough as indicated by (10) or (11) in Figure 22.57. When synchronous clearing occurs outside that interval, the initial value specified by the OLS bits in TOCR1A (TOCR1B) is output. Even in the Tb interval at the trough, if synchronous clearing occurs in the initial value output period (indicated by (1) in Figure 22.57) immediately after the counters start operation, initial value output is not suppressed.

This function can be used in both channel combinations of MTU 3 and MTU4 and MTU6 and MTU7. In MTU3 and MTU4, synchronous clearing generated in MTU0, MTU1 and MTU2 can cause counter clearing; in MTU6 and MTU7, flag setting (compare match or input capture) in MTU0, MTU1 and MTU2 can cause counter clearing.

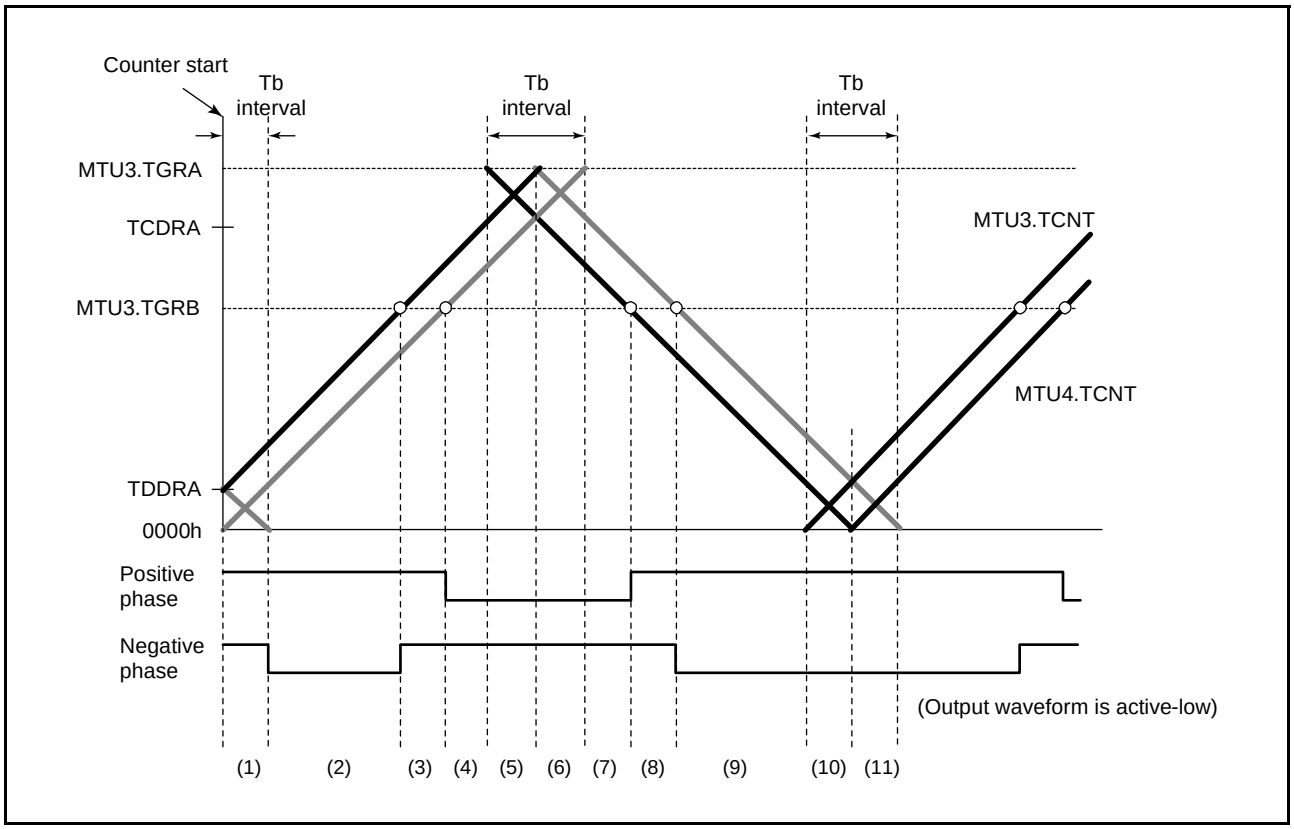


Figure 22.57 Timing for Synchronous Counter Clearing (MTU3 and MTU4)

- Example of Procedure for Setting Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode.

An example of the procedure for setting output waveform control at synchronous counter clearing in complementary PWM mode is shown in Figure 22.58.

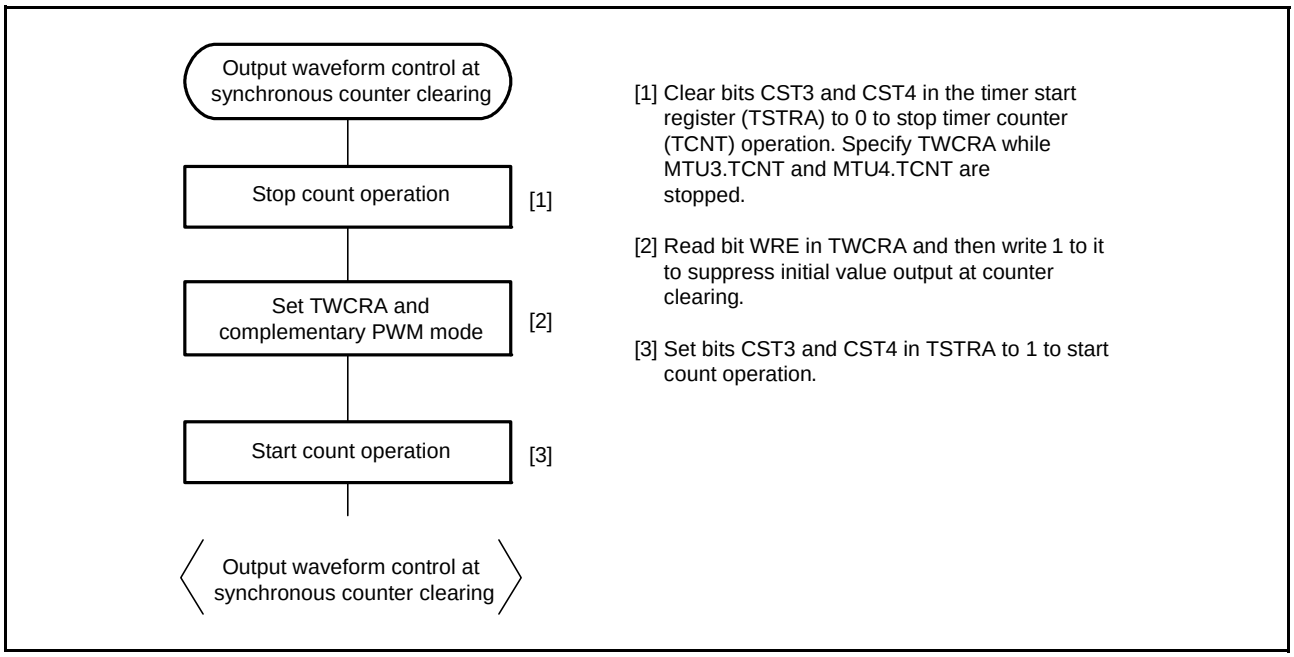


Figure 22.58 Example of Procedure for Setting Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode (MTU3 and MTU4)

- Examples of Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Figure 22.59 to Figure 22.62 show examples of output waveform control in which MTU3 and MTU4 operate in complementary PWM mode and synchronous counter clearing is generated while the WRE bit in TWCRA is set to 1. In the examples shown in Figure 22.59 to Figure 22.62, synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in Figure 22.57, respectively.

In MTU6 and MTU7, these examples are equivalent to the cases when MTU6 and MTU7 operate in complementary PWM mode and synchronous counter clearing is generated while the SCC bit is cleared to 0 and the WRE bit is set to 1 in TWCRB.

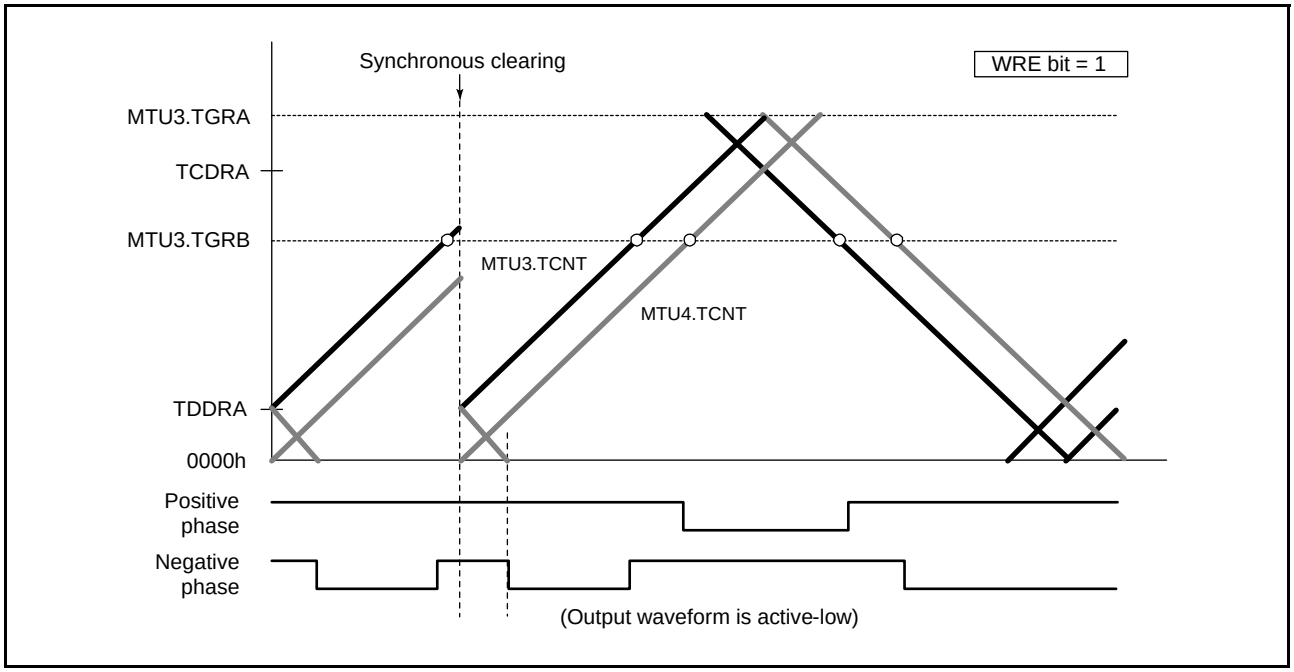


Figure 22.59 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 22.57; Bit WRE of TWCRA or TWCRB is 1)

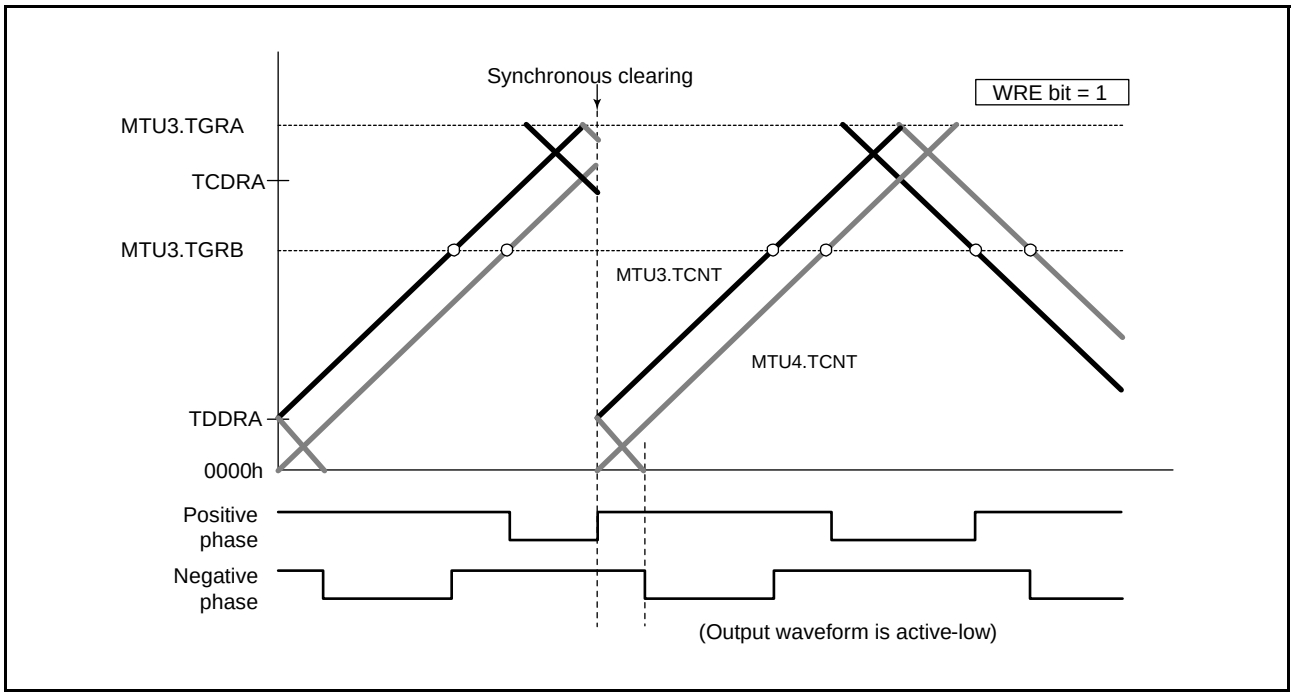


Figure 22.60 Example of Synchronous Clearing in Interval Tb at Crest (Timing (6) in Figure 22.57; Bit WRE of TWCRA or TWCRB is 1)

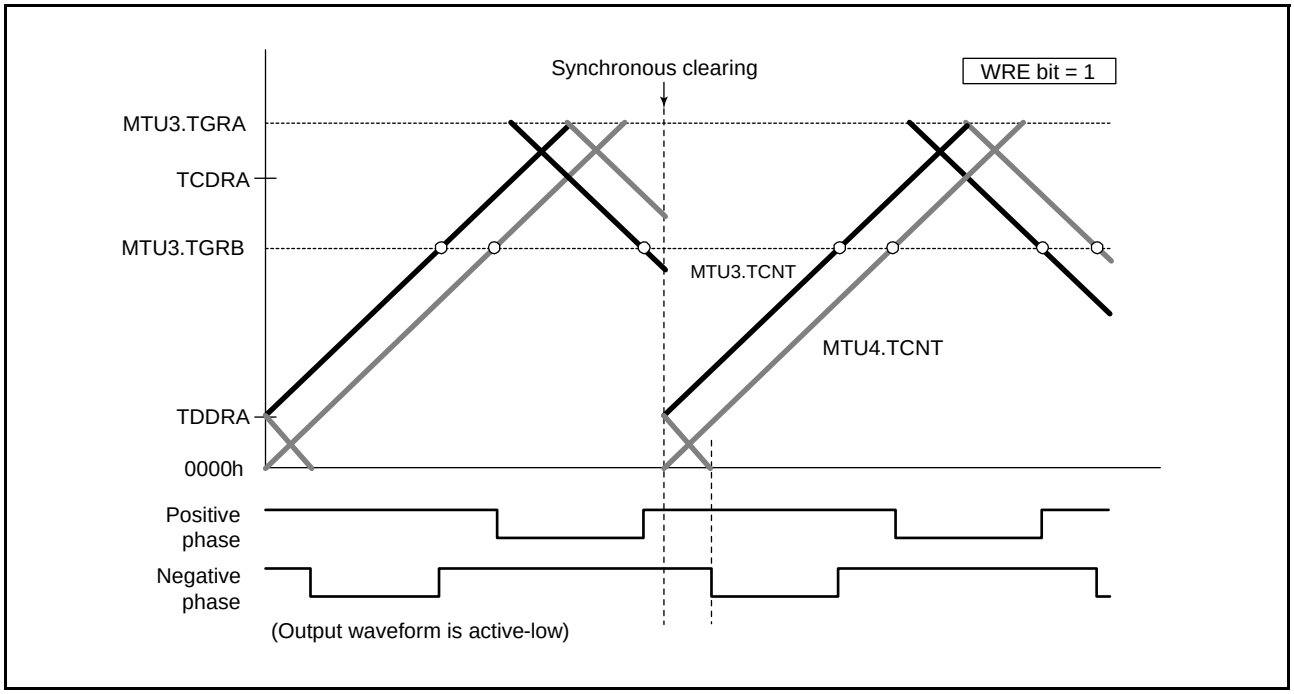


Figure 22.61 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 22.57; Bit WRE of TWCRA or TWCRB is 1)

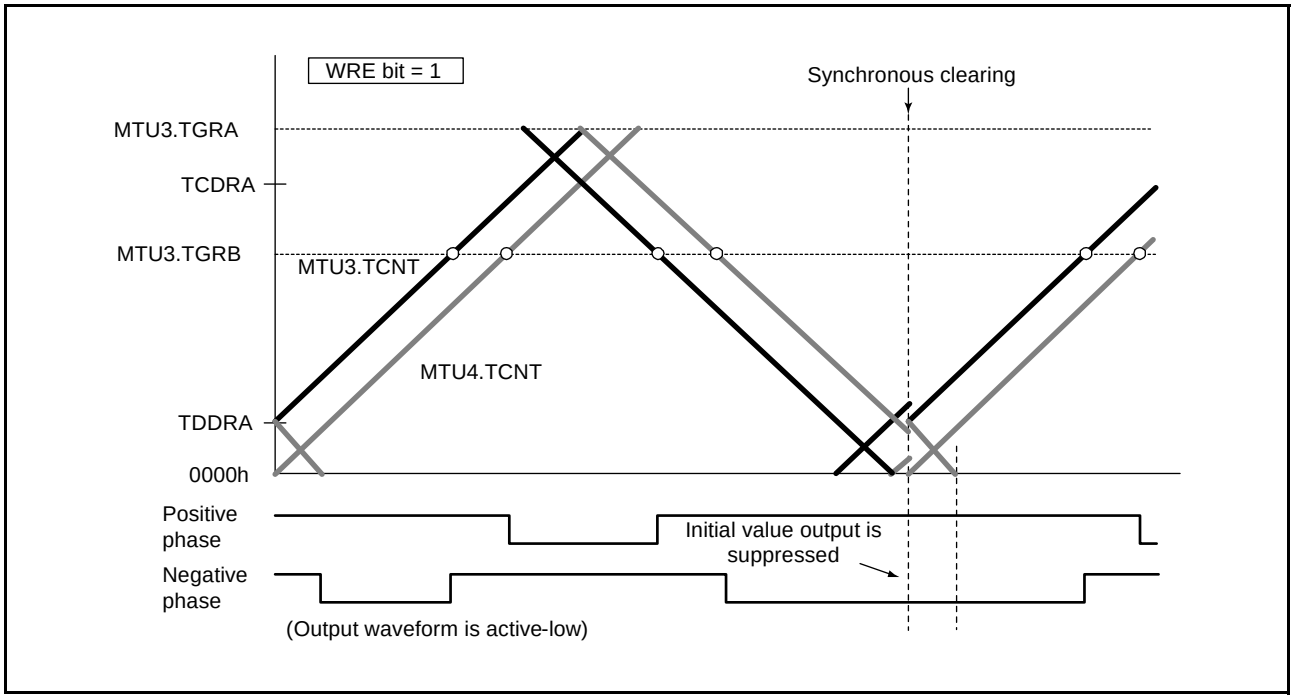


Figure 22.62 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 22.57; Bit WRE of TWCRA or TWCRB is 1)

(o) Suppressing Synchronous Counter Clearing for MTU0 to MTU2 and MTU6 and MTU7

In MTU6 and MTU7, setting the SCC bit in TWCRB to 1 suppresses synchronous counter clearing caused by MTU0 to MTU2.

Synchronous counter clearing is suppressed only within the interval shown in Figure 22.63. When using this function, MTU6 and MTU7 should be set to complementary PWM mode.

For details of synchronous clearing caused by MTU0 to MTU2, refer to section 22.3.10 (2) Clearing Counters of MTU6 and MTU7 by Flag Setting Sources (Synchronous Counter Clearing for MTU6 and MTU7).

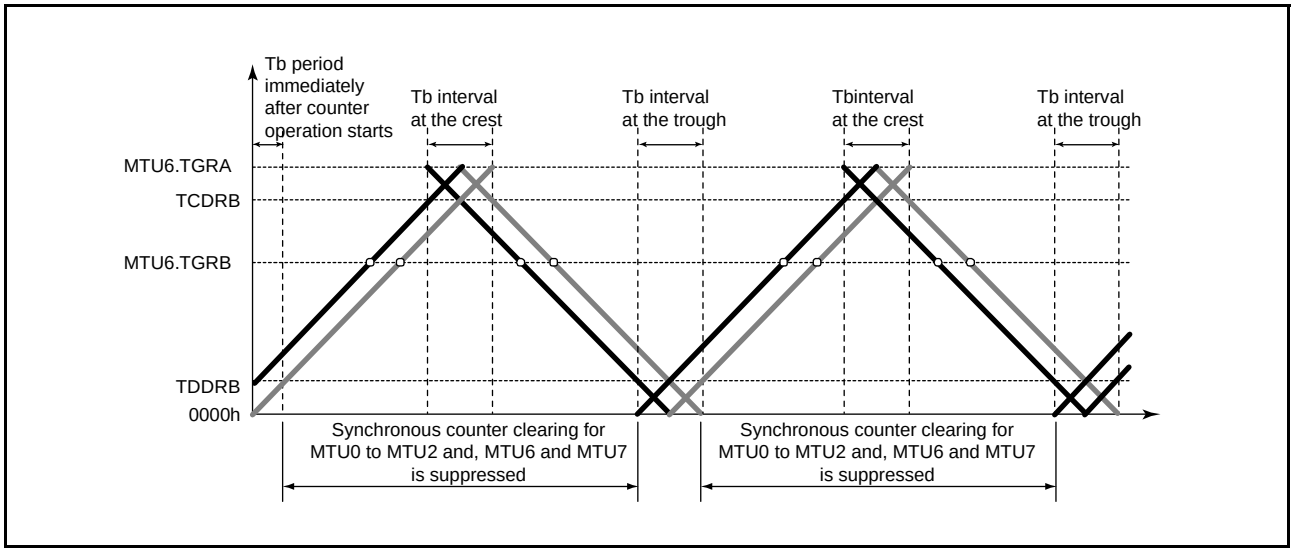


Figure 22.63 Synchronous Clearing-Suppressed Interval Specified by SCC Bit in TWCRB for MTU0, MTU1 and MTU2, and MTU6 and MTU7

- Example of Procedure for Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

An example of the procedure for suppressing synchronous counter clearing for MTU0 to MTU2, and MTU6 and MTU7 is shown in Figure 22.64.

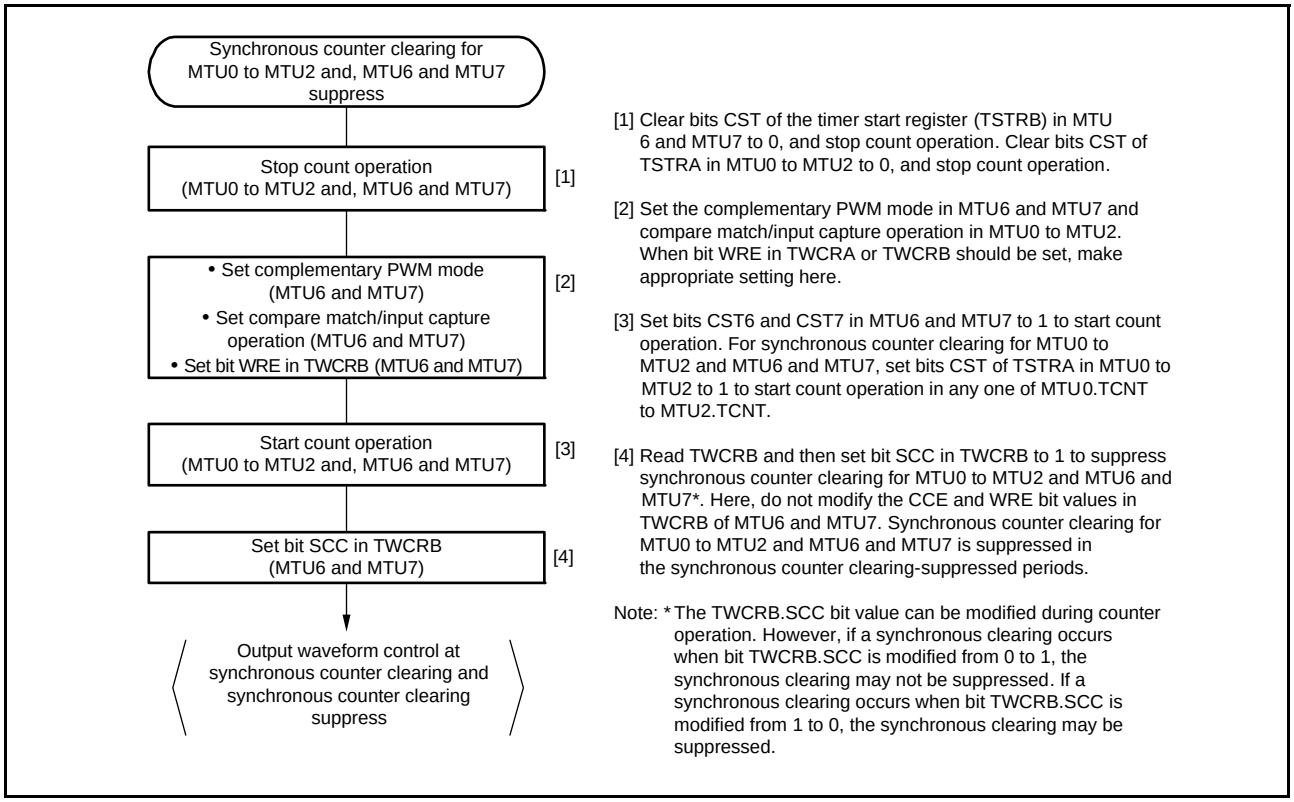


Figure 22.64 Example of Procedure for Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

- Examples of Suppression of Synchronous Counter Clearing for MTU 0 to MTU2, and MTU6 and MTU7

Figure 22.65 to Figure 22.68 show examples of operation in which MTU6 and MTU7 operate in complementary PWM mode and synchronous counter clearing for MTU 0 to MTU2, and MTU6 and MTU7 is suppressed by setting the SCC bit in TWCRB in MTU6 and MTU7 to 1. In the examples shown in Figure 22.65 to Figure 22.68, synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in Figure 22.57, respectively. In these examples, the WRE bit in TWCRB in MTU6 and MTU7 is set to 1.

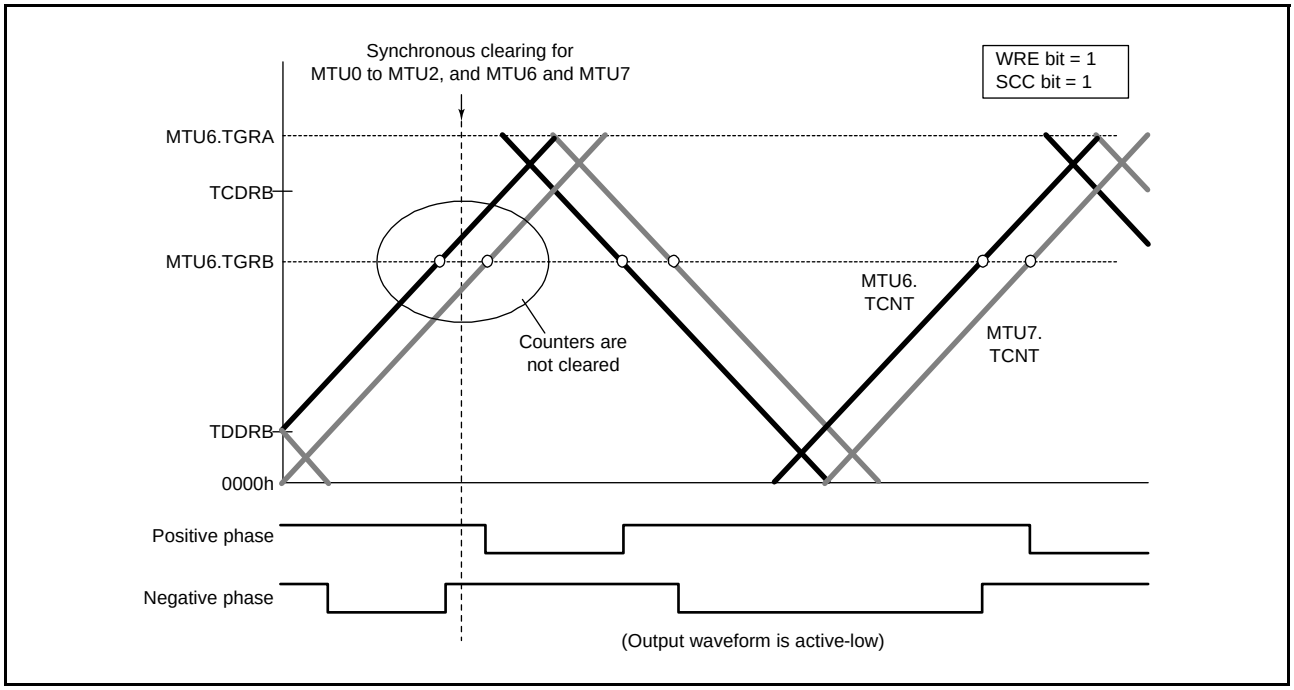


Figure 22.65 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 22.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

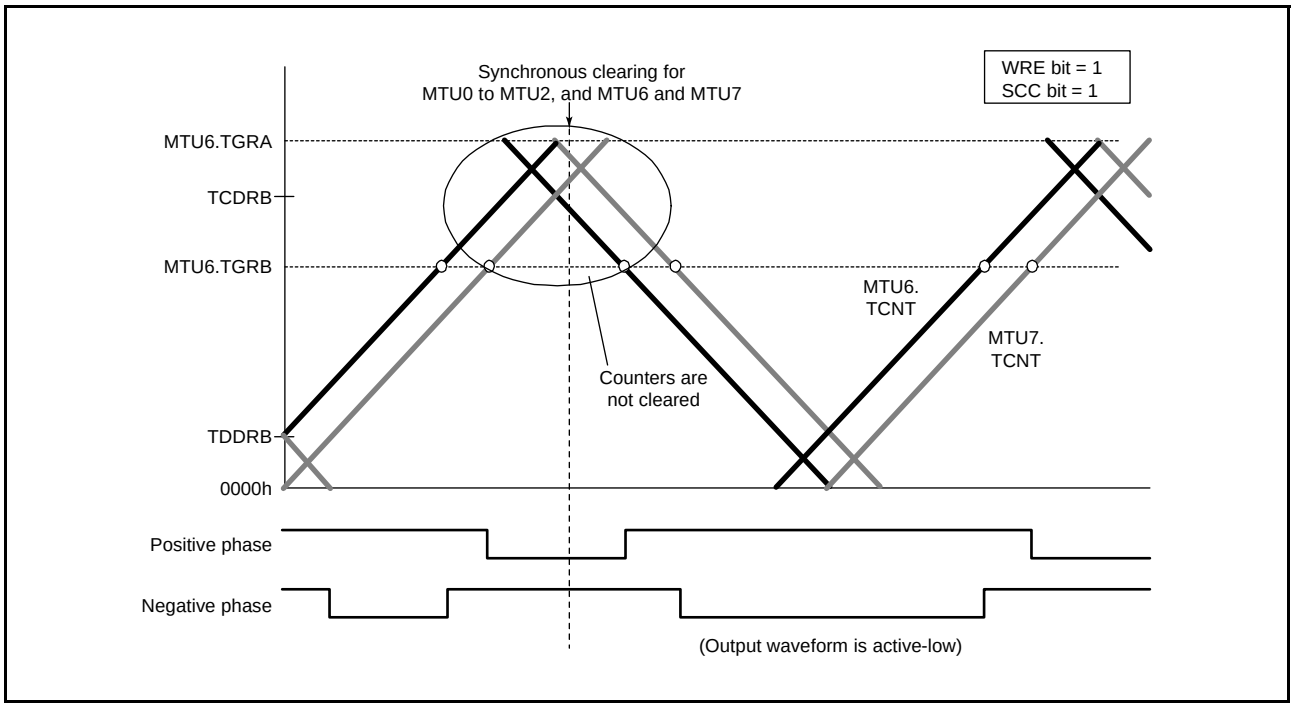


Figure 22.66 Example of Synchronous Clearing in Interval Tb at Crest (Timing (6) in Figure 22.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

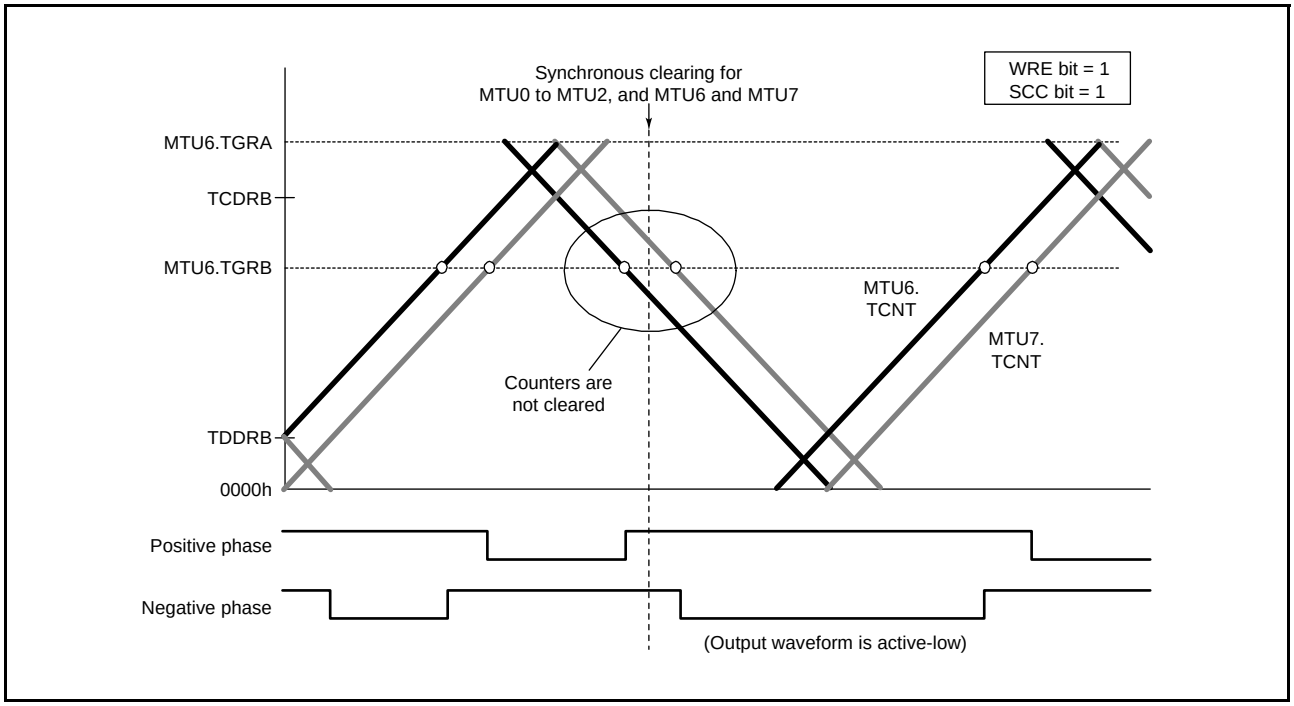


Figure 22.67 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 22.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

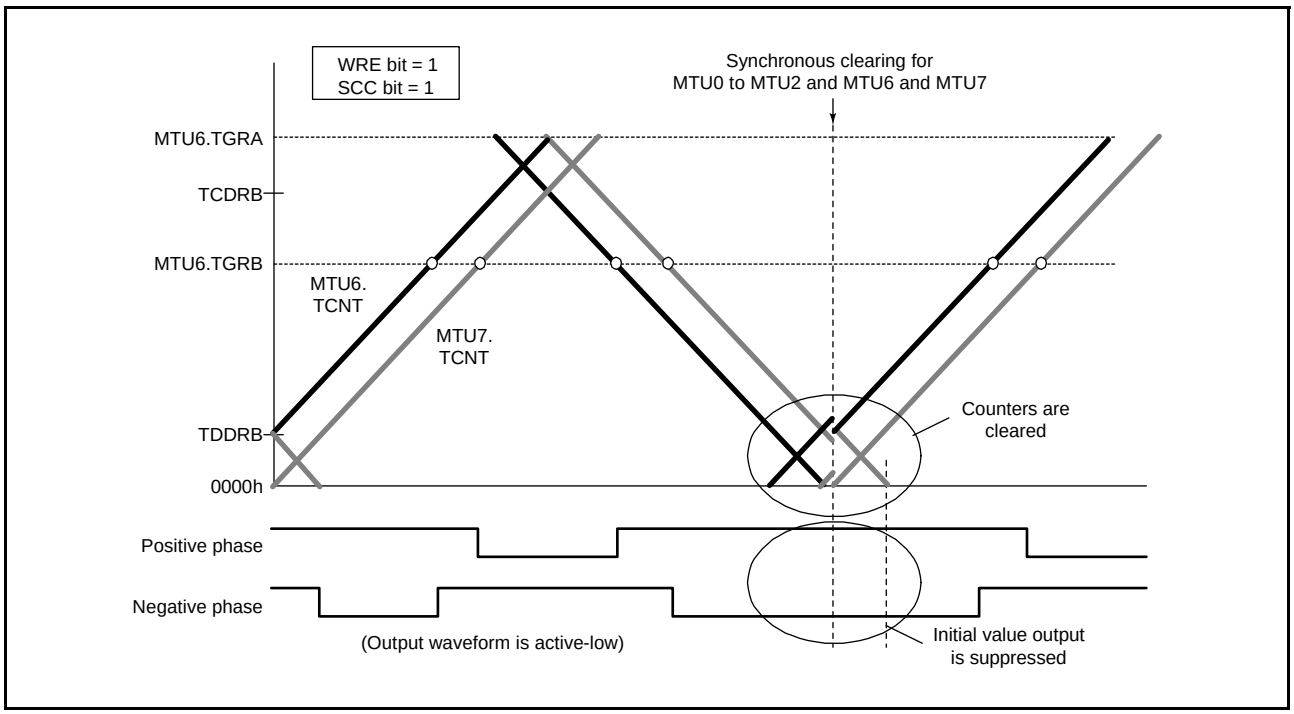


Figure 22.68 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 22.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

(p) Counter Clearing by MTU3.TGRA (MTU6.TGRA) Compare Match

In complementary PWM mode, MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) can be cleared by MTU3.TGRA (MTU6.TGRA) compare match when the CCE bit is set in the timer waveform control register (TWCRA or TWCRB).
Figure 22.69 illustrates an operation example.

Note 1. Use this function only in complementary PWM mode 1 (transfer at crest).
Note 2. Do not specify synchronous clearing by another channel (do not set the SYNC0 to SYNC4 or SYNC6 to SYNC7 bits in the timer synchronous register (TSYRA or TSYRB) to 1 or the CE0A to CE0D and CE1A to CE1D bits in the timer synchronous clear register (TSYCR) to 1).
Note 3. Do not set the PWM duty value to 0000h.
Note 4. Do not set the PSYE bit in timer output control register 1 (TOCR1A or TOCR1B) to 1.

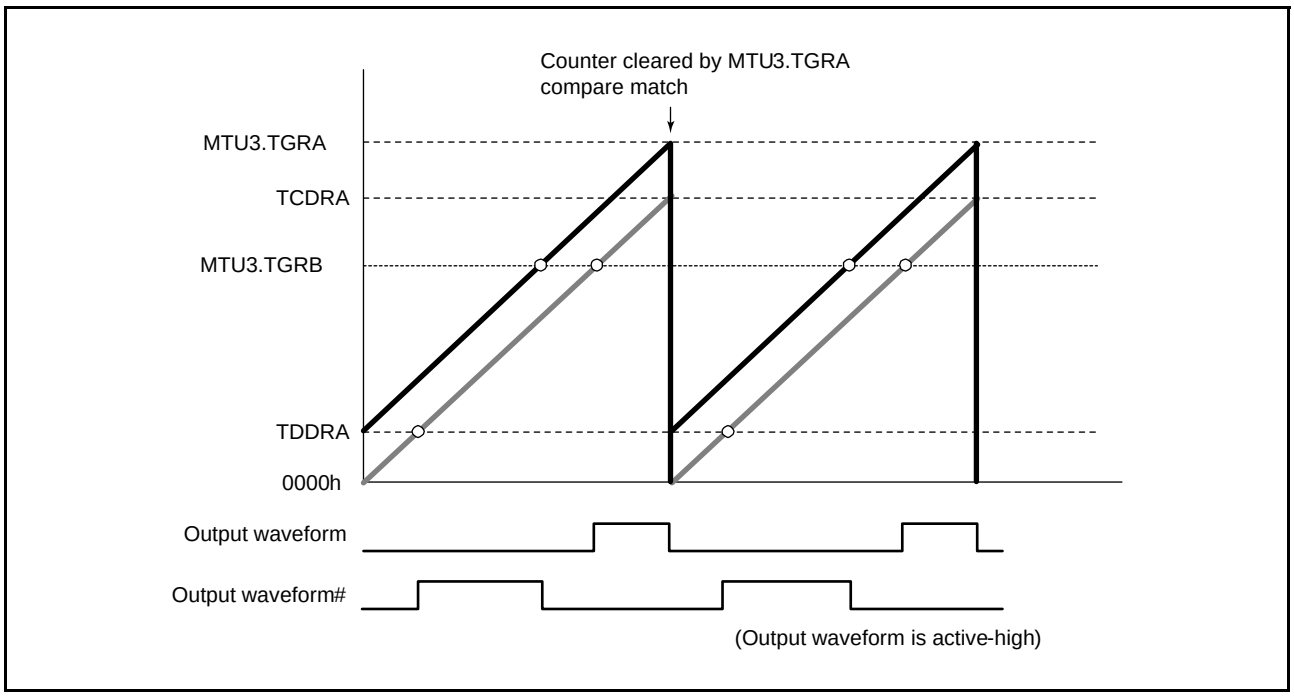


Figure 22.69 Example of Counter Clearing Operation by MTU3.TGRA Compare Match

(q) Example of Waveform Output for Driving AC Synchronous Motor (Brushless DC Motor)

In complementary PWM mode, a brushless DC motor can easily be controlled using the timer gate control register (TGCRA). Figure 22.70 to Figure 22.73 show examples of brushless DC motor driving waveforms created using TGCRA.

To switch the output phases for a 3-phase brushless DC motor by means of external signals detected with a Hall element, etc., clear the TGCRA.FB bit to 0. In this case, the external signals indicating the magnetic pole position should be input to timer input pins MTIOC0A, MTIOC0B, and MTIOC0C in MTU0 (make appropriate settings with the MPC and port mode registers (PMR) of the I/O ports). When an edge is detected at pin MTIOC0A, MTIOC0B, or MTIOC0C, the output on/off state is switched automatically.

When the TGCRA.FB bit is 1, the output on/off state is switched when the UF, VF, or WF bit in TGCRA is cleared to 0 or set to 1.

The driving waveforms are output from the 6-phase output pins for complementary PWM mode.

With this 6-phase output, while the output is turned on, chopping output is available through complementary PWM mode output function by setting the N bit or P bit in TGCRA to 1. When the N bit or P bit is 0, the level output is selected.

The active level of the 6-phase output (on output level) can be set with the OLSN and OLSP bits in the timer output control register 1A (TOCR1A) regardless of the setting of the N and P bits.

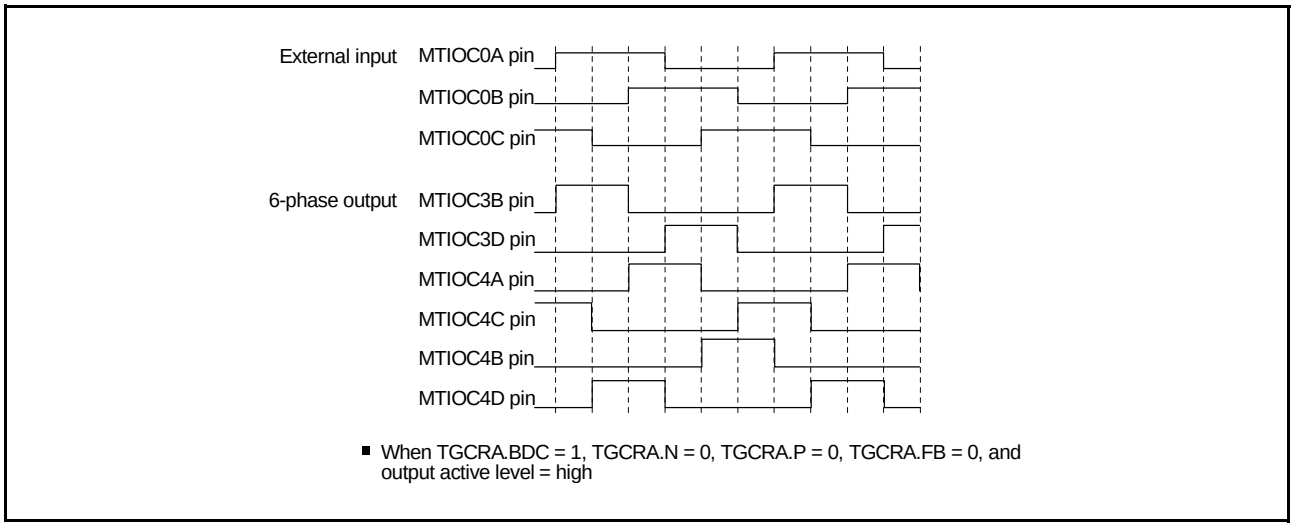


Figure 22.70 Example of Output Phase Switching by External Input (1)

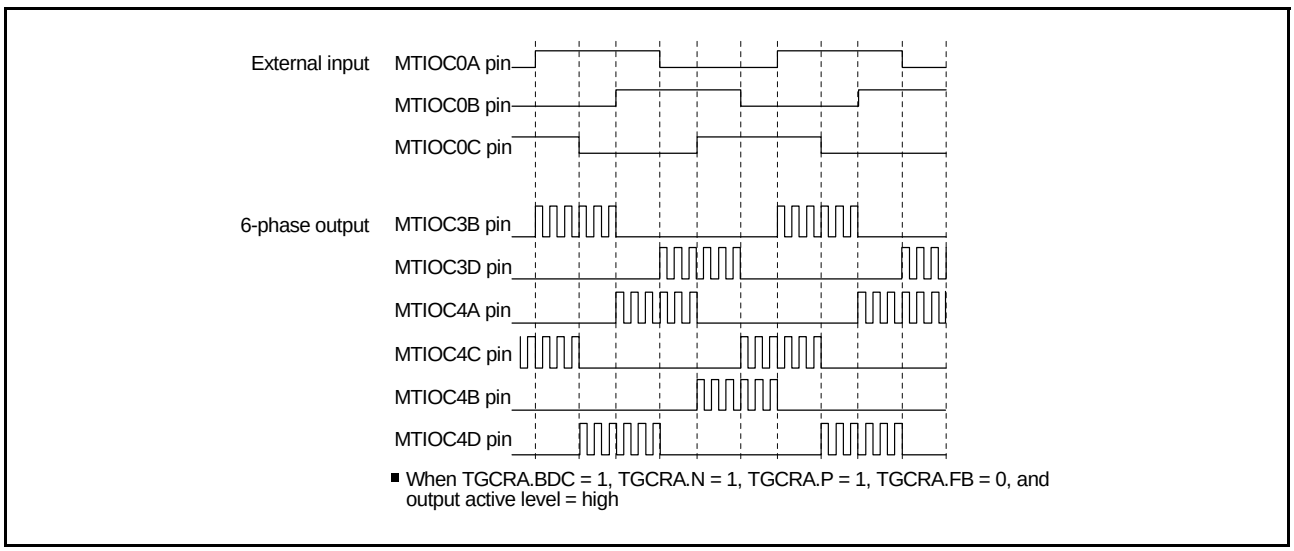


Figure 22.71 Example of Output Phase Switching by External Input (2)

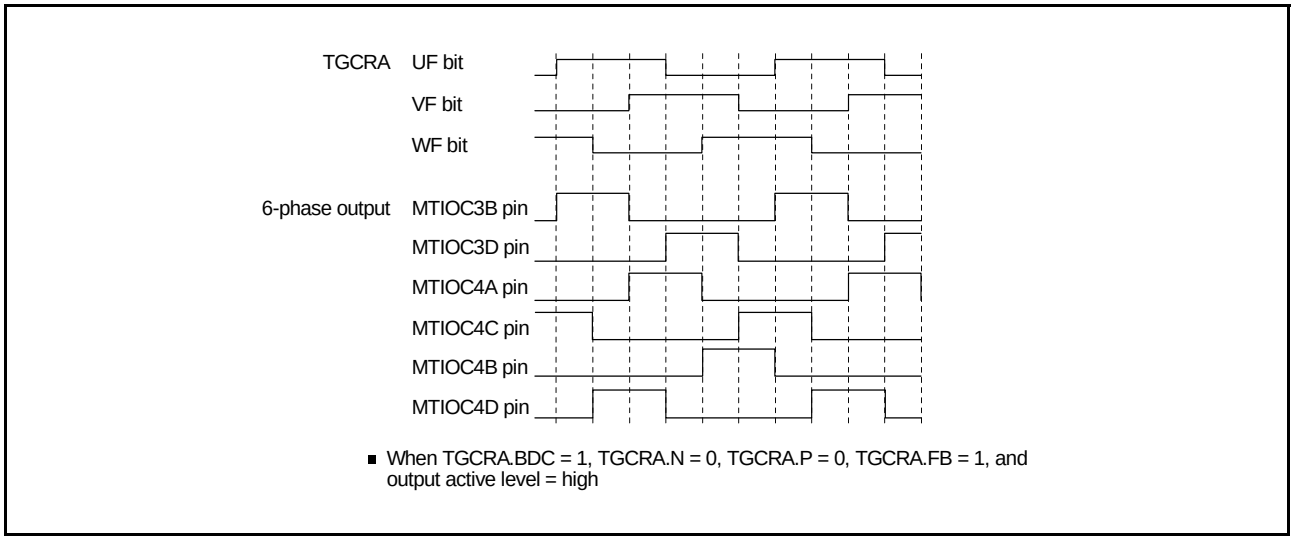


Figure 22.72 Example of Output Phase Switching through UF, VF, and WF Bit Settings (1)

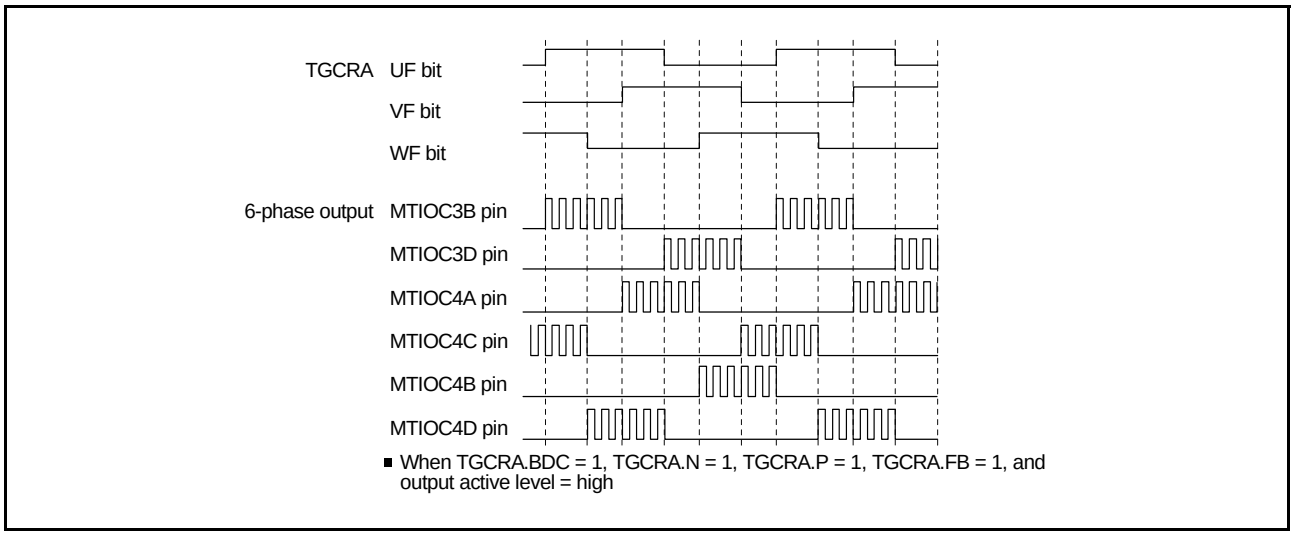


Figure 22.73 Example of Output Phase Switching through UF, VF, and WF Bit Settings (2)

(r) A/D Converter Start Request Setting

In complementary PWM mode, an A/D converter start request can be issued using MTU3.TGRA (MTU6.TGRA) compare match, MTU4.TCNT (MTU7.TCNT) underflow (trough), or compare match on a channel other than MTU3 and MTU4 (MTU6 and MTU7).
When start requests using MTU3.TGRA (MTU6.TGRA) compare match are specified, A/D conversion can be started at the crest of the MTU3.TCNT (MTU6.TCNT) count.
A/D converter start requests can be specified by setting the TTGE bit to 1 in the timer interrupt enable register (TIER).
To issue an A/D converter start request at an MTU4.TCNT (MTU7.TCNT) underflow (trough), set the TTGE2 bit in MTU4.TIER (MTU7.TIER) to 1.

(s) Double Buffer Function in Complementary PWM Mode

In complementary PWM mode 3 (transfer at the crest and trough), the PWM output setting resolution can be improved from ±2 to ±1 by setting the DRS bit in timer mode register 2 (TMDR2A or TMDR2B) to 1.
When setting buffer registers A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD), set also buffer registers B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF) at the same time. Each buffer register B should be set to the buffer register A value or (buffer register A value – 1). For details of the setting procedure, refer to section 22.3.8 (1)Example of Complementary PWM Mode Setting Procedure

Note 1. When a buffer register B is set to the buffer register A value, symmetric PWM waveforms are output. When a buffer register B is set to (buffer register A value – 1), asymmetric PWM waveforms are output.

Figure 22.74 shows an example of double buffer operation.
Each register data is transferred as follows.

- After MTU4.TGRD (buffer A) is written to, data is transferred from MTU4.TGRD (buffer A) to Temp3A (temporary A) and from MTU4.TGRF (buffer B) to Temp3B (temporary B).
- With timing (1) in the figure, data is transferred from Temp3A (temporary A) to MTU4.TGRB (compare).
- With timing (2) in the figure, data is transferred from Temp3B (temporary B) to MTU4.TGRB (compare).

In the crest interval (Tb interval at crest), the compare register and temporary register A are valid; in the trough interval (Tb interval at trough), the compare register and temporary register B are valid.

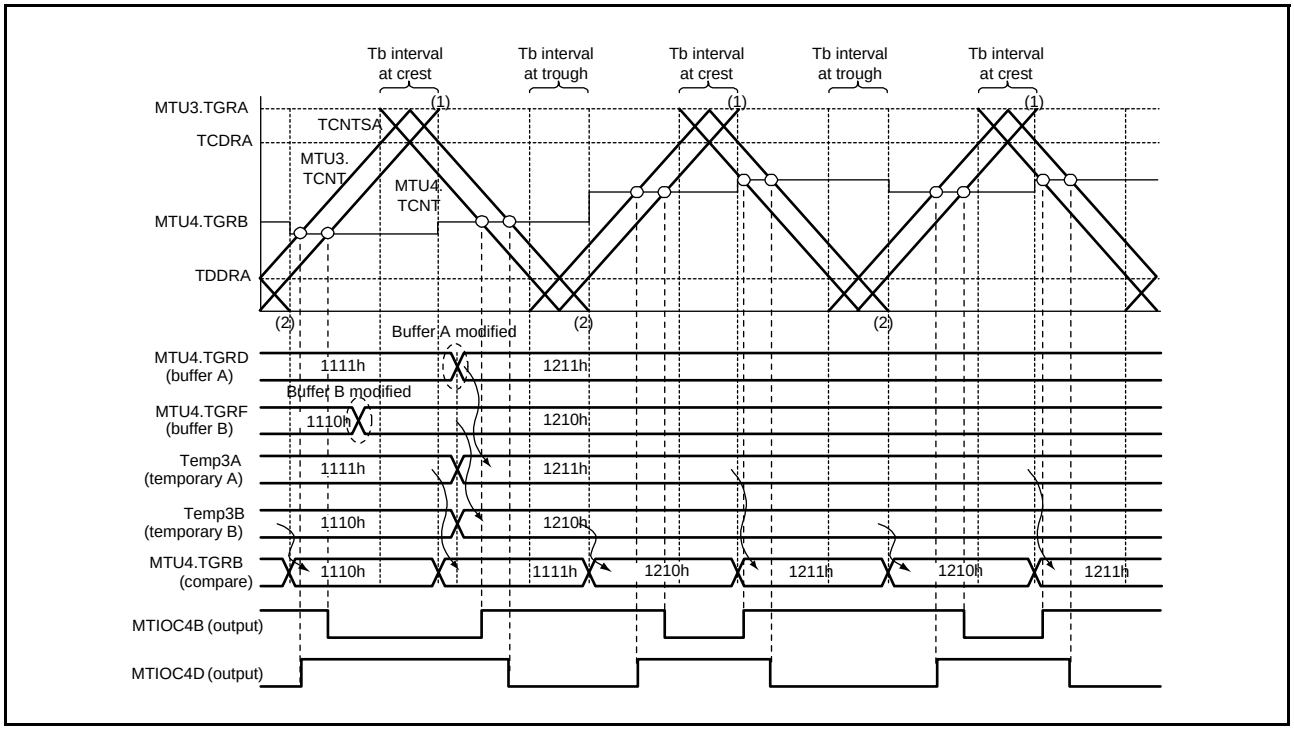


Figure 22.74 Example of Double Buffer Operation

Figure 22.75 shows an example when the buffer write value is smaller than the TDDRA value, and Figure 22.76 shows an example when the write value is greater than TCDRA.
In the crest interval, the output is controlled according to the compare match with the compare register or temporary register A; in the trough interval, the output is controlled according to the compare match with the compare register or temporary register B.

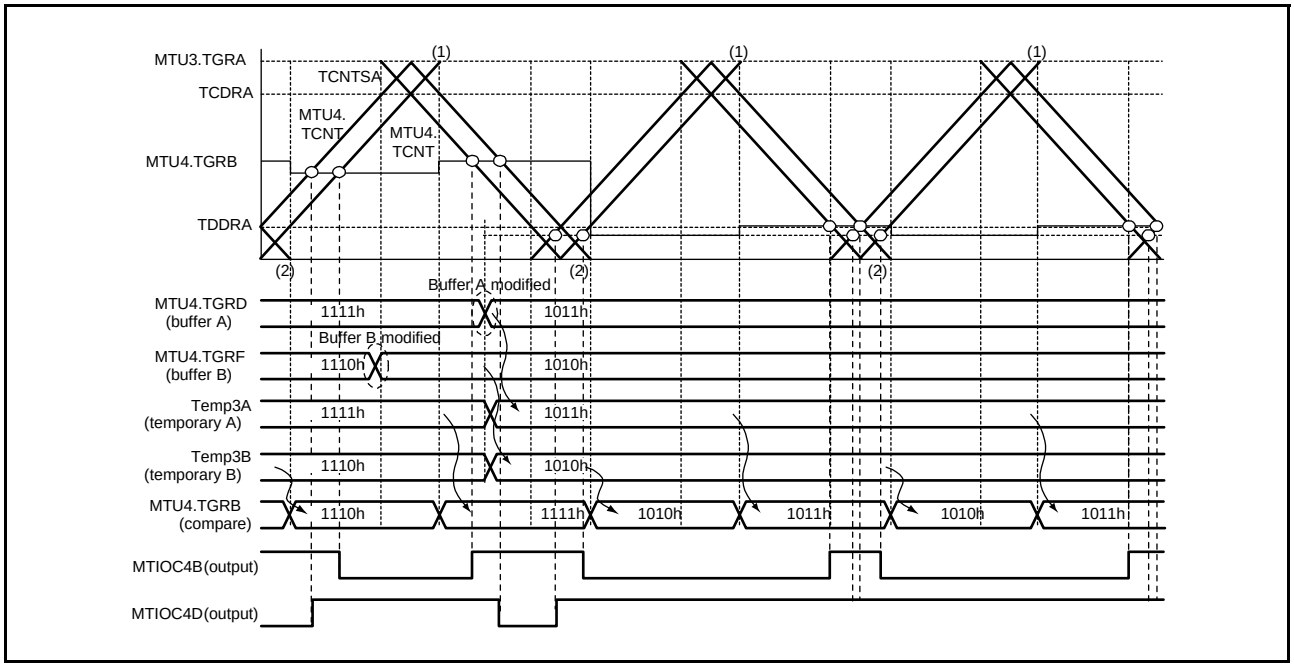


Figure 22.75 Example of Double Buffer Operation (Buffer Write Value is Smaller than TDDRA)

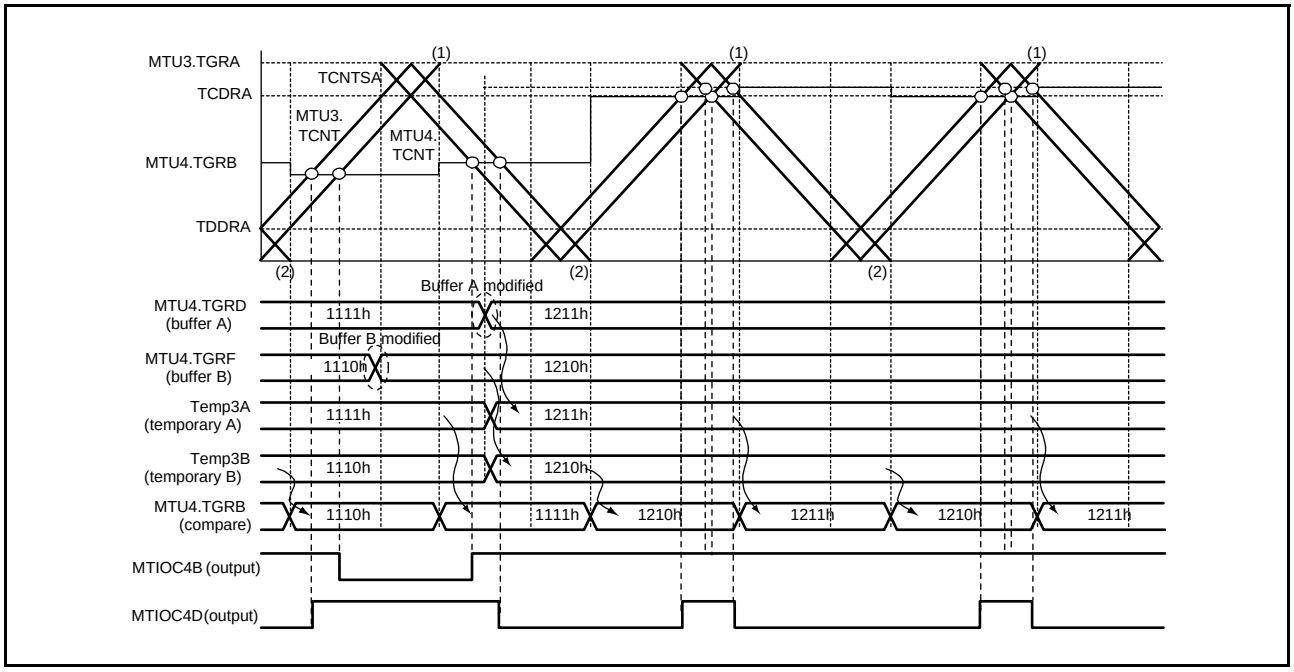


Figure 22.76 Example of Double Buffer Operation (Buffer Write Value is Greater than TCDRA)

(3) Interrupt Skipping Function 1 in Complementary PWM Mode

Interrupts TGIA3 (TGIA6) (at the crest) and TCIV4 (TCIV7) (at the trough) in MTU3 and MTU4 (MTU6 and MTU7) can be skipped up to seven times by making settings in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B).

Transfers from a buffer register to a temporary register or a compare register can be skipped in coordination with interrupt skipping by making settings in the timer buffer transfer register (TBTERA or TBTERB). For the linkage with buffer registers, refer to description (c), Buffer Transfer Control Linked with Interrupt Skipping, below.

A/D converter start requests generated by the A/D converter start request delaying function can also be skipped in coordination with interrupt skipping by making settings in the timer A/D converter request control register (MTU4.TADCR or MTU7.TADCR). For the linkage with the A/D converter start request delaying function, refer to section 22.3.9, A/D Converter Start Request Delaying Function.

The timer interrupt skipping setting register 1 (TITCR1A or TITCR1B) should be set while interrupt skipping function 1 is selected by setting the TITM bit to 0 in the timer interrupt skipping mode register (TITMRA or TITMRB) and TGIA3 (TGIA6) and TCIV4 (TCIV7) interrupt requests are disabled by the settings of MTU3.TIER and MTU4.TIER (MTU6.TIER and MTU7.TIER) under the conditions in which TGFA3 (TGFA6) and TCFV4 (TCFV7) flag settings by compare match never occur in TITCR1A (TITCR1B). Before changing the skipping count, be sure to clear the T3AEN (T6AEN) and T4VEN (T7VEN) bits to 0 to clear the skipping counter.

(a) Example of Interrupt Skipping Function 1 Setting Procedure

Figure 22.77 shows an example of the interrupt skipping function 1 setting procedure. Figure 22.78 shows the periods during which interrupt skipping count can be changed.

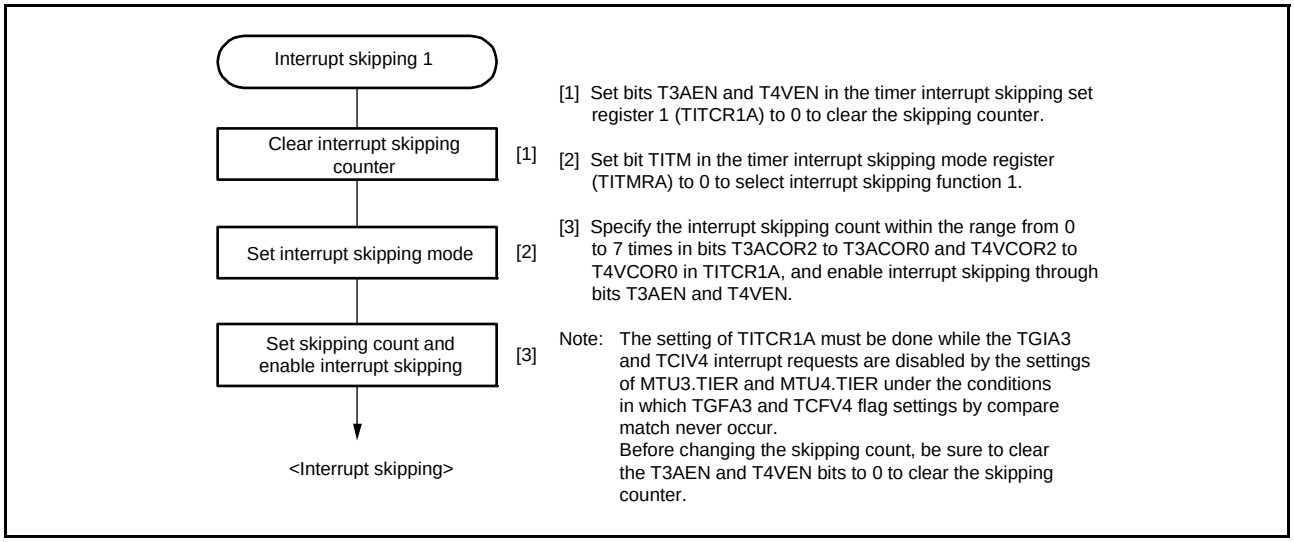


Figure 22.77 Example of Interrupt Skipping Function 1 Setting Procedure

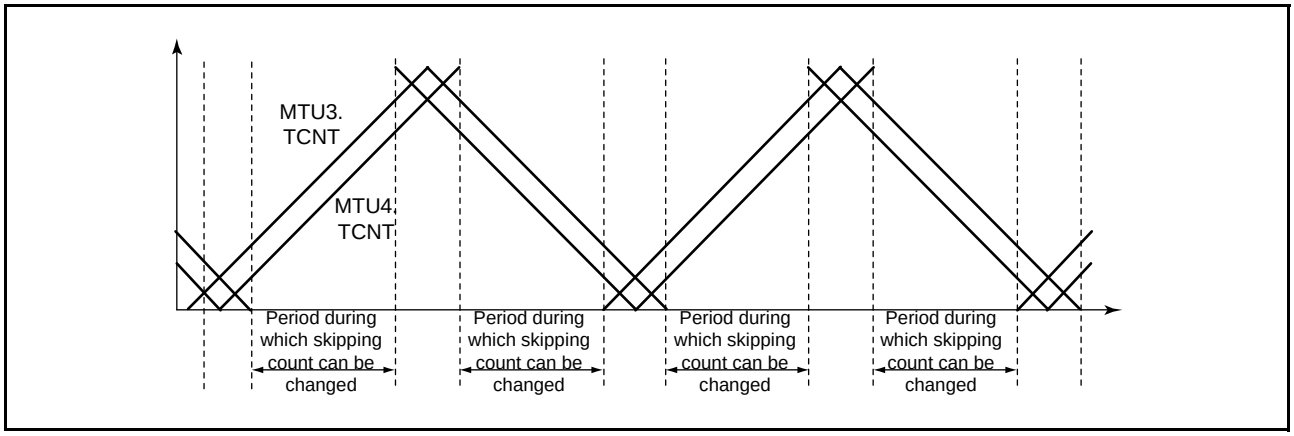


Figure 22.78 Periods during which Interrupt Skipping Count can be Changed

(b) Example of Interrupt Skipping Function 1

Figure 22.79 shows an example of TGIA3 (TGIA6) interrupt skipping in which the interrupt skipping count is set to three by the T3ACOR (T6ACOR) bits and the T3AEN (T6AEN) bit is set to 1 in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B).

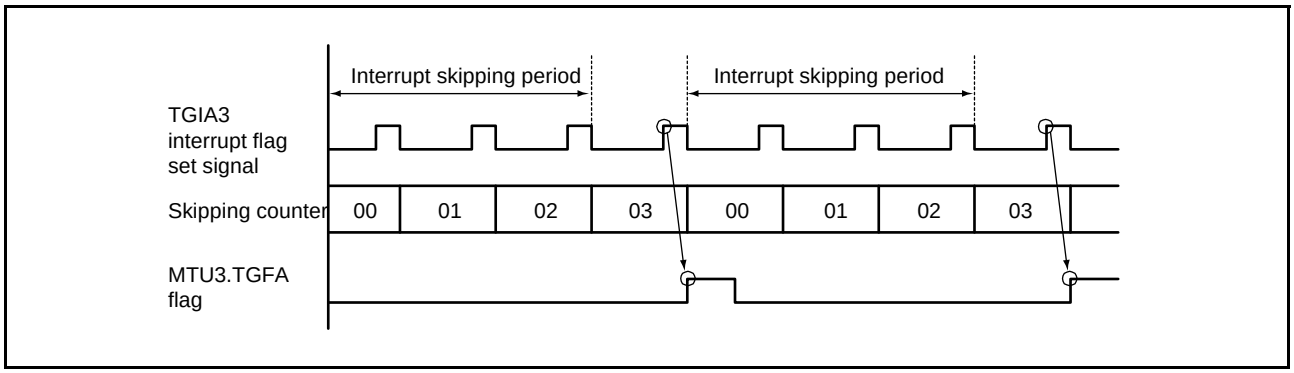


Figure 22.79 Example of Interrupt Skipping Function 1

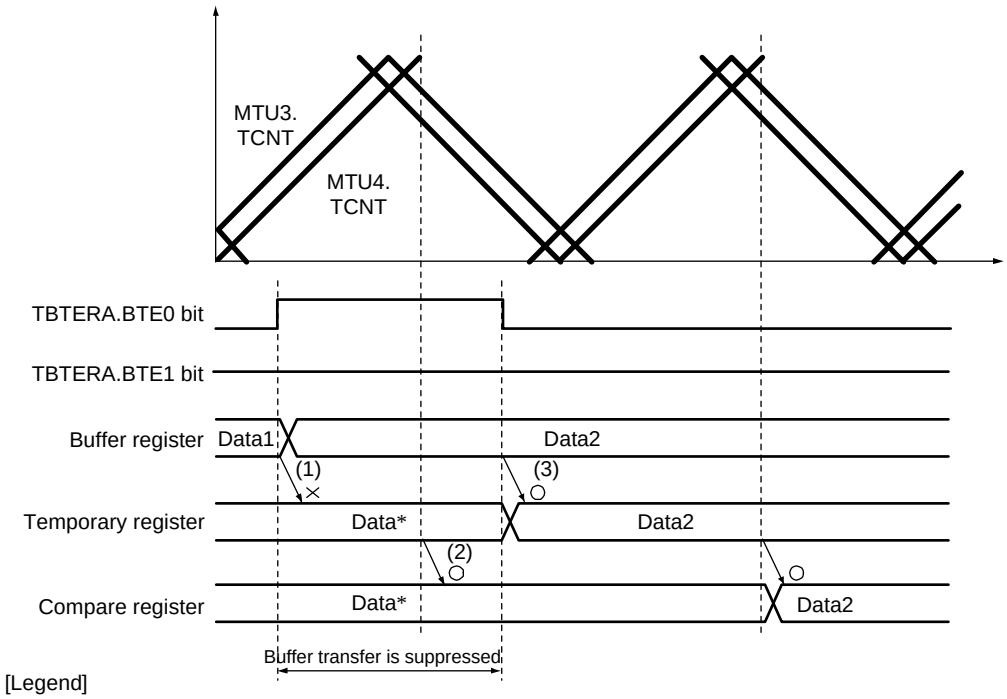
(c) Buffer Transfer Control Linked with Interrupt Skipping

In complementary PWM mode, whether to transfer data from a buffer register to a temporary register and whether to link the transfer with interrupt skipping can be specified with the BTE[1:0] bits in the timer buffer transfer set register (TBTERA or TBTERB).

Figure 22.80 shows an example of operation when buffer transfer is disabled (BTE[1:0] = 01b). While this setting is valid, data is not transferred from the buffer register to the temporary register.

Figure 22.81 shows an example of operation when buffer transfer is linked with interrupt skipping (BTE[1:0] = 10b). While this setting is valid, data is not transferred from the buffer register outside the buffer transfer-enabled period. Note that the buffer transfer-enabled period depends on the T3AEN (T6AEN) and T4VEN (T7VEN) bit settings in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B). Figure 22.82 shows the relationship between the T3AEN (T6AEN) and T4VEN (T7VEN) bit settings in TITCR1A (TITCR1B) and buffer transfer-enabled period.

Note 1. This function must always be used in combination with interrupt skipping function 1.
When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), make sure that buffer transfer is not linked with interrupt skipping (clear the BTE1 bit in TBTERA or TBTERB to 0).
If buffer transfer is linked with interrupt skipping while interrupt skipping is disabled, buffer transfer is never performed.



[Legend]

(1) No data is transferred from the buffer register to the temporary register in the buffer transfer-disabled period (bits BTE[1:0] in TBTERA are set to 01b).
(2) Data is transferred from the temporary register to the compare register even in the buffer transfer-disabled period.
(3) After buffer transfer is enabled, data is transferred from the buffer register to the temporary register.

Note: * When buffer transfer at the crest is selected.

Figure 22.80 Example of Operation when Buffer Transfer is Disabled (BTE[1:0] = 01b)

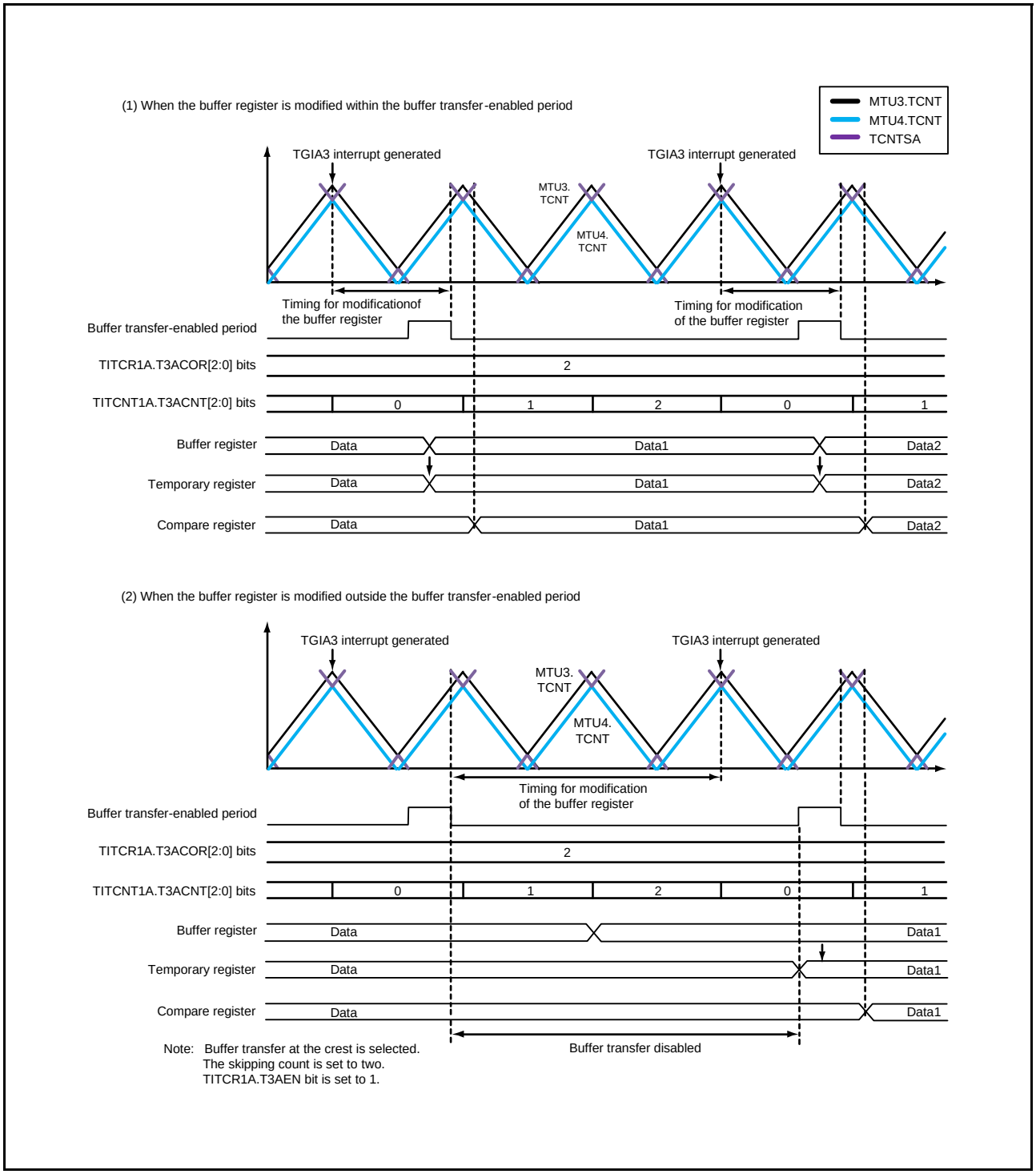


Figure 22.81 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b)

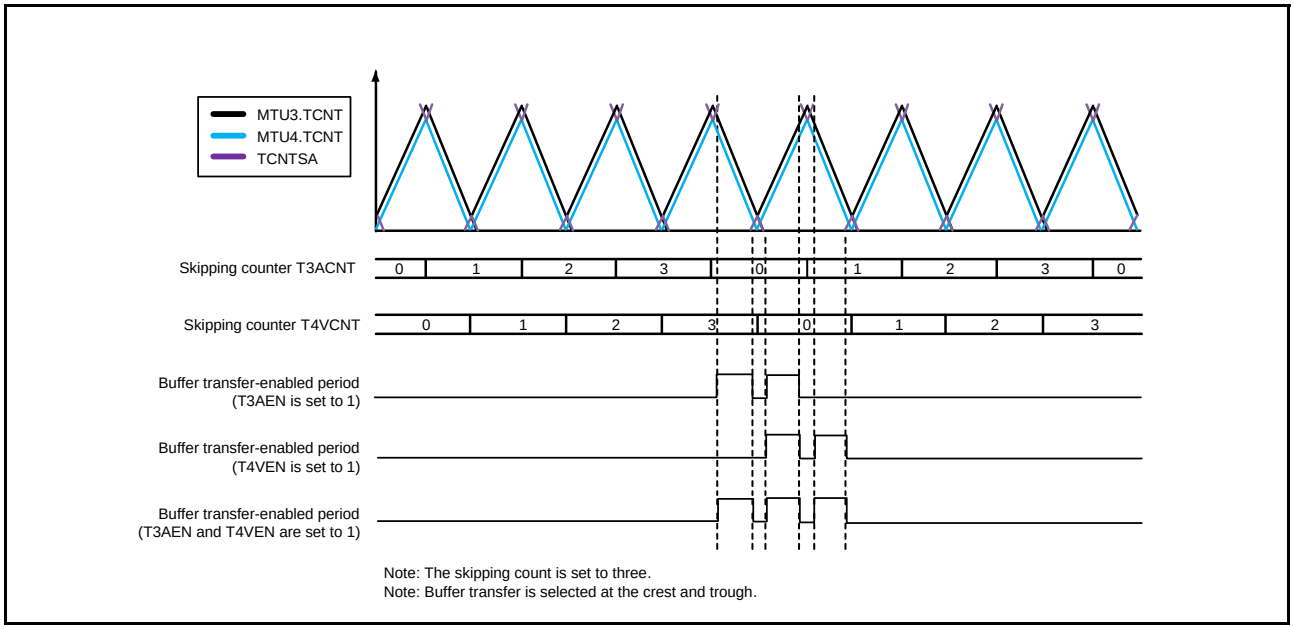


Figure 22.82 Relationship between Bits T3AEN and T4VEN in TITCR1A and Buffer Transfer-Enabled Period

(4) Complementary PWM Mode Output Protection Functions

The MTU3 provides the following protection functions for complementary PWM mode output.

(a) Register and Counter Miswrite Prevention Function

With the exception of the buffer registers, which can be modified at any time, access by the CPU can be enabled or disabled for the mode registers, control registers, compare registers, and counters used in complementary PWM mode by means of the RWE bit in the timer read/write enable register (TRWERA or TRWERB). The applicable registers are some of the registers in MTU3, MTU4, MTU6, and MTU7 shown below:
43 registers in total
MTU3.TCR, MTU4.TCR, MTU3.TMDR1, MTU4.TMDR1, MTU3.TIORH,
MTU4.TIORH, MTU3.TIORL, MTU4.TIORL, MTU3.TIER, MTU4.TIER,
MTU3.TCNT, MTU4.TCNT, MTU3.TGRA, MTU4.TGRA, MTU3.TGRB, MTU4.TGRB,
TOERA, TOCR1A, TOCR2A, TGCRA, TCDRA, TDDRA
MTU6.TCR, MTU7.TCR, MTU6.TMDR1, MTU7.TMDR1, MTU6.TIORH, MTU7.TIORH,
MTU6.TIORL, MTU7.TIORL, MTU6.TIER, MTU7.TIER, MTU6.TCNT, MTU7.TCNT,
MTU6.TGRA, MTU7.TGRA, MTU6.TGRB, MTU7.TGRB,
TOERB, TOCR1B, TOCR2B, TCDRB, and TDDRB
This function can disable CPU access to the mode registers, control registers, and counters to prevent miswriting due to CPU runaway. In the access-disabled state, the applicable registers are read as undefined and writing to these registers is ignored.

(b) Halting of PWM Output by External Signal

The 6-phase PWM output pins can be set to the high-impedance state automatically by inputting specified external signals.
See section 23, Port Output Enable 3 (POE3), for details.

(c) Halting of PWM Output when Oscillator is Stopped

Upon detecting that the clock input to this MCU has stopped, the 6-phase PWM output pins are automatically set to the high-impedance state. Note that the pin states are not guaranteed when the clock is restarted.
See section 10.4, Oscillation Stop Detection Function.

22.3.9 A/D Converter Start Request Delaying Function

A/D converter start requests can be issued in MTU4 or MTU7 by making settings in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR), timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB), and timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB).

The A/D converter start request delaying function compares MTU4.TCNT with MTU4.TADCORA or MTU4.TADCORB (MTU7.TCNT with MTU7.TADCORA or MTU7.TADCORB), and when their values match, the function issues a respective A/D converter start request (TRG4AN or TRG4BN (TRG7AN or TRG7BN)).

A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be skipped in coordination with interrupt skipping by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in MTU4.TADCR (the ITA6AE, ITA7VE, ITB6AE, and ITB7VE bits in MTU7.TADCR).

(1) Example of Procedure for Specifying A/D Converter Start Request Delaying Function

Figure 22.83 shows an example of procedure for specifying the A/D converter start request delaying function.

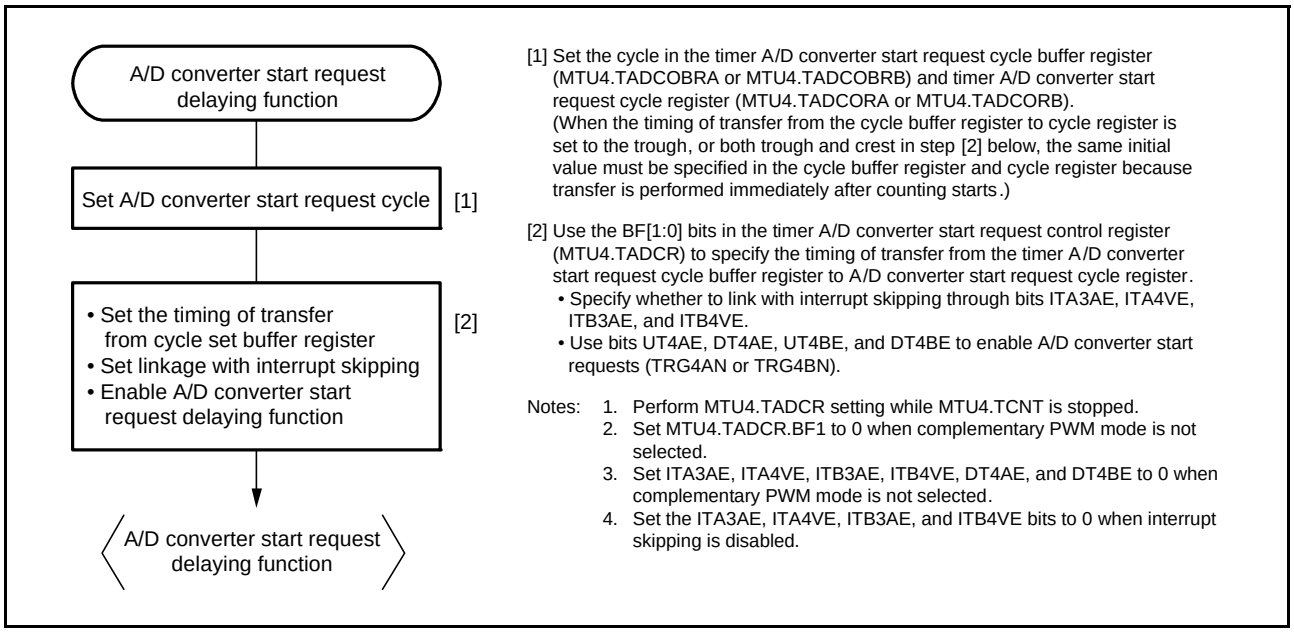


Figure 22.83 Example of Procedure for Specifying A/D Converter Start Request Delaying Function

(2) Basic Example of A/D Converter Start Request Delaying Function Operation

Figure 22.84 shows a basic example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when the trough of MTU4.TCNT (MTU7.TCNT) is specified for the buffer transfer timing and an A/D converter start request signal is output during MTU4.TCNT (MTU7.TCNT) down-counting.

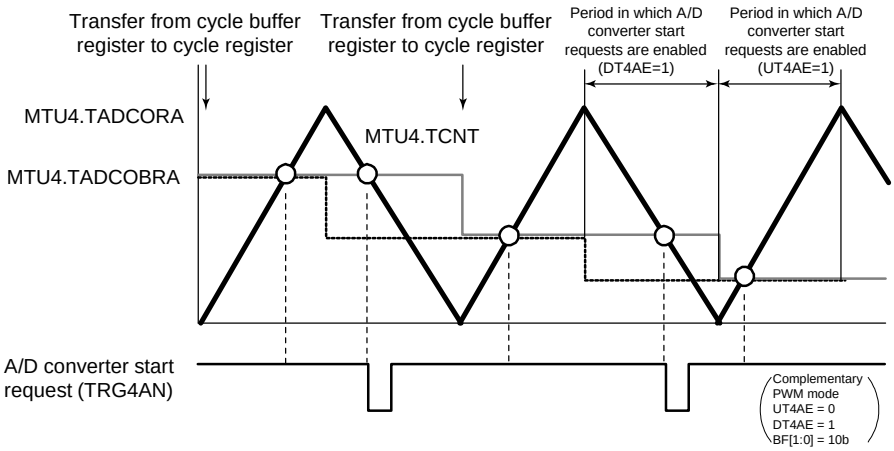


Figure 22.84 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation

(3) A/D converter Start Request Enabled Interval

When the MTU4.TCNT (MTU7.TCNT) counter and the MTU4.TADCORA or MTU4.TADCORB(MTU7.TADCORA or MTU7.TADCORB) register matches within the period enabled by the UT4AE and UT4BE (UT7AE and UT7BE) bits, the corresponding A/D converter start request (TRG4AN or TRG4BN) is issued.

When the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTU4.TCNT (MTU7.TCNT) upcounting (0 ≤ MTU4.TCNT (MTU7.TCNT) ≤ TCDR - 1). When the DT4AE and DT4BE (DT7AE and DT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, A/D converter start requests are enabled during MTU4.TCNT (MTU7.TCNT) down-counting (TCDR ≥ MTU4.TCNT (MTU7.TCNT) ≥ 1). See Figure 22.84.

(4) Buffer Transfer

The data in the timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB) is updated by writing data to the timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB). Data is transferred from the buffer registers to the respective cycle set registers at the timing selected with the BF[1:0] bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).
In complementary PWM mode, data is also transferred from the timer A/D converter start request cycle set buffer registers to the timer A/D converter start request cycle set registers when timer general register D (MTU4.TGRD or MTU7.TGRD) is updated.
There are notes on the timing for transferring data when using buffer transfer in complementary PWM mode.
For details, section 22, Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode.
In modes other than complementary PWM mode, set the BF1 bit in the MTU4.TADCR (MTU7.TADCR) register to 0.

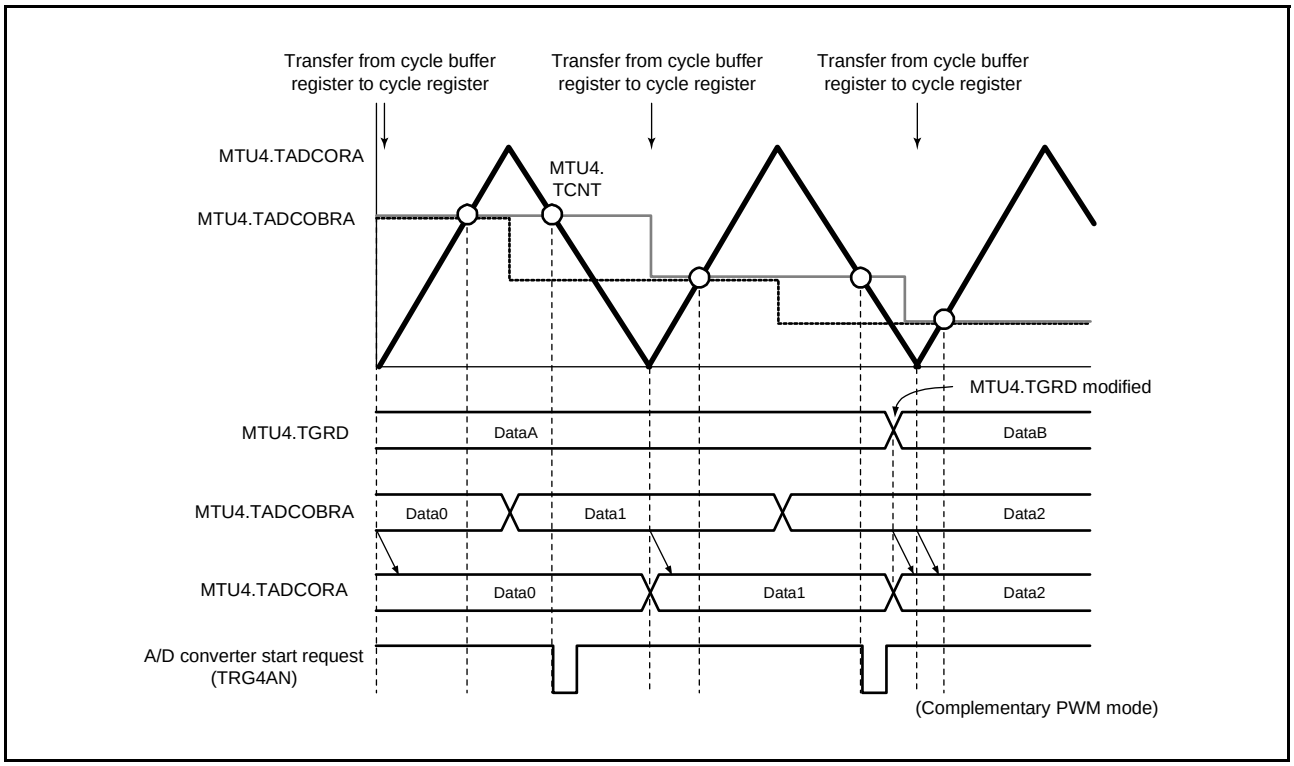


Figure 22.85 Example of A/D Converter Start Request Signal (TRG4AN) and Buffer Transfer Operation

(5) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1

In complementary PWM mode, A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be issued in coordination with interrupt skipping 1 by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).

In modes other than complementary PWM mode, do not use the A/D converter start request delaying function linked with the interrupt skipping function.

Set the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the MTU4.TADCR (MTU7.TADCR) register to 0.

Figure 22.86 shows an example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and down-counting and A/D converter start requests are linked with interrupt skipping 1.

Figure 22.87 shows another example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and A/D converter start requests are linked with interrupt skipping 1.

Note: • This function should be used in combination with interrupt skipping 1.
When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits in the timer interrupt skipping set register (TITCR1A (TITCR1B)) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), make sure that A/D converter start requests are not linked with interrupt skipping 1 (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the timer A/D converter start request control register (MTU4.TADCR (MTU7.TADCR)) to 0).
When this function is used, MTU4.TADCORA and MTU4.TADCORB (MTU7.TADCORA and MTU7.TADCORB) should be set with the value ranging 0002h to the value set in TCDRA minus 2 (value set in TCDRB minus 2).

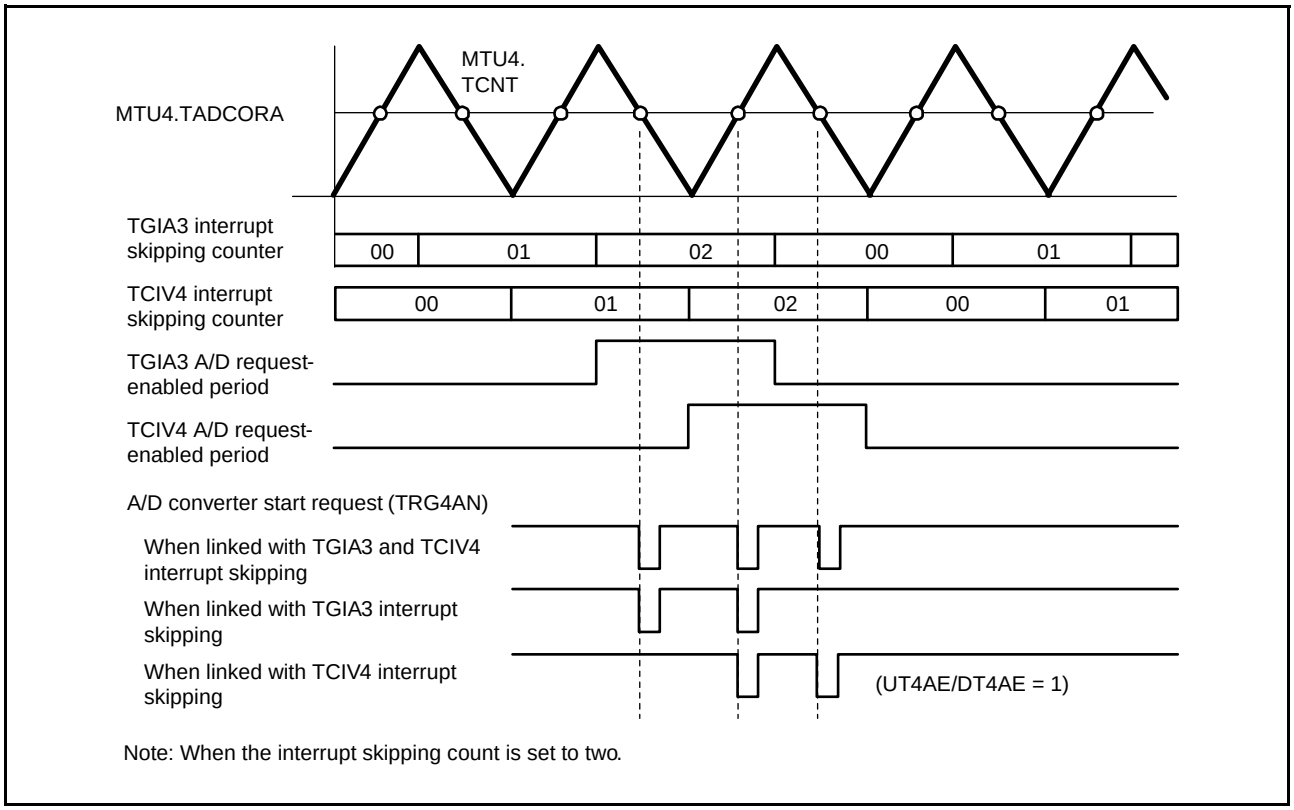


Figure 22.86 Example of A/D Converter Start Request Signal (TRG4AN) Operation Linked with Interrupt Skipping Function 1 (UT4AE and DT4AE = 1)

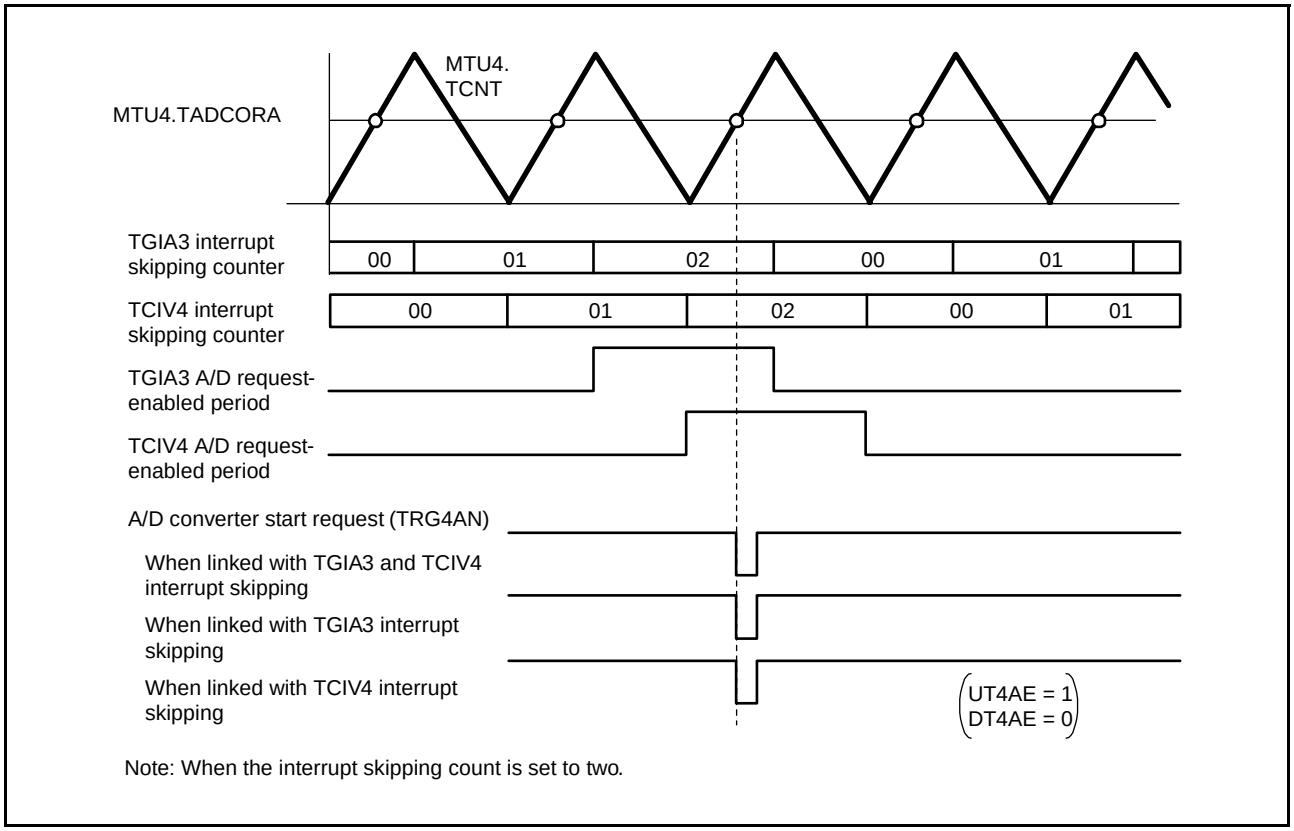


Figure 22.87 Example of A/D Converter Start Request Signal (TRG4AN) Operation Linked with Interrupt Skipping Function 1 (UT4AE = 1, DT4AE = 0)

(6) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 2

By setting the TITM bit to 1 in the timer interrupt skipping mode register (TITMRA or TITMRB), the counter starts down-counting from the value (0 to 7) set in the TRG4COR[2:0] (TRG7COR[2:0]) bits in timer interrupt skipping set register 2 (TITCR2A (TITCR2B)) every time an A/D converter start trigger (TGR4AN or TRG4BN (TGR7AN or TRG7BN)) is generated. When the counter value reaches 0 and is reloaded, the TRG4AN and TRG4BN (TRG7AN and TRG7BN) interrupts become valid and an A/D converter start request signal (TRG4ABN (TRG7ABN)) is output. This function is valid only when the A/D converter request delaying function is enabled.

(a) Example of Procedure for Setting Interrupt Skipping Function 2

Figure 22.88 shows an example of procedure for setting interrupt skipping function 2.

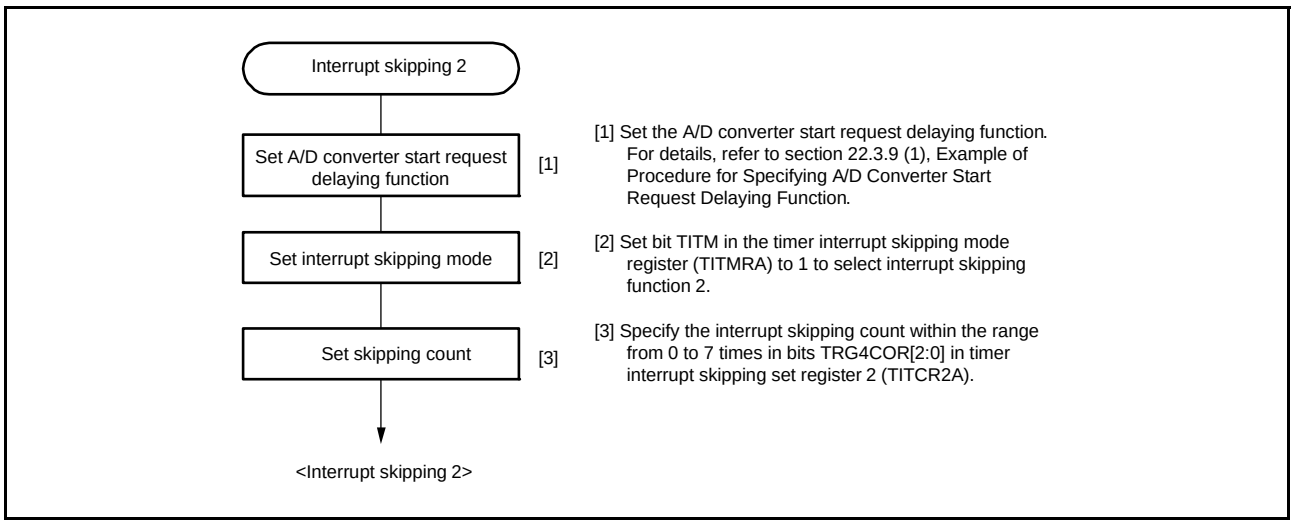


Figure 22.88 Example of Procedure for Setting Interrupt Skipping Function 2

(b) Example of Interrupt Skipping Function 2 Operation

Figure 22.89 shows an example of interrupt skipping 2 operation.

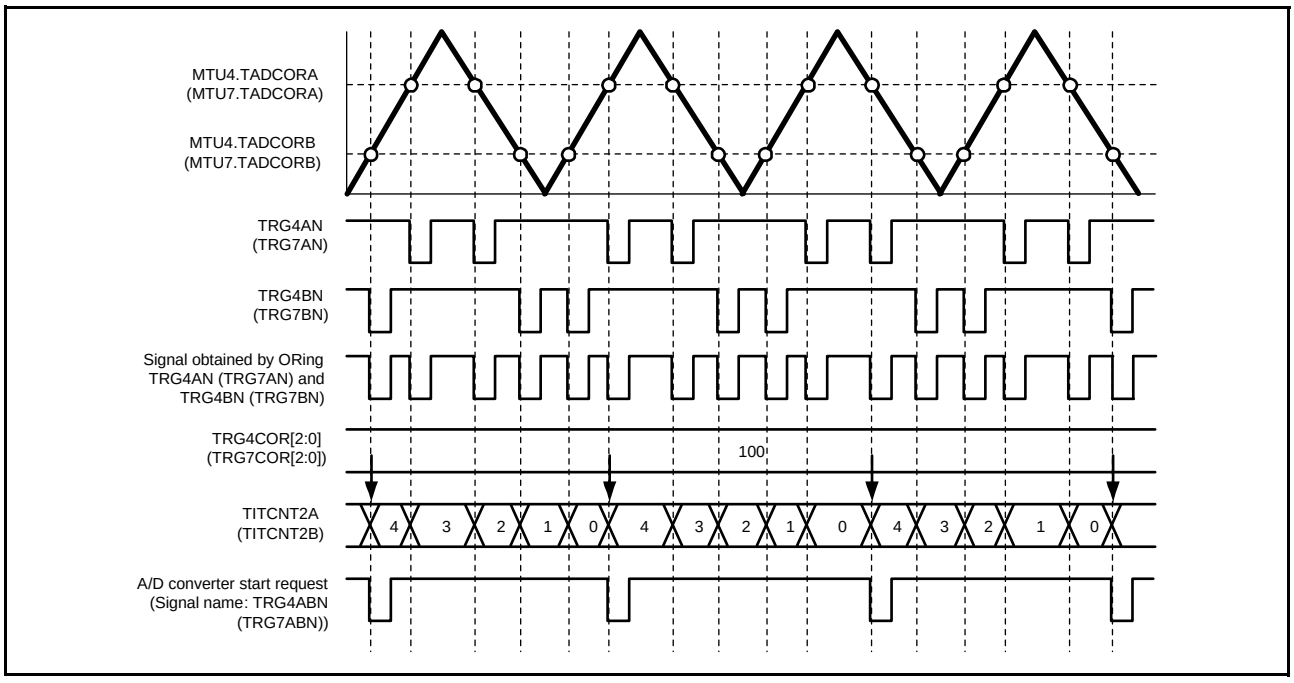


Figure 22.89 Example of Interrupt Skipping 2 Operation (Skipping Count is Set to Four)

22.3.10 Synchronous Operation of MTU0 to MTU4 and MTU6 and MTU7

(1) Synchronous Counter Start for MTU0 to MTU4 and MTU6 and MTU7

The counters in MTU0 to MTU4 and MTU6 and MTU7 can be started synchronously by making the TCSYSTR settings.

(a) Example of Procedure for Setting Synchronous Counter Start for MTU0 to MTU 4 and MTU6 and MTU7

Figure 22.90 shows an example of synchronous counter start setting procedure.

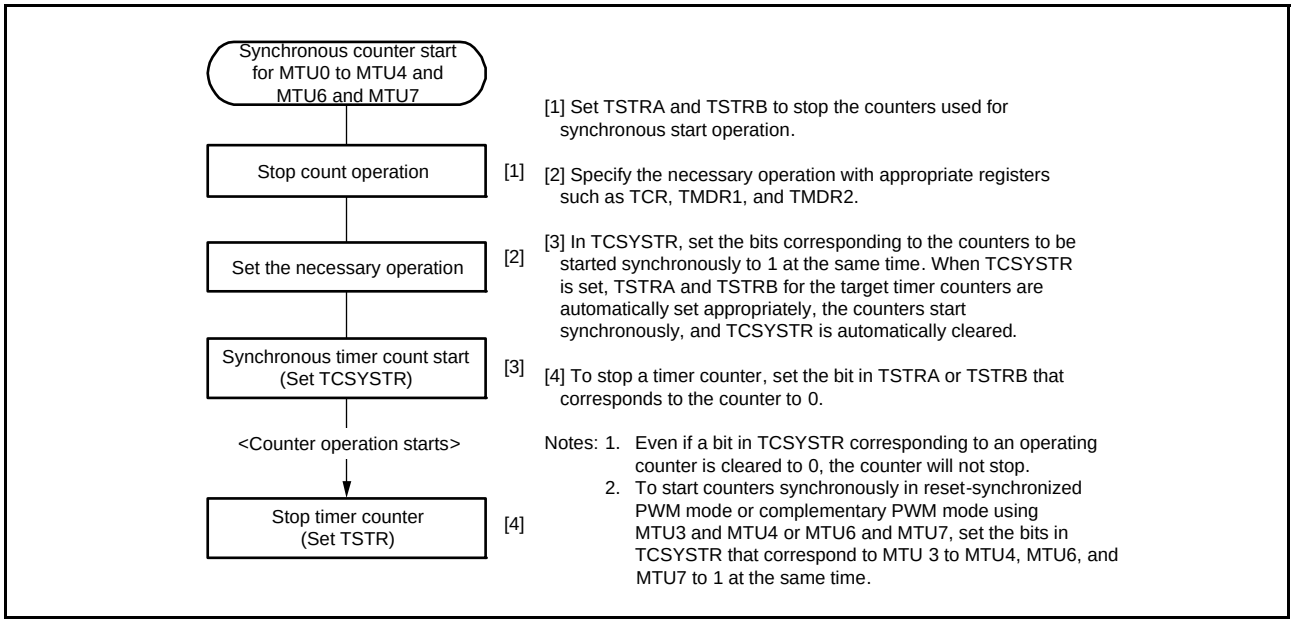


Figure 22.90 Example of Synchronous Counter Start Setting Procedure

(b) Examples of Synchronous Counter Start Operation

Figure 22.91 shows an example of synchronous counter start operation for MTU0 to MTU4 and MTU6 and MTU7.

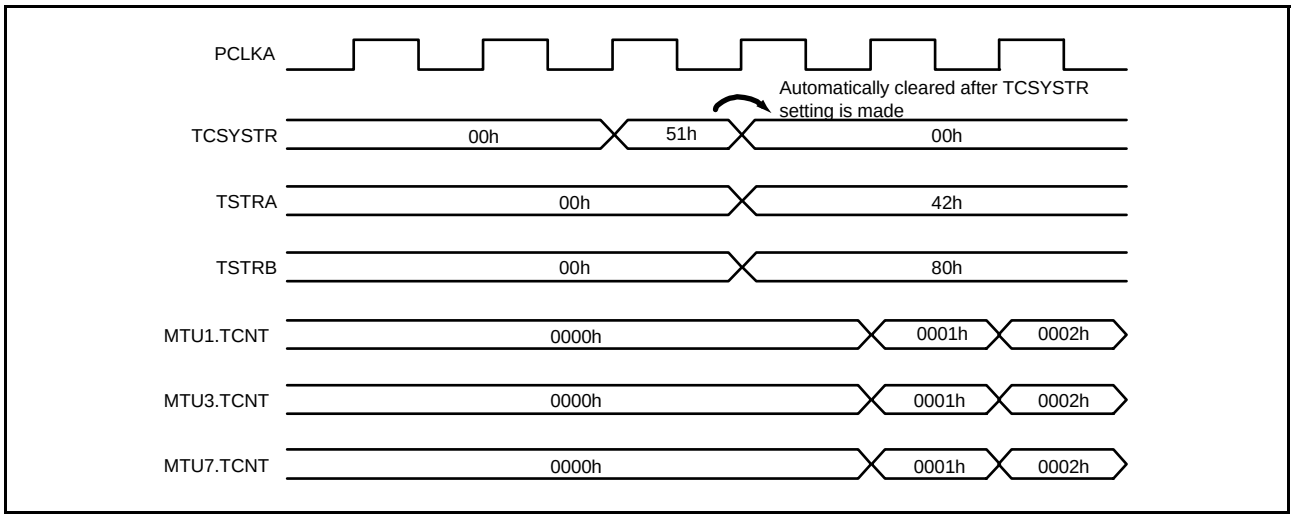


Figure 22.91 Example of Synchronous Counter Start Operation

(2) Clearing Counters of MTU6 and MTU7 by Flag Setting Sources (Synchronous Counter Clearing for MTU6 and MTU7)

The counters in MTU6 and MTU7 can be cleared by sources for setting the flags in MTU0.TSR to MTU2.TSR through the TSYCR setting.

(a) Example of Procedure for Specifying Counter Clearing for MTU6 and MTU7 by Flag Setting Sources

Figure 22.92 shows an example of procedure for specifying counter clearing for MTU6 and MTU7 by flag setting sources.

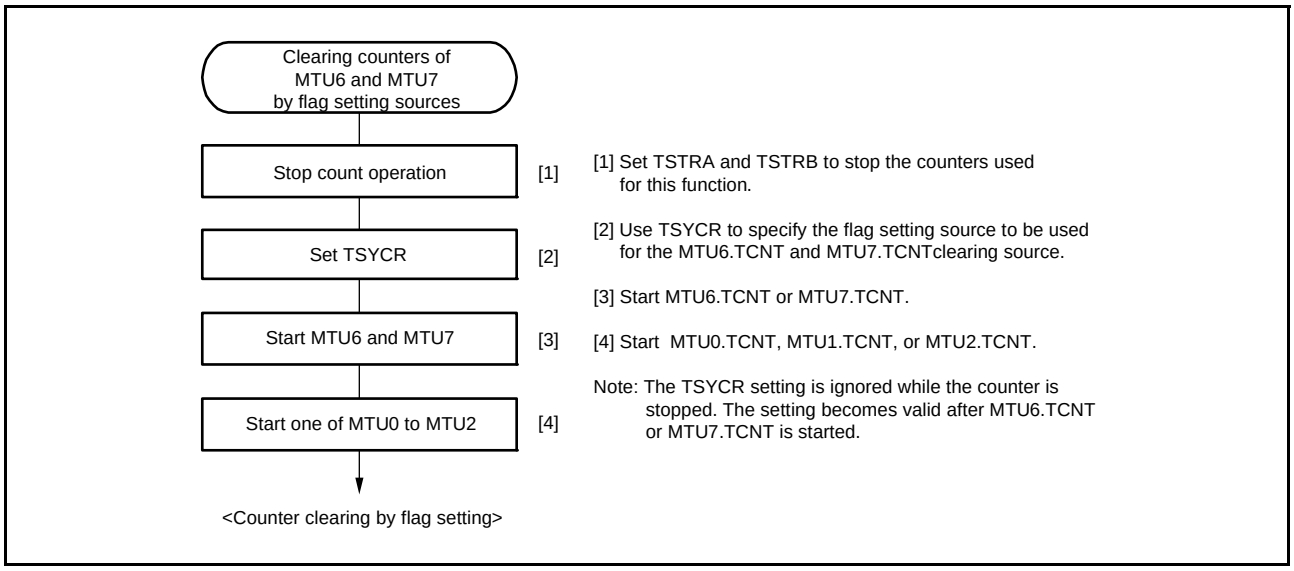


Figure 22.92 Example of Procedure for Specifying Counter Clearing for MTU6 and MTU7 by Flag Setting Sources

(b) Examples of Counter Clearing for MTU6 and MTU7 by Flag Setting Sources

Figure 22.93 and Figure 22.94 show examples of counter clearing for MTU6 and MTU7 by flag setting sources.

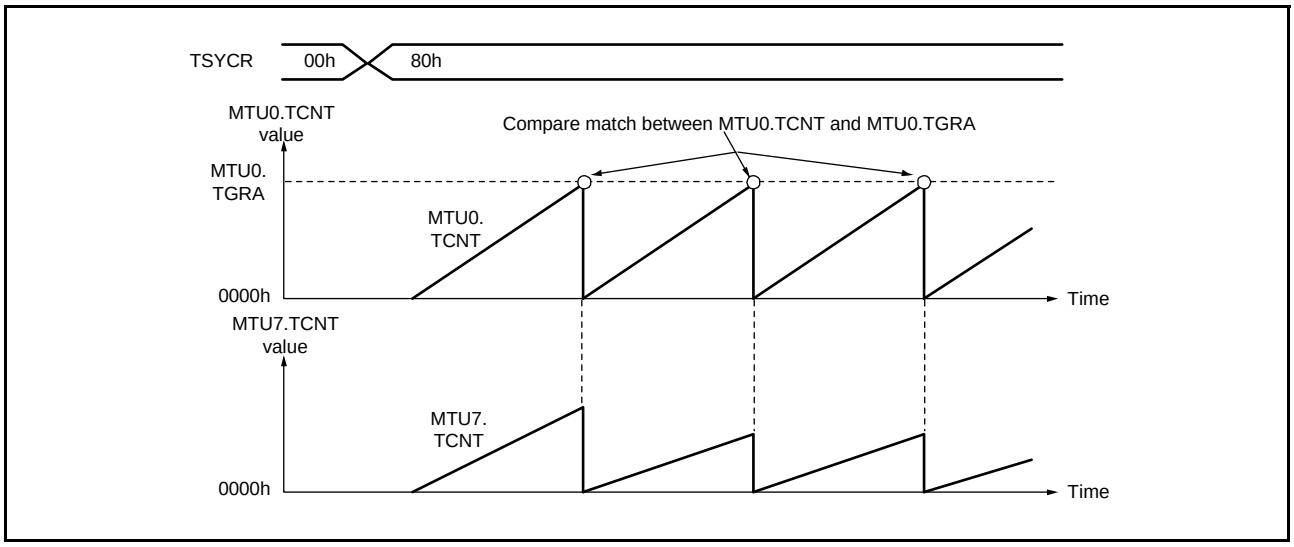


Figure 22.93 Example of Counter Clearing for MTU6 and MTU7 by Flag Setting Sources (1)

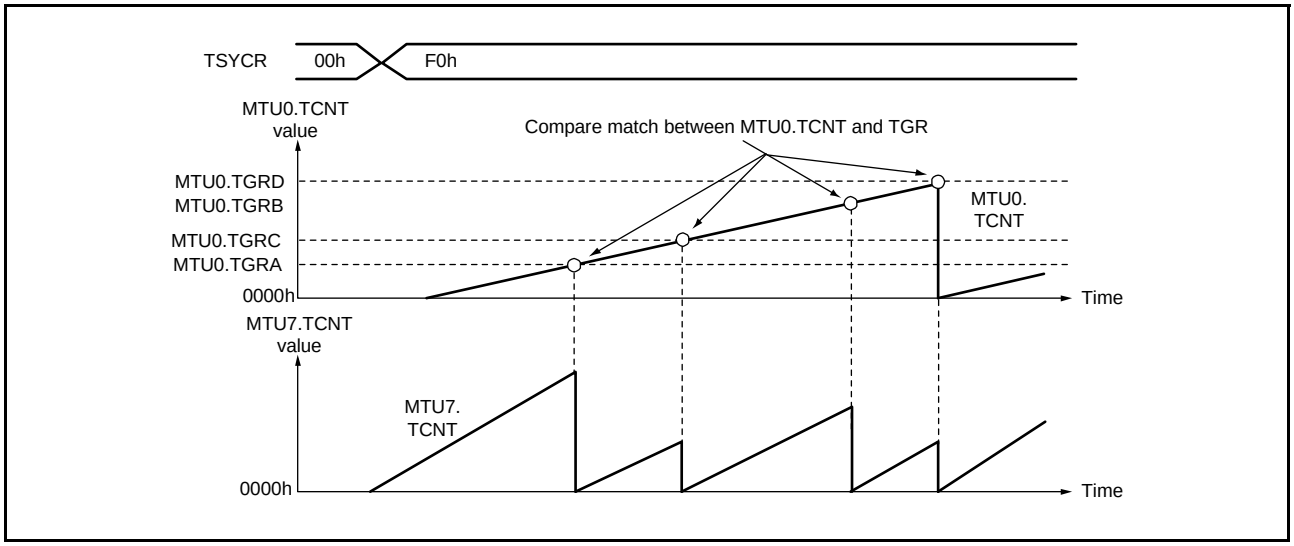


Figure 22.94 Example of Counter Clearing for MTU6 and MTU7 by Flag Setting Sources (2)

22.3.11 External Pulse Width Measurement

The pulse widths of up to three external input lines can be measured in MTU5.

(1) Example of External Pulse Width Measurement Setting Procedure

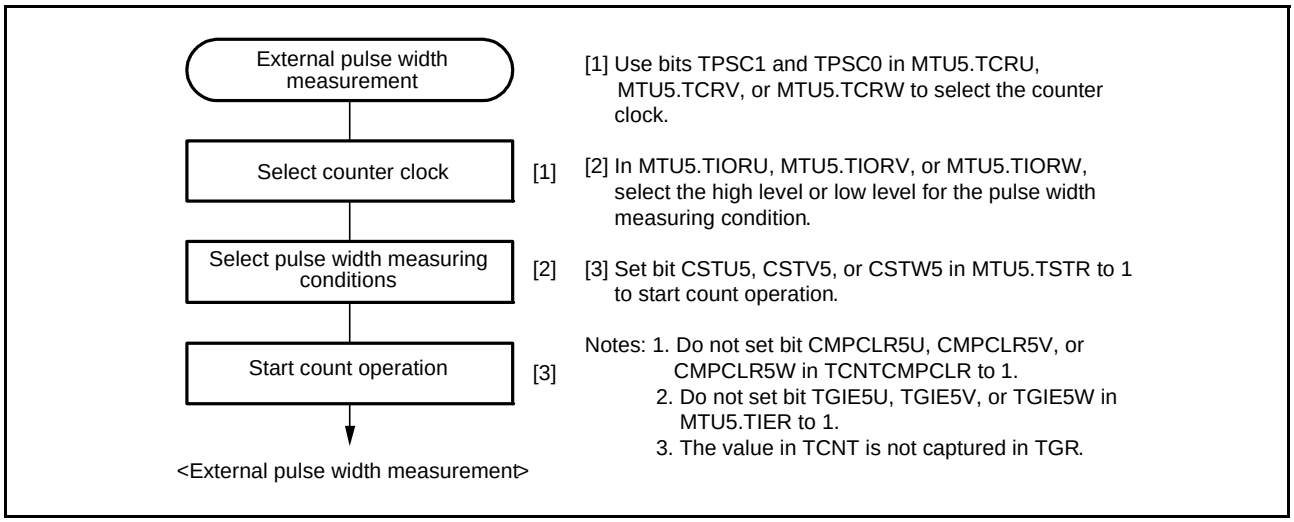


Figure 22.95 Example of External Pulse Width Measurement Setting Procedure

(2) Example of External Pulse Width Measurement

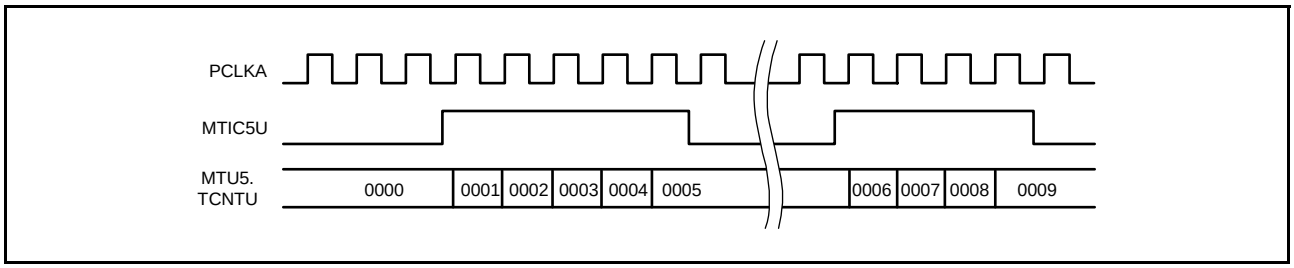


Figure 22.96 Example of External Pulse Width Measurement (Measuring High Pulse Width)

22.3.12 Dead Time Compensation

By measuring the delay of the output waveform and reflecting it to duty ratio, the external pulse width measurement function can be used as the dead time compensation function while the complementary PWM is in operation.

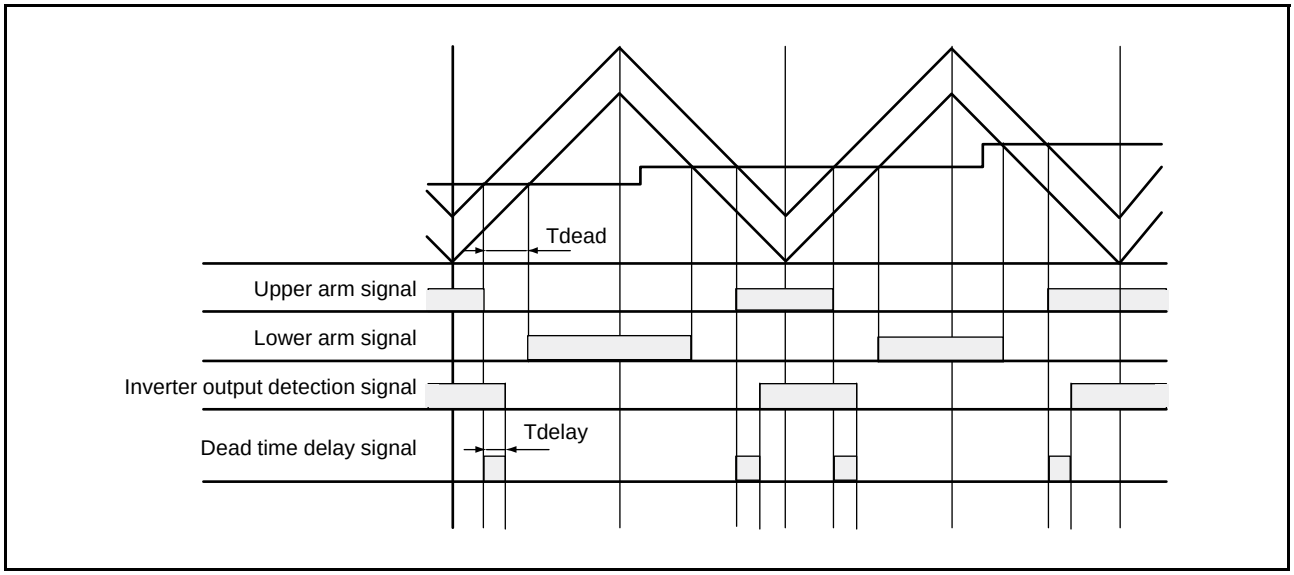
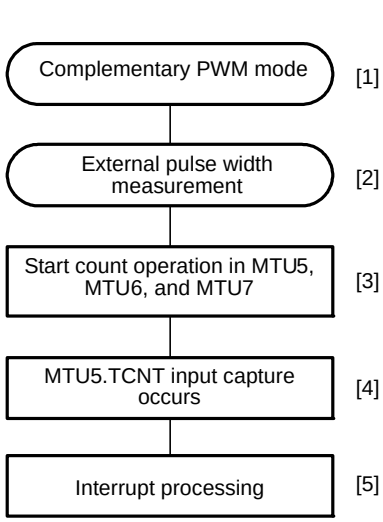


Figure 22.97 Delay in Dead Time in Complementary PWM Operation

(1) Example of Dead Time Compensation Setting Procedure

Figure 22.98 shows an example of dead time compensation setting procedure by using three counters in MTU5.



[1] Place MTU6 and MTU7 in complementary PWM mode. For details, refer to section 22.3.8, Complementary PWM Mode.

[2] Specify the external pulse width measurement function for the target TIOR in MTU5. For details, refer to section 22.3.11, External Pulse Width Measurement.

[3] Set bits CST6 and CST7 in TSTRB and bits CSTU5, CSTV5, and CSTW5 in MTU5.TSTR to 1 to start count operation.

[4] When the capture condition specified in TIOR is satisfied, the MTU5.TCNT value is captured in MTU5.TGR.

[5] For U-phase dead time compensation, when an interrupt is generated at the crest (TGIA6) or trough (TCIV7) in complementary PWM mode, read the MTU5.TGRU value, calculate the difference in time between MTU5.TGRU and MTU6.TGRB, and write the corrected value to MTU6.TGRD in the interrupt processing.
For the V phase and W phase, read the MTU5.TGRV and MTU5.TGRW values and write the corrected values to MTU7.TGRC and TGRD, respectively, in the same way as for U-phase compensation.
The MTU5.TCNT value should be cleared through the TCNTCMPCLR setting or by software.

Note: The MPC and port mode registers (PMR) of the I/O ports should be set up in advance.
As an interrupt flag is set under the capture condition specified in TIOR, do not enable interrupt requests in MTU5.TIER.

Figure 22.98 Example of Dead Time Compensation Setting Procedure

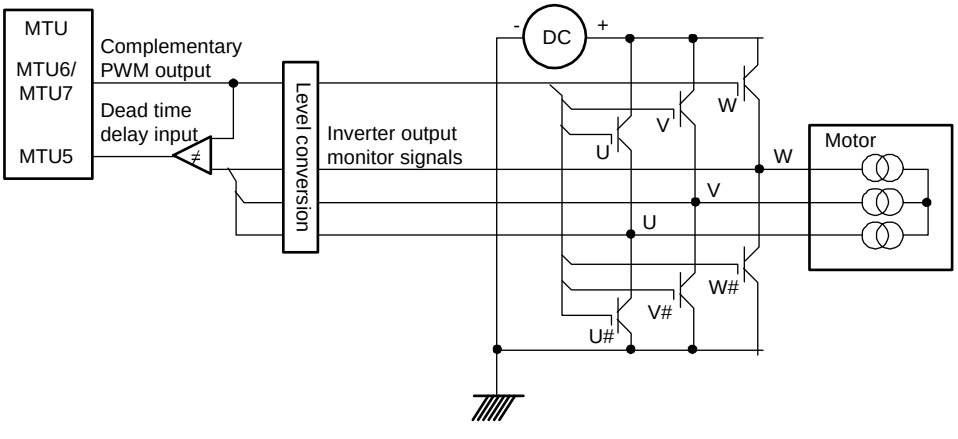


Figure 22.99 Example of Motor Control Circuit Configuration

22.3.13 TCNT Capture at Crest and/or Trough in Complementary PWM Mode

The TCNT value is captured in TGR at either the crest or trough or at both the crest and trough during complementary PWM mode. The timing for capturing in TGR can be selected by TIOR.

Figure 22.100 is an operating example in which TCNT is used as a free-running counter without being cleared, and the TCNT value is captured in TGR at the specified timing (either crest or trough, or both crest and trough).

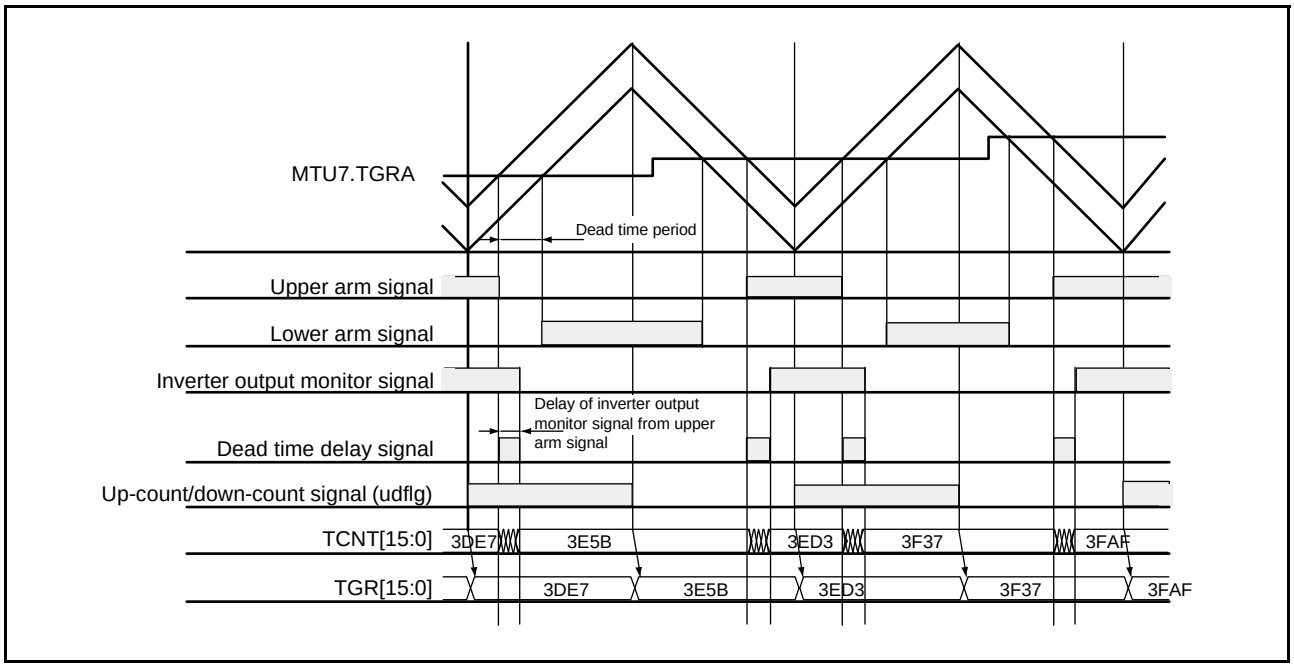


Figure 22.100 TCNT Capture at Crest and/or Trough in Complementary PWM Operation

22.4 Interrupt Sources

22.4.1 Interrupt Sources and Priorities

There are three kinds of MTU3 interrupt source; TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own status flag and enable/disable bit, allowing the generation of interrupt request signals to be enabled or disabled individually.

When an interrupt source is detected, the corresponding status flag in TSR is set to 1. If the corresponding enable/disable bit in TIER is set to 1 at this time, an interrupt is requested. Setting the status flag to 1 cancels the interrupt request. However, if a further interrupt is generated while the corresponding status flag is 1, the interrupt will be ignored. To enable the acceptance of an interrupt, the flag of the interrupt generation source should be 0.

Relative channel priorities can be changed by the interrupt controller; however the priority within a channel is fixed. For details, see section 15, Interrupt controller (ICUb).

Table 22.72 lists the MTU3 interrupt sources.

Table 22.72 MTU3 Interrupt Sources

Channel	Name	Interrupt Source	DTC/DMAC Activation	Priority
MTU0	TGIA0	MTU0.TGRA input capture/compare match	Possible	High
	TGIB0	MTU0.TGRB input capture/compare match	Possible	
	TGIC0	MTU0.TGRC input capture/compare match	Possible	
	TGID0	MTU0.TGRD input capture/compare match	Possible	
	TCIV0	MTU0.TCNT overflow	Not possible	
	TGIE0	MTU0.TGRE compare match	Not possible	
	TGIF0	MTU0.TGRF compare match	Not possible	
MTU1	TGIA1	MTU1.TGRA input capture/compare match	Possible	
	TGIB1	MTU1.TGRB input capture/compare match	Possible	
	TCIV1	MTU1.TCNT overflow	Not possible	
	TCIU1	MTU1.TCNT underflow	Not possible	
MTU2	TGIA2	MTU2.TGRA input capture/compare match	Possible	
	TGIB2	MTU2.TGRB input capture/compare match	Possible	
	TCIV2	MTU2.TCNT overflow	Not possible	
	TCIU2	MTU2.TCNT underflow	Not possible	
MTU3	TGIA3	MTU3.TGRA input capture/compare match	Possible	
	TGIB3	MTU3.TGRB input capture/compare match	Possible	
	TGIC3	MTU3.TGRC input capture/compare match	Possible	
	TGID3	MTU3.TGRD input capture/compare match	Possible	
	TCIV3	MTU3.TCNT overflow	Not possible	
MTU4	TGIA4	MTU4.TGRA input capture/compare match	Possible	
	TGIB4	MTU4.TGRB input capture/compare match	Possible	
	TGIC4	MTU4.TGRC input capture/compare match	Possible	
	TGID4	MTU4.TGRD input capture/compare match	Possible	
	TCIV4	MTU4.TCNT overflow/underflow (only in complementary PWM mode)	Possible	
MTU5	TGIU5	MTU5.TGRU input capture/compare match	Possible	
	TGIV5	MTU5.TGRV input capture/compare match	Possible	
	TGIW5	MTU5.TGRW input capture/compare match	Possible	
MTU6	TGIA6	MTU6.TGRA input capture/compare match	Possible	
	TGIB6	MTU6.TGRB input capture/compare match	Possible	
	TGIC6	MTU6.TGRC input capture/compare match	Possible	
	TGID6	MTU6.TGRD input capture/compare match	Possible	
	TCIV6	MTU6.TCNT overflow	Not possible	
MTU7	TGIA7	MTU7.TGRA input capture/compare match	Possible	
	TGIB7	MTU7.TGRB input capture/compare match	Possible	
	TGIC7	MTU7.TGRC input capture/compare match	Possible	
	TGID7	MTU7.TGRD input capture/compare match	Possible	
	TCIV7	MTU7.TCNT overflow/underflow (only in complementary PWM mode)	Possible	Low

Note 1. This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

(1) Input Capture/Compare Match Interrupt

An interrupt is requested if the TIER.TGIE bit is set to 1 when a TSR.TGR input capture/compare match occurs on a channel and the TSR.TGF flag is set to 1. Clearing the TSR.TGF flag to 0 cancels the interrupt request. The MTU has 29 input capture/compare match interrupts (six for MTU0, four each for MTU3, MTU4, MTU6, and MTU7, two each for MTU1 and MTU2, and three for MTU5). The MTU0.TGFE and MTU0.TGFF flags in MTU0 are not set by the occurrence of an input capture.

(2) Overflow Interrupt

An interrupt is requested if the TIER.TCIEV bit is set to 1 when a TCNT overflow occurs on a channel and the TSR.TCFV flag is set to 1. Clearing the TSR.TCFV flag to 0 cancels the interrupt request. The MTU has seven overflow interrupts (one for each channel).
Furthermore, when operation is in complementary PWM mode, an underflow of MTU4.TCNT and MTU7.TCNT leads to setting of the TCFV flag.

(3) Underflow Interrupt

An interrupt is requested if the TIER.TCIEU bit is set to 1 when a TCNT underflow occurs on a channel and the TSR.TCFU flag is set to 1. Clearing the TSR.TCFU flag to 0 cancels the interrupt request. The MTU has two underflow interrupts (one each for MTU1 and MTU2).

22.4.2 DMAC or DTC Activation

The DTC or DMAC can be activated by the TGR input capture/compare match interrupt in each channel or the overflow interrupt in MTU4 and MTU7. For details, see section 18, DMA Controller (DMACA) or section 19, Data Transfer Controller (DTCa).
The MTU provides a total of 29 input capture/compare match interrupts and overflow interrupts that can be used as DTC or DMAC activation sources: four each for MTU0, MTU3, and MTU6, two each for MTU1 and MTU2, five each for MTU4 and MTU7, and three for MTU5.
However, as similar to the interrupt handling, if a further DTC or DMAC activation request is generated while the corresponding status flag is 1, the interrupt will be ignored. To enable the acceptance of an interrupt, the flag of the interrupt generation source should be 0.

22.4.3 A/D Converter Activation

The A/D converter can be activated by one of the following three methods in the MTU3. Table 22.72 shows the relationship between interrupt sources and A/D converter start request signals.

(1) A/D Converter Activation by TGRA Input Capture/Compare Match or at MTU4.TCNT (MTU7.TCNT) Trough in Complementary PWM Mode

The A/D converter can be activated by the occurrence of a TGRA input capture/compare match in each channel. In addition, if complementary PWM operation is performed while the TTGE2 bit in MTU4.TIER (MTU7.TIER) is set to 1, the A/D converter can be activated at the trough of MTU4.TCNT (MTU7.TCNT) count (MTU4.TCNT (MTU7.TCNT) = 0000h).
A/D converter start request signal TRGAnN is issued to the A/D converter under either of the following conditions (n = MTU0 to MTU4, MTU6, or MTU7).

- When a TGRA input capture/compare match occurs on a channel and the TGFA flag in TSR is set to 1 while the TTGE bit in TIER is set to 1
- When the MTU4.TCNT (MTU7.TCNT) count reaches the trough (MTU4.TCNT (MTU7.TCNT) = 0000h) during complementary PWM operation while the TTGE2 bit in MTU4.TIER (MTU7.TIER) is set to 1

When either condition is satisfied, if A/D converter start request signal TRGAnN from the MTU3 is selected as the trigger in the A/D converter, A/D conversion will start.

(2) A/D Converter Activation by Compare Match between MTU0.TCNT and MTU0.TGRE

A/D converter start request signal TRG0AN is issued to the A/D converter when a compare match occurs between MTU0.TCNT and MTU0.TGRE in MTU0.
When the TGFE flag in MTU0.TSR2 is set to 1 by the occurrence of a compare match between MTU0.TCNT and MTU0.TGRE in MTU0 while the TTGE2 bit in MTU0.TIER2 is set to 1, A/D converter start request TGR0AN is issued to the A/D converter. If A/D converter start request signal TRG0AN from the MTU3 is selected as the trigger in the A/D converter, A/D conversion will start.

(3) A/D Converter Activation by A/D Converter Start Request Delaying Function

The A/D converter can be activated by generating A/D converter start request signal TRG4AN or TRG4BN (TRG7AN or TRG7BN) when the MTU4.TCNT (MTU7.TCNT) count matches the MTU4.TADCORA or MTU4.TADCORB (MTU7.TADCORA or MTU7.TADCORB) value if the UT4AE, DT4AE, UT4BE, or DT4BE (UT7AE, DT7AE, UT7BE, or DT7BE) bit in the A/D converter start request control register (MTU4.TADCR (MTU7.TADCR)) is set to 1. For details, refer to section 22.3.9, A/D Converter Start Request Delaying Function.
A/D conversion will start when TRG4AN (TRG7AN) is generated if A/D converter start request signal TRG4AN (TRG7AN) from the MTU3 is selected as the trigger in the A/D converter, when TRG4BN (TRG7BN) is generated if TRG4BN (TRG7BN) from the MTU3 is selected as the trigger in the A/D converter, or when TRG4ABN (TRG7ABN) is generated if TRG4ABN (TRG7ABN) from the MTU3 is selected as the trigger in the A/D converter.

Table 22.73 Interrupt Sources and A/D Converter Start Request Signals

Target Registers	Interrupt Source	A/D Converter Start Request Signal
MTU0.TGRA and MTU0.TCNT	Input capture/compare match	TRGA0N
MTU1.TGRA and MTU1.TCNT		TRGA1N
MTU2.TGRA and MTU2.TCNT		TRGA2N
MTU3.TGRA and MTU3.TCNT		TRGA3N
MTU4.TGRA and MTU4.TCNT*1		TRGA4N
MTU4.TCNT	MTU4.TCNT trough in complementary PWM mode	
MTU6.TGRA and MTU6.TCNT	Input capture/compare match	TRGA6N
MTU7.TGRA and MTU7.TCNT*1		TRGA7N
MTU7.TCNT	MTU7.TCNT trough in complementary PWM mode	
MTU0.TGRE and MTU0.TCNT	Compare match	TRG0AN
MTU4.TADCORA and MTU4.TCNT	Compare match	TRG4AN
MTU4.TADCORB and MTU4.TCNT		TRG4BN
MTU7.TADCORA and MTU7.TCNT		TRG7AN
MTU7.TADCORB and MTU7.TCNT		TRG7BN
MTU4.TADCORA and MTU4.TCNT, MTU4.TADCORB and MTU4.TCNT	Compare match (interrupt skipping function 2)	TRG4ABN
MTU7.TADCORA and MTU7.TCNT, MTU7.TADCORB and MTU7.TCNT		TRG7ABN

Note 1. Since PWM waveforms are generated in complementary PWM mode, MTU4.TGRA (MTU7.TGRA) compare match not only with MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) and TCNTSA (TCNTSB) is detected. Accordingly, when compare match with MTU3.TCNT (MTU6.TCNT) and TCNTSA (TCNTSB) occurs, TRGA4N (TRGA7N) is also generated. When MTU3 and MTU 4 (MTU 6 and MTU7) are made to operate in complementary PWM mode for generating an A/D converter start request, use the A/D converter start request by compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA/B (MTU7.TADCORA/B).

22.5 Operation Timing

22.5.1 Input/Output Timing

(1) TCNT Count Timing

Figure 22.101 and Figure 22.102 show the TCNT count timing in internal clock operation, Figure 22.103 shows the TCNT count timing in external clock operation (normal mode), and Figure 22.104 shows the TCNT count timing in external clock operation (phase counting mode).

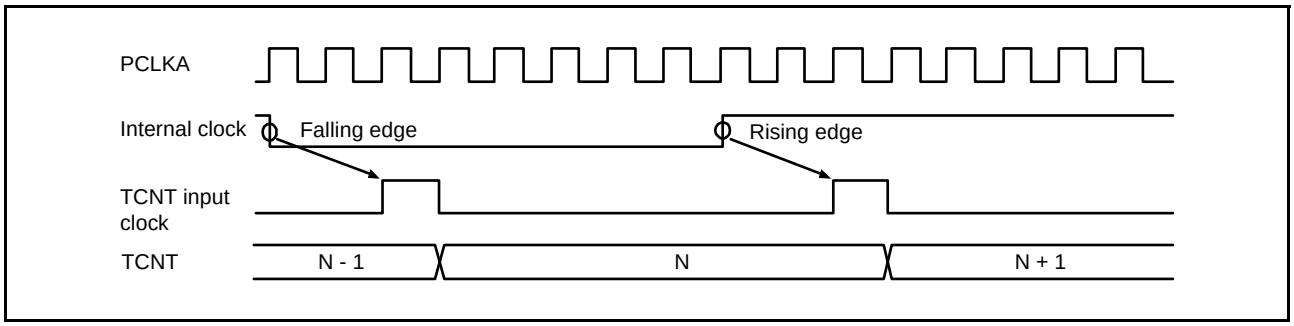


Figure 22.101 Count Timing in Internal Clock Operation (MTU0 to MTU4, MTU6, and MTU7)

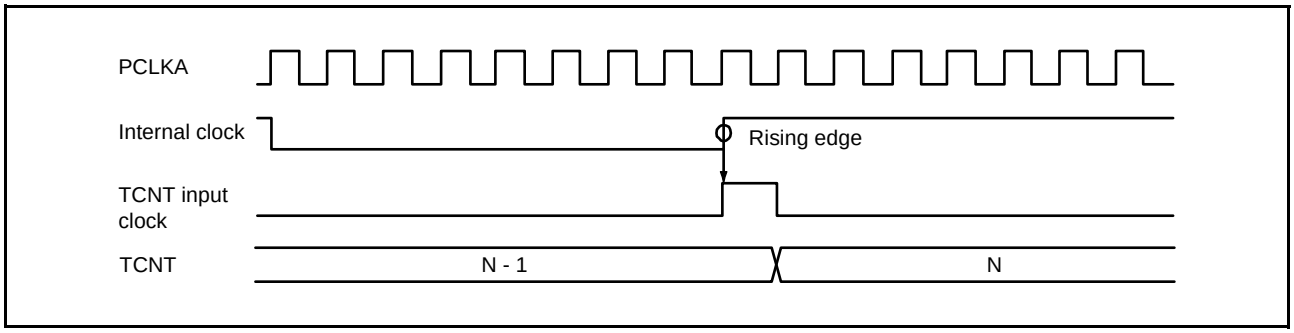


Figure 22.102 Count Timing in Internal Clock Operation (MTU5)

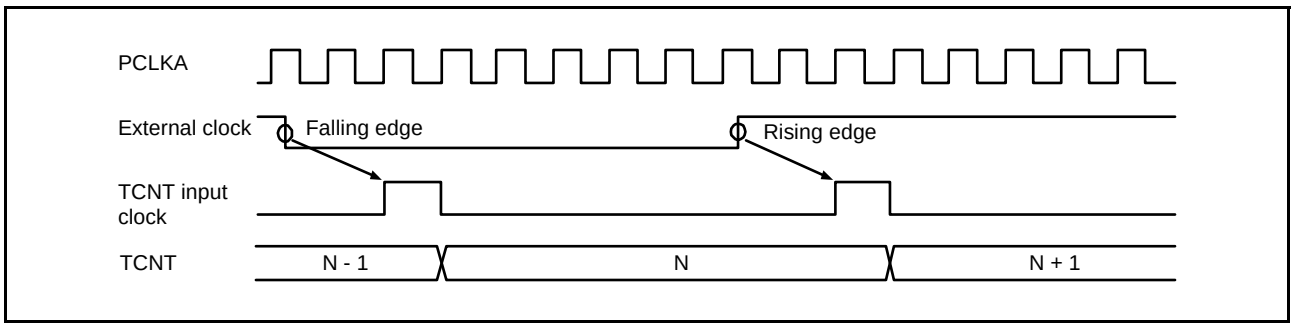


Figure 22.103 Count Timing in External Clock Operation (MTU0 to MTU4)

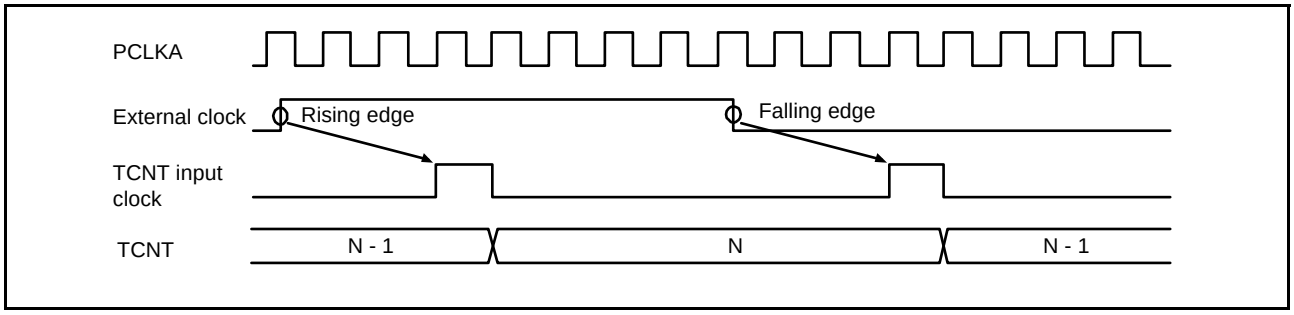


Figure 22.104 Count Timing in External Clock Operation (Phase Counting Mode)

(2) Output Compare Output Timing

A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the value set in TIOR is output from the output compare output pin the MTIOCnm pin (n = 0 to 4, 6, 7; m = A to D). After a match between TCNT and TGR, the compare match signal is not generated until the TCNT input clock is generated.

Figure 22.105 shows the output compare output timing (normal mode or PWM mode) and Figure 22.106 shows the output compare output timing (complementary PWM mode or reset-synchronized PWM mode).

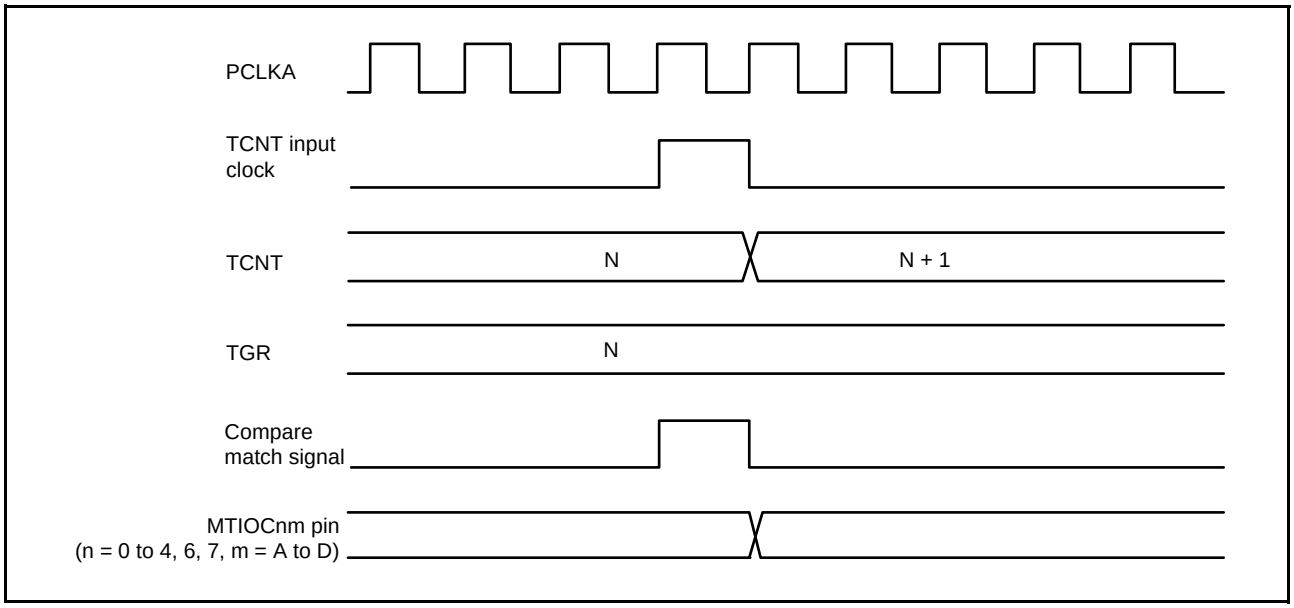


Figure 22.105 Output Compare Output Timing (Normal Mode or PWM Mode)

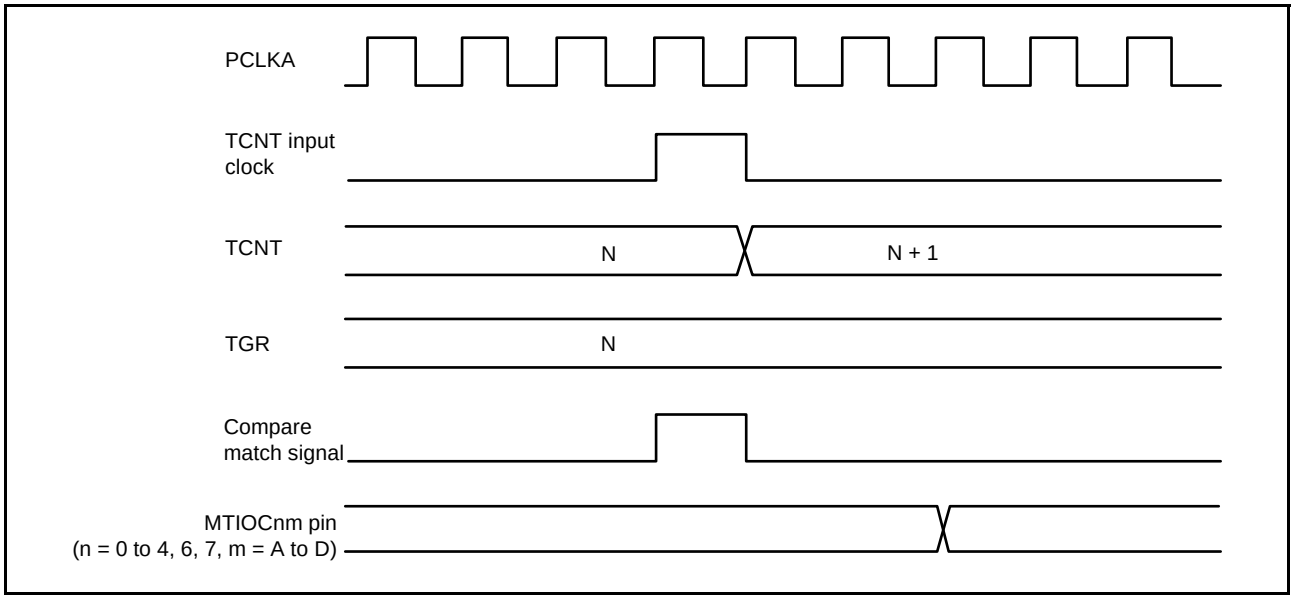


Figure 22.106 Output Compare Output Timing (Complementary PWM Mode or Reset-Synchronized PWM Mode)

(3) Input Capture Signal Timing

Figure 22.107 shows the input capture signal timing.

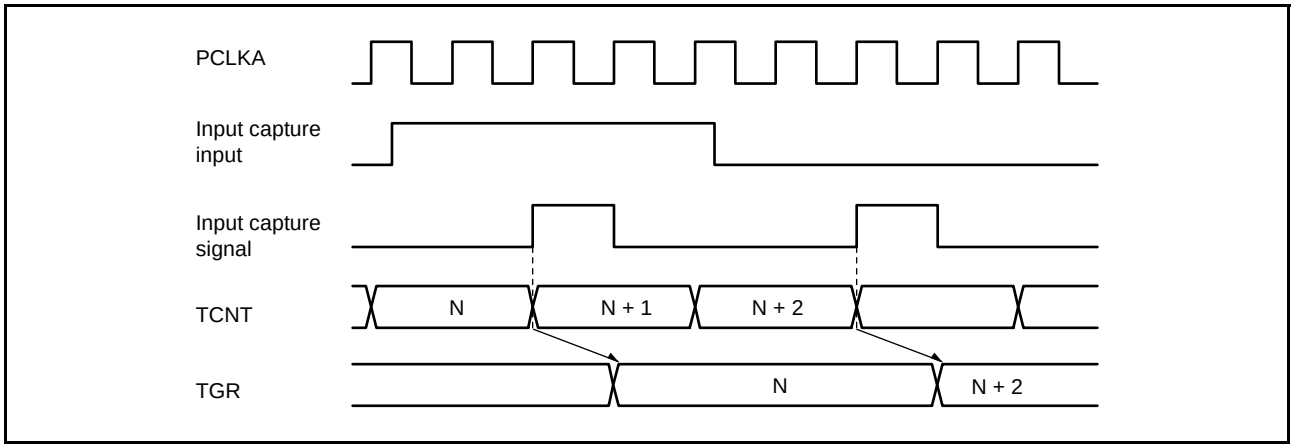


Figure 22.107 Input Capture Input Signal Timing

(4) Timing for Counter Clearing by Compare Match/Input Capture

FFigure 22.108 and Figure 22.109 show the timing when counter clearing on compare match is specified, and Figure 22.110 shows the timing when counter clearing on input capture is specified.

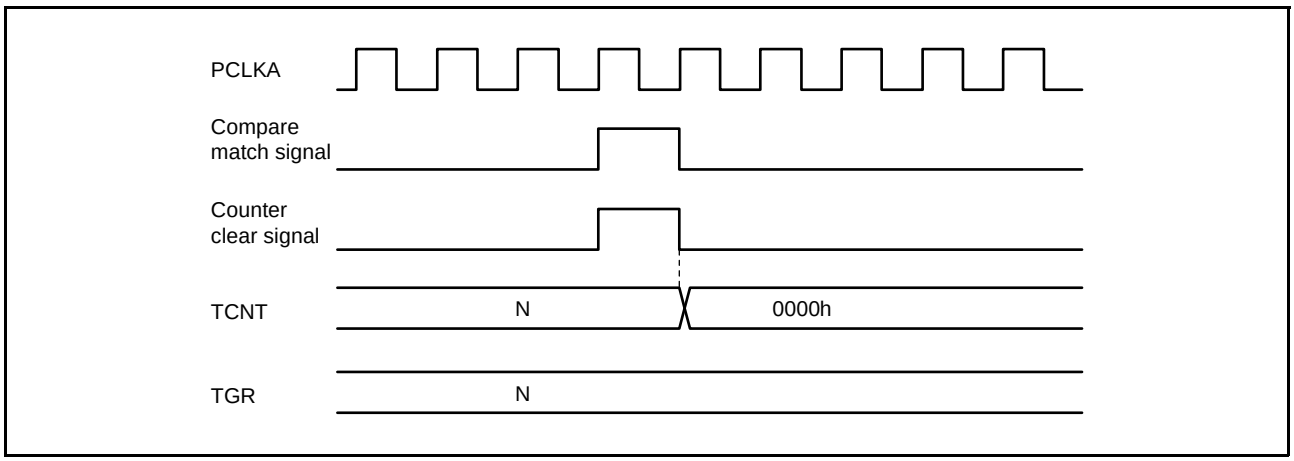


Figure 22.108 Counter Clear Timing (Compare Match) (MTU0 to MTU4, MTU6, and MTU7)

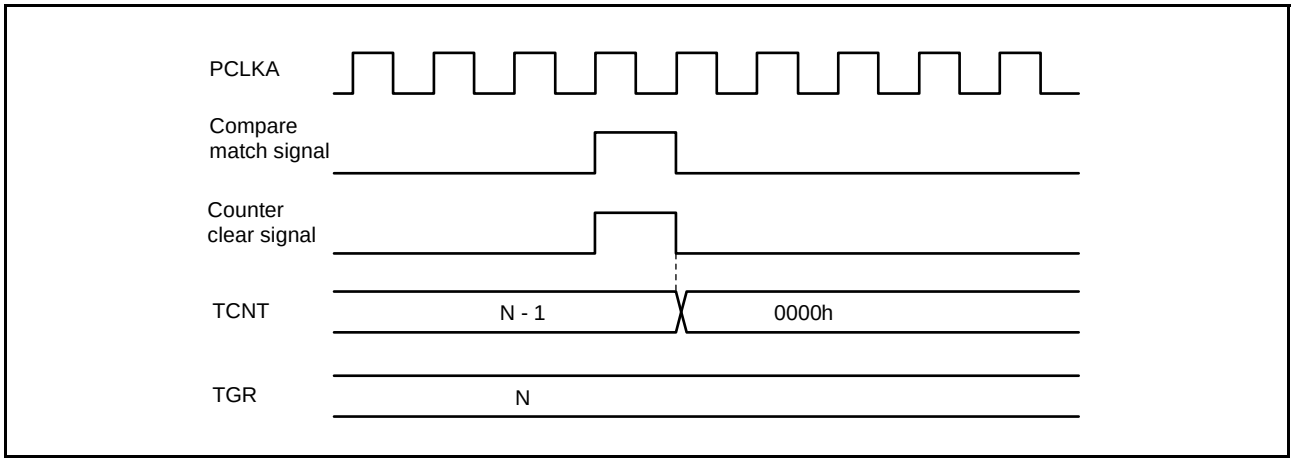


Figure 22.109 Counter Clear Timing (Compare Match) (MTU5)

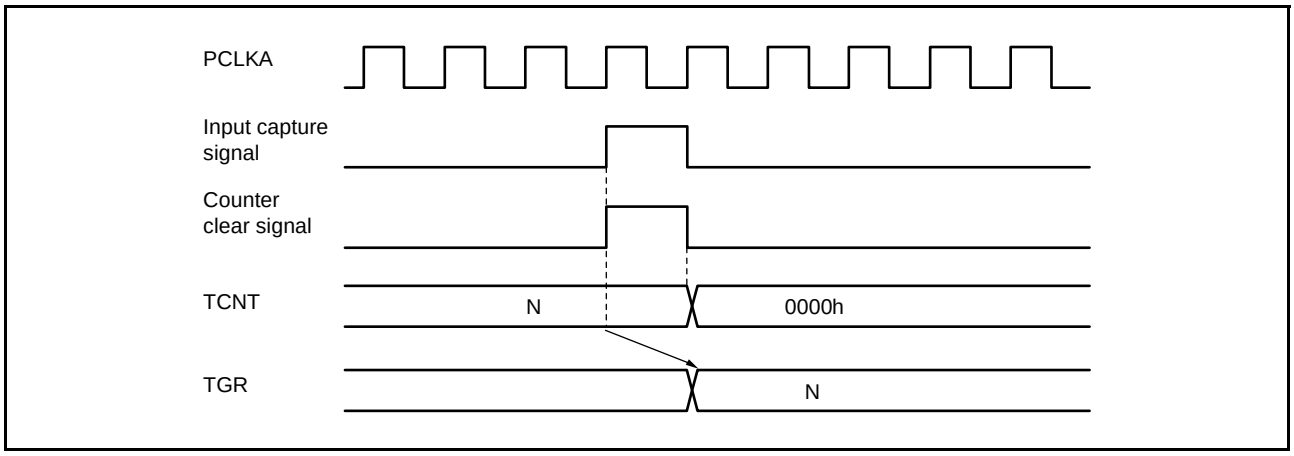


Figure 22.110 Counter Clear Timing (Input Capture) (MTU0 to MTU7)

(5) Buffer Operation Timing

Figure 22.111 to Figure 22.113 show the timing in buffer operation.

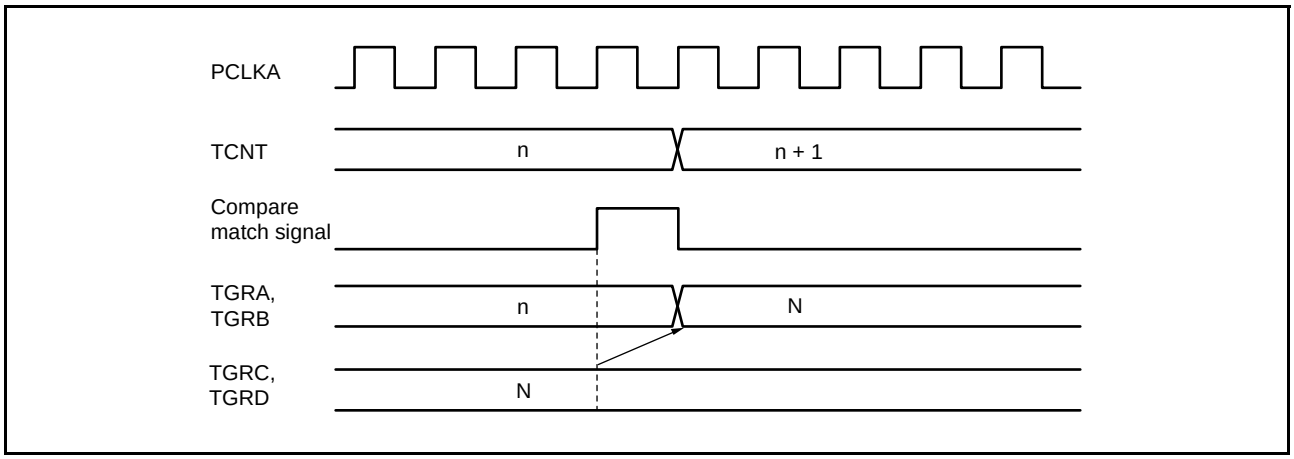


Figure 22.111 Buffer Operation Timing (Compare Match)

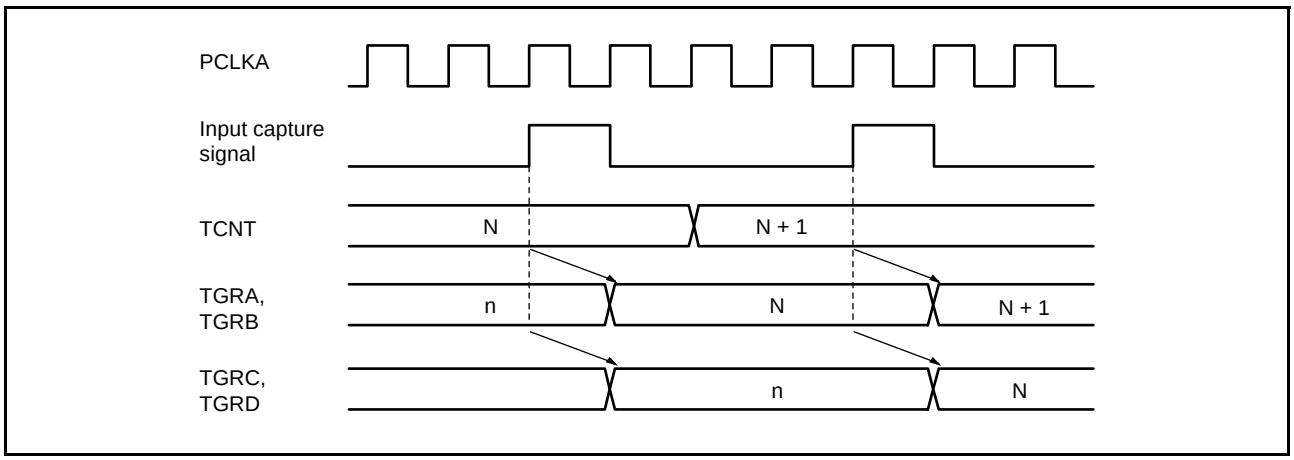


Figure 22.112 Buffer Operation Timing (Input Capture)

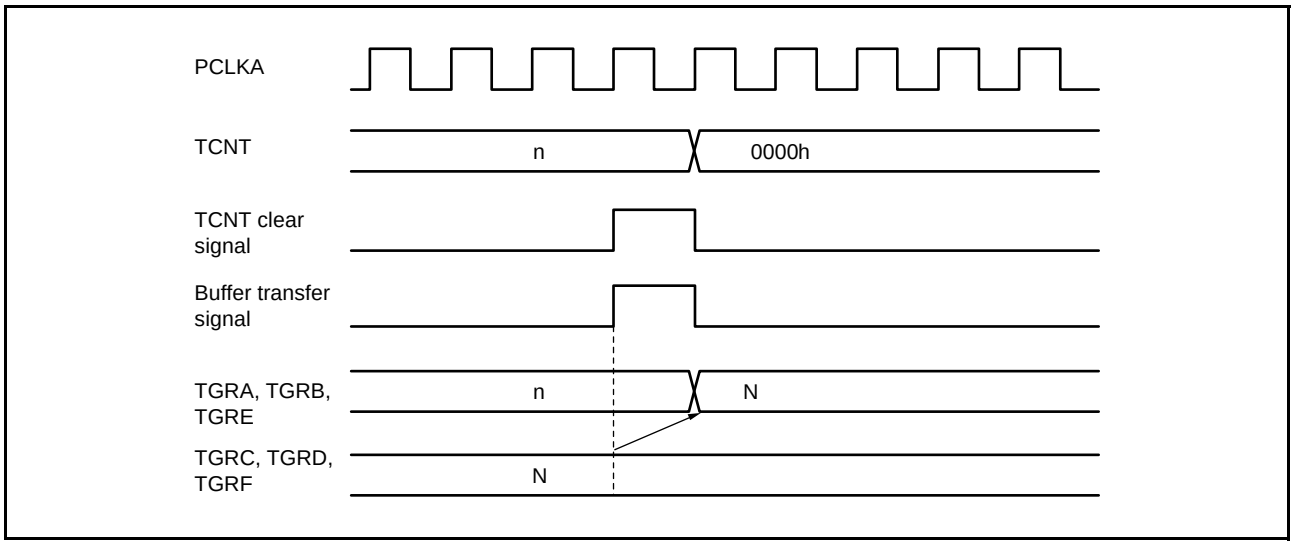


Figure 22.113 Buffer Operation Timing (when TCNT Cleared)

(6) Buffer Transfer Timing (Complementary PWM Mode)

Figure 22.114 to Figure 22.116 show the buffer transfer timing in complementary PWM mode.

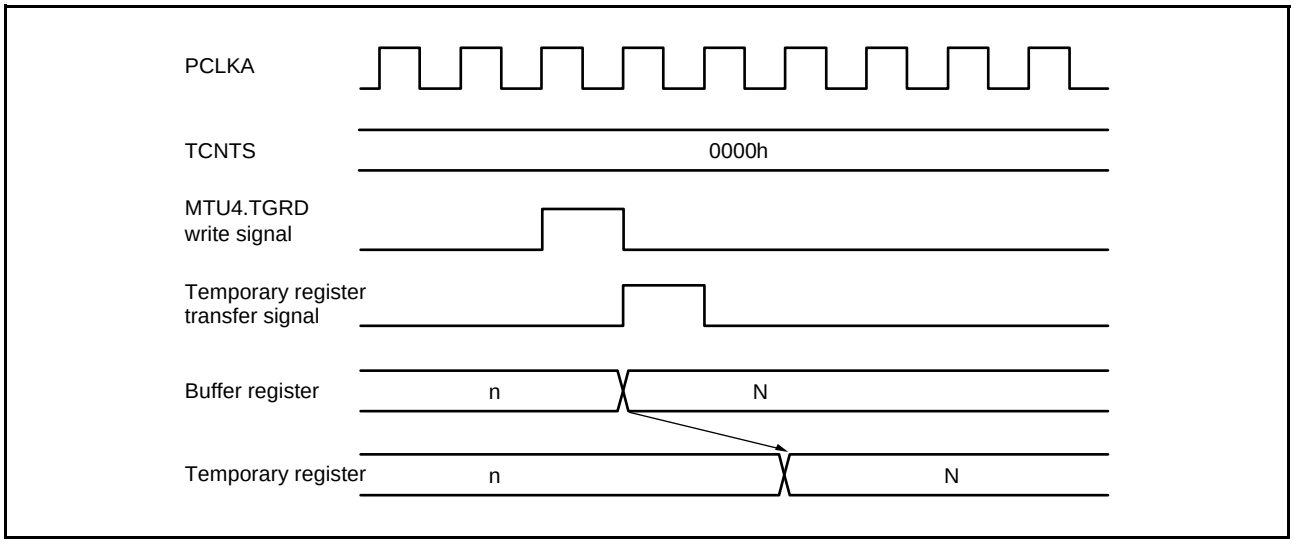


Figure 22.114 Transfer Timing from Buffer Register to Temporary Register (TCNTSA Stopped)

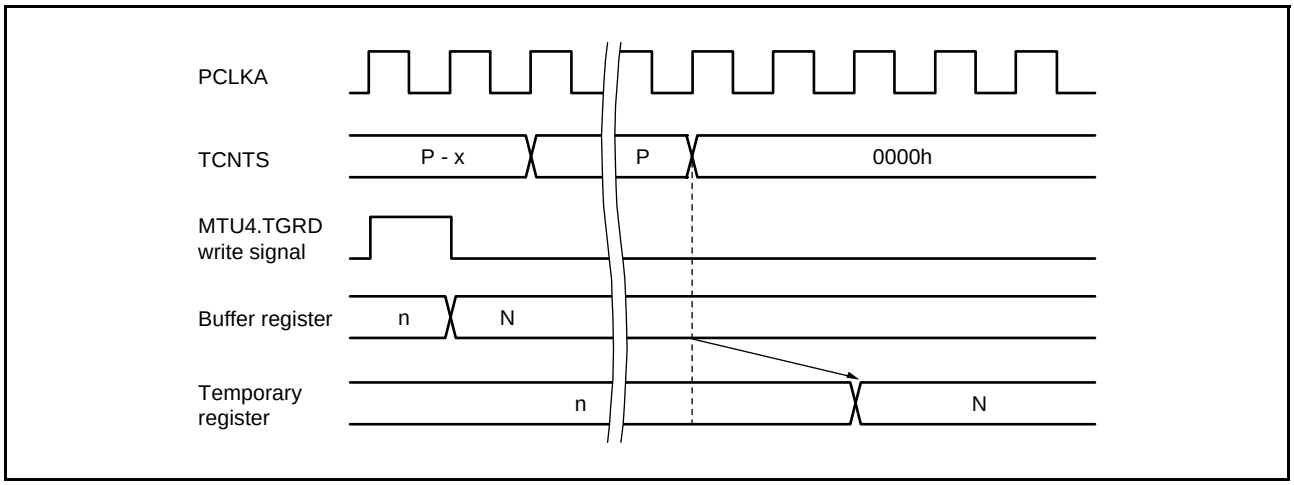


Figure 22.115 Transfer Timing from Buffer Register to Temporary Register (TCNTSA Operating)

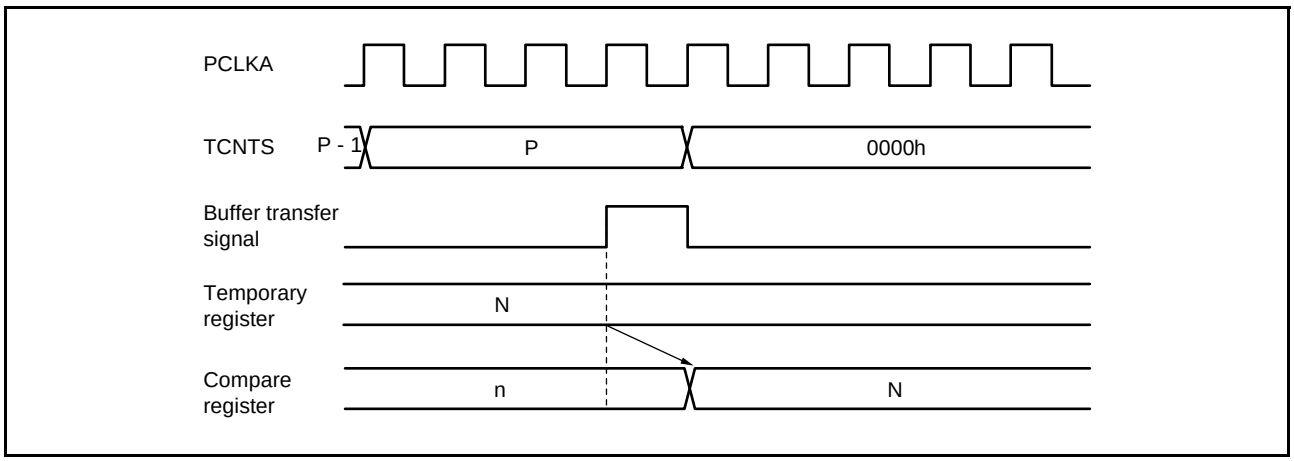


Figure 22.116 Transfer Timing from Temporary Register to Compare Register

22.5.2 Interrupt Signal Timing

(1) Timing for TGF Flag Setting by Compare Match

Figure 22.117 and Figure 22.118 show the timing of TGF flag setting in TSR on compare match and the TGI interrupt request signal timing.

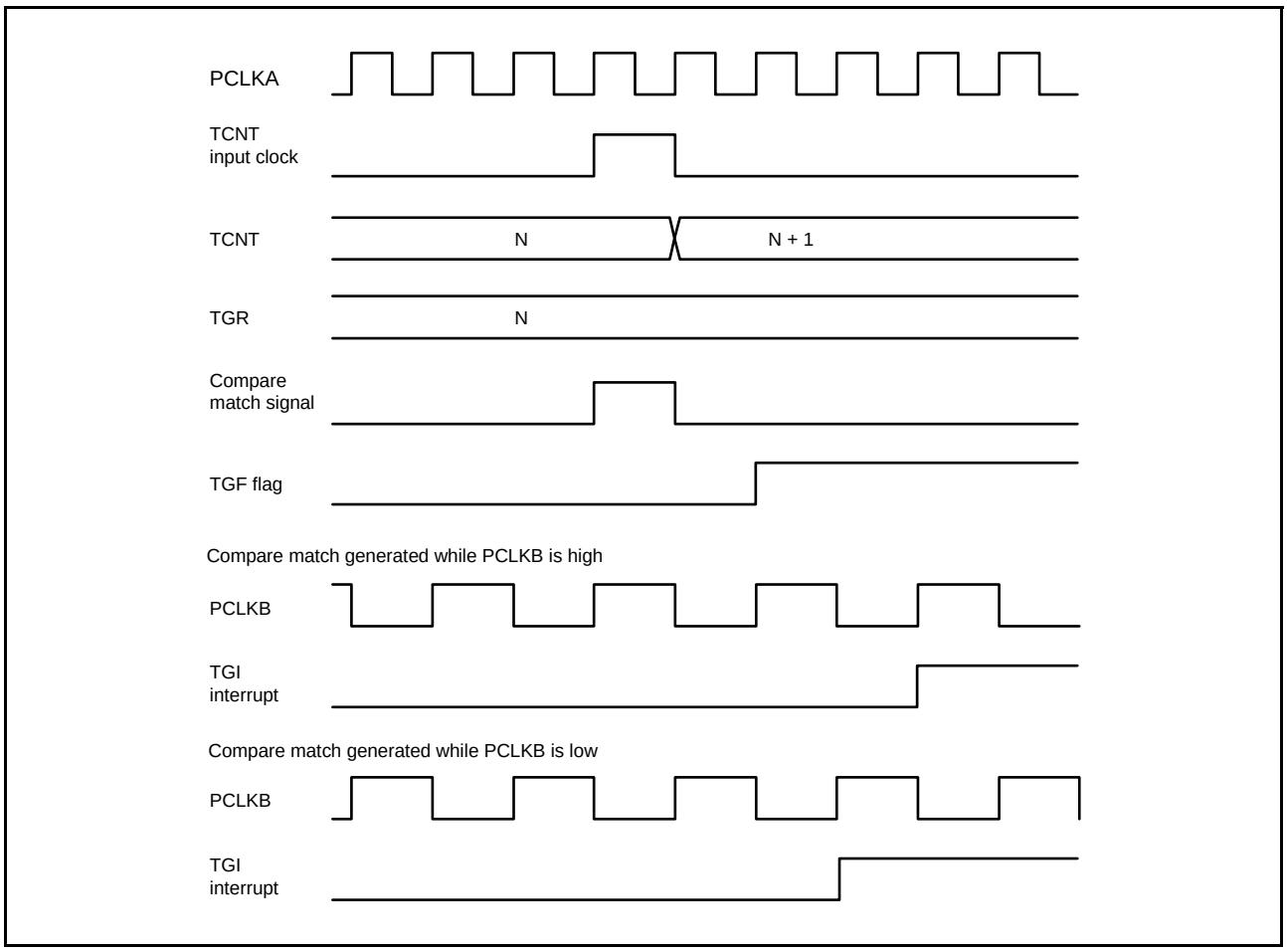


Figure 22.117 TGI Interrupt Timing (Compare Match) (MTU0 to MTU4, MTU6, and MTU7)

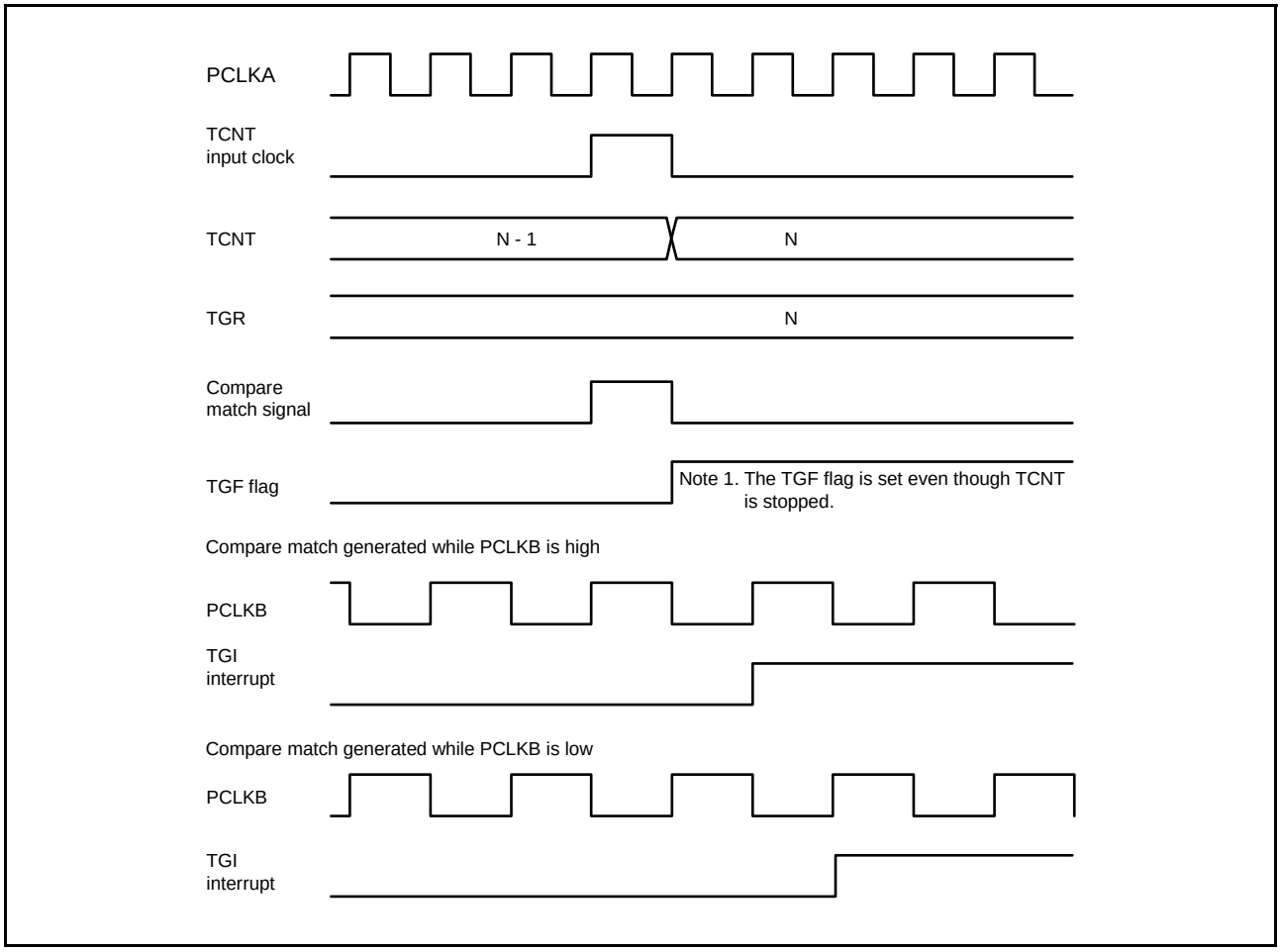


Figure 22.118 TGI Interrupt Timing (Compare Match) (MTU5)

(2) Timing for TGF Flag Setting by Input Capture

Figure 22.119 and Figure 22.120 show the timing of TGF flag setting in TSR on input capture and the TGI interrupt request signal timing.

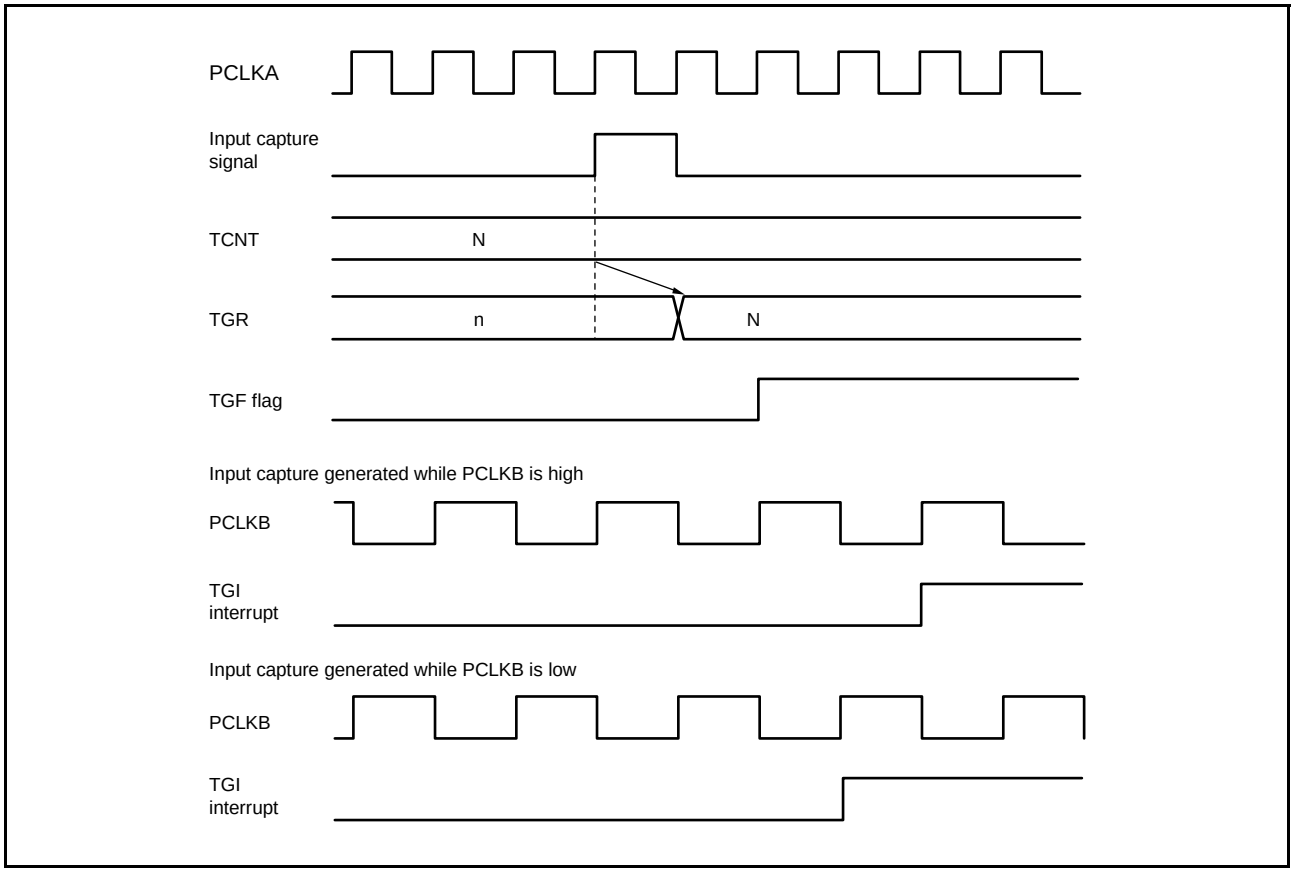


Figure 22.119 TGI Interrupt Timing (Input Capture) (MTU0 to MTU4, MTU6, and MTU7)

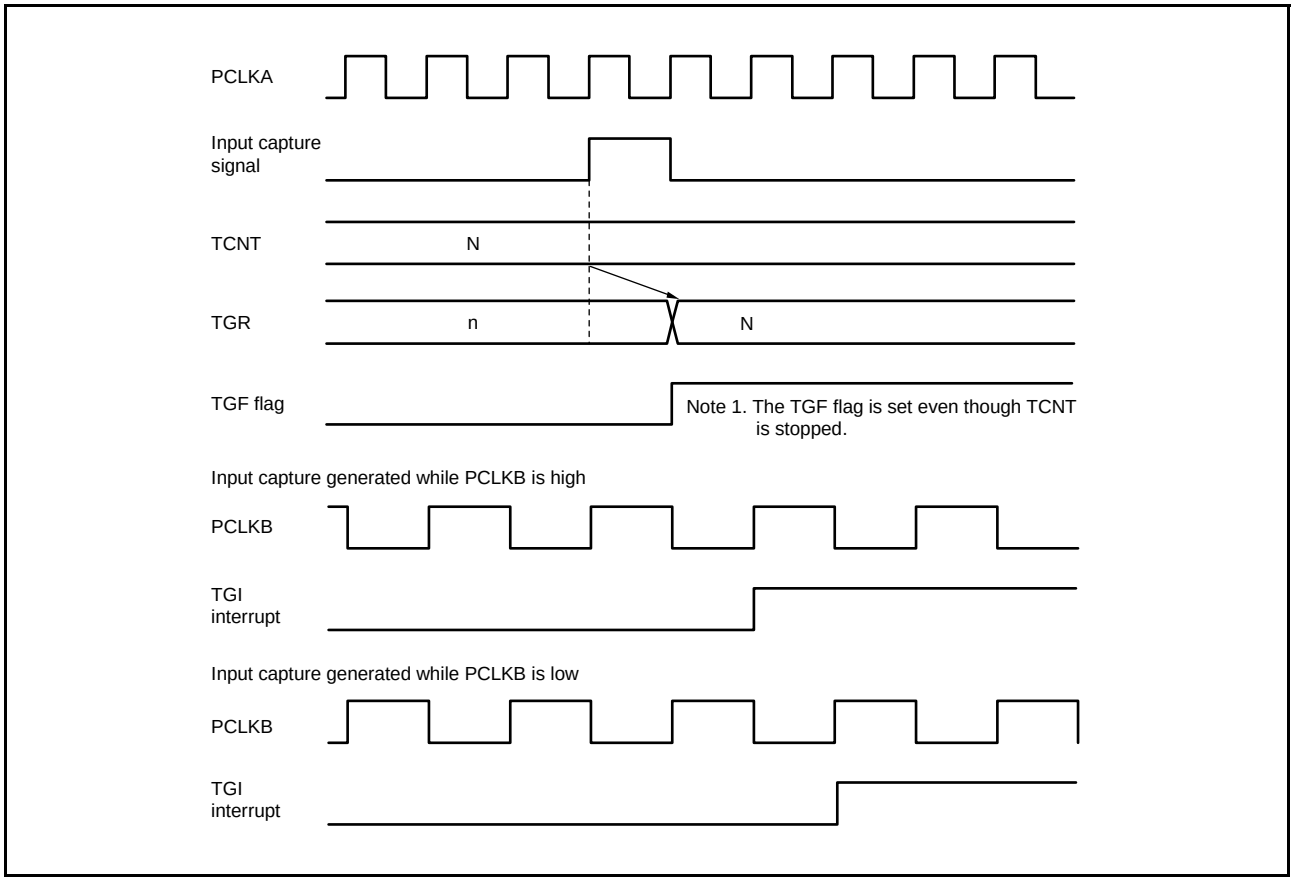


Figure 22.120 TGI Interrupt Timing (Input Capture) (MTU5)

(3) TCFV and TCFU Interrupt Timing

Figure 22.121 shows the timing of TCFV flag setting in TSR on overflow and the TCIV interrupt request signal timing. Figure 22.122 shows the timing of TCFU flag setting in TSR on underflow and the TCIU interrupt request signal timing.

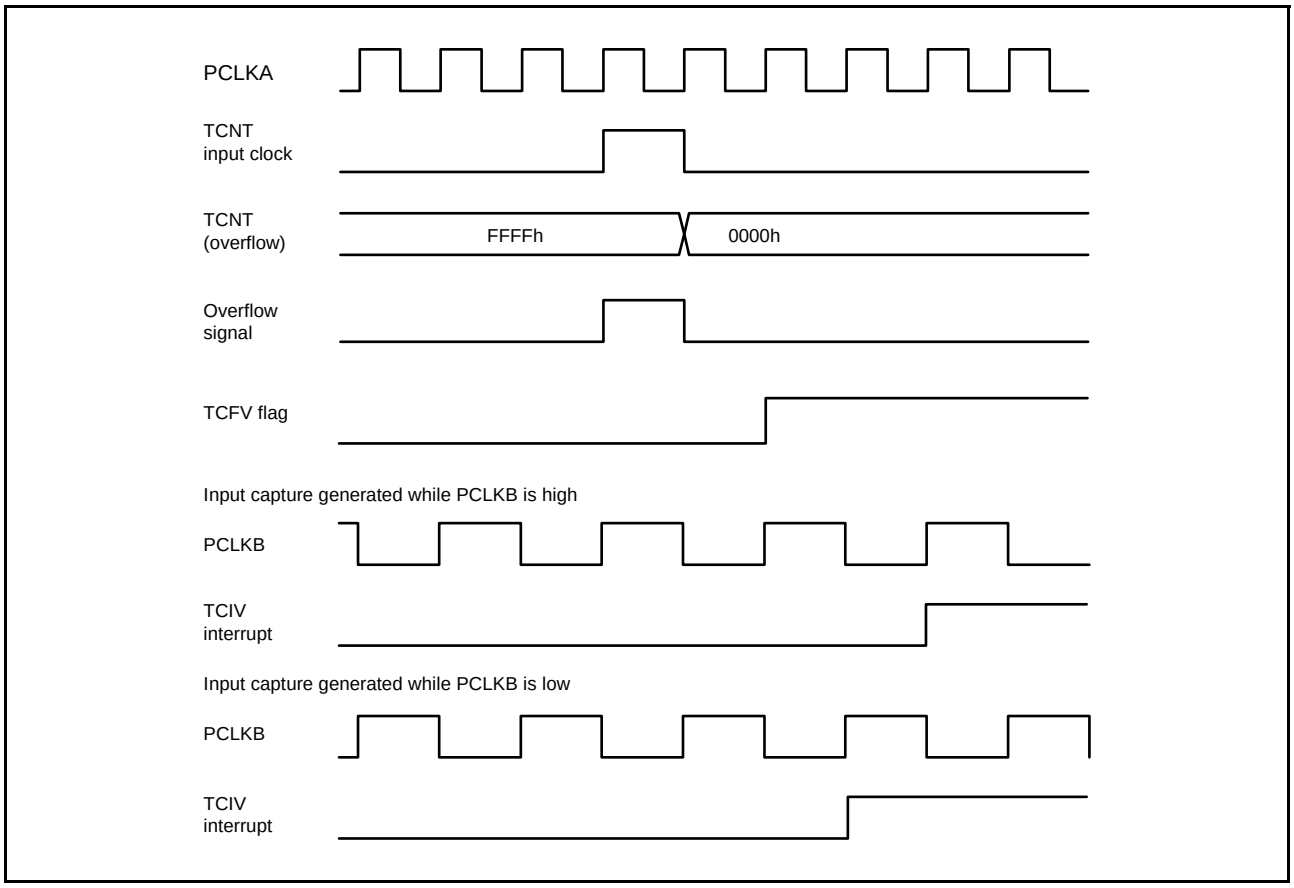


Figure 22.121 TCIV Interrupt Setting Timing

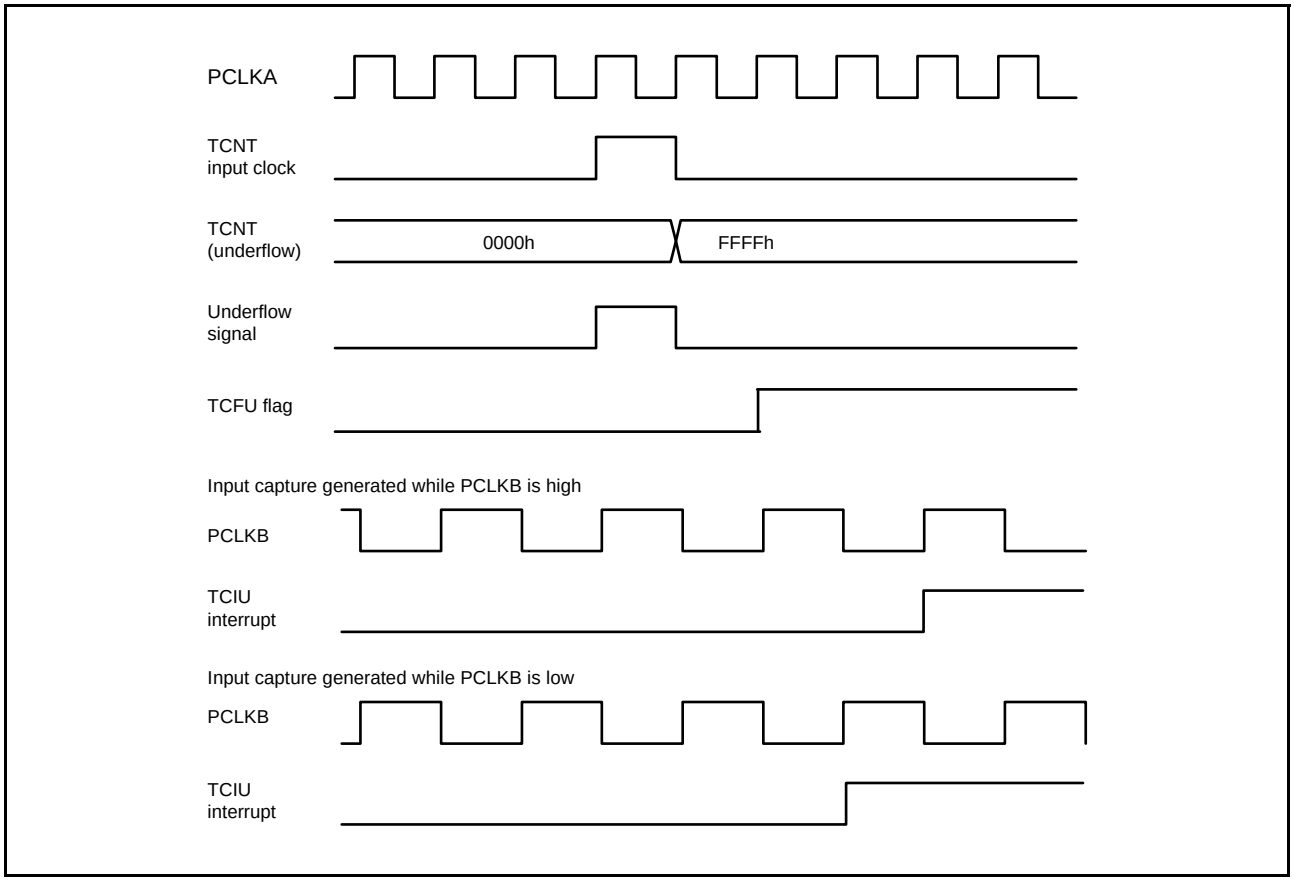


Figure 22.122 TCIU Interrupt Setting Timing

(4) Status Flag Clearing Timing

After the CPU reads a status flag as 1, it is cleared by writing 0 to it. Figure 22.123 shows the timing for status flag clearing by the CPU.

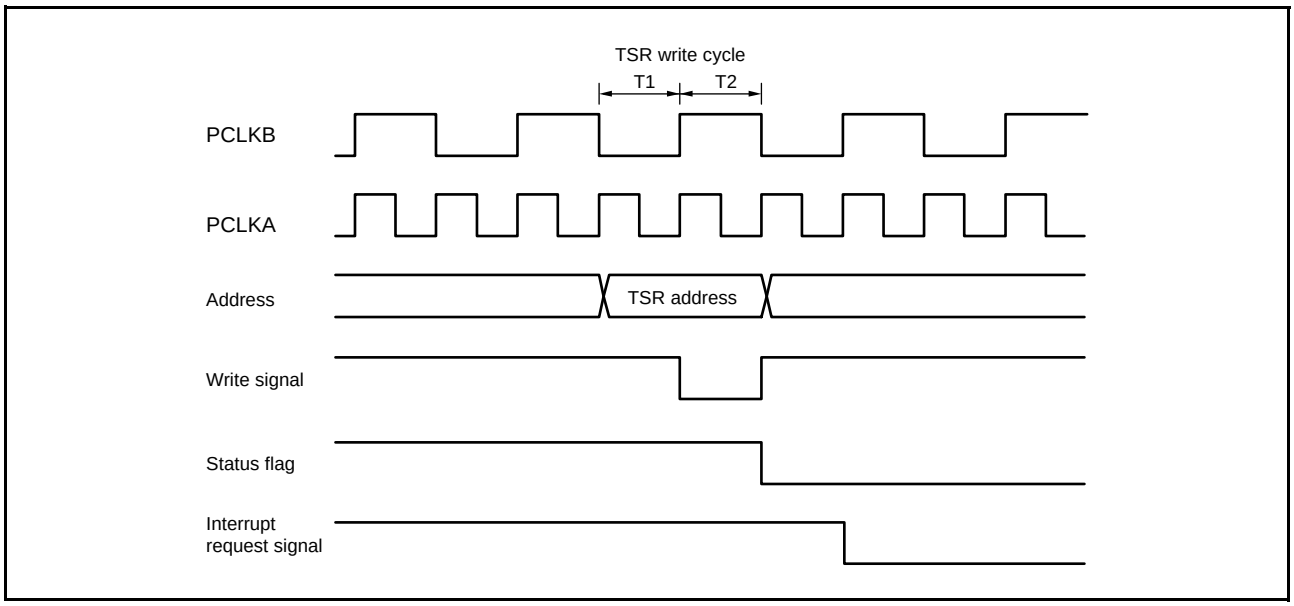


Figure 22.123 Timing for Status Flag Clearing by CPU (MTU0 to MTU7)

22.6 Usage Notes

22.6.1 Module Stop Function Setting

MTU operation can be disabled or enabled using the module stop control register. MTU operation is stopped with the initial setting. Register access is enabled by clearing the module clock stop state. For details, refer to section 12, Low Power Consumption.

22.6.2 Input Clock Restrictions

The input clock pulse width must be at least 3 cycles of PCLKA clock for single-edge detection, and at least 5 cycles of PCLKA clock for both-edge detection. The MTU will not operate properly at narrower pulse widths.
In phase counting mode, the phase difference and overlap between the two input clocks must be at least 3 cycles of PCLKA clock, and the pulse width must be at least 5 cycles of PCLKA clock. Figure 22.124 shows the input clock conditions in phase counting mode.

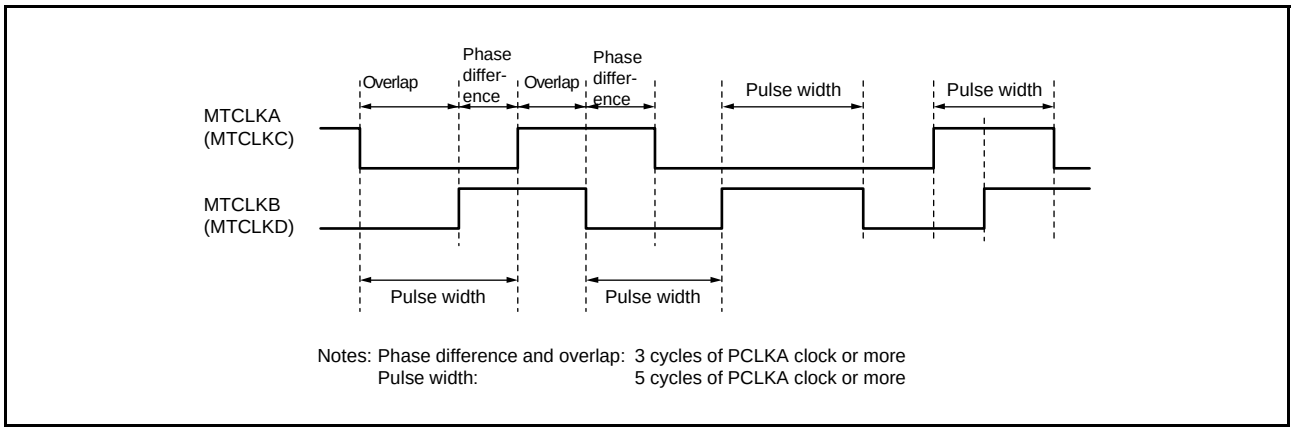


Figure 22.124 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

22.6.3 Note on Cycle Setting

When counter clearing on compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which TCNT updates the matched count value). Consequently, the actual counter frequency is given by the following formula:

- MTU0 to MTU4, MTU6, and MTU7

$$f = \frac{CNTCLK}{(N+1)}$$

- MTU5

$$f = \frac{CNTCLK}{N}$$

f: Counter frequency
CNTCLK: The counter-clock frequency set by TCR.TPSC[2:0].
N: TGR setting

22.6.4 Contention between TCNT Write and Clear Operations

If the counter clear signal is generated in a TCNT write cycle, TCNT clearing takes precedence and TCNT write operation is not performed.
Figure 22.125 shows the timing in this case.

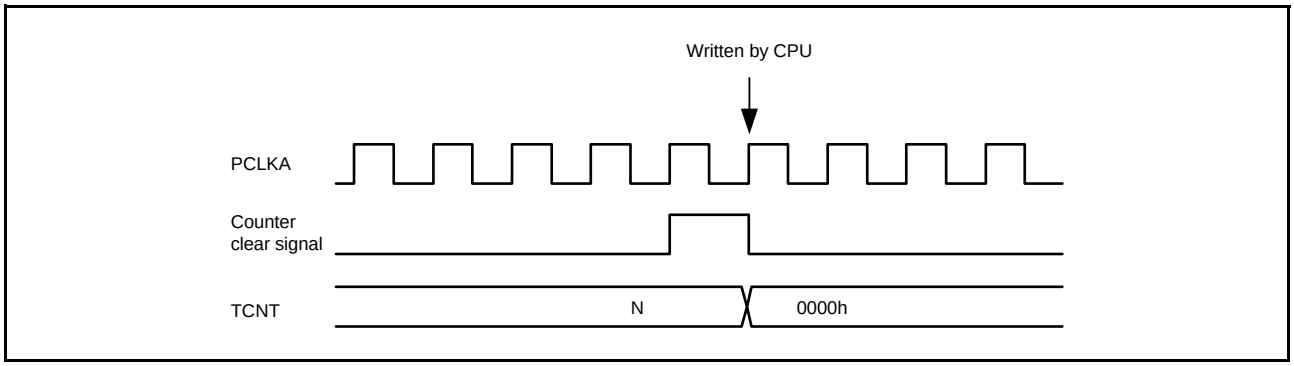


Figure 22.125 Contention between TCNT Write and Clear Operations

22.6.5 Contention between TCNT Write and Increment Operations

If incrementing occurs in a TCNT write cycle, TCNT write operation takes precedence and TCNT is not incremented.
Figure 22.126 shows the timing in this case.

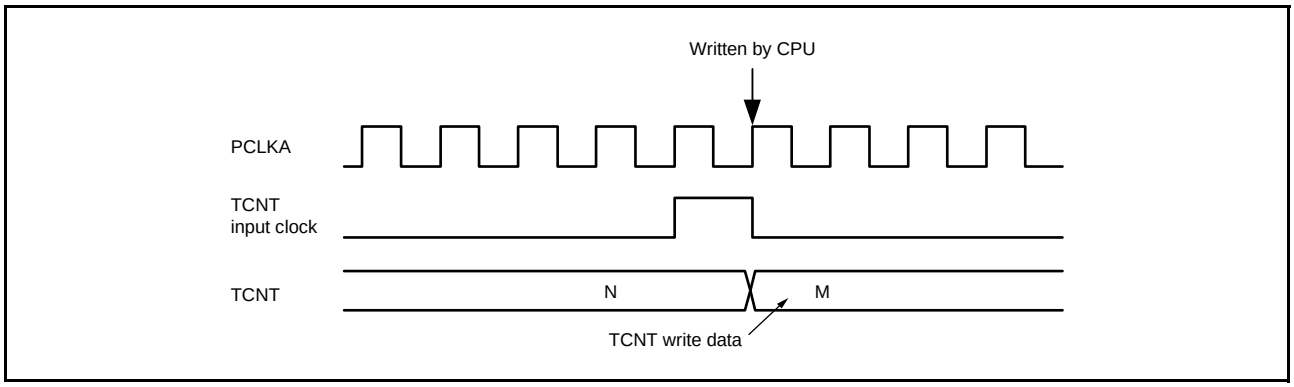


Figure 22.126 Contention between TCNT Write and Increment Operations

22.6.6 Contention between TGR Write Operation and Compare Match

If a compare match occurs in a TGR write cycle, TGR write operation is executed and the compare match signal is also generated.
Figure 22.127 shows the timing in this case.

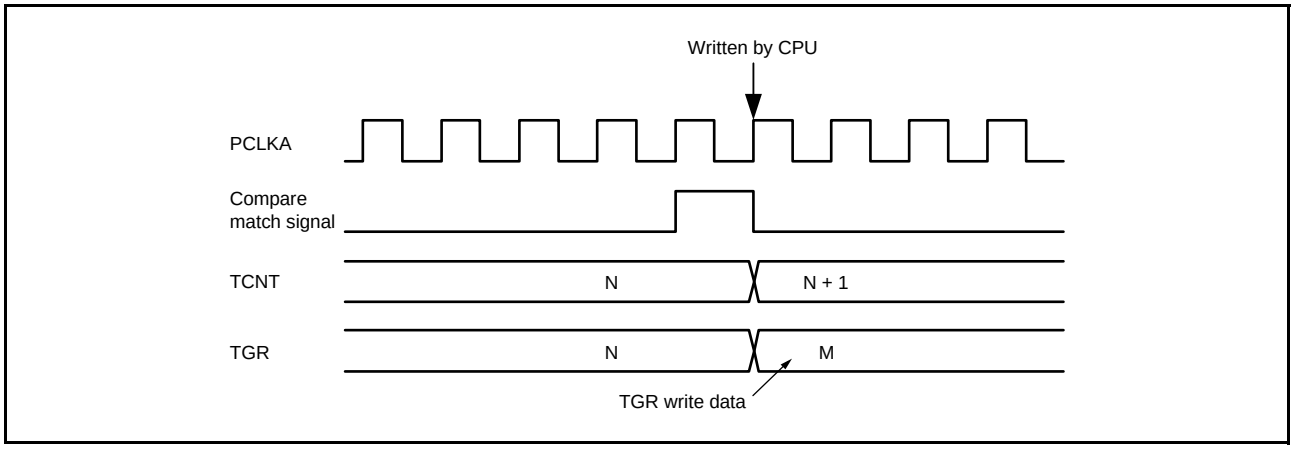


Figure 22.127 Contention between TGR Write Operation and Compare Match

22.6.7 Contention between Buffer Register Write Operation and Compare Match

If a compare match occurs in a TGR write cycle, the data before write operation is transferred to TGR by the buffer operation.
Figure 22.128 shows the timing in this case.

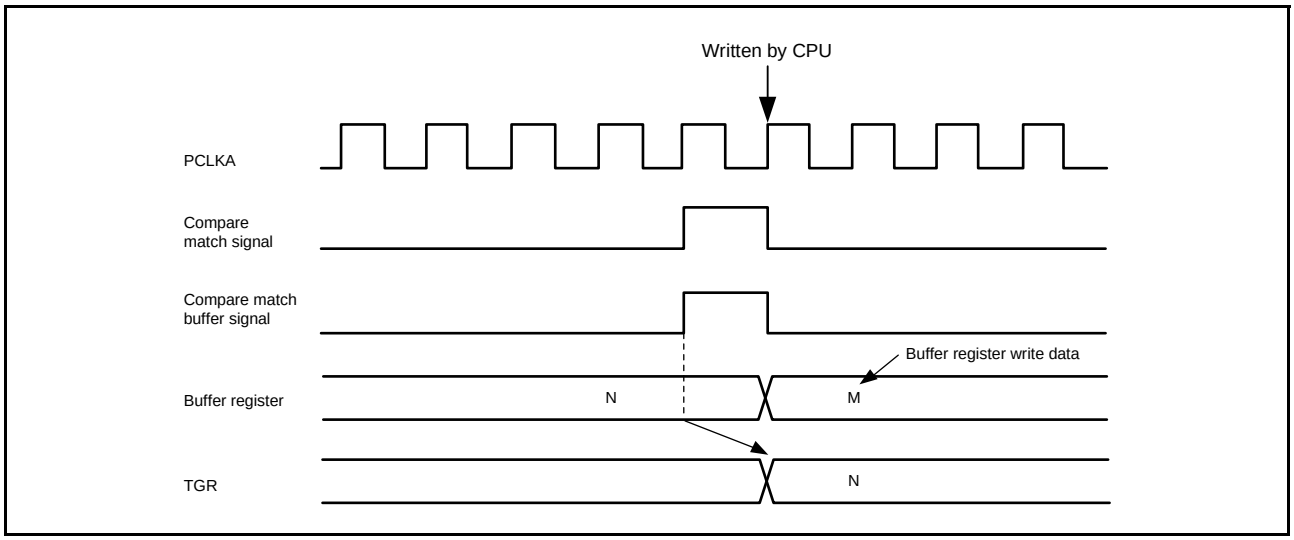


Figure 22.128 Contention between Buffer Register Write Operation and Compare Match

22.6.8 Contention between Buffer Register Write and TCNT Clear Operations

When the buffer transfer timing is set at the TCNT clear timing by the timer buffer operation transfer mode register (TBTM), if TCNT clearing occurs in a TGR write cycle, the data before write operation is transferred to TGR by the buffer operation.
Figure 22.129 shows the timing in this case.

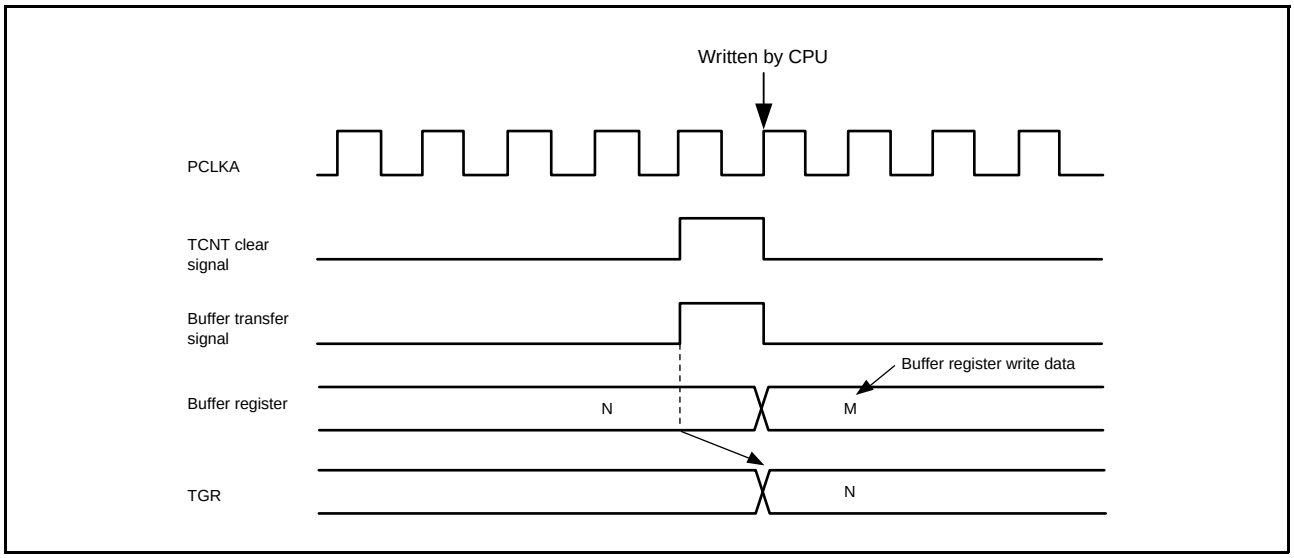


Figure 22.129 Contention between Buffer Register Write and TCNT Clear Operations

22.6.9 Contention between TGR Read Operation and Input Capture

If an input capture signal is generated in the T1 state in a TGR read cycle, the data before input capture transfer is read. Figure 22.130 show the timing in this case.

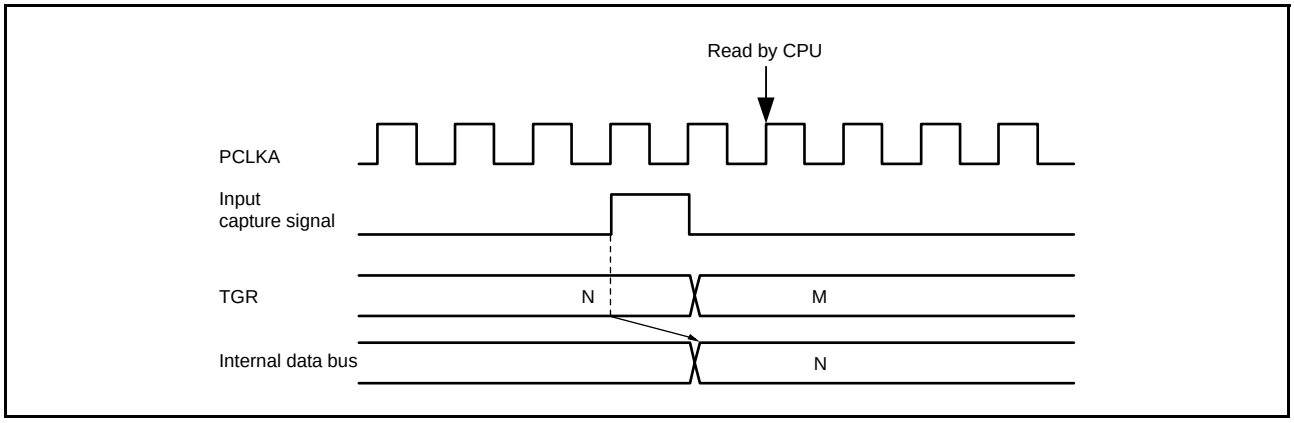


Figure 22.130 Contention between TGR Read Operation and Input Capture (MTU0 to MTU7)

22.6.10 Contention between TGR Write Operation and Input Capture

If an input capture signal is generated in a TGR write cycle, the input capture operation takes precedence and the TGR write operation is not performed in MTU0 to MTU4, MTU6, and MTU7. In MTU5, the TGR write operation is performed and the input capture signal is generated.
Figure 22.131 and Figure 22.132 show the timing in this case.

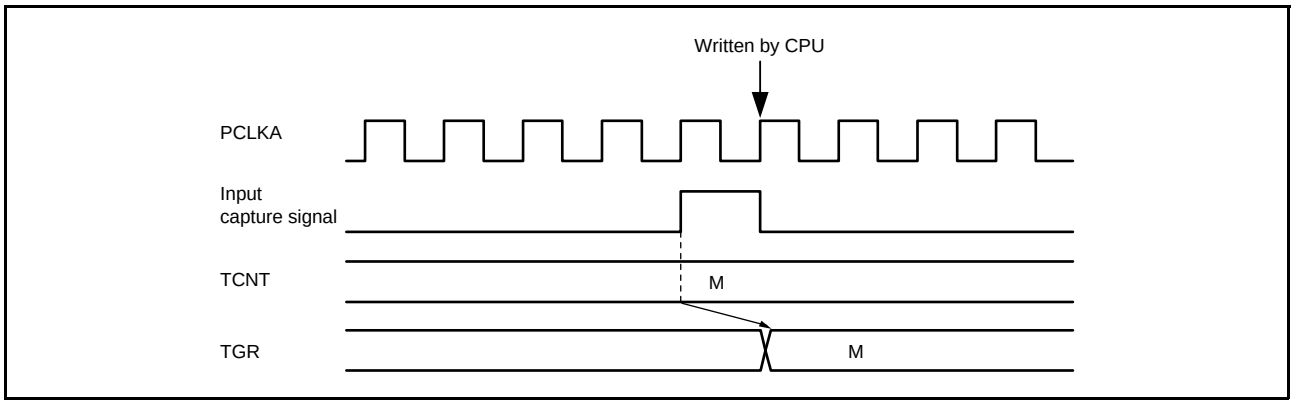


Figure 22.131 Contention between TGR Write Operation and Input Capture (MTU0 to MTU4, MTU6, and MTU7)

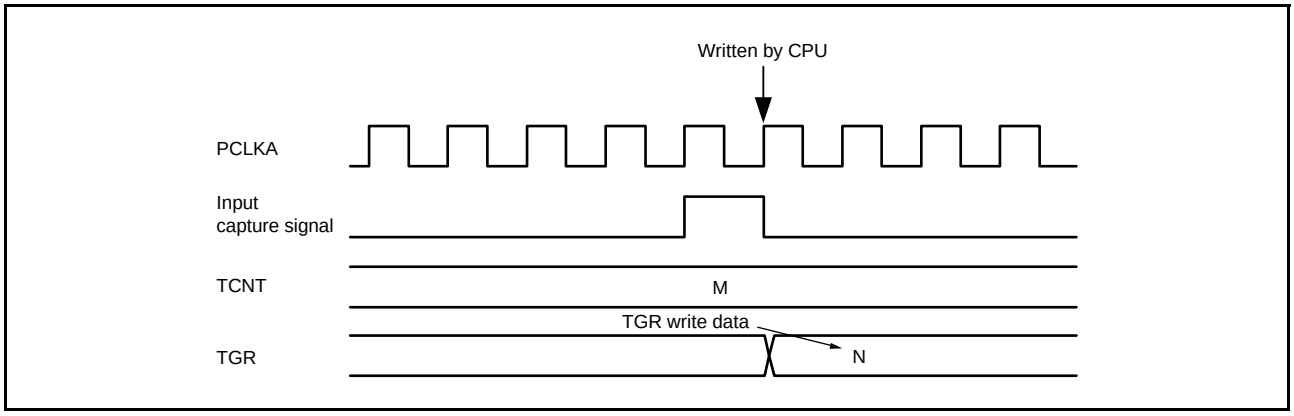


Figure 22.132 Contention between TGR Write Operation and Input Capture (MTU5)

22.6.11 Contention between Buffer Register Write Operation and Input Capture

If an input capture signal is generated in a buffer register write cycle, the buffer operation takes precedence and the buffer register write operation is not performed.

Figure 22.133 shows the timing in this case.

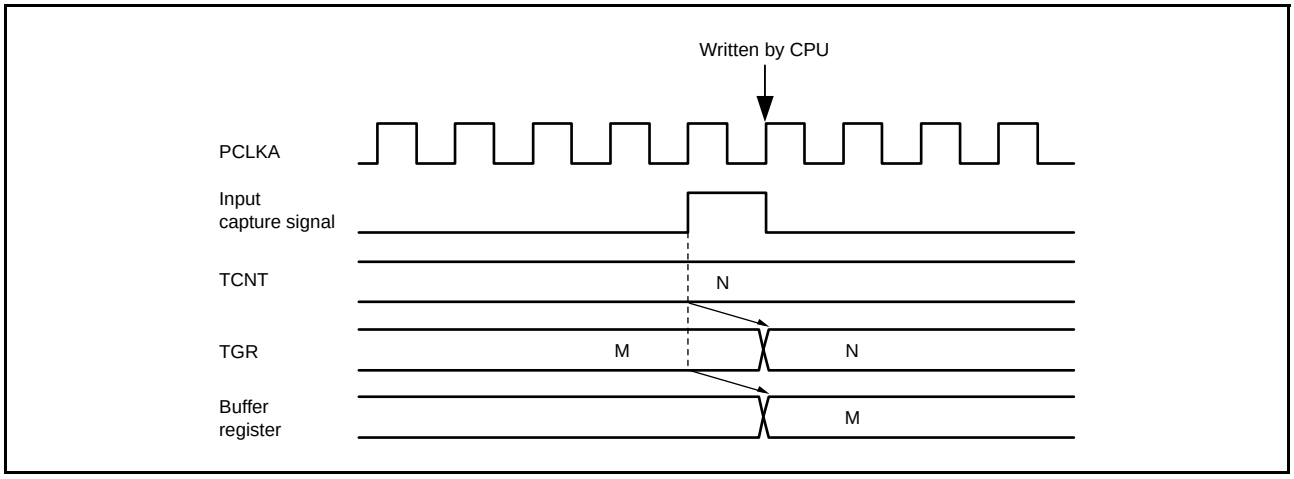


Figure 22.133 Contention between Buffer Register Write Operation and Input Capture

22.6.12 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation

With timer counters MTU1.TCNT and MTU2.TCNT in a cascade, when a contention occurs between MTU1.TCNT counting (an MTU2.TCNT overflow/underflow) and the MTU2.TCNT write cycle, the MTU2.TCNT write operation is performed and the MTU1.TCNT count signal is disabled. In this case, if MTU1.TGRA works as a compare match register and there is a match between the MTU1.TGRA and MTU1.TCNT values, a compare match signal is issued. Furthermore, when the MTU1.TCNT count clock is selected as the input capture source of MTU0, MTU0.TGRA to MTU0.TGRD work in input capture mode. In addition, when the MTU0.TGRC compare match/input capture is selected as the input capture source of MTU1.TGRB, MTU1.TGRB works in input capture mode.
Figure 22.134 shows the timing in this case.
When setting the TCNT clearing function in cascaded operation, be sure to synchronize MTU1 and MTU2.

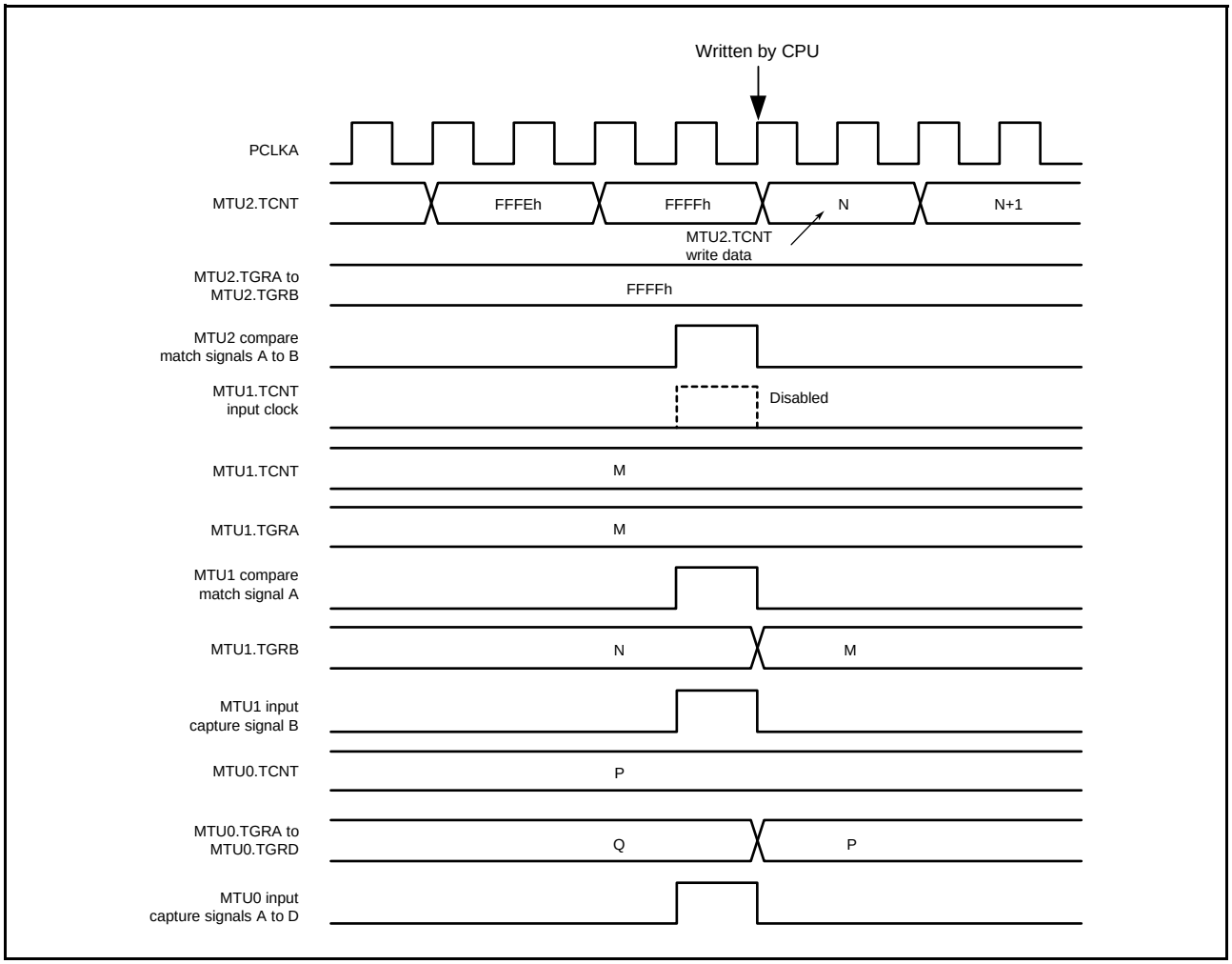


Figure 22.134 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation

22.6.13 Counter Value when Stopped in Complementary PWM Mode

When counting operation in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) is stopped in complementary PWM mode, the MTU3.TCNT (MTU6.TCNT) value is set to the timer dead time register (TDDRA (TDDRB)) value and MTU4.TCNT (MTU7.TCNT) is set to 0000h.
When operation is restarted in complementary PWM mode, counting begins automatically from the initial setting state. Figure 22.135 shows this operation.
When counting begins in another operating mode, be sure to make initial settings in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT).

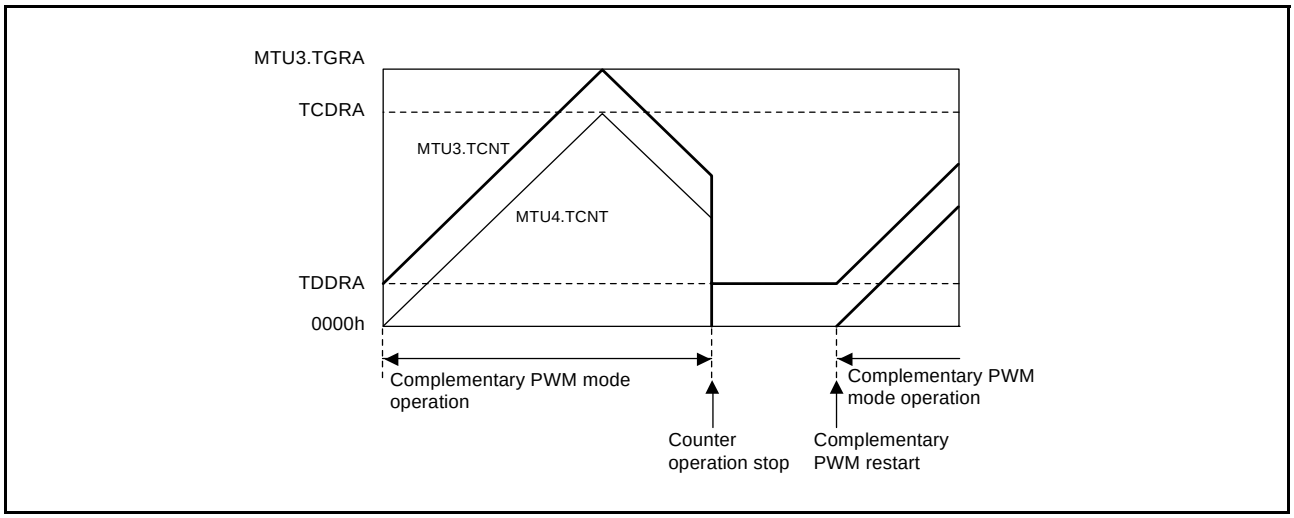


Figure 22.135 Counter Value when Stopped in Complementary PWM Mode

22.6.14 Buffer Operation Setting in Complementary PWM Mode

When modifying the PWM cycle set register (MTU3.TGRA or MTU6.TGRA), timer cycle data register (TCDRA or TCDRB), and duty set registers (MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB (MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB)) in complementary PWM mode, be sure to use buffer operation. In addition, set the MTU4.TMDR1.BFA (MTU7.TMDR1.BFA) and MTU4.TMDR1.BFB(MTU7.TMDR1.BFB) bits to 0. The MTIOC4C (MTIOC7C) pin cannot output waveforms if the MTU4.TMDR1.BFA(MTU7.TMDR1.BFA) bit is set to 1. Likewise, the MTIOC4D (MTIOC7D) pin cannot output waveforms if the BFB bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1.
In complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in the MTU3.TMDR1.BFA(MTU6.TMDR1.BFA) and MTU3.TMDR1.BFB (MTU6.TMDR1.BFB) bits. When the MTU3.TMDR1.BFA (MTU6.TMDR1.BFA) bit is set to 1, MTU3.TGRC (MTU6.TGRC) functions as a buffer register for MTU3.TGRA (MTU6.TGRA). At the same time, MTU4.TGRC (MTU7.TGRC) functions as a buffer register for MTU4.TGRA (MTU7.TGRA), and TCBRA (TCBRB) functions as a buffer register for TCDRA (TCDRB).

22.6.15 Buffer Operation and Compare Match Flags in Reset-Synchronized PWM Mode

When setting buffer operation in reset-synchronized PWM mode, set the MTU4.TMDR1.BFA (MTU7.TMDR1.BFA) bit to 0. The MTIOC4C (MTIOC7C) pin cannot output waveforms if the MTU4.TMDR1.BFB (MTU7.TMDR1.BFB) bits is set to 1. Likewise, the MTIOC4D (MTIOC7D) pin cannot output waveforms if the MTU4.TMDR1.BFB (MTU7.TMDR1.BFB) bit is set to 1.

In reset-synchronized PWM mode, buffer operation in MTU3 and MTU4 (or MTU 6 and MTU7) depends on the settings in the MTU3.TMDR1.BFA (MTU6.TMDR1.BFA) and MTU3.TMDR1.BFB (MTU6.TMDR1.BFB) bits. For example, if the MTU3.TMDR1.BFA (MTU6.TMDR1.BFA) bit is set to 1, MTU3.TGRC (MTU6.TGRC) functions as a buffer register for MTU3.TGRA (MTU6.TGRA). At the same time, MTU4.TGRC (MTU7.TGRC) functions as a buffer register for MTU4.TGRA (MTU7.TGRA).

While the MTU3.TGRC (MTU6.TGRC) and MTU3.TGRD (MTU6.TGRD) are operating as buffer registers, the MTU3.TSR.TGFC and MTU3.TSR.TGFD (MTU6.TSR.TGFC and MTU6.TSR.TGFD) bits and the MTU4.TSR.TGFC and MTU4.TSR.TGFD (MTU7.TSR.TGFC and MTU7.TSR.TGFD) bits are never set.

Figure 22.136 shows an example of the operation of the bits MTU3.TGR (MTU6.TGR), MTU4.TGR (MTU7.TGR), MTIOC3A (MTIOC6A), MTIOC3B (MTIOC6B), MTIOC3D (MTIOC6D), MTIOC4m (MTIOC7m) (m = A to D) with the MTU3.TMDR1.BFA (MTU6.TMDR1.BFA) and MTU3.TMDR1.BFB (MTU6.TMDR1.BFB) bits set to 1 and the MTU4.TMDR1.BFA (MTU7.TMDR1.BFA) and MTU4.TMDR1.BFB (MTU7.TMDR1.BFB) bits set to 0.

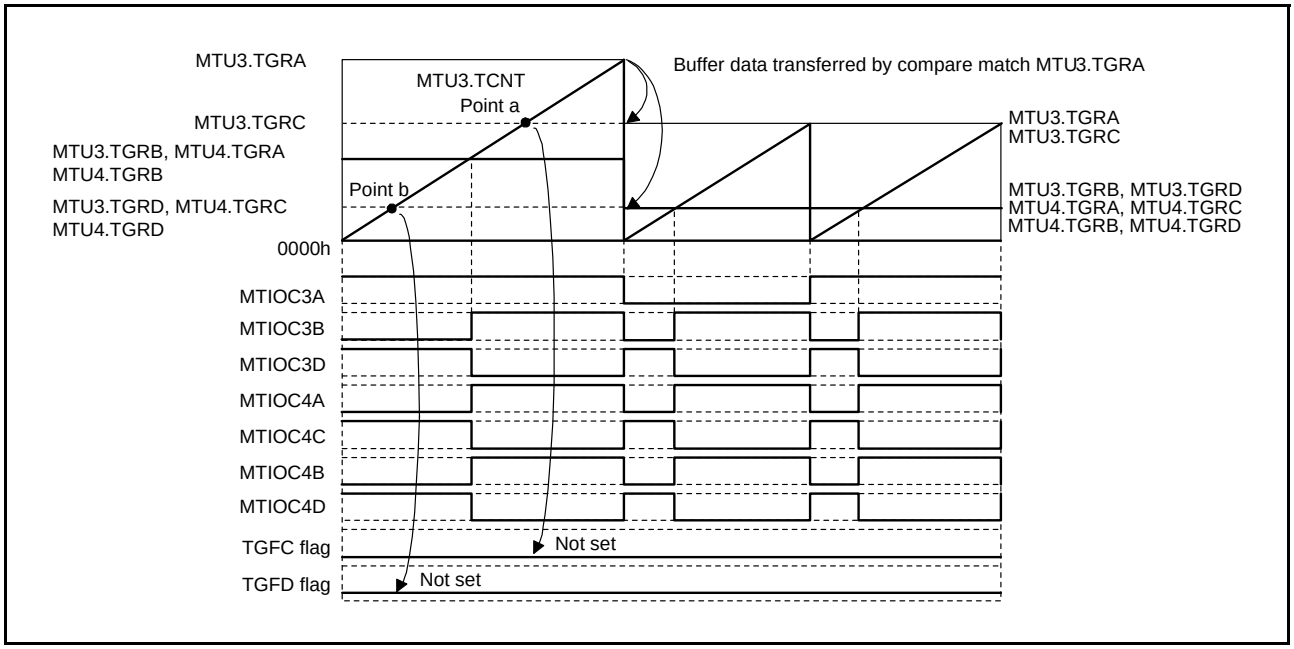


Figure 22.136 Buffer Operation and Compare Match Flags in Reset-Synchronized PWM Mode

22.6.16 Overflow Flags in Reset-Synchronized PWM Mode

After reset-synchronized PWM mode is selected, MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) start counting when the TSTRA.CST3 (TSTRB.CST6) bits is set to 1. In this state, the MTU4.TCNT (MTU7.TCNT) count clock source and count edge are determined by the MTU3.TCR (MTU6.TCR) setting.
In reset-synchronized PWM mode, with cycle register MTU3.TGRA (MTU6.TGRA) set to FFFFh and the MTU3.TGRA (MTU6.TGRA) compare match selected as the counter clearing source, MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) count up to FFFFh, then a compare match occurs with MTU3.TGRA (MTU6.TGRA), and MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) are both cleared. In this case, the TCFV flag in TSR is not set.
Figure 22.137 shows an example of TCFV flag operation in reset-synchronized PWM mode with cycle register MTU3.TGRA (MTU6.TGRA) set to FFFFh and the MTU3.TGRA (MTU6.TGRA) compare match specified for the counter clearing source.

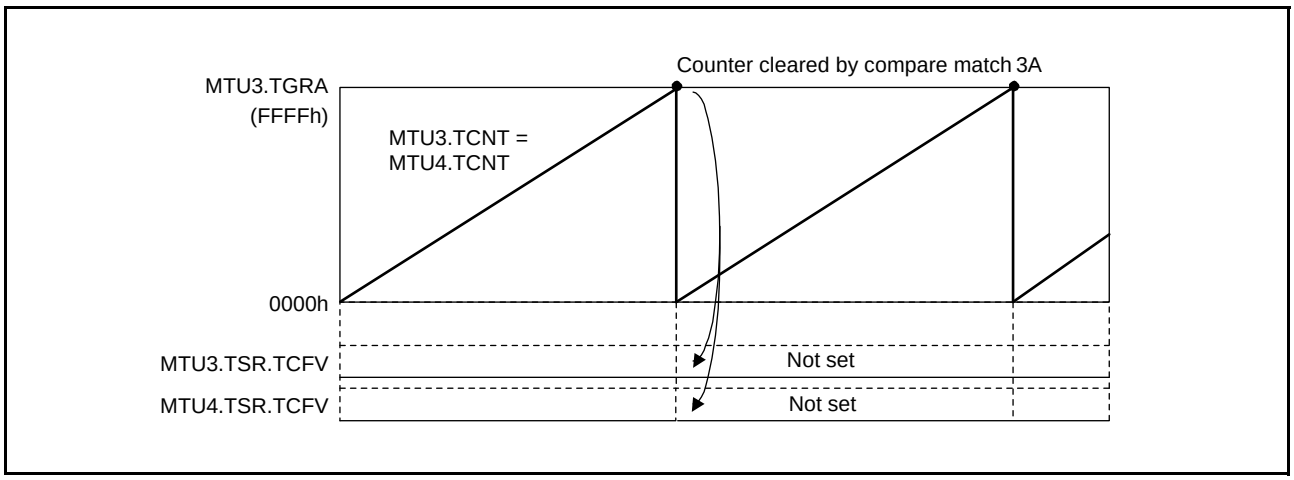


Figure 22.137 Overflow Flags in Reset-Synchronized PWM Mode

22.6.17 Contention between Overflow/Underflow and Counter Clearing

If an overflow/underflow and counter clearing occur simultaneously, the TCFV/TCFU flag in TSR is not set and TCNT clearing takes precedence.

Figure 22.138 shows the operation timing when a TGR compare match is specified as the clearing source and TGR is set to FFFFh.

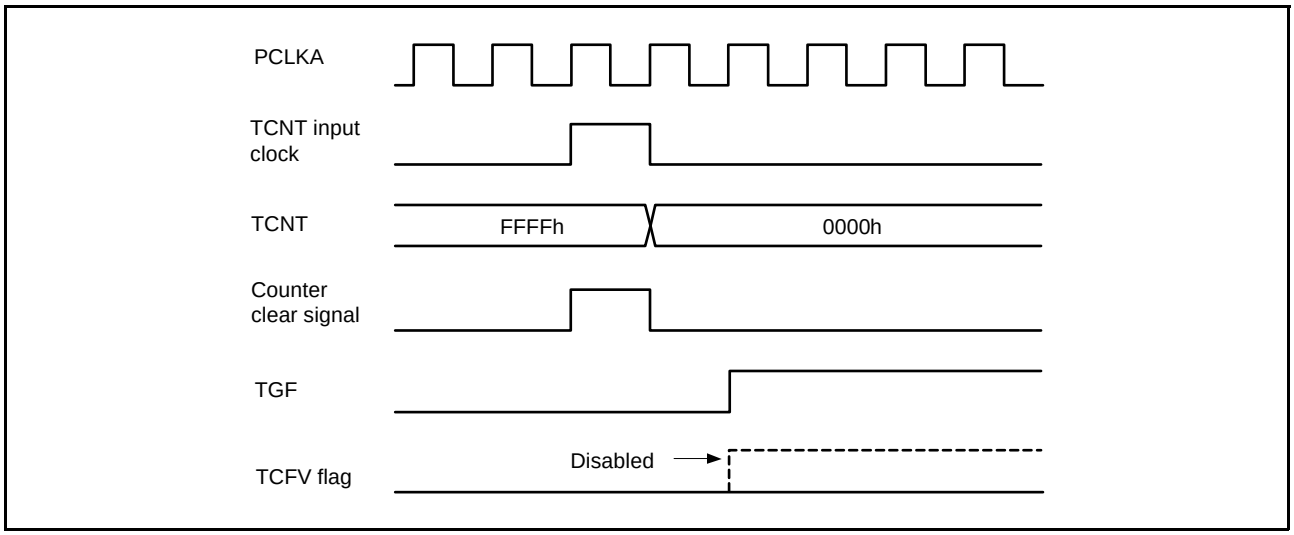


Figure 22.138 Contention between Overflow and Counter Clearing

22.6.18 Contention between TCNT Write Operation and Overflow/Underflow

If TCNT counts up or down in a TCNT write cycle and an overflow or an underflow occurs, the TCNT write operation takes precedence and the TCFV/TCFU flag in TSR is not set.

Figure 22.139 shows the operation timing when there is contention between TCNT write operation and overflow.

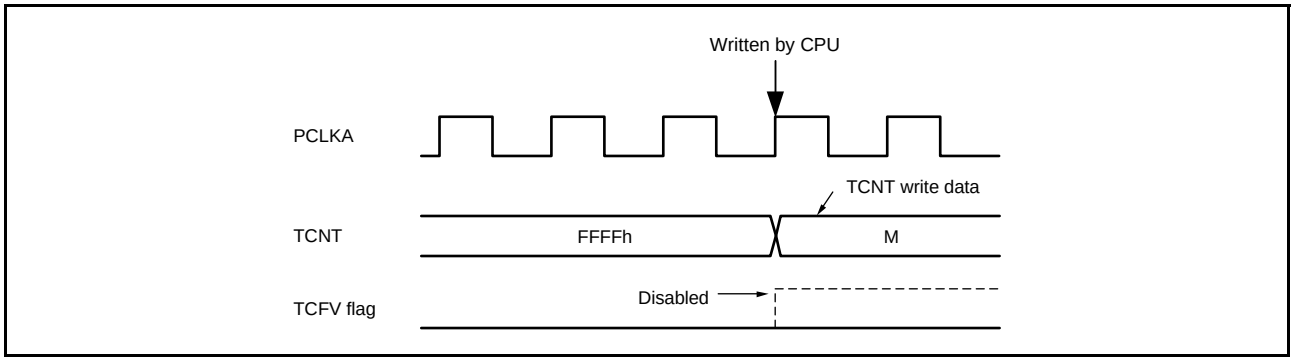


Figure 22.139 Contention between TCNT Write Operation and Overflow

22.6.19 Note on Transition from Normal Mode or PWM Mode 1 to Reset-Synchronized PWM Mode

When making a transition from normal mode or PWM mode 1 to reset-synchronized PWM mode in MTU3 and MTU4 (or MTU6 and MTU7), if the counter is stopped while the output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D) are held at a high level and then operation is started after a transition to reset-synchronized PWM mode, the initial pin output will not be correct.

When making a transition from normal mode to reset-synchronized PWM mode, write 11h to MTU3.TIORH, MTU3.TIORL, MTU4.TIORH, and MTU4.TIORL (MTU6.TIORH, MTU6.TIORL, MTU7.TIORH, and MTU7.TIORL) to initialize the output pin state to a low level, then set the registers to the initial value (00h) before making the mode transition.

When making a transition from PWM mode 1 to reset-synchronized PWM mode, switch to normal mode, initialize the output pin state to a low level, and then set the registers to the initial value (00h) before making the transition to reset-synchronized PWM mode.

22.6.20 Output Level in Complementary PWM Mode and Reset-Synchronized PWM Mode

When MTU3 and MTU4 (or MTU6 and MTU7) are in complementary PWM mode or reset-synchronized PWM mode, the PWM waveform output level is determined by the TOCR1A.OLSP, TOCR1A.OLSN, TOCR1B.OLSP, and TOCR1B.OLSN bits. In complementary PWM mode or reset-synchronized PWM mode, TIOR should be set to 00h.

22.6.21 Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection

When timer counters 1 and 2 (MTU1.TCNT and MTU2.TCNT) operate as a 32-bit counter in cascade connection, the cascaded counter value cannot be captured successfully in some cases even if input-capture input is simultaneously done to MTIOC1A and MTIOC2A or to MTIOC1B and MTIOC2B. This is because the input timing of MTIOC1A and MTIOC2A or to MTIOC1B and MTIOC2B may not be the same when external input-capture signals input into MTU1.TCNT and MTU2.TCNT are taken in synchronization with the internal clock.

For example, MTU1.TCNT (the counter for upper 16 bits) does not capture the count-up value by an overflow from MTU2.TCNT (the counter for lower 16 bits) but captures the count value before the up-counting. In this case, the values of MTU1.TCNT = FFF1h and MTU2.TCNT = 0000h should be transferred to MTU1.TGRA and MTU2.TGRA or to MTU1.TGRB and MTU2.TGRB, but the values of MTU1.TCNT = FFF0h and MTU2.TCNT = 0000h are erroneously transferred.

22.6.22 Interrupt-Skipping Function 2

When interrupt-skipping function 2 is in use and the difference between the values in MTU4.TADCORA and MTU4.TADCORB is small, correct counting of the number skipped may not be possible, in which case requests for A/D conversion will not be generated with the expected timing. The conditions listed below thus apply to these settings.
For MTU6 and MTU7, the same conditions apply to the settings of MTU7.TADCORA and MTU7.TADCORB.

(1) When the number skipped is zero for skipping function 2

- The difference between the values in MTU4.TADCORA and MTU4.TADCORB must be at least four.
- The interval of comparison for MTU4.TADCORA must be at least four cycles of PCLKA (the updated value of MTU4.TADCORA is set to the previous value plus or minus at least four).
- The interval of comparison for MTU4.TADCORB must be at least four cycles of PCLKA (the updated value of MTU4.TADCORB is set to the previous value plus or minus at least four).

(2) When the number skipped is one or more for skipping function 2

- The difference between the values in MTU4.TADCORA and MTU4.TADCORB must be at least two.
- The interval of comparison for MTU4.TADCORB must be at least two cycles of PCLKA (the updated value of MTU4.TADCORB is set to the previous value plus or minus at least two).

22.6.23 Note on Complementary PWM Mode when Output Protection Function is Not Used

Output protection function for complementary PWM mode is enabled at the initial state. To disable this function, write 00h to the POE.POECR2 register.

22.6.24 Preventing Malfunctions at Synchronous Clearing in Complementary PWM Mode

If control of the output waveform is enabled (TWCR.WRE = 1) at the time of synchronous counter clearing in complementary PWM mode, satisfaction of either condition 1 or 2 below has the following effects.

- Dead time on the PWM output pins is shortened (or eliminated).
- The active level is output on the PWM negative phase output pins beyond the period for active-level output.

Condition 1: In portion (10) of the initial output inhabitation period, synchronous clearing occurs within the dead time period for PWM output (see Figure 22.140).

Condition 2: In portions (10) and (11) of the initial inhabitation period, synchronous clearing occurs when any condition from among MTU3.TGRB (MTU6.TGRB) ≤ TDDRA (TDDRB), MTU4.TGRA (MTU7.TGRA) ≤ TDDRA (TDDRB), or MTU4.TGRB (MTU7.TGRB) ≤ TDDRA (TDDRB) (see Figure 22.141).

The following method avoids the above phenomena.

- Ensure that synchronous clearing proceeds with the value of each comparison register MTU3.TGRB (MTU6.TGRB) ≤ TDDRA (TDDRB), MTU4.TGRA (MTU7.TGRA) ≤ TDDRA (TDDRB), and MTU4.TGRB (MTU7.TGRB) ≤ TDDRA (TDDRB) set to at least double the value of the dead time register TDDRA (TDDRB).

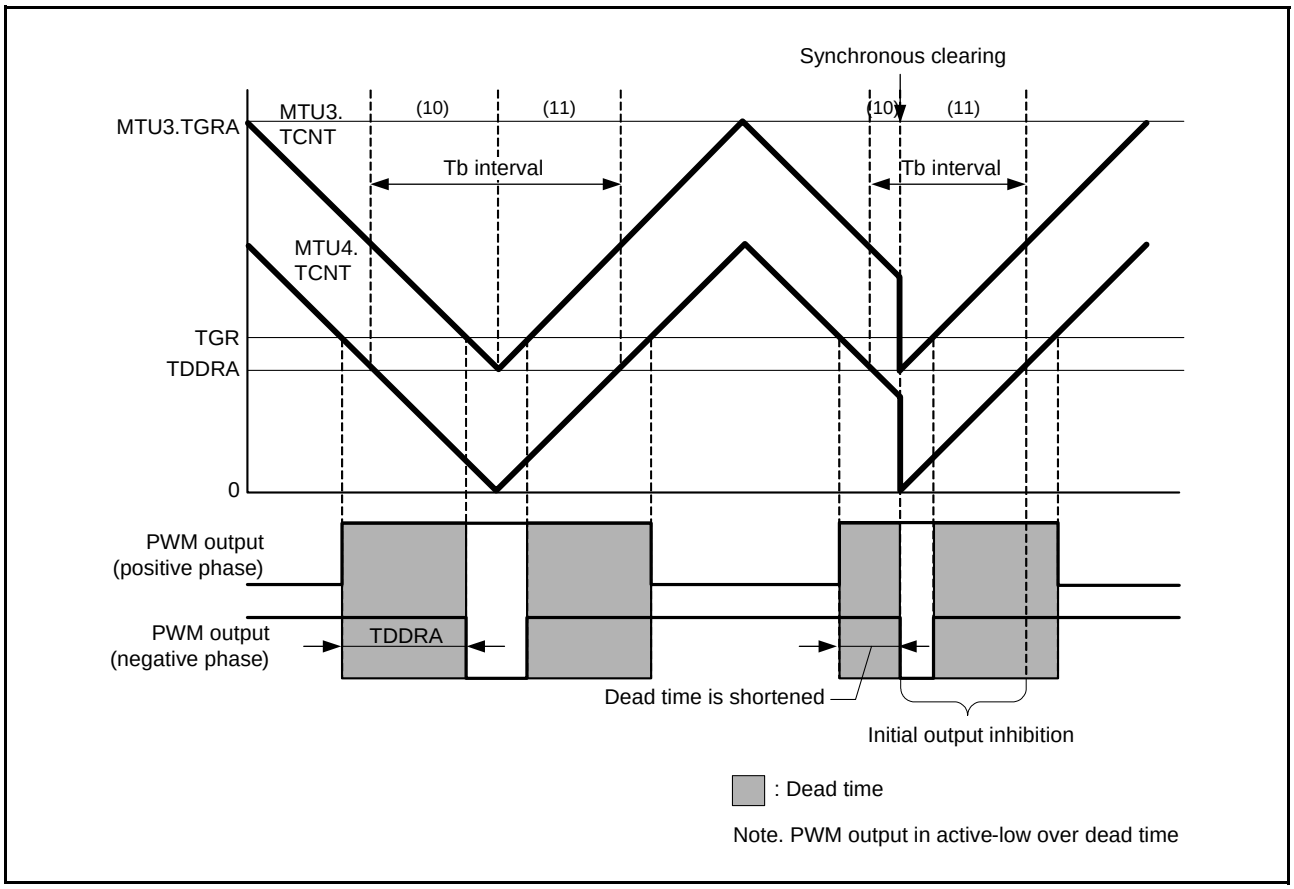


Figure 22.140 Example of Synchronous Clearing (Condition 1)

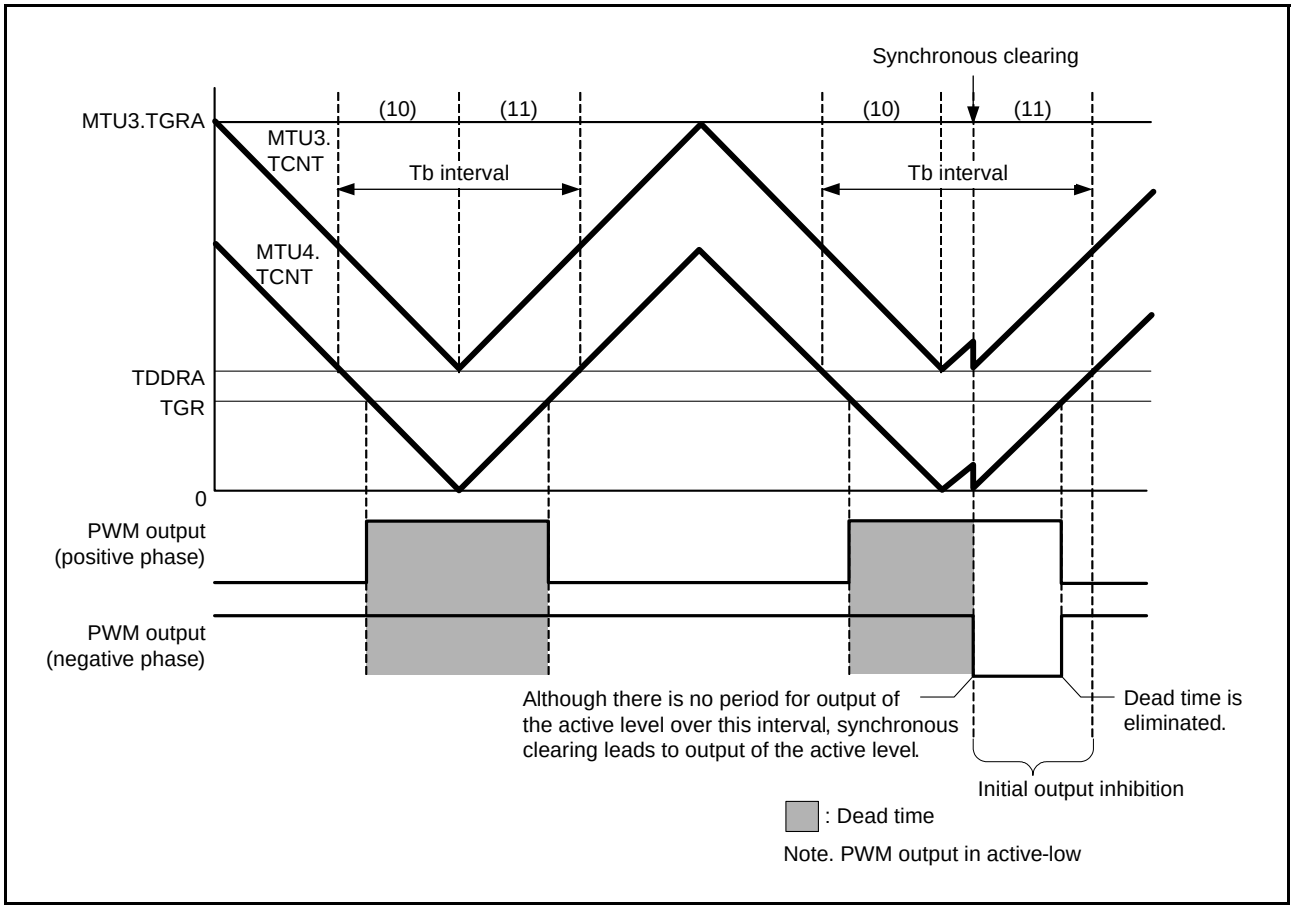


Figure 22.141 Example of Synchronous Clearing (Condition 2)

22.6.25 Continuous Output of Interrupt Signal in Response to a Compare Match

When TGR is set to 0000h, PCLKA/1 is set as the counter clock, and compare match is set as the trigger for clearing of the counter clock, the value of the TCNT counter remains 0000h, and the interrupt signal will be output continuously rather than output over a single cycle. Consequently, interrupts will not be detected in response to second and subsequent compare matches.

Figure 22.142 shows the timing for Continuous Output of Interrupt Signal in Response to a Compare Match.

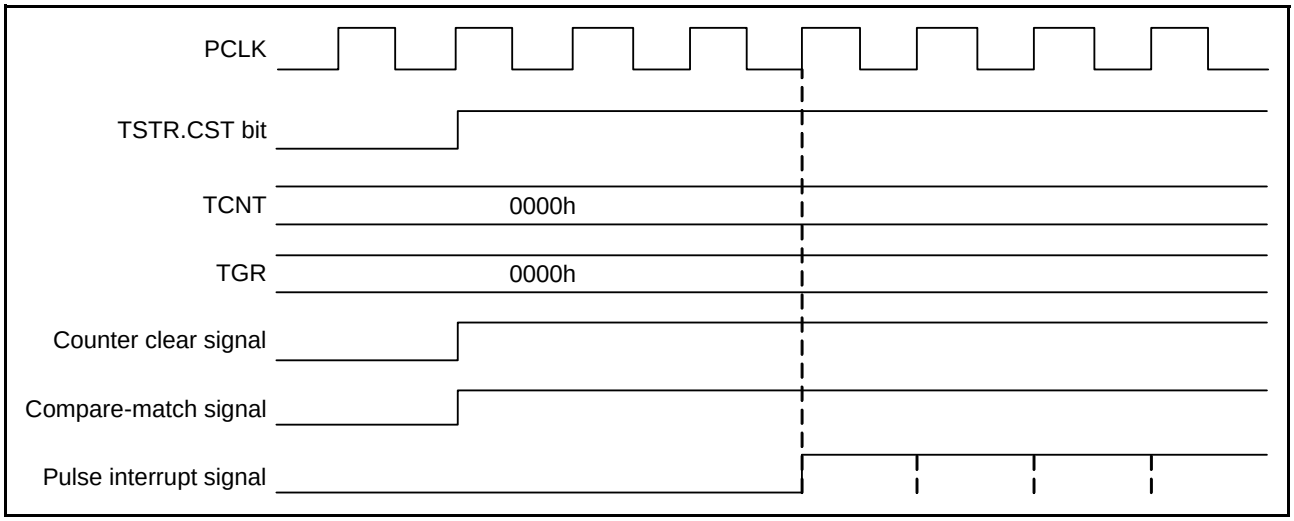


Figure 22.142 Continuous Output of Interrupt Signal in Response to a Compare Match

22.6.26 Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode

- When data is transferred from a buffer register at the trough of the MTU4.TCNT (MTU7.TCNT) counter while the MTU4.TADCOBRA and MTU4.TADCOBRB (MTU7.TADCOBRA and MTU7.TADCOBRB) registers are set to 0 and the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, no A/D converter start request is issued during up-counting immediately after transfer. See Figure 22.143.
- When data is transferred from a buffer register at the crest of the MTU4.TCNT (MTU7.TCNT) counter while the MTU4.TADCOBRA and MTU4.TADCOBRB (MTU7.TADCOBRA and MTU7.TADCOBRB) registers are set to the same value as the TCDR and the DT4AE and DT4BE (DT7AE and DT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, no A/D converter start request is issued during down-counting immediately after transfer. See Figure 22.144.
- To issue an A/D converter start request linked with the interrupt skipping function, set the MTU4.TADCORA and MTU4.TADCORB (MTU7.TADCORA and MTU7.TADCORB) registers so that 2 ≤ MTUn.TADCORA/ TADCORB ≤ TCDR - 2 is satisfied (n = 4, 7).

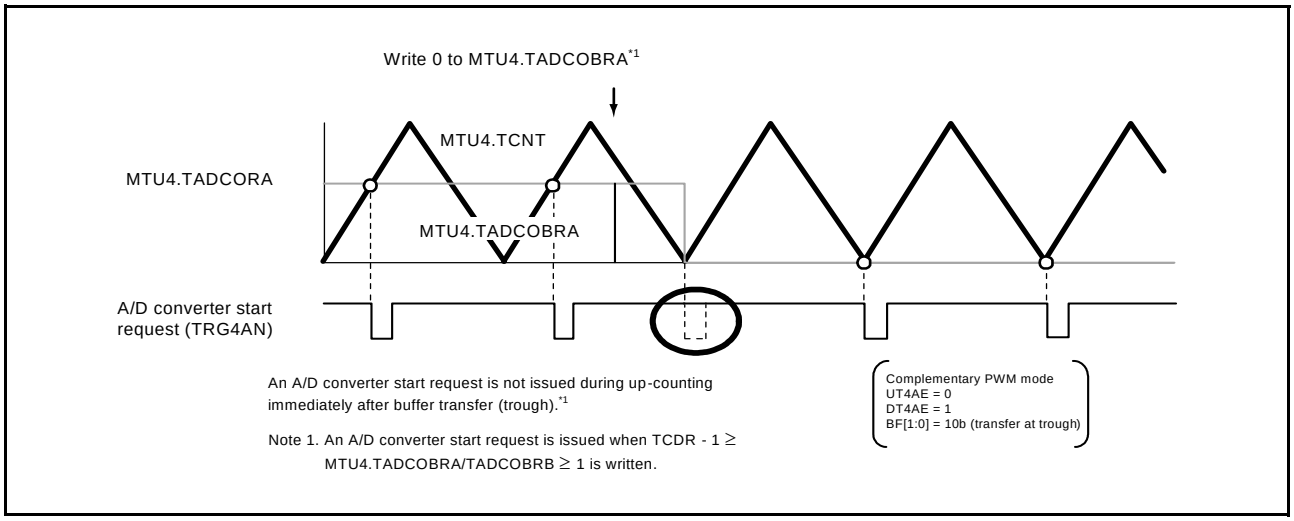


Figure 22.143 A/D Converter Start Request When 0 is Written to MTU4.TADCOBRA

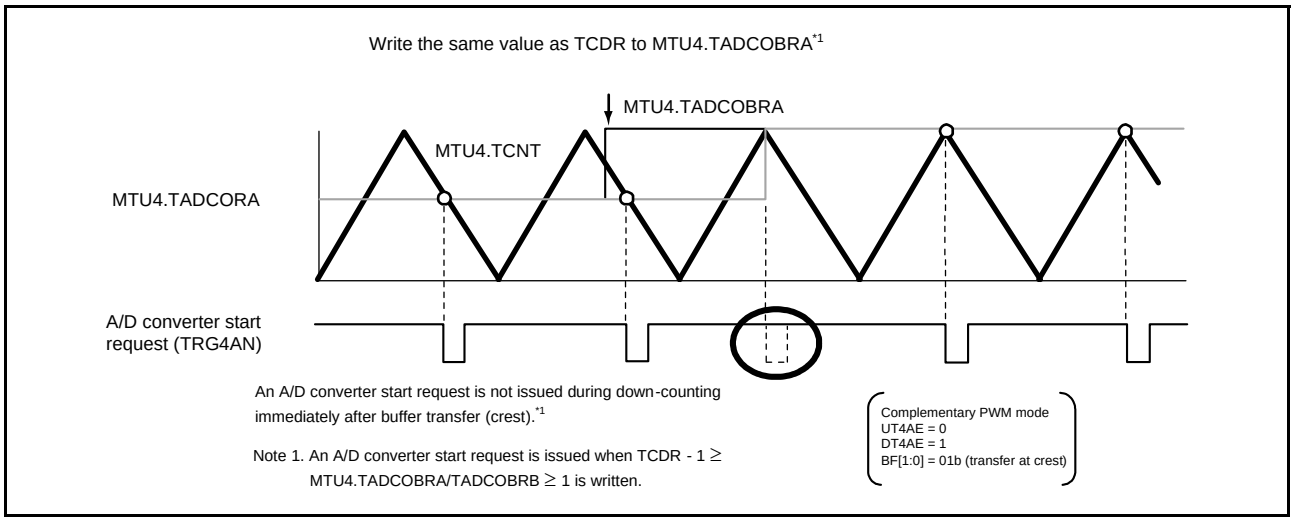


Figure 22.144 A/D Converter Start Request When the Same Value as TCDR is Written to MTU4.TADCOBRA

22.7 MTU Output Pin Initialization

22.7.1 Operating Modes

The MTU has the following six operating modes. Waveforms can be output in any of these modes.

- Normal mode (MTU0 to MTU4, MTU6, and MTU7)
- PWM mode 1 (MTU0 to MTU4, MTU6, and MTU)
- PWM mode 2 (MTU0 to MTU2)
- Phase counting modes 1 to 4 (MTU1 and MTU2)
- Complementary PWM mode (MTU3, MTU4, MTU6, and MTU7)
- Reset-synchronized PWM mode (MTU3, MTU4, MTU6, and MTU7)

This section describes how to initialize the MTU3 output pins in each of these modes.

22.7.2 Operation in Case of Re-Setting Due to Error during Operation

If an error occurs during MTU operation, MTU output should be cut off by the system. The output can be cut off by allowing non-active level output from the pins by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports. MTU output can be disabled through TIOR settings. Complementary PWM output (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D) should be specified through TOERA and TOERB settings. For PWM output pins, output can also be cut by hardware, using port output enable 3 (POE3). The pin initialization procedures for re-setting due to an error during operation and the procedures for restarting in a different mode after re-setting are described below.

The MTU has six operating modes, as stated above. There are thus 36 mode transition combinations, but some transitions are not available with certain channel and mode combinations. Available mode transition combinations are shown in Table 22.74.

Table 22.74 Mode Transition Combinations

	Normal	PWM1	PWM2	PCM	CPWM	RPWM
Normal	(1)	(2)	(3)	(4)	(5)	(6)
PWM1	(7)	(8)	(9)	(10)	(11)	(12)
PWM2	(13)	(14)	(15)	(16)	Not available	Not available
PCM	(17)	(18)	(19)	(20)	Not available	Not available
CPWM	(21)	(22)	Not available	Not available	(23) (24)	(25)
RPWM	(26)	(27)	Not available	Not available	(28)	(29)

Normal: Normal mode
PWM1: PWM mode 1
PWM2: PWM mode 2
PCM: Phase counting modes 1 to 4
CPWM: Complementary PWM mode
RPWM: Reset-synchronized PWM mode

22.7.3 Overview of Initialization Procedures and Mode Transitions in Case of Error during Operation

- When making a transition to a mode (Normal, PWM1, PWM2, or PCM) in which the pin output level is selected by the timer I/O control register (TIOR) setting, initialize the pins by means of TIOR setting.
- In PWM mode 1, waveforms are not output to the MTIOCnB and MTIOCnD (n = 3, 4, 6, or 7) pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- In PWM mode 2, waveforms are not output to the cycle register pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- In normal mode or PWM mode 2, if TGRC and TGRD operate as buffer registers, waveforms are not output to the corresponding pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- In PWM mode 1, if either TGRC or TGRD operates as a buffer register, waveforms are not output to the corresponding pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- When making a transition to a mode (CPWM or RPWM) in which the pin output level is selected by the timer output control register (TOCR1A, TOCR2A, TOCR1B, or TOCR2B) setting, temporarily disable output in MTU3 and MTU4 (or MTU6 and MTU7) with the timer output master enable register (TOERA or TOERB). At this time, if no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports. Switch to normal mode, perform initialization with TIOR, restore TIOR to its initial value, then operate the MTU3 in accordance with the mode setting procedure (TOCR1A setting, TOCR2A setting, TMDR1 setting, and TOERA setting (TOCR1B setting, TOCR2B setting, TMDR1 setting, and TOERB setting)).

Note: • Channel number is substituted for “n” indicated in this section.

Pin initialization procedures are described below for the numbered combinations in Table 22.74. The active level is assumed to be low.

(1) Operation when Error Occurs in Normal Mode and Operation is Restarted in Normal Mode

Figure 22.145 shows a case in which an error occurs in normal mode and operation is restarted in normal mode after re-setting.

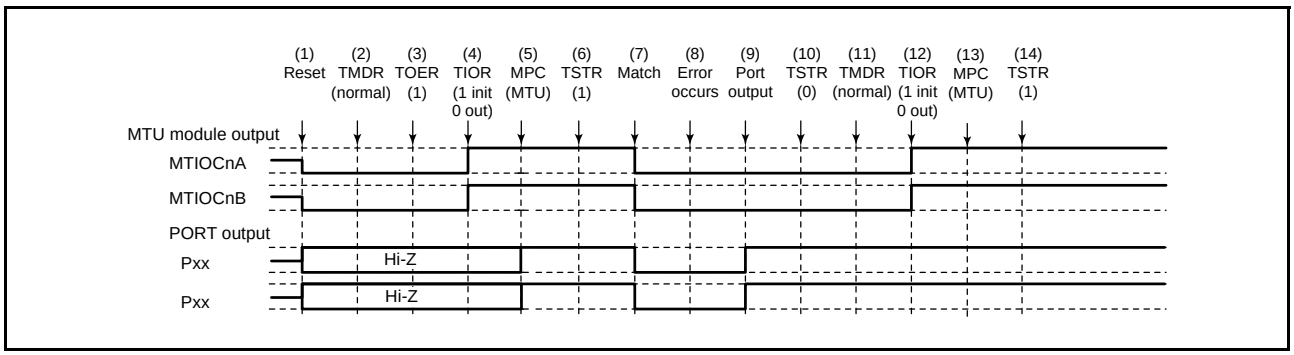


Figure 22.145 Error Occurrence in Normal Mode, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) After a reset, the TMDR1 setting is for normal mode.
(3) For MTU3 and MTU4, enable output with TOERA before initializing the pins with TIOR.
(4) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence.)
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) Output goes low on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting TSTRA.
(11) This step is not necessary when restarting in normal mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(2) Operation when Error Occurs in Normal Mode and Operation is Restarted in PWM Mode 1

Figure 22.146 shows a case in which an error occurs in normal mode and operation is restarted in PWM mode 1 after re-setting.

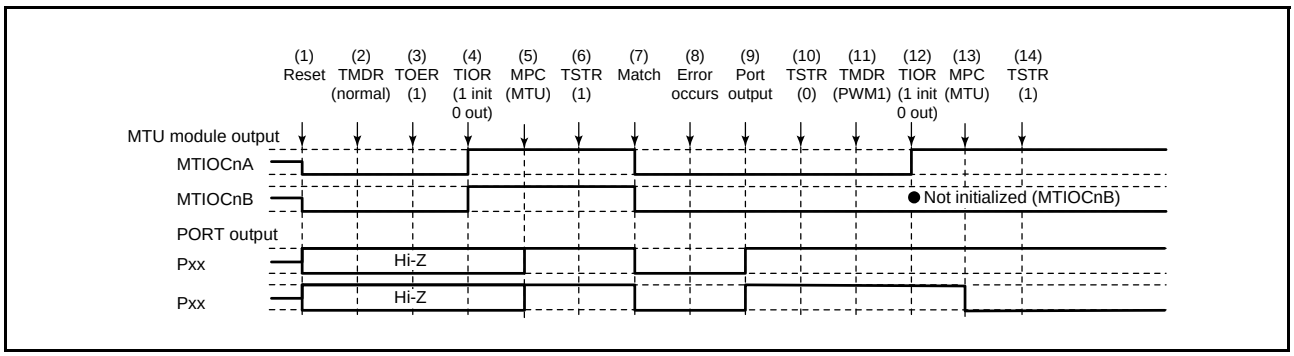


Figure 22.146 Error Occurrence in Normal Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 22.145.
(11) Set PWM mode 1.
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(3) Operation when Error Occurs in Normal Mode and Operation is Restarted in PWM mode 2

Figure 22.147 shows a case in which an error occurs in normal mode and operation is restarted in PWM mode 2 after re-setting.

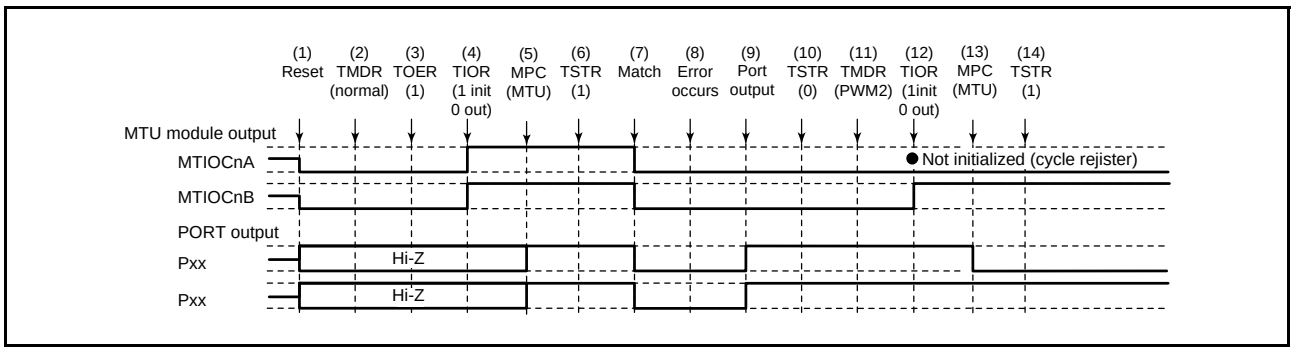


Figure 22.147 Error Occurrence in Normal Mode, Recovery in PWM Mode 2

(1) to (10) are the same as in Figure 22.145.
(11) Set PWM mode 2.
(12) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: • PWM mode 2 can only be selected for MTU0 to MTU2, and therefore TOERA setting is not necessary.

(4) Operation when Error Occurs in Normal Mode and Operation is Restarted in Phase Counting Mode

Figure 22.148 shows a case in which an error occurs in normal mode and operation is restarted in phase counting mode after re-setting.

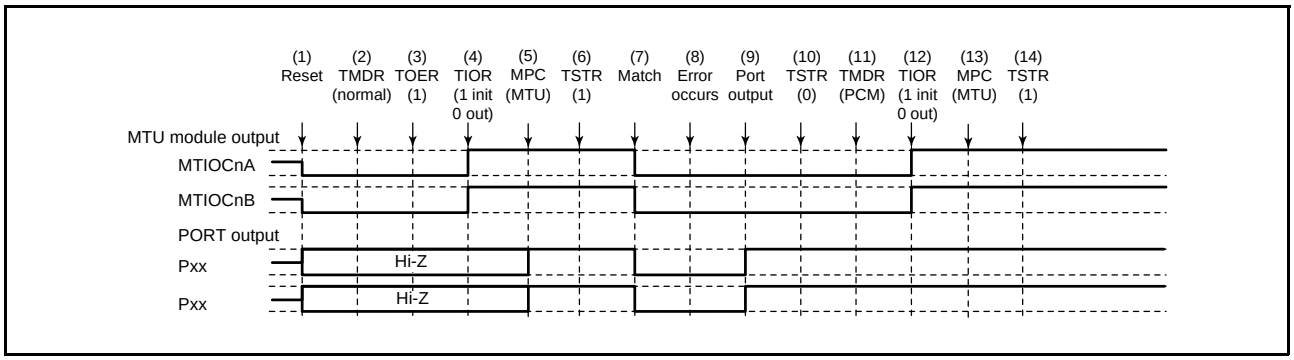


Figure 22.148 Error Occurrence in Normal Mode, Recovery in Phase Counting Mode

(1) to (10) are the same as in Figure 22.145.
(11) Set the phase counting mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: • The phase counting mode can only be selected for MTU1 and MTU2, and therefore TOERA setting is not necessary.

(5) Operation when Error Occurs in Normal Mode and Operation is Restarted in Complementary PWM Mode

Figure 22.149 shows a case in which an error occurs in normal mode and operation is restarted in complementary PWM mode after re-setting.

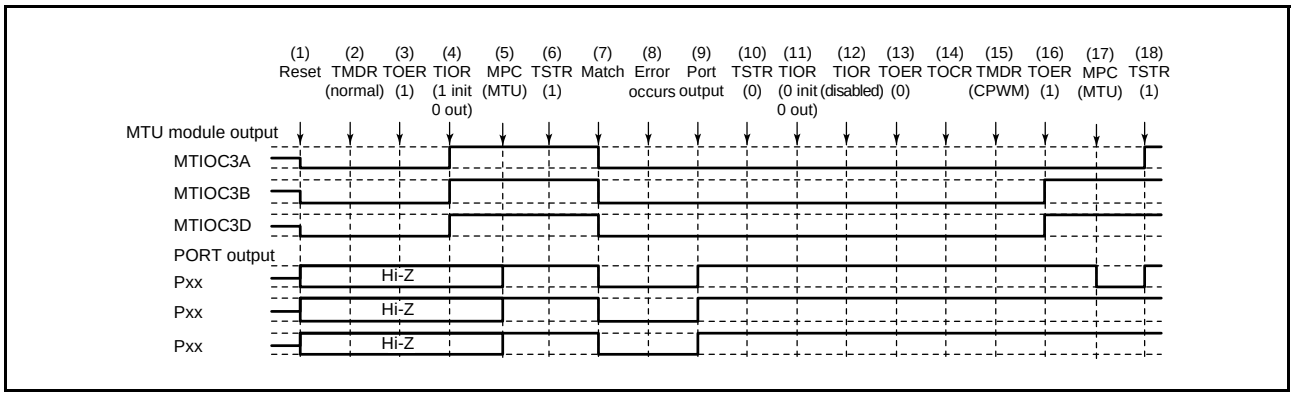


Figure 22.149 Error Occurrence in Normal Mode, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 22.145.
(11) Initialize the normal mode waveform generation section with TIOR.
(12) Disable operation of the normal mode waveform generation section with TIOR.
(13) Disable output in MTU3 and MTU4 with TOERA.
(14) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(15) Set complementary PWM mode.
(16) Enable output in MTU3 and MTU4 with TOERA.
(17) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(18) Restart operation by setting TSTRA.

(6) Operation when Error Occurs in Normal Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 22.150 shows a case in which an error occurs in normal mode and operation is restarted in reset-synchronized PWM mode after re-setting.

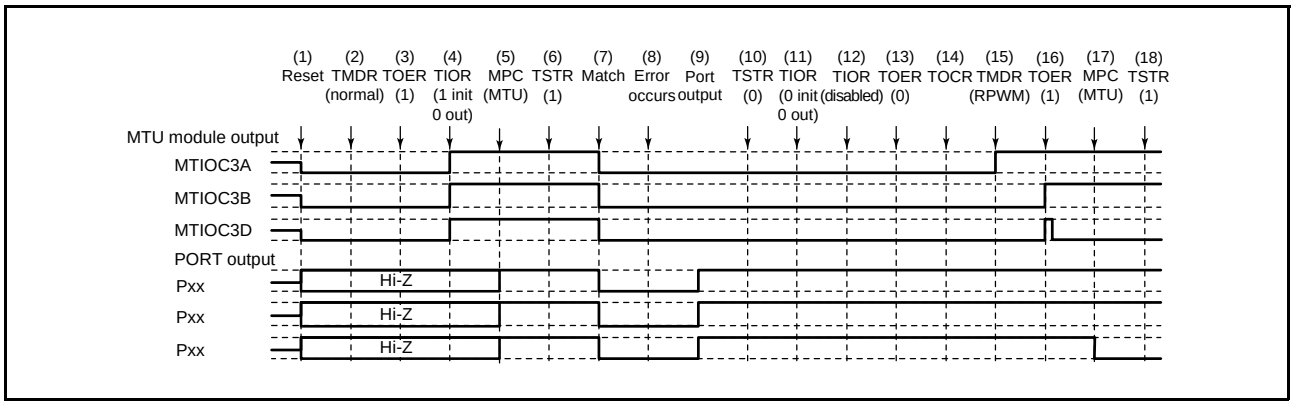


Figure 22.150 Error Occurrence in Normal Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (13) are the same as in Figure 22.145.
(14) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(15) Set reset-synchronized PWM mode.
(16) Enable output in MTU3 and MTU4 with TOERA.
(17) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(18) Restart operation by setting TSTRA.

(7) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Normal Mode

Figure 22.151 shows a case in which an error occurs in PWM mode 1 and operation is restarted in normal mode after re-setting.

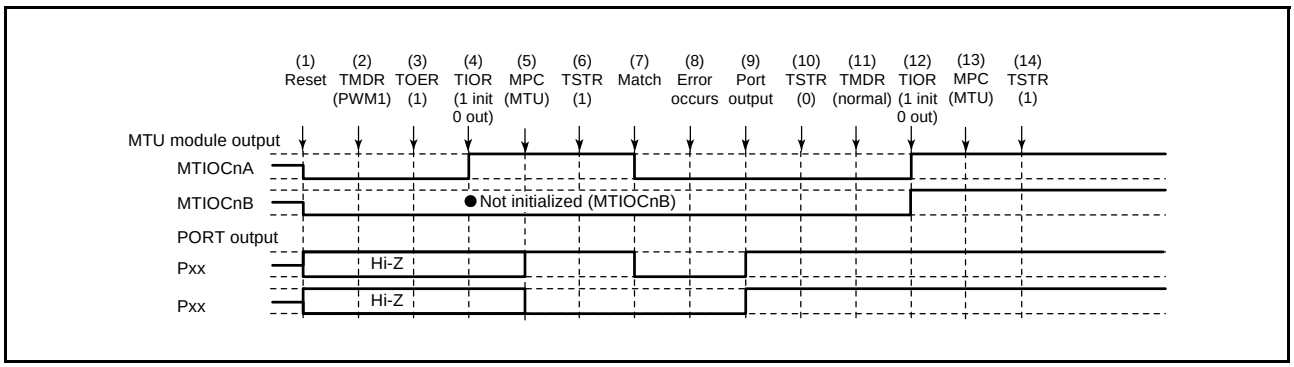


Figure 22.151 Error Occurrence in PWM Mode 1, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) Set PWM mode 1.
(3) For MTU3 and MTU4, enable output with TOERA before initializing the pins with TIOR.
(4) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence. In PWM mode 1, the MTIOCnB side is not initialized.)
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) Output goes low on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting TSTRA.
(11) Set normal mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(8) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in PWM mode 1

Figure 22.152 shows a case in which an error occurs in PWM mode 1 and operation is restarted in PWM mode 1 after re-setting.

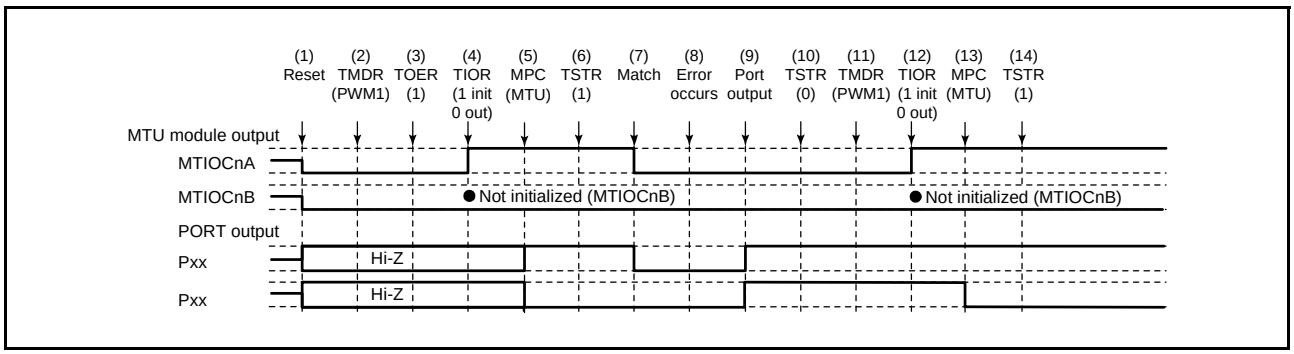


Figure 22.152 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 22.151.
(11) This step is not necessary when restarting in PWM mode 1.
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(9) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in PWM mode 2

Figure 22.153 shows a case in which an error occurs in PWM mode 1 and operation is restarted in PWM mode 2 after re-setting.

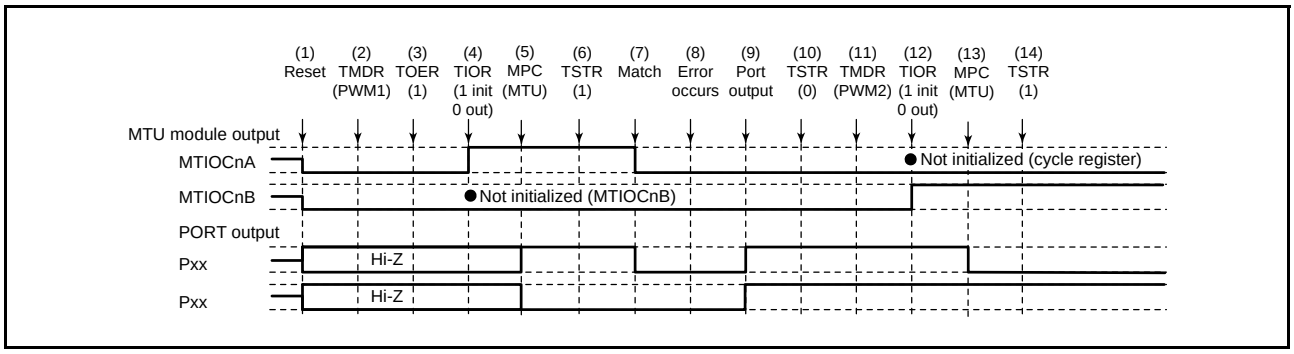


Figure 22.153 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 2

(1) to (10) are the same as in Figure 22.151.
(11) Set PWM mode 2.
(12) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: • PWM mode 2 can only be selected for MTU0 to MTU2, and therefore TOERA setting is not necessary.

(10) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Phase Counting Mode

Figure 22.154 shows a case in which an error occurs in PWM mode 1 and operation is restarted in phase counting mode after re-setting.

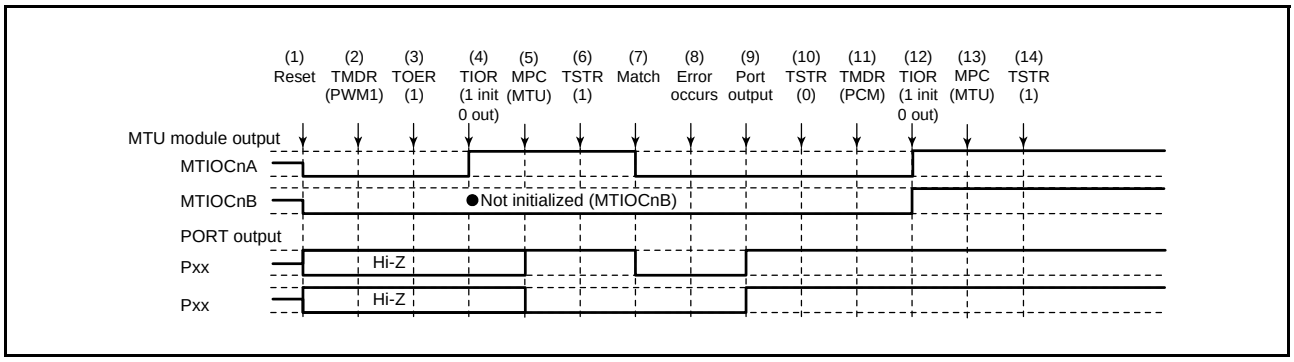


Figure 22.154 Error Occurrence in PWM Mode 1, Recovery in Phase Counting Mode

(1) to (10) are the same as in Figure 22.151.
(11) Set the phase counting mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: • The phase counting mode can only be selected for MTU1 and MTU2, and therefore TOERA setting is not necessary.

(11) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Complementary PWM Mode

Figure 22.155 shows a case in which an error occurs in PWM mode 1 and operation is restarted in complementary PWM mode after re-setting.

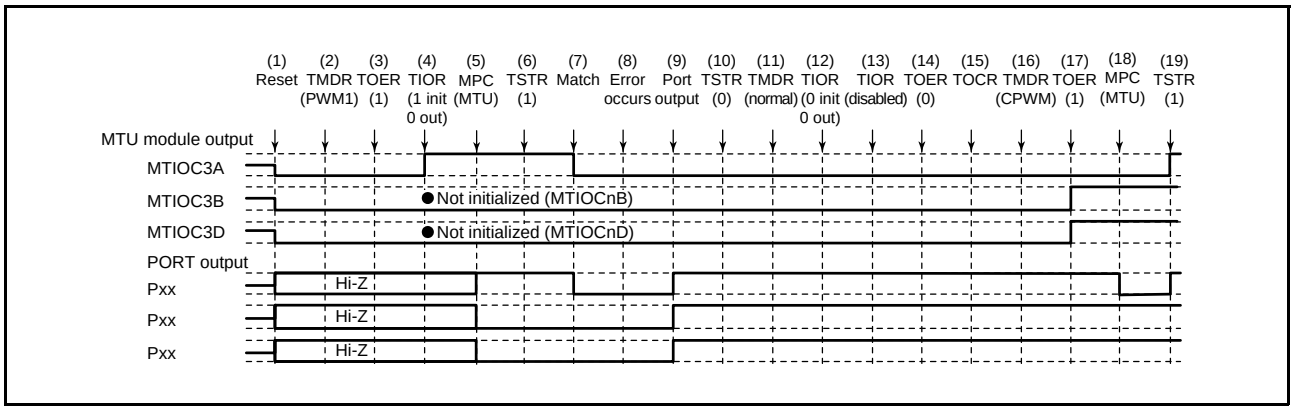


Figure 22.155 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 22.151.
(11) Set normal mode to initialize the normal mode waveform generation section.
(12) Initialize the PWM mode 1 waveform generation section with TIOR.
(13) Disable operation of the PWM mode 1 waveform generation section with TIOR
(14) Disable output in MTU3 and MTU4 with TOERA.
(15) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(16) Set complementary PWM mode.
(17) Enable output in MTU3 and MTU4 with TOERA.
(18) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(19) Restart operation by setting TSTRA.

(12) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 22.156 shows a case in which an error occurs in PWM mode 1 and operation is restarted in reset-synchronized PWM mode after re-setting.

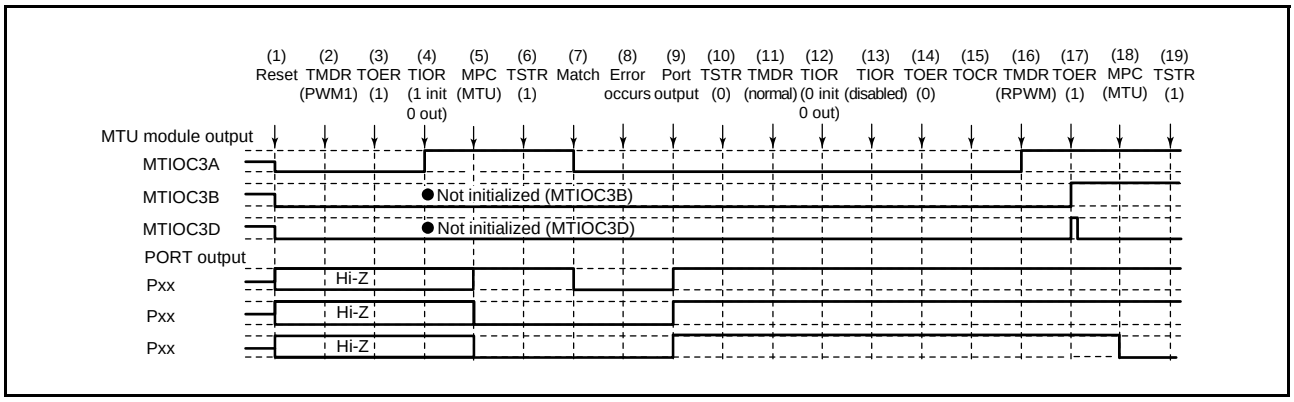


Figure 22.156 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronized PWM Mode

(1) to (14) are the same as in Figure 22.155.
(15) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(16) Set reset-synchronized PWM mode.
(17) Enable output in MTU3 and MTU4 with TOERA.
(18) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(19) Restart operation by setting TSTRA.

(13) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in Normal Mode

Figure 22.157 shows a case in which an error occurs in PWM mode 2 and operation is restarted in normal mode after re-setting.

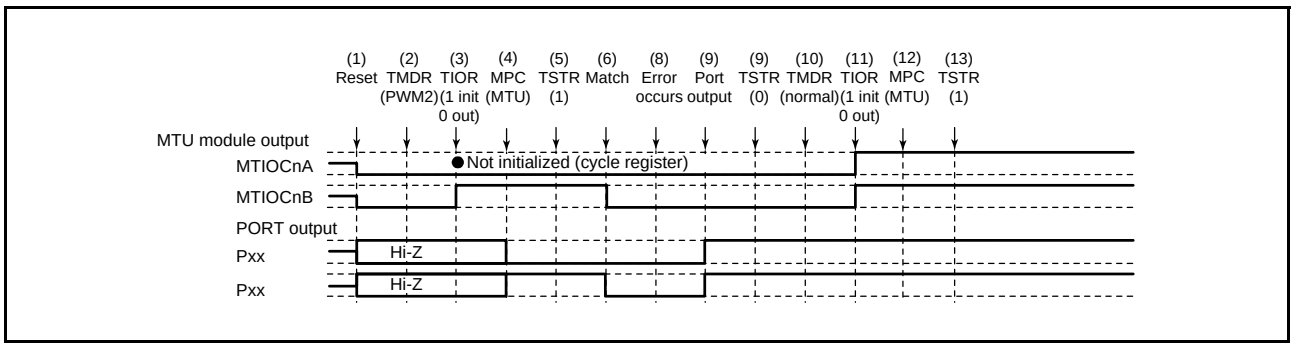


Figure 22.157 Error Occurrence in PWM Mode 2, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) Set PWM mode 2.
(3) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence. In PWM mode 2, the cycle register pins are not initialized. In the example, MTIOCnA is the cycle register.)
(4) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(5) Start count operation by setting TSTRA.
(6) Output goes low on compare match occurrence.
(7) An error occurs.
(8) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(9) Stop count operation by setting TSTRA.
(10) Set normal mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(14) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in PWM Mode 1

Figure 22.158 shows a case in which an error occurs in PWM mode 2 and operation is restarted in PWM mode 1 after re-setting.

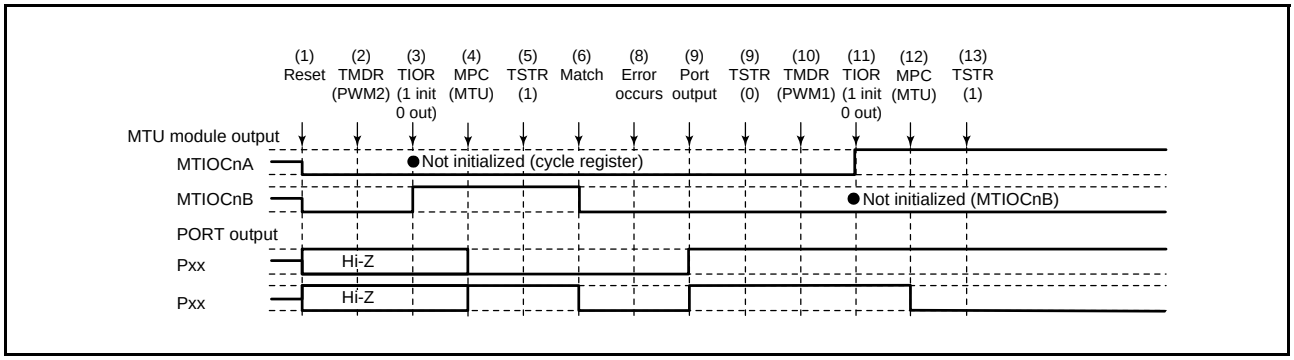


Figure 22.158 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 1

(1) to (9) are the same as in Figure 22.157.
(10) Set PWM mode 1.
(11) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(15) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in PWM Mode 2

Figure 22.159 shows a case in which an error occurs in PWM mode 2 and operation is restarted in PWM mode 2 after re-setting.

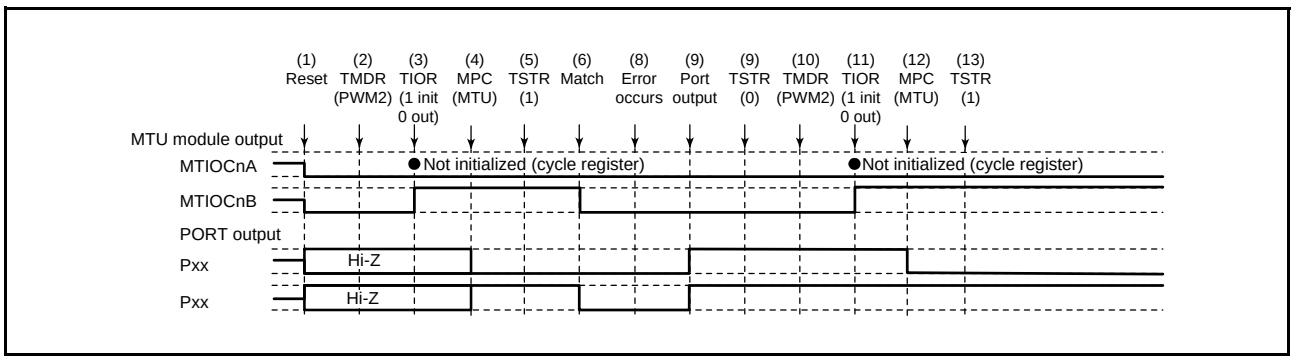


Figure 22.159 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 2

(1) to (9) are the same as in Figure 22.157.
(10) This step is not necessary when restarting in PWM mode 2.
(11) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(16) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in Phase Counting Mode

Figure 22.160 shows a case in which an error occurs in PWM mode 2 and operation is restarted in phase counting mode after re-setting.

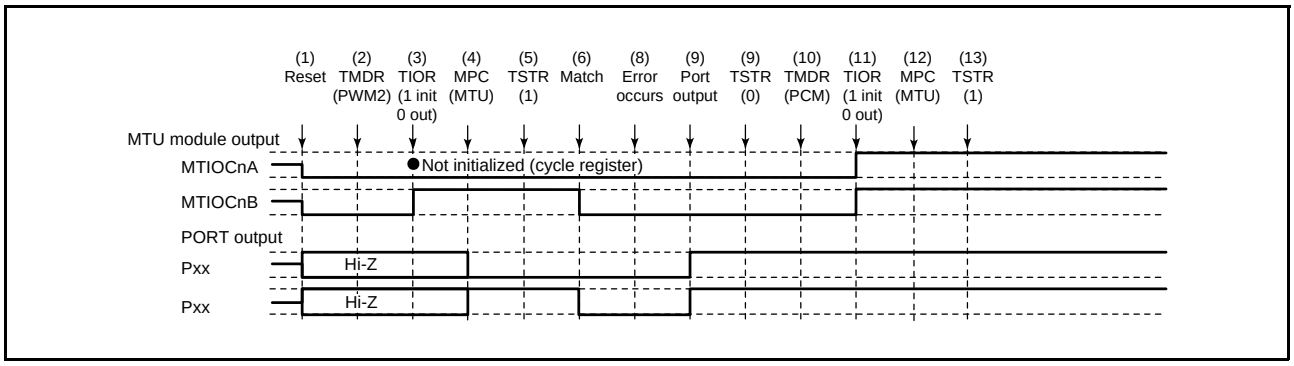


Figure 22.160 Error Occurrence in PWM Mode 2, Recovery in Phase Counting Mode

(1) to (9) are the same as in Figure 22.157.
(10) Set the phase counting mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(17) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in Normal Mode

Figure 22.161 shows a case in which an error occurs in phase counting mode and operation is restarted in normal mode after re-setting.

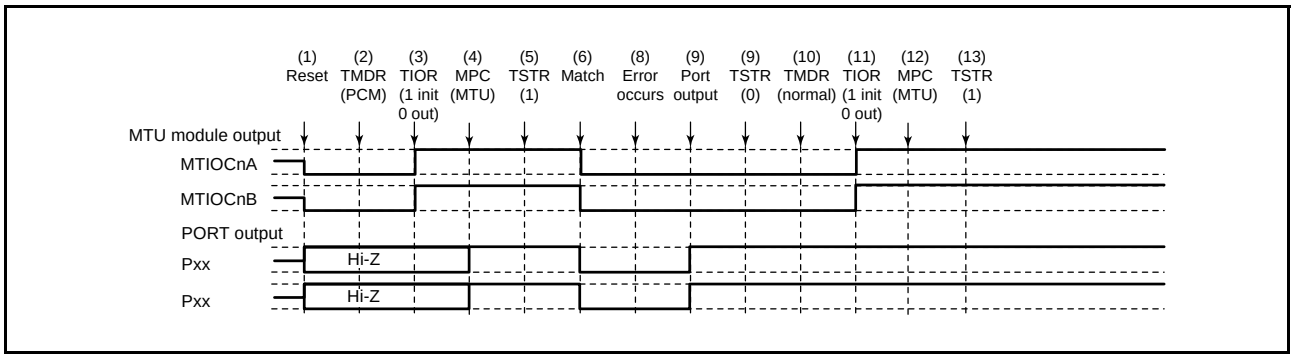


Figure 22.161 Error Occurrence in Phase Counting Mode, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) Set phase counting mode.
(3) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence.)
(4) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(5) Start count operation by setting TSTRA.
(6) Output goes low on compare match occurrence.
(7) An error occurs.
(8) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(9) Stop count operation by setting TSTRA.
(10) Set normal mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(18) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in PWM Mode 1

Figure 22.162 shows a case in which an error occurs in phase counting mode and operation is restarted in PWM mode 1 after re-setting.

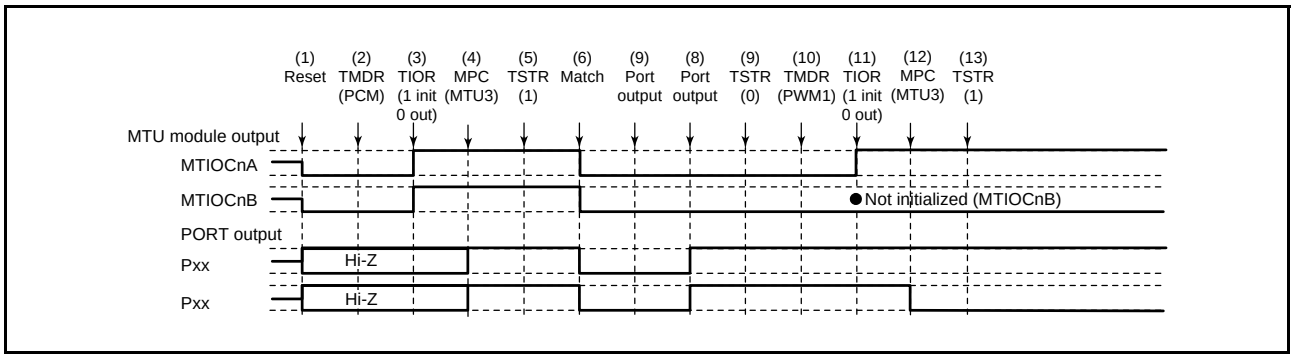


Figure 22.162 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 1

(1) to (9) are the same as in Figure 22.161.
(10) Set PWM mode 1.
(11) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(19) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in PWM Mode 2

Figure 22.163 shows a case in which an error occurs in phase counting mode and operation is restarted in PWM mode 2 after re-setting.

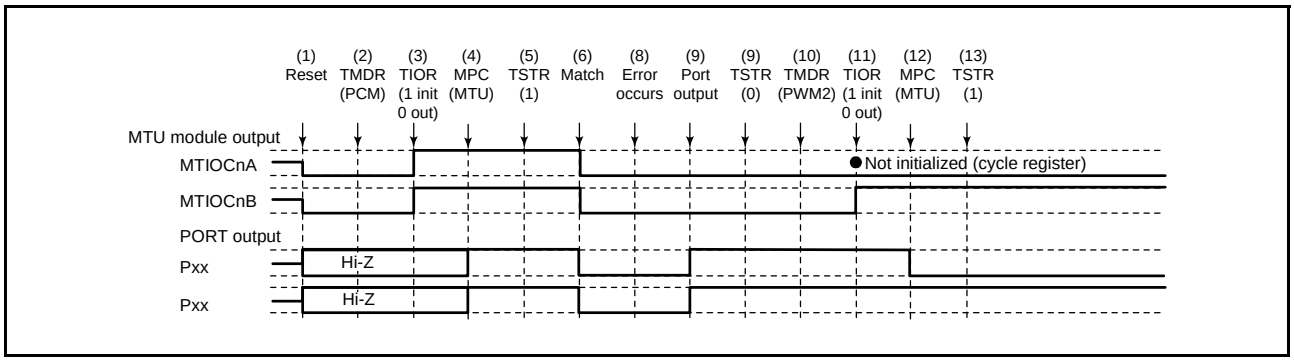


Figure 22.163 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 2

(1) to (9) are the same as in Figure 22.161.
(10) Set PWM mode 2.
(11) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(20) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in Phase Counting Mode

Figure 22.164 shows a case in which an error occurs in phase counting mode and operation is restarted in phase counting mode after re-setting.

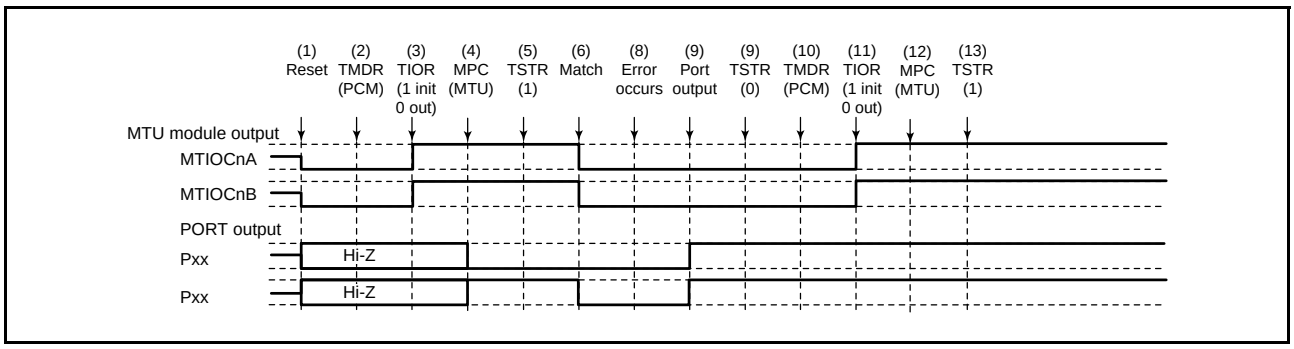


Figure 22.164 Error Occurrence in Phase Counting Mode, Recovery in Phase Counting Mode

(1) to (9) are the same as in Figure 22.161.
(10) This step is not necessary when restarting in phase counting mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(21) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Normal Mode

Figure 22.165 shows a case in which an error occurs in complementary PWM mode and operation is restarted in normal mode after re-setting.

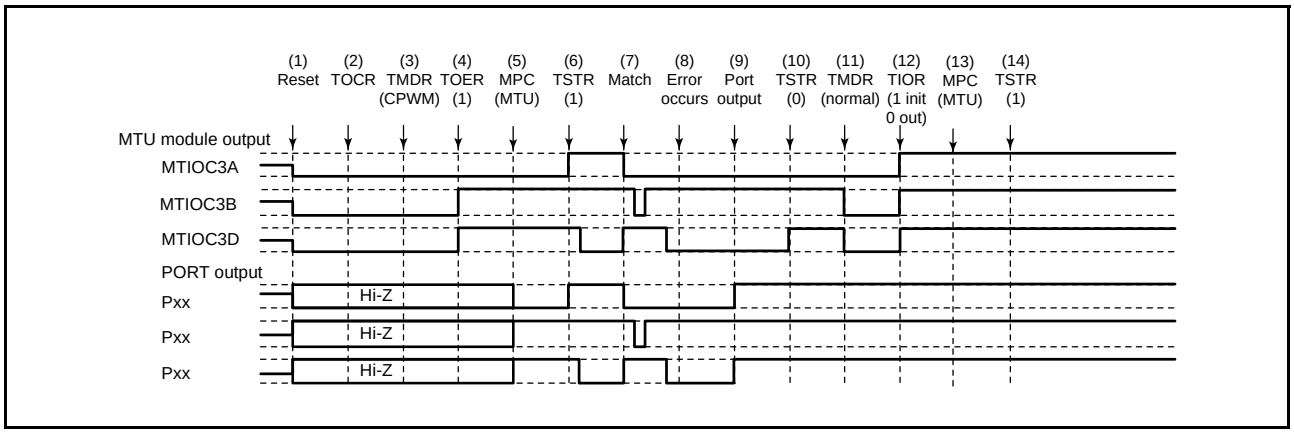


Figure 22.165 Error Occurrence in Complementary PWM Mode, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(3) Set complementary PWM mode.
(4) Enable output in MTU3 and MTU4 with TOERA.
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) The complementary PWM waveform is output on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting TSTRA. (MTU3 output becomes the initial complementary PWM output value).
(11) Set normal mode (MTU3 output goes low).
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(22) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in PWM Mode 1

Figure 22.166 shows a case in which an error occurs in complementary PWM mode and operation is restarted in PWM mode 1 after re-setting.

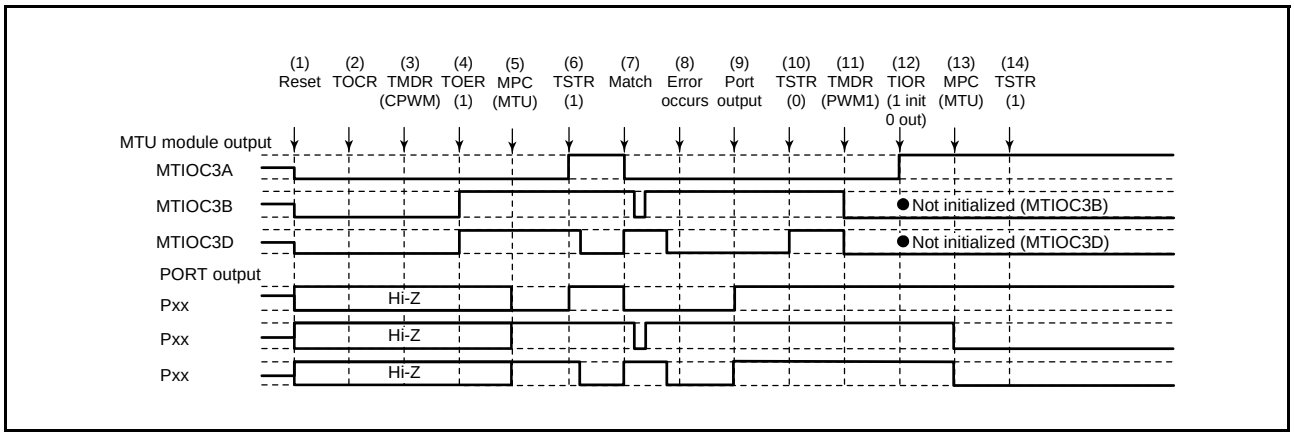


Figure 22.166 Error Occurrence in Complementary PWM Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 22.165.
(11) Set PWM mode 1 (MTU3 output goes low).
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(23) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Complementary PWM Mode

Figure 22.167 shows a case in which an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (when operation is restarted using the cycle and duty settings at the time of stopping the counter).

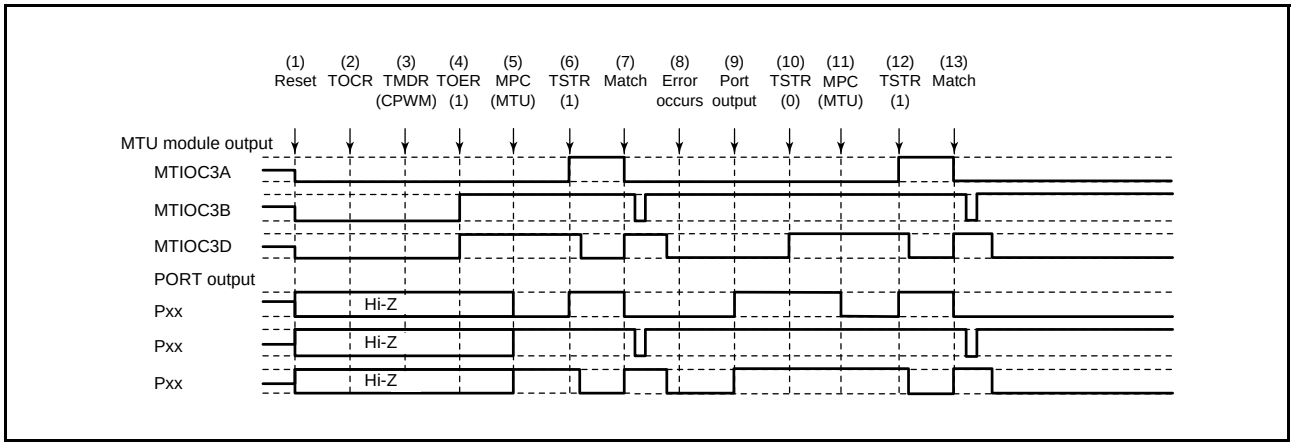


Figure 22.167 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode (1)

(1) to (10) are the same as in Figure 22.165.
(11) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(12) Restart operation by setting TSTRA.
(13) The complementary PWM waveform is output on compare match occurrence.

(24) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Complementary PWM Mode with New Settings

Figure 22.168 shows a case in which an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (operation is restarted using new cycle and duty ratio settings).

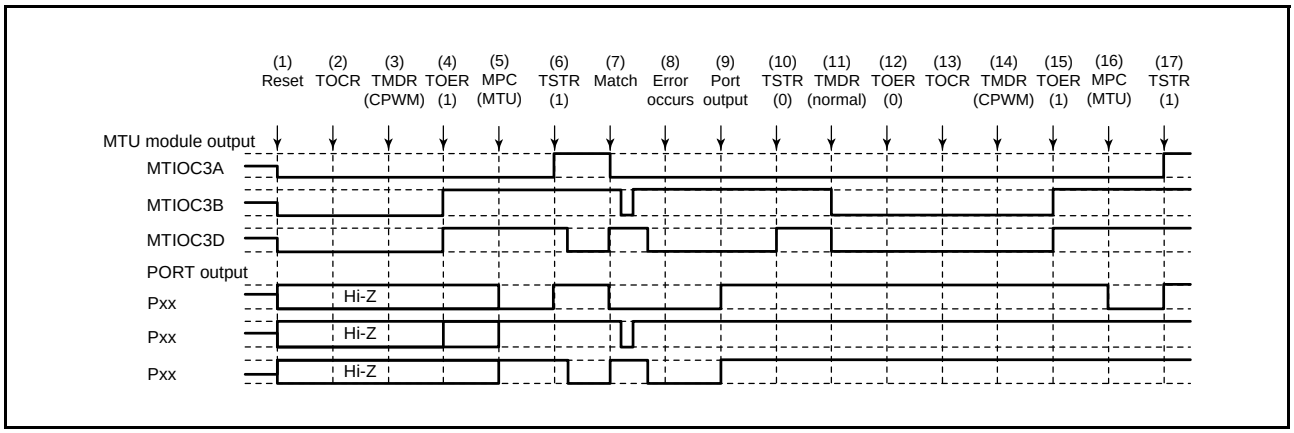


Figure 22.168 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode (2)

(1) to (10) are the same as in Figure 22.165.
(11) Set normal mode and make new settings (MTU3 output goes low).
(12) Disable output in MTU3 and MTU4 with TOERA.
(13) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(14) Set complementary PWM mode.
(15) Enable output in MTU3 and MTU4 with TOERA.
(16) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(17) Restart operation by setting TSTRA.

(25) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 22.169 shows a case in which an error occurs in complementary PWM mode and operation is restarted in reset-synchronized PWM mode after re-setting.

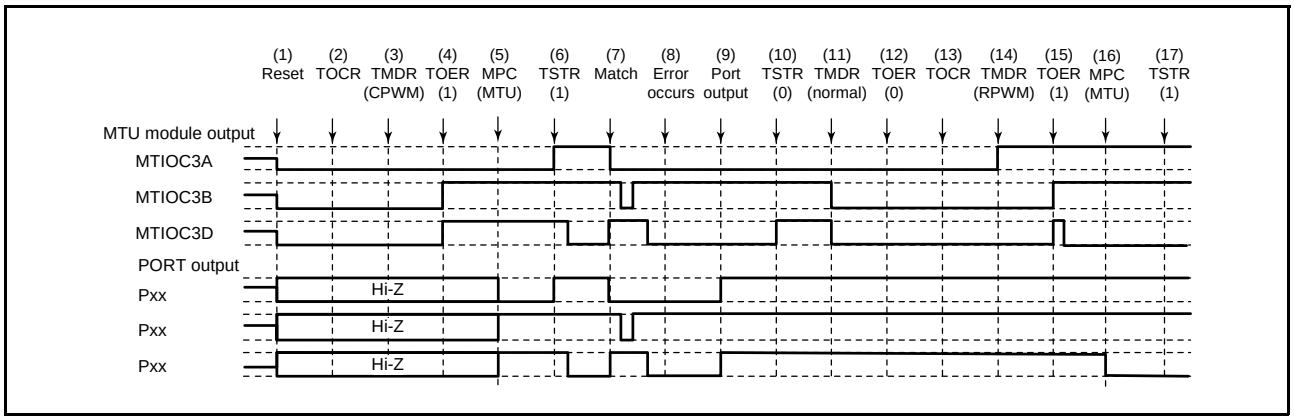


Figure 22.169 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (9) are the same as in Figure 22.165.
(11) Set normal mode (MTU3 output goes low).
(12) Disable output in MTU3 and MTU4 with TOERA.
(13) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(14) Set reset-synchronized PWM mode.
(15) Enable output in MTU3 and MTU4 with TOERA.
(16) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(17) Restart operation by setting TSTRA.

(26) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Normal Mode

Figure 22.170 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in normal mode after re-setting.

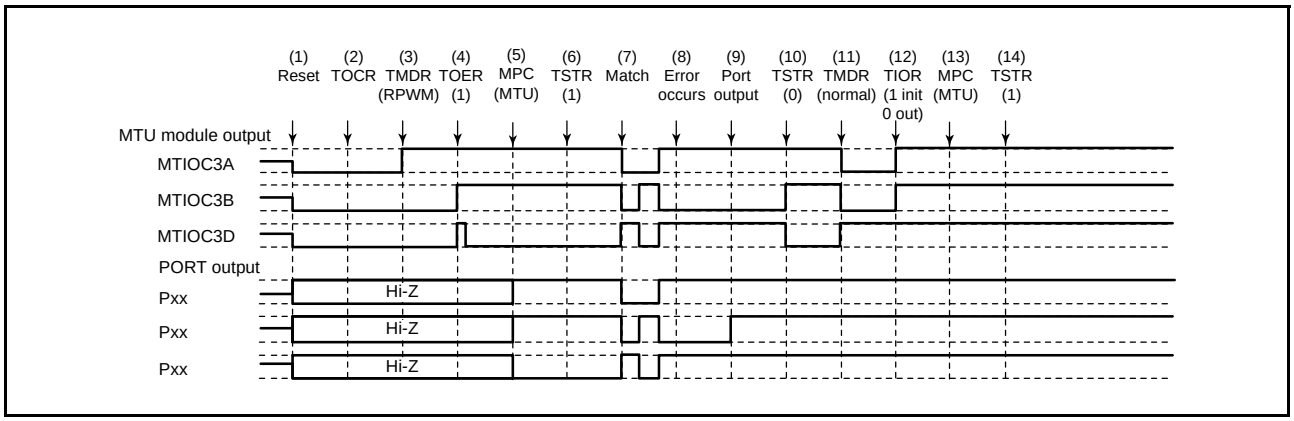


Figure 22.170 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(3) Set reset-synchronized PWM mode.
(4) Enable output in MTU3 and MTU4 with TOERA.
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) The reset-synchronized PWM waveform is output on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.(10) Stop count operation by setting TSTRA. (MTU3 output becomes the initial reset-synchronized PWM output value.)
(11) Set normal mode (positive-phase MTU3 output goes low, and negative-phase output goes high).
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(27) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in PWM Mode 1

Figure 22.171 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in PWM mode 1 after re-setting.

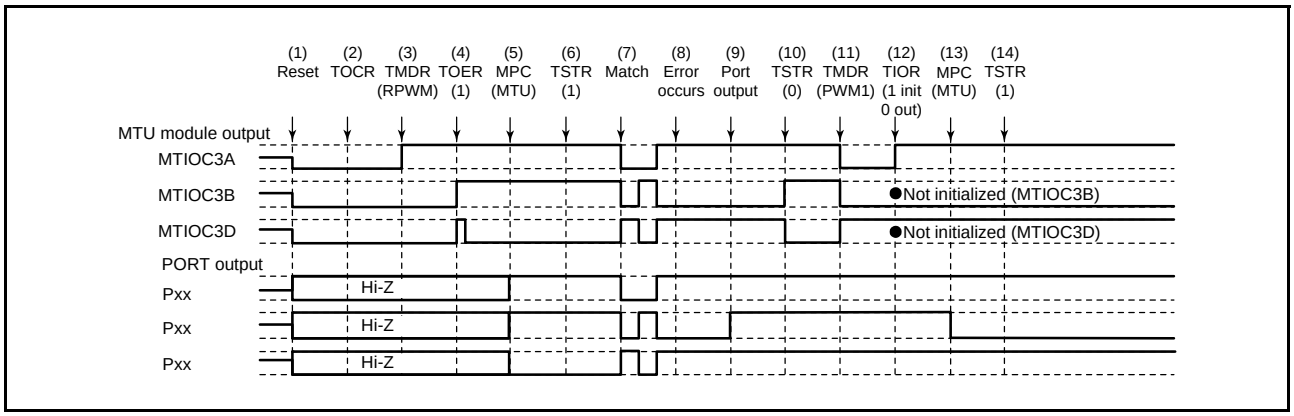


Figure 22.171 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 22.170.
(11) Set PWM mode 1 (positive-phase MTU3 output goes low, and negative-phase output goes high).
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(28) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Complementary PWM Mode

Figure 22.172 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in complementary PWM mode after re-setting.

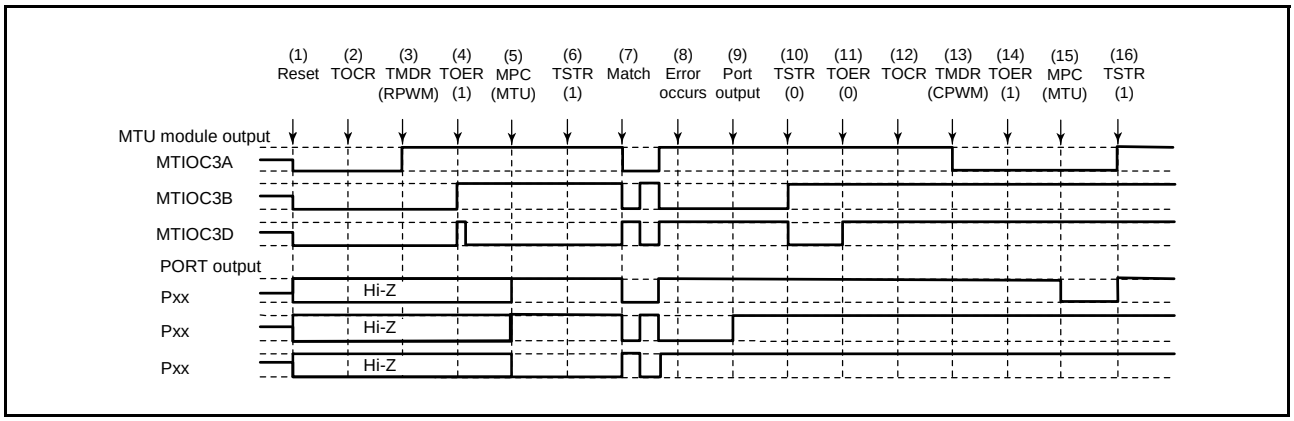


Figure 22.172 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 22.170.
(11) Disable output in MTU3 and MTU4 with TOERA.
(12) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(13) Set complementary PWM mode (MTU3 cyclic output pin goes low).
(14) Enable output in MTU3 and MTU4 with TOERA.
(15) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(16) Restart operation by setting TSTRA.

(29) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 22.173 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in reset-synchronized PWM mode after re-setting.

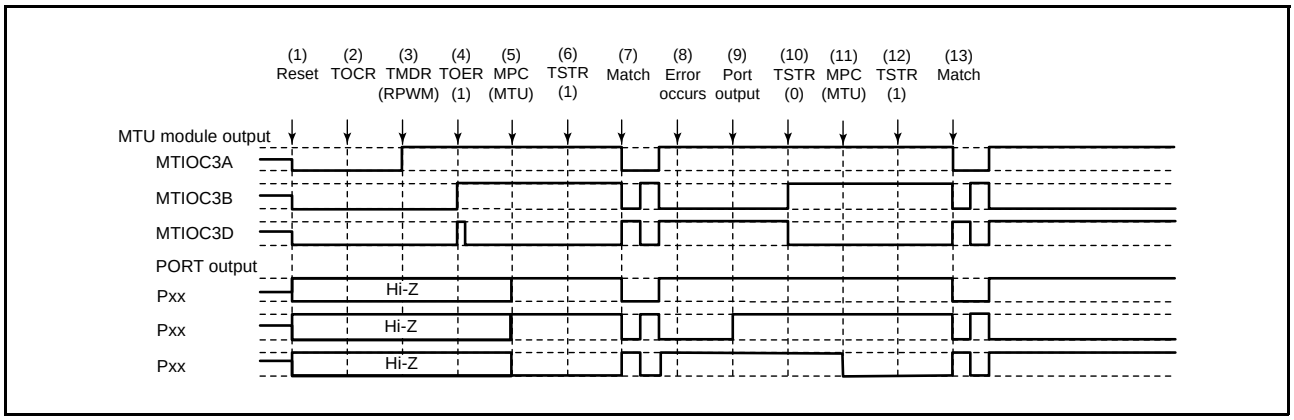


Figure 22.173 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (10) are the same as in Figure 22.170.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(11) Restart operation by setting TSTRA.
(13) The reset-synchronized PWM waveform is output on compare match occurrence.

23. Port Output Enable 3 (POE3)

The port output enable 3 (POE3) register can be used to place complementary PWM output pins for the MTU (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D) and output pins for the GPT (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC4A, GTIOC4B, GTIOC5A, GTIOC5B, GTIOC6A, and GTIOC6B) in the high-impedance state in accord with changes in the input signals on the POE0#, POE4#, POE8#, POE10#, POE11# and POE12# pins, and to place pin functions multiplexed with complementary PWM output pins for the MTU, pins for MTU0 (MTIOC0A, MTIOC0B, MTIOC0C, and MTIOC0D), and pins for the GPT (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B, GTIOC4A, GTIOC4B, GTIOC5A, GTIOC5B, GTIOC6A, GTIOC6B, GTIOC7A, and GTIOC7B) in the high-impedance state in accord with register settings. It can also simultaneously generate interrupt requests. Furthermore, it is capable of placing pin functions multiplexed with complementary PWM output pins for the MTU, pins for MTU0, and pins for the GPT in the high-impedance state in response to stoppage of the clock signal from the clock oscillator and comparator detection by the 12-bit A/D converter (S12ADB).

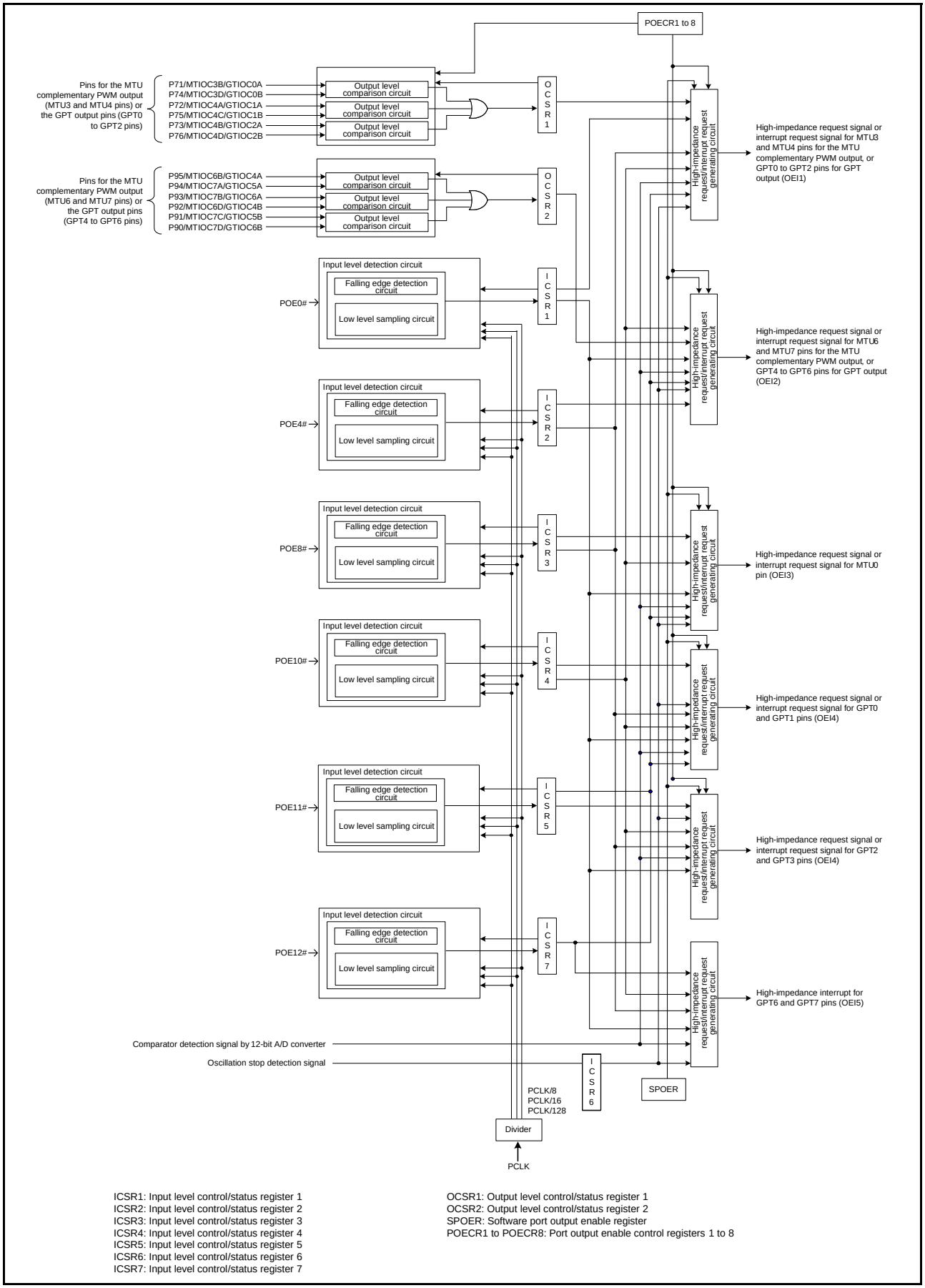
23.1 Overview

Table 23.1 lists the specifications of the POE3, and Figure 23.1 shows a block diagram of the POE3.

Table 23.1 POE3 Specifications

Item	Description
Function	• Each of the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low sampling. • Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in high-impedance state by POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pin falling-edge or low sampling. • Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in high-impedance state when the oscillation-stop detection circuit in the clock pulse generator detects stopped oscillation. • Pins for the MTU complementary PWM output can be placed in high-impedance state when output levels of the MTU complementary PWM output pins and the GPT output pins are compared and simultaneous active-level output continues for one cycle or more. • Pins for the MTU complementary PWM output, and MTU0, and GPT pins can be placed in the high-impedance state in response to comparator detection by the 12-bit A/D converter (S12ADB). • Pins for the MTU complementary PWM output, and MTU0, and GPT pins can be placed in the high-impedance state by modifying settings of the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.

The POE3 has input level detection circuits, output level comparison circuits, and a high-impedance request/interrupt request generating circuit as shown in Figure 23.1.



ICSR1: Input level control/status register 1
ICSR2: Input level control/status register 2
ICSR3: Input level control/status register 3
ICSR4: Input level control/status register 4
ICSR5: Input level control/status register 5
ICSR6: Input level control/status register 6
ICSR7: Input level control/status register 7

OCSR1: Output level control/status register 1
OCSR2: Output level control/status register 2
SPOER: Software port output enable register
POECR1 to POECR8: Port output enable control registers 1 to 8

Figure 23.1 POE3 Block Diagram

Table 23.2 shows input/output pins to be used by the POE3.

Table 23.2 POE3 Input/Output Pins

Pin Name	I/O	Description
POE0#	Input	[144-, 120-, 112- and 100-pin versions] Request signal to place the MTU3 and MTU4 pins for MTU complementary PWM output in high-impedance state, and in accord with register settings, is also capable of placing the MTU0, MTU6, MTU7, and GPT pins in the high-impedance state. [64- and 48-pin versions] Request signal to place the MTU3 and MTU4 or MTU6 and MTU7pins for MTU complementary PWM output in high-impedance state, and in accord with register settings, is also capable of placing the MTU0 and GPT pins in the high-impedance state.
POE4#	Input	Request signal to place the MTU6 and MTU7pins for MTU complementary PWM output in high-impedance state, and in accord with register settings, is also capable of placing the MTU0, MTU3, MTU4, and GPT pins in the high-impedance state.
POE8#	Input	[144-, 120-, 112- and 100-pin versions] Request signal to place the pins for MTU0 in high-impedance state, and in accord with register settings, is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, and GPT pins in high-impedance state. [64- and 48-pin versions] Request signal to place the pins for MTU0 in high-impedance state, and in accord with register settings, is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, and GPT pins in high-impedance state.
POE10#	Input	[144-, 120-, 112- and 100-pin versions] Request signal to place the GPT0 and GPT1 pins in high-impedance state, and in accord with register settings, is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, MTU0, GPT2, GPT3, GPT6, and GPT7 pins in high-impedance state. [64- and 48-pin versions] Request signal to place the GPT0 and GPT1 pins in high-impedance state, and in accord with register settings, is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, MTU0, GPT2, and GPT3 pins in high-impedance state
POE11#	Input	[144-, 120-, 112- and 100-pin versions] Request signal to place the pins for GPT2 and GPT3 in high-impedance state, and in accord with register settings, is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, MTU0, GPT0, GPT1, GPT6, and GPT7 pins in high-impedance state. [64- and 48-pin versions] Request signal to place the pins for GPT2 and GPT3 in high-impedance state, and in accord with register settings, is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, MTU0, GPT0, and GPT1 pins in high-impedance state.
POE12#	Input	Request signal to place the pins for GPT6 and GPT7 in high-impedance state, and in accord with register settings, is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, MTU0, GPT0, GPT1, GPT2, and GPT3 pins in high-impedance state.

Table 23.3 shows output-level comparisons with pin combinations.

Table 23.3 Pin Combinations

Pin Combination	I/O	Description
MTIOC3B and MTIOC3D	Output	The MTU3 and MTU4 pins for MTU complementary PWM output are placed in high-impedance state when both pins of a pair simultaneously output the active level (low level when the OLSP bit in TOCR1A of MTUn is 0 with the TOCS bit in TOCR1A of MTUn cleared to 0 or high level when the OLSP bit is 1, or low level when the OLS3N, OLS3P, OLS2N, OLS2P, OLS1N, and OLS1P bits in TOCR2A of MTUn are 0 with the TOCS bit in TOCR1A of MTUn set to 1 and high level when these bits are 1) for one or more cycles of the peripheral clock (PCLK). Pin combinations for output comparison and high-impedance control can be selected by registers of POE3.
MTIOC4A and MTIOC4C	Output	
MTIOC4B and MTIOC4D	Output	
MTIOC6B and MTIOC6D	Output	The MTU6 and MTU7 pins for MTU complementary PWM output are placed in high-impedance state when both pins of a pair simultaneously output the active level (low level when the OLSP bit in TOCR1B of MTUn is 0 with the TOCS bit in TOCR1B of MTUn cleared to 0 or high level when the OLSP bit is 1, or low level when the OLS3N, OLS3P, OLS2N, OLS2P, OLS1N, and OLS1P bits in TOCR2B of MTUn are 0 with the TOCS bit in TOCR1B of MTUn set to 1 and high level when these bits are 1) for one or more cycles of the peripheral clock (PCLK). Pin combinations for output comparison and high-impedance control can be selected by registers of POE3.
MTIOC7A and MTIOC7C	Output	
MTIOC7B and MTIOC7D	Output	
GTIOC0A and GTIOC0B	Output	The GPT0 to GPT2 pins for the GPT output are placed in high-impedance state when both pins of a pair simultaneously output the active level (low level when the OLSG2B, OLSG2A, OLSG1B, OLSG1A, OLSG0B, and OLSG0A bits in ALR1 are 0 or high level when those bits are 1) for one or more cycles of the peripheral clock (PCLK). Pin combinations for output comparison and high-impedance control can be selected by registers of POE3.
GTIOC1A and GTIOC1B	Output	
GTIOC2A and GTIOC2B	Output	
GTIOC4A and GTIOC4B	Output	The GPT4 to GPT6 pins for the GPT output are placed in high-impedance state when both pins of a pair simultaneously output the active level (low level when the OLSG2B, OLSG2A, OLSG1B, OLSG1A, OLSG0B, and OLSG0A bits in ALR2 are 0 or high level when those bits are 1) for one or more cycles of the peripheral clock (PCLK). Pin combinations for output comparison and high-impedance control can be selected by registers of POE3.
GTIOC5A and GTIOC5B	Output	
GTIOC6A and GTIOC6B	Output	

23.2 Register Descriptions

The POE3 registers are initialized by a reset.

23.2.1 Input Level Control/Status Register 1 (ICSR1)

Address(es): 0008 C4C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE0F	—	—	—	PIE1	—	—	—	—	—	—	POE0M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE0M[1:0]	POE0 Mode Select	b1 b0 0 0: Accepts a high-impedance control request on the falling edge of the POE0# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE1	Port Interrupt Enable 1	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE0F	POE0 Flag	0: Indicates that a high-impedance control request has not been input to the POE0# pin input. 1: Indicates that a high-impedance control request has been input to the POE0# pin input.	R/(W)*2
b13 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

ICSR1 selects the input modes for the POE0# to POE3# pins, controls the enable/disable of interrupts, and indicates status.

POE0M[1:0] Bits (POE0 Mode Select)

These bits select the input mode of the POE0# pin.

PIE1 Bit (Port Interrupt Enable 1)

This bit enables or disables interrupt requests when any one of the POE0F bit of the ICSR1 is set to 1.

POE0F Flag (POE0 Flag)

This flag indicates that a high-impedance request has been input to the POE0# pin.
[Clearing condition]

- By writing 0 to POE0F after reading POE0F = 1
  When writing 0 to the flag while low-level sampling is selected with the POE8M[1:0] bits, the POE8# pin input must be at the high level.
  For details, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When the input set by POE0M[1:0] occurs at the POE0# pin

23.2.2 Input Level Control/Status Register 2 (ICSR2)

Address(es): 0008 C4C4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE4F	—	—	—	PIF2	—	—	—	—	—	—	POE4M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE4M[1:0]	POE4 Mode	b1 b0 0 0: Accepts a high-impedance control request on the falling edge of the POE4# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE4# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE4# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE4# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIF2	Port Interrupt Enable 1	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE4F	POE4 Flag	0: Indicates that a high-impedance control request has not been input to the POE4# pin input. 1: Indicates that a high-impedance control request has been input to the POE4# pin input.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

ICSR2 selects the input mode for the POE4# pin, controls the enable/disable of interrupts, and indicates status.

POE4M[1:0] Bits (POE4 Mode Select)

These bits select the input mode of the POE8# pin.

PIF2 Bit (Port Interrupt Enable 1)

This bit enables or disables interrupt requests when the POE4F bit in ICSR2 is set to 1.

POE4F Flag (POE4 Flag)

This flag indicates that a high-impedance request has been input to the POE4# pin.

[Clearing condition]

- By writing 0 to POE4F after reading POE4F = 1
  When writing 0 to the flag while low-level sampling is selected with the POE4M[1:0] bits, the POE4# pin input must be at the high level.
  For details, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When the input set by POE4M[1:0] occurs at the POE4# pin

23.2.3 Output Level Control/Status Register 1 (OCSR1)

Address(es): 0008 C4C2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OSF1	—	—	—	—	—	OCE1	OIE1	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b8	OIE1	Output Short Interrupt Enable 1	0: Interrupt requests disabled. 1: Interrupt requests enabled.	R/W
b9	OCE1	Output Short High-Impedance Enable 1	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b15	OSF1	Output Short Flag 1	0: Indicates that outputs have not simultaneously become an active level. 1: Indicates that outputs have simultaneously become an active level.	R/(W)*2

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

OCSR1 controls the enable/disable of output level comparison and interrupts, and indicates status.

OIE1 Bit (Output Short Interrupt Enable 1)

This bit enables or disables interrupt requests when the OSF1 bit in OCSR1 is set to 1.

OCE1 Bit (Output Short High-Impedance Enable 1)

This bit specifies whether to place the pins in high-impedance state when the OSF1 bit in OCSR1 is set to 1.

OSF1 Flag (Output Short Flag 1)

[144-, 120-, 112- and 100-pin versions]
This flag indicates that any one of the three pairs among P71 to P76 of two-phase MTU3 and MTU4 pins for MTU complementary PWM output or GPT0 to GPT2 pins for the GPT output to be compared has simultaneously become an active level.
[64- and 48-pin versions]
This flag indicates that any one of the three pairs among P71 to P76 of two-phase MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output or GPT0 to GPT2 pins for the GPT output to be compared has simultaneously become an active level.
[Clearing condition]

- By writing 0 to OSF1 after reading OSF1 = 1
  The complementary output pins for the MTU or GPT output pins must be at the inactive level when 0 is written to the flag.
  For details, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When any one of the three pairs of two-phase outputs has simultaneously become an active level

23.2.4 Output Level Control/Status Register 2 (OCSR2)

Address(es): 0008 C4C6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OSF2	—	—	—	—	—	OCE2	OIE2	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b8	OIE2	Output Short Interrupt Enable 2	0: Interrupt requests disabled. 1: Interrupt requests enabled.	R/W
b9	OCE2	Output Short High-Impedance Enable 2	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b15	OSF2	Output Short Flag 2	0: Indicates that outputs have not simultaneously become an active level. 1: Indicates that outputs have simultaneously become an active level.	R/(W)*2

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

OCSR2 controls the enable/disable of output level comparison and interrupts, and indicates status.

OIE2 Bit (Output Short Interrupt Enable 2)

This bit enables or disables interrupt requests when the OSF1 bit in OCSR1 is set to 1.

OCE2 Bit (Output Short High-Impedance Enable 2)

This bit specifies whether to place the pins in high-impedance state when the OSF2 bit in OCSR2 is set to 1.

OSF2 Flag (Output Short Flag 2)

This flag indicates that any one of the three pairs of two-phase MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output or GPT4 to GPT6 pins for the GPT output to be compared has simultaneously become an active level.

[Clearing condition]

- By writing 0 to OSF2 after reading OSF2 = 1
  The complementary output pins for the MTU or GPT output pins must be at the inactive level when 0 is written to the flag.
  For details, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When any one of the three pairs of two-phase outputs has simultaneously become an active level

23.2.5 Active Level Setting Register 1 (ALR1)

Address(es): 0008 C4DAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MTUCHSEL	OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSG0A	MTIOC3B/GTIOC0A Active Level Setting	0: Active low 1: Active high	R/W*1
b1	OLSG0B	MTIOC3D/GTIOC0sB Active Level Setting	0: Active low 1: Active high	R/W*1
b2	OLSG1A	MTIOC4A/GTIOC1A Active Level Setting	0: Active low 1: Active high	R/W*1
b3	OLSG1B	MTIOC4C/GTIOC1B Active Level Setting	0: Active low 1: Active high	R/W*1
b4	OLSG2A	MTIOC4B/GTIOC2A Active Level Setting	0: Active low 1: Active high	R/W*1
b5	OLSG2B	MTIOC4D/GTIOC2B Active Level Setting	0: Active low 1: Active high	R/W*1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	OLSEN	Active Level Setting Enable	0: Disabled 1: Enabled	R/W*1
b8	MTUCHSEL	MTU Output Active Level Channel Setting	[144-, 120-, 112- and 100-pin versions] This bit is read as 0. The write value should be 0. [64-, 48-pin versions] 0: Selects MTU3 and MTU4 (TOCR1A and TOCR2A) 1: Selects MTU6 and MTU7 (TOCR1B and TOCR2B)	R/W*1
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

ALR1 specifies the active levels of the MTU3 and GPT outputs for detection of short circuits of those outputs as reflected in OCSR1.

OLSG0A bit (MTIOC3B/GTIOC0A Active Level Setting)

[144-, 120-, 112- and 100-pin versions]

This bit sets the active level of the MTIOC3B and GTIOC0A outputs on P71. Specifically, setting the OLSG0A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

[64- and 48-pin versions]

This bit sets the active level of the MTIOC3B, MTIOC6B, and GTIOC0A outputs on P71. Specifically, setting the OLSG0A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG0B bit (MTIOC3D/GTIOC0B Active Level Setting)

[144-, 120-, 112- and 100-pin versions]

This bit sets the active level of the MTIOC3D and GTIOC0B outputs on P74. Specifically, setting the OLSG0B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

[64- and 48-pin versions]

This bit sets the active level of the MTIOC3D, MTIOC6D, and GTIOC0B outputs on P74. Specifically, setting the OLSG0B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG1A bit (MTIOC4A/GTIOC1A Active Level Setting)

[144-, 120-, 112- and 100-pin versions]
This bit sets the active level of the MTIOC4A and GTIOC1A outputs on P72. Specifically, setting the OLSG1A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.
[64- and 48-pin versions]
This bit sets the active level of the MTIOC4A, MTIOC7A, and GTIOC1A outputs on P72. Specifically, setting the OLSG1A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG1B bit (MTIOC4C/GTIOC1B Active Level Setting)

[144-, 120-, 112- and 100-pin versions]
This bit sets the active level of the MTIOC4C and GTIOC1B outputs on P75. Specifically, setting the OLSG1B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.
[64- and 48-pin versions]
This bit sets the active level of the MTIOC4C, MTIOC7C, and GTIOC1B outputs on P75. Specifically, setting the OLSG1B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG2A bit (MTIOC4B/GTIOC2A Active Level Setting)

[144-, 120-, 112- and 100-pin versions]
This bit sets the active level of the MTIOC4B and GTIOC2A outputs on P73. Specifically, setting the OLSG2A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.
[64- and 48-pin versions]
This bit sets the active level of the MTIOC4B, MTIOC7B, and GTIOC2A outputs on P73. Specifically, setting the OLSG2A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG2B bit (MTIOC4D/GTIOC2B Active Level Setting)

[144-, 120-, 112- and 100-pin versions]
This bit sets the active level of the MTIOC4D and GTIOC2B outputs on P76. Specifically, setting the OLSG2B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.
[64- and 48-pin versions]
This bit sets the active level of the MTIOC4D, MTIOC7D, and GTIOC2B outputs on P76. Specifically, setting the OLSG2B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSEN bit (Active Level Setting)

This bit selects enabling or disabling of the active-level settings in the OLSGnm bits (n is 0 to 2, m is A or B). Clearing the OLSEN bit to 0 disables the OLSGnm bits, in which case the active levels of the MTU output are determined by the MTU.TOCR1 and MTU.TOCR2 as selected by the MTUCHSEL bit.

Setting the OLSEN bit to 1 enables the OLSGnm bits, in which case the active levels of the MTU output are as selected by the OLSGnm bits in this register.

Active levels for the GPT output can only be set when the OLSEN bit is 1. When output short-circuit detection is to be used on the GPT outputs, set the OLSEN bit to 1 and then use the OLSGnm bits to set the active levels for the GPT outputs.

MTUCHSEL Bit (MTU Output Active Level Channel Setting)

This bit selects whether MTU3 and MTU4 (MTUn.TOCR1A, MTUn.TOCR2A) or MTU6 and MTU7 (MTUm.TOCR1B, MTUm.TOCR2B) are selected as the MTU complementary PWM output pins (n is 3 or 4, m is 6 or 7). When using the MTU complementary PWM output function, set the MTUCHSEL bit before setting the output pins after a reset. This bit is available with 64- and 48-pin products. In 144-, 120-, 112-, and 100-pin products, this bit is reserved and is read as 0. The write value should be 0.

23.2.6 Active Level Setting Register 2 (ALR2)

Address(es): 0008 C4DEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OLSEN	—	OLSG6B	OLSG6A	OLSG5B	OLSG5A	OLSG4B	OLSG4A
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSG4A	OLSG4A MTIOC6B/GTIOC4A Active Level Setting	0: Active low 1: Active high	R/W*1
b1	OLSG4B	OLSG4B MTIOC6D/GTIOC4B Active Level Setting	0: Active low 1: Active high	R/W*1
b2	OLSG5A	OLSG5A MTIOC7A/GTIOC5A Active Level Setting	0: Active low 1: Active high	R/W*1
b3	OLSG5B	OLSG5B MTIOC7C/GTIOC5B Active Level Setting	0: Active low 1: Active high	R/W*1
b4	OLSG6A	OLSG6A MTIOC7B/GTIOC6A Active Level Setting	0: Active low 1: Active high	R/W*1
b5	OLSG6B	OLSG6B MTIOC7D/GTIOC6B Active Level Setting	0: Active low 1: Active high	R/W*1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	OLSEN	Active Level Setting Enable	0: Disabled 1: Enabled	R/W*1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

ALR2 specifies the active levels of the MTU and GPT outputs for detection of short circuits of those outputs as reflected in OCSR2.

OLSG4A bit (MTIOC6B/GTIOC0A Active Level Setting)

This bit sets the active level of the MTIOC6B and GTIOC0A outputs. Specifically, setting the OLSG4A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG4B bit (MTIOC6D/GTIOC0B Active Level Setting)

This bit sets the active level of the MTIOC6D and GTIOC0B outputs. Specifically, setting the OLSG4B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG5A bit (MTIOC7A/GTIOC1A Active Level Setting)

This bit sets the active level of the MTIOC7A and GTIOC1A outputs. Specifically, setting the OLSG5A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG5B bit (MTIOC7C/GTIOC1B Active Level Setting)

This bit sets the active level of the MTIOC7C and GTIOC1B outputs. Specifically, setting the OLSG5B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG6A bit (MTIOC7B/GTIOC2A Active Level Setting)

This bit sets the active level of the MTIOC7B and GTIOC2A outputs. Specifically, setting the OLSG6A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG6B bit (MTIOC7D/GTIOC2B Active Level Setting)

This bit sets the active level of the MTIOC7D and GTIOC2B outputs. Specifically, setting the OLSG6B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSEN bit (Active Level Setting)

This bit selects enabling or disabling of the active-level settings in the OLSGnm bits (n is 4 to 6, m is A or B). Clearing the OLSEN bit to 0 disables the OLSGnm bits, in which case the active levels of the MTU output are determined by the MTU.TOCR1 and MTU.TOCR2 as selected by the MTUCHSEL bit.

Setting the OLSEN bit to 1 enables the OLSGnm bits, in which case the active levels of the MTU output are as selected by the OLSGnm bits in this register.

Active levels for the GPT output can only be set when the OLSEN bit is 1. When output short-circuit detection is to be used on the GPT outputs, set the OLSEN bit to 1 and then use the OLSGnm bits to set the active levels for the GPT outputs.

23.2.7 Input Level Control/Status Register 3 (ICSR3)

Address(es): 0008 C4C8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE8F	—	—	POE8E	PIE3	—	—	—	—	—	—	POE8M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE8M[1:0]	POE8 Mode Select	b1 b0 0 0: Accepts a high-impedance control request on the falling edge of the POE8# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE3	Port Interrupt Enable 3	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE8E	POE8 High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE8F	POE8 Flag	0: Indicates that a high-impedance control request has not been input to the POE8# pin input. 1: Indicates that a high-impedance control request has been input to the POE8# pin input.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

ICSR3 selects the input mode for the POE8# pin, controls the enable/disable of interrupts, and indicates status.

POE8M[1:0] Bits (POE8 Mode Select)

These bits select the input mode of the POE8# pin.

PIE3 Bit (Port Interrupt Enable 3)

This bit enables or disables interrupt requests when the POE8F bit in ICSR3 is set to 1.

POE8E Bit (POE8 High-Impedance Enable)

This bit specifies whether to place the corresponding pin in high-impedance state when the POE8F bit is set to 1.

POE8F Flag (POE8 Flag)

This flag indicates that a high-impedance request has been input to the POE8# pin.
[Clearing condition]

- By writing 0 to POE8F after reading POE8F = 1
  When low sampling is selected with the POE8M[1:0] bits, 0 can be written only after a high level is input to the POE8# pin.
  For the detail, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When the input set by POE8M[1:0] occurs at the POE8# pin

23.2.8 Input Level Control/Status Register 4 (ICSR4)

Address(es): 0008 C4D6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE10F	—	—	POE10E	PIE4	—	—	—	—	—	—	POE10M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE10M[1:0]	POE10 Mode Select	b1 b0 0 0: Accepts a high-impedance control request on the falling edge of the POE10# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b8	PIE4	Port Interrupt Enable 4	0: Interrupt requests disabled. 1: Interrupt requests enabled.	R/W
b9	POE10E	POE10 High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b12	POE10F	POE10 Flag	0: Indicates that a high-impedance control request has not been input to the POE10# pin input. 1: Indicates that a high-impedance control request has been input to the POE10# pin input.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	RW

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

ICSR4 selects the POE10# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE10M[1:0] Bits (POE10 Mode Select)

These bits select the input mode of the POE10# pin.

PIE4 Bit (Port Interrupt Enable 4)

This bit enables or disables interrupt requests when the POE10F bit is set to 1.

POE10E Bit (POE10 High-Impedance Enable)

This bit specifies whether to place the corresponding pin in high-impedance state when the POE10F bit is set to 1.

POE10F Bit (POE10 Flag)

This flag indicates that a request for the high-impedance state has been input to the POE10# pin.
[Clearing condition]

- By writing 0 to POE10F after reading POE10F = 1
  When low sampling is selected with the POE10M[1:0] bits, 0 can be written only after a high level is input to the POE10# pin.
  For the detail, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When the input set by POE10M[1:0] occurs at the POE10# pin

23.2.9 Input Level Control/Status Register 5 (ICSR5)

Address(es): 0008 C4D8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE11F	—	—	POE11E	PIE5	—	—	—	—	—	—	POE11M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	
b1, b0	POE11M[1:0]	POE11 Mode Select	b1 b0 0 0: Accepts a high-impedance control request on the falling edge of the POE11# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE11# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE11# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE11# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b8	PIE5	Port Interrupt Enable 5	0: Interrupt requests disabled. 1: Interrupt requests enabled.	R/W
b9	POE11E	POE11 High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b12	POE11F	POE11 Flag	0: Indicates that a high-impedance control request has not been input to the POE11# pin input. 1: Indicates that a high-impedance control request has been input to the POE11# pin input.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	RW

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

ICSR5 selects the POE11# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE11M[1:0] Bits (POE11 Mode Select)

These bits select the input mode of the POE11# pin.

PIE5 Bit (Port Interrupt Enable 5)

This bit enables or disables interrupt requests when the POE11F bit is set to 1.

POE11E Bit (POE11 High-Impedance Enable)

This bit specifies whether to place the corresponding pin in high-impedance state when the POE11F bit is set to 1.

POE11F Flag (POE11 Flag)

This flag indicates that a request for the high-impedance state has been input to the POE11# pin.

[Clearing condition]

- By writing 0 to POE11F after reading POE11F = 1
  When low sampling is selected with the POE11M[1:0] bits, 0 can be written only after a high level is input to the POE11# pin.
  For the detail, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When the input set by POE11M[1:0] occurs at the POE11# pin

23.2.10 Input Level Control/Status Register 7 (ICSR7)

Address(es): 0008 C4E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE12F	—	—	POE12E	PIE7	—	—	—	—	—	—	POE12M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	
b1, b0	POE12M[1:0]	POE12 Mode Select	b1 b0 0 0: Accepts a high-impedance control request on the falling edge of the POE12# pin input. 0 1: Accepts a high-impedance control request when the low level of the POE12# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a high-impedance control request when the low level of the POE12# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a high-impedance control request when the low level of the POE12# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b8	PIE7	Port Interrupt Enable 7	0: Interrupt requests disabled. 1: Interrupt requests enabled.	R/W
b9	POE12E	POE12 High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b12	POE12F	POE12 Flag	0: Indicates that a high-impedance control request has not been input to the POE12# pin input. 1: Indicates that a high-impedance control request has been input to the POE12# pin input.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	RW

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

ICSR7 selects the POE12# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE12M[1:0] Bits (POE12 Mode Select)

These bits select the input mode of the POE12# pin.

PIE7 Bit (Port Interrupt Enable 7)

This bit enables or disables interrupt requests when the POE7F bit is set to 1.

POE12E Bit (POE12 High-Impedance Enable)

This bit specifies whether to place the corresponding pin in high-impedance state when the POE12F bit is set to 1.

POE12F Flag (POE11 Flag)

This flag indicates that a request for the high-impedance state has been input to the POE12# pin.

[Clearing condition]

- By writing 0 to POE12F after reading POE12F = 1
  When low sampling is selected with the POE12M[1:0] bits, 0 can be written only after a high level is input to the POE12# pin.
  For the detail, see section 23.3.7, Release from High-Impedance State.

[Setting condition]

- When the input set by POE12M[1:0] occurs at the POE12# pin

23.2.11 Software Port Output Enable Register (SPOER)

Address(es): 0008 C4CAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	GPT67 HIZ	—	GPT23 HIZ	GPT01 HIZ	MTUC H0HIZ	MTUCH 67HIZ	MTUC H34HIZ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTUCH34HIZ	MTU3 and MTU4 or MTU6 and MTU7 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W
b1	MTUCH67HIZ	MTU6 and MTU7 Output High-Impedance Enable	[144-, 120-, 112- and 100-pin versions] 0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b2	MTUCH0HIZ	MTU0 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W
b3	GPT01HIZ	GPT0 and GPT1 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W
b4	GPT23HIZ	GPT2 and GPT3 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	RW
b5	—	Reserved	This bit is read as 0. The write value should be 0.	RW
b6	GPT67HIZ	GPT6 and GPT7 Output High-Impedance Enable	[144-, 120-, 112- and 100-pin versions] 0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	RW
b7	—	Reserved	This bit is read as 0. The write value should be 0.	RW

SPOER controls high-impedance state of the pins.

MTUCH34HIZ Bit (MTU3 and MTU4 Output High-Impedance Enable)

[144-, 120-, 112- and 100-pin versions]

This bit specifies whether to place P71 to P76, the MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D) or the GPT output pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, and GTIOC2B) are assigned to, in high-impedance state.

[64- and 48-pin versions]

This bit specifies whether to place P71 to P76, the MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D, or MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D) or the GPT output pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, and GTIOC2B) are

assigned to, in high-impedance state.
[Clearing condition]

- Reset
- By writing 0 to MTUCH34HIZ after reading MTUCH34HIZ = 1

[Setting condition]

- By writing 1 to MTUCH34HIZ

MTUCH67HIZ Bit (MTU6 and MTU7 Output High-Impedance Enable)

This bit specifies whether to place P90 to P95, the MTU complementary PWM output pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D) or the GPT output pins (GTIOC4A, GTIOC4B, GTIOC5A, GTIOC5B, GTIOC6A, and GTIOC6B) are assigned to, in high-impedance state.
[Clearing condition]

- Reset
- By writing 0 to MTUCH67HIZ after reading MTUCH67HIZ = 1

[Setting condition]

- By writing 1 to MTUCH67HIZ

MTUCH0HIZ Bit (MTU0 Output High-Impedance Enable)

This bit specifies whether to place the MTU0 pins of P30, P31, and PB0 to PB3, the MTU0 pins are assigned to, in high-impedance state.
[Clearing conditions]

- Reset
- By writing 0 to MTUCH0HIZ after reading MTUCH0HIZ = 1

[Setting condition]

- By writing 1 to MTUCH0HIZ

GPT01HIZ Bit (GPT0 and GPT1 Output High-Impedance Enable)

This bit specifies whether to place PD4 to PD7, the GPT0 and GPT1 pins (GTIOC0A, GTIOC0B, GTIOC1A, and GTIOC1B) are assigned to, in high-impedance state.
[Clearing conditions]

- Reset
- By writing 0 to GPT01HIZ after reading GPT01HIZ = 1

[Setting condition]

- By writing 1 to GPT01HIZ

GPT23HIZ Bit (GPT2 and GPT3 Output High-Impedance Enable)

[144-, 120-, 112- and 100-pin versions]
This bit specifies whether to place PD0 to PD3, the GPT2 and GPT3 pins (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B) are assigned to, in high-impedance state.
[64- and 48-pin versions]
This bit specifies whether to place P00, P01, PD3, PB6, and PB7, the GPT2 and GPT3 pins (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B) are assigned to, in high-impedance state.
[Clearing conditions]

- Reset
- By writing 0 to GPT23HIZ after reading GPT23HIZ = 1

[Setting condition]

- By writing 1 to GPT23HIZ

GPT67HIZ Bit (GPT6 and GPT7 Output High-Impedance Enable)

This bit specifies whether to place PG0, PG1, PG3, and PG4, the GPT 6 and GPT7 pins (GTIOC6A, GTIOC6B, GTIOC7A, and GTIOC7B) are assigned to, in high-impedance state.

[Clearing conditions]

- Reset
- By writing 0 to GPT67HIZ after reading GPT67HIZ = 1

[Setting condition]

- By writing 1 to GPT67HIZ

23.2.12 Port Output Enable Control Register 1 (POECR1)

Address(es): 0008 C4CBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MTU0DZE	MTU0CZE	MTU0BZE	MTU0AZE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTU0AZE	MTU CH0A High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b1	MTU0BZE	MTU CH0B High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b2	MTU0CZE	MTU CH0C High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b3	MTU0DZE	MTU CH0D High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

POECR1 controls high-impedance state of the MTU0 pins.

MTU0AZE Bit (MTU CH0A High-Impedance Enable)

This bit specifies whether to place P31 and PB3, the MTIOC0A output for the MTU0 pin is assigned to, in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, OSTSTE bit in ICSR6, or, as additionally specified in the POECR5, the POEmF (n is 1, 2, 4, 5 or 7, m is 0, 4, 10, 11 or 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU0BZE Bit (MTU CH0B High-Impedance Enable)

This bit specifies whether to place P30 and PB2, the MTIOC0B output for the MTU0 pin is assigned to, in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, OSTSTE bit in ICSR6, or, as additionally specified in the POECR5, the POEmF (n is 1, 2, 4, 5 or 7, m is 0, 4, 10, 11 or 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU0CZE Bit (MTU CH0C High-Impedance Enable)

This bit specifies whether to place PB1, the MTIOC0C output for the MTU0 pin is assigned to, in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, and OSTSTE bit in ICSR6, or, as additionally specified in the POECR5, the POEmF (n is 1, 2, 4, 5 or 7, m is 0, 4, 10, 11 or 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU0DZE Bit (MTU CH0D High-Impedance Enable)

This bit specifies whether to place PB0, the MTIOC0D output for the MTU0 pin is assigned to, in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, and OSTSTE bit in ICSR6, or, as additionally specified in the POECR5, the POEmF (n is 1, 2, 4, 5 or 7, m is 0, 4, 10, 11 or 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

23.2.13 Port Output Enable Control Register 2 (POECR2)

Address(es): 0008 C4CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE	—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	MTU7BDZE	MTU CH7BD High Impedance Enable	[144-, 120-, 112- and 100-pin versions] 0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W*1
b1	MTU7ACZE	MTU CH7AC High Impedance Enable	[144-, 120-, 112- and 100-pin versions] 0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W*1
b2	MTU6BDZE	MTU CH6BD High Impedance Enable	[144-, 120-, 112- and 100-pin versions] 0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	MTU4BDZE	MTU CH4BD High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b9	MTU4ACZE	MTU CH4AC High-Impedance Enable	This bit is read as 0. The write value should be 0.	R/W*1
b10	MTU3BDZE	MTU CH3BD High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	RW

Note 1. Can be modified only once after a reset.

POECR2 controls high-impedance state of the MTU complementary PWM output pins (MTU3, MTU4, MTU6, and MTU7 pins) and the GPT output pin (GPT0 to GPT2 pins).

MTU7BDZE Bit (MTU CH7BD High-Impedance Enable)

This bit specifies whether to place P93 and P90, the MTIOC7B/GTIOC6A outputs and MTIOC7D/GTIOC6B outputs for the MTU7/GPT6 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH67HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU7ACZE Bit (MTU CH7AC High-Impedance Enable)

This bit specifies whether to place P94 and P91, the MTIOC7A/GTIOC5A outputs and MTIOC7C/GTIOC5B outputs for the MTU7/GPT5 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH67HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU6BDZE Bit (MTU CH6BD High-Impedance Enable)

This bit specifies whether to place P95 and P92, the MTIOC6B/GTIOC4A outputs and MTIOC6D/GTIOC4B outputs for the MTU6/GPT4 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH67HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU4BDZE Bit (MTU CH4BD High-Impedance Enable)

[144-, 120-, 112- and 100-pin versions]

This bit specifies whether to place P73 and P76, the MTIOC4B/GTIOC2A outputs and MTIOC4D/GTIOC2B outputs for the MTU4/GPT2 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

[64- and 48-pin versions]

This bit specifies whether to place P73 and P76, the MTIOC4B/MTIOC7B/GTIOC2A outputs and MTIOC4D/MTIOC7D/GTIOC2B outputs for the MTU4/MTU7/GPT2 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU4ACZE Bit (MTU CH4AC High-Impedance Enable)

[144-, 120-, 112- and 100-pin versions]

This bit specifies whether to place P72 and P75, the MTIOC4A/GTIOC1A outputs and MTIOC4C/GTIOC1B outputs for the MTU4/GPT1 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

[64- and 48-pin versions]

This bit specifies whether to place P72 and P75, the MTIOC4A/MTIOC7A/GTIOC1A outputs and MTIOC4C/MTIOC7C/GTIOC1B outputs for the MTU4/MTU7/GPT1 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

MTU3BDZE Bit (MTU CH3BD High-Impedance Enable)

[144-, 120-, 112- and 100-pin versions]

This bit specifies whether to place P71 and P74, the MTIOC3B/GTIOC0A outputs and MTIOC3D/GTIOC0B outputs for the MTU3/GPT0 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

[64- and 48-pin versions]

This bit specifies whether to place P71 and P74, the MTIOC3B/MTIOC6B/GTIOC0A outputs and MTIOC3D/MTIOC6D/GTIOC0B outputs for the MTU3/MTU6/GPT0 pins are assigned to, in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR4 register, the POEmF (n is 3 to 5, m is 8 or 10 to 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

23.2.14 Port Output Enable Control Register 3 (POECR3)

Address(es): 0008 C4CEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	GPT3ABZE	GPT2ABZE	—	—	—	—	—	—	GPT1ABZE	GPT0ABZE
Value after reset:	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	GPT0ABZE	GPT CH0AB High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b1	GPT1ABZE	GPT CH1AB High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	GPT2ABZE	GPT CH2AB High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b9	GPT3ABZE	GPT CH3AB High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0	RW

Note 1. Can be modified only once after a reset.

POECR3 controls high-impedance state of the GPT pin.

GPT0ABZE Bit (GPT CH0AB High-Impedance Enable)

This bit specifies whether to place PD7 and PD6, the GTIOC0A/GTIOC0B outputs for the GPT0 pin is assigned to, in high-impedance state when any one of the POE10F flag in ICSR4, GPT01HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR6, the POEmF (n is 1 to 3, 5, or 7, m is 0, 4, 8, 11, or 12) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

GPT1ABZE Bit (GPT CH1AB High-Impedance Enable)

This bit specifies whether to place PD5 and PD4, the GTIOC1A/GTIOC1B outputs for the GPT1 pin is assigned to, in high-impedance state when any one of the POE10F flag in ICSR4, GPT01HIZ bit in SPOER, OSTSTE bit in ICSR6, as additionally specified in the POECR6, the POEmF (n is 1, 3, or 5, m is 0, 8, or 11) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

GPT2ABZE Bit (GPT CH2AB High-Impedance Enable)

[144-, 120-, 112- and 100-pin versions]

This bit specifies whether to place PD3 and PD2, the GTIOC2A/GTIOC2B/GTIOC2B-C outputs for the GPT2 pin is assigned to, in high-impedance state when any one of the POE11F flag in ICSR5, GPT23HIZ bit in SPOER, OSTSTE bit in ICSR6, as additionally specified in the POECR6, the POEmF (n is 1, 3, or 4, m is 0, 8, or 10) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

[64- and 48-pin versions]

This bit specifies whether to place PD3, PB6 and PB7, the GTIOC2A/GTIOC2B outputs for the GPT2 pin is assigned to, in high-impedance state when any one of the POE11F flag in ICSR5, GPT23HIZ bit in SPOER, OSTSTE bit in ICSR6, as additionally specified in the POECR6, the POEmF (n is 1, 3, or 4, m is 0, 8, or 10) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

GPT3ABZE Bit (GPT CH3AB High-Impedance Enable)

[144-, 120-, 112- and 100-pin versions]

This bit specifies whether to place PD1 and PD0, the GTIOC3A/GTIOC3B outputs for the GPT3 pin is assigned to, in high-impedance state when any one of the POE11F flag in ICSR5, GPT23HIZ bit in SPOER, OSTSTE bit in ICSR6, as additionally specified in the POECR6, the POEmF (n is 1, 3, or 4, m is 0, 8, or 10) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

[64- and 48-pin versions]

This bit specifies whether to place P00 and P01, the GTIOC3A/GTIOC3B outputs for the GPT3 pin is assigned to, in high-impedance state when any one of the POE11F flag in ICSR5, GPT23HIZ bit in SPOER, OSTSTE bit in ICSR6, as additionally specified in the POECR6, the POEmF (n is 1, 3, or 4, m is 0, 8, or 10) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

23.2.15 Port Output Enable Control Register 4 (POECR4)

Address(es): 0008 C4D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IC6ADDMT67ZE	IC5ADDMT67ZE	IC4ADDMT67ZE	IC3ADDMT67ZE	—	IC1ADDMT67ZE	CMADOMT67ZE	—	IC6ADDMT34ZE	IC5ADDMT34ZE	IC4ADDMT34ZE	IC3ADDMT34ZE	IC2ADDMT34ZE	—	CMADDMT34ZE
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDMT34ZE	MTU CH34 High-Impedance CFLAG Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	RW
b2	IC2ADDMT34ZE	MTU CH34 High-Impedance POE4F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b3	IC3ADDMT34ZE	MTU CH34 High-Impedance POE8F Add	0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W
b4	IC4ADDMT34ZE	MTU CH34 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b5	IC5ADDMT34ZE	MTU CH34 High-Impedance POE11F Add	0: Does not add the pins the high-impedance control conditions. 1: Adds the pins to high-impedance conditions.	R/W*1
b6	IC6ADDMT34ZE	MTU CH34 High-Impedance POE12F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0	R/W
b8	CMADOMT67ZE	MTU CH67 High-Impedance CFLAG Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b9	IC1ADDMT67ZE	MTU CH67 High-Impedance POE0F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b10	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b11	IC3ADDMT67ZE	MTU CH67 High-Impedance POE8F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b12	IC4ADDMT67ZE	MTU CH67 High-Impedance POE10F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b13	IC5ADDMT67ZE	MTU CH67 High-Impedance POE11F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b14	IC6ADDMT67ZE	MTU CH67 High-Impedance POE12F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR4 is used to extend the control conditions of the high-impedance state for the MTU3, MTU4, MTU6, and MTU7 pins for the MTU complementary PWM output and the GPT0 to GPT2, and GPT4 to GPT6 pins for the GPT output.

CMADDMT34ZE Bit (MTU CH34 High-Impedance CFLAG Add)

Adds the CjFLAG (n is 0 or 1, j is 000 to 002) flag in the ADCMPFR of the S12ADn to the high-impedance control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/MTIOC3D/GTIOC0A/GTIOC0B/MTIOC4A/MTIOC4C/GTIOC1A/GTIOC1B/MTIOC4B/MTIOC4D/GTIOC2A/GTIOC2B). However, when this flag is placed in the high-impedance, the OEIn (n is 1 to 5) interrupt will not occur.

IC2ADDMT34ZE Bit (MTU CH34 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 to the high-impedance control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins ICSR2 (MTIOC3B/MTIOC3D/GTIOC0A/GTIOC0B/MTIOC4A/MTIOC4C/GTIOC1A/GTIOC1B/MTIOC4B/MTIOC4D/GTIOC2A/GTIOC2B).

IC3ADDMT34ZE Bit (MTU CH34 High-Impedance POE8F Add)

Adds the POE8F flag in ICSR3 to the high-impedance control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/MTIOC3D/GTIOC0A/GTIOC0B/MTIOC4A/MTIOC4C/GTIOC1A/GTIOC1B/MTIOC4B/MTIOC4D/GTIOC2A/GTIOC2B).

IC4ADDMT34ZE Bit (MTU CH34 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR4 to the high-impedance control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/MTIOC3D/GTIOC0A/GTIOC0B/MTIOC4A/MTIOC4C/GTIOC1A/GTIOC1B/MTIOC4B/MTIOC4D/GTIOC2A/GTIOC2B).

IC5ADDMT34ZE Bit (MTU CH34 High-Impedance POE11F Add)

Adds the POE11F flag in ICSR5 to the high-impedance control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/MTIOC3D/GTIOC0A/GTIOC0B/MTIOC4A/MTIOC4C/GTIOC1A/GTIOC1B/MTIOC4B/MTIOC4D/GTIOC2A/GTIOC2B).

IC6ADDMT34ZE Bit (MTU CH34 High-Impedance POE12F Add)

Adds the POE12F flag in ICSR7 to the high-impedance control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/MTIOC3D/GTIOC0A/GTIOC0B/MTIOC4A/MTIOC4C/GTIOC1A/GTIOC1B/MTIOC4B/MTIOC4D/GTIOC2A/GTIOC2B).

CMADOMT67ZE Bit (MTU CH67 High-Impedance CFLAG Add)

Adds the CjFLAG (n is 0 or 1, j is 000 to 002) flag in the ADCMPFR of the S12AD to the high-impedance control conditions for the MTU6, MTU7, and GPT4 to GPT6 pins of P90 to P95 (MTIOC6B/MTIOC6D/GTIOC4A/GTIOC4B/MTIOC7A/MTIOC7C/GTIOC5A/GTIOC5B/MTIOC7B/MTIOC7D/GTIOC6A/GTIOC6B). However, when this flag is placed in the high-impedance, the OEIn (n is 1, or 5) interrupt will not occur.

IC1ADDMT67ZE Bit (MTU CH67 High-Impedance POE0F Add)

Adds the POE0F flag in ICSR1 to the high-impedance control conditions for the MTU6, MTU7, and GPT4 to GPT6 pins of P90 to P95 (MTIOC6B/MTIOC6D/GTIOC4A/GTIOC4B/MTIOC7A/MTIOC7C/GTIOC5A/GTIOC5B/MTIOC7B/MTIOC7D/GTIOC6A/GTIOC6B).

IC3ADDMT67ZE Bit (MTU CH67 High-Impedance POE8F Add)

Adds the POE8F flag in ICSR3 to the high-impedance control conditions for the MTU6, MTU7, and GPT4 to GPT6 pins of P90 to P95 (MTIOC6B/MTIOC6D/GTIOC4A/GTIOC4B/MTIOC7A/MTIOC7C/GTIOC5A/GTIOC5B/MTIOC7B/MTIOC7D/GTIOC6A/GTIOC6B).

IC4ADDMT67ZE Bit (MTU CH67 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR4 to the high-impedance control conditions for the MTU6, MTU7, and GPT4 to GPT6 pins of P90 to P95 (MTIOC6B/MTIOC6D/GTIOC4A/GTIOC4B/MTIOC7A/MTIOC7C/GTIOC5A/GTIOC5B/MTIOC7B/MTIOC7D/GTIOC6A/GTIOC6B).

IC5ADDMT67ZE Bit (MTU CH67 High-Impedance POE11F Add)

Adds the POE11F flag in ICSR5 to the high-impedance control conditions for the MTU3, MTU4, MTU6, MTU7, and GPT4 to GPT6 pins of P90 to P95 (MTIOC6B/MTIOC6D/GTIOC4A/GTIOC4B/MTIOC7A/MTIOC7C/GTIOC5A/GTIOC5B/MTIOC7B/MTIOC7D/GTIOC6A/GTIOC6B).

IC6ADDMT67ZE Bit (MTU CH67 High-Impedance POE12F Add)

Adds the POE12F flag in ICSR7 to the high-impedance control conditions for the MTU6, MTU7, and GPT4 to GPT6 pins of P90 to P95 (MTIOC6B/MTIOC6D/GTIOC4A/GTIOC4B/MTIOC7A/MTIOC7C/GTIOC5A/GTIOC5B/MTIOC7B/MTIOC7D/GTIOC6A/GTIOC6B).

23.2.16 Port Output Enable Control Register 5 (POECR5)

Address(es): 0008 C4D2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	IC6ADDMT0ZE	IC5ADDMT0ZE	IC4ADDMT0ZE	—	IC2ADDMT0ZE	IC1ADDMT0ZE	CMADDMT0ZE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDMT0ZE	MTU CH0 High-Impedance CFLAG Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b1	IC1ADDMT0ZE	MTU CH0 High-Impedance POE0F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b2	IC2ADDMT0ZE	MTU CH0 High-Impedance POE4F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W*1
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	IC4ADDMT0ZE	MTU CH0 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b5	IC5ADDMT0ZE	MTU CH0 High-Impedance POE11F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b6	IC6ADDMT0ZE	MTU CH0 High-Impedance POE12F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W*1
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR5 is used to extend the control conditions of the high-impedance for the MTU0 pin.

CMADDMT0ZE Bit (MTU CH0 High-Impedance CFLAG Add)

The CjFLAG (n is 0 or 1, j is 000 to 002) flag in the ADCMPFR of the S12ADAn is added to the high-impedance control conditions for the MTU0 pins of P30, P31, and PB0 to PB3 (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D). However, when this flag is placed in the high-impedance, the OEIn (n is 1 to 5) interrupt will not occur.

IC1ADDMT0ZE Bit (MTU CH0 High-Impedance POE0F Add)

Adds the POE0F flag in ICSR1 to the high-impedance control conditions for the MTU0 pins of P30, P31, and PB0 to PB3 (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC2ADDMT0ZE Bit (MTU CH0 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 to the high-impedance control conditions for the MTU0 pins of P30, P31, and PB0 to PB3 (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC4ADDMT0ZE Bit (MTU CH0 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR4 to the high-impedance control conditions for the MTU0 pins of P30, P31, and PB0 to PB3 (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC5ADDMT0ZE Bit (MTU CH0 High-Impedance POE11F Add)

Adds the POE11F flag in ICSR5 to the high-impedance control conditions for the MTU0 pins of P30, P31, and PB0 to PB3 (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC6ADDMT0ZE Bit (MTU CH0 High-Impedance POE12F Add)

Adds the POE12F flag in ICSR7 to the high-impedance control conditions for the MTU0 pins of P30, P31, and PB0 to PB3 (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

23.2.17 Port Output Enable Control Register 6 (POECR6)

Address(es): 0008 C4D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IC6ADDGPT23ZE	—	IC4ADDGPT23ZE	IC3ADDGPT23ZE	IC2ADDGPT23ZE	IC1ADDGPT23ZE	CMADDGPT23ZE	—	IC6ADDGPT01ZE	IC5ADDGPT01ZE	—	IC3ADDGPT01ZE	IC2ADDGPT01ZE	IC1ADDGPT01ZE	CMADDGPT01ZE
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDGPT01ZE	GPT CH01 High-Impedance CFLAG Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b1	IC1ADDGPT01ZE	GPT CH01 High-Impedance POE0F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b2	IC2ADDGPT01ZE	GPT CH01 High-Impedance POE4F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W *1
b3	IC3ADDGPT01ZE	GPT CH01 High-Impedance POE8F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b4	—	Reserved	This bit is always read as 1. The write value should be 1.	R/W
b5	IC5ADDGPT01ZE	GPT CH01 High-Impedance POE11F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b6	IC6ADDGPT01ZE	GPT CH01 High-Impedance POE12F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W *1
b7	—	Reserved	This bit is read as 0. The write value should be 0	R/W
b8	CMADDGPT23ZE	GPT CH23 High-Impedance CFLAG Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b9	IC1ADDGPT23ZE	GPT CH23 High-Impedance POE0F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b10	IC2ADDGPT23ZE	GPT CH23 High-Impedance POE4F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W *1
b11	IC3ADDGPT23ZE	GPT CH23 High-Impedance POE8F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b12	IC4ADDGPT23ZE	GPT CH23 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W *1
b13	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b14	IC6ADDGPT23ZE	GPT CH23 High-Impedance POE12F Add	[144-, 120-, 112- and 100-pin versions] 0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions. [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W *1
b15	—	Reserved	This bit is are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR6 is used to extend the control conditions of the high-impedance for the GPT0 to GPT3 pins.

CMADDGPT01ZE Bit (GPT CH01 High-Impedance CFLAG Add)

Adds the CjFLAG (n is 0 or 1, j is 000 to 002) flag in the ADCMPFR of the S12ADn to the high-impedance control conditions for the GPT0 and GPT1 pins of PD4 to PD7 (GTIOC0A, GTIOC0B, GTIOC1A, and GTIOC1B). However, when this flag is placed in the high-impedance, the OEIn (n is 1 to 5) interrupt will not occur.

IC1ADDGPT01ZE Bit (GPT CH01 High-Impedance POE0F Add)

Adds the POE0F flag in ICSR1 to the high-impedance control conditions for the GPT0 and GPT1 pins of PD4 to PD7 (GTIOC0A, GTIOC0B, GTIOC1A, and GTIOC1B).

IC2ADDGPT01ZE Bit (GPT CH01 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 to the high-impedance control conditions for the GPT0 and GPT1 pins of PD4 to PD7 (GTIOC0A, GTIOC0B, GTIOC1A, and GTIOC1B).

IC3ADDGPT01ZE Bit (GPT CH01 High-Impedance POE8F Add)

Adds the POE8F flag in ICSR3 to the high-impedance control conditions for the GPT0 and GPT1 pins of PD4 to PD7 (GTIOC0A, GTIOC0B, GTIOC1A, and GTIOC1B).

IC5ADDGPT01ZE Bit (GPT CH01 High-Impedance POE11F Add)

Adds the POE11F flag in ICSR5 to the high-impedance control conditions for the GPT0 and GPT1 pins of PD4 to PD7 (GTIOC0A, GTIOC0B, GTIOC1A, and GTIOC1B).

IC6ADDGPT01ZE Bit (GPT CH01 High-Impedance POE12F Add)

Adds the POE12F flag in ICSR7 to the high-impedance control conditions for the GPT0 and GPT1 pins of PD4 to PD7 (GTIOC0A, GTIOC0B, GTIOC1A, and GTIOC1B).

CMADDGPT23ZE Bit (GPT CH23 High-Impedance CFLAG Add)

[144-, 120-, 112- and 100-pin versions]

The CjFLAG (n is 0 or 1, j is 000 to 002) flag in the ADCMPFR of the S12ADn is added to the high-impedance control conditions for the GPT2 and GPT3 pins of PD0 to PD3 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B). However, when those flags are placed in the high-impedance, the OEIn (n is 1 to 5) interrupt will not occur.

[64- and 48-pin versions]

The CjFLAG (n is 0 or 1, j is 000 to 002) flag in the ADCMPFR of the S12ADn is added to the high-impedance control conditions for the GPT2 and GPT3 pins of PD3, PB6, PB7, P00, and P01 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B). However, when those flags are placed in the high-impedance, the OEIn (n is 1 to 5) interrupt will not occur.

IC1ADDGPT23ZE Bit (GPT CH23 High -Impedance POE0F Add)

[144-, 120-, 112- and 100-pin versions]

Adds the POE0F flag in ICSR1 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD0 to PD3 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B).

[64- and 48-pin versions]

Adds the POE0F flag in ICSR1 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD3, PB6, PB7, P00, and P01 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B).

IC2ADDGPT23ZE Bit (GPT CH23 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD0 to PD3 (GTIOC2A, GTIOC2B, GTIOC2B, GTIOC3A, and GTIOC3B).

IC3ADDGPT23ZE Bit (GPT CH23 High -Impedance POE8F Add)

[144-, 120-, 112- and 100-pin versions]

Adds the POE8F flag in ICSR1 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD0 to PD3 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B).

[64- and 48-pin versions]

Adds the POE8F flag in ICSR1 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD3, PB6, PB7, P00, and P01 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B).

IC4ADDGPT23ZE Bit (GPT CH23 High -Impedance POE10F Add)

[144-, 120-, 112- and 100-pin versions]

Adds the POE10F flag in ICSR1 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD0 to PD3 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B).

[64- and 48-pin versions]

Adds the POE10F flag in ICSR1 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD3, PB6, PB7, P00, and P01 (GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B).

IC6ADDGPT23ZE Bit (GPT CH23 High-Impedance POE12F Add)

Adds the POE12F flag in ICSR7 to the high-impedance control conditions for the GPT2 and GPT3 pins of PD0 to PD3 (GTIOC2A, GTIOC2B, GTIOC2B, GTIOC3A, and GTIOC3B).

23.2.18 Port Output Enable Control Register 7 (POECR7)

Address(es): 0008 C4E2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	GPT7ABZE	GPT6ABZE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	GPT6ABZE	GPT6ABZE High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b9	GPT7ABZE	GPT7ABZE High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

POECR7 controls high-impedance state of the GPT6 and GPT7 pins.

GPT6ABZE Bit (GPT6ABZE High-Impedance Enable)

This bit specifies whether to place PG3 and PG4, the GTIOC6A/GTIOC6B outputs for the GPT6 pin is assigned to, in high-impedance state when any one of the POE12F flag in ICSR7, GPT67HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR8, the POEmF (n = 1 to 5, m = 0, 4, 8, 10, and 11) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

GPT7ABZE Bit (GPT7ABZE High-Impedance Enable)

This bit specifies whether to place PG0 and PG1, the GTIOC7A/GTIOC7B outputs for the GPT7 pin is assigned to, in high-impedance state when any one of the POE12F flag in ICSR7, GPT67HIZ bit in SPOER, OSTSTE bit in ICSR6 or, as additionally specified in the POECR8, the POEmF (n = 1 to 5, m = 0, 4, 8, 10, and 11) flag in ICSRn and CjFLAG (n is 0 or 1, j is 000 to 002) flag in ADCMPFR of the S12ADn, is set to 1.

23.2.19 Port Output Enable Control Register 8 (POECR8)

Address(es): 0008 C4E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	IC5ADDGPT67ZE	IC4ADDGPT67ZE	IC3ADDGPT67ZE	IC2ADDGPT67ZE	IC1ADDGPT67ZE	CMADDGPT67ZE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDGPT67ZE	GPT CH67 High-Impedance CFLAG Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b1	IC1ADDGPT67ZE	GPT CH67 High-Impedance POE0F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b2	IC2ADDGPT67ZE	GPT CH67 High-Impedance POE4F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b3	IC3ADDGPT67ZE	GPT CH67 High-Impedance POE8F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b4	IC4ADDGPT67ZE	GPT CH67 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b5	IC5ADDGPT67ZE	GPT CH67 High-Impedance POE11F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to high-impedance control conditions.	R/W*1
b6	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR8 is used to extend the control conditions of the high-impedance for the GPT6 and GPT7 pins.

CMADDGPT67ZE Bit (GPT CH67 High-Impedance CFLAG Add)

The CjFLAG (n is 0 or 1, j is 000 to 002) flag in the ADCMPFR of the S12AD is added to the high-impedance control conditions for the GPT6 and GPT7 pins of PG0, PG1, PG3, and PG4 (GTIOC6A, GTIOC6B, GTIOC7A, GTIOC7B). However, when this flag is placed in the high-impedance, the OEIn (n is 1 to 5) interrupt will not occur.

IC1ADDGPT67ZE Bit (GPT CH67 High-Impedance POE0F Add)

Adds the POE0F flag in ICSR1 to the high-impedance control conditions for the GPT6 and GPT7 pins of PG0, PG1, PG3, and PG4 (GTIOC6A, GTIOC6B, GTIOC7A, GTIOC7B).

IC2ADDGPT67ZE Bit (GPT CH67 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 to the high-impedance control conditions for the GPT6 and GPT7 pins of PG0, PG1, PG3, and PG4 (GTIOC6A, GTIOC6B, GTIOC7A, GTIOC7B).

IC3ADDGPT67ZE Bit (GPT CH67 High-Impedance POE8F Add)

Adds the POE7F flag in ICSR3 to the high-impedance control conditions for the GPT6 and GPT7 pins of PG0, PG1, PG3, and PG4 (GTIOC6A, GTIOC6B, GTIOC7A, GTIOC7B).

IC4ADDGPT67ZE Bit (GPT CH67 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR4 to the high-impedance control conditions for the GPT6 and GPT7 pins of PG0, PG1, PG3, and PG4 (GTIOC6A, GTIOC6B, GTIOC7A, GTIOC7B).

IC5ADDGPT67ZE Bit (GPT CH67 High-Impedance POE11F Add)

Adds the POE11F flag in ICSR5 to the high-impedance control conditions for the GPT6 and GPT7 pins of PG0, PG1, PG3, and PG4 (GTIOC6A, GTIOC6B, GTIOC7A, GTIOC7B).

23.2.20 Input Level Control/Status Register 6 (ICSR6)

Address(es): 0008 C4DCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OSTSTF	—	—	OSTSTE	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	OSTSTE	OSTST High-Impedance Enable	0: Does not place the MTU complementary PWM output pins, MTU0 pins, or GPT pins in high-impedance state. 1: Places the MTU complementary PWM output pins, MTU0 pins, and GPT pins in high-impedance state.	R/W*1
b11 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	OSTSTF	OSTST High-Impedance Flag	0: Indicates that a stopped oscillation high-impedance request has not been generated. 1: Indicates that a stopped oscillation high-impedance request has been generated.	R/W*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

ICSR6 controls the stopped oscillation high-impedance and indicates status.

OSTSTE Bit (OSTST High-Impedance Enable)

This bit enables/disables the MTU complementary PWM output pins, MTU0 pins, and GPT pins to be placed in the high-impedance state when stopped oscillation is detected.

OSTSTF Flag (OSTST High-Impedance Enable)

This flag indicates that a stopped oscillation high-impedance request has been generated.
When stopped oscillation is detected, this flag is set to 1. When clearing this flag to 0, do so while the stopped oscillation detection signal is negated; writing 0 to this flag while the stopped oscillation detection signal is asserted does not clear this flag to 0. After clearing this flag, confirm that the flag has actually been modified to 0.

[Clearing condition]

- By writing 0 to OSTSTF after reading OSTSTF = 1

[Setting condition]

- When stopped oscillation is detected

23.3 Operation

Table 23.4 shows the target pins for high-impedance control and conditions to place the pins in high-impedance state.

Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions] (1/6)

Pins	Conditions	Detailed Conditions
MTU3B/MTU3D pins (MTIOC3B (P71) and MTIOC3D (P74))	• POE0# input level detection • MTIOC3B and MTIOC3D output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE4#, POE8#, POE10#, POE11#, POE12# input level detection	MTU3BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC2ADDMT34ZE•POE4F) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F) + (IC6ADDMT34ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
MTU4A/MTU4C pins (MTIOC4A (P72) and MTIOC4C (P75))	• POE0# input level detection • MTIOC4A and MTIOC4C output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE4#, POE8#, POE10#, POE11#, POE12# input level detection	MTU4ACZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC2ADDMT34ZE•POE4F) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F) + (IC6ADDMT34ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
MTU4B/MTU4D pins (MTIOC4B (P73) and MTIOC4D (P76))	• POE0# input level detection • MTIOC4B and MTIOC4D output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE4#, POE8#, POE10#, POE11#, POE12# input level detection	MTU4BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC2ADDMT34ZE•POE4F) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F) + (IC6ADDMT34ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
MTU6B/MTU6D pins (MTIOC6B (P95) and MTIOC6D (P92))	• POE4# input level detection • MTIOC6B and MTIOC6D output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 - 12-bit A/D converter comparator detection - POE0#, POE8#, POE10#, POE11#, POE12# input level detection	MTU6BDZE• ((POE4F) + (OSF2•OCE2) + (MTUCH67HIZ) + (ICSR6.OSTSTE) + (CMADDMT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT67ZE•POE0F) + (IC3ADDMT67ZE•POE8E•POE8F) + (IC4ADDMT67ZE•POE10E•POE10F) + (IC5ADDMT67ZE•POE11E•POE11F) + (IC6ADDMT67ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)

Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions] (2/6)

Pins	Conditions	Detailed Conditions
MTU7A/MTU7C pins (MTIOC7A (P94) and MTIOC7C (P91))	• POE4# input level detection • MTIOC7A and MTIOC7C output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 - 12-bit A/D converter comparator detection - POE0#, POE8#, POE10#, POE11#, POE12# input level detection	MTU7ACZE• ((POE4F) + (OSF2•OCE2) + (MTUCH67HIZ) + (ICSR6.OSTSTE) + (CMADDMT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT67ZE•POE0F) + (IC3ADDMT67ZE•POE8E•POE8F) + (IC4ADDMT67ZE•POE10E•POE10F) + (IC5ADDMT67ZE•POE11E•POE11F) + (IC6ADDMT67ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
MTU7B/MTU7D pins (MTIOC7B (P93) and MTIOC7D (P90))	• POE4# input level detection • MTIOC7B and MTIOC7D output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 - 12-bit A/D converter comparator detection - POE0#, POE8#, POE10#, POE11#, POE12# input level detection	MTU7BDZE• ((POE4F) + (OSF2•OCE2) + (MTUCH67HIZ) + (ICSR6.OSTSTE) + (CMADDMT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT67ZE•POE0F) + (IC3ADDMT67ZE•POE8E•POE8F) + (IC4ADDMT67ZE•POE10E•POE10F) + (IC5ADDMT67ZE•POE11E•POE11F) + (IC6ADDMT67ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
GPT0 pins (GTIOC0A (P71) and GTIOC0B (P74))	• POE0# input level detection • GTIOC0A-A and GTIOC0B-A output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE4#, POE8#, POE10#, POE11#, POE12# input level detection	MTU3BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC2ADDMT34ZE•POE4F) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F) + (IC6ADDMT34ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
GPT1 pins (GTIOC1A (P72) and GTIOC1B (P75))	• POE0# input level detection • GTIOC1A-A and GTIOC1B-A output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE4#, POE8#, POE10#, POE11#, POE12# input level detection	MTU4ACZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC2ADDMT34ZE•POE4F) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F) + (IC6ADDMT34ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)

Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions] (3/6)

Pins	Conditions	Detailed Conditions
GPT2 pins (GTIOC2A (P73) and GTIOC2B (P76))	• POE0# input level detection • GTIOC2A-A and GTIOC2B-A output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE4#, POE8#, POE10#, POE11#, POE12# input level detection	MTU4BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC2ADDMT34ZE•POE4F) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F) + (IC6ADDMT34ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
GPT4 pins (GTIOC4A (P95) and GTIOC4B (P92))	• POE4# input level detection • GTIOC4A and GTIOC4B output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 - 12-bit A/D converter comparator detection - POE0#, POE8#, POE10#, POE11#, POE12# input level detection	MTU6BDZE• ((POE4F) + (OSF2•OCE2) + (MTUCH67HIZ) + (ICSR6.OSTSTE) + (CMADDMT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT67ZE•POE0F) + (IC3ADDMT67ZE•POE8E•POE8F) + (IC4ADDMT67ZE•POE10E•POE10F) + (IC5ADDMT67ZE•POE11E•POE11F) + (IC6ADDMT67ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
GPT5 pins (GTIOC5A (P94) and GTIOC5B (P91))	• POE4# input level detection • GTIOC5A and GTIOC5B output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 - 12-bit A/D converter comparator detection - POE0#, POE8#, POE10#, POE11#, POE12# input level detection	MTU7ACZE• ((POE4F) + (OSF2•OCE2) + (MTUCH67HIZ) + (ICSR6.OSTSTE) + (CMADDMT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT67ZE•POE0F) + (IC3ADDMT67ZE•POE8E•POE8F) + (IC4ADDMT67ZE•POE10E•POE10F) + (IC5ADDMT67ZE•POE11E•POE11F) + (IC6ADDMT67ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002
GPT6 pins (GTIOC6A (P93) and GTIOC6B (P90))	• POE4# input level detection • GTIOC6A-A and GTIOC6B-A output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 - 12-bit A/D converter comparator detection - POE0#, POE8#, POE10#, POE11#, POE12# input level detection	MTU7BDZE• ((POE4F) + (OSF2•OCE2) + (MTUCH67HIZ) + (ICSR6.OSTSTE) + (CMADDMT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT67ZE•POE0F) + (IC3ADDMT67ZE•POE8E•POE8F) + (IC4ADDMT67ZE•POE10E•POE10F) + (IC5ADDMT67ZE•POE11E•POE11F) + (IC6ADDMT67ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)

Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions] (4/6)

Pins	Conditions	Detailed Conditions
MTU0A pins (MTIOC0A (P31 and PB3))	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE10#, POE11#, POE12# input level detection	MTU0AZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT0ZE•POE0F) + (IC2ADDMT0ZE•POE4F) + (IC4ADDMT0ZE•POE10E•POE10F) + (IC5ADDMT0ZE•POE11E•POE11F) + (IC6ADDMT0ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
MTU0B pins (MTIOC0B (P30 and PB2))	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE10#, POE11#, POE12# input level detection	MTU0BZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT0ZE•POE0F) + (IC2ADDMT0ZE•POE4F) + (IC4ADDMT0ZE•POE10E•POE10F) + (IC5ADDMT0ZE•POE11E•POE11F) + (IC6ADDMT0ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
MTU0C pin (MTIOC0C (PB1))	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE10#, POE11#, POE12# input level detection	MTU0CZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT0ZE•POE0F) + (IC2ADDMT0ZE•POE4F) + (IC4ADDMT0ZE•POE10E•POE10F) + (IC5ADDMT0ZE•POE11E•POE11F) + (IC6ADDMT0ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
MTU0D pin (MTIOC0D (PB0))	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE10#, POE11#, POE12# input level detection	MTU0DZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDMT0ZE•POE0F) + (IC2ADDMT0ZE•POE4F) + (IC4ADDMT0ZE•POE10E•POE10F) + (IC5ADDMT0ZE•POE11E•POE11F) + (IC6ADDMT0ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)

Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions] (5/6)

Pins	Conditions	Detailed Conditions
GPT0 pins (GTIOC0A (PD7) and GTIOC0B (PD6))	• POE10# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE8#, POE11#, POE12# input level detection	GPT0ABZE• ((POE10F•POE10E) + (GPT01HIZ) + (ICSR6.OSTSTE) + (CMADDGPT01ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDGPT01ZE•POE0F) + (IC2ADDGPT01ZE•POE4F) + (IC3ADDGPT01ZE•POE8E•POE8F) + (IC5ADDGPT01ZE•POE11E•POE11F) + (IC6ADDGPT01ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
GPT1pins (GTIOC1A (PD5) and GTIOC1B (PD4))	• POE10# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE8#, POE11#, POE12# # input level detection	GPT1ABZE• ((POE10F•POE10E) + (GPT01HIZ) + (ICSR6.OSTSTE) + (CMADDGPT01ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDGPT01ZE•POE0F) + (IC2ADDGPT01ZE•POE4F) + (IC3ADDGPT01ZE•POE8E•POE8F) + (IC5ADDGPT01ZE•POE11E•POE11F) + (IC6ADDGPT01ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
GPT2 pins (GTIOC2A (PD3) and GTIOC2B (PD2)	• POE11# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE8#, POE10#, POE12# input level detection	GPT2ABZE• ((POE11F•POE11E) + (GPT23HIZ) + (ICSR6.OSTSTE) + (CMADDGPT23ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDGPT23ZE•POE0F) + (IC2ADDGPT23ZE•POE4F) + (IC3ADDGPT23ZE•POE8E•POE8F) + (IC4ADDGPT23ZE•POE10E•POE10F) + (IC6ADDGPT23ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)
GPT3 pins (GTIOC3A (PD1) and GTIOC3B (PD0))	• POE11# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE4#, POE8#, POE10#, POE12# input level detection	GPT3ABZE• ((POE11F•POE11E) + (GPT23HIZ) + (ICSR6.OSTSTE) + (CMADDGPT23ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDGPT23ZE•POE0F) + (IC2ADDGPT23ZE•POE4F) + (IC3ADDGPT23ZE•POE8E•POE8F) + (IC4ADDGPT23ZE•POE10E•POE10F) + (IC6ADDGPT23ZE•POE12E•POE12F)) (n = 0,1, j = 000 to 002)

Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions] (6/6)

Pins	Conditions	Detailed Conditions
GPT6 pins (GTIOC6A (PG3) and GTIOC6B (PG4))	• POE12# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR8 - 12-bit A/D converter comparator detection - POE0#, POE4#, POE8#, POE10#, POE11# input level detection	GPT6ABZE• ((POE12F•POE12E) + (GPT67HIZ) + (ICSR6.OSTSTE) + (CMADDGPT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDGPT67ZE•POE0F) + (IC2ADDGPT67ZE•POE4F) + (IC3ADDGPT67ZE•POE8E•POE8F) + (IC4DDGPT67ZE•POE10E•POE10F) + (IC5DDGPT67ZE•POE11E•POE11F)) (n =0,1, j = 000 to 002)
GPT7 pins (GTIOC7A (PG0) and GTIOC7B (PG1))	• POE12# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR8 - 12-bit A/D converter comparator detection - POE0#, POE4#, POE8#, POE10#, POE11# input level detection	GPT7ABZE• ((POE12F•POE12E) + (GPT67HIZ) + (ICSR6.OSTSTE) + (CMADDGPT67ZE• S12ADn.ADCMPSEL.POERQj• S12ADn.ADCMPFR.CjFLAG) + (IC1ADDGPT67ZE•POE0F) + (IC2ADDGPT67ZE•POE4F) + (IC3ADDGPT67ZE•POE8E•POE8F) + (IC4DDGPT67ZE•POE10E•POE10F) + (IC5DDGPT67ZE•POE11E•POE11F)) (n = 0,1, j = 000 to 002)

Table 23.5 Target Pins and Conditions for High-Impedance Control [64- and 48-Pin Versions] (1/3)

Pins	Conditions	Detailed Conditions
MTU3B/MTU3D pins or MTU6B/MTU6D pins (MTIOC3B, MTIOC3D, MTIOC6B, and MTIOC6D)	• POE0# input level detection • MTIOC3B and MTIOC3D or MTIOC6B and MTIOC6D output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE8#, POE10#, POE11# input level detection	MTU3BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F)) (n = 000 to 002)
MTU4A/MTU4C pins or MTU7A/MTU7C pins (MTIOC4A, MTIOC4C, MTIOC7A, and MTIOC7C)	• POE0# input level detection • MTIOC4A and MTIOC4C or MTIOC7A and MTIOC7C output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE8#, POE10#, POE11# input level detection	MTU4ACZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F)) (n = 000 to 002)
MTU4B/MTU4D pins or MTU7B/MTU7D pins (MTIOC4B, MTIOC4D, MTIOC7B, and MTIOC7D)	• POE0# input level detection • MTIOC4B and MTIOC4D or MTIOC7B and MTIOC7D output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE8#, POE10#, POE11# input level detection	MTU4BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F)) (n = 000 to 002)
GPT0 pins (GTIOC0A (PD7), and GTIOC0B (PD6))	• POE0# input level detection • GTIOC0A and GTIOC0B output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE8#, POE10#, POE11# input level detection	MTU3BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F)) (n = 000 to 002)
GPT1 pins (GTIOC1A(PD5), and GTIOC1B(PD4))	• POE0# input level detection • GTIOC1A and GTIOC1B output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE8#, POE10#, POE11# input level detection	MTU4ACZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F)) (n = 000 to 002)

Table 23.5 Target Pins and Conditions for High-Impedance Control [64- and 48-Pin Versions] (2/3)

Pins	Conditions	Detailed Conditions
GPT2 pins (GTIOC2A(PD3), and GTIOC2B(PB6, PB7))	• POE0# input level detection • GTIOC2A and GTIOC2B output level comparison • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR4 – 12-bit A/D converter comparator detection – POE8#, POE10#, POE11# input level detection	MTU4BDZE• ((POE0F) + (OSF1•OCE1) + (MTUCH34HIZ) + (ICSR6.OSTSTE) + (CMADDMT34ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC3ADDMT34ZE•POE8E•POE8F) + (IC4ADDMT34ZE•POE10E•POE10F) + (IC5ADDMT34ZE•POE11E•POE11F)) (n = 000 to 002)
MTU0A pins (MTIOC0A (P31, PB3))	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE10#, POE11# input level detection	MTU0AZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDMT0ZE•POE0F) + (IC4ADDMT0ZE•POE10E•POE10F) + (IC5ADDMT0ZE•POE11E•POE11)) (n = 000 to 002)
MTU0B pins (MTIOC0B (P30, PB2))	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE10#, POE11# input level detection	MTU0BZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDMT0ZE•POE0F) + (IC4ADDMT0ZE•POE10E•POE10F) + (IC5ADDMT0ZE•POE11E•POE11F)) (n = 000 to 002)
MTU0C pins (MTIOC0C)	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE10#, POE11# input level detection	MTU0CZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDMT0ZE•POE0F) + (IC4ADDMT0ZE•POE10E•POE10F) + (IC5ADDMT0ZE•POE11E•POE11F)) (n = 000 to 002)
MTU0D pins (MTIOC0D)	• POE8# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR5 – 12-bit A/D converter comparator detection – POE0#, POE10#, POE11# input level detection	MTU0DZE• ((POE8F•POE8E) + (MTUCH0HIZ) + (ICSR6.OSTSTE) + (CMADDMT0ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDMT0ZE•POE0F) + (IC4ADDMT0ZE•POE10E•POE10F)) + (IC5ADDMT0ZE•POE11E•POE11F)) (n = 000 to 002)

Table 23.5 Target Pins and Conditions for High-Impedance Control [64- and 48-Pin Versions] (3/3)

Pins	Conditions	Detailed Conditions
GPT0 pins (GTIOC0A(PD7) and GTIOC0B(PD6))	• POE10# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE8#, POE11# input level detection	GPT0ABZE• ((POE10F•POE10E) + (GPT01HIZ) + (ICSR6.OSTSTE) + (CMADDGPT01ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDGPT01ZE•POE0F) + (IC3ADDGPT01ZE•POE8E•POE8F) + (IC5ADDGPT01ZE•POE11E•POE11F)) (n = 000 to 002)
GPT1pins (GTIOC1A(PD5) and GTIOC1B(PD4))	• POE10# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE8#, POE11# # input level detection	GPT1ABZE• ((POE10F•POE10E) + (GPT01HIZ) + (ICSR6.OSTSTE) + (CMADDGPT01ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDGPT01ZE•POE0F) + (IC3ADDGPT01ZE•POE8E•POE8F) + (IC5ADDGPT01ZE•POE11E•POE11F)) (n = 000 to 002)
GPT2 pins (GTIOC2A(PD3) and GTIOC2B(PB6, PB7))	• POE11# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE8#, POE10# input level detection	GPT2ABZE• ((POE11F•POE11E) + (GPT23HIZ) + (ICSR6.OSTSTE) + (CMADDGPT23ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDGPT23ZE•POE0F) + (IC3ADDGPT23ZE•POE8E•POE8F) + (IC4ADDGPT23ZE•POE10E•POE10F)) (n = 000 to 002)
GPT3 pins (GTIOC3A and GTIOC3B)	• POE11# input level detection • SPOER setting • Detection of stopped oscillation • Additional conditions of the POECR6 – 12-bit A/D converter comparator detection – POE0#, POE8#, POE10# input level detection	GPT3ABZE• ((POE11F•POE11E) + (GPT23HIZ) + (ICSR6.OSTSTE) + (CMADDGPT23ZE• S12AD.ADCMPSEL.POE• (S12AD.ADCMPFR.CnFLAG)) + (IC1ADDGPT23ZE•POE0F) + (IC3ADDGPT23ZE•POE8E•POE8F) + (IC4ADDGPT23ZE•POE10E•POE10F)) (n = 000 to 002)

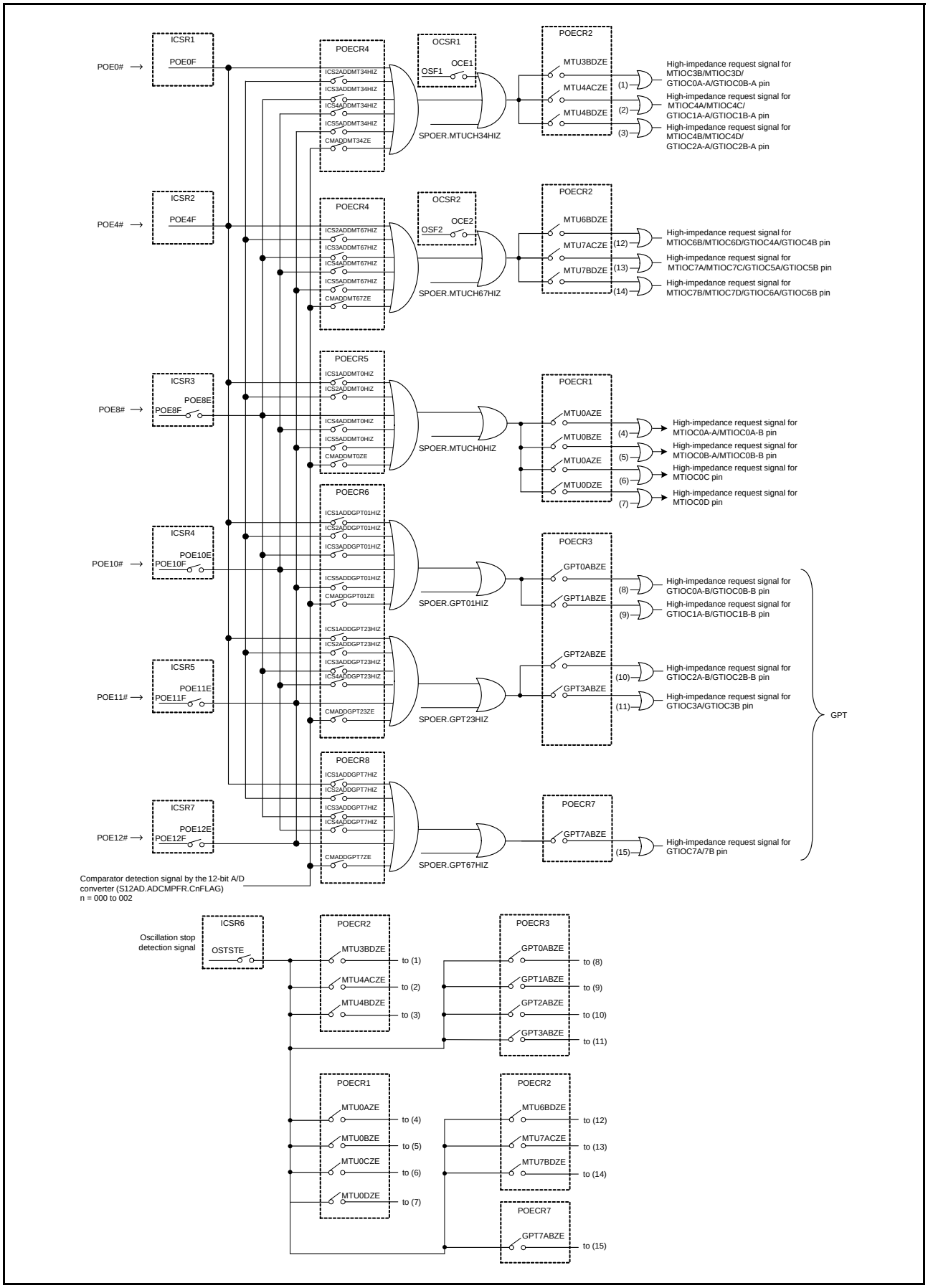


Figure 23.2 Target Pins and Conditions for High-Impedance Control

23.3.1 Input Level Detection Operation

If the input conditions set by ICSR1 to ICSR5 and ICSR7 occur on the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins, the MTU3 and MTU4 or MTU6 and MTU7 pins for the MTU complementary PWM output, and MTU0 pins, and GPT pins are placed in high-impedance state. Note however, that these pins are still placed in the high-impedance state even when the GPT and MTU functions are not selected for the pins.

(1) Falling Edge Detection

When a change from a high to low level is input to the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins, the pins for the MTU complementary PWM output, and MTU0 pins, and pin functions multiplexed with the GPT pins are placed in high-impedance state. Figure 23.3 shows a sample timing after the level changes in input to the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins until the respective pins enter high-impedance state.

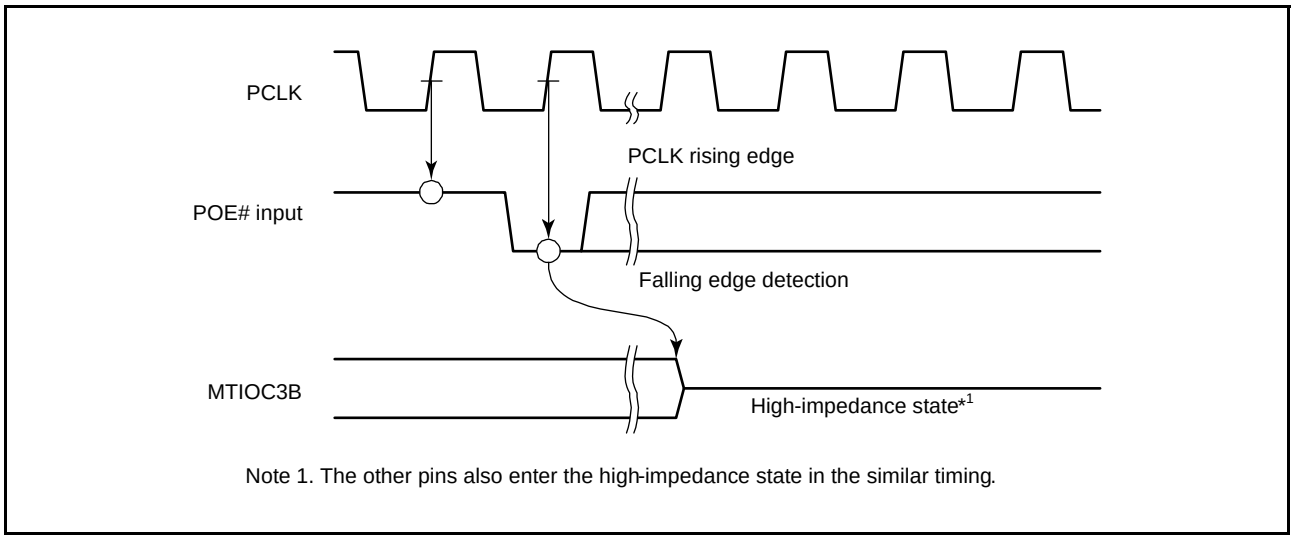


Figure 23.3 Falling Edge Detection

(2) Low Detection

Figure 23.4 shows the low detection operation. Sampling of sixteen continuous low with the sampling clock selected by ICSR1 to ICSR5 and ICSR7 is regarded as a low detection that drives the MTU2 complementary PWM output pin and MTU0 pin to be high-impedance state. If even one high is detected during this interval, the low is not accepted.
The timing when pins for the MTU complementary PWM output, and MTU0 pins and GPT pins enter the high-impedance state after the sampling clock is input is the same in both falling-edge detection and in low detection.

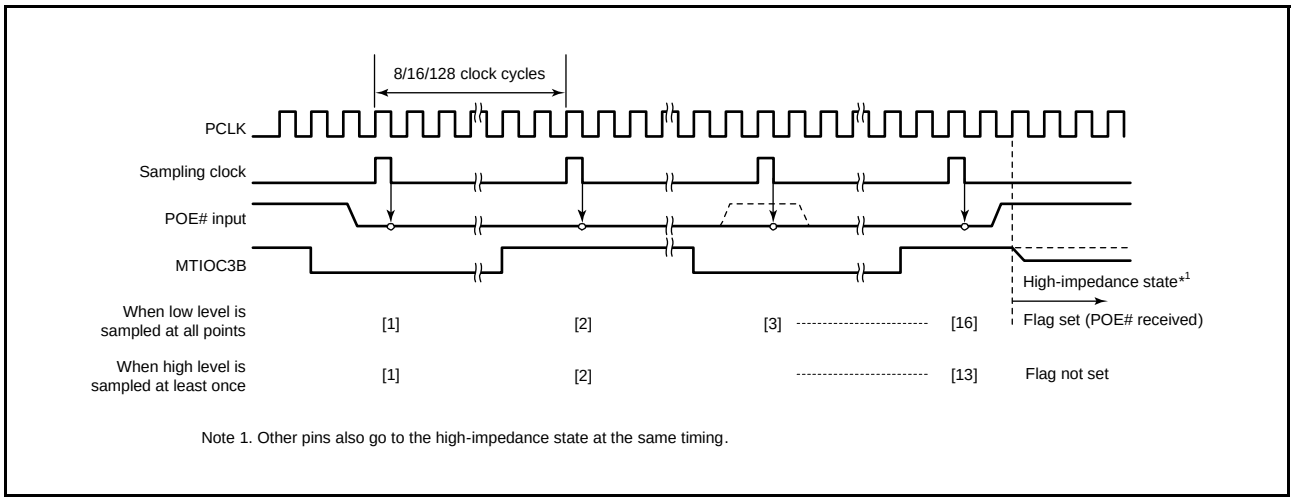


Figure 23.4 Low Detection Operation

23.3.2 Output-Level Compare Operation

Figure 23.5 shows an example of the output-level compare operation for the combination of MTIOC3B and MTIOC3D. The operation is the same for the other pin combinations.

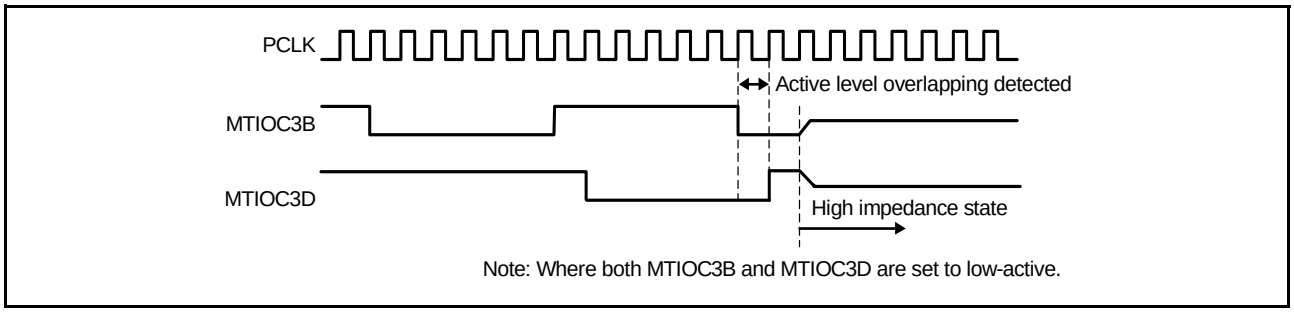


Figure 23.5 Output-Level Compare Operation

23.3.3 High-Impedance Control Using Registers

The pins to which MTU complementary PWM output, MTU0 output, GPT output are assigned to can be driven to high-impedance state by writing to SPOER.
For instance, setting the SPOER.CH34HIZ bit to 1 places the MTU complementary PWM output pin specified by POECR2 to high-impedance state.
The other pins can also be placed to high-impedance state by setting the appropriate bits in SPOER.

23.3.4 High-Impedance Control through Detection of Stopped Oscillation

When the oscillation stop detect function in the clock generation circuit detects an oscillation stop while ICSR6.OSTSTE is 1, the pins to which MTU complementary PWM output set by POECR2, MTU0 output set by POECR1, and GPT output set by POECR3 are assigned to driven to high-impedance state.

23.3.5 High-impedance Control through Detection of the Comparator

The pins to which the MTU complementary PWM output pins, the MTU0 pin, and the GPT pins are assigned to can be placed in the high-impedance state in response to detection by the comparator within the 12-bit A/D converter.
For instance, adding the S12AD.ADCMPFR.CjFLAG (j is 000 to 002) flags to the control conditions for the high-impedance state of the MTU3 and MTU4 pins by setting the POECR4.CMADDMT34ZE bit to 1 leads to the MTU complementary PWM output pins set by POECR2 being placed in the high-impedance state on comparator detection.
The other pins can also be placed to high-impedance state by setting the appropriate bits in the POECR1 to POECR8.

23.3.6 Additional Functions for Controlling High-Impedance States

Settings in POECR4 to POECR6 and POECR8 can add further high-impedance control conditions for the MTU complementary PWM output, MTU0 output, and GPT output pins.
For instance, the settings listed below can be added as high-impedance control conditions for the MTU3 and MTU4 pins.

- Setting the CMADDMT34ZE bit in POECR4 to 1 adds comparator detection
- Setting the IC2ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE4#
- Setting the IC3ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE8#
- Setting the IC4ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE10#
- Setting the IC5ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE11#
- Setting the IC6ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE12#

The high-impedance state of other pins can also be controlled by setting the appropriate bits in the POECR4 to POECR6 and POECR8.

23.3.7 Release from High-Impedance State

MTU pins which have entered high-impedance state due to input-level detection can be released from the state either by returning them to their initial state with a reset, or by clearing all of the ICSR1.POE0F, ICSR3.POE8F, ICSR4.POE10F, and ICSR5.POE11F flags. However, note that when low sampling is selected with the ICSR1.POE0M[1:0], ICSR3.POE8M[1:0], ICSR4.POE10M[1:0], and ICSR5.POE11M[1:0] bits, just writing 0 to a flag is ignored (the flag is not cleared); flags can be cleared by writing 0 to it only after a high level is input to the POE0#, POE8#, POE10#, POE11#, POE12# pins and is detected.

MTU pins which have entered high-impedance state due to output-level detection can be released from the state either by returning them to their initial state with a reset, or by clearing the OCSR1.OSF1 flag. When the OCSR1.OSF1 flag and OCSR2.OSF2 flag are set to 0, the inactive level is output by setting the MTU, GPT and ALR1 registers.

MTU pins which have entered high-impedance state due to comparator detection can be released from the state either by returning them to their initial state with a reset, S12AD.ADCMPFR.CnFLAG (n = 000 to 002) flags, respectively. A comparator detection flag (S12AD.ADCMPFR.CnFLAG; n = 0 to 2, 4 to 6) becoming 0 indicates that the analog input signal that triggered comparator detection has returned to a normal voltage, so read this bit and confirm that its value is 0 before proceeding with AD conversion and so on. Take care on this point because the comparator detection flag (S12AD.ADCMPFR.CnFLAG) is not re-set to 1 if this bit is cleared without confirmation that the analog input signal has returned to a normal voltage and the analog input signal actually remains below the low-side threshold voltage or above the high-side threshold voltage.

23.4 Interrupts

The POE3 issues a request to generate an interrupt when the specified condition is satisfied during input level detection or output level comparison. Table 23.6 shows the interrupt sources and their conditions.

Table 23.6 Interrupt Sources and Conditions

Name	Interrupt Source	Interrupt Flag	Condition
OEI1	Output enable interrupt 1	POE0F and OSF1	PIE1•POE0F + OIE1•OSF1
OEI2	Output enable interrupt 2	POE4F and OSF2	PIE2F•POE4 + OIE2•OSF2
OEI3	Output enable interrupt 3	POE8F	PIE3•POE8F
OEI4	Output enable interrupt 4	POE10F and POE11F	PIE4•POE10F + PIE5•POE11F
OEI5	Output enable interrupt 5	POE4F and POE12F	PIE2F•POE4 + PIE7•POE12F

23.5 Usage Notes

When the POE3 is used, do not make a transition to software standby mode or deep software standby mode. In these modes, the POE3 stops and thus the high-impedance state of pins cannot be controlled.

24. General PWM Timer (GPT)

This MCU has a general PWM timer (GPT) consisting of an eight-channel 16-bit timer. The GPT operates at a maximum of 100 MHz.

24.1 Overview

Table 24.1 lists the specifications for the GPT, and Table 24.2 shows the functions of the GPT. Figure 24.1 shows a block diagram of the GPT.

Table 24.1 Specifications of GPT

Item	Description
Function	• 16 bits × 8 channels • Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter. • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers (hardware sources) • Internal trigger sources: output of the comparator detection, software, and compare match • The frequency-divided timer module clock (PCLKA) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the IWDT-dedicated clock signal (IWDTCLK) (to detect abnormal oscillation). • A PWM delay with an accuracy of up to 1/32 times the period of the peripheral module clock (PCLKA) can be generated to control the timing with which signals from the two PWM output pins from each of channels 0 to 3 rise and fall.

Table 24.2 Functions of GPT (GPT0 to GPT3) (1/2)

Item		GPT0	GPT1	GPT2	GPT3
Count clock		PCLKA PCLKA/2 PCLKA/4 PCLKA/8	PCLKA PCLKA/2 PCLKA/4 PCLKA/8	PCLKA PCLKA/2 PCLKA/4 PCLKA/8	PCLKA PCLKA/2 PCLKA/4 PCLKA/8
Output compare/input capture registers (GTCCR)		GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register		GTPR	GTPR	GTPR	GTPR
Cycle setting buffer registers		GTPBR GTPDBR	GTPBR GTPDBR	GTPBR GTPDBR	GTPBR GTPDBR
I/O pins		GTIOC0A GTIOC0B	GTIOC1A GTIOC1B	GTIOC2A GTIOC2B	GTIOC3A GTIOC3B
External trigger input pin		GTETRG0			
Counter clear sources		GTPR compare match, input capture, comparator detection, GTETRG pin input, GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B internal output (output compare)			
Compare match output	Low output	√	√	√	√
	High output	√	√	√	√
	Toggle output	√	√	√	√
Input capture function		√	√	√	√
Synchronized operation		√	√	√	√
Phase shift start		√	√	√	√
Automatic addition of dead time		√	√	√	√
PWM mode		√	√	√	√
Buffer operation		√	√	√	√
One-shot operation		√	√	√	√
DTC activation		All the interrupt sources			
A/D converter start trigger		Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB
Interrupt sources		Five sources • GTCCRA compare match/input capture (GTCIA0) • GTCCRB compare match/input capture (GTCIB0) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC0) • GTCCRE compare match/GTCCRF compare match (GTCIE0) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV0)	Five sources • GTCCRA compare match/input capture (GTCIA1) • GTCCRB compare match/input capture (GTCIB1) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC1) • GTCCRE compare match/GTCCRF compare match (GTCIE1) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV1)	Five sources • GTCCRA compare match/input capture (GTCIA2) • GTCCRB compare match/input capture (GTCIB2) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC2) • GTCCRE compare match/GTCCRF compare match (GTCIE2) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV2)	Five sources • GTCCRA compare match/input capture (GTCIA3) • GTCCRB compare match/input capture (GTCIB3) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC3) • GTCCRE compare match/GTCCRF compare match (GTCIE3) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV3)
Common interrupt source		External trigger/IWDTCLK count function interrupt (LOCOI)			

Table 24.2 Functions of GPT (GPT0 to GPT3) (2/2)

Item	GPT0	GPT1	GPT2	GPT3
Interrupt skipping function	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV0) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV1) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV2) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV3) interrupts (with interlocking function for other interrupts or A/D conversion requests).

√: Possible
—: Not possible

Table 24.3 Functions of GPT (GPT4 to GPT7) (1/2)

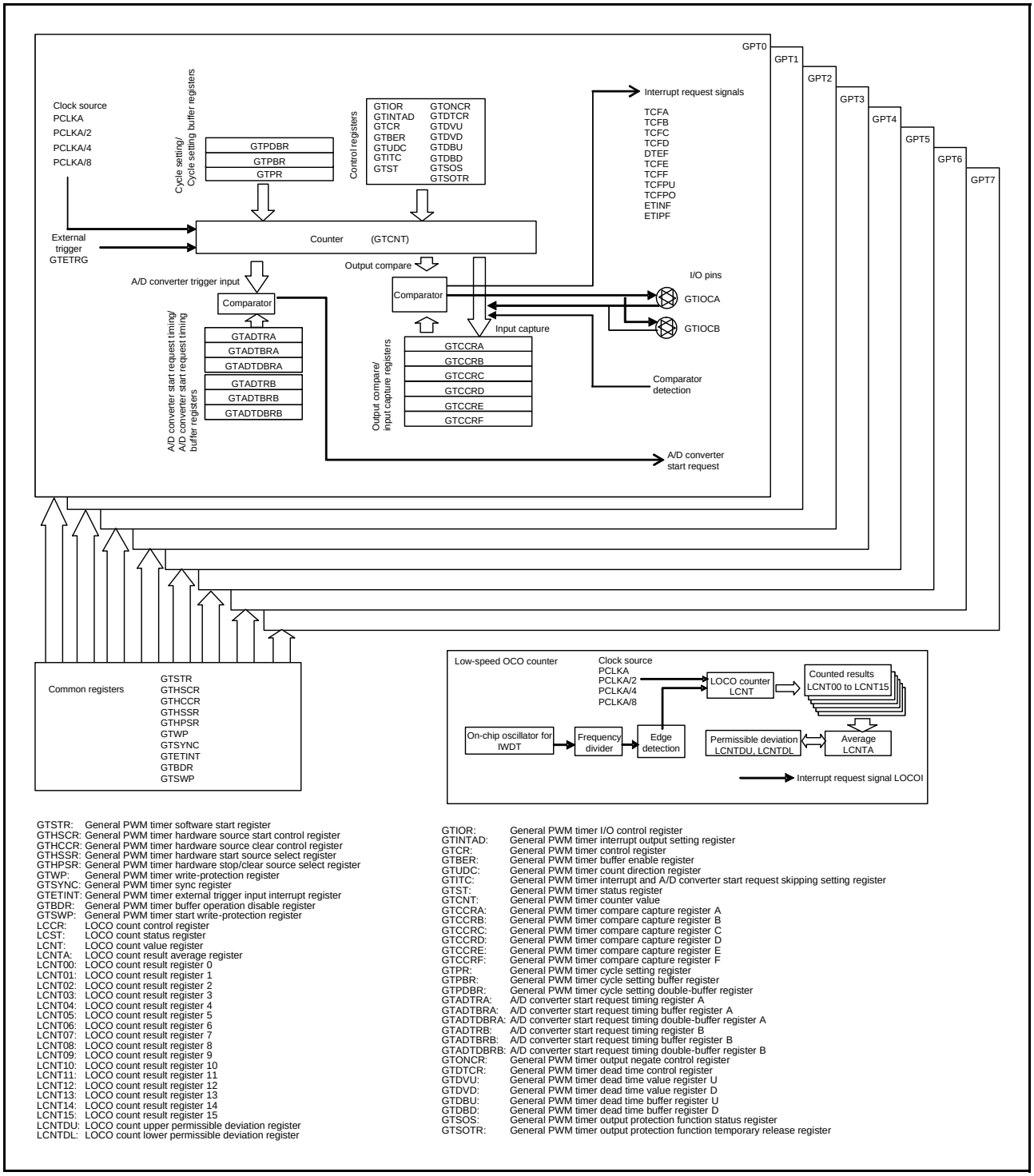
Item		GPT4	GPT5	GPT6	GPT7
Count clock		PCLKA PCLKA/2 PCLKA/4 PCLKA/8	PCLKA PCLKA/2 PCLKA/4 PCLKA/8	PCLKA PCLKA/2 PCLKA/4 PCLKA/8	PCLKA PCLKA/2 PCLKA/4 PCLKA/8
Output compare/input capture registers (GTCCR)		GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register		GTPR	GTPR	GTPR	GTPR
Cycle setting buffer registers		GTPBR GTPDBR	GTPBR GTPDBR	GTPBR GTPDBR	GTPBR GTPDBR
I/O pins		GTIOC4A GTIOC4B	GTIOC5A GTIOC5B	GTIOC6A GTIOC6B	GTIOC7A GTIOC7B
External trigger input pin		GTETRG1			
Counter clear sources		GTPR compare match, input capture, comparator detection, GTETRG pin input, GTIOC7A/B pin input, and GTIOC7A/B internal output (output compare)			
Compare match output	Low output	√	√	√	√
	High output	√	√	√	√
	Toggle output	√	√	√	√
Input capture function		√	√	√	√
Synchronized operation		√	√	√	√
Phase shift start		√	√	√	√
Automatic addition of dead time		√	√	√	√
PWM mode		√	√	√	√
Buffer operation		√	√	√	√
One-shot operation		√	√	√	√
DTC activation		All the interrupt sources			
A/D converter start trigger		Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB

Table 24.3 Functions of GPT (GPT4 to GPT7) (2/2)

Item	GPT4	GPT5	GPT6	GPT7
Interrupt sources	Five sources • GTCCRA compare match/input capture (GTCIA4) • GTCCRB compare match/input capture (GTCIB4) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC4) • GTCCRE compare match/GTCCRF compare match (GTCIE4) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV4)	Five sources • GTCCRA compare match/input capture (GTCIA5) • GTCCRB compare match/input capture (GTCIB5) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC5) • GTCCRE compare match/GTCCRF compare match (GTCIE5) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV5)	Five sources • GTCCRA compare match/input capture (GTCIA6) • GTCCRB compare match/input capture (GTCIB6) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC6) • GTCCRE compare match/GTCCRF compare match (GTCIE6) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV6)	Five sources • GTCCRA compare match/input capture (GTCIA7) • GTCCRB compare match/input capture (GTCIB7) • GTCCRC compare match/GTCCRD compare match/dead time error (GTCIC7) • GTCCRE compare match/GTCCRF compare match (GTCIE7) • GTCNT overflow (GTPR compare match)/GTCNT undervlow (GTCIV7)
Common interrupt source	External trigger/IWDTCLK count function interrupt (LOCOI)			
Interrupt skipping function	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV4) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV5) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV6) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)/ GTCNT underflow (GTCIV7) interrupts (with interlocking function for other interrupts or A/D conversion requests).

√: Possible

—: Not possible



GTSTR: General PWM timer software start register
GTHSCR: General PWM timer hardware source start control register
GTHCCR: General PWM timer hardware source clear control register
GTHSSR: General PWM timer hardware start source select register
GTHPSR: General PWM timer hardware stop/clear source select register
GTWP: General PWM timer write-protection register
GTSYNC: General PWM timer sync register
GTETINT: General PWM timer external trigger input interrupt register
GTBDR: General PWM timer buffer operation disable register
GTSWP: General PWM timer start write-protection register
LCCR: LOCO count control register
LCST: LOCO count status register
LCNT: LOCO count value register
LCNTA: LOCO count result average register
LCNT00: LOCO count result register 0
LCNT01: LOCO count result register 1
LCNT02: LOCO count result register 2
LCNT03: LOCO count result register 3
LCNT04: LOCO count result register 4
LCNT05: LOCO count result register 5
LCNT06: LOCO count result register 6
LCNT07: LOCO count result register 7
LCNT08: LOCO count result register 8
LCNT09: LOCO count result register 9
LCNT10: LOCO count result register 10
LCNT11: LOCO count result register 11
LCNT12: LOCO count result register 12
LCNT13: LOCO count result register 13
LCNT14: LOCO count result register 14
LCNT15: LOCO count result register 15
LCNTDU: LOCO count upper permissible deviation register
LCNTDL: LOCO count lower permissible deviation register

GTIOR: General PWM timer I/O control register
GTINTAD: General PWM timer interrupt output setting register
GTCR: General PWM timer control register
GTBER: General PWM timer buffer enable register
GTUDC: General PWM timer count direction register
GTITC: General PWM timer interrupt and A/D converter start request skipping setting register
GTST: General PWM timer status register
GTCNT: General PWM timer counter value
GTCCRA: General PWM timer compare capture register A
GTCCRB: General PWM timer compare capture register B
GTCCRC: General PWM timer compare capture register C
GTCCRD: General PWM timer compare capture register D
GTCCRE: General PWM timer compare capture register E
GTCCRF: General PWM timer compare capture register F
GTPR: General PWM timer cycle setting register
GTPBR: General PWM timer cycle setting buffer register
GTPDBR: General PWM timer cycle setting double-buffer register
GTADTRA: A/D converter start request timing register A
GTADTBRA: A/D converter start request timing buffer register A
GTADTDBRA: A/D converter start request timing double-buffer register A
GTADTRB: A/D converter start request timing register B
GTADTBRB: A/D converter start request timing buffer register B
GTADTDBRB: A/D converter start request timing double-buffer register B
GTONCR: General PWM timer output negate control register
GTDTCR: General PWM timer dead time control register
GTDVU: General PWM timer dead time value register U
GTDVD: General PWM timer dead time value register D
GTDBU: General PWM timer dead time buffer register U
GTDBD: General PWM timer dead time buffer register D
GTSOS: General PWM timer output protection function status register
GTSOTR: General PWM timer output protection function temporary release register

Figure 24.1 Block Diagram of GPT

Table 24.4 lists the I/O pins used in the GPT.

Table 24.4 I/O Pins of GPT

Channel	Pin Name	I/O	Function
GPT	GTETRG0	Input	External trigger input pin
GPT0	GTIOC0A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC0B	I/O	GTCCRB input capture input/output compare output/PWM output pin
GPT1	GTIOC1A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC1B	I/O	GTCCRB input capture input/output compare output/PWM output pin
GPT2	GTIOC2A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC2B	I/O	GTCCRB input capture input/output compare output/PWM output pin
GPT3	GTIOC3A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC3B	I/O	GTCCRB input capture input/output compare output/PWM output pin
GPT	GTETRG1	Input	External trigger input pin
GPT4	GTIOC4A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC4B	I/O	GTCCRB input capture input/output compare output/PWM output pin
GPT5	GTIOC5A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC5B	I/O	GTCCRB input capture input/output compare output/PWM output pin
GPT6	GTIOC6A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC6B	I/O	GTCCRB input capture input/output compare output/PWM output pin
GPT7	GTIOC7A	I/O	GTCCRA input capture input/output compare output/PWM output pin
	GTIOC7B	I/O	GTCCRB input capture input/output compare output/PWM output pin

24.2 Register Descriptions

24.2.1 General PWM Timer Software Start Register (GTSTR)

Address(es): GPT.GTSTR 000C 2000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CST3	CST2	CST1	CST0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST0	GPT0.GTCNT Count Start	0: Count operation is stopped 1: Count operation is performed	R/W
b1	CST1	GPT1.GTCNT Count Start		R/W
b2	CST2	GPT2.GTCNT Count Start		R/W
b3	CST3	GPT3.GTCNT Count Start		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTSTR starts or stops the GPTn.GTCNT counting operation (n = 0 to 3).

CSTn Bit (GPTn.GTCNT Count Start) (n = 0 to 3)

This bit starts or stops GPTn.GTCNT operation.

If the SWPn bit in the general PWM timer start write-protection register (GTSWP) is set to disable writing to the CSTn bit, writing to the CSTn bit is ignored.

The counter operation can also be started or stopped by GTHSCR. When count operation is started by a hardware source, this bit is automatically set to 1, and when count operation is stopped by a hardware source, this bit is automatically cleared to 0.

Address(es): GPTB.GTSTR 000C 2800h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CST7	CST6	CST5	CST4
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST4	GPT4.GTCNT Count Start	0: Count operation is stopped 1: Count operation is performed	R/W
b1	CST5	GPT5.GTCNT Count Start		R/W
b2	CST6	GPT6.GTCNT Count Start		R/W
b3	CST7	GPT7.GTCNT Count Start		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTSTR starts or stops the GPTn.GTCNT counting operation (n = 4 to 7).

CSTn Bit (GPTn.GTCNT Count Start) (n = 4 to 7)

This bit starts or stops GPTn.GTCNT operation.

If the SWPn bit in the general PWM timer start write-protection register (GTSWP) is set to disable writing to the CSTn bit, writing to the CSTn bit is ignored.

The counter operation can also be started or stopped by GTHSCR. When count operation is started by a hardware source, this bit is automatically set to 1, and when count operation is stopped by a hardware source, this bit is automatically cleared to 0.

24.2.2 General PWM Timer Hardware Source Start Control Register (GTHSCR)

Address(es): GPT.GTHSCR 000C 2004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CPHW3[1:0]		CPHW2[1:0]		CPHW1[1:0]		CPHW0[1:0]		CSHW3[1:0]		CSHW2[1:0]		CSHW1[1:0]		CSHW0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CSHW0[1:0]	GPT0.GTCNT Hardware Source Count Start	0 0: Count operation is not started by a hardware source. 0 1: Count operation is started at the rising edge of a hardware source. 1 0: Count operation is started at the falling edge of a hardware source. 1 1: Count operation is started at both rising and falling edges of a hardware source.	R/W
b3, b2	CSHW1[1:0]	GPT1.GTCNT Hardware Source Count Start		R/W
b5, b4	CSHW2[1:0]	GPT2.GTCNT Hardware Source Count Start		R/W
b7, b6	CSHW3[1:0]	GPT3.GTCNT Hardware Source Count Start		R/W
b9, b8	CPHW0[1:0]	GPT0.GTCNT Hardware Source Count Stop	0 0: Count operation is not stopped by a hardware source. 0 1: Count operation is stopped at the rising edge of a hardware source. 1 0: Count operation is stopped at the falling edge of a hardware source. 1 1: Count operation is stopped at both rising and falling edges of a hardware source.	R/W
b11, b10	CPHW1[1:0]	GPT1.GTCNT Hardware Source Count Stop		R/W
b13, b12	CPHW2[1:0]	GPT2.GTCNT Hardware Source Count Stop		R/W
b15, b14	CPHW3[1:0]	GPT3.GTCNT Hardware Source Count Stop		R/W

GTHSCR starts or stops the GPTn.GTCNT counting operation by a hardware source (n = 0 to 3).
When starting and stopping of GPTn.GTCNT by a hardware source occur simultaneously, counter start is given priority.

CSHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Start) (n = 0 to 3)

GPTn.GTCNT counting is started by a hardware source.
When the count operation is started by a hardware source, the corresponding bit in GTSTR automatically becomes 1.
The hardware source can be selected by GTHSSR.

CPHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Stop) (n = 0 to 3)

GPTn.GTCNT counting is stopped by a hardware source.
When the count operation is stopped by a hardware source, the corresponding bit in GTSTR automatically becomes 0.
The hardware source can be selected by GTHPSR.

Address(es): GPTB.GTHSCR 000C 2804h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CPHW7[1:0]		CPHW6[1:0]		CPHW5[1:0]		CPHW4[1:0]		CSHW7[1:0]		CSHW6[1:0]		CSHW5[1:0]		CSHW4[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CSHW4[1:0]	GPT4.GTCNT Hardware Source Count Start	0 0: Count operation is not started by a hardware source. 0 1: Count operation is started at the rising edge of a hardware source. 1 0: Count operation is started at the falling edge of a hardware source. 1 1: Count operation is started at both rising and falling edges of a hardware source.	R/W
b3, b2	CSHW5[1:0]	GPT5.GTCNT Hardware Source Count Start		R/W
b5, b4	CSHW6[1:0]	GPT6.GTCNT Hardware Source Count Start		R/W
b7, b6	CSHW7[1:0]	GPT7.GTCNT Hardware Source Count Start		R/W
b9, b8	CPHW4[1:0]	GPT4.GTCNT Hardware Source Count Stop	0 0: Count operation is not stopped by a hardware source. 0 1: Count operation is stopped at the rising edge of a hardware source. 1 0: Count operation is stopped at the falling edge of a hardware source. 1 1: Count operation is stopped at both rising and falling edges of a hardware source.	R/W
b11, b10	CPHW5[1:0]	GPT5.GTCNT Hardware Source Count Stop		R/W
b13, b12	CPHW6[1:0]	GPT6.GTCNT Hardware Source Count Stop		R/W
b15, b14	CPHW7[1:0]	GPT7.GTCNT Hardware Source Count Stop		R/W

GTHSCR starts or stops the GPTn.GTCNT counting operation by a hardware source (n = 4 to 7).
When starting and stopping of GPTn.GTCNT by a hardware source occur simultaneously, counter start is given priority.

CSHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Start) (n = 4 to 7)

GPTn.GTCNT counting is started by a hardware source.
When the count operation is started by a hardware source, the corresponding bit in GTSTR automatically becomes 1.
The hardware source can be selected by GTHSSR.

CPHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Stop) (n = 4 to 7)

GPTn.GTCNT counting is stopped by a hardware source.
When the count operation is stopped by a hardware source, the corresponding bit in GTSTR automatically becomes 0.
The hardware source can be selected by GTHPSR.

24.2.3 General PWM Timer Hardware Source Clear Control Register (GTHCCR)

Address(es): GPT.GTHCCR 000C 2006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CCSW3	CCSW2	CCSW1	CCSW0	CCHW3[1:0]		CCHW2[1:0]		CCHW1[1:0]		CCHW0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCHW0[1:0]	GPT0.GTCNT Hardware Source Counter Clear	0 0: Counter is not cleared by a hardware source. 0 1: Counter is cleared at the rising edge of a hardware source. 1 0: Counter is cleared at the falling edge of a hardware source. 1 1: Counter is cleared at both rising and falling edges of a hardware source.	R/W
b3, b2	CCHW1[1:0]	GPT1.GTCNT Hardware Source Counter Clear		R/W
b5, b4	CCHW2[1:0]	GPT2.GTCNT Hardware Source Counter Clear		R/W
b7, b6	CCHW3[1:0]	GPT3.GTCNT Hardware Source Counter Clear		R/W
b8	CCSW0	GPT0.GTCNT Counter Clear	When 1 is written to this bit, the counter is cleared. This bit automatically returns to 0 after the writing of 1. These bits are read as 0.	R/W
b9	CCSW1	GPT1.GTCNT Counter Clear		R/W
b10	CCSW2	GPT2.GTCNT Counter Clear		R/W
b11	CCSW3	GPT3.GTCNT Counter Clear		R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTHCCR sets clearing of GPTn.GTCNT by a hardware source (n = 0 to 3).
Once the clearing of GPTn.GTCNT counter by a hardware source is set, counter clearing by the hardware source is executed whether the GPTn.GTCNT count operation is performed (GTSTR.CSTn = 1; n = 0 to 3) or stopped (GTSTR.CSTn = 0, n = 0 to 3).

CCHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Clear) (n = 0 to 3)

GPTn.GTCNT is cleared by a hardware source.
The hardware source can be selected by GTHPSR.
When CCHWn[1:0] is 01b, 10b, or 11b, the hardware source can be accepted repeatedly.

CCSWn Bit (GPTn.GTCNT Counter Clear) (n = 0 to 3)

When 1 is written to this bit, the GPTn.GTCNT counter is cleared. This bit automatically returns to 0 after the writing of 1. This bit is always read as 0.

Address(es): GPTB.GTHCCR 000C 2806h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CCSW7	CCSW6	CCSW5	CCSW4	CCHW7[1:0]		CCHW6[1:0]		CCHW5[1:0]		CCHW4[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCHW4[1:0]	GPT4.GTCNT Hardware Source Counter Clear	0 0: Counter is not cleared by a hardware source. 0 1: Counter is cleared at the rising edge of a hardware source. 1 0: Counter is cleared at the falling edge of a hardware source. 1 1: Counter is cleared at both rising and falling edges of a hardware source.	R/W
b3, b2	CCHW5[1:0]	GPT5.GTCNT Hardware Source Counter Clear		R/W
b5, b4	CCHW6[1:0]	GPT6.GTCNT Hardware Source Counter Clear		R/W
b7, b6	CCHW7[1:0]	GPT7.GTCNT Hardware Source Counter Clear		R/W
b8	CCSW4	GPT4.GTCNT Counter Clear	When 1 is written to this bit, the counter is cleared. This bit automatically returns to 0 after the writing of 1. These bits are read as 0.	R/W
b9	CCSW5	GPT5.GTCNT Counter Clear		R/W
b10	CCSW6	GPT6.GTCNT Counter Clear		R/W
b11	CCSW7	GPT7.GTCNT Counter Clear		R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTHCCR sets clearing of GPTn.GTCNT by a hardware source (n = 4 to 7).
Once the clearing of GPTn.GTCNT counter by a hardware source is set, counter clearing by the hardware source is executed whether the GPTn.GTCNT count operation is performed (GTSTR.CSTn = 1; n = 4 to 7) or stopped (GTSTR.CSTn = 0, n = 4 to 7).

CCHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Clear) (n = 4 to 7)

GPTn.GTCNT is cleared by a hardware source.
The hardware source can be selected by GTHPSR.
When CCHWn[1:0] is 01b, 10b, or 11b, the hardware source can be accepted repeatedly.

CCSWn Bit (GPTn.GTCNT Counter Clear) (n = 4 to 7)

When 1 is written to this bit, the GPTn.GTCNT counter is cleared. This bit automatically returns to 0 after the writing of 1. This bit is always read as 0.

24.2.4 General PWM Timer Hardware Start Source Select Register (GTHSSR)

Address(es): GPT.GTHSSR 000C 2008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHSL3[3:0]				CSHSL2[3:0]				CSHSL1[3:0]				CSHSL0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHSL0[3:0]	GPT0.GTCNT Hardware Counter Start Source Select	b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output*2 (output compare) 1 0 1 1: GTIOC3B internal output*2 (output compare) 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W
b7 to b4	CSHSL1[3:0]	GPT1.GTCNT Hardware Counter Start Source Select	b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output*2 (output compare) 1 0 1 1: GTIOC3B internal output*2 (output compare) 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W
b11 to b8	CSHSL2[3:0]	GPT2.GTCNT Hardware Counter Start Source Select	b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output*2 (output compare) 1 0 1 1: GTIOC3B internal output*2 (output compare) 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b15 to b12	CSHSL3[3:0]	GPT3.GTCNT Hardware Counter Start Source Select	b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W

Note 1. Do not make this setting in 64- and 48-pin products.
Note 2. Though the output pin is not available with the 48-pin products, such pin can be used as the source.

GTHSSR sets the hardware source to start GPTn.GTCNT (n = 0 to 3).
To change the source, clear the GTHSCR.CSHWn[1:0] bits to 0 before changing the source.

CSHSLn[3:0] Bits (GPTn.GTCNT Hardware Counter Start Source Select) (n = 0 to 3)

These bits select the hardware source to start GPTn.GTCNT.

Select 1000b as a hardware source with GPT3.GTIOR.GTIOA[5] = 0 and GPT3.GTONCR.OAE = 0. Select 1001b as a hardware source with GPT3.GTIOR.GTIOB[5] = 0 and GPT3.GTONCR.OBE = 0.

Address(es): GPTB.GTHSSR 000C 2008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHSL7[3:0]				CSHSL6[3:0]				CSHSL5[3:0]				CSHSL4[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHSL4[3:0]	GPT4.GTCNT Hardware Counter Start Source Select	b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 0 1 0: GTIOC7A internal output*1 (output compare) 1 0 1 1: GTIOC7B internal output*1 (output compare) 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W
b7 to b4	CSHSL5[3:0]	GPT5.GTCNT Hardware Counter Start Source Select	b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 0 1 0: GTIOC7A internal output*1 (output compare) 1 0 1 1: GTIOC7B internal output*1 (output compare) 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W
b11 to b8	CSHSL6[3:0]	GPT6.GTCNT Hardware Counter Start Source Select	b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 0 1 0: GTIOC7A internal output*1 (output compare) 1 0 1 1: GTIOC7B internal output*1 (output compare) 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b15 to b12	CSHSL7[3:0]	GPT7.GTCNT Hardware Counter Start Source Select	b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W

Note 1. Though the output pin is not available with the 100-pin product, such pin can be used as the source.

GTHSSR sets the hardware source to start GPTn.GTCNT (n = 4 to 7).
To change the source, clear the GTHSCR.CSHWn[1:0] bits to 0 before changing the source.

CSHSLn[3:0] Bits (GPTn.GTCNT Hardware Counter Start Source Select) (n = 4 to 7)

These bits select the hardware source to start GPTn.GTCNT.

Select 1000b as a hardware source with GPT7.GTIOR.GTIOA[5] = 0 and GPT7.GTONCR.OAE = 0. Select 1001b as a hardware source with GPT7.GTIOR.GTIOB[5] = 0 and GPT7.GTONCR.OBE = 0.

24.2.5 General PWM Timer Hardware Stop/Clear Source Select Register (GTHPSR)

Address(es): GPT.GTHPSR 000C 200Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHPL3[3:0]				CSHPL2[3:0]				CSHPL1[3:0]				CSHPL0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHPL0[3:0]	GPT0.GTCNT Hardware Counter Stop/ Clear Source Select	b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare)*2 1 0 1 1: GTIOC3B internal output (output compare)*2 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W
b7 to b4	CSHPL1[3:0]	GPT1.GTCNT Hardware Counter Stop/ Clear Source Select	b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare)*2 1 0 1 1: GTIOC3B internal output (output compare)*2 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W
b11 to b8	CSHPL2[3:0]	GPT2.GTCNT Hardware Counter Stop/ Clear Source Select	b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare)*2 1 0 1 1: GTIOC3B internal output (output compare)*2 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b15 to b12	CSHPL3[3:0]	GPT3.GTCNT Hardware Counter Stop/ Clear Source Select	b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*1 0 1 0 1: AN101 comparator detection*1 0 1 1 0: AN102 comparator detection*1 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG0 pin input Settings other than above are prohibited.	R/W

Note 1. Do not make this setting in 64- and 48-pin products.
Note 2. Though the output pin is not available with the 48-pin products, such pin can be used as the source.

GTHPSR sets the hardware source to stop or clear GPTn.GTCNT (n = 0 to 3).
To change the source, clear the GTHSCR.CPHWn[1:0] bits and GTHCCR.CCHWn[1:0] bits to 0 before changing the source.

CSHPLn[3:0] Bits (GPTn.GTCNT Hardware Counter Stop/Clear Source Select) (n = 0 to 3)

These bits select the hardware source to stop or clear GPTn.GTCNT.

Address(es): GPTB.GTHPSR 000C 280Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHPL7[3:0]				CSHPL6[3:0]				CSHPL5[3:0]				CSHPL4[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHPL4[3:0]	GPT4.GTCNT Hardware Counter Stop/ Clear Source Select	b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 0 1 0: GTIOC7A internal output*1 (output compare) 1 0 1 1: GTIOC7B internal output*1 (output compare) 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W
b7 to b4	CSHPL5[3:0]	GPT5.GTCNT Hardware Counter Stop/ Clear Source Select	b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 0 1 0: GTIOC7A internal output*1 (output compare) 1 0 1 1: GTIOC7B internal output*1 (output compare) 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W
b11 to b8	CSHPL6[3:0]	GPT6.GTCNT Hardware Counter Stop/ Clear Source Select	b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 0 1 0: GTIOC7A internal output*1 (output compare) 1 0 1 1: GTIOC7B internal output*1 (output compare) 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b15 to b12	CSHPL7[3:0]	GPT7.GTCNT Hardware Counter Stop/ Clear Source Select	b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC7A pin input 1 0 0 1: GTIOC7B pin input 1 1 0 0: GTETRG1 pin input Settings other than above are prohibited.	R/W

Note 1. Though the output pin is not available with the 100-pin product, such pin can be used as the source.

GTHPSR sets the hardware source to stop or clear GPTn.GTCNT (n = 4 to 7).
To change the source, clear the GTHSCR.CPHWn[1:0] bits and GTHCCR.CCHWn[1:0] bits to 0 before changing the source.

CSHPLn[3:0] Bits (GPTn.GTCNT Hardware Counter Stop/Clear Source Select) (n = 4 to 7)

These bits select the hardware source to stop or clear GPTn.GTCNT.

24.2.6 General PWM Timer Write-Protection Register (GTWP)

Address(es): GPT.GTWP 000C 200Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WP3	WP2	WP1	WP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WP0	GPT0 Register Write Disable	0: Write to the register is enabled 1: Write to the register is disabled	R/W
b1	WP1	GPT1 Register Write Disable		R/W
b2	WP2	GPT2 Register Write Disable		R/W
b3	WP3	GPT3 Register Write Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTWP enables or disables writing to registers to prevent accidental modification.

For registers that are write enabled or disabled depending on the setting of the GTWP register, refer to section 24.7.1, Write-Protection for Registers .

WPn Bit (GPTn Register Write Disable) (n = 0 to 3)

This bit enables or disables writing to GPTn registers.

Address(es): GPTB.GTWP 000C 280Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WP7	WP6	WP5	WP4
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WP4	GPT4 Register Write Disable	0: Write to the register is enabled 1: Write to the register is disabled	R/W
b1	WP5	GPT5 Register Write Disable		R/W
b2	WP6	GPT6 Register Write Disable		R/W
b3	WP7	GPT7 Register Write Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

WPn Bit (GPTn Register Write Disable) (n = 4 to 7)

This bit enables or disables writing to GPTn registers.

24.2.7 General PWM Timer Sync Register (GTSYNC)

Address(es): GPT.GTSYNC 000C 200Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SYNC3[1:0]		—	—	SYNC2[1:0]		—	—	SYNC1[1:0]		—	—	SYNC0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SYNC0[1:0]	GPT0.GTCNT Counter Synchronized-Clear Source Select	b1 b0 0 0: GPT0.GTCNT is cleared by a GPT0 clearing source (synchronized clear is not performed). 0 1: GPT0.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT0.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT0.GTCNT is synchronously cleared by a GPT3 clearing source.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	SYNC1[1:0]	GPT1.GTCNT Counter Synchronized-Clear Source Select	b5 b4 0 0: GPT1.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT1.GTCNT is cleared by a GPT1 clearing source (synchronized clear is not performed). 1 0: GPT1.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT1.GTCNT is synchronously cleared by a GPT3 clearing source.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SYNC2[1:0]	GPT2.GTCNT Counter Synchronized-Clear Source Select	b9 b8 0 0: GPT2.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT2.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT2.GTCNT is cleared by a GPT2 clearing source (synchronized clear is not performed). 1 1: GPT2.GTCNT is synchronously cleared by a GPT3 clearing source.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	SYNC3[1:0]	GPT3.GTCNT Counter Synchronized-Clear Source Select	b13 b12 0 0: GPT3.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT3.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT3.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT3.GTCNT is cleared by a GPT3 clearing source (synchronized clear is not performed)	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTSYNC sets the clearing source of the GPTn.GTCNT counter for synchronized clearing/synchronized operation. This register can be modified when count operation of GPTn.GTCNT is stopped (n = 0 to 3).

SYNCn[1:0] Bits (GPTn.GTCNT Counter Synchronized-Clear Source Select) (n = 0 to 3)

These bits select which channel's counter clearing source is used to clear GPTn.GTCNT. When setting the SYNCn[1:0] bits, first set the GPTn.GTCR.CCLR[1:0] bits to 11b (cleared by counter clearing in another channel performing synchronized clearing/synchronized operation).

Address(es): GPTB.GTSYNC 000C 280Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SYNC7[1:0]		—	—	SYNC6[1:0]		—	—	SYNC5[1:0]		—	—	SYNC4[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SYNC4[1:0]	GPT4.GTCNT Counter Synchronized-Clear Source Select	b1 b0 0 0: GPT4.GTCNT is cleared by a GPT4 clearing source (synchronized clear is not performed). 0 1: GPT4.GTCNT is synchronously cleared by a GPT5 clearing source. 1 0: GPT4.GTCNT is synchronously cleared by a GPT6 clearing source. 1 1: GPT4.GTCNT is synchronously cleared by a GPT7 clearing source.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	SYNC5[1:0]	GPT5.GTCNT Counter Synchronized-Clear Source Select	b5 b4 0 0: GPT5.GTCNT is synchronously cleared by a GPT4 clearing source. 0 1: GPT5.GTCNT is cleared by a GPT5 clearing source (synchronized clear is not performed). 1 0: GPT5.GTCNT is synchronously cleared by a GPT6 clearing source. 1 1: GPT5.GTCNT is synchronously cleared by a GPT7clearing source.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SYNC6[1:0]	GPT6.GTCNT Counter Synchronized-Clear Source Select	b9 b8 0 0: GPT6.GTCNT is synchronously cleared by a GPT4 clearing source. 0 1: GPT6.GTCNT is synchronously cleared by a GPT5 clearing source. 1 0: GPT6.GTCNT is cleared by a GPT6 clearing source (synchronized clear is not performed). 1 1: GPT6.GTCNT is synchronously cleared by a GPT7 clearing source.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	SYNC7[1:0]	GPT7.GTCNT Counter Synchronized-Clear Source Select	b13 b12 0 0: GPT7.GTCNT is synchronously cleared by a GPT4 clearing source. 0 1: GPT7.GTCNT is synchronously cleared by a GPT5 clearing source. 1 0: GPT7.GTCNT is synchronously cleared by a GPT6 clearing source. 1 1: GPT7.GTCNT is cleared by a GPT7 clearing source (synchronized clear is not performed)	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTSYNC sets the clearing source of the GPTn.GTCNT counter for synchronized clearing/synchronized operation. This register can be modified when count operation of GPTn.GTCNT is stopped (n = 4 to 7).

SYNCn[1:0] Bits (GPTn.GTCNT Counter Synchronized-Clear Source Select) (n = 4 to 7)

These bits select which channel's counter clearing source is used to clear GPTn.GTCNT. When setting the SYNCn[1:0] bits, first set the GPTn.GTCR.CCLR[1:0] bits to 11b (cleared by counter clearing in another channel performing synchronized clearing/synchronized operation).

24.2.8 General PWM Timer External Trigger Input Interrupt Register (GTETINT)

Address(es): GPT.GTETINT 000C 2010h, GPTB.GTETINT 000C 2810h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ETINF	ETIPF	—	—	—	—	—	—	ETINEN	ETIPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ETIPEN	External Trigger Rising Input Interrupt Request Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b1	ETINEN	External Trigger Falling Input Interrupt Request Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ETIPF	External Trigger Rising Input Interrupt Request Flag	0: No interrupt request is generated 1: An interrupt request is generated	R/(W) *1
b9	ETINF	External Trigger Falling Input Interrupt Request Flag	0: No interrupt request is generated 1: An interrupt request is generated	R/(W) *1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag. When clearing the ETIPF or ETINF bits, be sure to clear only the target bit or bits for clearing and to write 1 to the other bits.

GPT.GTETINT enables or disables interrupts through the external trigger input pin (GTETRG0) and GPTB.GTETINT enables or disables interrupts through the external trigger input pin (GTETRG1). The interrupt request is generated as a LOCOI interrupt request.

ETIPEN Bit (External Trigger Rising Input Interrupt Request Enable)

This bit enables or disables an interrupt request generated at the rising edge of an external trigger input.

ETINEN Bit (External Trigger Falling Input Interrupt Request Enable)

This bit enables or disables an interrupt request generated at the falling edge of an external trigger input.

ETIPF Flag (External Trigger Rising Input Interrupt Request Flag)

This bit is a flag for an interrupt request generated at the rising edge of an external trigger input.

[Setting condition]

- An external trigger input rising edge has been detected.

[Clearing condition]

- 0 is written to this bit.

ETINF Flag (External Trigger Falling Input Interrupt Request Flag)

This bit is a flag for an interrupt request generated at the falling edge of an external trigger input.

[Setting condition]

- An external trigger input falling edge has been detected.

[Clearing condition]

- 0 is written to this bit.

24.2.9 General PWM Timer Buffer Operation Disable Register (GTBDR)

Address(es): GPT.GTBDR 000C 2014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BD3[3]	BD3[2]	BD3[1]	BD3[0]	BD2[3]	BD2[2]	BD2[1]	BD2[0]	BD1[3]	BD1[2]	BD1[1]	BD1[0]	BD0[3]	BD0[2]	BD0[1]	BD0[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BD0[0]	GPT0.GTCCR Buffer Operation Disable	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b1	BD0[1]	GPT0.GTPR Buffer Operation Disable		R/W
b2	BD0[2]	GPT0.GTADTR Buffer Operation Disable		R/W
b3	BD0[3]	GPT0.GTDV Buffer Operation Disable		R/W
b4	BD1[0]	GPT1.GTCCR Buffer Operation Disable		R/W
b5	BD1[1]	GPT1.GTPR Buffer Operation Disable		R/W
b6	BD1[2]	GPT1.GTADTR Buffer Operation Disable		R/W
b7	BD1[3]	GPT1.GTDV Buffer Operation Disable		R/W
b8	BD2[0]	GPT2.GTCCR Buffer Operation Disable		R/W
b9	BD2[1]	GPT2.GTPR Buffer Operation Disable		R/W
b10	BD2[2]	GPT2.GTADTR Buffer Operation Disable		R/W
b11	BD2[3]	GPT2.GTDV Buffer Operation Disable		R/W
b12	BD3[0]	GPT3.GTCCR Buffer Operation Disable		R/W
b13	BD3[1]	GPT3.GTPR Buffer Operation Disable		R/W
b14	BD3[2]	GPT3.GTADTR Buffer Operation Disable		R/W
b15	BD3[3]	GPT3.GTDV Buffer Operation Disable		R/W

GTBDR collectively enables or disables buffer operation of each channel. Even though a bit in GTBDR is set to 0 (buffer operation is enabled), buffer operation is not performed unless buffer operation is enabled by GTBER.

BDn[0] Bit (GPTn.GTCCR Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using GTCCRA, GTCCRC, and GTCCRD of GPTn together and buffer operation using GTCCRB, GTCCRE, and GTCCRF of GPTn together.

BDn[1] Bit (GPTn.GTPR Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using GTPR, GTPBR, and GTPDBR of GPTn together.

BDn[2] Bit (GPTn.GTADTR Counter Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using GTADTRA, GTADTBRA, and GTADTDBRA of GPTn together and buffer operation using GTADTRB, GTADTBRB, and GTADTDBRB of GPTn together.

BDn[3] Bit (GPTn.GTDV Counter Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using GTDVU and GTDBU of GPTn together and buffer operation using GTDVD and GTDBD of GPTn together.

Address(es): GPTB.GTBDR 000C 2814h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BD7[3]	BD7[2]	BD7[1]	BD7[0]	BD6[3]	BD6[2]	BD6[1]	BD6[0]	BD5[3]	BD5[2]	BD5[1]	BD5[0]	BD4[3]	BD4[2]	BD4[1]	BD4[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BD4[0]	GPT4.GTCCR Buffer Operation Disable	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b1	BD4[1]	GPT4.GTPR Buffer Operation Disable		R/W
b2	BD4[2]	GPT4.GTADTRR Buffer Operation Disable		R/W
b3	BD4[3]	GPT4.GTDV Buffer Operation Disable		R/W
b4	BD5[0]	GPT5.GTCCR Buffer Operation Disable		R/W
b5	BD5[1]	GPT5.GTPR Buffer Operation Disable		R/W
b6	BD5[2]	GPT5.GTADTR Buffer Operation Disable		R/W
b7	BD5[3]	GPT5.GTDV Buffer Operation Disable		R/W
b8	BD6[0]	GPT6.GTCCR Buffer Operation Disable		R/W
b9	BD6[1]	GPT6.GTPR Buffer Operation Disable		R/W
b10	BD6[2]	GPT6.GTADTR Buffer Operation Disable		R/W
b11	BD6[3]	GPT6.GTDV Buffer Operation Disable		R/W
b12	BD7[0]	GPT7.GTCCR Buffer Operation Disable		R/W
b13	BD7[1]	GPT7.GTPR Buffer Operation Disable		R/W
b14	BD7[2]	GPT7.GTADTR Buffer Operation Disable		R/W
b15	BD7[3]	GPT7.GTDV Buffer Operation Disable		R/W

GTBDR collectively enables or disables buffer operation of each channel. Even though a bit in GTBDR is set to 0 (buffer operation is enabled), buffer operation is not performed unless buffer operation is enabled by GTBER.

BDn[0] Bit (GPTn.GTCCR Buffer Operation Disable) (n = 4 to 7)

This bit disables buffer operation using GTCCRA, GTCCRC, and GTCCRD of GPTn together and buffer operation using GTCCRB, GTCCRE, and GTCCRF of GPTn together.

BDn[1] Bit (GPTn.GTPR Buffer Operation Disable) (n = 4 to 7)

This bit disables buffer operation using GTPR, GTPBR, and GTPDBR of GPTn together.

BDn[2] Bit (GPTn.GTADTR Buffer Operation Disable) (n = 4 to 7)

This bit disables buffer operation using GTADTRA, GTADTBRA, and GTADTDBRA of GPTn together and buffer operation using GTADTRB, GTADTBRB, and GTADTDBRB of GPTn together.

BDn[3] Bit (GPTn.GTDV Buffer Operation Disable) (n = 4 to 7)

This bit disables buffer operation using GTDVU and GTDBU of GPTn together and buffer operation using GTDVD and GTDBD of GPTn together.

24.2.10 General PWM Timer Start Write-Protection Register (GTSWP)

Address(es): GPT.GTSWP 000C 2018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SWP3	SWP2	SWP1	SWP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWP0	GTSTR.CST0 Bit Write Disable	0: Writing to the register bit is enabled 1: Writing to the register bit is disabled	R/W
b1	SWP1	GTSTR.CST1 Bit Write Disable		R/W
b2	SWP2	GTSTR.CST2 Bit Write Disable		R/W
b3	SWP3	GTSTR.CST3 Bit Write Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTSWP enables or disables writing to the GTSTR register to prevent accidental modification.

SWPn Bit (GTSTR.CSTn Bit Write Disable) (n = 0 to 3)

This bit enables or disables writing to the GTSTR.CSTn bit.

When this bit is set to disable writing, writing to the GTSTR.CSTn bit is ignored.

However, if the GTHSCR register is set to allow counter operation to be started or stopped by a hardware source, the status of counter operation (started or stopped by a hardware source) is written to the GTSTR.CSTn bit even if the SWPn bit is set to disable writing to GTSTR.CSTn bit.

Address(es): GPTB.GTSWP 000C 2818h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SWP7	SWP6	SWP5	SWP4
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWP4	GTSTR.CST4 Bit Write Disable	0: Writing to the register bit is enabled 1: Writing to the register bit is disabled	R/W
b1	SWP5	GTSTR.CST5 Bit Write Disable		R/W
b2	SWP6	GTSTR.CST6 Bit Write Disable		R/W
b3	SWP7	GTSTR.CST7 Bit Write Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTSWP enables or disables writing to the GTSTR register to prevent accidental modification.

SWPn Bit (GTSTR.CSTn Bit Write Disable) (n = 4 to 7)

This bit enables or disables writing to the GTSTR.CSTn bit.

When this bit is set to disable writing, writing to the GTSTR.CSTn bit is ignored.

However, if the GTHSCR register is set to allow counter operation to be started or stopped by a hardware source, the status of counter operation (started or stopped by a hardware source) is written to the GTSTR.CSTn bit even if the SWPn bit is set to disable writing to GTSTR.CSTn bit.

24.2.11 LOCO Count Control Register (LCCR)

Address(es): GPT.LCCR 000C 2080h, GPTB.LCCR 000C 2880h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LPSC[1:0]		TPSC[1:0]		LCNTAT	LCTO[2:0]			—	LCINTO	LCINTD	LCINTC	—	LCNTS	LCNTCR	LCNTE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LCNTE	Count Function Enable	0: Count function is stopped 1: Count function is operating	R/W
b1	LCNTCR	Count Value Clear	When 1 is written to this bit, the LCNT register is cleared. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.	R/W
b2	LCNTS	Count Value Setting	When 1 is written to this bit, the LCNT00 value is set to LCNT01 to LCNT15 registers. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	LCINTC	Frequency-Divided IWDTCLK Clock Rise Interrupt Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b5	LCINTD	Count Value Deviation Exceedance Interrupt Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b6	LCINTO	LCNT Overflow Interrupt Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10 to b8	LCTO[2:0]	Frequency-Divided IWDTCLK Clock Rise Interrupt Skipping Count Setting	b10 b8 0 0 0: Skipping is not performed 0 0 1: Setting prohibited 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Skipping count of 7 (counted once every 8 times) 1 0 1: Skipping count of 15 (counted once every 16 times) 1 1 0: Skipping count of 127 (counted once every 128 times) 1 1 1: Skipping count of 255 (counted once every 256 times)	R/W
b11	LCNTAT	Count Result Skipping Setting	0: Skipping is not performed 1: Skipping is performed	R/W
b13, b12	TPSC[1:0]	Count Clock Select	b13 b12 0 0: PCLKA (timer module clock) 0 1: PCLKA/2 (timer module clock/2) 1 0: PCLKA/4 (timer module clock/4) 1 1: PCLKA/8 (timer module clock/8)	R/W
b15, b14	LPSC[1:0]	Frequency-Divided Clock Select	b15 b14 0 0: 1 0 1: 1/16 1 0: 1/128 1 1: 1/256	R/W

LCCR sets the count function of the IWDT-dedicated on-chip oscillator. When using the count function, also operate the independent watchdog timer (IWDT).

LCNTE Bit (Count Function Enable)

This bit starts or stops operation of the count function.

LCNTCR Bit (Count Value Clear)

This bit clears the LCNT register.
When 1 is written to this bit, the count value is cleared. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.

LCNTS Bit (Count Value Setting)

This bit is used to set the LCNT00 register value to the LCNT01 to LCNT15 registers. When 1 is written to this bit, the LCNT00 value is set to LCNT01 to LCNT15. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.

LCINTC Bit (Frequency-Divided IWDTCLK Clock Rise Interrupt Enable)

This bit enables or disables an interrupt request generated by the rising edge of the frequency-divided IWDTCLK clock. The interrupt request is generated as a LOCOI interrupt request.

LCINTD Bit (Count Value Deviation Exceedance Interrupt Enable)

This bit enables or disables an interrupt request generated by the deviation exceedance of the count value. The interrupt request is generated as a LOCOI interrupt request.

LCINTO Bit (LCNT Overflow Interrupt Enable)

This bit enables or disables an interrupt request generated by an overflow of the LCNT counter. The interrupt request is generated as a LOCOI interrupt request.

LCTO[2:0] Bits (Frequency-Divided IWDTCLK Clock Rise Interrupt Skipping Count Setting)

These bits set the skipping count for the frequency-divided IWDTCLK clock rise interrupt.

LCNTAT Bit (Count Result Skipping Setting)

This bit specifies whether to skip the transfers of the count results to LCNTn (n = 00 to 15) as many times as the count specified with LCTO[2:0] bits.

TPSC[1:0] Bits (Count Clock Select)

These bits select the clock for counting frequency-divided IWDTCLK clock (LCNT operation clock).

LPSC[1:0] Bits (Frequency-Divided IWDTCLK Clock Select)

These bits select the frequency division ratio of the frequency-divided IWDTCLK clock.
The following relationship should be satisfied between the IWDTCLK clock division ratio selected by the LCCR.LPSC[1:0] bits and the IWDTCLK clock division ratio selected by the CKS[3:0] bits of the IWDTCR register in the independent watchdog timer (IWDT):

Clock division ratio selected by the LCCR.LPSC.LPSC[1:0] bits ≤ Clock division ratio selected by the CKS[3:0] bits

24.2.12 LOCO Count Status Register (LCST)

Address(es): GPT.LCST 000C 2082h, GPTB.LCST 000C 2882h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LISO	LISD	LISC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LISC	Frequency-Divided IWDTCLK Clock Rise Interrupt Request Flag	0: No interrupt request is generated. 1: An interrupt request is generated.	R/(W)*1
b1	LISD	IWDTCLK Count Value Deviation Exceedance Interrupt Request Flag	0: No interrupt request is generated. 1: An interrupt request is generated.	R/(W)*1
b2	LISO	LCNT Overflow Interrupt Request Flag	0: No interrupt request is generated. 1: An interrupt request is generated.	R/(W)*1
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag. When clearing the LISC, LISD, or LISO bits, be sure to clear only the target bit or bits for clearing and to write 1 to the other bits.

LCST indicates the count status of the frequency-divided IWDTCLK clock.

LISC Flag (Frequency-Divided IWDTCLK Clock Rise Interrupt Request Flag)

This bit is a flag for an interrupt request generated at the rising edge of the frequency-divided IWDTCLK clock. The next interrupt due to the frequency-divided IWDTCLK clock rising edge will not occur until this flag is cleared.
[Setting condition]
The frequency-divided IWDTCLK clock has a rising edge with LCINTC in LCCR set to 1.
[Clearing condition]
0 is written to this bit.

LISD Flag (IWDTCLK Count Value Deviation Exceedance Interrupt Request Flag)

This bit is a flag for an interrupt request generated by IWDTCLK count value deviation exceedance. The next interrupt due to the IWDTCLK count value deviation exceedance will not occur until this flag is cleared.
[Setting condition]
The IWDTCLK count value deviation exceedance has occurred with LCCR.LCINTD set to 1.
[Clearing condition]
0 is written to this bit.

LISO Flag (LCNT Overflow Interrupt Flag)

This bit is a flag for an interrupt request generated by the LCNT counter overflow. The next interrupt due to the LCNT counter overflow will not occur until this flag is cleared.
[Setting condition]
An overflow of the LCNT counter has occurred with LCCR.LCINTO set to 1.
[Clearing condition]
0 is written to this bit.

24.2.13 LOCO Count Value Register (LCNT)

Address(es): GPT.LCNT 000C 2084h, GPTB.LCNT 000C 2884h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The LCNT counter counts the frequency-divided IWDTCLK clock. The LCNT counter can only be read from.

24.2.14 LOCO Count Result Average Register (LCNTA)

Address(es): GPT.LCNTA 000C 2086h, GPTB.LCNTA 000C 2886h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LCNTA indicates the average of the frequency-divided IWDTCLK clock counting results (LCNT00 to LCNT15). LCNTA can only be read from.

24.2.15 LOCO Count Result Register n (LCNTn) (n = 00 to 15)

- LCNTn (n = 00 to 15)

Address(es): GPT.LCNT00 000C 2088h, GPT.LCNT01 000C 208Ah, GPT.LCNT02 000C 208Ch, GPT.LCNT03 000C 208Eh
GPT.LCNT04 000C 2090h, GPT.LCNT05 000C 2092h, GPT.LCNT06 000C 2094h, GPT.LCNT07 000C 2096h
GPT.LCNT08 000C 2098h, GPT.LCNT09 000C 209Ah, GPT.LCNT10 000C 209Ch, GPT.LCNT11 000C 209Eh
GPT.LCNT12 000C 20A0h, GPT.LCNT13 000C 20A2h, GPT.LCNT14 000C 20A4h, GPT.LCNT15 000C 20A6h
GPTB.LCNT00 000C 2888h, GPTB.LCNT01 000C 288Ah, GPTB.LCNT02 000C 288Ch, GPTB.LCNT03 000C 288Eh
GPTB.LCNT04 000C 2890h, GPTB.LCNT05 000C 2892h, GPTB.LCNT06 000C 2894h, GPTB.LCNT07 000C 2896h
GPTB.LCNT08 000C 2898h, GPTB.LCNT09 000C 289Ah, GPTB.LCNT10 000C 289Ch, GPTB.LCNT11 000C 289Eh
GPTB.LCNT12 000C 28A0h, GPTB.LCNT13 000C 28A2h, GPTB.LCNT14 000C 28A4h, GPTB.LCNT15 000C 28A6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LCNTn indicates the result of counting the frequency-divided IWDTCLK clock. This register can be modified only when counting is stopped (LCCR.LCNTE bit = 0).
The count value in LCNT00 is the latest result.

24.2.16 LOCO Count Upper/Lower Permissible Deviation Register (LCNTDU, LCNTDL)

Address(es): GPT.LCNTDU 000C 20A8h, GPTB.LCNTDU 000C 28A8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address(es): GPT.LCNTDL 000C 20AAh, GPTB.LCNTDL 000C 28AAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

LCNTDU and LCNTDL set the permissible deviation for the value obtained by counting the frequency-divided IWDTCLK clock cycles.
The IWDTCLK count value deviation exceedance interrupt is generated when the LCNT00 value exceeds the upper limit (LCNTA + LCNTDU) of the deviation or falls below the lower limit (LCNTA – LCNTDL) of the deviation.

24.2.17 General PWM Timer I/O Control Register (GTIOR)

Address(es): GPT0.GTIOR 000C 2100h, GPT1.GTIOR 000C 2180h, GPT2.GTIOR 000C 2200h, GPT3.GTIOR 000C 2280h, GPT4.GTIOR 000C 2900h, GPT5.GTIOR 000C 2980h, GPT6.GTIOR 000C 2A00h, GPT7.GTIOR 000C 2A80h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBHLD	OBDFLT	GTIOB[5: 0]						OAHLD	OADFLT	GTIOA[5: 0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	GTIOA[5: 0]	GTIOCnA Pin Function Select	See Table 24.5.	R/W
b6	OADFLT	Output Value at GTIOCnA Pin Count Stop	0: The GTIOCnA pin outputs low when counting is stopped. 1: The GTIOCnA pin outputs high when counting is stopped.	R/W
b7	OAHLD	Output Retain at GTIOCnA Pin Count Start/ Stop	0: The GTIOCnA pin output level at start/stop of counting depends on the register setting. 1: The GTIOCnA pin output level is retained at start/ stop of counting.	R/W
b13 to b8	GTIOB[5: 0]	GTIOCnB Pin Function Select	See Table 24.5.	R/W
b14	OBDFLT	Output Value at GTIOCnB Pin Count Stop	0: The GTIOCnB pin outputs low when counting is stopped. 1: The GTIOCnB pin outputs high when counting is stopped.	R/W
b15	OBHLD	Output Retain at GTIOCnB Pin Count Start/ Stop	0: The GTIOCnB pin output level at start/stop of counting depends on the register setting. 1: The GTIOCnB pin output level is retained at start/ stop of counting.	R/W

Note 1. (n = 0 to 7)

GPTn.GTIOR sets the functions of the GTIOCnA and GTIOCnB pins (n = 0 to 7). Each channel has one GTIOCnA pin and one GTIOCnB pin. Value written to GTIOR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

GTIOA[5:0] Bits (GTIOCnA Pin Function Select)

These bits select the GTIOCnA pin function. For details, see Table 24.5.

OADFLT Bit (Output Value at GTIOCnA Pin Count Stop)

This bit sets whether the GTIOCnA pin outputs high or low when counting is stopped.

OAHLD Bit (Output Retain at GTIOCnA Pin Count Start/Stop)

This bit specifies whether the GTIOCnA pin output level is retained or the level depends on the register setting when counting is started or stopped.

[When the OAHLD bit is set to 0]

- The value specified by bit 4 in GTIOR is output when counting starts.
- The value specified by the OADFLT bit is output when counting stops.
- If the OADFLT bit is modified while counting is stopped, it is immediately reflected in the output.

[When the OAHLD bit is set to 1]

- The output is retained when counting starts or stops.

GTIOB[5:0] Bits (GTIOCnB Pin Function Select)

These bits select the GTIOCnB pin function. For details, see Table 24.5.

OBDFLT Bit (Output Value at GTIOCnB Pin Count Stop)

This bit sets whether the GTIOCnB pin outputs high or low when counting is stopped.

OBHLD Bit (Output Retain at GTIOCnB Pin Count Start/Stop)

This bit specifies whether the GTIOCnB pin output level is retained or the level depends on the register setting when counting is started or stopped.

[When the OBHLD bit is set to 0]

- The value specified by bit 4 in GTIOR is output when counting starts.
- The value specified by the OBDFLT bit is output when counting stops.
- If the OBDFLT bit is modified while counting is stopped, it is immediately reflected in the output.

[When the OBHLD bit is set to 1]

- The output is retained when counting starts or stops.

Table 24.5 Settings of GTIOA[5:0] Bits (GTIOB[5:0] Bits) (1/2)

GTIOA/GTIOB[5:0] Bits						Function			
b5	b4	b3	b2	b1	b0	b5	b4	b3, b2	b1, b0
0	0	0	0	0	0	Compare match	Initial output is Low.	Output retained at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	0	0			Low output at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	0	0			High output at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	0	0			Toggle output at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match

Table 24.5 Settings of GTIOA[5:0] Bits (GTIOB[5:0] Bits) (2/2)

GTIOA/GTIOB[5:0] Bits						Function			
b5	**b4**	**b3**	**b2**	**b1**	**b0**	**b5**	**b4**	**b3, b2**	**b1, b0**
0	1	0	0	0	0	Compare match	Initial output is High.	Output retained at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	1	0	0			Low output at cycle end	Output retained at GTPn.GTCCRA/ GTCCRB compare match
0	1	0	1	0	1				Low output at GTPn.GTCCRA/ GTCCRB compare match
0	1	0	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	0	0	0			High output at cycle end	Output retained at GTPn.GTCCRA/ GTCCRB compare match
0	1	1	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	1	0	0			Toggle output at cycle end	Output retained at GTPn.GTCCRA/ GTCCRB compare match
0	1	1	1	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
1	x	x	x	0	0	Input capture	Don't care		Input capture at rising edge
1	x	x	x	0	1				Input capture at falling edge
1	x	x	x	1	0				Input capture at both edges
1	x	x	x	1	1				

x: Don't care

Note 1. The cycle end is an overflow (GTCNT = GTPR in up-count operation) or underflow (GTCNT = 0 in down-count operation) for saw waves, and the trough (GTCNT = 0) for triangle waves.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3-b2 setting is given priority in saw-wave PWM mode, and the b1-b0 setting is given priority in any other mode.

Note 3. Even though a compare match is set in GTIOR, output will not be made to the pins. GTONCR needs to be set separately.

24.2.18 General PWM Timer Interrupt Output Setting Register (GTINTAD)

Address(es): GPT0.GTINTAD 000C 2102h, GPT1.GTINTAD 000C 2182h, GPT2.GTINTAD 000C 2202h, GPT3.GTINTAD 000C 2282h, GPT4.GTINTAD 000C 2902h, GPT5.GTINTAD 000C 2982h, GPT6.GTINTAD 000C 2A02h, GPT7.GTINTAD 000C 2A82h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—	GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	GTINTA	GTCCRA Compare Match/Input Capture Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b1	GTINTB	GTCCRB Compare Match/Input Capture Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b2	GTINTC	GTCCRC Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b3	GTINTD	GTCCRD Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b4	GTINTE	GTCCRE Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b5	GTINTF	GTCCRF Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b7, b6	GTINTPR[1:0]	GTPR Compare Match Interrupt Enable	b7 b6 0 0: Interrupt request is disabled. 0 1: In saw-wave mode, interrupt requests are enabled at overflows. In triangle-wave mode, interrupt requests are enabled at crests. 1 0: In saw-wave mode, interrupt requests are enabled at underflows. In triangle-wave mode, interrupt requests are enabled at troughs. 1 1: In saw-wave mode, interrupt requests are enabled at both overflows and underflows. In triangle-wave mode, interrupt requests are enabled at both crests and troughs.	R/W
b10 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	EINT	Dead Time Error Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b12	ADTRAUEN	GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b13	ADTRADEN	GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b14	ADTRBUEN	GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b15	ADTRBDEN	GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W

GTINTAD enables or disables interrupt requests and A/D converter start requests. Value written to GTINTAD is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

GTINTA Bit (GTCCRA Compare Match/Input Capture Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRA compare match/input capture (GTCIA).

GTINTB Bit (GTCCRB Compare Match/Input Capture Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRB compare match/input capture (GTCIB).

GTINTC Bit (GTCCRC Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRC compare match (GTCIC).

GTINTD Bit (GTCCRD Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRD compare match (GTCID). The interrupt request is generated as a GTCIC interrupt.

GTINTE Bit (GTCCRE Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRE compare match (GTCIE).

GTINTF Bit (GTCCRF Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRF compare match (GTCIF). The interrupt request is generated as a GTCIE interrupt.

GTINTPR[1:0] Bits (GTPR Compare Match Interrupt Request Setting)

These bits enable or disable interrupt requests by a GTPR compare match (GTCNT counter overflow) and those by a GTCNT counter underflow (GTCIV).

EINT Bit (Dead Time Error Interrupt Enable)

This bit enables or disables interrupt requests by a dead time error (GTCIC). The interrupt request is generated as a GTCIC interrupt.

ADTRAUEN Bit (GTADTRA Compare Match (Up-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT up-count operation.

ADTRADEN Bit (GTADTRA Compare Match (Down-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT down-count operation.

ADTRBUEN Bit (GTADTRB Compare Match (Up-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT up-count operation.

ADTRBDEN Bit (GTADTRB Compare Match (Down-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT down-count operation.

24.2.19 General PWM Timer Control Register (GTCR)

Address(es): GPT0.GTCR 000C 2104h, GPT1.GTCR 000C 2184h, GPT2.GTCR 000C 2204h, GPT3.GTCR 000C 2284h, GPT4.GTCR 000C 2904h, GPT5.GTCR 000C 2984h, GPT6.GTCR 000C 2A04h, GPT7.GTCR 000C 2A84h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CCLR[1:0]		—	—	TPCS[1:0]		—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MD[2:0]	Mode Select	b2 b0 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at crest) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) fixed buffer operation) 1 1 1: Setting prohibited	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	TPCS[1:0]	Timer Prescaler Select	b9 b8 0 0: PCLKA (timer module clock) 0 1: PCLKA/2 (timer module clock/2) 1 0: PCLKA/4 (timer module clock/4) 1 1: PCLKA/8 (timer module clock/8)	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	CCLR[1:0]	Counter Clear Source Select	b13 b12 0 0: None of the following clearing sources is specified. 0 1: Cleared by GTCCRA input capture 1 0: Cleared by GTCCRB input capture 1 1: Cleared by counter clearing in another channel performing synchronized clearing/synchronized operation	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTCR controls GTCNT.

GTCR should be set while GTCNT operation is stopped. Value written to GTCR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

MD[2:0] Bits (Mode Select)

These bits select the GPT operating mode.

TPCS[1:0] Bits (Timer Prescaler Select)

These bits select the clock for GTCNT. A clock source can be selected independently for each channel.

CCLR[1:0] Bits (Counter Clear)

These bits select the clearing source for GTCNT.

In saw-wave mode, when synchronized clearing is selected, synchronized clearing is handled equally to clearing by the counter's overflow or underflow and the pin output and buffer transfer are performed. However, the overflow flag and underflow flag are not set.

In triangle-wave mode, when synchronized clearing is selected, only counter clearing is performed. Though the counter value becomes 0, it is not handled as a trough.

Once 01b, 10b, or 11b is selected as a counter clear source, counter clearing by the source is executed whether the

GPTn.GTCNT count operation is performed (GTSTR.CSTn = 1; n = 0 to 3) or stopped (GTSTR.CSTn = 0, n = 0 to 3). When synchronized clearing is in use, the CCLR[1:0] bits of the target channel should not be set to 01b or 10b.

24.2.20 General PWM Timer Buffer Enable Register (GTBER)

Address(es): GPT0.GTBER 000C 2106h, GPT1.GTBER 000C 2186h, GPT2.GTBER 000C 2206h, GPT3.GTBER 000C 2286h, GPT4.GTBER 000C 2906h, GPT5.GTBER 000C 2986h, GPT6.GTBER 000C 2A06h, GPT7.GTBER 000C 2A86h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCRA[1:0]	GTCCRA Buffer Operation	b1 b0 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTCCRA ⇔ GTCCRC) 1 x: Double buffer operation (GTCCRA ⇔ GTCCRC ⇔ GTCCRD)	R/W
b3, b2	CCRB[1:0]	GTCCRB Buffer Operation	b3 b2 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTCCRB ⇔ GTCCRE) 1 x: Double buffer operation (GTCCRB ⇔ GTCCRE ⇔ GTCCRF)	R/W
b5, b4	PR[1:0]	GTPR Buffer Operation	b5 b4 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTPBR ⇒ GTPR) 1 x: Double buffer operation (GTPDBR ⇒ GTPBR ⇒ GTPR)	R/W
b6	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation	Writing 1 to this bit forcibly performs buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9, b8	ADTTA[1:0]	GTADTRA Buffer Transfer Timing Select	• Triangle waves b9 b8 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Saw waves b9 b8 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting) or overflow (during up-counting) is performed.	R/W
b10	ADTDA	GTADTRA Double Buffer Operation	0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTRA)	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	ADTTB[1:0]	GTADTRB Buffer Transfer Timing Select	• Triangle waves b13 b12 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Saw waves b13 b12 0 0: No transfer Values other than 0 0: Transfer at an underflow (in down-counting) or overflow (in up-counting) is performed.	R/W
b14	ADTDB	GTADTRB Double Buffer Operation	0: Single buffer operation (GTADTBRB → GTADTRB) 1: Double buffer operation (GTADTDBRB → GTADTBRB → GTADTRB)	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

GTBER makes settings for buffer operation.
GTBER should be set while GTCNT operation is stopped. Value written to GTBER is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

CCRA[1:0] Bits (GTCCRA Buffer Operation)

These bits set buffer operation with GTCCRA, GTCCRC, and GTCCRD combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

CCRB[1:0] Bits (GTCCRB Buffer Operation)

These bits set buffer operation with GTCCRB, GTCCRE, and GTCCRF combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

PR[1:0] Bits (GTPR Buffer Operation)

These bits set buffer operation with GTPR, GTPBR, and GTPDBR combined.
When using down-counting in saw-wave operation, set the PR[1:0] bits to 00b.

CCRSWT Bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forcibly performs buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.
This bit is valid only when counting is stopped with compare match operation specified.

ADTTA[1:0] Bits (GTADTRA Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of GTADTRA, GTADTBRA, and GTADTDBRA.

ADTDA Bit (GTADTRA Double Buffer Operation)

These bits set buffer operation with GTADTRA, GTADTBRA, and GTADTDBRA combined.

ADTTB[1:0] Bits (GTADTRB Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of GTADTRB, GTADTBRB, and GTADTDBRB.

ADTDB Bit (GTADTRB Double Buffer Operation)

These bits set buffer operation with GTADTRB, GTADTBRB, and GTADTDBRB combined.

Note 1. The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (32-bit transfer at trough).

24.2.21 General PWM Timer Count Direction Register (GTUDC)

Address(es): GPT0.GTUDC 000C 2108h, GPT1.GTUDC 000C 2188h, GPT2.GTUDC 000C 2208h, GPT3.GTUDC 000C 2288h, GPT4.GTUDC 000C 2908h, GPT5.GTUDC 000C 2988h, GPT6.GTUDC 000C 2A08h, GPT7.GTUDC 000C 2A88h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	UD	Count Direction Setting	0: GTCNT counts down. 1: GTCNT counts up.	R/W
b1	UDF	Forcible Count Direction Setting	0: Not forcibly set 1: Forcibly set	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTUDC sets the direction in which GTCNT counts (up-counting or down-counting). Value written to GTUDC is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

- In saw-wave mode

When the UD value is set to 0 during up-counting, the count direction is changed at an overflow (GTCNT = GTPR).
When the UD value is set to 1 during up-counting, the count direction is changed at an underflow (GTCNT = 0).
If the UD value is changed from 1 to 0 with the UDF bit being 0 and while counting is stopped, the counter starts up-count operation and the count direction is changed at an overflow (GTCNT = GTPR).
If the UD value is changed from 0 to 1 with the UDF bit being 0 and while counting is stopped, the counter starts down-count operation and the count direction is changed at an underflow (GTCNT = 0).
When the UDF bit is set to 1 while counting is stopped, the UD bit value at that time is reflected in the count direction when counting starts.

- In triangle-wave mode

Even if the UD value is changed during counting, the change will not be reflected in the count direction.
If the UD value is modified while the UDF bit is 0 and counting is stopped, the change will not be reflected in the count direction when counting starts. If the UDF bit is set to 1 while counting is stopped, the UD bit value at that time is reflected in the count direction when counting starts.

UD Bit (Count Direction Setting)

This bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF Bit (Forcible Count Direction Setting)

This bit forcibly sets the count direction when GTCNT starts operation as the UD value.
Only 0 should be written to this bit during counter operation.
When 1 has been written to this bit while counting is stopped, this bit should be returned to 0 before counting starts.

24.2.22 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC)

Address(es): GPT0.GTITC 000C 210Ah, GPT1.GTITC 000C 218Ah, GPT2.GTITC 000C 220Ah, GPT3.GTITC 000C 228Ah, GPT4.GTITC 000C 290Ah, GPT5.GTITC 000C 298Ah, GPT6.GTITC 000C 2A0Ah, GPT7.GTITC 000C 2A8Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ITLA	GTCCRA Compare Match/ Input Capture Interrupt Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b1	ITLB	GTCCRB Compare Match/ Input Capture Interrupt Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b2	ITLC	GTCCRC Compare Match Interrupt Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b3	ITLD	GTCCRD Compare Match Interrupt Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b4	ITLE	GTCCRE Compare Match Interrupt Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b5	ITLF	GTCCRF Compare Match Interrupt Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b7, b6	IVTC[1:0]	GTCIV Interrupt Skipping Function Select	b7 b6 0 0: Skipping is not performed 0 1: Both overflow and underflow for saw waves and crest for triangle waves are counted and skipped 1 0: Both overflow and underflow for saw waves and trough for triangle waves are counted and skipped 1 1: Both overflow and underflow for saw waves and both crest and trough for triangle waves are counted and skipped	R/W
b10 to b8	IVTT[2:0]	GTCIV Interrupt Skipping Count Select	b10 b8 0 0 0: Skipping is not performed 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	ADTAL	GTADTRA A/D Converter Start Request Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	ADTBL	GTADTRB A/D Converter Start Request Link	0: Not linked with GTCIV interrupt skipping function. 1: Linked with GTCIV interrupt skipping function.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

GTITC sets the skipping function for GTCNT counter overflows (GTPR compare match) or underflow interrupts (GTCIV) and also sets whether to link the other interrupts and A/D converter start requests with the GTCIV interrupt skipping function. Note that dead time error interrupts cannot be linked with the GTCIV interrupt skipping function. When the interrupt skipping function is set, the change in the corresponding status flag is also skipped. Value written to GTITC is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

ITLA Bit (GTCCRA Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRA compare match/input capture interrupt (GTCIA) with the GTCIV interrupt skipping function.

ITLB Bit (GTCCRB Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRB compare match/input capture interrupt (GTCIB) with the GTCIV interrupt skipping function.

ITLC Bit (GTCCRC Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRC compare match interrupt (GTCIC) with the GTCIV interrupt skipping function.

ITLD Bit (GTCCRD Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRD compare match interrupt (GTCID) with the GTCIV interrupt skipping function.

ITLE Bit (GTCCRE Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRE compare match interrupt (GTCIE) with the GTCIV interrupt skipping function.

ITLF Bit (GTCCRF Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRF compare match interrupt (GTCIF) with the GTCIV interrupt skipping function.

IVTC[1:0] Bits (GTCIV Interrupt Skipping Function Select)

These bits set the skipping function for the GTPR compare match (GTCNT overflow)/GTCNT underflow interrupt (GTCIV).

IVTT[2:0] Bits (GTCIV Interrupt Skipping Count Select)

These bits select the skipping count for the GTPR compare match (GTCNT overflow)/GTCNT underflow interrupt (GTCIV).

When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL Bit (GTADTRA A/D Converter Start Request Link)

This bit specifies whether to link the GTADTRA A/D converter start request with GTCIVn interrupt skipping function.

ADTBL Bit (GTADTRB A/D Converter Start Request Link)

This bit specifies whether to link the GTADTRB A/D converter start request with GTCIVn interrupt skipping function.

24.2.23 General PWM Timer Status Register (GTST)

Address(es): GPT0.GTST 000C 210Ch, GPT1.GTST 000C 218Ch, GPT2.GTST 000C 220Ch, GPT3.GTST 000C 228Ch, GPT4.GTST 000C 290Ch, GPT5.GTST 000C 298Ch, GPT6.GTST 000C 2A0Ch, GPT7.GTST 000C 2A8Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	DTEF	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TCFA	Input Capture/Compare Match Flag A	0: No GTCCRA input capture/compare match has occurred. 1: A GTCCRA input capture/compare match has occurred.	R/(W) *1
b1	TCFB	Input Capture/Compare Match Flag B	0: No GTCCRB input capture/compare match has occurred. 1: A GTCCRB input capture/compare match has occurred.	R/(W) *1
b2	TCFC	Compare Match Flag C	0: No GTCCRC compare match has occurred. 1: A GTCCRC compare match has occurred.	R/(W) *1
b3	TCFD	Compare Match Flag D	0: No GTCCRD compare match has occurred. 1: A GTCCRD compare match has occurred.	R/(W) *1
b4	TCFE	Compare Match Flag E	0: No GTCCRE compare match has occurred. 1: A GTCCRE compare match has occurred.	R/(W) *1
b5	TCFF	Compare Match Flag F	0: No GTCCRF compare match has occurred. 1: A GTCCRF compare match has occurred.	R/(W) *1
b6	TCFPO	Overflow Flag	0: No overflow or crest has occurred. 1: An overflow or crest has occurred.	R/(W) *1
b7	TCFPU	Underflow Flag	0: No underflow or trough has occurred. 1: An underflow or trough has occurred.	R/(W) *1
b10 to b8	ITCNT[2:0]	GTCIV Interrupt Skipping Count Counter	Counter for counting the number of times a timer interrupt has been skipped.	R
b11	DTEF	Dead Time Error Flag	0: No dead time error has occurred. 1: A dead time error has occurred.	R
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	TUCF	Count Direction Flag	0: The GPTn.GTCNT counter counts downward. 1: The GPTn.GTCNT counter counts upward.	R

Note 1. Only 0 can be written to clear the flag. When clearing the TCFA, TCFB, TCFC, TCFD, TCFE, TCFF, TCFPO, or TCFPU bits, be sure to clear only the target bit or bits for clearing and to write 1 to the other bits.

GTST indicates the status of the GPT. Value written to GTST is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

TCFA Flag (Input Capture/Compare Match Flag A)

This status flag indicates generation of a GTCCRA input capture/compare match.

[Setting conditions]

- GTCNT matches GTCCRA when GTCCRA functions as a compare match register.
- The GTCNT value is transferred to GTCCRA by an input capture signal when GTCCRA functions as an input capture register.

[Clearing condition]

- 0 is written to the TCFA flag.

TCFB Flag (Input Capture/Compare Match Flag B)

This status flag indicates generation of a GTCCRB input capture/compare match.

[Setting conditions]

- GTCNT matches GTCCRB when GTCCRB functions as a compare match register
- The GTCNT value is transferred to GTCCRB by an input capture signal if GTCCRB is functioning as an input capture register

[Clearing condition]

- 0 is written to the TCFB flag.

TCFC Flag (Compare Match Flag C)

This status flag indicates generation of a GTCCRC compare match.
Comparison is not performed when GTCCRC is used for buffer operation.

[Setting condition]

- GTCNT matches GTCCRC.

[Clearing condition]

- 0 is written to the TCFC flag.

[Conditions for not performing comparison]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, or 11b (GTCCRC is used for buffer operation)

TCFD Flag (Compare Match Flag D)

This status flag indicates generation of a GTCCRD compare match.
Comparison is not performed when GTCCRD is used for buffer operation.

[Setting condition]

- GTCNT matches GTCCRD.

[Clearing condition]

0 is written to the TCFD flag.

[Conditions for not performing comparison]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b or 11b (GTCCRD is used for buffer operation)

TCFE Flag (Compare Match Flag E)

This status flag indicates generation of a GTCCRE compare match.
Comparison is not performed when GTCCRE is used for buffer operation.

[Setting condition]

- GTCNT matches GTCCRE.

[Clearing condition]

- 0 is written to the TCFE flag.

[Conditions for not performing comparison]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, or 11b (GTCCRE is used for buffer operation)

TCFF Flag (Compare Match Flag F)

This status flag indicates generation of a GTCCRF compare match.
Comparison is not performed when GTCCRF is used for buffer operation.

[Setting condition]

- GTCNT matches GTCCRF.

[Clearing condition]

- 0 is written to the TCFF flag.

[Conditions for not performing comparison]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b or 11b (GTCCRF is used for buffer operation)

TCFPO Flag (Overflow Flag)

This flag indicates generation of an overflow or crest.

[Setting conditions]

- For saw waves, when an overflow has occurred (GTCNT matches GTPR during up-count operation).
- For triangle waves, when a crest has occurred (GTCNT matches GTPR).

[Clearing condition]

- 0 is written to the TCFPO flag.

TCFPU Flag (Underflow Flag)

- This flag indicates generation of an underflow or trough.

[Setting conditions]

- For saw waves, when an underflow has occurred (GTCNT reaches 0 during down-count operation).
- For triangle waves, when a trough has occurred (GTCNT reaches 0).

[Clearing condition]

- 0 is written to the TCFPU flag.

ITCNT[2:0] Bits (GTCIV Interrupt Skipping Count Counter)

When the GTCIV interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter is incremented by 1 every time the GTCIV interrupt source is generated.

[Clearing conditions]

- The GTCIV interrupt skipping function is not used (GTITC.IVTT[2:0] is 000b when GTITC.IVTC[1:0] is 00b).
- The GTCIV interrupt skipping count matches the specified count (ITCNT[2:0] matches the skipping count specified by GTITC.IVTT[2:0]).

DTEF Flag (Dead Time Error Flag)

This flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.
This flag returns to 0 when the timer output toggle point after the automatic addition of dead time is back within the cycle. This flag can only be read from. (Writing 0 to clear the flag is not allowed.)
When an interrupt by the DTEF flag is enabled (GTINTAD.EINT = 1), a GTCIC interrupt is generated every time the DTEF flag changes from 0 to 1.
[Setting condition]

- The timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the timer cycle.

TUCF Flag (Count Direction Flag)

This flag indicates the count direction of GTCNT.

24.2.24 General PWM Timer Counter (GTCNT)

Address(es): GPT0.GTCNT 000C 210Eh, GPT1.GTCNT 000C 218Eh, GPT2.GTCNT 000C 220Eh, GPT3.GTCNT 000C 228Eh, GPT4.GTCNT 000C 290Eh, GPT5.GTCNT 000C 298Eh, GPT6.GTCNT 000C 2A0Eh, GPT7.GTCNT 000C 2A8Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCNT is a 16-bit readable/writable counter. There is a total of four GTCNT counters, one counter for each channel. There is one GTCNT counter for each channel.
GTCNT can be written to only when counting is stopped; GTCNT cannot be written to during counting operation.
GTCNT should always be accessed in 16-bits. Access in 8-bit units is prohibited. Value written to GTCNT is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

24.2.25 General PWM Timer Compare Capture Register m (GTCCRm) (m = A to F)

Address(es): GPT0.GTCCRA 000C 2110h, GPT1.GTCCRA 000C 2190h, GPT2.GTCCRA 000C 2210h, GPT3.GTCCRA 000C 2290h, GPT0.GTCCRB 000C 2112h, GPT1.GTCCRB 000C 2192h, GPT2.GTCCRB 000C 2212h, GPT3.GTCCRB 000C 2292h, GPT0.GTCCRC 000C 2114h, GPT1.GTCCRC 000C 2194h, GPT2.GTCCRC 000C 2214h, GPT3.GTCCRC 000C 2294h, GPT0.GTCCRD 000C 2116h, GPT1.GTCCRD 000C 2196h, GPT2.GTCCRD 000C 2216h, GPT3.GTCCRD 000C 2296h, GPT0.GTCCRE 000C 2118h, GPT1.GTCCRE 000C 2198h, GPT2.GTCCRE 000C 2218h, GPT3.GTCCRE 000C 2298h, GPT0.GTCCRF 000C 211Ah, GPT1.GTCCRF 000C 219Ah, GPT2.GTCCRF 000C 221Ah, GPT3.GTCCRF 000C 229Ah, GPT4.GTCCRA 000C 2910h, GPT5.GTCCRA 000C 2990h, GPT6.GTCCRA 000C 2A10h, GPT7.GTCCRA 000C 2A90h, GPT4.GTCCRB 000C 2912h, GPT5.GTCCRB 000C 2992h, GPT6.GTCCRB 000C 2A12h, GPT7.GTCCRB 000C 2A92h, GPT4.GTCCRC 000C 2914h, GPT5.GTCCRC 000C 2994h, GPT6.GTCCRC 000C 2A14h, GPT7.GTCCRC 000C 2A94h, GPT4.GTCCRD 000C 2916h, GPT5.GTCCRD 000C 2996h, GPT6.GTCCRD 000C 2A16h, GPT7.GTCCRD 000C 2A96h, GPT4.GTCCRE 000C 2918h, GPT5.GTCCRE 000C 2998h, GPT6.GTCCRE 000C 2A18h, GPT7.GTCCRE 000C 2A98h, GPT4.GTCCRF 000C 291Ah, GPT5.GTCCRF 000C 299Ah, GPT6.GTCCRF 000C 2A1Ah, GPT7.GTCCRF 000C 2A9Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTCCRm registers are 16-bit readable/writable registers. There are six GTCCRm registers for each channel.
GTCCRA and GTCCRB are registers used for both output compare and input capture.
GTCCRC and GTCCRE are compare match registers that can also function as buffer registers for GTCCRA and GTCCRB.
GTCCRD and GTCCRF are compare match registers that can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB). Value written to GTCCRm is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7; m = A to F).

24.2.26 General PWM Timer Cycle Setting Register (GTPR)

Address(es): GPT0.GTPR 000C 211Ch, GPT1.GTPR 000C 219Ch, GPT2.GTPR 000C 221Ch, GPT3.GTPR 000C 229Ch, GPT4.GTPR 000C 291Ch, GPT5.GTPR 000C 299Ch, GPT6.GTPR 000C 2A1Ch, GPT7.GTPR 000C 2A9Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPR is an 16-bit readable/writable register that is used to set the maximum count of the GTCNT counter. The MTU has 4 GTPR registers, one for each channel.
For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.
Do not change GTPR when using down-counting in saw-wave operation.
Value written to GTPR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

24.2.27 General PWM Timer Cycle Setting Buffer Register (GTPBR)

Address(es): GPT0.GTPBR 000C 211Eh, GPT1.GTPBR 000C 219Eh, GPT2.GTPBR 000C 221Eh, GPT3.GTPBR 000C 229Eh, GPT4.GTPBR 000C 291Eh, GPT5.GTPBR 000C 299Eh, GPT6GTPBR 000C 2A1Eh, GPT7.GTPBR 000C 2A9Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPBR is a 16-bit readable/writable register that functions as a buffer register for GTPR. There is one GTPBR register for each channel. Setting of buffered operation is prohibited when down-counting is used in saw-wave generation.

The buffer transfer is performed on an overflow or counter clearing in saw-wave mode, and at the troughs in triangle-wave mode. Value written to GTPBR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

24.2.28 General PWM Timer Cycle Setting Double-Buffer Register (GTPDBR)

Address(es): GPT0.GTPDBR 000C 2120h, GPT1.GTPDBR 000C 21A0h, GPT2.GTPDBR 000C 2220h, GPT3.GTPDBR 000C 22A0h, GPT4.GTPDBR 000C 2920h, GPT5.GTPDBR 000C 29A0h, GPT6.GTPDBR 000C 2A20h, GPT7.GTPDBR 000C 2AA0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPDBR is a 16-bit readable/writable register that functions as a buffer register for GTPBR (double-buffer register for GTPR). There is one GTPDBR register for each channel. Value written to GTPDBR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

24.2.29 A/D Converter Start Request Timing Register m (GTADTRm) (m = A, B)

Address(es): GPT0.GTADTRA 000C 2124h, GPT1.GTADTRA 000C 21A4h, GPT2.GTADTRA 000C 2224h, GPT3.GTADTRA 000C 22A4h, GPT0.GTADTRB 000C 212Ch, GPT1.GTADTRB 000C 21Ach, GPT2.GTADTRB 000C 222Ch, GPT3.GTADTRB 000C 22ACh, GPT4.GTADTRA 000C 2924h, GPT5.GTADTRA 000C 29A4h, GPT6.GTADTRA 000C 2A24h, GPT7.GTADTRA 000C 2AA4h, GPT4.GTADTRB 000C 292Ch, GPT5.GTADTRB 000C 29ACh, GPT6.GTADTRB 000C 2A2Ch, GPT7.GTADTRB 000C 2AACh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTADTRm registers are 16-bit readable/writable registers that set the timing of A/D converter start request generation. When the GTADTRm value matches the GTCNT counter value, an A/D converter start request is generated. There are two GTADTRm registers for each channel.

GTADTRm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Value written to GTADTRm is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7; m = A, B).

24.2.30 A/D Converter Start Request Timing Buffer Register m (GTADTBRm) (m = A, B)

Address(es): GPT0.GTADTBRA 000C 2126h, GPT1.GTADTBRA 000C 21A6h, GPT2.GTADTBRA 000C 2226h, GPT3.GTADTBRA 000C 22A6h, GPT0.GTADTBRB 000C 212Eh, GPT1.GTADTBRB 000C 21AEh, GPT2.GTADTBRB 000C 222Eh, GPT3.GTADTBRB 000C 22AEh, GPT4.GTADTBRA 000C 2926h, GPT5.GTADTBRA 000C 29A6h, GPT6.GTADTBRA 000C 2A26h, GPT7.GTADTBRA 000C 2AA6h, GPT4.GTADTBRB 000C 292Eh, GPT5.GTADTBRB 000C 29AEh, GPT6.GTADTBRB 000C 2A2Eh, GPT7.GTADTBRB 000C 2AAEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTADTBRm registers are 16-bit readable/writable registers that function as buffer registers for GTADTRm. There are two GTADTBRm registers for each channel.

GTADTBRm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Value written to

GTADTBRm is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7; m = A, B).

24.2.31 A/D Converter Start Request Timing Double-Buffer Register m (GTADTDBRm) (m = A, B)

Address(es): GPT0.GTADTDBRA 000C 2128h, GPT1.GTADTDBRA 000C 21A8h, GPT2.GTADTDBRA 000C 2228h, GPT3.GTADTDBRA 000C 22A8h, GPT0.GTADTDBRB 000C 2130h, GPT1.GTADTDBRB 000C 21B0h, GPT2.GTADTDBRB 000C 2230h, GPT3.GTADTDBRB 000C 22B0h, GPT4.GTADTDBRA 000C 2928h, GPT5.GTADTDBRA 000C 29A8h, GPT6.GTADTDBRA 000C 2A28h, GPT7.GTADTDBRA 000C 2AA8h, GPT4.GTADTDBRB 000C 2930h, GPT5.GTADTDBRB 000C 29B0h, GPT6.GTADTDBRB 000C 2A30h, GPT7.GTADTDBRB 000C 2AB0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTADTDBRm registers are 16-bit readable/writable registers that function as buffer registers for GTADTBRm (double-buffer registers for GTADTR). There are two GTADTDBRm registers for each channel.
GTADTDBRm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Value written to GTADTDBRm is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7; m = A, B).

24.2.32 General PWM Timer Output Negate Control Register (GTONCR)

Address(es): GPT0.GTONCR 000C 2134h, GPT1.GTONCR 000C 21B4h, GPT2.GTONCR 000C 2234h, GPT3.GTONCR 000C 22B4

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBE	OAE	—	SWN	—	—	—	NFV	NFS[3:0]				NVB	NVA	NEB	NEA
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NEA	GTIOCnA Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W
b1	NEB	GTIOCnB Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W
b2	NVA	GTIOCnA Pin Negate Value Setting	0: GTIOCnA pin is set to 0 when negate control is performed. 1: GTIOCnA pin is set to 1 when negate control is performed.	R/W
b3	NVB	GTIOCnB Pin Negate Value Setting	0: GTIOCnB pin is set to 0 when negate control is performed. 1: GTIOCnB pin is set to 1 when negate control is performed.	R/W
b7 to b4	NFS[3:0]	GTIOC Output Negate Source Select	b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection*2 0 1 0 1: AN101 comparator detection*2 0 1 1 0: AN102 comparator detection*2 0 1 1 1: GTETRG0 pin input 1 x x x: Software control (control through SWN bit)	R/W
b8	NFV	Negate Source Polarity Select	0: Negate control is provided when the negate source has become 0. 1: Negate control is provided when the negate source has become 1.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b12	SWN	Software Negate Control	When NFV bit is 0: 0: Negate control is provided. 1: Negate control is not provided. When NFV bit is 1: 0: Negate control is not provided. 1: Negate control is provided.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	OAE	GTIOCnA Pin Output Enable	0: No pin output 1: Pin output	R/W
b15	OBE	GTIOCnB Pin Output Enable	0: No pin output 1: Pin output	R/W

Note 1. n=0 to 3
Note 2. Do not make this setting in 64- and 48-pin products.

GTONCR controls negate of the GTIOCnA pin output and GTIOCnB pin output. Value written to GTONCR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 3).

NEA Bit (GTIOCnA Pin Negate Control Enable)

This bit enables negate control of the GTIOCnA pin output.

NEB Bit (GTIOCnB Pin Negate Control Enable)

This bit enables negate control of the GTIOCnB pin output.

NVA Bit (GTIOCnA Pin Negate Value Setting)

This bit sets the output value of the GTIOCnA pin at negate control.

NVB Bit (GTIOCnB Pin Negate Value Setting)

This bit sets the output value of the GTIOCnB pin at negate control.

NFS[3:0] Bits (GTIOC Output Negate Source Select)

These bits select the negate source for the GTIOCnA pin output and GTIOCnB pin output.

NFV Bit (Negate Source Polarity Select)

This bit selects the negate source polarity for the GTIOCnA pin output and GTIOCnB pin output.

SWN Bit (Software Negate Control)

This bit specifies whether to provide negate control for the GTIOCnA pin output and GTIOCnB pin output.
This bit setting is valid when software control is selected as the negate source (NFS[3] bit is set to 1).

OAE Bit (GTIOCnA Pin Output Enable)

This bit selects whether to output the GTIOCnA pin output. This bit setting is valid only when compare match has been set (bit 5 in GTIOR is 0).

OBE Bit (GTIOCnB Pin Output Enable)

This bit selects whether to output the GTIOCnB pin output.This bit setting is valid only when compare match has been set (bit 13 in GTIOR is 0).

Address(es): GPT4.GTONCR 000C 2934h, GPT5.GTONCR 000C 29B4h, GPT6.GTONCR 000C 2A34h, GPT7.GTONCR 000C 2AB4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBE	OAE	—	SWN	—	—	—	NFV	NFS[3:0]				NVB	NVA	NEB	NEA
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NEA	GTIOCnA Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W
b1	NEB	GTIOCnB Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W
b2	NVA	GTIOCnA Pin Negate Value Setting	0: GTIOCnA pin is set to 0 when negate control is performed. 1: GTIOCnA pin is set to 1 when negate control is performed.	R/W
b3	NVB	GTIOCnB Pin Negate Value Setting	0: GTIOCnB pin is set to 0 when negate control is performed. 1: GTIOCnB pin is set to 1 when negate control is performed.	R/W
b7 to b4	NFS[3:0]	GTIOC Output Negate Source Select	b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: GTETRG1 pin input 1 x x x: Software control (control through SWN bit)	R/W
b8	NFV	Negate Source Polarity Select	0: Negate control is provided when the negate source has become 0. 1: Negate control is provided when the negate source has become 1.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	SWN	Software Negate Control	When NFV bit is 0: 0: Negate control is provided. 1: Negate control is not provided. When NFV bit is 1: 0: Negate control is not provided. 1: Negate control is provided.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	OAE	GTIOCnA Pin Output Enable	0: No pin output 1: Pin output	R/W
b15	OBE	GTIOCnB Pin Output Enable	0: No pin output 1: Pin output	R/W

Note: • n=4 to 7

GTONCR controls negate of the GTIOCnA pin output and GTIOCnB pin output. Value written to GTONCR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 4 to 7).

NEA Bit (GTIOCnA Pin Negate Control Enable)

This bit enables negate control of the GTIOCnA pin output.

NEB Bit (GTIOCnB Pin Negate Control Enable)

This bit enables negate control of the GTIOCnB pin output.

NVA Bit (GTIOCnA Pin Negate Value Setting)

This bit sets the output value of the GTIOCnA pin at negate control.

NVB Bit (GTIOCnB Pin Negate Value Setting)

This bit sets the output value of the GTIOCnB pin at negate control.

NFS[3:0] Bits (GTIOC Output Negate Source Select)

These bits select the negate source for the GTIOCnA pin output and GTIOCnB pin output.

NFV Bit (Negate Source Polarity Select)

This bit selects the negate source polarity for the GTIOCnA pin output and GTIOCnB pin output.

SWN Bit (Software Negate Control)

This bit specifies whether to provide negate control for the GTIOCnA pin output and GTIOCnB pin output.
This bit setting is valid when software control is selected as the negate source (NFS[3] bit is set to 1).

OAE Bit (GTIOCnA Pin Output Enable)

This bit selects whether to output the GTIOCnA pin output. This bit setting is valid only when compare match has been set (bit 5 in GTIOR is 0).

OBE Bit (GTIOCnB Pin Output Enable)

This bit selects whether to output the GTIOCnB pin output. This bit setting is valid only when compare match has been set (bit 13 in GTIOR is 0).

24.2.33 General PWM Timer Dead Time Control Register (GTDTCR)

Address(es): GPT0.GTDTCR 000C 2136h, GPT1.GTDTCR 000C 21B6h, GPT2.GTDTCR 000C 2236h, GPT3.GTDTCR 000C 22B6h, GPT4.GTDTCR 000C 2936h, GPT5.GTDTCR 000C 29B6h, GPT6.GTDTCR 000C 2A36h, GPT7.GTDTCR 000C 2AB6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: GTCCRB is set without using GTDVU and GTDVD. 1: GTDVU and GTDVD are used to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TDBUE	GTDVU Buffer Operation Enable	0: GTDVU buffer operation is disabled 1: GTDVU buffer operation is enabled	R/W
b5	TDBDE	GTDVD Buffer Operation Enable	0: GTDVD buffer operation is disabled 1: GTDVD buffer operation is enabled	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TDFER	GTDVD Setting	0: GTDVU and GTDVD are set separately. 1: The value written to GTDVU is automatically set to GTDVD.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. Value written to GTDTCR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

TDE Bit (Negative-Phase Waveform Setting)

This bit sets whether to use GTDVU and GTDVD. When GTDVU and GTDVD are used, the compare match value for a negative-phase waveform with dead time that was obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU and GTDVD) is automatically set in GTCCRB.
The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The automatically set GTCCRB value has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB and the GPTn.GTST.DTEF flag is set to 1.

- Triangle waves
  Upper limit value: GTPR – 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode
  Upper limit value: GTPR
  Lower limit value: 0

TDBUE Bit (GTDVU Buffer Operation Enable)

This bit enables buffer operation with GTDVU and GTDBU combined.
The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves.

TDBDE Bit (GTDVD Buffer Operation Enable)

This bit enables buffer operation with GTDVD and GTDBD combined.

The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves.

When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

TDFER Bit (GTDVD Setting)

This bits sets whether or not the value written to GTDVU is also set to GTDVD automatically.

24.2.34 General PWM Timer Dead Time Value Register m (GTDVm) (m = U, D)

Address(es): GPT0.GTDVU 000C 2138h, GPT1.GTDVU 000C 21B8h, GPT2.GTDVU 000C 2238h, GPT3.GTDVU 000C 22B8h, GPT0.GTDVD 000C 213Ah, GPT1.GTDVD 000C 21Bah, GPT2.GTDVD 000C 223Ah, GPT3.GTDVD 000C 22BAh, GPT4.GTDVU 000C 2938h, GPT5.GTDVU 000C 29B8h, GPT6.GTDVU 000C 2A38h, GPT7.GTDVU 000C 2AB8h GPT4.GTDVD 000C 293Ah, GPT5.GTDVD 000C 29BAh, GPT6.GTDVD 000C 2A3Ah, GPT7.GTDVD 000C 2ABAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDVm is a 16-bit readable/writable register that sets the dead time for generating PWM waveforms with dead time.

There are two GTDVm registers for each channel: GTDVU used for up-counting and GTDVD used for down-counting.

Setting a dead time value that exceeds the cycle is prohibited. The set value can be confirmed by reading from GTCCRB.

When GTDVm is used, writing to GTCCRB is prohibited.

When this register is set to 0, waveforms without dead time are output.

GTDVm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Value written to GTDVm is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

24.2.35 General PWM Timer Dead Time Buffer Register m (GTDBm) (m = U, D)

Address(es): GPT0.GTDBU 000C 213Ch, GPT1.GTDBU 000C 21BCh, GPT2.GTDBU 000C 223Ch, GPT3.GTDBU 000C 22BCh, GPT0.GTDBD 000C 213Eh, GPT1.GTDBD 000C 21Beh, GPT2.GTDBD 000C 223Eh, GPT3.GTDBD 000C 22BEh, GPT4.GTDBU 000C 293Ch, GPT5.GTDBU 000C 29BCh, GPT6.GTDBU 000C 2A3Ch, GPT7.GTDBU 000C 2ABCh GPT4.GTDBD 000C 293Eh, GPT5.GTDBD 000C 29BEh, GPT6.GTDBD 000C 2A3Eh, GPT7.GTDBD 000C 2ABEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDBm is a 16-bit readable/writable register that functions as a buffer register for GTDVm.

There are two GTDBm registers for each channel:

GTDBm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Value written to GTDBm is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

24.2.36 General PWM Timer Output Protection Function Status Register (GTSOS)

Address(es): GPT0.GTSOS 000C 2140h, GPT1.GTSOS 000C 21C0h, GPT2.GTSOS 000C 2240h, GPT3.GTSOS 000C 22C0h, GPT4.GTSOS 000C 2940h, GPT5.GTSOS 000C 29C0h, GPT6.GTSOS 000C 2A40h, GPT7.GTSOS 000C 2AC0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SOS[1:0]	Output Protection Function Status	b1 b0 0 0: Normal operation 0 1: Protected state (GTCCRA = 0 is set during transfer at trough or crest) 1 0: Protected state (GTCCRA ≥ GTPR is set during transfer at trough) 1 1: Protected state (GTCCRA ≥ GTPR is set during transfer at crest)	R
b7 to b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b9, b8	—	Reserved	The read value is undefined. These bits cannot be modified.	R
b15 to b10	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

GTSOS is a status register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (GTDTCR.TDE bit = 1) in triangle-wave mode.

SOS Bit (Output Protection Function Status)

This bit indicates the status of the output protection function in triangle-wave PWM mode. For details of the output protection function, see Output Protection Function for GTIOC Pin Output, Output Protection Function for GTIOC Pin Output Function for GTIOC Pin Output.

24.2.37 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR)

Address(es): GPT0.GTSOTR 000C 2142h, GPT1.GTSOTR 000C 21C2h, GPT2.GTSOTR 000C 2242h, GPT3.GTSOTR 000C 22C2h
GPT4.GTSOTR 000C 2942h, GPT5.GTSOTR 000C 29C2h, GPT6.GTSOTR 000C 2A42h, GPT7.GTSOTR 000C 2AC2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SOTR	Output Protection Function Temporary Release	0: Protected state is not released 1: Protected state is released	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTSOTR temporarily releases the protected state of GTIOCnB pin output when output protection has been set.
The protected state can be released only for the case of GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA ≥ GTPR has occurred during transfer at trough). The protected state cannot be released for any other case. Value written to GTSOTR is ignored when write-protection is set to the relevant channel by the GTWP.WPn bit (n = 0 to 7).

SOTR Bit (Output Protection Function Temporary Release)

This bit sets whether to temporarily release the protected state of the GTIOCnB pin output in an output protected state. After the SOTR bit has been set to 1, the output protection function is canceled from the first trough. After the SOTR bit has been set to 0, output protection is resumed from the first trough.

24.2.38 PWM Output Delay Control Register (GTDLYCR)

Address(es): GPT0.GTDLYCR 000C 2300h, GPT1.GTDLYCR 000C 2302h, GPT2.GTDLYCR 000C 2304h, GPT3.GTDLYCR 000C 2306h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DLYEN	DLYRST	DLLEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DLLEN	DLL Operation Enable	0: DLL operation is disabled 1: DLL operation is enabled	R/W
b1	DLYRST	PWM Delay Generation Circuit Reset	0: Normal operation 1: Reset	R/W
b2	DLYEN	PWM Delay Generation Circuit Enable	0: Delay generation circuit is disabled (bypass operation) 1: Delay generation circuit is enabled	R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDLYCR controls the PWM delay generation circuit that applies delays to the PWM outputs.

DLLEN Bit (DLL Operation Enable)

This bit selects whether the internal DLL in the PWM delay generation circuit is activated or not.

DLYRST Bit (PWM Delay Generation Circuit Reset)

This bit resets the internal state of the PWM delay generation circuit.

DLYEN Bit (PWM Delay Generation Circuit Enable)

This bit selects whether delays are applied to PWM output signals from the GTIOCnA and GTIOCnB pins (n = 0 to 3) by the PWM delay generation circuit or whether the circuit is bypassed.

A signal delayed at the PWM delay generation circuit is output with a delay of 3 cycles of PCLKA compared with the signal bypassed the PWM delay generation circuit.

24.2.39 GTIOC Rising Output Delay Register (GTDLYRA)

Address(es): GPT0.GTDLYRA 000C 2318h, GPT1.GTDLYRA 000C 231Ch, GPT2.GTDLYRA 000C 2320h, GPT3.GTDLYRA 000C 2324h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0 to b4	DLY[4:0]	GTIOCA Output Rising Delay Time Setting	b4 b0 0 0 0 0 0: No delay on rising edges 0 0 0 0 1: Delay of 1/ 32 times the PCLKA period is applied. 0 0 0 1 0: Delay of 2/ 32 times the PCLKA period is applied. 0 0 0 1 1: Delay of 3/ 32 times the PCLKA period is applied. 0 0 1 0 0: Delay of 4/ 32 times the PCLKA period is applied. 0 0 1 0 1: Delay of 5/ 32 times the PCLKA period is applied. 0 0 1 1 0: Delay of 6/ 32 times the PCLKA period is applied. 0 0 1 1 1: Delay of 7/ 32 times the PCLKA period is applied. 0 1 0 0 0: Delay of 8/ 32 times the PCLKA period is applied. 0 1 0 0 1: Delay of 9/ 32 times the PCLKA period is applied. 0 1 0 1 0: Delay of 10/ 32 times the PCLKA period is applied. 0 1 0 1 1: Delay of 11/ 32 times the PCLKA period is applied. 0 1 1 0 0: Delay of 12/ 32 times the PCLKA period is applied. 0 1 1 0 1: Delay of 13/ 32 times the PCLKA period is applied. 0 1 1 1 0: Delay of 14/ 32 times the PCLKA period is applied. 0 1 1 1 1: Delay of 15/ 32 times the PCLKA period is applied. 1 0 0 0 0: Delay of 16/ 32 times the PCLKA period is applied. 1 0 0 0 1: Delay of 17/ 32 times the PCLKA period is applied. 1 0 0 1 0: Delay of 18/ 32 times the PCLKA period is applied. 1 0 0 1 1: Delay of 19/ 32 times the PCLKA period is applied. 1 0 1 0 0: Delay of 20/ 32 times the PCLKA period is applied. 1 0 1 0 1: Delay of 21/ 32 times the PCLKA period is applied. 1 0 1 1 0: Delay of 22/ 32 times the PCLKA period is applied. 1 0 1 1 1: Delay of 23/ 32 times the PCLKA period is applied. 1 1 0 0 0: Delay of 24/ 32 times the PCLKA period is applied. 1 1 0 0 1: Delay of 25/ 32 times the PCLKA period is applied. 1 1 0 1 0: Delay of 26/ 32 times the PCLKA period is applied. 1 1 0 1 1: Delay of 27/ 32 times the PCLKA period is applied. 1 1 1 0 0: Delay of 28/ 32 times the PCLKA period is applied. 1 1 1 0 1: Delay of 29/ 32 times the PCLKA period is applied. 1 1 1 1 0: Delay of 30/ 32 times the PCLKA period is applied. 1 1 1 1 1: Delay of 31/ 32 times the PCLKA period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDLYRA sets the delay time to be applied to rising edges of the output signals on the GTIOCA pin. On the timing for the transfer of settings, see section 24.2.39, GTIOC Rising Output Delay Register (GTDLYRA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.41, GTIOCB Rising Output Delay Register (GTDLYRB), and section 24.2.42, GTIOCB Falling Output Delay Register (GTDLYFB).

24.2.40 GTIOCA Falling Output Delay Register (GTDLYFA)

Address(es): GPT0.GTDLYFA 000C 2328h, GPT1.GTDLYFA 000C 232Ch, GPT2.GTDLYFA 000C 2330h, GPT3.GTDLYFA 000C 2334h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0 to b4	DLY[4:0]	GTIOCA Output Falling Delay Time Setting	b4 b0 0 0 0 0 0: Not delay on falling edges 0 0 0 0 1: Delay of 1/ 32 times the PCLKA period is applied. 0 0 0 1 0: Delay of 2/ 32 times the PCLKA period is applied. 0 0 0 1 1: Delay of 3/ 32 times the PCLKA period is applied. 0 0 1 0 0: Delay of 4/ 32 times the PCLKA period is applied. 0 0 1 0 1: Delay of 5/ 32 times the PCLKA period is applied. 0 0 1 1 0: Delay of 6/ 32 times the PCLKA period is applied. 0 0 1 1 1: Delay of 7/ 32 times the PCLKA period is applied. 0 1 0 0 0: Delay of 8/ 32 times the PCLKA period is applied. 0 1 0 0 1: Delay of 9/ 32 times the PCLKA period is applied. 0 1 0 1 0: Delay of 10/ 32 times the PCLKA period is applied. 0 1 0 1 1: Delay of 11/ 32 times the PCLKA period is applied. 0 1 1 0 0: Delay of 12/ 32 times the PCLKA period is applied. 0 1 1 0 1: Delay of 13/ 32 times the PCLKA period is applied. 0 1 1 1 0: Delay of 14/ 32 times the PCLKA period is applied. 0 1 1 1 1: Delay of 15/ 32 times the PCLKA period is applied. 1 0 0 0 0: Delay of 16/ 32 times the PCLKA period is applied. 1 0 0 0 1: Delay of 17/ 32 times the PCLKA period is applied. 1 0 0 1 0: Delay of 18/ 32 times the PCLKA period is applied. 1 0 0 1 1: Delay of 19/ 32 times the PCLKA period is applied. 1 0 1 0 0: Delay of 20/ 32 times the PCLKA period is applied. 1 0 1 0 1: Delay of 21/ 32 times the PCLKA period is applied. 1 0 1 1 0: Delay of 22/ 32 times the PCLKA period is applied. 1 0 1 1 1: Delay of 23/ 32 times the PCLKA period is applied. 1 1 0 0 0: Delay of 24/ 32 times the PCLKA period is applied. 1 1 0 0 1: Delay of 25/ 32 times the PCLKA period is applied. 1 1 0 1 0: Delay of 26/ 32 times the PCLKA period is applied. 1 1 0 1 1: Delay of 27/ 32 times the PCLKA period is applied. 1 1 1 0 0: Delay of 28/ 32 times the PCLKA period is applied. 1 1 1 0 1: Delay of 29/ 32 times the PCLKA period is applied. 1 1 1 1 0: Delay of 30/ 32 times the PCLKA period is applied. 1 1 1 1 1: Delay of 31/ 32 times the PCLKA period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDLYFA sets the delay time to be applied to the falling edges of output signals on the GTIOCA pin. On the timing for the transfer of settings, see section 24.2.39, GTIOC Rising Output Delay Register (GTDLYRA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.41, GTIOCB Rising Output Delay Register (GTDLYRB), and section 24.2.42, GTIOCB Falling Output Delay Register (GTDLYFB).

24.2.41 GTIOCB Rising Output Delay Register (GTDLYRB)

Address(es): GPT0.GTDLYRB 000C 231Ah, GPT1.GTDLYRB 000C 231Eh, GPT2.GTDLYRB 000C 2322h, GPT3.GTDLYRB 000C 2326h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0 to b4	DLY[4:0]	GTIOCB Output Rising Delay Time Setting	b4 b0 0 0 0 0 0: No delay on rising edges 0 0 0 0 1: Delay of 1/ 32 times the PCLKA period is applied. 0 0 0 1 0: Delay of 2/ 32 times the PCLKA period is applied. 0 0 0 1 1: Delay of 3/ 32 times the PCLKA period is applied. 0 0 1 0 0: Delay of 4/ 32 times the PCLKA period is applied. 0 0 1 0 1: Delay of 5/ 32 times the PCLKA period is applied. 0 0 1 1 0: Delay of 6/ 32 times the PCLKA period is applied. 0 0 1 1 1: Delay of 7/ 32 times the PCLKA period is applied. 0 1 0 0 0: Delay of 8/ 32 times the PCLKA period is applied. 0 1 0 0 1: Delay of 9/ 32 times the PCLKA period is applied. 0 1 0 1 0: Delay of 10/ 32 times the PCLKA period is applied. 0 1 0 1 1: Delay of 11/ 32 times the PCLKA period is applied. 0 1 1 0 0: Delay of 12/ 32 times the PCLKA period is applied. 0 1 1 0 1: Delay of 13/ 32 times the PCLKA period is applied. 0 1 1 1 0: Delay of 14/ 32 times the PCLKA period is applied. 0 1 1 1 1: Delay of 15/ 32 times the PCLKA period is applied. 1 0 0 0 0: Delay of 16/ 32 times the PCLKA period is applied. 1 0 0 0 1: Delay of 17/ 32 times the PCLKA period is applied. 1 0 0 1 0: Delay of 18/ 32 times the PCLKA period is applied. 1 0 0 1 1: Delay of 19/ 32 times the PCLKA period is applied. 1 0 1 0 0: Delay of 20/ 32 times the PCLKA period is applied. 1 0 1 0 1: Delay of 21/ 32 times the PCLKA period is applied. 1 0 1 1 0: Delay of 22/ 32 times the PCLKA period is applied. 1 0 1 1 1: Delay of 23/ 32 times the PCLKA period is applied. 1 1 0 0 0: Delay of 24/ 32 times the PCLKA period is applied. 1 1 0 0 1: Delay of 25/ 32 times the PCLKA period is applied. 1 1 0 1 0: Delay of 26/ 32 times the PCLKA period is applied. 1 1 0 1 1: Delay of 27/ 32 times the PCLKA period is applied. 1 1 1 0 0: Delay of 28/ 32 times the PCLKA period is applied. 1 1 1 0 1: Delay of 29/ 32 times the PCLKA period is applied. 1 1 1 1 0: Delay of 30/ 32 times the PCLKA period is applied. 1 1 1 1 1: Delay of 31/ 32 times the PCLKA period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDLYRB sets the delay time to be applied to rising edges of output signals on the GTIOCB pin. On the timing for the transfer of settings, see section 24.2.39, GTIOC Rising Output Delay Register (GTDLYRA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.41, GTIOCB Rising Output Delay Register (GTDLYRB), and section 24.2.42, GTIOCB Falling Output Delay Register (GTDLYFB).

24.2.42 GTIOCB Falling Output Delay Register (GTDLYFB)

Address(es): GPT0.GTDLYFB 000C 232Ah, GPT1.GTDLYFB 000C 232Eh, GPT2.GTDLYFB 000C 2332h, GPT3.GTDLYFB 000C 2336h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0 to b4	DLY[4:0]	GTIOCB Output Falling Delay Time Setting	b4 b0 0 0 0 0 0: No delay on falling edges 0 0 0 0 1: Delay of 1/ 32 times the PCLKA period is applied. 0 0 0 1 0: Delay of 2/ 32 times the PCLKA period is applied. 0 0 0 1 1: Delay of 3/ 32 times the PCLKA period is applied. 0 0 1 0 0: Delay of 4/ 32 times the PCLKA period is applied. 0 0 1 0 1: Delay of 5/ 32 times the PCLKA period is applied. 0 0 1 1 0: Delay of 6/ 32 times the PCLKA period is applied. 0 0 1 1 1: Delay of 7/ 32 times the PCLKA period is applied. 0 1 0 0 0: Delay of 8/ 32 times the PCLKA period is applied. 0 1 0 0 1: Delay of 9/ 32 times the PCLKA period is applied. 0 1 0 1 0: Delay of 10/ 32 times the PCLKA period is applied. 0 1 0 1 1: Delay of 11/ 32 times the PCLKA period is applied. 0 1 1 0 0: Delay of 12/ 32 times the PCLKA period is applied. 0 1 1 0 1: Delay of 13/ 32 times the PCLKA period is applied. 0 1 1 1 0: Delay of 14/ 32 times the PCLKA period is applied. 0 1 1 1 1: Delay of 15/ 32 times the PCLKA period is applied. 1 0 0 0 0: Delay of 16/ 32 times the PCLKA period is applied. 1 0 0 0 1: Delay of 17/ 32 times the PCLKA period is applied. 1 0 0 1 0: Delay of 18/ 32 times the PCLKA period is applied. 1 0 0 1 1: Delay of 19/ 32 times the PCLKA period is applied. 1 0 1 0 0: Delay of 20/ 32 times the PCLKA period is applied. 1 0 1 0 1: Delay of 21/ 32 times the PCLKA period is applied. 1 0 1 1 0: Delay of 22/ 32 times the PCLKA period is applied. 1 0 1 1 1: Delay of 23/ 32 times the PCLKA period is applied. 1 1 0 0 0: Delay of 24/ 32 times the PCLKA period is applied. 1 1 0 0 1: Delay of 25/ 32 times the PCLKA period is applied. 1 1 0 1 0: Delay of 26/ 32 times the PCLKA period is applied. 1 1 0 1 1: Delay of 27/ 32 times the PCLKA period is applied. 1 1 1 0 0: Delay of 28/ 32 times the PCLKA period is applied. 1 1 1 0 1: Delay of 29/ 32 times the PCLKA period is applied. 1 1 1 1 0: Delay of 30/ 32 times the PCLKA period is applied. 1 1 1 1 1: Delay of 31/ 32 times the PCLKA period is applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTDLYFB sets the delay time to be applied to falling edges of output signals on the GTIOCB pin. On the timing for the transfer of settings, see section 24.2.39, GTIOC Rising Output Delay Register (GTDLYRA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.40, GTIOCA Falling Output Delay Register (GTDLYFA), section 24.2.41, GTIOCB Rising Output Delay Register (GTDLYRB), and section 24.2.42, GTIOCB Falling Output Delay Register (GTDLYFB).

24.3 Operation

24.3.1 Basic Operation

Each channel has a 16-bit timer which performs up-counting, down-counting, and up-/down-counting.
The cycle is controlled by compare register GTPR.
When the counter value matches the value in GTCCRA or GTCCRB, the output from the corresponding pin GTIOCnA or GTIOCnB can be changed (n = 0 to 7). GTCCRA or GTCCRB can be used as an input capture register with the GTIOCnA or GTIOCnB pin as the input.
GTCCRC and GTCCRD can function as buffer registers of GTCCRA, and GTCCRE and GTCCRF can function as buffer registers of GTCCRB.

24.3.1.1 Counter Operation

(1) Periodic Count Operation (in Up-Count Operation)

The counter in each channel starts up-count operation when the corresponding CST bit in GTSTR is set to 1. When the GTCNT value matches the GTPR value (overflow), the GTST.TCFPO flag is set to 1. If the GTINTAD.GTINTPR[0] bit is 1 at this time, a GTCIV interrupt is requested. After GTCNT overflows, up-count operation is resumed from 0000h.
Figure 24.2 shows an example of periodic count operation in up-count operation.

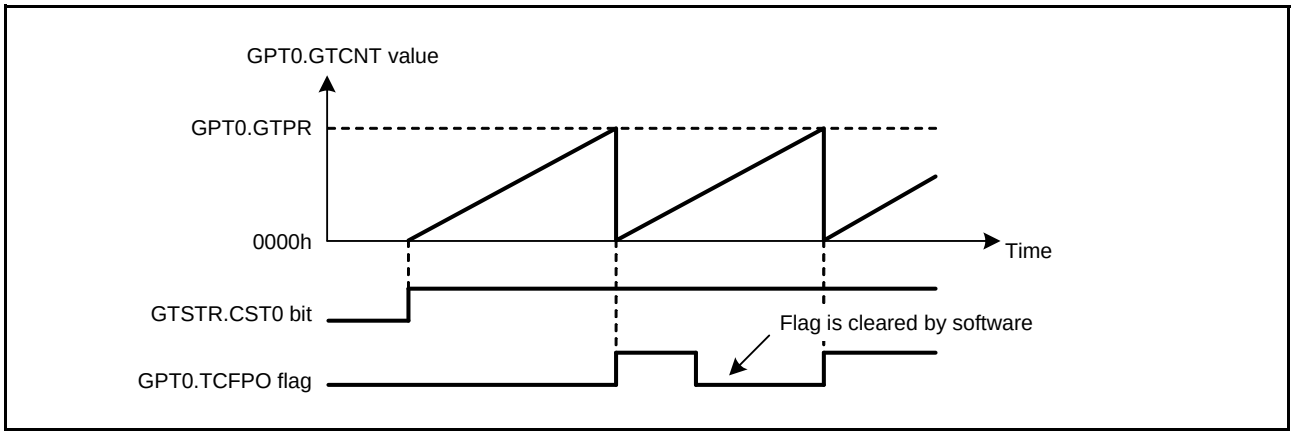


Figure 24.2 Example of Periodic Count Operation (in Up-Count Operation)

Figure 24.3 shows an example for setting periodic count operation in up-count operation.

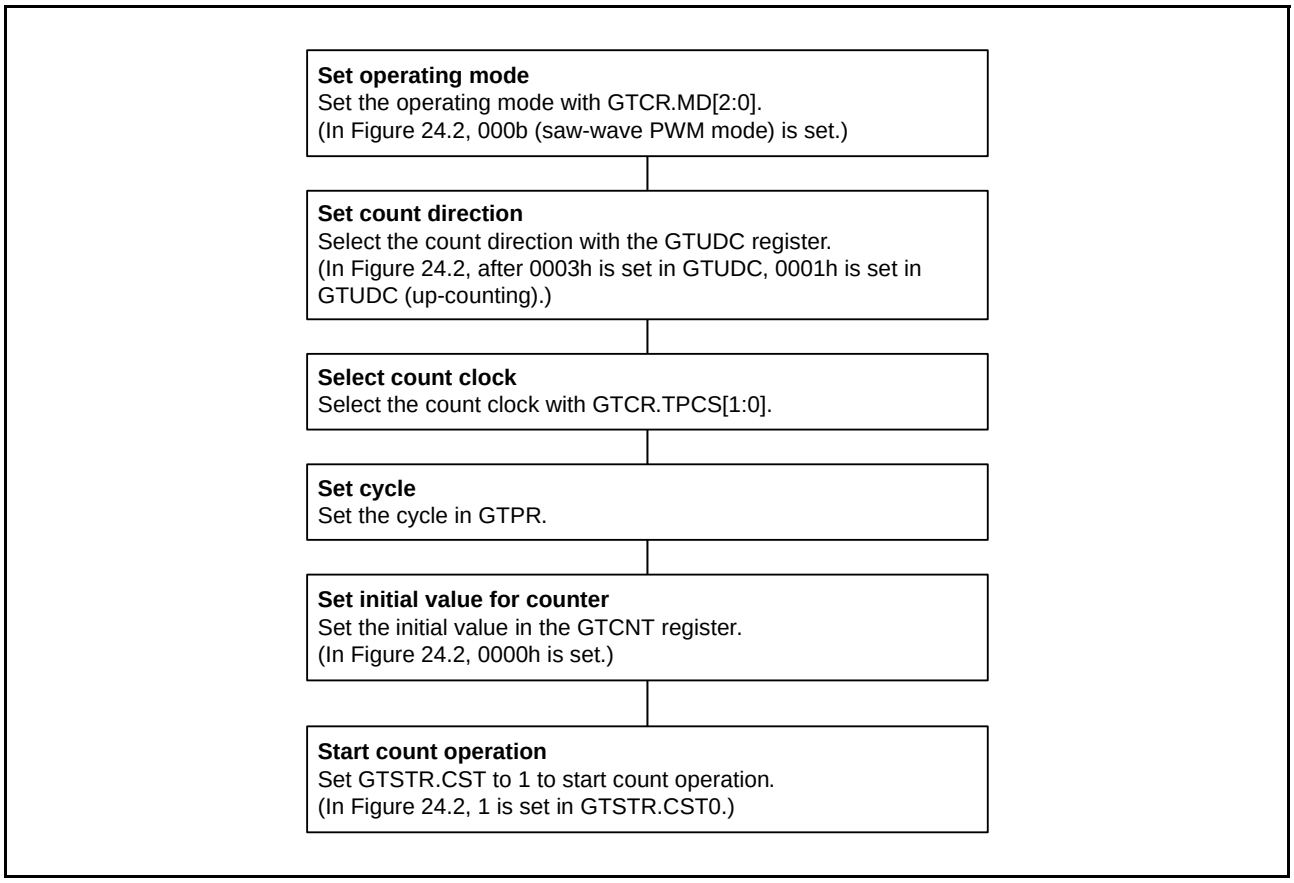


Figure 24.3 Example for Setting Periodic Count Operation (in Up-Count Operation)

(2) Periodic Count Operation (in Down-Count Operation)

The counter in each channel can perform down-count operation by setting GTUDC.
When GTCNT reaches 0 (underflow), the GTST.TCFPU flag is set to 1. If the GTINTAD.GTINTPR[1] bit is 1 at this time, a GTCIV interrupt is requested. After the GTCNT counter underflows, down-count operation is resumed from the GTPR value.
Figure 24.4 shows an example of periodic count operation in down-count operation.

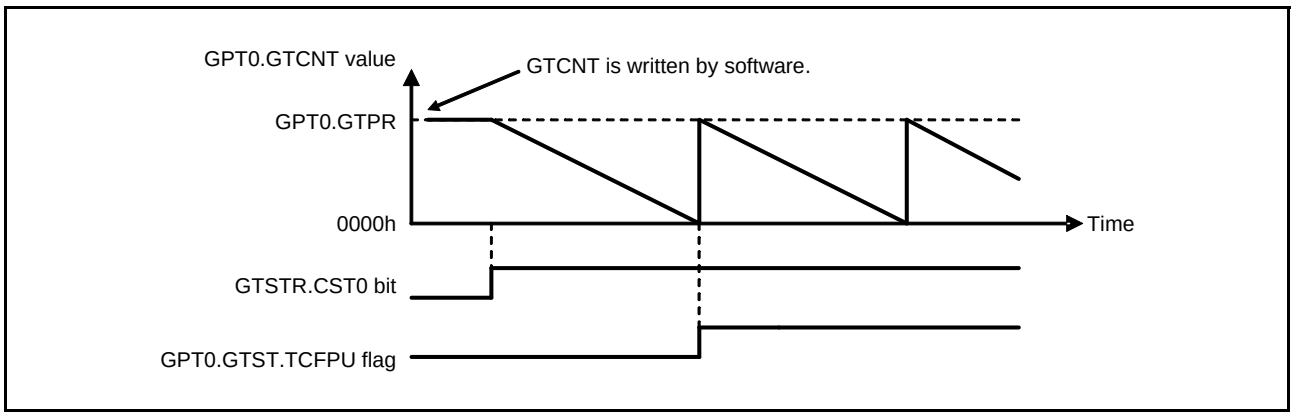


Figure 24.4 Example of Periodic Count Operation (in Down-Count Operation)

Figure 24.5 shows an example for setting periodic count operation in down-count operation.

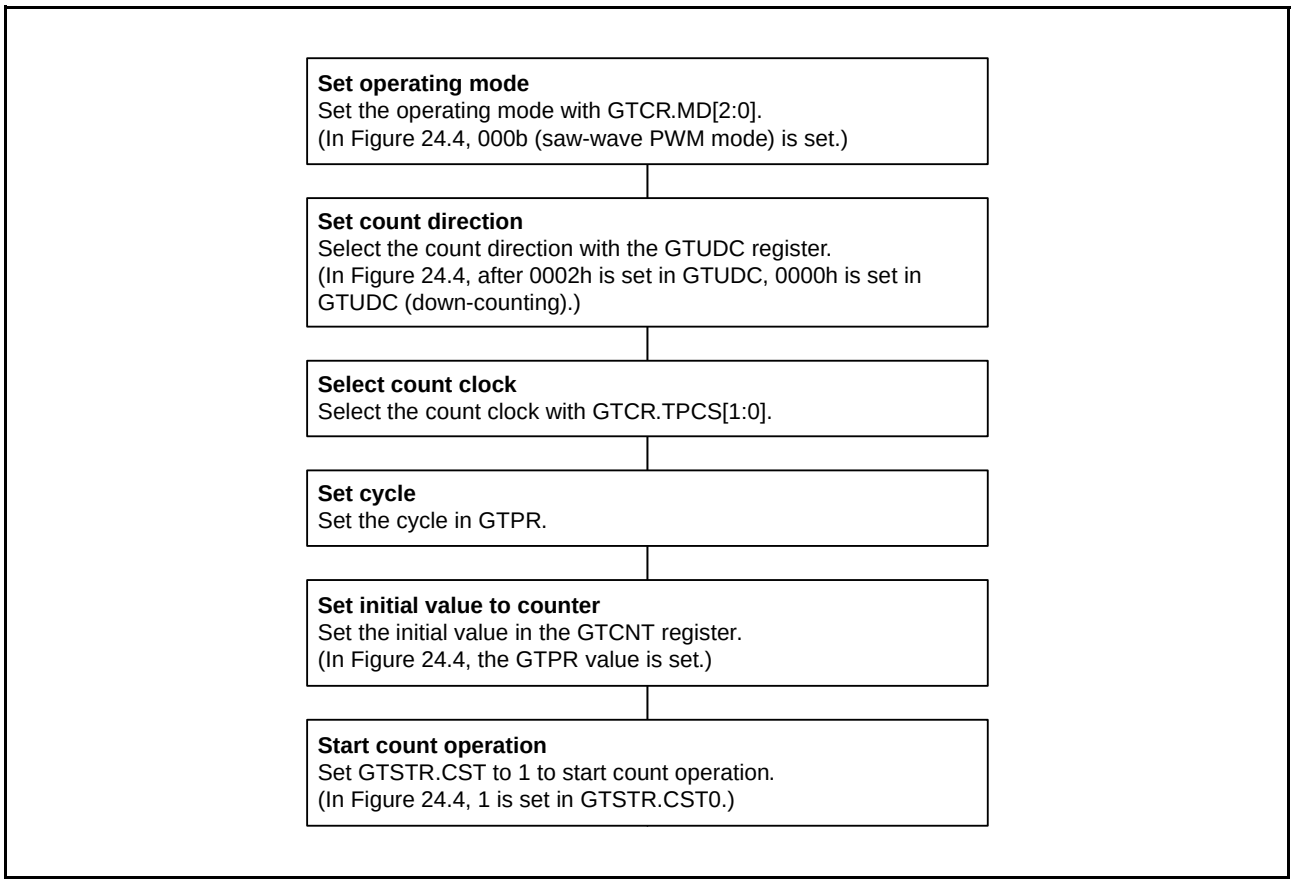


Figure 24.5 Example for Setting Periodic Count Operation (in Down-Count Operation)

24.3.1.2 Waveform Output by Compare Match

When the GPTn.GTCNT counter value matches GTPn.GTCCRA or GTPn.GTCCRB, the GPT can output low or high or toggles output from the corresponding GTIOCnA or GTIOCnB output pin (n = channel number).
In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the “cycle end” which is determined by GPTn.GTPR.
The cycle end is:

- For saw waves in up-count operation: When GPTn.GTPR = GPTn.GTCNT (overflow)
- For saw waves in down-count operation: When GPTn.GTCNT = 0 (underflow)
- For triangle waves: When GPTn.GTCNT = 0 (trough)

(1) Low Output and High Output

Figure 24.6 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.
In this example, up-count operation is performed in channel 0, and settings have been made so that high is output from the GTIOC0A pin by a GPT0.GTCCRA compare match, and low is output from the GTIOC0B pin by a GPT0n.GTCCRB compare match. The pin level does not change when the specified level and pin level match.

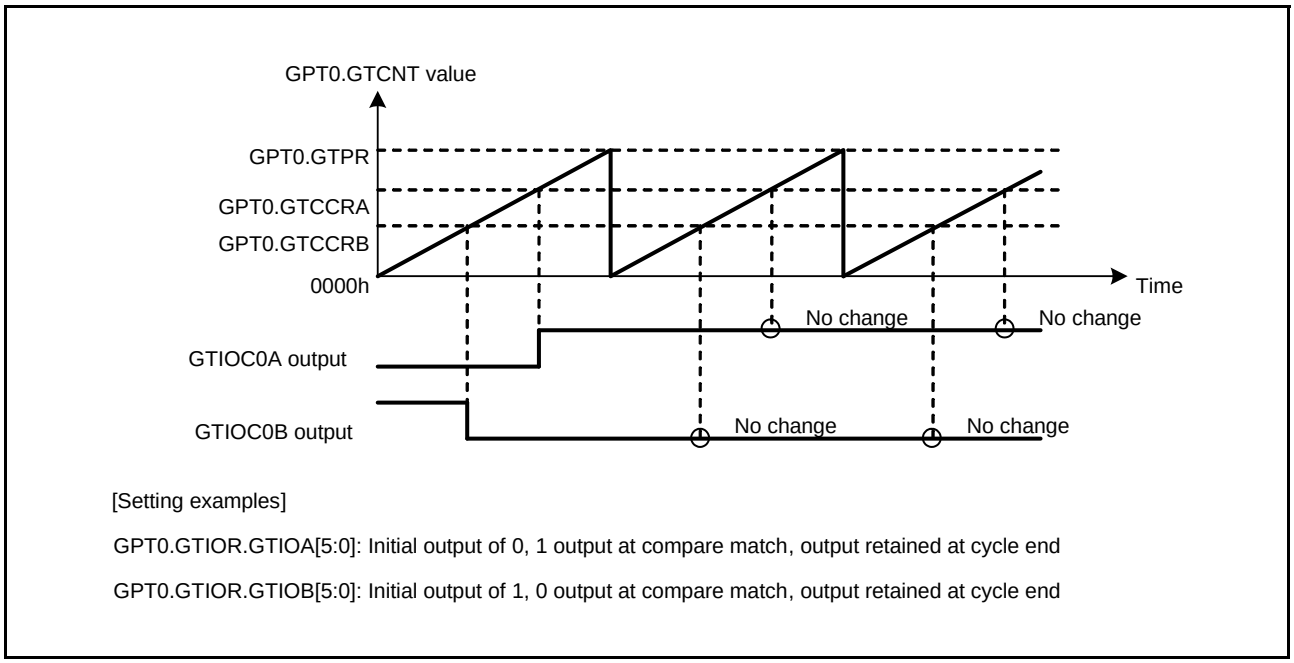


Figure 24.6 Example of Low Output and High Output Operation

Figure 24.7 shows an example for setting low output and high output operation

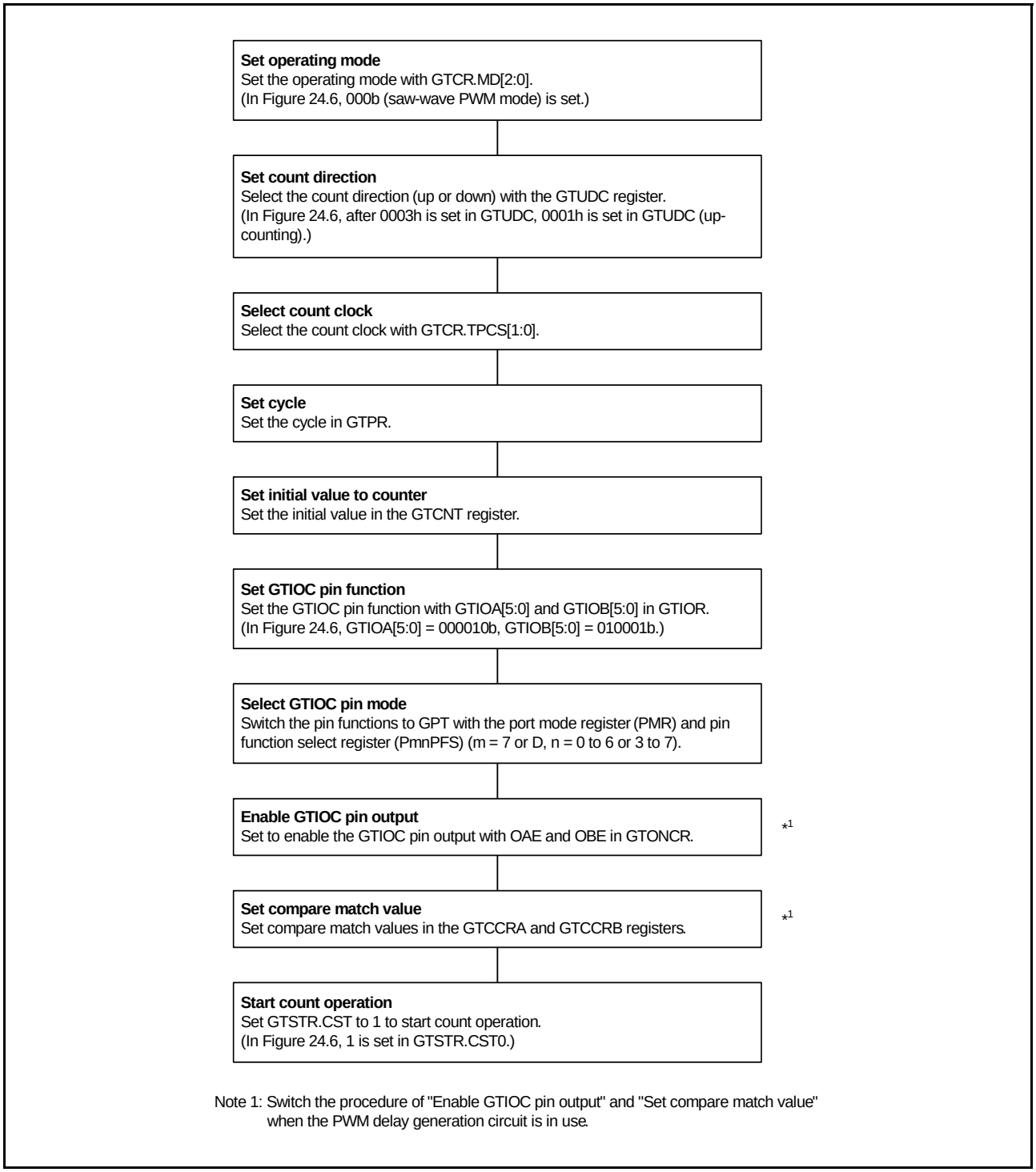
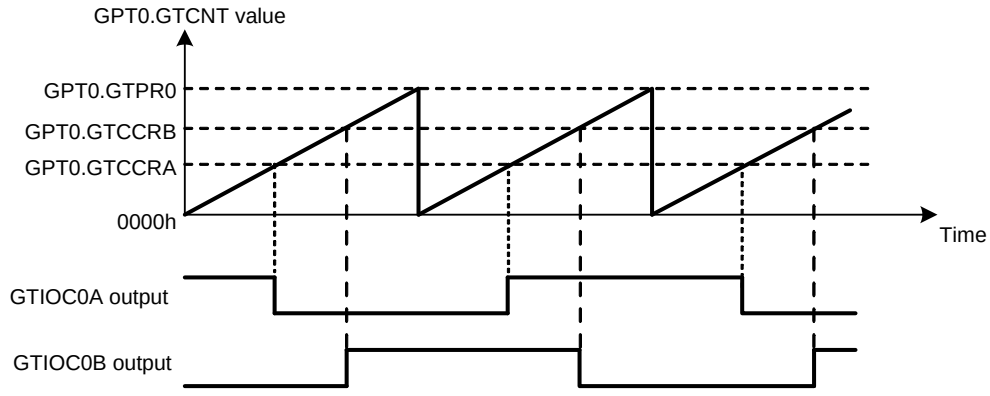


Figure 24.7 Example for Setting Low Output and High Output Operation

(2) Toggled Output

Figure 24.8 and Figure 24.9 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB. In Figure 24.8, up-count operation is performed in channel 0, and settings have been made so that the GTIOC0A pin output by a GPT0.GTCCRA compare match and GTIOC0B pin output by a GPT0n.GTCCRB compare match are toggled.

In Figure 24.9, up-count operation is performed in channel 0, and settings have been made so that the GTIOC0A output is toggled by a compare match of GPT0.GTCCRA and the GTIOC0B output is toggled at the cycle end.

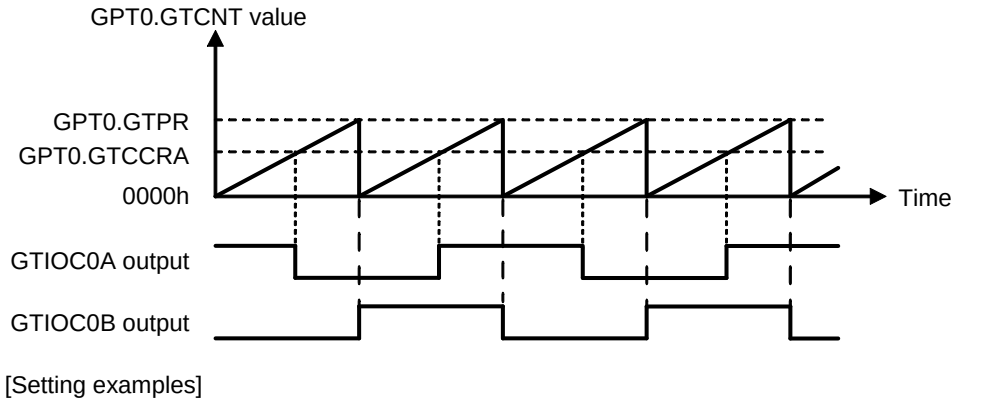


[Setting examples]

GPT0.GTIOR.GTIOA[5:0]: Initial output of 1, toggle output at compare match, output retained at cycle end

GPT0.GTIOR.GTIOB[5:0]: Initial output of 0, toggle output at compare match, output retained at cycle end

Figure 24.8 Example of Toggled Output Operation (1)



[Setting examples]

GPT0.GTIOR.GTIOA[5:0]: Initial output of 1, toggle output at compare match, output retained at cycle end

GPT0.GTIOR.GTIOB[5:0]: Initial output of 0, output retained at compare match, toggle output at cycle end

Figure 24.9 Example of Toggled Output Operation (2)

Figure 24.10 shows an example for setting toggled output operation

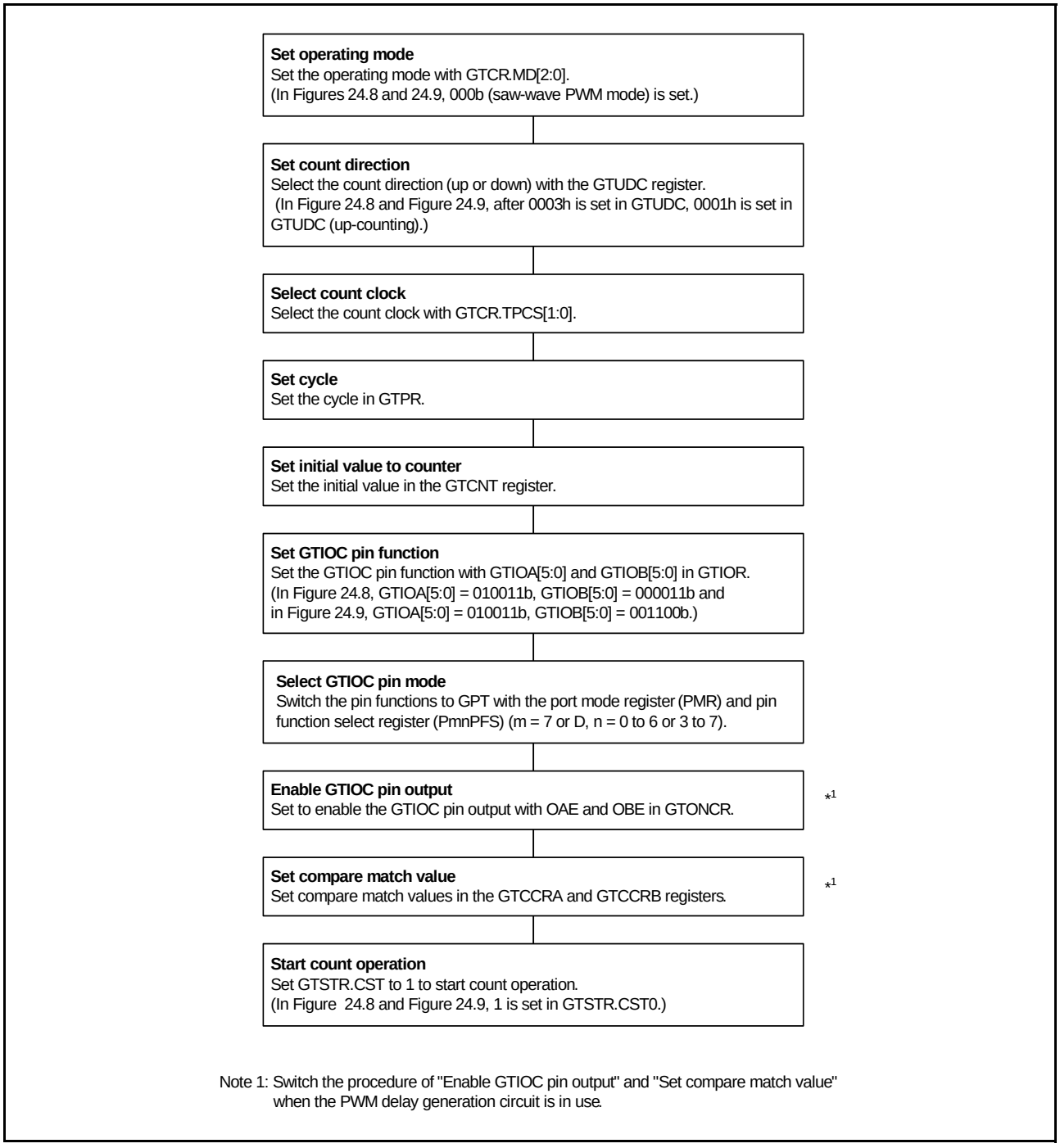


Figure 24.10 Example for Setting Toggled Output Operation

24.3.1.3 Input Capture Function

The GPTn.GTCNT counter value can be transferred to either GPTn.GTCCRA or GPTn.GTCCRB on detection of the input edge of the GTIOCnA input pin or GTIOCnB input pin, respectively (n: channel number). The rising edge, falling edge, or both edges can be selected as the detection edge.

Figure 24.11 shows an example of the input capture function. In this example, up-count operation is performed on channel 0, and settings have been made so that an input capture is performed at both edges of the GTIOC0A input pin and at the rising edge of the GTIOC0B input pin.

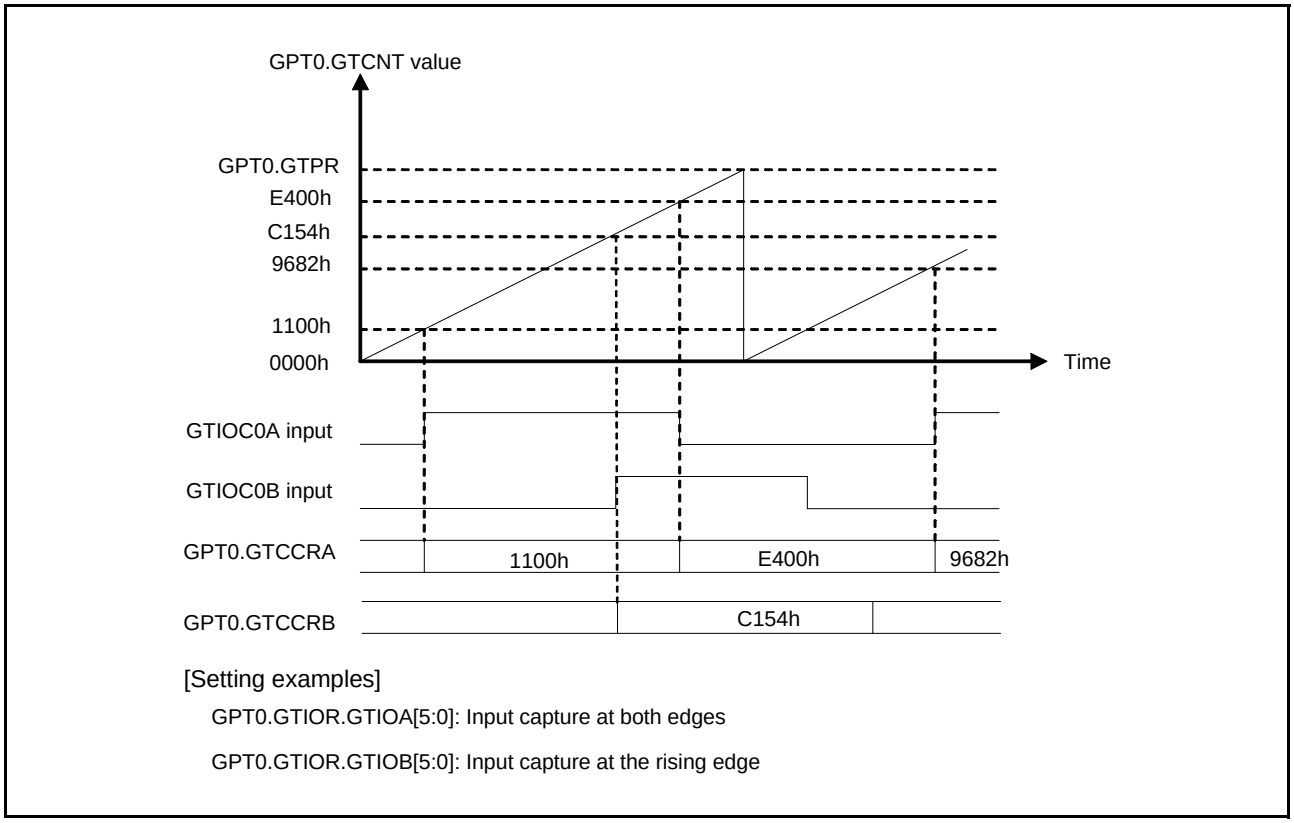


Figure 24.11 Example of Input Capture Operation

Figure 24.12 shows an example for setting input capture operation.

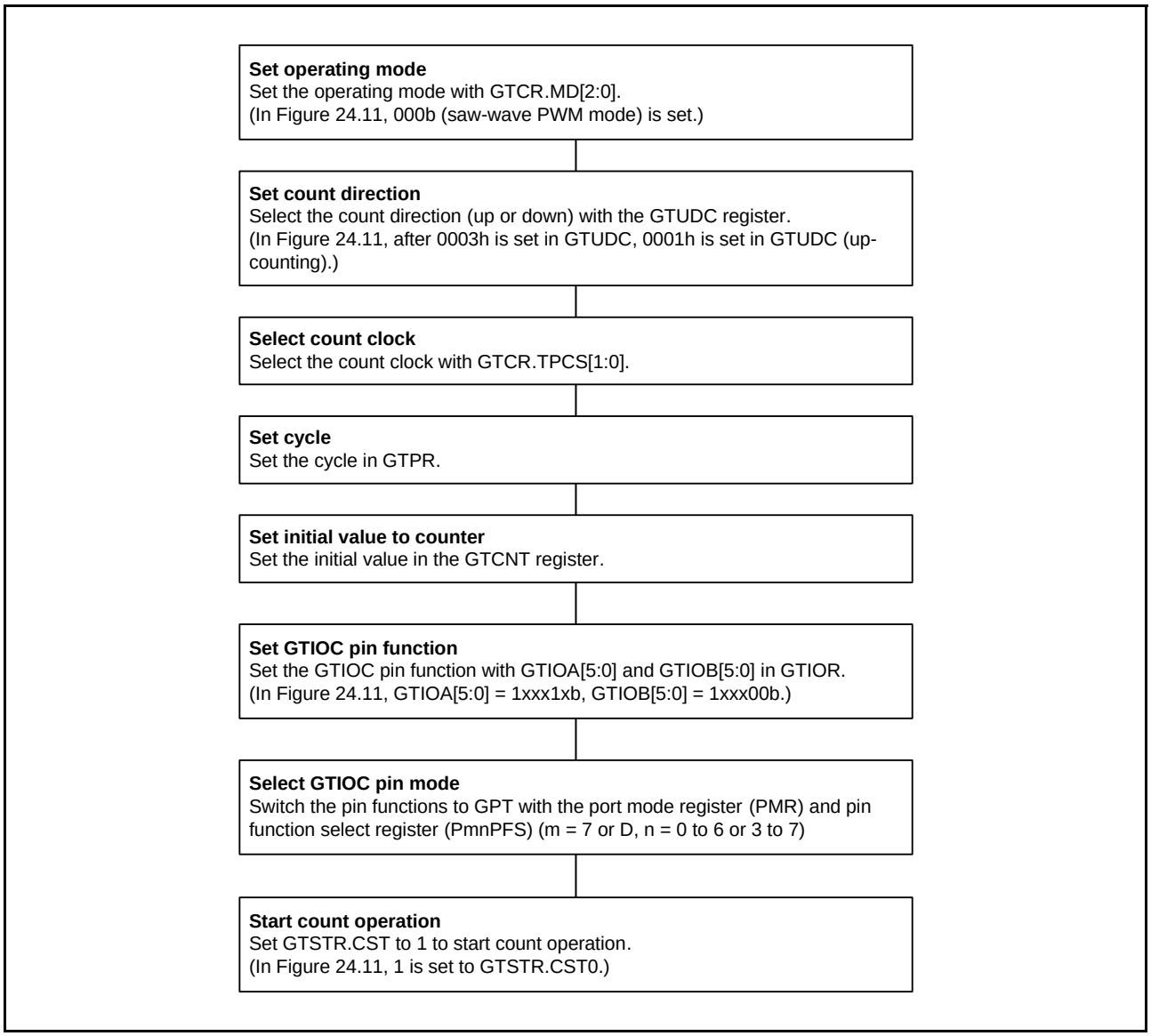


Figure 24.12 Example for Setting Input Capture Operation

24.3.2 Buffer Operation

The following buffer operation can be set with GTBER.

- Buffer operation with GTCCRA, GTCCRC, and GTCCRD used together
- Buffer operation with GTCCRB, GTCCRE, and GTCCRF used together
- Buffer operation with GTPR, GTPBR, and GTPDBR used together
- Buffer operation with GTADTRA, GTADTBRA, and GTADTDBRA used together
- Buffer operation with GTADTRB, GTADTBRB, and GTADTDBRB used together

The following buffer operation can be set with GTDTCR.

- Buffer operation with GTDVU and GTDBU used together
- Buffer operation with GTDVU and GTDBD used together

24.3.2.1 GTPR Register Buffer Operation

GTPBR can function as a buffer register for GTPR, and GTPDBR can function as a buffer register for GTPBR (double-buffer register for GTPR).

Setting of buffered operation is prohibited when down-counting is used in saw-wave generation.

The buffer transfer is performed on an overflow or counter clearing in saw-wave mode, and at the troughs in triangle-wave mode.

To set GTPR to function as double buffer, set GTBER.PR[1:0] to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.

Figure 24.13 to Figure 24.14 show examples of GTPR buffer operation and Figure 24.15 shows an example for setting GTPR buffer operation.

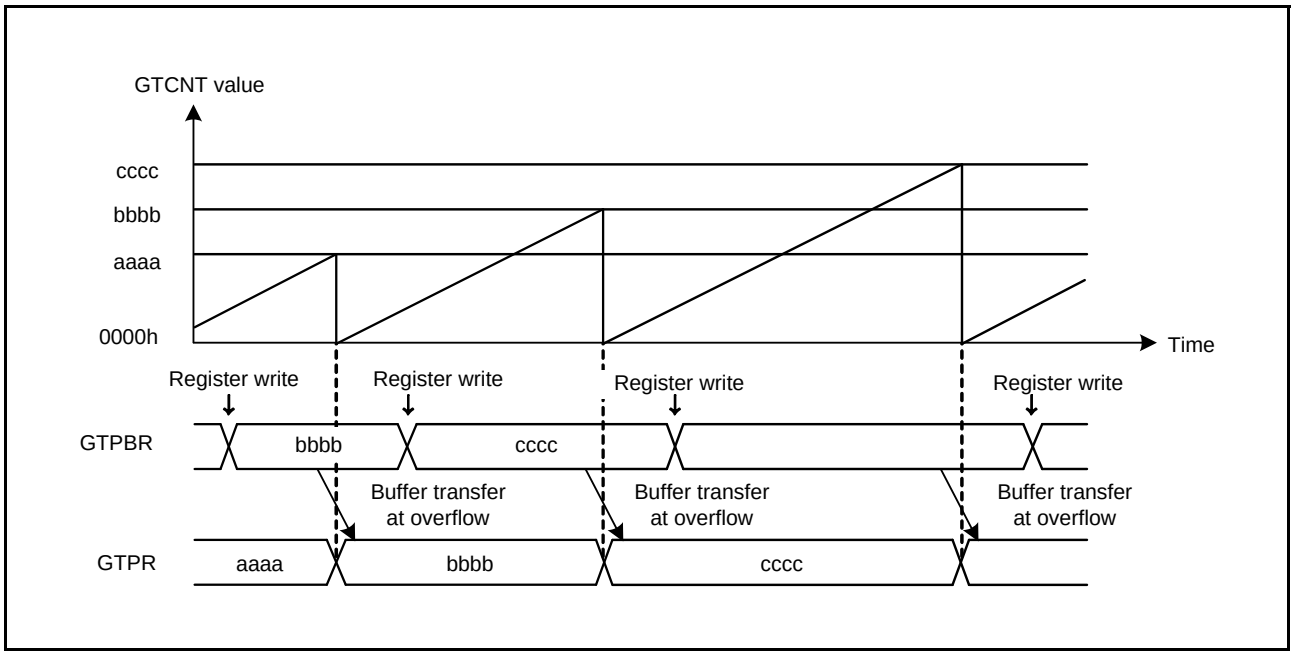


Figure 24.13 Example of GTPR Buffer Operation (Saw Waves in Up-Count Operation)

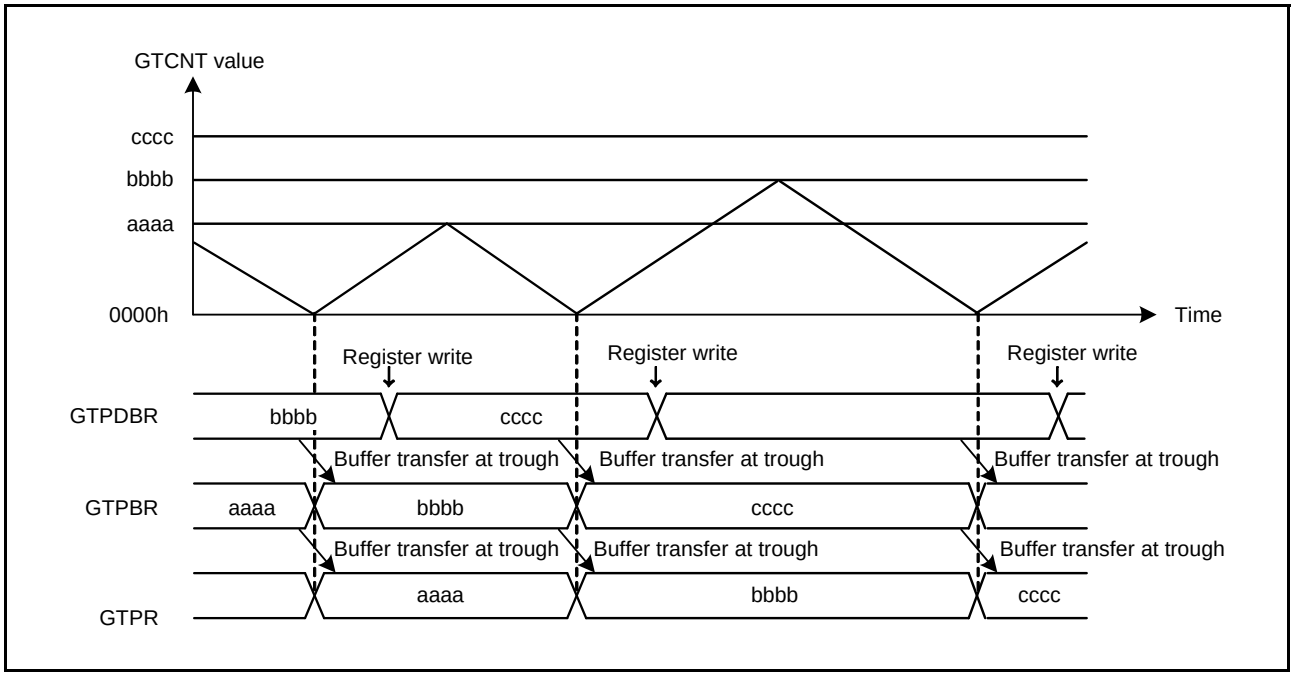


Figure 24.14 Example of GTPR Double Buffer Operation (Triangle Waves)

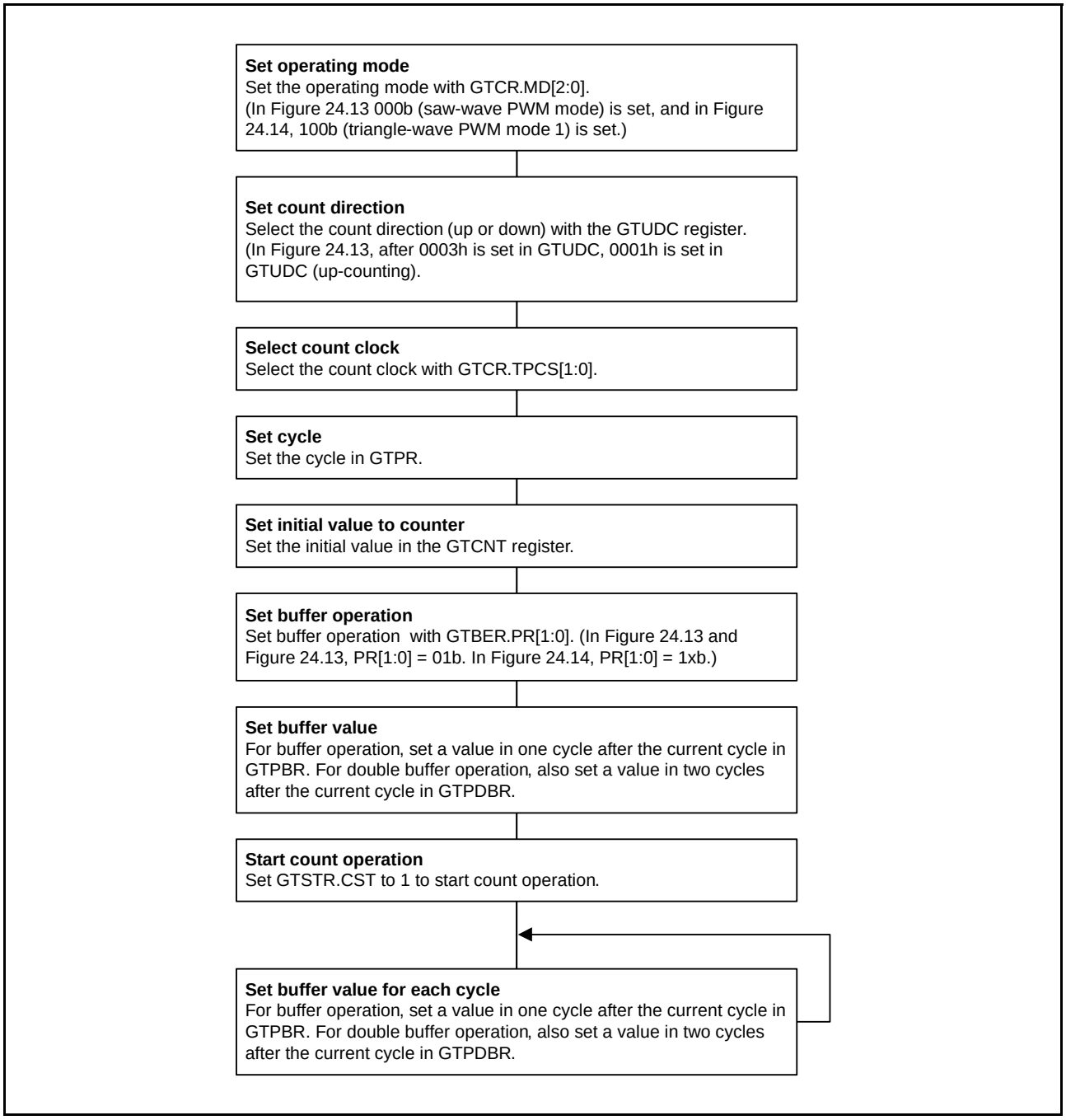


Figure 24.15 Example for Setting GTPR Buffer Operation

24.3.2.2 Buffer Operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).
To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.

(1) When GTCCRA or GTCCRB Functions as Output Compare Register

Buffer transfer is performed at an overflow (during up-count operation) or an underflow (during down-count operation) in saw-wave mode, and at both crest and trough in triangle-wave mode.
Figure 24.16 to Figure 24.18 show examples of GTCCRA and GTCCRB buffer operation and Figure 24.19 shows an example for setting GTCCRA and GTCCRB buffer operation.

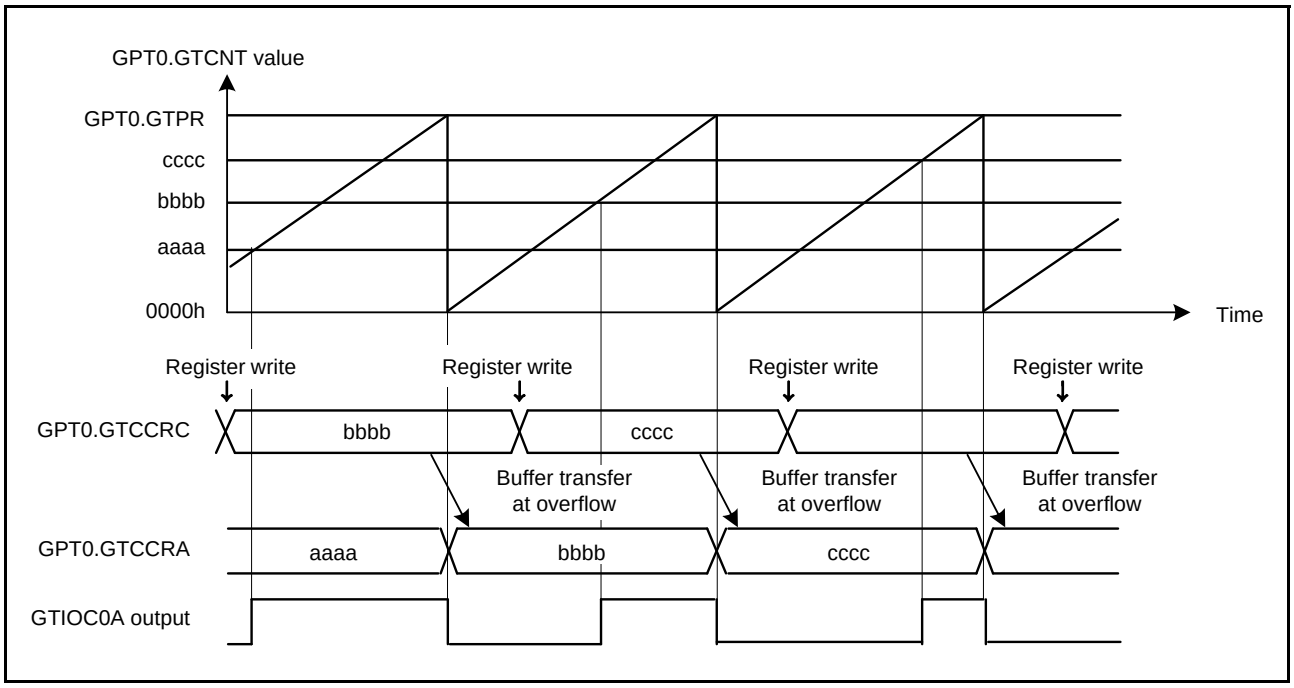


Figure 24.16 Example of GTCCRA and GTCCRB Buffer Operation (Output Compare, Saw Waves in Up-Count Operation, High Output at GTCCRA Compare Match, Low Output at Cycle End)

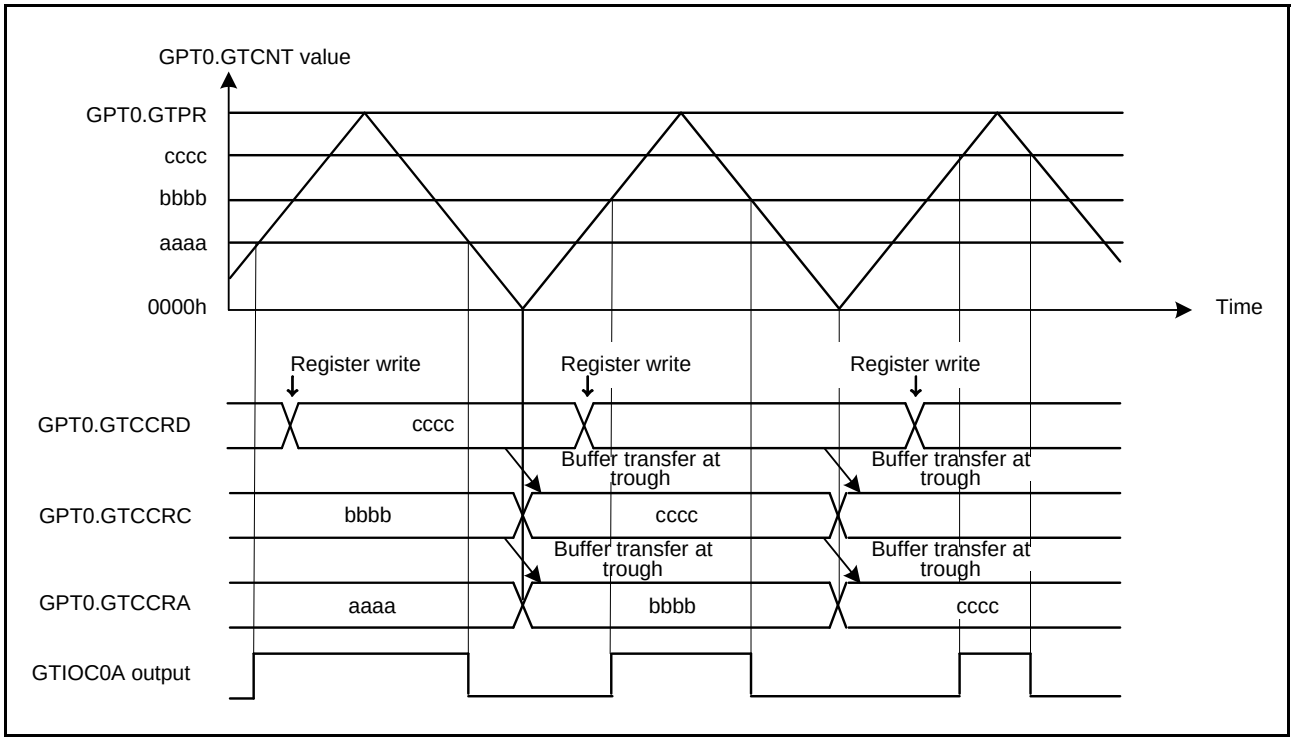


Figure 24.17 Example of GTCCRA and GTCCRB Double Buffer Operation (Output Compare, Triangle Waves, Buffer Operation at Trough, Toggle Output at GTCCRA Compare Match, Output Retained at Cycle End)

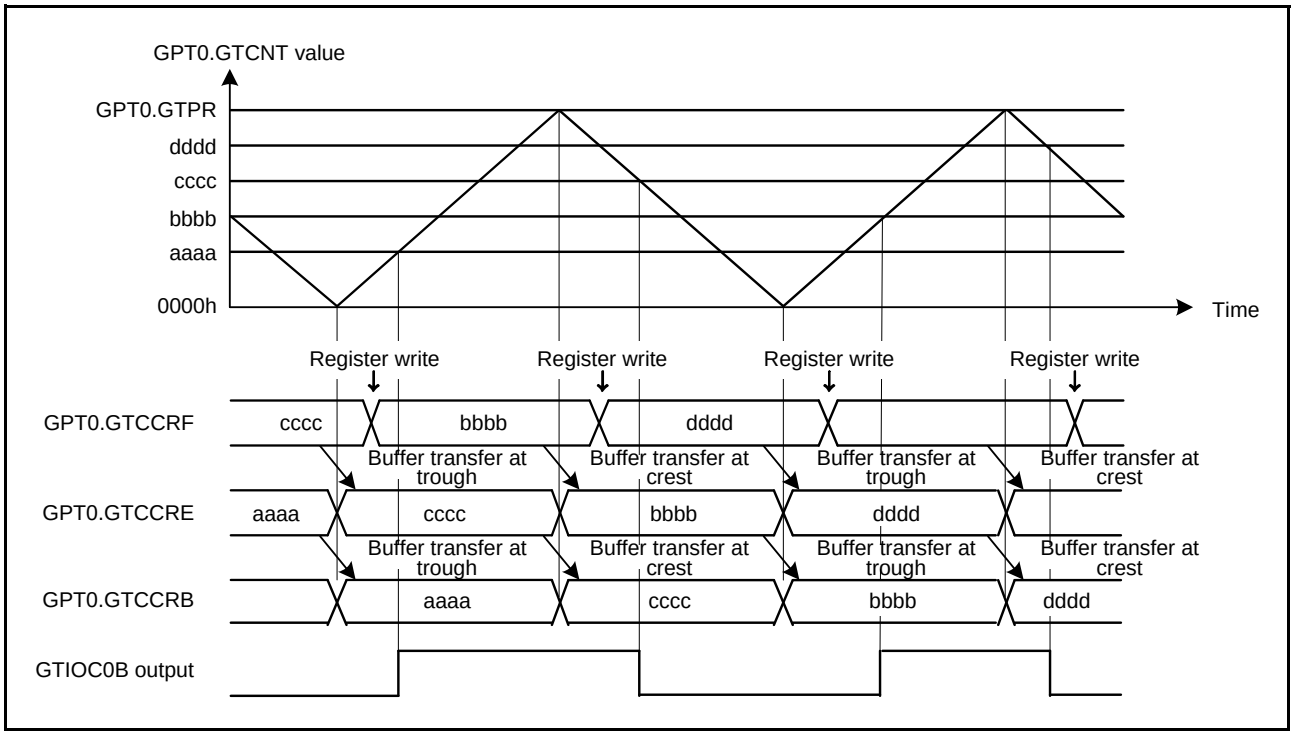


Figure 24.18 Example of GTCCRA and GTCCRB Double Buffer Operation (Output Compare, Triangle Waves, Buffer Operation at Both Troughs and Crests, Toggle Output at GTCCRB Compare Match, Output Retained at Cycle End)

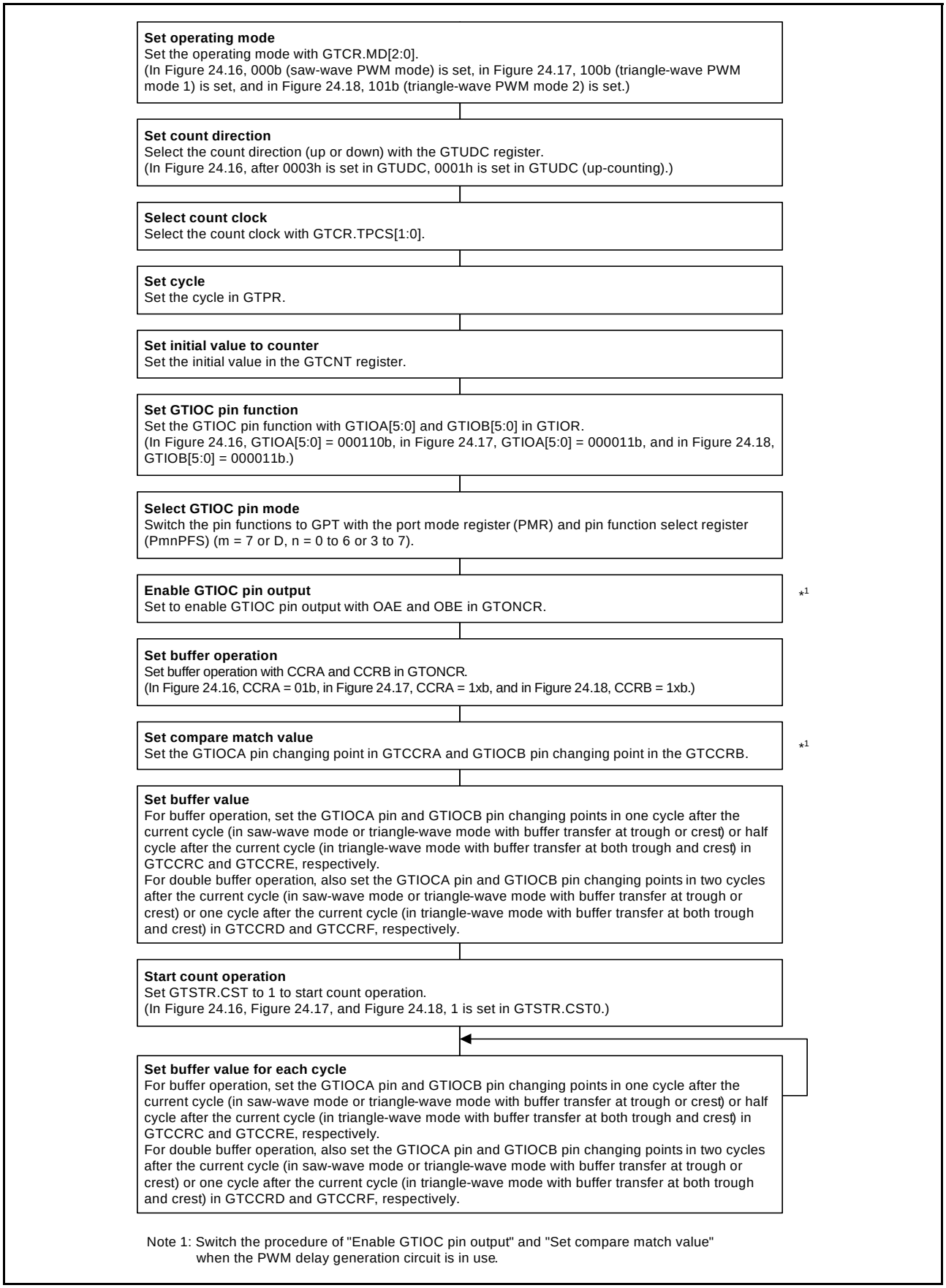


Figure 24.19 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Output Compare)

(2) When GTCCRA or GTCCRB Functions as Input Capture Register

Buffer transfer is performed at a point when an input capture is generated. When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to buffer registers.

Figure 24.20 and Figure 24.21 show examples of GTCCRA and GTCCRB buffer operation and Figure 24.22 shows an example for setting GTCCRB buffer operation.

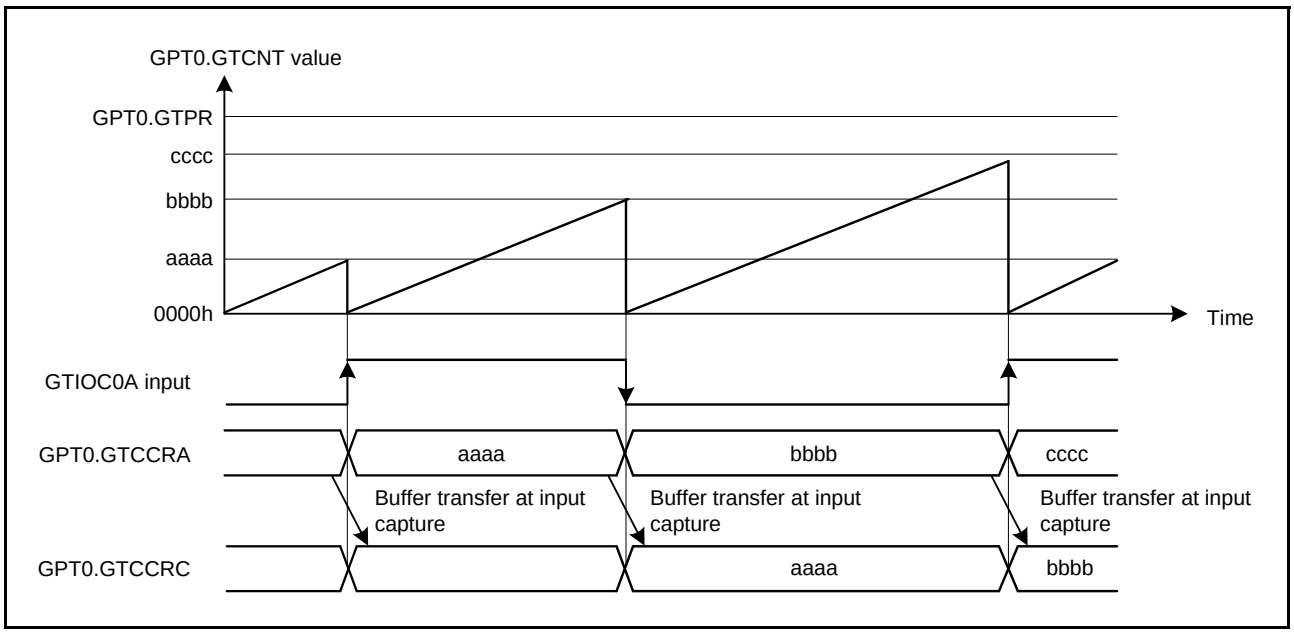


Figure 24.20 Example of GTCCRA and GTCCRB Buffer Operation (Input Capture at Both Edges of GTIOC0A Input, Saw Waves in Up-Count Operation, GTCNT Counter Cleared at GTCCRA Input Capture)

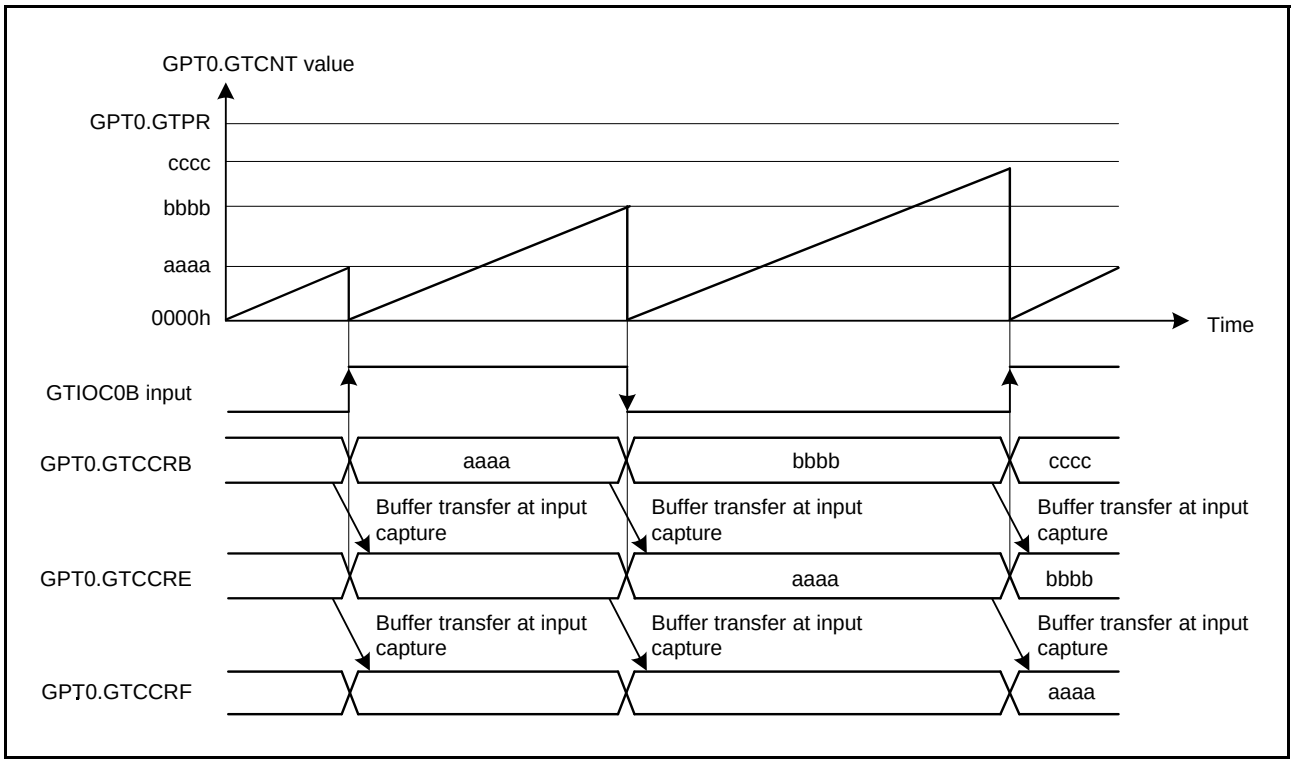


Figure 24.21 Example of GTCCRA and GTCCRB Double Buffer Operation (Input Capture at Both Edges of GTIOC0B Input, Saw Waves in Up-Count Operation, GTCNT Counter Cleared at GTCCRB Input Capture)

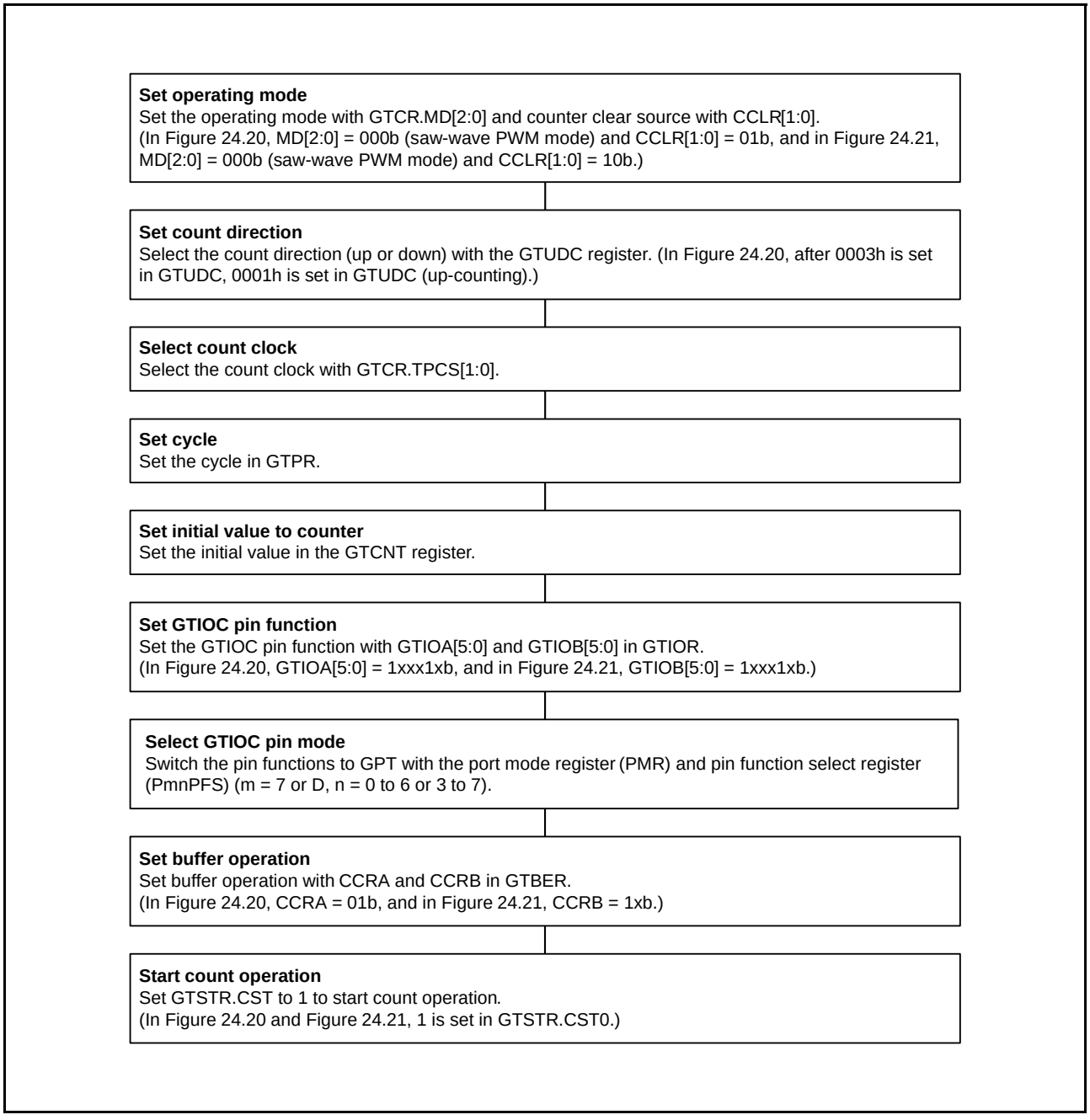


Figure 24.22 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Input Capture)

24.3.2.3 Buffer Operation for GTADTRA and GTADTRB

GTADTBRA can function as the GTADTRA buffer register and GTADTDBRA can function as the GTADTBRA buffer register (double-buffer register for GTADTRA). Similarly, GTADTBRB can function as the GTADTRB buffer register and GTADTDBRB can function as the GTADTBRB buffer register (double-buffer register for GTADTRB).
To set GTADTRA or GTADTRB to function as a double buffer, set GTBER.ADTDA or GTBER.ADTDB to 1. For single buffer operation, set 0. Not to function as buffer, set GTBER.ADTTA[1:0] or GTBER.ADTTB[1:0] to 00b.
The buffer transfer timing can be set with the GTBER.ADTTA[1:0] bits. For saw waves, overflows (during up-count operation) or underflows (during down-count operation) can be selected. For triangle waves, crests are selected when GTBER.ADTTA[1:0] = 01b, troughs are selected when GTBER.ADTTA[1:0] = 10b, and both crests and troughs are selected when GTBER.ADTTA[1:0] = 00b.
Figure 24.23 to Figure 24.25 show examples of GTADTRA and GTADTRB buffer operation and Figure 24.26 shows an example for setting GTADTRA and GTADTRB buffer operation.

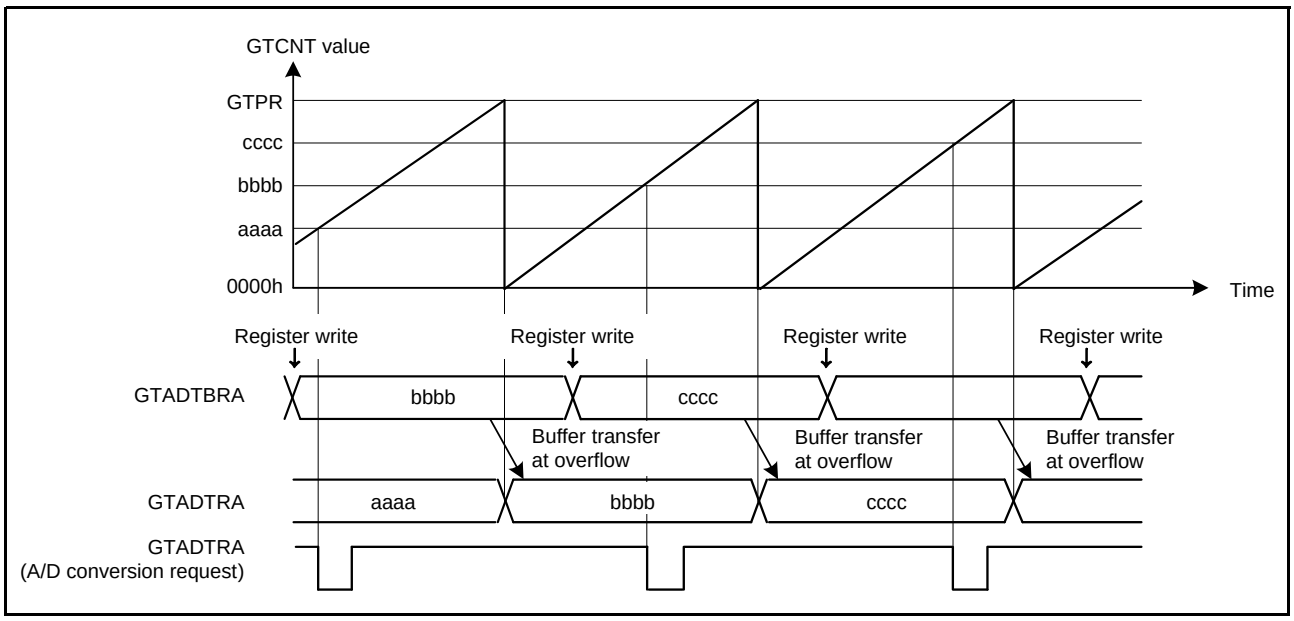


Figure 24.23 Example of GTADTRA and GTADTRB Buffer Operation (Saw Waves in Up-Count Operation, A/D Converter Start Request Generated by Up-Counting)

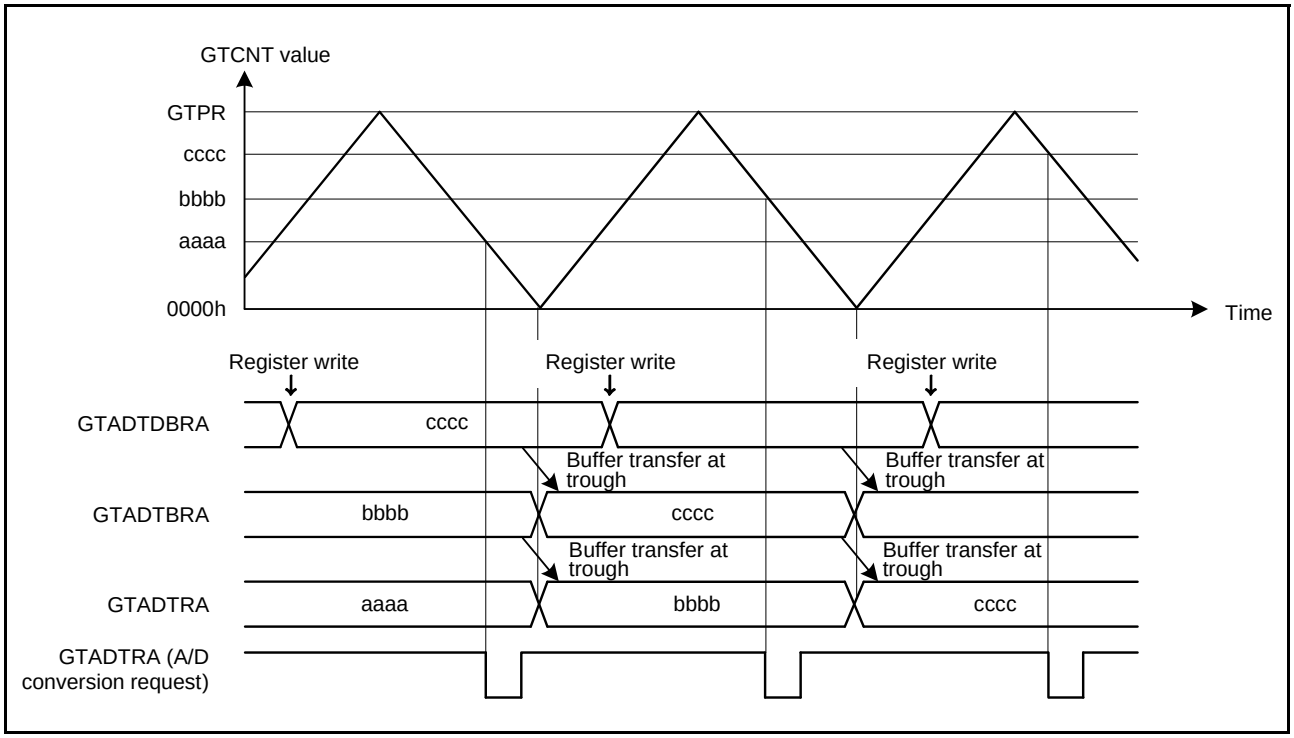


Figure 24.24 Example of GTADTRA and GTADTRB Double Buffer Operation (Triangle Waves, Buffer Transfer at Troughs, A/D Converter Start Request Generated by Down-Counting)

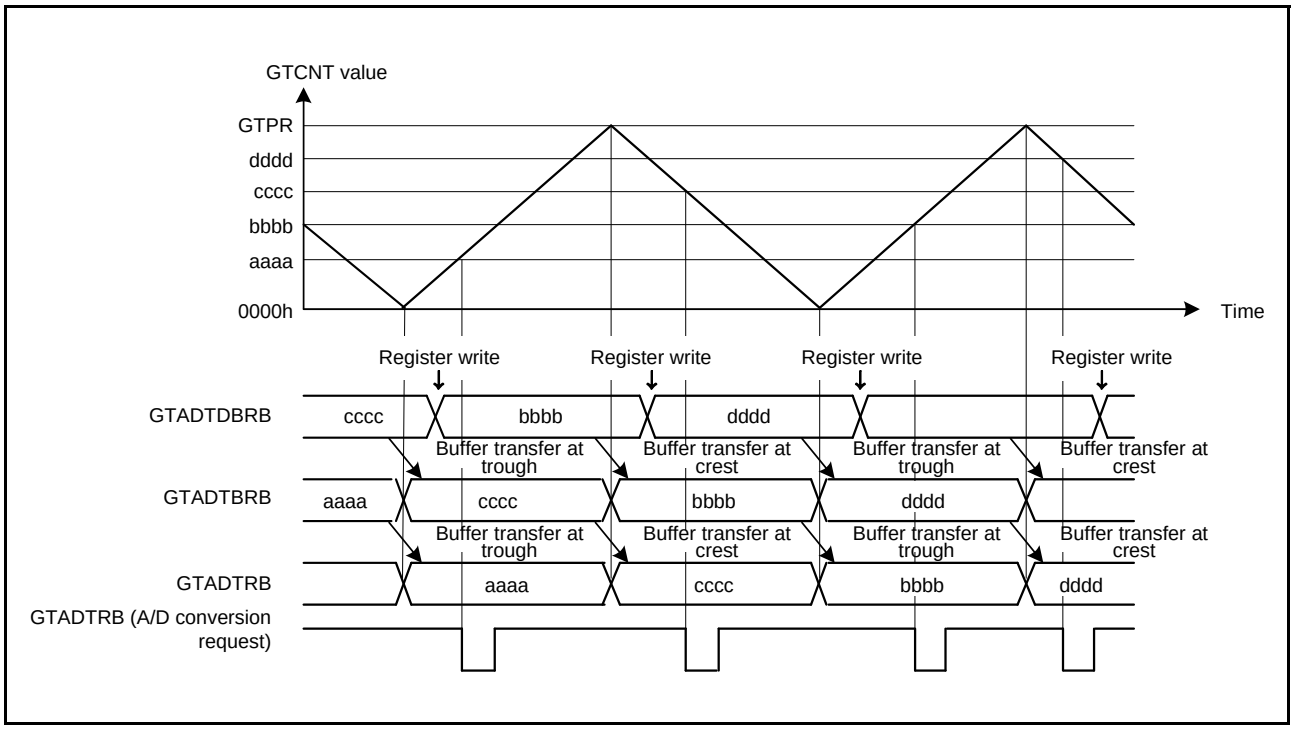


Figure 24.25 Example of GTADTRA and GTADTRB Double Buffer Operation (Triangle Waves, Buffer Transfer at Both Troughs and Crests, A/D Converter Start Request Generated by Both Up- and Down-Counting)

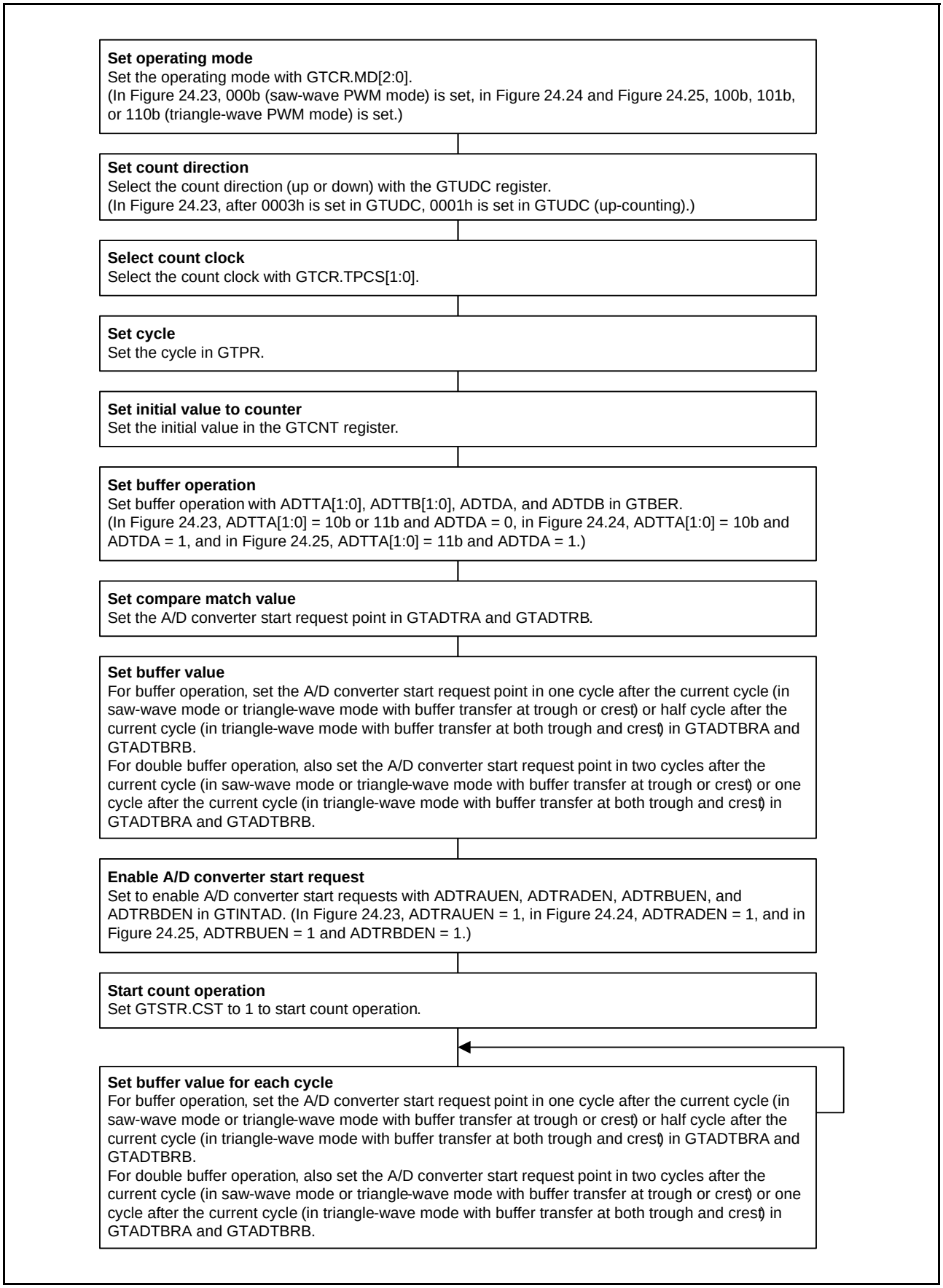


Figure 24.26 Example for Setting GTADTRA and GTADTRB Buffer Operation

24.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA pin or GTIOCnB pin by a compare match between the GPTn.GTCNT counter and GPTn.GTCCRA or GPTn.GTCCRB (n: channel number). An operating mode can be set independently for each channel, and synchronized operation on channels is also possible.
By setting GTDTCR, GTDVU, and GTDVD, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

(1) Saw-Wave PWM Mode

In saw-wave PWM mode, GPTn.GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA or GPTn.GTCCRB compare match occurs (n: channel number). The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting
Figure 24.27 shows an example of saw-wave PWM mode operation, and Figure 24.28 shows an example for setting saw-wave PWM mode.

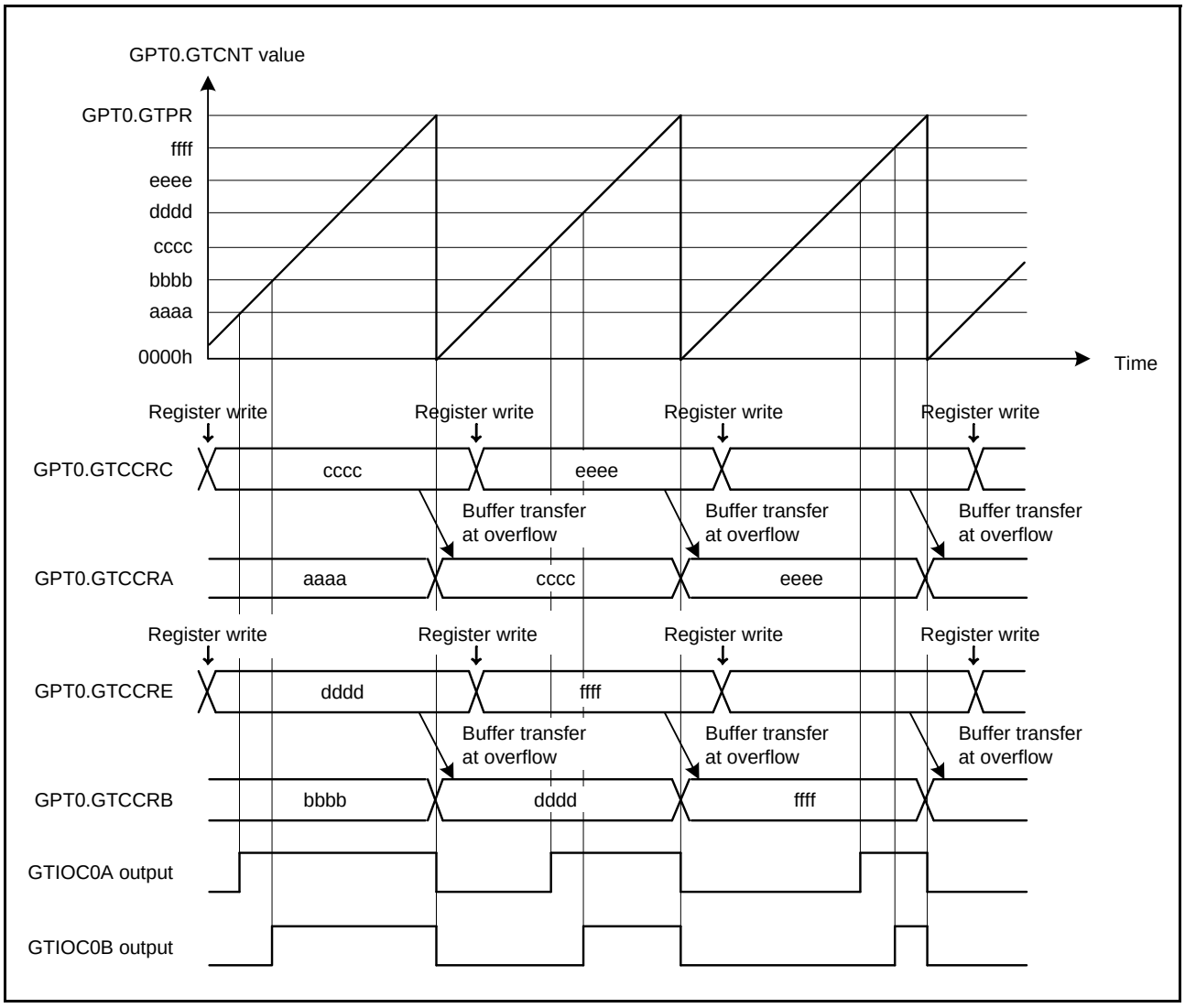
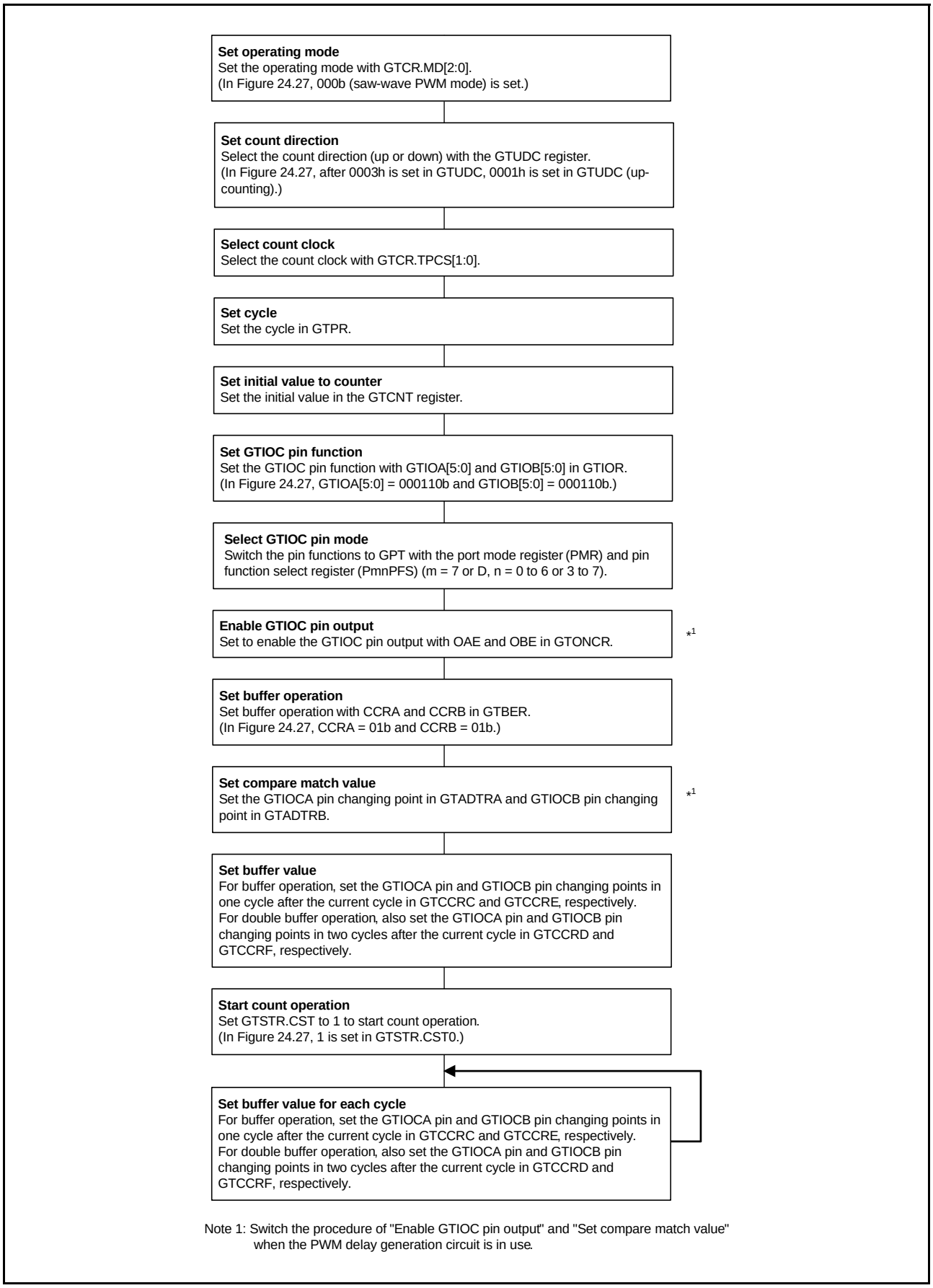


Figure 24.27 Example of Saw-Wave PWM Mode Operation (Up-Count Operation, Buffer Operation, High Output at GTCCRA/GTCCRB Compare Match, Low Output at Cycle End)



Note 1: Switch the procedure of "Enable GTIOC pin output" and "Set compare match value" when the PWM delay generation circuit is in use.

Figure 24.28 Example for Setting Saw-Wave PWM Mode

(2) Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin at a compare match of GPTn.GTCCRA or GPTn.GTCCRB with buffer operation fixed (n: channel number).

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from GTCCRC to GTCCRA, from GTCCRE to GTCCRB, from GTCCRD to temporary register A, and from GTCCRF to temporary register B at the cycle end, and from temporary register A to GTCCRA at a GTCCRA compare match and from temporary register B to GTCCRB at a GTCCRB compare match. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 24.29 shows an example of saw-wave one-shot pulse mode operation, and Figure 24.30 shows an example for setting saw-wave one-shot pulse mode.

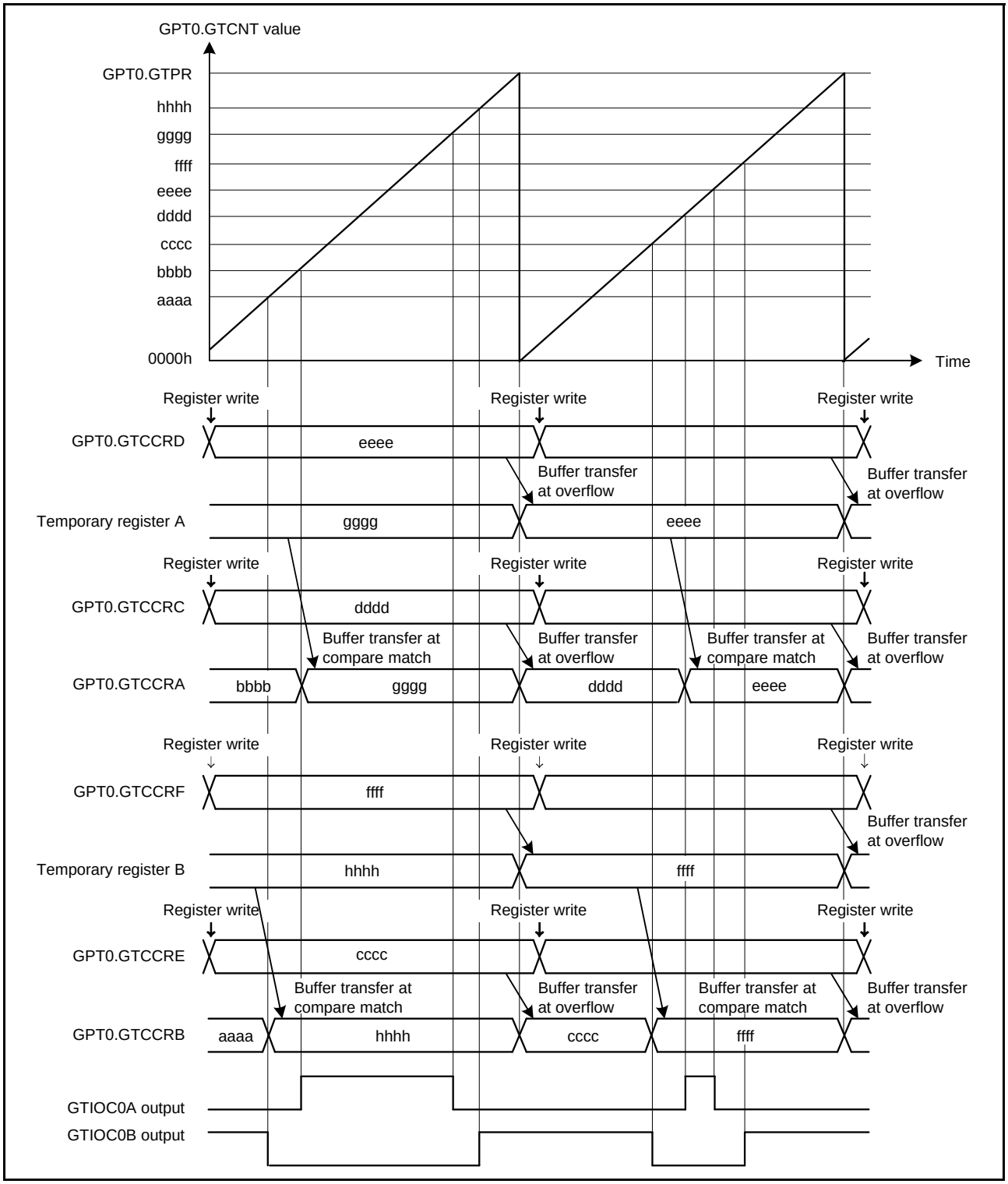


Figure 24.29 Example of Saw-Wave One-Shot Pulse Mode Operation (Up-Count Operation, Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

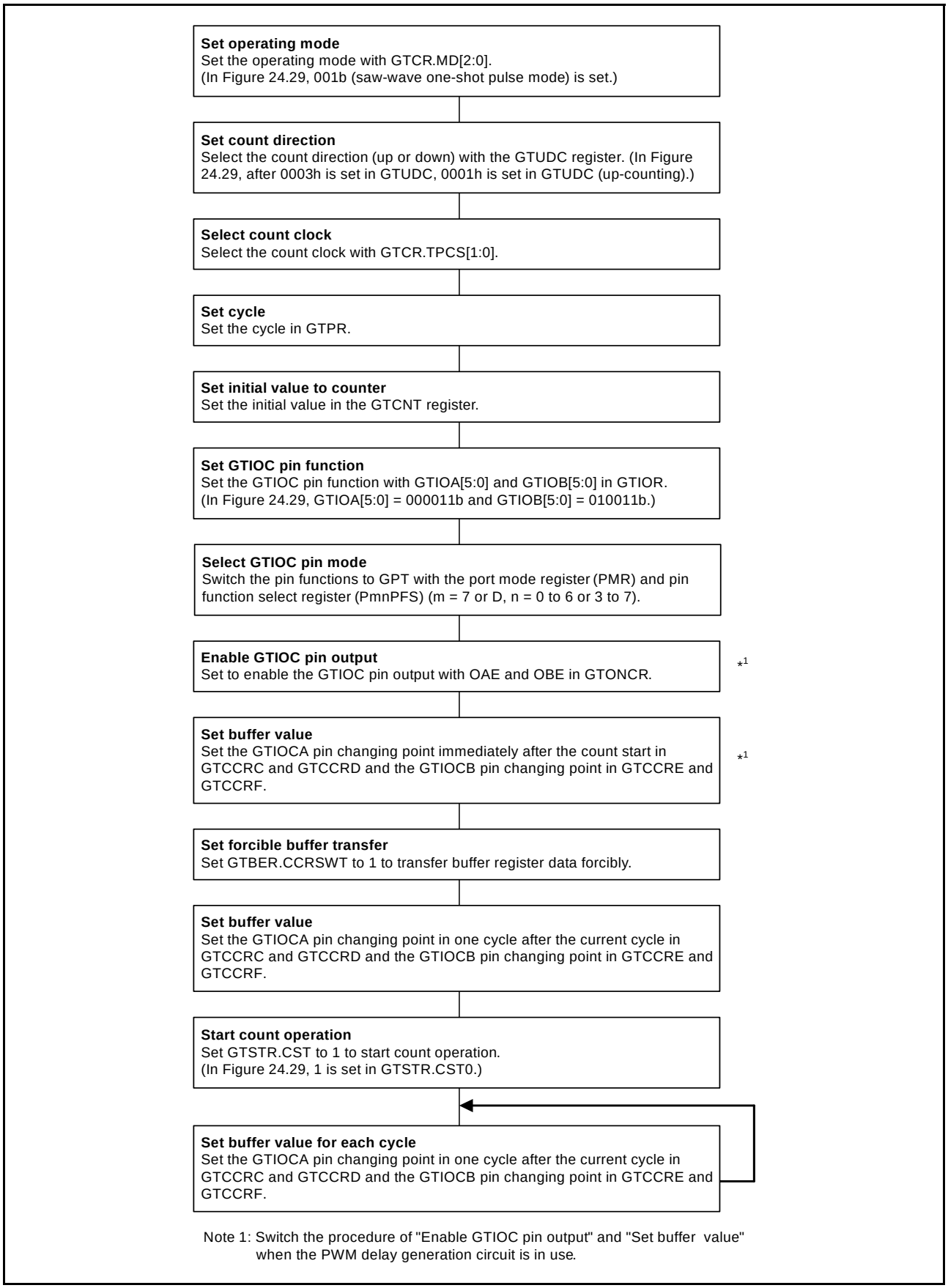


Figure 24.30 Example for Setting Saw-Wave One-Shot Pulse Mode

(3) Triangle-Wave PWM Mode 1 (16-Bit Transfer at Trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA or GPTn.GTCCRB compare match occurs (n: channel number). Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.
By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.
Figure 24.31 shows an example of triangle-wave PWM mode 1 operation, and Figure 24.32 shows an example for setting triangle-wave PWM mode 1.

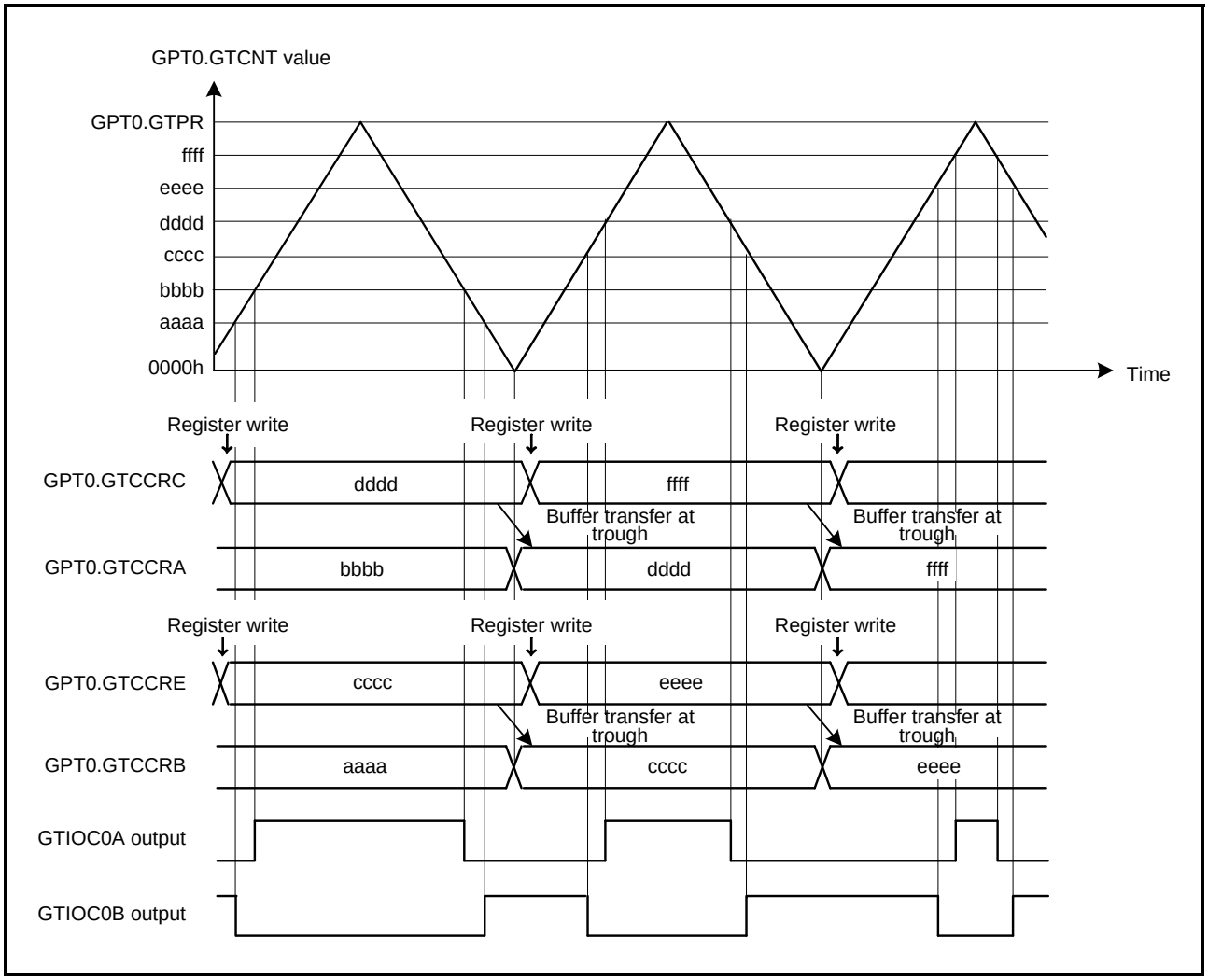


Figure 24.31 Example of Triangle-Wave PWM Mode 1 Operation (Buffer Operation, Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

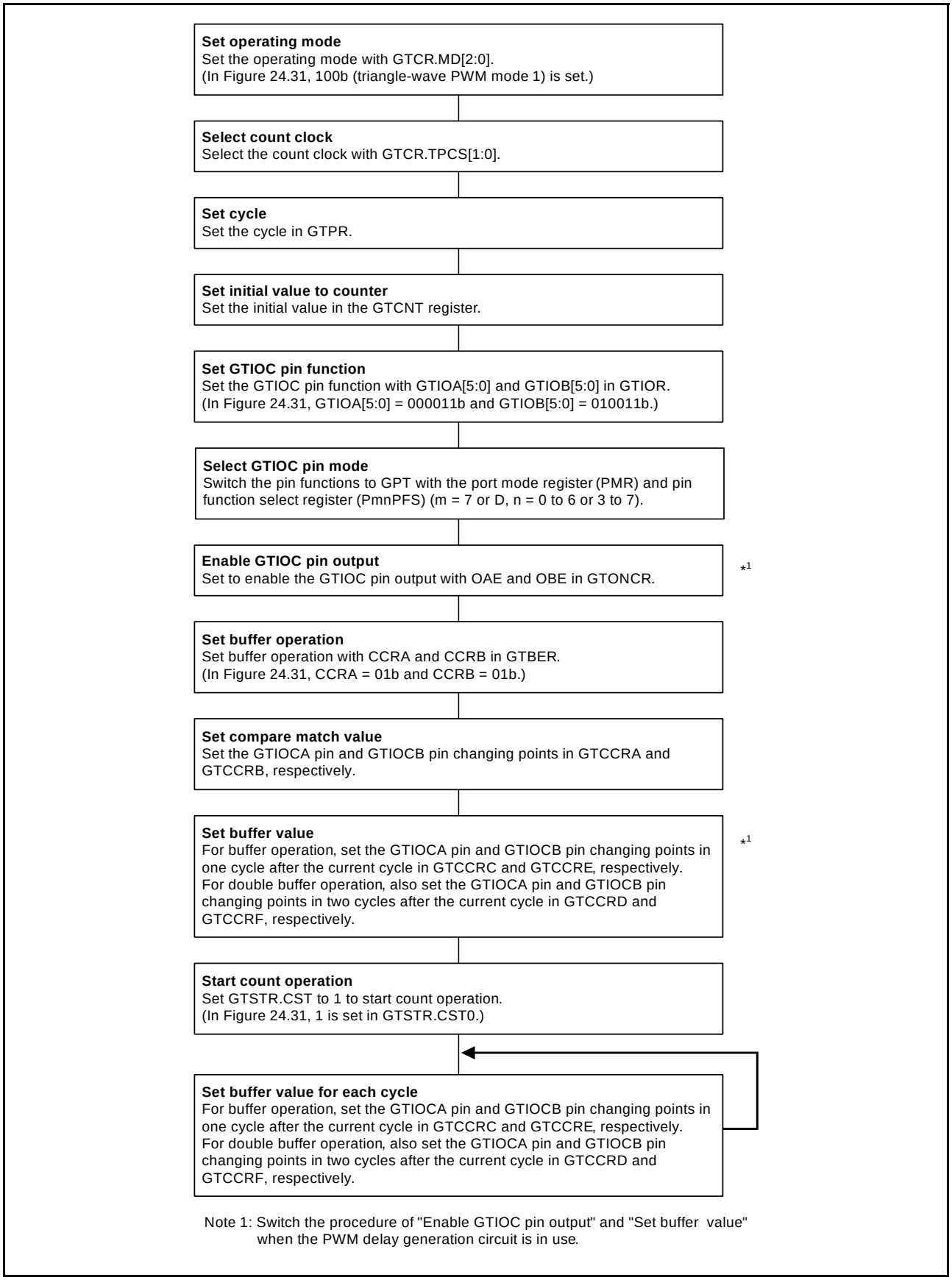


Figure 24.32 Example for Setting Triangle-Wave PWM Mode 1

(4) Triangle-Wave PWM Mode 2 (16-Bit Transfer at Crest and Trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA or GPTn.GTCCRB compare match occurs (n: channel number). The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.
By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.
Figure 24.33 shows an example of triangle-wave PWM mode 2 operation, and Figure 24.34 shows an example for setting triangle-wave PWM mode 2.

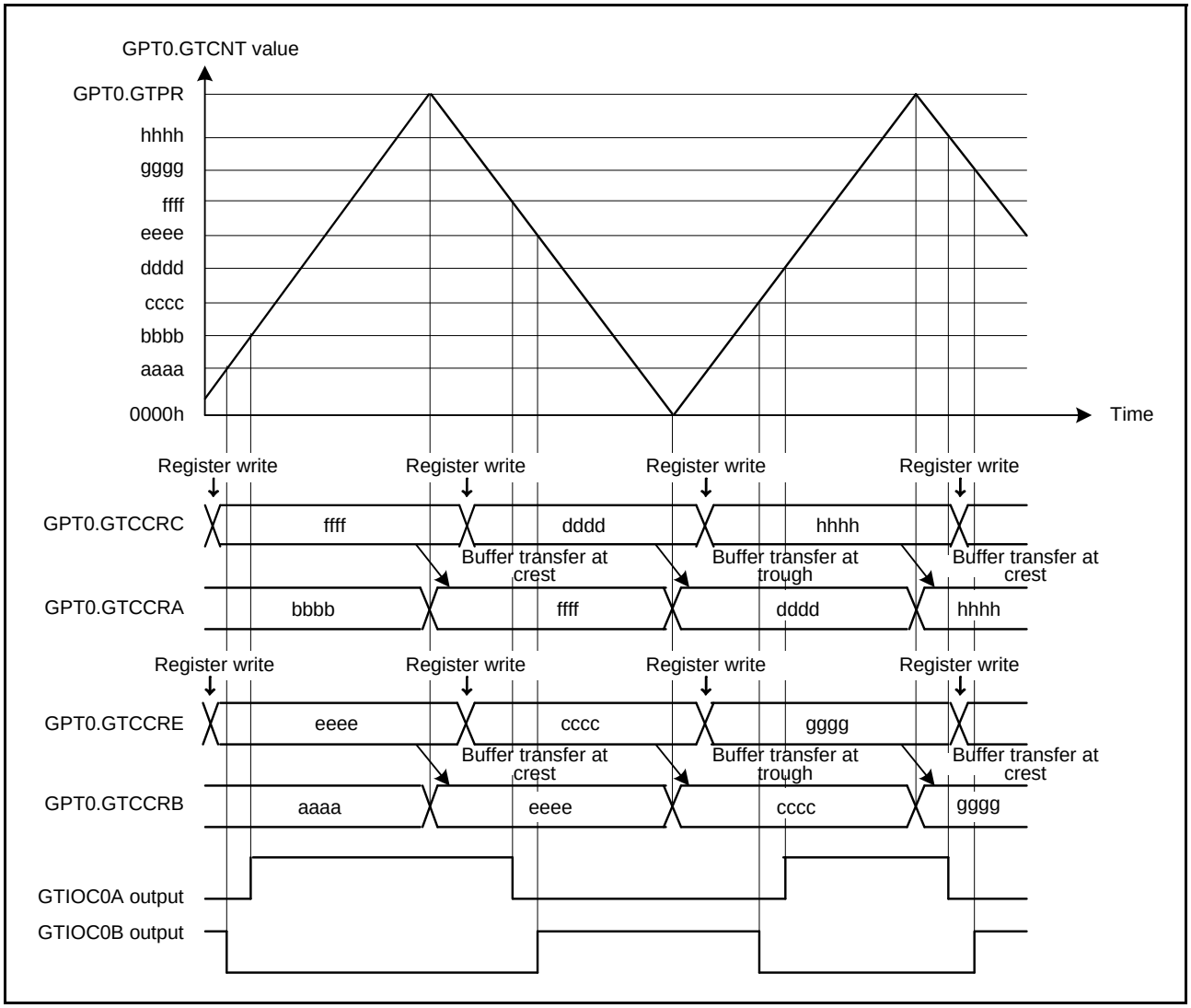


Figure 24.33 Example of Triangle-Wave PWM Mode 2 Operation (Buffer Operation, Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

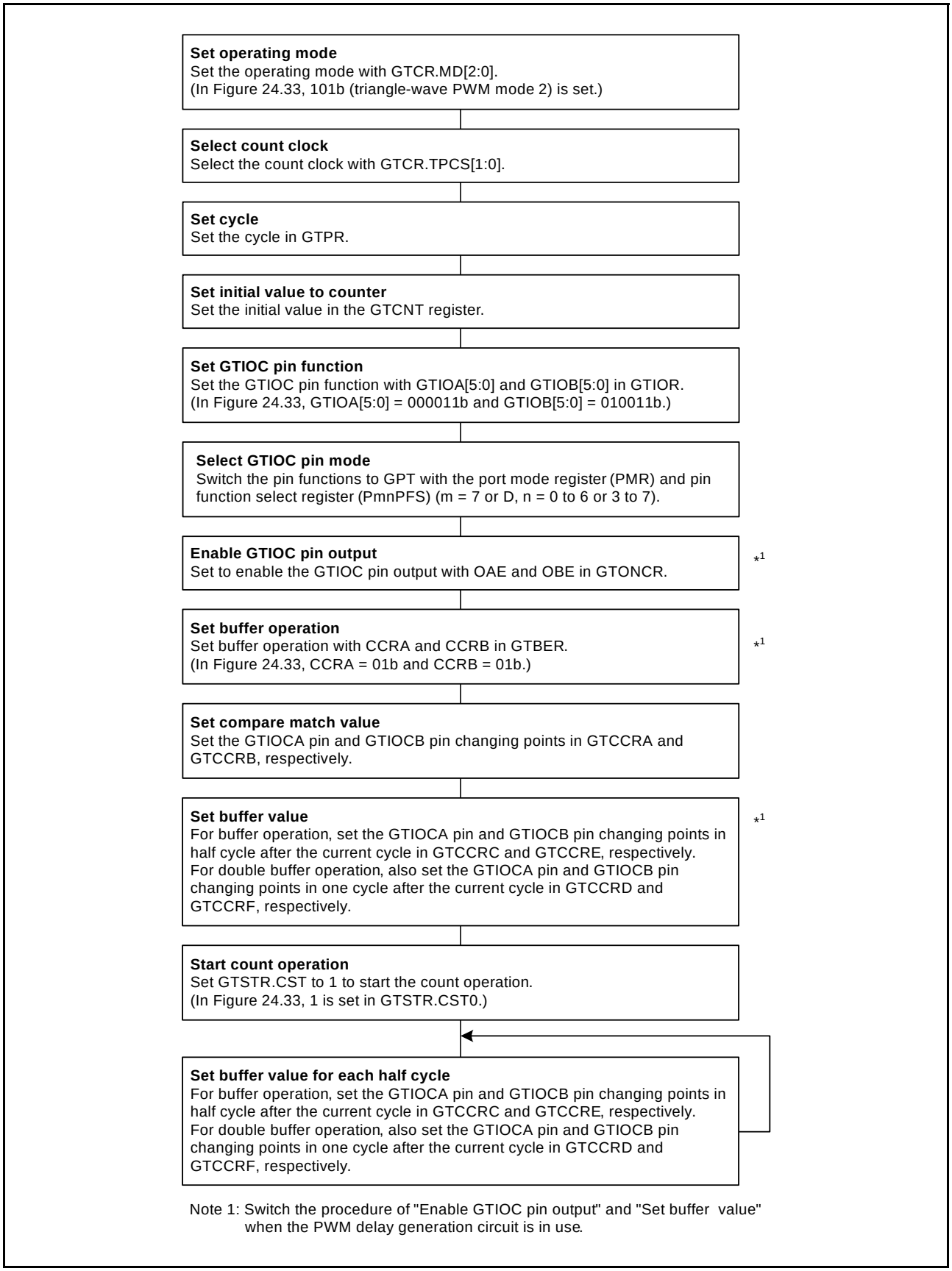


Figure 24.34 Example for Setting Triangle-Wave PWM Mode 2

(5) Triangle-Wave PWM Mode 3 (32-Bit Transfer at Trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin at a compare match of GPTn.GTCCRA or GPTn.GTCCRB with buffer operation fixed (n: channel number). Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from GTCCRC to GTCCRA, from GTCCRE to GTCCRB, from GTCCRD to temporary register A, and from GTCCRF to temporary register B at the trough, and from temporary register A to GTCCRA and from temporary register B to GTCCRB at the crest. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 24.35 shows an example of triangle-wave PWM mode 3 operation, and Figure 24.36 shows an example for setting triangle-wave PWM mode 3.

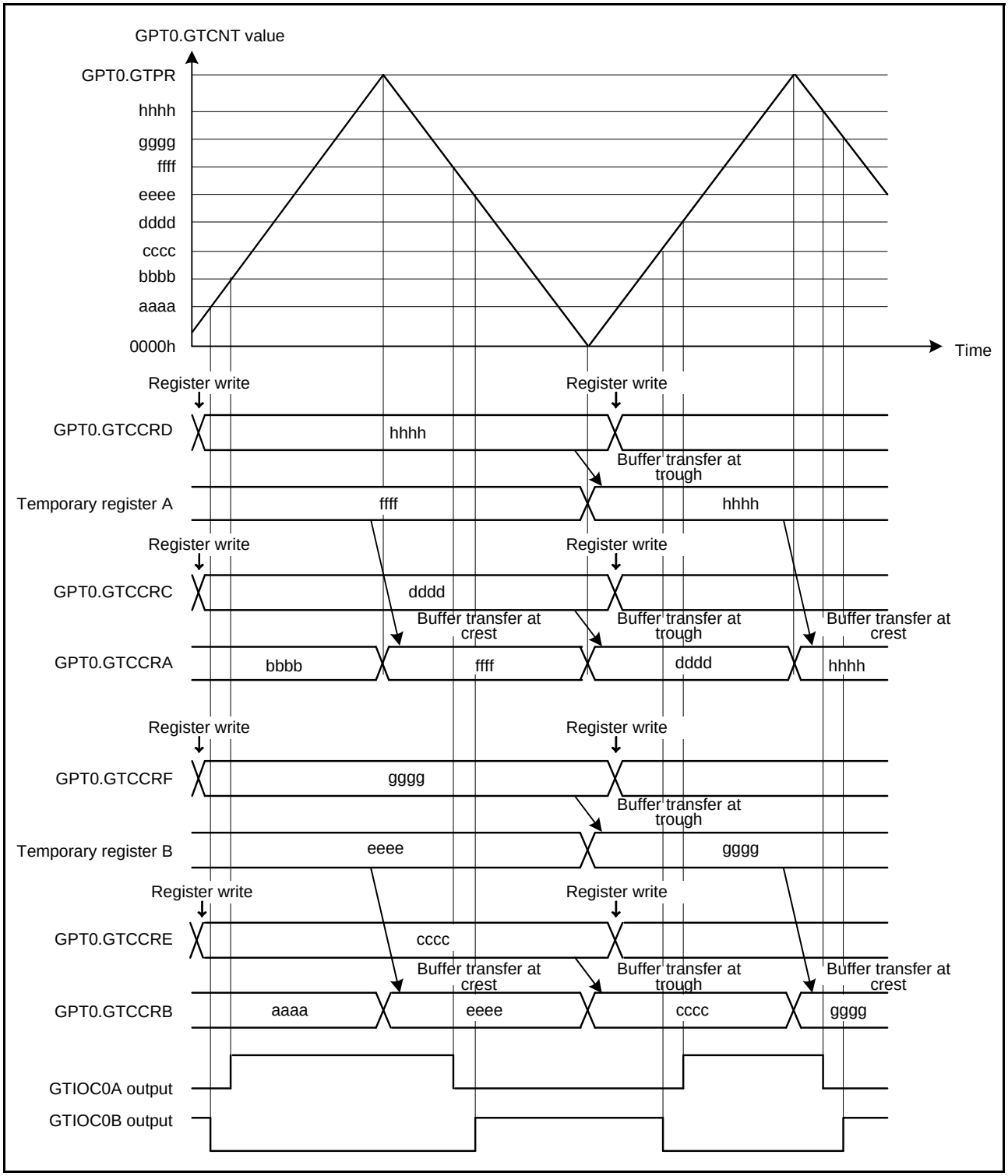


Figure 24.35 Example of Triangle-Wave PWM Mode 3 Operation (Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

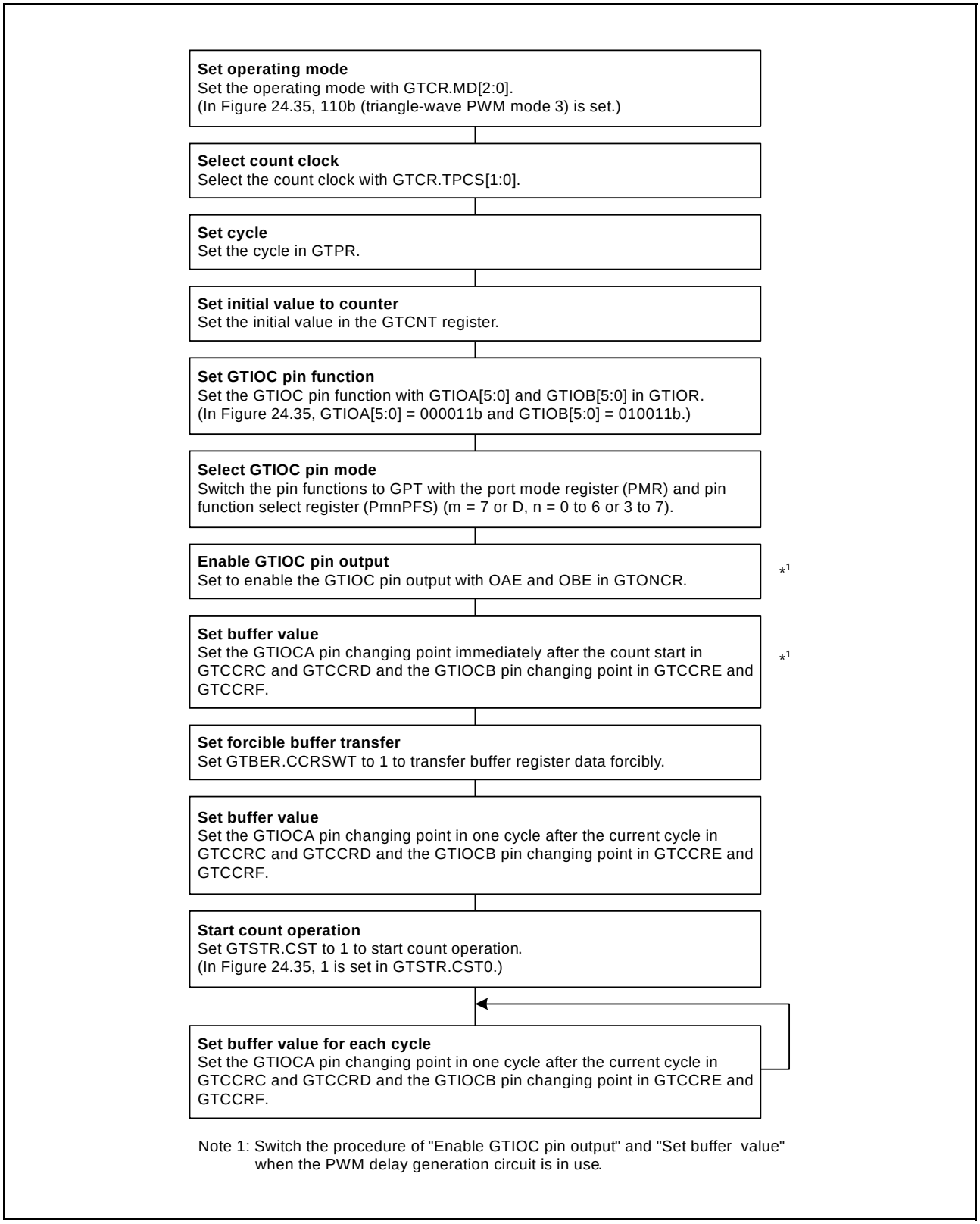


Figure 24.36 Example for Setting Triangle-Wave PWM Mode 3

24.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time values (GTDVU and GTDVD values) can automatically be set to GTCCRB.

The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes. Dead time can be separately set for the first half and second half of a waveform. Dead time for the changing point in the first half of a negative waveform is set in GTDVU and that in the second half is set in GTDVD. The same dead time can also be set for the first and second halves.

GTDBU can be used as a buffer register of GTDVU, and GTDBD can be used as a buffer register of GTDVD. Buffer transfer is performed at the cycle end (at a GTCNT overflow (during up-count operation) or an underflow (during down-count operation) for saw waves and at the trough for triangle waves).

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB.

Figure 24.37 to Figure 24.39 show examples of automatic dead time setting function operation. Figure 24.40 and Figure 24.41 show the setting examples.

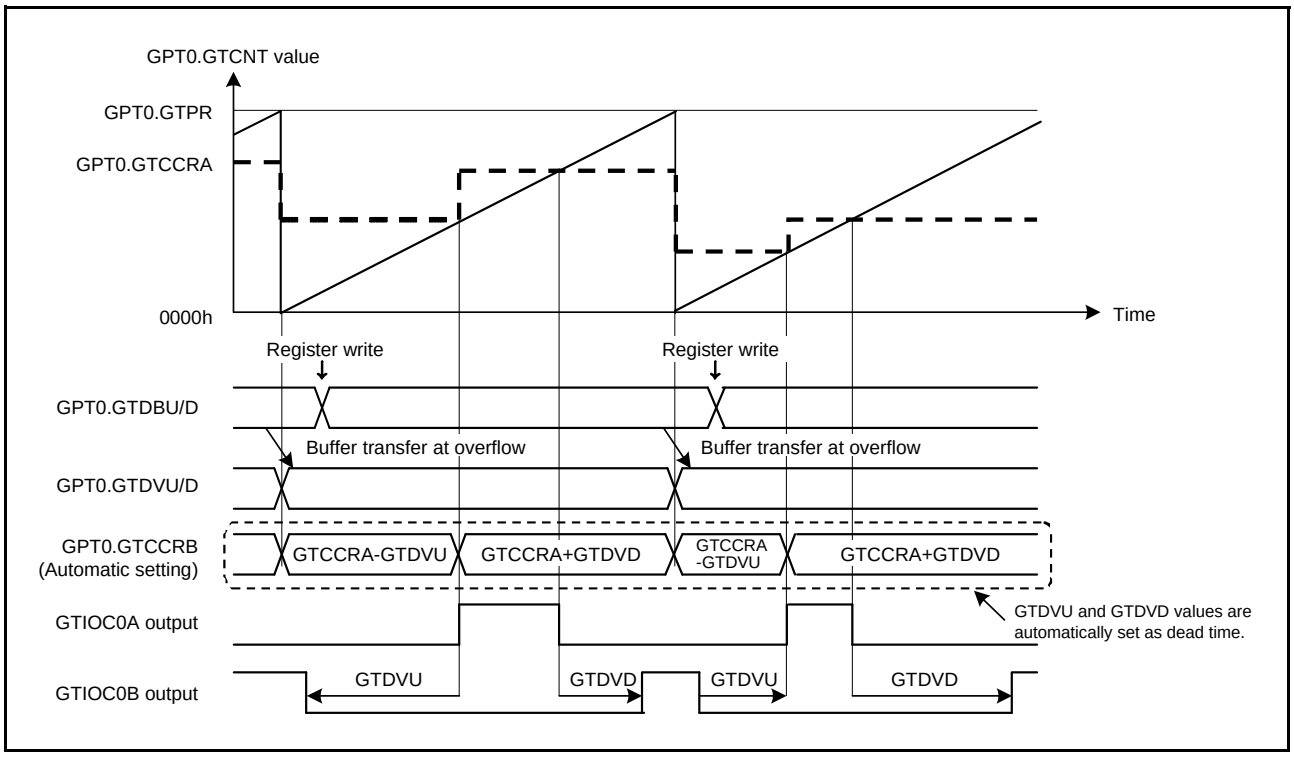


Figure 24.37 Example of Automatic Dead Time Setting Function Operation (Saw-Wave One-Shot Pulse Mode, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

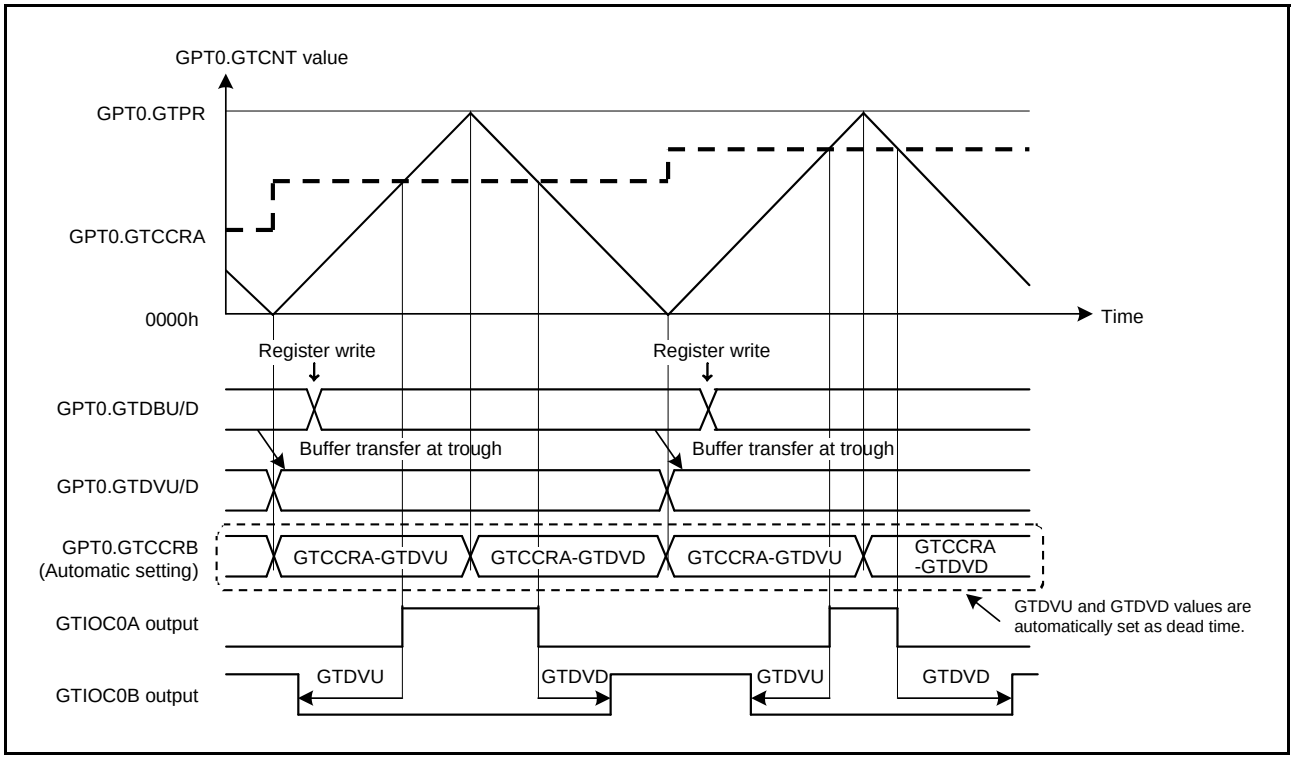


Figure 24.38 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 1, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

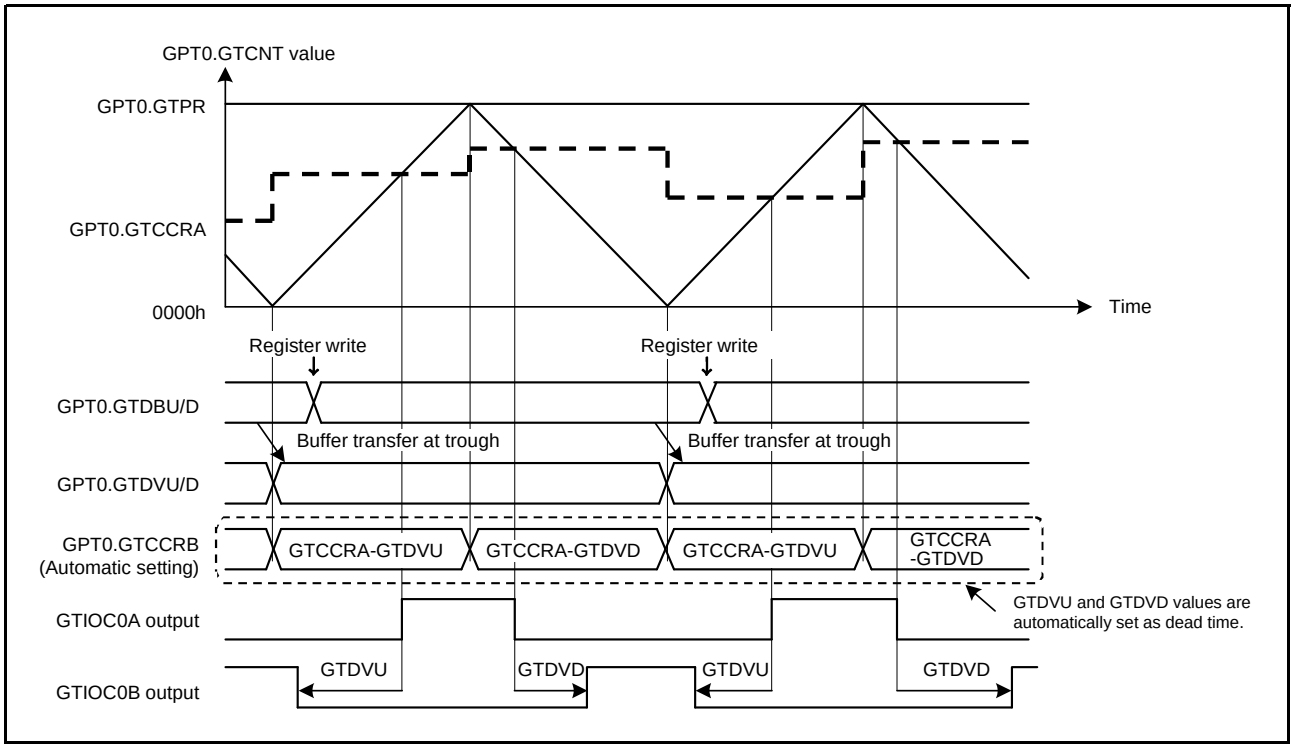


Figure 24.39 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 2 or 3, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

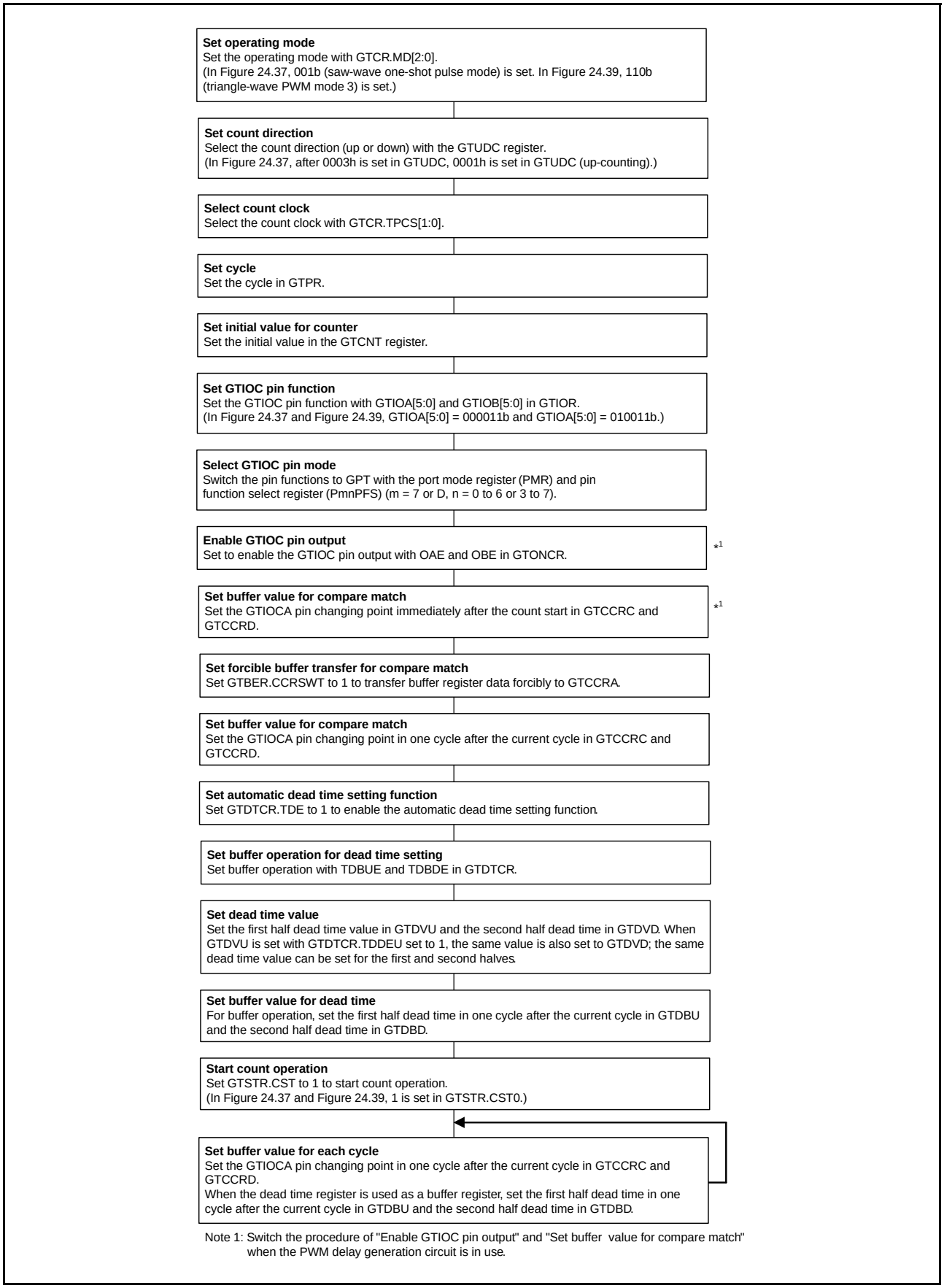
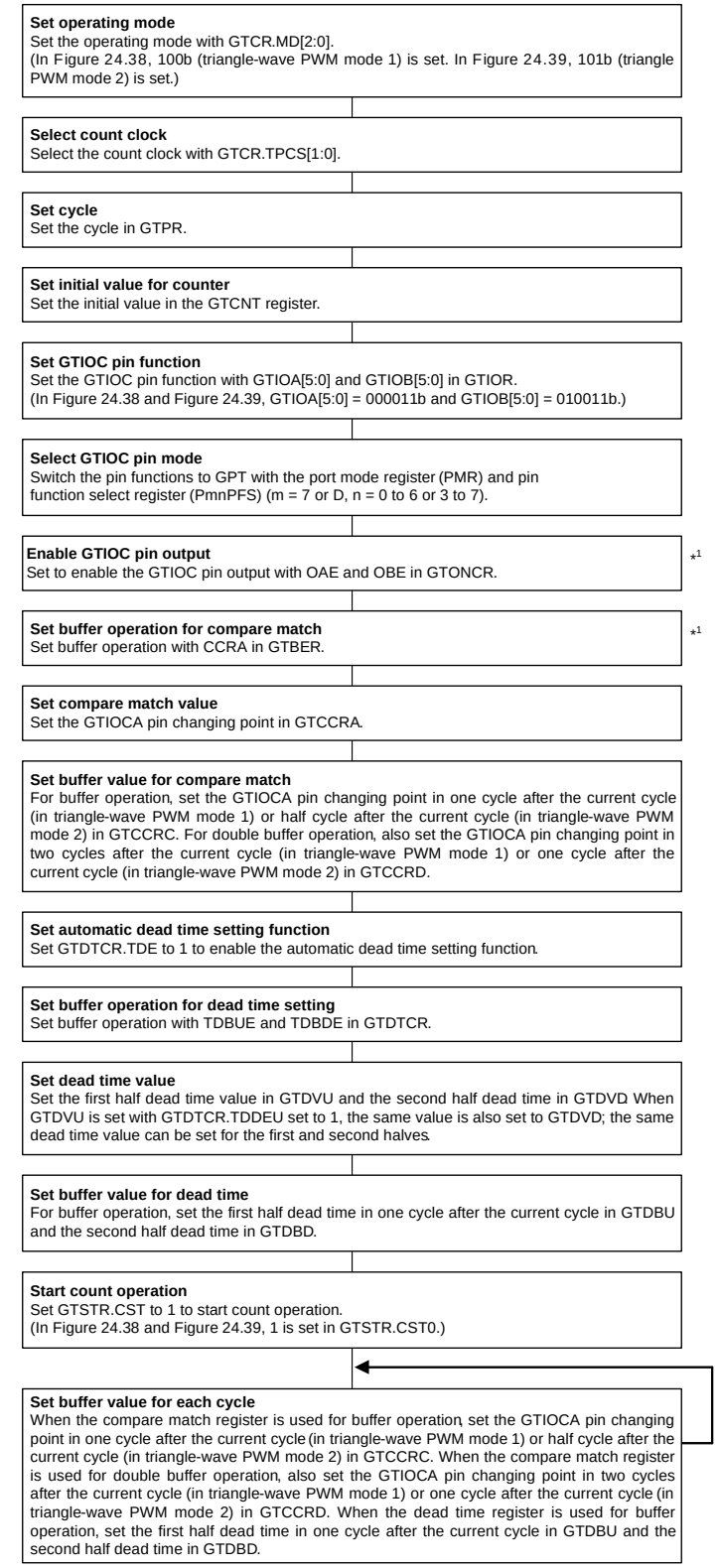


Figure 24.40 Example for Setting Automatic Dead Time Setting Function (Saw-Wave One-Shot Pulse Mode, Triangle-Wave PWM Mode 3)



Note 1: Switch the procedure of "Enable GTIOC pin output" and "Set buffer value for compare match" when the PWM delay generation circuit is in use.

Figure 24.41 Example for Setting Automatic Dead Time Setting Function (Triangle-Wave PWM Mode 1 or 2)

24.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDC.
In saw-wave mode, if the UD bit in GTUDC is modified during count operation, the count direction is changed at an overflow (when modified during up-count operation) or an underflow (when modified during down-count operation). If the UD bit is modified while count operation is stopped and the UDF bit is 0, the UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while count operation is stopped, the UD bit value at that time is reflected at the start of counting.
In triangle-wave mode, the count direction is not changed even though the UD bit in GTUDC is modified during count operation. Similarly, even though the UD bit is modified while count operation is stopped and UDF bit is 0, the UD bit value is not reflected to the count operation. If the UDF bit is set to 1 while count operation is stopped, the UD bit value at that time is reflected at the start of counting.
If the count direction is changed during saw-wave count operation, the GTPR value after the start of up-counting is reflected to the count cycle during up-count operation and the GTPR value before the start of down-counting is reflected during down-count operation.

Figure 24.42 shows an example of count direction changing function operation.

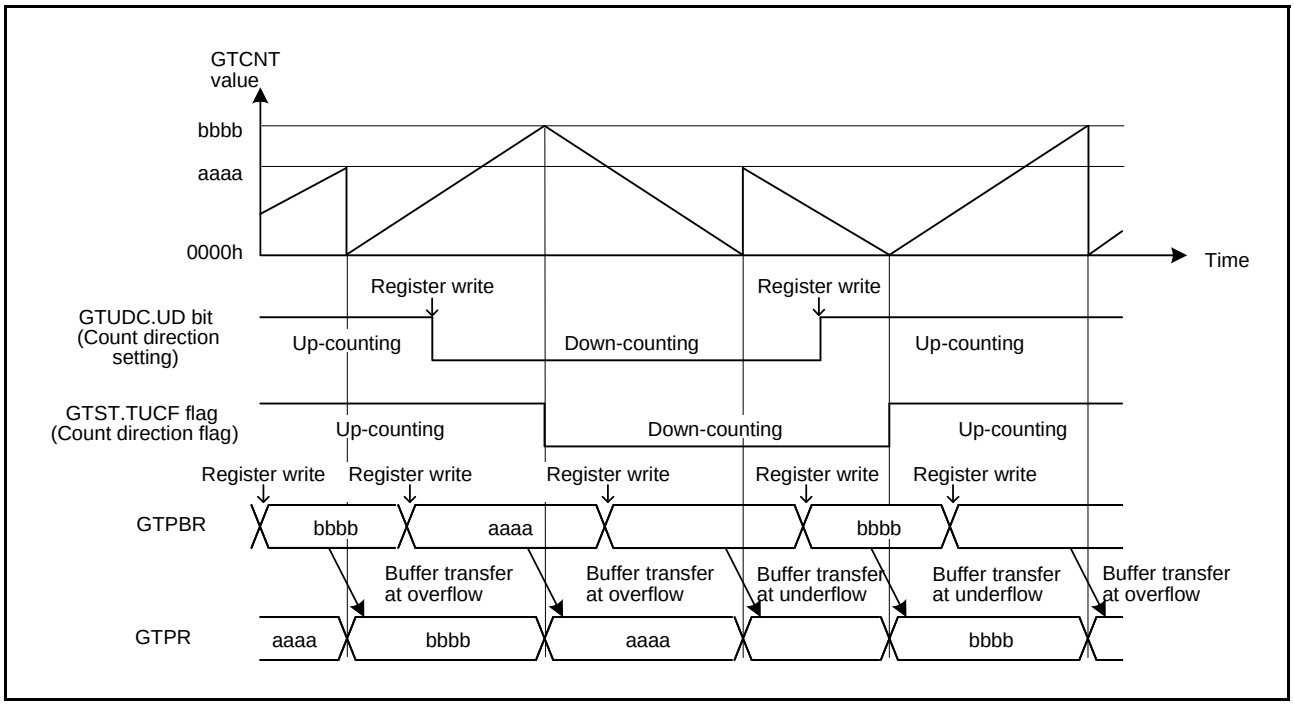


Figure 24.42 Example of Count Direction Changing Function Operation (during Buffer Operation)

24.3.6 Hardware Start/Stop and Clear Operation

The GTCNT counter can be started, stopped, or cleared by a hardware source in this MCU. There are four hardware sources: GTETRG0/GTETRG1 pin input, comparator detection, GTIOC3A/GTIOC7A and GTIOC3B/GTIOC7B pin input, and GTIOC3A/GTIOC7A and GTIOC3B/ GTIOC7B internal output (output compare).
The counter can also be cleared by the GTCCRA or GTCCRB input capture.

24.3.6.1 Hardware Start Operation

The GTCNT counter can be started by a hardware source. Select a hardware source to start counting using GTHSSR.CSHSL, set the changing edge for the hardware source with GTHSCR.CSHW, and then enable to start counting.
Figure 24.43 shows an example of count start operation by a hardware source. Figure 24.44 shows the setting example.

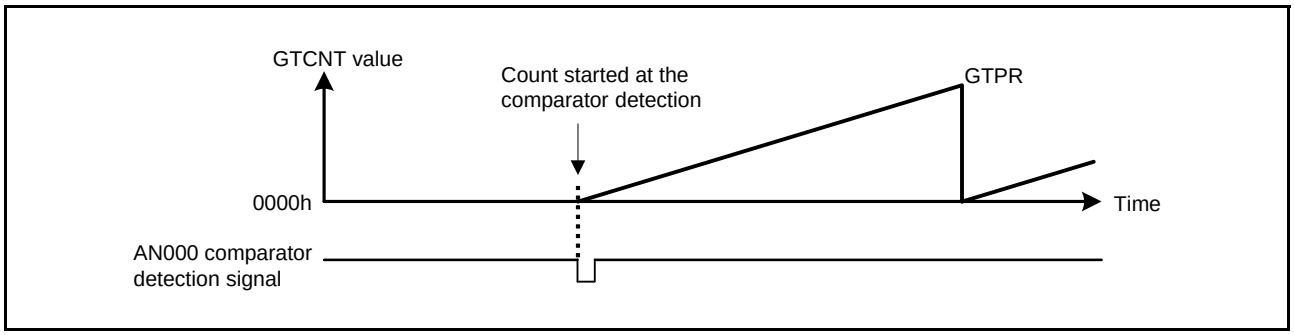


Figure 24.43 Example of Count Start Operation by Hardware Source (Started at AN000 Comparator Detection)

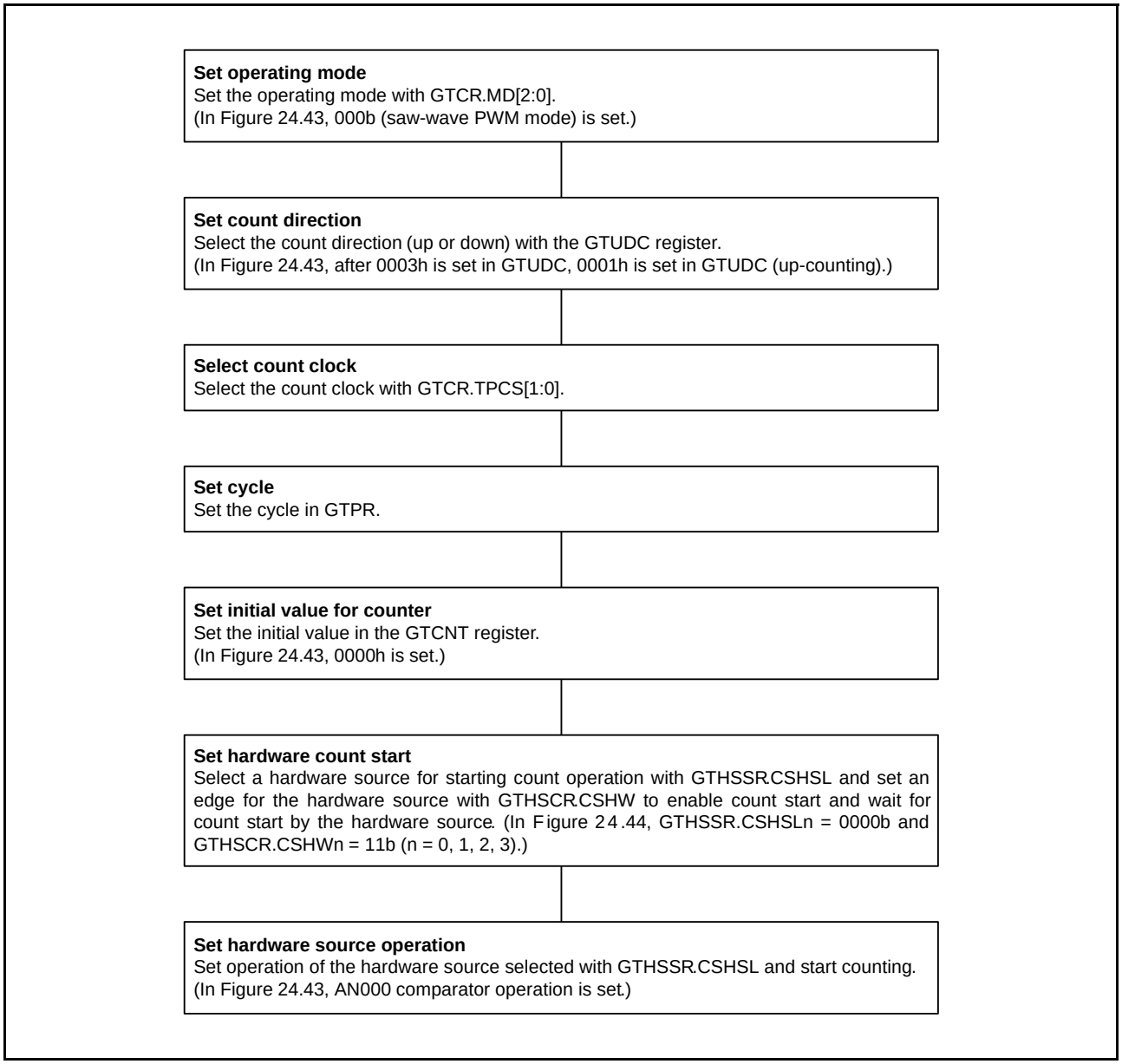


Figure 24.44 Example for Setting Count Start Operation by Hardware Source

24.3.6.2 Hardware Stop Operation

The GTCNT counter can be stopped by a hardware source. Select a hardware source to stop counting using GTHPSR.CSHPL, set the changing edge for the hardware source with GTHSCR.CPHW, and then enable to stop counting.

Figure 24.45 shows an example of count stop operation by a hardware source. Figure 24.46 shows the setting example. In this example, the count operation is stopped at both edges of the GTIOC3A internal output (output compare) and is restarted at both edges of the GTIOC3B internal output (output compare).

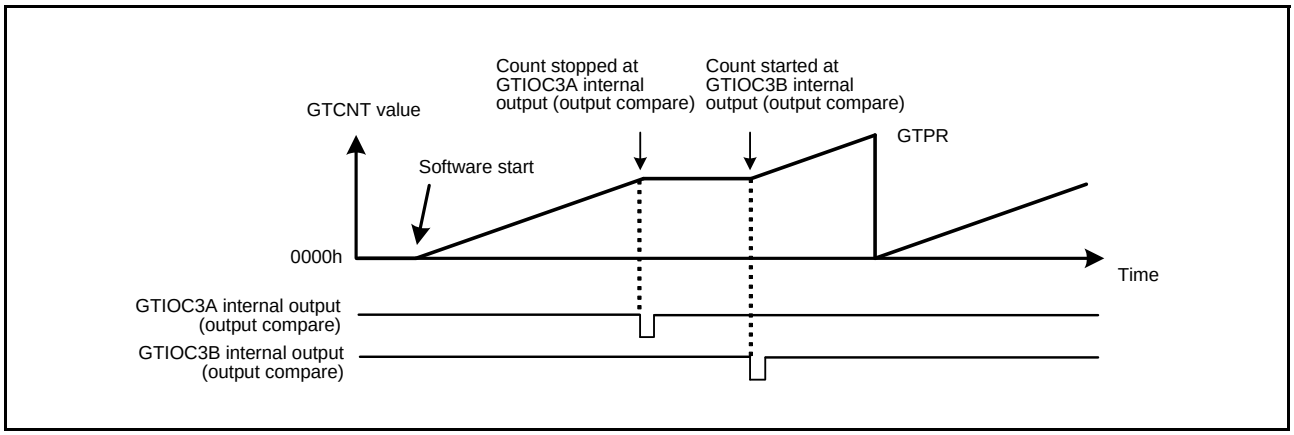


Figure 24.45 Example of Count Stop Operation by Hardware Source (Started by Software, Stopped at GTIOC3A Internal Output (Output Compare), Restarted at GTIOC3B Internal Output (Output Compare))

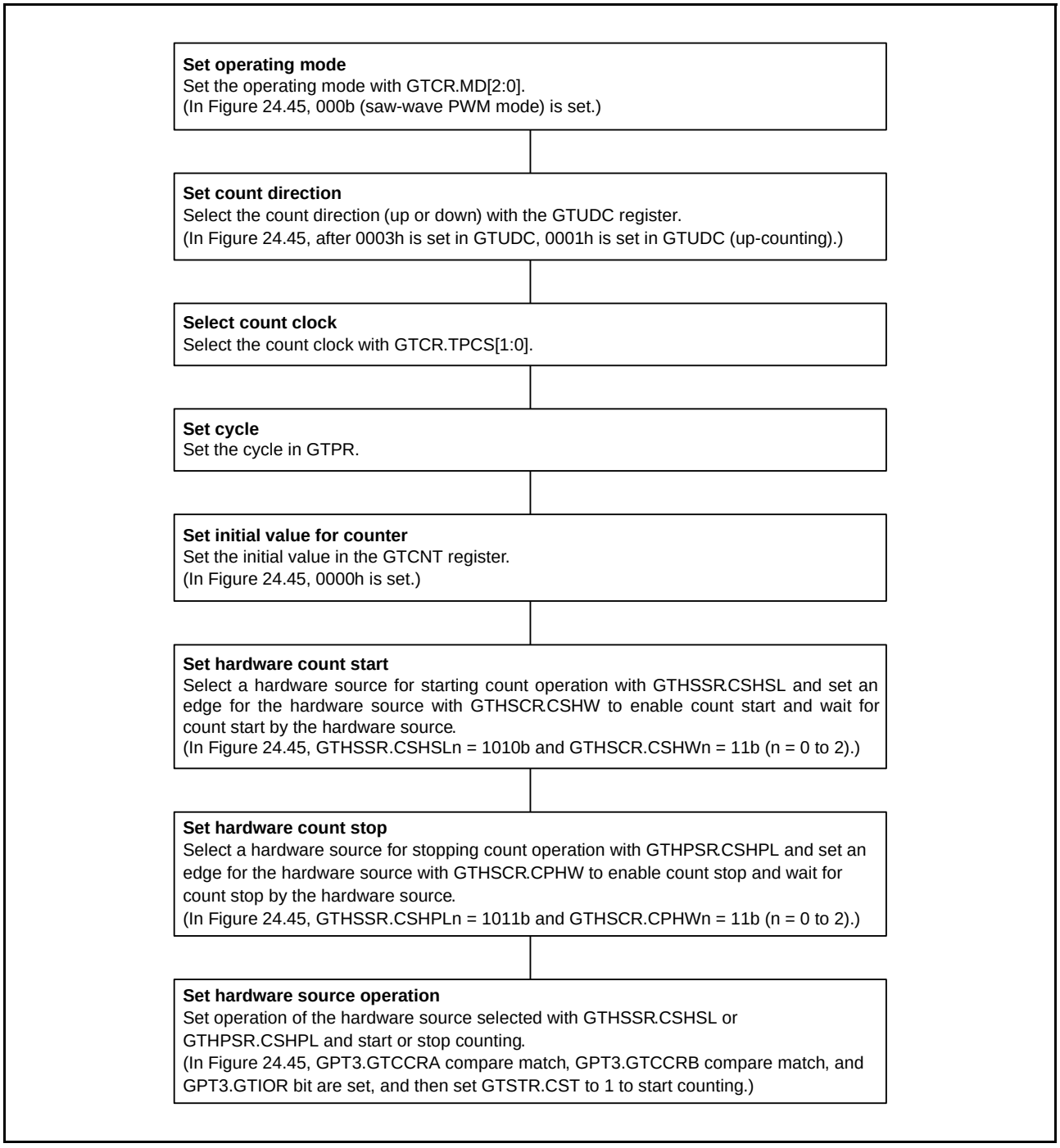


Figure 24.46 Example for Setting Count Stop Operation by Hardware Source

Figure 24.47 shows an example of count start/stop operation by a hardware source. Figure 24.48 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGn (n = 0, 1).

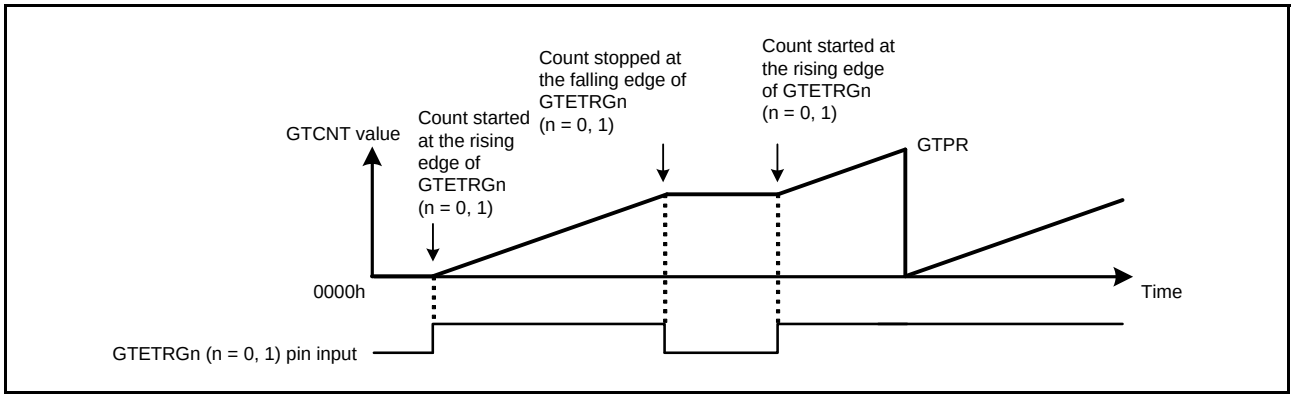


Figure 24.47 Example of Count Start/Stop Operation by Hardware Source (Started at Rising Edge of GTETRGn (n = 0, 1) Pin Input, Stopped at Falling Edge of GTETRGn (n = 0, 1) Pin Input)

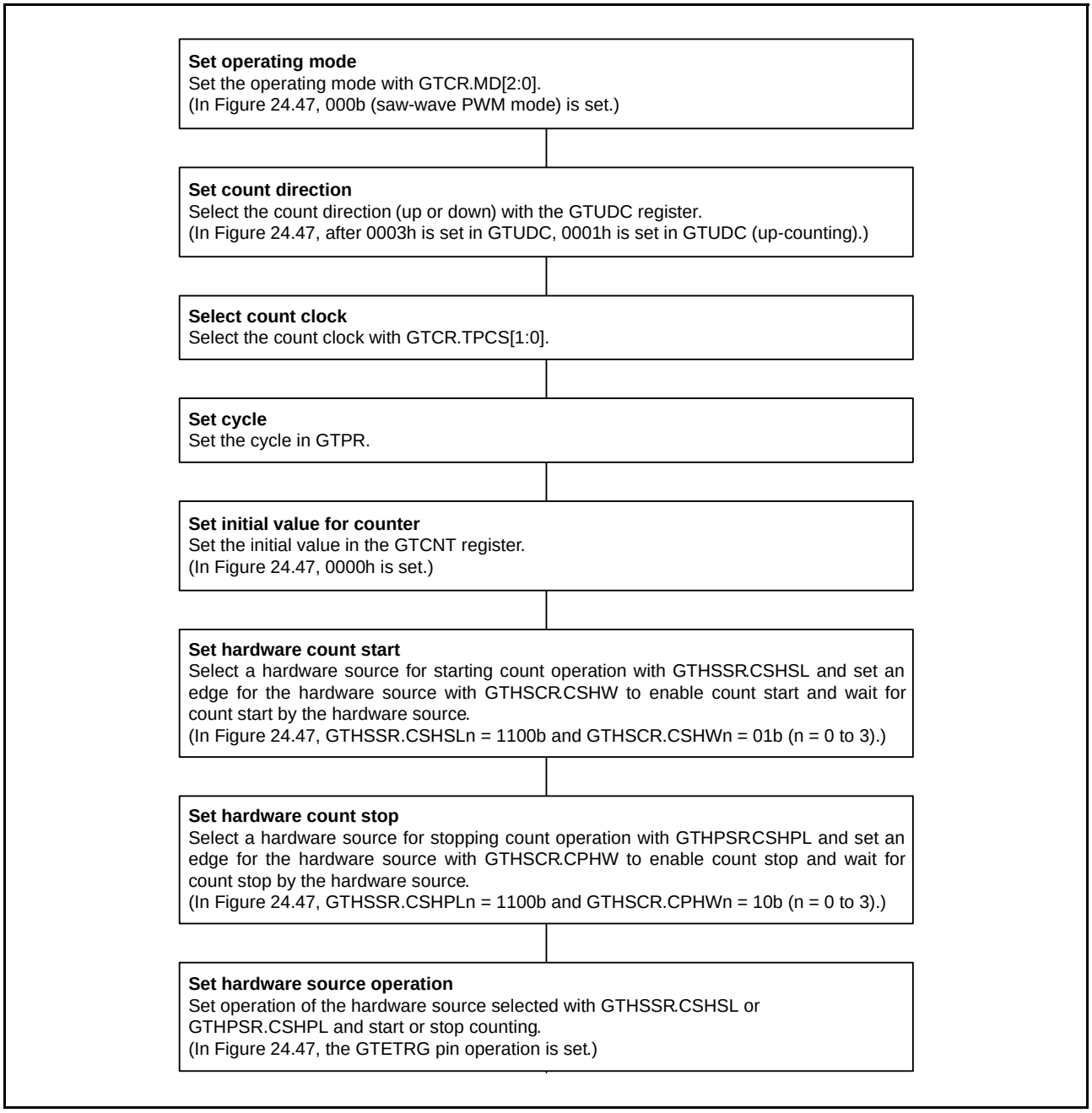


Figure 24.48 Example for Setting Count Start/Stop Operation by Hardware Source

24.3.6.3 Hardware Clear Operation

The GTCNT counter can be cleared by a hardware source. Select a hardware source to clear the counter using GTHPSR.CSHPL, set the changing edge for the hardware source with GTHCCR.CCHW, and then enable to clear the counter.

The counter can also be cleared by a GTCCRA or GTCCRB input capture by setting GTCR.CCLR[1:0].

Note that the GTCIV interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 24.49 and Figure 24.50 show examples of counter clearing operation by a hardware source. Figure 24.51 shows the setting example. In this example, the counter is started at both edges of the GTIOC3A pin, and the counter is stopped/cleared at both edges of the GTIOC3B pin input.

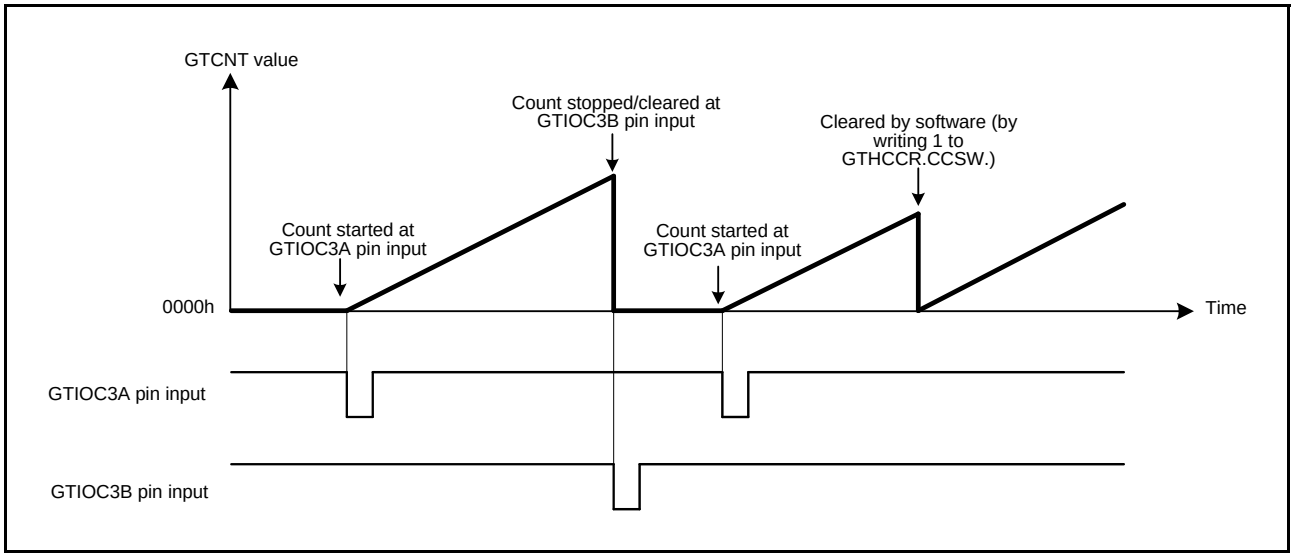


Figure 24.49 Examples of Count Clearing Operation by Hardware Source (Saw-Wave Up-Counting, Started at GTIOC3A Pin Input, Stopped/Cleared at GTIOC3B Pin Input)

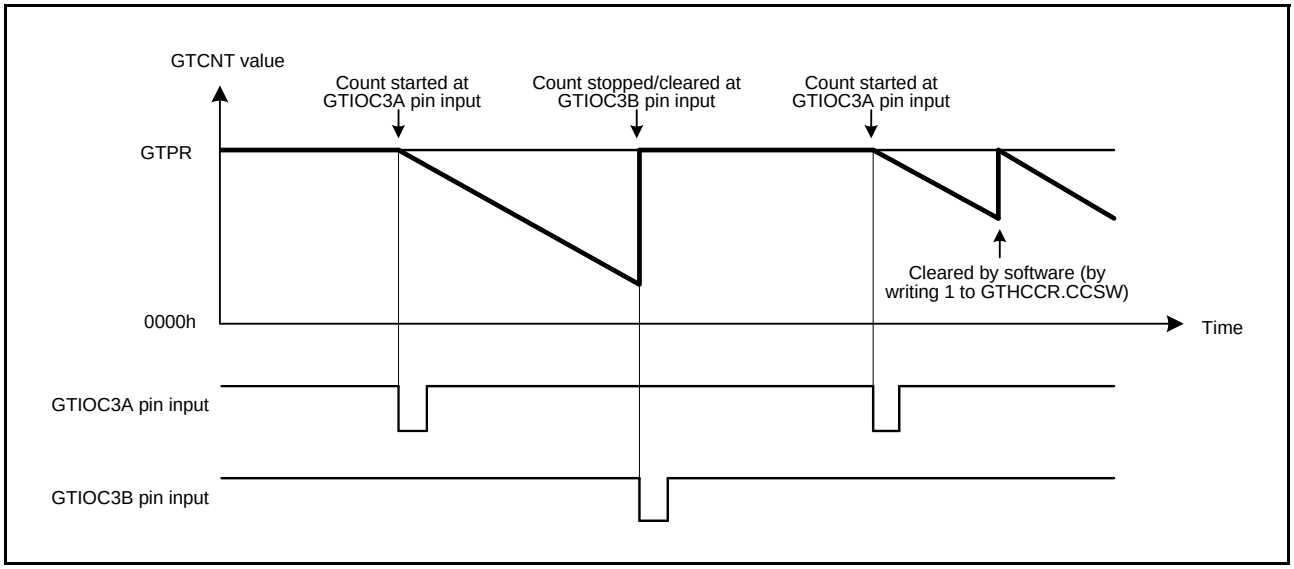


Figure 24.50 Examples of Count Clearing Operation by Hardware Source (Saw-Wave Down-Counting, Started at GTIOC3A Pin Input, Stopped/Cleared at GTIOC3B Pin Input)

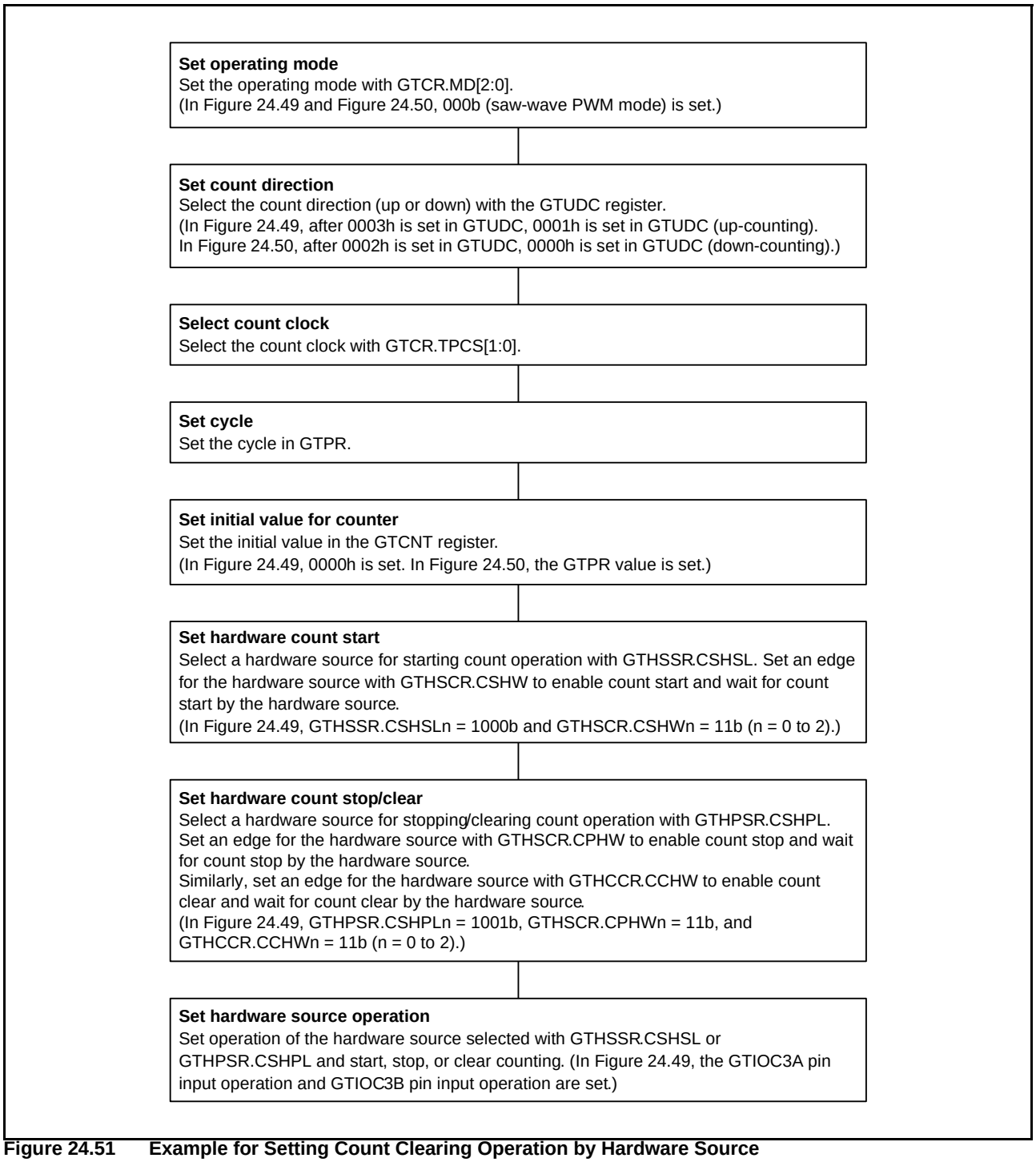


Figure 24.51 Example for Setting Count Clearing Operation by Hardware Source

The GTCIV interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 24.52 shows the relationship between the counter clearing by a hardware source and the GTCIV interrupt.

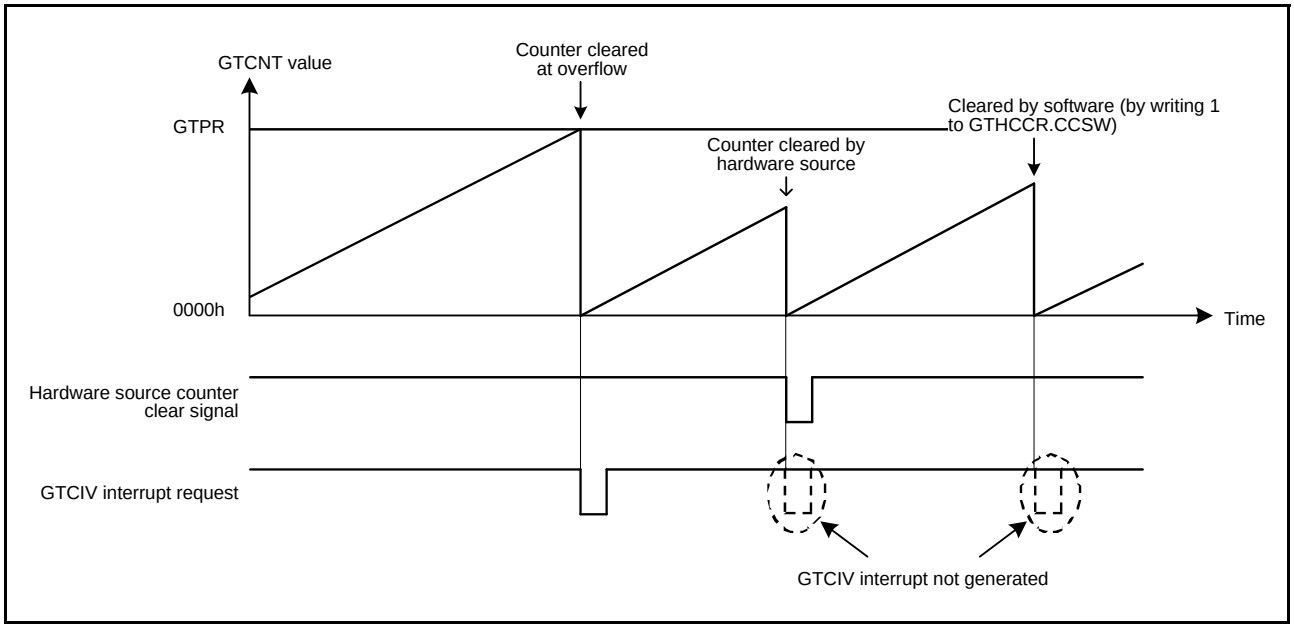


Figure 24.52 Relationship between Counter Clearing by Hardware Source and GTCIV Interrupt

24.3.7 Synchronized Operation

Synchronized operation on channels (synchronized clear operation, synchronized start operation) can be performed.

24.3.7.1 Synchronized Clear Operation

Synchronized clearing on GPT0 to GPT3 and synchronized clearing on GPT4 to GPT7 can be controlled. Select which channels to be synchronously cleared by setting GTCR.CCLR[1:0] of the pertinent channels to 11b and which channel clearing source to be used for synchronized clearing by setting GTSYNC.SYNCn[1:0] (n = 0 to 7).
Figure 24.53 shows an example of synchronized clear operation, and Figure 24.55 shows the setting example. In this example, GPT1.GTCNT and GPT2.GTCNT are synchronously cleared by the GPT0.GTCNT clearing source (overflow).
Synchronized clearing of channels by a clear source does not cause synchronized clearing of another channel by the same clear source. (Synchronized clearing is not transmitted.)
Figure 24.54 shows an operation example in which two channels are synchronously cleared by the clear source of one of the channels and another channel is synchronously cleared by the clear source of the other one of the two channels. Figure 24.55 shows the setting example. In this example, GPT1.GTCNT is synchronously cleared by GPT0.GTCNT clearing source (overflow), and GPT2.GTCNT is synchronously cleared by GPT1.GTCNT clearing source (overflow). Although GPT1.GTCNT is synchronously cleared by the GPT0.GTCNT clearing source (overflow), GPT2.GTCNT is not synchronously cleared when GPT1.GTCNT is cleared by the GPT0.GTCNT clearing source.

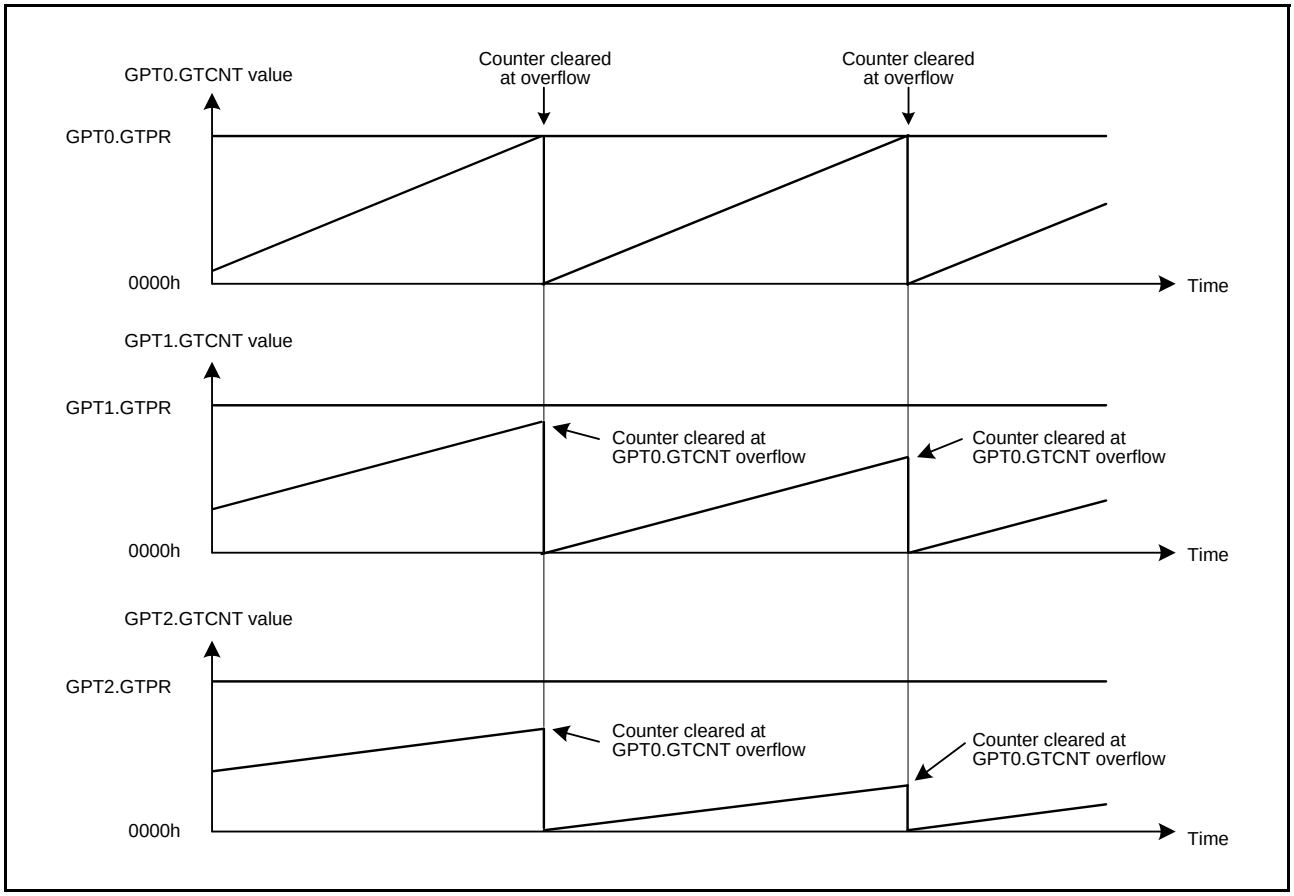


Figure 24.53 Example of Synchronized Clear Operation (GPT1.GTCNT and GPT2.GTCNT are Synchronously Cleared by GPT0.GTCNT Clearing Source)

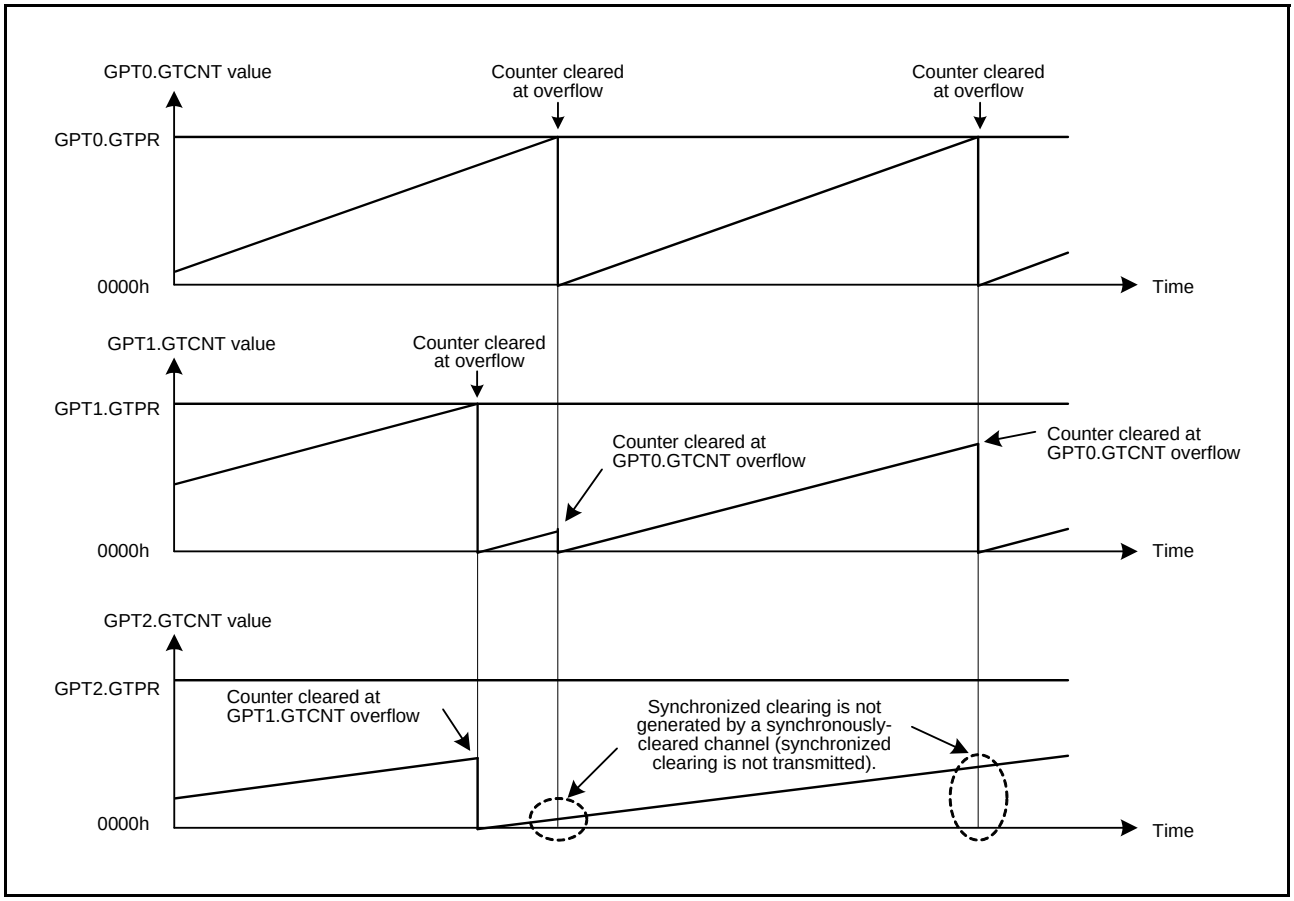


Figure 24.54 Example of Synchronized Clear Operation (GPT1.GTCNT is Synchronously Cleared by GPT0.GTCNT Clearing Source and GPT2.GTCNT is Synchronously Cleared by GPT1.GTCNT Clearing Source)

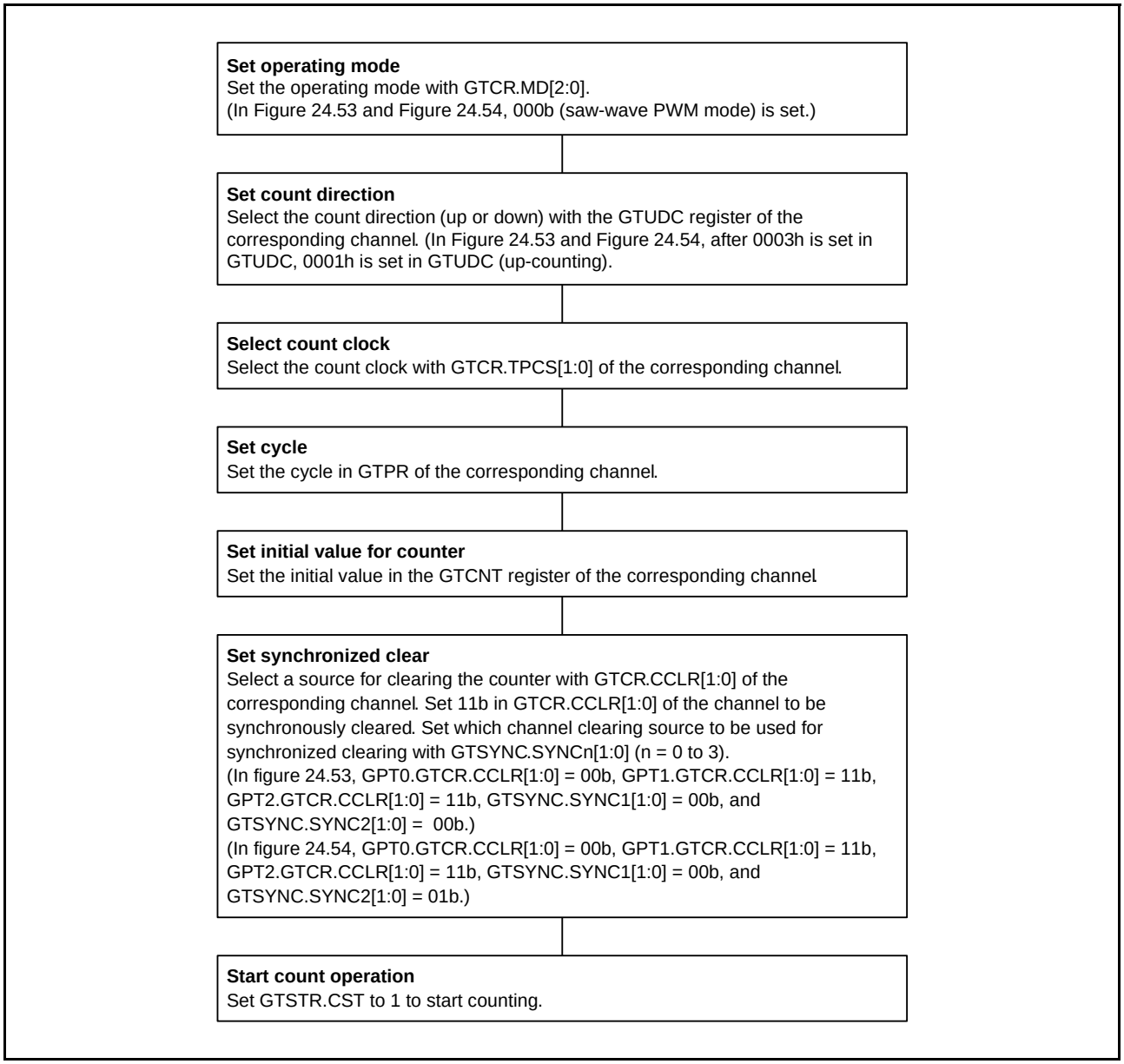


Figure 24.55 Example for Setting Synchronized Clear Operation

24.3.7.2 Synchronized Start Operation

(1) Simultaneous Start by Software

Count operation can be started simultaneously on GPT0 to GPT3 and on GPT4 to GPT7 by simultaneously setting the GTSTR.CST bits which correspond to the channels to be started simultaneously to 1 (n = 0 to 7).
Figure 24.56 shows an example of simultaneous start by software.

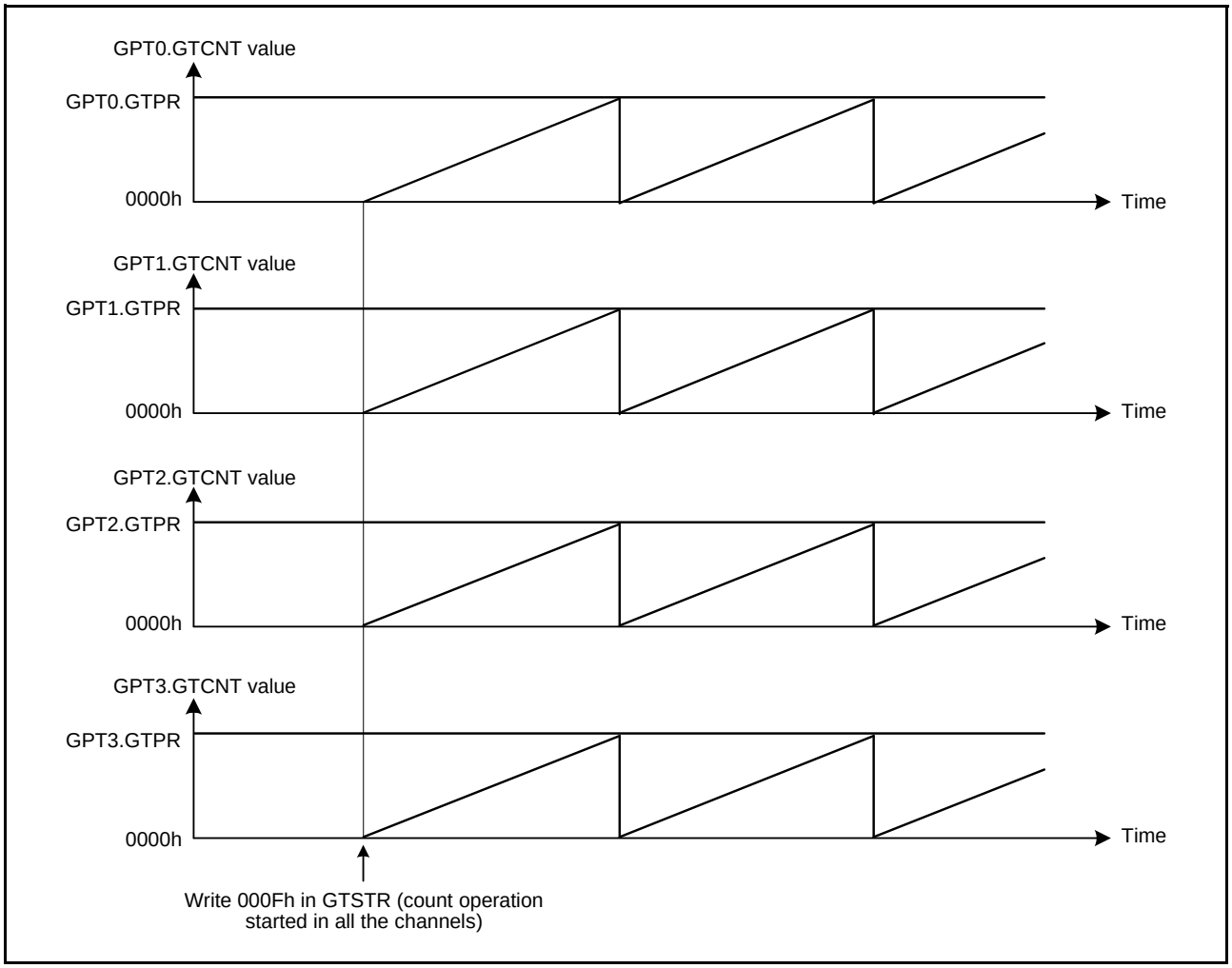


Figure 24.56 Example of Simultaneous Start by Software (with Same Count Cycle (GTPR Value))

(2) Phase Start by Software

Count start with a phase difference is possible by setting the initial value in GTCNT before counting starts and then simultaneously setting the CST bits in GTSTR which correspond to the GPT0 to GPT3 and GPT4 to GPT7 to be started simultaneously to 1 (n = 0 to 7).

Figure 24.57 shows an example of phase start operation by software.

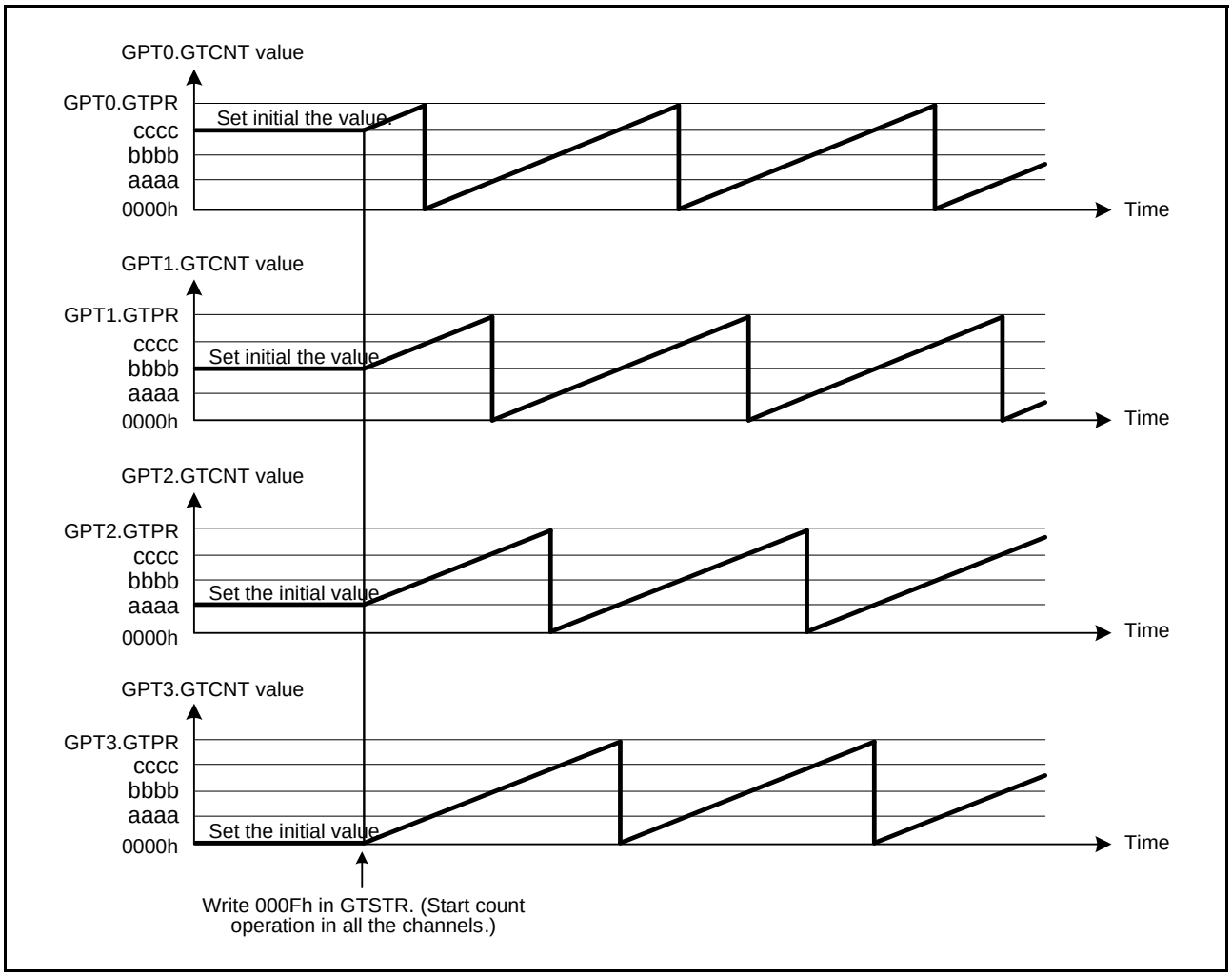


Figure 24.57 Example of Software Phase Start (with Same Count Cycle (GTPR Value))

(3) Simultaneous Start by Hardware Source

Count operation can be started simultaneously on GPT0 to GPT3 and on GPT4 to GPT7 by a hardware source in this MCU. There are four hardware sources: GTETRG0/GTETRG1 pin input, comparator detection, GTIOC3A/GTIOC7A and /GTIOC3B/GTIOC7B pin input, and GTIOC3A/GTIOC7A and /GTIOC3B/GTIOC7B internal output (output compare).

Figure 24.58 shows an example of simultaneous start operation by a hardware source and Figure 24.59 shows the setting example. In this example, count operation is started in all the channels by the AN000 comparator detection.

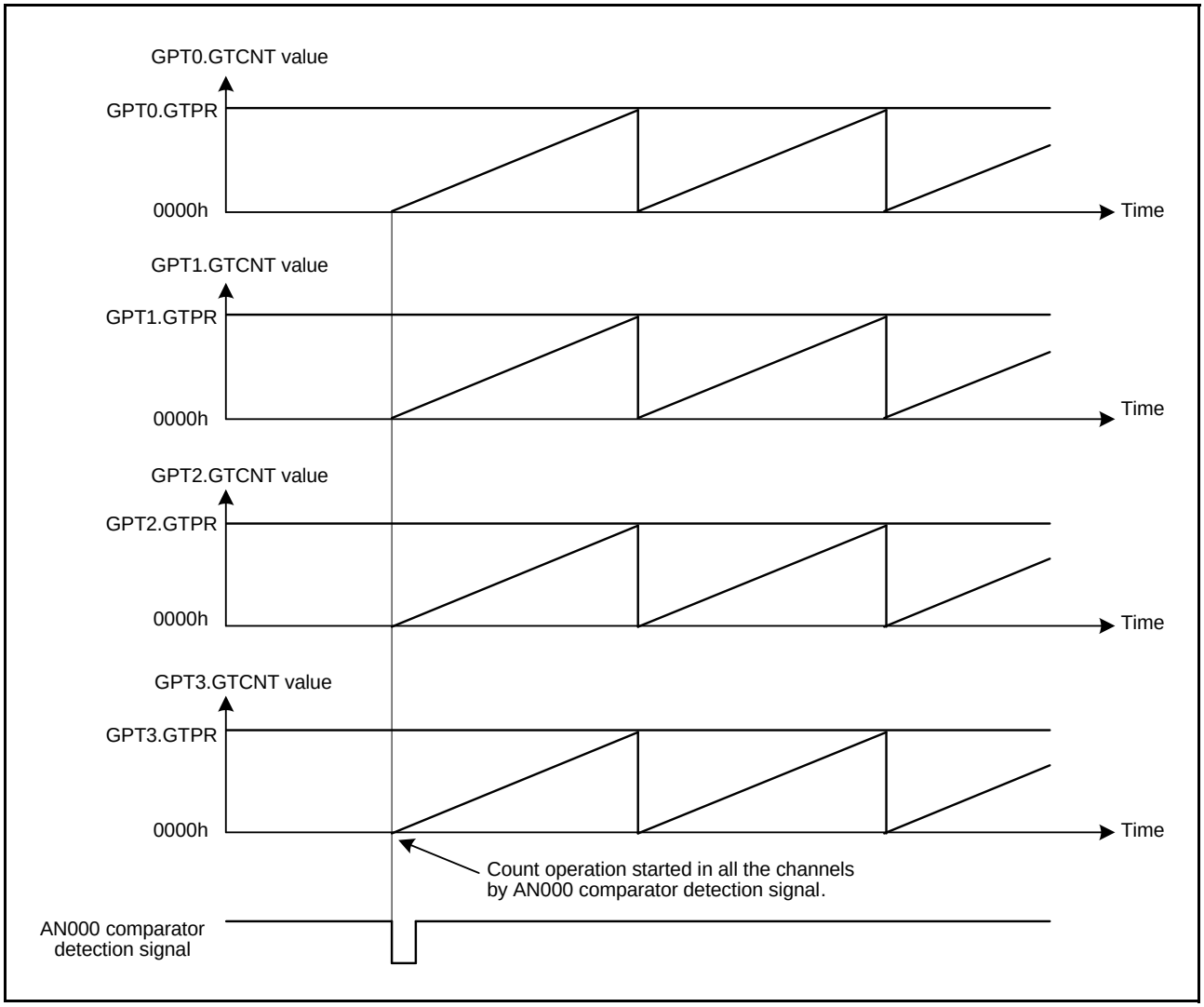


Figure 24.58 Example of Simultaneous Start Operation by Hardware Source (with Same Count Cycle (GTPR Value))

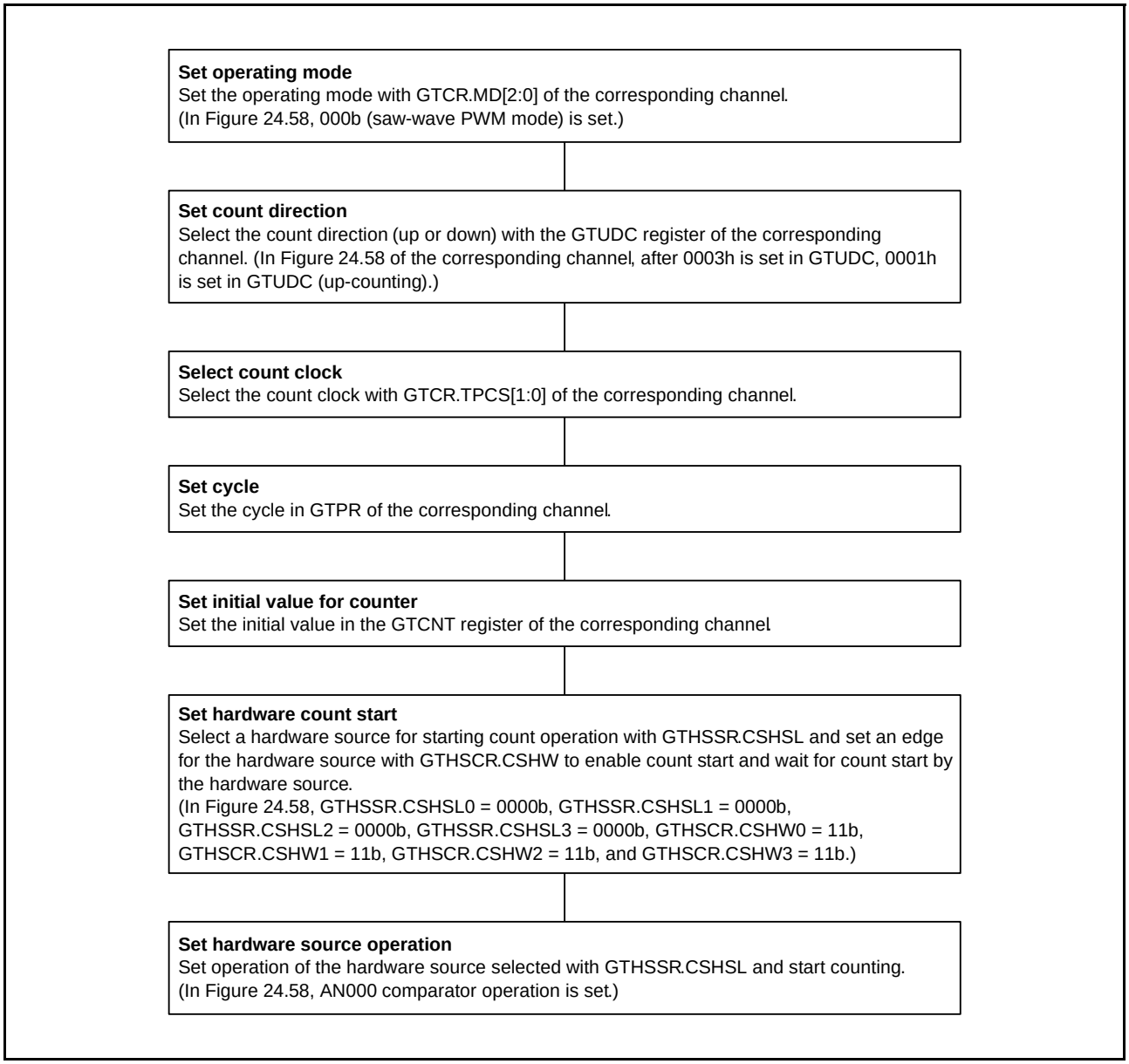


Figure 24.59 Example for Setting Simultaneous Start by Hardware Source

(4) Phase Start by Hardware Source

Count start with a phase difference on GPT0 to GPT3 and on GPT4 to GPT7 is possible by a hardware source in this MCU.

There are four hardware sources: GTETRG0/GTETRG1 pin input, comparator detection, GTIOC3A/GTIOC7A and /GTIOC3B/GTIOC7B pin input, and GTIOC3A/GTIOC7A and /GTIOC3B/GTIOC7B internal output (output compare). Figure 24.60 shows an example of phase start operation by a hardware source and Figure 24.61 shows the setting example. In this example, GPT3.GTCNT and GPT0.GTCNT simultaneously start counting and GPT1.GTCNT and GPT2.GTCNT start counting by the GTIOC3A and GTIOC3B internal outputs (output compare).

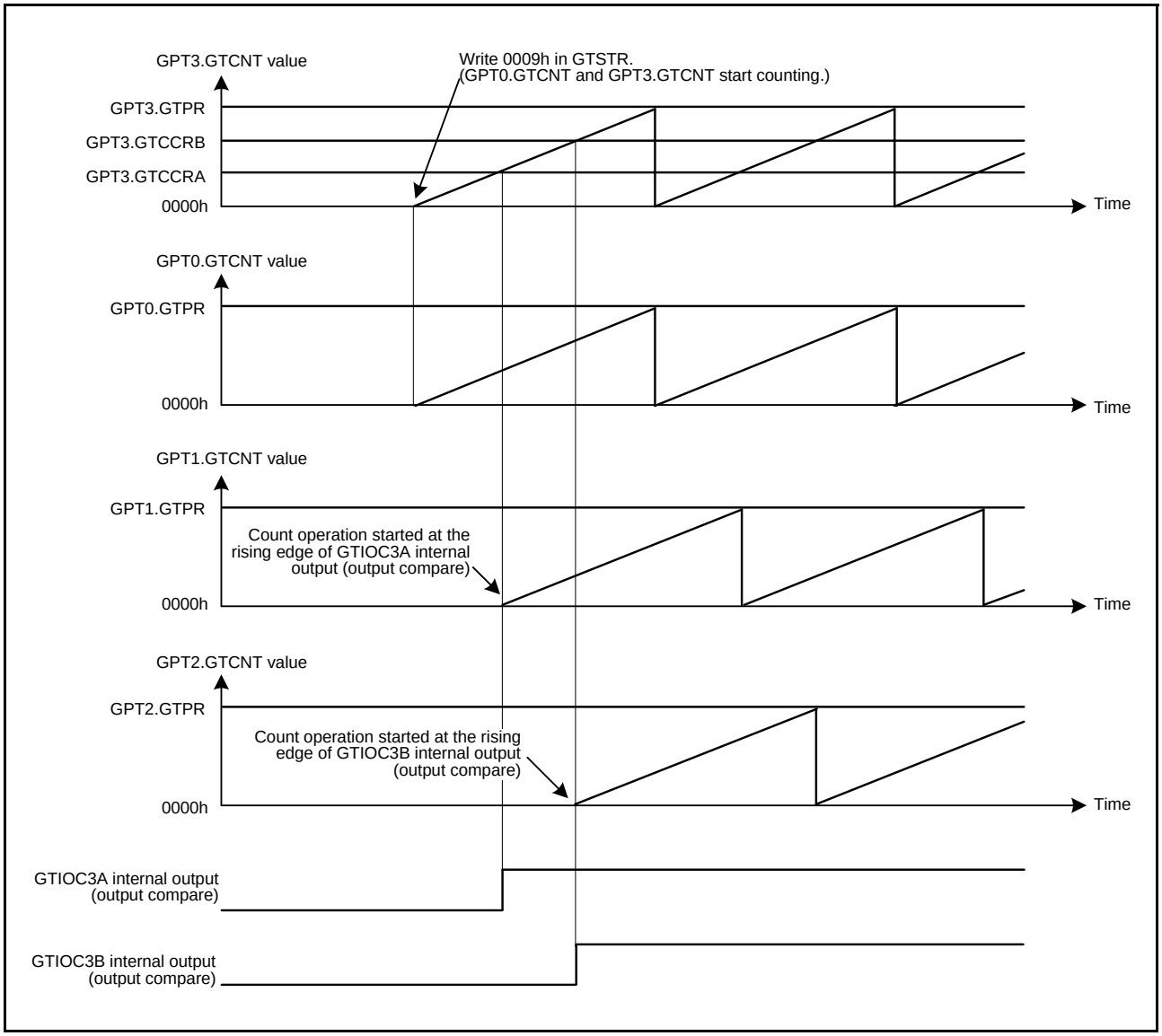


Figure 24.60 Example of Phase Start Operation by Hardware Source (with Same Count Cycle (GTPR Value))

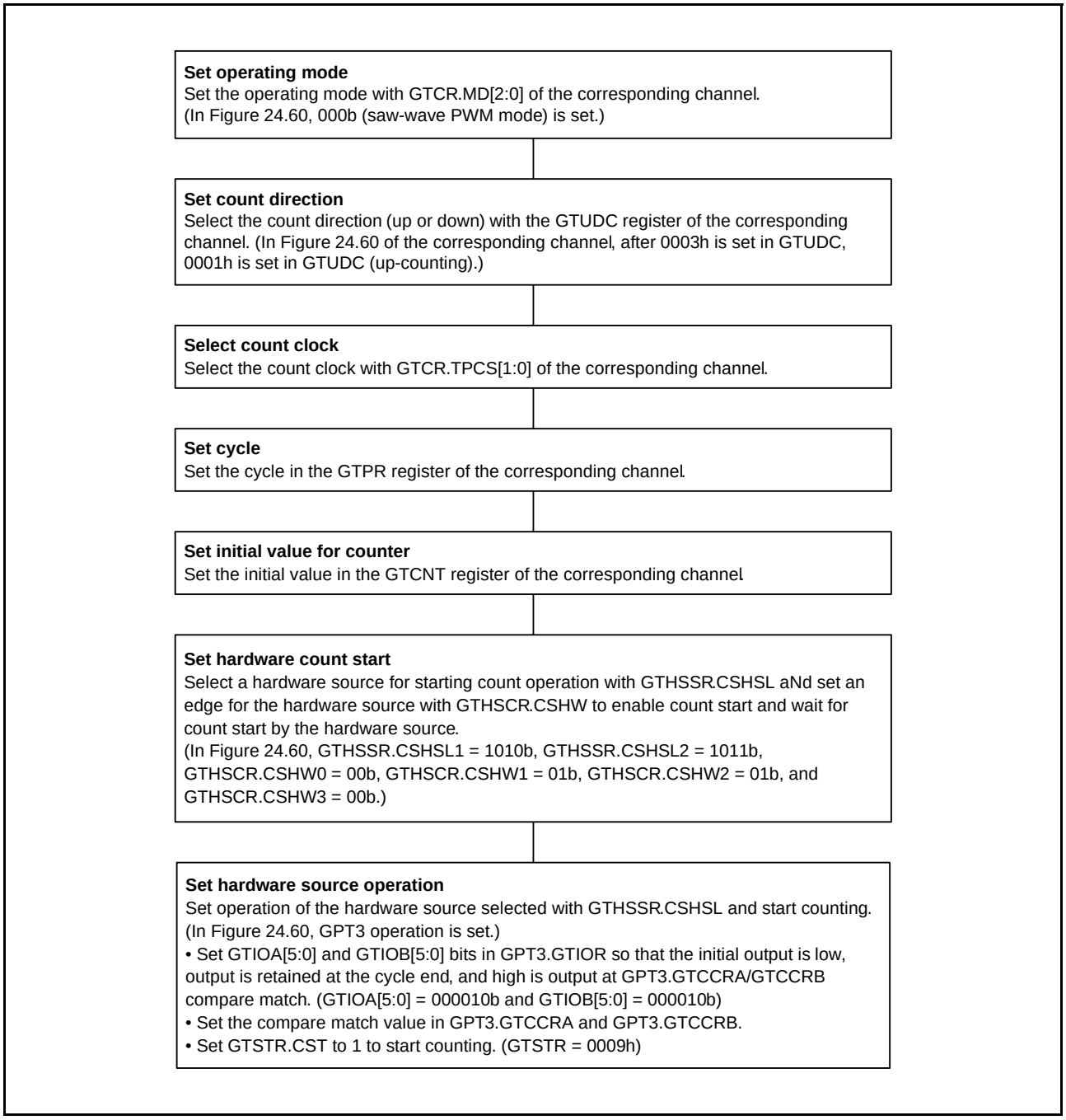


Figure 24.61 Example for Setting Phase Start by Hardware Source

24.3.8 PWM Output Operation Examples

(1) Synchronized PWM Output

The GPT can output eight phases of linked PWM waveforms for a maximum of four channels by synchronizing operation of the channels.

Figure 24.62 shows an example in which all the channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it will output low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

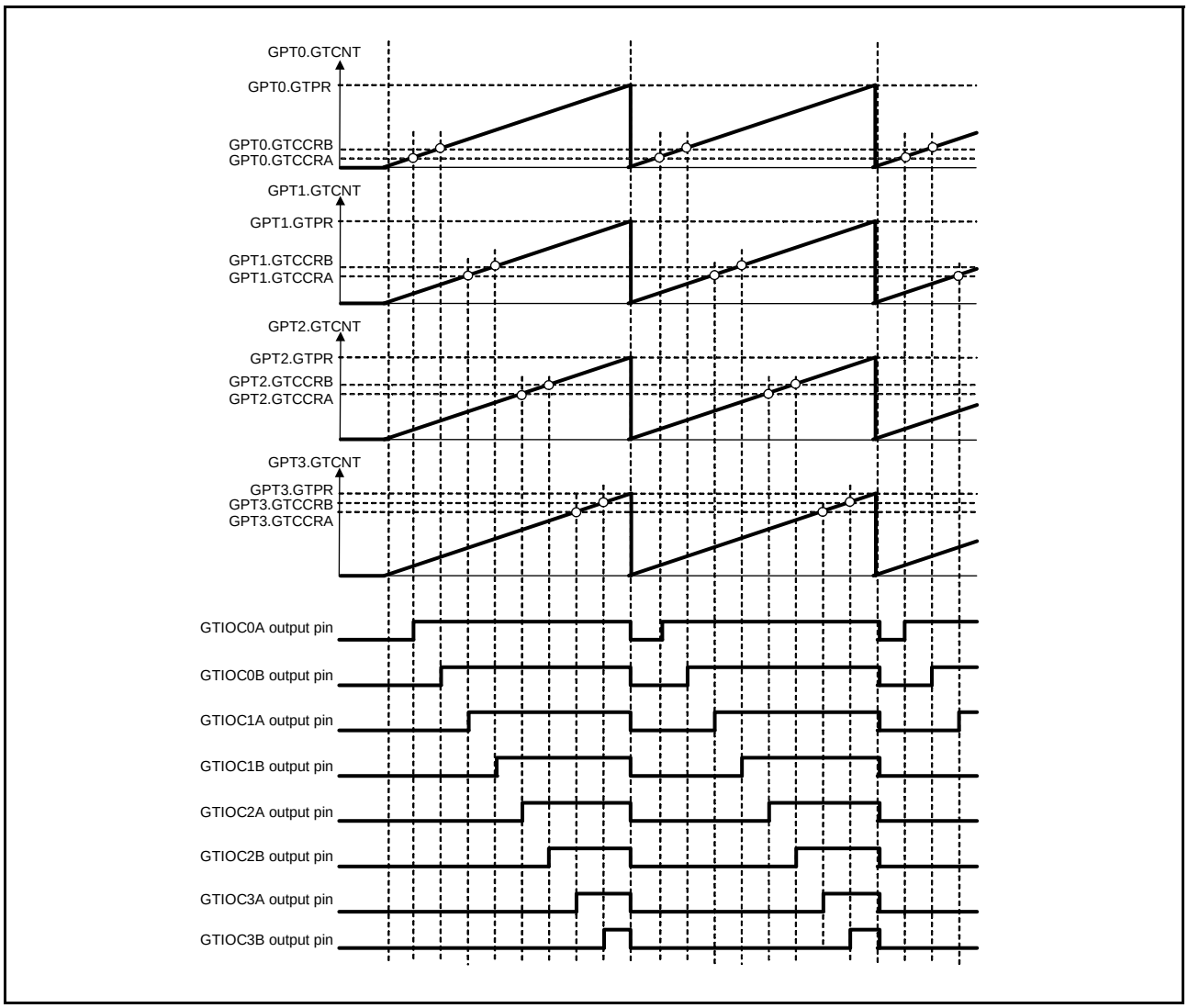


Figure 24.62 Example of Synchronized PWM Output

(2) Three-Phase Saw-Wave Complementary PWM Output

Figure 24.63 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it will output high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

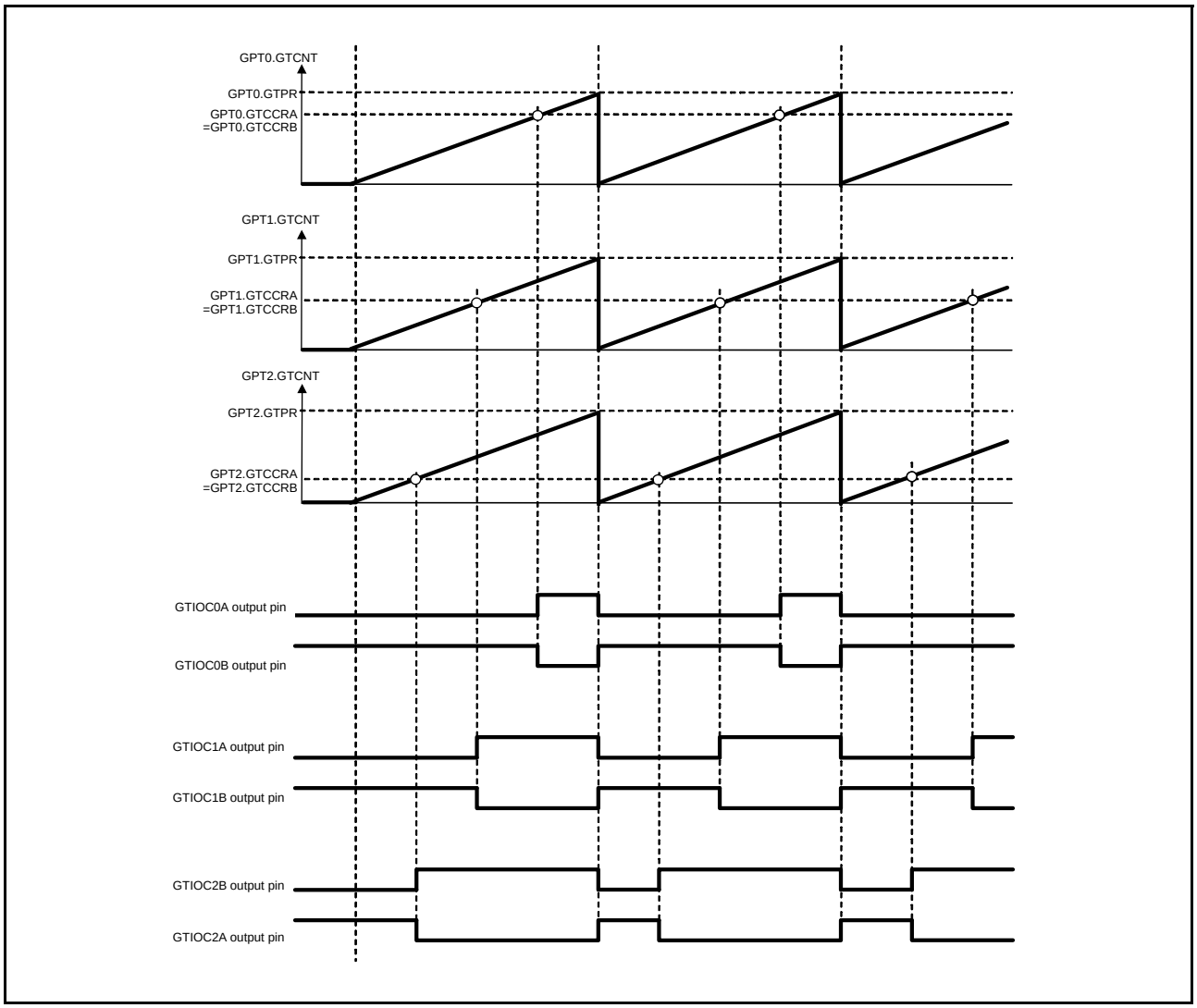


Figure 24.63 Example of Three-Phase Saw-Wave Complementary PWM Output

(3) Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 24.64 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

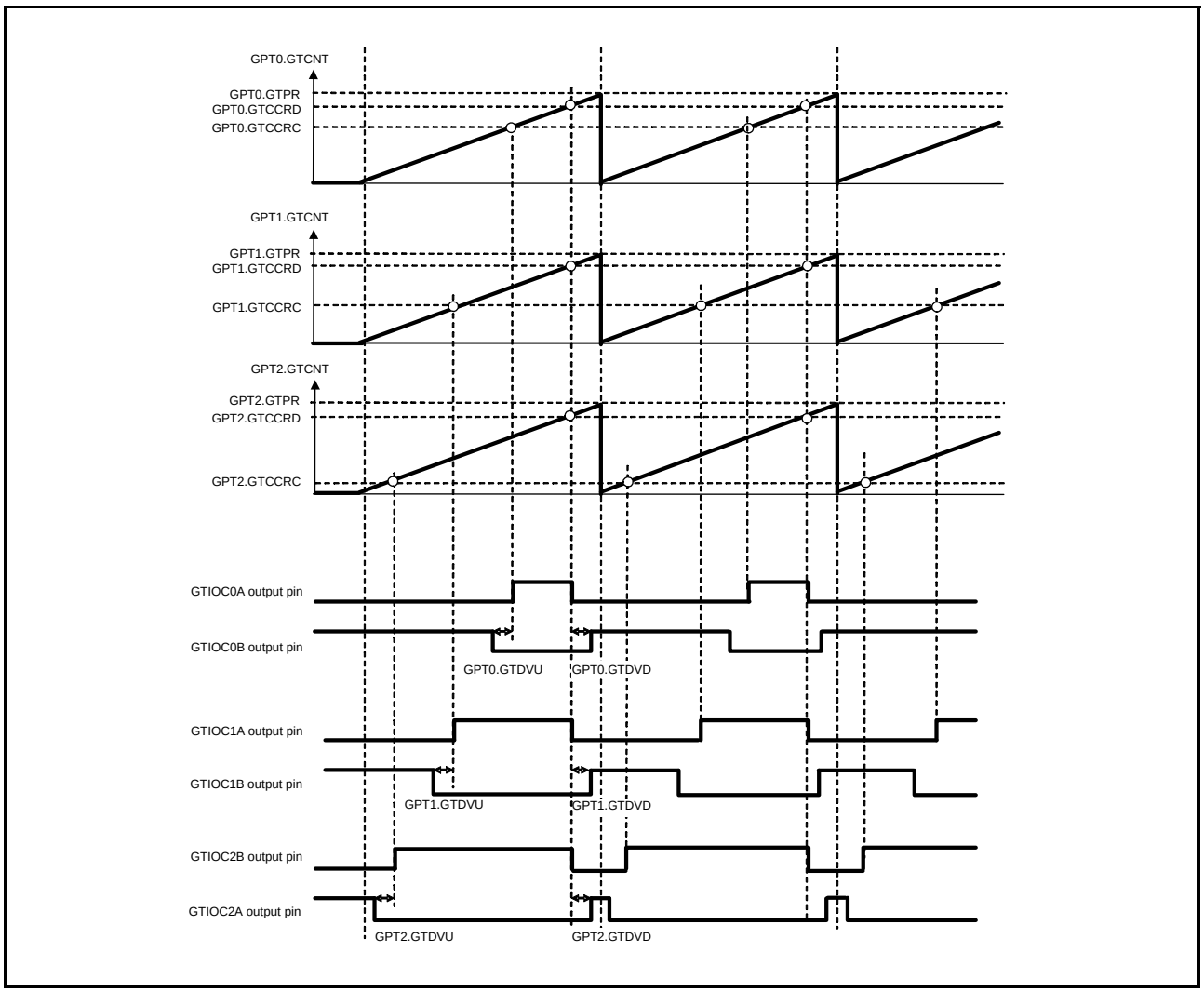


Figure 24.64 Example of Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

(4) Three-Phase Triangle-Wave Complementary PWM Output

Figure 24.65 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

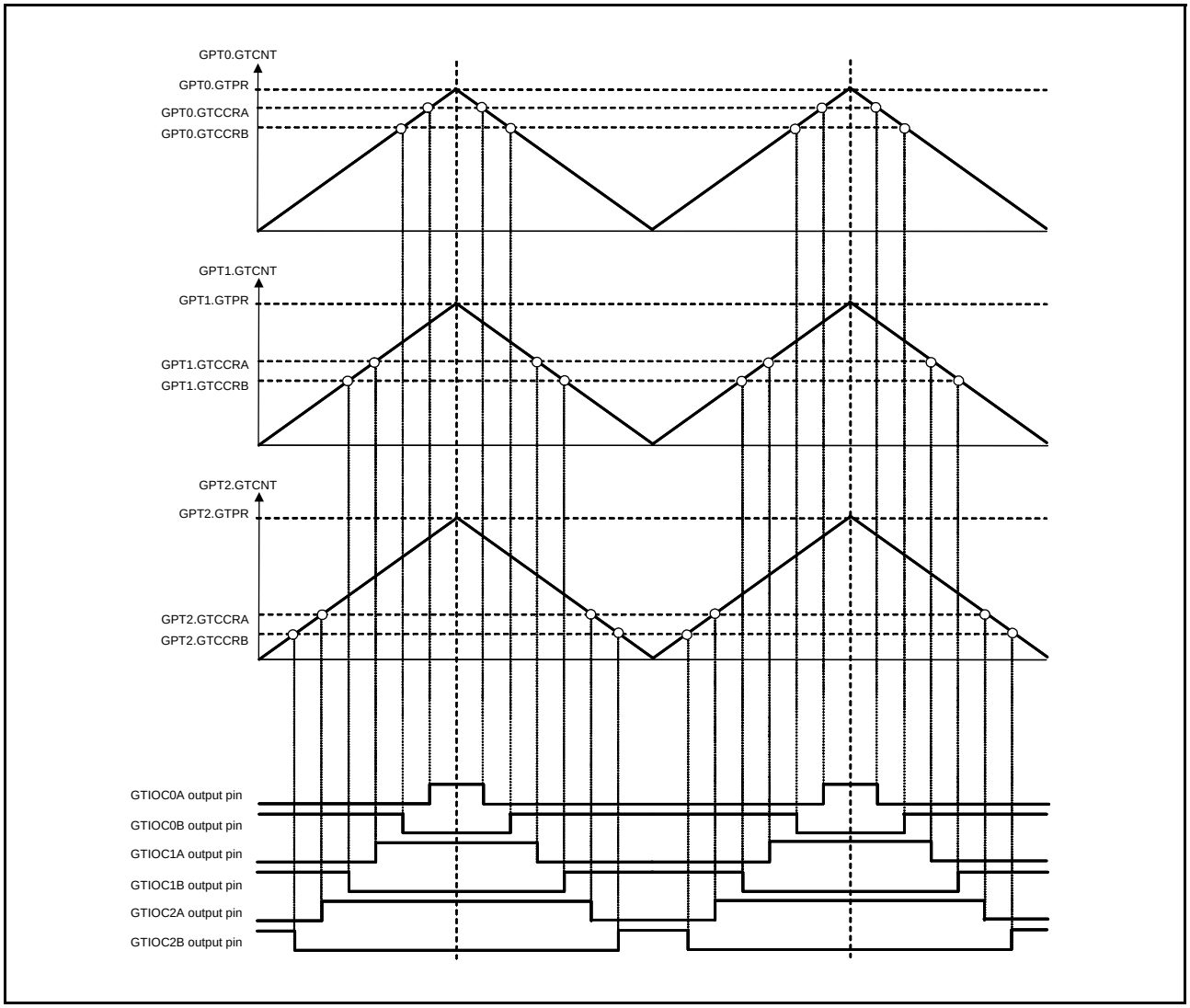


Figure 24.65 Example of Three-Phase Triangle-Wave Complementary PWM Output

(5) Three-Phase Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 24.66 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

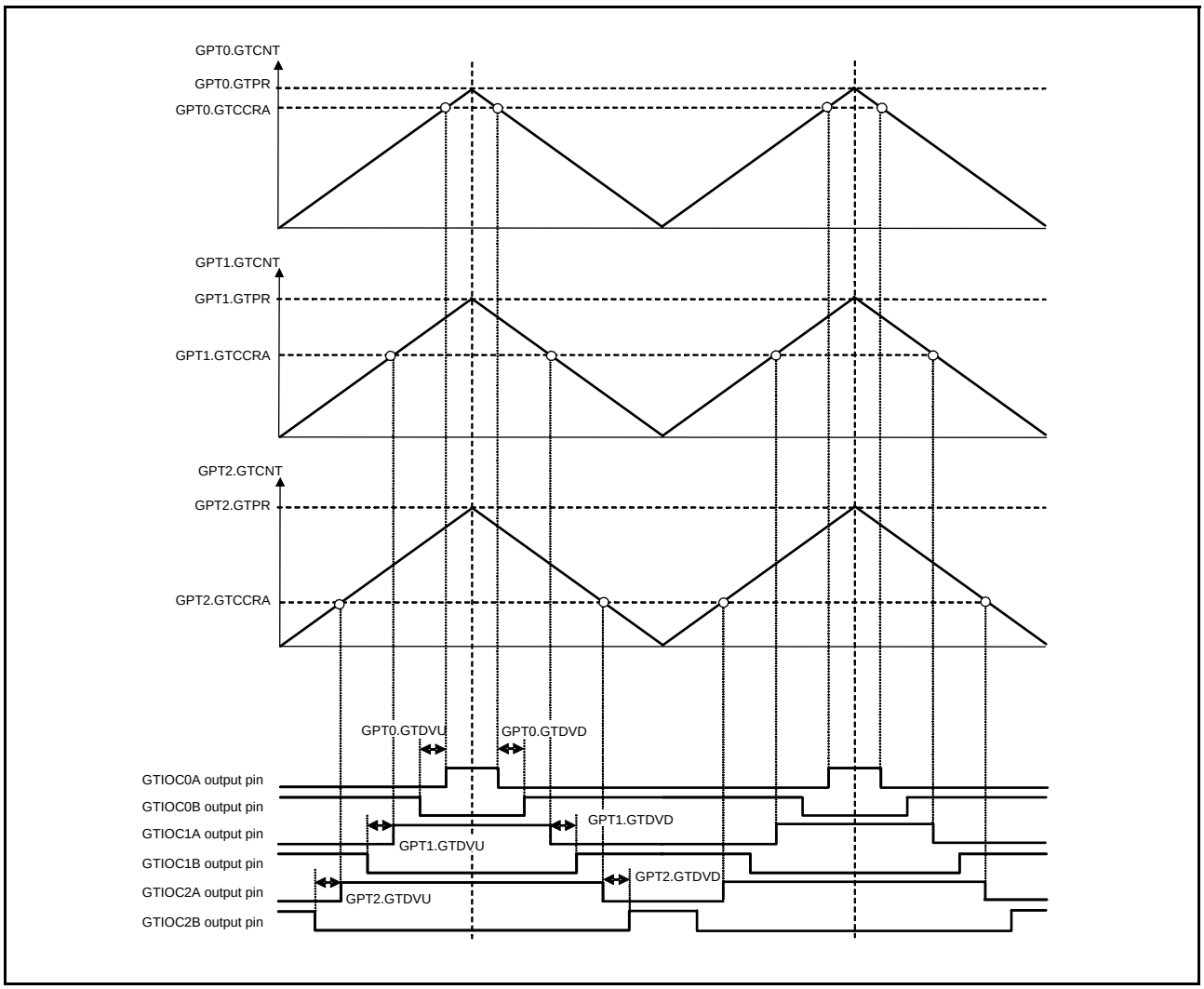


Figure 24.66 Example of Three-Phase Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

(6) Three-Phase Asymmetric Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 24.67 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

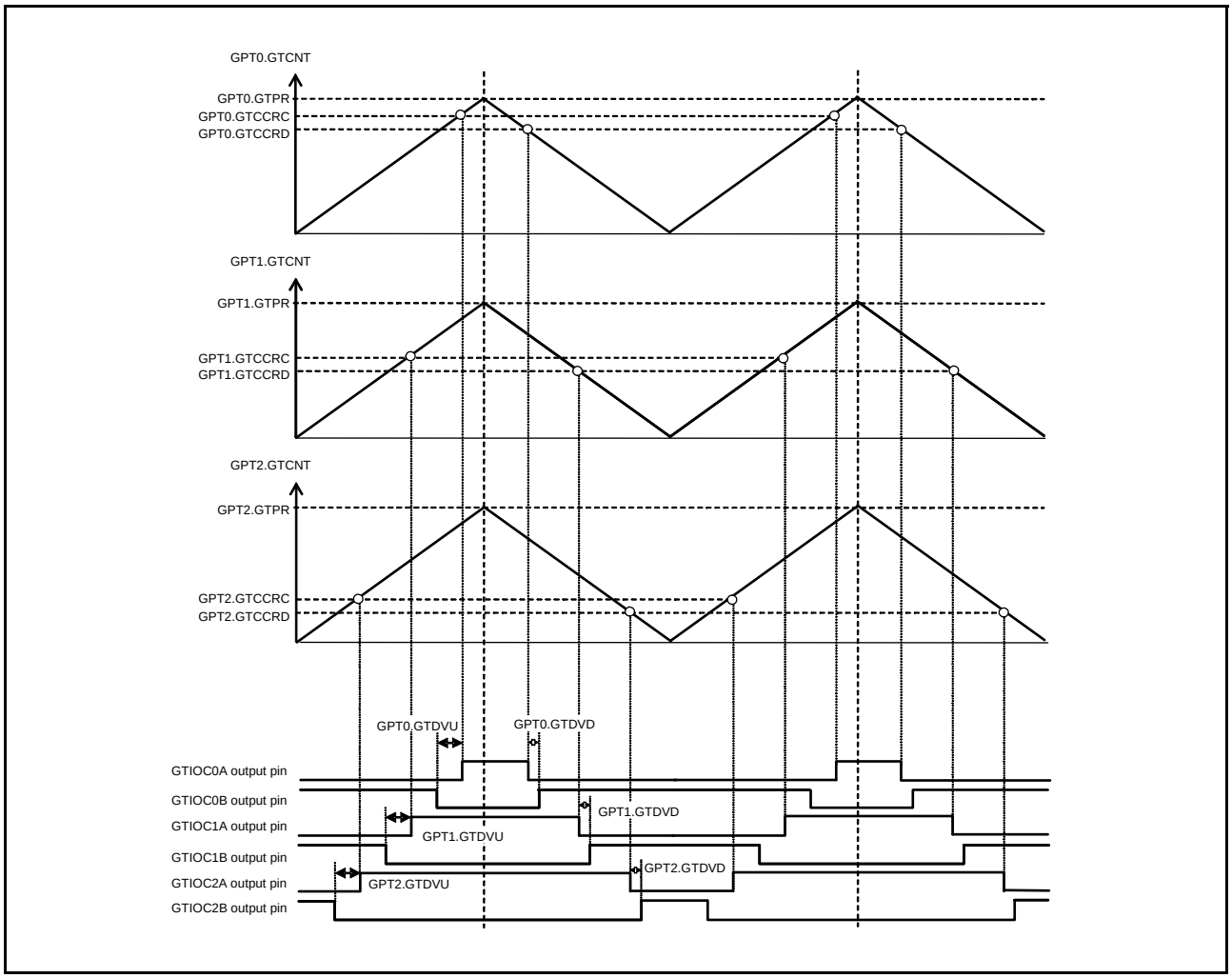


Figure 24.67 Example of Three-Phase Asymmetric Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

24.3.9 Adjustment to the Timing of Rising and Falling Edges in PWM Waveforms

The timing of rising and falling edges in PWM waveforms which are output from the GTIOCnA and GTIOCnB pins (n = 0 to 3) can be delayed to an accuracy of 1/32 of the system clock (PCLKA) period. If this is to be used, make sure that the system clock is running at a frequency no lower than 80 MHz.

If the timing of rising or falling edges in PWM waveforms output from the GTIOCnA and GTIOCnB pins is to be adjusted, make initial settings for the PWM generation circuit in accord with the procedure shown in Figure 24.68.

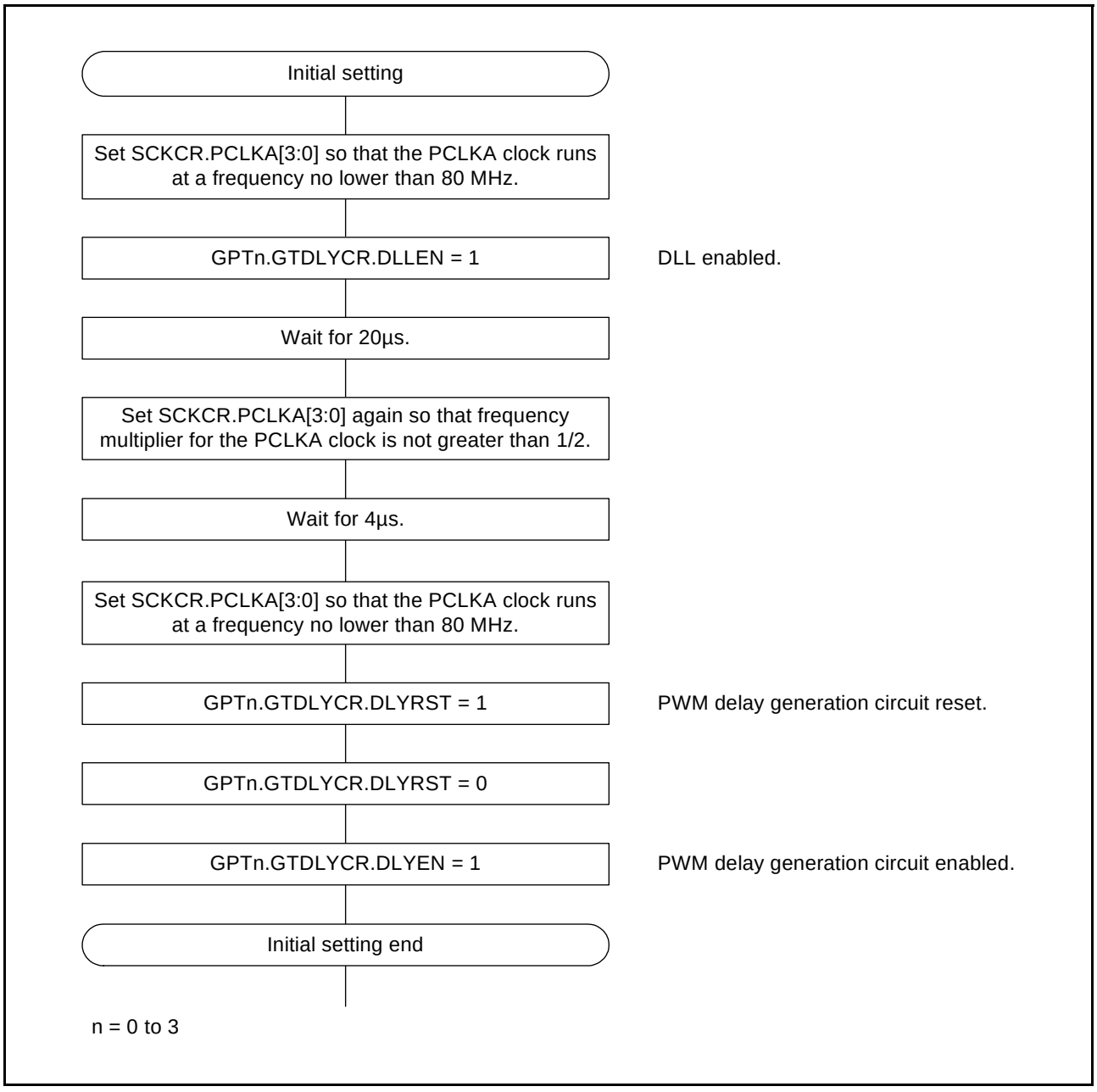


Figure 24.68 Example of PWM Delay Generation Circuit Initialization

In the PWM delay generation circuit, delays can be applied to rising and falling edges of the PWM outputs to an accuracy of 1/32 of the PCLKA clock. This is described in section section 24.3.3, PWM Output Operating Mode. The values of delay time are set in the GTDLYRA, GTLDYRB, GTDLYFA, and GTDLYFB registers. The set delay times are reflected in the PWM outputs with the timing described in section 24.3.10, Timing for Transfer of GTDLYRA, GTLDYRB, GTDLYFA, and GTDLYFB Register Settings. Table 24.6 lists the correspondences between the GTDLYRA, GTLDYRB, GTDLYFA, and GTDLYFB registers, and signals on the PWM output pins.

Table 24.6 Correspondence between PWM Output Pins and Delay Setting Registers

PWM Output Pin	Rising-Edge Delay Setting Register	Falling-Edge Delay Setting Register
GTIOC0A	GPT0.GTDLYRA	GPT0.GTDLYFA
GTIOC0B	GPT0.GTDLYRB	GPT0.GTDLYFB
GTIOC1A	GPT1.GTDLYRA	GPT1.GTDLYFA
GTIOC1B	GPT1.GTDLYRB	GPT1.GTDLYFB
GTIOC2A	GPT2.GTDLYRA	GPT2.GTDLYFA
GTIOC2B	GPT2.GTDLYRB	GPT2.GTDLYFB
GTIOC3A	GPT3.GTDLYRA	GPT3.GTDLYFA
GTIOC3B	GPT3.GTDLYRB	GPT3.GTDLYFB

When the PWM delay generation circuit is in use, the timing with which a PWM output signal rises and falls can be controlled to an accuracy of 1/32 of the period of the PCLKA clock. When this facility is not in use, the period of the PWM output waveform is controlled to an accuracy of one period of the input clock for the timer counter (which is PCLKA). That is, with the PWM delay generation circuit, the output can be controlled to an accuracy 32 times better. Furthermore, the delay settings also control the periods at high and low level for the PWM waveform to the given accuracy. Each of the four PWM channels includes a PWM delay generation circuit, and the circuits can be individually enabled or disabled.

24.3.10 Timing for Transfer of GTDLYRA, GTLDYRB, GTDLYFA, and GTDLYFB Register Settings

Settings for the GTDLYRA, GTLDYRB, GTDLYFA, and GTDLYFB registers are initially transferred to a temporary registers, and then reflected in the amounts of delay on the GTIOCnA and GTIOCnB (n = 0 to 3) outputs. Transfer of the settings takes place on overflows (counting up) or underflow (counting down) for saw waves, and in the troughs of triangle waves.

Figure 24.69 shows an operation example of GTDLYRA and Figure 24.70 shows an operation example of GTDLYFA.

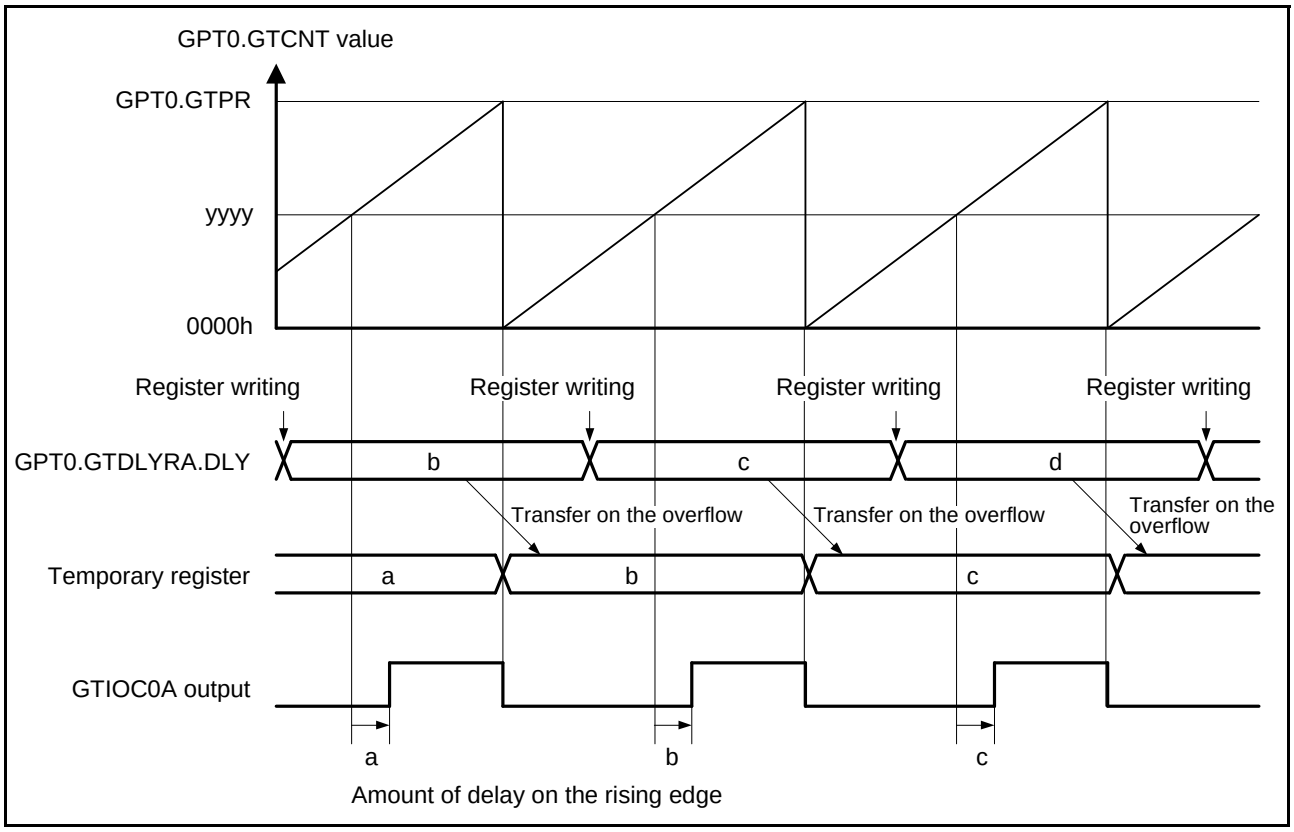


Figure 24.69 GTDLYRA Operation (Sawtooth Waveform PWM)

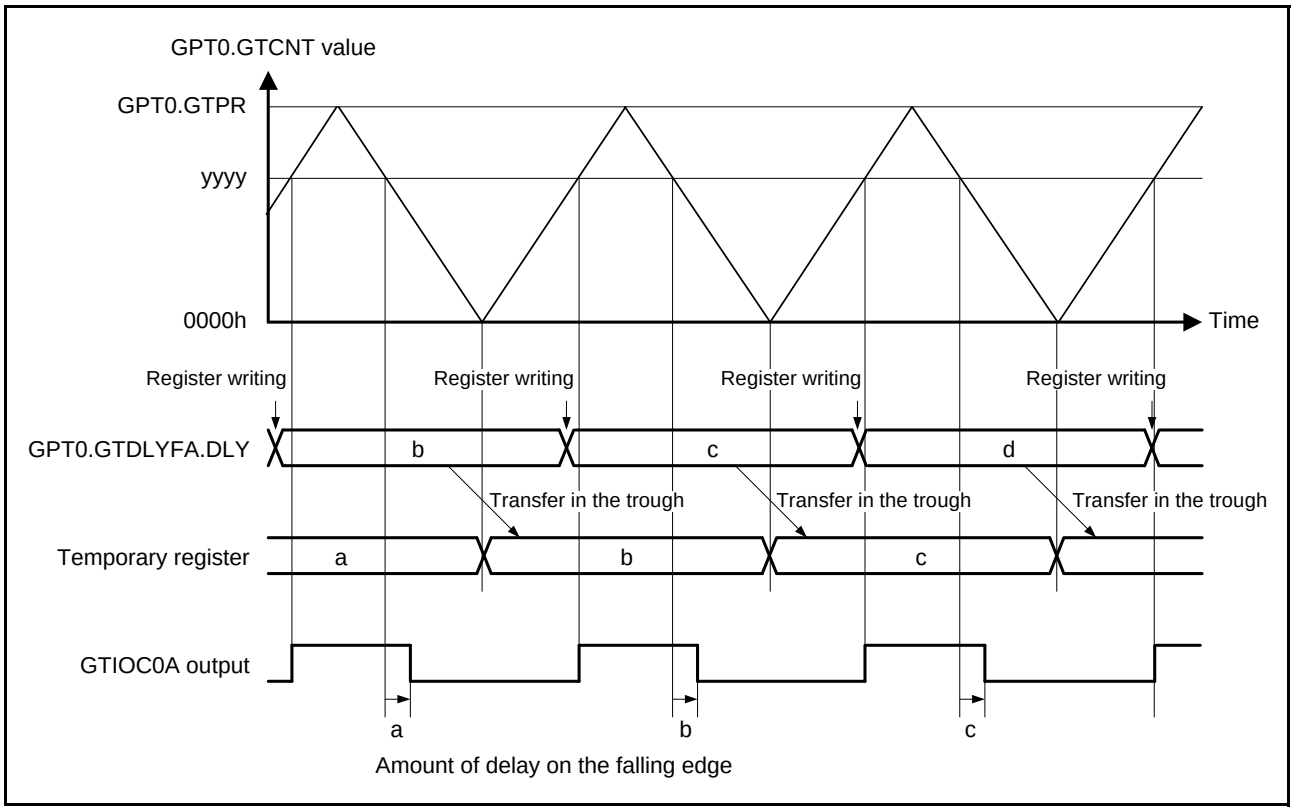


Figure 24.70 GTDLYFA Operation (Triangle Waveform PWM)

24.4 Interrupt Sources

24.4.1 Interrupt Sources and Priorities

There are four kinds of GPT interrupt sources; GTCCR input capture/compare match, GTCNT counter overflow (GTPR compare match)/underflow, dead time error, and IWDTCLK count function interrupt. Each interrupt source has its own status flag and enable/disable bit, allowing the generation of interrupt request signals to be enabled or disabled individually

When an interrupt source is generated, the corresponding status flag in GTST is set to 1. If the corresponding enable/disable bit in GTINTAD is set to 1 at this time, an interrupt is requested.

However, if a further interrupt is generated while the corresponding status flag is 1, the interrupt will be ignored. To enable the acceptance of an interrupt, the flag of the interrupt generation source should be 0.

Relative channel priorities can be changed by the interrupt controller; however the priority within a channel is fixed. For details, see section 15, Interrupt controller (ICUb). Table 24.7 lists the GPT interrupt sources.

Table 24.7 GPT Interrupt Sources (1/2)

Channel	Name	Interrupt Source		Interrupt Flag	DMAC/DTC Activation	Priority
0	GTCIA0	GPT0.GTCCRA input capture/compare match		TCFA	Possible	High
	GTCIB0	GPT0.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC0	GPT0.GTCCRC compare match		TCFC	Possible	
		GPT0.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE0	GPT0.GTCCRE compare match		TCFE	Possible	
		GPT0.GTCCRF compare match		TCFF		
	GTCIV0	GPT0.GTCNT overflow (GPT0.GTPR compare match)		TCFPO	Possible	
		GPT0.GTCNT underflow		TCFPU		
	LOCOI	IWDTCLK count function interrupt	LCNT overflow	LISO	Possible	
			IWDTCLK count value deviation exceedance	LISD		
			Frequency-divided IWDTCLK clock rise	LISC		
		External trigger input	External trigger falling input	ETINF		
			External trigger rising input	ETIPF		
1	GTCIA1	GPT1.GTCCRA input capture/compare match		TCFA	Possible	
	GTCIB1	GPT1.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC1	GPT1.GTCCRC compare match		TCFC	Possible	
		GPT1.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE1	GPT1.GTCCRE compare match		TCFE	Possible	
		GPT1.GTCCRF compare match		TCFF		
	GTCIV1	GPT1.GTCNT overflow (GPT1.GTPR compare match)		TCFPO	Possible	
		GPT1.GTCNT underflow		TCFPU		
2	GTCIA2	GPT2.GTCCRA input capture/compare match		TCFA	Possible	
	GTCIB2	GPT2.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC2	GPT2.GTCCRC compare match		TCFC	Possible	
		GPT2.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE2	GPT2.GTCCRE compare match		TCFE	Possible	
		GPT2.GTCCRF compare match		TCFF		
	GTCIV2	GPT2.GTCNT overflow (GPT2.GTPR compare match)		TCFPO	Possible	
		GPT2.GTCNT underflow		TCFPU		
3	GTCIA3	GPT3.GTCCRA input capture/compare match		TCFA	Possible	
	GTCIB3	GPT3.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC3	GPT3.GTCCRC compare match		TCFC	Possible	
		GPT3.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE3	GPT3.GTCCRE compare match		TCFE	Possible	
		GPT3.GTCCRF compare match		TCFF		
	GTCIV3	GPT3.GTCNT overflow (GPT3.GTPR compare match)		TCFPO	Possible	
		GPT3.GTCNT underflow		TCFPU		Low

Table 24.7 GPT Interrupt Sources (2/2)

Channel	Name	Interrupt Source		Interrupt Flag	DMAC/DTC Activation	Priority
4	GTCIA4	GPT4.GTCCRA input capture/compare match		TCFA	Possible	High
	GTCIB4	GPT4.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC4	GPT4.GTCCRC compare match		TCFC	Possible	
		GPT4.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE4	GPT4.GTCCRE compare match		TCFE	Possible	
		GPT4.GTCCRF compare match		TCFF		
	GTCIV4	GPT4.GTCNT overflow (GPT4.GTPR compare match)		TCFPO	Possible	
		GPT4.GTCNT underflow		TCFPU		
	LOCOI	IWDTCLK count function interrupt	LCNT overflow	LISO	Possible	
			IWDTCLK count value deviation exceedance	LISD		
			Frequency-divided IWDTCLK clock rise	LISC		
		IWDTCLK count function interrupt	LCNT overflow	ETINF		
			IWDTCLK count value deviation exceedance	ETIPF		
5	GTCIA5	GPT5.GTCCRA input capture/compare match		TCFA	Possible	
	GTCIB5	GPT5.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC5	GPT5.GTCCRC compare match		TCFC	Possible	
		GPT5.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE5	GPT5.GTCCRE compare match		TCFE	Possible	
		GPT5.GTCCRF compare match		TCFF		
	GTCIV5	GPT5.GTCNT overflow (GPT1.GTPR compare match)		TCFPO	Possible	
		GPT5.GTCNT underflow		TCFPU		
6	GTCIA6	GPT6.GTCCRA input capture/compare match		TCFA	Possible	
	GTCIB6	GPT6.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC6	GPT6.GTCCRC compare match		TCFC	Possible	
		GPT6.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE6	GPT6.GTCCRE compare match		TCFE	Possible	
		GPT6.GTCCRF compare match		TCFF		
	GTCIV6	GPT6.GTCNT overflow (GPT2.GTPR compare match)		TCFPO	Possible	
		GPT6.GTCNT underflow		TCFPU		
7	GTCIA7	GPT7.GTCCRA input capture/compare match		TCFA	Possible	
	GTCIB7	GPT7.GTCCRB input capture/compare match		TCFB	Possible	
	GTCIC7	GPT7.GTCCRC compare match		TCFC	Possible	
		GPT7.GTCCRD compare match		TCFD		
		Dead time error		DTEF		
	GTCIE7	GPT7.GTCCRE compare match		TCFE	Possible	
		GPT7.GTCCRF compare match		TCFF		
	GTCIV7	GPT7.GTCNT overflow (GPT3.GTPR compare match)		TCFPO	Possible	
		GPT7.GTCNT underflow		TCFPU		Low

Note 1. This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

(1) Input Capture/Compare Match Interrupt

If the corresponding interrupt enable bit in GTINTAD is 1 when a GTCCR input capture/compare match in each channel occurs, an interrupt is requested.

(2) Overflow/Underflow (Periodic) Interrupt

A periodic interrupt whose generation interval is determined by GTPR of each channel can be generated.
For saw-waves, the GTST.TCFPO flag is set to 1 when the GTCNT counter value matches GTPR (overflow) in up-count operation, the GTST.TCFPU flag is set to 1 when GTCNT reaches 0 (underflow) in down-count operation, and a GTCIV interrupt request is generated if the bits that correspond to GTINTPR.GTINTPR[1:0] are set to 01b, 10b, or 11b.
For triangle waves, GTST.TCFPO flag is set to 1 when the GTCNT counter value matches GTPR (crest) in up-count operation, the GTST.TCFPU flag is set to 1 when GTCNT reaches 0 (trough) in down-count operation, and a GTCIV interrupt request is generated if bits that correspond to GTINTPR.GTINTPR[1:0] are set to 01b, 10b, or 11b.

(3) IWDTCLK Count Function Interrupt

When the frequency-divided IWDTCLK clock rising is detected, IWDTCLK count value exceeds the specified deviation, or an overflow occurs in the LCNT counter, the corresponding status flag in LCST is set to 1. If the corresponding interrupt enable bit in LCCR is 1 at this time, a LOCOI interrupt request is generated.
Similarly, when the GTETRG external trigger input rising or falling is detected, the corresponding status flag in GTETINT is set to 1. If the corresponding interrupt enable bit in GTETINT is 1 at this time, a LOCOI interrupt request is generated.

(4) Dead Time Error Interrupt

When automatic dead time setting has been made, the GTST.DTEF flag becomes 1 when the timer output toggle point with dead time added exceeds the timer cycle. If GTINTAD.EINT is 1 at this time, a LOCOI interrupt request is generated.

Table 24.8 Interrupt Signals, Interrupt Enable Bits, and Status Flags

Interrupt Signal	Interrupt Enable Bit	Status Flag
GTCIV	GTINTAD[7:6](GTINTPR[1:0])	GTST[7] (TCFPU)
		GTST[6] (TCFPO)
GTCIE	GTINTAD[5] (GTINTF)	GTST[5] (TCFF)
	GTINTAD[4] (GTINTE)	GTST[4] (TCFE)
GTCIC	GTINTAD[11](EINT)	GTST[11] (DTEF)
	GTINTAD[3] (GTINTD)	GTST[3] (TCFD)
	GTINTAD[2] (GTINTC)	GTST[2] (TCFC)
GTCIB	GTINTAD[1] (GTINTB)	GTST[1] (TCFB)
GTCIA	GTINTAD[0] (GTINTA)	GTST[0] (TCFA)
LOCOI	LCCR[6] (LCINTO)	LCST[2] (LISO)
	LCCR[5] (LCINTD)	LCST[1] (LISD)
	LCCR[4] (LCINTC)	LCST[0] (LISC)
	GTETINT[1] (ETINEN)	GTETINT[9] (ETINF)
	GTETINT[0] (ETIPEN)	GTETINT[8] (ETIPF)

(5) Notes on Using Multiple Interrupt Sources Simultaneously

Special care is required when one interrupt is shared by multiple interrupt sources such as GTCICn, GTCIEn, GTCIVn, and LOCOI (n = 0 to 7). While the ICUA interrupt request flag (IR flag) is 1, which is set by a certain source (e.g., TCFC flag for GTCICn), if another source (TCFD flag) sharing the same interrupt (GTCICn) is generated to request the interrupt, the interrupt request caused by another source (TCFD flag) is ignored. Therefore, when using multiple interrupt sources sharing the same interrupt simultaneously, check all the flags for the interrupt sources used and execute the appropriate processes according to the asserted source flags in the interrupt processing routine.

24.4.2 DMAC or DTC Activation

The DTC or DMAC can be activated by the interrupt in each channel. For details, see section 15, Interrupt controller (ICUb), section 18, DMA Controller (DMACA), and section 19, Data Transfer Controller (DTCa).
However, as similar to the interrupt handling, if a further DTC or DMAC activation request is generated while the corresponding status flag is 1, the interrupt will be ignored. To enable the acceptance of an interrupt, the flag of the interrupt generation source should be 0.

24.4.3 Interrupt and A/D Conversion Request Skipping Function

By setting the GTITC register, the GTCNT counter overflows (GTPR compare matches)/underflow interrupts (GTCIV) can be skipped. Other interrupts and A/D converter start request signals can be skipped in coordination with the GTCIV skipping function. However, the dead time error interrupts cannot be linked with the GTCIV skipping function. If an interrupt is skipped, the change in the corresponding status flag is also skipped and the skipping function operates while the status flag is set.
When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times of skipping is odd, GTCIV interrupt requests cannot be generated at troughs only or at crests only depending on the skipping counter start timing. Therefore, in order to count both troughs and crests and generate the GTCIV interrupts at troughs only or crests only in triangle-wave mode, the number of times of skipping should be even.
Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GTCIV interrupt requests cannot be generated at overflows only or at underflows only. Therefore, in order to count both overflows and underflows with the count direction changed and generate the GTCIV interrupts at overflows only or underflows only in saw wave mode, the skipping state should be carefully checked before using.
When changing the skipping count, be sure to release the skipping count setting (GTITC.IVTC[1:0] = 00b).
Figure 24.71 to Figure 24.76 show examples of skipping function operation.

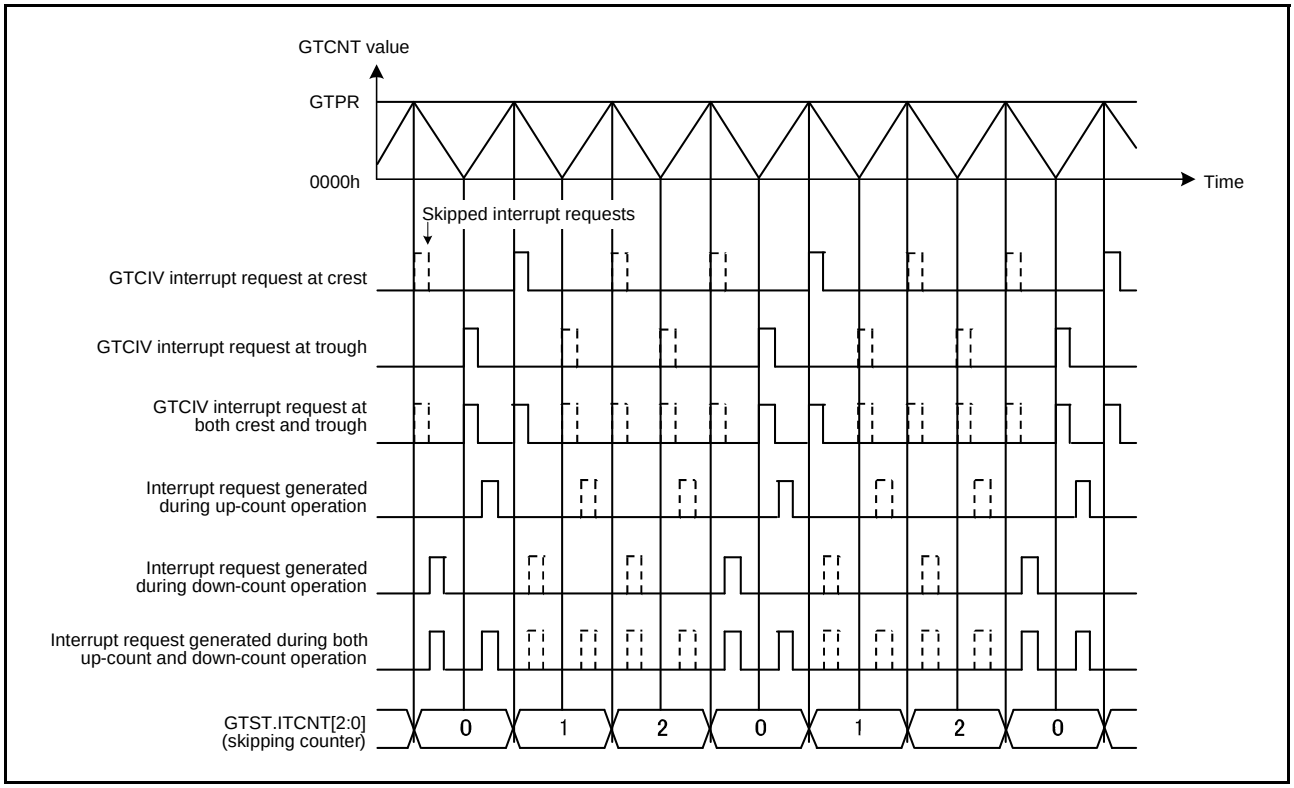


Figure 24.71 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Crests, Skipping Count: 2)

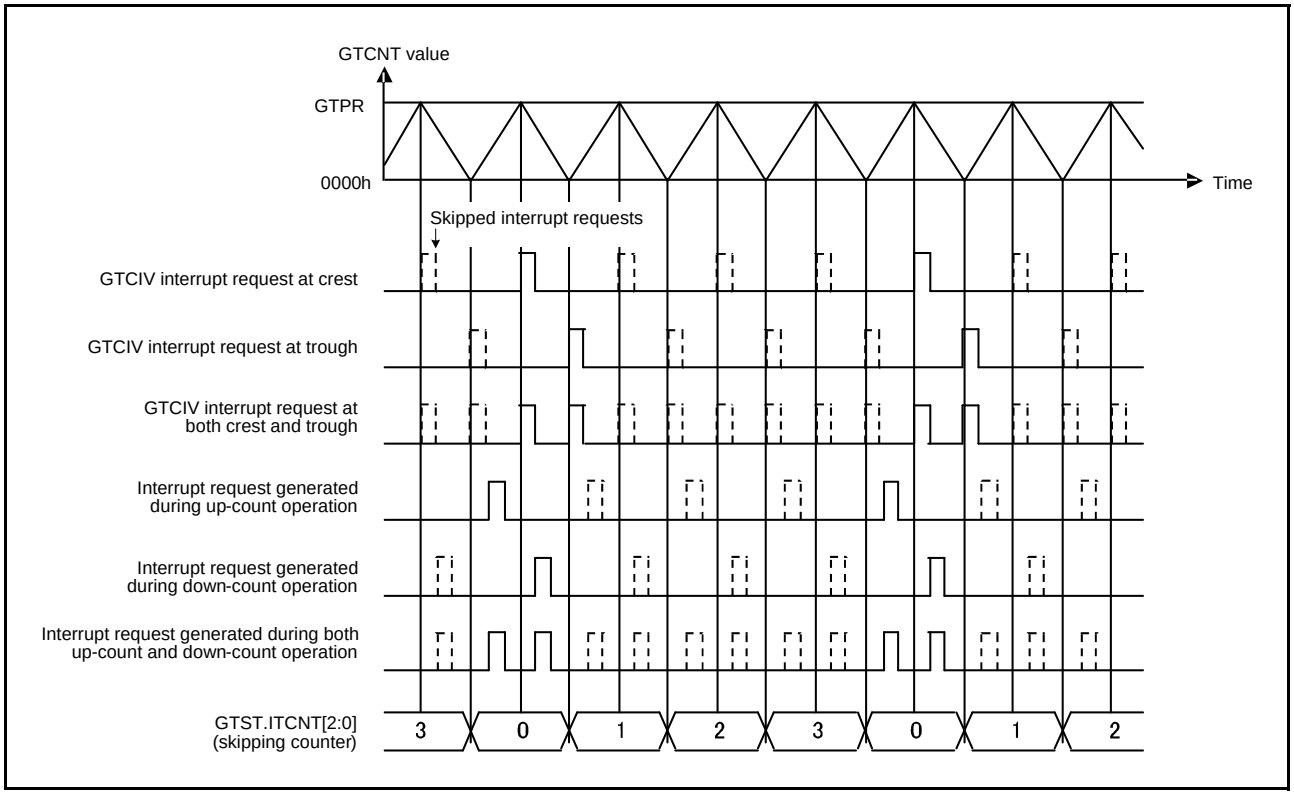


Figure 24.72 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Troughs, Skipping Count: 3)

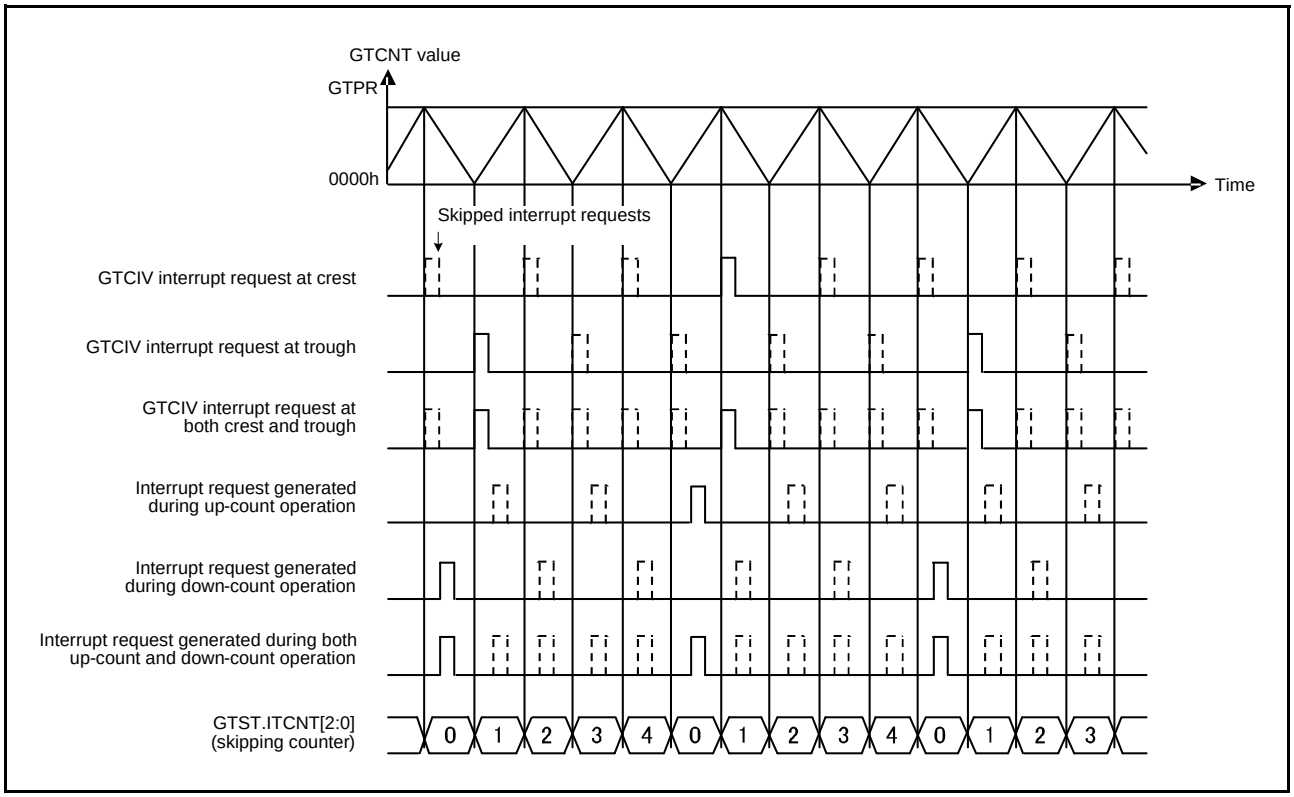


Figure 24.73 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 4)

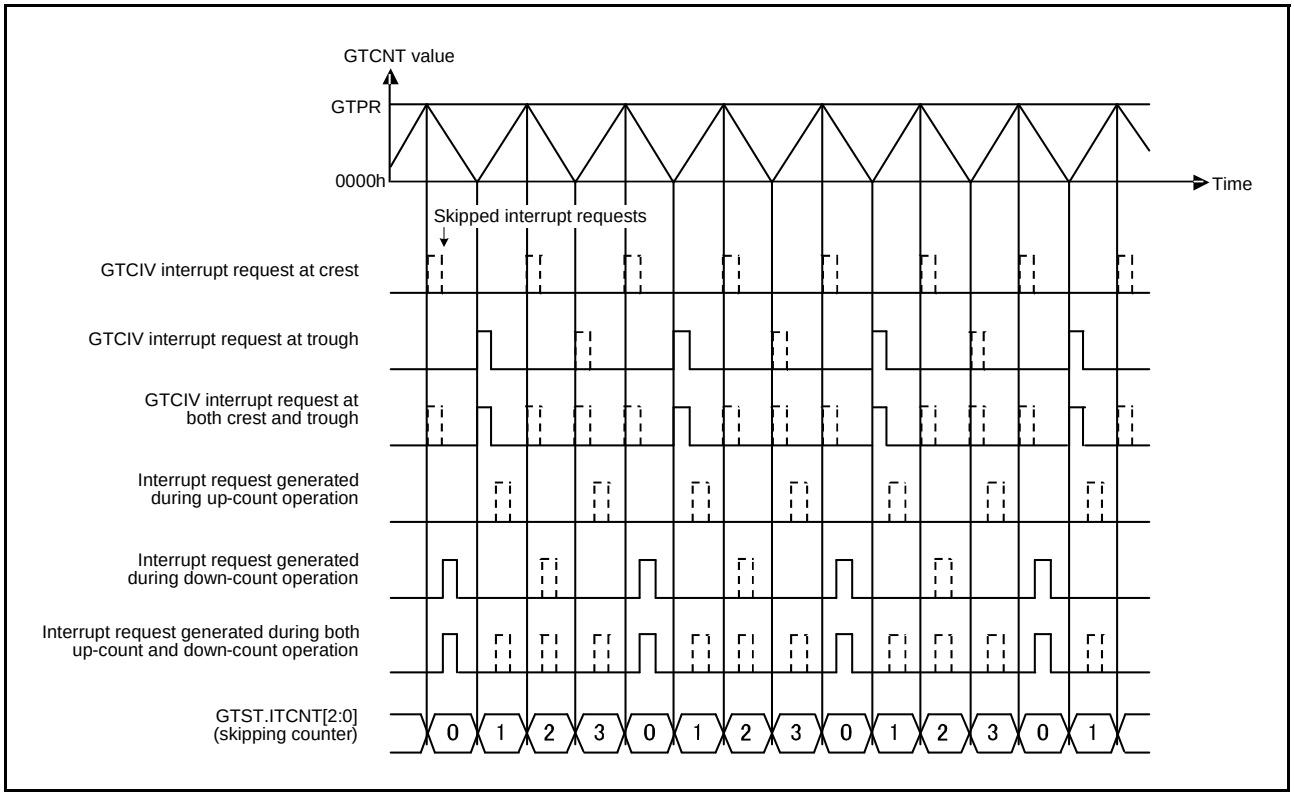


Figure 24.74 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Up-Counting)

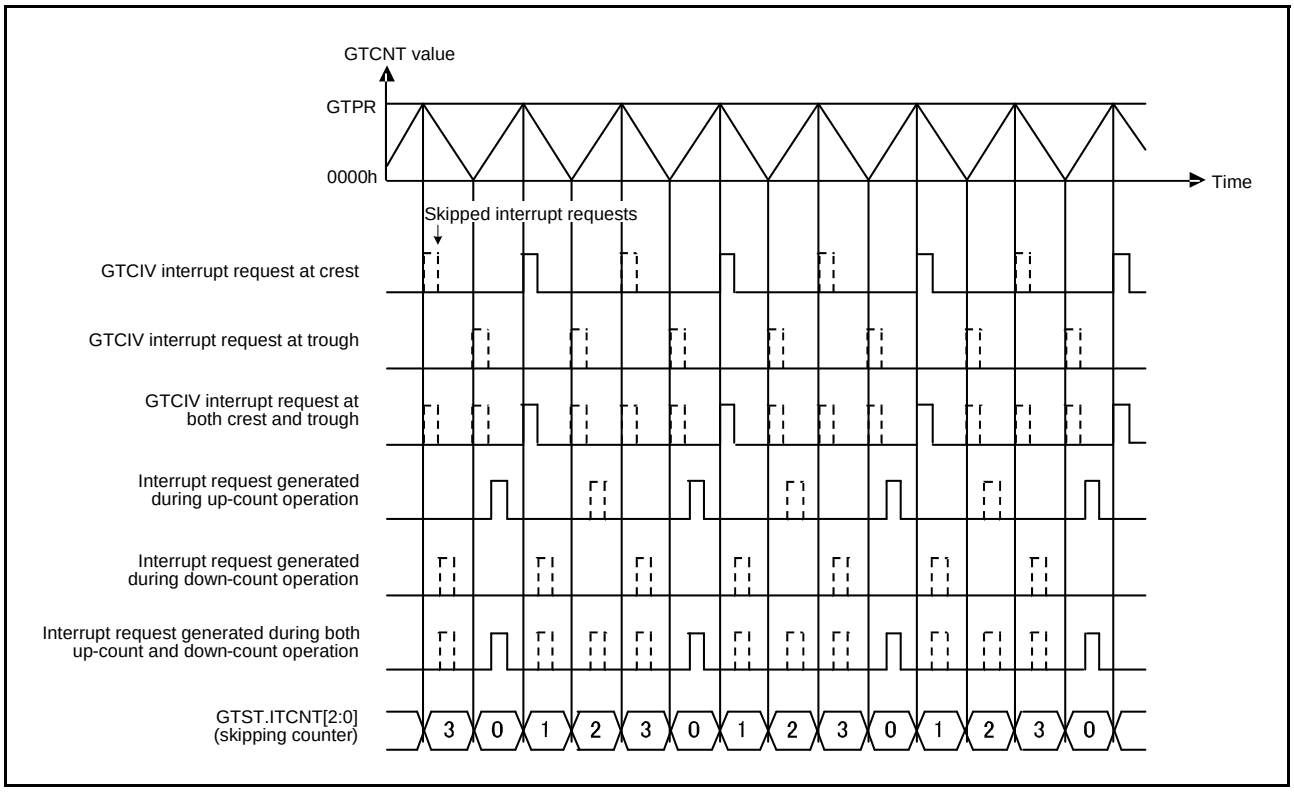


Figure 24.75 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Down-Counting)

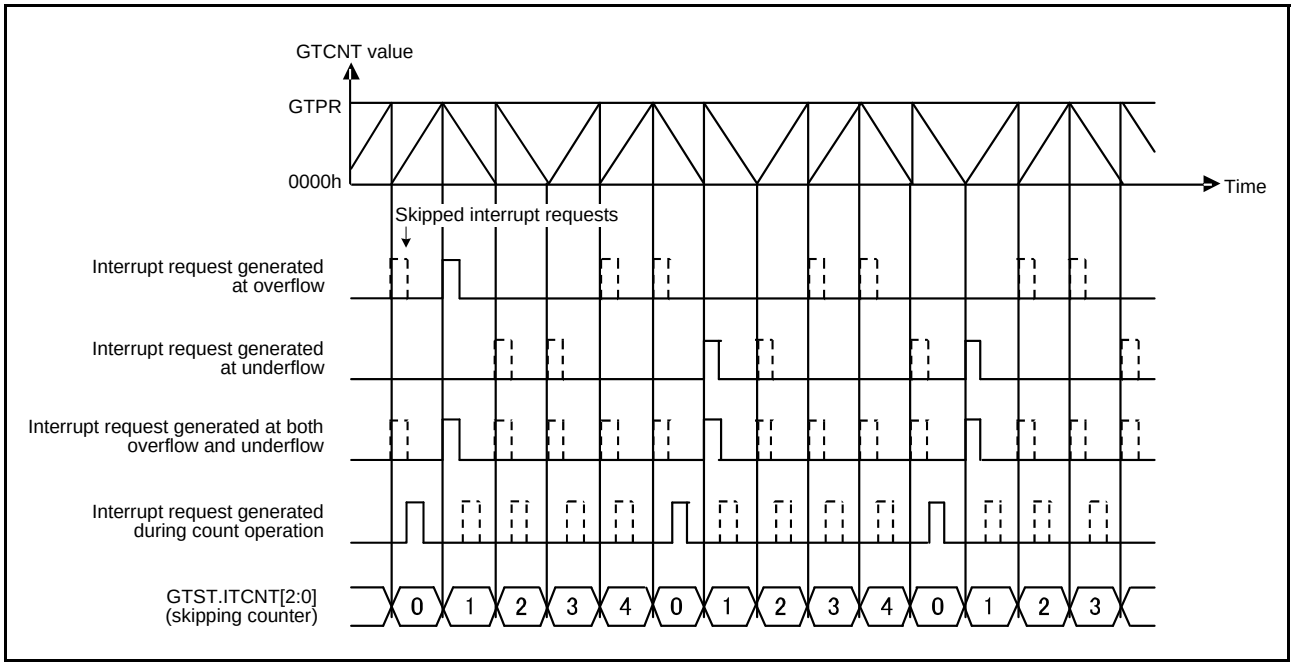


Figure 24.76 Example of Interrupt Skipping Function Operation (Saw Waves, Operation with Count Direction Changed, Counting and Skipping Both Overflows and Underflows, Skipping Count: 4)

24.5 A/D Converter Start Request

An A/D converter start request can be issued at a compare match between the GTCNT counter and GTADTRA or GTADTRB, and up-counting only, down-counting only, or both up-counting and down-counting can be specified. GTADTRA and GTADTRB each has two buffer registers. Buffer operation with GTADTRA used together with GTADTBRA and GTADTDBRA, and buffer operation with GTADTRB used together with GTADTBRB and GTADTDBRB can be performed.

Figure 24.77 shows an example of A/D converter start request operation, and Figure 24.78 shows an example for setting A/D converter start request operation.

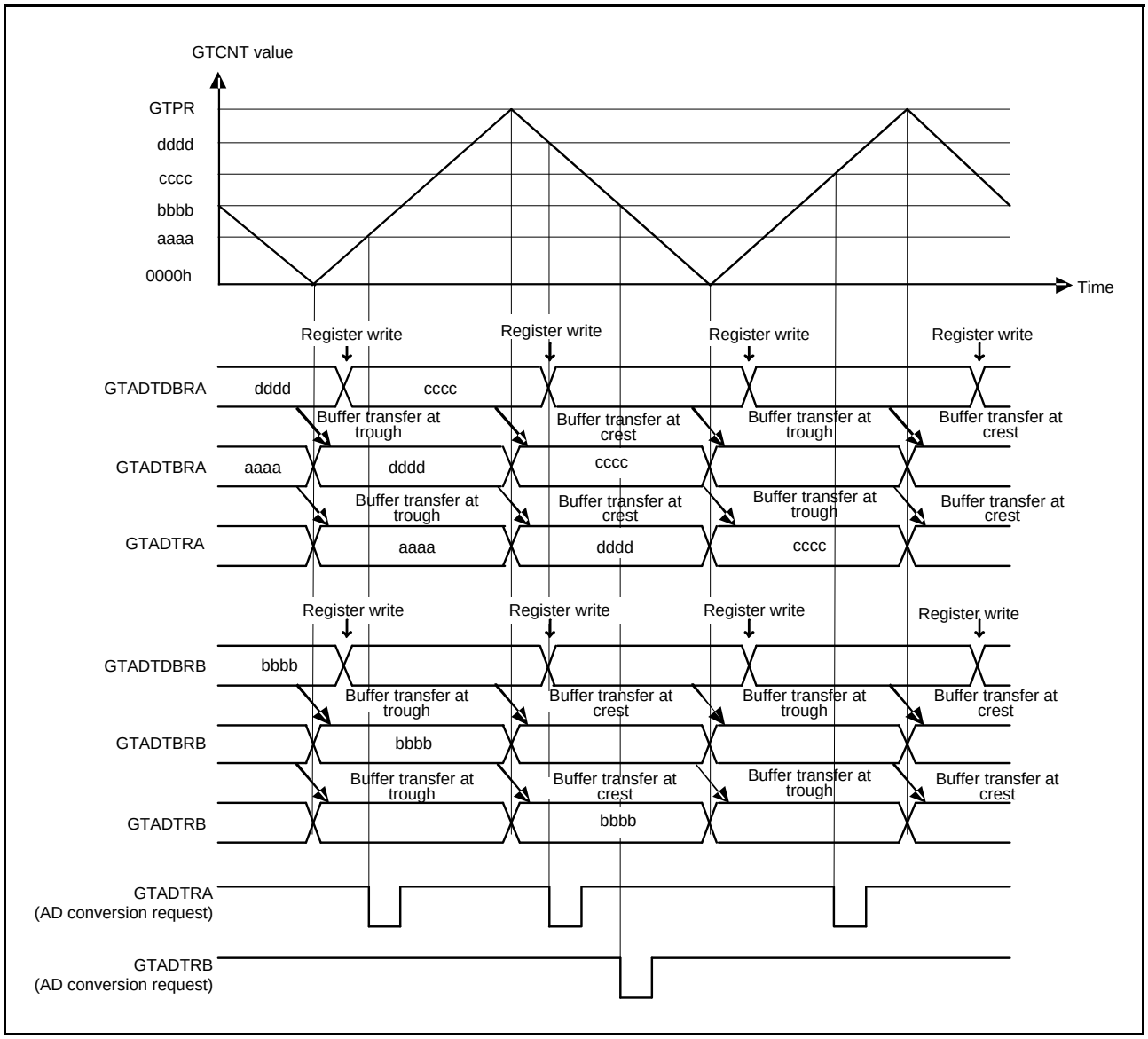


Figure 24.77 Example of A/D Converter Start Request Timing Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests, A/D Converter Start Requested by GTADTRA0 at Both Up-Counting and Down-Counting, A/D Converter Start Requested by GTADTRB0 at Down-Counting)

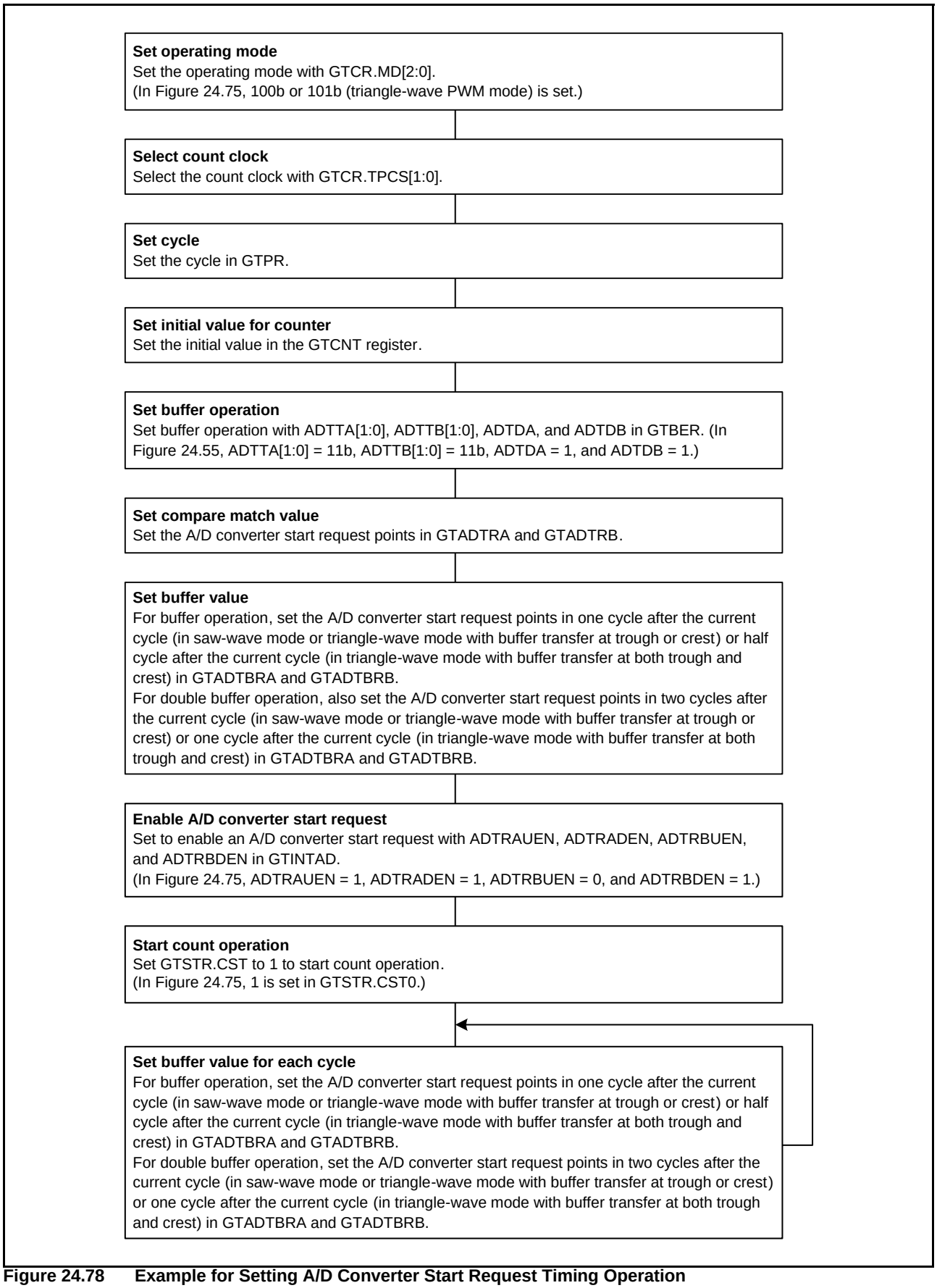


Figure 24.78 Example for Setting A/D Converter Start Request Timing Operation

24.6 IWDTCLK Count Function

The GPT can measure the cycle of the frequency-divided IWDTCLK (LOCO). By this function, the main clock oscillation frequency errors can be detected.

The target IWDTCLK to be measured (frequency-divided IWDTCLK clock) can be selected from the IWDTCLK/1, IWDTCLK/16, IWDTCLK/128, and IWDTCLK/256, and the count clock for measuring the frequency-divided IWDTCLK clock can be selected from PCLKA/1 clock, PCLKA/2 clock, PCLKA/4 clock, and PCLKA/8 clock.

The LCNT counter counts the frequency-divided IWDTCLK clock cycle with the count clock, and the recent 16 count results are stored in LCNT00 to LCNT15 (the latest count result in LCNT00). The average value of the recent 16 count results is automatically computed and stored in LCNTA.

The frequency-divided IWDTCLK clock rise interrupt requests can be generated when the rising edge of the frequency-divided IWDTCLK clock is detected. The frequency-divided IWDTCLK clock rise interrupt requests can be skipped, and the count results can also be skipped. When the count result (LCNT00 value) exceeds the upper limit or lower limit value, the IWDTCLK deviation exceedance interrupt request can be generated. The upper and lower limits can be set in LCNTDU and LCNTDL, respectively, and the upper limit value is obtained by (LCNTA value + LCNTDU value) and the lower limit value is obtained by (LCNTA value – LCNTDL value). When the frequency-divided IWDTCLK clock frequency is too low and the LCNT counter overflows, the LCNT overflow interrupt request can be generated. Since all of these interrupts are output as LOCOI interrupts, the interrupt source should be determined by reading the status flags after the interrupt generation.

When using the IWDTCLK count function, the independent watchdog timer (IWDT) should be activated.

Table 24.9 shows a frequency setting example for the IWDTCLK count function.

Figure 24.79 shows an example of IWDTCLK count function operation, and Figure 24.80 shows the setting flow example.

Table 24.9 Frequency Setting Example for IWDTCLK Count Function

Frequency-Divided IWDTCLK Clock		Count Clock		
LCCR.LPSC[1:0] Setting	**Frequency**	**LCCR.TPSC[1:0] Setting**	**Frequency (When PCLKA = 100 MHz)**	**Desired Count Result Value**
00 (not divided)	125 kHz	00 (not divided)	100 MHz	320h
01 (divided by 16)	7.81 kHz	00 (not divided)	100 MHz	3200h
10 (divided by 128)	976 Hz	10 (divided by 4)	25 MHz	6400h
11 (divided by 256)	488 Hz	11 (divided by 8)	12.5 MHz	6400h

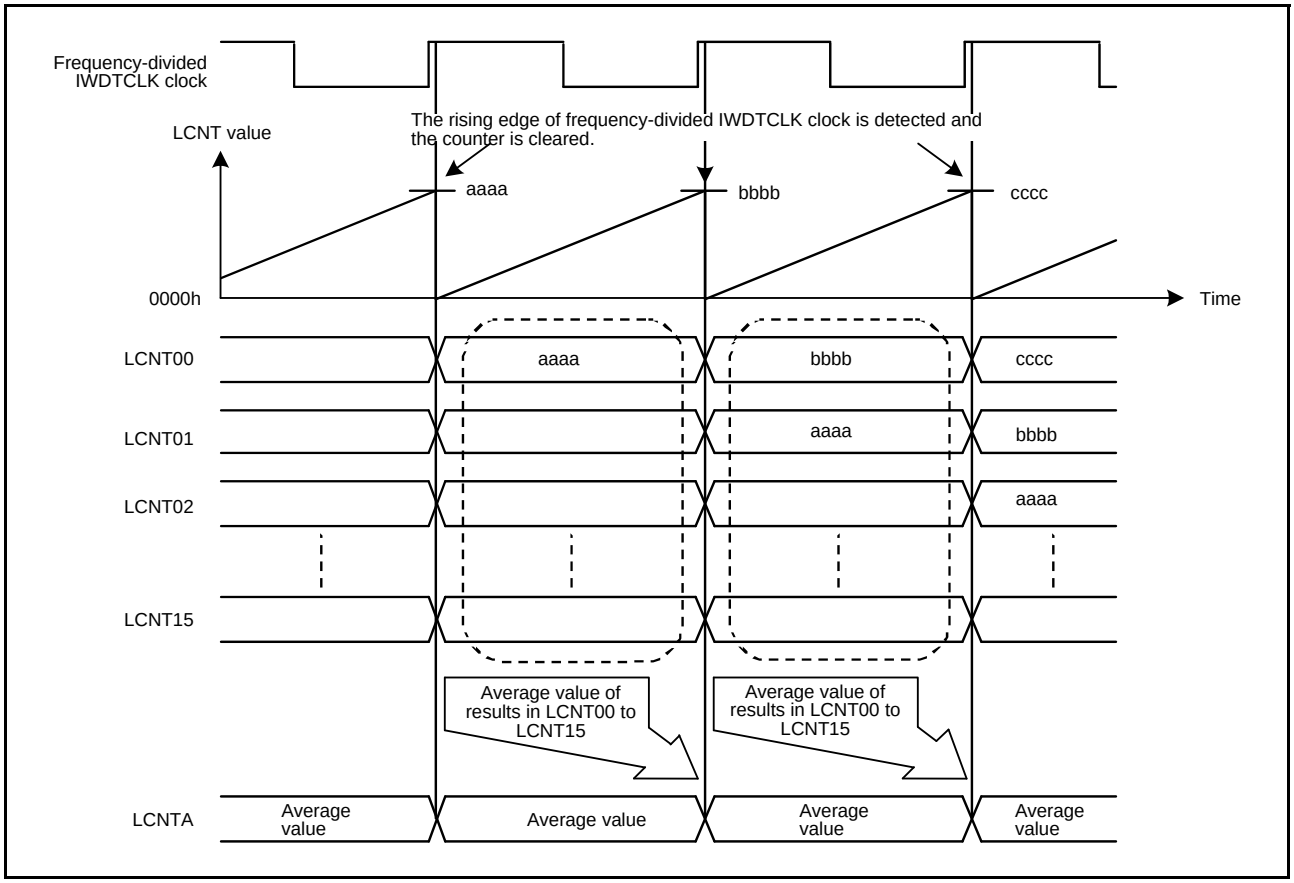


Figure 24.79 Example of IWDTCLK Count Function Operation

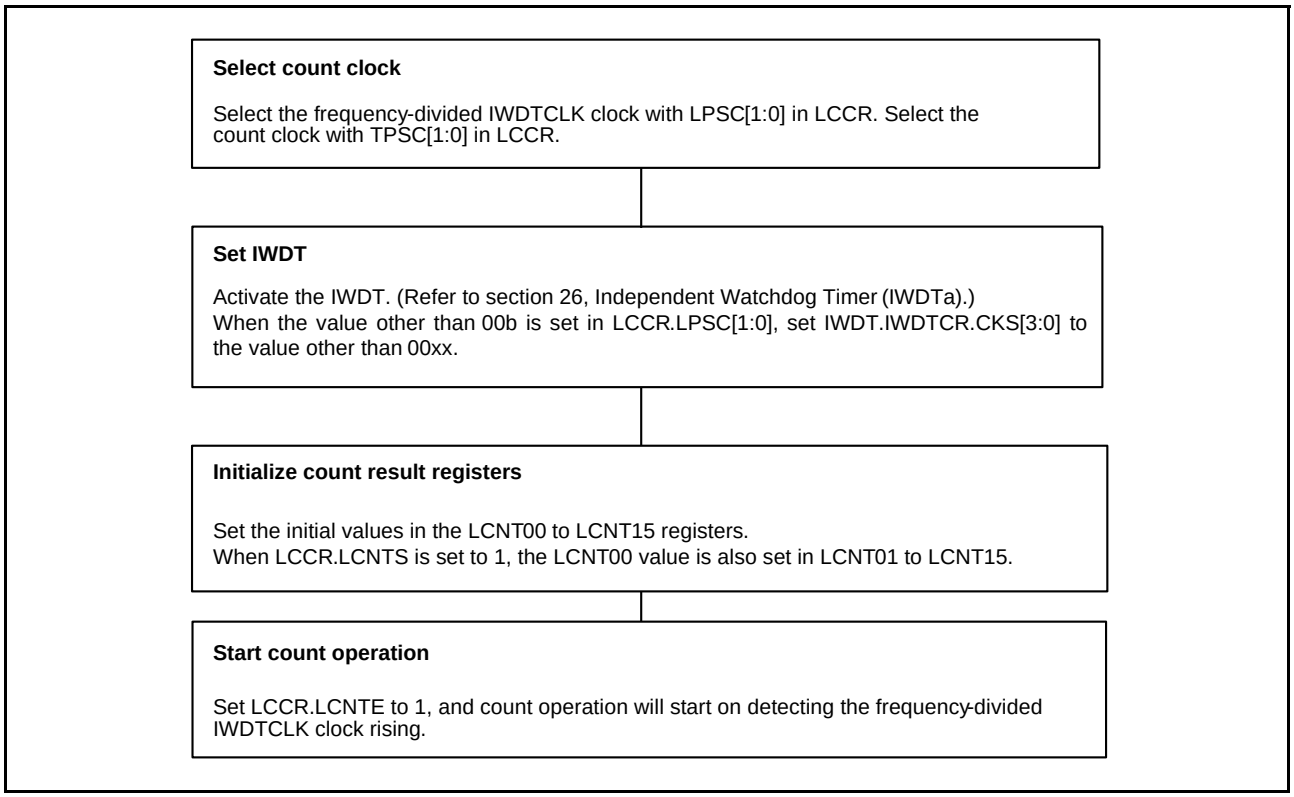


Figure 24.80 Example for Setting IWDTCLK Count Function Operation

The frequency-divided IWDTCLK clock rise interrupt requests can be skipped, and the count results can also be skipped. The skipping count can be selected from 7, 15, 127, and 255 times with LCCR.LCTO[2:0]. Whether to skip the count results is set with LCCR.LCNTAT.

Figure 24.81 shows an example in which the count result is not skipped, and Figure 24.82 shows an example in which the count result is also skipped.

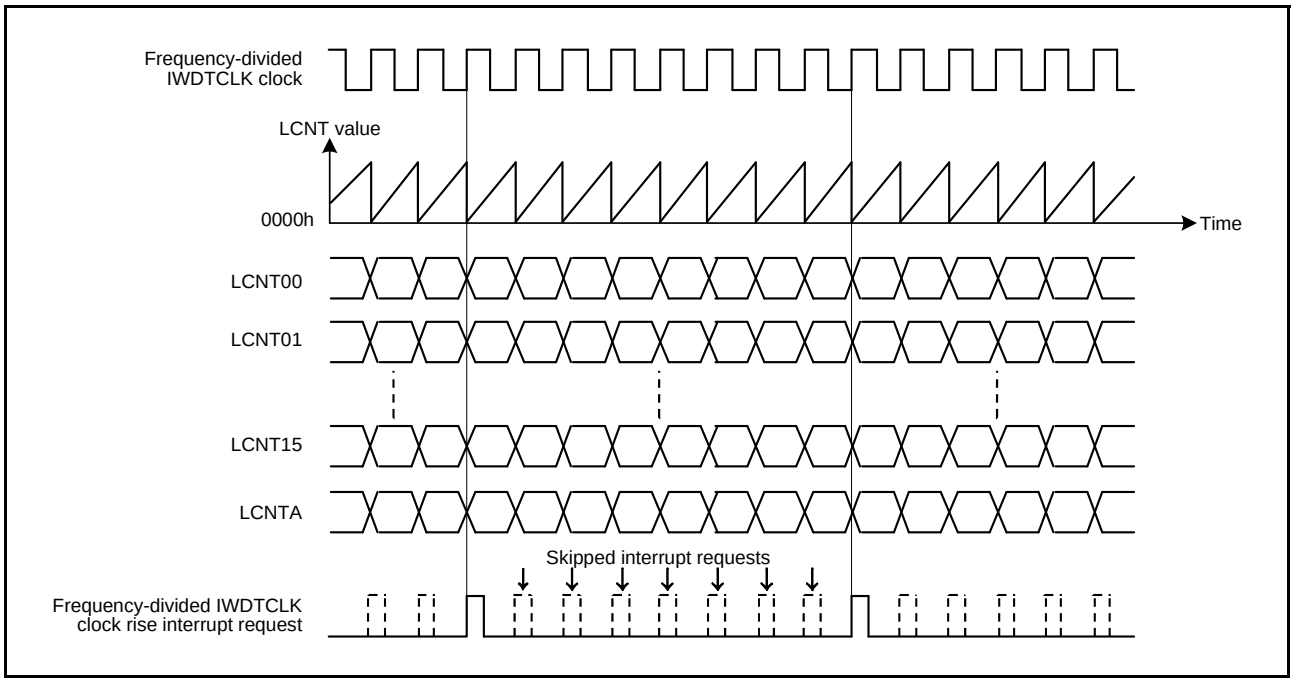


Figure 24.81 Example of IWDTCLK Count Skipping Function Operation (Skipping Count: 7, Count Result not Skipped)

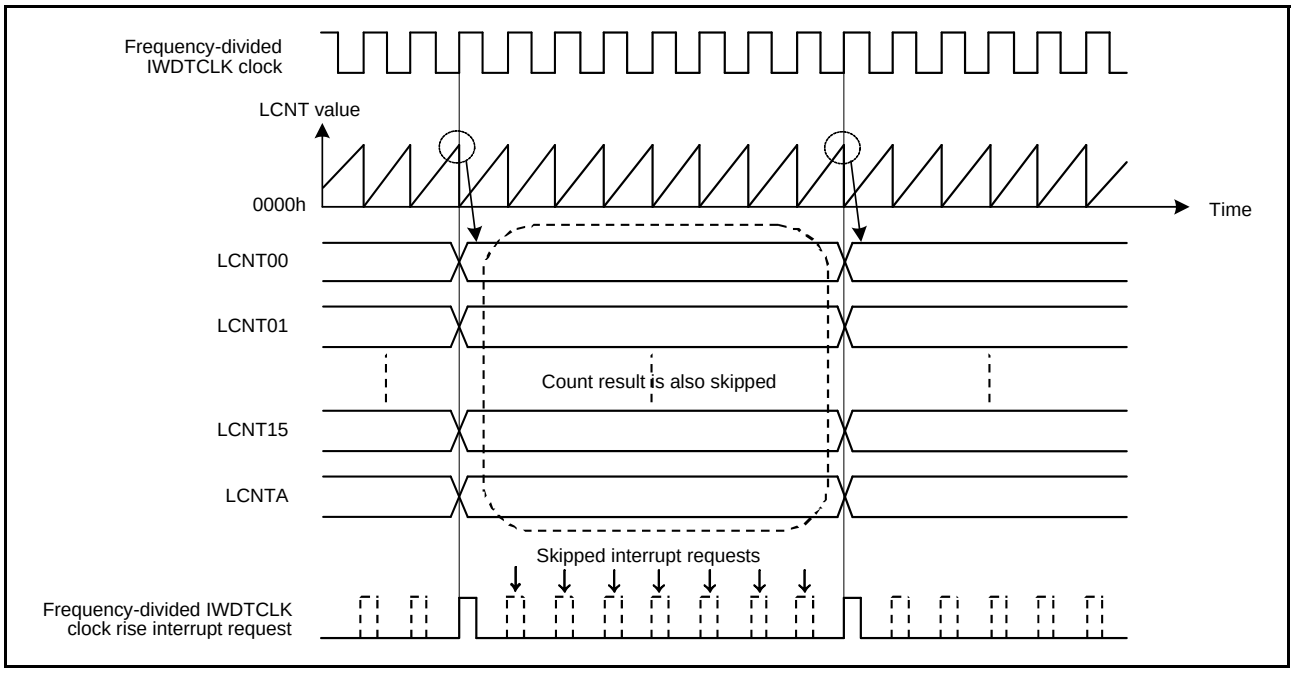


Figure 24.82 Example of IWDTCLK Count Skipping Function Operation (Skipping Count: 7, Count Result Skipped)

24.7 Protection Function

24.7.1 Write-Protection for Registers

In order to prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WPn (n = 0 to 7).
The write-protection can be set for the following registers:

Table 24.10 Write-Protected Registers

Symbol	Register Name
GTIOR	General PWM timer I/O control register
GTINTAD	General PWM timer interrupt output setting register
GTCR	General PWM timer control register
GTBER	General PWM timer buffer enable register
GTUDC	General PWM timer count direction register
GTITC	General PWM timer interrupt and A/D converter start request skipping setting register
GTST	General PWM timer status register
GTCNT	General PWM timer counter value
GTCCRA to GTCCRF	General PWM timer compare capture register A to F
GTPR	General PWM timer cycle setting register
GTPBR	General PWM timer cycle setting buffer register
GTPDBR	General PWM timer cycle setting double-buffer register
GTADTRA, GTADTRB	A/D converter start request timing register A and B
GTADTBRA, GTADTBRB	A/D converter start request timing buffer register A and B
GTADTDBRA, GTADTDBRB	A/D converter start request timing double-buffer register A and B
GTONCR	General PWM timer output negate control register
GTDTCR	General PWM timer dead time control register
GTDVU, GTDVD	General PWM timer dead time value register U and D
GTDBU, GTDBD	General PWM timer dead time buffer register U and D
GTSOTR	General PWM timer output protection function temporary release register

24.7.2 Disabling of Buffer Operation

If the timing of buffer register write is too late for the buffer transfer timing, buffer operation can be suspended with the GTBDR setting. Specifically, buffer transfer can be temporarily disabled, even though a buffer transfer condition is generated during buffer register write, by setting the corresponding GTBDR bit to 1 (buffer operation disabled) before buffer register write and clearing the bit to 0 (buffer operation enabled) after completion of writing to all the buffer registers.
Figure 24.83 shows an example of operation for disabling buffer operation

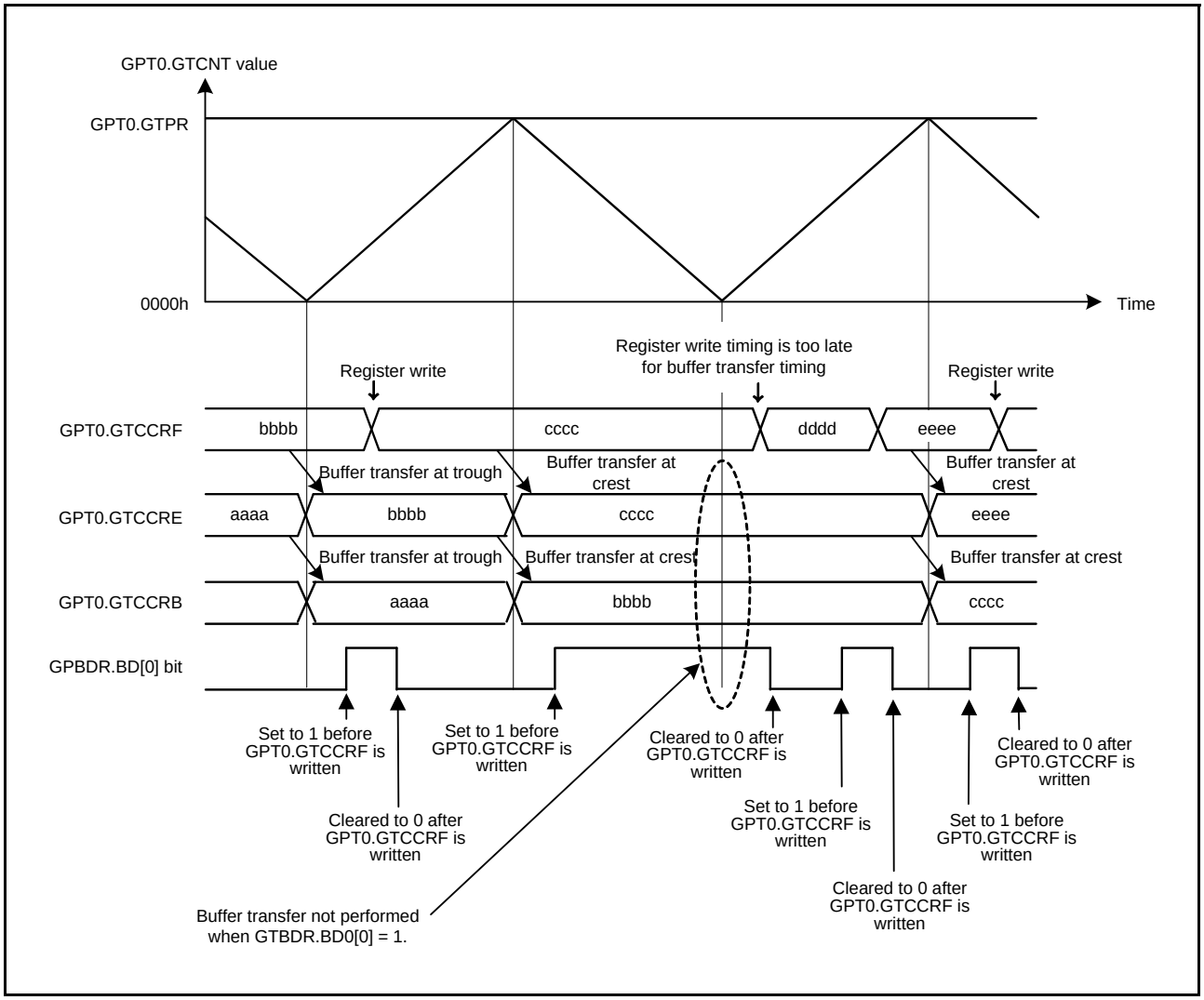


Figure 24.83 Example of Operation for Disabling Buffer Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests)

24.7.3 GTIOC Pin Output Negate Control

For protection from system failure, the negate control (deactivating the output level) is provided for GTIOC pin output with the GTONCR setting. There are three negate control sources: the comparator detection, GTETRG pin input, and writing to GTONCR.SWN.

Figure 24.84 shows an example of the GTIOC pin output negate control operation.

Note that once the negate control is performed, the negate control will not be released in the same cycle if the negate condition is no longer satisfied. The negate control is released in the next cycle.

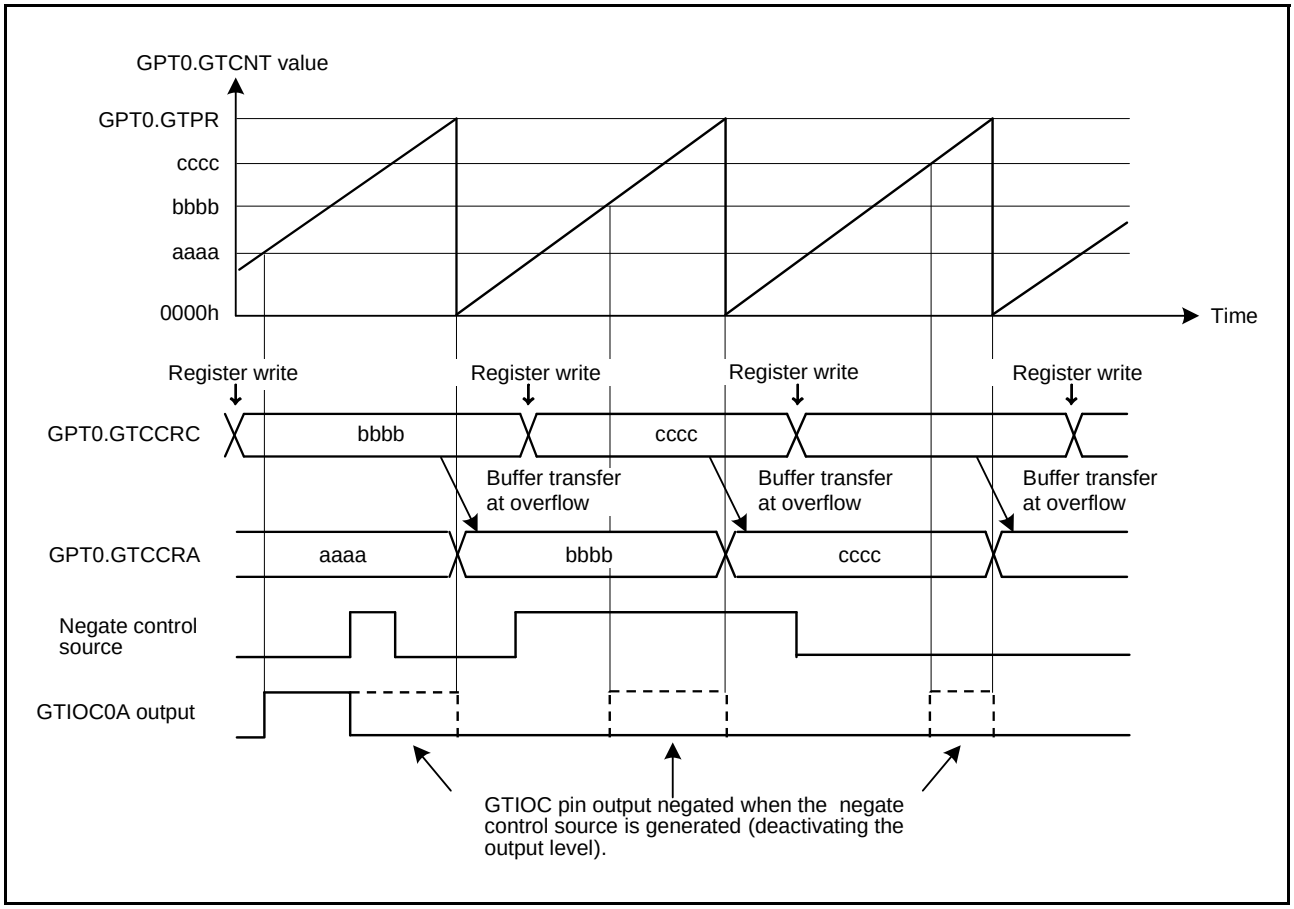


Figure 24.84 Example of GTIOC Pin Output Negate Control Operation (Saw-Wave Up-Counting, Buffer Operation, Active Level: 1, High Output at GTCCRA Compare Match, Low Output at Cycle End)

24.7.4 Output Protection Function for GTIOC Pin Output

In preparation for incorrect GTCCRA settings (settings outside the range of 0 < GTCCRA < GTPR), the output protection function for the GTIOC pin output (disabling function) is activated when the automatic dead time setting (GTDTCR.TDE = 1) is made in triangle-wave mode.
The status of the output protection function can be read from GTSOS.SOS[1:0].
Figure 24.85 shows the output protection function state transition.

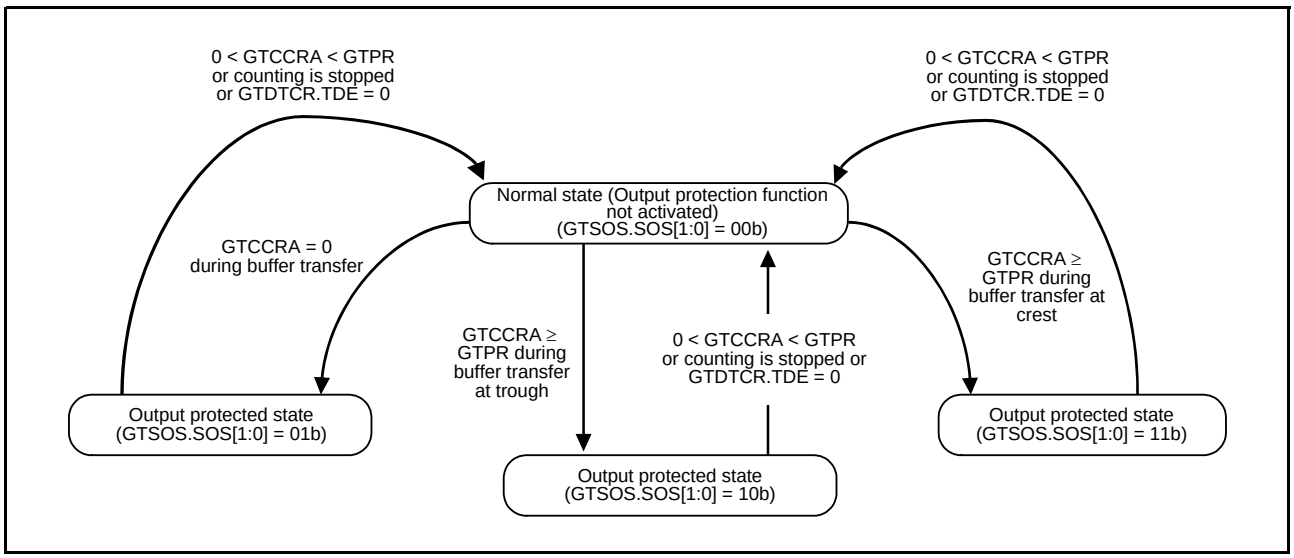
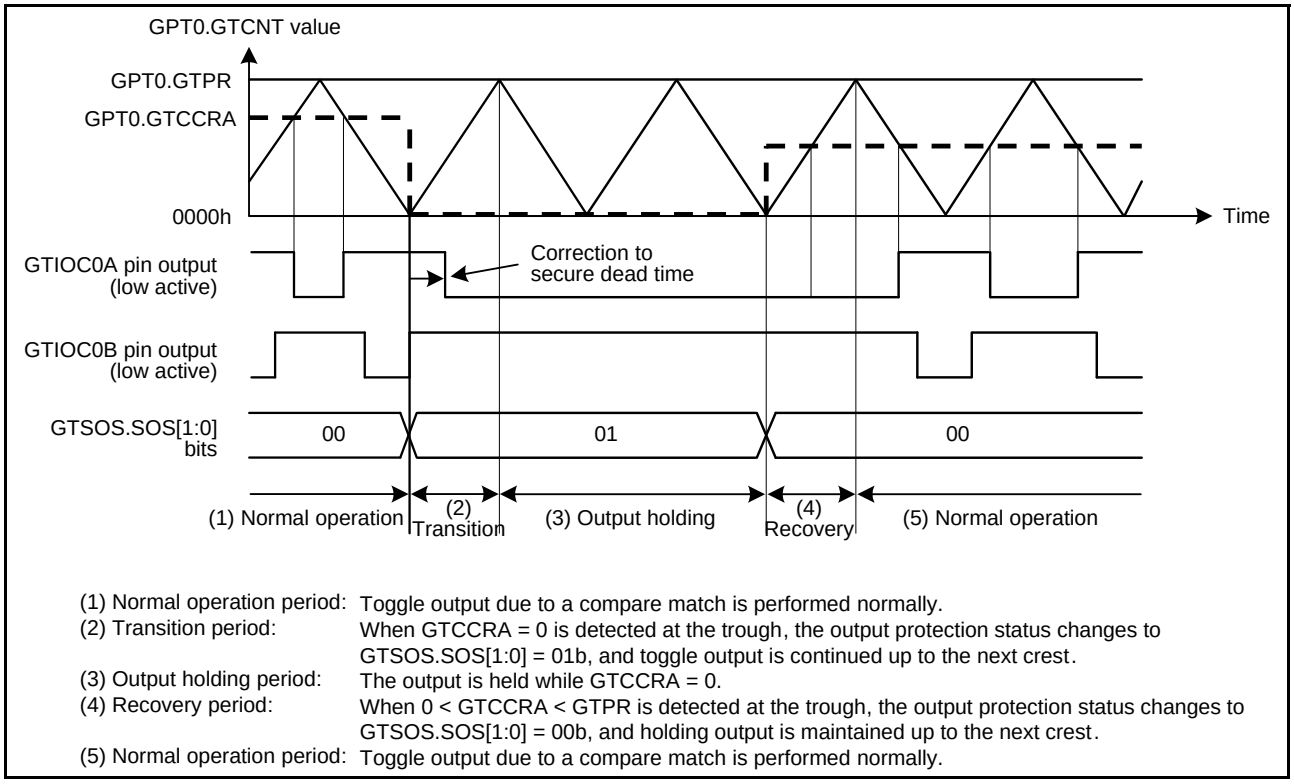


Figure 24.85 Output Protection Function

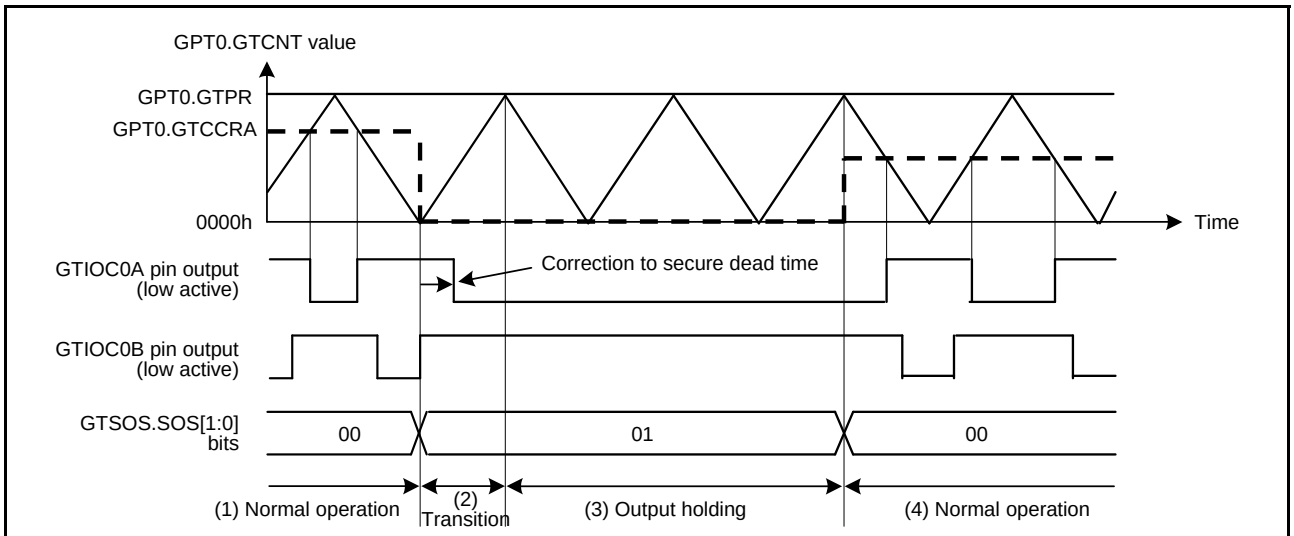
(1) Output Protection Function When GTCCRA is Set to 0 during Buffer Transfer

Figure 24.86 and Figure 24.87 show examples of output protection function operation when GTCCRA is set to 0 during buffer transfer at troughs, and Figure 24.88 and Figure 24.89 show examples when GTCCRA is set to 0 during buffer transfer at crests.



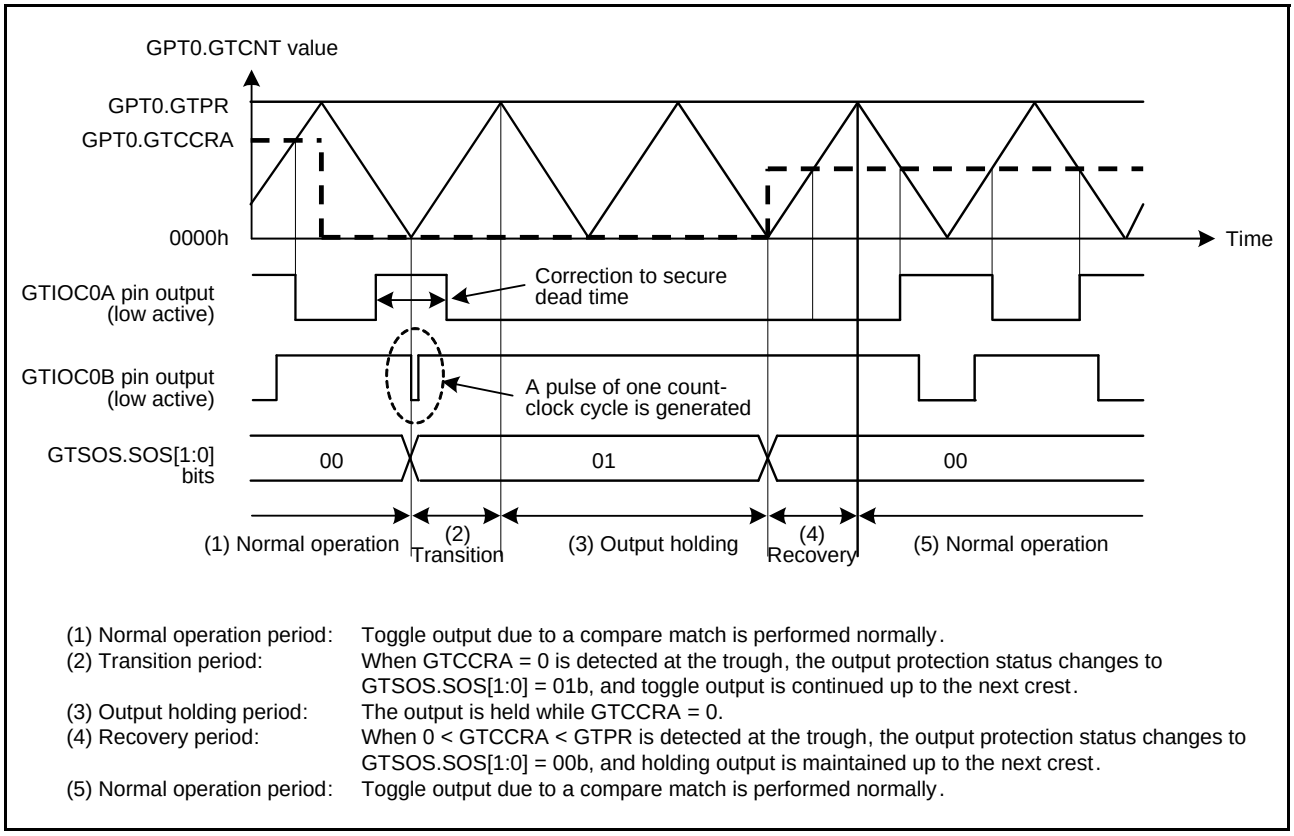
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Recovery period: When 0 < GTCCRA < GTPR is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 24.86 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)



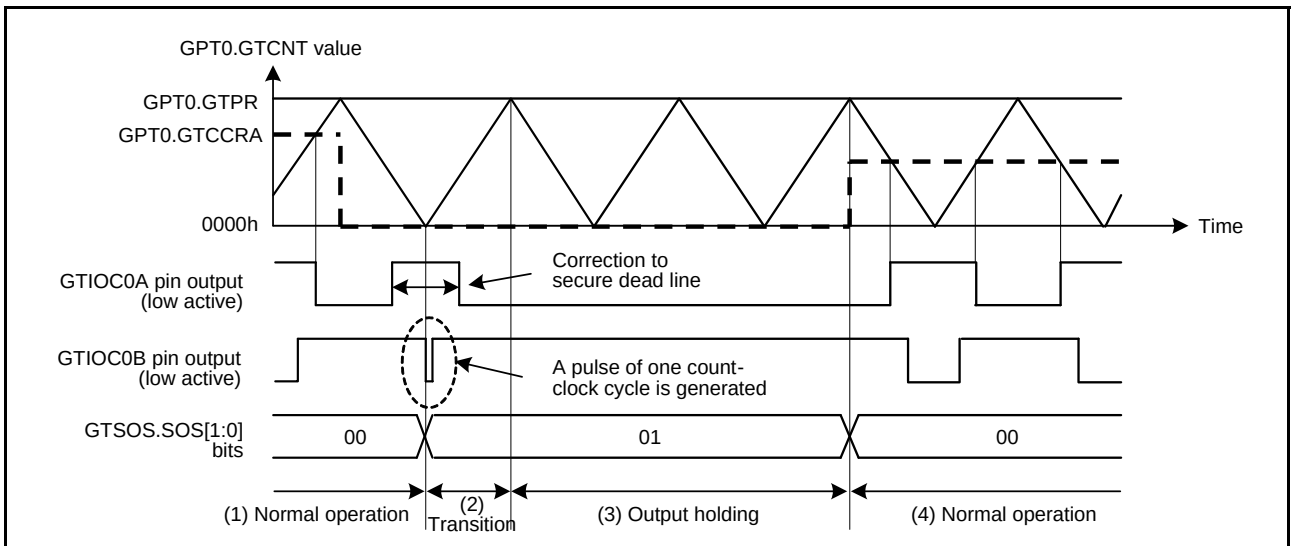
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Normal operation period: When 0 < GTCCRA < GTPR is detected at the crest, the output protection status changes to GTSOS.SOS[1:0] = 00b, and toggle output due to a compare match is performed normally.

Figure 24.87 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)



(1) Normal operation period:	Toggle output due to a compare match is performed normally.
(2) Transition period:	When GTCCRA = 0 is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 01b, and toggle output is continued up to the next crest.
(3) Output holding period:	The output is held while GTCCRA = 0.
(4) Recovery period:	When 0 < GTCCRA < GTPR is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period:	Toggle output due to a compare match is performed normally.

Figure 24.88 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

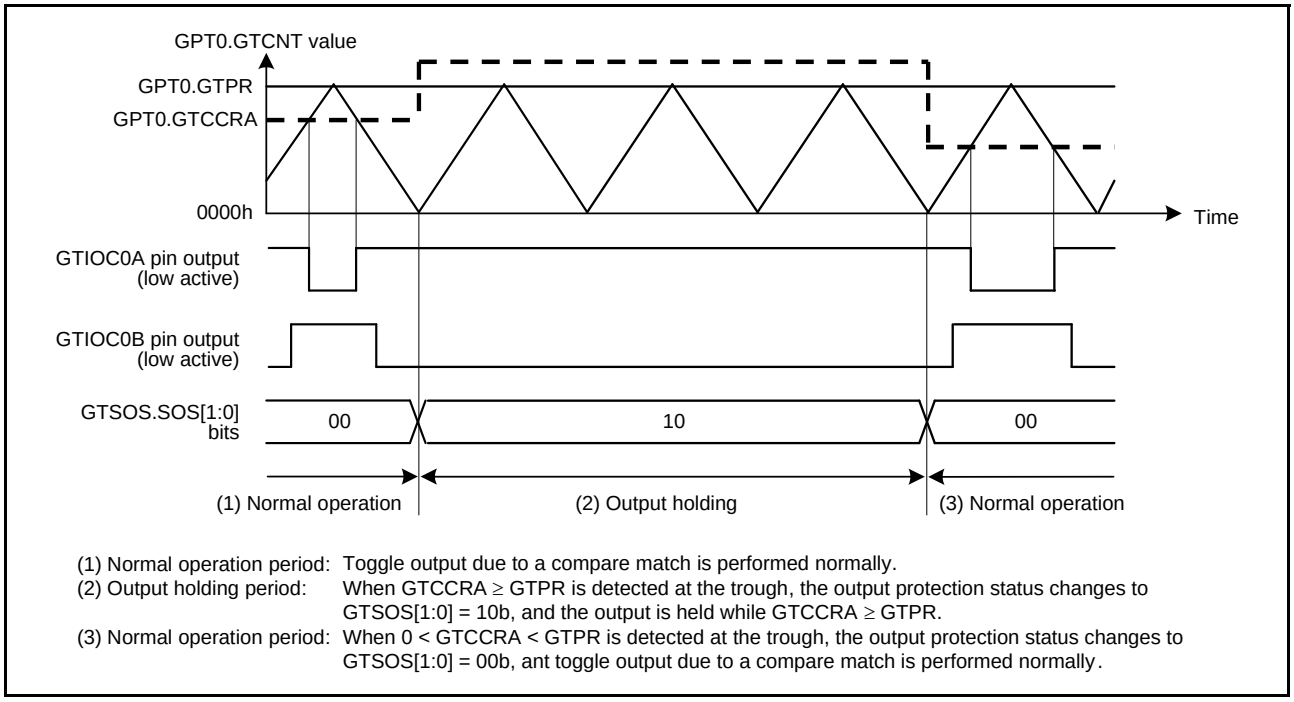


(1) Normal operation period:	Toggle output due to a compare match is performed normally.
(2) Transition period:	When GTCCRA = 0 is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 01b, and toggle output is continued up to the next crest.
(3) Output holding period:	The output is held while GTCCRA = 0.
(4) Recovery period:	When 0 < GTCCRA < GTPR is detected at the crest, the output protection status changes to GTSOS.SOS[1:0] = 00b, and toggle output due to a compare match is performed normally.

Figure 24.89 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)

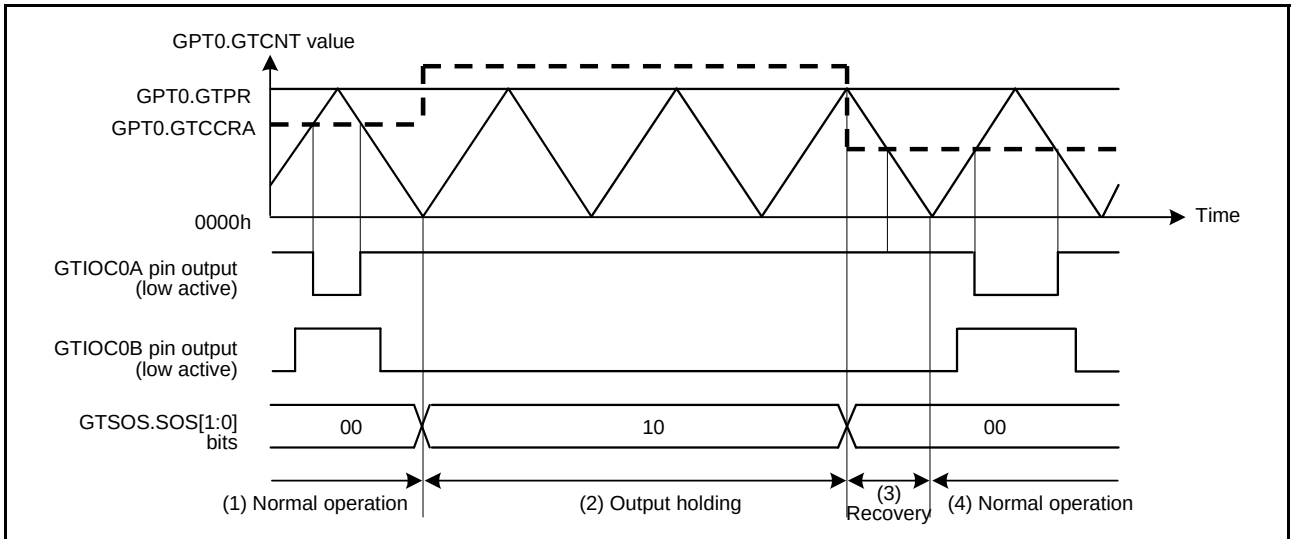
(2) Output Protection Function When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs

Figure 24.90 and Figure 24.91 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected at the trough, the output protection status changes to GTSOS[1:0] = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period: When 0 < GTCCRA < GTPR is detected at the trough, the output protection status changes to GTSOS[1:0] = 00b, ant toggle output due to a compare match is performed normally.

Figure 24.90 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

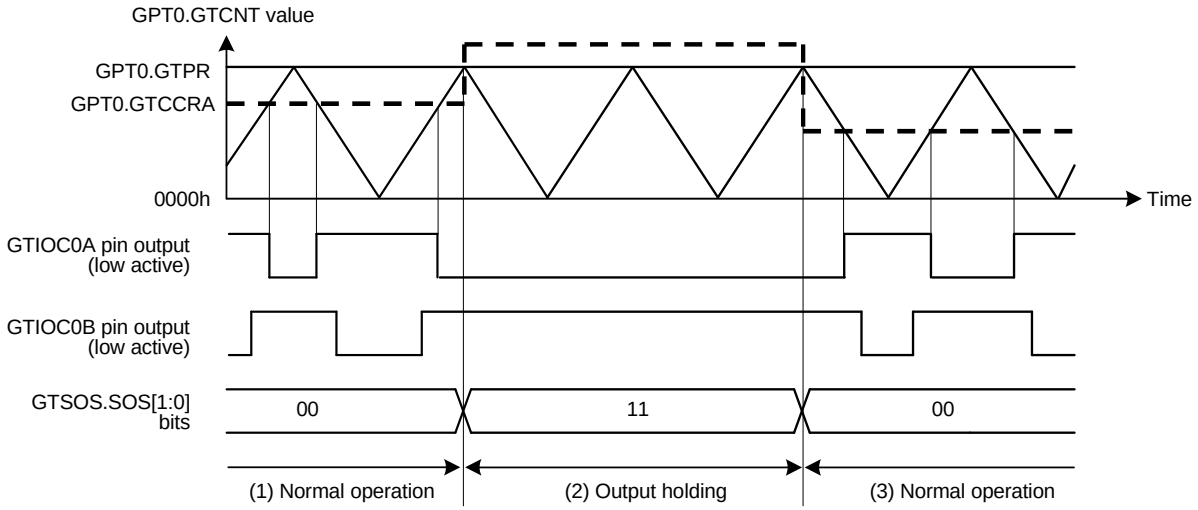


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected at the trough, the output protection status changes to GTSOS[1:0] = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period: When 0 < GTCCRA < GTPR is detected at the crest, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 24.91 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)

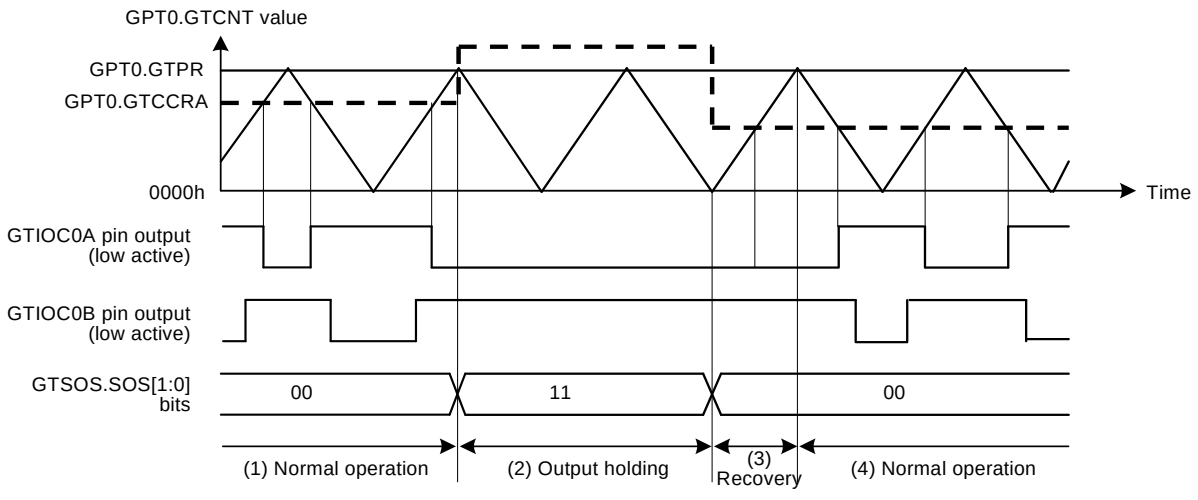
(3) Output Protection Function When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests

Figure 24.92 and Figure 24.93 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected at the crest, the output protection status changes to GTSOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period: When 0 < GTCCRA < GTPR is detected at the crest, the output protection status changes to GTSOS.SOS[1:0] = 00b, and toggle output due to a compare match is performed normally.

Figure 24.92 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR Is detected at the crest, the output protection status changes to GTSOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period: When 0 < GTCCRA < GTPR is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 24.93 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

(4) Restricted Specification of Output Protection Function

The GTCCRA value must be set within the range of (0 < GTCCRA < GTPR) at count start.
If an incorrect value is set in GTCCRA during count operation, (a setting outside the range of 0 < GTCCRA < GTPR), the output protection function deactivates the level of one of the positive and negative outputs. However, the function does not operate correctly if counting starts with an incorrect value set in GTCCRA.

24.7.5 High-Impedance Control of GTIOC Pin Output by POE Function

For protection from system failure, the high-impedance state of the GTIOCnm pin output can be controlled by the port output enable (POE) function. (n = 0 to 7; m = A, B)
For details, see section 23, Port Output Enable 3 (POE3).

24.8 Initialization Method of Output Pins

24.8.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port mode (PMR and PmnPFS), setting GTIOR and the OAE and OBE bits in GTONCR and outputting the GPT function to external pins.

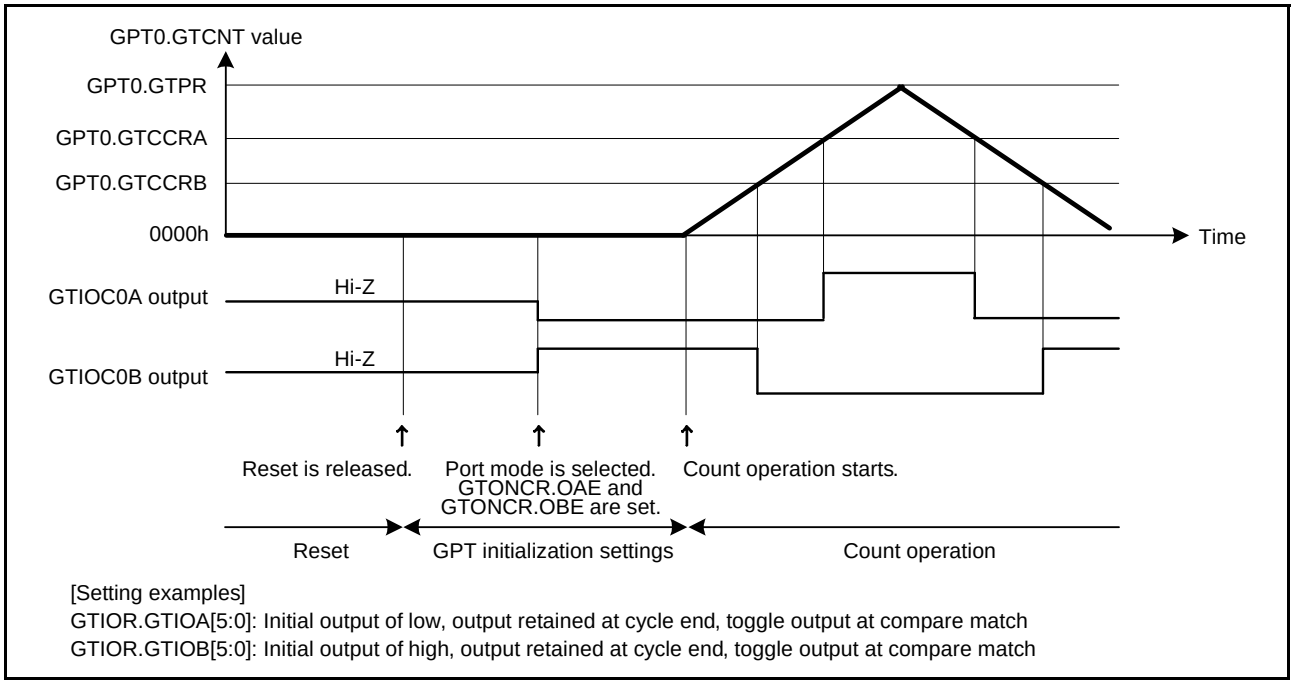


Figure 24.94 Example of Pin Settings after Reset

24.8.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization.

(1) Set OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop.
(2) Set OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop.
(3) Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR, and PMR registers of the I/O port in advance. Set the OAE and OBE bits in GTONCR to 0 and the control bit in PMR that corresponds to the pin to 0 to allow the arbitrary values to be output from the pin set as a general output port when an error occurs.
(4) Drive the output to a high impedance state using the POE function of the port output enable 3 (POE3).

When automatic dead time setting has been made, clear the GTDTCR.TDE bit to 0 once after counting is stopped.

When counting is stopped, only the values of registers that are changed by a GPT external source will change. If counting is resumed, operation will carry on from where it was stopped.
If counting was stopped, registers should be initialized before counting is started.

24.9 Usage Notes

24.9.1 Module Stop Function Setting

Operation of the GPT can be disabled or enabled by the module stop control register. The GPT is stopped at the initial value. Register access is enabled by clearing module stop state. For details, see section 12, Low Power Consumption.

24.9.2 Settings of GTCCRn during Compare Match Operation (n = A to F)

(1) When automatic dead time setting has been made in triangle-wave PWM mode

GTCCRA should be set within the range of GTDVU < GTCCRA, GTDVD < GTCCRA, and GTCCRA < GTPR.
When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made during count operation, the output protection function is activated.
Be sure to set 0 < GTCCRA < GTPR at count start. Otherwise, the output protection function is not be activated correctly. For details, refer to section 24.7.4, Output Protection Function for GTIOC Pin Output.

(2) When automatic dead time setting has not been made in triangle-wave PWM mode

GTCCRA should be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA ≥ GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. In the case of GTCCRA > GTPR, no compare match occurs.
Similarly, GTCCRB should be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRA ≥ GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. In the case of GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting has been made in saw-wave one-shot pulse mode

GTCCRC and GTCCRD should be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

- In up-count operation: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-count operation: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVD

(4) When automatic dead time setting has not been made in saw-wave one-shot pulse mode

GTCCRC and GTCCRD should be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-count operation: 0 < GTCCRC < GTCCRD < GTPR
- In down-count operation: GTPR > GTCCRC > GTCCRD > 0

Similarly, GTCCRE and GTCCRF should be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-count operation: 0 < GTCCRE < GTCCRF < GTPR
- In down-count operation: GTPR > GTCCRE > GTCCRF > 0

(5) In saw-wave PWM mode

GTCCRA should be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.
Similarly, GTCCRB should be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

24.9.3 Stopping the Timer in the Safe Way

When the timer stopping by the GTSTR writing and the GPT compare match interrupt conflict, an interrupt may be generated after the GTSTR writing.
Therefore, stop the timer in the following order. Then, a compare match interrupt is not generated after the timer has been stopped, and the timer can be stopped in the safe way.

(1) Disable the interrupt request by the interrupt request enable registers (IER15 to IER18) of the ICU.
(2) Disable the interrupt request by the interrupt output setting register (GTINTAD) of the GPT.
(3) Clear the CSTn bit in GTSTR to 0.

24.9.4 Low-Power Consumption Setting when the IWDTCLK Count Function is in Use

In the case when the GPT operation is stopped during the IWDTCLK count operation by the module stop control register or standby control register and then restarted, first clear the LCCR.LCNTE bit to 0 to stop the IWDTCLK count before the GPT operation is stopped. Then, set the LCCR.LCNTE bit to 1 to restart the IWDTCLK count after the GPT operation is restarted.
For details on the module stop control register and the standby control register, see section 12, Low Power Consumption.

24.9.5 Target Channels for Synchronous Operation

Synchronous operation described in section 24.3.7, Synchronized Operation is targeted for channels 0 to 3 or channels 4 to 7. Note that synchronous operation for channels 0 to 7 is not supported.

24.9.6 Notes on Delay Time Settings for PWM Delay Generation Circuit

When the PWM delay generation circuit generated delays for a PWM output waveform and the waveform is being toggled in response to compare-matches, do not change the settings for delay time while compare-match value is within the ranges listed in the following table. This restriction applied to the GTDLYFA, GTDLYRA, GTDLYFB, and GTDLYRB registers.

Mode	Direction of Counting	Compare-Match Value
Sawtooth waveform	Up	GTPR - 2 or above
	Down	2 or below
Triangle waveform	Down	2 or below

An example of how the restrictions apply to the timing of setting GTDLYFA in sawtooth waveform one-shot pulse mode (counting up) is shown as Figure 24.95. Do not change the value set in GTDLYFA while GTCCRD ≥ GTPR - 2.

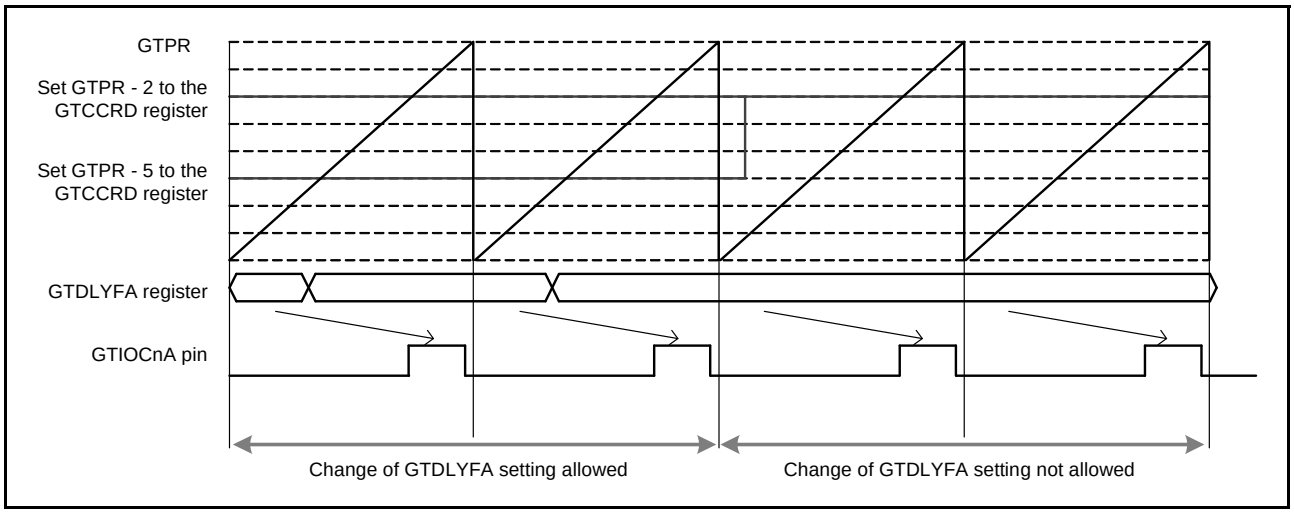


Figure 24.95 Restriction on the Timing of GTDLYFA Register Settings

Changing the values in the GTDLYFA, GTDLYRA, GTDLYFB, and GTDLYRB registers during periods where changes to settings are not allowed may lead to faulty output waveforms, i.e., shifts in the timing of output waveform transitions from the expected values.

25. Compare Match Timer (CMT)

This MCU has two on-chip compare match timer (CMT) units (unit 0 and unit 1) each consisting of a two-channel 16-bit timer (i.e., a total of four channels). The CMT has a 16-bit counter, and can generate interrupts at set intervals.

25.1 Overview

Table 25.1 lists the specifications for the CMT.
Figure 25.1 shows a block diagram of the CMT (unit 0). A two-channel CMT constitutes a unit. Unit 0 and unit 1 are the same in terms of specifications.

Table 25.1 Specifications of CMT

Item	Description
Count clock	• Four frequency dividing clocks One clock from PCLK/8 clock, PCLK/32 clock, PCLK/128 clock, and PCLK/512 clock can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.
Low power consumption facilities	Each unit can be placed in a module-stop state.

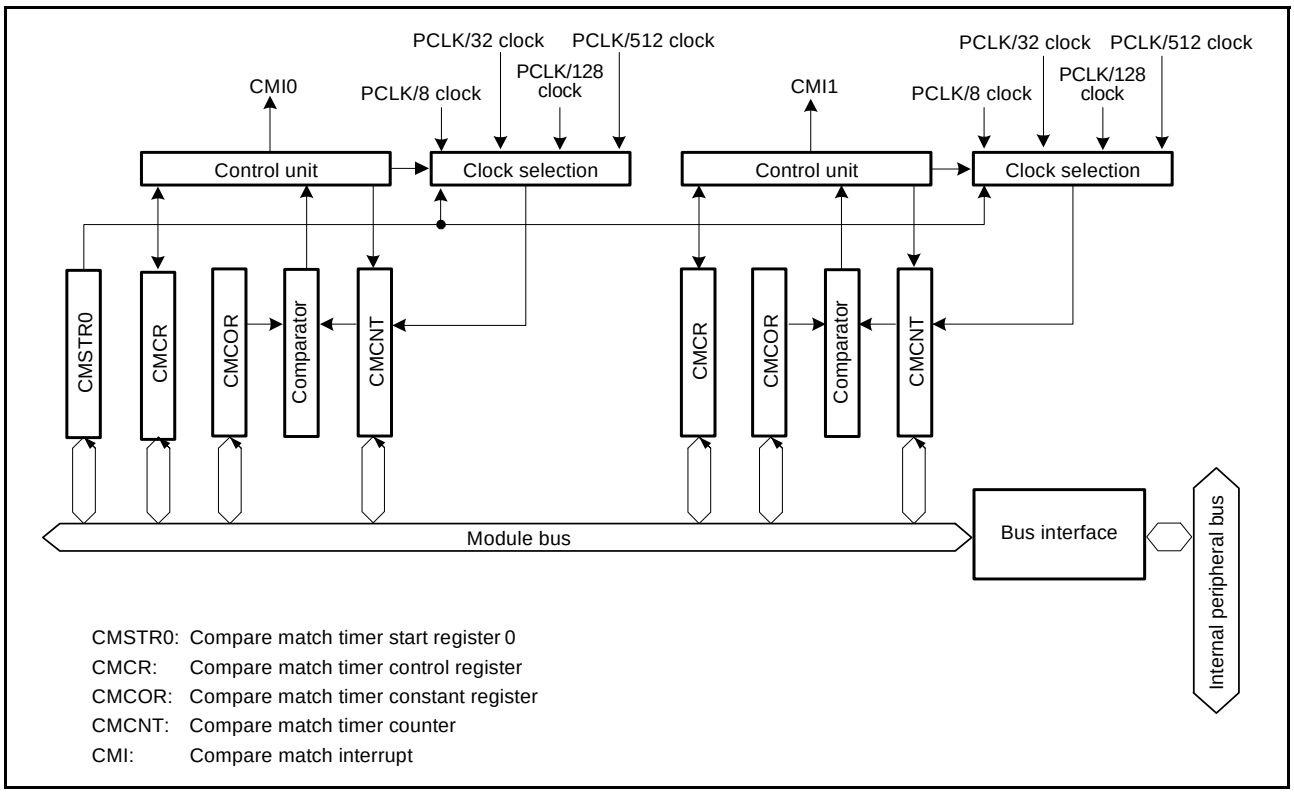


Figure 25.1 Block Diagram of CMT (Unit 0)

25.2 Register Descriptions

25.2.1 Compare Match Timer Start Register 0 (CMSTR0)

Address(es): 0008 8000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR1	STR0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR0	Count Start 0	0: CMT0.CMCNT count is stopped 1: CMT0.CMCNT count is started	R/W
b1	STR1	Count Start 1	0: CMT1.CMCNT count is stopped 1: CMT1.CMCNT count is started	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

25.2.2 Compare Match Timer Start Register 1 (CMSTR1)

Address(es): 0008 8010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR3	STR2
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR2	Count Start 2	0: CMT2.CMCNT count is stopped 1: CMT2.CMCNT count is started	R/W
b1	STR3	Count Start 3	0: CMT3.CMCNT count is stopped 1: CMT3.CMCNT count is started	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

25.2.3 Compare Match Timer Control Register (CMCR)

Address(es): CMT0.CMCR 0008 8002h, CMT1.CMCR 0008 8008h,
CMT2.CMCR 0008 8012h, CMT3.CMCR 0008 8018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CMIE	—	—	—	—	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK/8 clock 0 1: PCLK/32 clock 1 0: PCLK/128 clock 1 1: PCLK/512 clock	R/W
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CMIE	Compare Match Interrupt Enable	0: Compare match interrupt (CMIn) disabled 1: Compare match interrupt (CMIn) enabled	R/W
b7	—	Reserved	This bit is read as undefined. The write value should be 1.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CKS[1:0] Bits (Clock Select)

These bits select the count clock to be input to CMCNT from four frequency dividing clocks obtained by dividing the peripheral clock (PCLK).

When the STRn (n = 0 to 3) bit in CMSTRm (m = 0 or 1) is set to 1, CMCNT starts counting up on the clock selected with bits CKS[1:0].

CMIE Bit (Compare Match Interrupt Enable)

The CMIE bit enables or disables compare match interrupt (CMIn) (n = 0 to 3) generation when CMCNT and CMCOR values match.

25.2.4 Compare Match Timer Counter (CMCNT)

Address(es): CMT0.CMCNT 0008 8004h, CMT1.CMCNT 0008 800Ah,
CMT2.CMCNT 0008 8014h, CMT3.CMCNT 0008 801Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CMCNT is a readable/writable up-counter to generate interrupt requests.
When an frequency dividing clock is selected by bits CKS[1:0] in CMCR and the STRn (n = 0 to 3) bit in CMSTRm (m = 0 or 1) is set to 1, CMCNT starts counting up using the selected clock.
When the value in CMCNT and the value in CMCOR match, CMCNT is cleared to 0000h. At the same time, a compare match interrupt (CMIn) (n = 0 to 3) is generated.

25.2.5 Compare Match Timer Constant Register (CMCOR)

Address(es): CMT0.CMCOR 0008 8006h, CMT1.CMCOR 0008 800Ch,
CMT2.CMCOR 0008 8016h, CMT3.CMCOR 0008 801Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

CMCOR is a readable/writable register to set a compare match cycle with CMCNT.

25.3 Operation

25.3.1 Periodic Count Operation

When an frequency dividing clock is selected by bits CKS[1:0] in CMCR and the STRn (n = 0 to 3) bit in CMSTRm (m = 0 or 1) is set to 1, CMCNT starts counting up using the selected clock.
When the value in CMCNT and the value in CMCOR match, CMCNT is cleared to 0000h. At the same time, a compare match interrupt (CMIn) (n = 0 to 3) is generated. CMCNT then starts counting up again from 0000h. Figure 25.2 shows the operation of the CMCNT counter.

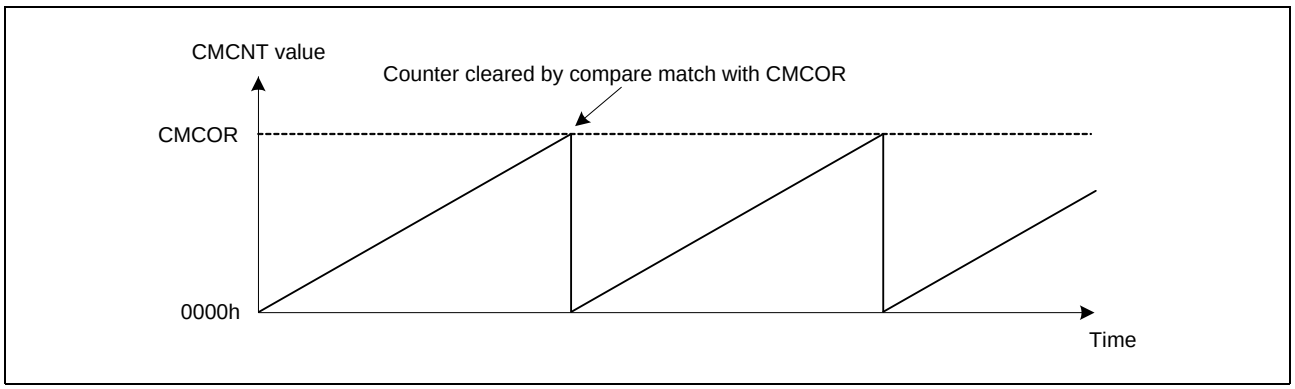


Figure 25.2 CMCNT Counter Operation

25.3.2 CMCNT Count Timing

As the count clock to be input to CMCNT, one of four frequency dividing clocks (PCLK/8, PCLK/32, PCLK/128, and PCLK/512) obtained by dividing the peripheral clock (PCLK) can be selected with the CKS[1:0] bits in CMCR. Figure 25.3 shows the timing of CMCNT.

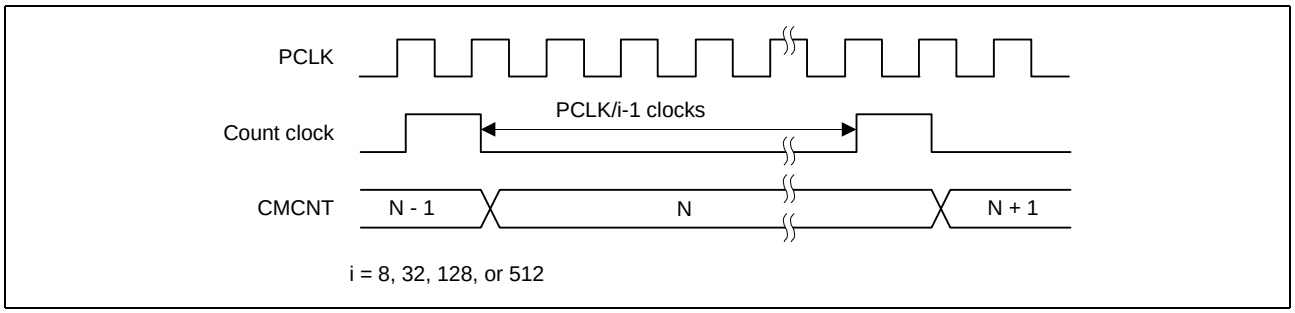


Figure 25.3 CMCNT Count Timing

25.4 Interrupts

25.4.1 Interrupt Sources

The CMT has channels and each of them to which a different vector address is allocated has a compare match interrupt (CMIn) (n = 0 to 3). When a compare match interrupt occurs, the corresponding interrupt request is output.
When the interrupt is used to activate a CPU interrupt, the priority of channels can be changed by the interrupt controller settings. For details, see section 15, Interrupt controller (ICUb).

Table 25.2 CMT Interrupt Sources

Name	Interrupt Sources	DTC Activation	DMAC Activation
CMI0	Compare match between CMT0.CMCNT and CMT0.CMCOR	Possible	Possible
CMI1	Compare match between CMT1.CMCNT and CMT1.CMCOR	Possible	Possible
CMI2	Compare match between CMT2.CMCNT and CMT2.CMCOR	Possible	Possible
CMI3	Compare match between CMT3.CMCNT and CMT3.CMCOR	Possible	Possible

25.4.2 Timing of Compare Match Interrupt Generation

When CMCNT and CMCOR match, a compare match interrupt (CMIn) (n = 0 to 3) is generated.
A compare match signal is generated at the last state in which the values match (the timing when the CMCNT counter updates the matched count value). That is, after a match between CMCOR and CMCNT, the compare match signal is not generated until the next CMCNT input clock.
Figure 25.4 shows the timing for the setting of a compare match interrupt.

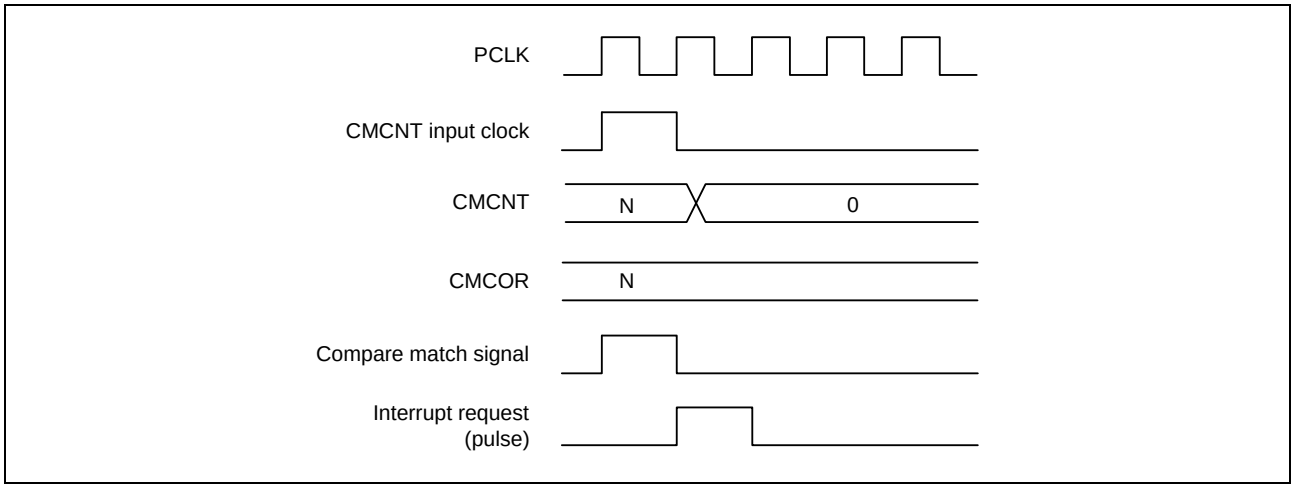


Figure 25.4 Timing for the Setting of a Compare Match Interrupt

25.5 Usage Notes

25.5.1 Setting the Module-Stop Function

The CMT can be enabled or disabled using the module-stop control register. The CMT is stopped at the initial value. The registers can be accessed by canceling the module-stop state. For details, see section 12, Low Power Consumption.

25.5.2 Conflict between Write and Compare-Match Processes of CMCNT

When the compare match signal is generated while writing to CMCNT, clearing CMCNT has priority over writing to it. In this case, CMCNT is not written to. Figure 25.5 shows the timing to clear the CMCNT counter.

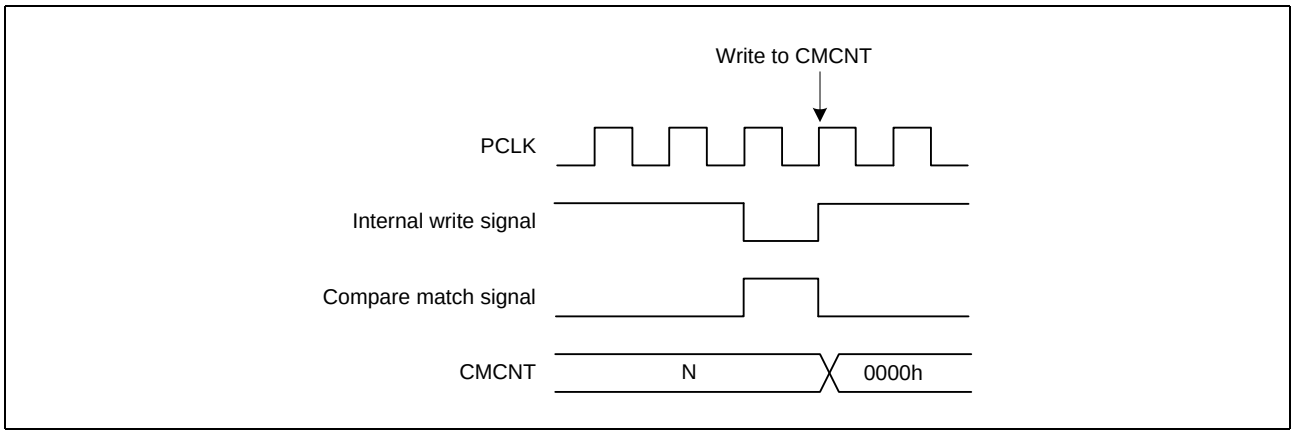


Figure 25.5 Conflict between Write and Compare Match Processes of CMCNT

25.5.3 Conflict between Write and Count-Up Processes of CMCNT

Even when the count-up occurs while writing to CMCNT, the writing has priority over the count-up. In this case, the count-up is not performed. Figure 25.6 shows the timing to write the CMCNT counter.

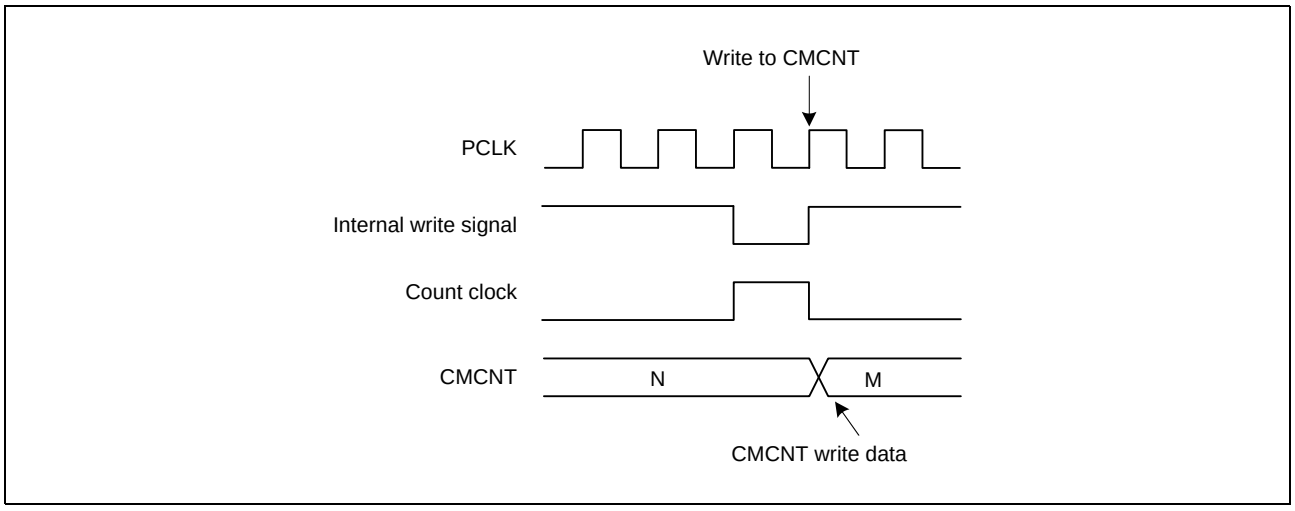


Figure 25.6 Conflict between Write and Count-Up Processes of CMCNT

26. Watchdog Timer (WDTA)

The WDT has a 14-bit down-counter, and can be set up so that the chip is reset by a reset output when counting down from the initial value causes an underflow of the counter. Alternatively, generation of an interrupt request is selectable when the counter underflows. The initial value for counting can be restored to the down-counter by refreshing its value. The interval over which refreshing is possible can also be selected. Refreshing the counter during this interval will restore its initial value for counting, while attempting to refresh the counter beyond this interval leads to the output of a reset or interrupt request. The refresh interval can be adjusted and used to detect the program entering runaway conditions. The WDT stops counting after an underflow or an attempt at refreshing the counter beyond the allowed interval. Counting is restarted by refreshing the counter when the WDT is in register start mode. When the WDT is in auto-start mode, counting is restarted automatically after output of the reset or interrupt request.

26.1 Overview

The WDT has two start modes: auto-start mode, in which counting automatically starts after release from the reset state, and register start mode, in which counting is started by refreshing the WDT (writing to the register).
In auto-start mode, necessary settings (clock division ratio, refresh window start and end positions, time-out period, and reset or non-maskable interrupt request output at an underflow) should be made in the option function select register 0 (OFS0) before release from the reset state. In register start mode, necessary settings (clock division ratio, refresh window start and end positions, time-out period, and reset or non-maskable interrupt request output at an underflow) should be made in the respective registers before the counter is started by refreshing after release from the reset state.
Set the WDT start mode select bit (OFS0.WDTSTRT bit) to select auto-start mode or register start mode.
When auto-start mode is selected (OFS0.WDTSTRT = 0), the WDT control register (WDTCR), and WDT reset control register (WDTRCR) settings are disabled and the settings of the OFS0 register are enabled.
When register start mode is selected (OFS0.WDTSTRT = 1), the settings of the OFS0 register are disabled and the WDTCR and WDTRCR settings are enabled.
Specifications of the WDT are listed in Table 26.1. Figure 26.1 is a block diagram of the WDT.

Table 26.1 Specifications of WDT (1/2)

Item	Specifications
Count source	Peripheral clock (PCLK)
Clock division ratio	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started by refreshing the WDTRR register (writing 00h and then FFh) (register start mode)
Conditions for stopping the counter	• Pin reset (the down-counter and registers return to their initial values) • A counter underflows or a refresh error is generated Count restarts automatically in auto-start mode, or by refreshing the counter in register start mode.
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset-output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Interrupt request output sources	• A non-maskable interrupt (WUNI) is generated by an underflow of the down-counter • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the WDTSR register.
Output signal (internal signal)	• Reset output • Interrupt request output
Auto-start mode (controlled by the option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.WDTCKS[3:0] bits) • Selecting the time-out period of the watchdog timer (OFS0.WDTTOPS[1:0] bits) • Selecting the window start position in the watchdog timer (OFS0.WDTRPSS[1:0] bits) • Selecting the window end position in the watchdog timer (OFS0.WDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.WDTRSTIRQS bit)

Table 26.1 Specifications of WDT (2/2)

Item	Specifications
Register start mode (controlled by the WDT registers)	• Selecting the clock frequency division ratio after refreshing (WDTCR.CKS[3:0] bits) • Selecting the time-out period of the watchdog timer (WDTCR.TOPS[1:0] bits) • Selecting the window start position in the watchdog timer (WDTCR.RPSS[1:0] bits) • Selecting the window end position in the watchdog timer (WDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (WDTRCR.RSTIRQS bit)

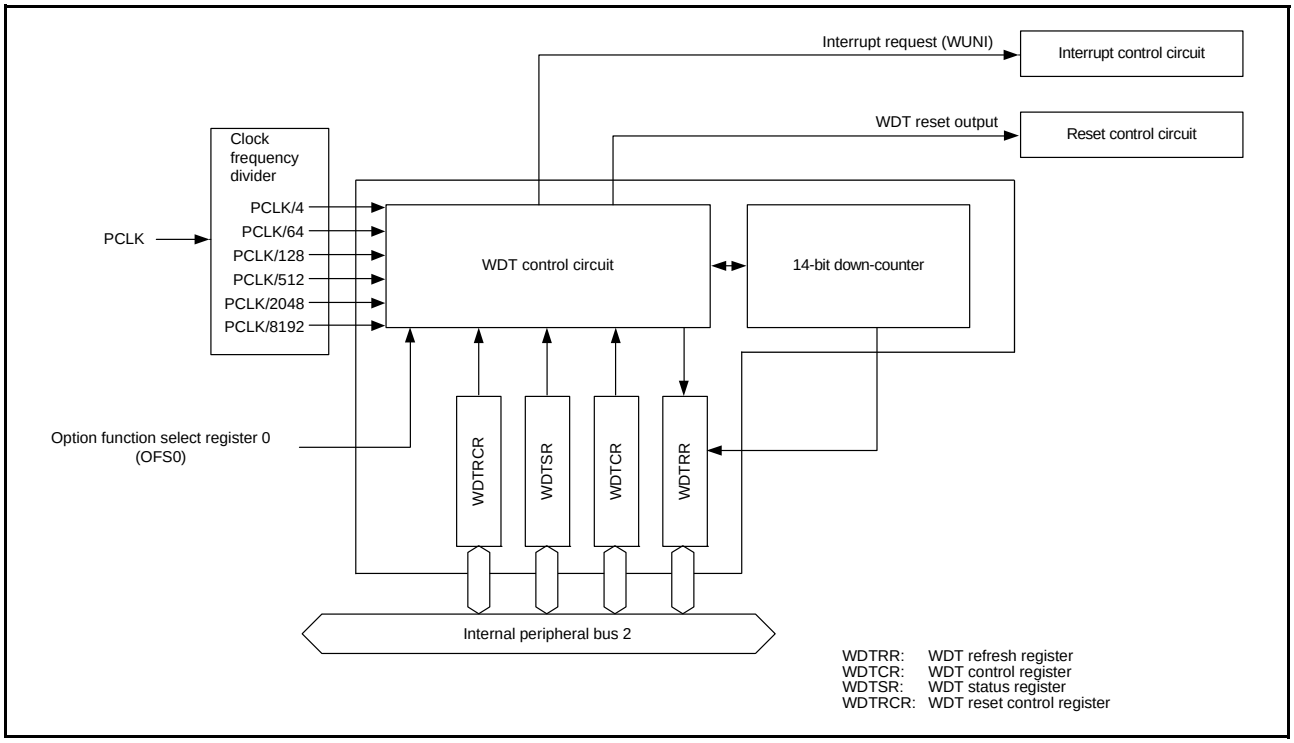
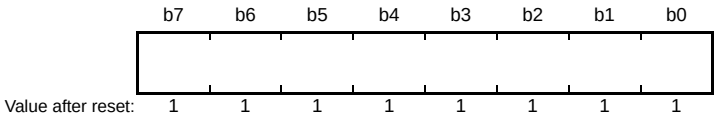


Figure 26.1 Block Diagram of WDT

26.2 Register Descriptions

26.2.1 WDT Refresh Register (WDTRR)

Address(es): 0008 8020h



Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register	R/W

WDTRR refreshes the down-counter of the WDT.
The down-counter of the WDT is refreshed by writing 00h and then writing FFh to WDTRR (refresh operation) within the refresh-permitted period.
After the down-counter has been refreshed, it starts counting down from the value selected by setting the WDT time-out period selection (OFS0.WDTTOPS[1:0]) bits in option function select register 0 in auto-start mode. In register start mode, counting down starts from the value selected by setting the time-out period selection (WDTCR.TOPS[1:0]) bits in the WDT control register by the first refresh operation after release from the reset state.
When 00h is written, the read value is 00h, when a value other than 00h is written, the read value is FFh.
For details of the refresh operation, refer to section 26.3.3, Refresh Operation.

26.2.2 WDT Control Register (WDTCR)

Address(es): 0008 8022h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TOPS[1:0]	Time-Out Period Selection	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	R/W
b3, b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7 to b4	CKS[3:0]	Clock Division Ratio Selection	b7 b4 0 0 0 1: PCLK/4 0 1 0 0: PCLK/64 1 1 1 1: PCLK/128 0 1 1 0: PCLK/512 0 1 1 1: PCLK/2048 1 0 0 0: PCLK/8192 Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Selection	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (window end position is not specified)	R/W
b11, b10	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b13, b12	RPSS[1:0]	Window Start Position Selection	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (window start position is not specified)	R/W
b15, b14	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

There are some restrictions on writing to the WDTCR register. For details, refer to section 26.3.2, Control over Writing to the WDTCR and WDTRCR Registers.

In auto-start mode, the settings in the WDTCR register are disabled, and the settings in the option function select register 0 (OFS0) are enabled. The bit setting made to the WDTCR register can also be made in the OFS0 register. For details, refer to section 26.3.8, Correspondence between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] Bits (Time-Out Period Selection)

The TOPS[1:0] bits select the time-out period (period until the down-counter underflows) from among 1,024, 4,096, 8,192, and 16,384 cycles, taking the divided clock specified by the CKS[3:0] bits as one cycle.

After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the time (number of PCLK cycles) until the counter underflows.

Relations between the CKS[3:0] and TOPS[1:0] bit settings, the time-out period, and the number of PCLK cycles are listed in Table 26.2.

Table 26.2 Time-Out Period Settings

CKS[3:0] Bits				TOPS[1:0] Bits		Clock Division Ratio	Time-Out Period (Number of Cycles)	Cycles of PCLK Clock
b7	b6	b5	b4	b1	b0			
0	0	0	1	0	0	PCLK/4	1024	4096
				0	1		4096	16384
				1	0		8192	32768
				1	1		16384	65536
0	1	0	0	0	0	PCLK/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	PCLK/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	1	0	0	0	PCLK/512	1024	524288
				0	1		4096	2097152
				1	0		8192	4194304
				1	1		16384	8388608
0	1	1	1	0	0	PCLK/2048	1024	2097152
				0	1		4096	8388608
				1	0		8192	16777216
				1	1		16384	33554432
1	0	0	0	0	0	PCLK/8192	1024	8388608
				0	1		4096	33554432
				1	0		8192	67108864
				1	1		16384	134217728

CKS[3:0] Bits (Clock Division Ratio Selection)

These bits select the peripheral clock (PCLK) division ratio from among division by 4, 64, 128, 512, 2,048, and 8,192. Combined with the TOPS[1:0] bit setting, a count period between 4,096 and 134, 217, 728 cycles of the PCLK clock can be selected for the WDT.

RPES[1:0] Bits (Window End Position Selection)

These bits select 75%, 50%, 25%, or 0% of the count period for the window end position of the down-counter. The window end position should be a value smaller than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

The counter values for the window start and end positions selected by setting the RPSS[1:0] and RPES[1:0] bits change depending on the TOPS[1:0] bit setting.

Table 26.3 lists the counter values for the window start and end positions corresponding to the TOPS[1:0] bit values.

Table 26.3 Correspondence between Time-Out Period and Window Start and End Counter Values

TOPS[1:0] Bits		Time-Out Period		Window Start and End Counter Value			
		Cycles	Counter Value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] Bits (Window Start Position Selection)

These bits select 100%, 75%, 50%, or 25% of the count period for the window start position of the down-counter (100% when the count starts and 0% when the counter underflows). The interval between the window start position and window end position is the refresh-permitted period and the other periods are refresh-prohibited periods.

Figure 26.2 shows the relationship between the RPSS[1:0] and RPES[1:0] bit settings and the refresh-permitted and refresh-prohibited periods.

RPSS[1:0] Bits		RPES[1:0] Bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

Note: • If window end setting ≥ window start setting, the window end setting is set to 0%.

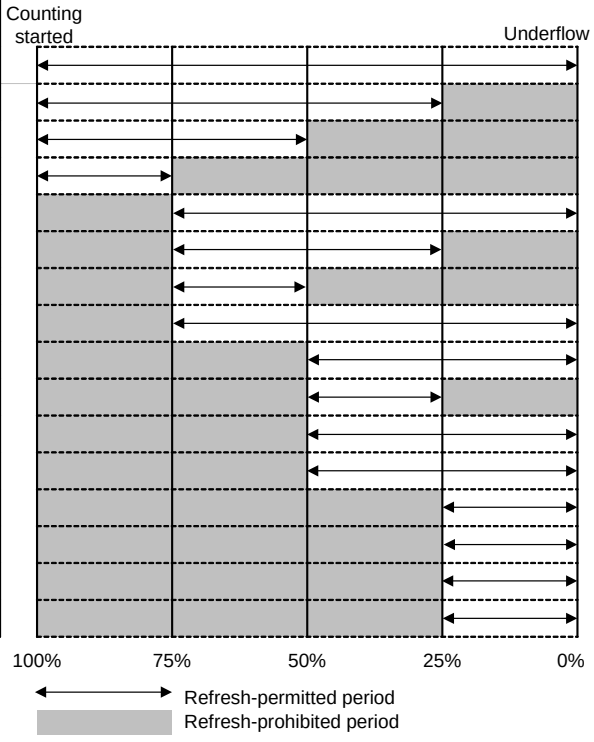


Figure 26.2 RPSS[1:0] and RPES[1:0] Bit Settings and the Refresh-Permitted Period

26.2.3 WDT Status Register (WDTSR)

Address(es): 0008 8024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred	R(/W) *1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

WDTSR is initialized by the reset source of the WDT. WDTSR is not initialized by other reset sources.

CNTVAL[13:0] Bits (Down-Counter Value)

Read these bits to confirm the value of the down-counter, but note that the read value may differ from the actual count by a value of one count.

UNDFF Flag (Underflow Flag)

Read this bit to confirm whether or not an underflow has occurred in the down-counter.
The value 1 indicates that the down-counter has underflowed. The value 0 indicates that the down-counter has not underflowed.
Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

REFEF Flag (Refresh Error Flag)

Read this bit to confirm whether or not a refresh error (performing a refresh operation during a refresh-prohibited period) has occurred.
The value 1 indicates that a refresh error has occurred. The value 0 indicates that no refresh error has occurred.
Clear the REFEF flag by writing 0 to it. Writing 1 has no effect.

26.2.4 WDT Reset Control Register (WDTRCR)

Address(es): 0008 8026h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	RSTIRQS	Reset Interrupt Request Selection	0: Non-maskable interrupt request output is enabled 1: Reset output is enabled	R/W

There are some restrictions on writing to the WDTRCR register. For details, refer to section 26.3.2, Control over Writing to the WDTCR and WDTRCR Registers.

In auto-start mode, the WDTRCR register settings are disabled, and the settings in the option function select register 0 (OFS0) enabled. The bit setting made to the WDTCR register can also be made in the OFS0 register. For details, refer to section 26.3.8, Correspondence between Option Function Select Register 0 (OFS0) and WDT Registers.

26.2.5 Option Function Select Register 0 (OFS0)

For details on the OFS0 register, refer to section 26.3.8, Correspondence between Option Function Select Register 0 (OFS0) and WDT Registers.

26.3 Operation

26.3.1 Count Operation in Each Start Mode

Select the WDT start mode by setting the WDT start mode selection bit (OFS0.WDTSTRT) in the option function select register 0.
When the OFS0.WDTSTRT bit is 1 (register start mode), the WDT control register (WDTCR) and WDT reset control register (WDTRCR) are enabled, and counting is started by refreshing (writing) the WDT refresh register (WDTRR).
When the OFS0.WDTSTRT bit is 0 (auto-start mode), the OFS0 register is enabled, and counting automatically starts after reset.

26.3.1.1 Register Start Mode

When the WDT start mode selection (OFS0.WDTSTRT) bit in the option function select register 0 is 1, register start mode is selected, and the WDT control register (WDTCR) and WDT reset control register (WDTRCR) are enabled. After cancelling from the reset, set the clock division ratio, window start and end positions, and time-out period in the WDTCR register, and the reset output or interrupt request output in the WDTRCR register. Then, refresh the down-counter to start counting down from the value selected by setting the time-out period selection (WDTCR.TOPS[1:0]) bits.
Thereafter, as long as the program continues normal operation and the counter is refreshed in the refresh-permitted period, the value in the counter is re-set each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as this continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs a reset signal or a non-maskable interrupt request (WUNI). Select reset output or interrupt request output by setting the reset interrupt request selection (WDTRCR.RSTIRQS) bit.

Figure 26.3 shows an example of operation under the following conditions.

- The WDT start mode selection (OFS0.WDTSTRT) bit is 1 (register start mode)
- The reset interrupt request selection (WDTRCR.RSTIRQS) bit is 1 (reset output is enabled)
- The window start position selection (WDTCR.RPSS[1:0]) bits are 10b (75%)
- The window end position selection (WDTCR.RPES[1:0]) bits are 10b (25%)

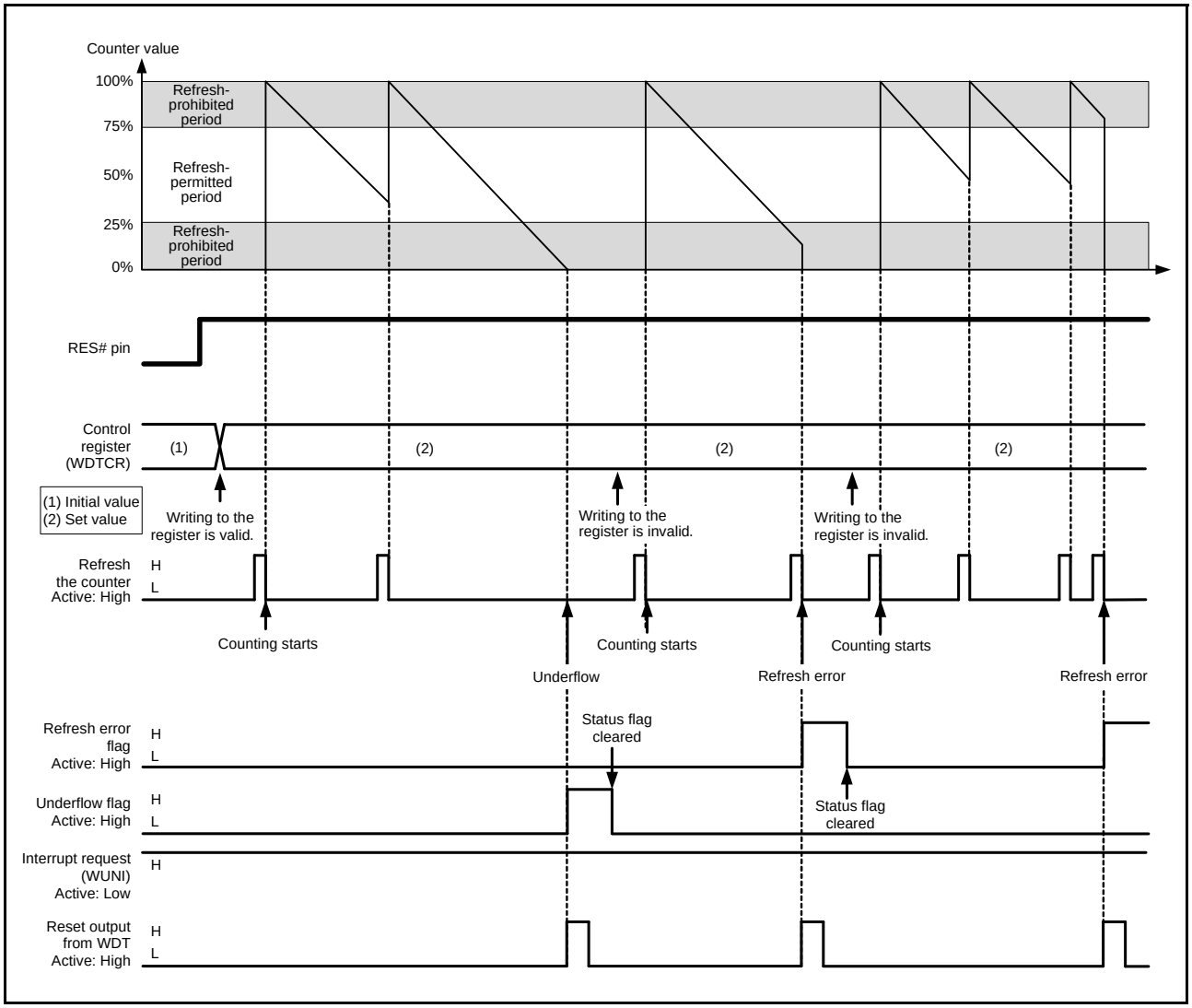


Figure 26.3 Operation Example in Register Start Mode

26.3.1.2 Auto-Start Mode

When the WDT start mode selection (OFS0.WDTSTRT) bit in the option function select register 0 is 0, auto-start mode is selected, and the WDT control register (WDTCR) and WDT reset control register (WDTRCR) are disabled.
Within the reset state, the clock division ratio, window start and end positions, time-out period, and reset output or interrupt request output are set by the option function select register (OFS0). When the reset state is canceled, the down-counter automatically starts counting down from the value selected by the WDT time-out period selection (OFS0.WDTTOPS[1:0]) bits.
After that, as long as the program continues normal operation and the counter is refreshed in the refresh-permitted period, the value in the counter is re-set when the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as this continues. However, if the down-counter underflows because refreshing of the down-counter is not possible due to the program having entered crashed execution or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT outputs the reset signal or non-maskable interrupt request (WUNI). After output of the reset or non-maskable interrupt request for one cycle of counting, the down-counter is reloaded and counting is restarted when the time-out interval elapses. The reset output or interrupt request output can be selected through the WDT reset interrupt request selection (OFS0.WDTRSTIRQS) bit.

Figure 26.4 shows an example of operation under the following conditions.

- The WDT start mode select (OFS0.WDTSTRT) bit is 0 (auto-start mode)
- The reset interrupt request select (OFS0.WDTRSTIRQS) bit is 0 (non-maskable interrupt request output is enabled)
- The window start position select (OFS0.WDTRPSS[1:0]) bits are 10b (75%)
- The window end position select (OFS0.WDTRPES[1:0]) bits are 10b (25%)

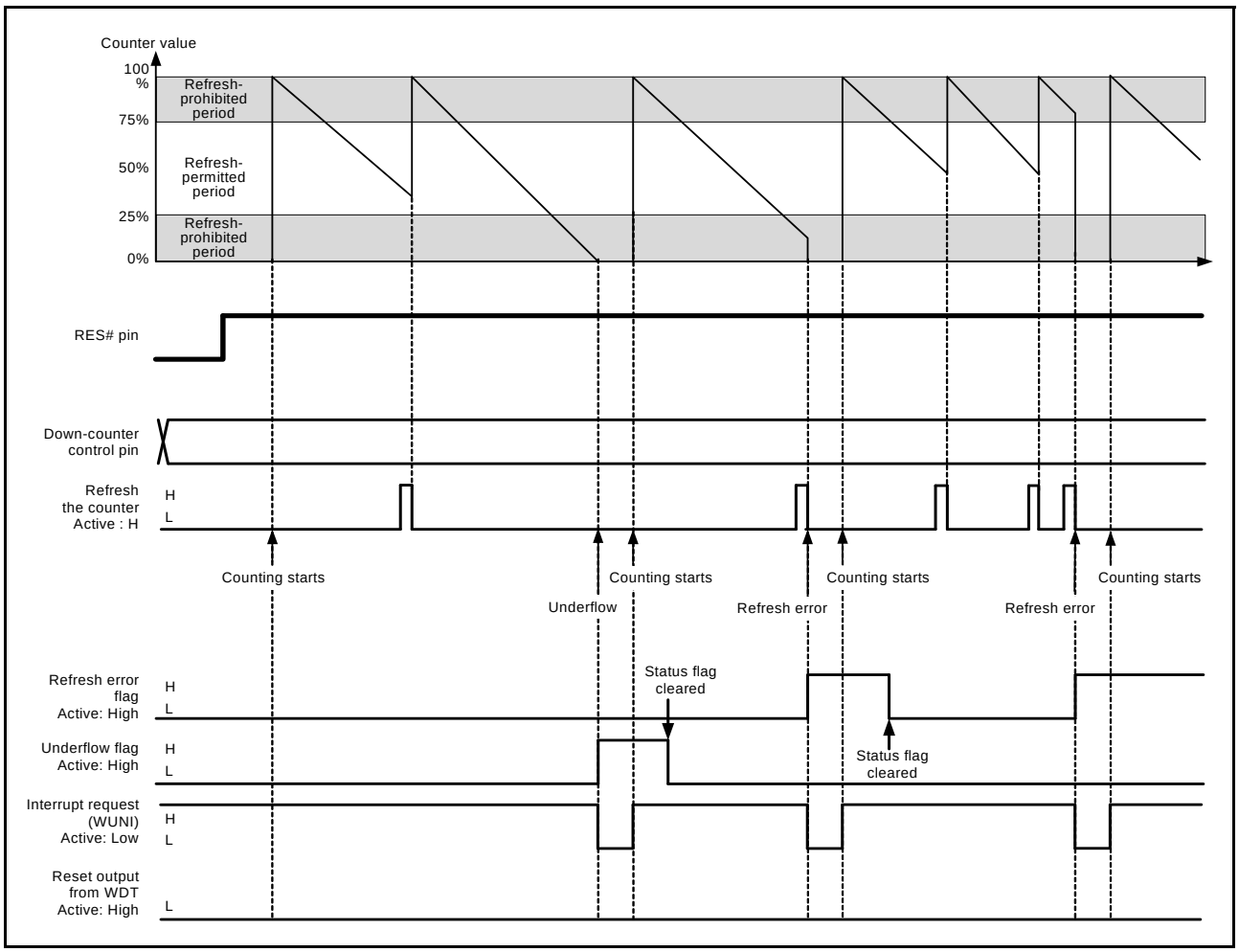


Figure 26.4 Operation Example in Auto-Start Mode

26.3.2 Control over Writing to the WDTCR and WDTRCR Registers

Writing to the WDT control register (WDTCR) or WDT reset control register (WDTRCR) is only possible once between the release from the reset state and the first refresh operation.

After a refresh operation (counting starts) or by writing to WDTCR or WDTRCR, the protection signal in the WDT becomes 1 to protect WDTCR and WDTRCR against subsequent attempts at writing.

This protection is released by the reset source of the WDT. With other reset sources, the protection is not released.

Figure 26.5 shows control waveforms produced in response to writing to the WDTCR.

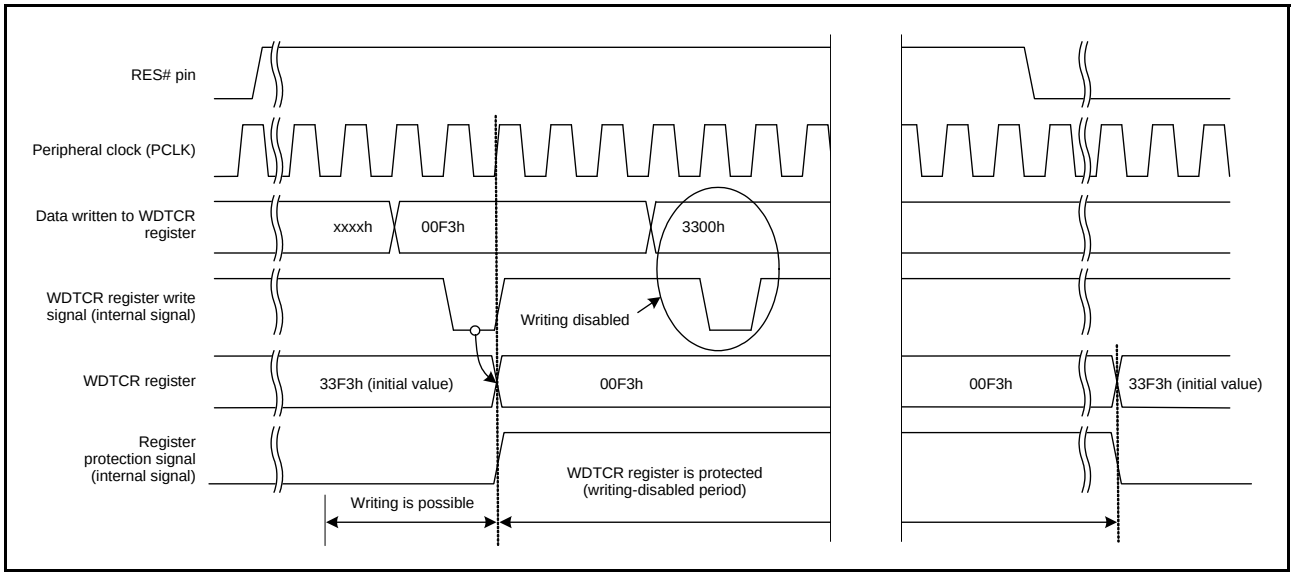


Figure 26.5 Control Waveforms Produced in Response to Writing to the WDTCR

26.3.3 Refresh Operation

The down-counter is refreshed and starts operation (counting is started by refreshing) by writing the values 00h and then FFh to the WDT refresh register (WDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. After such invalid writing, correct refreshing is performed by again writing 00h and then FFh to the WDT refresh register (WDTRR).

When writing is done in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied; writing 00h (n–1-th time) → 00h (n–th time) → FFh is valid and correct refreshing will be done. Even when the first value written before 00h is not 00h, correct refreshing will be done if the operation contains the set of writing 00h → FFh. Moreover, even if a register other than WDTRR is accessed or WDTRR is read between writing 00h and writing FFh to WDTRR, correct refreshing will be done.

[Sample sequences of writing that are valid for refreshing the counter]

- 00h→FFh
- 00h (n–1-th time) → 00h (n-th time) → FFh
- 00h→access to another register or read from WDTRR→FFh

[Sample sequences of writing that are not valid for refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h→54h (a value other than FFh)
- 00h→AAh (00h and a value other than FFh) → FFh

Even when 00h is written to WDTRR outside the refresh-permitted period, if FFh is written to WDTRR in the refresh-permitted period, the writing sequence is valid and refreshing will be done.

After FFh is written to the WDTRR register, refreshing the down-counter requires up to four cycles of the signal for counting (the clock division ratio selection (WDTCR.CKS[3:0]) bits determine how many cycles of the peripheral clock (PCLK) make up one cycle for counting). Therefore, writing FFh to the WDTRR should be completed four-count cycles before the end position of the refresh-permitted period or a counter underflow. The value of the down-counter can be checked by the down-counter value bits (WDTSR.CNTVAL[13:0]).

[Sample refreshing timings]

- When the window start position is set to 1FFFh, even if 00h is written to WDTRR before 1FFFh is reached (2002h, for example), refreshing is done if FFh is written to WDTRR after the value of the WDTSR.CNTVAL[13:0] bits has reached 1FFFh.
- When the window end position is set to 1FFFh, refreshing is done if 2003h (four-count cycles before 1FFFh) or a greater value is read from the WDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to WDTRR.
- When the refresh-permitted period continues until count 0000h, refreshing can be done immediately before an underflow. In this case, if 0003h (four-count cycles before an underflow) or a greater value is read from the WDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to WDTRR, no underflow occurs and refreshing is done.

Figure 26.6 shows the WDT refresh-operation waveforms when the clock division ratio = PCLK/64.

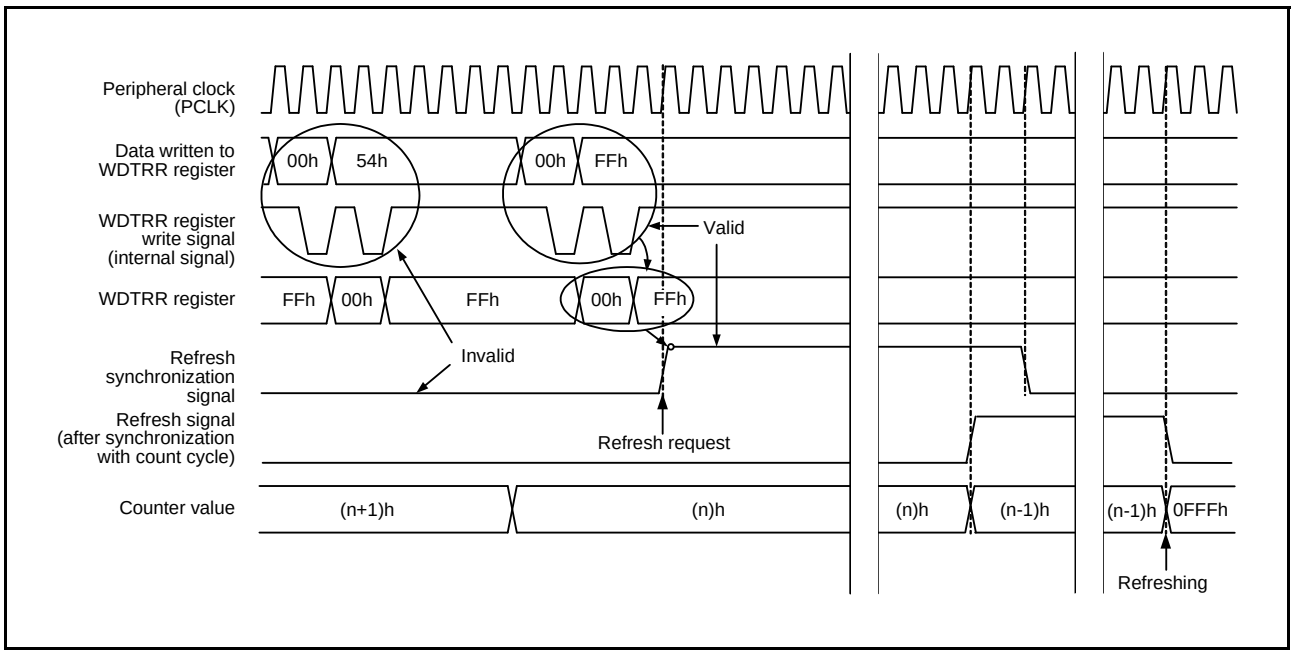


Figure 26.6 WDT Refresh Operation Waveforms (WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b)

26.3.4 Status Flags

The refresh error (WDTSR.REFEF) and underflow (WDTSR.UNDFF) flags retain the source of the reset signal output from the WDT or the source of the interrupt request from the WDT.

Thus, after release from the reset state or interrupt request generation, read the WDTSR.REFEF and WDTSR.UNDFF flags to check for the reset or interrupt source.

For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared, at the time of the next reset or interrupt request from the WDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written.

In addition, several (at least five) cycles of the PCLK. are required to read the reflected value after clearing the flag by writing 0 to the bit.

26.3.5 Reset Output

When the reset interrupt selection (WDTRCR.RSTIRQS) bit is set to 1 in register start mode or when the WDT reset interrupt request selection (OFS0.WDTRSTIRQS) bit in the option function select register 0 is set to 1 in auto-start mode, a reset signal is output for one-count cycle when an underflow in the down-counter or a refresh error occurs.
In register start mode, the down-counter is initialized (all bits cleared to 0) and kept in that state after assertion of the reset signal. After the reset is cancelled and the program is restarted, the counter is set up again and counting down is started by refreshing.
In auto-start mode, counting down automatically starts after the reset output.

26.3.6 Interrupt Source

When the reset interrupt selection (WDTRCR.RSTIRQS) bit is set to 0 in register start mode or when the WDT reset interrupt request selection (OFS0.WDTRSTIRQS) bit in the option function select register 0 is set to 0 in auto-start mode, a non-maskable interrupt (WUNI) signal is output when an underflow in the down-counter or a refresh error occurs.

Table 26.4 WDT Interrupt Source

Name	Interrupt Source	DTC Activation	DMAC Activation
WUNI	Down-counter underflow Refresh error	Not possible	Not possible

26.3.7 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value (WDTSR.CNTVAL[13:0]) bits of the WDT status register. Thus, the counter value can be checked through the WDTSR.CNTVAL[13:0] bits.
Figure 26.7 shows the processing for reading the WDT down-counter value when the clock division ratio = PCLK/64.

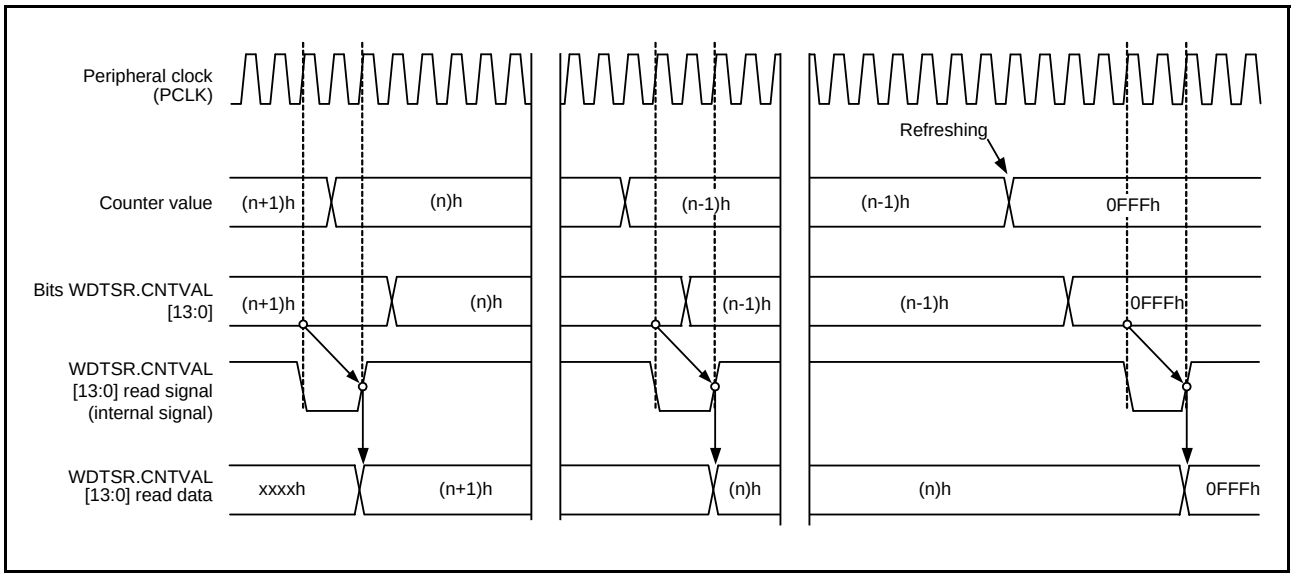


Figure 26.7 Processing for Reading WDT Down-Counter Value (WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b)

26.3.8 Correspondence between Option Function Select Register 0 (OFS0) and WDT Registers

Table 26.5 lists the correspondence between the option function select register 0 (OFS0) and the WDT registers (WDT control register (WDTCR) and WDT reset control register (WDTRCR)) regarding control of the down-counter and reset or interrupt request output. Control can be switched between the OFS0 register and the WDT registers (WDTCR and WDTRCR) through the setting of the WDT start mode selection (OFS0.WDTSTRT) bit.
Note that the OFS0 register setting should be kept unchanged during WDT operation.
For details on the OFS0 register, see section 8.2.1, Option Function Select Register 0 (OFS0).

Table 26.5 Correspondence between Option Function Select Register 0 (OFS0) and WDT Registers

Target of Control	Function	OFS0 Register (Effective in Auto-Start Mode) OFS0.WDTSTRT = 0	WDT Registers (Effective in Register Start Mode) OFS0.WDTSTRT = 1
Down-counter	Time-out period selection	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position selection	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position selection	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output selection	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS

27. Independent Watchdog Timer (IWDTa)

The independent watchdog timer (IWDT) is used independently of the conventional watchdog timer to detect programs entering runaway conditions. The IWDT has a 14-bit down-counter, and can be set up so that the chip is reset by a reset output when counting down from the initial value causes an underflow of the counter. Alternatively, generation of an interrupt request is selectable when the counter underflows. The initial value for counting can be restored to the down-counter by refreshing its value. The interval over which refreshing is possible can also be selected. Refreshing the counter during this interval will restore its initial value for counting, while attempting to refresh the counter beyond this interval leads to the output of a reset or interrupt request. The refresh interval can be adjusted and used to detect the program entering runaway conditions. The IWDT stops counting after an underflow or an attempt at refreshing the counter beyond the allowed interval. Counting is restarted by refreshing the counter when the IWDT is in register start mode. When the IWDT is in auto-start mode, counting is restarted automatically after output of the reset or interrupt request.

27.1 Overview

The IWDT has two start modes: auto-start mode, in which counting automatically starts after release from the reset state, and register start mode, in which counting is started by refreshing the IWDT (writing to the register).
In auto-start mode, necessary settings (clock division ratio, refresh window start and end positions, time-out period, reset or non-maskable interrupt request output at an underflow, and count stop control in sleep mode) should be made in the option function select register 0 (OFS0) before release from the reset state. In register start mode, necessary settings (clock division ratio, refresh window start and end positions, time-out period, reset or non-maskable interrupt request output at an underflow, and count stop control in sleep mode) should be made in the respective registers before the counter is started by refreshing after release from the reset state.
In register start mode, necessary settings (clock division ratio, refresh window start and end positions, time-out period, reset or non-maskable interrupt request output at an underflow, and count stop control in sleep mode) should be made in the respective registers before the counter is started by refreshing after release from the reset state.
Set the IWDT start mode select bit (OFS0.IWDTSTRT) to select auto-start mode or register start mode.
When auto-start mode is selected (OFS0.IWDTSTRT = 0), the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR) settings are disabled and the OFS0 register settings are enabled.
When register start mode is selected (OFS0.IWDTSTRT = 1), the OFS0 register settings are ignored and the IWDTCR, IWDTRCR, and IWDTCSTPR settings take effect.
Specifications of the IWDT are listed in Table 27.1.

Table 27.1 Specifications of IWDT (1/2)

Item	Specifications
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started by refreshing the IWDTRR register (writing 00h and then FFh) (register start mode)
Conditions for stopping the counter	• Pin reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated Count restarts automatically in auto-start mode, or by refreshing the counter in register start mode
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset-output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Interrupt request output sources	• A non-maskable interrupt () is generated by an underflow of the down-counter • When refreshing is done outside the refresh-permitted period (refresh error)

Table 27.1 Specifications of IWDT (2/2)

Item	Specifications
Reading the counter value	The down-counter value can be read by the IWDTSR register.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output
Auto-start mode (controlled by the option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the time-out period of the watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the time-out period of the watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Note 1. Set the count source so that the peripheral module clock frequency ≥ 4 x (the count source clock divided frequency).

To use the IWDT, two clocks (peripheral clock (PCLK) and IWDT-dedicated clock (IWDTCLK)) should be supplied so that the IWDT works while the peripheral clock (PCLK) stops. The bus interface and registers operate with PCLK, and the 14-bit down-counter and control circuits operate with IWDTCLK.
Signal lines between the blocks operating with the peripheral clock and IWDT-dedicated clock are connected through synchronization circuits.
Figure 27.1 is a block diagram of the IWDT

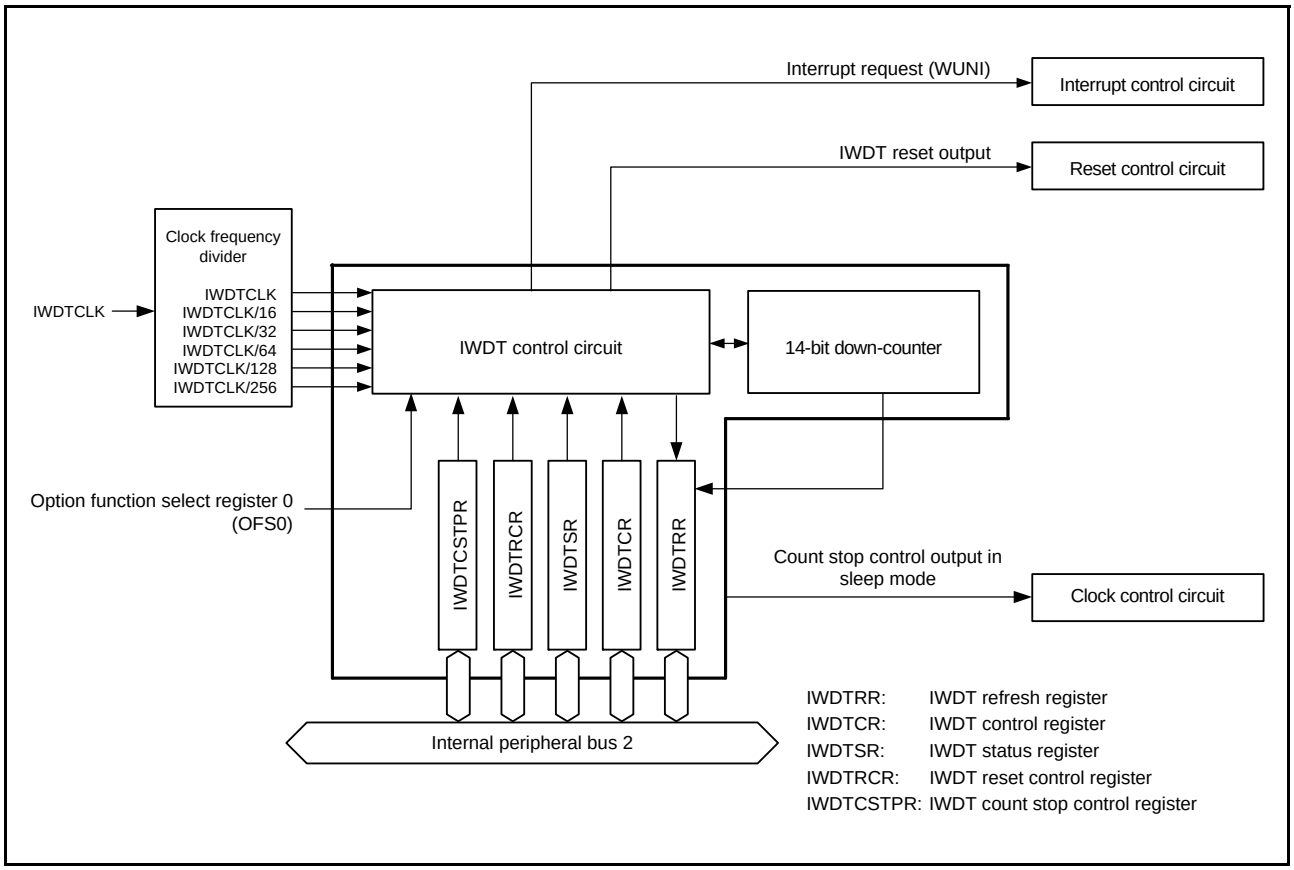
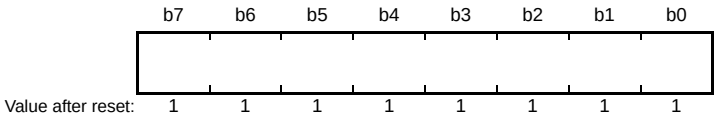


Figure 27.1 Block Diagram of IWDT

27.2 Register Descriptions

27.2.1 IWDT Refresh Register (IWDTRR)

Address(es): 0008 8030h



Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register	R/W

IWDTRR refreshes the down-counter of the IWDT.
The down-counter of the IWDT is refreshed by writing 00h and then writing FFh to IWDTRR (refresh operation) within the refresh-permitted period.
After the down-counter has been refreshed, it starts counting down from the value selected by the IWDT time-out period selection (OFS0.IWDTTOPS[1:0]) bits in option function select register 0 in auto-start mode. In register start mode, counting down starts from the value selected by setting the time-out period selection (TOPS[1:0]) bits in the IWDT control register (IWDTCR) in the first refresh operation after release from the reset state.
When 00h is written, the read value is 00h. When a value other than 00h is written, the read value FFh.
For details of the refresh operation, refer to section 27.3.3, Refresh Operation.

27.2.2 IWDT Control Register (IWDTCR)

Address(es): 0008 8032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TOPS[1:0]	Time-Out Period Selection	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	R/W
b3, b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7 to b4	CKS[3:0]	Clock Division Ratio Selection	b7 b4 0 0 0 0: IWDTCLK 0 0 1 0: IWDTCLK/16 0 0 1 1: IWDTCLK/32 0 1 0 0: IWDTCLK/64 1 1 1 1: IWDTCLK/128 0 1 0 1: IWDTCLK/256 Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Selection	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (window end position is not specified)	R/W
b11, b10	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b13, b12	RPSS[1:0]	Window Start Position Selection	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (window start position is not specified)	R/W
b15, b14	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

There are some restrictions on writing to the IWDTCR register. For details, refer to section 27.3.2, Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers.

In auto-start mode, the settings in the IWDTCR register are disabled, and the settings in the option function select register 0 (OFS0) are enabled. The bit setting made to the IWDTCR register can also be made in the OFS0 register. For details, refer to section 27.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

TOPS[1:0] Bits (Time-Out Period Selection)

The TOPS[1:0] bits select the time-out period (period until the down-counter underflows) from among 1,024, 4,096, 8,192, or 16,384 cycles, taking the divided clock specified by the CKS[3:0] bits as one cycle.
After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the time (number of IWDTCLK cycles) until the counter underflows.
Relations between the CKS[3:0] and TOPS[1:0] bit settings, the time-out period, and the number of IWDTCLK cycles are listed in Table 27.2.

Table 27.2 Settings and Time-Out Periods

CKS[3:0] Bits				TOPS[1:0] Bits				
b7	b6	b5	b4	b1	b0	Clock Division Ratio	Time-Out Period (Number of Cycles)	Cycles of IWDTCLK
0	0	0	0	0	0	IWDTCLK	1024	1024
				0	1		4096	4096
				1	0		8192	8192
				1	1		16384	16384
0	0	1	0	0	0	IWDTCLK/16	1024	16384
				0	1		4096	65536
				1	0		8192	131072
				1	1		16384	262144
0	0	1	1	0	0	IWDTCLK/32	1024	32768
				0	1		4096	131072
				1	0		8192	262144
				1	1		16384	524288
0	1	0	0	0	0	IWDTCLK/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	IWDTCLK/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	0	1	0	0	IWDTCLK/256	1024	262144
				0	1		4096	1048576
				1	0		8192	2097152
				1	1		16384	4194304

CKS[3:0] Bits (Clock Division Ratio Selection)

These bits select the IWDTCLK clock division ratio from among division by 1, 16, 32, 64, 128, and 256. Combined with the TOPS[1:0] bit setting, a count period between 1,024 and 4,194, 304 cycles of the IWDTCLK clock can be selected for the IWDT.

RPES[1:0] Bits (Window End Position Selection)

These bits select 75%, 50%, 25% or 0% of the count period for the window end position of the down-counter. The window end position should be a value smaller than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

The counter values for the window start and end positions selected by setting the RPSS[1:0] and RPES[1:0] bits change depending on the TOPS[1:0] bit setting.

Table 27.3 lists the counter values for the window start and end positions corresponding to TOPS[1:0] bit values.

Table 27.3 Relationship between Time-Out Period and Window Start and End Counter Values

TOPS[1:0] Bits		Time-Out Period		Window Start and End Counter Value			
b1	b0	Cycles	Counter Value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] Bits (Window Start Position Selection)

These bits select 100%, 75%, 50%, or 25% of the count period for the window start position for the down-counter (100% when the count starts and 0% when the counter underflows). The interval between the window start position and window end position is the refresh-permitted period and the other periods are refresh-prohibited periods.

Figure 27.2 shows the relationship between the RPSS[1:0] and RPES[1:0] bit setting and the refresh-permitted and refresh-prohibited periods.

RPSS[1:0] Bits		RPES[1:0] Bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

Note: • If window end setting ≥ window start setting, the window end setting is set to 0%.

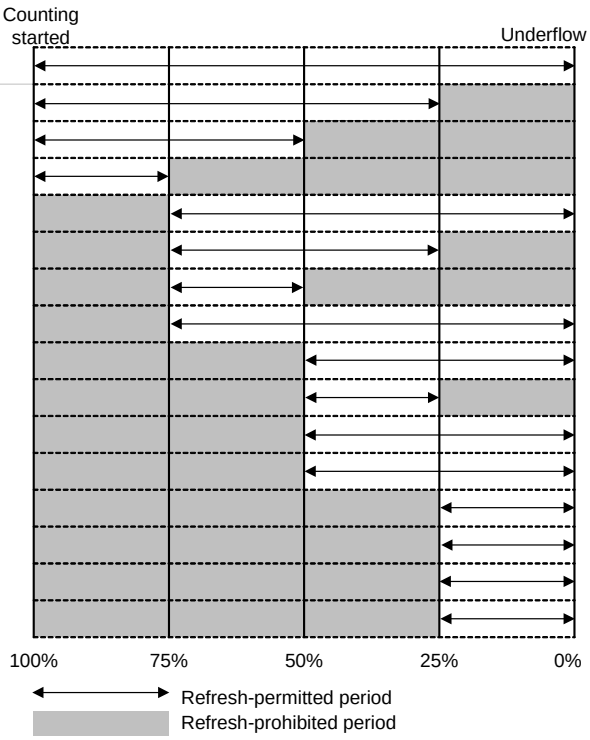


Figure 27.2 RPSS[1:0] and RPES[1:0] Bit Settings and the Refresh-Permitted Period

27.2.3 IWDT Status Register (IWDTSR)

Address(es): 0008 8034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred	R(/W) *1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

IWDTSR is initialized by the reset source of the IWDT. IWDTSR is not initialized by other reset sources.

CNTVAL[13:0] Bits (Down-Counter Value)

Read these bits to confirm the value of the down-counter, but note that the read value may differ from the actual count by a value of one count.

UNDFF Flag (Underflow Flag)

Read this bit to confirm whether or not an underflow has occurred in the down-counter.
The value 1 indicates that the down-counter has underflowed. The value 0 indicates that the down-counter has not underflowed.
Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

REFEF Flag (Refresh Error Flag)

Read this bit to confirm whether or not a refresh error (performing a refresh operation during a refresh-prohibited period).
The value 1 indicates that a refresh error has occurred. The value 0 indicates that no refresh error has occurred.
Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

27.2.4 IWDT Reset Control Register (IWDTRCR)

Address(es): 0008 8036h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	RSTIRQS	Reset Interrupt Request Selection	0: Non-maskable interrupt request output is enabled 1: Reset output is enabled	R/W

There are some restrictions on writing to the IWDTRCR register. For details, refer to section 27.3.2, Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers.
In auto-start mode, the IWDTRCR register settings are disabled, and the settings in the option function select register 0 (OFS0) enabled. The bit setting mode to the IWDTRCR register can also be made in the OFS0 register. For details, refer to section 27.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

27.2.5 IWDT Count Stop Control Register (IWDTCSTPR)

Address(es): 0008 8038h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	SLCSTP	Sleep-Mode Count Stop Control	0: Count stop is disabled 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode	R/W

There are some restrictions on writing to the IWDTCSTPR register. For details, refer to section 27.3.2, Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers.
In auto-start mode, the settings in the IWDTCSTPR register are ignored, and the settings in the option function select register 0 (OFS0) take effect. The bit setting mode to the IWDTCSTPR register can also be made in the OFS0 register. For details, refer to section 27.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

SLCSTP Bit (Sleep-Mode Count Stop Control)

This bit selects whether to stop counting at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.

27.2.6 Option Function Select Register 0 (OFS0)

For the OFS0 register, refer to section 27.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

27.3 Operation

27.3.1 Count Operation in Each Start Mode

Select the IWDT start mode by setting the IWDT start mode selection bit (OFS0.IWDTSTRT) in the option function select register 0.
When the OFS0.IWDTSTRT bit is 1 (register start mode), the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR) are enabled, and counting is started by refreshing (writing) the IWDT refresh register (IWDTRR). When the OFS0.IWDTSTRT bit is 0 (auto-start mode), the setting of the OFS0 register is enabled, and counting automatically starts after reset.

27.3.1.1 Register Start Mode

When the IWDT start mode selection (OFS0.IWDTSTRT) bit in the option function select register 0 is 1, register start mode is selected, and the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR) are enabled.
After cancelling from the reset, set the clock division ratio, window start and end positions, and time-out period in the IWDTCR register, the reset output or interrupt request output in the IWDTRCR register, and the down-counter stop control at transitions to low-power-consumption modes in the IWDTCSTPR register. Then, refresh the down-counter to start counting down from the value selected by setting the time-out period selection (IWDTCR.TOPS[1:0]) bits.
Thereafter, as long as the program continues normal operation and the counter is refreshed in the refresh-permitted period, the value in the counter is re-set each time the counter is refreshed and counting down continues. The IWDT does not output the reset signal as long as this continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the IWDT outputs a reset signal or a non-maskable interrupt request (). Select reset output or interrupt request output by setting the reset interrupt request selection (IWDTRCR.RSTIRQS) bit.

Figure 27.3 shows an example of operation under the following conditions.

- The IWDT start mode selection (OFS0.IWDTSTRT) bit is 1 (register start mode)
- The reset interrupt request selection (IWDTRCR.RSTIRQS) bit is 1 (reset output is enabled)
- The window start position selection (IWDTCR.RPSS[1:0]) bits are 10b (75%)
- The window end position selection (IWDTCR.RPES[1:0]) bits are 10b (25%)

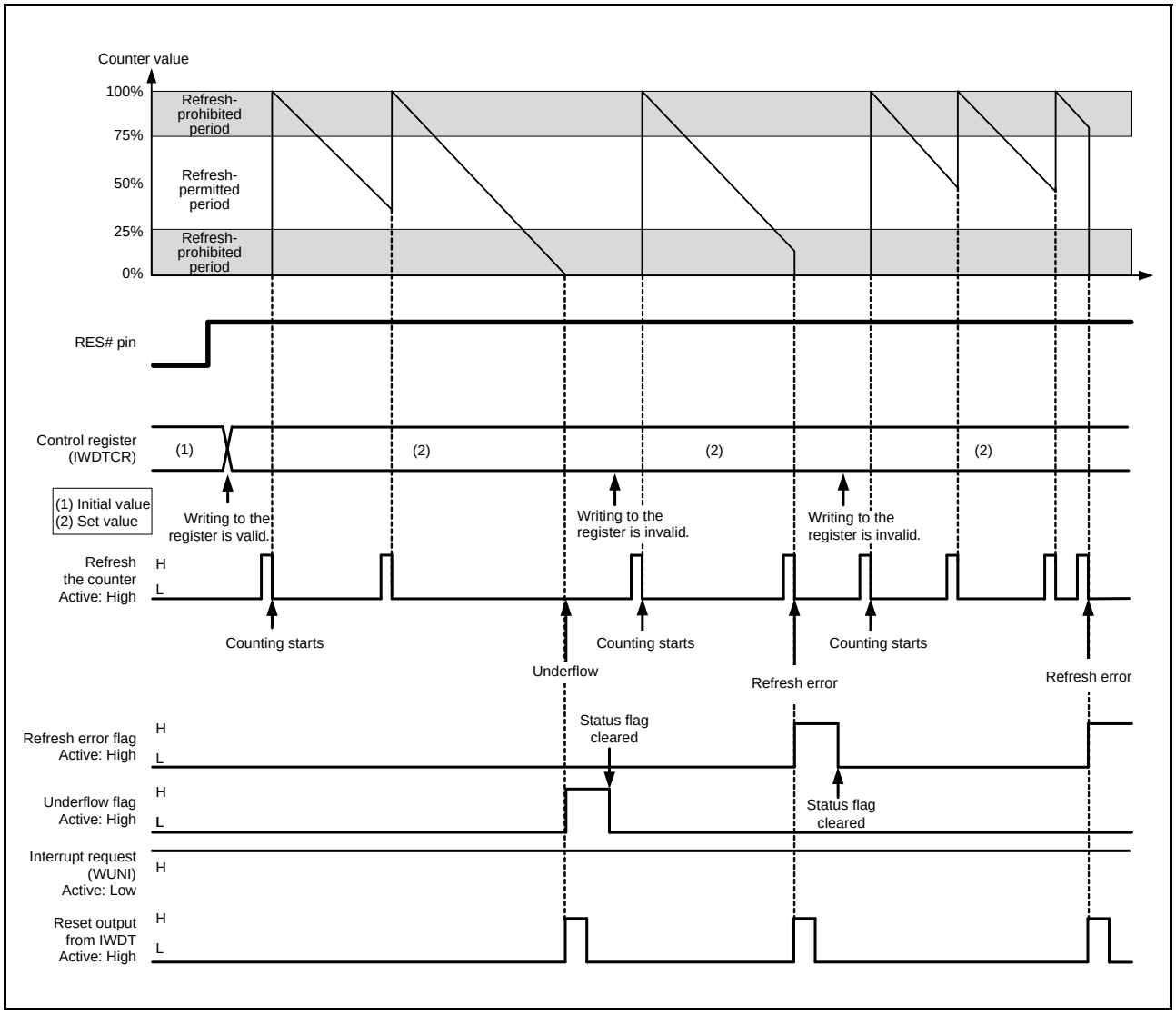


Figure 27.3 Operation Example in Register Start Mode

27.3.1.2 Auto-Start Mode

When the IWDT start mode selection (OFS0.IWDTSTRT) bit in the option function select register 0 is 0, auto-start mode is selected, and the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR) are disabled.

Within the reset state, the clock division ratio, window start and end positions, time-out period, reset output or interrupt request output, and down-counter stop control at transitions to low-power-consumption modes should be specified in the OFS0 register. When the reset state is canceled, the down-counter automatically starts counting down from the value selected by the IWDT time-out period selection (OFS0.IWDTTOPS[1:0]) bits.

After that, as long as the program continues normal operation and the counter is refreshed in the refresh-permitted period, the value in the counter is re-set when the counter is refreshed and counting down continues. The IWDT does not output the reset signal as long as this continues. However, if the down-counter underflows because refreshing of the down-counter is not possible due to the program having entered crashed execution or if a refresh error occurs due to refreshing outside the refresh-permitted period, the IWDT outputs the reset signal or non-maskable interrupt request (). After output of the reset or non-maskable interrupt request for one cycle of counting, the down-counter is reloaded and counting is restarted when the time-out interval elapses. The reset output or interrupt request output can be selected through the IWDT reset interrupt request selection (OFS0.IWDTRSTIRQS) bit.

Figure 27.4 shows an example of operation under the following conditions.

- The IWDT start mode selection (OFS0.IWDTSTRT) bit is 0 (auto-start mode)
- The reset interrupt request selection (OFS0.IWDTRSTIRQS) bit is 0 (non-maskable interrupt request output is enabled)
- The window start position selection (OFS0.IWDTRPSS[1:0]) bits are 10b (75%)
- The window end position selection (OFS0.IWDTRPES[1:0]) bits are 10b (25%)

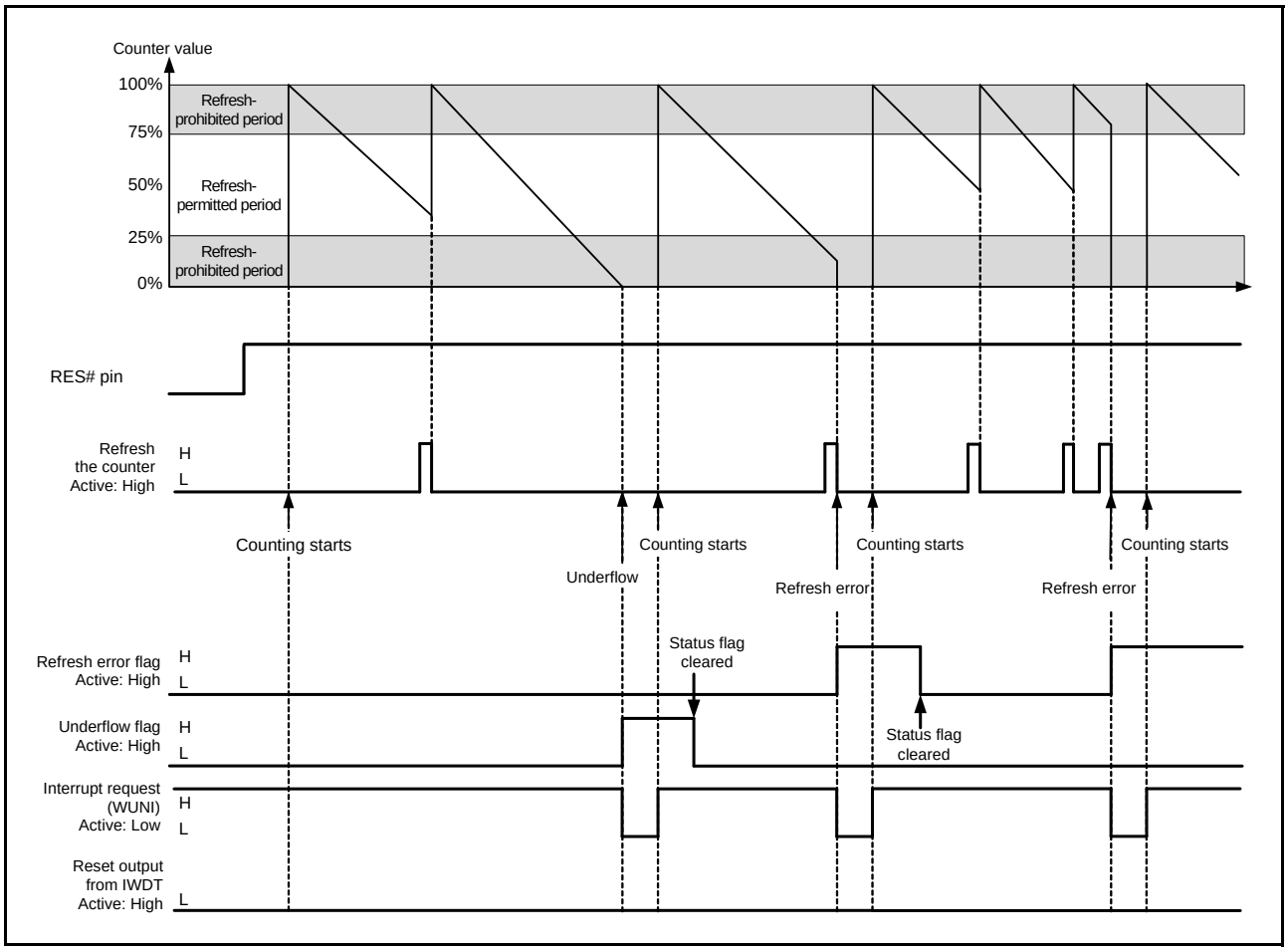


Figure 27.4 Operation Example in Auto-Start Mode

27.3.2 Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers

Writing to the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), or IWDT count stop control register (IWDTCSTPR) is only possible once between the release from the reset state and the first refresh operation. After a refresh operation (counting starts) or IWDTCR, IWDTRCR, or IWDTCSTPR is written to, the protection signal in the IWDT becomes 1 to protect IWDTCR, IWDTRCR, and IWDTCSTPR against subsequent attempts at writing. This protection is released by the reset source of the IWDT. With other reset sources, the protection is not released. Figure 27.5 shows control waveforms produced in response to writing to the IWDTCR.

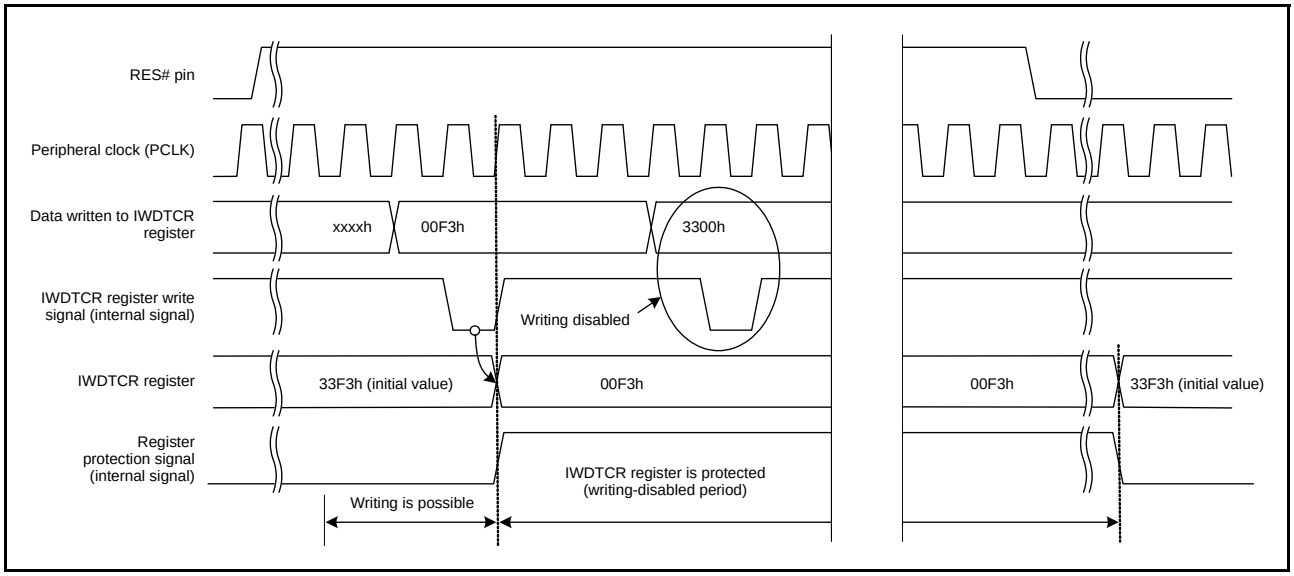


Figure 27.5 Control Waveforms Produced in Response to Writing to the IWDTCR

27.3.3 Refresh Operation

The down-counter is refreshed and starts operation (counting is started by refreshing) by writing the values 00h and then FFh to the IWDT refresh register (IWDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. After such invalid writing, correct refreshing is performed by again writing 00h and then FFh to the IWDT refresh register (IWDTRR).

When writing is done in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied; writing 00h (n–1-th time) → 00h (n–th time) → FFh is valid and correct refreshing will be done. Even when the first value written before 00h is not 00h, correct refreshing will be done if the operation contains the set of writing 00h → FFh. Moreover, even if a register other than IWDTRR is accessed or IWDTRR is read between writing 00h and writing FFh to IWDTRR, correct refreshing will be done.

[Sample sequences of writing that are valid for refreshing the counter]

- 00h→FFh
- 00h (n–1-th time) → 00h (n-th time) → FFh
- 00h→access to another register or read from IWDTRR→FFh

[Sample sequences of writing that are not valid for refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h→54h (a value other than FFh)
- 00h→AAh (00h and a value other than FFh) → FFh

Even when 00h is written to IWDTRR outside the refresh-permitted period, if FFh is written to IWDTRR in the refresh-permitted period, the writing sequence is valid and refreshing will be done.

After FFh is written to the IWDTRR register, refreshing the down-counter requires up to four cycles of the signal for counting (the clock division ratio selection (the clock division ratio selection (IWDTCR.CKS[3:0]) bits determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up one cycle for counting). Therefore, writing FFh to the IWDTRR should be completed four-count cycles before the end position of the refresh-permitted period or a counter underflow. The value of the down-counter can be checked by the counter bits (IWDTSR.CNTVAL[13:0]).

[Sample refreshing timings]

- When the window start position is set to 1FFFh, even if 00h is written to IWDTRR before 1FFFh is reached (2002h, for example), refreshing is done if FFh is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits has reached 1FFFh.
- When the window end position is set to 1FFFh, refreshing is done if 2003h (four-count cycles before 1FFFh) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR.
- When the refresh-permitted period continues until count 0000h, refreshing can be done immediately before an underflow. In this case, if 0003h (four-count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR, no underflow occurs and refreshing is done.

Figure 27.6 shows the IWDT refresh-operation waveforms when PCLK > IWDTCLK and clock division ratio = IWDTCLK, and Figure 27.7 shows those when PCLK < IWDTCLK and clock division ratio = IWDTCLK/16.

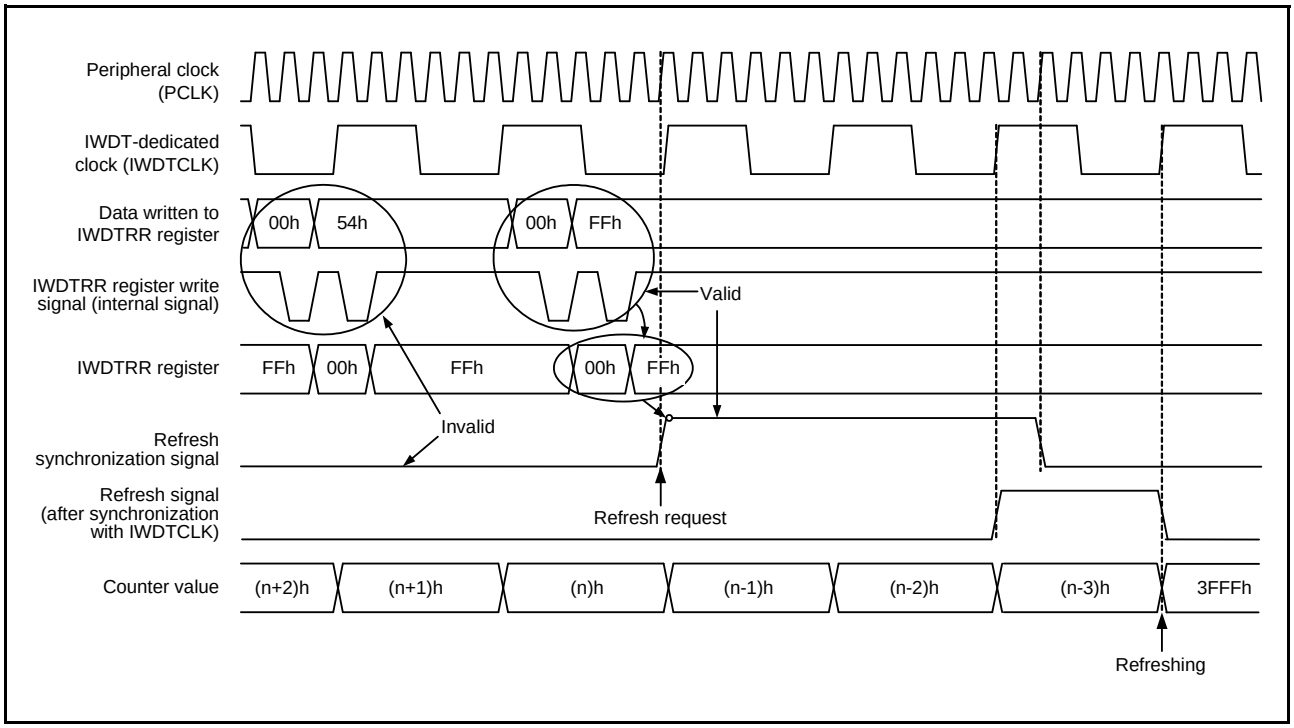


Figure 27.6 IWDT Refresh Operation Waveforms (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b)

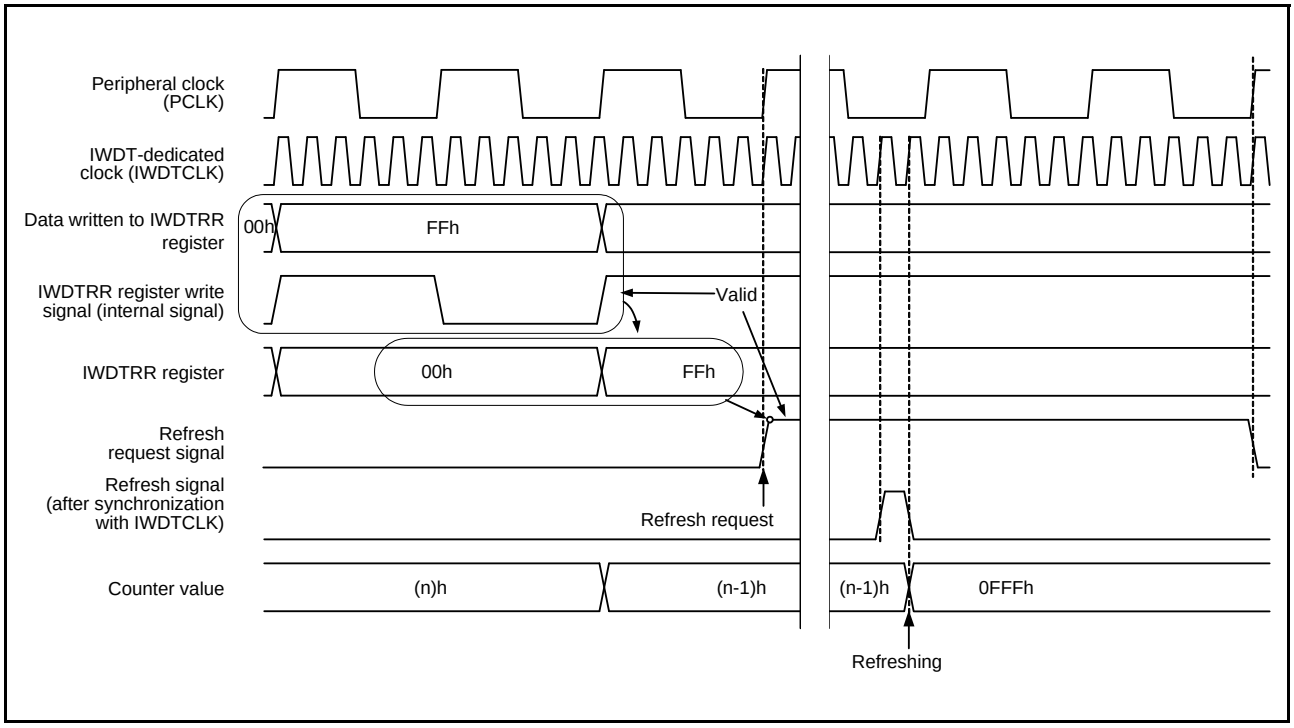


Figure 27.7 IWDT Refresh Operation Waveforms (IWDTCR.CKS[3:0] = 0010b, IWDTCR.TOPS[1:0] = 01b)

27.3.4 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the reset signal output from the IWDT or the source of the interrupt request from the IWDT.

Thus, after release from the reset state or interrupt request generation, read the IWDTSR.REFEF and IWDTSR.UNDFF flags to check for the reset or interrupt source.

For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared, at the time of the next reset or interrupt request from the IWDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written.

In addition, several cycles of the IWDTCLK (at least three) and of the PCLK (at least two) are required to read the reflected value after clearing the flag by writing 0 to the bit.

27.3.5 Reset Output

When the reset interrupt selection (IWDTRCR.RSTIRQS) bit is set to 1 in register start mode or when the IWDT reset interrupt request selection (OFS0.IWDTRSTIRQS) bit in the option function select register 0 is set to 1 in auto-start mode, a reset signal is output for one-count cycle when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits cleared to 0) and kept in that state after assertion of the reset signal. After the reset is cancelled and the program is restarted, the counter is set up again and counting down is started by refreshing.

In auto-start mode, counting down automatically starts after the reset output.

27.3.6 Interrupt Source

When the reset interrupt selection (IWDTRCR.RSTIRQS) bit is set to 0 in register start mode or when the IWDT reset interrupt request selection (OFS0.IWDTRSTIRQS) bit in the option function select register 0 is set to 0 in auto-start mode, a non-maskable interrupt () signal is output when an underflow in the down-counter or a refresh error occurs.

Table 27.4 IWDT Interrupt Source

Name	Interrupt Source	DTC Activation	DMAC Activation
	Down-counter underflow Refresh error	Not possible	Not possible

27.3.7 Reading the Down-Counter Value

As the down-counter in IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLK) and stores it in the down-counter value (IWDTSR.CNTVAL[13:0]) bits of the IWDT status register.
Thus, the counter value can be checked indirectly through the IWDTSR.CNTVAL[13:0] bits.
Reading the down-counter value requires multiple PCLK clock cycles (up to four clock cycles), and the read counter value may differ from the actual down-counter value by a value of one count.
Figure 27.8 shows the processing for reading the IWDT down-counter value when PCLK > IWDTCLK and clock division ratio = IWDTCLK, and Figure 27.9 shows the processing when PCLK < IWDTCLK and clock division ratio = IWDTCLK/16.

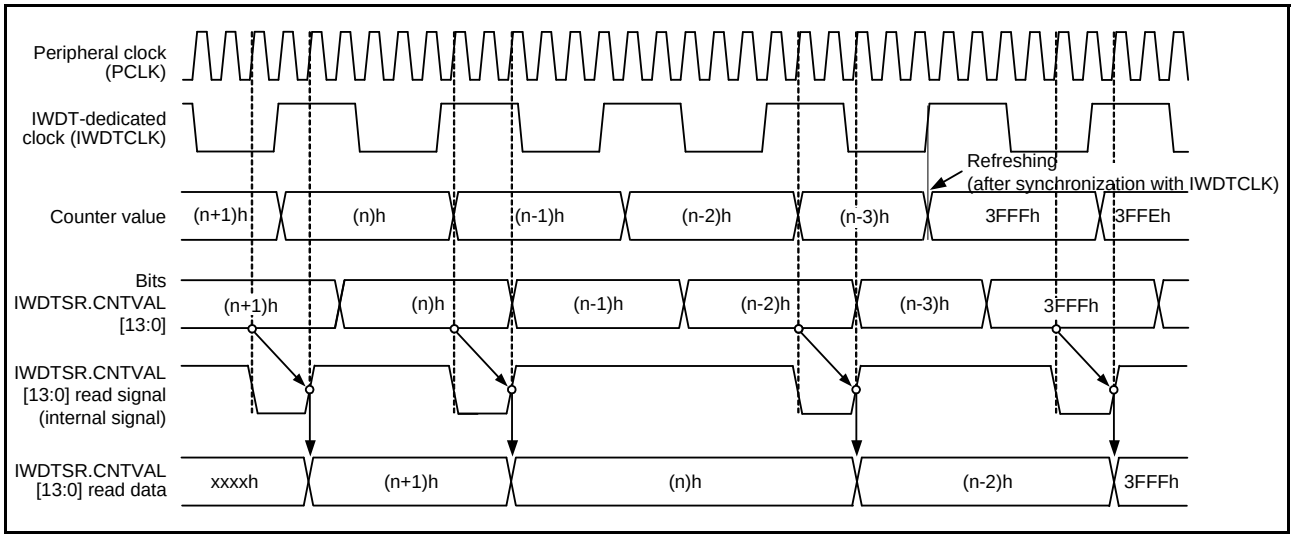


Figure 27.8 Processing for Reading IWDT Down-Counter Value (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b)

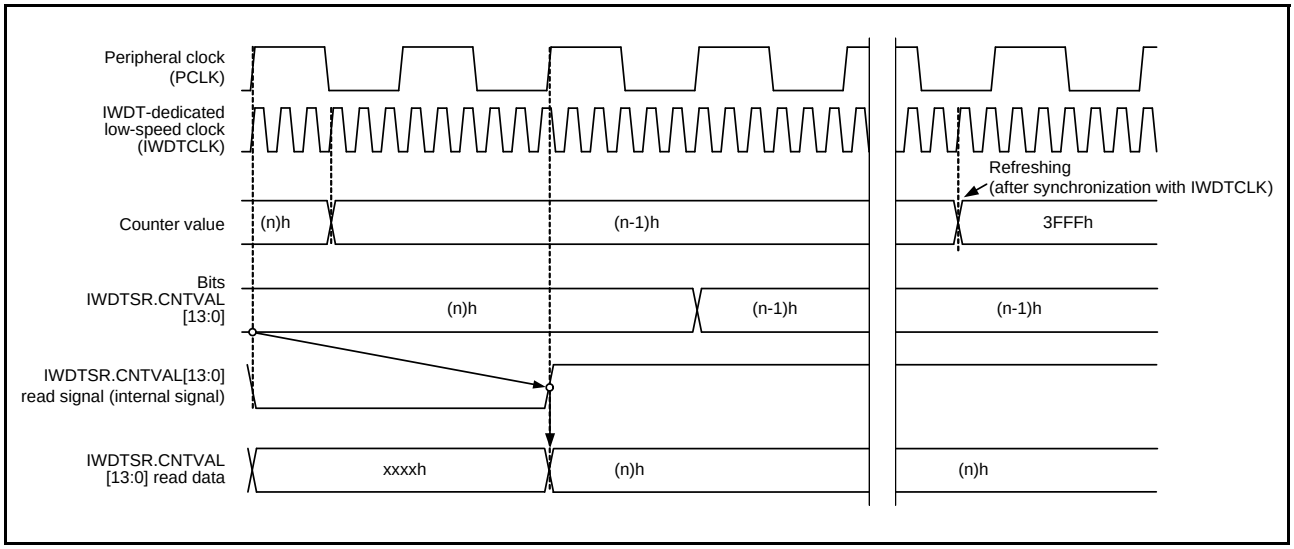


Figure 27.9 Processing for Reading IWDT Down-Counter Value (IWDTCR.CKS[3:0] = 0010b, IWDTCR.TOPS[1:0] = 11b)

27.3.8 Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers

Table 27.5 lists the correspondence between the option function select register 0 (OFS0) and the IWDT registers (IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR)) regarding control of the down-counter, reset or interrupt request output, and count stop function. Control can be switched between the option function select register 0 (OFS0) and the IWDT registers (IWDTCR, IWDTRCR, and IWDTCSTPR) through the setting of the IWDT start mode selection (OFS0.IWDTSTRT) bit in the option function select register 0 (OFS0).

Note that the option function select register 0 (OFS0) setting should be kept unchanged during IWDT operation.

For details on the option function select register 0 (OFS0), see section 8.2.1, Option Function Select Register 0 (OFS0).

Table 27.5 Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers

Target of Control	Function	OFS0 Register (Effective in Auto-Start Mode) OFS0.IWDTSTRT = 0	IWDT Registers (Effective in Register Start Mode) OFS0.IWDTSTRT = 1
Down-counter	Time-out period selection	OFS0.IWDTTOPS[1:0]	IWDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.IWDTCKS[3:0]	IWDTCR.CKS[3:0]
	Window start position selection	OFS0.IWDTRPSS[1:0]	IWDTCR.RPSS[1:0]
	Window end position selection	OFS0.IWDTRPES[1:0]	IWDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output selection	OFS0.IWDTRSTIRQS	IWDTRCR.RSTIRQS
Count stop	Sleep-mode count stop selection	OFS0.IWDTSLCSTP	IWDTCSTPR.SLCSTP

27.4 Usage Notes

27.4.1 Refresh Operations

When making the settings to control the timing of refreshing, consider variations in the range of errors due to the accuracy of the PCLK and IWDTCLK and set values which ensure that refreshing is possible.

28. USB 2.0 Host/Function Module (USBa)

28.1 Overview

This MCU Group incorporates a USB2.0 host/function module (USB0) for one USB port.
The USB module is a USB controller that is equipped to operate as a host controller or function controller. As host controller or function controller, the module supports full-speed transfer as defined in revision 2.0 of the Universal Serial Bus Specification. The module has an internal USB transceiver and supports all of the transfer types defined in the USB specification.
The USB has buffer memory for data transfer, providing a maximum of ten pipes. Any endpoint numbers can be assigned to PIPE1 to PIPE9, based on the peripheral devices or user system for communication.
Table 28.1 shows the specifications of the USB.

Table 28.1 Specifications of USB

Item	Specifications
Features	• USB Device Controller (UDC) and transceiver for USB2.0 are incorporated. • One port is provided. USB0 operates as a host controller or function controller, or in the OTG roles. • Software can switch between the host controller and function controller (can be switched by software). • Self-power mode or bus-power mode can be selected. • OTG (On-The-Go) is supported.
	When host controller operation is selected: • Full-speed transfer (12 Mbps) is supported*1 • Communications with multiple peripheral devices connected via a single HUB • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers
	When function controller operation is selected: • Full-speed transfer (12 Mbps) is supported*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF recovery function
Communication data transfer type	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Internal bus interface	• Connected to internal peripheral bus 3
Pipe configuration	• Buffer memory for USB communications is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.
	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC) Buffer size: 8, 16, 32, or 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer Buffer size: 8, 16, 32, or 64 bytes for bulk transfer or 1 to 256 bytes for isochronous transfer (double buffer can be specified) • PIPE3 to PIPE5: Bulk transfer only Buffer size: 8, 16, 32, or 64 bytes (double buffer can be specified) • PIPE6 to PIPE9: Interrupt transfer only Buffer size: 1to 64 bytes (single buffer)
Others	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)
Power consumption reducing function	Module stop state can be set.

Note 1. Note 1. Low-speed transfer (1.5 Mbps) is not supported.

Figure 28.1 shows a block diagram of the USB.

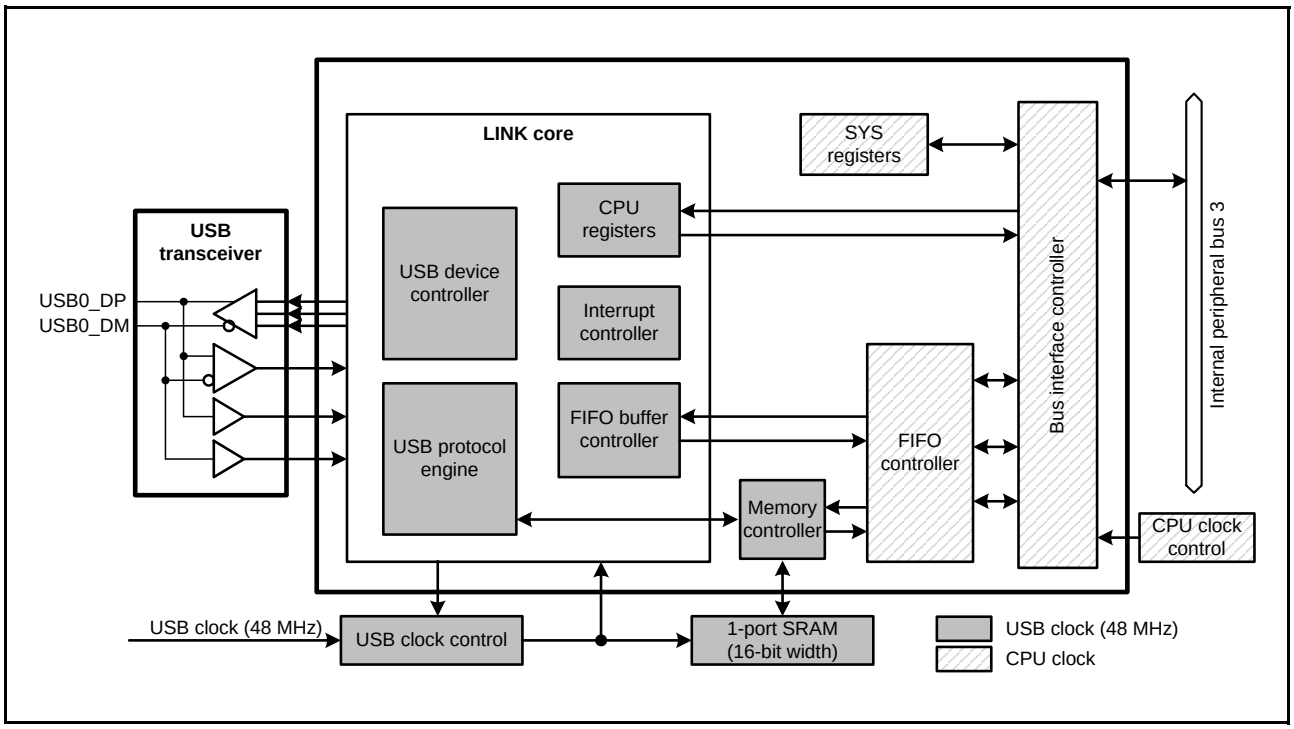


Figure 28.1 Block Diagram of USB

Table 28.2 shows the input/output pins of the USB.

Table 28.2 USB Pin Configuration

Port	Pin Name	I/O	Function
USB0	USB0_DP	I/O	D+ I/O pin of the port 0 USB on-chip transceiver This pin should be connected to the D+ pin of the USB bus.
	USB0_DM	I/O	D– I/O pin of the port 0 USB on-chip transceiver This pin should be connected to the D– pin of the USB bus.
	USB0_VBUS	Input	Port 0 USB cable connection monitor pin This pin should be connected to VBUS of the USB bus. Whether VBUS is connected or disconnected can be detected during operation as a function controller.
	USB0_EXICEN	Output	Low-power control signal for port 0 external power supply (OTG) chip
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for port 0 external power supply chip
	USB0_OVRCURA USB0_OVRCURB	Input	Port 0 external overcurrent detection signals should be connected to these pins. VBUS comparator signals should be connected to these pins when the OTG power supply chip is connected.
	USB0_ID	Input	Mini-AB connector ID input signal should be connected to this pin when port 0 operates in OTG mode.
	USB0_DPUPE	Output	1.5-kΩ pull-up resistor control signal for USB D+ signal when port 0 operates as a function controller
	USB0_DPRPD USB0_DRPD	Output	15-kΩ pull-down resistor control signal for USB D+ and USB D– signals when port 0 operates as a host controller
Common	VCC_USB	Input	USB power supply pin
	VSS_USB	Input	USB ground pin

28.2 Register Descriptions

28.2.1 System Configuration Control Register (SYSCFG)

Address(es): USB0.SYSCFG 000A 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKE	—	—	—	DCFM	DRPD	DPRPU	—	—	—	USBE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	USBE	USB Operation Enable	0: USB operation is disabled. 1: USB operation is enabled.	R/W
b3 to b1	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b4	DPRPU	D+ Line Resistor Control	0: Pulling up the line is disabled. 1: Pulling up the line is enabled.	R/W
b5	DRPD	D+/D- Line Resistor Control	0: Pulling down the lines is disabled. 1: Pulling down the lines is enabled.	R/W
b6	DCFM	Controller Function Select	0: Function controller function is selected. 1: Host controller function is selected.	R/W
b9 to b7	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b10	SCKE	USB Clock Enable	0: Stops supplying the clock signal to the USB. 1: Enables supplying the clock signal to the USB.	R/W
b15 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

USBE Bit (USB Operation Enable)

The USBE bit enables or disables operation of the USB.

Modifying the USBE bit from 1 to 0 initializes some register bits as listed in Table 28.3.

This bit should be modified while the SCKE bit is 1.

When the host controller function is selected, this bit should be set to 1 after setting the DRPD bit to 1, eliminating SYSSTS0.LNST[1:0] bits chattering, and checking that the USB bus state has been settled.

Table 28.3 Registers Initialized by Writing SYSCFG.USBE = 0

Selected Function	Register	Bit	Remarks
Function controller function	SYSSTS0	LNST[1:0]	The value is retained when the host controller function is selected.
	DVSTCTR0	RHST[2:0]	
	INTSTS0	DVSQ[2:0]	The value is retained when the host controller function is selected.
	USBADDR	USBADDR[6:0]	The value is retained when the host controller function is selected.
	USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]	The value is retained when the host controller function is selected.
	USBVAL	WVALUE[15:0]	The value is retained when the host controller function is selected.
	USBINDX	WINDEX[15:0]	The value is retained when the host controller function is selected.
	USBLENG	WLENGTH[15:0]	The value is retained when the host controller function is selected.
Host controller function	DVSTCTR0	RHST[2:0]	
	FRMNUM	FRNM[10:0]	The value is retained when the function controller function is selected.

DPRPU Bit (D+ Line Resistor Control)

The DPRPU bit enables or disables pulling up the D+ line when the function controller function is selected.
Setting the DPRPU bit to 1 when the function controller function is selected allows the USB to assert the USBm_DPUPE pin, thus notifying the USB host of connection. Modifying the DPRPU bit from 1 to 0 allows the USB to negate the USBm_DPUPE pin, thus notifying the USB host of disconnection.
This bit should be set to 1 if the function controller function is selected, and should be set to 0 if the host controller function is selected.

DRPD Bit (D+/D- Line Resistor Control)

The DRPD bit enables or disables pulling down D+ and D- lines by the USB0_DPRPD and USB0_DRPD pins when the host controller function is selected.
This bit should be set to 1 if the host controller function is selected, and should be set to 0 if the function controller function is selected.

DCFM Bit (Controller Function Select)

The DCFM bit selects the function of the USB.
This bit should be modified while both the DPRPU and DRPD bits are 0.

SCKE Bit (USB Clock Enable)

The SCKE bit stops or enables supplying 48-MHz clock signals to the USB.
When this bit is 0, only SYSCFG can be read from and written to; the other registers in the USB cannot be read from or written to.

28.2.2 System Configuration Status Register 0 (SYSSTS0)

Address(es): USB0.SYSSTS0 000A 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	—	—	—	IDMON	LNST[1:0]	
Value after reset:	0*1	0*1	0	0	0	0	0	0	0	0	0	0	0	0*1	0	0

Note 1. Depends on the USB0_OVRCURA/USB0_OVRCURB and USB0_ID pin status.

Bit	Symbol	Bit Name	Description	R/W
b1, b0	LNST[1:0]	USB Data Line Status Monitor	b1 b0 0 0: SE0 0 1: J-State 1 0: K-State 1 1: SE1	R
b2	IDMON	USB0_ID Input Pin Monitor	Indicates the status of the USB0_ID pin.	R
b5 to b3	—	Reserved	These bits are always read as 0 and cannot be modified.	R
b6	HTACT	USB Host Sequencer Status Monitor	0: Host sequencer of the USB0 is completely stopped. 1: Host sequencer of the USB0 is not completely stopped.	R
b13 to b7	—	Reserved	These bits are always read as 0 and cannot be modified.	R
b15, b14	OVCMON[1:0]	External USB0_OVRCURA/ USB0_OVRCURB Input Pin Monitor	The OVCMON[1] bit indicates the status of the USB0_OVRCURA pin. The OVCMON[0] bit indicates the status of the USB0_OVRCURB pin.	R

LNST[1:0] Bits (USB Data Line Status Monitor)

The LNST[1:0] bits indicate the state of the USB data lines (D+ and D- lines).

The LNST[1:0] bits should be read after the connection processing (the SYSCFG.DPRPU bit = 1 is set) when the function controller function is selected; whereas after enabling pull-down of the lines (the SYSCFG.DRPD bit = 1 is set) when the host controller function is selected.

HTACT Bit (USB Host Sequencer Status Monitor)

The HTACT bit is 0 when the host sequencer of the USB0 is completely stopped.

Make sure the HTACT bit is 0 when stopping the clock supply to the USB0.

OVCMON[1:0] Bits (External USB0_OVRCURA/USB0_OVRCURB Input Pin Monitor)

The OVCMON[1:0] bits indicate the status of overcurrent from an external power-supply chip.

28.2.3 Device State Control Register 0 (DVSTCTR0)

Address(es): USB0.DVSTCTR0 000A 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	RHST[2:0]	USB Bus Reset Status	• When the host controller function is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection*1 0 1 0: Full-speed connection x: Don't care • When the function controller function is selected b2 b0 0 0 0: Communication speed not determined 0 1 0: USB bus reset in progress or full-speed connection	R
b3	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b4	UACT	USB Bus Enable	0: Downstream port is disabled (SOF transmission is disabled). 1: Downstream port is enabled (SOF transmission is enabled).	R/W
b5	RESUME	Resume Output	0: Resume signal is not output. 1: Resume signal is output.	R/W
b6	USBRST	USB Bus Reset Output	0: USB bus reset signal is not output. 1: USB bus reset signal is output.	R/W
b7	RWUPE	Wakeup Detection Enable	0: Downstream port wakeup is disabled. 1: Downstream port wakeup is enabled.	R/W
b8	WKUP	Wakeup Output	0: Remote wakeup signal is not output. 1: Remote wakeup signal is output.	R/W
b9	VBUSEN	USB0_VBUSEN Output Pin Control	The VBUSEN bit value is output as the status of the external USB0_VBUSEN pin without change.	R/W
b10	EXICEN	USB0_EXICEN Output Pin Control	The EXICEN bit value is output as the status of the external USB0_EXICEN pin without change.	R/W
b11	HNPBTOA	Host Negotiation Protocol (HNP) Control	This bit is used when switching from device B to device A while in OTG mode. If the HNPBTOA bit is 1, the internal function control keeps the suspended state until the HNP processing ends even though SYSCFG.DPRPU = 0 or SYSCFG.DCFM = 1 is set.	R/W
b15-b12	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. The USB controller does not support communications with a low-speed device. When this value is read, abnormal connection processing should be executed in a higher application.

RHST[2:0] Bits (USB Bus Reset Status)

The RHST[2:0] bits indicate the status of the USB bus reset.
When the host controller function is selected, the RHST[2:0] bits indicate 100b after software has written 1 to the USBRST bit.
The USB fixes the value of the RHST[2:0] bits when software writes 0 to the USBRST bit and the USB completes SE0 driving.
When the function controller function is selected, a DVST interrupt is generated as soon as the USB detects the USB bus reset and then the RHST[2:0] bits are fixed to 010b.

UACT Bit (USB Bus Enable)

The UACT bit enables operation of the USB0 bus (controls the SOF packet transmission to the USB bus) when the host controller function is selected.
With this bit set to 1, the USB0 puts the USB0 port to the USB-bus enabled state and performs SOF output and data transmission and reception.
This module starts outputting SOF packets within one frame after software has written 1 to the UACT bit.
With this bit set to 0, the USB0 enters the idle state after outputting SOF packets.
The USB0 sets the UACT bit to 0 on any of the following conditions.

- A DTCH interrupt is detected during communication (while UACT = 1).
- An EOFERR interrupt is detected during communication (while UACT = 1).

Writing 1 to this bit should be done at the end of the USB reset processing (writing 0 to the USBRST bit) or at the end of the resume processing from the suspended state (writing 0 to the RESUME bit).
This bit should be set to 0 if the function controller function is selected.

RESUME Bit (Resume Output)

The RESUME bit controls the resume signal output when the host controller function is selected.
Setting the RESUME bit to 1 allows the USB0 to drive the port to the K-state and output the resume signal. When a remote wakeup signal is detected while the RWUPE bit is 1 in the suspended state, the USB0 sets the RESUME bit to 1 and performs the same operation.
The USB0 continues outputting K-state while the RESUME bit = 1 (until software sets the RESUME bit to 0). The RESUME bit should be 1 (= resume period) for the time defined by the USB Specifications 2.0.
This bit should be set to 1 in the suspended state.
Write 1 to the UACT bit simultaneously with the end of the resume processing (writing 0 to the RESUME bit).
This bit should be set to 0 if the function controller function is selected.

USBRST Bit (USB Bus Reset Output)

The USBRST bit controls the USB bus reset signal output when the host controller function is selected.
When the host controller function is selected, setting this bit to 1 allows the USB0 to drive SE0 of the USB port to reset the USB bus.
The USB0 continues outputting SE0 while USBRST = 1 (until software sets the USBRST bit to 0). The USBRST bit should be 1 (= USB bus reset period) for the time defined by the USB Specifications 2.0.
Writing 1 to this bit during communication (the UACT bit = 1) or during the resume processing (the RESUME bit = 1) prevents the USB0 from starting the USB bus reset processing until both the UACT and RESUME bits become 0.
Write 1 to the UACT bit simultaneously with the end of the USB bus reset processing (writing 0 to the USBRST bit).
This bit should be set to 0 if the function controller function is selected.

RWUPE Bit (Wakeup Detection Enable)

The RWUPE bit enables or disables the downstream port peripheral device to use the remote wakeup function (resume signal output) when the host controller function is selected.
With this bit set to 1, on detecting the remote wakeup signal, the USB detects the resume signal (K-state for 2.5 ms) from the downstream port device and performs the resume processing (drives the port to the K-state).
With this bit set to 0, the USB0 ignores the detected remote wakeup signal (K-state) from the peripheral device connected to the USB port.
While the RWUPE bit is 1, the internal clock should not be stopped even in the suspended state (the SYSCFG.SCKE bit should be set to 1).
This bit should be set to 0 if the function controller function is selected.

WKUP Bit (Wakeup Output)

The WKUP bit enables or disables outputting the remote wakeup signal (resume signal) to the USB bus when the function controller function is selected.
The USB controls the output time of a remote wakeup signal. When this bit is set to 1, the USB clears this bit to 0 after outputting the 10-ms K-state.
According to the USB Specifications, the USB bus idle state must be kept for 5 ms or longer before a remote wakeup signal is sent. If the USB writes 1 to this bit right after detection of the suspended state, the K-state will be output after 2 ms.
Do not write 1 to this bit, unless the device state is in the suspended state (bits INTSTS0.DVSQ[2:0] = 1xxb) and the USB host enables the remote wakeup signal. When this bit is set to 1, the internal clock must not be stopped even in the suspended state (write 1 to this bit while the SYSCFG.SCKE bit = 1).
This bit should be set to 0 if the host controller function is selected.

HNPBTOA Bit (Host Negotiation Protocol (HNP) Control)

The HNPBTOA bit is used when switching from device B to device A while in OTG mode. If the HNPBTOA bit is 1, the internal function control keeps the suspended state until the HNP processing ends even though the SYSCFG.DPRPU bit = 0 or SYSCFG.DCFM = 1 is set. Even if the falling edge of the D+ signal is detected at this time, no resume (RESM) interrupt is generated.
After this bit is set to 1, write 0 to this bit at FW to terminate the HNP processing when connection to the host (pull-up on the target side) or timeout of the HNP processing is detected.

28.2.4 CFIFO Port Register (CFIFO)
D0FIFO Port Register (D0FIFO)
D1FIFO Port Register (D1FIFO)

(1) When the MBW bit is 1

Address(es): USB0.CFIFO 000A 0014h, USB0.D0FIFO 000A 0018h, USB0.D1FIFO 000A 001Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	—	FIFO Port	This port is used for reading receive data from the FIFO buffer and writing transmit data to the FIFO buffer.	R/W

(2) When the MBW bit is 0

Address(es): USB0.CFIFO 000A 0014h, USB0.D0FIFO 000A 0018h, USB0.D1FIFO 000A 001Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	L[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	L[7:0]	FIFO Port	This port is used for reading receive data from the FIFO buffer and writing transmit data to the FIFO buffer.	R/W

FIFO Port Bits

Accessing the FIFO port bits allows reading the received data from the FIFO buffer or writing the transmit data to the FIFO buffer.

Each FIFO port register can be accessed only while the FRDY bit in each FIFO port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is 1.

The valid bits in a FIFO port register depend on the settings of the corresponding MBW bit of the FIFO port select register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL).

When the MBW bit is 1 (16-bit width), the data arrangement may differ from the data arrangement on the RAM depending on the state of the MDE pin and the setting of the BIGEND bit (CFIFOSEL.BIGEND, D0FIFOSEL.BIGEND, or D1FIFOSEL.BIGEND). Table 28.4 lists the endian operation in 16-bit access. Note that if the total number of transmit data bytes is odd, access the L[7:0] bits in bytes when writing the last data.

When the MBW bit is 0 (8-bit width), access the L[7:0] bits in bytes.

Table 28.4 Endian Operation in 16-Bit Access

MDMONR.MDE flag	CFIFOSEL.BIGEND Bit D0FIFOSEL.BIGEND Bit D1FIFOSEL.BIGEND Bit	Bit15 to 8	Bit7 to 0	Remarks
0 (little endian)	0 (little endian)	Data in address N+1	Data in address N	
	1 (big endian)	Data in address N	Data in address N+1	Bytes reversed
1 (big endian)	0 (little endian)	Data in address N+1	Data in address N	Bytes reversed
	11 (big endian)	Data in address N	Data in address N+1	

28.2.5 CFIFO Port Select Register (CFIFOSEL) D0FIFO Port Select Register (D0FIFOSEL) D1FIFO Port Select Register (D1FIFOSEL)

- CFIFOSEL

Address(es): USB0.CFIFOSEL 000A 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CURPIPE [3:0]	CFIFO Port Access Pipe Specification	b3 b0 0 0 0 0: DCP (Default control pipe) 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9 Other than above: Setting prohibited	R/W
b4	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b5	ISEL	CFIFO Port Access Direction When DCP is Selected	0: Reading from the buffer memory is selected 1: Writing to the buffer memory is selected	R/W
b7, b6	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8	BIGEND	CFIFO Port Endian Control	0: Little endian 1: Big endian	R/W
b9	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b10	MBW	CFIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width	R/W
b13 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b14	REW	Buffer Pointer Rewind	0: The buffer pointer is not rewound. 1: The buffer pointer is rewound.	R/W*1
b15	RCNT	Read Count Mode	0: The DTLN[8:0] bits are cleared when all of the receive data has been read from the CFIFO. (In double buffer mode, the DTLN bit Value is cleared when all the data has been read from only a single plane.) 1: The DTLN[8:0] bits are decremented each time the receive data is read from the CFIFO.	R/W

Note 1. Only 0 can be read.

The same pipe should not be specified by the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are cleared to 0000b, no pipe is selected.

The pipe number should not be changed while the DMA/DTC transfer is enabled.

CURPIPE[3:0] Bits (CFIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number using which data is read or written through the CFIFO port.
After writing to these bits, read these bits to check that the written value agrees with the read value before proceeding to the next process.
Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.
Even if an attempt is made to modify the setting of these bits during access to the FIFO buffer, the current access setting is retained until the access is completed. Then, the modification becomes effective, thus enabling continuous access.

ISEL Bit (CFIFO Port Access Direction When DCP is Selected)

After writing to the ISEL bit with the DCP being a selected pipe, read this bit to check that the written value agrees with the read value before proceeding to the next process.
Set this bit and the CURPIPE bits simultaneously.

MBW Bit (CFIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the CFIFO port.
When the selected pipe is in the receiving direction, once reading data is started after setting this bit, this bit should not be modified until all the data has been read.
When the selected pipe is in the receiving direction, set the CURPIPE[3:0] bits and MBW bits simultaneously.
When the selected pipe is in the transmitting direction, the bit width cannot be changed from 8-bit width to 16-bit width while data is being written to the buffer memory.
An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

REW Bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.
When the selected pipe is in the receiving direction, setting the REW bit to 1 while the FIFO buffer is being read allows re-reading the FIFO buffer from the first data (in double buffer mode, re-reading the currently-read FIFO buffer plane from the first data is allowed).
Do not set the REW bit to 1 simultaneously with modifying the CURPIPE[3:0] bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.
To re-write to the FIFO buffer again from the first data for the pipe in the transmitting direction, use the BCLR bit.

- D0FIFOSEL, D1FIFOSEL

Address(es): USB0.D0FIFOSEL 000A 0028h, USB0.D1FIFOSEL 000A 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	—	MBW	—	BIGEND	—	—	—	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CURPIPE[3:0]	CFIFO Port Access Pipe Specification	b3 b0 0 0 0 0: DCP (Default control pipe) 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9 Other than above: Setting prohibited	R/W
b7 to b4	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8	BIGEND	CFIFO Port Endian Control	0: Little endian 1: Big endian	R/W
b9	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b10	MBW	CFIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width	R/W
b11	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b12	DREQE	DMA/DTC Transfer Request Enable	0: DMA/DTC transfer request is disabled. 1: DMA/DTC transfer request is enabled.	R/W
b13	DCLRM	Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read	0: Auto buffer clear mode is disabled. 1: Auto buffer clear mode is enabled.	R/W
b14	REW	Buffer Pointer Rewind	0: The buffer pointer is not rewound. 1: The buffer pointer is rewound.	R/W*1
b15	RCNT	Read Count Mode	0: The DTLN[8:0] bits are cleared when all of the receive data has been read from the DnFIFO. (In double buffer mode, the DTLN bit Value is cleared when all the data has been read from only a single plane.) 1: The DTLN[8:0] bits are decremented each time the receive data is read from the DnFIFO.(n = 0, 1)	R/W

Note 1. Only 0 can be read.

The same pipe should not be specified by the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are cleared to 0000b, no pipe is selected.

The pipe number should not be changed while the DMA/DTC transfer is enabled.

CURPIPE[3:0] Bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number using which data is read or written through the D0FIFO port or D1FIFO port.
After writing to these bits, read these bits to check that the written value agrees with the read value before proceeding to the next process.
Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.
Even if an attempt is made to modify the setting of these bits during access to the FIFO buffer, the current access setting is retained until the access is completed. Then, the modification becomes effective, thus enabling continuous access.

MBW Bit (FIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the D0FIFO port or D1FIFO port.
When the selected pipe is in the receiving direction, once reading data is started after setting this bit, this bit should not be modified until all the data has been read.
When the selected pipe is in the receiving direction, set the CURPIPE[3:0] bits and MBW bits simultaneously.
When the selected pipe is in the transmitting direction, the bit width cannot be changed from 8-bit width to 16-bit width while data is being written to the buffer memory.
An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

DREQE Bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables the DMA/DTC transfer request to be issued.
Before setting the DREQE bit to 1 to enable the DMA/DTC transfer request to be issued, set the CURPIPE[3:0] bits.
When modifying the setting of the CURPIPE[3:0] bits, set this bit to 0 first.

DCLRM Bit (Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read)

The DCLRM bit enables or disables the buffer memory to be cleared automatically after data has been read out using the selected pipe.
With this bit set to 1, the USB sets the BCLR bit to 1 for the FIFO buffer of the selected pipe on receiving a zero-length packet while the FIFO buffer assigned to the selected pipe is empty, or on receiving a short packet and reading the data while the PIPECFG.BFRE bit is 1.
When using the USB with the SOFCFG.BRDYM bit set to 1, set this bit to 0.

REW Bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.
When the selected pipe is in the receiving direction, setting the REW bit to 1 while the FIFO buffer is being read allows re-reading the FIFO buffer from the first data (in double buffer mode, re-reading the currently-read FIFO buffer plane from the first data is allowed).
Do not set the REW bit to 1 simultaneously with modifying the CURPIPE[3:0] bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.
To re-write to the FIFO buffer again from the first data for the pipe in the transmitting direction, use the BCLR bit.

RCNT Bit (Read Count Mode)

The RCNT bit specifies the read mode for the value in the CFIFOCTR.DTLN bitDnFIFOSEL.DTLN (n = 0, 1) bit.
When accessing DnFIFO with the PIPECFG.BFRE bit set to 1, set the RCNT bit to 0.

28.2.6 CFIFO Port Control Register (CFIFOCTR)
D0FIFO Port Control Register (D0FIFOCTR)
D1FIFO Port Control Register (D1FIFOCTR)

Address(es): USB0.CFIFOCTR 000A 0022h, USB0.D0FIFOCTR 000A 002Ah, USB0.D1FIFOCTR 000A 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	DTLN[8:0]	Receive Data Length	Indicates the length of the receive data. These bits indicate different values depending on the setting of the RCNT bit in the port select register. For details, refer to the description on the DTLN[8:0] bits shown below.	R
b12 to b9	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b13	FRDY	FIFO Port Ready	0: FIFO port access is disabled. 1: FIFO port access is enabled.	R
b14	BCLR	CPU Buffer Clear	0: Invalid 1: Clears the buffer memory on the CPU side.	R/W *1
b15	BVAL	Buffer Memory Valid Flag	0: Invalid 1: Writing ended	R/W

Note 1. This bit is read as 0.

CFIFOCTR, D0FIFOCTR, and D1FIFOCTR are used for the corresponding FIFO ports.

DTLN[8:0] Bits (Receive Data Length)

The DTLN[8:0] bits indicate the length of the receive data.

While the FIFO buffer is being read, the DTLN[8:0] bits indicate different values depending on the DnFIFOSEL.RCNT (n = 0, 1)CFIFOSEL.RCNT or DnFIFOSEL.RCNT (n = 0, 1) bit value as described below.

- RCNT = 0

  The USB sets the DTLN[8:0] bits to indicate the length of the receive data until the CPU (DMACDTC or DMAC) has read all the received data from a single FIFO buffer plane all the received data from a single FIFO buffer plane has been read by the CPU or DMA/DTC transfer.

  While the PIPECFG.BFRE bit = 1, these bits retain the length of the receive data until the BCLR bit is set to 1 even after all the data has been read.

- RCNT = 1

  The USB decrements the value indicated by the DTLN[8:0] bits each time data is read from the FIFO buffer. (The value is decremented by one when the MBW bit is 0, and by two when the MBW bit is 1.)

  The USB sets these bits to 0 when all the data has been read from one FIFO buffer plane. However, in double buffer mode, if data has been received in one FIFO buffer plane before all the data has been read from the other plane, the USB sets these bits to indicate the length of the receive data in the former plane when all the data has been read from the latter plane.

FRDY Bit (FIFO Port Ready)

The FRDY bit indicates whether the FIFO port can be accessed by the CPU or by the DMA/DTC transfer.
In the following cases, the USB sets the FRDY bit to 1 but data cannot be read via the FIFO port because there is no data to be read. In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty.
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit = 1.

BCLR Bit (CPU Buffer Clear)

The BCLR bit should be set to 1 to clear the FIFO buffer on the CPU side for the selected pipe.
When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USB clears only one plane of the FIFO buffer even when both planes are read-enabled.
When the selected pipe is the DCP, setting the BCLR bit to 1 allows the USB to clear the FIFO buffer regardless of whether the FIFO buffer is on the CPU side or SIE side. To clear the buffer on the SIE side, set the DCPCTR.PID[1:0] bits for the DCP to NAK before setting the BCLR bit to 1.
When the selected pipe is in the transmitting direction, if 1 is written to the BVAL flag and the BCLR bit simultaneously, the USB clears the data that has been written before it, enabling transmission of a zero-length packet.
When the selected pipe is not the DCP, writing 1 to the BCLR bit should be done while the FRDY bit in the FIFO port control register is 1 (set by the USB).

BVAL Flag (Buffer Memory Valid Flag)

The BVAL flag should be set to 1 when data has been completely written to the FIFO buffer on the CPU side for the pipe selected using the CURPIPE[3:0] bits (selected pipe).
When the selected pipe is in the transmitting direction, set the BVAL flag to 1 in the following cases. Then, the USB switches the FIFO buffer from the CPU side to the SIE side, thus enabling transmission.

- To transmit a short packet, set the BVAL flag to 1 after data has been written.
- To transmit a zero-length packet, set the BVAL flag to 1 before data is written to the FIFO buffer.

When data of the maximum packet size has been written for the pipe in continuous transfer mode, the USB sets the BVAL flag to 1 and switches the FIFO buffer from the CPU side to the SIE side, thus enabling transmission.
Writing 1 to the BVAL flag should be done while the FRDY bit is 1 (set by the USB).
When the selected pipe is in the receiving direction, do not set the BVAL flag to 1.

28.2.7 Interrupt Enable Register 0 (INTENB0)

Address(es): USB0.INTENB0 000A 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8	BRDYE	Buffer Ready Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b9	NRDYE	Buffer Not Ready Response Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b10	BEMPE	Buffer Empty Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b11	CTRE	Control Transfer Stage Transition Interrupt Enable*1	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b12	DVSE	Device State Transition Interrupt Enable*1	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b13	SOFE	Frame Number Update Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b14	RSME	Resume Interrupt Enable*1	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b15	VBSE	VBUS Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W

Note 1. The RSME, DVSE, and CTRE bits can be set to 1 only when the function controller function is selected; do not set these bits to 1 to enable the corresponding interrupt output when the host controller function is selected.

On detecting the interrupt corresponding to the bit in INTENB0 to which software has set 1, the USB generates the USB interrupt.

The USB sets 1 to each status bit in INTSTS0 when a detection condition of the corresponding interrupt source has been satisfied regardless of the setting in INTENB0 (regardless of whether the interrupt output is enabled or disabled).

While the status bit in INTSTS0 corresponding to the interrupt source indicates 1, the USB generates the USB interrupt when software modifies the corresponding interrupt enable bit in INTENB0 from 0 to 1.

28.2.8 Interrupt Enable Register 1 (INTENB1)

Address(es): USB0.INTENB1 000A 0032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b4	SACKE	Setup Transaction Normal Response Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	SIGNE	Setup Transaction Error Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	EOFERRE	EOF Error Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b10 to b7	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b11	ATTCHE	Connection Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b12	DTCHE	Disconnection Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b13	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b14	BCHGE	USB Bus Change Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b15	OVRCRE	Overcurrent Input Change Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W

Note: • The bits in INTENB1 can be set to 1 only when the host controller function is selected; do not set these bits to 1 to enable the corresponding interrupt output when the function controller function is selected.

INTENB1 specifies the interrupt masks when the host controller function is selected, and for the setup transaction.
On detecting the interrupt corresponding to the bit in INTENB1 to which software has set 1, the USB0 generates the USB interrupt.
The USB0 sets 1 to each status bit in INTSTS1 when a detection condition of the corresponding interrupt source has been satisfied regardless of the setting in INTENB1 (regardless of whether the interrupt output is enabled or disabled).
While the status bit in INTSTS1 corresponding to the interrupt source indicates 1, the USB0 generates the USB interrupt when software modifies the corresponding interrupt enable bit in INTENB1 from 0 to 1.
When the function controller function is selected, the interrupts should not be enabled.

28.2.9 BRDY Interrupt Enable Register (BRDYENB)

Address(es): USB0.BRDYENB 000A 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDYE	PIPE8BRDYE	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	PIPE3BRDYE	PIPE2BRDYE	PIPE1BRDYE	PIPE0BRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PIPE0BRDYE	BRDY Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b1	PIPE1BRDYE	BRDY Interrupt Enable for PIPE1	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b2	PIPE2BRDYE	BRDY Interrupt Enable for PIPE2	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b3	PIPE3BRDYE	BRDY Interrupt Enable for PIPE3	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b4	PIPE4BRDYE	BRDY Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	PIPE5BRDYE	BRDY Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	PIPE6BRDYE	BRDY Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b7	PIPE7BRDYE	BRDY Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b8	PIPE8BRDYE	BRDY Interrupt Enable for PIPE8	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b9	PIPE9BRDYE	BRDY Interrupt Enable for PIPE9	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

BRDYENB enables or disables the INTSTS0.BRDY bit to be set to 1 when the BRDY interrupt is detected for each pipe.

On detecting the BRDY interrupt for the pipe corresponding to the bit in BRDYENB to which software has set 1, the USB sets 1 to the corresponding PIPEnBRDY bit (n = 0 to 9) and the INTSTS0.BRDY bit, and generates the BRDY interrupt.

While at least one PIPEnBRDY bit indicates 1, the USB generates the BRDY interrupt when software modifies the corresponding interrupt enable bit in BRDYENB from 0 to 1.

28.2.10 NRDY Interrupt Enable Register (NRDYENB)

Address(es): USB0.NRDYENB 000A 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDYE	PIPE8NRDYE	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	PIPE3NRDYE	PIPE2NRDYE	PIPE1NRDYE	PIPE0NRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PIPE0NRDYE	NRDY Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b1	PIPE1NRDYE	NRDY Interrupt Enable for PIPE1	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b2	PIPE2NRDYE	NRDY Interrupt Enable for PIPE2	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b3	PIPE3NRDYE	NRDY Interrupt Enable for PIPE3	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b4	PIPE4NRDYE	NRDY Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	PIPE5NRDYE	NRDY Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	PIPE6NRDYE	NRDY Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b7	PIPE7NRDYE	NRDY Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b8	PIPE8NRDYE	NRDY Interrupt Enable for PIPE8	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b9	PIPE9NRDYE	NRDY Interrupt Enable for PIPE9	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

NRDYENB enables or disables the INTSTS0.NRDY bit to be set to 1 when the NRDY interrupt is detected for each pipe.

On detecting the NRDY interrupt for the pipe corresponding to the bit in NRDYENB to which software has set 1, the USB sets 1 to the corresponding PIPEnNRDY bit (n = 0 to 9) and the INTSTS0.NRDY bit, and generates the NRDY interrupt.

While at least one PIPEnNRDY bit indicates 1, the USB generates the NRDY interrupt when software modifies the corresponding interrupt enable bit in NRDYENB from 0 to 1.

28.2.11 BEMP Interrupt Enable Register (BEMPENB)

Address(es): USB0.BEMPENB 000A 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMPE	PIPE8BEMPE	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	PIPE3BEMPE	PIPE2BEMPE	PIPE1BEMPE	PIPE0BEMPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PIPE0BEMPE	BEMP Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b1	PIPE1BEMPE	BEMP Interrupt Enable for PIPE1	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b2	PIPE2BEMPE	BEMP Interrupt Enable for PIPE2	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b3	PIPE3BEMPE	BEMP Interrupt Enable for PIPE3	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b4	PIPE4BEMPE	BEMP Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	PIPE5BEMPE	BEMP Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	PIPE6BEMPE	BEMP Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b7	PIPE7BEMPE	BEMP Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b8	PIPE8BEMPE	BEMP Interrupt Enable for PIPE8	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b9	PIPE9BEMPE	BEMP Interrupt Enable for PIPE9	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

BEMPENB enables or disables the INTSTS0.BEMP bit to be set to 1 when the BEMP interrupt is detected for each pipe. On detecting the BEMP interrupt for the pipe corresponding to the bit in BEMPENB to which software has set 1, the USB sets 1 to the corresponding PIPEnBEMP bit (n = 0 to 9) and the INTSTS0.BEMP bit, and generates the BEMP interrupt.

While at least one PIPEnBEMP bit in BEMPSTS indicates 1, the USB generates the BEMP interrupt when software modifies the corresponding interrupt enable bit in BEMPENB from 0 to 1.

28.2.12 SOF Output Configuration Register (SOFCFG)

Address(es): USB0.SOFCFG 000A 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	BRDYM	—	EDGESTS	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b4	EDGESTS *1	Edge Interrupt Output Status Monitor	Indicates 1 when the edge interrupt output signal is in the middle of the edge processing.	R
b5	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b6	BRDYM	BRDY Interrupt Status Clear Timing	0: Software clears the status. 1: The USB clears the status when data has been read from the FIFO buffer or data has been written to the FIFO buffer.	R/W
b7	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b8	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b15 to b9	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. Make sure this bit is 0 before stopping the USB module clocks.

EDGESTS Bit (Edge Interrupt Output Status Monitor)

The EDGESTS bit indicates 1 when the edge interrupt output signal is in the middle of the edge processing. Make sure the EDGESTS bit is 0 when stopping the clock supply to the USB.

BRDYM Bit (BRDY Interrupt Status Clear Timing)

The BRDYM bit specifies the timing for clearing the BRDY interrupt status for each pipe.

28.2.13 Interrupt Status Register 0 (INTSTS0)

Address(es): USB0.INTSTS0 000A 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after reset:	0	0	0	0/1 *1	0	0	0	0	0 *2	0 *3	0 *3	0/1 *3	0	0	0	0

Note 1. The value is 0 after the MCU is reset, and the value is 1 after a USB bus reset.
Note 2. The value is 1 when the USBm_VBUS pin is high, and the value is 0 when the USBm_VBUS pin is low.
Note 3. The value is 000b after the MCU is reset, and the value is 001b after a USB bus reset.

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	CTSQ[2:0]	Control Transfer Stage	b2 b0 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error 1 1 1: Setting prohibited	R
b3	VALID	USB Request Reception	0: Not detected 1: Setup packet reception	R/W *1
b6 to b4	DVSQ[2:0]	Device State	b6 b4 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state 1 x x: Suspended state x: Don't care	R
b7	VBSTS	VBUS Input Status	0: USBm_VBUS pin is low. 1: USBm_VBUS pin is high.	R
b8	BRDY	Buffer Ready Interrupt Status	0: BRDY interrupts are not generated. 1: BRDY interrupts are generated.	R
b9	NRDY	Buffer Not Ready Interrupt Status	0: NRDY interrupts are not generated. 1: NRDY interrupts are generated.	R
b10	BEMP	Buffer Empty Interrupt Status	0: BEMP interrupts are not generated. 1: BEMP interrupts are generated.	R
b11	CTRT	Control Transfer Stage Transition Interrupt Status*2	0: Control transfer stage transition interrupts are not generated. 1: Control transfer stage transition interrupts are generated.	R/W *1
b12	DVST	Device State Transition Interrupt Status*2	0: Device state transition interrupts are not generated. 1: Device state transition interrupts are generated.	R/W *1
b13	SOFR	Frame Number Refresh Interrupt Status	0: SOF interrupts are not generated. 1: SOF interrupts are generated. (1) When the host controller function is selected The USB sets the SOFR bit to 1 on updating the frame number when software has set the UACT bit to 1. (A SOFR interrupt is detected every 1 ms.) (2) When the function controller function is selected The USB sets the SOFR bit to 1 on updating the frame number. (A SOFR interrupt is detected every 1 ms.) The USB can detect an SOFR interrupt through the internal recovery function even when a damaged SOF packet is received from the USB host.	R/W *1
b14	RESM	Resume Interrupt Status*2,*3	0: Resume interrupts are not generated. 1: Resume interrupts are generated.	R/W *1
b15	VBINT	VBUS Interrupt Status*3	0: VBUS interrupts are not generated. 1: VBUS interrupts are generated.	R/W *1

Note 1. To clear the VBINT, RESM, SOFR, DVST, CTRT, or VALID bit, write 0 only to the bits to be cleared; write 1 to the other bits. Do not write 0 to the status bits indicating 0.
Note 2. A change in the status of the RESM, DVST, and CTRT bits occur only when the function controller function is selected; disable the corresponding interrupt enable bits (set to 0) when the host controller function is selected.
Note 3. A change in the status indicated by the VBINT and RESM bits can be detected even while the clock supply is stopped (the SCKE bit = 0), and the interrupts are output when the corresponding interrupt enable bits are enabled. Clearing the status through software should be done after enabling the clock supply.

CTSQ[2:0] Bits (Control Transfer Stage)

When the host controller function is selected, the read value is invalid.

VALID Bit (USB Request Reception)

When the host controller function is selected, the read value is invalid.

DVSQ[2:0] Bits (Device State)

The DVSQ[2:0] bits are initialized by a USB bus reset.
When the host controller function is selected, the read value is invalid.

BRDY Bit (Buffer Ready Interrupt Status)

Indicates the BRDY interrupt status.
The USB sets the BRDY bit to 1 when at least one PIPEnBRDY bit (n=0 to 9) is set to 1 among the PIPEnBRDY bits corresponding to the PIPEnBRDYE bits (n=0 to 9) to which 1 has been set (when the USB detects the BRDY interrupt status in at least one pipe among the pipes for which software enables the BRDY interrupt output).
For the conditions for PIPEnBRDY status assertion, refer to section 28.3.3.1, BRDY Interrupt.
The USB clears the BRDY bit to 0 when software writes 0 to all the PIPEnBRDY bits corresponding to the PIPEnBRDYE bits to which 1 has been set.
The BRDY bit cannot be cleared to 0 even if software writes 0 to this bit.

NRDY Bit (Buffer Not Ready Interrupt Status)

The USB sets the NRDY bit to 1 when at least one PIPEnNRDY bit (n=0 to 9) is set to 1 among the PIPEnNRDY bits corresponding to the PIPEnNRDYE bits (n=0 to 9) to which 1 has been set (when the USB detects the NRDY interrupt status in at least one pipe among the pipes for which software enables the NRDY interrupt output).
For the conditions for PIPEnNRDY status assertion, refer to section 28.3.3.2, NRDY Interrupt.
The USB clears the NRDY bit to 0 when software writes 0 to all the PIPEnNRDY bits corresponding to the PIPEnNRDYE bits to which 1 has been set.
The NRDY bit cannot be cleared to 0 even if software writes 0 to this bit.

BEMP Bit (Buffer Empty Interrupt Status)

The USB sets the BEMP bit to 1 when at least one PIPEnBEMP bit (n=0 to 9) is set to 1 among the PIPEnBEMP bits corresponding to the PIPEnBEMPE bits (n=0 to 9) to which 1 has been set (when the USB detects the BEMP interrupt status in at least one pipe among the pipes for which software enables the BEMP interrupt output).
For the conditions for PIPEnBEMP status assertion, refer to section 28.3.3.3, BEMP Interrupt.
The USB clears the BEMP bit to 0 when software writes 0 to all the PIPEnBEMP bits corresponding to the PIPEnBEMPE bits to which 1 has been set.
The BEMP bit cannot be cleared to 0 even if software writes 0 to this bit.

CTRT Bit (Control Transfer Stage Transition Interrupt Status)

When the function controller function is selected, the USB updates the value of the CTSQ[2:0] bits and sets the CTRT bit to 1 on detecting a change in the control transfer stage.
When a control transfer stage transition interrupt is generated, clear the status before the USB detects the next control transfer stage transition.
When the host controller function is selected, the read value is invalid.

DVST Bit (Device State Transition Interrupt Status)

When the function controller function is selected, the USB updates the DVSQ [2:0] value and sets the DVST bit to 1 on detecting a change in the device state.
When a device state transition interrupt is generated, clear the status before the USB detects the next device state transition.
When the host controller function is selected, the read value is invalid.

SOFR Bit (Frame Number Refresh Interrupt Status)

(1) When the host controller function is selected
The USB sets the SOFR bit to 1 on updating the frame number when software has set the UACT bit in DVSTCTR0 to 1. (A frame number refresh interrupt is detected every 1 ms.)
(2) When the function controller function is selected
The USB sets the SOFR bit to 1 on updating the frame number. (A frame number refresh interrupt is detected every 1 ms.)
The USB can detect an SOFR interrupt through the internal recovery function even when a damaged SOF packet is received from the USB host.

RESM Bit (Resume Interrupt Status)

When the function controller function is selected, the USB sets the RESM bit to 1 on detecting the falling edge of the signal on the USBm_DP pin in the suspended state (DVSQ [2:0] = 1xxb).
When the host controller function is selected, the read value is invalid.

VBINT Bit (VBUS Interrupt Status)

The USB sets the VBINT bit to 1 on detecting a level change (high to low or low to high) in the USBm_VBUS pin input value. The USB sets the VBSTS bit to indicate the USBm_VBUS pin input value. When the VBUS interrupt is generated, use software to repeat reading the VBSTS bit until the same value is read three or more times, and eliminate chattering.

28.2.14 Interrupt Status Register 1 (INTSTS1)

Address(es): USB0.INTSTS1 000A 0042h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b4	SACK	Setup Transaction Normal Response Interrupt Status	0: SACK interrupts are not generated. 1: SACK interrupts are generated.	R/W *1
b5	SIGN	Setup Transaction Error Interrupt Status	0: SIGN interrupts are not generated. 1: SIGN interrupts are generated.	R/W *1
b6	EOFERR	EOF Error Detection Interrupt Status	0: EOFERR interrupts are not generated. 1: EOFERR interrupts are generated.	R/W *1
b10 to b7	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b11	ATTCH	ATTCH Interrupt Status	0: ATTCH interrupts are not generated. 1: ATTCH interrupts are generated.	R/W *1
b12	DTCH	USB Disconnection Detection Interrupt Status	0: DTCH interrupts are not generated. 1: DTCH interrupts are generated.	R/W *1
b13	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b14	BCHG	USB Bus Change Interrupt Status*2	0: BCHG interrupts are not generated. 1: BCHG interrupts are generated.	R/W *1
b15	OVRCR	Overcurrent Input Change Interrupt Status*2	0: OVRCR interrupts are not generated. 1: OVRCR interrupts are generated.	R/W *1

Note 1. To clear the status indicated by the bits in INTSTS1, write 0 only to the bits to be cleared; write 1 to the other bits.
Note 2. A change in the status indicated by the OVRCR or BCHG bit can be detected even while the clock supply is stopped (while the SYSCFG.SCKE bit = 0), and the interrupt is output when the corresponding interrupt enable bit is enabled. Clearing the status through software should be done after enabling the clock supply.
No interrupts other than those indicated by the BCHG and OVRCR bits can be detected while the clock supply is stopped (while the SYSCFG.SCKE bit = 0).

INTSTS1 is used to confirm the status of each interrupt when the host controller function is selected.
The various status change interrupts indicated by the bits in INTSTS1 should be enabled only when the host controller function is selected.

SACK Bit (Setup Transaction Normal Response Interrupt Status)

Indicates the status of the setup transaction normal response interrupt when the host controller function is selected.
The USB0 detects the SACK interrupt when ACK response is returned from the peripheral device during the setup transactions issued by the USB0, and sets the SACK bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB0 generates the SACK interrupt.
When the function controller function is selected, the read value is invalid.

SIGN Bit (Setup Transaction Error Interrupt Status)

Indicates the status of the setup transaction error interrupt when the host controller function is selected.
The USB0 detects the SIGN interrupt when ACK response is not returned from the peripheral device three consecutive times during the setup transactions issued by this module, and sets the SIGN bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB0 generates the SIGN interrupt.
Specifically, the USB0 detects the SIGN interrupt when any of the following response conditions occur for three consecutive setup transactions.

- Timeout is detected by the USB0 when the peripheral device has returned no response.
- A damaged ACK packet is received.
- A handshake other than ACK (NAK, NYET, or STALL) is received.

When the function controller function is selected, the read value is invalid.

EOFERR Bit (EOF Error Detection Interrupt Status)

Indicates the status of the EOFERR interrupt when the host controller function is selected.
The USB0 detects the EOFERR interrupt on detecting that communication is not completed at the EOF2 timing prescribed by the USB Specifications 2.0, and sets the EOFERR bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB0 generates the EOFERR interrupt.
After detecting the EOFERR interrupt, the USB0 controls hardware as described below (irrespective of the setting of the corresponding interrupt enable bit). Software should terminate all the pipes in which communications are currently carried for the USB port and perform re-enumeration of the USB port.

- Modifies the DVSTCTR0.UACT bit for the port in which an EOFERR interrupt has been detected to 0.
- Puts the port in which an EOFERR interrupt has been generated into the idle state.

When the function controller function is selected, the read value is invalid.

ATTCH Bit (ATTCH Interrupt Status)

Indicates the status of the ATTCH interrupt when the host controller function is selected.
The USB0 detects the ATTCH interrupt on detecting J-state or K-state of the full-speed signal level for 2.5 µs, and sets the ATTCH bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB0 generates the interrupt.
Specifically, the USB0 detects the ATTCH interrupt on any of the following conditions.

- K-state, SE0, or SE1 changes to J-state, and J-state continues for 2.5 µs.
- J-state, SE0, or SE1 changes to K-state, and K-state continues for 2.5 µs.

When the function controller function is selected, the read value is invalid.

DTCH Bit (USB Disconnection Detection Interrupt Status)

Indicates the status of the USB disconnection detection interrupt when the host controller function is selected.
The USB0 detects the DTCH interrupt on detecting USB bus disconnection, and sets the DTCH bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB0 generates the interrupt.
The USB0 detects bus disconnection based on the USB Specifications 2.0.
After detecting the DTCH interrupt, the USB0 controls hardware as described below (irrespective of the setting of the corresponding interrupt enable bit). Software should terminate all the pipes in which communications are currently carried out for the USB port and make a transition to the wait state for bus connection to the USB port (wait state for ATTCH interrupt generation).

- Modifies the DVSTCTR0.UACT bit for the port in which a DTCH interrupt has been detected to 0.
- Puts the port in which a DTCH interrupt has been generated into the idle state.

When the function controller function is selected, the read value is invalid.

BCHG Bit (USB Bus Change Interrupt Status)

Indicates the status of the USB bus change interrupt.
The USB0 detects the BCHG interrupt when a change in the full-speed signal level occurs on the USB port (a change from J-state, K-state, or SE0 to J-state, K-state, or SE0), and sets the BCHG bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB generates the interrupt.
The USB0 sets the LNST[1:0] bits to indicate the current input state of the USB port. When the BCHG interrupt is generated, use software to repeat reading the LNST[1:0] bits until the same value is read three or more times, and eliminate chattering.
A change in the USB bus state can be detected even while the internal clock supply is stopped.
When the function controller function is selected, the read value is invalid.

OVRCR Bit (Overcurrent Input Change Interrupt Status)

Indicates the status of the USB0_OVRCURA and USB0_OVRCURB input pin change interrupt.
The USB0 detects the OVRCR interrupt when a change (high to low or low to high) occurs in at least one of the input values to the USB0_OVRCURA and USB0_OVRCURB pins, and sets the OVRCR bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB0 generates the interrupt.

28.2.15 BRDY Interrupt Status Register (BRDYSTS)

Address(es): USB0.BRDYSTS 000A 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDY	PIPE8BRDY	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	PIPE3BRDY	PIPE2BRDY	PIPE1BRDY	PIPE0BRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PIPE0BRDY	BRDY Interrupt Status for PIPE0*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b1	PIPE1BRDY	BRDY Interrupt Status for PIPE1*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b2	PIPE2BRDY	BRDY Interrupt Status for PIPE2*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b3	PIPE3BRDY	BRDY Interrupt Status for PIPE3*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b4	PIPE4BRDY	BRDY Interrupt Status for PIPE4*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b5	PIPE5BRDY	BRDY Interrupt Status for PIPE5*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b6	PIPE6BRDY	BRDY Interrupt Status for PIPE6*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b7	PIPE7BRDY	BRDY Interrupt Status for PIPE7*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b8	PIPE8BRDY	BRDY Interrupt Status for PIPE8*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b9	PIPE9BRDY	BRDY Interrupt Status for PIPE9*2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. When the SOFCFG.BRDYM bit is set to 0, to clear the status indicated by the bits in BRDYSTS, write 0 only to the bits to be cleared; write 1 to the other bits.

Note 2. When the SOFCFG.BRDYM bit is set to 0, clearing BRDY Interrupts should be done before accessing the FIFO.

28.2.16 NRDY Interrupt Status Register (NRDYSTS)

Address(es): USB0.NRDYSTS 000A 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDY	PIPE8NRDY	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	PIPE3NRDY	PIPE2NRDY	PIPE1NRDY	PIPE0NRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PIPE0NRDY	NRDY Interrupt Status for PIPE0	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b1	PIPE1NRDY	NRDY Interrupt Status for PIPE1	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b2	PIPE2NRDY	NRDY Interrupt Status for PIPE2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b3	PIPE3NRDY	NRDY Interrupt Status for PIPE3	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b4	PIPE4NRDY	NRDY Interrupt Status for PIPE4	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b5	PIPE5NRDY	NRDY Interrupt Status for PIPE5	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b6	PIPE6NRDY	NRDY Interrupt Status for PIPE6	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b7	PIPE7NRDY	NRDY Interrupt Status for PIPE7	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b8	PIPE8NRDY	NRDY Interrupt Status for PIPE8	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b9	PIPE9NRDY	NRDY Interrupt Status for PIPE9	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. To clear the status indicated by the bits in NRDYSTS, write 0 only to the bits to be cleared; write 1 to the other bits.

28.2.17 BEMP Interrupt Status Register (BEMPSTS)

Address(es): USB0.BEMPSTS 000A 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMP	PIPE8BEMP	PIPE7BEMP	PIPE6BEMP	PIPE5BEMP	PIPE4BEMP	PIPE3BEMP	PIPE2BEMP	PIPE1BEMP	PIPE0BEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PIPE0BEMP	BEMP Interrupt Status for PIPE0	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b1	PIPE1BEMP	BEMP Interrupt Status for PIPE1	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b2	PIPE2BEMP	BEMP Interrupt Status for PIPE2	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b3	PIPE3BEMP	BEMP Interrupt Status for PIPE3	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b4	PIPE4BEMP	BEMP Interrupt Status for PIPE4	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b5	PIPE5BEMP	BEMP Interrupt Status for PIPE5	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b6	PIPE6BEMP	BEMP Interrupt Status for PIPE6	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b7	PIPE7BEMP	BEMP Interrupt Status for PIPE7	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b8	PIPE8BEMP	BEMP Interrupt Status for PIPE8	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b9	PIPE9BEMP	BEMP Interrupt Status for PIPE9	0: Interrupts are not generated. 1: Interrupts are generated.	R/W *1
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. To clear the status indicated by the bits in BEMPSTS, write 0 only to the bits to be cleared; write 1 to the other bits.

28.2.18 Frame Number Register (FRMNUM)

Address(es): USB0.FRMNUM 000A 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b10 to b0	FRNM[10:0]	Frame Number	Frame number	R
b13 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b14	CRCE	Receive Data Error	0: No error 1: An error occurred	R/W *1
b15	OVRN	Overrun/Underrun Detection Status	0: No error 1: An error occurred	R/W *1

Note 1. When setting each status to 0, write 0 to the bit that is cleared, and write 1 to the other bit.

FRNM[10:0] Bits (Frame Number)

These bits indicate the latest frame number for the USB after the issuing of an SOF packet every 1 ms or writing to the FRNM[10:0] bits at the SOF packet reception.
When reading these bits, read them twice and ensure that the values match.

CRCE Bit (Receive Data Error)

Indicates whether a CRC error or bit stuffing error has been detected in the pipe during isochronous transfer.
Software can clear the CRCE bit to 0 by writing 0 to the CRCE bit. Here, 1 should be written to the other bits in FRMNUM.
The USB generates an internal NRDY interrupt request when a CRC error is detected.

OVRN Bit (Overrun/Underrun Detection Status)

Indicates whether an overrun/underrun error has been detected in the pipe during isochronous transfer.
Software can clear the OVRN bit to 0 by writing 0 to the OVRN bit. Here, 1 should be written to the other bits in FRMNUM.
(1) When the host controller function is selected
The USB sets the OVRN bit to 1 on any of the following conditions.

- For the isochronous transfer pipe in the transmitting direction, the time to issue an OUT token comes before all the transmit data has been written to the FIFO buffer.
- For the isochronous transfer pipe in the receiving direction, the time to issue an IN token comes when no FIFO buffer planes are empty.

(2) When the function controller function is selected
The USB sets the OVRN bit to 1 on any of the following conditions.

- For the isochronous transfer pipe in the transmitting direction, the IN token is received before all the transmit data has been written to the FIFO buffer.
- For the isochronous transfer pipe in the receiving direction, the OUT token is received when no FIFO buffer planes are empty.

28.2.19 Device State Change Register (DVCHGR)

Address(es): USB0.DVCHGR 000A 004Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b14 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15	DVCHG	Device State Change	0: Disables the writing to the USBADDR.STSRECOV[3:0] bits and USBADDR.USBADDR[6:0]. 1: Enables the writing to the USBADDR.STSRECOV[3:0] bits and USBADDR.USBADDR[6:0].	R/W

28.2.20 USB Address Register (USBADDR)

Address(es): USB0.USBADDR 000A 0050h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	STSRECOV[3:0]				—	USBADDR[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	USBADDR[6:0]	USB Address	When the function controller function is selected, these bits indicate the USB address assigned by the host when the SET_ADDRESS request is successfully processed.	R/W
b7	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b11 to b8	STSRECOV[3:0]	Status Recovery	• Recovery when the function controller function is selected b11 b8 1 0 0 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 001b (Default state) 1 0 1 0: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 010b (Address state) 1 0 1 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 011b (Configured state) Other than above: Setting prohibited • Recovery when the host controller function is selected b11 b8 1 0 0 0: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b) Other than above: Setting prohibited	R/W
b15 to b12	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

USBADDR[6:0] Bits (USB Address)

On detecting the USB bus reset, the USB sets the USBADDR[6:0] bits to 00h.

The writing to these bits is enabled while the DVCHGR.DVCHG bits are set to 1. On returning from the USB power shut-off, the operation can resume to the USB address before the shut-off by the software.

When the host controller function is selected, the USBADDR[6:0] bits are invalid.

STSRECOV[3:0] Bits (Status Recovery)

These bits are used to resume the state of the internal sequencer on returning from the USB power shut-off.

The writing to the STSRECOV[3:0] bits is enabled while the DVCHGR.DVCHG bit is set to 1.

28.2.21 USB Request Type Register (USBREQ)

Address(es): USB0.USBREQ 000A 0054h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	Request Type	These bits store the USB request bmRequestType value.	R/W *1
b15 tob8	BREQUEST[7:0]	Request	These bits store the USB request bRequest value.	R/W *1

Note 1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

USBREQ stores setup requests for control transfers.
When the function controller function is selected, the values of bRequest and bmRequestType that have been received are stored. When the host controller function is selected, the values of bRequest and bmRequestType to be transmitted are set.
USBREQ is initialized by a USB bus reset.

BMREQUESTTYPE[7:0] Bits (Request Type)

These bits hold the value of the bmRequestType field of a USB request.

- When host controller operation is selected:
  Set these bits to the value of the USB request data in setup transactions for transmission. Do not overwrite the value of the BMREQUESTTYPE[7:0] bits while the DCPCTR.SUREQ bit = 1.
- When function controller operation is selected:
  These bits indicate the value of the USB request data in setup transactions for reception. Writing to the bits has no effect.

BREQUEST[7:0] Bits (Request)

These bits store bRequest value of the USB request.

- When host controller operation is selected:
  Set these bits to the value of the USB request data in setup transactions for transmission. Do not overwrite the value of the BREQUEST[7:0] bits while the DCPCTR.SUREQ bit = 1.
- When function controller operation is selected:
  These bits indicate the value of the USB request data in setup transactions for reception. Writing to the bits has no effect.

28.2.22 USB Request Value Register (USBVAL)

Address(es): USB0.USBVAL 000A 0056h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WVALUE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	WVALUE[15:0]	Value	These bits store the USB request wValue value.	R/W *1

Note 1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

When the function controller function is selected, the value of wValue that has been received is stored in USBVAL.
When the host controller function is selected, the value of wValue to be transmitted is set.
USBVAL is initialized by a USB bus reset.

WVALUE[15:0] Bits (Value)

These bits store wRequest value of the USB request.

- When host controller operation is selected:
  Set these bits to the value of the wValue field in USB requests of setup transactions for transmission. Do not overwrite the value of the WVALUE[15:0] bits while the DCPCTR.SUREQ bit = 1.
- When function controller operation is selected:
  These bits indicate the value of the wValue field in USB requests received in setup transactions for reception. Writing to the WVALUE[15:0] bits has no effect.

28.2.23 USB Request Index Register (USBINDX)

Address(es): USB0.USBINDX 000A 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	WINDEX[15:0]	Index	These bits store the USB request wIndex value.	R/W *1

Note 1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

USBINDX stores setup requests for control transfers.
When the function controller function is selected, the value of wIndex that has been received is stored. When the host controller function is selected, the value of wIndex to be transmitted is set.
USBINDX is initialized by a USB bus reset.

WINDEX[15:0] Bits (Index)

These bits hold the value of the wIndex field of a USB request.

- When host controller operation is selected:
  Set these bits to the value of the wIndex field in USB requests of setup transactions for transmission. Do not overwrite the value of the WINDEX[15:0] bits while the DCPCTR.SUREQ bit = 1.
- When function controller operation is selected:
  These bits indicate the value of the wIndex field in USB requests received in setup transactions for reception. Writing to the WINDEX[15:0] bits has no effect.

28.2.24 USB Request Length Register (USBLENG)

Address(es): USB0.USBLENG 000A 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENGTH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	WLENGTH[15:0]	Length	These bits store the USB request wLength value.	R/W *1

Note 1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

USBLENG stores setup requests for control transfers.
When the function controller function is selected, the value of wLength that has been received is stored. When the host controller function is selected, the value of wLength to be transmitted is set.
USBLENG is initialized by a USB bus reset.

WLENGTH[15:0] Bits (Length)

These bits hold the value of the wLength field of a USB request.

- When host controller operation is selected:
  Set these bits to the value of the wLength field in USB requests of setup transactions for transmission. Do not overwrite the value of the WLENGTH[15:0] bits while the DCPCTR.SUREQ bit = 1.
- When function controller operation is selected:
  These bits indicate the value of the wLength field in USB requests received in setup transactions for reception. Writing to the WLENGTH[15:0] bits has no effect.

28.2.25 DCP Configuration Register (DCPCFG)

Address(es): USB0.DCPCFG 000A 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SHTNAK	—	—	DIR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b4	DIR	Transfer Direction	0: Data receiving direction 1: Data transmitting direction	R/W
b6, b5	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Pipe continued at the end of transfer 1: Pipe disabled at the end of transfer	R/W
b15 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. Modify this bit while PID is NAK. Before modifying this bit after modifying the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK, check that the DCPCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

DIR Bit (Transfer Direction)

When the host controller function is selected, the DIR bit sets the transfer direction of the data stage and status stage.
When the function controller function is selected, the DIR bit should be set to 0.

SHTNAK Bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to modify PID to NAK upon the end of transfer when the selected pipe is in the receiving direction.
The SHTNAK bit is valid when the selected pipe in the receiving direction.
When the SHTNAK bit is set to 1, the USB modifies the DCPCTR.PID [1:0] bits for the DCP to NAK on determining the end of the transfer. The USB determines that the transfer has ended on the following condition.

- A short packet (including a zero-length packet) is successfully received.

28.2.26 DCP Maximum Packet Size Register (DCPMAXP)

Address(es): USB0.DCPMAXP 000A 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	MXPS[6:0]	Maximum Packet Size*1	These bits set the maximum amount of data (maximum packet size) in payloads for the DCP.	R/W
b11 to b7	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b12	DEVSEL[3:0]	Device Select*2	b15 b12 0 0 0 0: Address 0000 0 0 0 1: Address 0001 0 0 1 0: Address 0010 0 0 1 1: Address 0011 0 1 0 0: Address 0100 0 1 0 1: Address 0101 Other than above: Setting prohibited	R/W

Note 1. Modify the MXPS[6:0] bits while PID is NAK. Before modifying these bits after modifying the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK, check that the DCPCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB0, checking the PBUSY bit through software is not necessary. After modifying the MXPS[6:0] bits and the DCP has been set to the CURPIPE[3:0] bits in a port select register, clear the buffer by setting the BCLR bit the port control register to 1.

Note 2. Modify the DEVSEL[3:0] bits while PID is NAK and the DCPCTR.SUREQ bit is 0. To modify these bits after modifying the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK, check that the DCPCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

MXPS[6:0] Bits (Maximum Packet Size)

The MXPS[6:0] bits specify the maximum amount of data (maximum packet size) in payloads for the DCP. The initial value of the bits is 40h (64 bytes).

Ensure that the setting of the MXPS[6:0] bits is in compliance with the USB specification.

Do not write to the FIFO buffer or set PID = BUF while the setting of the MXPS[6:0] bits is 0.

DEVSEL[3:0] Bits (Device Select)

When the host controller function is selected, these bits specify the address of the peripheral device which is the communication target during control transfer.

The DEVSEL[3:0] bits should be set after setting the address to the DEVADDn (n = 0 to 5) register corresponding to the value to be set in the DEVSEL[3:0] bits. For example, before setting the DEVSEL[3:0] bits to 0010, the address should be set to DEVADD2.

When the function controller function is selected, the DEVSEL[3:0] bits should be set to 0000b.

28.2.27 DCP Control Register (DCPCTR)

Address(es): USB0.DCPCTR 000A 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	SUREQ	—	—	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response	R/W
b2	CCPL	Control Transfer End Enable	0: Invalid 1: Completion of control transfer is enabled.	R/W
b4, b3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b5	PBUSY	Pipe Busy	0: DCP is not used for the transaction. 1: DCP is used for the transaction.	R
b6	SQMON	Sequence Toggle Bit Monitor	0: DATA0 1: DATA1	R
b7	SQSET	Toggle Bit Set*2	0: Invalid 1: Specifies DATA1.	R/W *1
b8	SQCLR	Toggle Bit Clear*2	0: Invalid 1: Specifies DATA0.	R/W *1
b10, b9	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b11	SUREQCLR	SUREQ Bit Clear	0: Invalid 1: Clears the SUREQ bit to 0.	R/W
b13, b12	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b14	SUREQ	Setup Token Transmission	0: Invalid 1: Transmits the setup packet.	R/W
b15	BSTS	Buffer Status	0: Buffer access is disabled. 1: Buffer access is enabled.	R

Note 1. This bit is read as 0.

Note 2. Write 1 to the SQSET and SQCLR bits while PID is NAK. Before modifying these bits after modifying the PID[1:0] bits for the DCP from BUF to NAK, check that the PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

PID[1:0] Bits (Response PID)

The PID[1:0] bits control the response type of the USB during control transfer.

(1) When the host controller function is selected

Modify the setting of the PID[1:0] bits from NAK to BUF using the following procedure.

- When the transmitting direction is set
  Write all the transmit data to the FIFO buffer while the DVSTCTR0.UACT bit is 1 and PID is NAK, and then set PID to BUF. After PID has been set to BUF, the USB executes the OUT transaction.
- When the receiving direction is set
  Check that the FIFO buffer is empty (or empty the buffer) while the DVSTCTR0.UACT bit is 1 and PID is NAK, and then set PID to BUF. After PID has been set to BUF, the USB executes the IN transaction.

The USB modifies the setting of the PID[1:0] bits as follows.

- The USB sets PID to STALL (11b) on receiving the data of a size exceeding the maximum packet size when software has set the PID[1:0] bits to BUF.
- The USB sets PID to NAK on detecting a receive error, such as a CRC error, three consecutive times.
- The USB also sets PID to STALL (11b) on receiving the STALL handshake.

(2) When the function controller function is selected

The USB modifies the setting of the PID[1:0] bits as follows.

- The USB modifies the PID[1:0] bits to NAK on receiving the setup packet. Here, the USB sets the INTSTS0.VALID bit to 1. Software cannot modify the setting of the PID[1:0] bits until software sets the INTSTS0.VALID bit to 0.
- The USB sets PID to STALL (11b) on receiving the data of a size exceeding the maximum packet size when software has set the PID[1:0] bits to BUF.
- The USB sets PID to STALL (1xb) on detecting the control transfer sequence error.
- The USB sets PID to NAK on detecting the USB bus reset.

The USB does not check to the setting of the PID[1:0] bits while the SET_ADDRESS request is processed.
The PID[1:0] bits are initialized by a USB bus reset.

CCPL Bit (Control Transfer End Enable)

When the function controller function is selected, setting the CCPL bit to 1 enables the status stage of the control transfer to be completed.
When software sets the CCPL bit to 1 while the corresponding PID[1:0] bits are set to BUF, the USB completes the control transfer stage.
During control read transfer, the USB transmits the ACK handshake in response to the OUT transaction from the USB host, and transmits the zero-length packet in response to the IN transaction from the USB host during control write or no-data control transfer. However, on detecting the SET_ADDRESS request, the USB operates in auto response mode from the setup stage up to the status stage completion irrespective of the setting of the CCPL bit.
The USB modifies the CCPL bit from 1 to 0 on receiving a new setup packet.
Software cannot write 1 to the CCPL bit while the INTSTS0.VALID bit is 1.
The PID[1:0] bits are initialized by a USB bus reset.
The CCPL bit is initialized by a USB bus reset.
When the host controller function is selected, be sure to write 0 to the CCPL bit.

PBUSY Bit (Pipe Busy)

The PBUSY bit indicates whether DCP is used or not for the transaction when USB changes the PID[1:0] bits from BUF to NAK.

The USB modifies the PBUSY bit from 0 to 1 upon start of the USB transaction for the relevant pipe, and modifies the PBUSY bit from 1 to 0 upon completion of one transaction.

Reading the PBUSY bit after software has set PID to NAK allows checking whether modification of the pipe settings is possible.

For details, refer to section 28.3.4.1, Pipe Control Register Switching Procedures.

SQMON Bit (Sequence Toggle Bit Monitor)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during the DCP transfer.

The USB allows the SQMON bit to toggle upon normal completion of the transaction. However, the SQMON bit is not allowed to toggle when a DATA-PID disagreement occurs during the transfer in the receiving direction.

When the function controller function is selected, the USB sets the SQMON bit to 1 (specifies DATA1 as the expected value) upon successful reception of the setup packet.

When the function controller function is selected, the USB does not reference the SQMON bit during the IN/OUT transaction of the status stage, and does not allow the SQMON bit to toggle upon normal completion.

SQSET Bit (Toggle Bit Set)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR Bit (Toggle Bit Clear)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer. The SQCLR bit indicates 0

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SUREQCLR Bit (SUREQ Bit Clear)

When the host controller function is selected, setting the SUREQCLR bit to 1 clears the SUREQ bit to 0. The SUREQCLR bit always indicates 0.

Set the SUREQCLR bit to 1 through software when communication has stopped with the SUREQ bit being 1 during the setup transaction. However, for normal setup transactions, the USB0 automatically clears the SUREQ bit to 0 upon completion of the transaction; therefore, clearing the SUREQ bit through software is not necessary.

Controlling the SUREQ bit through the SUREQCLR bit must be done while the DVSTCTR0.UACT bit is 0 and thus communication is halted or while no transfer is being performed with bus disconnection detected.

When the function controller function is selected, be sure to write 0 to the SUREQCLR bit.

SUREQ Bit (Setup Token Transmission)

The USB transmits the setup packet by setting the SUREQ bit to 1 when the host controller function is selected.

After completing the setup transaction process, the USB0 generates either the SACK or SIGN interrupt and clears the SUREQ bit to 0.

The USB0 also clears the SUREQ bit to 0 when software sets the SUREQCLR bit to 1.

Before setting the SUREQ bit to 1, set the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, and USBLENG appropriately to transmit the desired USB request in the setup transaction. Before setting this bit to 1, check that the PID[1:0] bits for the DCP are set to NAK. After setting the SUREQ bit to 1, do not modify the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, or USBLENG until the setup transaction is completed (the SUREQ bit = 1).

Write 1 to the SUREQ bit only when transmitting the setup token; for other purposes, write 0.

When the function controller function is selected, be sure to write 0 to the SUREQ bit.

BSTS Bit (Buffer Status)

Indicates whether DCP FIFO buffer access is enabled or disabled.

The meaning of the BSTS bit depends on the setting of ISEL bit in the port select register as shown below.

- When the ISEL bit = 0, the BSTS bit indicates whether the received data can be read from the buffer.
- When the ISEL bit = 1, the BSTS bit indicates whether the data to be transmitted can be written to the buffer.

28.2.28 Pipe Window Select Register (PIPESEL)

Address(es): USB0.PIPESEL 000A 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	PIPESEL[3:0]	Pipe Window Select	b3 b0 0 0 0 0: No pipe selected 0 0 0 1: PIPE1 0 0 1 0: PIPE2 0 0 1 1: PIPE3 0 1 0 0: PIPE4 0 1 0 1: PIPE5 0 1 1 0: PIPE6 0 1 1 1: PIPE7 1 0 0 0: PIPE8 1 0 0 1: PIPE9 Other than above: Setting prohibited	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PIPE1 to PIPE 9 should be set using PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN.
After selecting the pipe using PIPESEL, functions of the pipe should be set using PIPECFG, PIPEMAXP, and PIPEPERI. PIPEnCTR, PIPEnTRE, and PIPEnTRN can be set regardless of the pipe selection in PIPESEL.

PIPESEL[3:0] Bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number corresponding to PIPECFG, PIPEMAXP, and PIPEPERI which data are written to or read from.
Selecting a pipe number through the PIPESEL[3:0] bits allows writing to and reading from PIPECFG, PIPEMAXP, and PIPEPERI which correspond to the selected pipe number.
When PIPESEL[3:0] = 0000b, 0 is read from all of the bits in PIPECFG, PIPEMAXP, PIPEPERI, and PIPEnCTR. Writing to these bits is invalid.

28.2.29 Pipe Configuration Register (PIPECFG)

Address(es): USB0.PIPECFG 000A 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	EPNUM[3:0]	Endpoint Number*1	These bits specify the endpoint number for the selected pipe. Setting 0000 means unused pipe.	R/W
b4	DIR	Transfer Direction*2,*3	0: Receiving direction 1: Transmitting direction	R/W
b6, b5	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Pipe continued at the end of transfer 1: Pipe disabled at the end of transfer	R/W
b8	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b9	DBLB	Double Buffer Mode*2,*3	0: Single buffer 1: Double buffer	R/W
b10	BFRE	BRDY Interrupt Operation Specification*2,*3	0: BRDY interrupt upon transmitting or receiving data 1: BRDY interrupt upon completion of reading data	R/W
b13 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15, b14	TYPE[1:0]	Transfer Type*1	• PIPE1 and PIPE2 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Isochronous transfer • PIPE3 to PIPE5 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Setting prohibited • PIPE6 to PIPE9 b15 b14 0 0: Pipe not used 0 1: Setting prohibited 1 0: Interrupt transfer 1 1: Setting prohibited	R/W

Note 1. Modify the TYPE, SHTNAK, and EPNUM[3:0] bits while PID is NAK. Before modifying these bits after modifying the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID [1:0]bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

Note 2. Modify the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected by the CURPIPE[3:0] bits in the port select register. Before modifying these bits after modifying the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PIPEnCTR.PBUSY[1:0] bits through software is not necessary.

Note 3. To modify the BFRE, DBLB, and DIR bits after completing USB communication using the selected pipe, write 1 and then 0 to the PIPEnCTR.ACLRM bit continuously through software to clear the FIFO buffer assigned to the selected pipe while the PID and CURPIPE bits are in the state described in the above note 2.

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint numbers for PIPE1 to PIPE9. It also selects single or double buffer mode, and whether to continue or disable pipe operation at the end of transfer.

EPNUM[3:0] Bits (Endpoint Number)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe.
Setting 0000b means unused pipe.
Do not make the settings such that the combination of the settings of the DIR and EPNUM[3:0] bits should be the same for two or more pipes (bits EPNUM[3:0] = 0000b can be set for all of the pipes).

DIR Bit (Transfer Direction)

The DIR bit specifies the transfer direction for the selected pipe.
When software has set the DIR bit to 0, the USB uses the selected pipe in the receiving direction, and when software has set the DIR bit to 1, the USB uses the selected pipe in the transmitting direction.

SHTNAK Bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to modify PID to NAK upon the end of transfer when the selected pipe is in the receiving direction.
The SHTNAK bit is valid when the selected pipe is PIPE1 to PIPE5 in the receiving direction.
When software has set the SHTNAK bit to 1 for the selected pipe in the receiving direction, the USB modifies the PIPEnCTR.PID[1:0] bits corresponding to the selected pipe to NAK on determining the end of the transfer. The USB determines that the transfer has ended on any of the following conditions.

- A short packet (including a zero-length packet) is successfully received.
- The transaction counter is used and the number of packets specified by the counter are successfully received.

DBLB Bit (Double Buffer Mode)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe.
The DBLB bit is valid when PIPE1 to PIPE5 are selected.

BFRE Bit (BRDY Interrupt Operation Specification)

Specifies the BRDY interrupt generation timing from the USB to the CPU with respect to the selected pipe.
When software has set the BFRE bit to 1 and the selected pipe is in the receiving direction, the USB detects the transfer completion and generates the BRDY interrupt on having read the relevant packet.
When the BRDY interrupt is generated with the above conditions, software needs to write 1 to the BCLR bit in the port control register. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.
When software has set the BFRE bit to 1 and the selected pipe is in the transmitting direction, the USB does not generate the BRDY interrupt.
For details, refer to section 28.3.3.1, BRDY Interrupt.

TYPE[1:0] Bits (Transfer Type)

The TYPE[1:0] bits select the transfer type for the pipe selected by the PIPESEL.PIPESEL[3:0] bits (selected pipe).
Before setting PID to BUF for the selected pipe (before starting USB communication using the selected pipe), set the TYPE[1:0] bits to a value other than 00b.

28.2.30 Pipe Maximum Packet Size Register (PIPEMAXP)

Address(es): USB0.PIPEMAXP 000A 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	MXPS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0/1	0	0	0	0	0	0

Note 1. The value of these bits is 0000h when no pipe is selected with the PIPESEL.PIPESEL[3:0] bits and 0040h when a pipe is selected.

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	MXPS[8:0]	Maximum Packet Size bit*1	• PIPE1 and PIPE2: 1 byte (001h) to 256 bytes (100h) • PIPE3 to PIPE5: 8 bytes (008h), 16 bytes (010h), 32 bytes (020h), 64 bytes (040h) (Bits [8:7] and [2:0] are not provided.) • PIPE6 to PIPE9: 1 byte (001h) to 64 bytes (040h) (Bits [8:7] are not provided.)	R/W
b11 to b9	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b12	DEVSEL[3:0]	Device Select bit*2	b3 b0 0 0 0 0: Address 0000 0 0 0 1: Address 0001 0 0 1 0: Address 0010 0 0 1 1: Address 0011 0 1 0 0: Address 0100 0 1 0 1: Address 0101 Other than above: Setting prohibited	R/W

Note 1. Modify the MXPS[8:0] bits while PID is NAK and before the pipe is selected by the CURPIPE[3:0] bits in the port select register. Before modifying these bits after modifying the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

Note 2. Modify the DEVSEL[3:0] bits while PID is NAK. To modify these bits after modifying the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB0, checking the PBUSY bit through software is not necessary.

PIPEMAXP specifies the maximum packet size for PIPE1 to PIPE9.

MXPS[8:0] Bits (Maximum Packet Size)

Specifies the maximum data payload (maximum packet size) for the selected pipe.

These bits should be set to the appropriate value for each transfer type based on the USB Specifications. Note that the maximum value for PIPE1 and PIPE2 is 256. While the MXPS[8:0] bits are 000h, do not write to the FIFO buffer or do not set the PID[1:0] bits to 01b (BUF).

DEVSEL[3:0] Bits (Device Select)

When the host controller function is selected, these bits specify the USB device address of the peripheral device which is the communication target.

The DEVSEL[3:0] bits should be set after setting the address to the DEVADDn (n = 0 to 5) register corresponding to the value to be set in the DEVSEL[3:0] bits. For example, before setting the DEVSEL[3:0] bits to 0010b, the address should be set to DEVADD2.

When the function controller function is selected, the DEVSEL[3:0] bits should be set to 0000b.

28.2.31 Pipe Cycle Control Register (PIPEPERI)

Address(es): USB0.PIPEPERI 000A 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	IITV[2:0] *1	Interval Error Detection Interval	Specifies the interval error detection timing for the selected pipe in terms of frames, which is expressed as n-th power of 2.	R/W
b11 to b3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b12	IFIS	Isochronous IN Buffer Flush	0: The buffer is not flushed. 1: The buffer is flushed.	R/W
b15 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. Modify the IITV[2:0] bits while PID is NAK. To modify these bits after modifying the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

PIPEPERI selects whether the buffer is flushed or not when an interval error occurred during isochronous IN transfer, and sets the interval error detection interval for PIPE1 to PIPE9.

IITV[2:0] Bits (Interval Error Detection Interval)

Before modifying the IITV[2:0] bits after USB communication has been completed with the IITV[2:0] bits set to a certain value, set PID to NAK and then set the PIPEnCTR.ACLRM bit to 1 to initialize the interval timer.
The IITV[2:0] bits are invalid for PIPE3 to PIPE5; set the IITV[2:0] bits to 000b for PIPE3 to PIPE5.

IFIS Bit (Isochronous IN Buffer Flush)

Specifies whether to flush the buffer when the pipe selected by the PIPE.PIPESEL[3:0] bits (selected pipe) is used for isochronous IN transfers.
When the function controller function is selected and the selected pipe is for isochronous IN transfers, the USB automatically clears the FIFO buffer when the USB fails to receive the IN token from the USB host within the interval set by the IITV[2:0] bits in terms of frames.
In double buffer mode (the PIPECFG.DBLB bit = 1), the USB only clears the data in the plane used earlier.
The USB clears the FIFO buffer on receiving the SOF packet immediately after the frame in which the USB has expected to receive the IN token. Even if the SOF packet is damaged, the USB also clears the FIFO buffer at the right timing to receive the SOF packet by using the internal recovery function.
When the host controller function is selected, set the IITV[2:0] bits to 000b.
When the selected pipe is not for isochronous transfer, set the IITV[2:0] bits to 000b.

28.2.32 PIPEn Control Registers (PIPEnCTR) (n = 1 to 9)

- PIPEnCTR (n = 1 to 5)

Address(es): USB0.PIPE1CTR 000A 0070h, USB0.PIPE2CTR 000A 0072h, USB0.PIPE3CTR 000A 0074h, USB0.PIPE4CTR 000A 0076h, USB0.PIPE5CTR 000A 0078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response	R/W
b4 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b5	PBUSY	Pipe Busy	0: The relevant pipe is not used for the transaction. 1: The relevant pipe is used for the transaction.	R
b6	SQMON	Toggle Bit Confirmation	0: DATA0 1: DATA1	R
b7	SQSET	Toggle Bit Set*2	0: Invalid 1: Specifies DATA1.	R/W *1
b8	SQCLR	Toggle Bit Clear*2	0: Invalid 1: Specifies DATA0.	R/W *1
b9	ACLRM	Auto Buffer Clear Mode*3	0: Disabled 1: Enabled (all buffers are initialized)	R/W
b10	ATREPM	Auto Response Mode*2	0: Auto response is disabled. 1: Auto response is enabled.	R/W
b13 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b14	INBUFM	Transmit Buffer Monitor	0: There is no data to be transmitted in the buffer memory. 1: There is data to be transmitted in the buffer memory.	R
b15	BSTS	Buffer Status	0: Buffer access by the CPU is disabled. 1: Buffer access by the CPU is enabled.	R

Note 1. This bit is read as 0.
Note 2. Modify the ATREPM bit or write 1 to the SQCLR or SQSET bit while PID is NAK. Before modifying these bits after modifying the PID[1:0] bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.
Note 3. Modify the ACLRM bit while PID[1:0] is NAK and before the pipe is selected by the CURPIPE[3:0] bits in the port select register. Before modifying this bit after modifying the PID[1:0] bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

PIPEnCTR can be set regardless of the pipe selection in PIPESEL.

PID[1:0] Bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction of the relevant pipe.
The default setting of the PID[1:0] bits is NAK. Modify the setting of the PID[1:0] bits to BUF to use the relevant pipe for USB transfer. Table 28.5 and Table 28.6 show the basic operation (operation when there are no errors in the transmitted and received packets) of the USB depending on the PID[1:0] bit setting.
After modifying the setting of the PID[1:0] bits through software from BUF to NAK during USB communication using the relevant pipe, check that the PBUSY bit is 1 to see if USB transfer using the relevant pipe has actually entered the NAK state. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.
The USB modifies the setting of the PID[1:0] bits in the following cases.

- The USB sets PID to NAK on recognizing the completion of the transfer when the relevant pipe is in the receiving direction and software has set the PIPECFG.SHTNAK bit for the selected pipe to 1.
- The USB sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the relevant pipe.
- The USB sets PID to NAK on detecting a USB bus reset when the function controller function is selected.
- The USB sets PID to NAK on detecting a receive error, such as a CRC error, three consecutive times when the host controller function is selected.
- The USB sets PID to STALL (11) on receiving the STALL handshake when the host controller function is selected.

To specify each response type, set the PID[1:0] bits as follows.

- To make a transition from NAK (00b) to STALL, set 10b.
- To make a transition from BUF (01b) to STALL, set 11b.
- To make a transition from STALL (11b) to NAK, set 10b and then 00b.
- To make a transition from STALL to BUF, set 00b (NAK) and then 01b (BUF).

PBUSY Bit (Pipe Busy)

The PBUSY bit indicates whether the relevant pipe is being currently used or not for the transaction.
The USB modifies the PBUSY bit from 0 to 1 upon start of the USB transaction for the relevant pipe, and modifies the PBUSY bit from 1 to 0 upon completion of one transaction.
Reading the PBUSY bit after software has set PID to NAK allows checking whether modification of the pipe settings is possible.
For details, refer to section 28.3.4.1, Pipe Control Register Switching Procedures.

SQMON Bit (Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
When the relevant pipe is not for the isochronous transfer, the USB allows the SQMON bit to toggle upon normal completion of the transaction. However, the SQMON bit is not allowed to toggle when a DATA-PID disagreement occurs during the transfer in the receiving direction.

SQSET Bit (Toggle Bit Set)

The SQSET bit should be set to 1 to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQSET bit to 1 through software allows the USB to set DATA1 as the expected value of the sequence toggle bit of the relevant pipe. The USB sets the SQSET bit to 0.

SQCLR Bit (Toggle Bit Clear)

The SQCLR bit should be set to 1 to clear the expected value (to set DATA0 as the expected value) of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQCLR bit to 1 through software allows the USB to set DATA0 as the expected value of the sequence toggle bit of the relevant pipe. The USB sets the SQCLR bit to 0.

ACLRM Bit (Auto Buffer Clear Mode)

Enables or disables auto buffer clear mode for the relevant pipe.
To delete the information in the FIFO buffer assigned to the relevant pipe completely, write 1 and then 0 to the ACLRM bit continuously.
Table 28.7 shows the information cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which clearing the information is necessary.

ATREPM Bit (Auto Response Mode)

Enables or disables auto response mode for the relevant pipe.
When the function controller function is selected and the relevant pipe is for bulk transfer, the ATREPM bit can be set to 1.
When the ATREPM bit is set to 1, the USB responds to the token from the USB host as described below.
(1) When the relevant pipe is for bulk IN transfer (the PIPECFG.TYPE[1:0] bits = 01b and the PIPECFG.DIR bit = 1)
When the ATREPM bit = 1 and PID = BUF, the USB transmits a zero-length packet in response to the IN token.
The USB updates (allows toggling of) the sequence toggle bit (DATA-PID) each time the USB receives ACK from the USB host (in a single transaction, IN token is received, zero-length packet is transmitted, and then ACK is received.).
In this case, the USB does not generate the BRDY or BEMP interrupt.
(2) When the relevant pipe is for bulk OUT transfer (the PIPECFG.TYPE[1:0] bit = 01b and the PIPECFG.DIR bit = 0)
When the ATREPM bit = 1 and PID = BUF, the USB returns NAK in response to the OUT token and generates the NRDY interrupt.
For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty. Do not write to the FIFO buffer during USB communication in auto response mode.
When the relevant pipe is for isochronous transfer, be sure to set the ATREPM bit to 0.
When the host controller function is selected, be sure to set the ATREPM bit to 0.

INBUFM Bit (Transmit Buffer Monitor)

Indicates the relevant FIFO buffer status when the relevant pipe is in the transmitting direction.
When the relevant pipe is in the transmitting direction (the PIPECFG.DIR bit = 1), the USB sets the INBUFM bit to 1 when software (or DMAC) completes writing data to at least one FIFO buffer plane when writing data to at least one FIFO buffer plane has been completed by the CPU or the DMA/DTC transfer.
The USB sets the INBUFM bit to 0 when the USB completes transmitting the data from the FIFO buffer plane to which all the data has been written. In double buffer mode (the PIPECFG.DBLB bit = 1), the USB sets the INBUFM bit to 0 when the USB completes transmitting the data from the two FIFO buffer planes before software (or DMAC) completes writing data to one FIFO buffer plane before writing data to one FIFO buffer plane has been completed by the CPU or DMA/DTC transfer.
The INBUFM bit indicates the same value as the BSTS bit when the relevant pipe is in the receiving direction (the PIPECFG.DIR bit = 0).

BSTS Bit (Buffer Status)

Indicates the FIFO buffer status for the relevant pipe.
The meaning of the BSTS bit depends on the settings of the PIPECFG.DIR bit, PIPECFG.BFRE bit, and DnFIFOSEL.DCLRM bits as shown in Table 28.8.

Table 28.5 Operation of USB depending on PID[1:0] Bits Setting (When Host Controller Function is Selected)

Bits PID[1:0]	Transfer Type	Transfer Direction (DIR Bit)	Operation of USB
00b (NAK)	Operation does not depend on the setting.	Operation does not depend on the setting.	Does not issue tokens.
01b (BUF)	Bulk or interrupt	Operation does not depend on the setting.	Issues tokens while the DVSTCTR0.UACT bit is 1 and the FIFO buffer corresponding to the relevant pipe is ready for transmission and reception. Does not issue tokens while the DVSTCTR0.UACT bit is 0 or the FIFO buffer corresponding to the relevant pipe is not ready for transmission or reception.
	Isochronous	Operation does not depend on the setting.	Issues tokens irrespective of the status of the FIFO buffer corresponding to the relevant pipe.
10b (STALL) or 11b (STALL)	Operation does not depend on the setting.	Operation does not depend on the setting.	Does not issue tokens.

Table 28.6 Operation of USB depending on PID[1:0] Bits Setting (When Function Controller Function is Selected)

Bits PID[1:0]	Transfer Type	Transfer Direction (DIR Bit)	Operation of USB
00b (NAK)	Bulk or interrupt	Operation does not depend on the setting.	Returns NAK in response to the token from the USB host. For the operation when the ATREPM bit is 1, refer to the description of the ATREPM bit.
	Isochronous	Operation does not depend on the setting.	Returns nothing in response to the token from the USB host.
01b (BUF)	Bulk	Receiving direction (the DIR bit = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer corresponding to the relevant pipe is ready for reception.
	Interrupt	Receiving direction (the DIR bit = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer corresponding to the relevant pipe is ready for reception.
	Bulk or interrupt	Transmitting direction (the DIR bit = 1)	Transmits data in response to the token from the USB host if the corresponding FIFO buffer is ready for transmission. Returns NAK if not ready.
	Isochronous	Receiving direction (the DIR bit = 0)	Receives data in response to the OUT token from the USB host if the FIFO buffer corresponding to the relevant pipe is ready for reception. Discards data if not ready.
	Isochronous	Transmitting direction (the DIR bit = 1)	Transmits data in response to the token from the USB host if the corresponding FIFO buffer is ready for transmission. Transmits the zero-length packet if not ready.
10b (STALL) or 11b (STALL)	Bulk or interrupt	Operation does not depend on the setting.	Returns STALL in response to the token from the USB host.
	Isochronous	Operation does not depend on the setting.	Returns nothing in response to the token from the USB host.

Table 28.7 Information Cleared by USB by Setting ACLRM = 1

No.	Information Cleared by ACLRM Bit Manipulation	Cases in which Clearing Information is Necessary
1	All the information in the FIFO buffer assigned to the relevant pipe (both FIFO buffer planes are cleared when double buffer mode is selected)	When the pipe is to be initialized
2	The interval count value when the relevant pipe is for isochronous transfer	When the interval count value is to be reset
3	Internal flags concerning the PIPECFG.BFRE bit	When the PIPECFG.BFRE setting is modified
4	FIFO buffer toggle control	When the PIPECFG.DBLB setting is modified
5	Internal flags concerning the transaction count	When the transaction count function is forcibly terminated

Table 28.8 Operation of BSTS Bit

DIR Bit	BFRE Bit	DCLRM Bit	BSTS Bit Function
0	0	0	The received data can be read from the FIFO buffer. The received data has been completely read from the FIFO buffer.
		1	Setting prohibited
	1	0	The received data can be read from the FIFO buffer. Software has set the BCLR bit in the port control register to 1 after the received data has been completely read from the FIFO buffer.
		1	The received data can be read from the FIFO buffer. The received data has been completely read from the FIFO buffer.
1	0	0	The transmit data can be written to the FIFO buffer. The transmit data has been completely written to the FIFO buffer.
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

- PIPEnCTR (n = 6 to 9)

Address(es): USB0.PIPE6CTR 000A 007Ah, USB0.PIPE7CTR 000A 007Ch, USB0.PIPE8CTR 000A 007Eh, USB0.PIPE9CTR 000A 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response	R/W
b4 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b5	PBUSY	Pipe Busy	0: The relevant pipe is not used at the USB bus. 1: The relevant pipe is used at the USB bus.	R
b6	SQMON	Toggle Bit Confirmation	0: DATA0 1: DATA1	R
b7	SQSET	Toggle Bit Set*2	0: Invalid 1: Specifies DATA1.	R/W *1
b8	SQCLR	Toggle Bit Clear*2	0: Invalid 1: Specifies DATA0.	R/W *1
b9	ACLRM	Auto Buffer Clear Mode*2,*3	0: Auto buffer clear mode is disabled. 1: Auto buffer clear mode is enabled (all buffers are initialized)	R/W
b14 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15	BSTS	Buffer Status	0: Buffer access is disabled. 1: Buffer access is enabled.	R

Note 1. Only 0 can be read. Only 1 can be written.
Note 2. Write 1 to the SQCLR or SQSET bit while PID is NAK. Before modifying these bits after modifying the PID[1:0] bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.
Note 3. Modify the ACLRM bit while PID is NAK and before the pipe is selected by the CURPIPE[3:0] bits in the port select register. Before modifying this bit after modifying the PID[1:0] bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

PID[1:0] Bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction of the relevant pipe.
The default setting of the PID[1:0] bits is NAK. Modify the setting of the PID[1:0] bits to BUF to use the relevant pipe for USB transfer. Table 28.5 and Table 28.6 show the basic operation (operation when there are no errors in the transmitted and received packets) of the USB depending on the setting of the PID[1:0] bits.
After modifying the setting of the PID[1:0] bits through software from BUF to NAK during USB communication using the relevant pipe, check that the PBUSY bit is 1 to see if USB transfer using the relevant pipe has actually entered the NAK state. However, if the PID bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.
The USB modifies the setting of the PID[1:0] bits in the following cases.

- The USB sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the relevant pipe.
- The USB sets PID to NAK on detecting a USB bus reset when the function controller function is selected.
- The USB sets PID to NAK on detecting a receive error, such as a CRC error, three consecutive times when the host controller function is selected.
- The USB sets PID to STALL (11b) on receiving the STALL handshake when the host controller function is selected.

To specify each response type, set the PID[1:0] bits as follows.

- To make a transition from NAK (00b) to STALL, set 10b.
- To make a transition from BUF (01b) to STALL, set 11b.
- To make a transition from STALL (11b) to NAK, set 10b and then 00b.
- To make a transition from STALL to BUF, set 00b (NAK) and then 01b (BUF).

PBUSY Bit (Pipe Busy)

The PBUSY bit indicates whether the relevant pipe is being currently used or not for the transaction.
The USB modifies the PBUSY bit from 0 to 1 upon start of the USB transaction for the relevant pipe, and modifies the PBUSY bit from 1 to 0 upon completion of one transaction.
Reading the PBUSY bit after software has set PID to NAK allows checking whether modification of the pipe settings is possible.

SQMON Bit (Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
The USB allows the SQMON bit to toggle upon normal completion of the transaction. However, the SQMON bit is not allowed to toggle when a DATA-PID disagreement occurs during the transfer in the receiving direction.

SQSET Bit (Toggle Bit Set)

The SQSET bit should be set to 1 to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQSET bit through software allows the USB to set DATA1 as the expected value of the sequence toggle bit of the relevant pipe. The USB sets the SQSET bit to 0.

SQCLR Bit (Toggle Bit Clear)

The SQCLR bit should be set to 1 to clear the expected value (to set DATA0 as the expected value) of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQCLR bit to 1 through software allows the USB to set DATA0 as the expected value of the sequence toggle bit of the relevant pipe. The USB sets the SQCLR bit to 0.

ACLRM Bit (Auto Buffer Clear Mode)

Enables or disables auto buffer clear mode for the relevant pipe.

To delete the information in the FIFO buffer assigned to the relevant pipe completely, write 1 and then 0 to the ACLRM bit continuously.

Table 28.9 shows the information cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which clearing the information is necessary.

BSTS Bit (Buffer Status)

Indicates the FIFO buffer status for the relevant pipe.

The meaning of the BSTS bit depends on the settings of the PIPECFG.DIR bit, PIPECFG.BFRE bit, and DnFIFOSEL.DCLRM bits as shown in Table 28.8.

Table 28.9 Information Cleared by USB by Setting the ACLRM Bit = 1

No.	Information Cleared by ACLRM Bit Manipulation	Cases in which Clearing Information is Necessary
1	All the information in the FIFO buffer assigned to the selected pipe	When the pipe is to be initialized
2	The interval count value when the selected pipe is for interrupt transfer and the host controller function is selected	When the interval count value is to be reset
3	Internal flags concerning the PIPECFG.BFRE bit	When the PIPECFG.BFRE setting is modified
4	Internal flags concerning the transaction count	When the transaction count function is forcibly terminated

28.2.33 PIPEn Transaction Counter Enable Registers (PIPEnTRE) (n = 1 to 5)

Address(es): USB0.PIPE1TRE 000A 0090h, USB0.PIPE2TRE 000A 0094h, USB0.PIPE3TRE 000A 0098h, USB0.PIPE4TRE 000A 009Ch, USB0.PIPE5TRE 000A 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8	TRCLR	Transaction Counter Clear	0: Invalid 1: The current counter value is cleared.	R/W
b9	TRENB	Transaction Counter Enable	0: Transaction counter is disabled. 1: Transaction counter is enabled.	R/W
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note: • Modify each bit in PIPEnTRE while PID is NAK. Before modifying these bits after modifying the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID[1:0] bits have been modified to NAK by the USB, checking the PBUSY bit through software is not necessary.

TRCLR Bit (Transaction Counter Clear)

Clears the current value of the transaction counter corresponding to the relevant pipe and then sets the TRCLR bit to 0.

TRENB Bit (Transaction Counter Enable)

Enables or disables the transaction counter.

For the pipe in the receiving direction, setting the TRENB bit to 1 after setting the total number of the packets to be received in the PIPEnTRN.TRNCNT[15:0] bits through software allows the USB to control hardware as described below on having received the number of packets equal to the setting of the TRNCNT[15:0] bits.

- While the PIPECFG.SHTNAK bit is 1, the USB modifies the PID bits to NAK for the corresponding pipe on having received the number of packets equal to the setting of the TRNCNT[15:0] bits.
- While the PIPECFG.BFRE bit is 1, the USB asserts the BRDY interrupt on having received the number of packets equal to the setting of the TRNCNT[15:0] bits and then reading out the last received data.

For the pipe in the transmitting direction, set the TRENB bit to 0.

When the transaction counter is not used, set the TRENB bit to 0.

When the transaction counter is used, set the TRNCNT[15:0] bits before setting the TRENB bit to 1. Set the TRENB bit to 1 before receiving the first packet to be counted by the transaction counter.

28.2.34 PIPEn Transaction Counter Registers (PIPEnTRN) (n = 1 to 5)

Address(es): USB0.PIPE1TRN 000A 0092h, USB0.PIPE2TRN 000A 0096h, USB0.PIPE3TRN 000A 009Ah, USB0.PIPE4TRN 000A 009Eh, USB0.PIPE5TRN 000A 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TRNCNT[15:0]	Transaction Counter	• When written to: Specifies the number of transactions to be transferred through DMA. • When read from: Indicates the specified number of transactions if the PIPEnTRE.TRENB bit is 0. Indicates the number of currently counted transactions if the PIPEnTRE.TRENB bit is 1.	R/W

PIPEnTRN retains the setting by a USB bus reset.

TRNCNT[15:0] Bits (Transaction Counter)

The USB increments the value of the TRNCNT[15:0] bits by one when all of the following conditions are satisfied on receiving the packet.

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value ≠ current counter value + 1) on receiving the packet.
- The payload of the received packet agrees with the setting of the PIPEMAXP.MXPS[8:0] bits.

The USB clears the value of the TRNCNT[15:0] bits to 0 when any of the following conditions are satisfied.

(1) All of the following conditions are satisfied.
- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value = current counter value + 1) on receiving the packet.
- The payload of the received packet agrees with the setting of the PIPEMAXP.MXPS[8:0] bits.

(2) All of the following conditions are satisfied.
- The PIPEnTRE.TRENB bit = 1
- The USB has received a short packet.

(3) All of the following conditions are satisfied.
- The PIPEnTRE.TRENB bit = 1
- Software has set the PIPEnTRE.TRCLR bit to 1.

For the pipe in the transmitting direction, set the TRNCNT[15:0] bits to 0.
When the transaction counter is not used, set the TRNCNT[15:0] bits to 0.
Setting the number of transactions to be transferred to the TRNCNT[15:0] bits is only enabled when the PIPEnTRE.TRENB bit is 0. To modify the number of transactions to be transferred, set the TRCLR bit to 1 (to clear the current counter value) before setting the PIPEnTRE.TRENB bit to 1.

28.2.35 Device Address n Configuration Registers (DEVADDn) (n = 0 to 5)

Address(es): USB0.DEVADD0 000A 00D0h, USB0.DEVADD1 000A 00D2h, USB0.DEVADD2 000A 00D4h, USB0.DEVADD3 000A 00D6h, USB0.DEVADD4 000A 00D8h, USB0.DEVADD5 000A 00DAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	USBSPD[1:0]		—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b7, b6	USBSPD[1:0]	Transfer Speed of Communication Target Device	b7 b6 0 0: DEVADDn is not used 0 1: Setting prohibited 1 0: Full speed 1 1: Setting prohibited	R/W
b15 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

DEVADDn specifies the transfer speed of the peripheral device which is the communication target for PIPE0 to PIPE9. When the host controller function is selected, the bits in DEVADDn should be set before starting communication using each pipe.

The bits in DEVADDn should be modified while no valid pipes are using the settings of the bits. Valid pipes refer to the pipes satisfying both of the following conditions:

- DEVADDn is selected by the DEVSEL[3:0] bits.
- The PID[1:0] bits are set to BUF for the selected pipe or the selected pipe is the DCP with the DCPCTR.SUREQ bit set to 1.

USBSPD[1:0] Bits (Transfer Speed of Communication Target Device)

Specifies the USB transfer speed of the communication target peripheral device.

Set these bits to 10b when a full-speed device is connected via the HUB.

When the host controller function is selected, the USB refers to the setting of the USBSPD[1:0] bits to generate packets.

When the function controller function is selected, set these bits to 00b.

28.3 Operation

28.3.1 System Control

This section describes the register settings that are necessary for initialization of this module and power consumption control.

28.3.1.1 Starting Operation

Setting the SYSCFG.USBE bit to 1 after starting the clock supply to the USB (the SYSCFG.SCKE bit = 1) enables and starts USB operation.

28.3.1.2 Controller Function Selection

For the USB0, the host controller function or function controller function can be selected using the SYSCFG.DCFM bit. Set the DCFM bit during initialization after a reset is released or while D+ pull-up and D+/D- pull-down are disabled (bits SYSCFG.DPRPU and SYSCFG.DRPD are 0).

28.3.1.3 Example of USB External Connection Circuit

Figure 28.2 shows an example of OTG connection of the USB connector (USB0) in the self-powered state.
The USB0 controls the signals for enabling a pull-up resistor for the D+ signal and pull-down resistors for the D+ and D- signals. These signals can be pulled up or down using the SYSCFG.DPRPU and SYSCFG.DRPD bits.
When the function controller function is selected and the DPRPU bit is cleared to 0 during communication with the host controller, the pull-up resistor of the USB data line is disabled, making it possible to notify the USB host of the device disconnection.

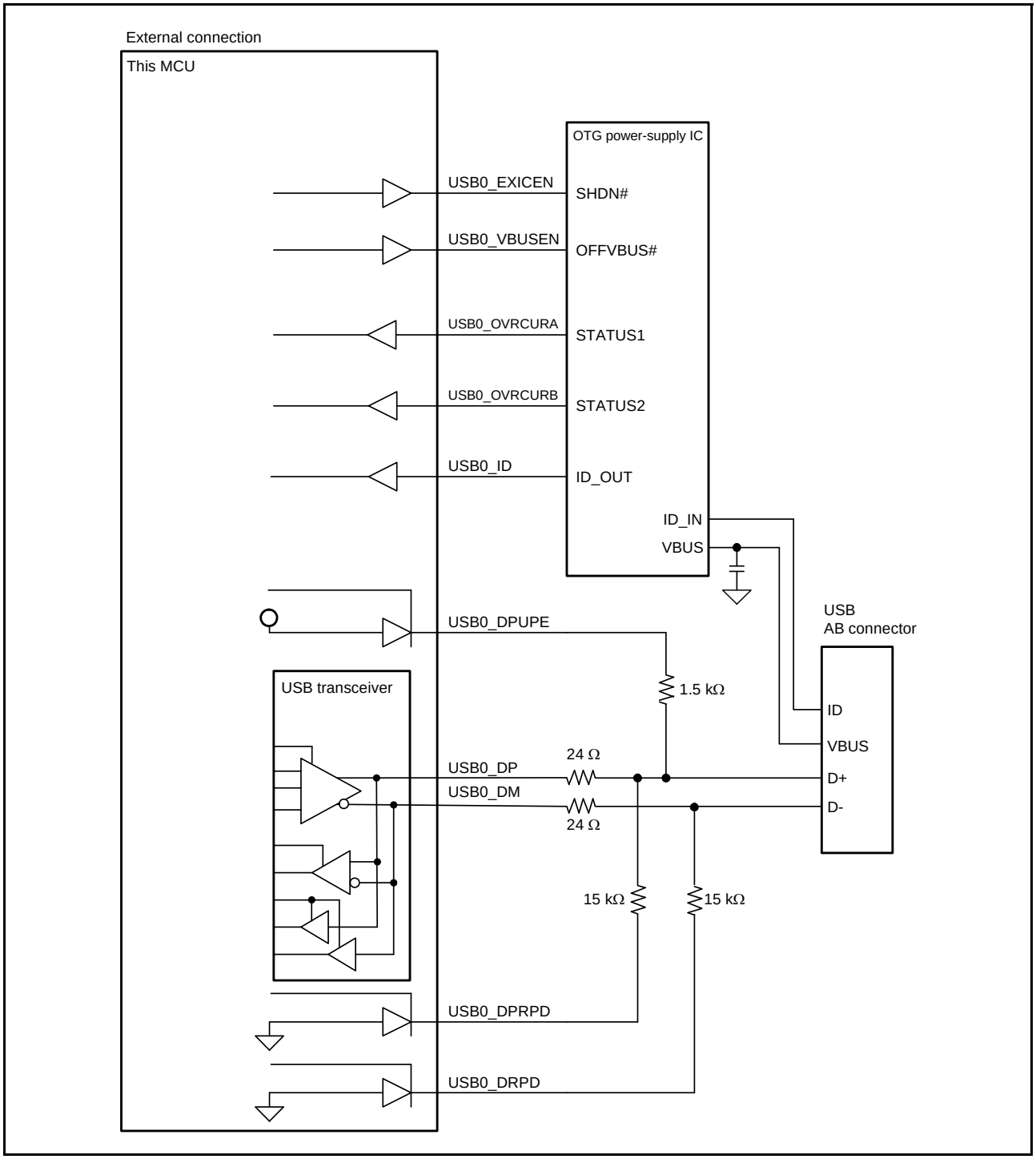


Figure 28.2 Sample OTG Connection of USB Connector (USB0) in Self-Powered State

Figure 28.3 shows an example of functional connection sample of the USB connector in the self-powered state.

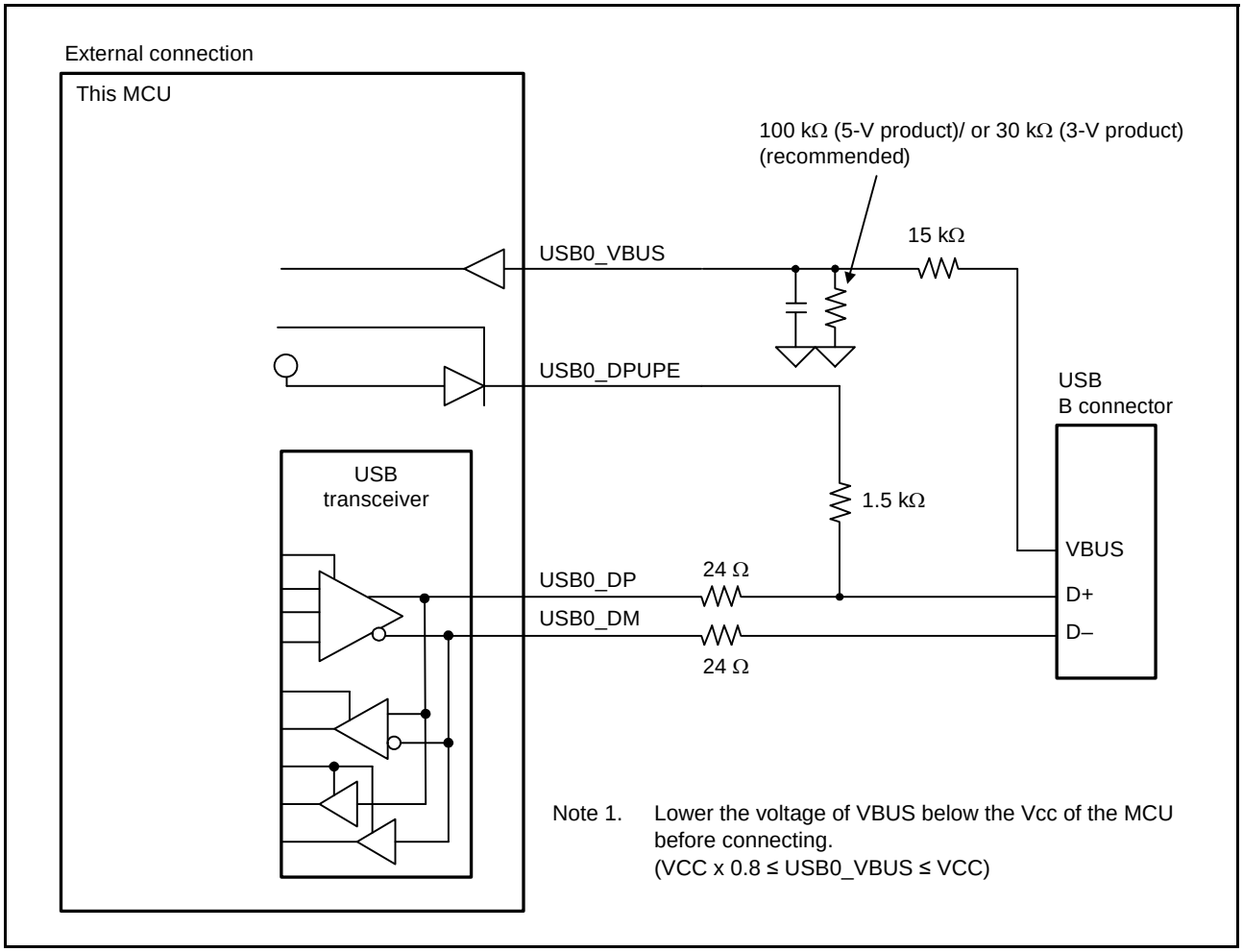


Figure 28.3 Functional Connection Sample of USB Connector in Self-Powered State

Figure 28.4 shows an example of host connection of the USB connector (USB0).

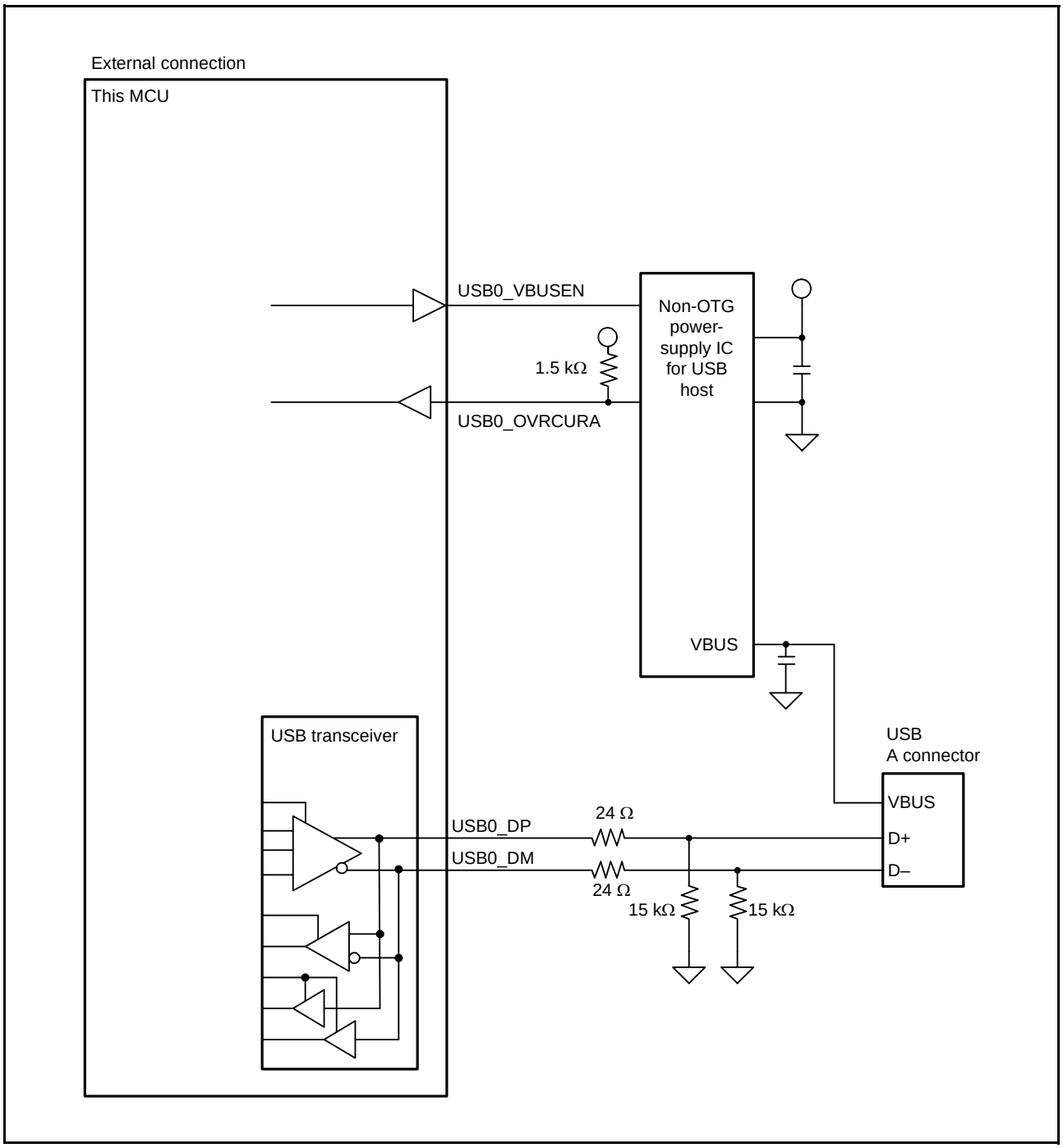


Figure 28.4 Sample Host Connection of USB Connector (USB0)

Figure 28.5 shows a functional connection example of the USB connector in the bus-powered state.

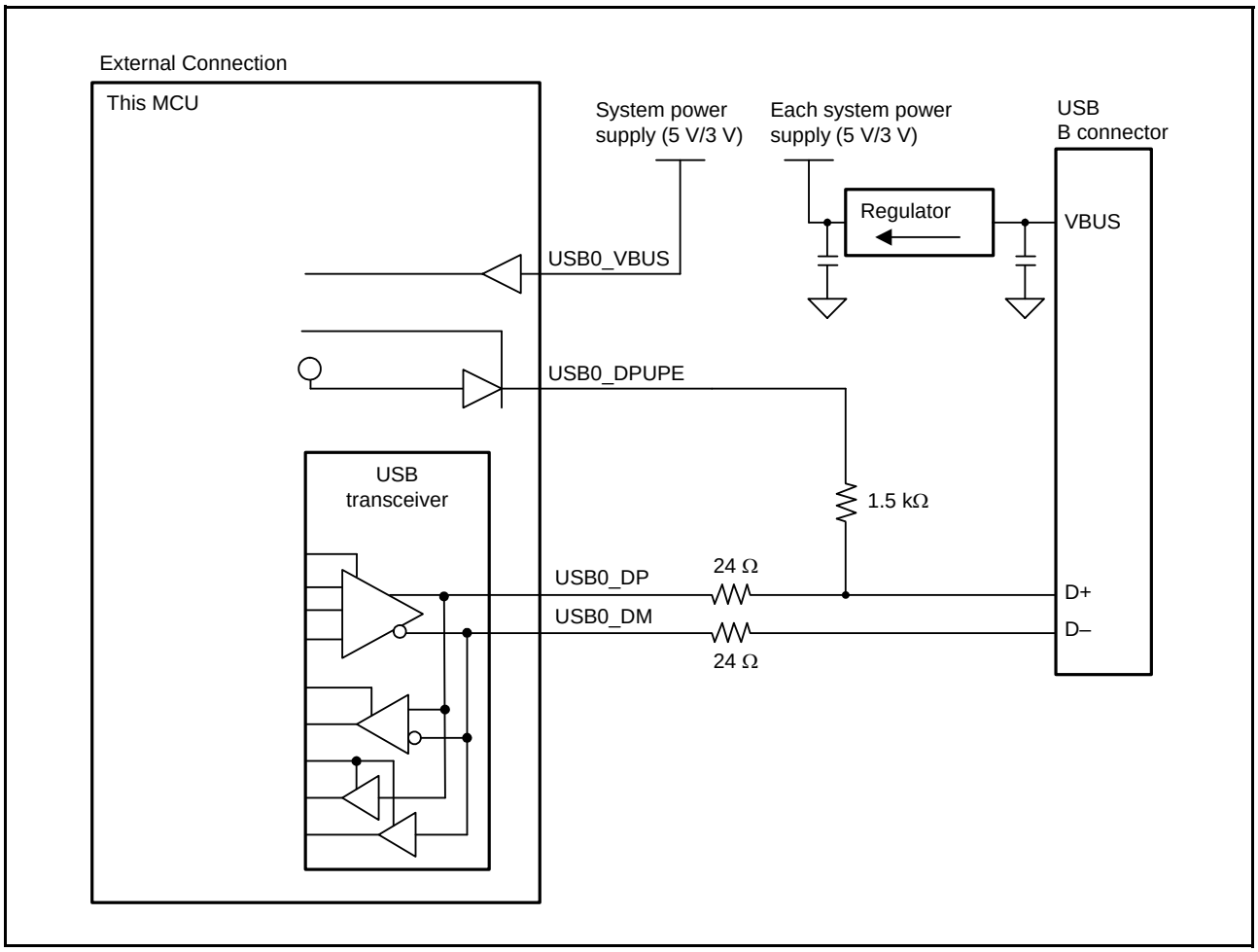


Figure 28.5 Functional Connection Example of USB Connector in Bus-Powered State

The examples of external circuits given in this section are simplified circuits, and their operation in every system is not guaranteed.

28.3.2 Interrupt Sources

Table 28.10 lists the interrupt sources in the USB.

When an interrupt generation condition is satisfied and the interrupt output is enabled using the corresponding interrupt enable register, the USB issues a USB interrupt request to the interrupt controller (ICUA) and an USB interrupt will be generated.

Table 28.10 Interrupt Sources

Bit to be Set	Name	Interrupt Source	Function That Generates the Interrupt	Status Flag
VBINT	VBUS interrupt	• When a change in the state of the USBm_VBUS input pin has been detected (low to high or high to low)	Host/function*1	INTSTS0. VBSTS
RESM	Resume interrupt	• When a change in the state of the USB bus has been detected in the suspended state (J-state to K-state or J-state to SE0)	Function	—
SOFR	Frame number update interrupt	[Host controller function is selected] • When an SOF packet with a different frame number has been transmitted [Function controller function is selected] • When an SOF packet with a different frame number has been received	Host/function	—
DVST	Device state transition interrupt	• When a device state transition has been detected (any of the following conditions) A USB bus reset detected Suspend state detected SET_ADDRESS request received SET_CONFIGURATION request received	Function	INTSTS0. DVSQ[2:0]
CTRT	Control transfer stage transition interrupt	• When a stage transition has been detected in control transfer (any of the following conditions) Setup stage completed Control write transfer status stage transition Control read transfer status stage transition Control transfer completed A control transfer sequence error occurred	Function	INTSTS0. CTSQ[2:0]
BEMP	Buffer empty interrupt	• When transmission of all data in the buffer memory has been completed and the buffer has become empty • When a packet larger than the maximum packet size has been received	Host/function	BEMPSTS. PIPEnBEMP
NRDY	Buffer not ready interrupt	[Host controller function is selected] • When STALL has been received from the peripheral device for the issued token • When a response has not been received correctly from the peripheral device for the issued token (no response was returned three consecutive times or a packet reception error occurred three consecutive times) • When an overrun/underrun occurred during isochronous transfer [Function controller function is selected] • When NAK has been returned for an IN or OUT token while the PID = BUF • When a CRC error or a bit stuffing error occurred during data reception in isochronous transfer • When an overrun/underrun occurred during data reception in isochronous transfer	Host/function	NRDYSTS. PIPEnNRDY
BRDY	Buffer ready interrupt	• When the buffer has become ready (reading or writing is enabled)	Host/function	BRDYSTS. PIPEnBRDY
OVRCR	Overcurrent input change interrupt*2	• When a change in the state of the USB0_OVRCURA or USB0_OVRCURB input pin has been detected (low to high or high to low)	Host	INTSTS1. OVRCR
BCHG	Bus change interrupt*2	• When a change of USB bus state has been detected	Host/function	SYSSTS0. LNST[1:0]
DTCH	Disconnection detection during full-speed operation*2	• When disconnection of a peripheral device has been detected in full-speed operation	Host	DVSTCTR0. RHST[2:0]
ATTCH	Device connection detection*2	• When J-State or K-State is detected on the USB port for 2.5µs. Used for checking whether a peripheral device is connected.	Host	—
EOFERR	EOF error detection*2	• When an EOF error of a peripheral device has been detected	Host	—
SACK	Normal setup operation*2	• When the normal response (ACK) for the setup transaction has been received	Host	—
SIGN	Setup error*2	• When a setup transaction error (no response or ACK packet corruption) was detected three consecutive times	Host	—

Note 1. Though this interrupt can be generated while the host function is selected, it is not usually used with the host function.
Note 2. These interrupts are not provided in USB1.

Figure 28.6 shows the circuits related to the interrupts in the USB0.

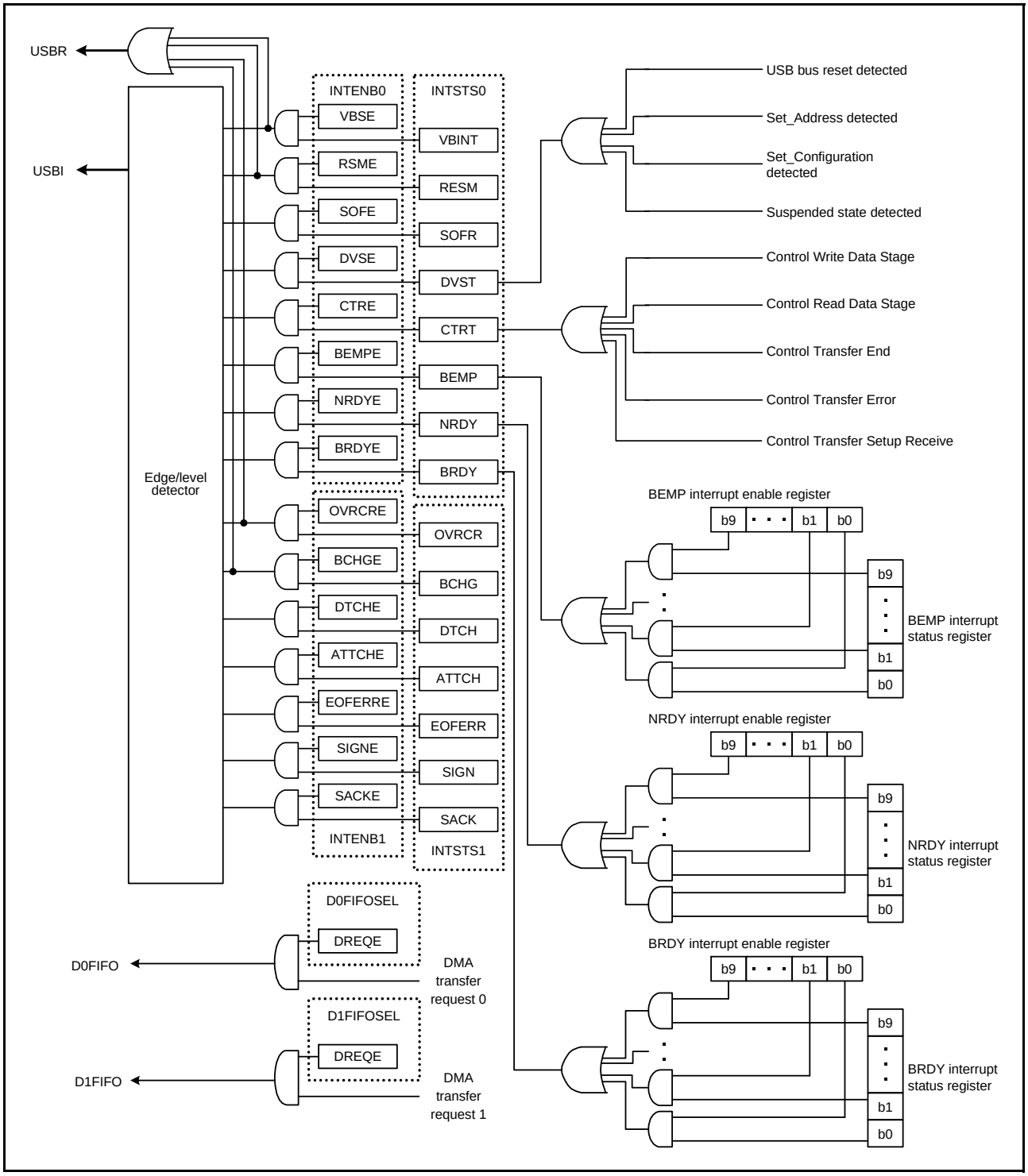


Figure 28.6 Circuits Related to Interrupts in the USB0

Table 28.11 shows the interrupts generated in the USB0.

Table 28.11 USB0 Interrupts

Interrupt Name	Interrupt Flag	DTC Activation	DMAC Activation	Priority
D0FIFO	DMA transfer request 0	Possible	Possible	High
D1FIFO	DMA transfer request 1	Possible	Possible	
USBI	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt, overcurrent input change interrupt, bus change interrupt, disconnection detection during full-speed operation, device connection detection, EOF error detection, normal setup operation, and setup error	Not possible	Not possible	
USBR	VBUS interrupt, resume interrupt, overcurrent input change interrupt, and bus change interrupt	Not possible	Not possible	—

Low

28.3.3 Interrupt Descriptions

28.3.3.1 BRDY Interrupt

The BRDY interrupt is generated when either of the host controller function or function controller function is selected. The following shows the conditions under which the USB sets 1 to a corresponding bit in BRDYSTS. Under this condition, the USB generates a BRDY interrupt if software has set 1 to the PIPEnBRDYE bit that corresponds to the pipe and 1 to the INTENB0.BRDYE bit.
The conditions for generating and clearing the BRDY interrupt depend on the settings of the SOFCFG.BRDYM bit and PIPECFG.BFRE bit for each pipe as described below.

(1) When the SOFCFG.BRDYM Bit = 0 and the PIPECFG.BFRE Bit = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.
On any of the following conditions, the USB generates an internal BRDY interrupt request trigger and sets 1 to the BRDYSTS.PIPEnBRDY bit corresponding to the pertinent pipe.

(a) For the pipe in the transmitting direction:

- When software changes the DIR bit from 0 to 1.
- When packet transmission is completed using the pertinent pipe while write-access from the CPU to the FIFO buffer for the pertinent pipe is disabled (when the BSTS bit is read as 0).
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode.
- No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is completed.
- When the hardware flushes the buffer of the pipe for isochronous transfers.
- When 1 is written to the PIPEnCTR.ACLRM bit, which causes the FIFO buffer to make transition from the write-disabled to write-enabled state.

No request trigger is generated for the DCP (that is, during data transmission for control transfers).

(b) For the pipe in the receiving direction:

- When packet reception is completed successfully thus enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the pertinent pipe is disabled (when the BSTS bit is read as 0).
  No request trigger is generated for the transaction in which DATA-PID disagreement has occurred.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode.
  No request trigger is generated until completion of reading data from the currently-read FIFO buffer even if reception by the other FIFO buffer is completed.

When the function controller function is selected, the BRDY interrupt is not generated in the status stage of control transfers.
The PIPEnBRDY interrupt status of the pertinent pipe can be cleared to 0 by writing 0 to the corresponding PIPEnBRDY bit in BRDYSTS through software. In this case, 1s should be written to the PIPEnBRDY bits for the other pipes.
Clear the BRDY status before accessing the FIFO buffer.

(2) When the SOFCFG.BRDYM Bit = 0 and the PIPECFG.BFRE Bit = 1

With these settings, the USB generates a BRDY interrupt on completion of reading all data for a single transfer using the pipe in the receiving direction, and sets 1 to the bit in BRDYSTS corresponding to the pertinent pipe.
On any of the following conditions, the USB determines that the last data for a single transfer has been received.

- When a short packet including a zero-length packet is received.
- When the transaction counter register (PIPEnTRN) is used and the number of packets specified by the PIPEnTRN.TRNCNT[15:0] bits are completely received.

When the pertinent data is completely read out after any of the above conditions has been satisfied, the USB determines that all data for a single transfer has been completely read out.
When a zero-length packet is received while the FIFO buffer is empty, the USB determines that all data for a single transfer has been completely read out upon passing the zero-length packet data to the CPU. In this case, to start the next transfer, write 1 to the BCLR bit in the corresponding port control register through software.
With these settings, the USB does not detect a BRDY interrupt for the pipe in the transmitting direction.
The PIPEnBRDY interrupt status of the pertinent pipe can be cleared to 0 by writing 0 to the corresponding BRDYSTS.PIPEnBRDY bit through software. In this case, 1s should be written to the PIPEnBRDY bits for the other pipes.
In this mode, the PIPECFG.BFRE bit setting should not be modified until all data for a single transfer has been processed. When it is necessary to modify the PIPECFG.BFRE bit before completion of processing, all FIFO buffers for the pertinent pipe should be cleared using the PIPEnCTR.ACLRM bit.

(3) When the SOFCFG.BRDYM Bit = 1 and the PIPECFG.BFRE Bit = 0

With these settings, the BRDYSTS.PIPEnBRDY values are linked to the BSTS bit setting for each pipe. In other words, the BRDY interrupt status bits (PIPEnBRDY) are set to 1 or 0 by the USB depending on the FIFO buffer status.

(a) For the pipe in the transmitting direction:

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for write access, and are set to 0 when it is not ready.
However, the BRDY interrupt is not generated even if the DCP in the transmitting direction is ready for write access.

(b) For the pipe in the receiving direction:

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for read access, and are set to 0 when all data have been read (not ready for read access).
When a zero-length packet is received while the FIFO buffer is empty, the pertinent bit is set to 1 and the BRDY interrupt is continuously generated until BCLR = 1 is written through software.
With this setting, the PIPEnBRDY bit cannot be cleared to 0 through software.
When the SOFCFG.BRDYM bit is set to 1, all PIPECFG.BFRE bits (for all pipes) should be cleared to 0.

Figure 28.7 shows the timing of BRDY interrupt generation.

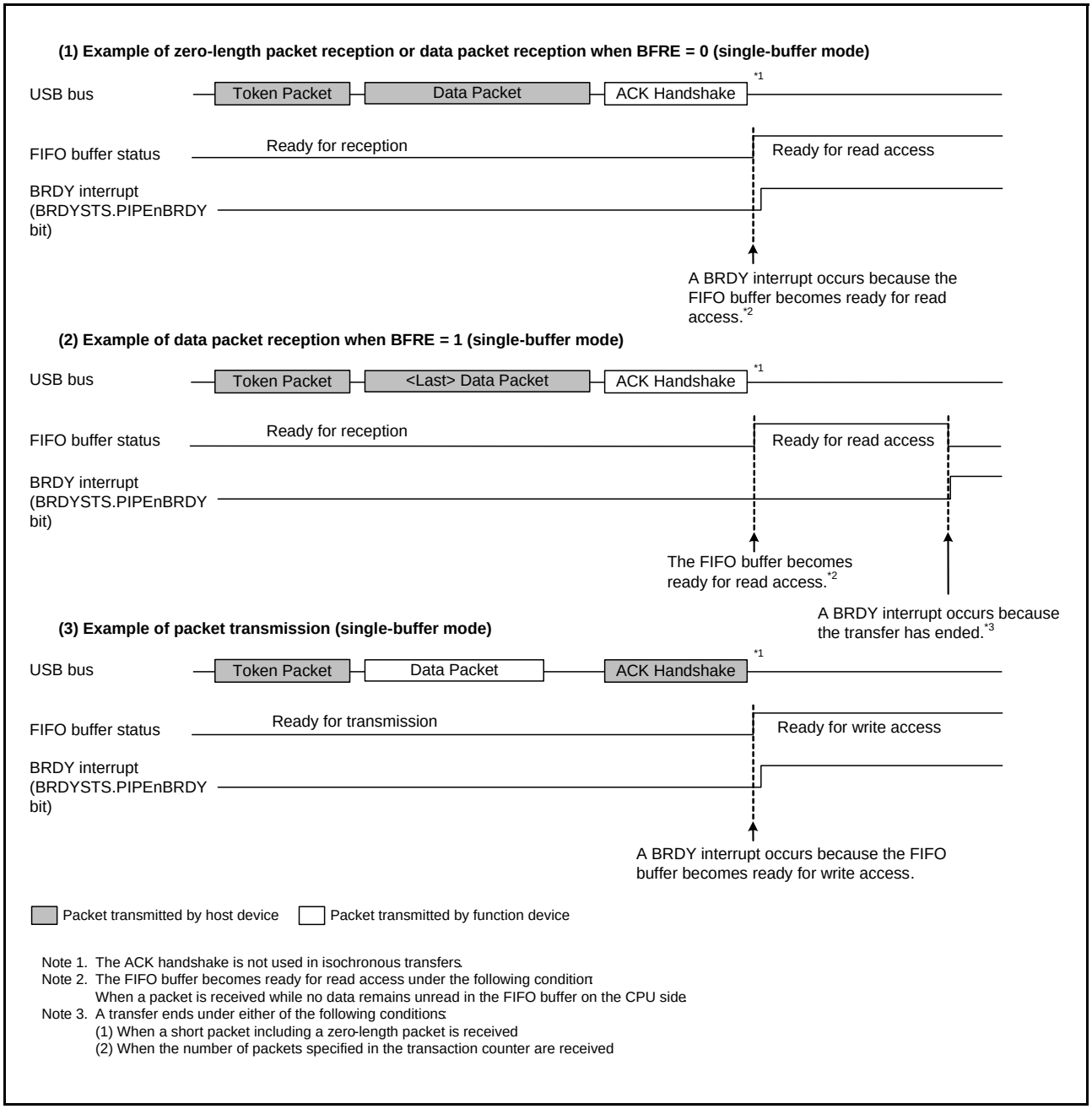


Figure 28.7 Timing of BRDY Interrupt Generation

The condition that USB clears the INTSTS0.BRDY bit depends on the SOFCFG.BRDYM bit setting. Table 28.12 shows the condition for clearing the BRDY bit.

Table 28.12 Condition for Clearing BRDY Bit

BRDYM Bit	Condition for Clearing BRDY Bit
0	The USB clears the BRDY bit when software has cleared all bits in BRDYSTS.
1	The USB clears the BRDY bit when the BSTS bits for all piles have become 0.

28.3.3.2 NRDY Interrupt

On generating an internal NRDY interrupt request for the pipe whose PID bits are set to BUF by software, the USB sets the corresponding PIPEnNRDY bit in NRDYSTS to 1. If the corresponding bit in NRDYENB has been set to 1 by software, the USB sets the INTSTS0.NRDY bit to 1 and generates a USB interrupt.
The following describes the conditions on which the USB generates the internal INTSTS0.NRDY interrupt request for a given pipe.
Note that the internal NRDY interrupt request is not generated during setup transaction execution when the host controller function is selected. During setup transactions when the host controller function is selected, the SACK or SIGN interrupt is detected.
The internal NRDY interrupt request is not generated during status stage execution of the control transfer when the function controller function is selected.

(1) When Host Controller Function is Selected

(a) For the pipe in the transmitting direction:

On any of the following conditions, the USB detects an NRDY interrupt.

- For the pipe for isochronous transfers, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer.
  In this case, the USB transmits a zero-length packet following the OUT token and sets the bit corresponding to the NRDYSTS.PIPEnNRDY bit and the FRMNUM.OVRN bit to 1.
- During communications other than setup transactions using the pipe for the transfers other than isochronous transfers, when any combination of the following two cases occur three consecutive times: 1) no response is returned from the peripheral device (when timeout is detected before detection of the handshake packet from the peripheral device) and 2) an error is detected in the packet from the peripheral device.
  In this case, the USB sets the bit corresponding to the PIPEnNRDY bit to 1 and modifies the setting of the PID[1:0] bits of the corresponding pipe to NAK.
- During communications other than setup transactions, when the STALL handshake is received from the peripheral device.
  In this case, the USB sets the bit corresponding to the PIPEnNRDY bit to 1 and modifies the setting of the PID[1:0] bits of the corresponding pipe to STALL (11b).

(b) For the pipe in the receiving direction:

- For the pipe for isochronous transfers, when the time to issue an IN token comes while there is no space available in the FIFO buffer.
  In this case, the USB discards the received data for the IN token and sets the PIPEnNRDY bit corresponding to the pipe and the OVRN bit to 1.
  When a packet error is detected in the received data for the IN token, the USB also sets the FRMNUM.CRCE bit to 1.
- For the pipe for the transfers other than isochronous transfers, when any combination of the following two cases occur three consecutive times: 1) no response is returned from the peripheral device for the IN token issued by the USB (when timeout is detected before detection of the DATA packet from the peripheral device) and 2) an error is detected in the packet from the peripheral device.
  In this case, the USB sets the PIPEnNRDY bit corresponding to the pipe to 1 and modifies the setting of the PID[1:0] bits of the corresponding pipe to NAK.
- For the pipe for isochronous transfers, when no response is returned from the peripheral device for the IN token (when timeout is detected before detection of the DATA packet from the peripheral device) or an error is detected in the packet from the peripheral device.
  In this case, the USB sets the PIPEnNRDY bit corresponding to the pipe to 1. (The setting of the PID[1:0] bits of the pipe is not modified.)

- For the pipe for isochronous transfers, when a CRC error or a bit stuffing error is detected in the received data packet.
  In this case, the USB sets the PIPEnNRDY bit corresponding to the pipe and the CRCE bit to 1.
- When the STALL handshake is received.
  In this case, the USB sets the PIPEnNRDY bit corresponding to the pipe to 1 and modifies the setting of the PID[1:0] bits of the corresponding pipe to STALL.

(2) When Function Controller Function is Selected

(a) For the pipe in the transmitting direction:

- When an IN token is received while there is no data to be transmitted in the FIFO buffer.
  In this case, the USB generates a NRDY interrupt request at the reception of the IN token and sets the NRDYSTS.PIPEnNRDY bit to 1.
  For the pipe for the isochronous transfers in which an interrupt is generated, the USB transmits a zero-length packet and sets the FRMNUM.OVRN bit to 1.

(b) For the pipe in the receiving direction:

- When an OUT token is received while there is no space available in the FIFO buffer.
  For the pipe for the isochronous transfers in which an interrupt is generated, the USB generates a NRDY interrupt request at the reception of the OUT token and sets the PIPEnNRDY bit to 1 and OVRN bit to 1.
  For the pipe for the transfers other than isochronous transfers in which an interrupt is generated, the USB generates a NRDY interrupt request when a NAK handshake is transferred after the data following the OUT token is received, and sets the PIPEnNRDY bit to 1.
  However, during re-transmission (due to DATA-PID disagreement), the NRDY interrupt request is not generated.
  In addition, if an error occurs in the DATA packet, the NRDY interrupt request is not generated.
- For the pipe for isochronous transfers, when a token is not received successfully within an interval frame.
  In this case, the USB generates a NRDY interrupt request when SOF is received, and sets the PIPEnNRDY bit to 1.

Figure 28.8 shows the timing of NRDY interrupt generation when the function controller function is selected.

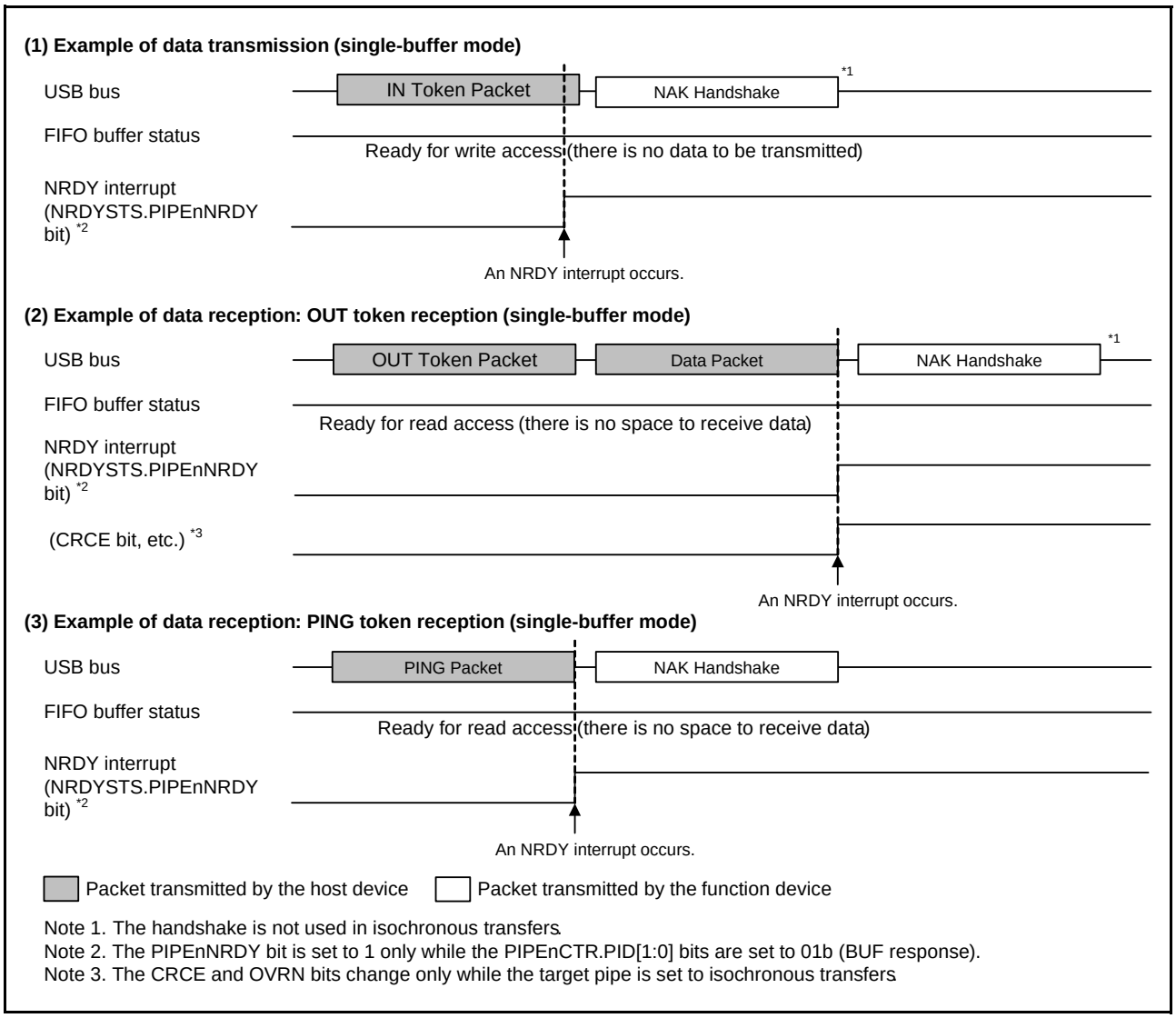


Figure 28.8 Timing of NRDY Interrupt Generation (When Function Controller Function is Selected)

28.3.3.3 BEMP Interrupt

On detecting a BEMP interrupt for the pipe whose PID bits are set to BUF by software, the USB sets the corresponding BEMPSTS.PIPEnBEMP bit to 1. If the corresponding bit in BEMPENB has been set to 1 by software, the USB sets the INTSTS0.BEMP bit to 1 and generates a USB interrupt.

The following describes the conditions on which the USB generates an internal BEMP interrupt request.

(1) For the pipe in the transmitting direction:

When the FIFO buffer of the corresponding pipe is empty on completion of transmission (including zero-length packet transmission).
In single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for the pipe other than DCP. However, the internal BEMP interrupt request is not generated on any of the following conditions.

- When writing data to the FIFO buffer of the CPU has already started by the CPU or DMA/DTC transfer on completion of transmitting data from one FIFO buffer in double buffer mode.
- When the buffer is cleared (emptied) by setting the PIPEnCTR.ACLRM or the BCLR bit in the port control register to 1.
- When IN transfer (zero-length packet transmission) is performed during the control transfer status stage while the function controller function is selected.

(2) For the pipe in the receiving direction:

When the successfully-received data packet size exceeds the specified maximum packet size.
In this case, the USB generates a BEMP interrupt request, sets the corresponding BEMPSTS.PIPEnBEMP bit to 1, discards the received data, and modifies the setting of the PID[1:0] bits of the corresponding pipe to STALL (11).
Here, the USB returns no response when used as the host controller, and returns STALL response when used as the function controller.
However, the internal BEMP interrupt request is not generated on any of the following conditions.

- When a CRC error or a bit stuffing error is detected in the received data.
- When a setup transaction is being performed,
  Writing 0 to the BEMPSTS.PIPEnBEMP bit clears the status.
  Writing 1 to the BEMPSTS.PIPEnBEMP bit has no effect.

Figure 28.9 shows the timing of BEMP interrupt generation when the function controller function is selected.

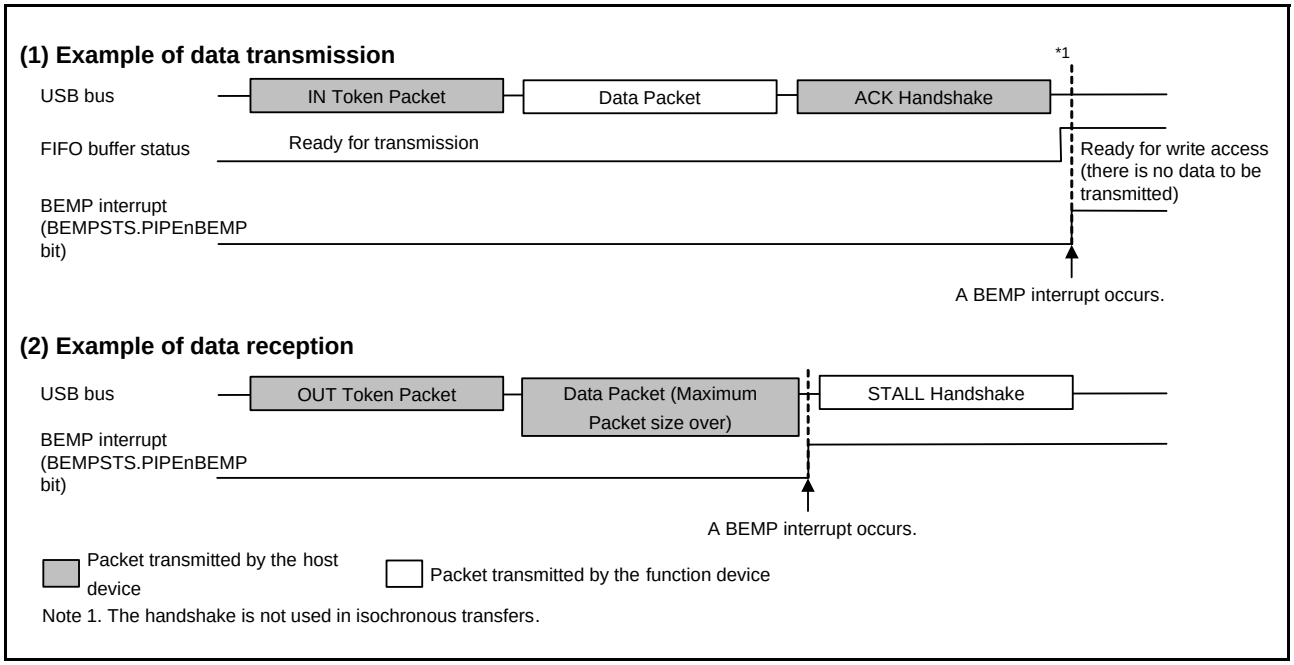


Figure 28.9 Timing of BEMP Interrupt Generation (When Function Controller Function is Selected)

28.3.3.4 Device State Transition Interrupt

Figure 28.10 is a diagram of device state transitions in the USB. The USB controls device state and generates device state transition interrupts. However, recovery from the suspended state (resume signal detection) is detected by means of the resume interrupt. The device state transition interrupts can be enabled or disabled individually using INTENB0. The device state to which a transition was made can be confirmed using the DVSQ bits in INTSTS0.
When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is detected.
Device state can be controlled only when the function controller function is selected. The device state transition interrupts can also be generated only when the function controller function is selected.

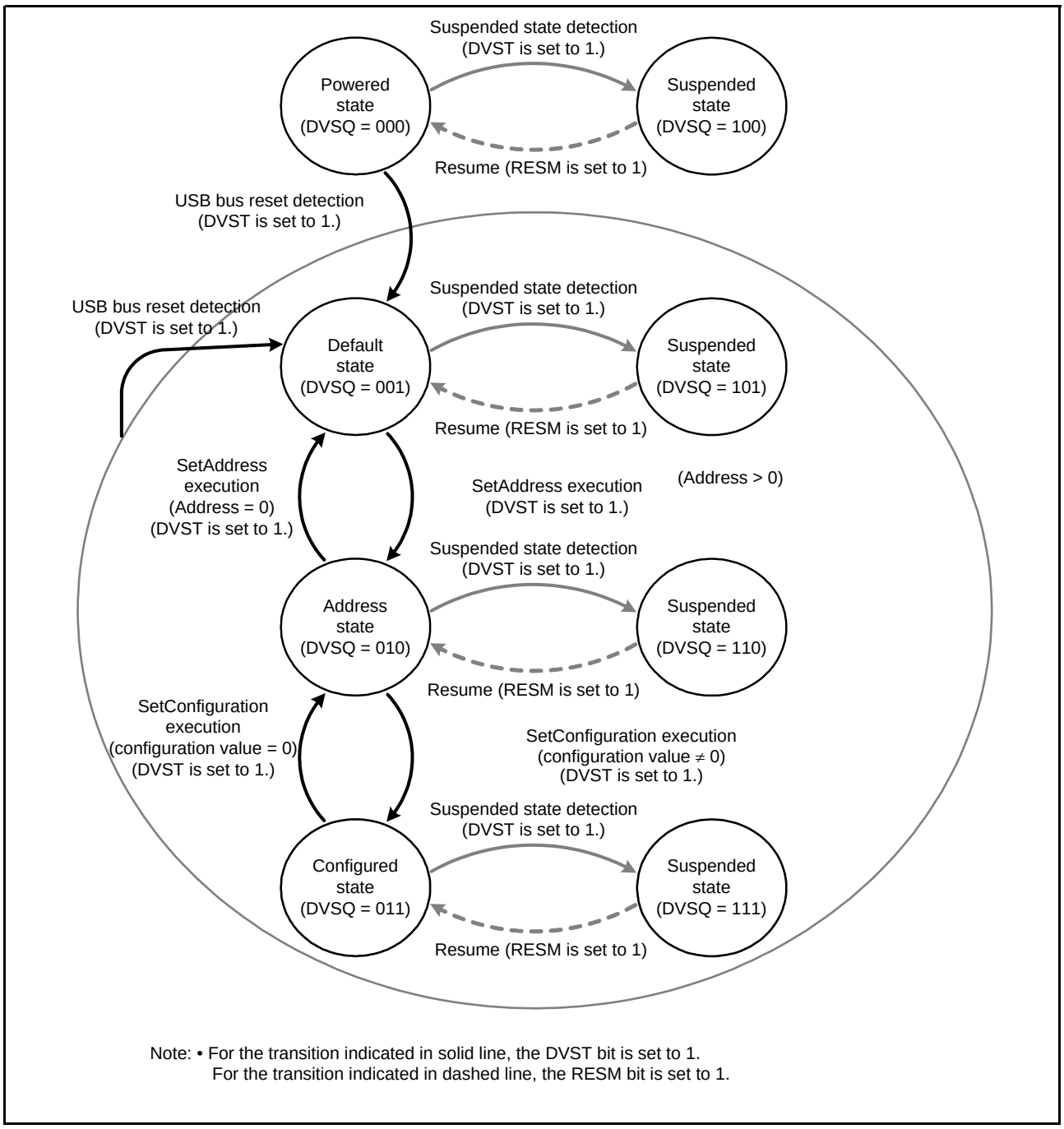


Figure 28.10 Device State Transitions

28.3.3.5 Control Transfer Stage Transition Interrupt

Figure 28.11 is a diagram of control transfer stage transitions in the USB. The USB controls the control transfer sequence and generates control transfer stage transition interrupts. The control transfer stage transition interrupts can be enabled or disabled individually using INTENB0. The transfer stage to which a transition was made can be confirmed using the CTSQ[2:0] bits in INTSTS0.

Control transfer stage transition interrupts are generated only when the function controller function is selected.

The control transfer sequence errors are listed below. If an error occurs, the DCPCTR.PID[1:0] bits are set to 1xb (STALL response).

During control read transfer:

- An OUT token is received while no data has been transferred for the IN token at the data stage.
- An IN token is received at the status stage.
- A data packet with DATAPID = DATA0 is received at the status stage.

During control write transfer:

- An IN token is received while no ACK response has been returned for the OUT token at the data stage.
- A data packet with DATAPID = DATA0 is received for the first data packet at the data stage.
- An OUT token is received at the status stage
- During no-data control transfers:
- An OUT token is received at the status stage.

At the control write transfer data stage, if the number of receive data exceeds the wLength value of the USB request, it cannot be recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error (INTSTS0.CTRT= 1), CTSQ[2:0] = 110b value is retained until the CTRT bit = 0 is written from the system (the interrupt status is cleared). Therefore, while CTSQ[2:0] = 110b is being held, the CTRT interrupt that ends the setup stage will not be generated even if a new USB request is received. (The USB retains the setup stage end, and after the interrupt status has been cleared by software, a setup stage end interrupt is generated.)

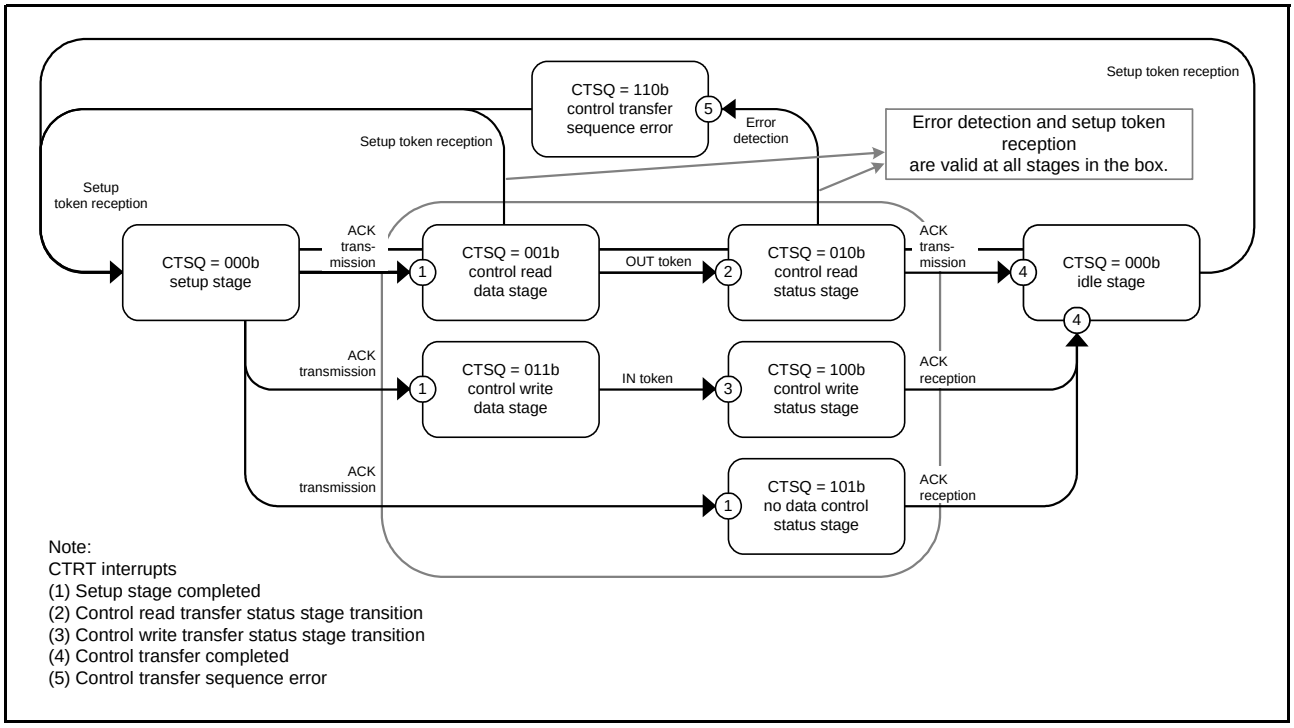


Figure 28.11 Control Transfer Stage Transitions

28.3.3.6 Frame Update Interrupt

With the host controller function selected, an interrupt is generated at the timing when the frame number is updated. With the function controller function selected, an SOFR interrupt is generated when the frame number is updated.
When the function controller function is selected, the USB updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

28.3.3.7 VBUS Interrupt

When the USB0_VBUS pin level changes, a VBUS interrupt is generated. The level of the USB0_VBUS pin can be checked with the INTSTS0.VBSTS bit. Whether the host controller is connected or disconnected can be confirmed using the VBUS interrupt. However, if the system is activated with the host controller connected, the first VBUS interrupt is not generated because there is no change in the USB0_VBUS pin level.

28.3.3.8 Resume Interrupt

When the function controller function is selected, a resume interrupt is generated when the device state is the suspended state and the USB bus state has changed (from J-state to K-state, or from J-state to SE0). Recovery from the suspended state is detected by means of the resume interrupt.
When the host controller function is selected, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

28.3.3.9 OVRCR Interrupt

An OVRCR interrupt is generated when the USB0_OVRCURA or USB0_OVRCURB pin level has changed. The levels of the USB0_OVRCURA and USB0_OVRCURB pins can be checked with the SYSSTS0.OCVMON[1:0] bits. The external power-supply IC can check whether overcurrent has been detected using the OVRCR interrupt.
For On-The-Go connection, whether a change has been detected in the VBUS comparator can be checked using the OVRCR interrupt.

28.3.3.10 BCHG Interrupt

A BCHG interrupt is generated when the USB bus state has changed. The BCHG interrupt can be used to detect whether the peripheral device is connected and can also be used to detect a remote wakeup when the host controller function is selected. The BCHG interrupt is generated regardless of whether the host controller function or function controller function is selected.

28.3.3.11 DTCH Interrupt

A DTCH interrupt is generated when disconnection of the USB bus is detected while the host controller function is selected. The USB detects bus disconnection based on USB Specification 2.0.
After detecting a DTCH interrupt, the USB controls hardware as described below (irrespective of the value set in the corresponding interrupt enable bit). Software should terminate all pipes in which communications are currently carried out for the pertinent port and make a transition to the wait state for bus connection to the pertinent port (wait state for ATTCH interrupt generation).

- Modifies the DVSTCTR0.UACT bit for the port in which a DTCH interrupt has been detected to 0.
- Puts the port in which a DTCH interrupt has been generated into the idle state.

28.3.3.12 SACK Interrupt

A SACK interrupt is generated when an ACK response for the transmitted setup packet has been received from the peripheral device with the host controller function selected. The SACK interrupt can be used to confirm that the setup transaction has been completed successfully.

28.3.3.13 SIGN Interrupt

A SIGN interrupt is generated when an ACK response for the transmitted setup packet has not been correctly received from the peripheral device three consecutive times with the host controller function selected. The SIGN interrupt can be used to detect no ACK response transmitted from the peripheral device or corruption of an ACK packet.

28.3.3.14 ATTCH Interrupt

An ATTCH interrupt is generated when J-state or K-state of the full-speed signal level is detected on the USB port for 2.5 s with the host controller function selected. To be more specific, an ATTCH interrupt is detected on any of the following conditions.
When K-state, SE0, or SE1 changes to J-state, and J-state continues 2.5 µs.
When J-state, SE0, or SE1 changes to K-state, and K-state continues 2.5 µs.

28.3.3.15 EOFERR Interrupt

An EOFERR interrupt is generated when it is detected that communication is not completed at the EOF2 timing prescribed in USB Specification 2.0.
After detecting an EOFERR interrupt, the USB controls hardware as described below (irrespective of the value set in the corresponding interrupt enable bit). Software should terminate all pipes in which communications are currently carried out for the pertinent port and perform re-enumeration of the pertinent port.

- Modifies the DVSTCTR0.UACT bit for the port in which an EOFERR interrupt has been detected to 0.
- Puts the port in which an EOFERR interrupt has been generated into the idle state.

28.3.4 Pipe Control

Table 28.13 lists the pipe setting items in the USB. With USB data transfer, data transfer has to be carried out using the logic pipe called the endpoint. The USB has ten pipes that are used for data transfer.
Appropriate settings should be made for each of the pipes according to the specifications of the system.

Table 28.13 Pipe Setting Items

Register Name	Bit Name	Setting	Remarks
DCPCFG PIPECFG	TYPE	Specifies the transfer type	PIPE1 to PIPE9: Can be set
	BFRE	Selects the BRDY interrupt mode	PIPE1 to PIPE5: Can be set
	DBLB	Selects double buffer mode	PIPE1 to PIPE5: Can be set
	DIR	Selects transfer direction	IN or OUT can be set
	EPNUM	Endpoint number	PIPE1 to PIPE9: Can be set A value other than 0000 should be set when the pipe is used.
	SHTNAK	Selects disabled state for pipe when transfer ends	PIPE1 and PIPE2: Can be set (only when bulk transfer has been selected) PIPE3 to PIPE5: Can be set
DCPMAXP PIPEMAXP	DEVSEL	Selects a device	Referenced only when the host controller function is selected.
	MXPS	Maximum packet size	Compliant with the USB standard.
PIPEPERI	IFIS	Buffer flush	PIPE1 and PIPE2: Can be set (only when isochronous transfer has been selected) PIPE3 to PIPE9: Cannot be set
	IITV[2:0]	Interval counter	PIPE1 and PIPE2: Can be set (only when isochronous transfer has been selected) PIPE3 to PIPE5: Cannot be set PIPE6 to PIPE9: Can be set (only when the host controller function has been selected)
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit.
	INBUFM	IN buffer monitor	Available only for PIPE3 to PIPE5.
	SUREQ	SETUP request	Can be set only for the DCP. Can be controlled only when the host controller function has been selected.
	SUREQCLR	SUREQ clear	Can be set only for the DCP. Can be controlled only when the host controller function has been selected.
	ATREPM	Auto response mode	PIPE1 to PIPE5: Can be set Can be set only when the function controller function has been selected.
	ACLRM	Auto buffer clear	PIPE1 to PIPE9: Can be set
	SQCLR	Sequence clear	Clears the data toggle bit.
	SQSET	Sequence set	Sets the data toggle bit.
	SQMON	Sequence monitor	Monitors the data toggle bit.
	PBUSY	Pipe busy status	
	PID	Response PID	See section 28.3.4.6, Response PID.
PIPEnTRE	TRENB	Transaction counter enable	PIPE1 to PIPE5: Can be set
	TRCLR	Current transaction counter clear	PIPE1 to PIPE5: Can be set
PIPEnTRN	TRNCNT	Transaction counter	PIPE1 to PIPE5: Can be set

28.3.4.1 Pipe Control Register Switching Procedures

The following bits in the pipe control registers can be modified only when USB communication is disabled (PID = NAK).

Registers that Should Not be Set in the USB Communication Enabled (PID = BUF) State:

- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Bits in PIPEnTRE and PIPEnTRN

In order to modify the above bits in the USB communication enabled (PID = BUF) state, follow the procedure shown below:

1. A request to modify bits in the pipe control register occurs.
2. Modify the PID[1:0] bit corresponding to the pipe to NAK.
3. Wait until the corresponding PBUSY bit is cleared to 0.
4. Modify the bits in the pipe control register.

The following bits in the pipe control registers can be modified only when the pertinent pipe information has not been set by the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Registers that Should Not be Set When CURPIPE[3:0] in FIFO-PORT is set:

- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG, PIPEMAXP and PIPEPERI

In order to modify pipe information, the CURPIPE[3:0] bits in the port select registers should be set to a pipe other than the pipe to be modified. For the DCP, the buffer should be cleared using the BCLR in the port control register after the pipe information is modified.

28.3.4.2 Transfer Types

The PIPECFG.TYPE[1:0] bits are used to specify the transfer type for each pipe. The transfer types that can be set for the pipes are as follows.

- DCP: No setting is necessary (fixed at control transfer).
- PIPE1 and PIPE2: These should be set to bulk transfer or isochronous transfer.
- PIPE3 to PIPE5: These should be set to bulk transfer.
- PIPE6 to PIPE9: These should be set to interrupt transfer.

28.3.4.3 Endpoint Number

The PIPECFG.EPNUM[3:0] bits are used to set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to endpoint 15.

- DCP: No setting is necessary (fixed at end point 0).
- PIPE1 to PIPE9: The endpoint numbers from 1 to 15 should be selected and set.
  These should be set so that the combination of the PIPECFG.DIR bit and EPNUM[3:0] bits is unique.

28.3.4.4 Maximum Packet Size Setting

The DCPMAXP.MXPS[6:0] bits and the MXPS[8:0] in PIPEMAXP are used to specify the maximum packet size for each pipe. DCP and PIPE1 to PIPE5 can be set to any of the maximum pipe sizes defined by the USB specification. For PIPE6 to PIPE9, 64 bytes are the upper limit of the maximum packet size. The maximum packet size should be set before beginning the transfer (PID = BUF).

- DCP: Set 8, 16, 32, or 64.
- PIPE1 to PIPE5: Set 8, 16, 32, or 64 when using bulk transfer.
- PIPE1 and PIPE2: Set a value between 1 and 256 when using isochronous transfer.
- PIPE6 to PIPE9: Set a value between 1 and 64.

28.3.4.5 Transaction Counter (For PIPE1 to PIPE5 in Reading Direction)

When the specified number of transactions has been completed in the data packet receiving direction, the USB recognizes that the transfer has ended. Two transaction counters are provided: one is the PIPEnTRN register that specifies the number of transactions to be executed and the other is the current counter that internally counts the number of executed transactions. With the PIPECFG.SHTNAK bit set to 1, when the current counter value matches the specified number of transactions, the corresponding PIPEnCTR.PID[1:0] bits are set to NAK and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the PIPEnTRE.TRCLR bit. The information read from PIPEnTRN differs depending on the setting of the PIPEnTRE.TRENB bit.

- The TRENB bit = 0: The specified transaction counter value can be read.
- The TRENB bit = 1: The current counter value indicating the internally counted number of executed transactions can be read.

When operating the TRCLR bit, the following should be noted.

- If the transactions are being counted and PID = BUF, the current counter cannot be cleared.
- If there is any data left in the buffer, the current counter cannot be cleared.

28.3.4.6 Response PID

The PID[1:0] bits in DCPCTR and PIPEnCTR are used to set the response PID for each pipe.
The following shows the USB operation with various response PID settings:

(1) Response PID settings when the host controller function is selected:

The response PID is used to specify the execution of transactions.

- NAK setting: Using pipes is disabled. No transaction is executed.
- BUF setting: Transactions are executed based on the status of the buffer memory.
  For OUT direction: If there are transmit data in the buffer memory, an OUT token is issued.
  For IN direction: If there is an area to receive data in the buffer memory, an IN token is issued.
- STALL setting: Using pipes is disabled. No transaction is executed.

Note: • Setup transactions for the DCP are set with the DCPCTR.SUREQ bit.

(2) Response PID settings when the function controller function is selected:

The response PID is used to specify the response to transactions from the host.

- NAK setting: The NAK response is returned in response to the generated transaction.
- BUF setting: Responses are made to transactions according to the status of the buffer memory.
- STALL setting: The STALL response is returned in response to the generated transaction.

Note: • For setup transactions, an ACK response is returned regardless of the PID[1:0] bits setting, and the USB request is stored in the register.

The USB may write to the PID[1:0] bits, depending on the results of the transaction as described below.

(3) When the host controller function has been selected and the response PID is set by hardware:

- NAK setting: In the following cases, PID = NAK is set and issuing of tokens is automatically stopped:
  When a transfer other than isochronous transfer has been performed and an NRDY interrupt is generated. (For details, see section 28.3.3.2, NRDY Interrupt.)
  - If a short packet is received when the PIPECFG.SHTNAK bit has been set to 1 for bulk transfer.
  - If the transaction counting ends when the SHTNAK bit has been set to 1 for bulk transfer.
- BUF setting: There is no BUF writing by the USB.
- STALL setting: In the following cases, PID = STALL is set and issuing of tokens is automatically stopped:
  When STALL is received in response to the transmitted token.
  When the size of the receive data packet exceeds the maximum packet size.

(4) When the function controller function has been selected and the response PID is set by hardware:

- NAK setting: In the following cases, PID = NAK is set and NAK is returned in response to transactions:
  When the SETUP token is received normally (DCP only).
  If the transaction counting ends or a short packet is received when the PIPECFG.SHTNAK bit has been set to 1 for bulk transfer.
- BUF setting: There is no BUF writing by the USB.
- STALL setting: In the following cases, PID = STALL is set and STALL is returned in response to transactions:
  When a maximum packet size exceeded error is detected in the received data packet.
  When a control transfer sequence error has been detected (DCP only).

28.3.4.7 Data PID Sequence Bit

The USB automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit switches at the timing of ACK handshake reception. When data is received, the sequence bit switches at the timing of ACK handshake transmission. The SQCLR bit in DCPCTR and the SQSET bit in PIPEnCTR can be used to change the data PID sequence bit.

When the function controller function has been selected and control transfer is used, the USB automatically sets the sequence bit when a stage transition is made. DATA0 is returned when the setup stage is ended and DATA1 is returned in a status stageDATA1 is returned when the setup stage is ended. The sequence bit is not read in a status stage and PID = DATA1 is returned. Therefore, software settings are not required. However, when the host controller function has been selected and control transfer is used, the sequence bit should be set by software at a stage transition.

For the ClearFeature request transmission or reception, the data PID sequence bit should be set by software regardless of whether the host controller function or function controller function is selected.

28.3.4.8 Response PID = NAK Function

The USB has a function that disables pipe operation (PID response = NAK) at the timing at which the final data packet of a transaction is received (the USB automatically distinguishes this based on reception of a short packet or the transaction counter) by setting the PIPECFG.SHTNAK bit to 1.

When the double buffer mode is being used for the buffer memory, using this function enables reception of data packets in transfer units. If pipe operation has been disabled, software should set the pipe to the enabled state again (PID response = BUF).

The response PID = NAK function can be used only when bulk transfers are used.

28.3.4.9 Auto Response Mode

With the pipes for bulk transfer (PIPE1 to PIPE5), when the PIPEnCTR.ATREPM bit is set to 1, a transition is made to auto response mode. During an OUT transfer (the PIPECFG.DIR bit = 0), OUT-NAK mode is entered, and during an IN transfer (the DIR bit = 1), null auto response mode is entered.

28.3.4.10 OUT-NAK Mode

With the pipes for bulk OUT transfer, NAK is returned in response to an OUT token and an NRDY interrupt is output when the PIPEnCTR.ATREPM bit is set to 1. To make a transition from normal mode to OUT-NAK mode, OUT-NAK mode should be specified in the pipe operation disabled state (response PID = NAK) before enabling pipe operation (response PID = BUF). After pipe operation has been enabled, OUT-NAK mode becomes valid. However, if an OUT token is received immediately before pipe operation is disabled, the token data is normally received, and an ACK is retuned to the host.

To make a transition from OUT-NAK mode to normal mode, OUT-NAK mode should be canceled in the pipe operation disabled state (response PID = NAK) before enabling pipe operation (response PID = BUF). In normal mode, reception of OUT data is enabled.

28.3.4.11 Null Auto Response Mode

With the pipes for bulk IN transfer, zero-length packets are continuously transmitted when the PIPEnCTR.ATREPM bit is set to 1.

To make a transition from normal mode to null auto response mode, null auto response mode should be set in the pipe operation disabled state (response PID = NAK) before enabling pipe operation (response PID = BUF). After pipe operation has been enabled, null auto response mode becomes valid. Before setting null auto response mode, the PIPEnCTR.INBUFM = 0 should be confirmed because the mode can be set only when the buffer is empty. If the INBUFM bit is 1, the buffer should be emptied with the PIPEnCTR.ACLRM bit. While a transition to null auto response mode is being made, data should not be written from the FIFO port.

To make a transition from null auto response mode to normal mode, pipe operation disabled state (response PID = NAK) should be retained for the period of zero-length packet transmission (about 10 s) before canceling null auto response mode. In normal mode, data can be written from the FIFO port; therefore, packet transmission to the host is enabled by enabling pipe operation (response PID = BUF).

28.3.5 FIFO Buffer Memory

28.3.5.1 FIFO Buffer Memory

The USB has FIFO buffer memory for data transfer. The memory area used for each pipe is managed by the USB. The FIFO buffer memory has two states depending on whether the access right is assigned to the system (CPU side) or the USB (SIE side).

(1) Buffer Status

Table 28.14 and Table 28.15 show the buffer status in the USB. The buffer memory status can be confirmed using the BSTS bit in DCPCTR and the INBUFM bit in PIPEnCTR. The access direction for the buffer memory can be specified using either the PIPECFG.DIR bit or the CFIFOSEL.ISEL bit (when DCP is selected).
The INBUFM bit is valid for PIPE0 to PIPE5 in the transmitting direction.
When a transmitting pipe uses the double buffer configuration, software can read the BSTS bit to monitor the buffer memory status on the CPU side and the INBUFM bit to monitor the buffer memory status on the SIE side. When the BEMP interrupt may not show the buffer empty status because the write access to the FIFO port by the CPU or the DMA/DTC tranfser is slow, software can use the INBUFM bit to confirm the end of transmission.

Table 28.14 Buffer Status Indicated by the BSTS Bit

ISEL or DIR	BSTS	Buffer Memory Status
0 (receiving direction)	0	There is no received data, or data is being received. Reading from the FIFO port is disabled.
0 (receiving direction)	1	There is received data, or a zero-length packet has been received. Reading from the FIFO port is allowed. Note that when a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	The transmission has not been completed. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	The transmission has been completed. CPU write is allowed.

Table 28.15 Buffer Status Indicated by the INBUFM Bit

DIR	INBUFM	Buffer Memory Status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	The transmission has been completed. There is no waiting data to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

28.3.5.2 FIFO Buffer Clearing

Table 28.16 shows the clearing of the FIFO buffer memory by the USB. The buffer memory can be cleared using the BCLR, DnFIFOSEL.DCLRM, and PIPEnCTR.ACLRM bit in the port control register.

Table 28.16 List of Buffer Clearing Methods

FIFO Buffer Clearing Mode	Clearing Buffer Memory on CPU Side	Mode for Automatically Clearing Buffer Memory after Reading Specified Pipe Data	Auto Buffer Clear Mode for Discarding All Received Packets
Register used	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Bit used	BCLR	DCLRM	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid	1: Mode valid 0: Mode invalid

(1) Auto Buffer Clear Mode Function

With the USB, all received data packets are discarded if the PIPEnCTR.ACLRM bit is set to 1. If a correct data packet has been received, the ACK response is returned to the host controller. The auto buffer clear mode function can be set only in the buffer memory reading direction.

If the ACLRM bit is set to 1 and then to 0, the buffer memory of the selected pipe can be cleared regardless of the access direction.

An access cycle of at least 100 ns is required for the internal hardware sequence processing time between ACLRM = 1 and ACLRM = 0.

(2) Buffer Memory Specifications (Single or Double Setting)

Either a single or double buffer configuration can be selected for PIPE1 to PIPE5, using the PIPECFG.DBLB bit.

28.3.5.3 FIFO Port Functions

Table 28.17 shows the settings for the FIFO port functions of the USB. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, the BVAL bit in the port control register should be set to end writing. To send a zero-length packet, the BCLR bit in the register should be used to clear the buffer and then the BVAL bit set in order to end writing.
In reading, reception of new packets is automatically enabled when all data has been read. Data cannot be read when a zero-length packet has been received (the DTLN[8:0] bits = 0), so the BCLR bit in the register should be used to clear the buffer. The length of the receive data can be confirmed using the DTLN[8:0] bits in the port control register.

Table 28.17 FIFO Port Function Settings

Register Name	Bit Name	Description
CFIFOSEL, DnFIFOSEL (n = 0 or 1)	RCNT	Selects DTLN read mode.
	REW	Buffer memory rewind (re-read, rewrite).
	DCLRM	Automatically clears receive data for a specified pipe after the data has been read (only for DnFIFO).
	DREQE	Enables DMA/DTC transfers (only for DnFIFO).
	MBW	FIFO port access bit width.
	BIGEND	Selects FIFO port endian.
	ISEL	FIFO port access direction (only for DCP).
	CURPIPE	Selects the current pipe.
CFIFOCTR, DnFIFOCTR (n = 0 or 1)	BVAL	Ends writing to the buffer memory.
	BCLR	Clears the buffer memory on the CPU side.
	DTLN	Checks the length of receive data.

(1) FIFO Port Selection

Table 28.18 shows the pipes that can be selected with the various FIFO ports. The pipe to be accessed should be selected using the CURPIPE[3:0] bits in the port select register. After the pipe is selected, whether the written value can be correctly read from the CURPIPE[3:0] bits should be checked. (If the previous pipe number is read, it indicates that the pipe modification is being executed by the USB controller.) Then, the FRDY bit in a port control register = 1 is checked.
In addition, the bus width to be accessed should be selected using the MBW bit in the port select register. The buffer memory access direction conforms to the PIPECFG.DIR bit. Only for the DCP, the ISEL bit in the port select register determines the direction.

Table 28.18 FIFO Port Access Categorized by Pipe

Pipe	Access Method	Port that can be Used
DCP	CPU access	CFIFO port register
PIPE1 to PIPE9	CPU access	CFIFO port register D0FIFO/D1FIFO port register
	DMA/DTC access	D0FIFO/D1FIFO port register

(2) REW Bit

It is possible to temporarily stop access to the pipe currently being accessed, access a different pipe, and then continue processing for the current pipe again. The REW bit in the port select register is used for this processing.
If a pipe is selected through the CURPIPE[3:0] bits in the port select register with the REW bit set to 1, after confirming that the FRDY bit has been set to 1, the pointer used for reading from and writing to the buffer memory is reset, and reading or writing can be carried out from the first byte. If a pipe is selected with 0 set for the REW bit, data can be read and written in continuation from the previous selection, without the pointer being reset.
To access the FIFO port, the FRDY bit in the port control register = 1 should be checked after selecting a pipe.

28.3.5.4 DMA/DTC Transfers (D0FIFO and D1FIFO Ports)

(1) Overview of DMA/DTC Transfers

For PIPE1 to PIPE9, the FIFO port can be accessed using the DMAC. When accessing the buffer for the pipe targeted for DMA/DTC transfer is enabled, a DMA/DTC transfer request is issued.
The unit of transfer to the FIFO port should be selected using the DnFIFOSEL.MBW bit and the pipe targeted for the DMA/DTC transfer should be selected using the DnFIFOSEL.CURPIPE[3:0] bits. The selected pipe should not be changed during the DMA/DTC transfer.

(2) DnFIFO Auto Clear Mode (D0FIFO and D1FIFO Port Reading Direction)

If 1 is set in the DnFIFOSEL.DCLRM bit, the USB automatically clears the buffer memory of the selected pipe when reading of data from the buffer memory has been completed.
Table 28.19 shows the packet reception and buffer memory clearing processing by software for each of the various settings. As shown in Table 28.19, the buffer clearing conditions depend on the value set in the PIPECFG.BFRE bit.
Using the DnFIFOSEL.DCLRM bit eliminates the need for the buffer to be cleared by software in any situation that requires buffer clearing. This enables DMA/DTC transfers without involving software.
The DnFIFO auto clear mode can be set only in the buffer memory reading direction.

Table 28.19 Packet Reception and Buffer Memory Clearing Processing by Software

Buffer Status When Packet is Received	Register Setting			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	Automatically cleared	Automatically cleared	Automatically cleared	Automatically cleared
Zero-length packet reception	Cleared by software	Cleared by software	Automatically cleared	Automatically cleared
Normal short packet reception	Automatically cleared	Cleared by software	Automatically cleared	Automatically cleared
Transaction count end	Automatically cleared	Cleared by software	Automatically cleared	Automatically cleared

28.3.6 Control Transfers (DCP)

In the data stage of control transfers, data is transferred using the default control pipe (DCP).
The DCP buffer memory is a 64-byte single buffer and is a fixed area that is shared for both control reading and control writing. The buffer memory can be accessed only through the CFIFO port.

28.3.6.1 Control Transfers when Host Controller Function is Selected

(1) Setup Stage

USBREQ, USBVAL, USBINDX, and USBLENG are the registers that are used to transmit a USB request for setup transactions. Writing setup packet data to the registers and writing 1 to the DCPCTR.SUREQ bit transmits the specified data for setup transactions. Upon completion of the transaction, the SUREQ bit is cleared to 0. The above USB request registers should not be modified while SUREQ = 1.
After the attached state of the connected function device is detected, the first setup transaction for the device should be issued by using the sequence described above with the DCPMAXP.DEVSEL[3:0] bits set to 0 and the DEVADD0.USBSPD[1:0] bits set appropriately.
After the connected function device is shifted to the Address state, setup transactions should be issued by using the sequence described above with the assigned USB address set in the DEVSEL[3:0] bits and the bits in DEVADDn corresponding to the specified USB address set appropriately. For example, when PIPEMAXP.DEVSEL[3:0] = 0x2, make appropriate settings in DEVADD2; when PIPEMAXP.DEVSEL[3:0] = 0x5, make appropriate settings in DEVADD5.
When the setup transaction data has been sent, an interrupt request is generated according to the response received from the peripheral device (SIGN1 or SACK bit in INTSTS1), by means of which the result of the setup transactions can be confirmed.
A data packet of DATA0 (USB request) is transmitted as the data packet for a setup transaction regardless of the setting of the SQMON bit in DCPCTR.

(2) Data Stage

Data is transferred using the DCP buffer memory.
The access direction of the DCP buffer memory should be specified using the CFIFOSEL.ISEL bit. The transfer direction should be specified using the DCPCFG.DIR bit.
For the first data packet of the data stage, the data PID should be transferred as DATA1. Set data PID = DATA1 in the DCPCTR.SQSET bit and the PID bits = BUF in DCPCFG. Completion of data transfer is detected using the BRDY or BEMP interrupt.
For control write transfers, when the number of data bytes to be sent is an integer multiple of the maximum packet size, software should control so as to send a zero-length packet at the end.

(3) Status Stage

Zero-length packet data is transferred in the direction opposite to that in the data stage. As in the data stage, data is transferred using the DCP buffer memory. Transactions are done in the same manner as the data stage.
For the data packets of the status stage, the data PID should be set to DATA1 using the DCPCTR.SQSET bit.
For reception of a zero-length packet, the received data length should be confirmed using the CFIFOCTR.DTLN[8:0] after a BRDY interrupt is generated, and the buffer memory should then be cleared using the CFIFOCTR.BCLR bit.

28.3.6.2 Control Transfers when Function Controller Function is Selected

(1) Setup Stage

The USB always sends an ACK response for a correct setup packet targeted to the USB. The operation of the USB in the setup stage is described below.
When receiving a new setup packet, the USB sets the following bits.

- Set the INTSTS0.VALID bit to 1.
- Set the DCPCTR.PID[1:0] bits to NAK.
- Set the DCPCTR.CCPL bit to 0.

When receiving a data packet right after the setup packet, the USB stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Response processing with respect to the control transfer should always be carried out after setting the VALID bit = 0. In the VALID bit = 1 state, PID = BUF cannot be set, and the data stage cannot be terminated.
Using the function of the VALID bit, the USB can suspend the current request processing when receiving a new USB request during a control transfer, and can send a response to the newest request.
In addition, the USB automatically detects the direction bit (bit 8 of bmRequestType) and the request data length (wLength) of the received USB request, distinguishes between control read transfer, control write transfer, and no-data control transfer, and controls stage transitions. For a wrong sequence, the sequence error of the control transfer stage transition interrupt is generated, and the software is notified of occurrence of the error. For the stage control of the USB, see Figure 28.11.

(2) Data Stage

Data transfers corresponding to received USB requests should be done using the DCP. Before accessing the DCP buffer memory, the access direction should be specified using the CFIFOSEL.ISEL bit.
If the transfer data is larger than the size of the DCP buffer memory, the data transfer should be carried out using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

(3) Status Stage

Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to BUF. After the above settings have been made, the USB automatically executes the status stage in accordance with the data transfer direction determined at the setup stage. The specific procedure is as follows.

- For control read transfers
  The USB receives a zero-length packet from the USB host and sends an ACK response.
- For control write transfers and no-data control transfers
  The USB transmits a zero-length packet and receives an ACK response from the USB host.

(4) Control Transfer Auto Response Function

The USB automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, a response from the software is necessary.

- bmRequestType is not 00h: Any transfer other than a control write transfer
- wIndex is not 00h: Request error
- wLength is not 00h: Any transfer other than a no-data control transfer
- wValue is larger than 7Fh: Request error
- The INTSTS0.DVSQ[2:0] bits are 011b (configured state): Control transfer of a device state error

For all requests other than the SET_ADDRESS request, a response is required from the corresponding software.

28.3.7 Bulk Transfers (PIPE1 to PIPE5)

The buffer memory usage (single/double buffer setting) can be selected for bulk transfers. The USB provides the following functions for bulk transfers.

- BRDY interrupt function (PIPECFG.BFRE bit: see section 28.3.3.1, (2) When the SOFCFG.BRDYM Bit = 0 and the PIPECFG.BFRE Bit = 1
- Transaction count function
  (PIPEnTRE.TRENB, TRCLR, and PIPEnTRN.TRNCNT[15:0] bits: see section 28.3.4.5, Transaction Counter (For PIPE1 to PIPE5 in Reading Direction)
- Response PID = NAK function (PIPECFG.SHTNAK bit: see section 28.3.4.8, Response PID = NAK Function
- Auto response mode (PIPEnCTR.ATREPM bit: see section 28.3.4.9, Auto Response Mode)

28.3.8 Interrupt Transfers (PIPE6 to PIPE9)

When the function controller function is selected, the USB carries out interrupt transfers in accordance with the timing controlled by the host controller.
When the host controller function is selected, the timing of issuing a token can be specified using the interval counter.

28.3.8.1 Interval Counter during Interrupt Transfers when Host Controller Function is Selected

For interrupt transfers, intervals between transactions are set in the PIPEPERI.IITV[2:0] bits. The USB controller issues interrupt transfer tokens based on the specified intervals.

(1) Counter Initialization

The interval counter is initialized when the MCU is reset or when the PIPEnCTR.ACLRM bit is set to 1. The PIPEPERI.IITV[2:0] bits are not initialized when the interval counter is initialized by using the ACLRM bit.
Note that the interval counter is not initialized in the following case.

- USB bus reset or USB suspended
  The IITV[2:0] bits are not initialized. Setting 1 to the UACT bit in DVSTCTR0 starts counting from the value before entering the USB bus reset state or USB suspended state.

(2) Operation when Transmission/Reception is Impossible at Token Issuance Timing

The USB cannot issue tokens even at token issuance timing in the following cases. In such a case, the USB attempts transactions at the subsequent interval.

- When the PID is set to NAK or STALL.
- When the buffer memory is full at the token sending timing in the receiving (IN) direction.
- When there is no data to be sent in the buffer memory at the token sending timing in the transmitting (OUT) direction.

28.3.9 Isochronous Transfers (PIPE1 and PIPE2)

The USB has the following functions for isochronous transfers.

- Notification of isochronous transfer error information
- Interval counter (specified by the PIPEPERI.IITV[2:0] bits)
- Isochronous IN transfer data setup control (see section 28.3.9.3, Interval Counter (4) Setup of Data to be Transmitted using Isochronous Transfer when Function Controller Function is Selected)
- Isochronous IN transfer buffer flush function (specified by the PIPEPERI.IFIS bit)

28.3.9.1 Error Detection in Isochronous Transfers

The USB has a function for detecting the error information described below, so that when errors occur in isochronous transfers, software can control them. Table 28.20 and Table 28.21 show the priority in which errors are confirmed and the interrupts generated corresponding to errors.

(a) PID errors

- If the PID of the received packet is illegal.

(b) CRC errors and bit stuffing errors

- If an error occurs in the CRC of the received packet or the bit stuffing is illegal.

(c) Maximum packet size exceeded

- The data of the received packet is larger than the specified maximum packet size.

(d) Overrun and underrun errors

- When host controller function is selected
  When the buffer memory is full at the token sending timing in the IN (receiving) direction.
  When there is no data to be sent in the buffer memory at the token sending timing in the OUT (transmitting) direction.
- When function controller function is selected
  When there is no data to be sent in the buffer memory at the token receiving timing in the IN (transmitting) direction.
  When the buffer memory is full at the token receiving timing in the OUT (receiving) direction.

(e) Interval errors

An interval error is generated on any of the following conditions when the function controller function is selected.

- During an isochronous IN transfer, an IN token could not be received in the interval frame.
- During an isochronous OUT transfer, an OUT token could not be received in frames other than the interval frame.

Table 28.20 Error Detection when a Token is Received

Detection Priority	Error	Generated Interrupt and Status
1	PID errors	No interrupts are generated in both cases when the host controller function is selected and the function controller function is selected (ignored as a corrupted packet).
2	CRC errors and bit stuffing errors	No interrupts generated in both cases when the host controller function is selected and the function controller function is selected (ignored as a corrupted packet).
3	Overrun and underrun errors	An NRDY interrupt is generated to set the FRMNUM.OVRN bit to 1 in both cases when host controller function is selected and function controller function is selected. When the function controller function is selected, a zero-length packet is transmitted in response to IN token. However, no data packets are received in response to OUT token.

Table 28.20 Error Detection when a Token is Received

Detection Priority	Error	Generated Interrupt and Status
4	Interval errors	An NRDY interrupt is generated when the function controller function is selected. It is not generated when the host controller function is selected.

Table 28.21 Error Detection when a Data Packet is Received

Detection Priority	Error	Generated Interrupt and Status
1	PID errors	No interrupts are generated (ignored as a corrupted packet).
2	CRC errors and bit stuffing errors	An NRDY interrupt is generated to set the FRMNUM.CRCE to 1 bit in both cases when the host controller function is selected and the function controller function is selected.
3	Maximum packet size exceeded errors	A BEMP interrupt is generated to set the PID[1:0] bits to STALL in both cases when the host controller function is selected and the function controller function is selected.

28.3.9.2 DATA-PID

When the function controller function is selected, the USB operates as follows in response to the received PID.
IN direction

- DATA0: Sent as data packet PID
- DATA1: Not sent
- DATA2: Not sent
- mDATA: Not sent

OUT direction

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Packets are ignored
- mDATA: Packets are ignored

28.3.9.3 Interval Counter

The isochronous transfer interval can be set using the PIPEPERI.IITV[2:0] bits. The interval counter enables the functions shown in Table 28.22 when the function controller function is selected. When the host controller function is selected, the USB generates the token issuance timing. When the host controller function is selected, the interval counter operation is the same as that in the interrupt transfer.

Table 28.22 Interval Counter Function when the Function Controller Function is Selected

Transfer Direction	Function	Conditions for Detection
IN	Flushes transmit buffer	When an IN token cannot be successfully received in the interval frame during an isochronous IN transfer
OUT	Notifies that a token not being received	When an OUT token cannot be successfully received in the interval frame during an isochronous OUT transfer

The interval count is carried out when an SOF is received or for interpolated SOFs, so the isochronism can be maintained even if an SOF is damaged. The frame interval that can be set is the $2^{IITV[2:0]}$ frames.

(1) Counter Initialization when Function Controller Function is Selected

The interval counter is initialized when the MCU is reset or when the PIPEnCTR.ACLRM bit is set to 1. The PIPEPERI.IITV[2:0] bits are not initialized when the interval counter is initialized by using the ACLRM bit.
After the interval counter has been initialized, counting is started under either of the following conditions 1 and 2 when a packet has been transferred successfully.

1. An SOF is received after transmission of data in response to an IN token in the PID = BUF state.
2. An SOF is received after reception of data of an OUT token in the PID = BUF state.

Note that the interval counter is not initialized under the following conditions.

- When the PID[1:0] bits are set to NAK or STALL
  The interval timer does not stop. The USB attempts transactions at the subsequent interval.
- When the USB bus is reset or USB is suspended
  The IITV[2:0] bits are not initialized. When an SOF has been received, counting is restarted from the value prior to the reception of the SOF.

(2) Interval Counting and Transfer Control when Host Controller Function is Selected

The USB controls the interval between token issuance operations based on the PIPEPERI.IITV[2:0] bit settings. Specifically, the USB issues a token for a selected pipe once every $2^{IITV[2:0]}$ frames.
The USB starts counting the token issuance interval at the frame following the frame in which software has set the PID bits to BUF.

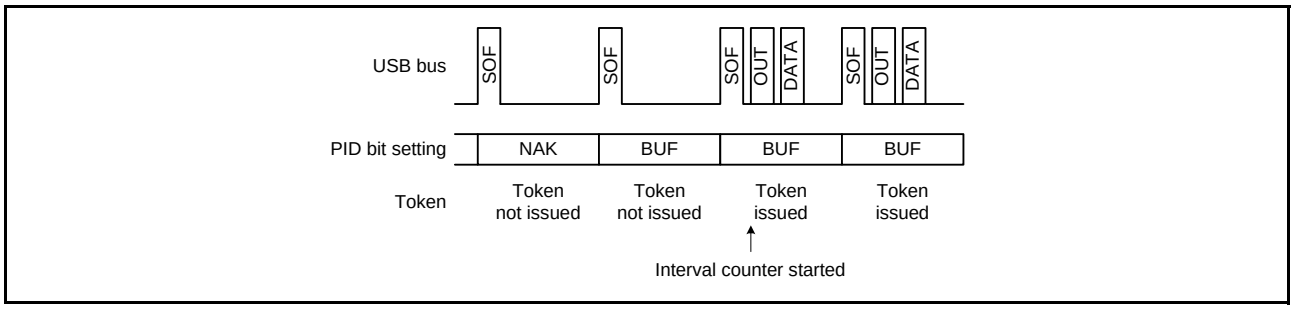


Figure 28.12 Token Issuance when IITV[2:0] = 0

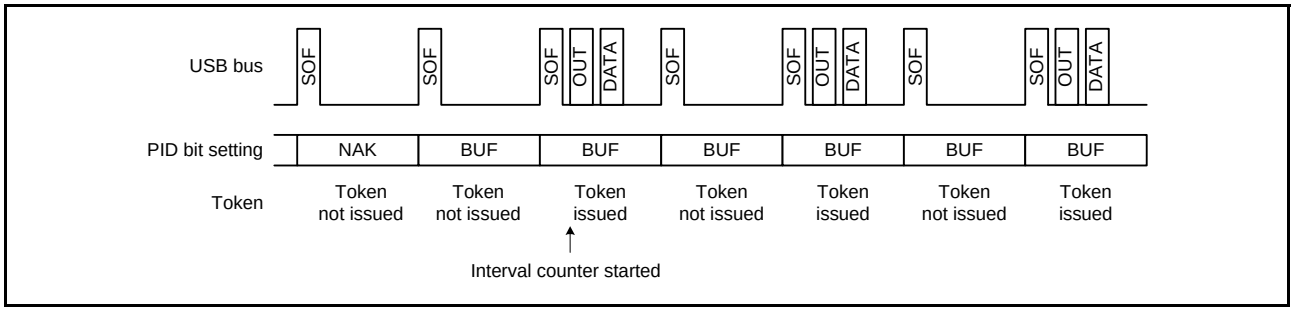


Figure 28.13 Token Issuance when IITV[2:0] = 1

When the selected pipe is set for isochronous transfers, the USB carries out the following operation in addition to controlling the token issuance interval. The USB issues a token even when the NRDY interrupt generation condition is satisfied.

(a) When the selected pipe is for isochronous IN transfers

The USB generates an NRDY interrupt when the USB issues an IN token but does not receive a packet successfully from a peripheral device (no response or packet error).
The USB sets the FRMNUM.OVRN bit to 1 generating an NRDY interrupt when the time to issue an IN token comes while the USB cannot receive data because the FIFO buffer is full (due to the fact that the CPU or the DMA/DTC transfer is too slow to read data from the FIFO buffer).

(b) When the selected pipe is for isochronous OUT transfers

The USB sets the OVRN bit to 1 generating an NRDY interrupt and transmitting a zero-length packet when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer (because the CPU or the DMA/DTC transfer is too slow to write data to the FIFO buffer).
The token issuance interval is reset on any of the following conditions.

- When the USB is reset through a reset pin
  (The IITV[2:0] bits are also cleared to 0).
- When software sets the PIPEnCTR.ACLRM bit to 1

(3) Interval Counting and Transfer Control when Function Controller Function is Selected

(a) When the selected pipe is for isochronous OUT transfers

The USB generates an NRDY interrupt when the USB fails to receive a data packet within the interval set by the PIPEPERI.IITV[2:0] bits.
The USB also generates an NRDY interrupt when the USB fails to receive data because of a CRC error or other errors contained in the data packet or because of the FIFO buffer being full.
The NRDY interrupt is generated at the timing of SOF packet reception. Even if the SOF packet is corrupted, the internal recovery allows the interrupt to be generated at the timing to receive the SOF packet.
However, when the IITV[2:0] bits is set to a value other than 0, the USB generates an NRDY interrupt on receiving an SOF packet for every interval after starting interval counting operation.
When the PID[1:0] bits are set to NAK by software after starting the interval timer, the USB does not generate an NRDY interrupt on receiving an SOF packet.
The timing to start interval counting depends on the setting of IITV[2:0] bits as shown below.

- When the IITV[2:0] = 0: The interval counting starts when software has set the PID[1:0] bits for the selected pipe to BUF.

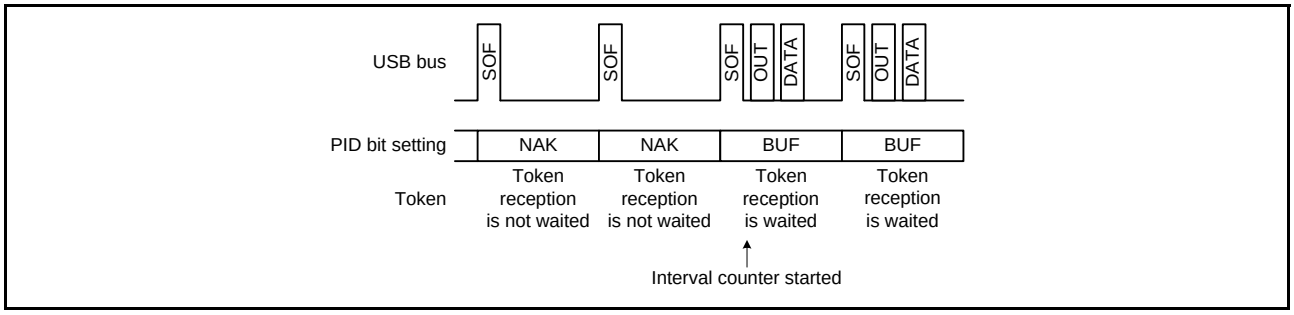


Figure 28.14 Relationship between Frames and Expected Token Reception when the IITV[2:0] = 0

- When the IITV[2:0] ≠ 0: The interval counting starts on completion of successful reception of the first data packet after the PID[1:0] bits for the selected pipe have been modified to BUF.

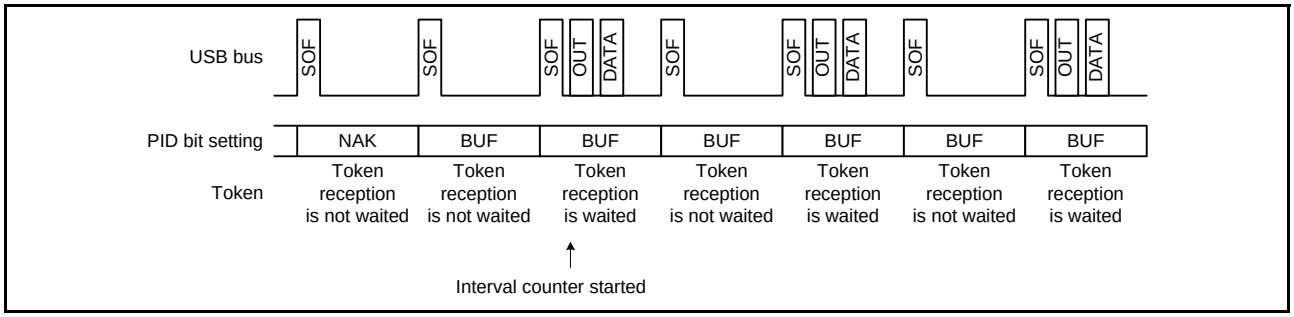


Figure 28.15 Relationship between Frames and Expected Token Reception when the IITV[2:0] ≠ 0

(b) When the selected pipe is for isochronous IN transfers

The PIPEPERI.IFIS bit should be 1 for this use. When IFIS = 0, the USB transmits a data packet in response to the received IN token irrespective of the setting of the PIPEPERI.IITV[2:0] bits.
When IFIS = 1, the USB clears the FIFO buffer when the USB fails to receive an IN token in the frame at the interval set by the IITV[2:0] bits while there is data to be transmitted in the FIFO buffer.
The USB also clears the FIFO buffer when the USB fails to receive an IN token successfully because of a bus error such as a CRC error contained in the IN token.
The FIFO buffer is cleared at the timing of SOF packet reception. Even if the SOF packet is corrupted, the internal recovery allows the FIFO buffer to be cleared at the timing to receive the SOF packet.

The timing to start interval counting depends on the setting of the IITV[2:0] bits (similar to the timing during OUT transfers).
The interval is counted on any of the following conditions in function controller mode.

- When a hardware-reset is applied to the USB (here, the IITV[2:0] bits are also cleared to 000b).
- When software sets the PIPEnCTR.ACLRM bit to 1.
- When the USB detects a USB bus reset.

(4) Setup of Data to be Transmitted using Isochronous Transfer when Function Controller Function is Selected

With isochronous data transmission using the USB in function controller function, after data has been written to the buffer memory, a data packet can be transmitted with the next frame after the frame in which an SOF packet is detected. This function is called the isochronous transfer transmission data setup function, and it makes it possible to designate the frame from which transmission began.

In a double buffer configuration, even after the writing of data to both buffers has been completed, transmission will be enabled for only one buffer to which data writing was completed first. Accordingly, even if multiple IN tokens are received, only one packet of data is transmitted from a single buffer.

When an IN token is received, if the buffer memory is in the transmission enabled state, the USB transmits data as a normal response. If the buffer memory is not in the transmission enabled state, however, a zero-length packet is sent and an underrun error occurs.

Figure 28.16 shows an example of transmission using the isochronous transfer transmission data setup function with the USB when IITV[2:0] = 000b (every frame) has been set.

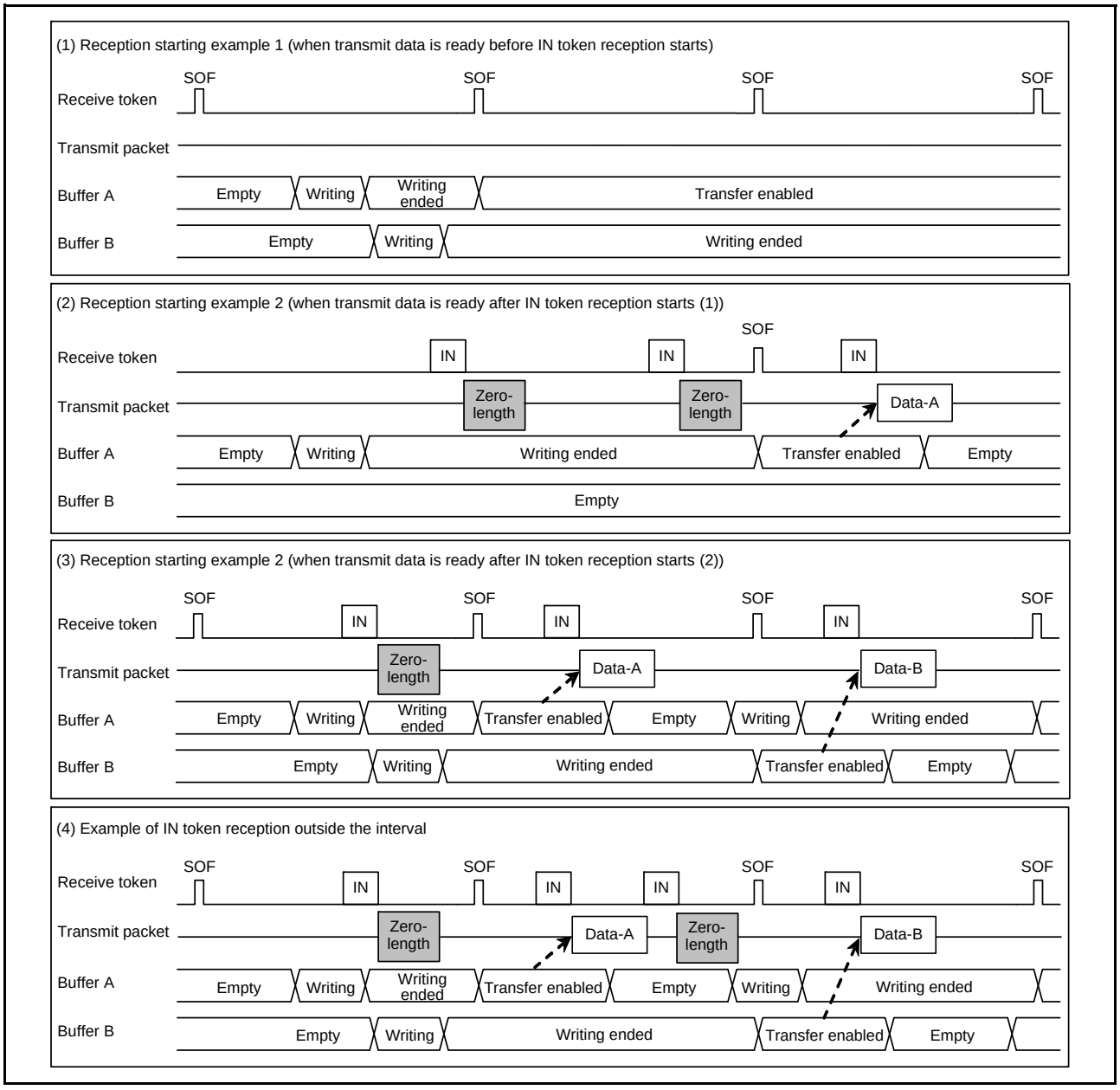


Figure 28.16 Example of Data Setup Function Operation

(5) Isochronous Transfer Transmission Buffer Flush when Function Controller Function is Selected

If an SOF packet of the next frame is received without receiving an IN token in an interval frame during isochronous data transmission, the USB operates as if an IN token had been corrupted, and clears the buffer for which transmission is enabled, putting that buffer in the writing enabled state.
If a double buffer configuration is used and writing to both buffers has been completed, the buffer memory that was cleared is assumed as the data having been sent in the interval frame, and transmission is enabled for the buffer memory that is not cleared with SOF packet reception.
The timing of the buffer flush function depends on the setting of the PIPEPERI.IITV[2:0] bits.

- When the IITV[2:0] = 0
  The buffer flush operation starts from the next frame after the pipe becomes valid.
- When the IITV[2:0] ≠ 0
  The buffer flush operation is carried out after the first successful transaction.

Figure 28.17 shows an example of the buffer flush function in the USB. When an unanticipated token is received before the interval frame, the USB sends the write data or a zero-length packet as an underrun error according to the data setup state.

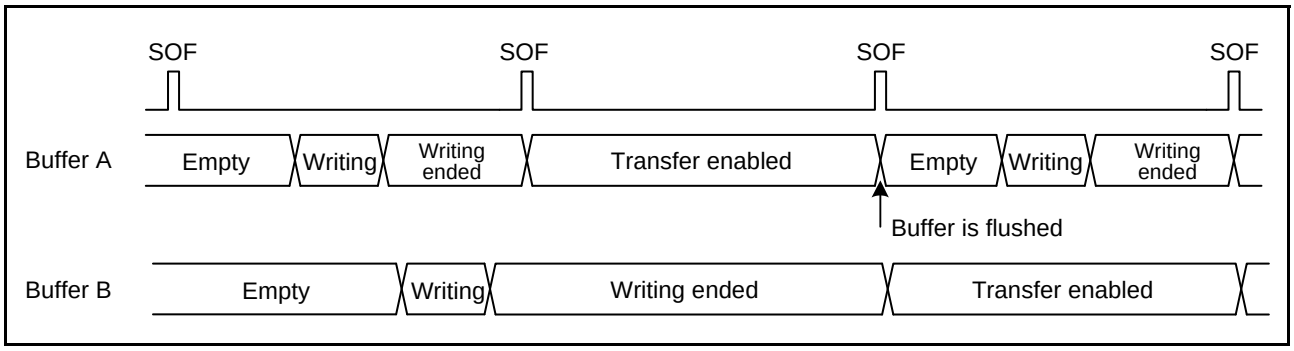


Figure 28.17 Example of Buffer Flush Operation

Figure 28.18 shows an example of interval error occurrence in the USB. There are five types of interval errors, as shown below. The interval error is generated at the timing indicated by (1) in the figure, and the buffer flush function is activated.

If an interval error occurs during an IN transfers, the buffer flush function is activated; if it occurs during an OUT transfer, an NRDY interrupt is generated.
The FRMNUM.OVRN bit should be used to distinguish between NRDY interrupts such as received packet errors and overrun errors.
In response to tokens that are shaded in the figure, responses are sent according to the buffer memory status.
IN direction

- If the buffer is in the transmission enabled state, the data is transferred as a normal response.
- If the buffer is in the transmission disabled state, a zero-length packet is sent and an underrun error occurs.

OUT direction

- If the buffer is in the reception enabled state, the data is received as a normal response.
- If the buffer is in the reception disabled state, the data is discarded and an overrun error occurs.

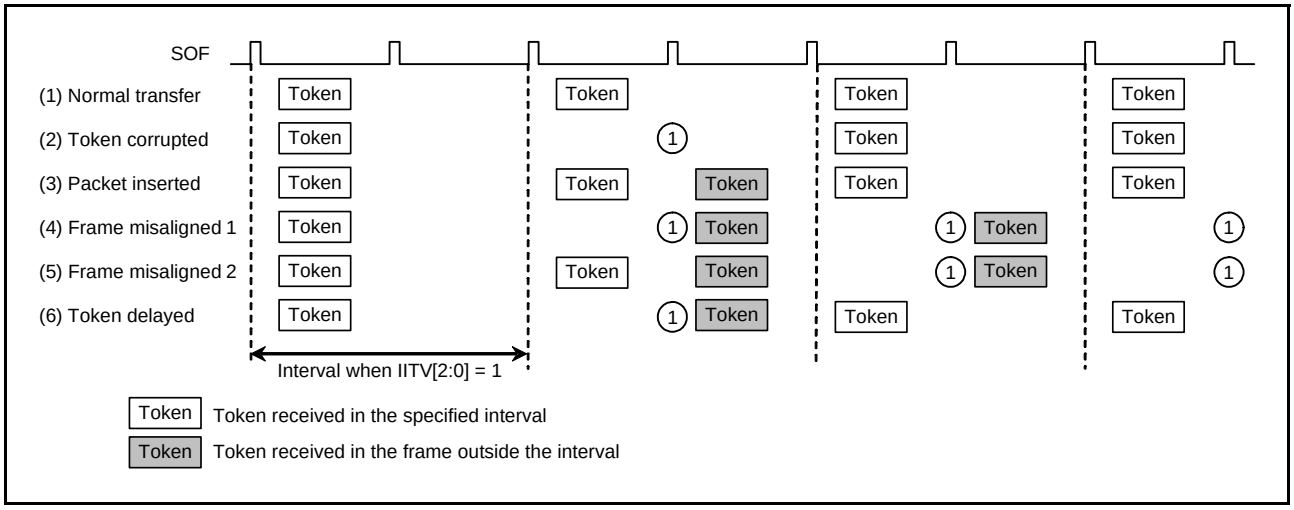


Figure 28.18 Example of Interval Error Occurrence when the IITV[2:0] = 1

28.3.10 SOF Recovery Function

When the function controller function is selected and if data could not be received at intervals of 1 ms because an SOF packet was corrupted or missing, the USB recovers the SOF. The SOF recovery operation begins when the USBE and SCKE bits in SYSCFG have been set to 1 and an SOF packet is received. The recovery function is initialized under the following conditions.

- MCU reset
- USB bus reset
- Suspended state detected

The SOF recovery operates as follows.

- The recovery function is not activated until an SOF packet is received.
- After the first SOF packet is received, recovery is carried out by counting 1 ms with an internal clock of 48 MHz.
- After the second and subsequent SOF packets are received, recovery is carried out at the previous reception interval.
- Recovery is not carried out in the suspended state or while a USB bus reset is being received.

The USB supports the following functions based on the SOF packet reception. These functions also operate normally with SOF recovery, if the SOF packet was missing.

- Updating of the frame number
- SOFR recovery timing
- Isochronous transfer interval count

If an SOF packet is missing when full-speed operation is being used, the FRMNUM.FRNM[10:0] bits are not updated.

28.3.11 Pipe Schedule

28.3.11.1 Conditions for Generating a Transaction

When the host controller function is selected and the DVSTCTR0.UACT bit has been set to 1, the USB generates a transaction under the conditions shown in Table 28.23.

Table 28.23 Conditions for Generating a Transaction

	Conditions for Generation				
Transaction	**DIR**	**PID**	**IITV[2:0]**	**Buffer State**	**SUREQ**
Setup	—*1	—*1	—*1	—*1	1 setting
Control transfer data stage, status stage, bulk transfer	IN	BUF	Invalid	Receive area exists	—*1
	OUT	BUF	Invalid	Transmit data exists	—*1
Interrupt transfer	IN	BUF	Valid	Receive area exists	—*1
	OUT	BUF	Valid	Transmit data exists	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. Symbols (—) in the table indicate that the condition is unrelated to the generating of tokens. “Valid” indicates that, for interrupt transfers and isochronous transfers, a transaction is generated only in transfer frames that are based on the interval counter. “Invalid” indicates that a transaction is generated regardless of the interval counter.
Note 2. This indicates that a transaction is generated regardless of whether there is a receive area. If there is no receive area, however, the received data is discarded.
Note 3. This indicates that a transaction is generated regardless of whether there is any data to be transmitted. If there is no data to be transmitted, however, a zero-length packet is transmitted.

28.3.11.2 Transfer Schedule

This section describes the transfer scheduling within a frame of the USB. After the USB sends an SOF, the transfer is carried out in the sequence described below.

1. Execution of periodic transfers
   A pipe is searched in the order of PIPE1 PIPE2 PIPE6 PIPE7 PIPE8 PIPE9, and then, if there is a pipe for which an isochronous or interrupt transfer transaction can be generated, the transaction is generated.
2. Setup transactions for control transfers
   The DCP is checked, and if a setup transaction is possible, it is sent.
3. Execution of bulk transfers, control transfer data stages, and control transfer status stages
   A pipe is searched in the order of DCP PIPE1 PIPE2 PIPE3 PIPE4 PIPE5, and then, if there is a pipe for which a transaction for a bulk transfer, a control transfer data stage, or a control transfer status stage can be generated, the transaction is generated.
   When a transaction is generated, processing moves to the next pipe transaction regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, step 3 is repeated.

28.3.11.3 Enabling USB Communication

Setting the DVSTCTR0.UACT bit to 1 initiates SOF transmission and transaction generation is enabled.
Setting the UACT bit to 0 stops SOF transmission and a suspend state is entered. If the setting of the UACT bit is changed from 1 to 0, processing stops after the next SOF is sent.

28.4 Usage Notes

28.4.1 Setting the Module-Stop Function

Operation of the USB module can be prohibited or permitted by a bit in module-stop control register B (MSTPCRB). The setting after a reset is for operation of the USB module to be stopped. The USB module is stopped at the initial value. The registers are made accessible by release from the module-stop state. For details, see section 12, Low Power Consumption.

29. Serial Communications Interface (SCIc, SCId)

This MCU has five independent serial communications interface (SCI) channels. The SCI is configured as SCIc module (SCI0 to SCI3) and SCId module (SCI12).
The SCIc (SCI0 to SCI3) can handle both asynchronous and clock synchronous serial communications.
Asynchronous serial data communications can be carried out with standard asynchronous communications chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communications Interface Adapter (ACIA).
As an extended function in asynchronous communications mode, the SCI also supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards). Single-master operation as an simple I^2C bus interface and simple SPI interfaces are also supported.
As well as the functions of the SCIc module, the SCId module (SCI12) supports an extended serial protocol with a structure formed from Start Frames and Information Frames.

29.1 Overview

Table 29.1 lists the specifications of the SCIc module, Table 29.2 lists the specifications of the SCId module, and Table 29.3 lists the specifications of the individual SCI channels.
Figure 29.1 is a block SCI0 to SCI3. Figure 29.2 is a block diagram of SCI12 (SCId).

Table 29.1 Specifications of SCIc (1/2)

Item		Specifications
Serial communications mode		• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable with on-chip baud rate generator.
Full-duplex communications		Transmitter: Enables continuous transmission by double-buffering. Receiver: Enables continuous reception by double-buffering.
I/O pins		See Table 29.4 to Table 29.6.
Data transfer		Selectable as LSB-first or MSB-first transfer*1
Interrupt sources		Transmit-end, transmit-data-empty, receive-data-full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Power consumption reduction function		Module-stop state can be set for each channel.
Asynchronous mode	Data length	7 or 8 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even, odd, or none
	Receive error detection	Parity, overrun, and framing errors
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.
	Break detection	Break can be detected by reading RXDn pin level directly in case of a framing error
	Clock source	Selectable from internal or external clock Enables transfer rate clock input from MTU3*2
	Multi-processor communications function	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun errors
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.

Table 29.1 Specifications of SCIc (2/2)

Item		Specifications
Smart card interface mode	Error processing	An error signal can be automatically transmitted on detection of a parity error during reception
		Data can be automatically re-transmitted on receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	I^2C bus format
	Operating mode	Master (single-master operation only)
	Transfer rate	Fast mode is supported (see section 29.2.9, Bit Rate Register (BRR) for details on setting the transfer rate).
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI bus	Data length	Eight bits
	Detection of errors	Overrun errors
	SS input pin function	Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock sense are selectable.

Note 1. In simple I^2C mode, only MSB-first is available.
Note 2. Not supported for 64-and 48-pin products.

Table 29.2 Specifications of SCId (1/2)

Item		Specifications
Serial communications mode		• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable with on-chip baud rate generator.
Full-duplex communications		Transmitter: Enables continuous transmission by double-buffering. Receiver: Enables continuous reception by double-buffering.
Input/output pins		See Table 29.4 to Table 29.7.
Data transfer		Selectable as LSB-first or MSB-first transfer*1
Interrupt sources		Transmit-end, transmit-data-empty, receive-data-full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Power consumption reduction function		Module-stop state can be set.
Asynchronous mode	Data length	7 or 8 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even, odd, or none
	Receive error detection	Parity, overrun, and framing errors
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.
	Break detection	Break can be detected by reading RXDn pin level directly in case of a framing error
	Clock source	Selectable from internal or external clock Enables transfer rate clock input from MTU3*2
	Multi-processor communications function	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun errors
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.

Table 29.2 Specifications of SCId (2/2)

Item		Specifications
Smart card interface mode	Error processing	An error signal can be automatically transmitted on detection of a parity error during reception
		Data can be automatically re-transmitted on receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.
Simple I2C mode	Transfer format	I2C bus format
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 384 kbps
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI bus	Data length	8 bits
	Detection of errors	Overrun errors
	SS input pin function	Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock sense are selectable.
Extended serial mode	Start Frame transmission	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection
	Start Frame reception	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field • Function for measuring bit rates
	I/O control function	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed though to SCIc when the extended serial mode control section is off.
	Timer function	• Usable as a reloading timer

Note 1. In simple I2C mode, only MSB-first is available.
Note 2. Not supported for 64-and 48-pin products.

Table 29.3 List of Functions of SCI Channels

Item	SCI0 to SCI3	SCI12
Asynchronous mode	○	○
Clock synchronous mode	○	○
Smart card interface mode	○	○
Simple I2C mode	○	○
Simple SPI bus	○	○
Extended serial mode	—	○
MTU3 clock input*1	○	○

Note 1. Not supported for 64-and 48-pin products.

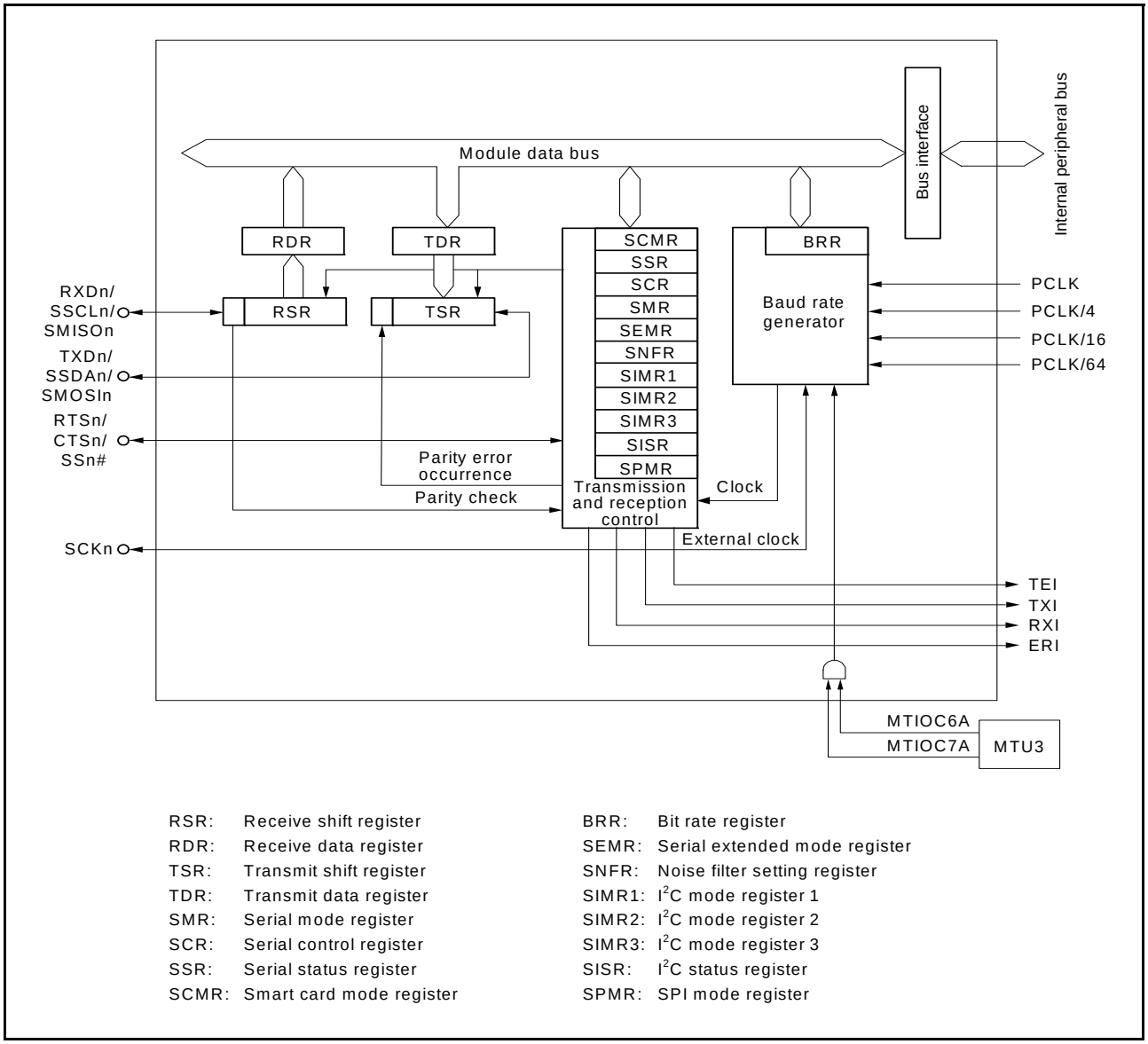


Figure 29.1 Block Diagram of SCI0 to SCI3

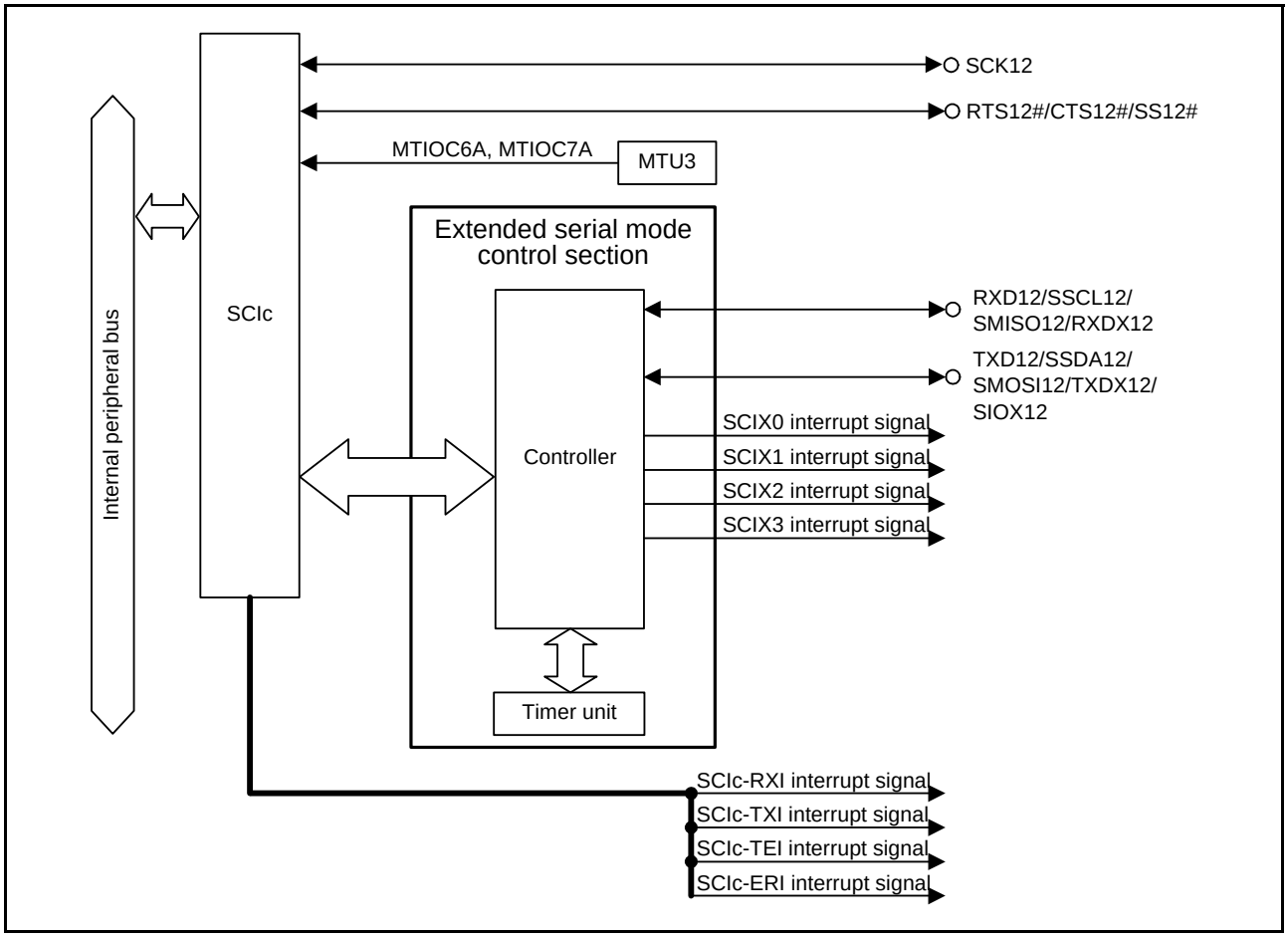


Figure 29.2 Block Diagram of SCI12 (SCId)

Table 29.4 to Table 29.7 list the pin configuration of the SCIs for the individual modes.

Table 29.4 Input and Output Pins of the SCIs (Asynchronous/Clock Synchronous Modes) (1/2)

Channel	Pin Name	I/O	Function
SCI0	SCK0	I/O	SCI0 clock input/output
	RXD0	Input	SCI0 receive data input
	TXD0	Output	SCI0 transmit data output
	CTS0#/RTS0#	I/O	SCI0 transfer start control input/output
SCI1	SCK1	I/O	SCI1 clock input/output
	RXD1	Input	SCI1 receive data input
	TXD1	Output	SCI1 transmit data output
	CTS1#/RTS1#	I/O	SCI1 transfer start control input/output
SCI2	SCK2	I/O	SCI2 clock input/output
	RXD2	Input	SCI2 receive data input
	TXD2	Output	SCI2 transmit data output
	CTS2#/RTS2#	I/O	SCI2 transfer start control input/output
SCI3	SCK3	I/O	SCI3 clock input/output
	RXD3	Input	SCI3 receive data input
	TXD3	Output	SCI3 transmit data output
	CTS3#/RTS3#	I/O	SCI3 transfer start control input/output

Table 29.4 Input and Output Pins of the SCIs (Asynchronous/Clock Synchronous Modes) (2/2)

Channel	Pin Name	I/O	Function
SCI12	SCK12	I/O	SCI12 clock input/output
	RXD12	Input	SCI12 receive data input
	TXD12	Output	SCI12 transmit data output
	CTS12#/RTS12#	I/O	SCI12 transfer start control input/output

Table 29.5 Pin Configuration of SCI (Simple I^2C Mode)

Channel	Pin Name	I/O	Function
SCI0	SSCL0	I/O	SCI0 I^2C clock input/output
	SSDA0	I/O	SCI0 I^2C data input/output
SCI1	SSCL1	I/O	SCI1 I^2C clock input/output
	SSDA1	I/O	SCI1 I^2C data input/output
SCI2	SSCL2	I/O	SCI2 I^2C clock input/output
	SSDA2	I/O	SCI2 I^2C data input/output
SCI3	SSCL3	I/O	SCI3 I^2C clock input/output
	SSDA3	I/O	SCI3 I^2C data input/output
SCI12	SSCL12	I/O	SCI12 I^2C clock input/output
	SSDA12	I/O	SCI12 I^2C data input/output

Table 29.6 Pin Configuration of SCI (Simple SPI Mode)

Channel	Pin Name	I/O	Function
SCI0	SCK0	I/O	SCI0 clock input/output
	SMISO0	I/O	SCI0 slave transmit data input/output
	SMOSI0	I/O	SCI0 master transmit data input/output
	SS0#	Input	SCI0 chip select input
SCI1	SCK1	I/O	SCI1 clock input/output
	SMISO1	I/O	SCI1 slave transmit data input/output
	SMOSI1	I/O	SCI1 master transmit data input/output
	SS1#	Input	SCI1 chip select input
SCI2	SCK2	I/O	SCI2 clock input/output
	SMISO2	I/O	SCI2 slave transmit data input/output
	SMOSI2	I/O	SCI2 master transmit data input/output
	SS2#	Input	SCI2 chip select input
SCI3	SCK3	I/O	SCI3 clock input/output
	SMISO3	I/O	SCI3 slave transmit data input/output
	SMOSI3	I/O	SCI3 master transmit data input/output
	SS3#	Input	SCI3 chip select input
SCI12	SCK12	I/O	SCI12 clock input/output
	SMISO12	I/O	SCI12 slave transmit data input/output
	SMOSI12	I/O	SCI12 master transmit data input/output
	SS12#	Input	SCI12 chip select input

Table 29.7 Pin Configuration of SCI (Extended Serial Mode)

Channel	Pin Name	I/O	Function
SCI12	RXDX12	Input	SCI12 receive data input
	TXDX12	Output	SCI12 transmit data output
	SIOX12	I/O	SCI12 transfer data input/output

29.2 Register Descriptions

29.2.1 Receive Shift Register (RSR)

RSR is a shift register which is used to receive serial data input from the RXDn pin and converts it into parallel data. When one frame of data has been received, it is transferred to RDR automatically.
RSR cannot be directly accessed by the CPU.

29.2.2 Receive Data Register (RDR)

Address(es): SCI0.RDR 0008 A005h, SCI1.RDR 0008 A025h, SCI2.RDR 0008 A045h, SCI3.RDR 0008 A065h, SCI12.RDR 0008 B305h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores receive data.
When the SCI has received one frame of serial data, it transfers the received serial data from RSR to RDR where it is stored. This allows RSR to receive the next data.
Since RSR and RDR function as a double buffer in this way, continuous receive operations can be performed.
Read RDR only once after a receive data full interrupt (RXI) has occurred. Note that if next one frame of data is received before reading receive data from RDR, an overrun error occurs.
RDR cannot be written to by the CPU.

29.2.3 Transmit Data Register (TDR)

Address(es): SCI0.TDR 0008 A003h, SCI1.TDR 0008 A023h, SCI2.TDR 0008 A043h, SCI3.TDR 0008 A063h, SCI12.TDR 0008 B303h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

TDR is an 8-bit register that stores transmit data.
When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission.
The double-buffered structures of TDR and TSR enable continuous serial transmission. If the next transmit data has already been written to TDR when one frame of data is transmitted, the SCI transfers the written data to TSR to continue transmission.
The CPU is able to read from or write to TDR at any time. Only write data for transmission to TDR once after each instance of the transmit data empty interrupt (TXI).

29.2.4 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data.

To perform serial data transmission, the SCI first automatically transfers transmit data from TDR to TSR, and then sends the data to the TXDn pin.

TSR cannot be directly accessed by the CPU.

29.2.5 Serial Mode Register (SMR)

Note: • Some bits in SMR have different functions in serial communications interface mode and smart card interface mode.

(1) Serial Communications Interface Mode (SMIF in SCMR = 0)

Address(es): SCI0.SMR 0008 A000h, SCI1.SMR 0008 A020h, SCI2.SMR 0008 A040h, SCI3.SMR 0008 A060h, SCI12.SMR 0008 B300h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*4
b2	MP	Multi-Processor Mode	(Valid only in asynchronous mode) 0: Multi-processor communications function is disabled 1: Multi-processor communications function is enabled	R/W*4
b3	STOP	Stop Bit Length	(Valid only in asynchronous mode) 0: 1 stop bit 1: 2 stop bits	R/W*4
b4	PM	Parity Mode	(Valid only when the PE bit is 1 in asynchronous mode) 0: Selects even parity 1: Selects odd parity	R/W*4
b5	PE	Parity Enable	(Valid only in asynchronous mode) • When transmitting 0: Parity bit addition is not performed 1: The parity bit is added • When receiving 0: Parity bit checking is not performed 1: The parity bit is checked	R/W*4
b6	CHR	Character Length	(Valid only in asynchronous mode) 0: Selects 8 bits as the data length*2 1: Selects 7 bits as the data length*3	R/W*4
b7	CM	Communications Mode	0: Asynchronous mode 1: Clock synchronous mode	R/W*4

Note 1. n is the decimal notation of the value of n in BRR (see section 29.2.9, Bit Rate Register (BRR)).
Note 2. In clock synchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB (bit 7) in TDR is not transmitted in transmission.
Note 4. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

CKS[1:0] Bits (Clock Select)

These bits select the clock source for the on-chip baud rate generator.

For the relation between the settings of these bits and the baud rate, see section 29.2.9, Bit Rate Register (BRR).

MP Bit (Multi-Processor Mode)

Disables/enables the multi-processor communications function. The settings of the PE bit and PM bit are invalid in multi-processor mode.

STOP Bit (Stop Bit Length)

Selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM Bit (Parity Mode)

Selects the parity mode (even or odd) for transmission and reception.

The setting of the PM bit is invalid in multi-processor mode.

PE Bit (Parity Enable)

When this bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception.

Irrespective of the setting of the PE bit, the parity bit is not added or checked in multi-processor format.

CHR Bit (Character Length)

Selects the data length for transmission and reception.

In clock synchronous mode, a fixed data length of 8 bits is used.

(2) Smart Card Interface Mode (SMIF in SCMR = 1)

Address(es): SCI0.SMR 0008 A000h, SCI1.SMR 0008 A020h, SCI2.SMR 0008 A040h, SCI3.SMR 0008 A060h, SCI12.SMR 0008 B300h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*3
b3, b2	BCP[1:0]	Base Clock Pulse	Selects the number of base clock cycles in combination with the BCP2 bit in SCMR. Setting values in BCP2 bit in SCMR and BCP[1:0] bits in SMR: BCP2 b3 b2 0 0 0: 93 clock cycles (S = 93)*2 0 0 1: 128 clock cycles (S = 128)*2 0 1 0: 186 clock cycles (S = 186)*2 0 1 1: 512 clock cycles (S = 512)*2 1 0 0: 32 clock cycles (S = 32)*2 (Initial value) 1 0 1: 64 clock cycles (S = 64)*2 1 1 0: 372 clock cycles (S = 372)*2 1 1 1: 256 clock cycles (S = 256)*2	R/W*3
b4	PM	Parity Mode	(Valid only when the PE bit is 1 in asynchronous mode) 0: Selects even parity 1: Selects odd parity	R/W*3
b5	PE	Parity Enable	When this bit is set to 1, a parity bit is added to data for transmission, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*3

Bit	Symbol	Bit Name	Description	R/W
b6	BLK	Block Transfer Mode	0: Normal mode operation 1: Block transfer mode operation	R/W*3
b7	GM	GSM Mode	0: Normal mode operation 1: GSM mode operation	R/W*3

Note 1. n is the decimal notation of the value of n in BRR (see section 29.2.9, Bit Rate Register (BRR)).
Note 2. S is the value of S in BRR (see section 29.2.9, Bit Rate Register (BRR)).
Note 3. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

CKS[1:0] Bits (Clock Select)

These bits select the clock source for the on-chip baud rate generator.
For the relationship between the settings of these bits and the baud rate, see section 29.2.9, Bit Rate Register (BRR).

BCP[1:0] Bits (Base Clock Pulse)

These bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode.
Set these bits in combination with the BCP2 bit in SCMR.
For details, see section 29.6.4, Receive Data Sampling Timing and Reception Margin.

PM Bit (Parity Mode)

Selects the parity mode for transmission and reception (even or odd).
For details on the usage of this bit in smart card interface mode, see section 29.6.2, Data Format (Except in Block Transfer Mode).

PE Bit (Parity Enable)

Set the PE bit to 1.
The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK Bit (Block Transfer Mode)

Setting this bit to 1 allows block transfer mode operation.
For details, see section 29.6.3, Block Transfer Mode.

GM Bit (GSM Mode)

Setting this bit to 1 allows GSM mode operation.
In GSM mode, the SSR.TEND flag set timing is put forward to 11.0 etu (elementary time unit = 1-bit transfer time) from the start and the clock output control function is appended. For details, see section 29.6.6, Serial Data Transmission (Except in Block Transfer Mode) and section 29.6.8, Clock Output Control.

29.2.6 Serial Control Register (SCR)

Note: • Some bits in SCR have different functions in serial communications interface mode and smart card interface mode.

(1) Serial Communications Interface Mode (SMIF in SCMR = 0)

Address(es): SCI0.SCR 0008 A002h, SCI1.SCR 0008 A022h, SCI2.SCR 0008 A042h, SCI3.SCR 0008 A062h, SCI12.SCR 0008 B302h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	(Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as I/O port. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock or MTU3 clock*3 • When an external clock is used, the clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. • The MTU3 clock can be used. The base clock to be input from MTU3 must be set to a frequency no greater than 1/4 that of PCLK. The SCKn pin functions as I/O port by setting the I/O port when MTU3 clock is in use. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	0: A TEI interrupt request is disabled 1: A TEI interrupt request is enabled	R/W
b3	MPIE	Multi-Processor Interrupt Enable	(Valid in asynchronous mode when SMR.MP = 1) 0: Normal reception 1: When the data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags ORER and FER in SSR to 1 is disabled. When the data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception is resumed.	R/W
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled	R/W*2
b6	RIE	Receive Interrupt Enable	0: RXI and ERI interrupt requests are disabled 1: RXI and ERI interrupt requests are enabled	R/W
b7	TIE	Transmit Interrupt Enable	0: A TXI interrupt request is disabled 1: A TXI interrupt request is enabled	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.

Note 2. A 1 can be written only when TE = 0 and RE = 0, while the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written in TE and RE. While the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.

Note 3. Only the input of an external clock is available for 64- and 48-pin products.

CKE[1:0] Bits (Clock Enable)

These bits select the clock source and SCKn pin function.
The combination of the settings of these bits and of the SEMR.ACS0 bit sets the internal MTU3 clock.

TEIE Bit (Transmit End Interrupt Enable)

Enables or disables a TEI interrupt request.
A TEI interrupt request is disabled by clearing the TEIE bit to 0.
In simple I^2C mode (when the IICM bit in SIMR1 is 1), the TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STI). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE Bit (Multi-Processor Interrupt Enable)

When this bit is set to 1 and the data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags ORER and FER in SSR to 1 is disabled. When the data with the multi-processor bit set to 1 is received, the MPIE is automatically cleared to 0, and normal reception is resumed. For details, see section 29.4, Multi-Processor Communications Function.
When the receive data includes the MPB bit is SSR set to 0, the receive data is not transferred from the RSR to the RDR, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.
When the receive data includes the MPB bit set to 1, the MPB bit is set to 1, the MPIE bit is automatically cleared to 0, the RXI and ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and setting the flags ORER and FER to 1 is enabled.
MPIE should be set to 0 if multi-processor communications function is not to be used.

RE Bit (Receive Enable)

Enables or disables serial reception.
When this bit is set to 1, serial reception is started by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Note that SMR should be set prior to setting the RE bit to 1 in order to designate the reception format.
Even if reception is halted by clearing the RE bit to 0, the ORER, FER, and PER flags in SSR are not affected and the previous value is retained.

TE Bit (Transmit Enable)

Enables or disables serial transmission.
When this bit is set to 1, serial transmission is started by writing transmit data to TDR. Note that SMR should be set prior to setting the TE bit to 1 in order to designate the transmission format.

RIE Bit (Receive Interrupt Enable)

Enables or disables RXI and ERI interrupt requests.
An RXI interrupt request is disabled by clearing the RIE bit to 0.
An ERI interrupt request can be cancelled by reading 1 from the ORER, FER, or PER flag in SSR and then clearing the flag to 0, or clearing the RIE bit to 0.

TIE Bit (Transmit Interrupt Enable)

Enables or disables notification of a TXI interrupt request.
Notification of a TXI interrupt request is disabled by clearing the TIE bit to 0.

(2) Smart Card Interface Mode (SMIF in SCMR = 1)

Address(es): SCI0.SCR 0008 A002h, SCI1.SCR 0008 A022h, SCI2.SCR 0008 A042h, SCI3.SCR 0008 A062h, SCI12.SCR 0008 B302h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• When GM in SMR = 0 b1 b0 0 0: Output disabled (The SCKn pin is available for use as an I/O port in accord with the I/O port settings.) 0 1: Clock output 1 x: (Setting prohibited) • When GM in SMR = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high	R/W*1
b2	TEIE	Transmit End Interrupt Enable	This bit should be 0 in smart card interface mode.	R/W
b3	MPIE	Multi-Processor Interrupt Enable	This bit should be 0 in smart card interface mode.	R/W
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled	R/W*2
b6	RIE	Receive Interrupt Enable	0: RXI and ERI interrupt requests are disabled 1: RXI and ERI interrupt requests are enabled	R/W
b7	TIE	Transmit Interrupt Enable	0: A TXI interrupt request is disabled 1: A TXI interrupt request is enabled	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.

Note 2. A 1 can be written only when TE = 0 and RE = 0, while the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written in TE and RE. While the SMR.CM bit is 0, writing is enabled under any condition.

For details on interrupt requests, see section 29.11, Interrupt Sources.

CKE[1:0] Bits (Clock Enable)

These bits control the clock output from the SCKn pin.

In GSM mode, clock output can be dynamically switched. For details, see section 29.6.8, Clock Output Control.

TEIE Bit (Transmit End Interrupt Enable)

This bit should be 0 in smart card interface mode.

MPIE Bit (Multi-Processor Interrupt Enable)

This bit should be 0 in smart card interface mode.

RE Bit (Receive Enable)

Enables or disables serial reception.

When this bit is set to 1, serial reception is started by detecting the start bit. Note that SMR should be set prior to setting the RE bit to 1 in order to designate the reception format.

Even if reception is halted by clearing the RE bit to 0, the ORER, FER, and PER flags in SSR are not affected and the

previous value is retained.

TE Bit (Transmit Enable)

Enables or disables serial transmission.
When this bit is set to 1, serial transmission is started by writing transmit data to TDR. Note that SMR should be set prior to setting the TE bit to 1 in order to designate the transmission format.

RIE Bit (Receive Interrupt Enable)

Enables or disables RXI and ERI interrupt requests.
An RXI interrupt request is disabled by clearing the RIE bit to 0.
An ERI interrupt request can be cancelled by reading 1 from the ORER, FER, or PER flag in SSR and then clearing the flag to 0, or clearing the RIE bit to 0.

TIE Bit (Transmit Interrupt Enable)

Enables or disables notification of a TXI interrupt request.
Notification of a TXI interrupt request is disabled by clearing the TIE bit to 0.

29.2.7 Serial Status Register (SSR)

Note: • Some bits in SSR have different functions in serial communications interface mode and smart card interface mode.

(1) Serial Communications Interface Mode (SMIF in SCMR = 0)

Address(es): SCI0.SSR 0008 A004h, SCI1.SSR 0008 A024h, SCI2.SSR 0008 A044h, SCI3.SSR 0008 A064h, SCI12.SSR 0008 B304h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Sets the multi-processor bit for adding to the transmission frame 0: Data are being transmitted. 1: The ID is being transmitted.	R/W
b1	MPB	Multi-Processor	Value of the multi-processor bit in the reception frame 0: Data are being transmitted. 1: The ID is being transmitted.	R
b2	TEND	Transmit End Flag	0: A character is being transmitted. 1: Character transfer has been completed.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error has occurred	R/(W) *1
b4	FER	Framing Error Flag	0: No framing error occurred 1: A framing error has occurred	R/(W) *1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error has occurred	R/(W) *1
b6	RDRF	Receive Data Full Flag	0: No valid data is held in the RDR register 1: Received data is held in the RDR register	R/(W) *2
b7	TDRE	Transmit Data Empty Flag	0: Data to be transmitted is held in the TDR register 1: No data is held in the TDR register	R/(W) *2

Note 1. Only 0 can be written to this bit, to clear the flag.
Note 2. Write 1 when writing is necessary.

MPB Bit (Multi-Processor)

Holds the value of the multi-processor bit in the reception frame. This bit does not change when the RE bit in SCR is 0.

TEND Flag (Transmission End Flag)

Indicates completion of transmission.

[Setting conditions]

- Clearing of the SCR.TE bit to 0 (disabling serial transmission operations)
  When the SCR.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- The TDR is not updated at the time of transmission of the tail-end bit of a character being transmitted

[Clearing condition]

- When data for transmission are written to the TDR while the SCR.TE is 1
  When the TEND flag should become clear because data for transmission have been written to the TDR, read the TEND flag to confirm that its value has actually become 0.

PER Flag (Parity Error Flag)

Indicates that a parity error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception
  Although receive data when the parity error occurs is transferred to RDR, no RXI interrupt request occurs. Note that when the PER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1 (after writing 0 to it, read the PER bit to check that it has actually been cleared to 0.)
  Even when the RE bit in SCR is cleared to 0 (which indicates that serial reception is disabled), the PER flag is not affected and retains its previous value.

FER Flag (Framing Error Flag)

Indicates that a framing error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When the stop bit is 0
  In 2-stop-bit mode, only the first stop bit is checked whether it is 1 but the second stop bit is not checked. Note that although receive data when the framing error occurs is transferred to RDR, no RXI interrupt request occurs. In addition, when the FER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to FER after reading FER = 1 (after writing 0 to it, read the FER bit to check that it has actually been cleared to 0.)
  Even when the RE bit in SCR is cleared to 0, the FER flag is not affected and retains its previous value.

ORER Flag (Overrun Error Flag)

Indicates that an overrun error has occurred during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data is read from RDR
  In RDR, receive data prior to an overrun error occurrence is retained, but data received after the overrun error occurrence is lost. When the ORER flag is set to 1, subsequent serial reception cannot be performed. Note that, in clock synchronous mode, serial transmission also cannot continue.

[Clearing condition]

- When a 0 is written to ORER after reading ORER = 1 (after writing a 0 to it, read the ORER bit to check that it has actually been cleared to 0.)
  Even when the RE bit in SCR is cleared to 0, the ORER flag is not affected and retains its previous value.

RDRF Flag (Receive Data Full Flag)

Indicates whether the RDR register has received data.

[Setting condition]

- When data has been received normally, and transferred from RSR to RDR.

[Clearing condition]

- When data is read from RDR

TDRE Flag (Transmit Data Empty Flag)

Indicates whether the TDR register has data to be transmitted.

[Setting condition]

- When data is transferred from TDR to TSR

[Clearing condition]

- When data is written to TDR

(2) Smart Card Interface Mode (SMIF in SCMR = 1)

Address(es): SCI0.SSR 0008 A004h, SCI1.SSR 0008 A024h, SCI2.SSR 0008 A044h, SCI3.SSR 0008 A064h, SCI12.SSR 0008 B304h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	x	x	0	0	0	1	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	This bit should be set to 0 in smart card interface mode.	R/W
b1	MPB	Multi-Processor	This bit is not used in smart card interface mode. It should be set to 0.	R
b2	TEND	Transmit End Flag	0: A character is being transmitted. 1: Character transfer has been completed.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error has occurred	R/(W) *1
b4	ERS	Error Signal Status Flag	0: Low error signal not responded 1: Low error signal responded	R/(W) *1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error has occurred	R/(W) *1
b7, b6	—	Reserved	The read value is undefined. The write value should be 1.	R/W

Note 1. Only 0 can be written to this bit, to clear the flag.

MPBT Bit (Multi-Processor Bit Transfer)

This bit should be set to 0 in smart card interface mode.

MPB Bit (Multi-Processor)

This bit is not used in smart card interface mode. It should be set to 0.

TEND Flag (Transmission End Flag)

With no error signal from the receiving side, this bit is set to 1 when further data for transfer is ready to be transferred to the TDR register.

[Setting conditions]

- When SCR.TE bit = 0 (disabling serial transmission operations)
  When the SCR.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period has elapsed after the latest transmission of one byte, the ERS flag is 0, and the TDR register is not updated
  The set timing is determined by register settings as listed below.
  When SMR.GM = 0 and SMR.BLK = 0, 12.5 etu after the start of transmission
  When SMR.GM = 0 and SMR.BLK = 1, 11.5 etu after the start of transmission
  When SMR.GM = 1 and SMR.BLK = 0, 11.0 etu after the start of transmission
  When SMR.GM = 1 and SMR.BLK = 1, 11.0 etu after the start of transmission

[Clearing condition]

- When data for transmission are written to the TDR while the SCR.TE is 1

PER Flag (Parity Error Flag)

Indicates that a parity error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception
  Although receive data when the parity error occurs is transferred to RDR, no RXI interrupt request occurs. Note that when the PER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1 (After writing 0 to it, read the PER bit to check that it has actually been cleared to 0.)
  Even when the RE bit in SCR is cleared to 0 (which indicates that serial reception is disabled), the PER flag is not affected and retains its previous value.

ERS Flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled

[Clearing condition]

- When 0 is written to ERS after reading ERS = 1

ORER Flag (Overrun Error Flag)

Indicates that an overrun error has occurred during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data is read from RDR
  In RDR, the receive data prior to an overrun error occurrence is retained, but data received following the overrun error occurrence is lost. When the ORER flag is set to 1, subsequent serial reception cannot be performed.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1 (After writing 0 to it, read the ORER bit to check that it has actually been cleared to 0.)
  Even when the RE bit in SCR is cleared to 0, the ORER flag is not affected and retains its previous value.

29.2.8 Smart Card Mode Register (SCMR)

Address(es): SCI0.SCMR 0008 A006h, SCI1.SCMR 0008 A026h, SCI2.SCMR 0008 A046h, SCI3.SCMR 0008 A066h, SCI12.SCMR 0008 B306h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	—	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	SMIF	Smart Card Interface Mode Select	0: Serial communications interface mode 1: Smart card interface mode	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	SINV	Transmitted/Received Data Invert	0: TDR contents are transmitted as they are. Receive data is stored as it is in RDR. 1: TDR contents are inverted before being transmitted. Receive data is stored in inverted form in RDR.	R/W*1
b3	SDIR	Transmitted/Received Data Transfer Direction*2	0: Transfer with LSB-first 1: Transfer with MSB-first	R/W*1
b6 to b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7	BCP2	Base Clock Pulse 2	Selects the number of base clock cycles in combination with the SMR.BCP[1:0] bits. Setting values in the SCMR.BCP2 bit and SMR.BCP[1:0] bits BCP2 BCP1 BCP0 0 0 0: 93 clock cycles (S = 93)*3 0 0 1: 128 clock cycles (S = 128)*3 0 1 0: 186 clock cycles (S = 186)*3 0 1 1: 512 clock cycles (S = 512)*3 1 0 0: 32 clock cycles (S = 32)*3 (Initial Value) 1 0 1: 64 clock cycles (S = 64)*3 1 1 0: 372 clock cycles (S = 372)*3 1 1 1: 256 clock cycles (S = 256)*3	R/W*1

Note 1. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).
Note 2. In simple I2C mode, set the SDIR bit to 1 (MSB-first).
Note 3. S is the value of S in BRR (see section 29.2.9, Bit Rate Register (BRR)).

SMIF Bit (Smart Card Interface Mode Select)

When this bit is set to 1, smart card interface mode is selected.
When this bit is set to 0, synchronous, clock synchronous, simple SPI, or simple I^2C mode is selected.

SINV Bit (Transmitted/Received Data Invert)

Inverts the transmit/receive data logic level in the smart card interface mode. This bit does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR.

SDIR Bit (Transmitted/Received Data Transfer Direction)

Selects the serial/parallel conversion format.

BCP2 Bit (Base Clock Pulse 2)

Selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR.BCP[1:0] bits.

29.2.9 Bit Rate Register (BRR)

Address(es): SCI0.BRR 0008 A001h, SCI1.BRR 0008 A021h, SCI2.BRR 0008 A041h, SCI3.BRR 0008 A061h, SCI12.BRR 0008 B301h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud-rate generator control, different bit rates can be set for each. Table 29.8 lists the relationships between the setting (N) in the BRR and the bit rate (B) for normal asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple I^2C mode.

The initial value of BRR is FFh.

BRR can be read from by the CPU at all times, but it can be written to only when the TE and RE bits in SCR are 0.

Table 29.8 Relationships between N Setting in BRR and Bit Rate B

Mode	ABCS Bit in SEMR	BRR Setting	Error
Asynchronous, multi-processor transfer	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	1	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
Clock synchronous, simple SPI		$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	
Smart card interface		$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\} \times 100$
Simple I^2C*1		$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	

B: Bit rate (bps)
N: BRR setting for baud rate generator ($0 \leq N \leq 255$)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR setting listed in the following table.
Note 1. Adjust the bit rate so that the widths at high and low level of the SCL output in simple I^2C mode satisfy the I^2C standard.

Table 29.9 Calculating Widths at High and Low Level for SCL

Mode	SCL	Formula (Result in Seconds)
I^2C	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

Table 29.10 Clock Source Settings

SMR Setting		
CKS[1:0] Bits	Clock Source	n
0 0	PCLK clock	0
0 1	PCLK/4 clock	1
1 0	PCLK/16 clock	2
1 1	PCLK/64 clock	3

Table 29.11 Base Clock Settings in Smart Card Interface Mode

SCMR Setting	SMR Setting	Basic number of clock pulses for a single bit-period	
BCP2 Bit	BCP[1:0] Bits		S
0	0 0	93 clock cycles	93
0	0 1	128 clock cycles	128
0	1 0	186 clock cycles	186
0	1 1	512 clock cycles	512
1	0 0	32 clock cycles	32
1	0 1	64 clock cycles	64
1	1 0	372 clock cycles	372
1	1 1	256 clock cycles	256

Table 29.12, Table 29.13 lists sample N settings in BRR in normal asynchronous mode. Table 29.13 lists the maximum bit rate settable for each operating frequency. Examples of BRR (N) settings in clock synchronous mode and simple SPI mode are listed in Table 29.15. Examples of BRR (N) settings in smart card interface mode are listed inTable 29.15. Examples of BRR (N) settings in simple I^2C mode are listed in Table 29.19. In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 29.6.4, Receive Data Sampling Timing and Reception Margin. Table 29.14, Table 29.16 list the maximum bit rates with external clock input.

When the asynchronous mode base clock select bit (ABCS) in the serial extended mode register (SEMR) is set to 1 in asynchronous mode, the bit rate is two times that of listed in Table 29.12.

Table 29.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (1)

	Operating Frequency PCLK (MHz)											
	8			9.8304			10			12		
Bit Rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	–2.34

Table 29.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (2)

	Operating Frequency PCLK (MHz)											
	12.288			14			16			17.2032		
Bit Rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	217	0.08	2	248	–0.17	3	70	0.03	3	75	0.48
150	2	159	0.00	2	181	0.16	2	207	0.16	2	223	0.00
300	2	79	0.00	2	90	0.16	2	103	0.16	2	111	0.00
600	1	159	0.00	1	181	0.16	1	207	0.16	1	223	0.00
1200	1	79	0.00	1	90	0.16	1	103	0.16	1	111	0.00
2400	0	159	0.00	0	181	0.16	0	207	0.16	0	223	0.00
4800	0	79	0.00	0	90	0.16	0	103	0.16	0	111	0.00
9600	0	39	0.00	0	45	–0.93	0	51	0.16	0	55	0.00
19200	0	19	0.00	0	22	–0.93	0	25	0.16	0	27	0.00
31250	0	11	2.40	0	13	0.00	0	15	0.00	0	16	1.20
38400	0	9	0.00	—	—	—	0	12	0.16	0	13	0.00

Note: • This is an example when the ABCS bit in SEMR is 0.
When the ABCS bit is set to 1, the bit rate is two times.

Table 29.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (3)

	Operating Frequency PCLK (MHz)											
	17.2032			18			19.6608			20		
Bit Rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	75	0.48	3	79	–0.12	3	86	0.31	3	88	–0.25
150	2	223	0.00	2	233	0.16	2	255	0.00	3	64	0.16
300	2	111	0.00	2	116	0.16	2	127	0.00	2	129	0.16
600	1	223	0.00	1	233	0.16	1	255	0.00	2	64	0.16
1200	1	111	0.00	1	116	0.16	1	127	0.00	1	129	0.16
2400	0	223	0.00	0	233	0.16	0	255	0.00	1	64	0.16
4800	0	111	0.00	0	116	0.16	0	127	0.00	0	129	0.16
9600	0	55	0.00	0	58	–0.69	0	63	0.00	0	64	0.16
19200	0	27	0.00	0	28	1.02	0	31	0.00	0	32	–1.36
31250	0	16	1.20	0	17	0.00	0	19	-1.70	0	19	0.00
38400	0	13	0.00	0	14	–2.34	0	15	0.00	0	15	1.73

Table 29.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (4)

	Operating Frequency PCLK (MHz)											
	25			30			33			50		
Bit Rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	110	–0.02	3	132	0.13	3	145	0.33	3	221	–0.02
150	3	80	0.47	3	97	–0.35	3	106	0.39	3	162	–0.15
300	2	162	–0.15	2	194	0.16	2	214	–0.07	3	80	0.47
600	2	80	0.47	2	97	–0.35	2	106	0.39	2	162	–0.15
1200	1	162	–0.15	1	194	0.16	1	214	–0.07	2	80	0.47
2400	1	80	0.47	1	97	–0.35	1	106	0.39	1	162	–0.15
4800	0	162	–0.15	0	194	0.16	0	214	–0.07	1	80	0.47
9600	0	80	0.47	0	97	–0.35	0	106	0.39	1	40	–0.76
19200	0	40	–0.76	0	48	–0.35	0	53	–0.54	0	80	0.47
31250	0	24	0.00	0	29	0	0	32	0	0	49	0.00
38400	0	19	1.73	0	23	1.73	0	26	–0.54	0	40	–0.76

Note: • This is an example when the ABCS bit in SEMR is 0.
When the ABCS bit is set to 1, the bit rate is two times.

Table 29.13 Maximum Bit Rate for Each Operating Frequency (Asynchronous Mode)

PCLK (MHz)	Maximum Bit Rate(bps)	n	N
8	250000	0	0
9.8304	307200	0	0
10	312500	0	0
12	375000	0	0
12.288	384000	0	0
14	437500	0	0
16	500000	0	0
17.2032	537600	0	0
18	562500	0	0
19.6608	614400	0	0
20	625000	0	0
25	781250	0	0
30	937500	0	0
33	1031250	0	0
50	1562500	0	0

Note: • When the ABCS bit in SEMR is set to 1, the bit rate is two times.

Table 29.14 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

		Maximum Bit Rate(bps)	
PCLK (MHz)	External Input Clock(MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000
25	6.2500	390625	781250
30	7.5000	468750	937500
33	8.2500	515625	1031250
50	12.500	781250	1562500

Table 29.15 BRR Settings for Various Bit Rates (Clock Synchronous Mode, Simple SPI Mode)

	Operating Frequency PCLK (MHz)															
	8		10		16		20		25		30		33		50	
Bit Rate (bps)	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																
250	3	124	—	—	3	249										
500	2	249	—	—	3	124	—	—			3	233				
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	194
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	3	77
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	155
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	2	77
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	124
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	61
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	124
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	49
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	24
1 M	0	0	—	—	0	3	0	4	—	—	—	—	—	—	—	—
2 M	0	0*1	—	—	0	1	—	—	—	—	—	—	—	—	—	—
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	4
4 M					0	0*1	—	—	—	—	—	—	—	—	—	—
5 M							0	0*1	—	—	—	—	—	—	—	—
6.25 M									0	0*1	—	—	—	—	0	1
7.5 M											0	0*1	—	—	—	—
8.25 M													0	0*1	—	—

Space: Setting prohibited.

—: Can be set, but there will be error.

Note 1. Though this setting can be made only when the clock for serial transfer is output, continuous transmission or reception is not possible. After a single-frame transmission or reception until transmission or reception of the next frame starts, a one-bit period elapses (output of the serial transfer clock is stopped for one-bit periods). Accordingly, transfer of one-flame (8-bit) data takes nine-bit periods, resulting in the average transfer rate being eight ninths.

Table 29.16 Maximum Bit Rate with External Clock Input (Clock Synchronous Mode, Simple SPI Mode)

PCLK (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bps)
8	1.3333	1333333.3
10	1.6667	1666666.7
12	2.0000	2000000.0
14	2.3333	2333333.3
16	2.6667	2666666.7
18	3.0000	3000000.0
20	3.3333	3333333.3
25	4.1667	4166666.7
30	5.0000	5000000.0
33	5.5000	5500000.0
50	8.3333	8333333.3

Table 29.17 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372)

Bit Rate (bps)	PCLK (MHz)	n	N	Error (%)
9600	7.1424	0	0	0.00
	10.00	0	1	30
	10.7136	0	1	25
	13.00	0	1	8.99
	14.2848	0	1	0.00
	16.00	0	1	12.01
	18.00	0	2	15.99
	20.00	0	2	6.66
	25.00	0	3	12.49
	30.00	0	3	5.01
	33.00	0	4	7.59
	50.00	0	6	0.01

Table 29.18 Maximum Bit Rate for Each Operating Frequency (Smart Card Interface Mode, S = 372)

PCLK (MHz)	Maximum Bit Rate (bps)	n	N
10.00	13441	0	0
10.7136	14400	0	0
13.00	17473	0	0
16.00	21505	0	0
18.00	24194	0	0
20.00	26882	0	0
25.00	33602	0	0
30.00	40323	0	0
33.00	44355	0	0
50.00	67204	0	0

Table 29.19 BRR Settings for Various Bit Rates (Simple I²C Mode) (1)

	Operating Frequency PCLK (MHz)											
	8			10			16			20		
Bit Rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	31	–2.3	1	12	–3.8	1	15	–2.3
25 k	0	9	0.0	0	12	–3.8	1	4	0.0	1	6	–10.7
50 k	0	4	0.0	0	6	–10.7	1	2	–16.7	1	3	–21.9
100 k	0	2	–16.7	0	3	–21.9	0	4	0.0	0	6	–10.7
250 k	0	0	0.0	0	1	–37.5	0	1	0.0	0	2	–16.7
350 k										0	1	–10.7

Table 29.19 BRR Settings for Various Bit Rates (Simple I2C Mode) (2)

	Operating Frequency PCLK (MHz)											
	25			30			33			50		
Bit Rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	19	–2.3	1	23	–2.3	1	25	–0.8	2	9	–2.3
25 k	1	7	–2.3	1	9	–6.3	1	10	–6.3	2	3	–2.3
50 k	1	3	–2.3	1	4	–6.3	1	5	–14.1	2	1	–2.3
100 k	1	1	–2.3	1	2	–21.9	1	2	–14.1	1	3	–2.3
250 k	0	3	–21.9	0	3	–6.3	0	4	–17.5	0	6	–10.7
350 k	0	2	–25.6	0	2	–10.7	0	2	–1.8	0	4	–10.7

Table 29.20 Minimum Widths at High and Low Level for SCL at Various Bit Rates (Simple I²C Mode) (1)

	Operating Frequency PCLK (MHz)											
	8			10			16			20		
Min. Widths at High/Low Level for SCL (µs)	n	N	High/Low Width	n	N	High/Low Width	n	N	High/Low Width	n	N	High/Low Width
10 k	0	24	43.75/50.00	0	31	44.80/51.20	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	6	19.60/22.40
50 k	0	4	8.75/10.00	0	6	9.80/11.20	1	2	10.50/12.00	1	3	11.20/12.80
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	1	2.80/3.20	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60

Table 29.20 Minimum Widths at High and Low Level for SCL at Various Bit Rates (Simple I2C Mode) (2)

	Operating Frequency PCLK (MHz)											
	25			30			33			50		
Min. Widths at High/Low Level for SCL (µs)	n	N	High/Low Width	n	N	High/Low Width	n	N	High/Low Width	n	N	High/Low Width
10 k	1	19	44.80/51.20	1	23	44.80/51.20	1	25	44.12/50.42	2	9	44.80/51.20
25 k	1	7	17.92/20.48	1	9	18.66/21.33	1	10	18.66/21.33	2	3	17.92/20.48
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	5	10.18/11.63	2	1	8.96/10.24
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.81	1	3	4.48/5.12
250 k	0	3	2.24/2.56	0	3	1.86/2.13	0	4	2.12/2.42	0	6	1.96/2.24
350 k	0	2	1.68/1.92	0	2	1.40/1.60	0	2	1.27/1.45	0	4	1.40/1.60

29.2.10 Serial Extended Mode Register (SEMR)

Address(es): SCI0.SEMR 0008 A007h, SCI1.SEMR 0008 A027h, SCI2.SEMR 0008 A047h, SCI3.SEMR 0008 A067h, SCI12.SEMR 0008 B307h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFEN	ABCS	—	—	—	ACS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ACS0	Asynchronous Mode Clock Source Select	[144-, 120-, 112, and 100-pin versions] (Valid only in asynchronous mode) 0: External clock input 1: MTU3 clock input (MTIOC6A, MTIOC7A) [64- and 48-pin versions] This bit is read as 0. The write value should be 0.	R/W*1
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	ABCS	Asynchronous Mode Base Clock Select	(Valid only in asynchronous mode) 0: Selects 16 base clock cycles for 1-bit period 1: Selects 8 base clock cycles for 1-bit period	R/W*1
b5	NFEN	Digital Noise Filter Function Enable	(In asynchronous mode) 0: Noise cancellation function for the RXDn input signal is disabled. 1: Noise cancellation function for the RXDn input signal is enabled. (in simple I^2C mode) 0: Noise cancellation function for the SSCLn and SSDAn input signals is disabled. 1: Noise cancellation function for the SSCLn and SSDAn input signals is enabled. The NFEN bit should be 0 in any mode other than above.	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

SEMR selects the clock source for 1-bit period in asynchronous mode.
The MTIOC6A and MTIOC7A outputs of MTU3 can be set as the serial transfer base clock. Figure 29.3 shows a setting example when the MTIOC6A and MTIOC7A outputs of MTU3 are selected.

ACS0 Bit (Asynchronous Mode Clock Source Select)

Selects the clock source in the asynchronous mode.
The ACS0 bit is valid in asynchronous mode (CM bit in SMR = 0) and when an external clock input is selected (CKE[1:0] bits in SCR = 10b or 11b). An external clock input or internal MTU3 clock input can be selected.
Clear the ACS0 bit to 0 in other than asynchronous mode.

NFEN Bit (Digital Noise Filter Function Enable)

This bit enables or disables the digital noise filter function.

When the function is enabled, noise cancellation is applied to the RXDn input signal in asynchronous mode, and noise cancellation is applied to the SSDAn and SSCLn input signals in simple I^2C mode.

In any mode other than above, set the NFEN bit to 0 to disable the digital noise filter function.

When the function is disabled, input signals are transferred as is, as internal signals.

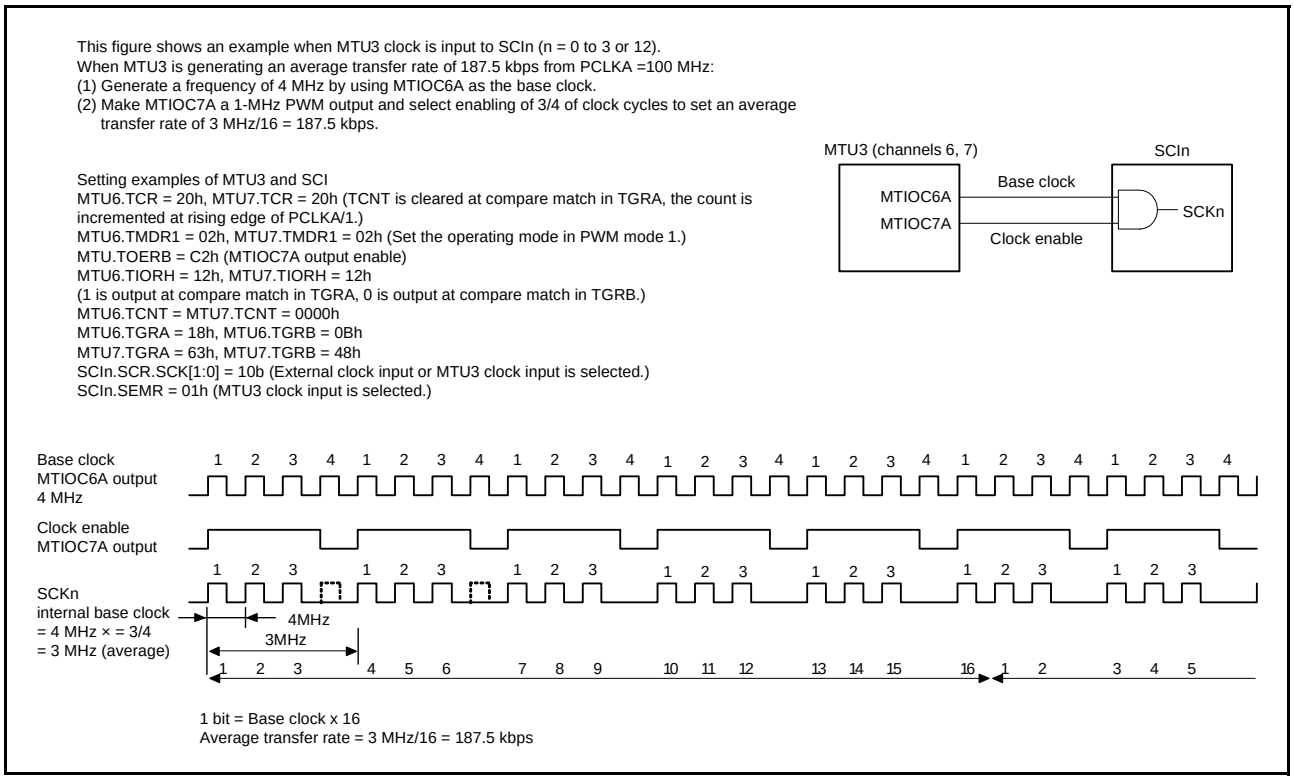


Figure 29.3 Example of Average Transfer Rate Setting when MTU3 Clock is Input

29.2.11 Noise Filter Setting Register (SNFR)

Address(es): SCI0.SNFR 0008 A008h, SCI1.SNFR 0008 A028h, SCI2.SNFR 0008 A048h, SCI3.SNFR 0008 A068h, SCI12.SNFR 0008 B308h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	NFCS[2:0]	Noise Filter Clock Select	In asynchronous mode, the standard setting for the base clock is as follows. b2 b0 0 0 0: The clock signal divided by 1 is used with the noise filter. In simple I2C mode, the standard settings for the clock source selected for the on-chip baud rate generator are given below. b2 b0 0 0 1: The clock signal divided by 1 is used with the noise filter. 0 1 0: The clock signal divided by 2 is used with the noise filter. 0 1 1: The clock signal divided by 4 is used with the noise filter. 1 0 0: The clock signal divided by 8 is used with the noise filter. Other values: Do not make settings other than those listed above.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (disabling reception and transmission).

NFCS[2:0] Bits (Noise Filter Clock Select)

These bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple I2C mode, set the bits to a value in the range from 001b to 100b.

29.2.12 I²C Mode Register 1 (SIMR1)

Address(es): SCI0.SIMR1 0008 A009h, SCI1.SIMR1 0008 A029h, SCI2.SIMR1 0008 A049h, SCI3.SIMR1 0008 A069h, SCI12.SIMR1 0008 B309h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IICM	Simple I²C Mode Select	SMIF IICM 0 0: Serial interface mode (in asynchronous, synchronous, or simple SPI mode) 0 1: Simple I²C mode 1 0: Smart card interface mode 1 1: Setting prohibited.	R/W*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b3	IICDL[4:0]	SSDA Delay Output Select	(Cycles below are of the clock signal from the on-chip baud rate generator.) b7 b3 0 0 0 0 0: No output delay 0 0 0 0 1: 0 to 1 cycle 0 0 0 1 0: 1 to 2 cycles 0 0 0 1 1: 2 to 3 cycles 0 0 1 0 0: 3 to 4 cycles 0 0 1 0 1: 4 to 5 cycles : : 1 1 1 1 0: 29 to 30 cycles 1 1 1 1 1: 30 to 31 cycles	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (disabling reception and transmission).

SIMR1 is used to select simple I²C mode and the number of delay stages for the SSDA output.

IICM Bit (Simple I²C Mode Select)

In conjunction with the SMIF bit in SCMR, this bit selects the operating mode.

IICDL[4:0] Bits (SSDA Output Delay Select)

These bits are used to set a delay for output on the SSDAn pin relative to the falling edge of the output on the SSCLn pin. The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLK by the divisor set in SMR.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator. Set these bits to 00000b unless operation is in simple I²C mode. In simple I²C mode, set the bits to a value in the range from 00001b to 11111b.

29.2.13 I2C Mode Register 2 (SIMR2)

Address(es): SCI0.SIMR2 0008 A00Ah, SCI1.SIMR2 0008 A02Ah, SCI2.SIMR2 0008 A04Ah, SCI3.SIMR2 0008 A06Ah, SCI12.SIMR2 0008 B30Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IICINTM	I2C Interrupt Mode Select	0: Use ACK/NACK interrupts. 1: Use reception and transmission interrupts.	R/W*1
b1	IICCSC	Clock Synchronization	0: No synchronization with the clock signal 1: Synchronization with the clock signal	R/W*1
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	IICACKT	ACK Transmission Data	0: ACK transmission 1: NACK transmission and reception of ACK/NACK	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (disabling serial reception and transmission).

SIMR2 is used to select how reception and transmission are controlled in simple I2C mode.

IICINTM Bit (I2C Interrupt Mode Select)

This bit selects the sources of interrupt requests in simple I2C mode.

IICCSC Bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SSCLn clock signal is to be synchronized when the SSCLn bit has been placed at the low level in the case of a wait inserted by the other device, etc.

The SSCLn clock signal is not synchronized if the IICCSC bit is 0. The SSCLn clock signal is generated in accord with the rate selected in the BRR regardless of the level being input on the SSCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT Bit (ACK Transmission Data)

Transmitted data contains ACK bits. Set this bit to 1 when ACK and NACK bits are received.

29.2.14 I²C Mode Register 3 (SIMR3)

Address(es): SCI0.SIMR3 0008 A00Bh, SCI1.SIMR3 0008 A02Bh, SCI2.SIMR3 0008 A04Bh, SCI3.SIMR3 0008 A06Bh, SCI12.SIMR3 0008 B30Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTP REQ	IICRST AREQ	IICSTA REQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IICSTAREQ	Start Condition Generation	0: A start condition is not generated. 1: A start condition is generated.*1,*3,*4	R/W
b1	IICRSTAREQ	Restart Condition Generation	0: A restart condition is not generated. 1: A restart condition is generated.*2,*3,*4	R/W
b2	IICSTPREQ	Stop Condition Generation	0: A stop condition is not generated. 1: A stop condition is generated.*2,*3,*4	R/W
b3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag	0: There are no requests for generating conditions or a condition is being generated. 1: All request generation has been completed.	R/W
b5, b4	IICSDAS[1:0]	SSDA Output Select	b5 b4 0 0: Serial data output 0 1: Generate a start, restart, or stop condition. 1 0: Output the low level on the SSDA pin. 1 1: Place the SSDA pin in the high-impedance state.	R/W
b7, b6	IICSCLS[1:0]	SSCL Output Select	b7 b6 0 0: Serial clock output 0 1: Generate a start, restart, or stop condition. 1 0: Output the low level on the SSCL pin. 1 1: Place the SSCL pin in the high-impedance state.	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that it is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that it is busy.
Note 3. Do not set more than one from among the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Execute the generation of a condition after the value of the IICSTIF flag is 0.

SIMR3 is used to control the simple I²C mode start and stop conditions, and to hold the SSDAn and SSCLn pins at fixed levels.

IICSTAREQ Bit (Start Condition Generation)

When a start condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the start condition

IICRSTAREQ Bit (Restart Condition Generation)

When a restart condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICRSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the restart condition

IICSTPREQ Bit (Stop Condition Generation)

When a stop condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICSTPREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the stop condition

IICSTIF Flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After execution for the generation of a condition, this bit indicates the state of generation being completed. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after clearing the IICSTIF flag to 0.

If the TEIE bit in the SCR is enabling interrupt requests, an STI is output on completion of generation of the start, restart, or stop condition when the IICSTIF flag is 1.

[Setting condition]

- Completion of the generation of a start, restart, or stop condition (however, in cases where this conflicts with any of the conditions for the flag becoming zero listed below, the other condition takes precedence)

[Clearing conditions]

- Writing 0 to the bit (confirm that the IICSTIF flag is 0 before doing so)
- Writing 0 to the IICM bit in SIMR1 (when operation is not in simple I^2C mode)
- Writing 0 to the TE bit in SCR

IICSDAS[1:0] Bits (SSDA Output Select)

These bits control output from the SSDAn pin.

Set the IICSDAS and IICSCLS bits to the same value during normal operations.

IICSCLS[1:0] Bits (SSCL Output Select)

These bits control output from the SSCLn pin.

Set the IICSCLS and IICSDAS bits to the same value during normal operations.

29.2.15 I²C Status Register (SISR)

Address(es): SCI0.SISR 0008 A00Ch, SCI1.SISR 0008 A02Ch, SCI2.SISR 0008 A04Ch, SCI3.SISR 0008 A06Ch, SCI12.SISR 0008 B30Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	IICACKR	ACK Reception Data Flag	0: ACK received 1: NACK received	R/W*1
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	—	Reserved	The read value is undefined	R
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	—	Reserved	The read value is undefined	R
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit, to clear the flag.

SISR is used to monitor state in relation to simple I²C mode.

IICACKR Flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from this bit.

The IICACK flag is updated at the rising of SSCLn clock for the ACK/NACK receiving bit.

29.2.16 SPI Mode Register (SPMR)

Address(es): SCI0.SPMR 0008 A00Dh, SCI1.SPMR 0008 A02Dh, SCI2.SPMR 0008 A04Dh, SCI3.SPMR 0008 A06Dh, SCI12.SPMR 0008 B30Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SSE	SS Pin Function Enable	0: SS pin function is disabled. 1: SS pin function is enabled.	R/W*1
b1	CTSE	CTS Enable	0: CTS pin function is disabled (RTS output function is enabled). 1: CTS pin function is enabled	R/W*1
b2	MSS	Master Slave Select	0: Transmission is through the TXDn pin and reception is through the RXDn pin (master mode). 1: Reception is through the TXDn pin and transmission is through the RXDn pin (slave mode).	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MFF	Mode Fault Flag	0: No mode-fault error 1: Mode-fault error	R/W*2
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	CKPOL	Clock Polarity Select	0: Clock polarity is not inverted. 1: Clock polarity is inverted.	R/W*1
b7	CKPH	Clock Phase Select	0: Clock is not delayed. 1: Clock is delayed.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (disabling reception and transmission).
Note 2. Only 0 can be written to these bits, which clears the flag.

SPMR is used to select the extension settings in asynchronous and clock-synchronous modes.

SSE Bit (SS Pin Function Enable)

Set this bit to 1 if the SSn# pin is to be used in control of transmission and reception (in simple SPI mode). Set this bit to 0 in any other mode. Furthermore, even for usage in simple SPI mode, the SS# pin on the master side is not required to control reception and transmission when master mode (SCR.CKE[1:0] = 00b and MSS = 0) is selected and there is a single master, so the setting for the SSE bit is 0. Do not set both the SSE and CTS bits to “enabled” (even if this setting is made, the functions will be disabled).

CTSE Bit (CTS Enable)

Set this bit to 1 if the SSn# pin is to be used for inputting of the CTS control signal to control of transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple I^2C mode. Do not set both the CTS and SSE bits to “enabled” (even if this setting is made, the functions will be disabled).

MSS Bit (Master Slave Select)

This bit selects between master and slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when the MSS bit is set to 1, so that data are received through the TXDn pin and transmitted through the RXDn pin.
Set this bit to 0 in modes other than simple SPI mode.

MFF Flag (Mode Fault Flag)

This bit indicates mode-fault errors.
In a multi-master configuration, determine the mode-fault error occurrence by reading the MFF flag.
[Setting condition]

- Input on the SS# pin being at the low level during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0)

[Clearing condition]

- Writing 0 to the bit after it was read as 1

CKPOL Bit (Clock Polarity Select)

This bit selects the polarity of the clock signal output through the SCKn pin. See Figure 29.51 for details.
Clear the bit to 0 in other than simple SPI mode and clock synchronous mode.

CKPH Bit (Clock Phase Select)

This bit selects the phase of the clock signal output through the SCKn pin. See Figure 29.51 for details.
Clear the bit to 0 in other than simple SPI mode and clock synchronous mode.

29.2.17 Extended Serial Module Enable Register (ESMER)

Address(es): SCI12.ESMER 0008 B320h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ESME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ESME	Extended Serial Mode Enable	0: The extended serial mode is disabled. 1: The extended serial mode is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ESME Bit (Extended Serial Mode Enable)

When the ESME bit is 1, the facilities of the extended serial mode control section are enabled.
When the ESME bit is 0, the extended serial mode control section enters the following states:

- the extended serial mode control section is initialized

Table 29.21 Settings of the ESME Bits and Guaranteed Operation by Timer Operation Mode

ESME bit	Timer Mode	Break Field Low Width Judgment Mode	Break Field Low Width Output Mode
0	○*1	×	×
1	○	○	○

○: Guarantee of operation is necessary. ×: Guarantee of operation is not necessary.
Note 1. Operation is only possible with PCLK selected.

29.2.18 Control Register 0 (CR0)

Address(es): SCI12.CR0 0008 B321h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	BRME	RXDSF	SFSF	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	SFSF	Start Frame Status Flag	0: Start Frame detection function is disabled. 1: Start Frame detection function is enabled.	R
b2	RXDSF	RXDX12 Input Status Flag	0: RXDX12 input is enabled. 1: RXDX12 input is disabled.	R
b3	BRME	Bit Rate Measurement Enable	0: Measurement of bit rate is disabled. 1: Measurement of bit rate is enabled.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

29.2.19 Control Register 1 (CR1)

Address(es): SCI12.CR1 0008 B322h

	b7	b6	b5	b4	b3	b2	b1	b0
	PIBS[2:0]			PIBE	CF1DS[1:0]		CF0RE	BFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BFE	Break Field Enable	0: Break Field detection is disabled. 1: Break Field detection is enabled.	R/W
b1	CF0RE	Control Field 0 Reception Enable	0: Reception of Control Field 0 is disabled. 1: Reception of Control Field 0 is enabled.	R/W
b3, b2	CF1DS[1:0]	Control Field 1 Data Register Select	b3 b2 0 0: Selects comparison with the value in PCF1DR. 0 1: Selects comparison with the value in SCF1DR. 1 0: Selects comparison with the values in PCF1DR and SCF1DR. 1 1: Setting prohibited.	R/W
b4	PIBE	Priority Interrupt Bit Enable	0: The priority interrupt bit is disabled. 1: The priority interrupt bit is enabled.	R/W
b7 to b5	PIBS[2:0]	Priority Interrupt Bit Select	b7 b5 0 0 0: 0th bit of Control Field 1 0 0 1: 1st bit of Control Field 1 0 1 0: 2nd bit of Control Field 1 0 1 1: 3rd bit of Control Field 1 1 0 0: 4th bit of Control Field 1 1 0 1: 5th bit of Control Field 1 1 1 0: 6th bit of Control Field 1 1 1 1: 7th bit of Control Field 1	R/W

29.2.20 Control Register 2 (CR2)

Address(es): SCI12.CR2 0008 B323h

	b7	b6	b5	b4	b3	b2	b1	b0
	RTS[1:0]		BCCS[1:0]		—	DFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	DFCS[2:0]	RXDX12 Signal Digital Filter Clock Select	b2 b0 0 0 0: Filter is disabled. 0 0 1: Filter is enabled (SCI base clock). 0 1 0: Filter is enabled (PCLK/8). 0 1 1: Filter is enabled (PCLK/16). 1 0 0: Filter is enabled (PCLK/32). 1 0 1: Filter is enabled (PCLK/64). 1 1 0: Filter is enabled (PCLK/128). 1 1 1: Setting prohibited	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	BCCS[1:0]	Bus Collision Detection Clock Select	b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited	R/W
b7, b6	RTS[1:0]	RXDX12 Reception Sampling Timing Select	• When SCI12.SEMR.ABCS = 0 b7 b6 0 0: Rising edge of the 8th cycle of SCI base clock 0 1: Rising edge of the 10th cycle of SCI base clock 1 0: Rising edge of the 12th cycle of SCI base clock 1 1: Rising edge of the 14th cycle of SCI base clock • When SCI12.SEMR.ABCS = 1 b7 b6 0 0: Rising edge of the 4th cycle of SCI base clock 0 1: Rising edge of the 5th cycle of SCI base clock 1 0: Rising edge of the 6th cycle of SCI base clock 1 1: Rising edge of the 7th cycle of SCI base clock	R/W

Note 1. The period of the SCI base clock is 1/16 of a single data period when the SCI12.SEMR.ABCS is 0, and 1/8 of a single data period when the SCI12.SEMR.ABCS is 1. To use the SCI base clock, set the SCI12.SCR.TE bit to 1.

29.2.21 Control Register 3 (CR3)

Address(es): SCI12.CR3 0008 B324h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SDST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SDST	Start Frame Detection Start	0: Detection of Start Frame is not performed. 1: Detection of Start Frame is performed.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SDST Bits (Start Frame Detection Start)

Detection of a Start Frame begins when this bit is set to 1. The bit is read as 0.

29.2.22 Port Control Register (PCR)

Address(es): SCI12.PCR 0008 B325h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SHARPS	—	—	RXDXPS	TXDXPS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TXDXPS	TXDX12 Signal Polarity Select	0: The polarity of TXDX12 signal is not inverted for output. 1: The polarity of TXDX12 signal is inverted for output.	R/W
b1	RXDXPS	RXDX12 Signal Polarity Select	0: The polarity of RXDX12 signal is not inverted for input. 1: The polarity of RXDX12 signal is inverted for input.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SHARPS	TXDX/RXDX Pin Multiplexing Select	0: The TXDX and RXDX pins are independent. 1: The TXDX and RXDX signals are multiplexed on the same pin.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SHARPS Bit (TXDX/RXDX Pin Multiplexing Selection)

When this bit is set to 1, the TXDX12 and RXDX12 signals are multiplexed on the same pin so that half-duplex communications become possible.

29.2.23 Interrupt Control Register (ICR)

Address(es): SCI12.ICR 0008 B326h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AEDIE	BCDIE	PIBDIE	CF1MIE	CF0MIE	BFDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BFDIE	Break Field Low Width Detected Interrupt Enable	0: Interrupts on detection of the low width for a Break Field are disabled. 1: Interrupts on detection of the low width for a Break Field are enabled.	R/W
b1	CF0MIE	Control Field 0 Match Detected Interrupt Enable	0: Interrupts on detection of a match with Control Field 0 are disabled. 1: Interrupts on detection of a match with Control Field 0 are enabled.	R/W
b2	CF1MIE	Control Field 1 Match Detected Interrupt Enable	0: Interrupts on detection of a match with Control Field 1 are disabled. 1: Interrupts on detection of a match with Control Field 1 are enabled.	R/W
b3	PIBDIE	Priority Interrupt Bit Detected Interrupt Enable	0: Interrupts on detection of the priority interrupt bit are disabled. 1: Interrupts on detection of the priority interrupt bit are enabled.	R/W
b4	BCDIE	Bus Collision Detected Interrupt Enable	0: Interrupts on detection of a bus collision are disabled. 1: Interrupts on detection of a bus collision are enabled.	R/W
b5	AEDIE	Valid Edge Detected Interrupt Enable	0: Interrupts on detection of a valid edge are disabled. 1: Interrupts on detection of a valid edge are enabled.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

29.2.24 Status Register (STR)

Address(es): SCI12.STR 0008 B327h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AEDF	BCDF	PIBDF	CF1MF	CF0MF	BFDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BFDF	Break Field Low Width Detection Flag	[Setting conditions] • Detection of the low width for a Break Field • Completion of the output of the low width for a Break Field • Underflow of the timer [Clearing condition] • Writing 1 to the BFDCL bit in STCR	R
b1	CF0MF	Control Field 0 Match Flag	[Setting condition] • A match between the value received in Control Field 0 and the set value. [Clearing condition] • Writing 1 to the CF0MCL bit in STCR	R
b2	CF1MF	Control Field 1 Match Flag	[Setting condition] • A match between the data received in Control Field 1 and the set values. [Clearing condition] • Writing 1 to the CF1MCL bit in STCR	R
b3	PIBDF	Priority Interrupt Bit Detection Flag	[Setting condition] • Detection of the priority interrupt bit [Clearing condition] • Writing 1 to the PIBDCL bit in STCR	R
b4	BCDF	Bus Collision Detected Flag	[Setting condition] • Detection of the bus collision [Clearing condition] • Writing 1 to the BCDCL bit in STCR	R
b5	AEDF	Valid Edge Detection Flag	[Setting condition] • Detection of a valid edge [Clearing condition] • Writing 1 to the AEDCL bit in STCR	R
b7, b6	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

29.2.25 Status Clear Register (STCR)

Address(es): SCI12.STCR 0008 B328h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AEDCL	BCDCL	PIBDCL	CF1MCL	CF0MCL	BFDCL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BFDCL	BFDF Clear	Setting this bit to 1 clears the STR.BFDF flag. This bit is read as 0.	R/W
b1	CF0MCL	CF0MF Clear	Setting this bit to 1 clears the STR.CF0MF flag. This bit is read as 0.	R/W
b2	CF1MCL	CF1MF Clear	Setting this bit to 1 clears the STR.CF1MF flag. This bit is read as 0.	R/W
b3	PIBDCL	PIBDF Clear	Setting this bit to 1 clears the STR.PIBDF flag. This bit is read as 0.	R/W
b4	BCDCL	BCDF Clear	Setting this bit to 1 clears the STR.BCDF flag. This bit is read as 0.	R/W
b5	AEDCL	AEDF Clear	Setting this bit to 1 clears the STR.AEDF flag. This bit is read as 0.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

29.2.26 Control Field 0 Data Register (CF0DR)

Address(es): SCI12.CF0DR 0008 B329h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

CF0DR is an 8-bit readable and writable register that holds a value for comparison with Control Field 0.

29.2.27 Control Field 0 Compare Enable Register (CF0CR)

Address(es): SCI12.CF0CR 0008 B32Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	CF0CE7	CF0CE6	CF0CE5	CF0CE4	CF0CE3	CF0CE2	CF0CE1	CF0CE0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CF0CE0	Control Field 0 Bit 0 Compare Enable	0: Comparison with bit 0 of Control Field 0 is disabled. 1: Comparison with bit 0 of Control Field 0 is enabled.	R/W
b1	CF0CE1	Control Field 0 Bit 1 Compare Enable	0: Comparison with bit 1 of Control Field 0 is disabled. 1: Comparison with bit 1 of Control Field 0 is enabled.	R/W
b2	CF0CE2	Control Field 0 Bit 2 Compare Enable	0: Comparison with bit 2 of Control Field 0 is disabled. 1: Comparison with bit 2 of Control Field 0 is enabled.	R/W
b3	CF0CE3	Control Field 0 Bit 3 Compare Enable	0: Comparison with bit 3 of Control Field 0 is disabled. 1: Comparison with bit 3 of Control Field 0 is enabled.	R/W
b4	CF0CE4	Control Field 0 Bit 4 Compare Enable	0: Comparison with bit 4 of Control Field 0 is disabled. 1: Comparison with bit 4 of Control Field 0 is enabled.	R/W
b5	CF0CE5	Control Field 0 Bit 5 Compare Enable	0: Comparison with bit 5 of Control Field 0 is disabled. 1: Comparison with bit 5 of Control Field 0 is enabled.	R/W
b6	CF0CE6	Control Field 0 Bit 6 Compare Enable	0: Comparison with bit 6 of Control Field 0 is disabled. 1: Comparison with bit 6 of Control Field 0 is enabled.	R/W
b7	CF0CE7	Control Field 0 Bit 7 Compare Enable	0: Comparison with bit 7 of Control Field 0 is disabled. 1: Comparison with bit 7 of Control Field 0 is enabled.	R/W

29.2.28 Control Field 0 Receive Data Register (CF0RR)

Address(es): SCI12.CF0RR 0008 B32Bh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

CF0RR is a read-only register that holds the value received in Control Field 0. Writing to this register from the CPU or the DMA/DTC transfer is not possible.

29.2.29 Primary Control Field 1 Data Register (PCF1DR)

Address(es): SCI12.PCF1DR 0008 B32Ch

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

PCF1DR is an 8-bit readable and writable register that holds the 8-bit primary value for comparison with Control Field 1.

29.2.30 Secondary Control Field 1 Data Register (SCF1DR)

Address(es): SCI12.SCF1DR 0008 B32Dh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

PCF1DR is an 8-bit readable and writable register that holds the 8-bit secondary value for comparison with Control Field 1.

29.2.31 Control Field 1 Compare Enable Register (CF1CR)

Address(es): SCI12.CF1CR 0008 B32Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CF1CE7	CF1CE6	CF1CE5	CF1CE4	CF1CE3	CF1CE2	CF1CE1	CF1CE0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CF1CE0	Control Field 1 Bit 0 Compare Enable	0: Comparison with bit 0 of Control Field 1 is disabled. 1: Comparison with bit 0 of Control Field 1 is enabled.	R/W
b1	CF1CE1	Control Field 1 Bit 1 Compare Enable	0: Comparison with bit 1 of Control Field 1 is disabled. 1: Comparison with bit 1 of Control Field 1 is enabled.	R/W
b2	CF1CE2	Control Field 1 Bit 2 Compare Enable	0: Comparison with bit 2 of Control Field 1 is disabled. 1: Comparison with bit 2 of Control Field 1 is enabled.	R/W
b3	CF1CE3	Control Field 1 Bit 3 Compare Enable	0: Comparison with bit 3 of Control Field 1 is disabled. 1: Comparison with bit 3 of Control Field 1 is enabled.	R/W
b4	CF1CE4	Control Field 1 Bit 4 Compare Enable	0: Comparison with bit 4 of Control Field 1 is disabled. 1: Comparison with bit 4 of Control Field 1 is enabled.	R/W
b5	CF1CE5	Control Field 1 Bit 5 Compare Enable	0: Comparison with bit 5 of Control Field 1 is disabled. 1: Comparison with bit 5 of Control Field 1 is enabled.	R/W
b6	CF1CE6	Control Field 1 Bit 6 Compare Enable	0: Comparison with bit 6 of Control Field 1 is disabled. 1: Comparison with bit 6 of Control Field 1 is enabled.	R/W
b6	CF1CE7	Control Field 1 Bit 7 Compare Enable	0: Comparison with bit 7 of Control Field 1 is disabled. 1: Comparison with bit 7 of Control Field 1 is enabled.	R/W

29.2.32 Control Field 1 Receive Data Register (CF1RR)

Address(es): SCI12.CF1RR 0008 B32Fh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

CF1RR is a read-only register that holds the value received in Control Field 1. Writing to this register from the CPU or the DMA/DTC transfer is not possible.

29.2.33 Timer Control Register (TCR)

Address(es): SCI12.TCR 0008 B330h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TCST	Timer Count Start	0: Stops the timer counting 1: Starts the timer counting	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

29.2.34 Timer Mode Register (TMR)

Address(es): SCI12.TMR 0008 F331h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TCSS[2:0]			TWRC	—	TOMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TOMS[1:0]	Timer Operating Mode Select*1	b1 b0 0 0: Timer mode 0 1: Break Field low width determination mode 1 0: Break Field low width output mode 1 1: Setting prohibited	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	TWRC	Counter Write Control	0: Writing is to the reload register and the counter. 1: Writing is only to the reload register	R/W
b6 to b4	TCSS[2:0]	Timer Count Clock Source Select*1	b6 b4 0 0 0: PCLK 0 0 1: PCLK/2 0 1 0: PCLK/4 0 1 1: PCLK/8 1 0 0: PCLK/16 1 0 1: PCLK/32 1 1 0: PCLK/64 1 1 1: PCLK/128	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The TOMS[1:0] or TCSS[2:0] bits must be rewritten while the counter is stopped (TCST = 0).

TWRC Bit (Counter Write Control)

These bits determine whether a value written to TPRE or TCNT is only written to the reload register or is written to both the reload register and the counter.

29.2.35 Timer Prescaler Register (TPRE)

Address(es): SCI12.TPRE 0008 B332h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

TPRE consists of an eight-bit reload register, a read buffer, and a counter, each of which has FFh as its initial value. The counter counts down in synchronization with the counter clock selected by the TMR.TCSS[2:0] bits, and is reloaded with the value in the reload register when it underflows. Underflows of this register provide the clock source to drive counting by the TCNT register. The reload register and read buffer are allocated to the same address, so in writing, transfer is to the reload register and in reading, transfer is of the counter value from the read buffer.
It takes 1 system operating clock cycle to load a value from the reload register to the counter.

29.2.36 Timer Count Register (TCNT)

Address(es): SCI12.TCNT 0008 B333h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

TCNT consists of an eight-bit reload register, a read buffer, and a counter, each of which has FFh as its initial value. This down-counter counts underflows of the TPRE register until the TCNT register underflows, and is then reloaded with the value from the reload register. The reload register and read buffer are allocated to the same address, so in writing, transfer is to the reload register and in reading, transfer is of the counter value from the read buffer.
It takes 1 system operating clock cycle to load a value from the reload register to the counter.

29.3 Operation in Asynchronous Mode

Figure 29.4 shows the general format for asynchronous serial communications.
One frame consists of a start bit (low level), transmit/receive data, a parity bit, and stop bits (high level).
In asynchronous serial communications, the communications line is usually held in the mark state (high level).
The SCI monitors the communications line, and when it goes to the space state (low level), recognizes a start bit and starts serial communications.
Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

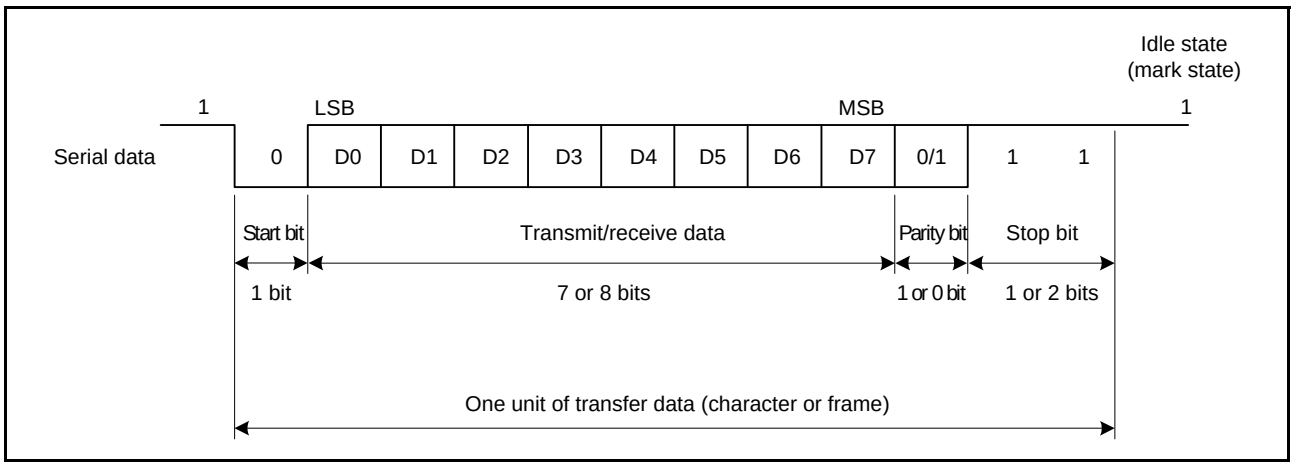


Figure 29.4 Data Format in Asynchronous Serial Communications (Example with 8-Bit Data, Parity, Two Stop Bits)

29.3.1 Serial Data Transfer Format

Table 29.22 lists the serial data transfer formats that can be used in asynchronous mode.
Any of 12 transfer formats can be selected according to the SMR setting. For details of multi-processor function, see section 29.4, Multi-Processor Communications Function.

Table 29.22 Serial Transfer Formats (Asynchronous Mode)

SMR Setting				Serial Transfer Format and Frame Length
CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12
0	0	0	0	S | 8-bit data | STOP
0	0	0	1	S | 8-bit data | STOP | STOP
0	1	0	0	S | 8-bit data | P | STOP
0	1	0	1	S | 8-bit data | P | STOP | STOP
1	0	0	0	S | 7-bit data | STOP
1	0	0	1	S | 7-bit data | STOP | STOP
1	1	0	0	S | 7-bit data | P | STOP
1	1	0	1	S | 7-bit data | P | STOP | STOP
0	—	1	0	S | 8-bit data | MPB | STOP
0	—	1	1	S | 8-bit data | MPB | STOP | STOP
1	—	1	0	S | 7-bit data | MPB | STOP
1	—	1	1	S | 7-bit data | MPB | STOP | STOP

S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multi-processor bit

29.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.
In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization. Since receive data is sampled at the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit, as shown in Figure 29.5. Thus the reception margin in asynchronous mode is determined by formula (1) below.

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{D - 0.5}{N}\ (1+F) \right| \times 100\ [\%] \quad \cdots \text{ Formula (1)}$$

M: Reception margin
N: Ratio of bit rate to clock (N = 16 when ABCS in SEMR = 0, N = 8 when ABCS in SEMR = 1)
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined by the formula below.

$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\%$

However, this is only the computed value, and a margin of 20% to 30% should be allowed in system design.

Note 1. This is an example when the ABCS bit in SEMR is 0. When the ABCS bit is 1, a frequency of 8 times the bit rate is used as a base clock and receive data is sampled at the rising edge of the 4th pulse of the base clock

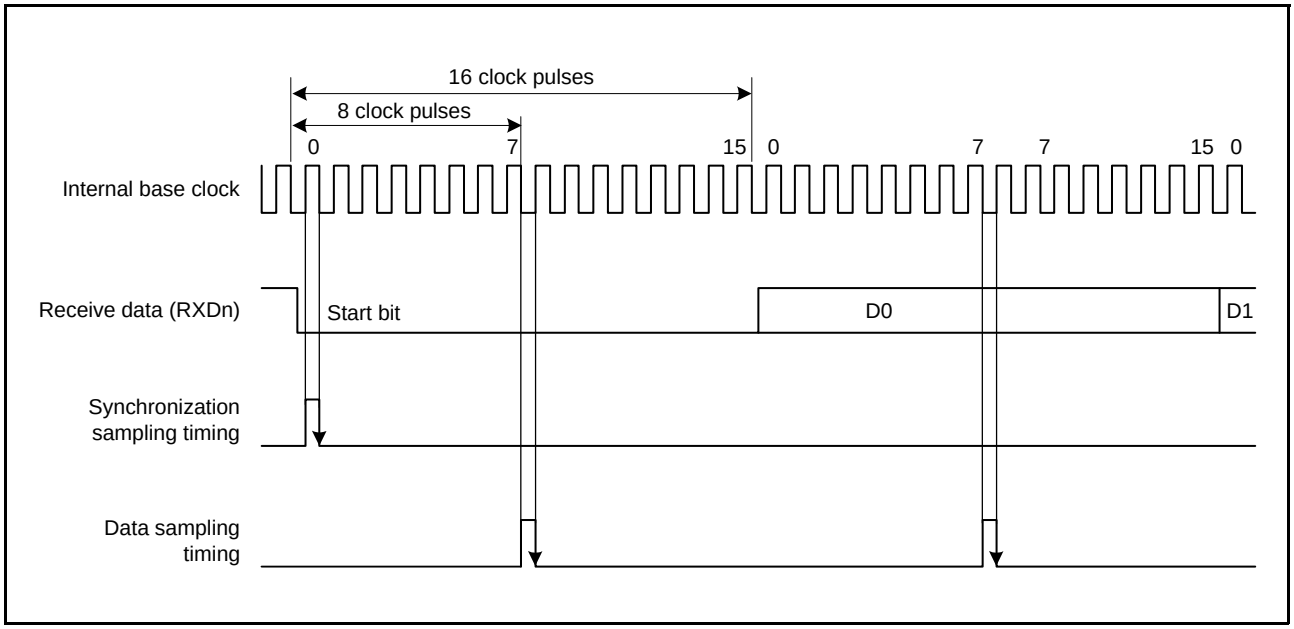


Figure 29.5 Receive Data Sampling Timing in Asynchronous Mode

29.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the SCI's transfer clock, according to the setting of the CM bit in SMR and the CKE[1:0] bits in SCR.
When an external clock is input to the SCKn pin, the clock frequency should be 16 times the bit rate (when ABCS in SEMR = 0) and 8 times the bit rate (when ABCS in SEMR = 1). In addition, when an external clock is specified, the base clock of MTU3 can be selected by the ACS0 bit in SEMR of SCIn (n = 0 to 3, 12).
When the SCI is operated on an internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in Figure 29.6.

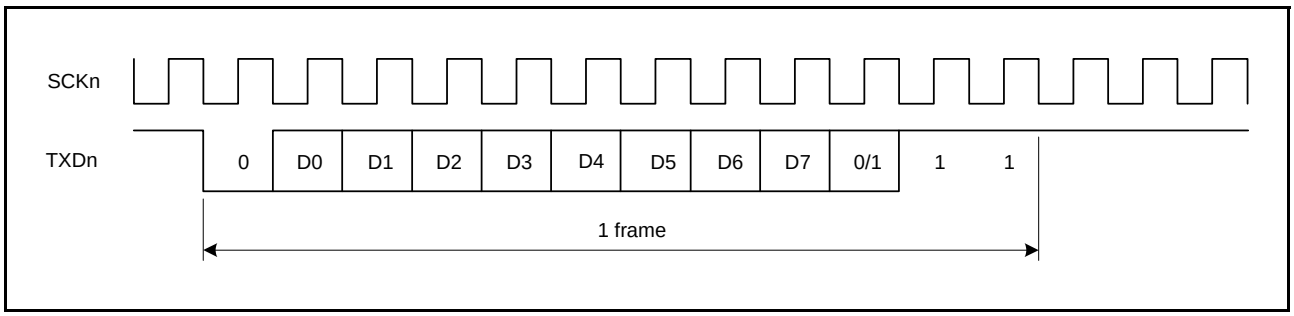


Figure 29.6 Phase Relationship between Output Clock and Transmit Data (Asynchronous Mode: SMR.CHR = 0, PE = 1, MP = 0, STOP = 1)

29.3.4 CTS and RTS Functions

The CTS function is the use of input on the CTSn# pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, placing the low level on the CTSn# pin causes transmission to start.
Applying the low level to the CTS# pin while transmission is in progress does not affect transmission of the current frame, which continues.
In the RTS function, by using the function of output on the RTSn# pin, a low level is output when reception becomes possible. Conditions for output of the low and high level are shown below.

[Conditions for low-level output]
Satisfaction of all conditions listed below

- The value of the RE bit in the SCR is 1
- Reception is not in progress
- There are no received data yet to be read
- The ORER, FER, and PER flags in the SSR are all 0

[Condition for high-level output]

- Any of the conditions for the low level not being satisfied

29.3.5 SCI Initialization (Asynchronous Mode)

Before transmitting and receiving data, start by writing the initial value “00h” to SCR and then continue through the procedure for SCI given in the sample flowchart (Figure 29.7). Whenever the operating mode or transfer format is changed, SCR must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied even during initialization.

Note that clearing the SCR.RE bit to 0 initializes neither the ORER, FER, nor the PER flags in SSR nor RDR.

Moreover, note that switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of a TXI (transmit data empty interrupt) request.

In processing to make initial settings, if the TE, TIE, and TEIE bits in the SCR register are set to 1 at the same time, caution is required because this will lead to the generation of a TEI (transmit end interrupt) before a TXI (transmit data empty interrupt).

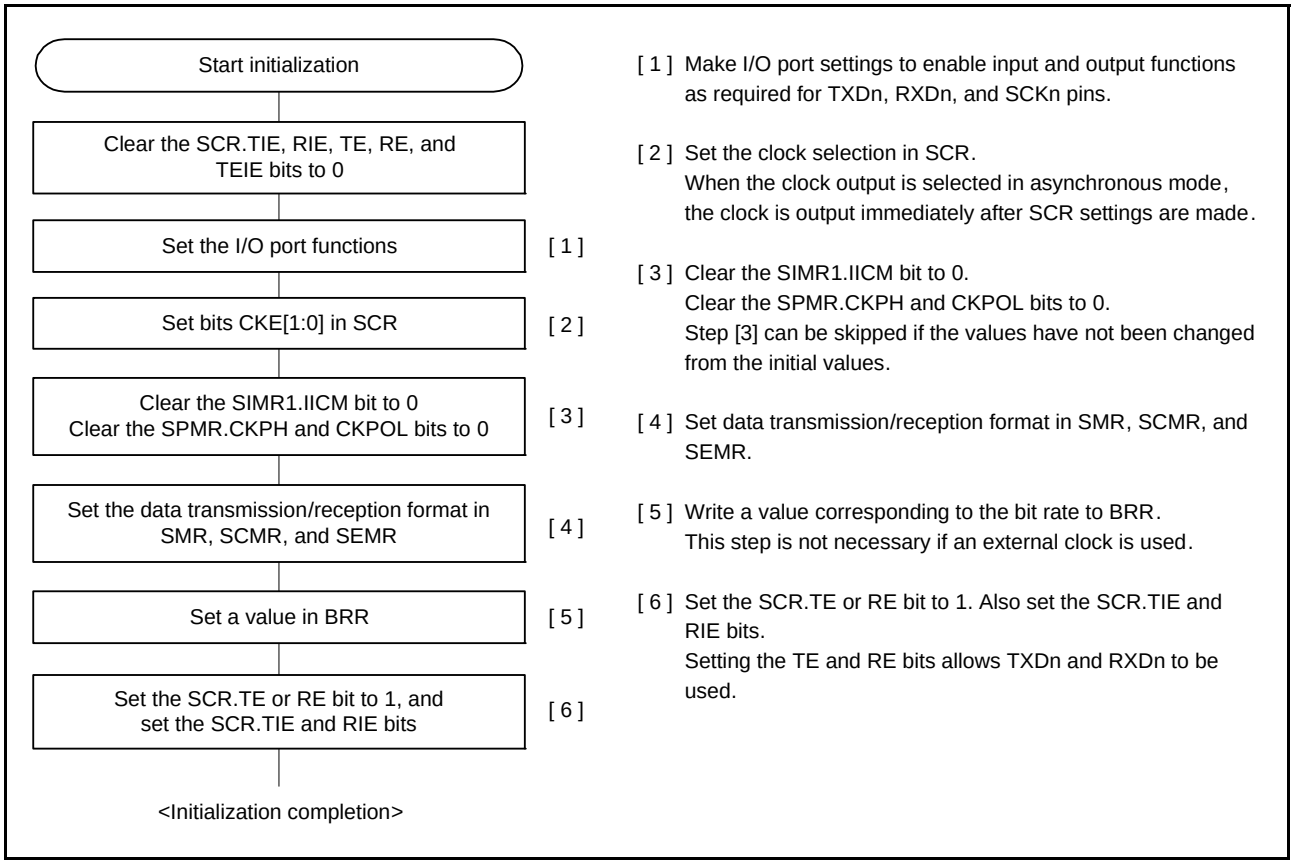


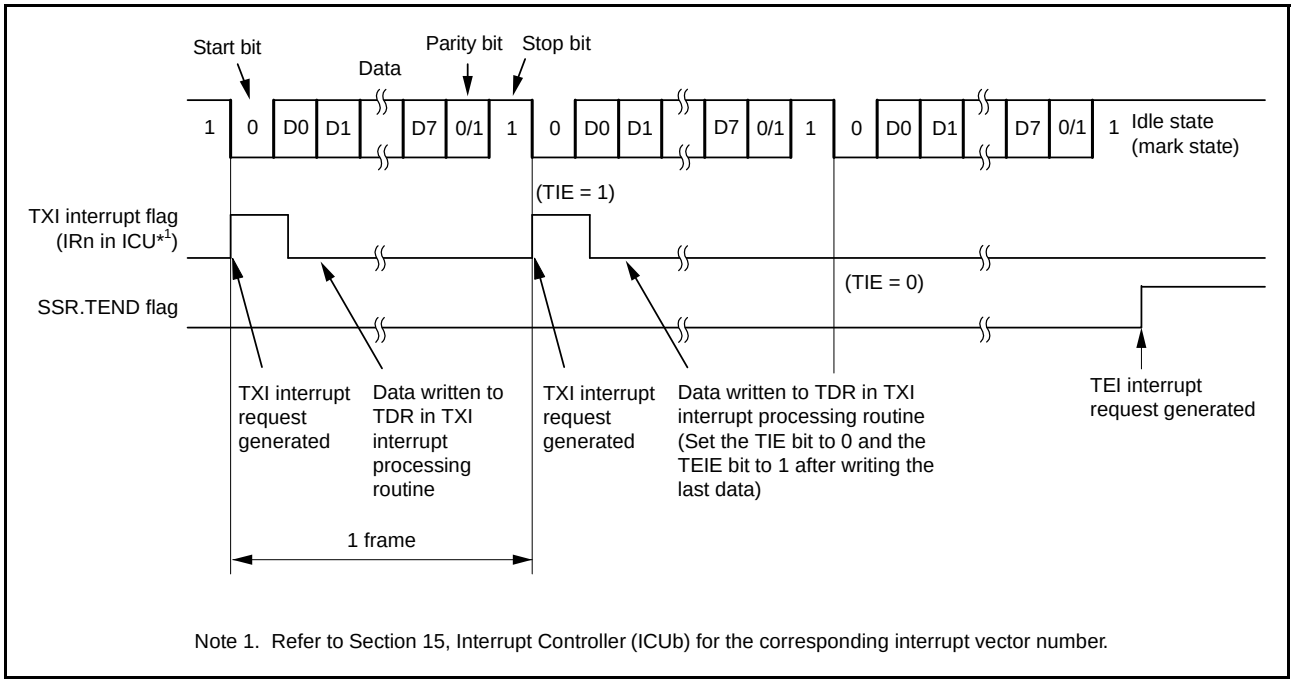
Figure 29.7 Sample SCI Initialization Flowchart (Asynchronous Mode)

29.3.6 Serial Data Transmission (Asynchronous Mode)

Figure 29.8 shows an example of the operation for serial transmission in asynchronous mode.
In serial transmission, the SCI operates as described below.

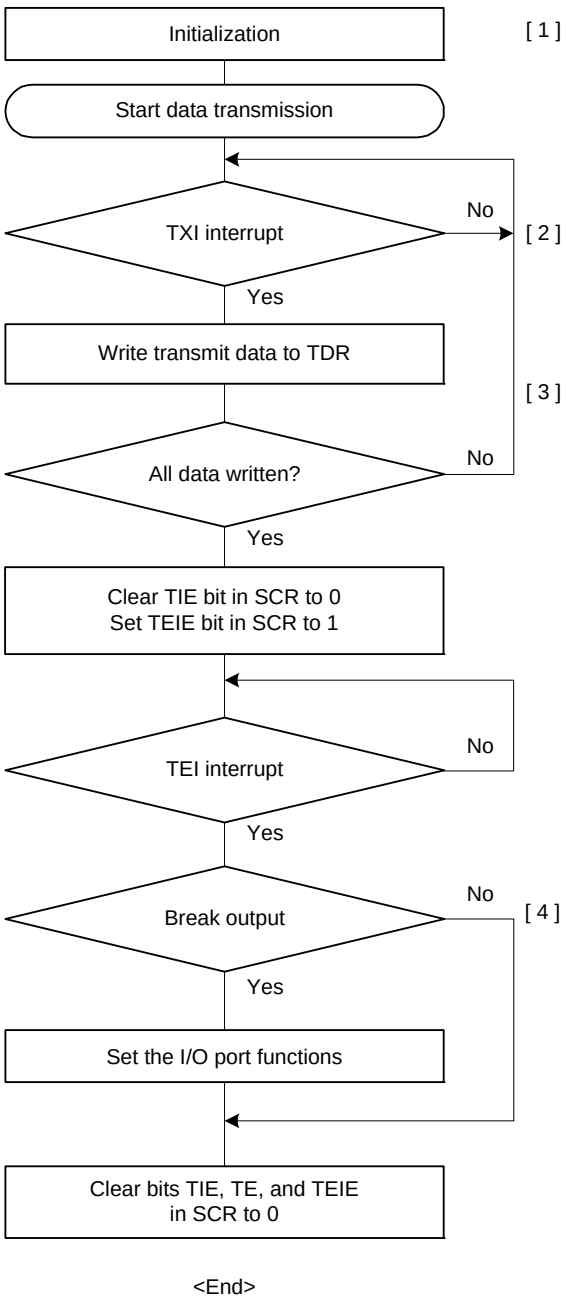
1. The SCI transfers data from TDR to TSR when data is written to TDR in the TXI interrupt processing routine. The TXI interrupt request at the beginning of transmission is generated when the TE bit in SCR is set to 1 after the TIE bit in SCR is set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the CTSE bit in SPMR is set to 0 (disabling the CTS function) and a low level on the CTS# pin causes data transfer from TDR to TSR. If the TIE bit in SCR is 1 at this time, a TXI interrupt request is generated. Continuous transmission is obtainable by writing the next data for transmission to TDR in the TXI interrupt processing routine before transmission of the current data for transmission is completed. When TEI interrupt requests are in use, set the SCR.TIE bit to 0 (disabling TXI requests) and the SCR.TEIE bit to 1 (enabling TEI requests) after the last of the data to be transmitted are written to the TDR from the processing routine for TXI requests.
3. Data is sent from the TXDn pin in the following order: start bit, transmit data, parity bit or multi-processor bit (may be omitted depending on the format), and stop bit.
4. The SCI checks for updating of (writing to) TDR at the time of stop bit output.
5. When TDR is updated, setting of the CTSE bit in SPMR to 0 (CTS function disabled) or a low level input on the CTSn# pin cause the next transfer of the next data for transmission from TDR to TSR and sending of the stop bit, after which serial transmission of the next frame starts.
6. If TDR is not updated, the TEND flag in SSR is set to 1, the stop bit is sent, and then the mark state is entered in which 1 is output. If the TEIE flag in SCR is 1 at this time, the TEND flag in SSR is set to 1 and a TEI interrupt request is generated.

Figure 29.9 shows a sample flowchart for serial transmission in asynchronous mode.



Note 1. Refer to Section 15, Interrupt Controller (ICUb) for the corresponding interrupt vector number.

Figure 29.8 Example of Operation for Serial Transmission in Asynchronous Mode (from the Middle of Transmission until Transmission Completion) (Example with 8-Bit Data, Parity, One Stop Bit)



[1] SCI initialization:
The TXDn automatically becomes the output pin for data being transmitted.
After the TE bit in SCR is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to TDR by a TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (TXI) request is generated.
Write transmit data to TDR once in the TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using a TXI interrupt request.
Transmit data can also be written to TDR by activating the DMAC or DTC.
When TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted are written to the TDR.

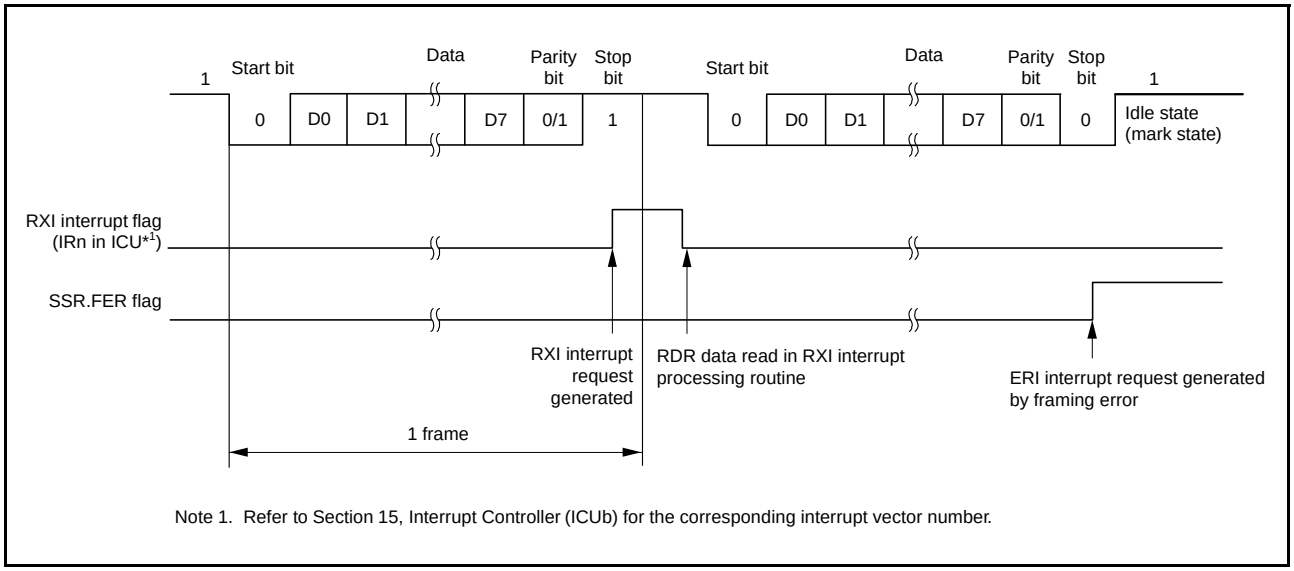
[4] Break output at the end of serial transmission:
To output a break in serial transmission, set the I/O port function corresponding to the TXDn pin (corresponding to output of the low level), and after switching the TXDn pin to the general I/O port function, set the TE bit in the SCR to 0.

Figure 29.9 Example of Serial Transmission Flowchart in Asynchronous Mode

29.3.7 Serial Data Reception (Asynchronous Mode)

Figure 29.10 and Figure 29.11 show examples of the operation for serial data reception in asynchronous mode. In serial data reception, the SCI operates as described below.

1. When the value of the RE bit in SCR becomes 1, the output signal on the RTSn# pin goes to the low level.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. If an overrun error occurs, the ORER flag in SSR is set to 1. If the RIE bit in SCR is 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR.
4. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is 1 at this time, an ERI interrupt request is generated.
5. If a framing error (when the stop bit is 0) is detected, the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is 1 at this time, an ERI interrupt request is generated.
6. When reception finishes successfully, receive data is transferred to RDR. If the RIE bit in SCR is 1 at this time, an RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to RDR in this RXI interrupt processing routine before reception of the next receive data is completed. Reading out the received data that have been transferred to RDR causes the RTSn# pin to output the low level.



Note 1. Refer to Section 15, Interrupt Controller (ICUb) for the corresponding interrupt vector number.

Figure 29.10 Example of SCI Operation for Serial Reception in Asynchronous Mode (1) (when RTS Function is not Used) (Example with 8-Bit Data, Parity, One Stop Bit)

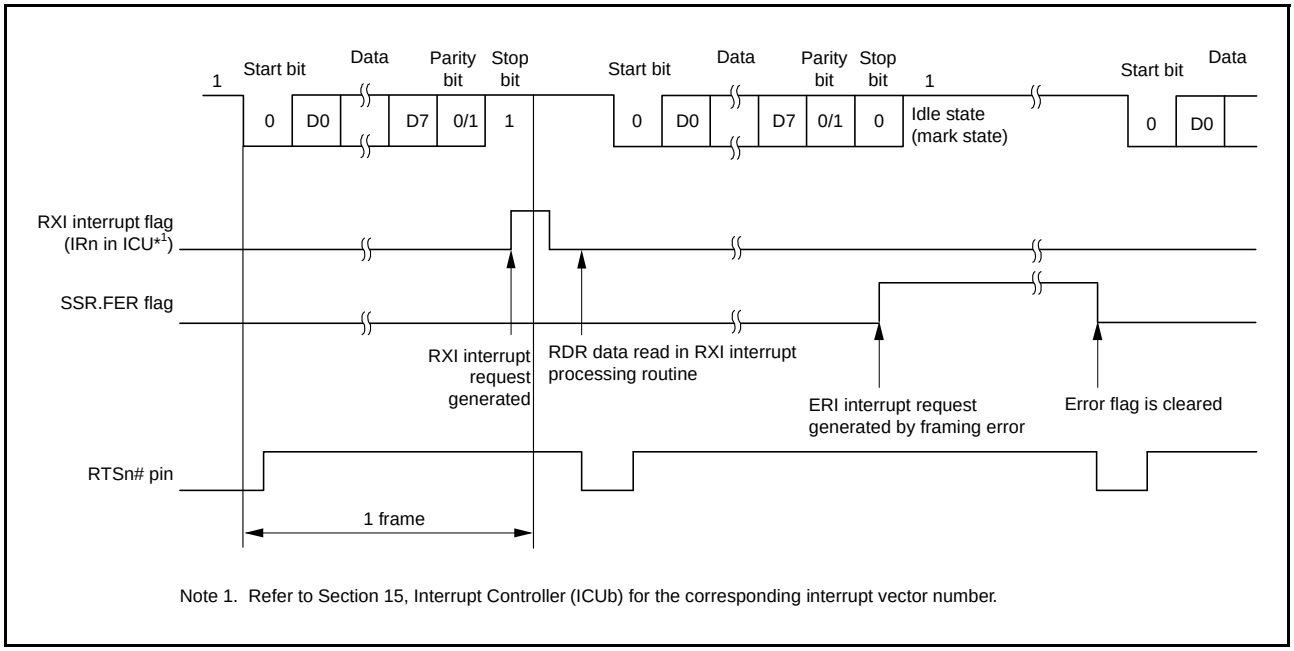


Figure 29.11 Example of SCI Operation for Serial Reception in Asynchronous Mode (2) (when RTS Function Is Used) (Example with 8-Bit Data, Parity, One Stop Bit)

Table 29.23 lists the states of the SSR status flags and receive data handling when a receive error is detected.
If a receive error is detected, an ERI interrupt request is generated but an RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, clear the ORER, FER, and PER bits to 0 before resuming reception. Moreover, be sure to read the RDR during overrun error processing.
Figure 29.12 and Figure 29.13 show samples of flowcharts for serial data reception.

Table 29.23 SSR Status Flags and Receive Data Handling

SSR Status Flag				
ORER	**FER**	**PER**	**Receive Data**	**Receive Error Type**
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR	Framing error
0	0	1	Transferred to RDR	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

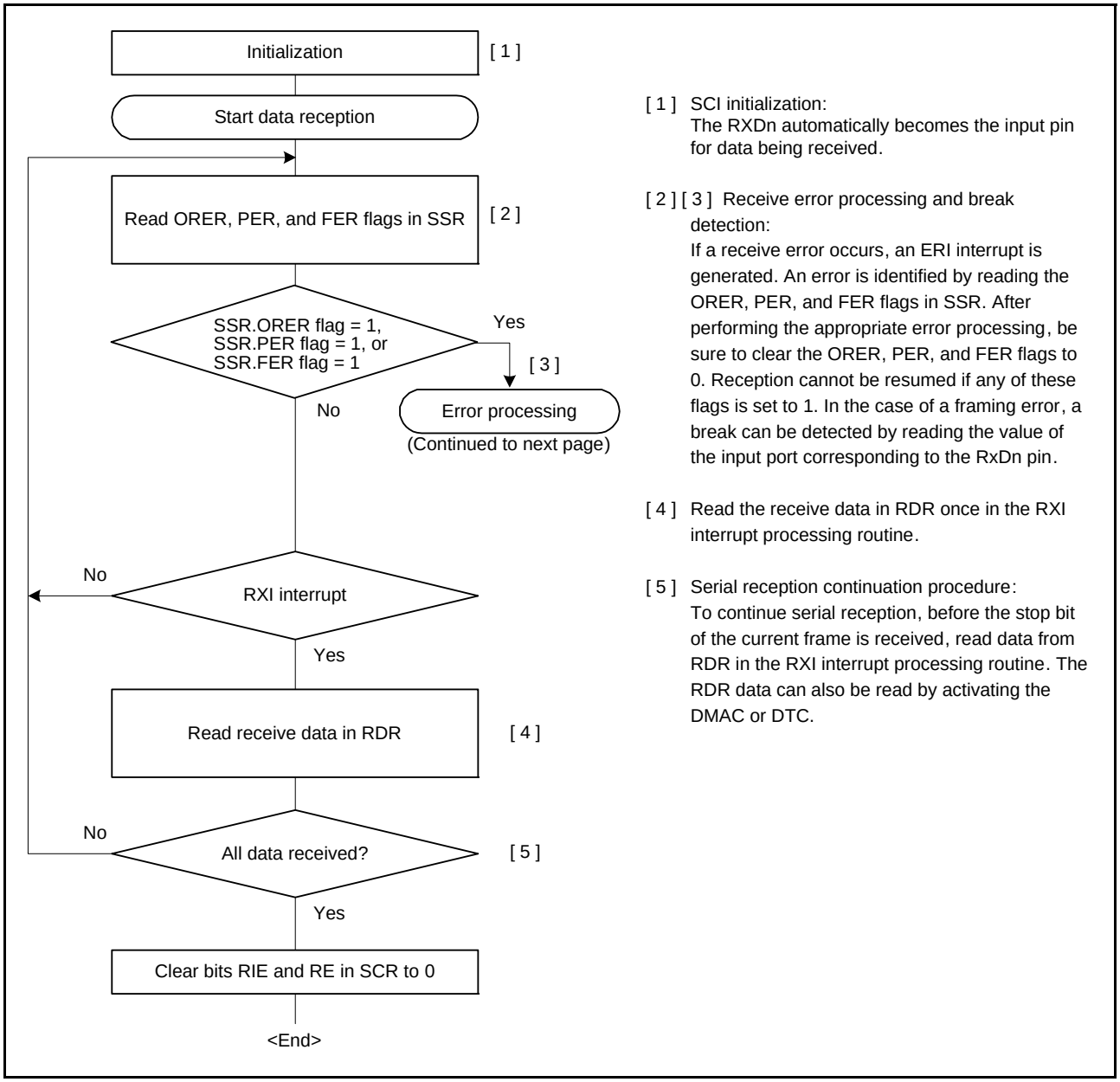


Figure 29.12 Example of Serial Reception Flowchart (1) (Asynchronous Mode)

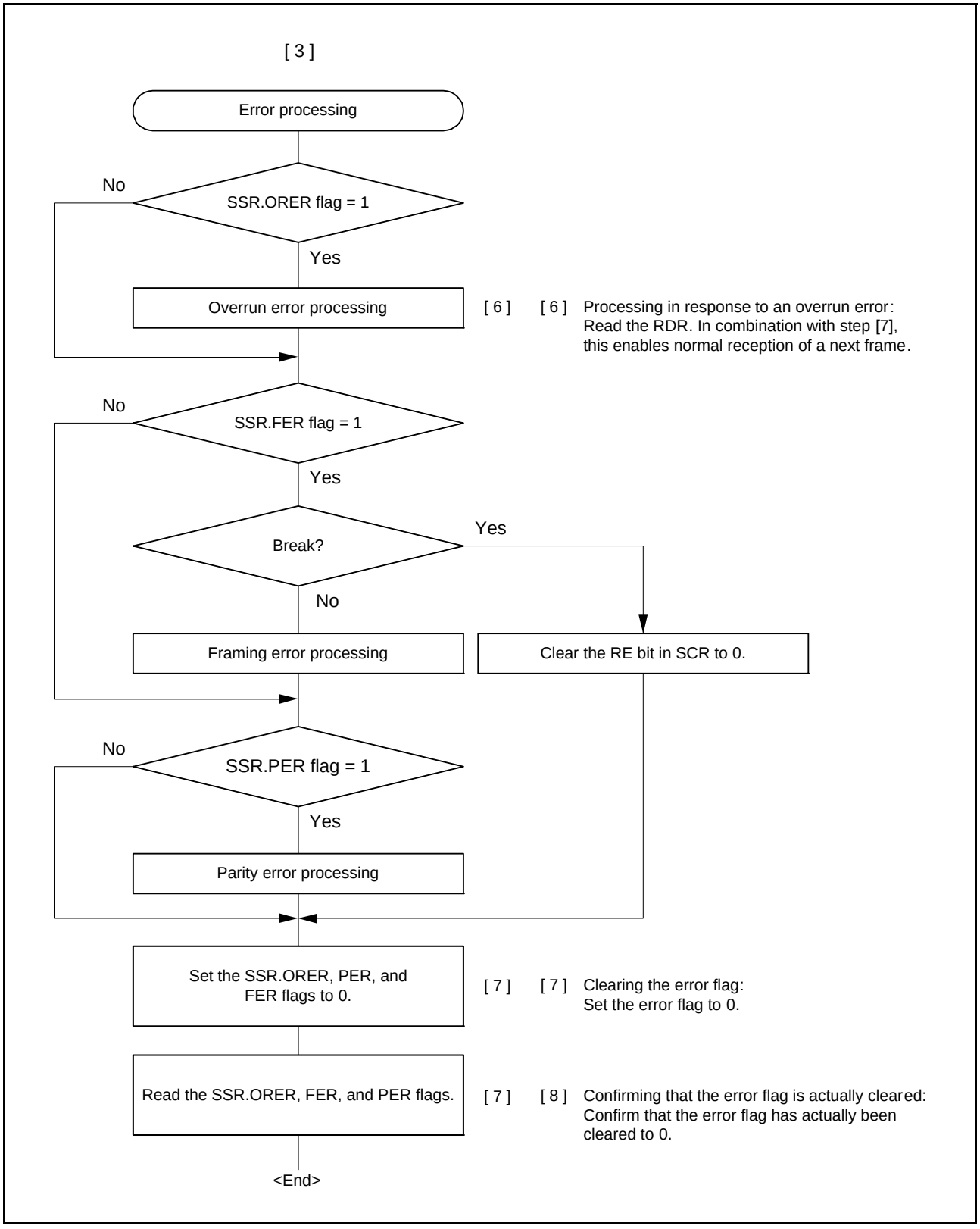


Figure 29.13 Example of Serial Reception Flowchart (2) (Asynchronous Mode)

29.4 Multi-Processor Communications Function

Using the multi-processor communication functions enables to transmit and receive data by sharing a communication line between multiple processors by using asynchronous serial communication in which the multi-processor bit is added. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station. The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle. When the multi-processor bit is set to 1, it indicates the ID transmission cycle and when the multi-processor bit is set to 0, it indicates the data transmission cycle. Figure 29.14 shows an example of communication between processors by using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1 is added to the ID code of the receiving station. Next, the transmitting station transmits the communication data in which the multi-processor bit set to 0 is added to the transmission data. Upon receiving the communication data in which the multi-processor bit is set to 1, the receiving station compares the received ID with the ID of the receiving station itself and if the two match, receives the communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until again receiving the communication data in which the multi-processor bit is set to 1.

For supporting this function, the SCI provides the MPIE bit in SCR. When the MPIE bit is set to 1, transfer of receive data from the RSR to the RDR, detection of a reception error, and setting the respective status flags ORER and FER in SSR are disabled until reception of data in which the multi-processor bit is set to 1. Upon receiving a reception character in which the multi-processor bit is set to 1, the MPBT bit in SSR is set to 1 and the MPIE bit in SCR is automatically cleared, thus returning to a normal reception operation. During this time, an RXI interrupt is generated if the RIE bit in SCR is set.

When the multi-processor format is specified, specification of the parity bit is disabled. Apart from this, there is no difference from the operation in the normal asynchronous mode. A clock which is used for the multi-processor communication is also the same as the clock used in the normal asynchronous mode.

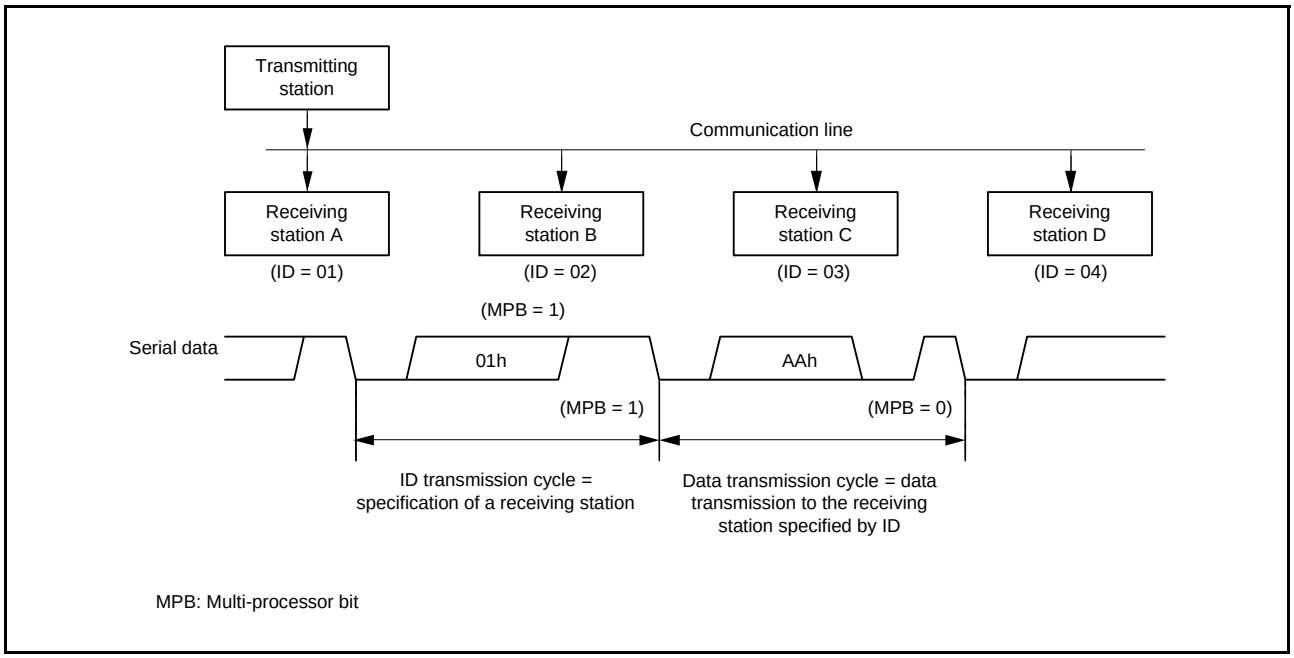


Figure 29.14 An Example of Communication using the Multi-Processor Format (Example of Transmission of Data AAh to Receiving Station A)

29.4.1 Multi-Processor Serial Data Transmission

Figure 29.15 is a sample flowchart of multi-processor data transmission. In the ID transmission cycle, the ID should be transmitted with the MPBT bit in SSR set to 1. In the data transmission cycle, the data should be transmitted with the MPBT bit set to 0. The other operations are the same as the operations in asynchronous mode.

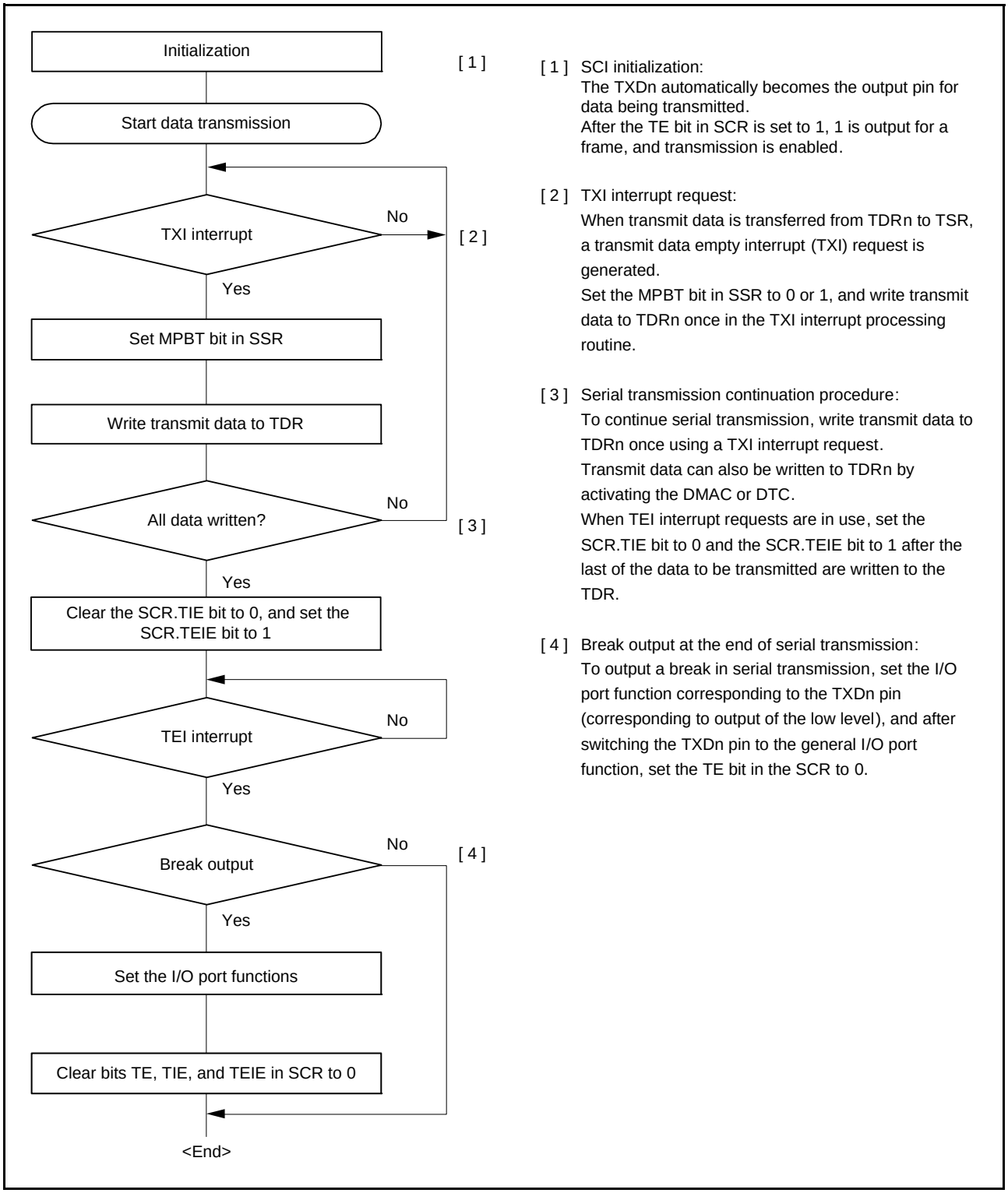


Figure 29.15 Example of Multi-Processor Serial Transmission Flowchart

29.4.2 Multi-Processor Serial Data Reception

Figure 29.17 and Figure 29.18 are sample flowcharts of multi-processor data reception. When the MPIE bit in SCR is set to 1, reading the communication data is skipped until reception of the communication data in which the multi-processor bit is set to 1. When the communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to RDR. During this time, the RXI interrupt request is generated. The other operations are the same as the operations in asynchronous mode.
Figure 29.16 is the example of operation for reception.

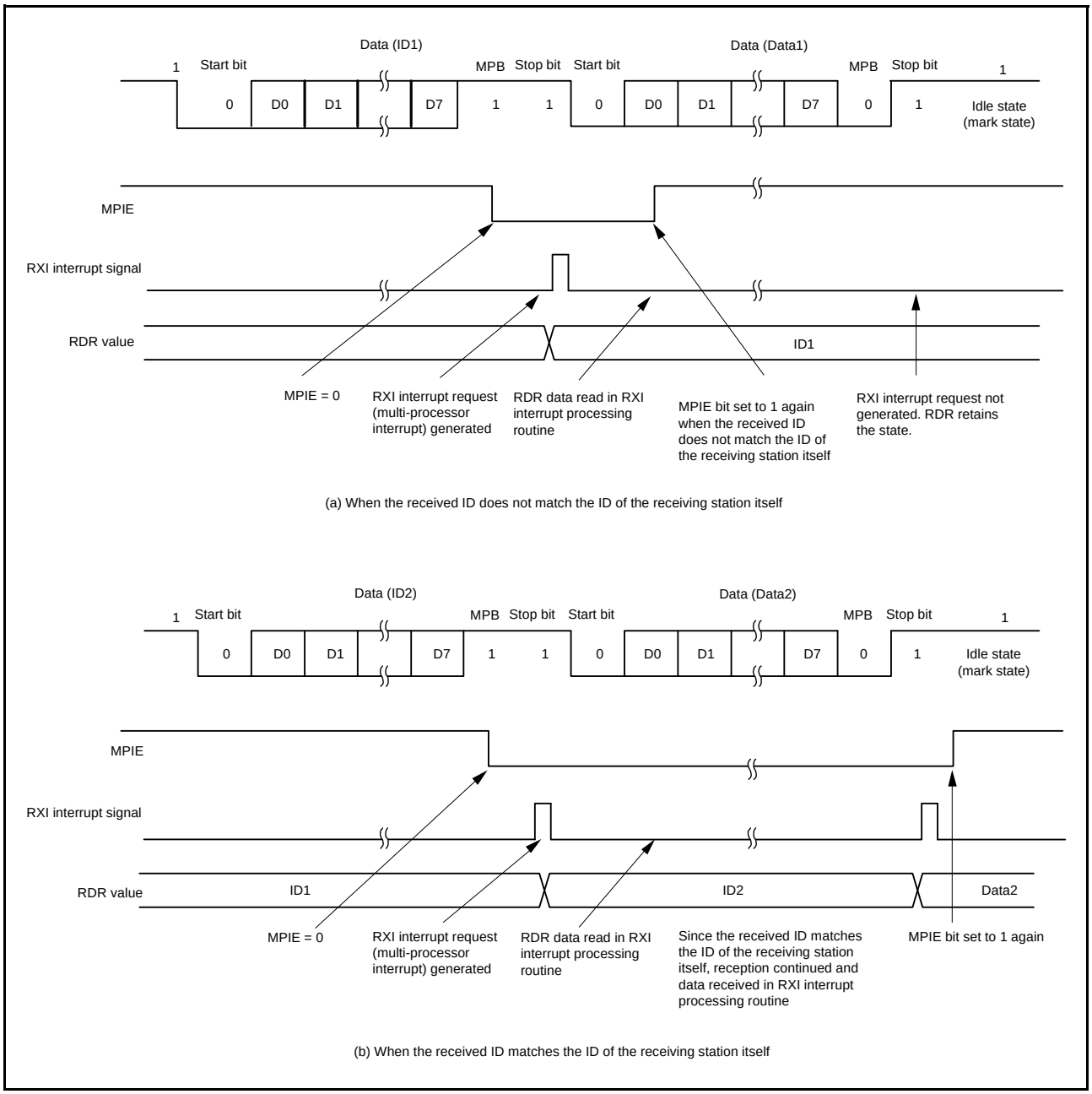


Figure 29.16 Example of SCI Reception (8-Bit Data/Multi-Processor Bit/One Stop Bit)

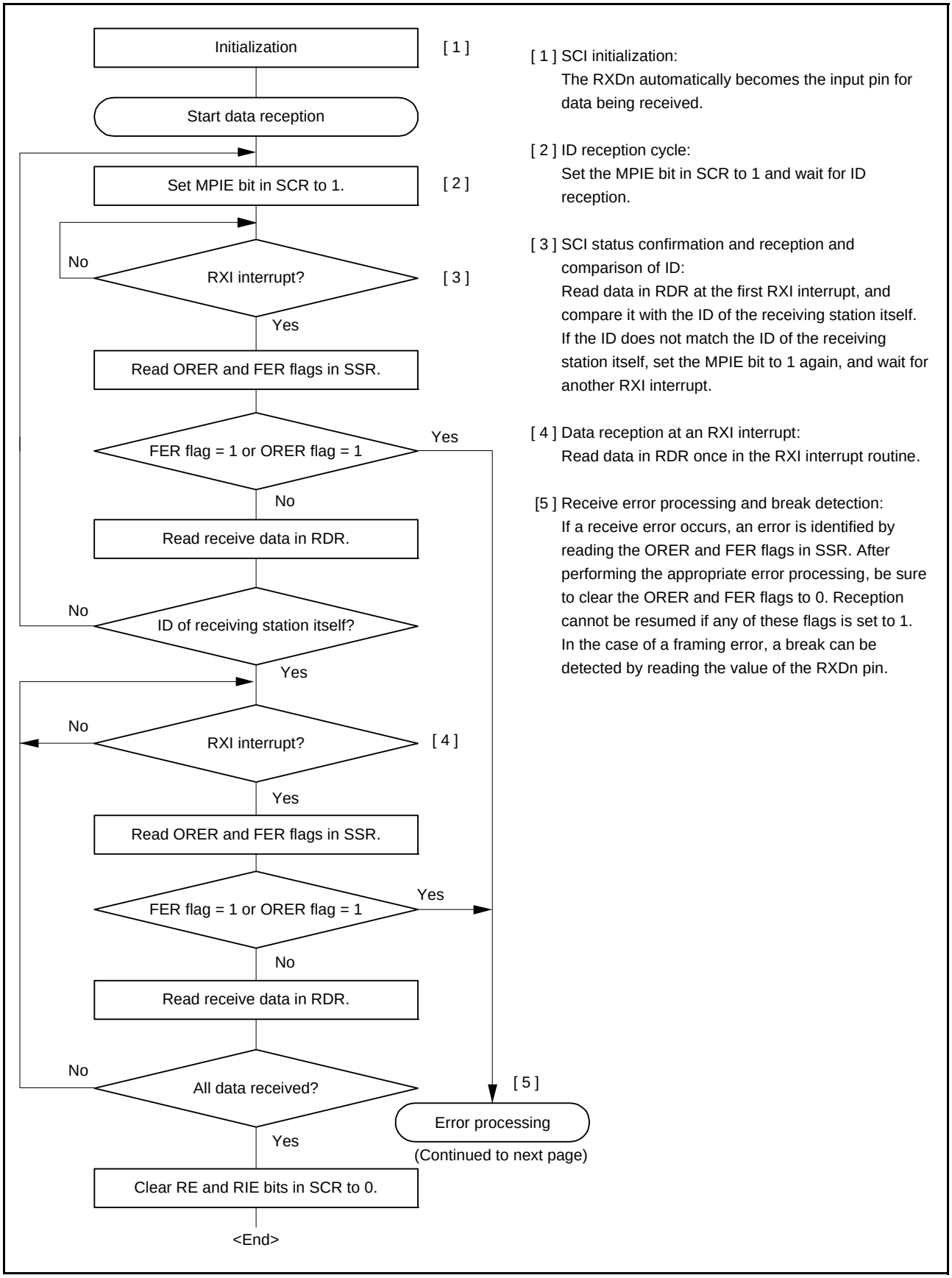


Figure 29.17 Example of Multi-Processor Serial Reception Flowchart (1)

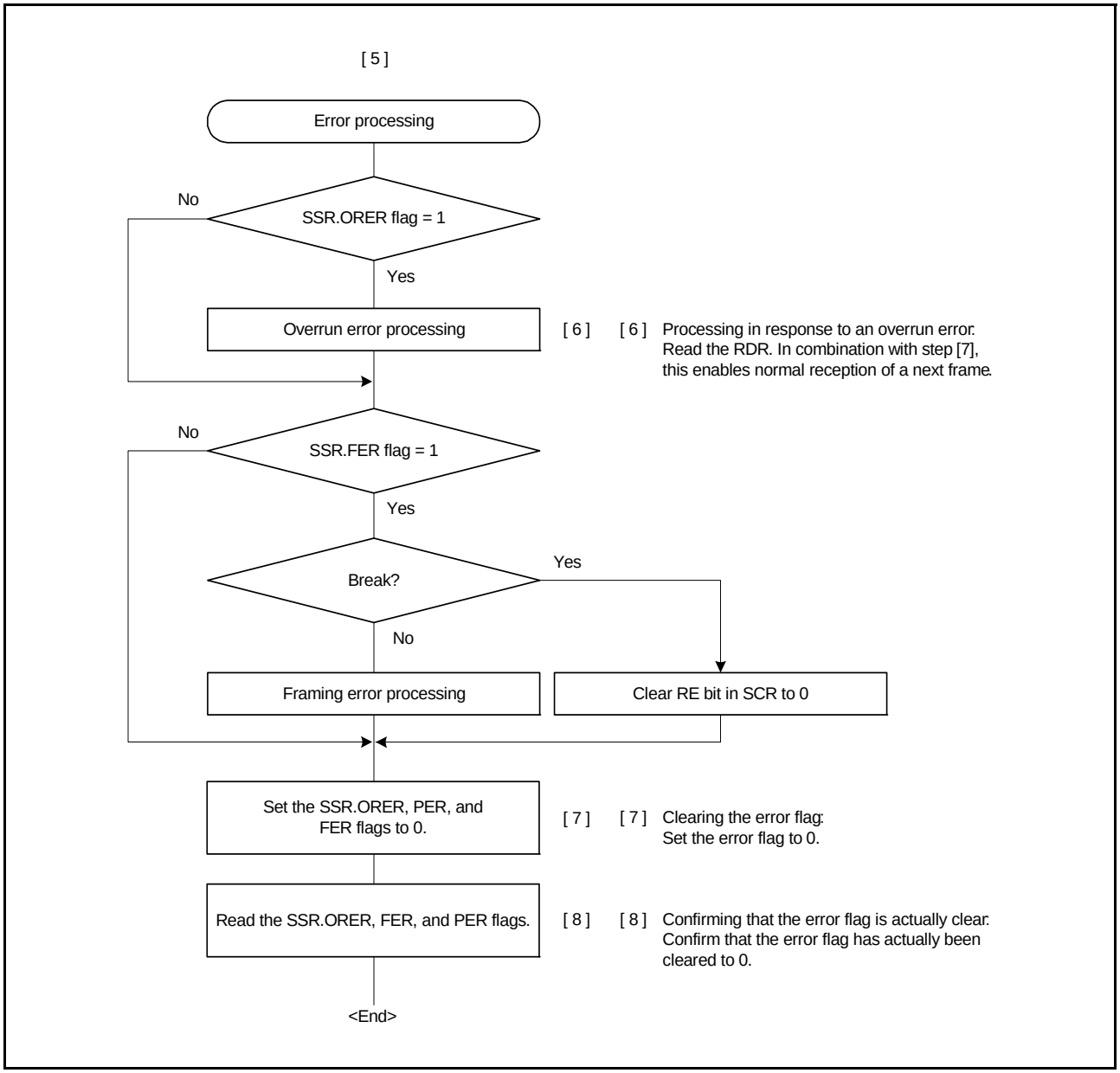
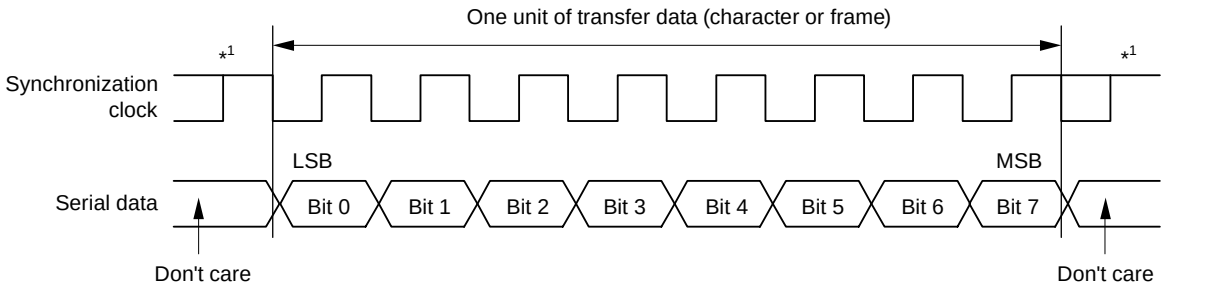


Figure 29.18 Example of Multi-Processor Serial Reception Flowchart (2)

29.5 Operation in Clock Synchronous Mode

Figure 29.19 shows the data format for clock synchronous serial data communications.
In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In clock synchronous mode, no parity bit can be added.
In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the last bit output state.
Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.



Note 1. Holds a high level except during continuous transfer.

Figure 29.19 Data Format in Clock Synchronous Serial Communications (LSB-First)

29.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected, according to the setting of the CKE[1:0] bits in SCR.
When the SCI is operated on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character, and when no transfer is performed the clock is held high. However, when only data reception is performed with the CTS function being disabled, the synchronizing clock output is started as the SCR.RE bit set to 1. The clock stops at the high level at occurrence of an overrun error or as the SCR.RE bit set to 1.
When only data reception is performed with the CTS function being enabled, the synchronizing clock output is not started even if the SCR.RE bit is set to 1 if the CTSn# pin input is high. The output starts when the SCR.RE bit set to 1 and the CTSn# pin input goes low. Then, if the CTSn# pin input is high at completion of frame reception, the clock stops at the high level at occurrence of an overrun error or as the SCR.RE bit set to 0.

29.5.2 CTS and RTS Functions

In the CTS function, CTSn# pin input is used to control reception/transmission start when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function.
When the CTS function is enabled, placing the low level on the CTSn# pin causes reception/transmission to start.
In the RTS function, RTSn# pin output is used to request reception/transmission start when the clock source is an external synchronizing clock. A low level is output when serial communications become possible. Conditions for output of the low and high level are shown below.

[Conditions for low-level output]
Satisfaction of all conditions listed below

- The value of the RE or TE bit in the SCR is 1
- Neither transmission nor reception is in progress
- There are no received data yet to be read (when the SCR.RE bit is 1)
- Transmit data has been written (when the SCR.TE bit is 1)
- ORER flag in SSR is 0

[Condition for high-level output]
Any of the conditions for the low level not being satisfied

29.5.3 SCI Initialization (Clock Synchronous Mode)

Before transmitting and receiving data, start by writing the initial value “00h” to the SCR and then continue through the procedure for SCI given in the sample flowchart (Figure 29.20). Whenever the operating mode or transfer format is changed, the SCR must be initialized before the change is made.
Note that clearing the SCR.RE bit to 0 initializes neither the ORER, FER, and PER flags in SSR nor RDR.
Moreover, note that switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of a TXI interrupt request.

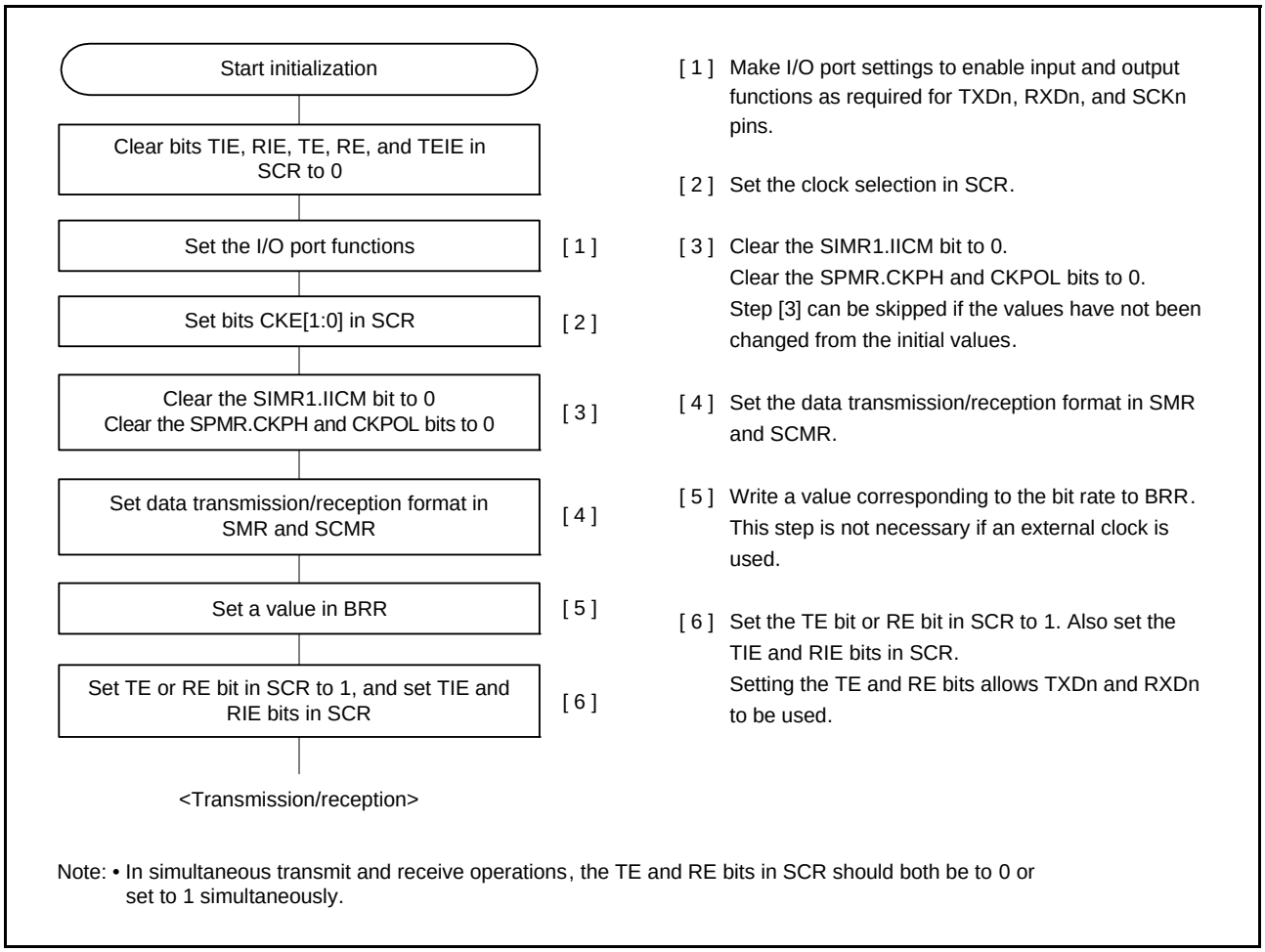


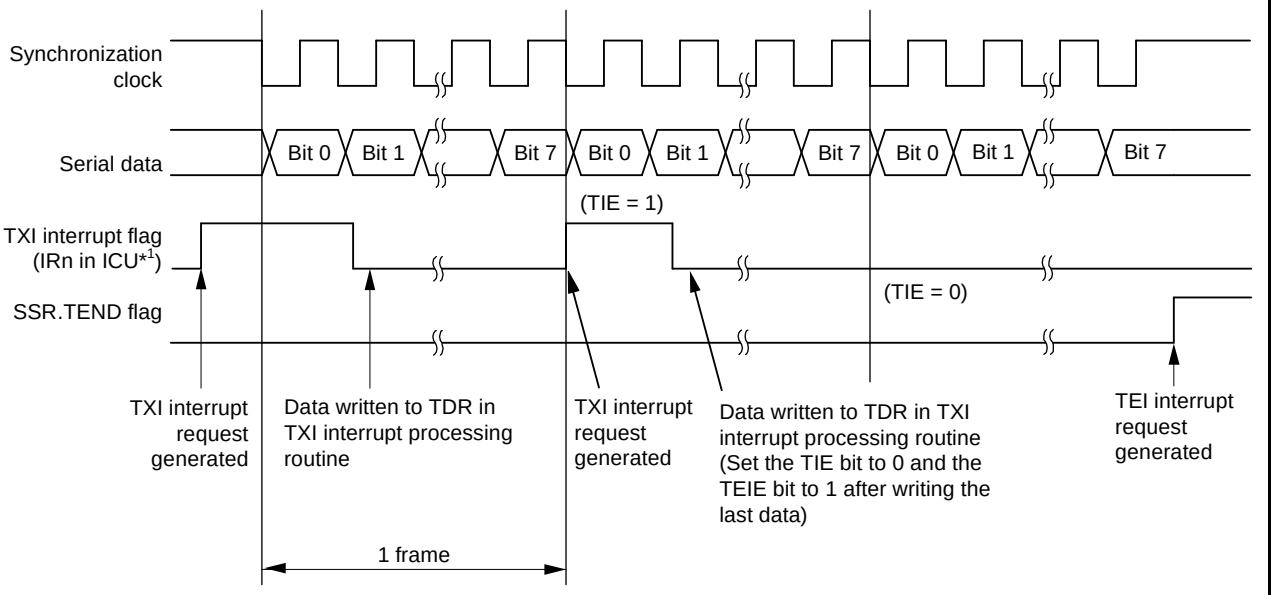
Figure 29.20 Example of SCI Initialization Flowchart (Clock Synchronous Mode)

29.5.4 Serial Data Transmission (Clock Synchronous Mode)

Figure 29.21 shows an example of the operation for serial transmission in clock synchronous mode.
In serial data transmission, the SCI operates as described below.

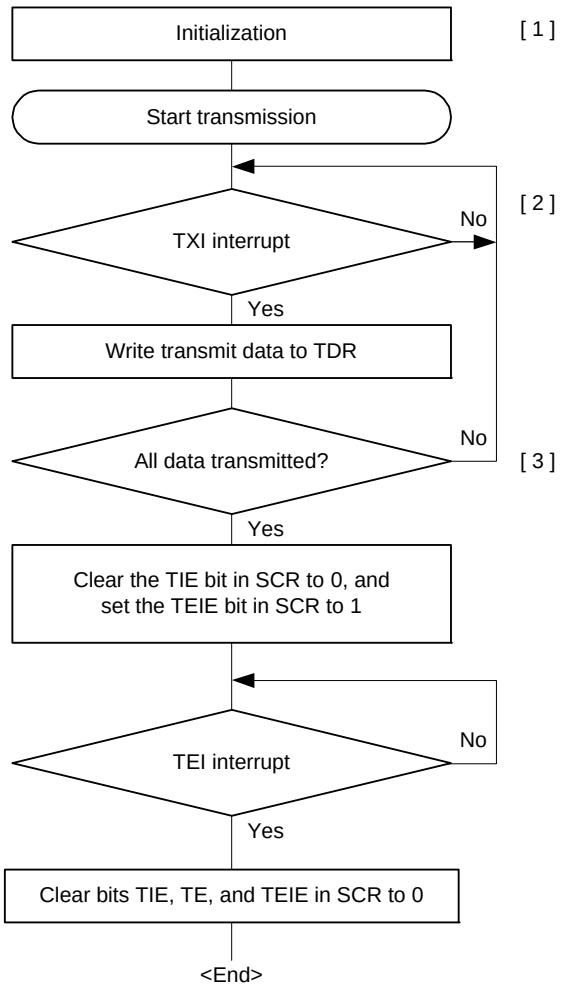
1. The SCI transfers data from TDR to TSR when data is written to TDR in the TXI interrupt processing routine. The TXI interrupt request at the beginning of transmission is generated when the TE bit in SCR is set to 1 after the TIE bit in SCR is set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the SCR.TIE bit is set to 1 at this time, a TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in this TXI interrupt processing routine before transmission of the current transmit data has finished. When TEI interrupt requests are in use, set the SCR.TIE bit to 0 (disabling TXI requests) and the SCR.TEIE bit to 1 (enabling TEI requests) after the last of the data to be transmitted are written to the TDR from the processing routine for TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when clock output mode has been specified and in synchronization with the input clock when use of an external clock has been specified. Output of the clock signal is suspended until the input CTS signal is at the low level while the CTSE bit in SPMR is 1 (enabling the CTS function).
4. The SCI checks for updating of (writing to) the TDR at the time of the last bit output.
5. When TDR is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame is started.
6. If TDR is not updated, set the SSR flag in TEND to 1 and the TXDn pin retains the output state of the last bit. If the TEIE bit in SCR is 1 at this time, a TEI interrupt request is generated. The SCKn pin is held high.

Figure 29.22 shows a sample flowchart of serial data transmission.
Transmission will not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Be sure to clear the receive error flags to 0 before starting transmission. Note that clearing the RE bit in SCR to 0 does not clear the receive error flags.



Note 1. Refer to Section 15, Interrupt Controller (ICUb) for the corresponding interrupt vector number.

Figure 29.21 Example of Operation for Serial Transmission in Clock Synchronous Mode (from the Middle of Transmission until Transmission Completion)



[1] SCI initialization:
The TXDn automatically becomes the output pin for data being transmitted.

[2] Writing transmit data write to TDR by a TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (TXI) request is generated.
Transmit data is written to TDR once from the processing routine for TXI requests.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR upon accepting a transmit data empty interrupt (TXI). Transmit data can also be written to TDR by activating the DMAC or DTC by the TXI interrupt request.

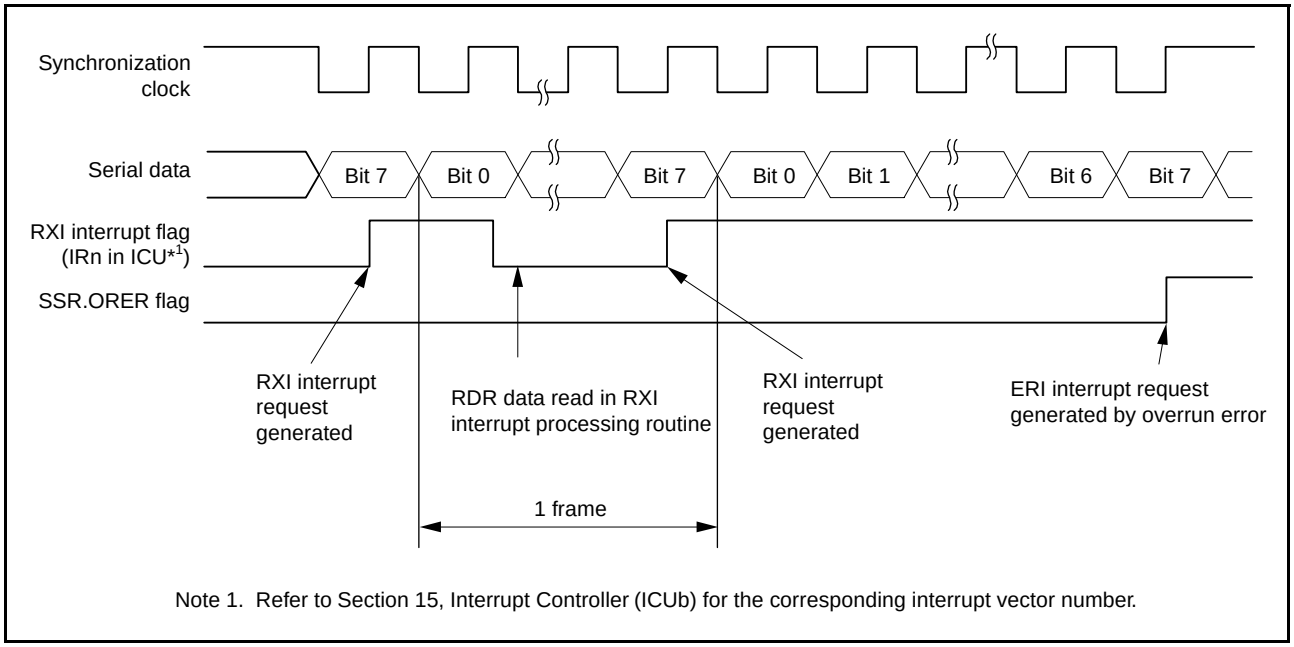
Note: • When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR.TEND flag to 1. Clearing the SCR.TE bit to 0 immediately after this may lead to insufficient received-data hold time on the receiver side.

Figure 29.22 Example of Serial Transmission Flowchart (Clock Synchronous Mode)

29.5.5 Serial Data Reception (Clock Synchronous Mode)

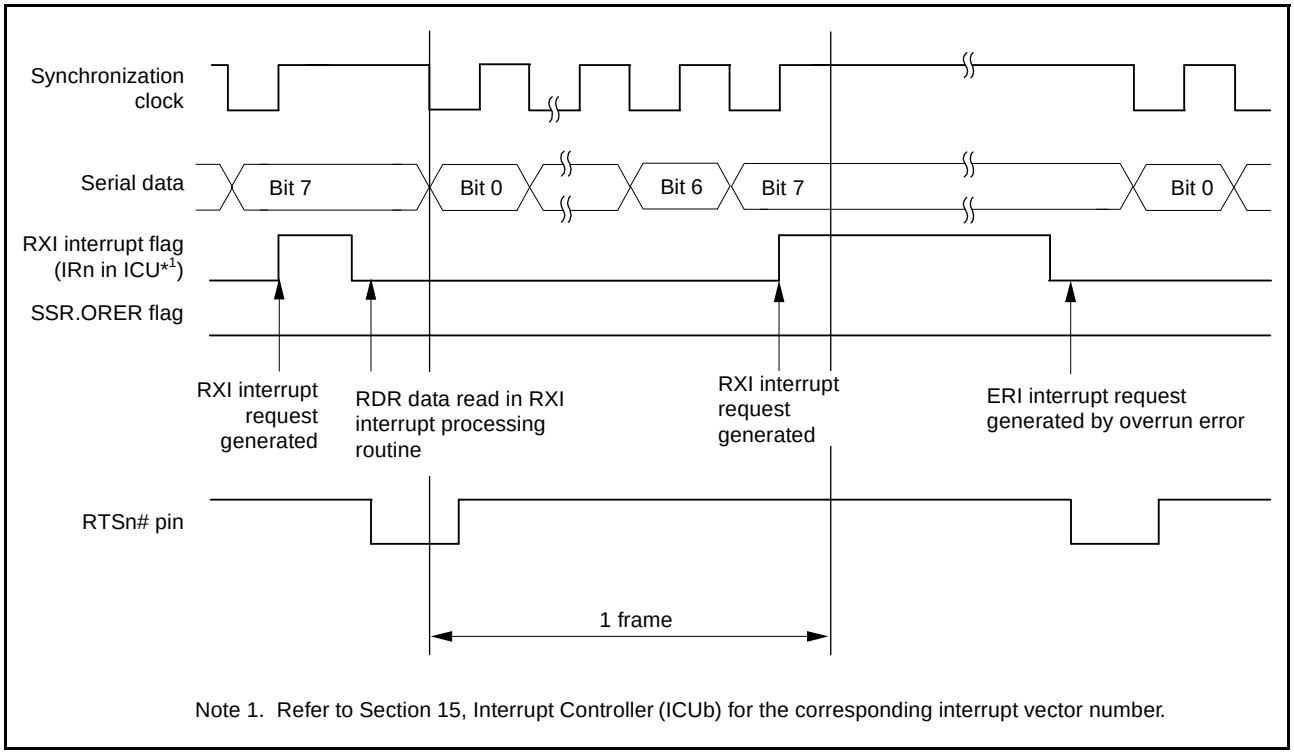
Figure 29.23 and Figure 29.25 show examples of SCI operation for serial reception in clock synchronous mode. In serial data reception, the SCI operates as described below.

1. The value of the RE bit in SCR becoming 1 places the signal output on the RTS pin at the low level (when the RTS function is in use).
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in RSR.
3. If an overrun error occurs, the ORER bit in SSR is set to 1. If the RIE bit in SCR is 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR.
4. When reception finishes successfully, receive data is transferred to RDR. If the RIE bit in SCR is 1 at this time, an RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to RDR in this RXI interrupt processing routine before reception of the next receive data is completed. Reading out the received data that have been transferred to RDR causes the RTSn# pin to output the low level (when the RTS function is in use).



Note 1. Refer to Section 15, Interrupt Controller (ICUb) for the corresponding interrupt vector number.

Figure 29.23 Example of Operation for Serial Reception in Clock Synchronous Mode (1) (when RTS Function is not Used)

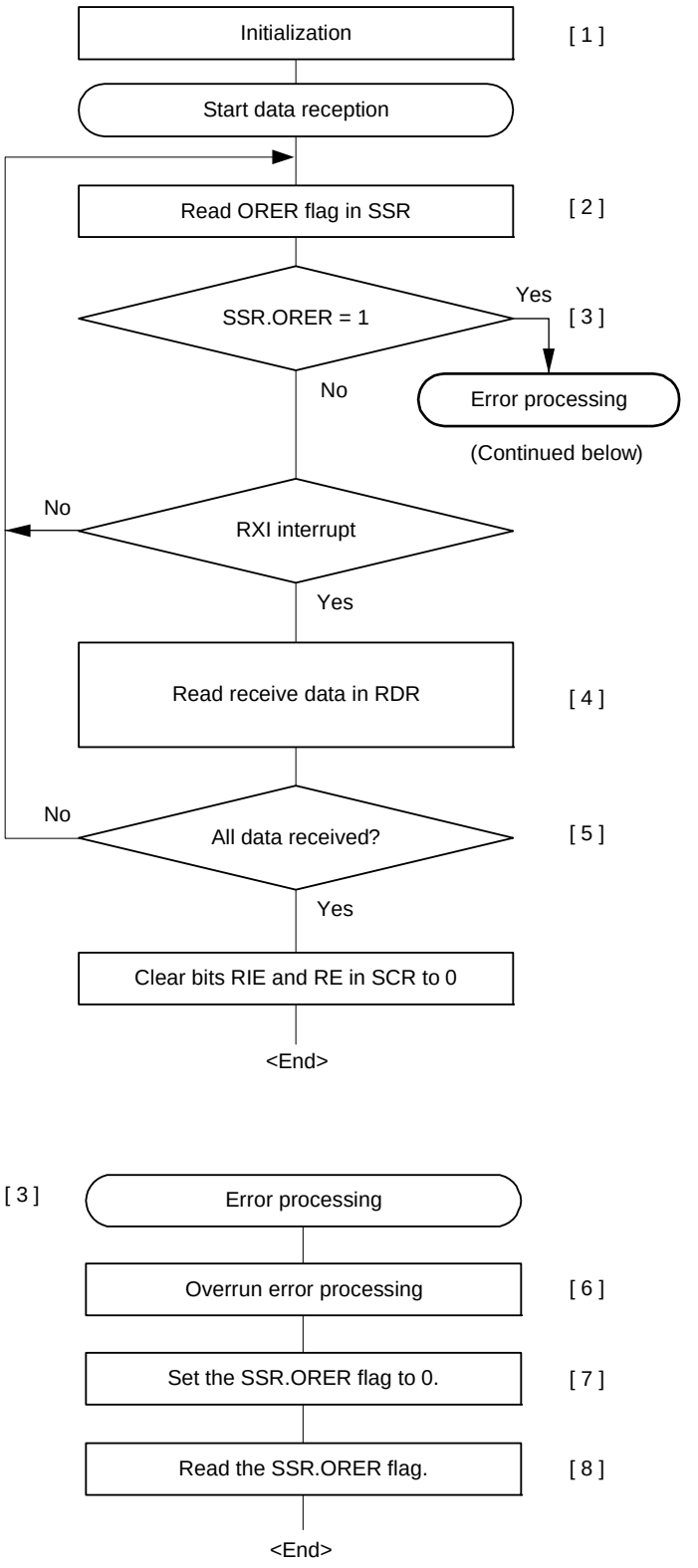


Note 1. Refer to Section 15, Interrupt Controller (ICUb) for the corresponding interrupt vector number.

Figure 29.24 Example of Operation for Serial Reception in Clock Synchronous Mode (2) (when RTS Function is Used)

Data transfer cannot be resumed while a receive error flag is 1. Accordingly, clear the ORER, FER, and PER bits in SSR to 0 before resuming reception. Moreover, be sure to read the RDR during overrun error processing. Read the RDR also when the SCR.RE bit is set to 0 during reception to forcibly stop the receive operation because unread receive data may remain in the RDR register.

Figure 29.25 shows a sample flowchart for serial data reception.



[1] SCI initialization:
Make input port-pin settings for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, and then clear the ORER flag to 0. Data reception cannot be resumed while the ORER flag is 1.

[4] Read the receive data in RDR once in the receive data full interrupt (RXI) request processing routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, finish reading the receive data in RDR. The RDR data can also be read by activating the DMAC or DTC by an RXI interrupt request.

[6] Processing in response to an overrun error:
Read the RDR. In combination with step [7], this enables normal reception of a next frame.

[7] Clearing the error flag:
Set the error flag to 0.

[8] Confirming that the error flag is actually clear:
Confirm that the error flag has actually been cleared to 0.

Figure 29.25 Example of Serial Reception Flowchart (Clock Synchronous Mode)

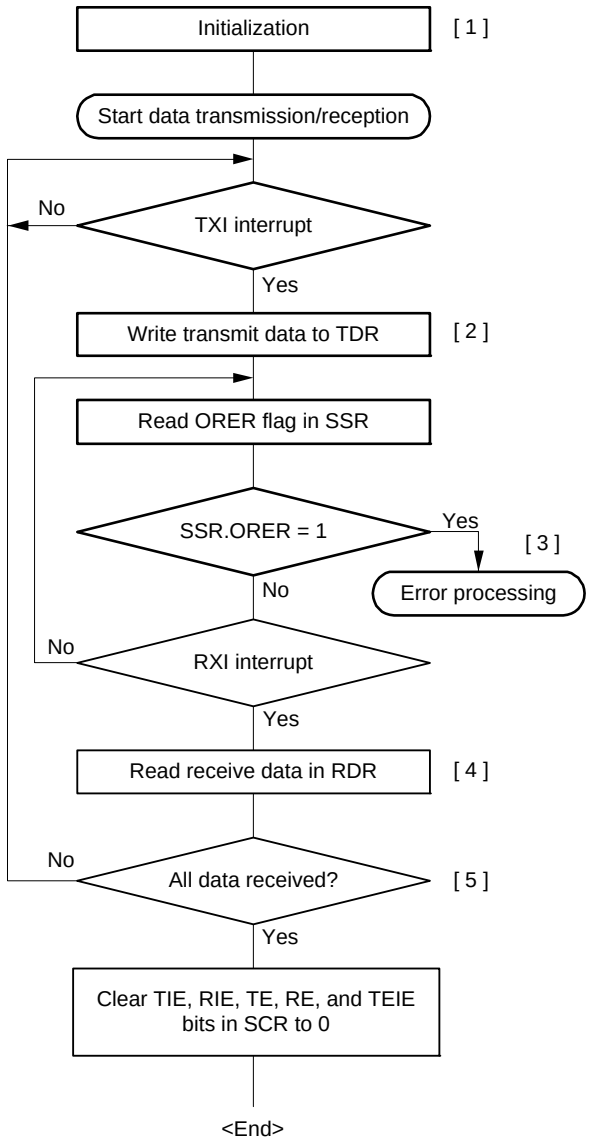
29.5.6 Simultaneous Serial Data Transmission and Reception (Clock Synchronous Mode)

Figure 29.26 shows a sample flowchart for simultaneous serial transmit and receive operations in clock synchronous mode.

After initializing the SCI, the following procedure should be used for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode, check that the SCI has finished transmission by reading that the TEND flag in SSR is 1, and then initialize the SCR register. Then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode, check that the SCI has finished reception, and then clear the RIE and RE bits to 0. Then check that the receive error flags (ORER, FER, and PER in SSR) are 0, and then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR once in the TXI interrupt request processing routine.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, and then clear the ORER flag to 0. Data reception cannot be resumed while the ORER flag is 1.

[4] Reading receive data:
Read the receive data in RDR once in the RXI interrupt request processing routine.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB (bit 7) of the current frame is received, finish reading the receive data in RDR by the RXI interrupt. Also, before the MSB (bit 7) of the current frame is transmitted, write data to TDR by the TXI interrupt.
Transmit data can also be written to TDR by activating the DMAC or DTC by a transmit data empty interrupt (TXI) request. Similarly, the RDR data can also be read by activating the DMAC or DTC by a receive data full interrupt (RXI) request.

Note: • When switching from transmit or receive operation to simultaneous transmit and receive operations, first clear the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, and then set TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 29.26 Example of Simultaneous Serial Transmission and Reception Flowchart (Clock Synchronous Mode)

29.6 Operation in Smart Card Interface Mode

The SCI supports the smart card (IC card) interface conforming to the ISO/IEC 7816-3 (Identification Card) standard, as an extended function of the SCI.
Smart card interface mode can be selected using the appropriate register.

29.6.1 Sample Connection

Figure 29.27 shows a sample connection between a smart card (IC card) and this MCU.
As in the figure, since this MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to Vcc using a resistor.
Setting the TE and RE bits in SCR to 1 with an IC card disconnected enables closed transmission/reception allowing self-diagnosis.
To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.
The output port of this MCU can be used to output a reset signal.

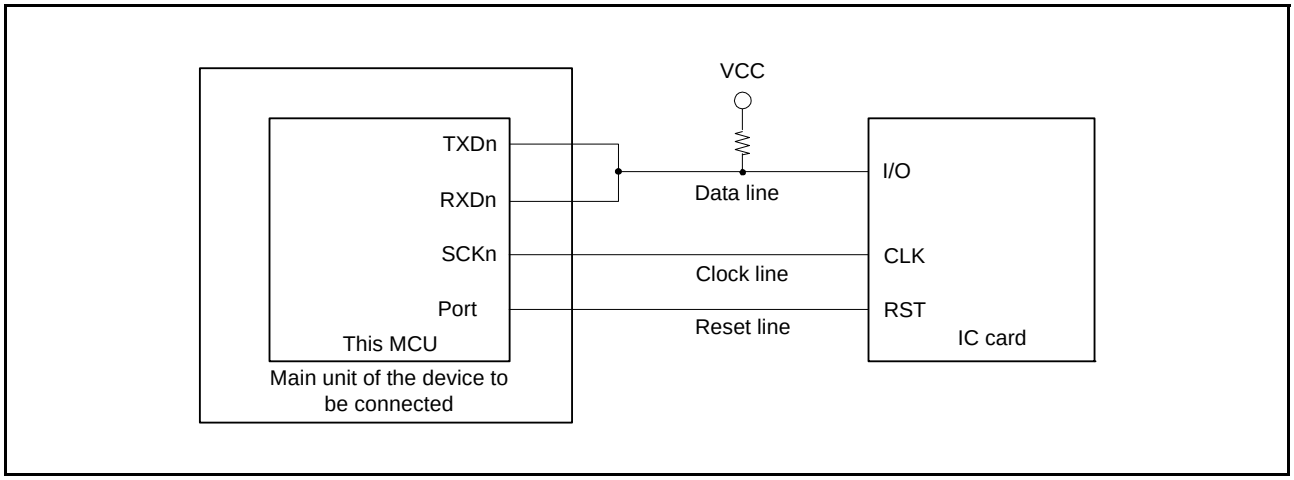


Figure 29.27 Sample Connection with a Smart Card (IC Card)

29.6.2 Data Format (Except in Block Transfer Mode)

Figure 29.28 shows the data transfer formats in smart card interface mode.

- One frame consists of 8-bit data and a parity bit in asynchronous mode.
- During transmission, at least 2 etu (elementary time unit: time required for transferring one bit) is secured as a guard time from the end of the parity bit until the start of the next frame.
- If a parity error is detected during reception, a low-level error signal is output for 1 etu after 10.5 etu has passed from the start bit.
- If an error signal is sampled during transmission, the same data is automatically re-transmitted after at least 2 etu.

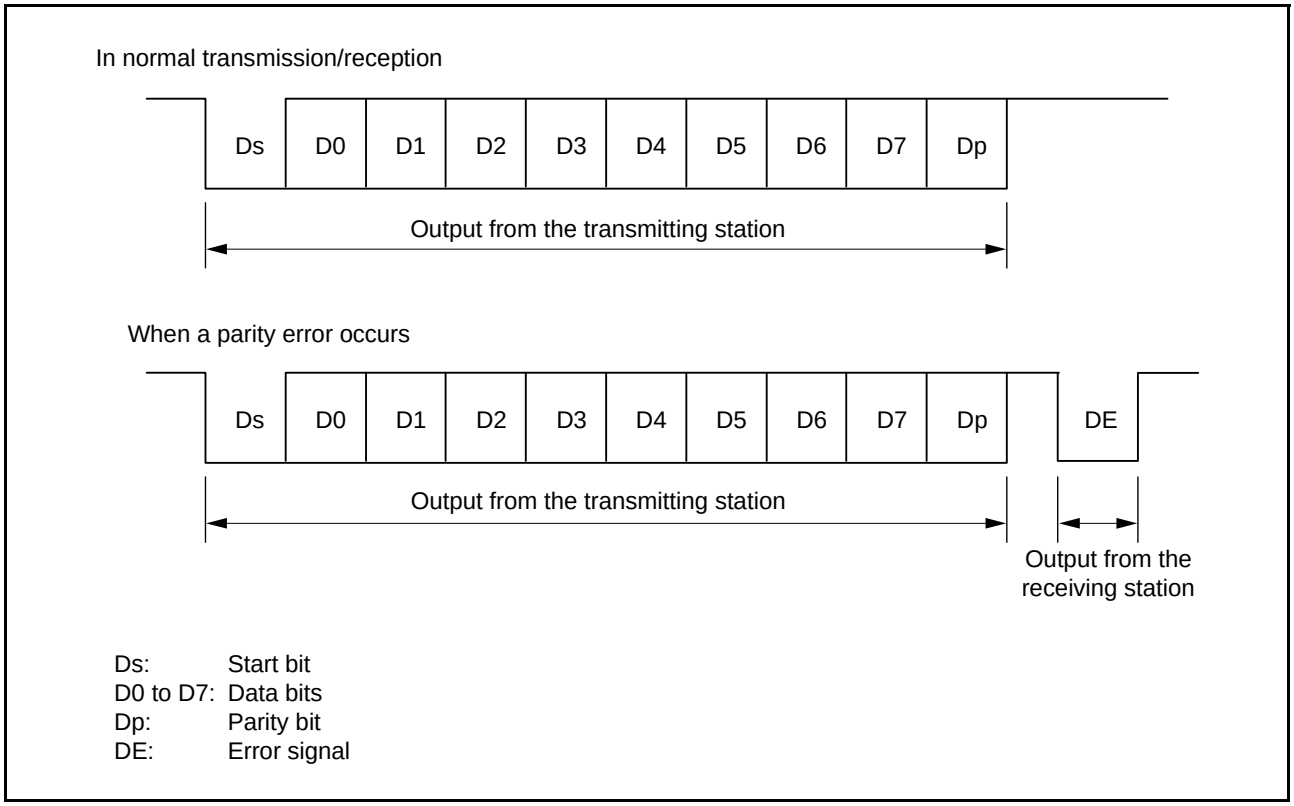


Figure 29.28 Data Formats in Smart Card Interface Mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedure below.

(1) Direct Convention Type

For the direct convention type, logic levels 1 and 0 correspond to states Z and A, respectively, and data is transferred with LSB-first as the start character, as shown in Figure 29.29. Therefore, data in the start character in the figure is 3Bh. When using the direct convention type, write 0 to both the SDIR and SINV bits in SCMR. Write 0 to the PM bit in SMR in order to use even parity, which is prescribed by the smart card standard.

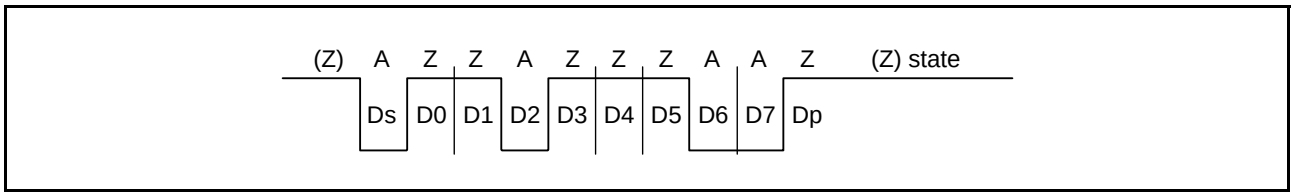


Figure 29.29 Direct Convention (SDIR in SCMR = 0, SINV in SCMR =0, PM in SMR = 0)

(2) Inverse Convention Type

For the inverse convention type, logic levels 1 and 0 correspond to states A and Z, respectively and data is transferred with MSB-first as the start character, as shown in Figure 29.30. Therefore, data in the start character in the figure is 3Fh. When using the inverse convention type, write 1 to both the SDIR and SINV bits in SCMR. The parity bit is logic level 0 to produce even parity, which is prescribed by the smart card standard, and corresponds to state Z. Since the SINV bit of the RX63T only inverts data bits D7 to D0, write 1 to the PM bit in SMR to invert the parity bit for both transmission and reception.

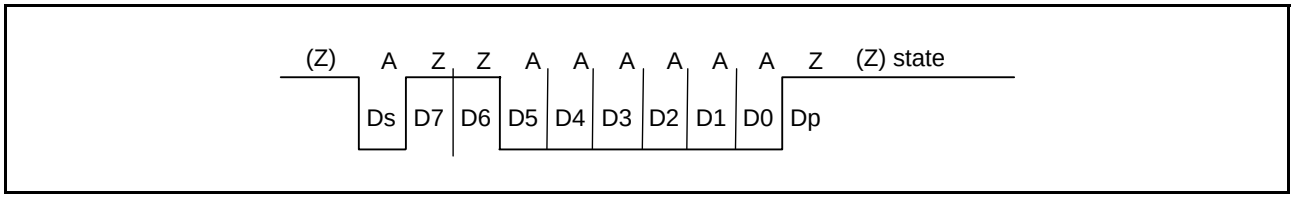


Figure 29.30 Inverse Convention (SDIR in SCMR = 1, SINV in SCMR =1, PM in SMR = 1)

29.6.3 Block Transfer Mode

Block transfer mode is different from normal smart card interface mode in the following respects.

- Even if a parity error is detected during reception, no error signal is output. Since the PER bit in SSR is set by error detection, clear the PER bit before receiving the parity bit of the next frame.
- During transmission, at least 1 etu is secured as a guard time from the end of the parity bit until the start of the next frame.
- Since the same data is not re-transmitted during transmission, the TEND flag in SSR is set 11.5 etu after transmission start.
- In block transfer mode, the ERS flag in SSR indicates the error signal status as in normal smart card interface mode, but the flag is always read as 0 because no error signal is transferred.

29.6.4 Receive Data Sampling Timing and Reception Margin

Only the internal clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate according to the settings of the BCP2 bit in SCMR and the BCP[1:0] bits in SMR (the frequency is always 16 times the bit rate in normal asynchronous mode).

For data reception, the falling edge of the start bit is sampled with the base clock to perform internal synchronization. Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 29.31. The reception margin here is determined by the following formula.

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\left| D - 0.5 \right|}{N}\ (1+F) \right| \times 100\ [\%]$$

M: Reception margin (%)
N: Ratio of bit rate to clock (N = 32, 64, 372, 256)
D: Duty cycle of clock (D = 0 to 1.0)
L: Frame length (L = 10)
F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the above formula, the reception margin is determined by the formula below.

$$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\%$$

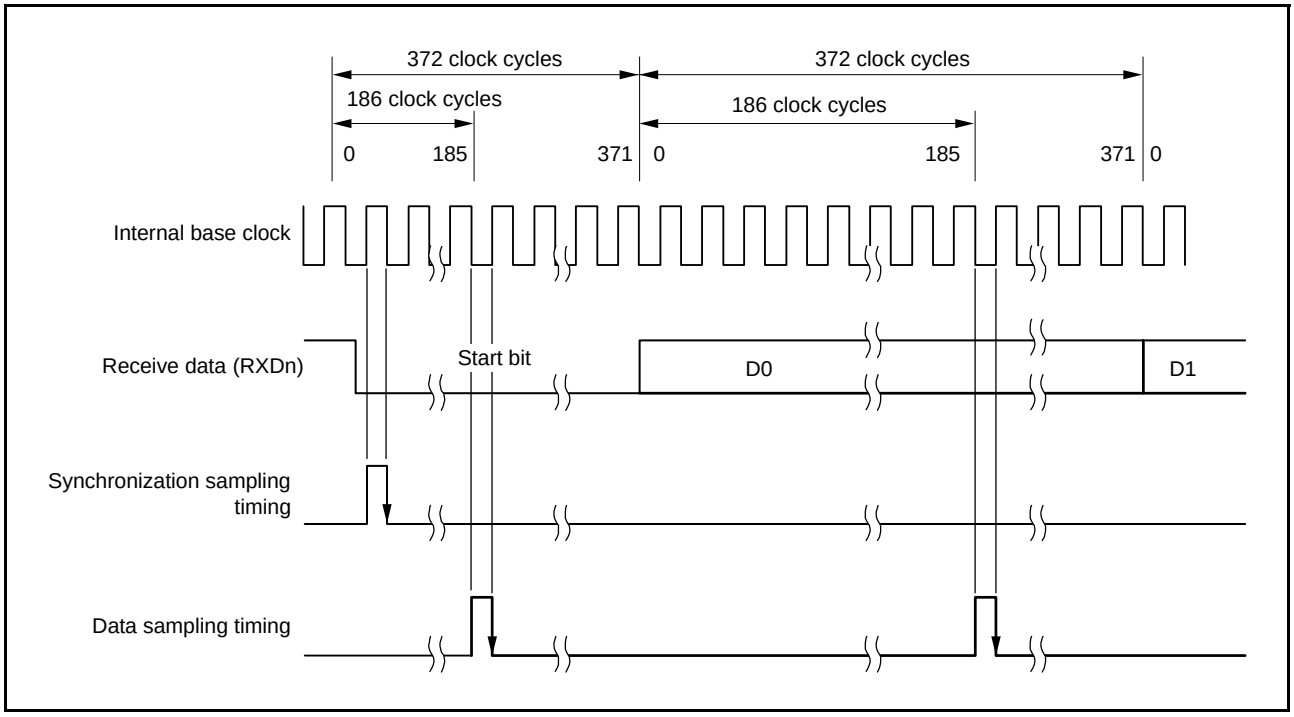


Figure 29.31 Receive Data Sampling Timing in Smart Card Interface Mode (When Clock Frequency is 372 Times the Bit Rate)

29.6.5 Initialization of the SCI (Smart Card Interface Mode)

Before transmitting and receiving data, initialize the SCI using the following procedure. Initialization is also necessary before switching from transmission to reception and vice versa.

1. Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0.
2. Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
3. Set the error flags ORER, ERS, and PER in SSR to 0.
4. Clear the SIMR1.IICM bit and the SPMR.CKPH and CKPOL bits to 0.
   This step can be skipped if the values have not been changed from the initial values.
5. Set bits GM, BLK, OE, BCP[1:0], and CKS[1:0] in SMR and the BCP2 bit in SCMR appropriately. Also set the PE bit in SMR to 1.
6. Set bits SDIR, SINV, and SMIF in SCMR appropriately. Then, the TXDn and RXDn pins are placed in the high impedance state.
7. Set the value corresponding to the bit rate in BRR.
8. Set the CKE[1:0] bits in SCR appropriately, and set bits TIE, RIE, TE, RE, and TEIE in SCR to 0 at the same time. When the CKE[1:0] bit is set to 1, the SCKn pin is allowed to output clock pulses.
9. Set the TIE, RIE, TE, and RE bits in SCR to 1. Setting the TE and RE bits to 1 simultaneously is prohibited except for self-diagnosis.

To change reception mode to transmission mode, first check that reception has completed, and then initialize the SCI. At the end of initialization, set TE = 1 and RE = 0. Reception completion can be verified by reading the RXI request, ORER, or PER flag in SSR.
To change transmission mode to reception mode, first check that transmission has completed, and then initialize the SCI. At the end of initialization, set TE = 0 and RE = 1. Transmission completion can be verified by reading the TEND flag in SSR.

29.6.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode), in that an error signal is sampled and data can be re-transmitted, is different from that in normal serial communications interface mode. Figure 29.32 shows the data retransfer operation during transmission.

1. When an error signal from the receiver end is sampled after one-frame data has been transmitted, the ERS flag in SSR is set to 1. If the RIE bit in SCR is 1 at this time, an ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
2. For a frame in which an error signal is received, the TEND flag in SSR is not set. Data is retransferred from TDR to TSR allowing automatic data retransmission.
3. If no error signal is returned from the receiver, the ERS flag is not set to 1.
4. In this case, the SCI judges that transmission of one-frame data (including retransfer) has been completed, and the TEND flag is set. If the TIE bit in SCR is 1 at this time, a TXI interrupt request is generated. Writing transmit data to TDR starts transmission of the next data.

Figure 29.34 shows a sample flowchart of serial transmission. All the processing steps are automatically performed using a TXI interrupt request to activate the DTC or DMAC.
When the TEND flag in SSR is set to 1 in transmission, if the TIE bit in SCR is 1, a TXI interrupt request is generated. The DTC or DMAC is activated by a TXI interrupt request if the TXI interrupt request is specified as a source of DTC or DMAC activation beforehand, allowing transfer of transmit data. The TEND flag is automatically cleared to 0 when the DTC or DMAC transfers the data.
If an error occurs, the SCI automatically re-transmits the same data. During this retransmission, the TEND flag is kept to 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission in the case of error occurrence. However, since the ERS flag is not automatically cleared, set the RIE bit to 1 beforehand to enable an ERI interrupt request to be generated at error occurrence, and clear the ERS flag to 0.
When transmitting/receiving data using the DTC or DMAC, be sure to make settings to enable the DTC or DMAC before making SCI settings.
For DTC or DMAC settings, see section 18, DMA Controller (DMACA) and section 19, Data Transfer Controller (DTCa).

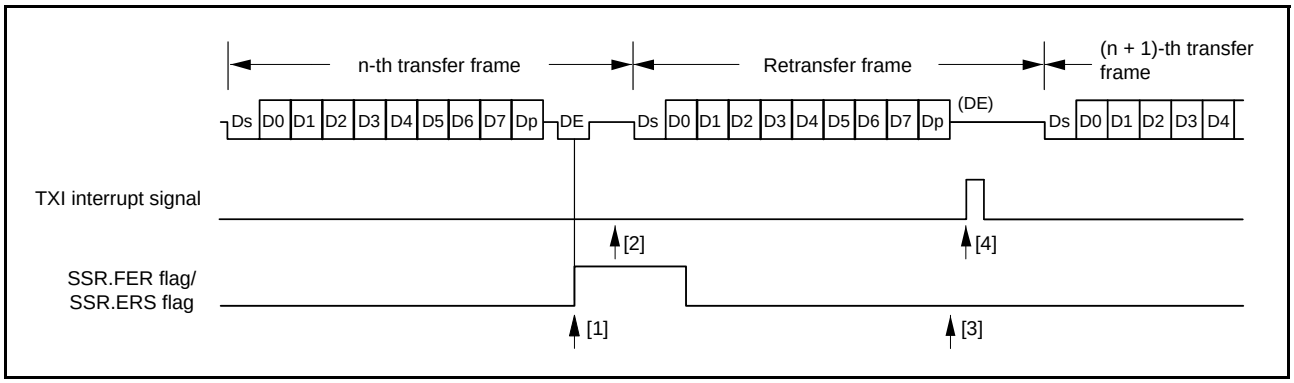


Figure 29.32 Data Retransfer Operation in SCI Transmission Mode

Note that the SSR.TEND flag is set in different timings depending on the GM bit setting in SMR. Figure 29.33 shows the TEND flag generation timing.

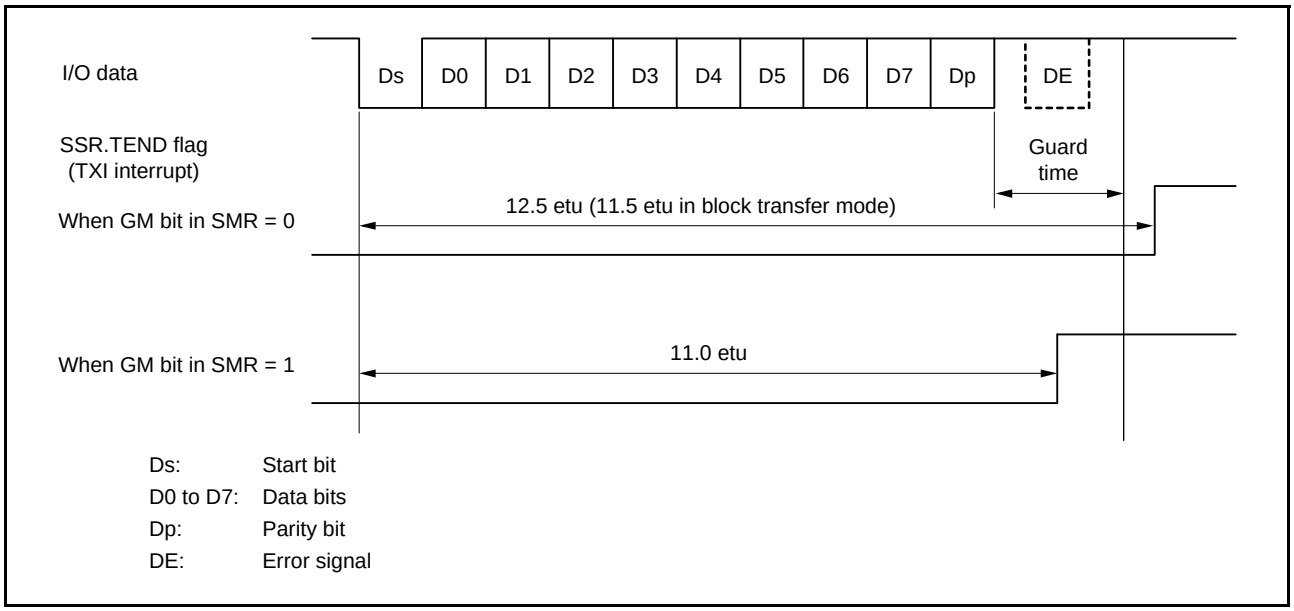


Figure 29.33 SSR.TEND Flag Generation Timing during Transmission

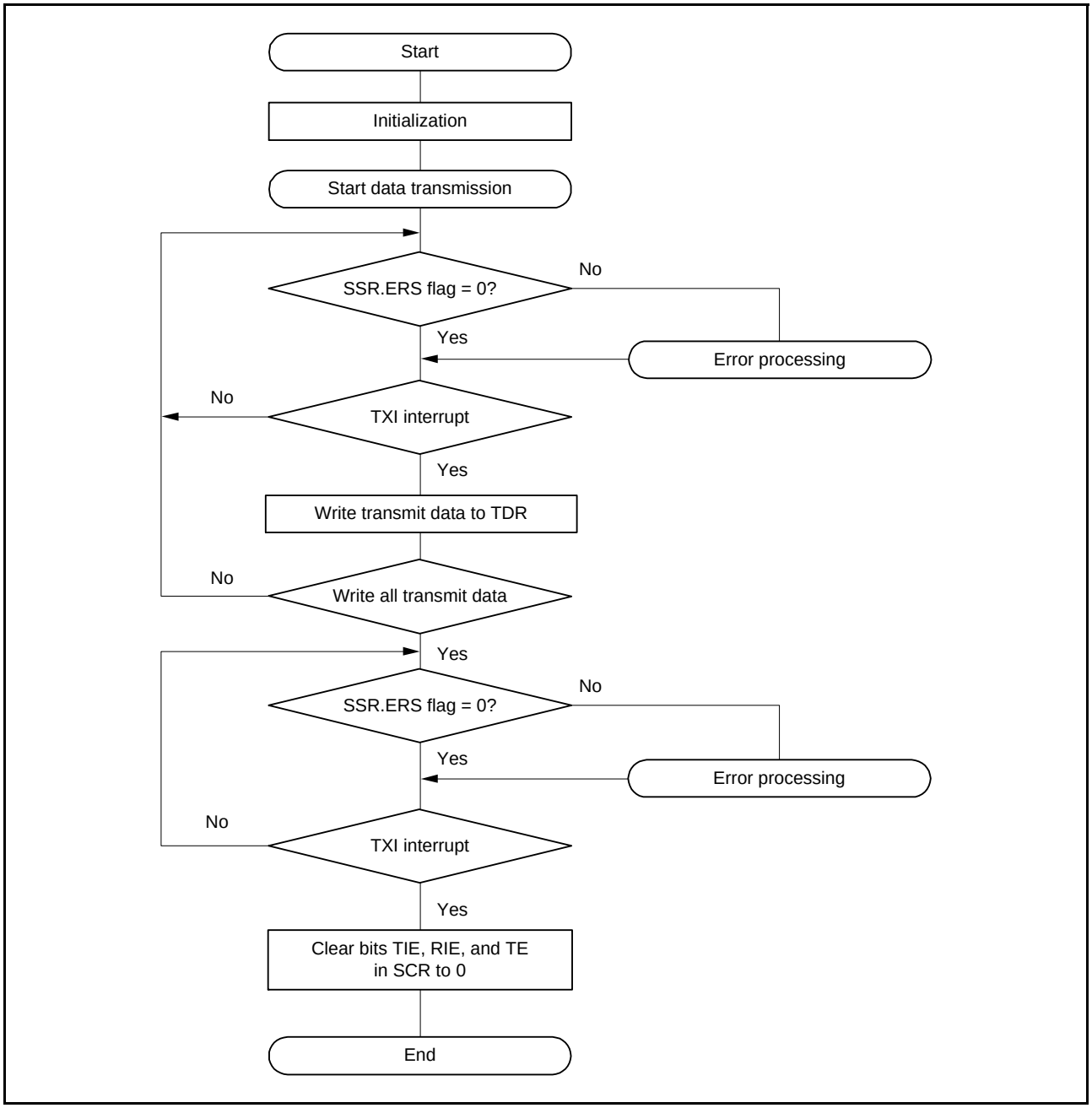


Figure 29.34 Sample Smart Card Interface Transmission Flowchart

29.6.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in serial communications interface mode. Figure 29.35 shows the data retransfer operation in reception mode.

1. If a parity error is detected in receive data, the PER flag in SSR is set to 1. When the RIE bit in SCR is 1 at this time, an ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
2. For a frame in which a parity error is detected, no RXI interrupt is generated.
3. When no parity error is detected, the PER flag in SSR is not set to 1.
4. In this case, data is determined to have been received successfully. When the RIE bit in SCR is 1, an RXI interrupt request is generated.

Figure 29.36 shows a sample flowchart for serial data reception. All the processing steps are automatically performed using an RXI interrupt request to activate the DTC or DMAC.
In reception, setting the RIE bit to 1 allows an RXI interrupt request to be generated. The DTC or DMAC is activated by an RXI interrupt request if the RXI interrupt request is specified as a source of DTC or DMAC activation beforehand, allowing transfer of receive data.
If an error occurs during reception and either the ORER or PER flag in SSR is set to 1, a receive error interrupt (ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC or DMAC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC or DMAC is transferred. Even if a parity error occurs and the PER flag is set to 1 during reception, receive data is transferred to RDR, thus allowing the data to be read.
Note 1. For operations in block transfer mode, see section 29.3, Operation in Asynchronous Mode.

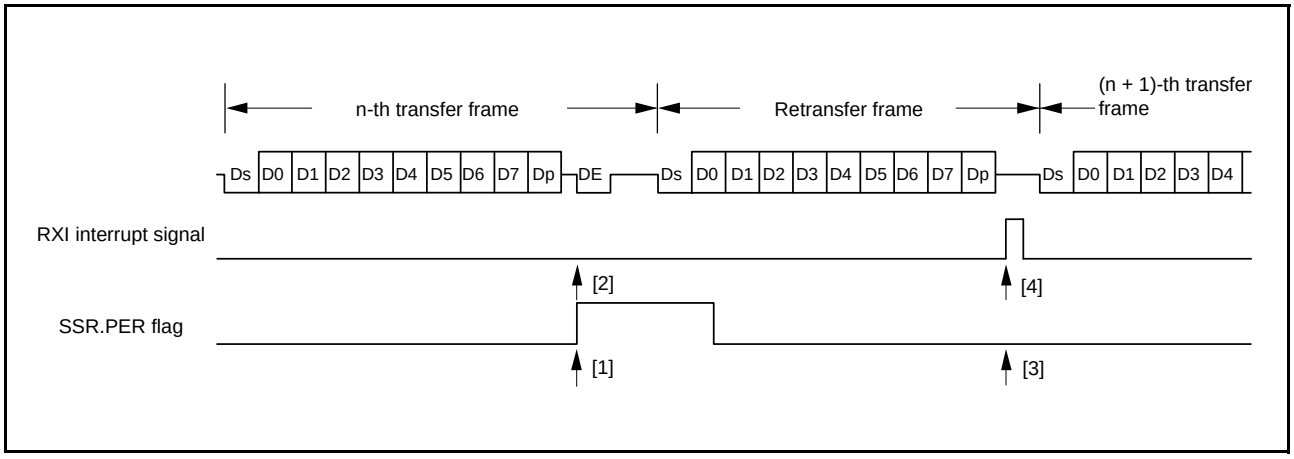


Figure 29.35 Data Retransfer Operation in SCI Reception Mode

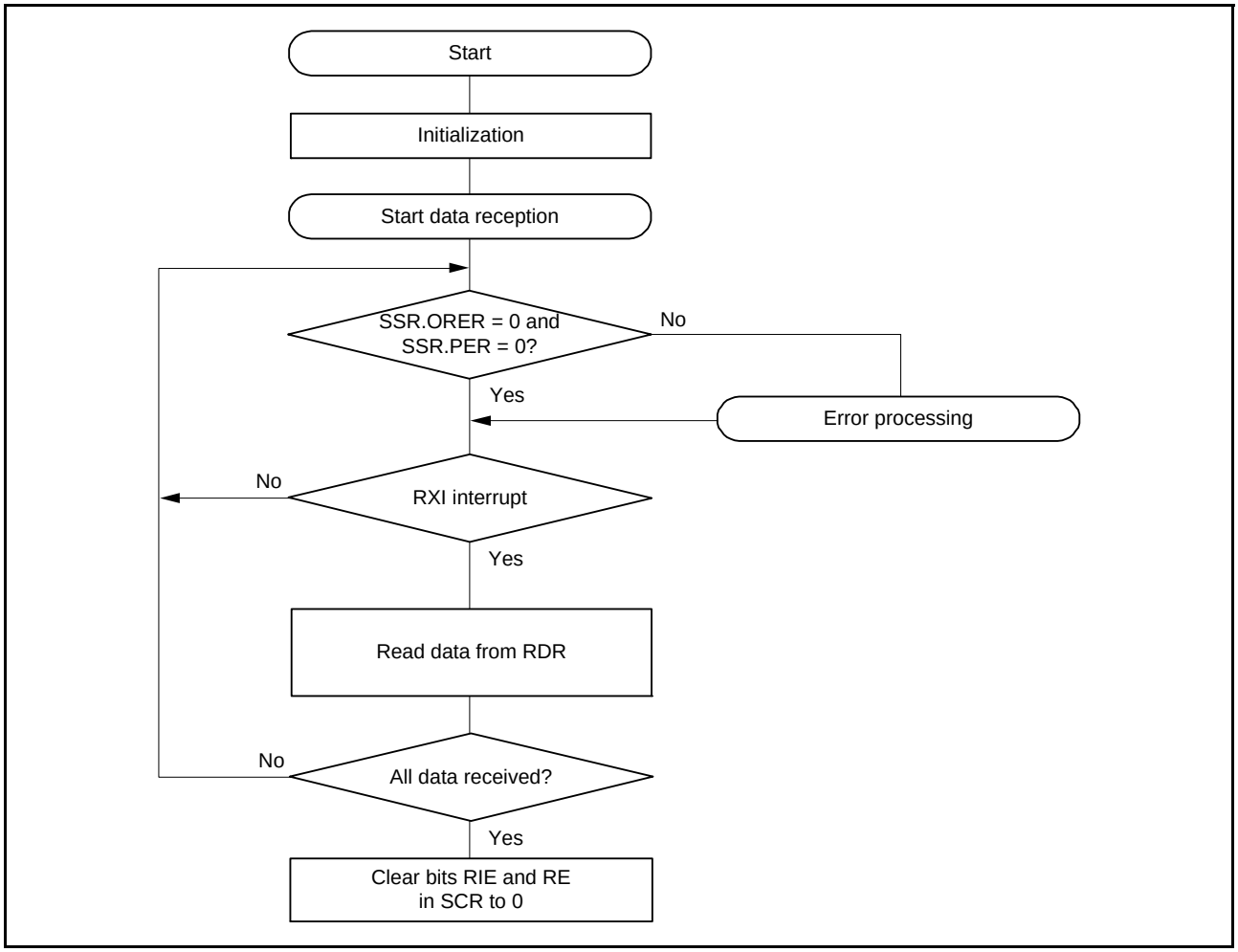


Figure 29.36 Sample Smart Card Interface Reception Flowchart

29.6.8 Clock Output Control

Clock output can be fixed using the CKE[1:0] bits in SCR when the GM bit in SMR is 1. Specifically, the minimum width of a clock pulse can be specified.

Figure 29.37 shows an example of clock output fixing timing when the CKE0 bit is controlled with GM = 1 and CKE1 = 0.

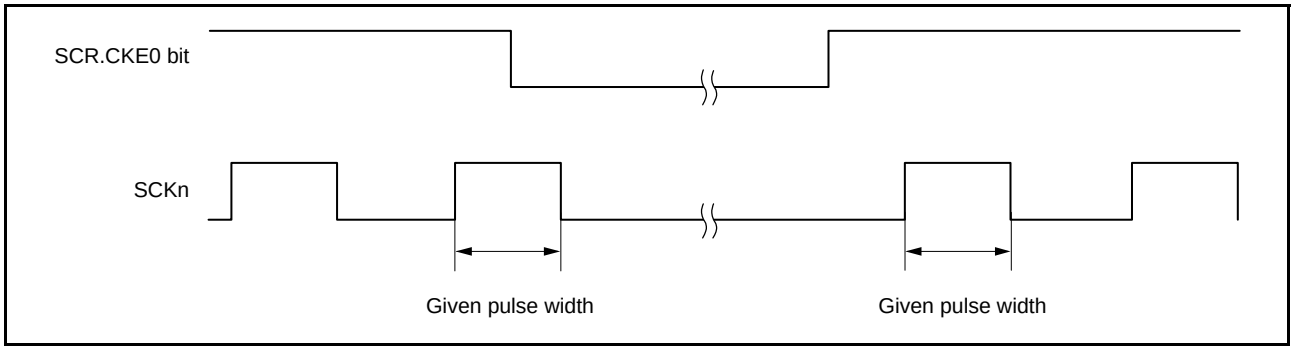


Figure 29.37 Clock Output Fixing Timing

At power-on and transitions to/from software standby mode, use the following procedure to secure the appropriate clock duty cycle.

(1) At Power-On

To secure the appropriate clock duty cycle simultaneously with power-on, use the following procedure.

1. Initially, port input is enabled in the high-impedance state. To fix the potential level, use a pull-up or pull-down resistor.
2. Fix the SCKn pin to the specified output by setting the SCR.CKE[1] bit and I/O port functions.
3. Set SMR and SCMR to enable smart card interface mode.
4. Set the SCR.CKE[0] bit to 1 to start clock output.

(2) At Mode Switching

(a) At transition from smart card interface mode to software standby mode

1. Set I/O port functions to make the SCKn pin fixed with a desired output value in software standby mode.
2. Write 0 to the TE and RE bits in SCR to stop transmission/reception.
   Simultaneously, set the SCR.CKE[1] bit to the value for the output fixed state in software standby mode.
3. Write 0 to the SCR.CKE[0] bit to stop the clock.
4. Wait for one cycle of the serial clock. In the mean time, the clock output is fixed to the specified level with the duty cycle retained.
5. After switching the SCKn pin to the general I/O port function, make a transition to software standby mode.

(b) Return from software standby mode to smart card interface mode

6. Cancel software standby mode.
7. Set the SCR.CKE[0] bit to 1 to start clock output. A clock signal with the appropriate duty cycle is then generated.

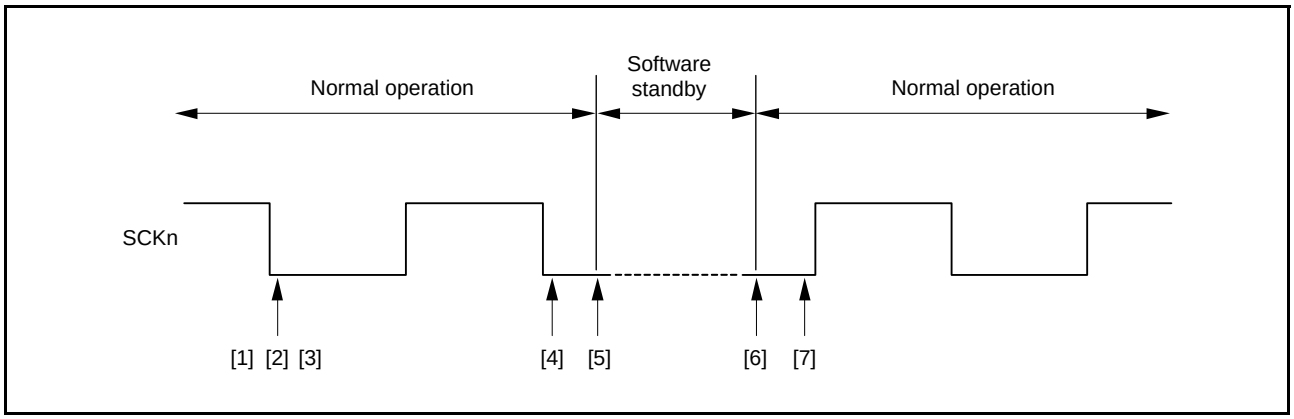


Figure 29.38 Clock Stop and Restart Procedure

29.7 Operation in Simple I²C Mode

Simple I²C bus master format is composed of eight data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device is able to specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The eight data bits in all frames are transmitted in order from the MSB.
The I²C format and timing of the I²C bus are shown in Figure 29.39 and Figure 29.40.

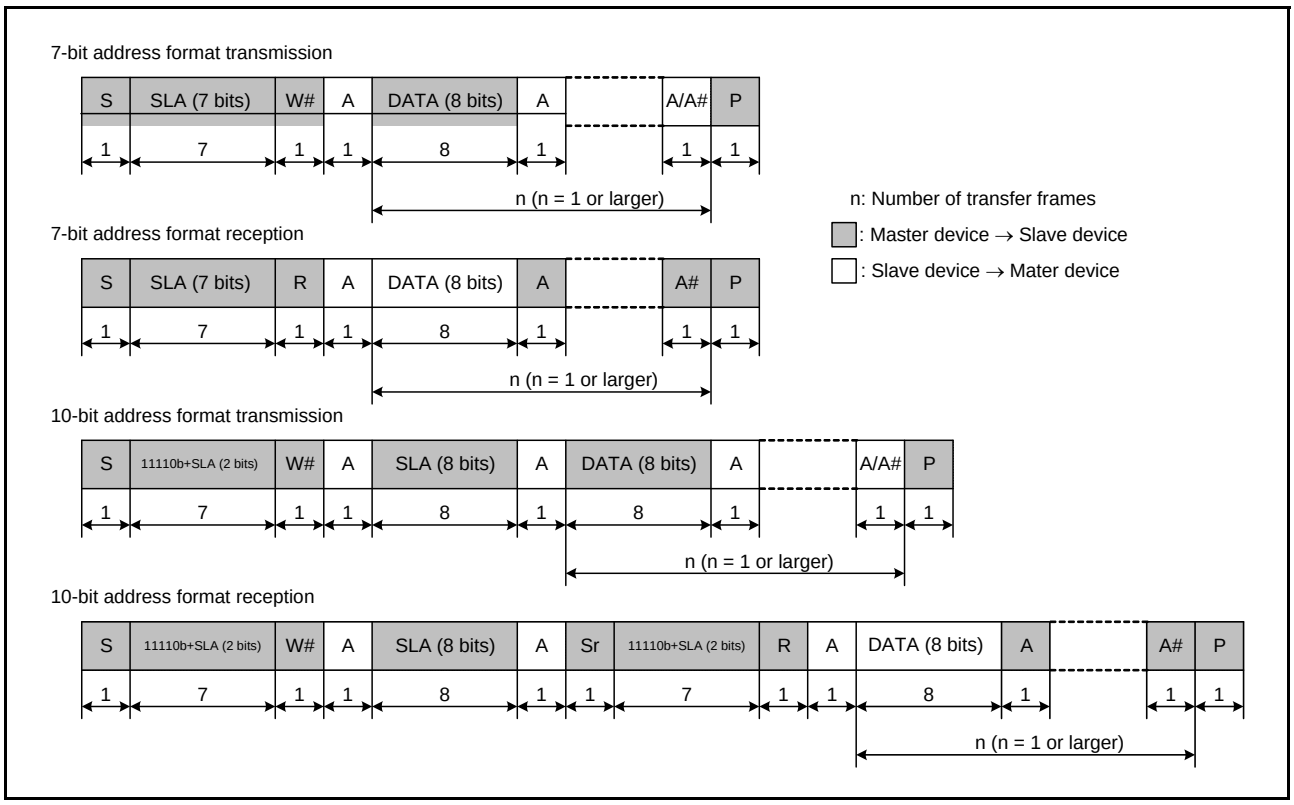


Figure 29.39 I²C Bus Master Format

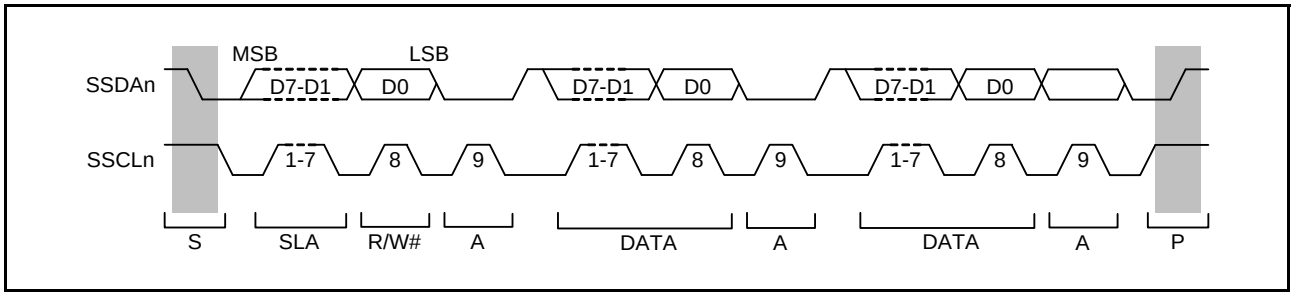


Figure 29.40 I²C Bus Timing (When SLA is 7 Bits)

S: Indicates a start condition, i.e. the master device changing the level on the SSDAn line from the high to the low level while the SSCLn line is at the high level.

SLA: Indicates a slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of transfer (reception or transmission). The value 1 corresponds to transfer from the slave device to the master device and 0 corresponds to transfer from the master device to the slave device.

A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return of the low level indicates ACK and return of the high level indicates NACK.

Sr: Indicates a restart condition, i.e. the master device changing the level on the SSDAn line from the high to the low level while the SSCLn line is at the high level and after the setup time has elapsed.

DATA: Indicates the data being received or transmitted.

P: Indicates a stop condition, i.e. the master device changing the level on the SSDAn line from the low to the high level while the SSCLn line is at the high level.

29.7.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the IICSTAREQ bit in SIMR3 causes the generation of a start condition. The generation of a start condition proceeds through the following operations.

- The level on the SSDAn line falls (from the high level to the low level) and the SSCLn line is kept in the released state.
- The hold time for the start condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The level on the SSCLn line falls (from the high level to the low level), the IICSTAREQ bit in SIMR3 is cleared (to 0), and a start-condition generated interrupt is output.

Writing 1 to the IICSTPREQ bit in SIMR3 causes the generation of a start condition. The generation of a start condition proceeds through the following operations.

- The SSDAn line is released and the SSCLn line is kept at the low level.
- The period at low level for the SSCLn line is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The SSCLn line is released (transition from the low to the high level).
- Once the high level on the SSCLn line is detected, the setup time for the restart condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The level on the SSDAn line falls (from the high level to the low level).
- The hold time for the restart condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The level on the SSCLn line falls (from the high level to the low level), the IICRSTAREQ bit in SIMR3 is cleared (to 0), and a restart-condition generated interrupt is output.

Writing 1 to the IICSTPREQ bit in SIMR3 causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations.

- The level on the SSDAn line falls (from the high level to the low level) and the SSCLn line is kept at the low level.
- The period at low level for the SSCLn line is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The SSCLn line is released (transition from the low to the high level).
- Once the high level on the SSCLn line is detected, the setup time for the stop condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The SSDAn is released (transition from the low to the high level), the IICSTPREQ bit in SIMR3 is cleared (to 0), and a stop-condition generated interrupt is output.

Figure 29.41 shows the timing of operations in the generation of start, restart, and stop conditions.

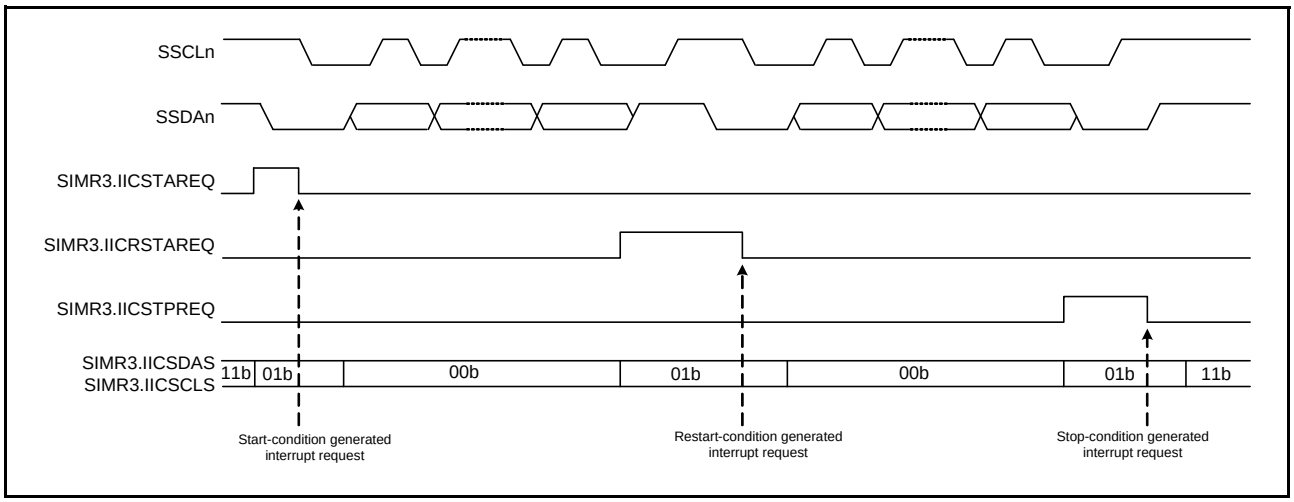


Figure 29.41 Timing of Operations in the Generation of Start, Restart, and Stop Conditions

29.7.2 Clock Synchronization

The SSCLn line may be placed at the low level in the case of a wait inserted by a slave device as the other side of transfer. Setting the IICCSC bit in SIMR2 to 1 applies control to obtain synchronization when the levels of the internal SSCLn clock signal and the level being input on the SSCLn pin differ.

When the IICCSC bit in SIMR2 is set to 1, the level of the internal SSCLn clock signal changes from low to high, counting to determine the period at high level is stopped while the low level is being input on the SSCLn pin, and counting to determine the period at high level starts after the transition of the input on the SSCLn pin to the high level. The interval from this time until counting to determine the period at high level starts on the transition of the SSCLn pin to the high level is the total of the delay of SSCLn input, delay for noise filtering of the input on the SSCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLK). The period at high level of the internal SSCLn clock is extended even if other devices are not placing the low level on the SSCLn line.

If the IICCSC bit in SIMR2 is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SSCLn pin and the internal SSCLn clock. If the IICCSC bit in SIMR2 is 0, synchronization with the internal SSCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a period of waiting into the interval until the transition of the internal SSCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a period of waiting after the transition of the internal SSCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the period of waiting, generation of the condition itself is not guaranteed. Figure 29.42 shows an example of operations to synchronize the clocks.

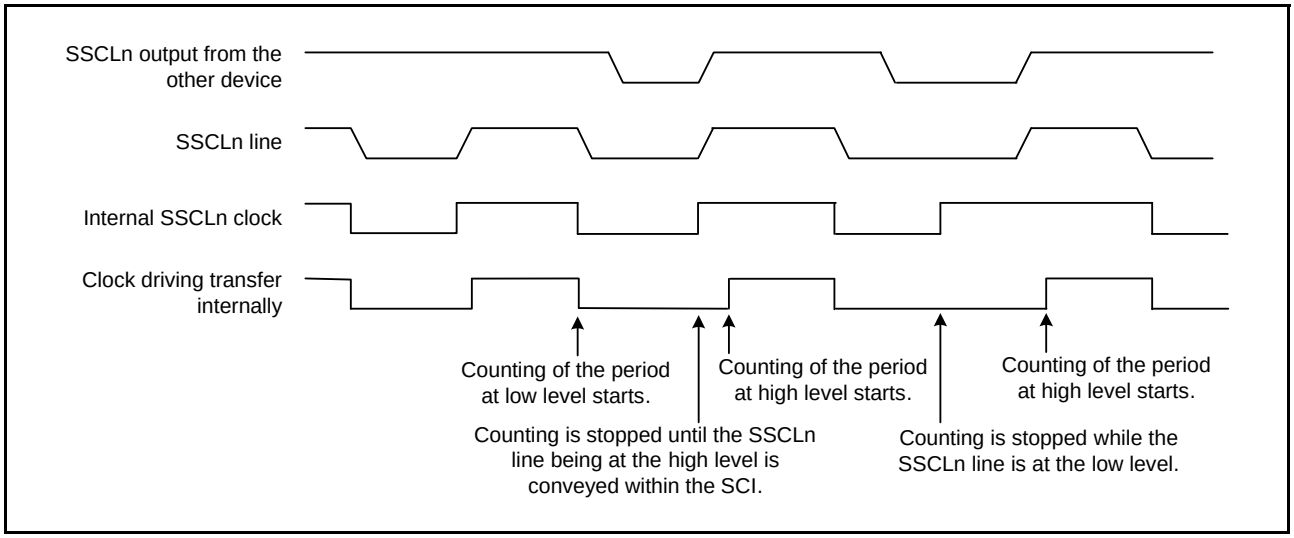


Figure 29.42 Example of Operations for Clock Synchronization

29.7.3 SSDA Output Delay

The IICDL[4:0] bits in SIMR1 can be used to set a delay for output on the SSDA pin relative to falling edges of output on the SSCLn pin. Delay-time settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLK, by the divisor selected by the CKS[1:0] bits in SMR). A delay for output on the SSDAn pin is for the start condition/restart condition/stop condition signal, 8-bit transmit data, and an acknowledge bit.

If the SSDA output delay is shorter than the time for the level on the SSCLn pin to fall, the change of the output on the SSDAn pin will start while the output level on the SSCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SSDA pin are for times greater than the time output on the SSCLn pin takes to fall (300 ns for I^2C in normal mode and fast mode).

Figure 29.43 shows the timing of delays in output on the SSDA pin.

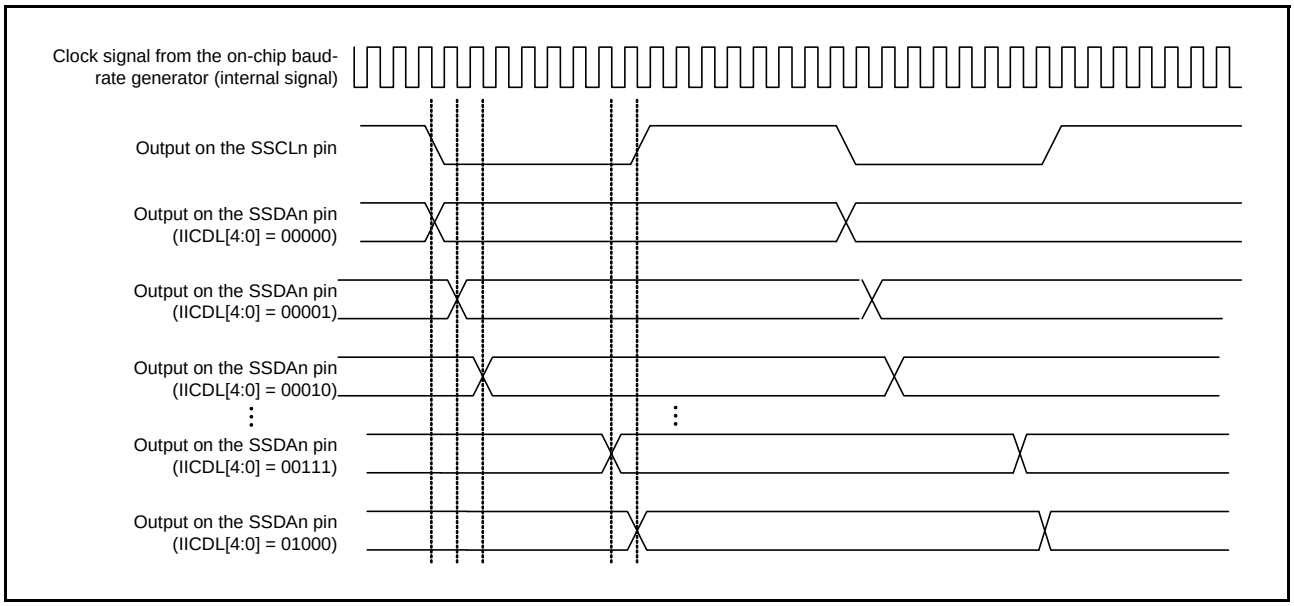


Figure 29.43 Timing of Delays in SSDA Output

29.7.4 SCI Initialization (Simple I2C Mode)

Before transferring data, write the initial value (00h) to SCR and initialize the interface in accordance with the flowchart shown as Figure 29.44.

When changing the operating mode, transfer format, and so on, be sure to set SCR to its initial value before proceeding with the changes.

In simple I2C mode, the open drain setting for the communication ports should be made on the port side.

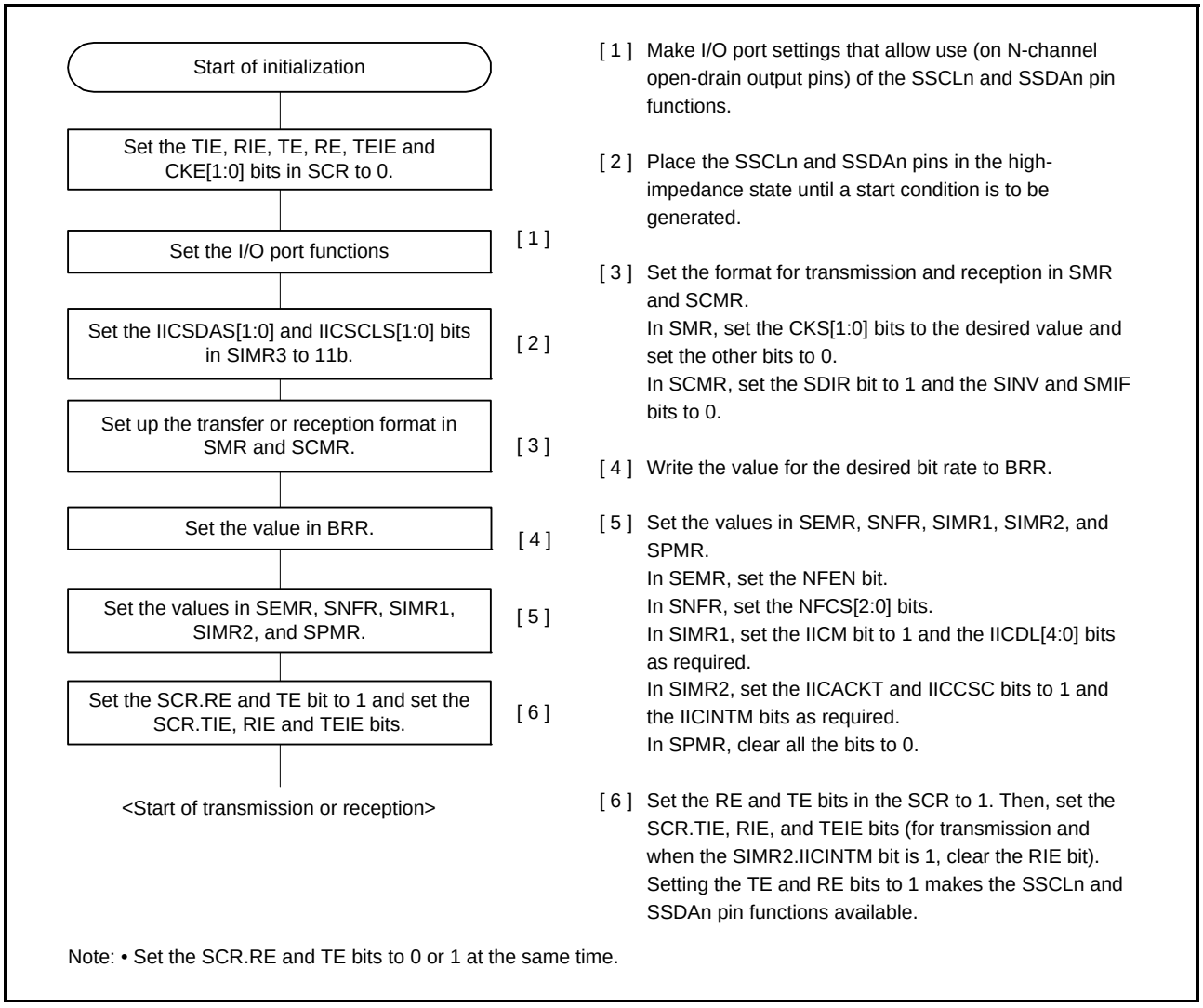


Figure 29.44 Example of the Flow of SCI Initialization (for Simple I2C Mode)

29.7.5 Operation in Master Transmission (Simple I2C Mode)

Figure 29.45 and Figure 29.46 show examples of operations in master transmission and Figure 29.47 is a flowchart showing the procedure for data transmission. The value of the SIMR2.IICINTM bit is assumed to be 1 (transmission and reception interrupts are in use) and the value of the SCR.RIE bit is assumed to be 0 (disabling reception interrupt requests). See Table 29.28 for more information on the STI interrupt.
When 10-bit slave addresses are in use, steps [3] and [4] in Figure 29.47 are repeated twice.
In simple I2C mode, the transmit end interrupt (TXI) is generated when communication of one frame is completed, unlike the TXI interrupt request generation timing during clock-synchronous transmission.

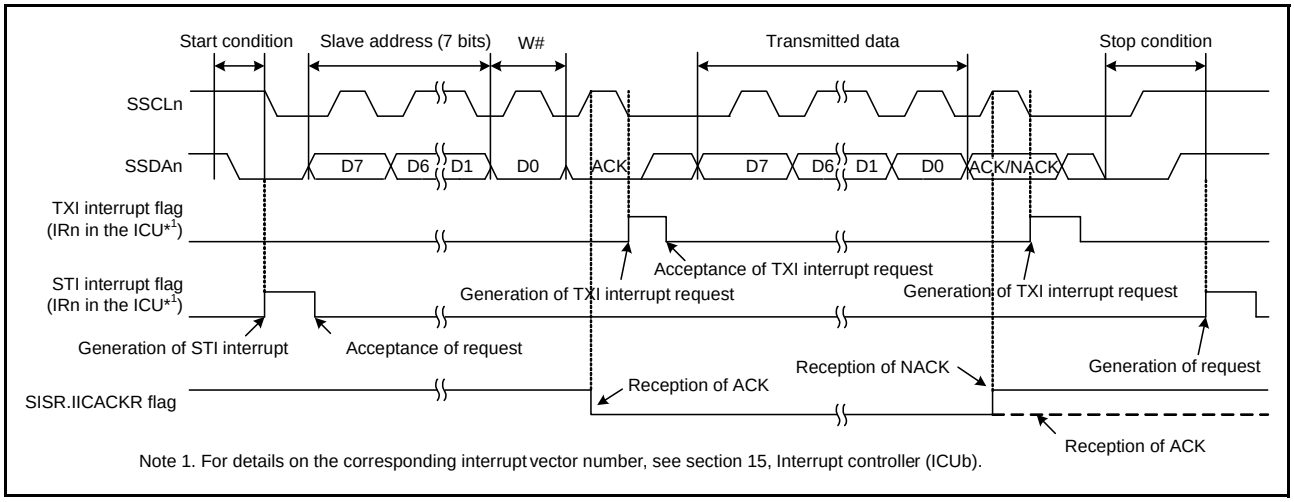


Figure 29.45 Example of Operations for Master Transmission in I2C Bus Mode (with Seven-Bit Slave Addresses, Transmission Interrupts, and Reception Interrupts in Use)

When the SIMR2.IICINTM bit is set to 0 (ACK and NACK interrupts are used) during master transmission, the DTC or DMAC is activated by the ACK interrupt as the trigger and necessary number of data bytes are transmitted. When the NACK is received, error processing, such as transmission stop and re-transmission, is performed by the NACK interrupt as the trigger.

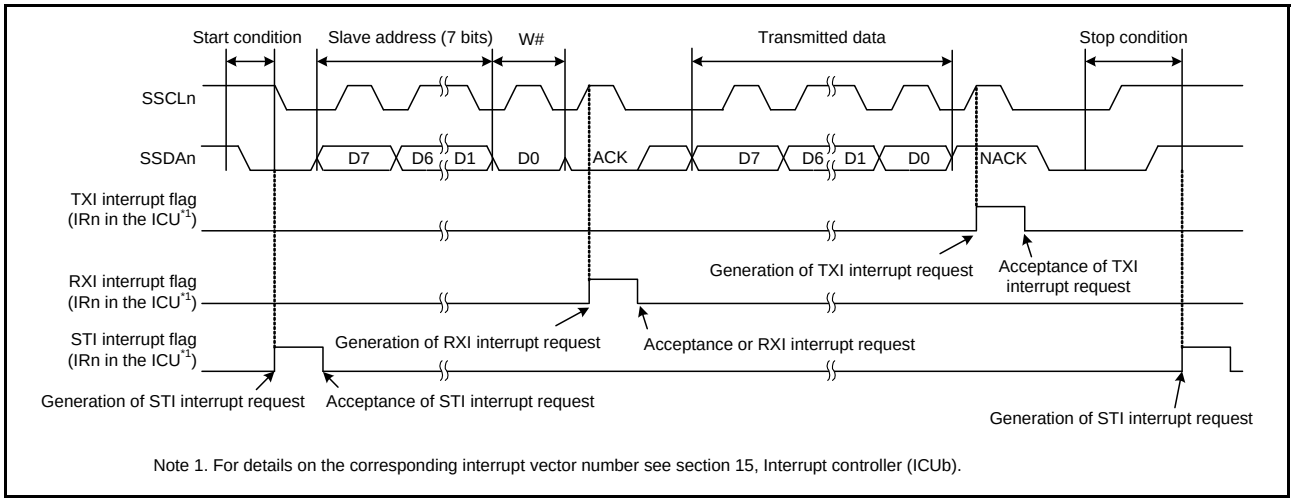


Figure 29.46 Example 2 of Operations for Master Transmission in Simple I2C Bus Mode (with Seven-Bit Slave Addresses, ACK Interrupts, and NACK Interrupts in Use)

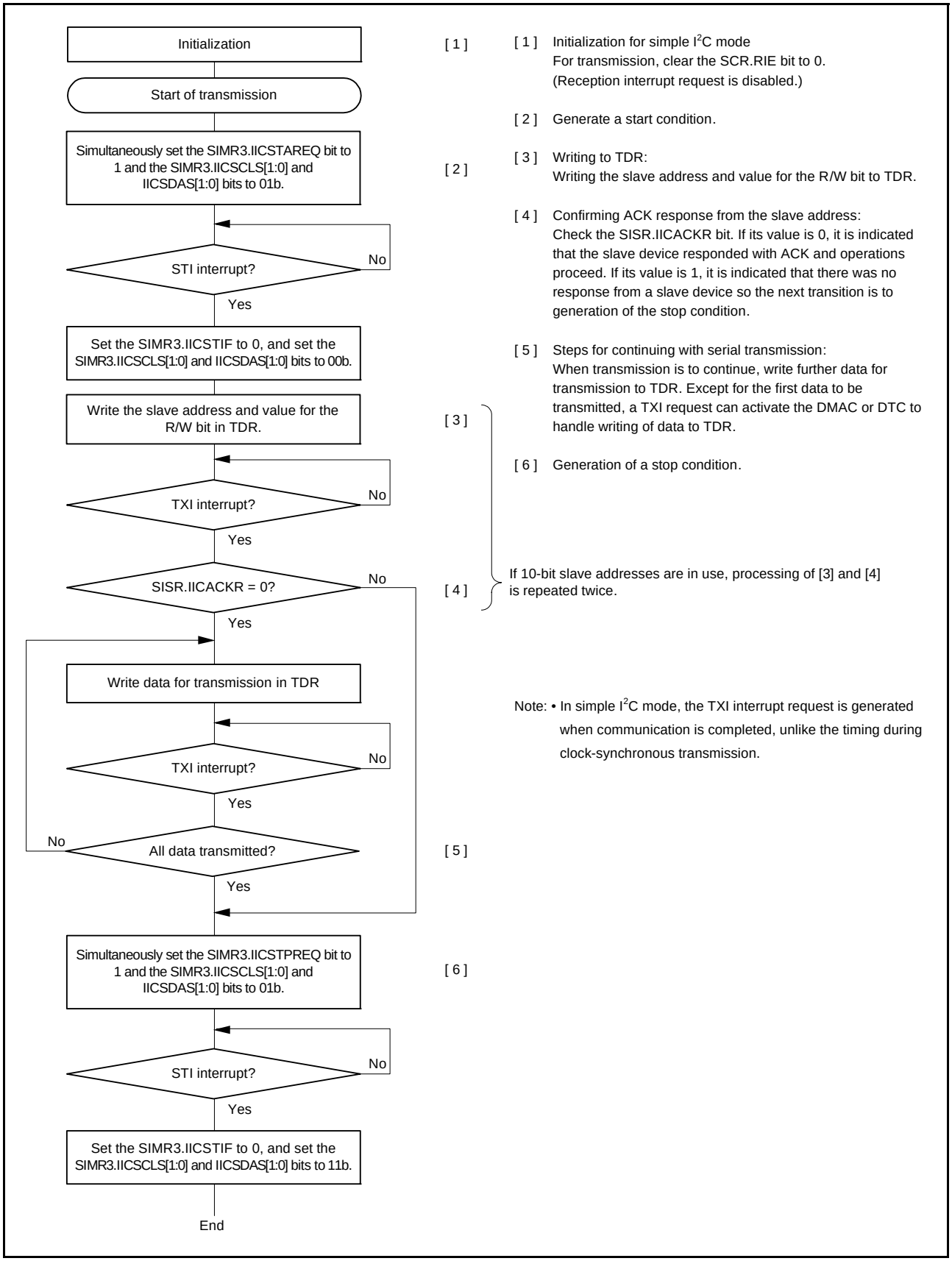
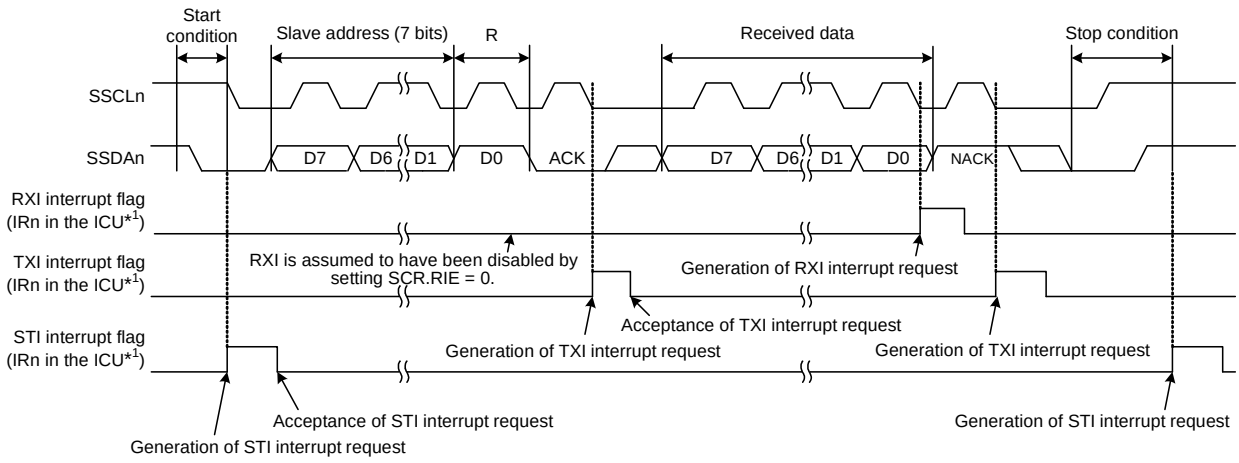


Figure 29.47 Example of the Procedure for Master Transmission Operations in Simple I2C Mode (with Transmission Interrupts and Reception Interrupts in Use)

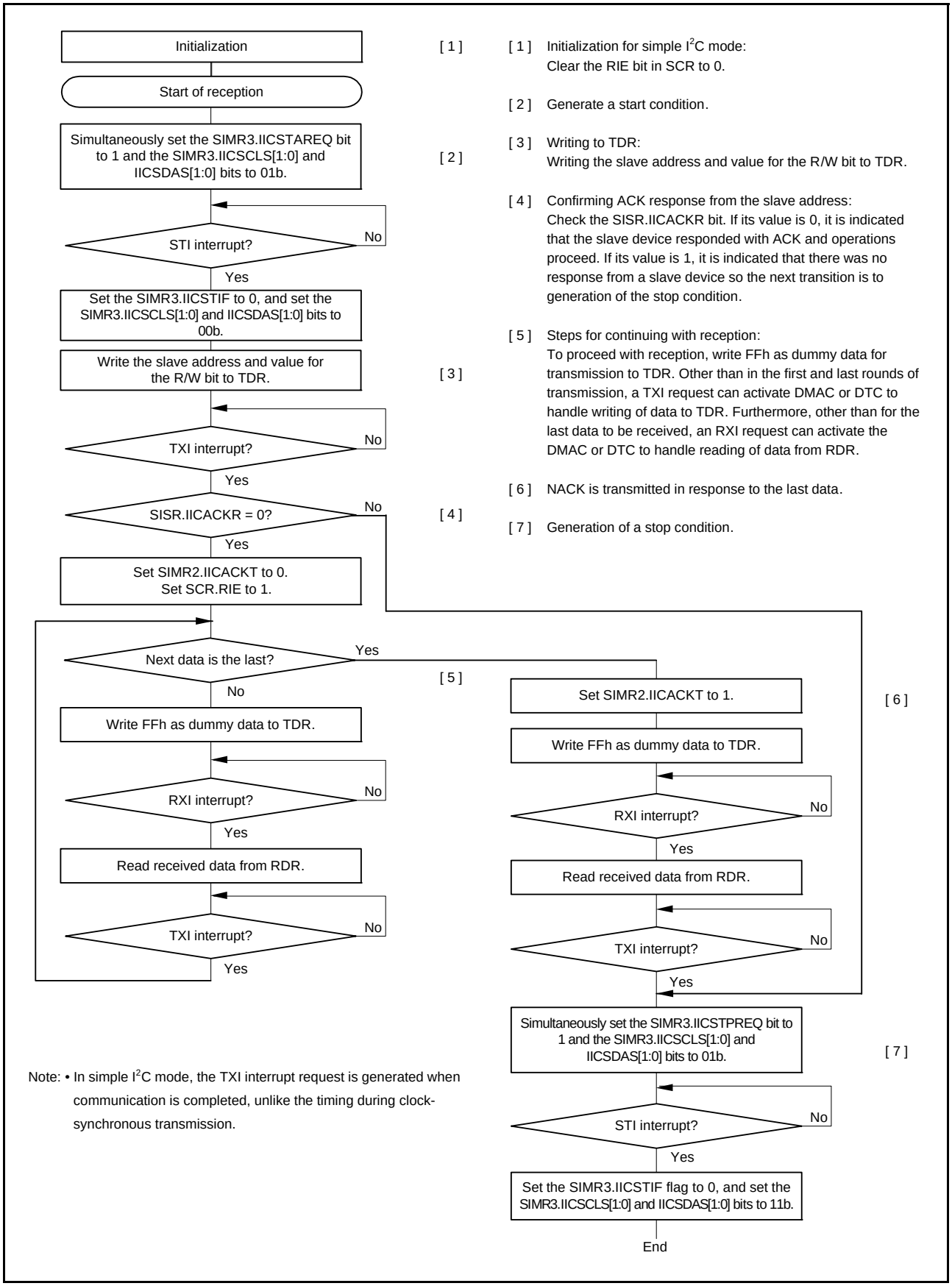
29.7.6 Master Reception (Simple I²C Mode)

Figure 29.48 shows an example of operations in simple I²C mode master reception and Figure 29.49 is a flowchart showing the procedure for master reception.
The value of the SIMR2.IICINTM bit is assumed to be 1 (transmission and reception interrupts are in use).
In simple I²C mode, the transmit end interrupt (TXI) is generated when communication of one frame is completed, unlike the TXI interrupt request generation timing during clock-synchronous transmission.



Note 1. For details on the corresponding interrupt vector number, see Section 15, Interrupt Controller (ICUb).

Figure 29.48 Example of Operations for Master Reception in I²C Bus Mode (with Seven-Bit Slave Addresses, Transmission Interrupts, and Reception Interrupts in Use)



[1] Initialization for simple I²C mode:
Clear the RIE bit in SCR to 0.

[2] Generate a start condition.

[3] Writing to TDR:
Writing the slave address and value for the R/W bit to TDR.

[4] Confirming ACK response from the slave address:
Check the SISR.IICACKR bit. If its value is 0, it is indicated that the slave device responded with ACK and operations proceed. If its value is 1, it is indicated that there was no response from a slave device so the next transition is to generation of the stop condition.

[5] Steps for continuing with reception:
To proceed with reception, write FFh as dummy data for transmission to TDR. Other than in the first and last rounds of transmission, a TXI request can activate DMAC or DTC to handle writing of data to TDR. Furthermore, other than for the last data to be received, an RXI request can activate the DMAC or DTC to handle reading of data from RDR.

[6] NACK is transmitted in response to the last data.

[7] Generation of a stop condition.

Note: • In simple I²C mode, the TXI interrupt request is generated when communication is completed, unlike the timing during clock-synchronous transmission.

Figure 29.49 Example of the Procedure for Master Reception Operations in Simple I²C Mode (with Transmission Interrupts and Reception Interrupts in Use)

29.8 Operation in Simple SPI Mode

As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.

Making the settings for clock-synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) plus setting the SSE bit in the SPMR to 1 places the SCI in simple SPI mode. However, the SS pin function on the master side is unnecessary for connection of the device used as the master in simple SPI mode when the configuration only has a single master, so set the SSE bit in the SPMR to 0 in such cases.

Figure 29.50 shows an example of connections for simple SPI mode. Control a general port pin to produce the SS output signal from the master.

In simple SPI mode, data are transferred in synchronization with clock pulses in the same way as in clock-synchronous mode. One character of data for transfer consists of eight bits of data, and parity bits cannot be appended to this. The data can be inverted by setting the SCMR.SINV bit to 1.

Since the reception and transmission sections are independent of each other within the SCI module, full-duplex communications are possible, with a common clock signal. Furthermore, since both sections have a buffered structure, writing of further data for transmission while transmission is in progress and reading of previously received data while reception is in progress are both possible. Continuous transfer is thus possible.

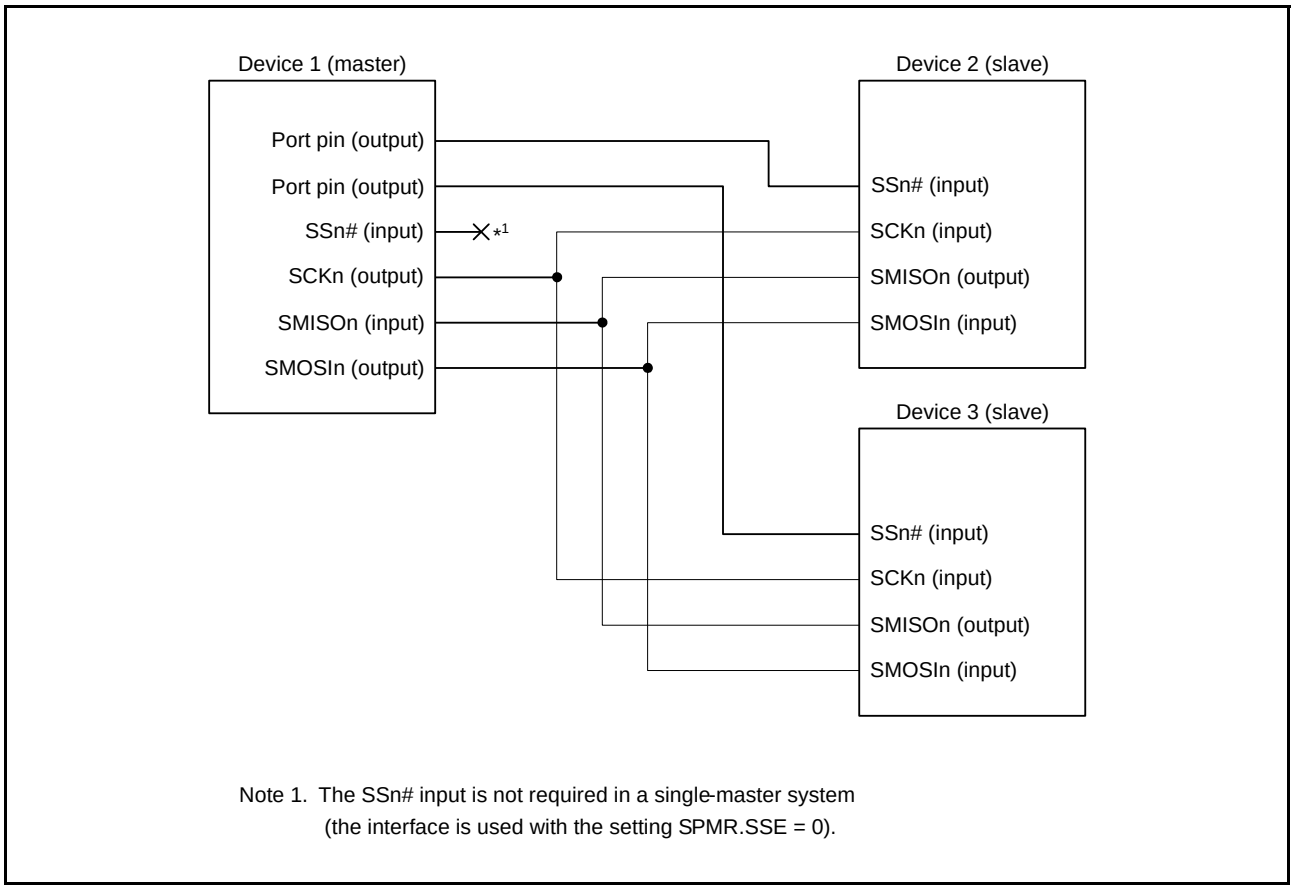


Figure 29.50 Example of Connections via a Simple SPI Mode (In Single Master Mode, SPMR.SSE Bit = 0)

29.8.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00 or 01 and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10 or 11 and SPMR.MSS = 1). Table 29.24 lists the states of pins according to the mode and the level on the SSn# pin.

Table 29.24 States of Pins by Mode and Input Level on the SSn# Pin

Mode	Input on SSn# pin	State of SMOSIn pin	State of SMISOn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High impedance	Input for received data (but disabled)	High impedance
Slave mode	High level (transfer can proceed)	Input for received data (but disabled)	High impedance	Clock input (but disabled)
	Low level (transfer cannot proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn# pin (this is equivalent to input of a high level on the SSn# pin). Since the SSn# pin function is not required, the pin is available for other purposes.
Note 2. The SMOSIn pin output is in the high-impedance state when transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when transmission is disabled (SCR.TE and RE bits = 00) in a multi-master configuration (SPMR.SSE = 1).

29.8.2 SS Function in Master Mode

Setting the CKE[1:0] bits in the SCR to 00 and the MSS bit in the SPMR to 0 selects master operation. The SSn# pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn# pin.

When the level on the SSn# pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission. When the level on the SSn# pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and this indicates that transmission or reception is in progress. At this time the SMOSIn output and SCKn pins will be placed in the high-impedance state and starting transmission or reception will not be possible. Furthermore, the value of the SPMR.MFF bit will be 1, indicating a mode-fault error. In a multi-master configuration, start error processing by reading SPMR.MFF flag. Also, even if a mode-fault error occurs while transmission or reception is in progress, transmission or reception will not be stopped, but the SMOSIn and SCKn output pins will be placed in the high-impedance state after the completion of the transfer.

Control a general port pin to produce the SS output signal from the master.

29.8.3 SS Function in Slave Mode

Setting the CKE[1:0] bits in the SCR to 10 and the MSS bit in the SPMR to 1 selects slave operation. When the level on the SSn# pin is high, the RxDn output pin will be in the high-impedance state and clock input through the SCKn pin will be ignored. When the level on the SSn# pin is low, clock input through the SCKn pin will be effective and transmission or reception can proceed. If the input on the SSn# pin changes from low to high level during transmission or reception, the SMISOn output pin will be placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception will continue at the rate of the clock input through the SCKn pin until processing for the character currently being transmitted or received is completed, after which it stops. At that time, an interrupt (the appropriate one from among TXI, RXI, and TEI) will be generated.

29.8.4 Relationship between Clock and Transmit/Receive Data

The SPMR.CKPOL and CKPH bits can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 29.51. The relation is the same for both master and slave operation. This is the same as when the level on the SSn# pin is high. The SSn# pin can be used for another purpose. For details, see section 29.8.2, SS Function in Master Mode.

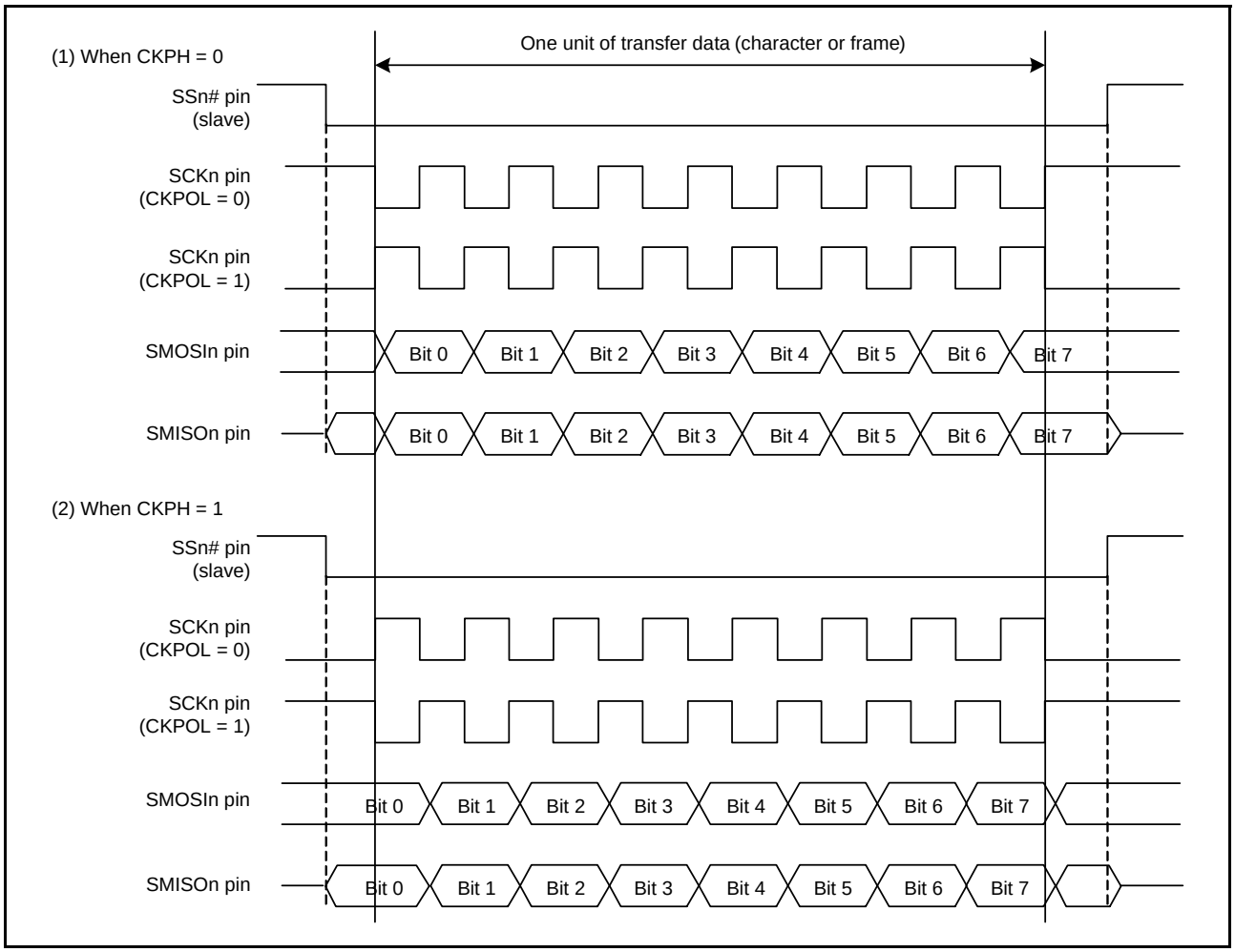


Figure 29.51 Relation between Clock Signal and Transmit/Receive Data in Simple SPI Mode

29.8.5 SCI Initialization (Simple SPI Mode)

The procedure is the same as for initialization in clock-synchronous mode (Figure 29.20, Sample SCI Initialization Flowchart). The CKPOL and CKPH bits in the SPMR must be set to endure that the kind of clock signal they select is suitable for both master and slave devices.

For initialization, changes to the operating mode, changes to the transfer format, and so on, initialize the SCR register before proceeding with changes.

Note that the ORER, FER, and PER flags, as well as the RDR, are not initialized even when the RE bit is set to 0.

Note that changing the value of the TE bit from 1 to 0 or from 0 to 1 will lead to the generation of a transmission interrupt (TXI) if the value of the TIE bit in the SCR is 1 at the time.

29.8.6 Transmission and Reception of Serial Data (Simple SPI Mode)

In master operation, ensure that the SSn# pin of the slave device on the other side of the transfer is at the low level before starting the transfer and at the high level on completion of the transfer. Otherwise, the procedures are the same as in clock-synchronous mode.

29.9 Extended Serial Mode Control Section: Description of Operation

29.9.1 Serial Transfer Protocol

In conjunction with an SCIc module, the extended serial mode control section of an SCId module can realize the serial transfer protocol composed of Start Frames and Information Frames that is shown in Figure 29.52.
A Start Frame is composed of a Break Field, Control Field 0, and Control Field 1. An Information Frame is composed of a number of Data Fields, a CRC16 Upper Field, and a CRC16 Lower Field.

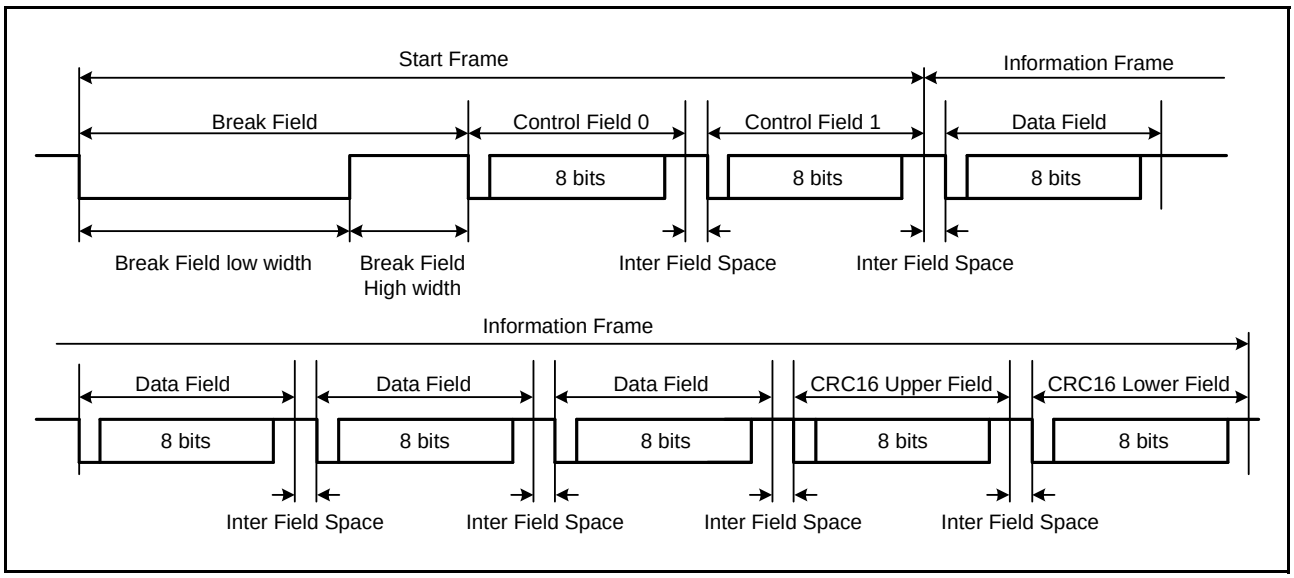


Figure 29.52 Protocol for Serial Transfer by the Extended Serial Mode Control Section

29.9.2 Transmitting a Start Frame

Figure 29.53 shows an example of operations to transmit a Start Frame, which is composed of the Break Field low width, Control Field 0, and Control Field 1. Figure 29.54 and Figure 29.55 are flowcharts for the transmission of a Start Frame.
Operations when the extended serial mode control section is to be used to transmit a Start Frame are as listed below. Be sure to use the SCI12 in asynchronous mode.

(1) With Break Field low width output mode as the operating mode for the timer, writing 1 to the TCST bit in TCR starts counting by the timer, and the low level will be output from the TXDX12 pin over the period corresponding to the TCNT and TPRE settings.
(2) The output on the TXDX12 pin is inverted when the timer counter underflows, and the BFDF bit in STR is set to 1. An SCIX0 interrupt is also generated if the value of the BFDIE bit in ICR is 1.
(3) Writing 0 to the TCST bit in TCR stops counting by the timer, and SCI2 is used to send the data for Control Field 0. After the Break Field low width output, stop counting before the next underflow occurs.
(4) Once the data for Control Field 0 have been transmitted, SCI12 is used to send the data for Control Field 1.
(5) Once the data for Control Field 1 have been transmitted, SCI12 is used to send an Information Frame.

Omit the Break Field and Control Field 0 to suit the structure of the Start Frame.

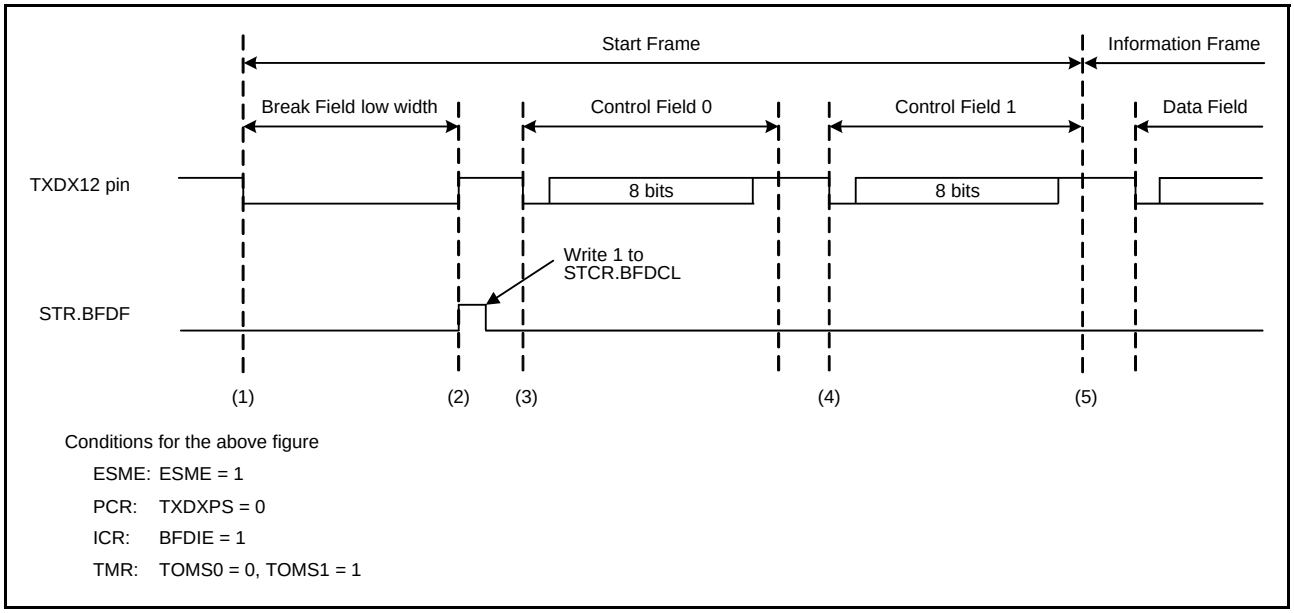


Figure 29.53 Example of Operations at the Time of Start-Frame Transmission

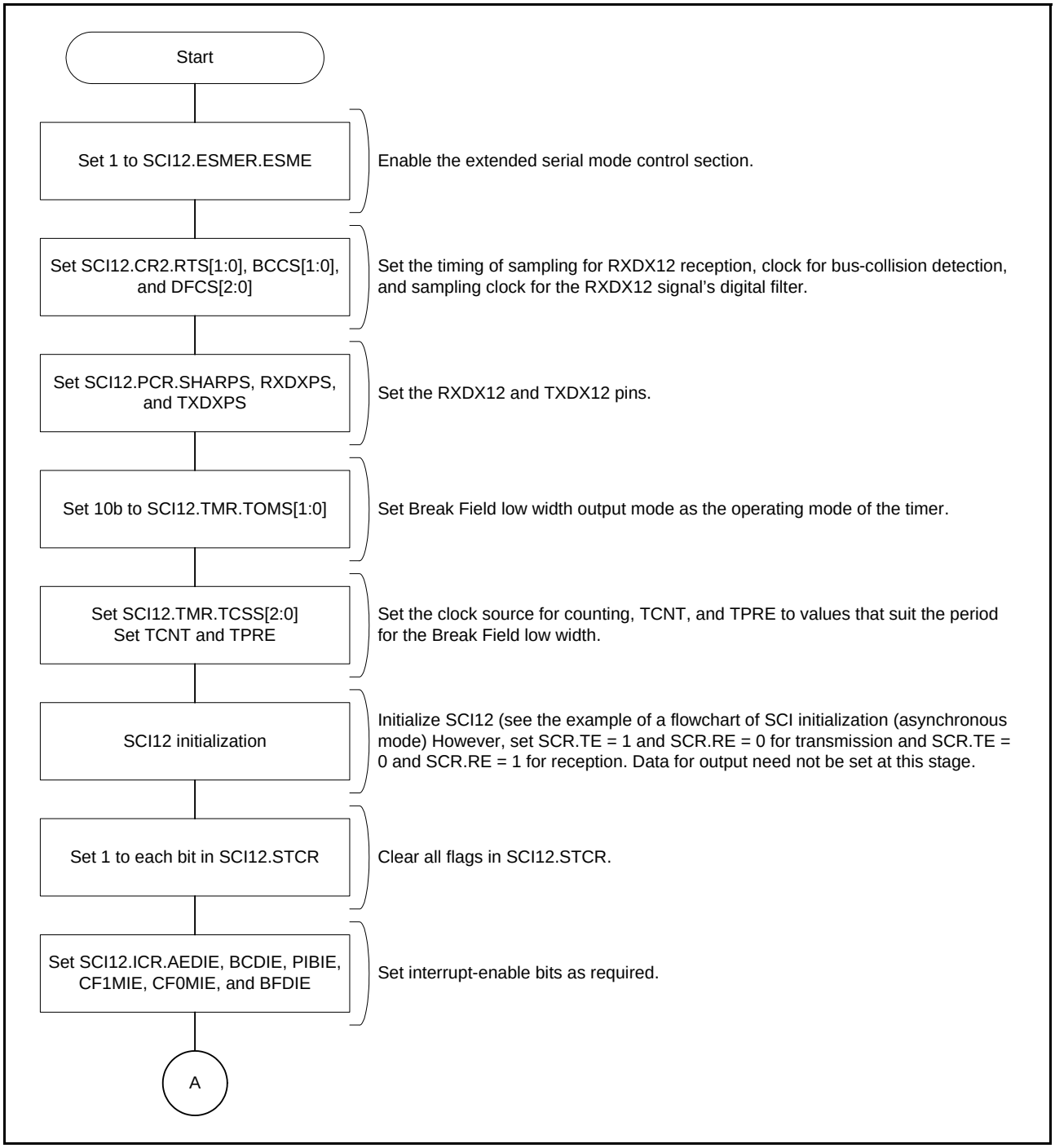


Figure 29.54 Sample Flowchart for Transmission of a Start Frame (1)

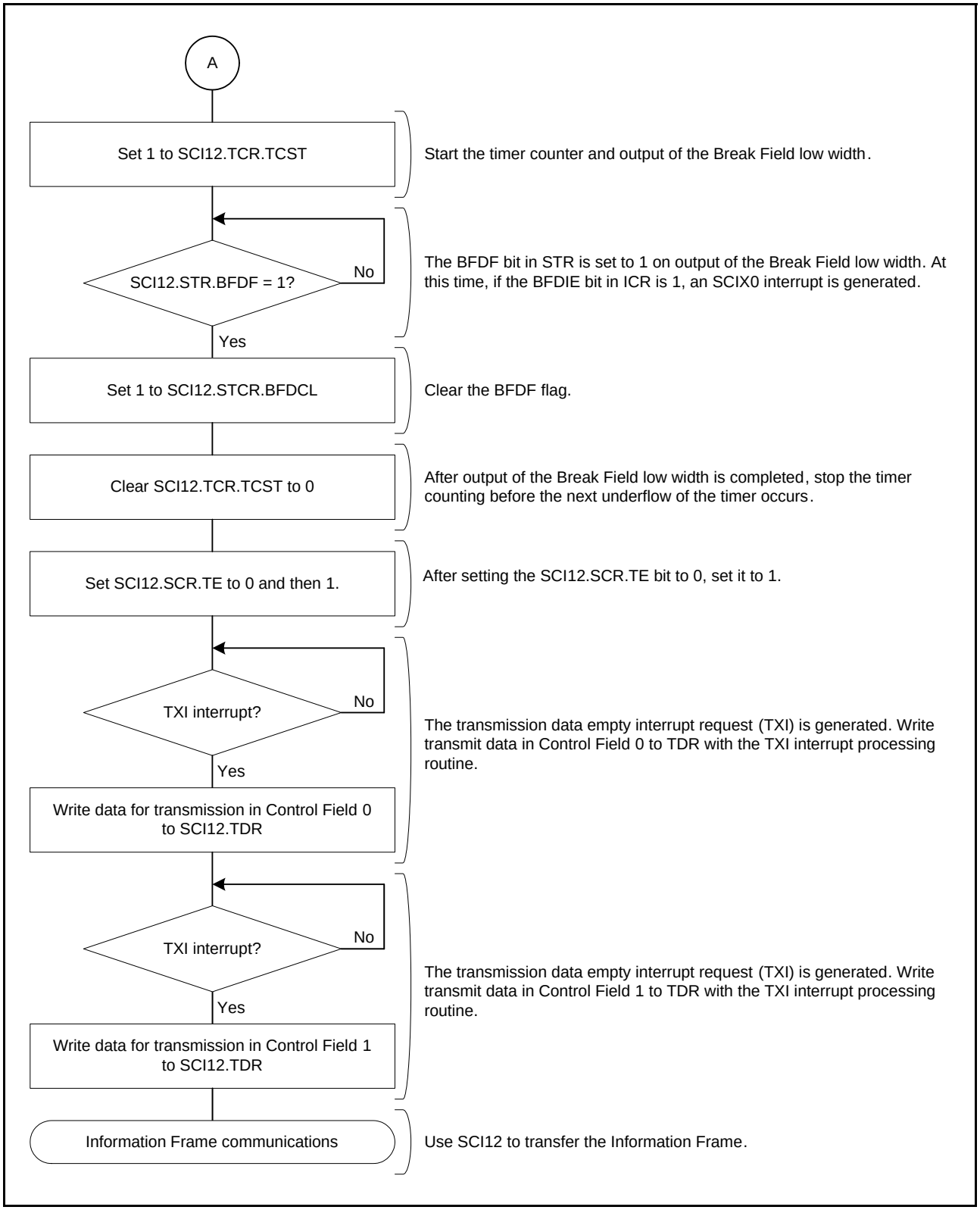


Figure 29.55 Sample Flowchart for Transmission of a Start Frame (2)

29.9.3 Receiving a Start Frame

The extended serial mode control section is capable of receiving Start Frames with the structures listed in Table 29.25.

Table 29.25 Structures of Start Frames

Bit Setting		Structures of Start Frames
BFE	CF0RE	
0	0	Control Field 1 (8 bits) → Information Frame
0	1	Control Field 0 (8 bits) → Control Field 1 (8 bits) → Information Frame
1	0	Break Field (Low width) → Control Field 1 (8 bits) → Information Frame
1	1	Break Field (Low width) → Control Field 0 (8 bits) → Control Field 1 (8 bits) → Information Frame

Figure 29.56 shows an example of operations to receive a Start Frame, which is composed of the Break Field low width, Control Field 0, and Control Field 1. Figure 29.57 and Figure 29.58 are flowcharts for the reception of a Start Frame, and Figure 29.58 is a state transition diagram for the extended serial mode control section.
Operations when the extended serial mode control section is to be used to receive a Start Frame are as listed below. Be sure to use the SCI12 in asynchronous mode.

(1) With Break Field low width detection mode as the operating mode for the timer, writing 1 to the SDST bit in CR3 enables detection of the Break Field low width. RXDX12 input to the SCIc module is disabled at this time.RXDX12 input to the SCI12 module is disabled at this time.
(2) Low-level input on the RXDX12 pin continuing over a period longer than that corresponding to the settings of TCNT and TPRE is detected as the Break Field low width. At this time, the BFDF bit in STR is set to 1. An SCIX0 interrupt is also generated if the value of the BFDIE bit in ICR is 1.
(3) When the input from the RXDX12 pin goes high after the Break Field low width, the RXDSF bit in CR0 becomes zero and reception of Control Field 0 by the SCI12 module starts.
(4) If the data received in Control Field 0 match the data set in CF0DR, the CF0MF bit in STR is set to 1. An SCIX1 interrupt is also generated if the value of the CF0MIE bit in ICR is 1. Reception of Control Field 1 by the SCI12 module starts after that. If the data received in Control Field 0 do not match the data set in CF0DR, a transition to the state prior to Break Field low width detection proceeds.
(5) If the data received in Control Field 1 match the data set in PCF1DR and SCF1DR, the CF1MF bit in STR is set to 1. An SCIX1 interrupt is also generated if the value of the CF1MIE bit in ICR is 1. Transfer of the Information Frame by the SCI12 module starts after that. If the data received in Control Field 1 do not match the data set in either or both of PCF1DR and SCF1DR, a transition to the state prior to Break Field low width detection proceeds.

Omit the Break Field and Control Field 0 to suit the structure of the Start Frame.

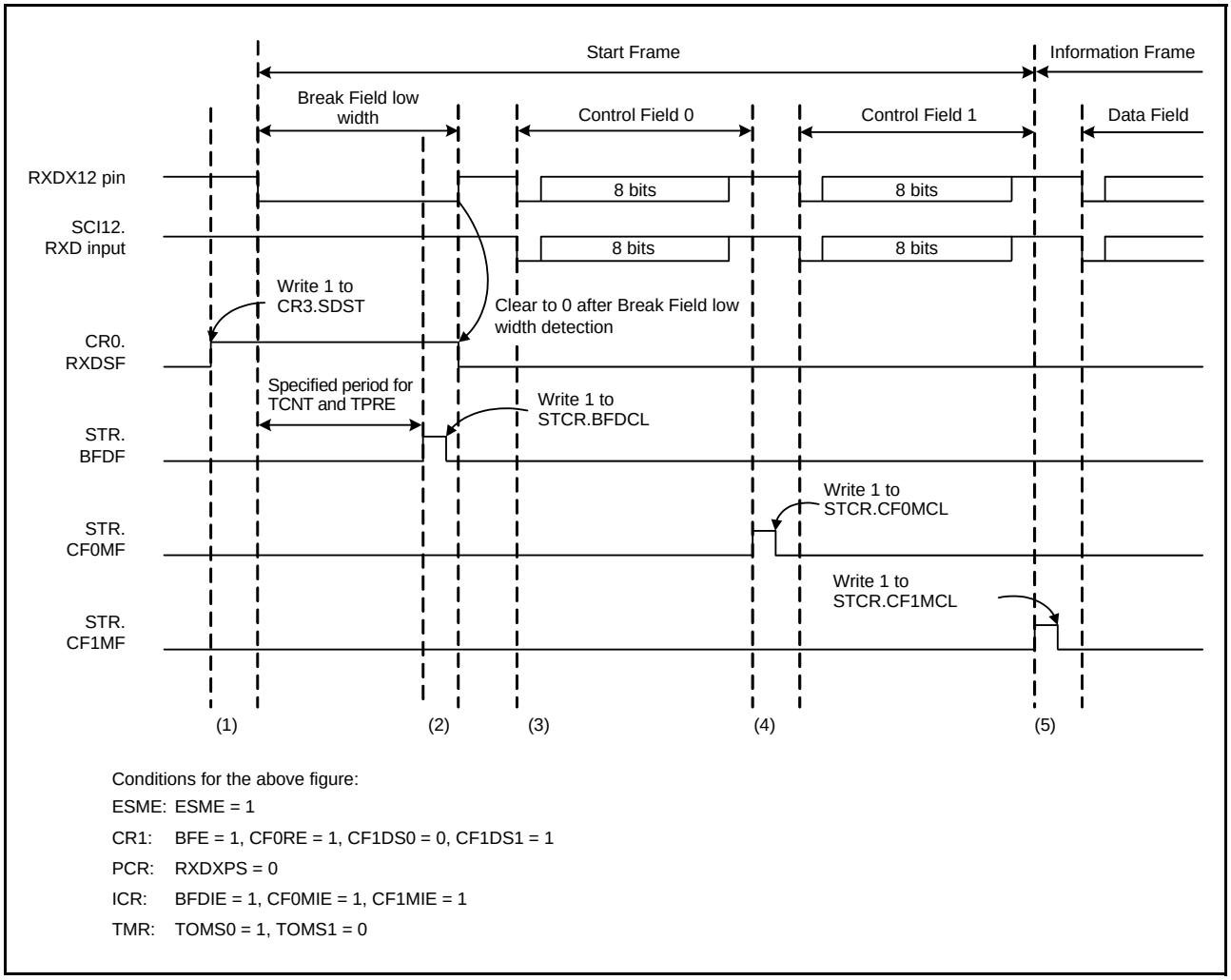


Figure 29.56 Example of Operations at the Time of Start-Frame Reception

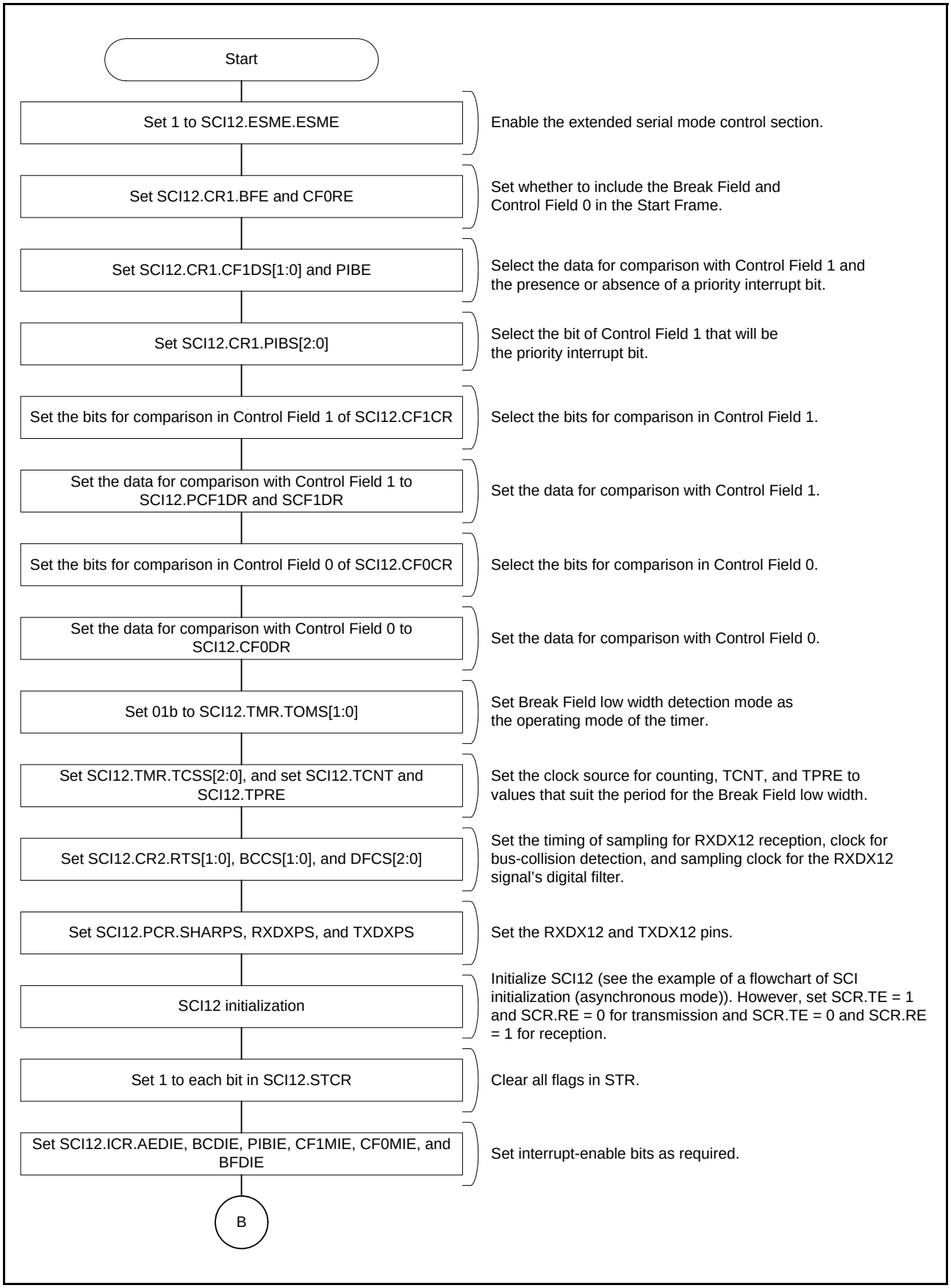


Figure 29.57 Sample Flowchart for Reception of a Start Frame (1)

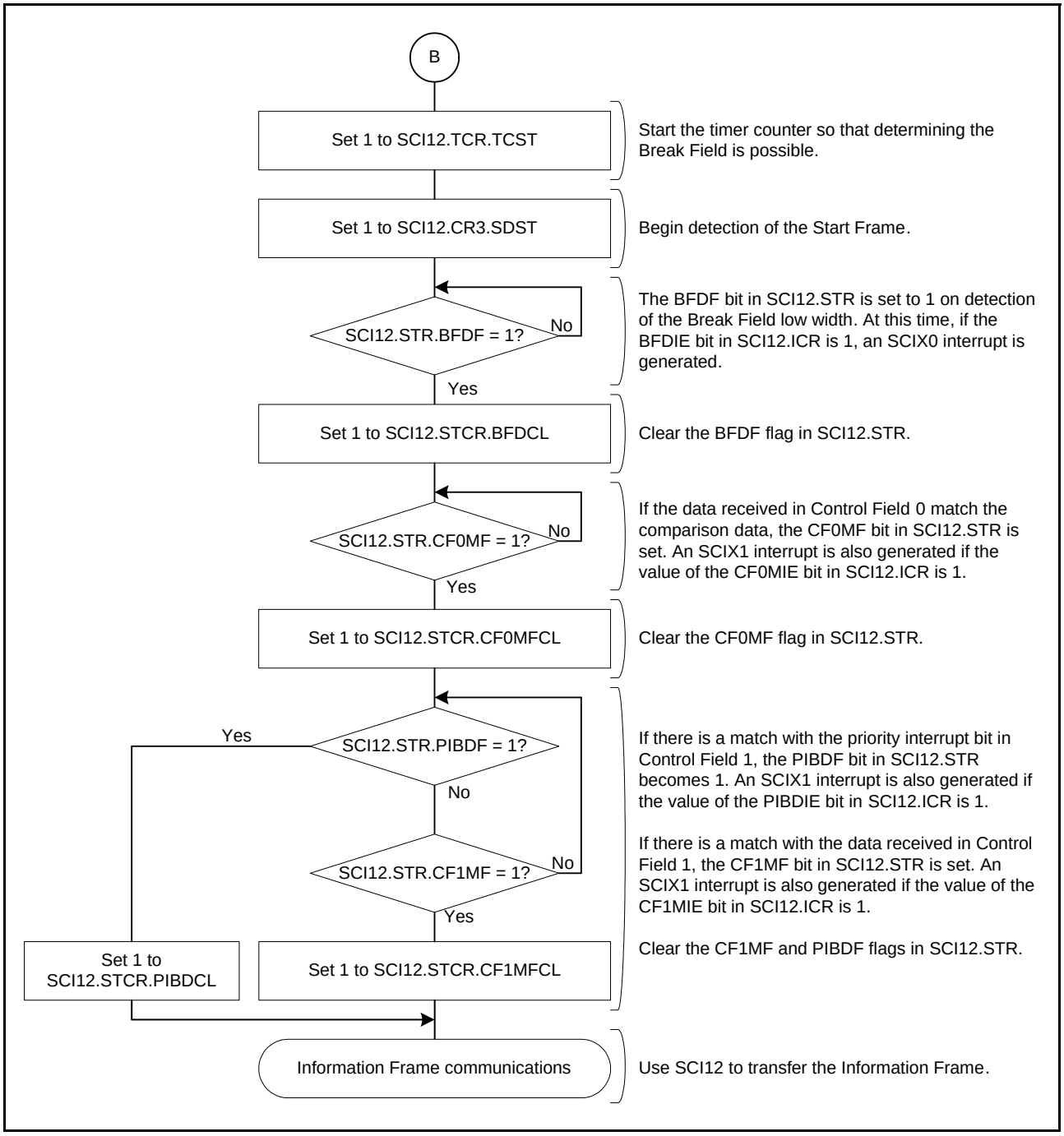


Figure 29.58 Sample Flowchart for Reception of a Start Frame (2)

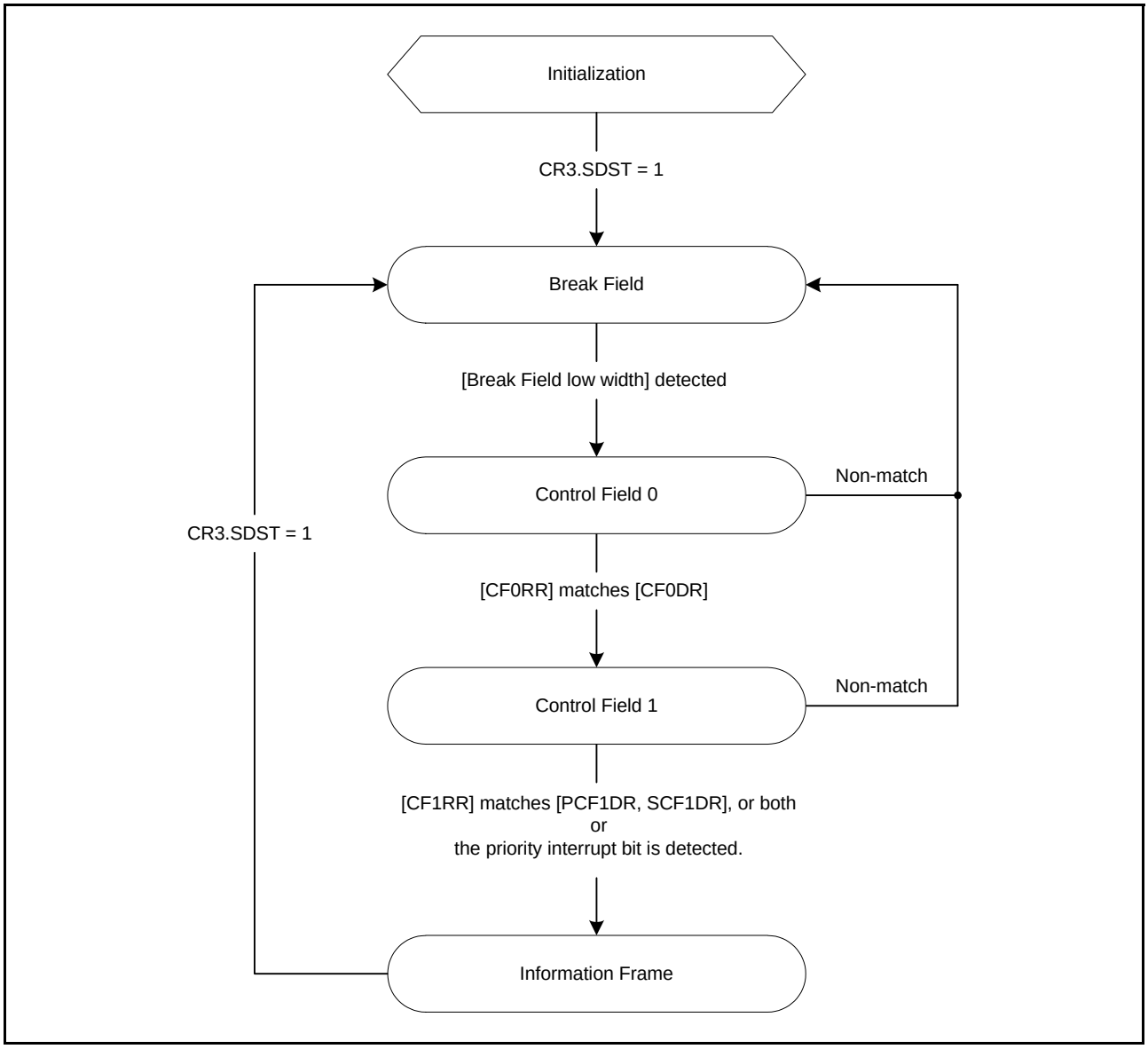


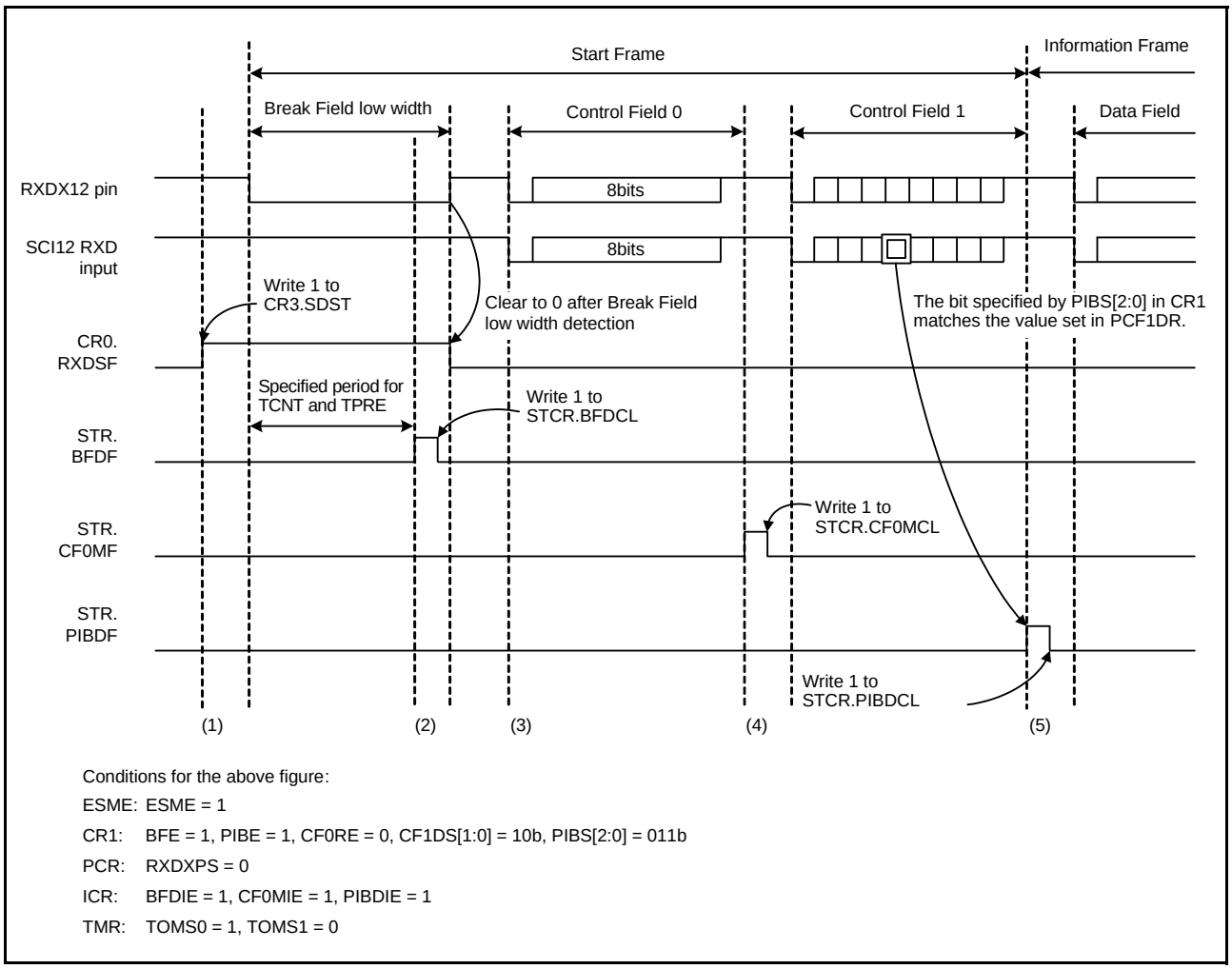
Figure 29.59 Diagram of State Transitions at the Time of Start-Frame Reception

29.9.3.1 Priority Interrupt Bit

Figure 29.60 shows an example of operation in Start-Frame reception where a priority interrupt bit is in use. Setting the PIBE bit in CR1 to 1 enables the use of a priority interrupt bit.
Operations of the extended serial mode control section in start-Frame reception where a priority interrupt bit is in use are as described below.

Steps (1) to (4) are the same as in Figure 29.56, for Start-Frame reception.

(5) If the value of the bit selected by the PIBS[2:0] bits in CR1 matches the corresponding bit in PCF1DR, the PIBDF bit in STR is set to 1. An SCIX1 interrupt is also generated if the value of the PIBDIE bit in ICR is 1. Transfer of the Information Frame by the SCI12 module starts after that. If the data received in Control Field 1 do not match the data set in either or both of PCF1DR and SCF1DR and the priority interrupt bit is not detected, a transition to the state prior to Break Field low width detection proceeds.



Conditions for the above figure:

ESME: ESME = 1

CR1: BFE = 1, PIBE = 1, CF0RE = 0, CF1DS[1:0] = 10b, PIBS[2:0] = 011b

PCR: RXDXPS = 0

ICR: BFDIE = 1, CF0MIE = 1, PIBDIE = 1

TMR: TOMS0 = 1, TOMS1 = 0

Figure 29.60 Example of Operations at the Time of Start-Frame Reception (with Priority Interrupts in Use)

29.9.4 Detection of Bus Collisions

Detection of bus collisions operate for cases where output of the Break Field low width and transmission of data by the SCI12 module are in progress when the ESMER.ESME and the SCI12.SCR.TE are set to 1.

Figure 29.61 shows an example of operations with bus collision detection. Signals output through TXDX12 and input through RXDX12 are sampled with the bus-collision detection clock set with CR2.BCCS[1:0] as the sampling clock, and the BCDF bit in STR is set to 1 if the signals fail to match three times in a row. An SCIX2 interrupt is also generated if the value of the BCDIE bit in ICR is 1.

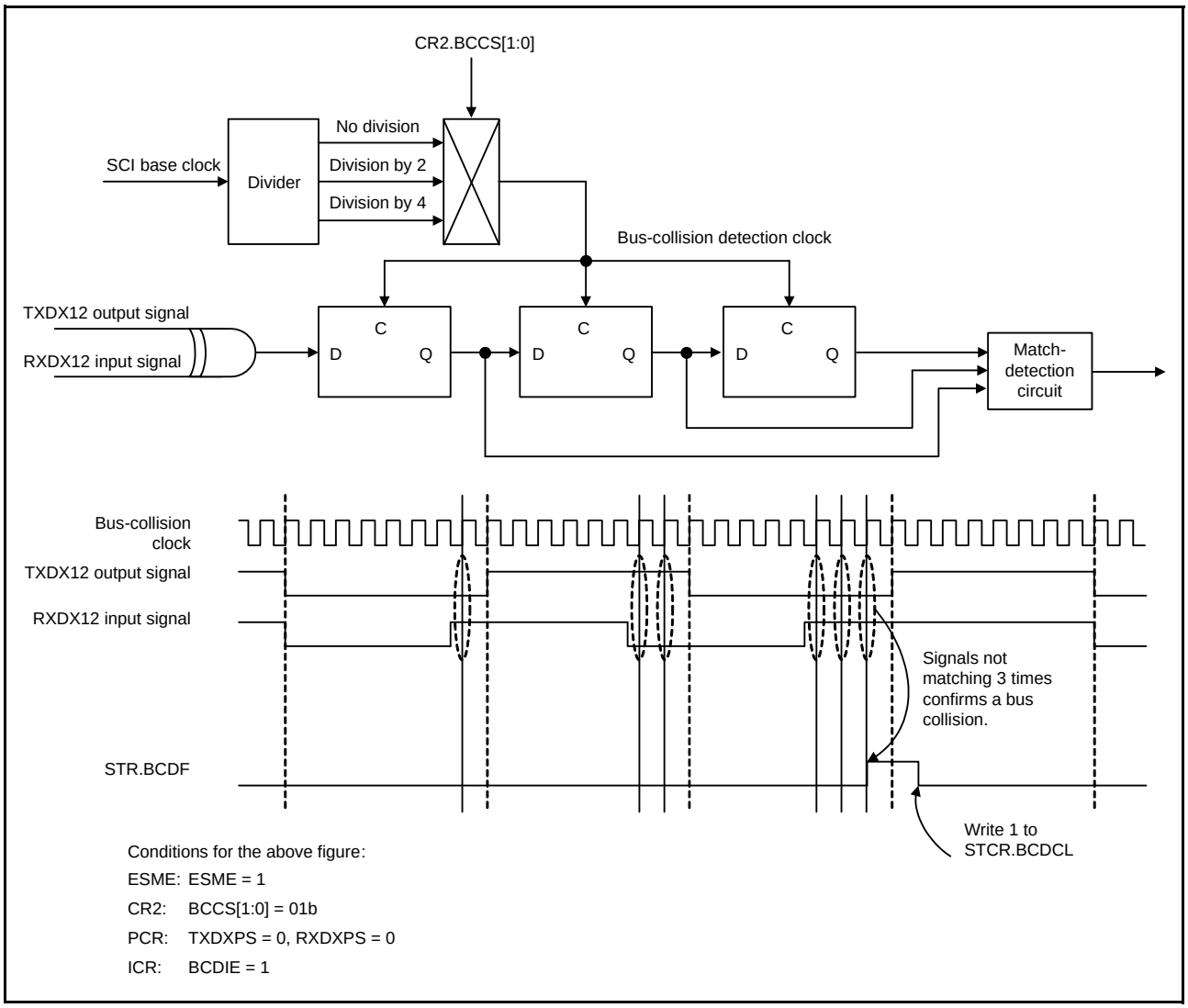


Figure 29.61 Example of Operations with Bus-Collision Detection

29.9.5 Digital Filter for Input on the RXDX12 Pin

Signals input through the RXDX12 pin can be passed through a digital filter before they are conveyed to the internal circuits. The digital filter consists of three flip-flop circuit stages connected in series and a match-detecting circuit. The DFCS[2:0] bits in CR2 select the sampling clock for the RXDX12 pin input signals. If the outputs of all three latches match, the given level is conveyed to subsequent circuits. If the levels do not match, the previous value is retained. In other words, levels are confirmed as being the signal if they are retained for at least three cycles of the sampling clock but judged to be noise rather than changes in the signal level if they change within three cycles of the sampling clock. Figure 29.62 shows an example of operations with the digital filter.

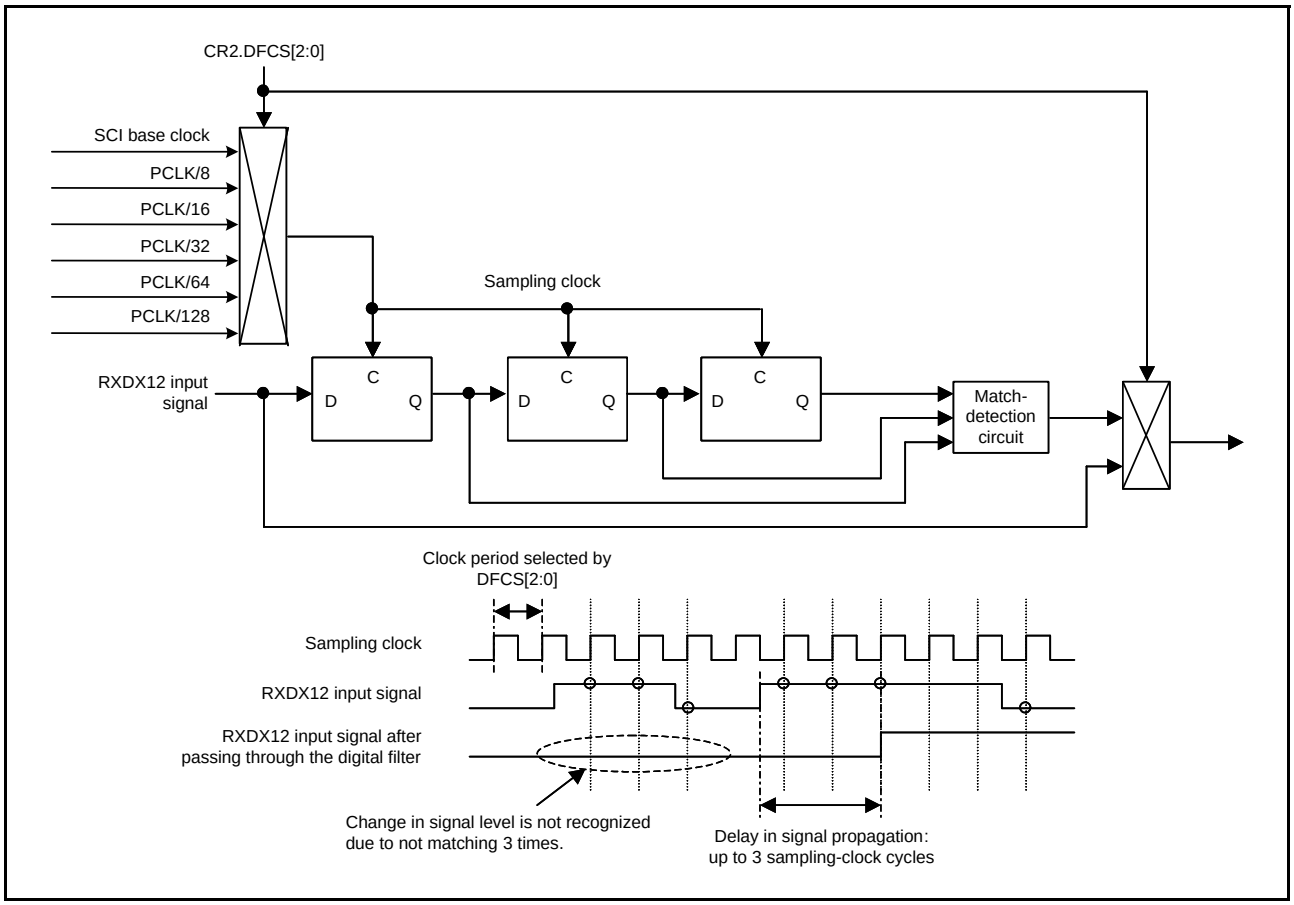
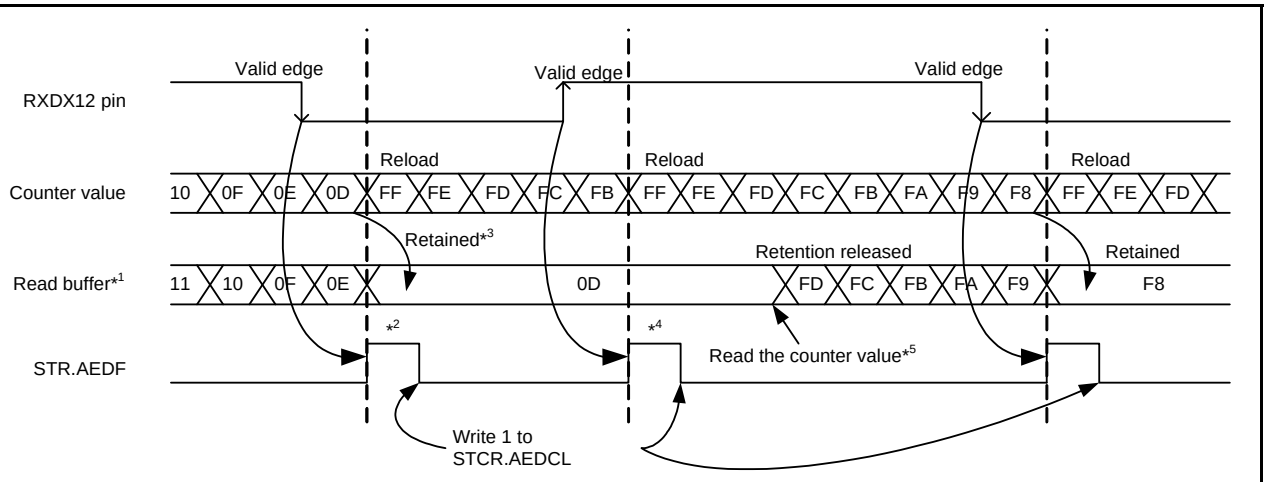


Figure 29.62 Example of Operations with the Digital Filter

29.9.6 Bit-Rate Measurement

The bit-rate measurement function measures the intervals between rising and falling edges and between falling and rising edges of the signal input from the RXDX12 pin. Figure 29.63 shows an example of operations for bit-rate measurement.

(1) Writing 1 to the BRME bit in CR0 enables bit-rate measurement. Only set BRME to 1 when you wish to proceed with bit-rate measurement. Furthermore, bit-rate measurement will not proceed during a Break Field, even if BRME is set to 1.
(2) After detection of the Break Field low width, bit-rate measurement starts when the level input on the RXDX12 pin becomes high.
(3) Once bit-rate measurement has started, counter values from the timer are retained in the read buffers on the input of valid edges from the RXDX12 pin (rising and falling edges) and the counter is reloaded. An SCIX3 interrupt is also generated if the value of the AEDIE bit in ICR is 1. Retention by TCNT and TPRE is released by reading these registers.
(4) The bit rate as calculated from the values counted during intervals between valid edges can be used for adjusting the rate by changing the settings of the SCI12 module. To disable the bit-rate measurement after a match with Control Field 1, write 0 to the BRME bit in CR0.



Note 1. The contents of the read buffers are read by reading TCNT and TPRE.
Note 2. The AEDF bit in STR becomes 1 on detection of a valid edge.
Note 3. The current counter value is retained in the read buffers on detection of a valid edge.
Note 4. The value retained in the read buffers due to one valid edge is not updated to the new value even if a further valid edge is detected.
Note 5. Retention of a value in a read buffer due to a valid edge is released by reading TCNT or TPRE.

Figure 29.63 Example of Operations for Bit-Rate Measurement

29.9.7 Selectable Timing for Sampling Data Received through RXDX12

The extended serial mode control section provides a way of adjusting the timing for the sampling of data received through the RXDX12 pin of an SCI12 module by setting the RTS0 and RTS1 bits in CR2 to select the rising edges of 8, 10, 12, or 14 cycles of SCI base clock. If the value of the ABCS bit in SEMR is 1, the bits select the rising edges of 4, 5, 6, or 7 cycles of the SCI base clock of the SCI12 module. Figure 29.64 shows timing for the sampling of data received through RXDX12.

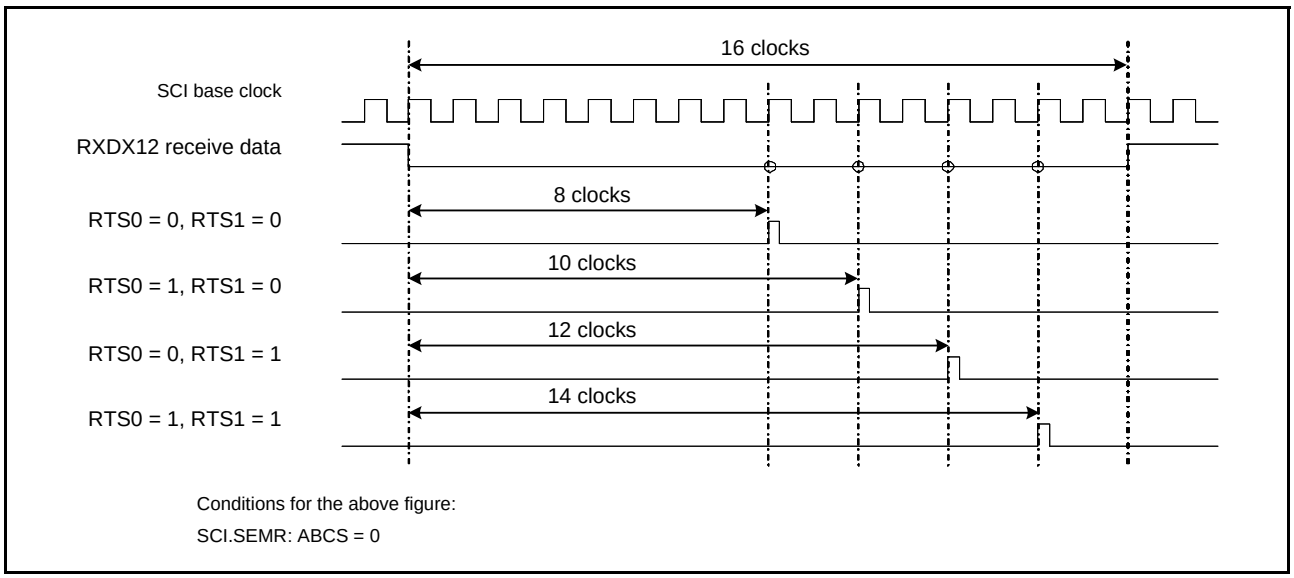


Figure 29.64 Timing for Sampling of Data Received through RXDX12

29.9.8 Timer

The timer has the following operating modes.

(1) Break Field Low Width Output Mode

This mode is for output through the TXDX12 pin of the low level over the Break Field low width at the time of transmitting a Start Frame. Setting TOMS0 to 0 and TOMS1 to 1 in TMR switches operation to Break Field low width output mode. The TCSS[2:0] bits in TMR select the clock source for the counter. When the TCST bit in TCR is set to 1, the output on the TXDX12 pin goes to the low level and counting starts. When the timer underflows, the output on the TXDX12 pin goes to the high level and the BFDF bit in the STR is set to 1. An SCIX0 interrupt is also generated if the value of the BFDIE bit in ICR is 1. When 0 is written to the TCST bit in TCR, counting stops after reloading of TPRE and TCNT. After output of the Break Field low width is completed, stop the timer before it underflows again. Figure 29.65 shows an example of operations in Break Field low width output mode.

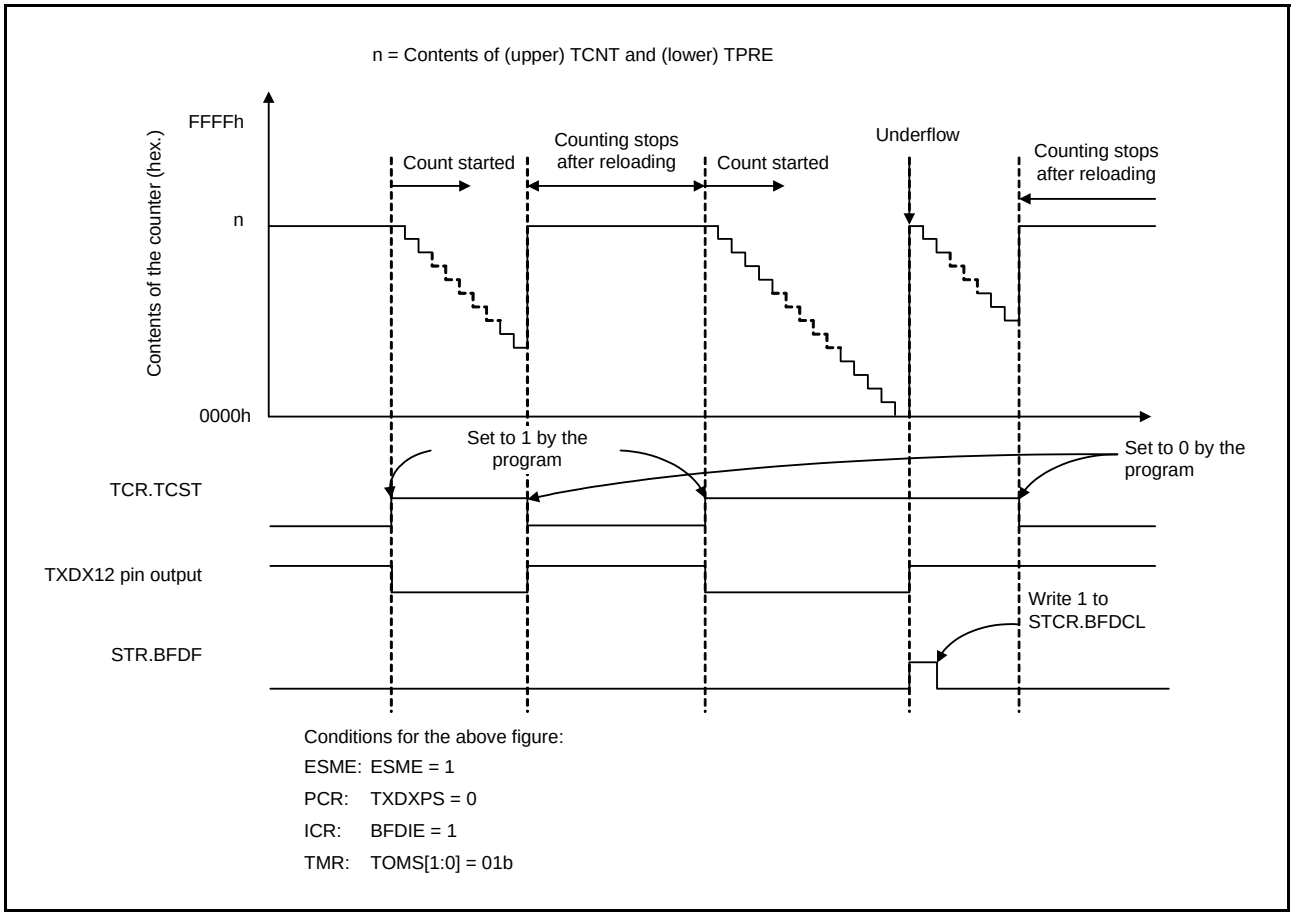


Figure 29.65 Example of Operations in Break Field Low Width Output Mode

(2) Break Field Low Width Determination Mode

This mode is for determining the Break Field low width in the input signal on the RXDX12 pin at the time of receiving a Start Frame. Setting TOMS0 to 1 and TOMS1 to 0 in TMR switches operation to Break Field low width determination mode. The TCSS[2:0] bits in TMR select the clock source for the counter. When the TCST bit in TCR is set to 1, the interface enters the Break Field low width determinable state. Determination starts when a low level is input from the RXDX12 pin. When a high level is then input on the RXDX12 pin, TPRE and TCNT are reloaded and the interface enters the Break Field low width determinable state. When the timer underflows during Break Field low width determination, the BFDF bit in STR is set to 1. An SCIX0 interrupt is also generated if the value of the BFDIE bit in ICR is 1. If an underflow of the timer during data transfer cause a problem in the form of interrupt generation, stop the timer after Break Field low width determination. Figure 29.66 shows an example of operations in Break Field low width output mode.

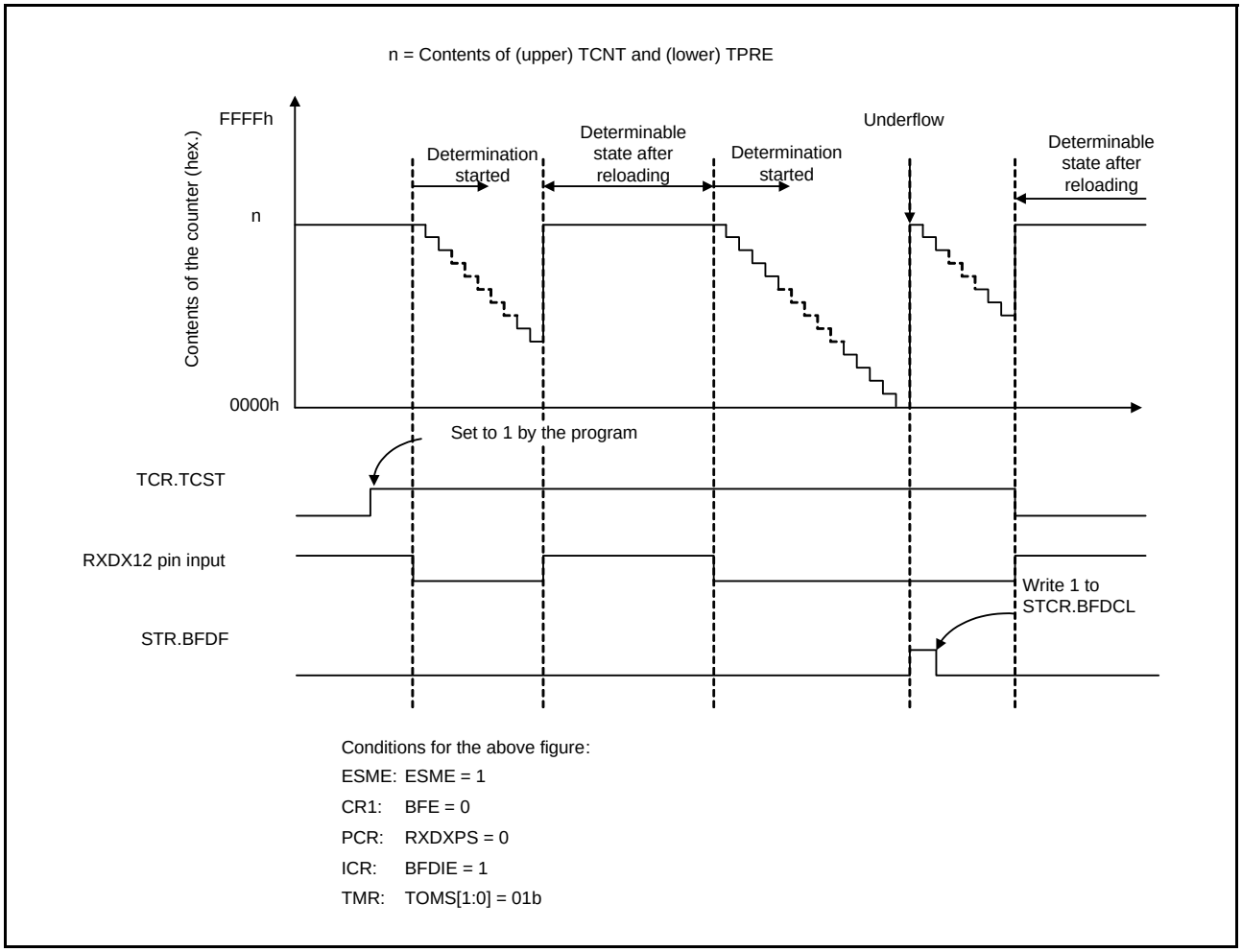


Figure 29.66 Example of Operations in Break Field Low Width Determination Mode

(3) Timer Mode

This mode is for counting cycles of the internal clock as the clock source. Setting TOMS0 to 0 and TOMS1 to 0 in TMR switches operation to timer mode. The TCSS[2:0] bits in TMR select the clock source for counting. Counting starts when 1 is written to the TCST bit in TCR and stops when 0 is written to TCST. TPRE and TCNT both count down. TPRE counts cycles of the clock source for counting, and underflows of TPRE provide the clock source for counting by TCNT. When the timer underflows, the BFDF bit in STR is set to 1. An SCIX0 interrupt is also generated if the value of the BFDIE bit in ICR is 1.

29.10 Noise Cancellation Function

Figure 29.67 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of two stages of flip-flop circuits and a match-detection circuit. When the level on the pin matches in three consecutive samples taken at the set sampling interval, the matching level continues to be conveyed internally until the level on the pin again matches in three consecutive samples.

In asynchronous mode, the noise cancellation function can be applied on the RXDn input signal. The period of the base clock (1/16th of a bit-period when SEMR.ABCS = 0 and 1/8th of a bit-period when SEMR.ABCS = 1) is the sampling interval.

In simple I^2C mode, the noise cancellation function can be applied on the SSDAn and SSCLn input signals. The sampling clock is the clock signal produced by frequency-dividing the signal from the clock source for the internal baud-

rate generator by one, two, four, or eight as selected by the setting of the SNFR.NFCS[2:0] bits.
If the base clock is stopped with the noise filter enabled and then the clock input is started again, the noise filter operation resumes from where the clock was stopped. If SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, it is determined that a level match is detected and is conveyed to the internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in three consecutive samples.

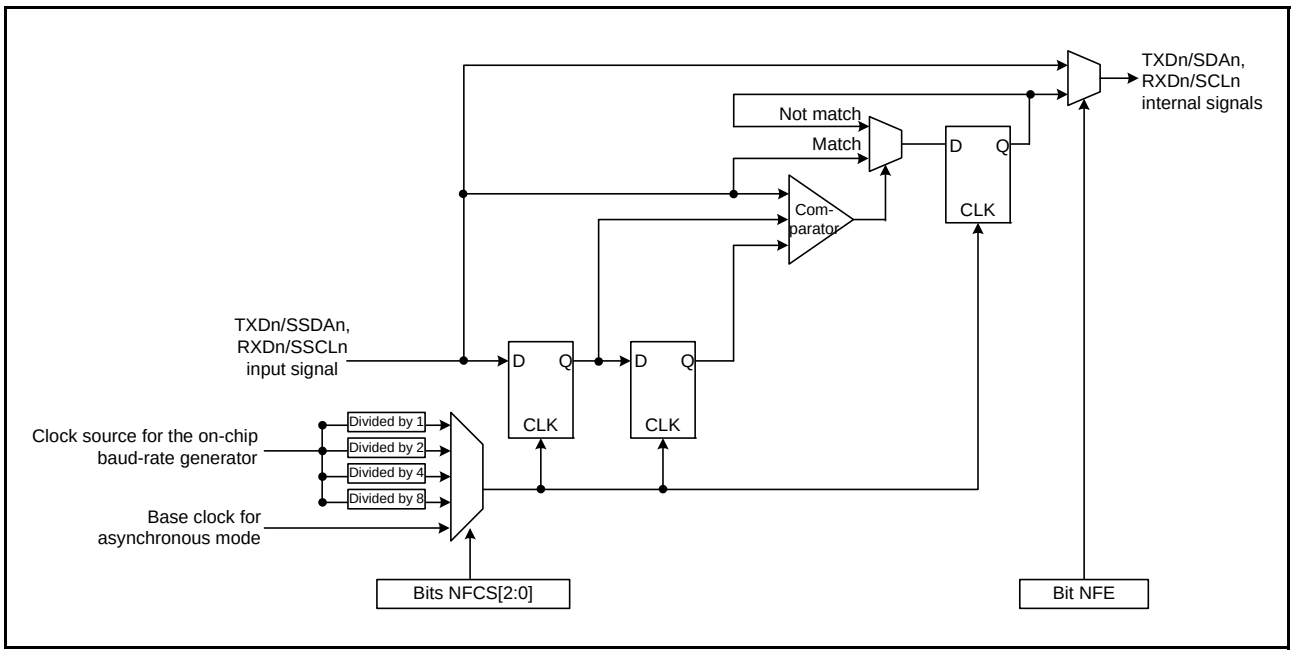


Figure 29.67 Block Diagram of Digital Noise Filter Circuit

29.11 Interrupt Sources

29.11.1 Buffer Operations for TXI and RXI Interrupts

If the conditions for a TXI and RXI interrupt are satisfied while the interrupt status flag in the interrupt controller is 1, the interrupt controller does not output the interrupt request but retains it internally (with a capacity for retention of one request per source).
When the value of the interrupt status flag in the interrupt controller becomes 0, the interrupt request retained within the interrupt controller is output. The internally retained interrupt request is automatically discarded once the actual interrupt is output. Clearing of the corresponding interrupt enable bit (the TIE or RIE bit in the SCR) can also be used to discard an internally retained interrupt request.

29.11.2 Interrupts in Serial Communications Interface and Simple SPI Mode

Table 29.26 lists interrupt sources in serial communication interface mode and simple SPI mode. A different interrupt vector is assigned to each interrupt source, and individual interrupt sources can be enabled or disabled with the enable bits in SCR.
If the SCR.TIE bit is 1, a TXI interrupt request is generated when data for transmission are transferred from the TDR to the TSR. A TXI interrupt request can also be generated by setting the SCR.TE bit to 1 after setting the SCR.TIE bit to 1 or by using a single instruction to set the SCR.TE and SCR.TIE bit to 1 at the same time. A TXI interrupt request can activate the DTC or DMAC to handle data transfer.
A TXI interrupt request is not generated by setting the SCR.TE bit to 1 while the setting of the SCR.TIE bit is 0 or by setting the SCR.TIE bit to 1 while the setting of the SCR.TE bit is 1.*1
When new data are not written by the time of transmission of the last bit of the current data for transmission and the

setting of the SCR.TEIE bit is 1, the SSR.TEND flag becomes 1 and a TEI interrupt request is generated. Furthermore, when the setting of the SCR.TE bit is 1, the SSR.TEND flag retains the value 1 until further data for transmission are written to the TDR, and setting the SCR.TEIE bit to 1 leads to the generation of a TEI interrupt request.
Writing data to the TDR leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the TEI interrupt request.
If the SCR.RIE bit is 1, an RXI interrupt request is generated when received data are stored in the RDR. An RXI interrupt request can activate the DTC or DMAC to handle data transfer.
Setting of any from among the ORER, FER, and PER flags in the SSR to 1 while the SCR.RIE bit is 1 leads to the generation of an ERI interrupt request. An RXI interrupt request is not generated at this time. Clearing all three flags (ORER, FER, and PER) leads to discarding of the ERI interrupt request.

Note 1. To temporarily prohibit TXI interrupts at the time of transmission of the last of the data and so on when you wish a new round of transmission to start after handling of the transmission-completed interrupt, control prohibiting and permitting of the interrupt by using the interrupt request enable bit in the interrupt controller rather than using the SCR.TIE bit. This can prevent the suppression of TXI interrupt requests in the transfer of new data.

Table 29.26 SCI Interrupt Sources

Name	**Interrupt Source**	Interrupt Flag	DTC Activation	DMAC Activation	Priority
ERI	Receive error	ORER, FER, or PER	Not possible	Not possible	High
RXI	Receive data full	—	Possible	Possible	↑
TXI	Transmit data empty	—	Possible	Possible	
TEI	Transmit end	TEND	Not possible	Not possible	Low

29.11.3 Interrupts in Smart Card Interface Mode

Table 29.27 lists interrupt sources in smart card interface mode. A transmit end interrupt (TEI) request cannot be used in this mode.

Table 29.27 SCI Interrupt Sources

Name	**Interrupt Source**	Interrupt Flag	DTC Activation	DMACA Activation	Priority
ERI	Receive error or error signal detection	ORER, PER, or ERS	Not possible	Not possible	High
RXI	Receive data full	—	Possible	Possible	↑
TXI	Transmit data empty	TEND	Possible	Possible	Low

Data transmission/reception using the DTC or DMAC is also possible in smart card interface mode, similar to in the normal SCI mode. In transmission, when the TEND flag in SSR is set to 1, a TXI interrupt request is generated. This TXI interrupt request activates the DTC or DMAC allowing transfer of transmit data if the TXI request is specified beforehand as a source of DTC or DMAC activation. The TEND flag is automatically cleared to 0 when the DTC or DMAC transfers the data.
If an error occurs, the SCI automatically re-transmits the same data. During the retransmission, the TEND flag is kept to 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission in the case of error occurrence. However, the ERS flag in SSR is not automatically cleared to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the RIE bit in SCR to 1 to enable an ERI interrupt request to be generated at error occurrence.
When transmitting/receiving data using the DTC or DMAC, be sure to make settings to enable the DTC or DMAC before making SCI settings. For DTC or DMAC settings, see section 18, DMA Controller (DMACA) and section 19, Data Transfer Controller (DTCa).

In reception, an RXI interrupt request is generated when receive data is set to RDR. This RXI interrupt request activates the DTC or DMAC allowing transfer of receive data if the RXI request is specified beforehand as a source of DTC or DMAC activation. If an error occurs, the error flag is set. Therefore, the DTC or DMAC is not activated and an ERI interrupt request is issued to the CPU instead; the error flag must be cleared.

29.11.4 Interrupts in Simple I2C Mode

The interrupt sources in simple I2C mode are listed in Table 29.28. The STI interrupt is allocated to the transmit end interrupt (TEI) request. The receive error interrupt (ERI) request cannot be used.
The DTC and DMAC can also be used to handle transfer in simple I2C mode.
When the value of the IICINTM bit in SIMR2 is 1, an RXI request will be generated on the falling edge of the SSCL signal for the eighth bit. If the RXI has been set up as an activating request for the DTC or DMAC beforehand, the RXI request will activate the DTC or DMAC to handle transfer of the received data. Furthermore, a TXI request is generated on the falling edge of the SSCLn signal for the ninth bit (acknowledge bit). If the TXI has been set up as an activating request for the DTC or DMAC beforehand, the TXI request will activate the DTC or DMAC to handle transfer of the data for transmission.
When the value of the IICINTM bit in SIMR2 is 0, an RXI request (ACK detection) if the input on the SSDAn pin is at the low level or a TXI request (NACK detection) if the input on the SSDAn pin is at the high level will be generated on the rising edge of the SSCLn signal for the ninth bit (acknowledge bit). If the RXI has been set up as an activating request for the DTC or DMAC beforehand, the RXI request will activate the DTC or DMAC to handle transfer of the received data.
Also, if the DTC or DMAC is used for data transfer in reception or transmission, be sure to set up and enable the DTC or DMAC before setting up the SCI.
When the IICSTAREQ, IICSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 29.28 SCI Interrupt Sources

Name	**Interrupt Source**	Interrupt Flag	DTC Activation	DMAC Activation	Priority
RXI	Reception, ACK detection	—	Possible	Possible	High
TXI	Transmission, NACK detection	—	Possible*1	Possible*1	↑
STI	Completion of generating a start, restart, or stop condition	IICSTIF	Not possible	Not possible	Low

Note 1. Activation of the DTC or DMAC is only possible when the SIMR2.IICINTM bit is 1 (selecting reception and interrupts).

29.11.5 Interrupts from the Extended Serial Mode Control Section

The extended serial mode control section has a total of six types of interrupt request for generating the SCIX0 interrupt (Break Field low width detected), SCIX1 interrupt (Control Field 0 match, Control Field 1 match, priority interrupt bit detected), SCIX2 interrupt (bus collision detected), and SCIX3 interrupt (valid edge detected). When any of the interrupt factors is generated, the corresponding status flag is set to 1. Details of all of the interrupt requests are listed in Table 29.29.

Table 29.29 Interrupt Sources of the Extended Serial Mode Control Section

Interrupt Request	Status Flag	Interrupt Factors
SCIX0 interrupt (Break Field low width detected)	BFDF	• Detection of a Break Field low width longer than the interval corresponding to the timer setting • Completion of the output of a Break Field low width over the interval corresponding to the timer setting • Underflow of the timer
SCIX1 interrupt (Control Field 0 match)	CF0MF	The data received in Control Field 0 matching the value set in CF0DR
SCIX1 interrupt (Control Field 1 match)	CF1MF	The data received in Control Field 1 matching the value set in PCF1DR or SCF1DR
SCIX1 interrupt (priority interrupt bit detected)	PIBDF	The value of the bit specified as the priority interrupt bit matching the value set in PCF1DR
SCIX2 interrupt (bus collision detected)	BCDF	The output level on the TXDX12 pin and the input level on the RXDX12 pin not matching on three consecutive cycles of the bus-collision detection clock
SCIX3 interrupt (valid edge detected)	AEDF	Detection of a valid edge during bit-rate measurement

29.12 Usage Notes

29.12.1 Setting the Module-Stop Function

Module-stop control registers B and C (MSTPCRB and MSTPCRC) are used to stop and start SCI operations. With the value after a reset, SCI operations are stopped. The registers of the modules only become accessible after release from the module-stop state. For details, refer to section 12, Low Power Consumption.

29.12.2 Break Detection and Processing

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and so the FER flag in SSR is set to 1 (framing error), and the PER flag in SSR may also be set to 1 (parity error). The SCI continues the receive operation even after a break is received. Therefore, note that even if the FER flag is cleared to 0 (no framing error), it will be set to 1 again.

29.12.3 The Mark State and Production of Breaks

When the SCR.TE bit is 0 (prohibiting serial transmission), setting the I/O port function makes selection of the level and direction (input or output) of the TXDn pin possible. If this is done, the TXDn pin can be placed in the mark state to send a break at the time of data transmission. Until the SCR.TE bit is set to 1 (permitting serial transmission), Set up output of the high level on the TXDn pin and select general input/output port as the pin’s mode. On the other hand, when you wish to transmit a break, use the I/O port function settings to select the output of a 0 on the TXDn pin and select general input/output port as the pin’s mode.When the SCR.TE bit is cleared to 0, the transmission section is initialized regardless of the current state of transmission.

29.12.4 Receive Error Flags and Transmit Operations (Clock Synchronous Mode Only)

Transmission cannot be started when a receive error flag (ORER) in SSR is set to 1, even if data is written to TDR. Be sure to clear the receive error flags to 0 before starting transmission. Note also that the receive error flags cannot be cleared to 0 even if the RE bit in SCR is cleared to 0 (serial reception disabled).

29.12.5 Writing Data to TDR

Data can always be written to TDR. However, if new data is written to TDR when transmit data is remaining in TDR, the previous data in TDR is lost because it has not been transferred to TSR yet. Be sure to write transmit data to TDR in the TXI interrupt request processing routine.

29.12.6 Restrictions on Clock Synchronous Transmission

When the external clock source is used as a synchronization clock, update TDR by the DMAC or DTC and wait for at least five clock cycles before allowing the transmit clock to be input. If the transmit clock is input within four clock cycles after TDR is updated, the SCI may malfunction.

29.12.7 Restrictions on Using DTC or DMAC

When using the DMAC or DTC to read RDR, be sure to set the receive end interrupt (RXI) as the activation source of the relevant SCI.

29.12.8 Points to Note on Starting Transfer

At the point where transfer starts when the interrupt status flag in the interrupt controller is 1, follow the procedure below to clear interrupt requests before permitting operations (by setting the SCR.TE or SCR.RE bit to 1).

- Confirm that transfer has stopped (the setting of the SCR.TE or SCR.RE bits is 0).
- Set the corresponding interrupt enable bit (SCR.TIE or SCR.RIE) to 0.
- Read out the corresponding interrupt enable bit (SCR.TIE or SCR.RIE bit) to check that it has actually become 0.
- Set the interrupt status flag in the interrupt controller to 0.

29.12.9 SCI Operations during Low Power Consumption State

(1) Transmission

When making the setting for module-stop state or a transition to software standby, do so after switching the general input/output port function for the TXDn pin and then stopping operation (clear TIE, TE, and TEIE in the SCR to 0). Clearing of the TE bit leads to resetting of the TSR and of the TEND bit in the SSR.The state of output on an output pin when the interface is in the module-stop state or the chip is on software standby depends on the port settings, but is at the high level on release. When a transition is made while transmission is in progress, the data that were being transmitted become undefined.

To transmit data in the same transmission mode after cancellation of the low power consumption state, set the TE bit to 1, read SSR, and write data to TDR sequentially to start data transmission. To transmit data with a different transmission mode, initialize the SCI first.

Figure 29.68 shows a sample flowchart for transition to software standby mode during transmission. Figure 29.69 and Figure 29.70 show the port pin states during transition to software standby mode.

Before specifying the module-stop state or making a transition to software standby mode from the transmission mode, stop the transmit operations (TE = 0). To start transmission after cancellation, set the TE bit to 1. The TXI interrupt flag is set to 1 and transmission starts.

(2) Reception

Before specifying the module-stop state or making a transition to software standby mode, stop the receive operations (RE = 0 in SCR). If transition is made during data reception, the data being received will be invalid.

To receive data in the same reception mode after cancellation of the low power consumption state, set the RE bit to 1, and then start reception. To receive data in a different reception mode, initialize the SCI first.

Figure 29.71 shows a sample flowchart for transition to software standby mode during reception.

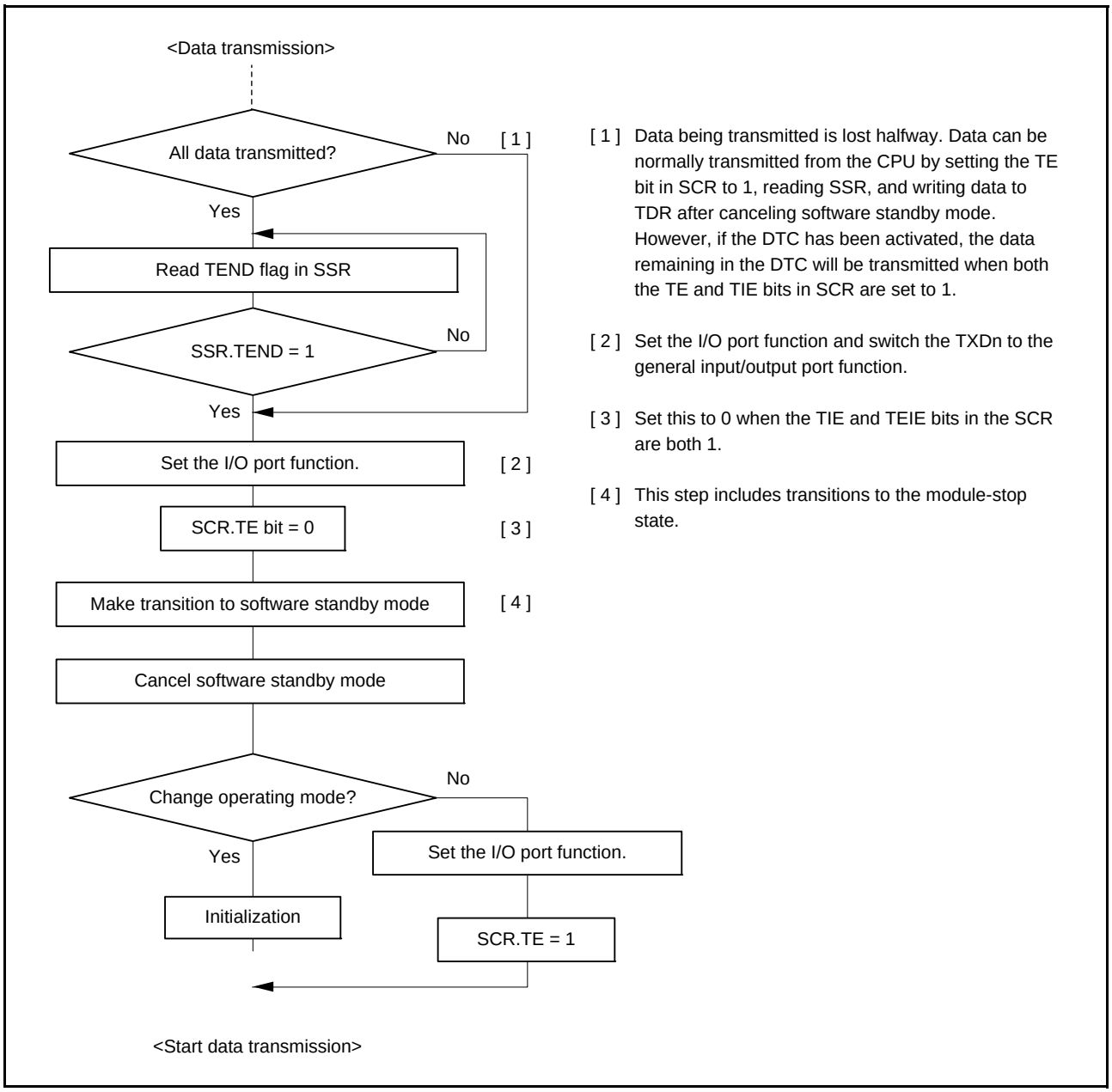


Figure 29.68 Example of Flowchart for Transition to Software Standby Mode during Transmission

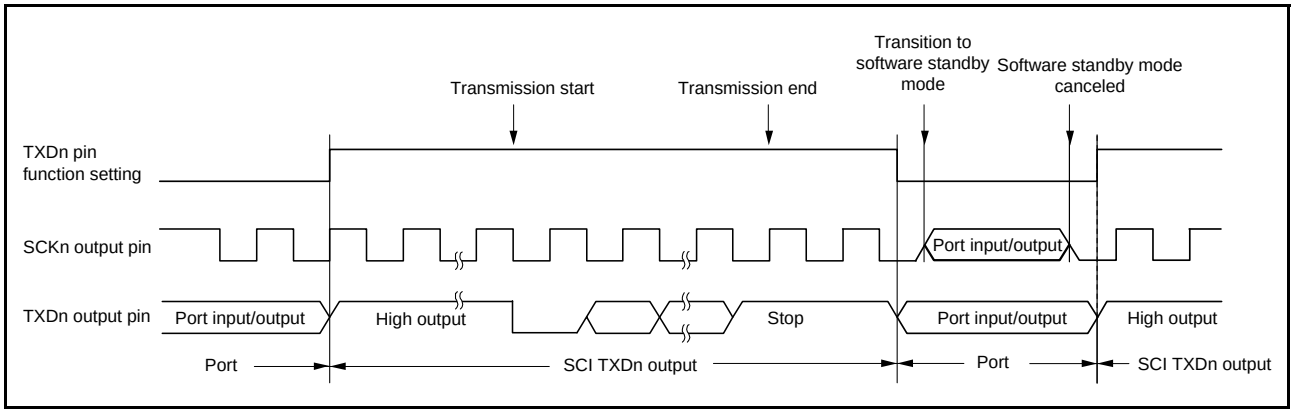
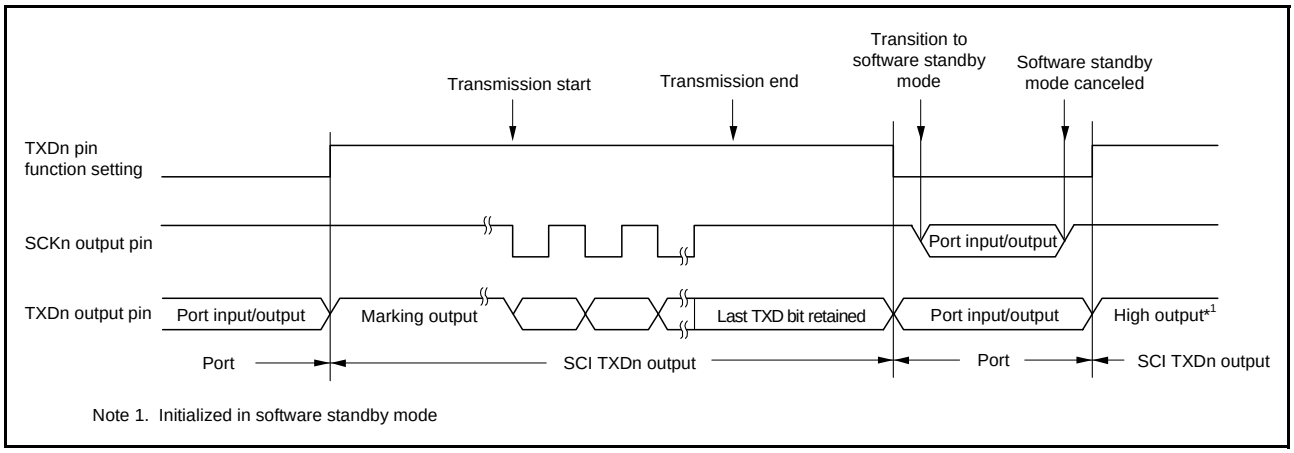


Figure 29.69 Port Pin States during Transition to Software Standby Mode (Internal Clock, Asynchronous Transmission)



Note 1. Initialized in software standby mode

Figure 29.70 Port Pin States during Transition to Software Standby Mode (Internal Clock, Clock Synchronous Transmission)

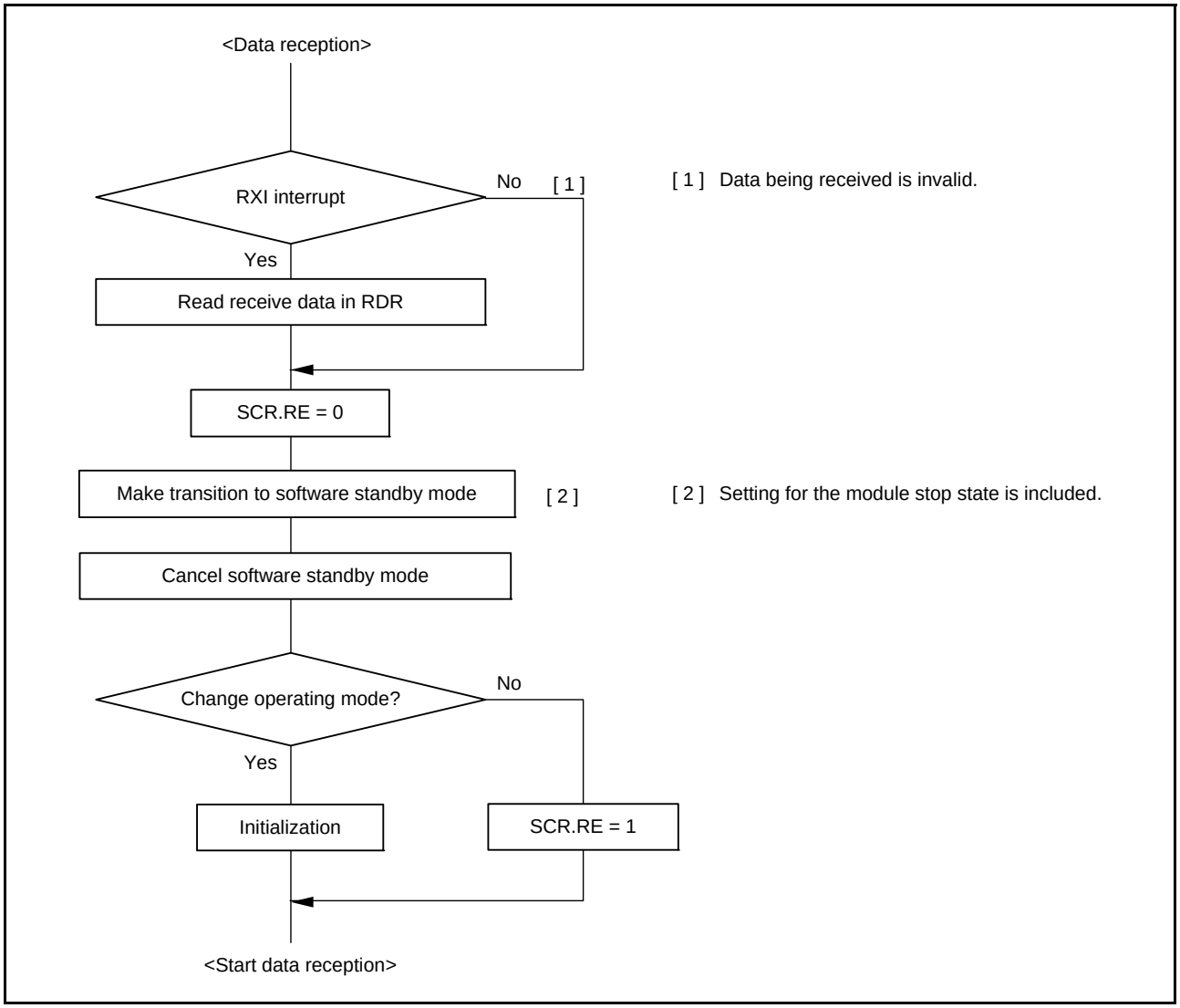


Figure 29.71 Example of Flowchart for Transition to Software Standby Mode during Reception

29.12.10 External Clock Input in Clock Synchronous Mode

In clock synchronous mode or simple SPI mode, the external clock SCKn must be input as follows:
High-pulse period, low-pulse period = 2 PCLK cycles or more, period = 6 PCLK cycles or more

29.12.11 Limitations on Simple SPI Mode

(1) Master Mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transmit/receive clock set by the SPMR.CKPH and CKPOL when the SPMR.SSE bit is 1. This is to prevent the clock line to enter high-impedance state when the SCR.TE bit is set to 0 and prevent occurrence of unintended edge on the clock line when the SCR.TE bit is changed from 0 to 1. The clock line does not enter high-impedance state even when the SCR.TE bit is set to 0 in master mode and when the SPMR.SSE bit is 0, that is, no pull up or pull down is required.
- In the case of the setting for clock delay (the SPMR.CKPH bit is 1), the received data full interrupt (RXI interrupt) is generated before the final clock edge on the SCKn pin as indicated in Figure 29.72. At this time, if the TE and RE bits in the SCR are cleared to 0 before the last edge of the clock signal on the SCKn pin, the SCKn pin enters the high-impedance state and the width of the last pulse of the transfer clock is reduced. Furthermore, the signal from a connected slave on the SSn# pin after an RXI interrupt going to the high level before the last edge of the clock signal on the SCKn pin creates a possibility of erroneous operation by the slave.
- When operation is in multi-master mode, take care because the SCKn pin output becomes high impedance while the input on the SS# pin is at the low level if a mode-fault error occurs as the current character is being transferred, stopping supply of the clock signal to the connected slave. Remake the settings for the connected slave to avoid misaligned bits when transfer is restarted

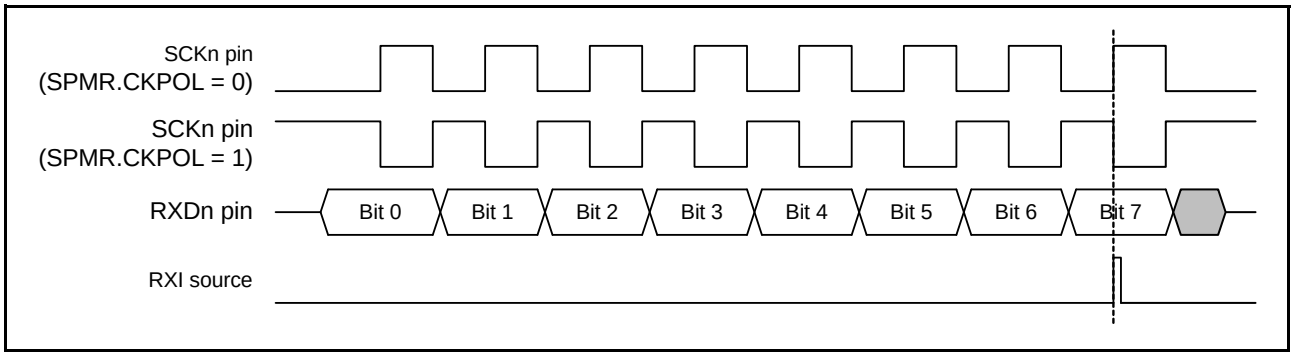


Figure 29.72 Timing of the RXI Interrupt in Simple SPI Mode (with Clock Delay)

(2) Slave Mode

- When data for transmission are written to the TDR, secure at least five cycles of the PCLK from input of the low level on the SSn# pin to input of the external clock.
- Provide an external clock signal to the master the same as the data length for transfer.
- Control the input on the SSn# pin before the start and after the end of data transfer.
- When the level being input on the SSn# pin is to be changed from low to high while the current character is being transferred, set the TE and RE bits in the SCR to 0 and, after remaking the settings, restart transfer of the first byte.

29.12.12 Limitation 1 on Usage of the Extended Serial Mode Control Section

When the SHARPS bit in PCR is set to 1, output on the TXDX12/RXDX12 pin is only possible when the following conditions apply.

- The timer of the SCId module is in Break Field low width output mode and the value of the TCST bit in TCR is 1 (when the TCST bit is set to 1, the high level continues to be output for up to one cycle of the clock source for counting by the timer counter before output of the low level)
- The value of the TE bit in SCI12.SCR is 1.

29.12.13 Limitation 2 on Usage of the Extended Serial Mode Control Section

An SCIc interrupt request is generated even if the extended serial mode is enabled. However, the SCIc interrupt should not be used during reception of a start frame because SCId uses an SCIc interrupt request.
The two ways of dealing with this are described below. When a reception error is detected, clear the error flag of the SCIc and initialize the control section of the SCId following the example of flowchart shown in Figure 29.73.

(1) Set the SCR.RIE bit of the SCIc to 0 to disable the output of interrupt requests. Check the error flags in the SSR register for SCIc on completion of the reception of a start frame, because an ERI interrupt is not generated if a reception error occurs. After reception of the start frame is completed, set the SCR.RIE bit of the SCIc to 1 by the time the first byte of the information frame is received.
(2) Set the SCR.RIE bit of the SCIc to 1 to disable RXI interrupts and enable ERI interrupts for ICU.
Clear the IRn.IR flag to enable the acceptance of RXI interrupts by ICU by the time the first byte of the information frame is received after the completion of start frame reception.

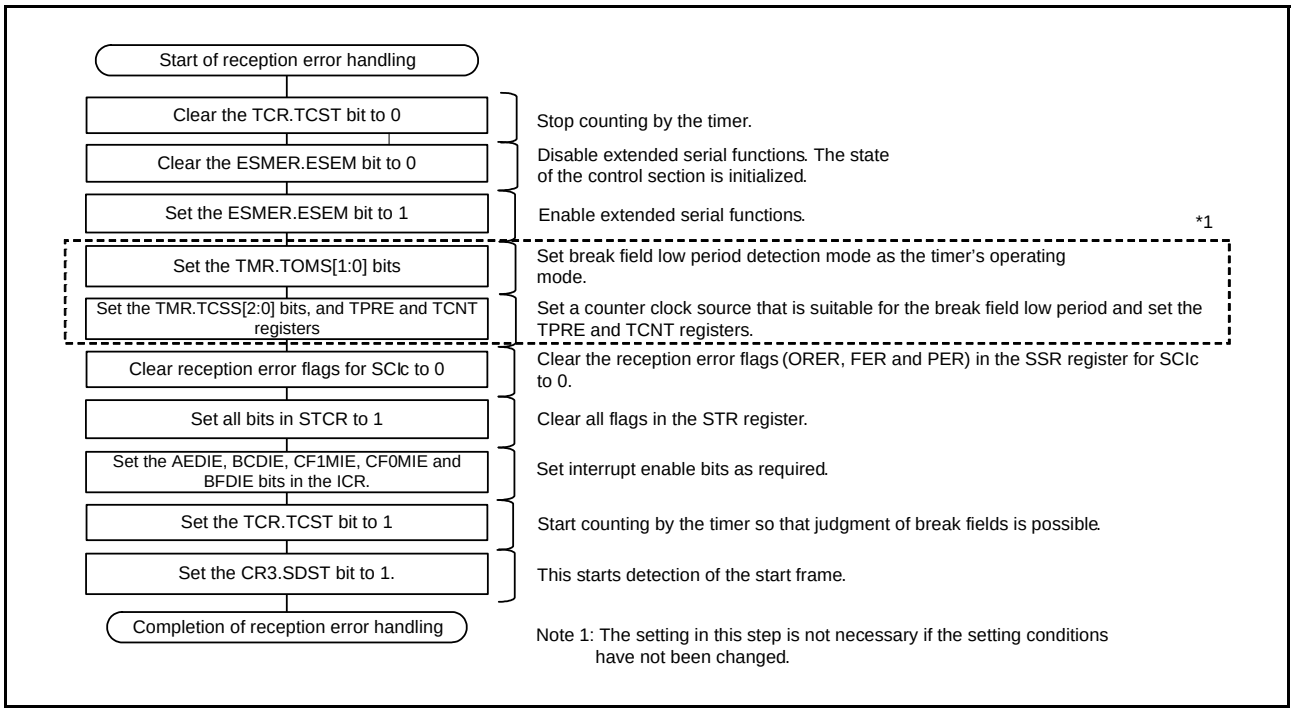


Figure 29.73 Example of Flowchart for Reception Error Handling (During Reception of the Start Frame)

29.12.14 Note in Relation to Transmit Enable Bit (TE)

When the SCR.TE bit is set to 0 (serial transmission disabled) with a pin functions as TXDn (n = 0 to 3, 12), the pin output goes high impedance. To avoid the TXDn line going high impedance, take any of the following methods.

(1) Connect pull-up resistor to the TXDn line.
(2) Before setting the SCR.TE bit to 0, modify the pin function to "general I/O port, output", or, after setting the SCR.TE bit to 1, modify the pin function to TXDn.

30. I2C Bus Interface (RIIC)

This MCU has two I2C bus interfaces (RIIC modules).
The RIIC module conforms with and provides a subset of the NXP I2C bus (Inter-IC-Bus) interface functions.

30.1 Overview

Table 30.1 lists the specifications of the RIIC, Figure 30.1 shows a block diagram of the RIIC, and Figure 30.2 shows an example of I/O pin connections to external circuits (I2C bus configuration example). Table 30.2 lists the I/O pins of the RIIC.

Table 30.1 RIIC Specifications

Item	Specifications
Communications format	• I2C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various set-up times, hold times, and bus-free times for the transfer rate
Transfer rate	Up to 400 kbps
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three slave-address settings can be made. • Seven- and ten-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the clock signal (SCL) at the low level: Waiting between the eighth and ninth clock cycles Waiting between the ninth clock cycle and the first clock cycle of the next transfer (WAIT function)
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation Operation to synchronize the SCL (clock) signal in cases of conflict with the SCL signal from another master is possible. When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal time-out function is capable of detecting long-interval stop of the SCL (clock signal).
Noise removal	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	• Four sources: Error in transfer or occurrence of events (detection of AL, NACK, time-out, a start condition including a restart condition, or a stop condition) Receive-data-full (including matching with a slave address) Transmit-data-empty (including matching with a slave address) Transmission complete
Low power consumption function	Module-stop state can be set.

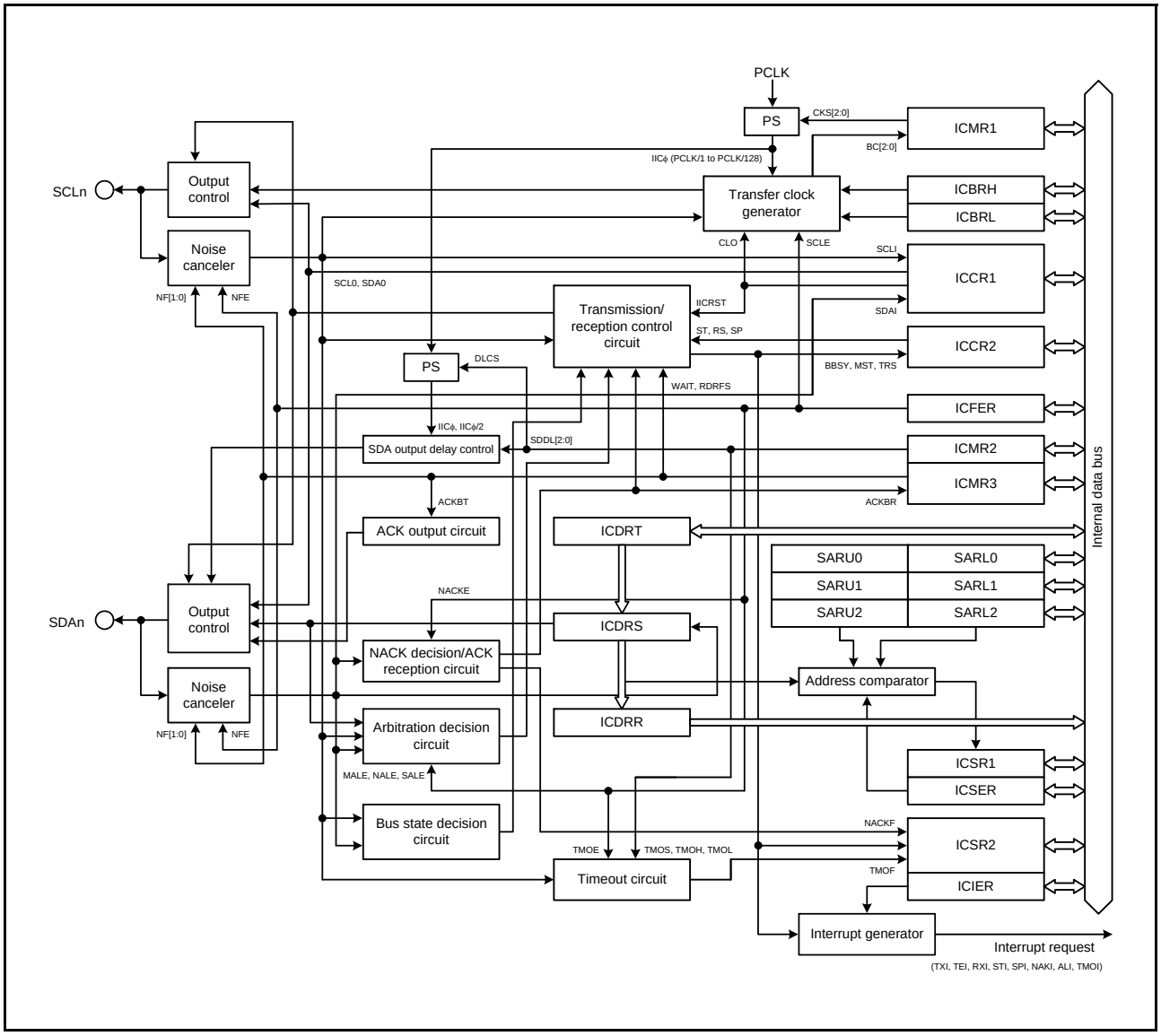


Figure 30.1 Block Diagram of RIIC

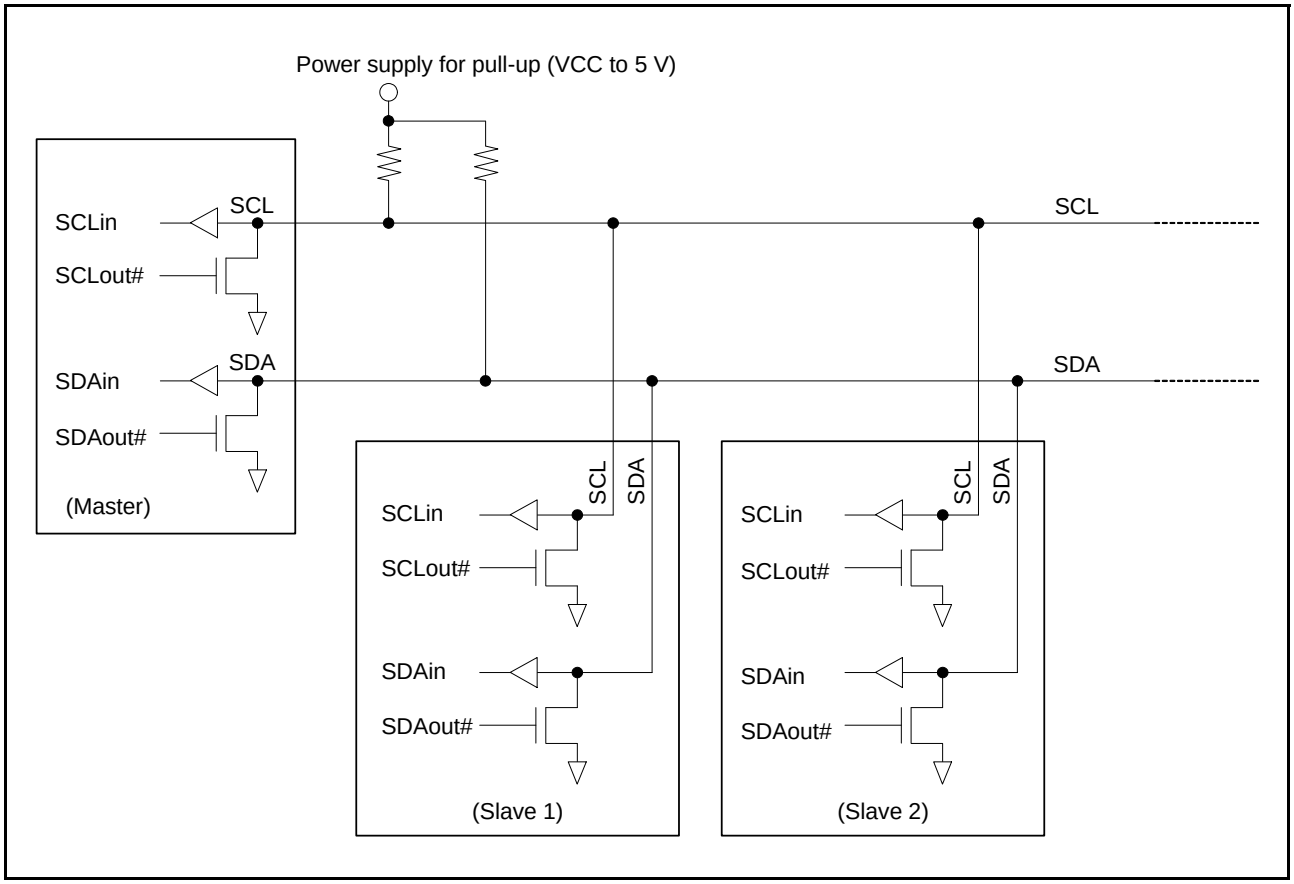


Figure 30.2 Connections to the External Circuit by the I/O Pins (I2C Bus Configuration Example)

The input level of the signals for RIIC is CMOS when I2C bus is selected (the ICMR3.SMBS bit = 0), or TTL when SMBus is selected (the ICMR3.SMBS bit = 1).

Table 30.2 Pin Configuration

Channel	Pin Name	I/O	Function
RIIC0	SCL0	I/O	RIIC0 serial clock I/O pin
	SDA0	I/O	RIIC0 serial data I/O pin
RIIC1	SCL1	I/O	RIIC1 serial clock I/O pin
	SDA1	I/O	RIIC1 serial data I/O pin

30.2 Register Descriptions

30.2.1 I2C Bus Control Register 1 (ICCR1)

Address(es): RIIC0.ICCR1 0008 8300h, RIIC1.ICCR1 0008 8320h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDAn line is at a low level. 1: SDAn line is at a high level.	R
b1	SCLI	SCL Line Monitor	0: SCLn line is at a low level. 1: SCLn line is at a high level.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: SDAn pin is at a low level. 1: SDAn pin is open. • Write: 0: Changes the SDAn pin to a low level. 1: Changes the SDAn pin to be open.	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: SCLn pin is at a low level. 1: SCLn pin is open. • Write: 0: Changes the SCLn pin to a low level. 1: Changes the SCLn pin to be open.	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: Allows the SCLO and SDAO bits to be rewritten. (This bit is read as 1.) 1: The SCLO and SDAO bits are write-protected.	R/W
b5	CLO	Extra SCL Clock Cycle Output	0: Does not output an extra SCLn clock cycle (default). 1: Outputs an extra SCLn clock cycle. (The CLO bit is cleared automatically after one clock cycle is output.)	R/W
b6	IICRST	I2C Bus Interface Internal Reset	0: Clears the RIIC reset or internal reset. 1: Initiates the RIIC reset or internal reset. (Clears the bit counter and the SCLn/SDAn output latch)	R/W
b7	ICE	I2C Bus Interface Enable	0: Disabled (SCLn, SDAn pins not driven). 0: Enabled (SCLn, SDAn pins driven). This bit also selects an RIIC reset or internal reset in combination with the IICRST bit.	R/W

SDAO Bit (SDA Output Control/Monitor), SCLO Bit (SCL Output Control/Monitor)

These bits directly control the SDAn and SCLn signals output from RIIC.

Writing value to these bits need to be accompanied by writing 0 to the SWOP bit.

Changes made to these bits are reflected in the RIIC via the input buffer. If slave mode is selected, depending on the content of the change made, the bus may be opened on detection of a start condition.

Do not rewrite these bits during start condition, stop condition, and restart condition, and while transmitting or receiving data. Otherwise, operation is not guaranteed.

Reading these bits returns the current state of the output signal from RIIC.

CLO Bit (Extra SCL Clock Cycle Output)

This bit is used to output an extra SCL clock cycle for debugging or error processing.

Normally, set the bit to 0. Setting the bit to 1 in a normal communication state causes a communication error.

For details on this function, see section 30.11.2, Extra SCL Clock Cycle Output Function.

IICRST Bit (I2C Bus Interface Internal Reset)

This bit is used to reset the internal states of the RIIC.

Setting this bit to 1 initiates an RIIC reset or internal reset.

Whether an RIIC reset or internal reset is initiated is determined according to the combination with the ICE bit. Table 30.3 lists the resets of the RIIC.

The RIIC reset resets all registers including the BBSY flag in ICCR2 and internal states of the RIIC, and the internal reset resets the bit counter (BC[2:0] bits in ICMR1), the I2C bus shift register (ICDRS), and the I2C bus status registers (ICSR1 and ICSR2) as well as the internal states of the RIIC. For the reset conditions for each register, see section 30.14, Reset States.

An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the RIIC without initializing the port settings and the control and setting registers of the RIIC when the bus or RIIC hangs up due to a communication error.

If the RIIC hangs up in a low level output state, resetting the internal states cancels the low level output state and releases the bus with the SCLn pin and SDAn pin at a high impedance.

Note: • If an internal reset is initiated using the IICRST bit for a bus hang-up occurred during communication with the master device in slave mode, the states may become different between the slave device and the master device (due to the difference in the bit counter information). For this reason, do not initiate an internal reset in slave mode, but initiate restoration processing from the master device. If an internal reset is necessary because the RIIC hangs up with the SCLn line in a low level output state in slave mode, initiate an internal reset and then issue a restart condition from the master device or resume communication from the start condition issuance after issuing a stop condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start condition or restart condition from the master device, synchronization will be lost because the master and slave devices operate asynchronously.

Table 30.3 RIIC Resets

IICRST	ICE	State	Specifications
1	0	RIIC reset	Resets all registers and internal states of the RIIC.
	1	Internal reset	Reset the BC[2:0] bits in ICMR1, and the ICSR1, ICSR2, ICDRS registers and the internal states of the RIIC.

ICE Bit (I2C Bus Interface Enable)

This bit is used to enable or disable the transfer operation of the RIIC.

When this bit is set to 0 to disable the RIIC, the SCLn pin and SDAn pin function as ports. An RIIC reset is initiated by setting the IICRST bit to 1 with the ICE bit set to 0, and an internal reset is initiated by setting the IICRST bit to 1 with the ICE bit set to 1.

To prevent unexpected communications, set the RIIC registers with the ICE bit set to 0 (to disable the RIIC), and set the ICE bit to 1 (to enable the transfer operation) after finishing all register settings.

Note: • In addition to the I2C bus pin functions, other functions are also multiplexed onto the pins of the RX63T Group. To use the pins as I2C bus pins (SCLn pin and SDAn pin), disable the other multiplexed functions. Since both of the SCLn pin and SDAn pin of the I2C bus pins are I/O pins, set the corresponding PORTn.PDR register to 0 (input).

30.2.2 I2C Bus Control Register 2 (ICCR2)

Address(es): RIIC0.ICCR2 0008 8301h, RIIC1.ICCR2 0008 8321h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ST	Start Condition Issuance Request	0: Does not request to issue a start condition. 1: Requests to issue a start condition.	R/W
b2	RS	Restart Condition Issuance Request	0: Does not request to issue a restart condition. 1: Requests to issue a restart condition.	R/W
b3	SP	Stop Condition Issuance Request	0: Does not request to issue a stop condition. 1: Requests to issue a stop condition.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	TRS	Transmit/Receive Mode	0: Receive mode 1: Transmit mode	R/W*1
b6	MST	Master/Slave Mode	0: Slave mode 1: Master mode	R/W*1
b7	BBSY	Bus Busy Detection Flag	0: The I2C bus is released (bus free state). 1: The I2C bus is occupied (bus busy state or in the bus free state).	R

Note 1. When the MTWP bit in ICMR1 is set to 1, the MST and TRS bits can be written to.

ST Bit (Start Condition Issuance Request)

This bit is used to request transition to master mode and issuance of a start condition.

When this bit is set to 1 to request to issue a start condition, a start condition is issued when the BBSY flag is set to 0 (bus free).

For details on the start condition issuance, see section 30.10, Start Condition/Restart Condition/Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition has been issued
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: • Set the ST bit to 1 (start condition issuance request) when the BBSY flag is set to 0 (bus free).
Note that arbitration may be lost if the ST bit is set to 1 (start condition issuance request) when the BBSY flag is set to 1 (bus busy).

RS Bit (Restart Condition Issuance Request)

This bit is used to request that a restart condition be issued in master mode.
When this bit is set to 1 to request to issue a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy) and the MST bit is set to 1 (master mode).
For details on the restart condition issuance, see section 30.10, Start Condition/Restart Condition/Stop Condition Issuing Function.
[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in ICCR2 set to 1

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition has been issued or a start condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: • Do not set the RS bit to 1 while issuing a stop condition.
Note: • In slave mode, if the RS bit is set to 1 (restart condition issuance request) in mode other than master mode, the restart condition is not issued in this mode but the restart condition issuance request bit remains set. If the operating mode changes to master mode with the bit not being cleared, the restart condition may be issued.

SP Bit (Stop Condition Issuance Request)

This bit is used to request that a stop condition be issued in master mode.
When this bit is set to 1 to request to issue a stop condition, a stop condition is issued when the BBSY flag is set to 1 (bus busy) and the MST bit is set to 1 (master mode).
For details on the stop condition issuance, see section 30.10, Start Condition/Restart Condition/Stop Condition Issuing Function.
[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in ICCR2 set to 1

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition has been issued or a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: • Writing to the SP bit is not possible while the setting of the BBSY flag is 0 (bus free).
Note: • Do not set the SP bit to 1 while a restart condition is being issued.

TRS Bit (Transmit/Receive Mode)

This bit indicates transmit or receive mode.
The RIIC is in receive mode when the TRS bit is set to 0 and is in transmit mode when the bit is set to 1. Combination of this bit and the MST bit indicates the operating mode of the RIIC.
The value of the TRS bit is automatically changed to the value for transmission mode or reception mode by detection or issuing of a start condition, setting or clearing of the R/W# bit, etc. Although writing to the TRS bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not necessary during normal usage.

[Setting conditions]

- When a start condition is issued normally according to the start condition issuance request (when a start condition is detected with the ST bit set to 1)
- When the R/W# bit added to the slave address is set to 0 in master mode

- When the address received in slave mode matches the address enabled in ICSER, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in ICMR1 set to 1

[Clearing conditions]

- When a stop condition is detected
- The AL (arbitration-lost) flag in ICSR2 being set to 1
- In master mode, reception of a slave address to which an R/W# bit with the value 1 is appended
- In slave mode, a match between the received address and the address enabled in ICSER when the value of the received R/W# bit is 0 (including cases where the received address is the general call address)
- In slave mode, a restart condition is detected (a start condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

MST Bit (Master/Slave Mode)

This bit indicates master or slave mode.

The RIIC is in slave mode when the MST bit is set to 0 and is in master mode when the bit is set to 1. Combination of this bit and the TRS bit indicates the operating mode of the RIIC.

The value of the MST bit is automatically changed to the value for master mode or slave mode by detection or issuing of a start condition, etc. Although writing to the MST bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not necessary during normal usage.

[Setting conditions]

- When a start condition is issued normally according to the start condition issuance request (when a start condition is detected with the ST bit set to 1)
- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 0 is written to the MST bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

BBSY Flag (Bus Busy Detection)

The BBSY flag indicates whether the I2C bus is occupied (bus busy) or released (bus free).

This bit is set to 1 when the SDAnn line changes from high to low under the condition of SCLn = high, assuming that a start condition has been issued.

When the SDAn line changes from low to high under the condition of SCLn = high, this bit is cleared to 0 after the bus free time (specified in ICBRL) start condition is not detected, assuming that a stop condition has been issued.

[Setting condition]

- When a start condition is detected

[Clearing conditions]

- When the bus free time (specified in ICBRL) start condition is not detected after detecting a stop condition
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (RIIC reset)

30.2.3 I2C Bus Mode Register 1 (ICMR1)

Address(es): RIIC0.ICMR1 0008 8302h, RIIC1.ICMR1 0008 8322h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	BC[2:0]	Bit Counter	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	R/W*1
b3	BCWP	BC Write Protect	0: Enables a value to be written in the BC[2:0] bits. (This bit is read as 1.)	R/W*1
b6 to b4	CKS[2:0]	Internal Reference Clock (IICϕ) Selection	b6 b4 0 0 0: PCLK/1 clock 0 0 1: PCLK/2 clock 0 1 0: PCLK/4 clock 0 1 1: PCLK/8 clock 1 0 0: PCLK/16 clock 1 0 1: PCLK/32 clock 1 1 0: PCLK/64 clock 1 1 1: PCLK/128 clock	R/W
b7	MTWP	MST/TRS Write Protect	0: Disables writing to the MST and TRS bits in ICCR2. 1: Enables writing to the MST and TRS bits in ICCR2.	R/W

Note 1. Set the BCWP bit to 0 to rewrite the BC[2:0] bits. The BC[2:0] bits must be rewritten by using the MOV instruction.

BC[2:0] Bits (Bit Counter)

These bits function as a counter that indicates the number of bits remaining to be transferred at the detection of a rising edge on the SCLn line. Although these bits are writable and readable, it is not necessary to access these bits under normal conditions.

To write to these bits, specify the number of bits to be transferred plus one (data is transferred with an additional acknowledge bit) between transferred frames when the SCLn line is at a low level.

The values of the BC[2:0] bits return to 000b at the end of a data transfer including the acknowledge bit or when a start condition including a restart condition is detected.

30.2.4 I2C Bus Mode Register 2 (ICMR2)

Address(es): RIIC0.ICMR2 0008 8303h, RIIC1.ICMR2 0008 8323h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			TMWE	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOS	Timeout Detection Time Selection	0: Long mode is selected. 1: Short mode is selected.	R/W
b1	TMOL	Timeout L Count Control	0: Count is disabled while the SCLn line is at a low level. 1: Count is enabled while the SCLn line is at a low level.	R/W
b2	TMOH	Timeout H Count Control	0: Count is disabled while the SCLn line is at a high level. 1: Count is enabled while the SCLn line is at a high level.	R/W
b3	TMWE	Timeout Internal Counter Write Enable	0: Writing to the timeout detection internal counter is disabled. 1: Writing to the timeout detection internal counter is enabled.	R/W
b6 to b4	SDDL[2:0]	SDA Output Delay Counter	• When ICMR2.DLCS = 0 (IICϕ) b6 b4 0 0 0: No output delay 0 0 1: 1 IICϕ cycle 0 1 0: 2 IICϕ cycles 0 1 1: 3 IICϕ cycles 1 0 0: 4 IICϕ cycles 1 0 1: 5 IICϕ cycles 1 1 0: 6 IICϕ cycles 1 1 1: 7 IICϕ cycles • When ICMR2.DLCS = 1 (IICϕ/2) b6 b4 0 0 0: No output delay 0 0 1: 1 or 2 IICϕ cycles 0 1 0: 3 or 4 IICϕ cycles 0 1 1: 5 or 6 IICϕ cycles 1 0 0: 7 or 8 IICϕ cycles 1 0 1: 9 or 10 IICϕ cycles 1 1 0: 11 or 12 IICϕ cycles 1 1 1: 13 or 14 IICϕ cycles	R/W
b7	DLCS	SDA Output Delay Clock Source Selection	0: The internal reference clock (IICϕ) is selected as the clock source of the SDA output delay counter. 1: The internal reference clock divided by 2 (IICϕ/2) is selected as the clock source of the SDA output delay counter.*1	R/W

Note 1. The setting DLCS = 1 (IICϕ/2) only becomes valid when SCL is at the low level. When SCL is at the high level, the setting DLCS = 1 becomes invalid and the clock source becomes the internal reference clock (IICϕ).

TMOS Bit (Timeout Detection Time Selection)

This bit is used to select long mode or short mode for the timeout detection time when the timeout function is enabled (TMOE bit = 1 in ICFER). When this bit is set to 0, long mode is selected. When this bit is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16 bit-counter. In short mode, the counter functions as a 14 bit-counter. While the SCLn line is in the state that enables this counter as specified by bits TMOH and TMOL, the counter counts up in synchronization with the internal reference clock (IICϕ) as a count source.
For details on the timeout function, see section 30.11.1, Timeout Function.

TMOL Bit (Timeout L Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCLn line is held low when the timeout function is enabled (TMOE bit = 1 in ICFER).

TMOH Bit (Timeout H Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCLn line is held high when the timeout function is enabled (TMOE bit = 1 in ICFER).

TMWE Bit (Timeout Internal Counter Write Enable)

This bit is used to allocate the slave address register (SARL0/SARU0) to the address of the timeout internal counter (TMOCNTL/TMOCNTU).

SDDL[2:0] Bits (SDA Output Delay Setup Counter)

The SDA output can be delayed by the SDDL[2:0] setting. This counter works with the clock source selected by the DLCS bit. The setting of this function can be used for all types of SDA output, including the transmission of the acknowledge bit.

For details on this function, see section 30.5, Facility for Delaying SDA Output.

Note: • Set the SDA output delay time to meet the I2C bus standard (within the data enable time/acknowledge enable time*1) or the SMBus standard (within the data hold time: 300 ns or more, and SCL-clock low-level period - the data setup time: 250 ns). Note that, if a value outside the standard is set, communication with communication devices may malfunction or it may seemingly become a start condition or stop condition depending on the bus state.

Note 1. Data enable time/acknowledge enable time
3,450 ns (up to 100 kbps: standard mode [Sm])
900 ns (up to 400 kbps: fast mode [fm])

30.2.5 I2C Bus Mode Register 3 (ICMR3)

Address(es): RIIC0.ICMR3 0008 8304h, RIIC1.ICMR3 0008 8324h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NF[1:0]	Noise Filter Stage Selection	b1 b0 0 0: Noise of up to one IICϕ cycle is filtered out (single-stage filter). 0 1: Noise of up to two IICϕ cycles is filtered out (2-stage filter). 1 0: Noise of up to three IICϕ cycles is filtered out (3-stage filter). 1 1: Noise of up to four IICϕ cycles is filtered out (4-stage filter).	R/W
b2	ACKBR	Receive Acknowledge	0: A 0 is received as the acknowledge bit (ACK reception). 1: A 1 is received as the acknowledge bit (NACK reception).	R
b3	ACKBT	Transmit Acknowledge	0: A 0 is sent as the acknowledge bit (ACK transmission). 1: A 1 is sent as the acknowledge bit (NACK transmission).	R/W*1
b4	ACKWP	ACKBT Write Protect	0: Modification of the ACKBT bit is disabled. 1: Modification of the ACKBT bit is enabled.	W*1
b5	RDRFS	RDRF Flag Set Timing Selection	0: The RDRF flag is set at the rising edge of the ninth SCL clock cycle. (The SCLn line is not held low at the falling edge of the eighth clock cycle.) 1: The RDRF flag is set at the rising edge of the eighth SCL clock cycle. (The SCLn line is held low at the falling edge of the eighth clock cycle.) Low-hold is released by writing a value to the ACKBT bit.	R/W*2
b6	WAIT	WAIT	0: No WAIT (The period between ninth clock cycle and first clock cycle is not held low.) 1: WAIT (The period between ninth clock cycle and first clock cycle is held low.) Low-hold is released by reading ICDRR.	R/W*2
b7	SMBS	SMBus/I2C Bus Selection	0: The I2C bus is selected. 1: The SMBus is selected.	R/W

Note 1. If it is attempted to write 1 to both ACKWP and ACKBT bits, the ACKBT bit cannot be set to 1.
Note 2. The WAIT and RDRFS bits are valid only in receive mode (invalid in transmit mode).

NF[1:0] Bits (Noise Filter Stage Selection)

These bits are used to select the number of stages of the digital noise filter.

For details of digital noise filter function, see section 30.6, Digital Noise-Filter Circuits

Note: • Set the noise range to be filtered out by the noise filter within a range less than the SCLn line high-level period or low-level period. If the noise range is set to a value of (SCL clock width: high-level period or low-level period, whichever is shorter) - [1.5 internal reference clock (IICϕ) cycles + analog noise filter: 120 ns (reference values)] or more, the SCL clock is regarded as noise by the noise filter function of the RIIC, which may prevent the RIIC from operating normally.

ACKBR Bit (Receive Acknowledge)

This bit is used to store the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1

[Clearing conditions]

- When 0 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (RIIC reset)

ACKBT Bit (Transmit Acknowledge)

This bit is used to set the bit to be sent at the acknowledge timing in receive mode.
[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When stop condition issuance is detected (when a stop condition is detected with the SP bit in ICCR2 set to 1)
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (RIIC reset)

Note: • The ACKBT bit must be written to while the ACKWP bit is 1. If the ACKBT bit is written to with the ACKWP bit cleared to 0, writing to the ACKBT bit is disabled.

ACKWP Bit (ACKBT Write Protect)

This bit is used to control the modification of the ACKBT bit.

RDRFS Bit (RDRF Flag Set Timing Selection)

This bit is used to select the RDRF flag set timing in receive mode and also to select whether to hold the SCLn line low at the falling edge of the eighth SCL clock cycle.
When the RDRFS bit is 0, the SCLn line is not held low at the falling edge of the eighth SCL clock cycle, and the RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle.
When the RDRFS bit is 1, the RDRF flag is set to 1 at the rising edge of the eighth SCL clock cycle and the SCLn line is held low at the falling edge of the eighth SCL clock cycle. The low-hold of the SCLn line is released by writing a value to the ACKBT bit.
After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1) according to receive data.

WAIT Bit (WAIT)

This bit is used to control whether to hold the period between the ninth SCL clock cycle and the first SCL clock cycle low until the receive data buffer (ICDRR) is completely read each time single-byte data is received in receive mode.
When the WAIT bit is 0, the receive operation is continued without holding the period between the ninth and the first SCL clock cycle low. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.
When the WAIT bit is 1, the SCLn line is held low from the falling edge of the ninth clock cycle until the ICDRR value is read each time single-byte data is received. This enables receive operation in byte units.

Note: • When the value of the WAIT bit is to be read, be sure to read the ICDRR beforehand.

SMBS Bit (SMBus/I2C Bus Selection)

Setting this bit to 1 selects the SMBus and enables the HOAE bit in ICSER.

30.2.6 I2C Bus Function Enable Register (ICFER)

Address(es): RIIC0.ICFER 0008 8305h, RIIC1.ICFER 0008 8325h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOE	Timeout Function Enable	0: The timeout function is disabled. 1: The timeout function is enabled.	R/W
b1	MALE	Master Arbitration-Lost Detection Enable	0: Master arbitration-lost detection is disabled. (Disables the arbitration-lost detection function and does not clear the MST and TRS bits in ICCR2 automatically when arbitration is lost.) 1: Master arbitration-lost detection is enabled. (Enables the arbitration-lost detection function and clears the MST and TRS bits in ICCR2 automatically when arbitration is lost.)	R/W
b2	NALE	NACK Transmission Arbitration-Lost Detection Enable	0: NACK transmission arbitration-lost detection is disabled. 1: NACK transmission arbitration-lost detection is enabled.	R/W
b3	SALE	Slave Arbitration-Lost Detection Enable	0: Slave arbitration-lost detection is disabled. 1: Slave arbitration-lost detection is enabled.	R/W
b4	NACKE	NACK Reception Transfer Suspension Enable	0: Transfer operation is not suspended during NACK reception (transfer suspension disabled). 1: Transfer operation is suspended during NACK reception (transfer suspension enabled).	R/W
b5	NFE	Digital Noise Filter Circuit Enable	0: No digital noise filter circuit is used. 1: A digital noise filter circuit is used.	R/W
b6	SCLE	SCL Synchronous Circuit Enable	0: No SCL synchronous circuit is used. 1: An SCL synchronous circuit is used.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

TMOE Bit (Timeout Function Enable)

This bit is used to enable or disable the timeout function.

For details on the timeout function, see section 30.11.1, Timeout Function.

MALE Bit (Master Arbitration-Lost Detection Enable)

This bit is used to specify whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE Bit (NACK Transmission Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode (such as when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with different number of receive bytes).

SALE Bit (Slave Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode (such as when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs due to noise).

NACKE Bit (NACK Reception Transfer Suspension Enable)

This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.
When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended.
When the NACKE bit is 0, the next transfer operation is continued regardless of the received acknowledge content.
For details on the NACK reception transfer suspension function, see section 30.8.2, NACK Reception Transfer Suspension Function.

SCLE Bit (SCL Synchronous Circuit Enable)

This bit is used to specify whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.
When the SCLE bit is cleared to 0 (SCL synchronous circuit not used), the RIIC does not synchronize the SCL clock with the SCL input clock. In this setting, the RIIC outputs the SCL clock with the transfer rate set in ICBRH and ICBRL regardless of the SCL line state. For this reason, if the bus load of the I2C bus line is much larger than the specification value or if the SCL clock output overlaps in multiple masters, the short-cycle SCL clock that does not meet the specification may be output. When no SCL synchronous circuit is used, it also affects the issuance of a start condition, restart condition, and stop condition, and the continuous output of extra SCL clock cycles.
This bit must not be cleared to 0 except for checking the output of the transfer rate.

30.2.7 I2C Bus Status Enable Register (ICSER)

Address(es): RIIC0.ICSER 0008 8306h, RIIC1.ICSER 0008 8326h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	SAR0E	Slave Address Register 0 Enable	0: Slave address in SARL0 and SARU0 is disabled. 1: Slave address in SARL0 and SARU0 is enabled.	R/W
b1	SAR1E	Slave Address Register 1 Enable	0: Slave address in SARL1 and SARU1 is disabled. 1: Slave address in SARL1 and SARU1 is enabled.	R/W
b2	SAR2E	Slave Address Register 2 Enable	0: Slave address in SARL2 and SARU2 is disabled. 1: Slave address in SARL2 and SARU2 is enabled.	R/W
b3	GCAE	General Call Address Enable	0: General call address detection is disabled. 1: General call address detection is enabled.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DIDE	Device-ID Address Detection Enable	0: Device-ID address detection is disabled. 1: Device-ID address detection is enabled.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOAE	Host Address Enable	0: Host address detection is disabled. 1: Host address detection is enabled.	R/W

SARyE Bit (Slave Address Register y Enable) (y = 0 to 2)

This bit is used to enable or disable the received slave address and the slave address set in SARLy and SARUy.

When this bit is set to 1, the slave address set in SARLy and SARUy is enabled and is compared with the received slave address.

When this bit is cleared to 0, the slave address set in SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

GCAE Bit (General Call Address Enable)

This bit is used to specify whether to ignore the general call address (0000 000b + 0 [W]: All 0) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the RIIC recognizes the received slave address as the general call address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs data receive operation.

When this bit is cleared to 0, the received slave address is ignored even if it matches the general call address.

DIDE Bit (Device-ID Address Detection Enable)

This bit is used to specify whether to recognize and execute the Device-ID address when a device ID (1111 100b) is received in the first frame after a start condition or restart condition is detected.

When this bit is set to 1, if the received first frame matches the device ID, the RIIC recognizes that the Device-ID address has been received. When the following R/W# bit is 0 [W], the RIIC recognizes the second and the following frames as slave addresses and continues the receive operation.

When this bit is cleared to 0, the RIIC ignores the received first frame even if it matches the device ID address and recognizes the first frame as a normal slave address.

For details on the device-ID address detection, see section 30.7.3, Device-ID Address Detection.

HOAE Bit (Host Address Enable)

This bit is used to specify whether to ignore received host address (0001 000b) when the SMBS bit in ICMR3 is 1. When this bit is set to 1 while the SMBS bit in ICMR3 is 1, if the received slave address matches the host address, the RIIC recognizes the received slave address as the host address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the receive operation.
When the SMBS bit in ICMR3 or the HOAE bit is cleared to 0, the received slave address is ignored even if it matches the host address.

30.2.8 I2C Bus Interrupt Enable Register (ICIER)

Address(es): RIIC0.ICIER 0008 8307h, RIIC1.ICIER 0008 8327h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOIE	Timeout Interrupt Enable	0: Timeout interrupt request (TMOI) is disabled. 1: Timeout interrupt request (TMOI) is enabled.	R/W
b1	ALIE	Arbitration-Lost Interrupt Enable	0: Arbitration-lost interrupt request (ALI) is disabled. 1: Arbitration-lost interrupt request (ALI) is enabled.	R/W
b2	STIE	Start Condition Detection Interrupt Enable	0: Start condition detection interrupt request (STI) is disabled. 1: Start condition detection interrupt request (STI) is enabled.	R/W
b3	SPIE	Stop Condition Detection Interrupt Enable	0: Stop condition detection interrupt request (SPI) is disabled. 1: Stop condition detection interrupt request (SPI) is enabled.	R/W
b4	NAKIE	NACK Reception Interrupt Enable	0: NACK reception interrupt request (NAKI) is disabled. 1: NACK reception interrupt request (NAKI) is enabled.	R/W
b5	RIE	Receive Data Full Interrupt Enable	0: Receive data full interrupt request (ICRXI) is disabled. 1: Receive data full interrupt request (ICRXI) is enabled.	R/W
b6	TEIE	Transmit End Interrupt Enable	0: Transmit end interrupt request (ICTEI) is disabled. 1: Transmit end interrupt request (ICTEI) is enabled.	R/W
b7	TIE	Transmit Data Empty Interrupt Enable	0: Transmit data empty interrupt request (ICTXI) is disabled. 1: Transmit data empty interrupt request (ICTXI) is enabled.	R/W

TMOIE Bit (Timeout Interrupt Enable)

This bit is used to enable or disable timeout interrupt requests (TMOI) when the TMOF flag in ICSR2 is set to 1. A TMOI interrupt request is canceled by clearing the TMOF flag or the TMOIE bit to 0.

ALIE Bit (Arbitration-Lost Interrupt Enable)

This bit is used to enable or disable arbitration-lost interrupt requests (ALI) when the AL flag in ICSR2 is set to 1. An ALI interrupt request is canceled by clearing the AL flag or the ALIE bit to 0.

STIE Bit (Start Condition Detection Interrupt Enable)

This bit is used to enable or disable start condition detection interrupt requests (STI) when the START flag in ICSR2 is set to 1. An STI interrupt request is canceled by clearing the START flag or the STIE bit to 0.

SPIE Bit (Stop Condition Detection Interrupt Enable)

This bit is used to enable or disable stop condition detection interrupt requests (SPI) when the STOP flag in ICSR2 is set to 1. An SPI interrupt request is canceled by clearing the STOP flag or the SPIE bit to 0.

NAKIE Bit (NACK Reception Interrupt Enable)

This bit is used to enable or disable NACK reception interrupt requests (NAKI) when the NACKF flag in ICSR2 is set to 1. An NAKI interrupt request is canceled by clearing the NACKF flag or the NAKIE bit to 0.

RIE Bit (Receive Data Full Interrupt Enable)

This bit is used to enable or disable receive data full interrupt requests (ICRXI) when the RDRF flag in ICSR2 is set to 1.

TEIE Bit (Transmit End Interrupt Enable)

This bit is used to enable or disable transmit end interrupts (ICTEI) when the TEND flag in ICSR2 is set to 1. An ICTEI interrupt request is canceled by clearing the TEND flag or the TEIE bit to 0.

TIE Bit (Transmit Data Empty Interrupt Enable)

This bit is used to enable or disable transmit data empty interrupts (ICTXI) when the TDRE flag in ICSR2 is set to 1.

30.2.9 I2C Bus Status Register 1 (ICSR1)

Address(es): RIIC0.ICSR1 0008 8308h, RIIC1.ICSR1 0008 8328h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	AAS0	Slave Address 0 Detection Flag	0: Slave address 0 is not detected. 1: Slave address 0 is detected. • This bit is set to 1 when the received slave address matches the SVA[6:0] value in SARL0 while the FS bit in SARU0 is 0 (7-bit address format selected). • This bit is set to 1 when the received slave address matches a value of (11110b + SVA[1:0] in SARU0) and the following address matches the SARL0 value while the FS bit in SARU0 is 1 (10-bit address format selected). (This bit is set at the rising edge of the ninth SCL clock cycle in the SARL0 match determination frame.)	R(/W) *1
b1	AAS1	Slave Address 1 Detection Flag	0: Slave address 1 is not detected. 1: Slave address 1 is detected. • This bit is set to 1 when the received slave address matches the SVA[6:0] value in SARL1 while the FS bit in SARU1 is 0 (7-bit address format selected). • This bit is set to 1 when the received slave address matches a value of (11110b + SVA[1:0] in SARU1) and the following address matches the SARL1 value while the FS bit in SARU1 is 1 (10-bit address format selected). (This bit is set at the rising edge of the ninth SCL clock cycle in the SARL1 match determination frame.)	R(/W) *1
b2	AAS2	Slave Address 2 Detection Flag	0: Slave address 2 is not detected. 1: Slave address 2 is detected. • This bit is set to 1 when the received slave address matches the SVA[6:0] value in SARL2 while the FS bit in SARU2 is 0 (7-bit address format selected). • This bit is set to 1 when the received slave address matches a value of (11110b + SVA[1:0] in SARU2) and the following address matches the SARL2 value while the FS bit in SARU2 is 1 (10-bit address format selected). (This bit is set at the rising edge of the ninth SCL clock cycle in the SARL2 match determination frame.)	R(/W) *1

Bit	Symbol	Bit Name	Description	R/W
b3	GCA	General Call Address Detection Flag	0: General call address is not detected. 1: General call address is detected. • This bit is set to 1 when the received slave address matches the general call address (all 0).	R(/W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DID	Device-ID Address Detection Flag	0: Device-ID command is not detected. 1: Device-ID command is detected. • This bit is set to 1 when the first frame received immediately after a start condition is detected matches a value of (device ID (1111 100b) + 0[W]).	R(/W) *1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOA	Host Address Detection Flag	0: Host address is not detected. 1: Host address is detected. • This bit is set to 1 when the received slave address matches the host address (0001 000b).	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

AASy Flag (Slave Address y Detection) (y = 0 to 2)

[Setting conditions]

<For 7-bit address format: SARUy.FS = 0>

- When the received slave address matches the SVA[6:0] value in SARLy with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

<For 10-bit address format: SARUy.FS = 1>

- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy) and the following address matches the SARLy value with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the AASy bit after reading AASy = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

<For 7-bit address format: SARUy.FS = 0>

- When the received slave address does not match the SVA[6:0] value in SARLy with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is cleared to 0 at the rising edge of the ninth SCL clock cycle in the frame.

<For 10-bit address format: SARUy.FS = 1>

- When the received slave address does not match a value of (11110b + SVA[1:0] in SARUy) with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is cleared to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy) and the following address does not match the SARLy value with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is cleared to 0 at the rising edge of the ninth SCL clock cycle in the frame.

GCA Flag (General Call Address Detection)

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]) with the GCAE bit in ICSER set to 1 (general call address detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the GCA bit after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]) with the GCAE bit in ICSER set to 1 (general call address detection enabled)
  This flag is cleared to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

DID Flag (Device-ID Address Detection)

[Setting condition]

- When the first frame received immediately after a start condition or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]) with the DIDE bit in ICSER set to 1 (Device-ID address detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the DID bit after reading DID = 1
- When a stop condition is detected
- When the first frame received immediately after a start condition or restart condition is detected does not match a value of (device ID (1111 100b)) with the DIDE bit in ICSER set to 1 (Device-ID address detection enabled)
  This flag is cleared to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When the first frame received immediately after a start condition or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]) and the second frame does not match any of slave addresses 0 to 2 with the DIDE bit in ICSER set to 1 (Device-ID address detection enabled)
  This flag is cleared to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

HOA Flag (Host Address Detection)

[Setting condition]

- When the received slave address matches the host address (0001 000b) with the HOAE bit in ICSER set to 1 (host address detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the HOA bit after reading HOA = 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b) with the HOAE bit in ICSER set to 1 (host address detection enabled)
  This flag is cleared to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

30.2.10 I2C Bus Status Register 2 (ICSR2)

Address(es): RIIC0.ICSR2 0008 8309h, RIIC1.ICSR2 0008 8329h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOF	Timeout Detection Flag	0: Timeout is not detected. 1: Timeout is detected.	R(/W) *1
b1	AL	Arbitration-Lost Flag	0: Arbitration is not lost. 1: Arbitration is lost.	R(/W) *1
b2	START	Start Condition Detection Flag	0: Start condition is not detected. 1: Start condition is detected.	R(/W) *1
b3	STOP	Stop Condition Detection Flag	0: Stop condition is not detected. 1: Stop condition is detected.	R(/W) *1
b4	NACKF	NACK Detection Flag	0: NACK is not detected. 1: NACK is detected.	R(/W) *1
b5	RDRF	Receive Data Full Flag	0: ICDRR contains no receive data. 1: ICDRR contains receive data.	R(/W) *1
b6	TEND	Transmit End Flag	0: Data is being transmitted. 1: Data has been transmitted.	R(/W) *1
b7	TDRE	Transmit Data Empty Flag	0: ICDRT contains transmit data. 1: ICDRT contains no transmit data.	R

Note 1. Only 0 can be written to clear the flag.

TMOF Flag (Timeout Detection)

This flag is set to 1 when the RIIC recognizes timeout after the SCLn line state remains unchanged for a certain period.
[Setting condition]

- When the SCLn line state remains unchanged for the period specified by bits TMOH, TMOL, and TMOS in ICMR2 with the TMOE bit in ICFER set to 1 (timeout detection enabled) in master mode or in the slave specification state.

[Clearing conditions]

- When 0 is written to the TMOF bit after reading TMOF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

AL Flag (Arbitration-Lost)

This flag shows that bus mastership has been lost (loss in arbitration) due to a bus conflict or some other reason when a start condition is issued or an address and data are transmitted. The RIIC monitors the level on the SDAn line during transmission and, if the level on the line does not match the value of the bit being output, sets the value of the AL bit to 1 to indicate that the bus is occupied by another device.
The RIIC can also set the flag to indicate the detection of loss of arbitration during NACK transmission in master mode or during data transmission in slave mode.

[Setting conditions]

<When master arbitration-lost detection is enabled: ICFER.MALE = 1>

- When the internal SDA output state does not match the SDAn line level at the rising edge of SCL clock except for the ACK period during data (including slave address) transmission in master transmit mode (when the SDAn line is driven low while the internal SDA output is at a high level (the SDAn pin is in the high-impedance state))
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition issuance request) or the internal SDA output state does not match the SDAn line level
- When the ST bit in ICCR2 is set to 1 (start condition issuance request) with the BBSY flag in ICCR2 set to 1.

<When NACK arbitration-lost detection is enabled: ICFER.NALE = 1>

- When the internal SDA output state does not match the SDAn line level at the rising edge of SCL clock in the ACK period during NACK transmission in receive mode

<When slave arbitration-lost detection is enabled: ICFER.SALE = 1>

- When the internal SDA output state does not match the SDAn line level at the rising edge of SCL clock except for the ACK period during data transmission in slave transmit mode

[Clearing conditions]

- When 0 is written to the AL bit after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Table 30.4 Relationship between Arbitration-Lost Generation Sources and Arbitration-Lost Enable Functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-Lost Generation Source
1	×	×	1	Start condition issuance error	When internal SDA output state does not match SDAn line level when a start condition is detected while the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 with BBSY in ICCR2 set to 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmit mode
×	1	×	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master receive mode or slave receive mode
×	×	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

×: Don't care

START Flag (Start Condition Detection)

[Setting condition]

- When a start condition (or a restart condition) is detected

[Clearing conditions]

- When 0 is written to the START bit after reading START = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

STOP Flag (Stop Condition Detection)

[Setting condition]

- When a stop condition is detected

[Clearing conditions]

- When 0 is written to the STOP bit after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

NACKF Flag (NACK Detection)

[Setting condition]

- When acknowledge is not received (NACK is received) from the receive device in transmit mode with the NACKE bit in ICFER set to 1 (transfer suspension enabled)

[Clearing conditions]

- When 0 is written to the NACKF bit after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: • When the NACKF flag is set to 1, the RIIC suspends data transmission/reception. Writing to ICDRT in transmit mode or reading from ICDRR in receive mode with the NACKF flag set to 1 does not enable data transmit/receive operation. To restart data transmission/reception, clear the NACKF flag to 0.

RDRF Flag (Receive Data Full)

[Setting conditions]

- When receive data has been transferred from ICDRS to ICDRR
  This flag is set to 1 at the rising edge of the eighth or ninth SCL clock cycle (selected by the RDRFS bit in ICMR3)
- When the received slave address matches after a start condition (or a restart condition) is detected with the TRS bit in ICCR2 cleared to 0

[Clearing conditions]

- When 0 is written to the RDRF bit after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

TEND Flag (Transmit End)

[Setting condition]

- At the rising edge of the ninth SCL clock cycle while the TDRE flag is 1

[Clearing conditions]

- When 0 is written to the TEND bit after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

TDRE Flag (Transmit Data Empty)

[Setting conditions]

- When data has been transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1
- When the received slave address matches while the TRS bit is 1

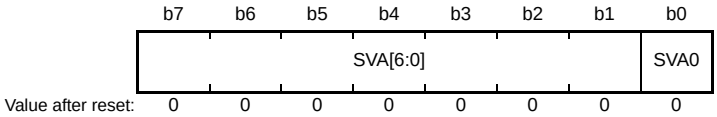
[Clearing conditions]

- When data is written to ICDRT
- When the TRS bit in ICCR2 is cleared to 0
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: • When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the RIIC suspends data transmission/reception. Here, if the TDRE flag is 0 (next transmit data has been written), data is transferred to the ICDRS register and the ICDRT register becomes empty at the rising edge of the ninth clock cycle, but the TDRE flag is not set to 1.

30.2.11 Slave Address Register Ly (SARLy) (y = 0 to 2)

Address(es): RIIC0.SARL0 0008 830Ah, RIIC1.SARL0 0008 832Ah, RIIC0.SARL1 0008 830Ch, RIIC1.SARL1 0008 832Ch, RIIC0.SARL2 0008 830Eh, RIIC1.SARL2 0008 832Eh



Bit	Symbol	Bit Name	Description	R/W
b0	SVA0	10-Bit Address LSB	The least significant bit (LSB) of a 10-bit slave address is set. • When the FS bit in SARUy is 0 (7-bit address format), this bit is invalid. • When the FS bit in SARUy is 1 (10-bit address format), this bit is the LSB of the lower 8-bit address (combined with the SVA[6:0] bits) of a 10-bit slave address.	R/W
b7 to b1	SVA[6:0]	7-Bit Address/10-Bit Address Lower Bits	A slave address is set. • When the FS bit in SARUy is 0 (7-bit address format), these bits form a 7-bit slave address. • When the FS bit in SARUy is 1 (10-bit address format), these bits form the lower 8-bit address (combined with the SVA0 bit) of a 10-bit slave address.	R/W

SVA0 Bit (10-Bit Address LSB)

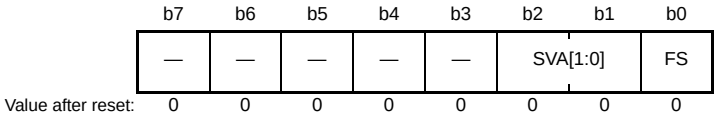
When the 10-bit address format is selected (SARUy.FS = 1), this bit functions as the LSB of a 10-bit address and forms the lower eight bits of a 10-bit address in combination with the SVA[6:0] bits.
When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, this bit is valid. While the SARUy.FS bit or SARyE bit is 0, the setting of this bit is ignored.

SVA[6:0] Bits (7-Bit Address/10-Bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS = 0), these bits function as a 7-bit address. When the 10-bit address format is selected (SARUy.FS = 1), these bits function as the lower eight bits of a 10-bit address in combination with the SVA0 bit.
While the SARyE bit in ICSER is 0, the setting of these bits is ignored.

30.2.12 Slave Address Register Uy (SARUy) (y = 0 to 2)

Address(es): RIIC0.SARU0 0008 830Bh, RIIC1.SARU0 0008 832Bh, RIIC0.SARU1 0008 830Dh, RIIC1.SARU1 0008 832Dh, RIIC0.SARU2 0008 830Fh, RIIC1.SARU2 0008 832Fh



Bit	Symbol	Bit Name	Description	R/W
b0	FS	7-Bit/10-Bit Address Format Selection	0: The 7-bit address format is selected. 1: The 10-bit address format is selected.	R/W
b2, b1	SVA[1:0]	10-Bit Address Upper Bits	A slave address is set. • When the SARUy.FS bit is 0 (7-bit address format), these bits are invalid. • When the SARUy.FS bit is 1 (10-bit address format), these bits form the upper two bits of a 10-bit slave address.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FS Bit (7-Bit/10-Bit Address Format Selection)

This bit is used to select 7-bit address or 10-bit address for slave address y (in SARLy and SARUy).

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in SARLy is valid, and the settings of the SVA[1:0] bits and the SVA0 bit in SARLy are ignored.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the settings of the SVA[1:0] bits and SARLy are valid.

While the SARyE bit in ICSER is 0 (SARLy and SARUy disabled), the setting of the SARUy.FS bit is invalid.

SVA[1:0] Bits (10-Bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), these bits function as the upper two bits of a 10-bit address.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, these bits are valid.

While the SARUy.FS bit or SARyE bit is 0, the setting of these bits is ignored.

30.2.13 I2C Bus Bit Rate Low-Level Register (ICBRL)

Address(es): RIIC0.ICBRL 0008 8310h, RIIC1.ICBRL 0008 8330h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	BRL[4:0]	Bit Rate Low-Level Period	Low-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

The ICBRL register is a 5-bit register that is used to set the width at low level for the SCL clock.
It also works to generate the data setup time for automatic SCL low-hold operation (see section 30.8, Automatically Low-Hold Function for SCL); when the RIIC is used only in slave mode, this register needs to be set to a value longer than the data setup time*1.
ICBRL counts the low-level period with the internal reference clock source (IICϕ) specified by the CKS[2:0] bits in ICMR1.
When the digital noise filter circuit is enabled (ICFER.NFE = 1), set the value of <the number of noise filter steps + 1> or above to the ICBRL register. For the number of noise filter steps, refer to the ICMR3.NF[1:0] bits.

Note 1. Data setup time (t_{SU}: DATA)
250 ns (up to 100 kbps: standard mode [Sm])
100 ns (up to 400 kbps: fast mode [fm])

30.2.14 I2C Bus Bit Rate High-Level Register (ICBRH)

Address(es): RIIC0.ICBRH 0008 8311h, RIIC1.ICBRH 0008 8331h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	BRH[4:0]	Bit Rate High-Level Period	High-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRH is a 5-bit register to set the high-level period of SCL clock. ICBRH is valid in master mode. If the RIIC is used only in slave mode, this register need not to set the high-level period.
ICBRH counts the high-level period with the internal reference clock source (IICϕ) specified by the CKS[2:0] bits in ICMR1.
When the digital noise filter circuit is enabled (ICFER.NFE = 1), set the value of <the number of noise filter steps + 1> or above to the ICBRL register. For the number of noise filter steps, refer to the ICMR3.NF[1:0] bits.

The I2C transfer rate and the SCL clock duty are calculated using the following expression.
Transfer rate = 1 / {[(ICBRH + 1) + (ICBRL + 1)] / IICϕ*1 + SCLn line rising time [tr] + SCLn line falling time [tf]}
Duty cycle = {SCLn line rising time [tr]*2 + (ICBRH + 1) / IICϕ} / {SCLn line falling time [tf]*2 + (ICBRL + 1) / IICϕ}

Note 1. IICϕ = PCLK × Division ratio
Note 2. The SCLn line rising time [tr] and SCLn line falling time [tf] depend on the total bus line capacitance [Cb] and the pull-up resistor [Rp]. For details, see the I2C bus standard from NXP Semiconductors.

Table 30.5 lists examples of ICBRH/ICBRL settings.

Table 30.5 Examples of ICBRH/ICBRL Settings for Transfer Rate (1)

Transfer Rate (kbps)	Operating Frequency PCLK (MHz)								
	8			10			12.5		
	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL
10	100b	22 (F6h)	25 (F9h)	101b	13 (EDh)	15 (EFh)	101b	16 (F0h)	20 (F4h)
50	010b	16 (F0h)	19 (F3h)	010b	21 (F5h)	24 (F8h)	011b	12 (ECh)	15 (EFh)
100	001b	15 (EFh)	18 (F2h)	001b	19 (F3h)	23 (F7h)	001b	24 (F8h)	29 (FDh)
400	000b	4 (E4h)	10 (EAh)	000b	5 (E5h)	12 (ECh)	000b	7 (E7h)	16 (F0h)

Table 30.5 Examples of ICBRH/ICBRL Settings for Transfer Rate (2)

Transfer Rate (kbps)	Operating Frequency PCLK (MHz)								
	16			20			25		
	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL
10	101b	22 (F6h)	25 (F9h)	110b	13 (EDh)	15 (EFh)	110b	16 (F0h)	20 (F4h)
50	011b	16 (F0h)	19 (F3h)	011b	21 (F5h)	24 (F8h)	100b	12 (ECh)	15 (EFh)
100	010b	15 (EFh)	18 (F2h)	010b	19 (F3h)	23 (F7h)	010b	24 (F8h)	29 (FDh)
400	000b	9 (E9h)	20 (F4h)	000b	11 (EBh)	25 (F9h)	001b	7 (E7h)	16 (F0h)

Table 30.5 Examples of ICBRH/ICBRL Settings for Transfer Rate (3)

Transfer Rate (kbps)	Operating Frequency PCLK (MHz)								
	30			33			50		
	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL
10	110b	20 (F4h)	24 (F8h)	110b	22 (F6h)	26 (FAh)	111b	16 (F0h)	20 (F4h)
50	100b	15 (EFh)	18 (F2h)	100b	17 (F1h)	20 (F4h)	100b	26 (FAh)	31 (FFh)
100	010b	2 (E2h)	3 (E3h)	011b	16 (F0h)	19 (F3h)	011b	24 (F8h)	29 (FDh)
400	001b	8 (E8h)	19 (F3h)	001b	9 (E9h)	21 (F5h)	010b	7 (E7h)	16 (F0h)

Note: • SCLn line rising time (tr): 100 kbps or less, [Sm]: 1000 ns, 400 kbps or less, [Fm]: 300 ns: 120 ns
SCLn line falling time (tf): 400 kbps or less, [Sm/Fm]: 300 ns: 120 ns
For the specified values of SCLn line rising time (tr) and SCLn line falling time (tf), see the I2C bus standard from NXP Semiconductors.

30.2.15 I2C Bus Transmit Data Register (ICDRT)

Address(es): RIIC0.ICDRT 0008 8312h, RIIC1.ICDRT 0008 8332h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

When ICDRT detects a space in the I2C bus shift register (ICDRS), it transfers the transmit data that has been written to ICDRT to ICDRS and starts transmitting data in transmit mode.
The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data has been written to ICDRT while the ICDRS data is being transmitted.
ICDRT can always be read and written. Write transmit data to ICDRT once when a transmit data empty interrupt (ICTXI) request is generated.

30.2.16 I2C Bus Receive Data Register (ICDRR)

Address(es): RIIC0.ICDRR 0008 8313h, RIIC1.ICDRR 0008 8333h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data has been received, the received data is transferred from the I2C bus shift register (ICDRS) to ICDRR to enable the next data to be received.
The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data has been read from ICDRR while ICDRS is receiving data.
ICDRR cannot be written. Read data from ICDRR once when a receive data full interrupt (ICRXI) request is generated.
If ICDRR receives the next receive data before the current data is read from ICDRR (while the RDRF flag in ICSR2 is 1), the RIIC automatically holds the SCLn clock low one cycle before the RDRF flag is set to 1 next.

30.2.17 I2C Bus Shift Register (ICDRS)

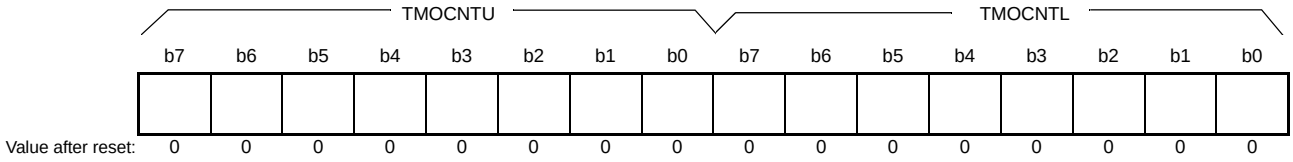
	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—

ICDRS is an 8-bit shift register to transmit and receive data.
During transmission, transmit data is transferred from ICDRT to ICDRS and is sent from the SDAn pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data has been received.
ICDRS cannot be accessed directly.

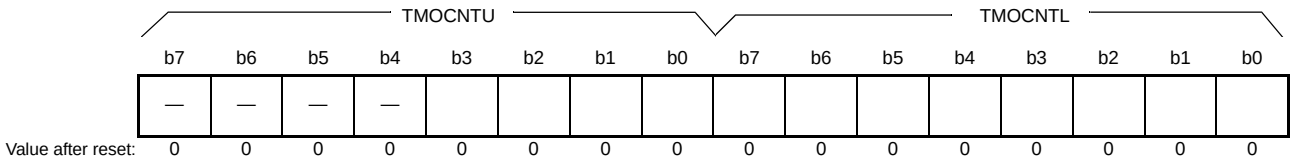
30.2.18 Timeout Internal Counter (TMOCNT)

Address (es): RIIC0.TMOCNTL 0008 830Ah, RIIC1.TMOCNTL 0008 832Ah*1
RIIC0.TMOCNTU 0008 830Bh, RIIC1.TMOCNTU 0008 832Bh*1

- ICMR2.TMOS = 0 (Long mode)



- ICMR2.TMOS = 1 (Short mode)



Note 1. Note that these registers have the same addresses as the SARLn and SARUn registers.

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMOCNTL	Timeout Internal Counter L	Timeout internal counter low-order byte	W*1

Note 1. The value in the internal timeout counter is not readable. If reading is attempted, the value read is FFFFh.

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMOCNTU	Timeout Internal Counter U	Timeout internal counter high-order byte*1	W*2

Note 1. With TMOS = 1 (short mode), b7 to b4 are reserved. They are writable but writing does not affect their values.
Note 2. The value in the internal timeout counter is not readable. If reading is attempted, the value read is FFFFh.

The timeout internal counter (TMOCNTL/TMOCNTU) is initialized (00h) after a reset if ICCR1.IICRST=1 or ICFER.TMOE=1 and PCLK/1 is selected while the setting of ICMR1.CKS[2:0] is 000b, and the counter-clearing condition specified by TMOH/TMOL of ICMR2 (SCL rising edge/falling edge detection) is satisfied. The initialization does not automatically take place other than ICMR1.CKS[2:0] = 000b (PCLK/1). Write 00h to TMOCNTL/TMOCNTU counter as necessary.
The TMOCNTL and TMOCNTU registers are also accessible in combination as a 16-bit register through 16-bit access. The arrangement of the registers when 16-bit access is used is listed in Table 30.6, Allocation of Registers for 16-bit Access.

Table 30.6 Allocation of Registers for 16-bit Access

Address	Eight Higher-Order Bits	Eight Lower-Order Bits
0008 830Ah	RIIC0.TMOCNTU	RIIC0.TMOCNTL
0008 832Ah	RIIC1.TMOCNTU	RIIC1.TMOCNTL

30.3 Operation

30.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start condition or restart condition is an address frame used to specify a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.
Figure 30.3 shows the I2C bus format, and Figure 30.4 shows the I2C bus timing.

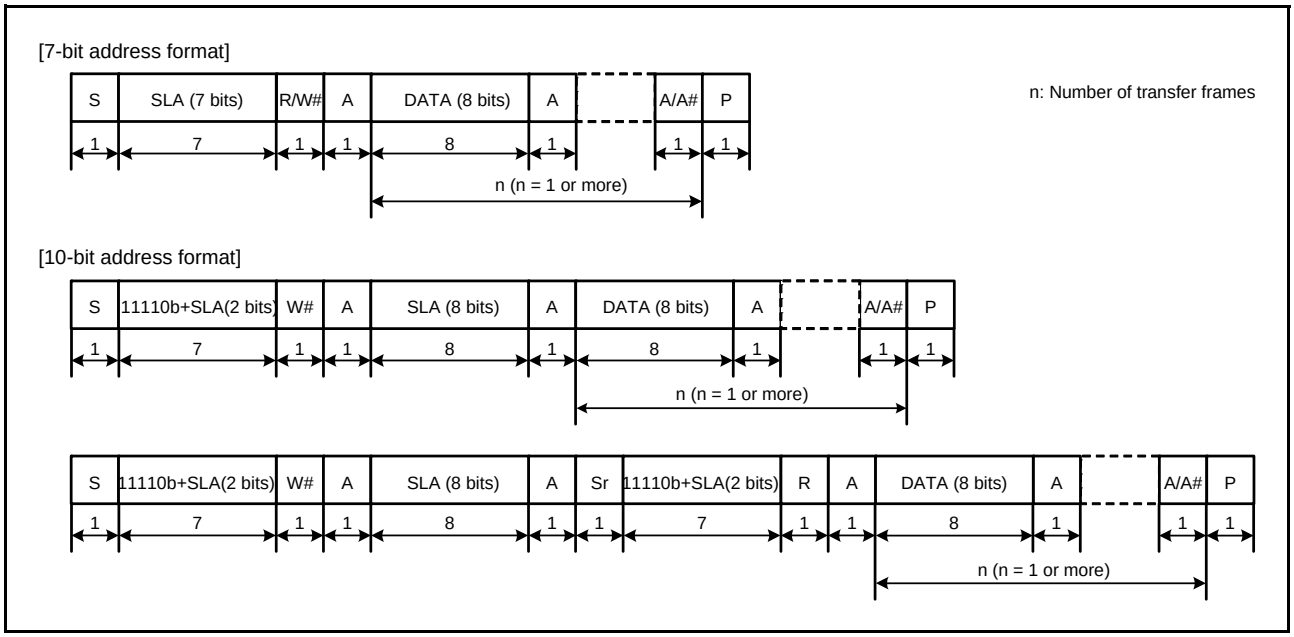


Figure 30.3 I2C Bus Format

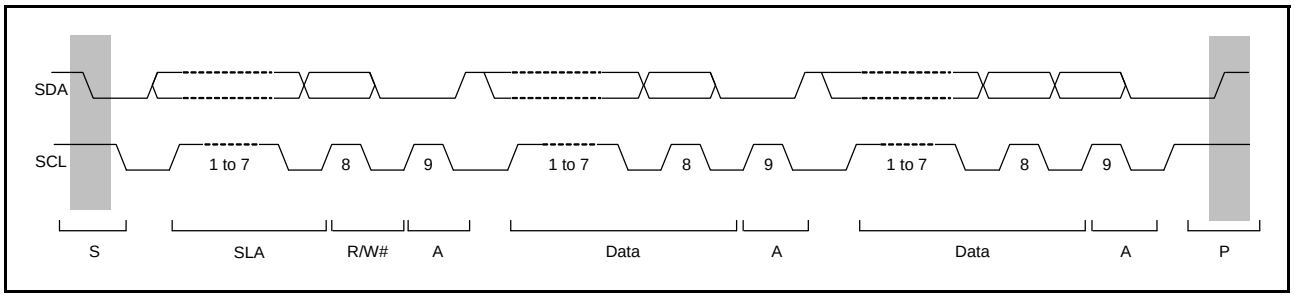


Figure 30.4 I2C Bus Timing (SLA = 7 Bits)

S: Start condition. The master device drives the SDAn line low from high level while the SCLn line is at a high level.

SLA: Slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W is 1, or from the master device to the slave device when R/W is 0.

A: Acknowledge. The receive device drives the SDAn line low. (In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.)

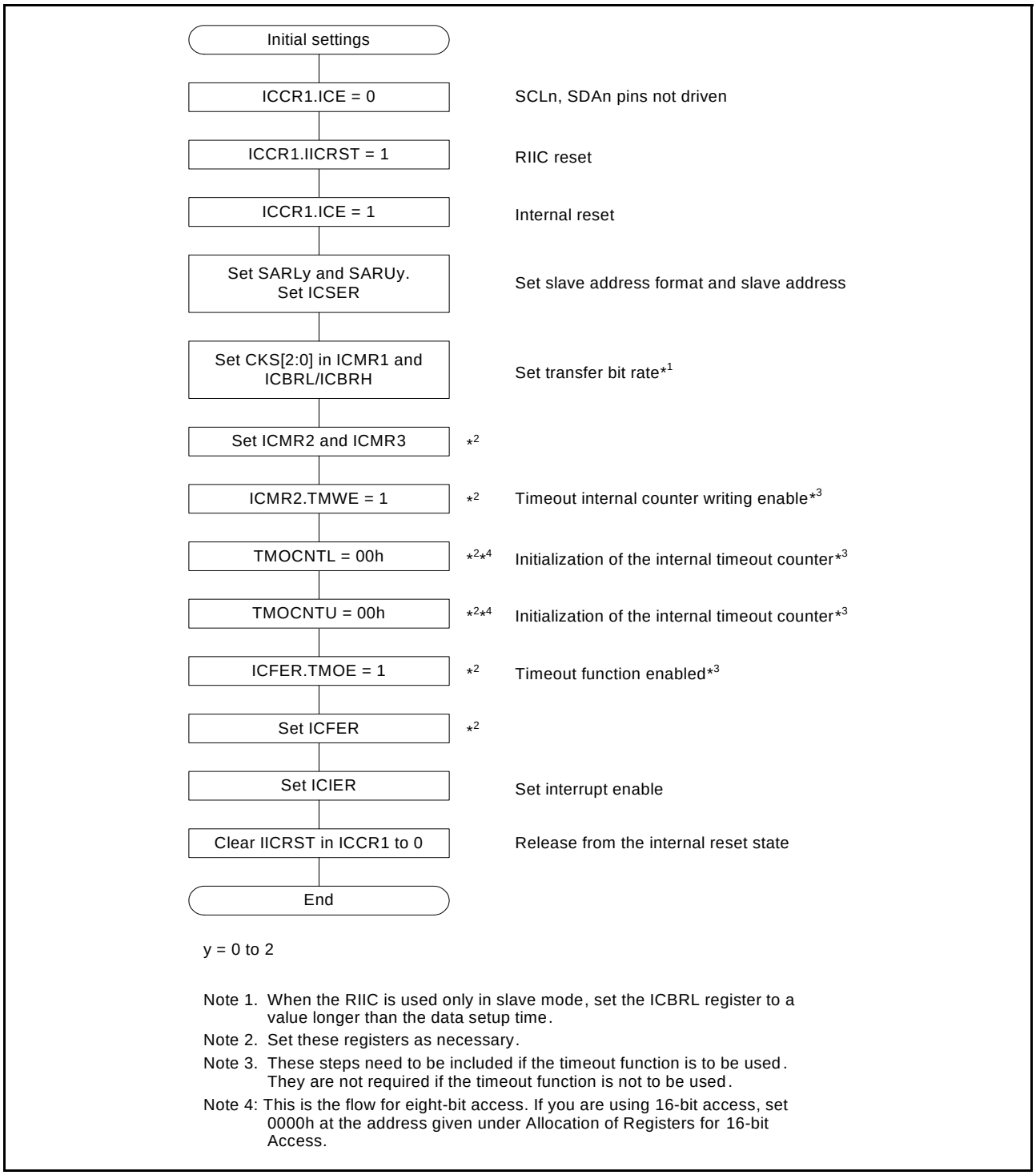
Sr: Restart condition. The master device drives the SDAn line low from the high level after the setup time has elapsed with the SCLn line at the high level.

DATA: Transmitted or received data

P: Stop condition. The master device drives the SDAn line high from low level while the SCLn line is at a high level.

30.3.2 Initial Settings

Before starting data transmission and reception, initialize the RIIC according to the procedure in Figure 30.5.
Set the IICRST bit in ICCR1 to 1 (RIIC reset) with the ICE bit in ICCR1 cleared to 0 (SCLn and SDAn pins not driven) and then set the ICE bit in ICCR1 to 1 (internal reset). This initializes the internal state and the various flags of ICSR1. After that, set registers SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL (y = 0 to 2), and set the other registers as necessary (for initial settings of the RIIC, see section 30.5, Facility for Delaying SDA Output). When the necessary register settings have been completed, set the ICCR1.IICRST bit to 0 (for release from the reset state). This step is not necessary if initialization of the RIIC has already been completed.



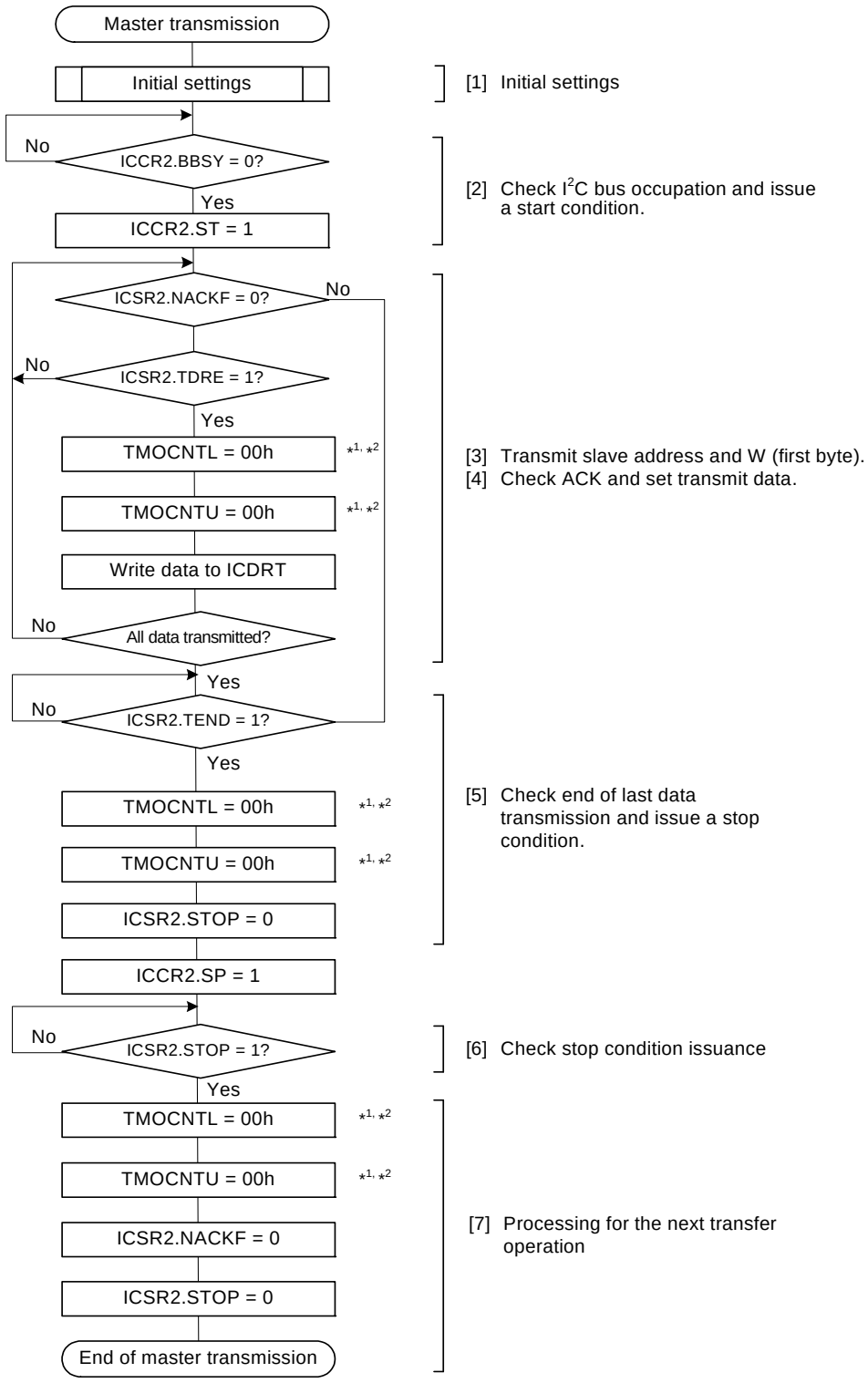
Note 1. When the RIIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.
Note 2. Set these registers as necessary.
Note 3. These steps need to be included if the timeout function is to be used. They are not required if the timeout function is not to be used.
Note 4: This is the flow for eight-bit access. If you are using 16-bit access, set 0000h at the address given under Allocation of Registers for 16-bit Access.

Figure 30.5 Example of RIIC Initialization Flowchart

30.3.3 Master Transmit Operation

In master transmit operation, the RIIC outputs the SCL (clock) and transmitted data signals as the master device, and the slave device returns acknowledgements. Figure 30.6 shows an example of usage of master transmission and Figure 30.7 to Figure 30.9 show the timing of operations in master transmission.
The following describes the procedure and operations for master transmission.

(1) Perform initial setting as described in section 30.3.2, Initial Settings.
(2) Read the BBSY flag in ICCR2 to check that the bus is open, and then set the ST bit in ICCR2 to 1 (start condition issuance request). Upon receiving the request, the RIIC issues a start condition. At the same time, the BBSY flag and the START flag in ICSR2 are automatically set to 1 and the ST bit is automatically cleared to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line have matched while the ST bit is 1, the RIIC recognizes that issuing of the start condition as requested by the ST bit has been successfully completed, and the MST and TRS bits in ICCR2 are automatically set to 1, placing the RIIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to setting of the TRS bit to 1.
(3) Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. Once the data for transmission are written to ICDRT, the TDRE flag is automatically cleared to 0, the data are transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the RIIC continues in master transmit mode.
Since the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For data transmission with an address in the 10-bit format, start by writing 1111 0b, the two higher-order bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the eight lower-order bits of the slave address to ICDRT.
(4) After confirming that the TDRE flag in ICSR2 is 1, write the data for transmission to the ICDRT register. The RIIC automatically holds the SCLn line low until the data for transmission are ready or a stop condition is issued.
(5) After all bytes of data for transmission have been written to the ICDRT register, wait until the value of the TEND flag in ICSR2 returns to 1, and then set the SP bit in ICCR2 to 1 (stop condition issuance request). Upon receiving a stop condition issuance request, the RIIC issues the stop condition.
(6) Upon detecting the stop condition, the RIIC automatically clears the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Furthermore, it automatically clears the TDRE and TEND flags to 0, and sets the STOP flag in ICSR2 to 1.
(7) After checking that the ICSR2.STOP flag is 1, clear the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.



Note 1. Timeout internal counter clearing
These steps need to be included if the timeout function is to be used.
They are not required if the timeout function is not to be used.

Note 2: This is the flow for eight-bit access. If you are using 16-bit access, set 0000h at the address given under Allocation of Registers for 16-bit Access.

Figure 30.6 Example of Master Transmission Flowchart

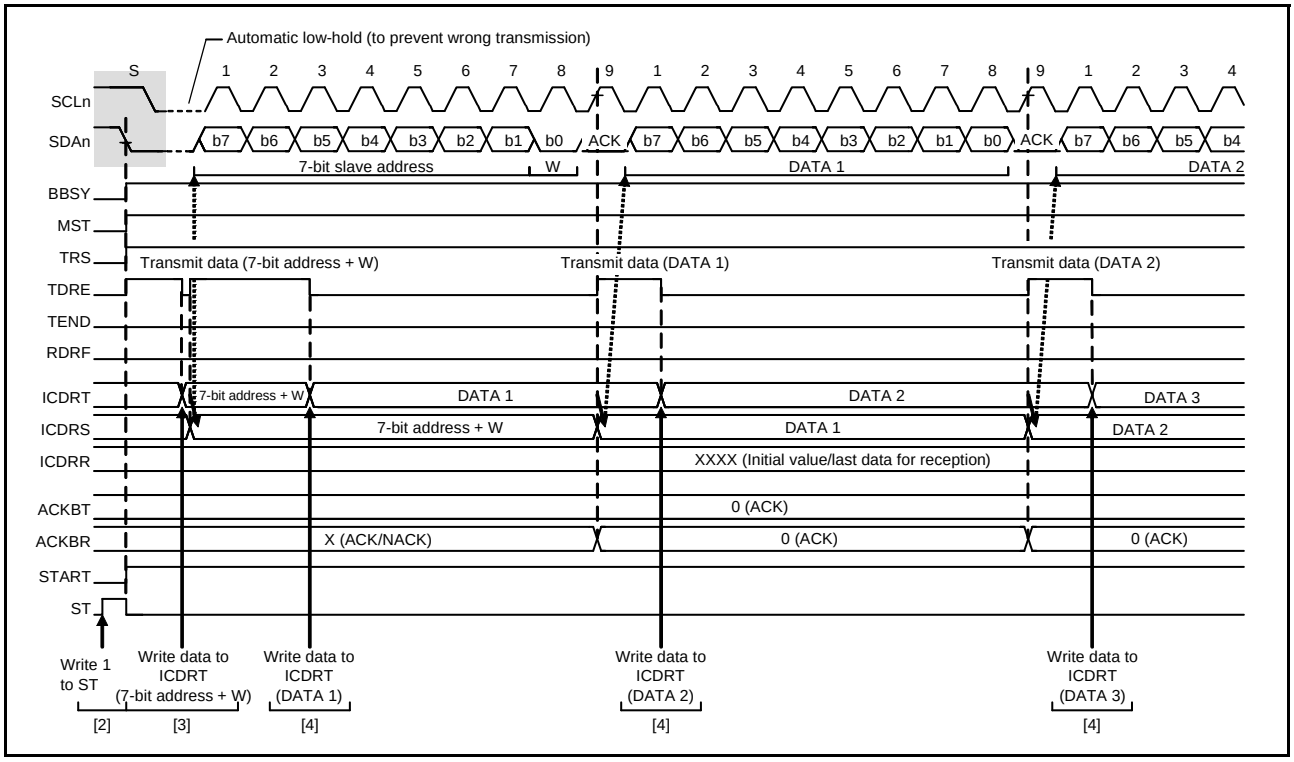


Figure 30.7 Master Transmit Operation Timing (1) (7-Bit Address Format)

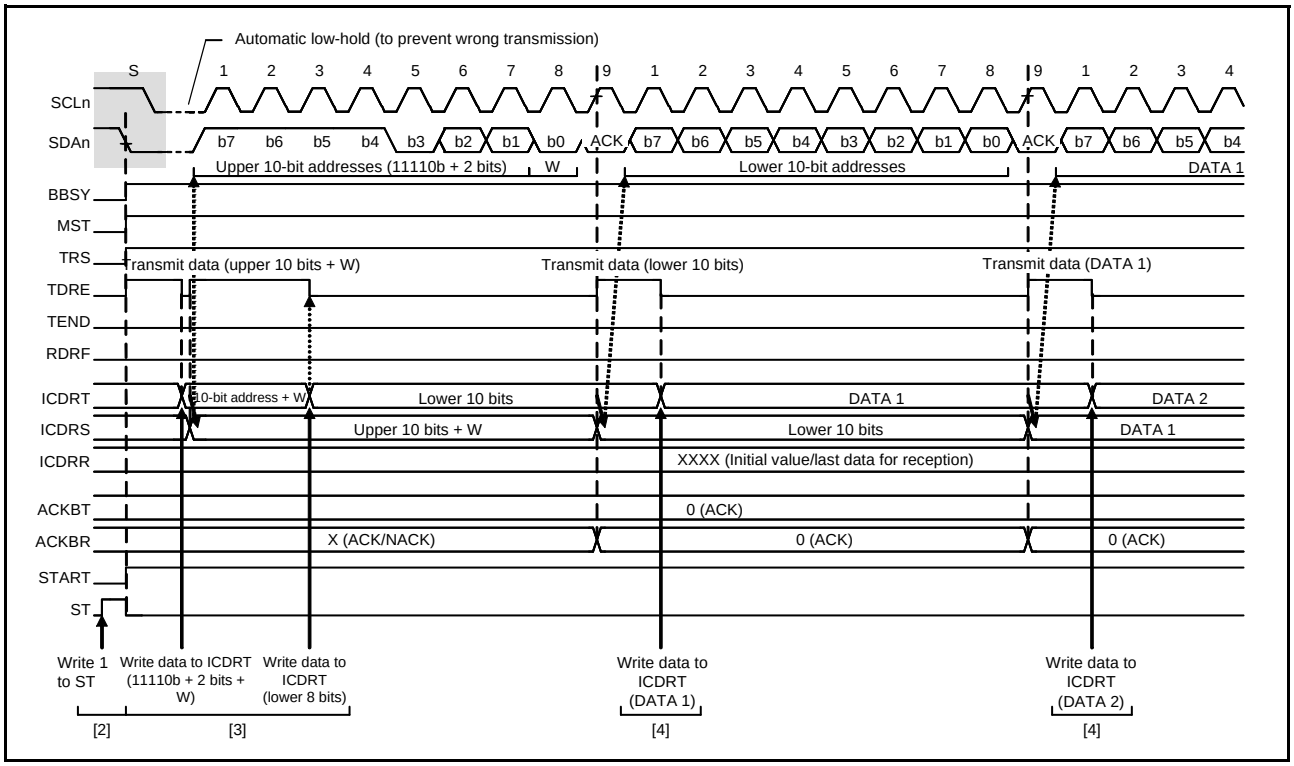


Figure 30.8 Master Transmit Operation Timing (2) (10-Bit Address Format)

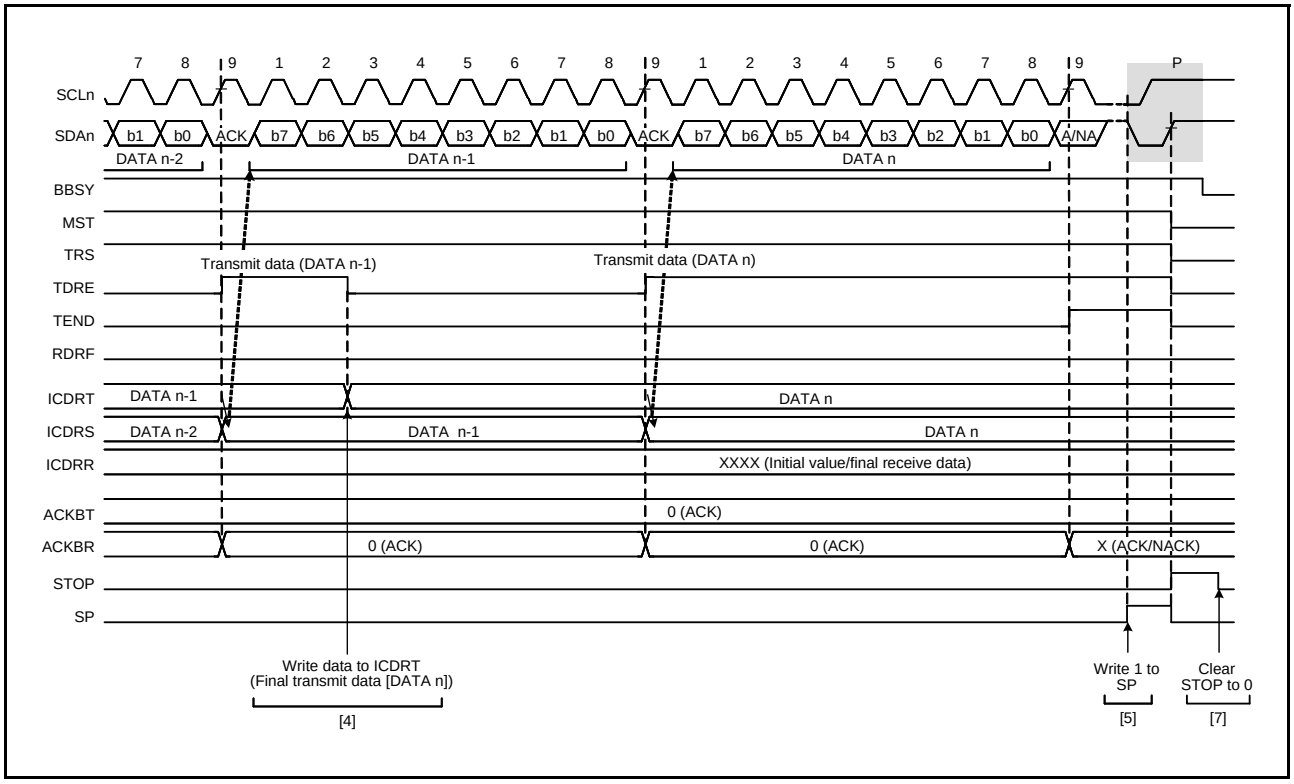


Figure 30.9 Master Transmit Operation Timing (3)

30.3.4 Master Receive Operation

In master receive operation, the RIIC as a master device outputs the SCL (clock) signal, receives data from the slave device, and returns acknowledgements. Since the RIIC must start by sending a slave address to the corresponding slave device, this part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.

Figure 30.11 shows an example of usage of master reception and Figure 30.12 and Figure 30.14 show the timing of operations in master reception.

The following describes the procedure and operations for master reception.

(1) Perform initial setting as described in section 30.3.2, Initial Settings.

(2) Read the BBSY flag in ICCR2 to check that the bus is open, and then set the ST bit in ICCR2 to 1 (start condition issuance request). Upon receiving the request, the RIIC issues a start condition. When the RIIC detects the start condition, the BBSY flag and the START flag in ICSR2 are automatically set to 1 and the ST bit is automatically cleared to 0. At this time, if the start condition is detected and the levels for the SDA output and the levels on the SDAn line have matched while the ST bit is 1, the RIIC recognizes that issuing of the start condition as requested by the ST bit has been successfully completed, and the MST and TRS bits in ICCR2 are automatically set to 1, placing the RIIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to setting of the TRS bit to 1.

(3) Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. Once the data for transmission are written to ICDRT, the TDRE flag is automatically cleared to 0, the data are transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. Once the byte containing the slave address and R/W# bit has been transmitted, the value of the ICCR2.TRS bit is automatically updated to select transmit or receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 1, the TRS bit is cleared to 0 on the rising edge of the ninth cycle of SCLn (the clock signal), placing the RIIC in master receive mode. At this time, the TDRE flag is automatically cleared to 0 and the ICSR2.RDRF flag is automatically set to 1.
Since the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmitting 1111 0b, the two higher-order bits of the slave address, and the R bit places the RIIC in master receive mode.

(4) Dummy read ICDRR after confirming that the RDRF flag in ICSR2 is 1; this makes the RIIC start output of the SCL (clock) signal and start data reception.

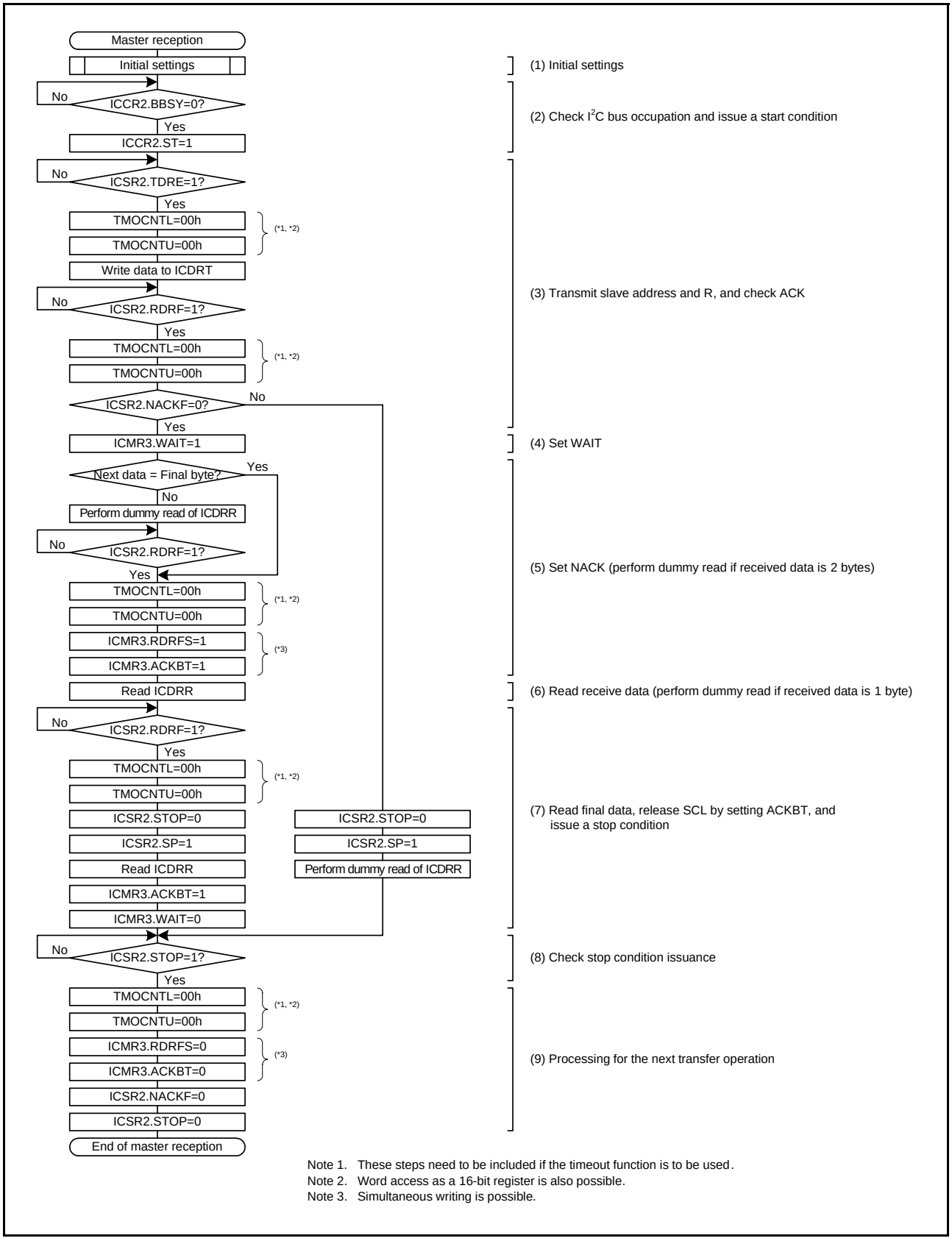
(5) After 1 byte of data has been received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the RDRFS bit in ICMR3. Reading out ICDRR at this time will produce the received data, and the RDRF flag is automatically cleared to 0 at the same time. Furthermore, the value of the acknowledgement field received during the ninth cycle of SCL clock is returned as the value set in the ACKBT bit of ICMR3. Furthermore, if the next byte to be received is the next to last byte, set the ICMR3.WAIT bit to 1 (for wait insertion) before reading the ICDRR (containing the second byte from last). As well as enabling NACK output even in the case of delays in processing to set the ICMR3.ACKBT bit to 1 (NACK) in step (6), due to other interrupts, etc., this fixes the SCLn line to the low level on the rising edge of the ninth clock cycle in reception of the last byte, so the state is such that issuing a stop condition is possible.

(6) When the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ACKBT bit in ICMR3 to 1 (NACK).

(7) After reading out the byte before last from the ICDRR register, if the value of the ICSR2.RDRF flag is confirmed to be 1, write 1 to the SP bit in ICCR2 (stop condition issuance request) and then read the last byte from ICDRR. When ICDRR is read, the RIIC is released from the wait state and issues the stop condition after low-level output in the ninth clock cycle is completed or the SCL line is released from the low-hold state.

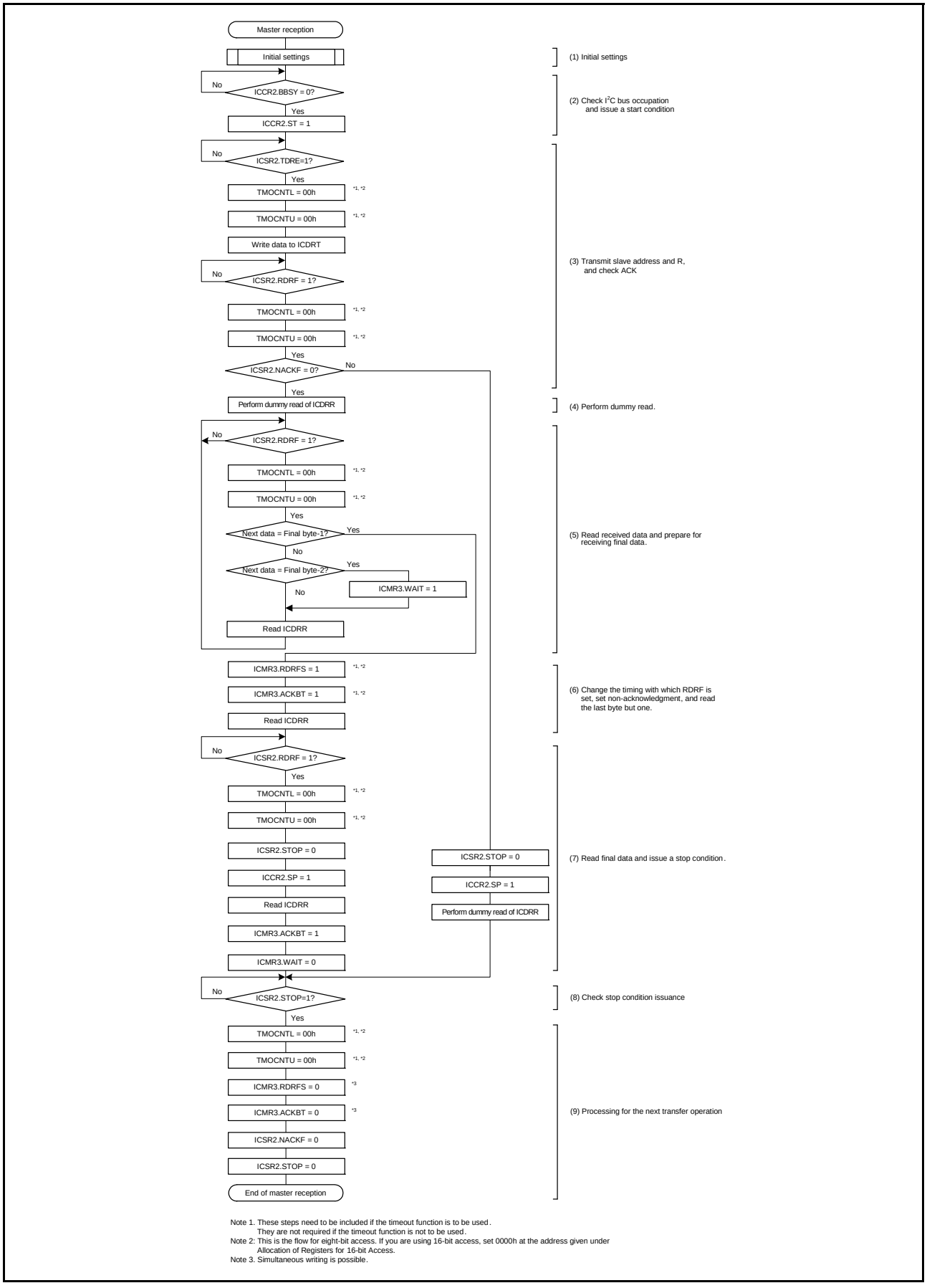
(8) Upon detecting the stop condition, the RIIC automatically clears the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Furthermore, detection of the stop condition leads to setting of the STOP flag in ICSR2 to 1.

(9) After checking that the ICSR2.STOP flag is 1, clear the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.



Note 1. These steps need to be included if the timeout function is to be used.
Note 2. Word access as a 16-bit register is also possible.
Note 3. Simultaneous writing is possible.

Figure 30.10 Example of Master Reception Flowchart (7-Bit Address Format with 2 Byte or Below)



Note 1. These steps need to be included if the timeout function is to be used. They are not required if the timeout function is not to be used.
Note 2: This is the flow for eight-bit access. If you are using 16-bit access, set 0000h at the address given under Allocation of Registers for 16-bit Access.
Note 3. Simultaneous writing is possible.

Figure 30.11 Example of Master Reception Flowchart (7-Bit Address Format with 3 Byte or more)

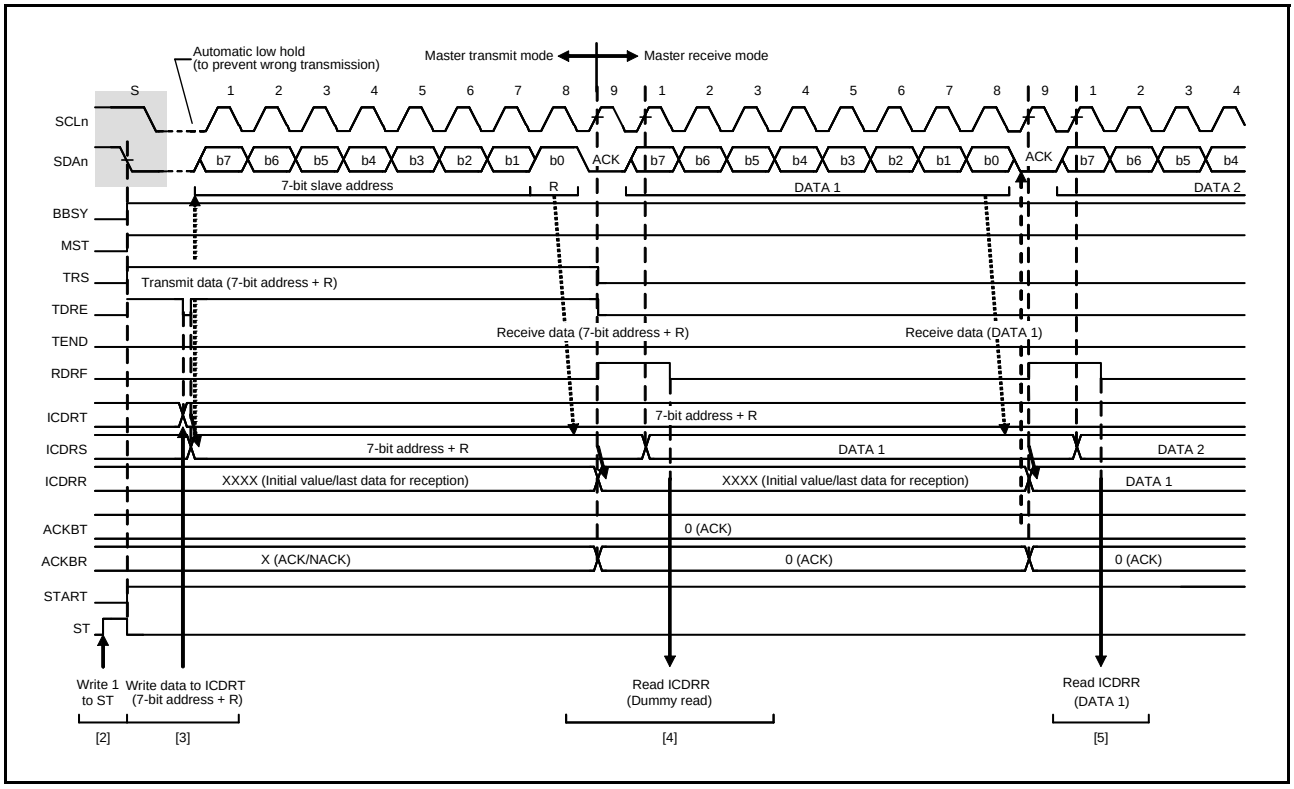


Figure 30.12 Master Receive Operation Timing (1) (7-Bit Address Format, when RDRFS = 0)

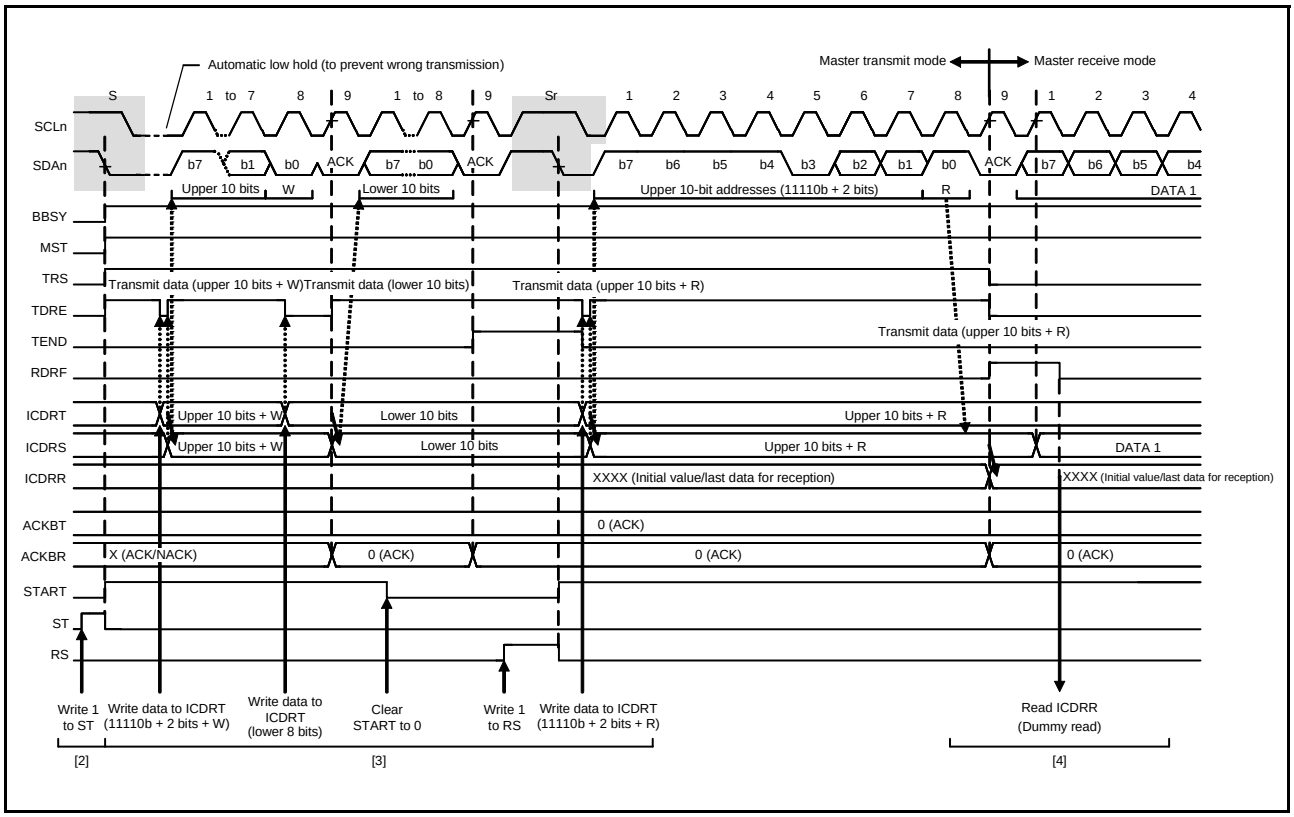


Figure 30.13 Master Receive Operation Timing (2) (10-Bit Address Format, when RDRFS = 0)

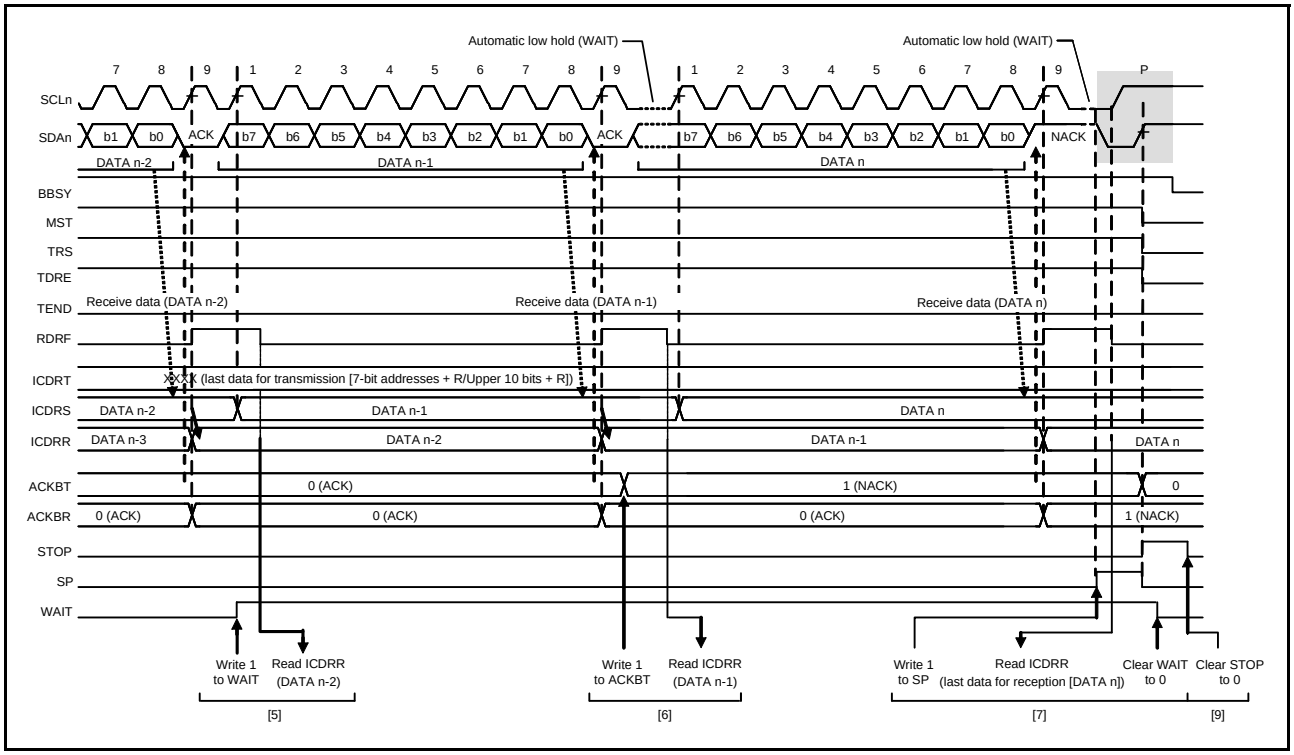


Figure 30.14 Master Receive Operation Timing (3) (when RDRFS = 0)

30.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL (clock) signal, the RIIC transmits data as a slave device, and the master device returns acknowledgements.

Figure 30.15 shows an example of usage of slave transmission and Figure 30.16 and Figure 30.17 show the timing of operations in slave transmission.

The following describes the procedure and operations for slave transmission.

(1) Perform initial setting as described in section 30.3.2, Initial Settings.

(2) After receiving a matching slave address, the RIIC sets one of the corresponding bits ICSR1.HOA, GCA, and AASy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 1, the RIIC automatically places itself in slave transmit mode by setting both the TRS bit and the TDRE flag in ICSR2 to 1.

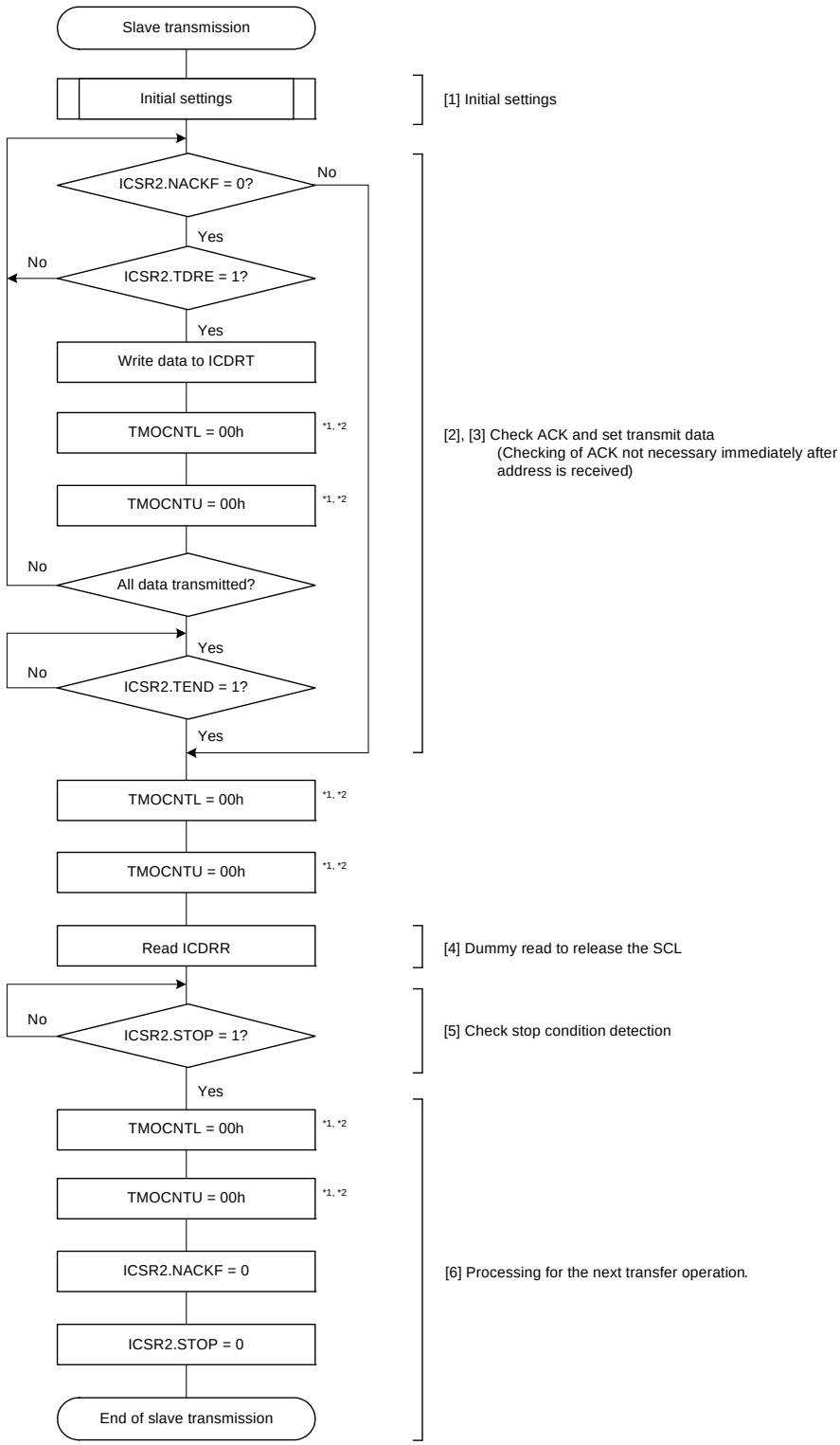
(3) After the ICSR2.TEND flag is confirmed to be 1, write the data for transmission to the ICDRT register. At this time, if the RIIC receives no acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the RIIC suspends transfer of the next data.

(4) Wait unit the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the RIIC drives the SCLn line low on the ninth falling edge of SCL clock.

(5) When the ICSR2.NACKF flag or the ICSR2.TEND flag is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.

(6) Upon detecting the stop condition, the RIIC automatically clears bits ICSR1.HOA, GCA, and AASy (y = 0 to 2), flags ICSR2.TDRE and TEND, and the ICCR2.TRS bit to 0, and enters slave receive mode.

(7) After checking that the ICSR2.STOP flag is 1, clear the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.



Note 1. These steps need to be included if the timeout function is to be used. They are not required if the timeout function is not to be used.
Note 2: This is the flow for eight-bit access. If you are using 16-bit access, set 0000h at the address given under Allocation of Registers for 16-bit Access.

Figure 30.15 Example of Slave Transmission Flowchart

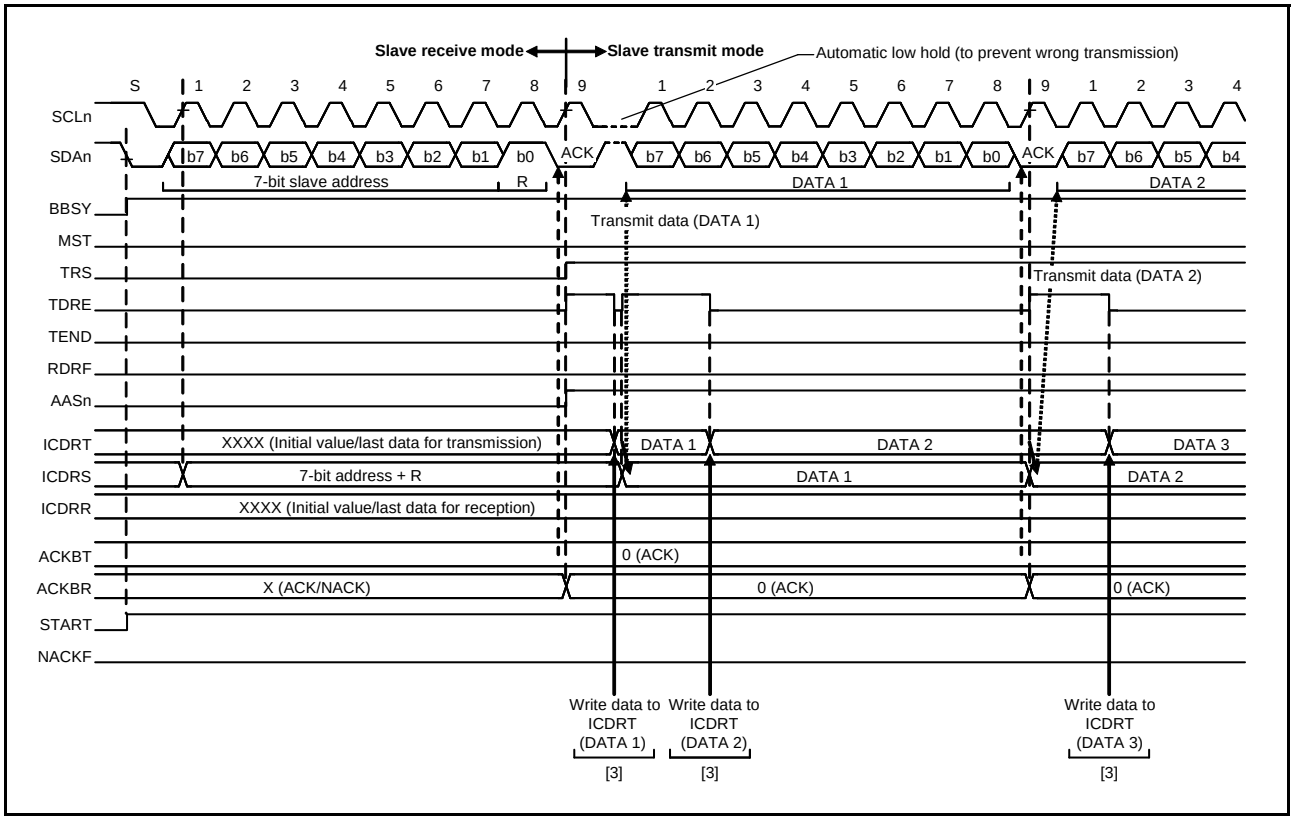


Figure 30.16 Slave Transmit Operation Timing (1) (7-Bit Address Format)

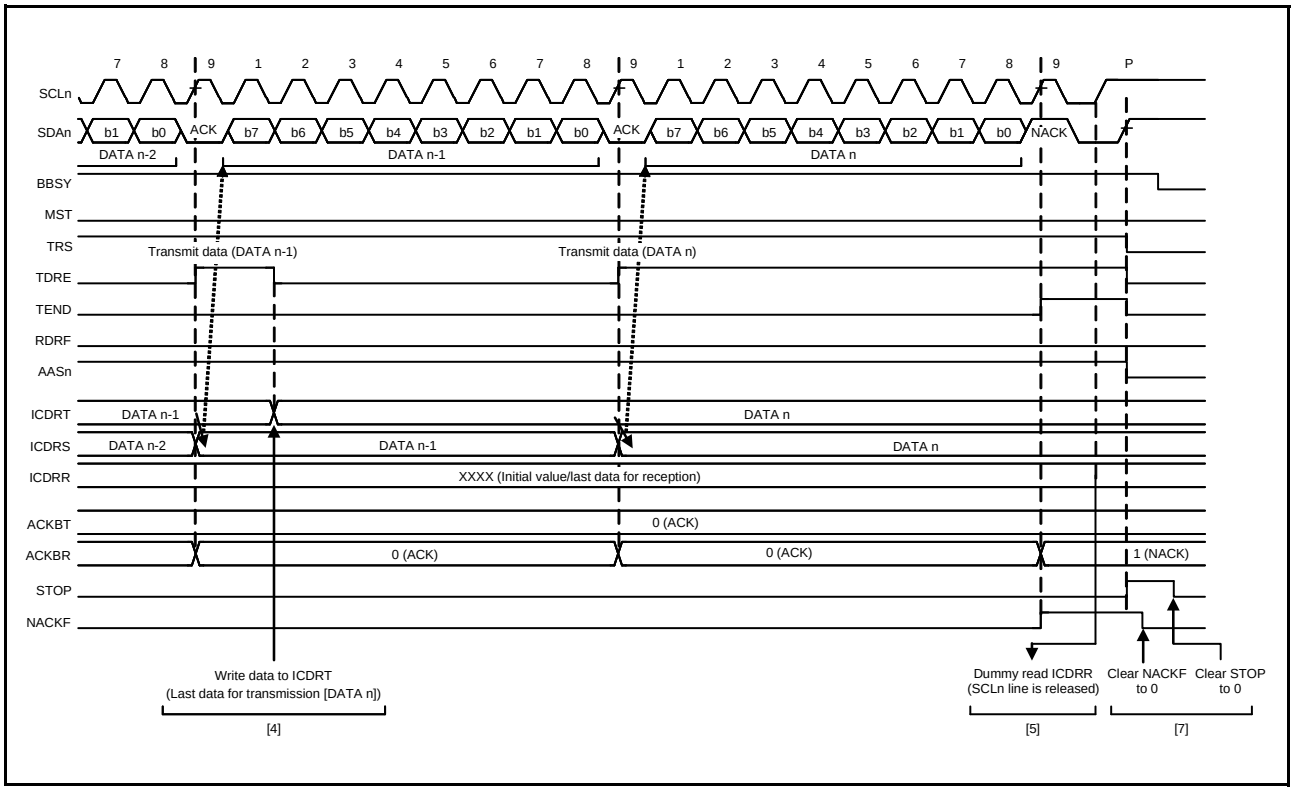


Figure 30.17 Slave Transmit Operation Timing (2)

30.3.6 Slave Receive Operation

In slave receive operation, the master device outputs the SCL clock and transmit data, and the RIIC returns acknowledgements as a slave device.

Figure 30.18 shows an example of usage of slave reception and Figure 30.19 and Figure 30.20 show the timing of operations in slave reception.

The following describes the procedure and operations for slave reception.

(1) Perform initial setting as described in section 30.3.2, Initial Settings.

(2) After receiving a matching slave address, the RIIC sets one of the corresponding bits ICSR1.HOA, GCA, and AASy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 0, the RIIC continues to place itself in slave receive mode and sets the RDRF flag in ICSR2 to 1.

(3) After the ICSR2.STOP flag is confirmed to be 0 and the ICSR2.RDRF flag to be 1, dummy read ICDRR (the dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower eight bits when the 10-bit address format is selected).

(4) When ICDRR is read, the RIIC automatically clears the ICSR2.RDRF flag to 0. If reading of ICDRR is delayed and a next byte is received while the RDRF flag is still set to 1, the RIIC holds the SCL line low from one SCL cycle before the timing with which RDRF should be set. In this case, reading ICDRR releases the SCL line from being held at the low level.
When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read ICDRR until all the data is completely received.

(5) Upon detecting the stop condition, the RIIC automatically clears bits ICSR1.HOA, GCA, and AASy (y = 0 to 2) to 0.

(6) After checking that the ICSR2.STOP flag is 1, clear the ICSR2. STOP flag to 0 for the next transfer operation.

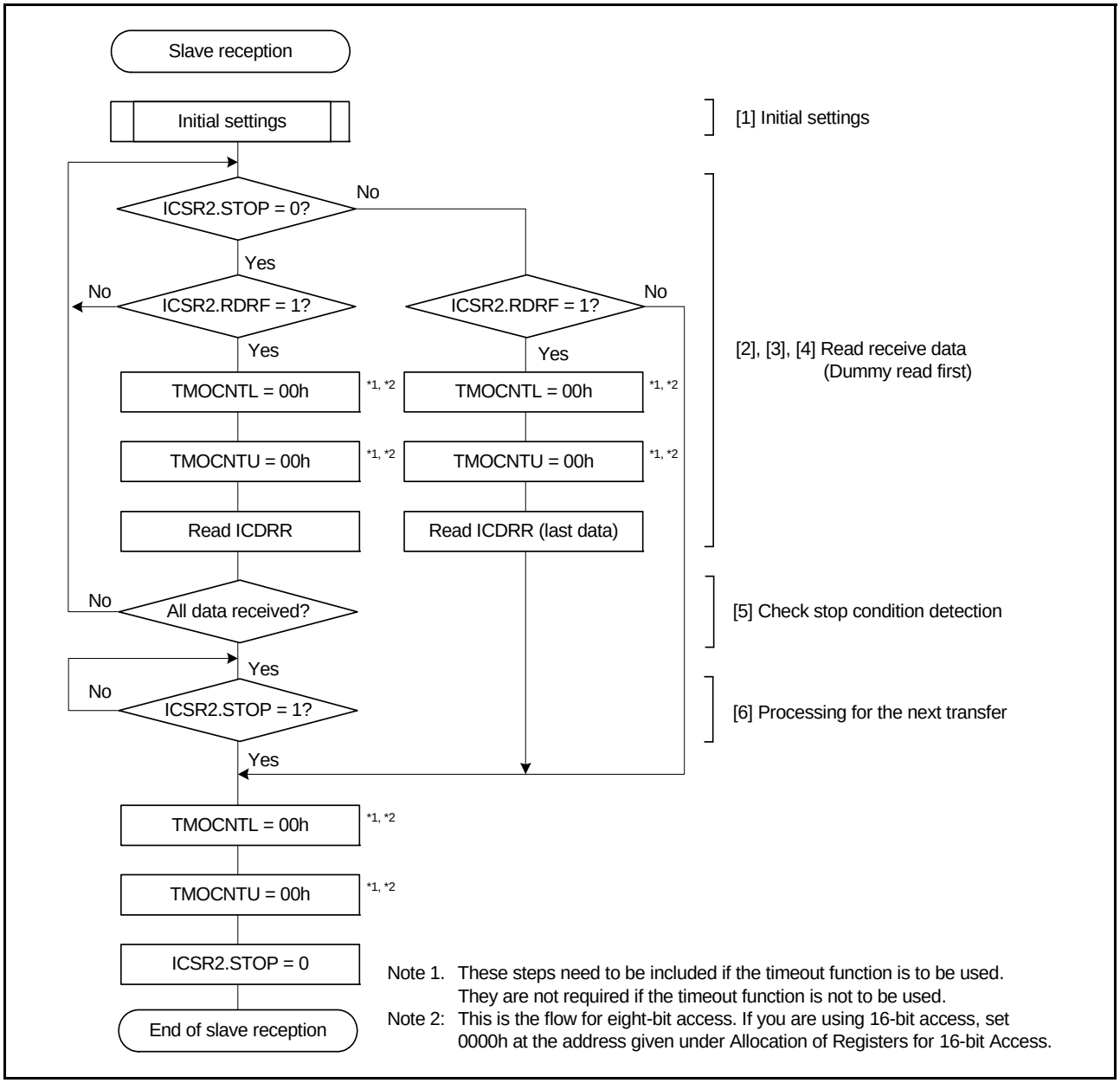


Figure 30.18 Example of Slave Reception Flowchart

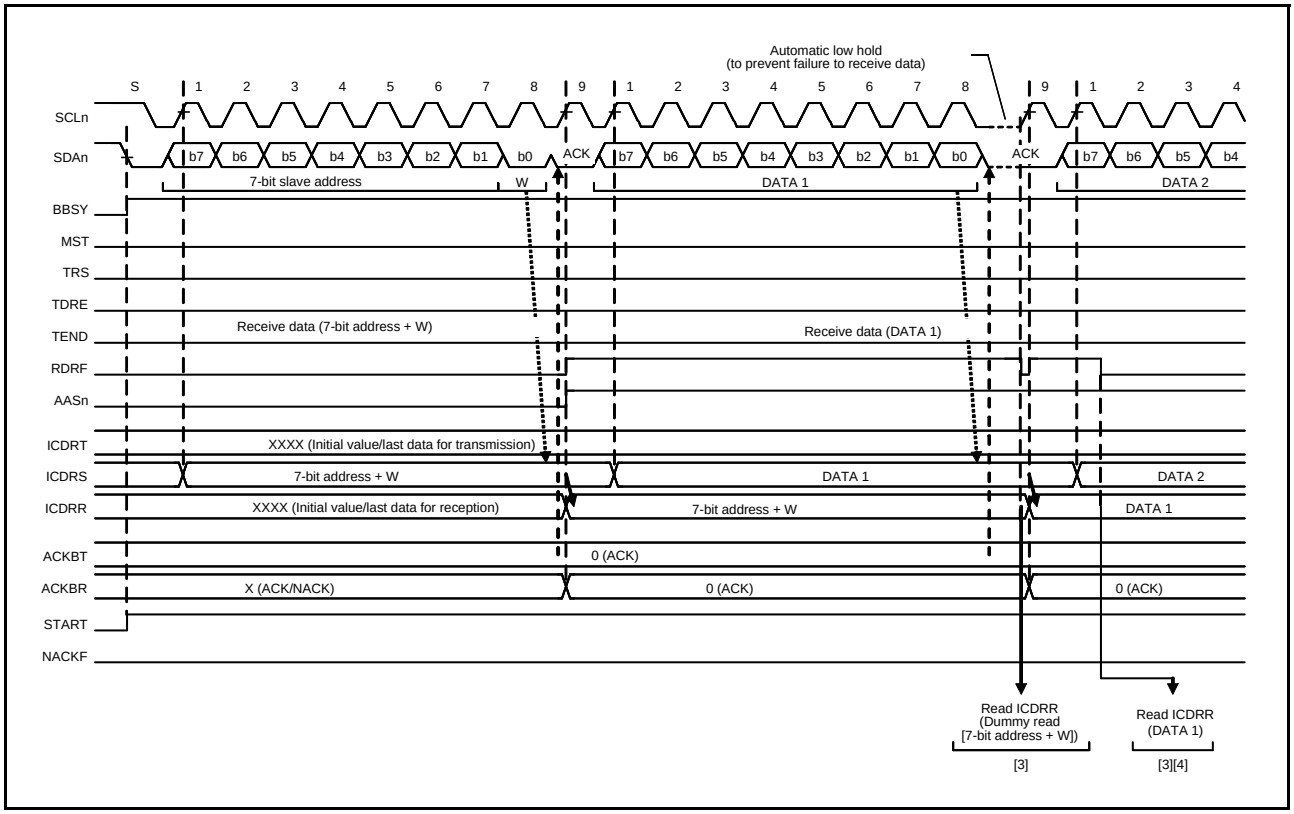


Figure 30.19 Slave Receive Operation Timing (1) (7-Bit Address Format, when RDRFS = 0)

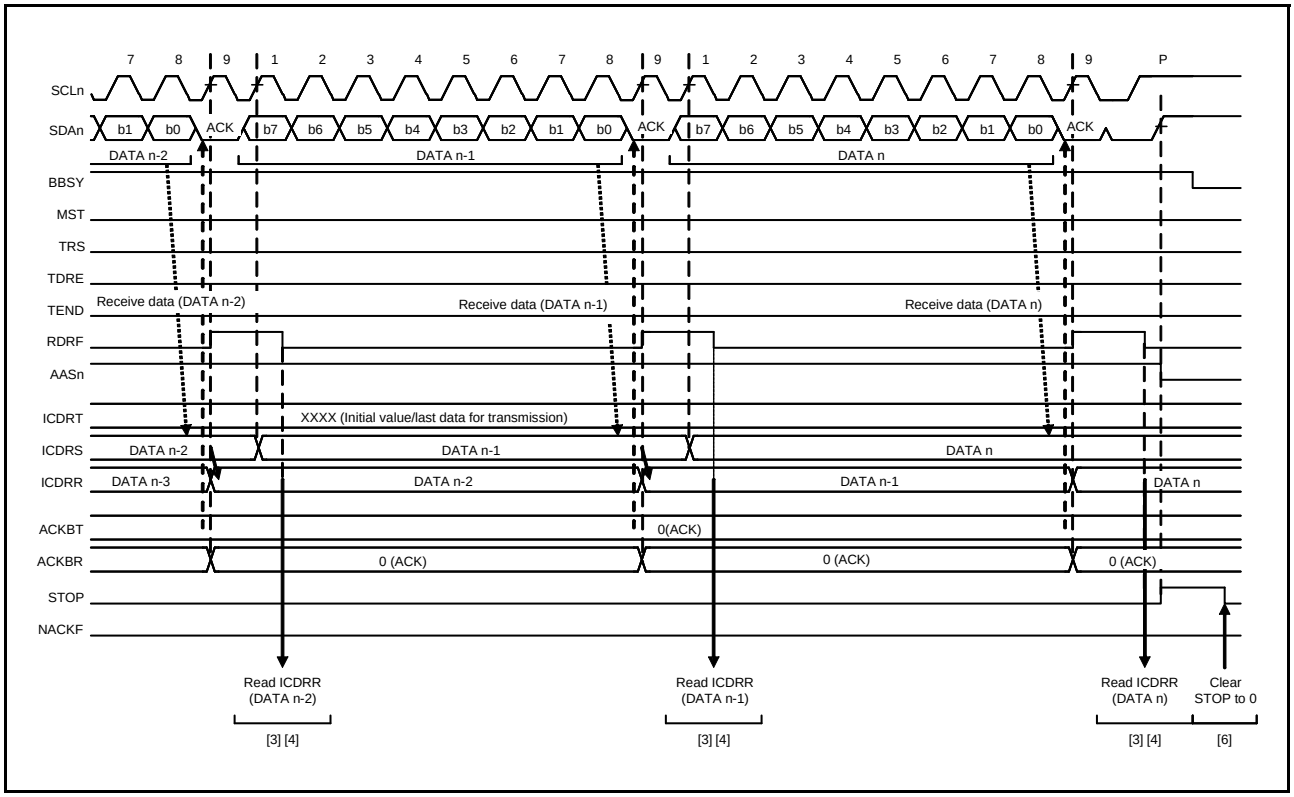


Figure 30.20 Slave Receive Operation Timing (2) (when RDRFS = 0)

30.4 SCL Synchronization Circuit

In generation of the SCL (clock) signal, the RIIC starts counting out the value for width at high level specified in ICBRH when it detects a rising edge on the SCLn line and drives the SCLn line low once counting of the width at high level is complete. When the RIIC detects the falling edge of the SCLn line, it starts counting out the width at low level period specified in ICBRL, and then stops driving the SCLn line (releases the line) once counting of the width at low level is complete. The SCL (clock) signal is thus generated.

If multiple master devices are connected to the I2C bus, a collision of SCL signals may arise due to contention with another master device. In such cases, the master devices have to synchronize their SCL signals. Since this synchronization of SCL signals must be bit by bit, the RIIC is equipped with a facility (the SCL synchronization circuit) to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When the RIIC has detected a rising edge on the SCLn line and thus started counting out the width at high level specified in ICBRH, and the level on the SCLn line falls because an SCL signal is being generated by another master device, the RIIC stops counting when it detects the falling edge, drives the level on the SCLn line low, and starts counting out the width at low level specified in ICBRL. When the RIIC finishes counting out the width at low level, it stops driving the SCLn line to the low level (i.e. releases the line). At this time, if the width at low level of the SCL clock signal from the other master device is longer than the width at low level set in the RIIC, the width at low level of the SCL signal will be extended. Once the width at low level for the other master device has ended, the SCL signal rises because the SCL line has been released. When the RIIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, in cases of contention of SCL signals from more than one master, the width at high level of the SCL signal is synchronized with that of the clock having the narrower width, and the width at low level of the SCL signal is synchronized with that of the clock having the broader width. However, such synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.

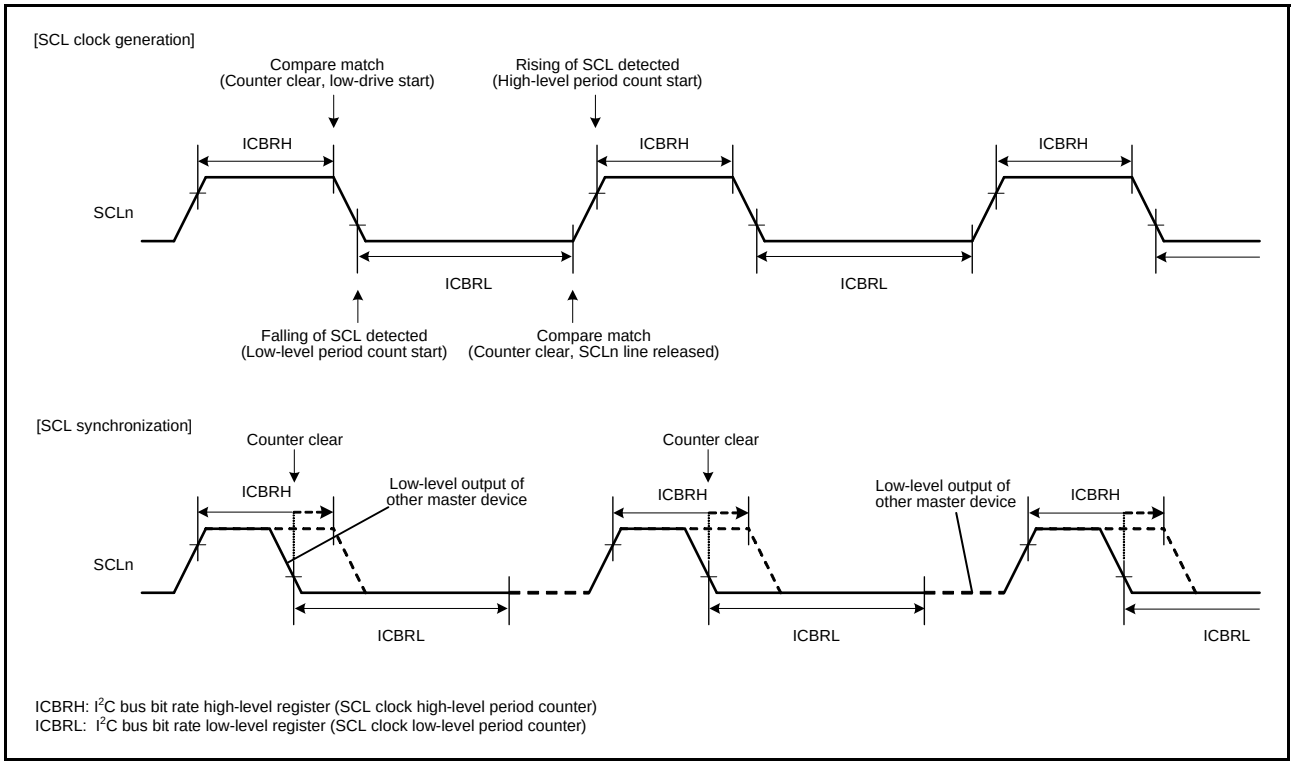


Figure 30.21 Generation and Synchronization of the SCL Signal from the RIIC

30.5 Facility for Delaying SDA Output

The RIIC module incorporates a facility for delaying output on the SDA line. The delay can be applied to all output (issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals) on the SDA line.

With the SDA output delay facility, SDA output is delayed from detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval over which the SCL (clock) signal is at the low level. Doing this leads to usage with the aim of preventing erroneous operation of communications devices, with the aim of satisfying the 300-ns (min.) data-hold time requirement of the SMBus specification.

The output delay facility is enabled by setting the SDDL[2:0] bits in ICMR2 to any value other than 000b, and disabled by setting the same bits to 000b.

While the SDA output delay facility is enabled (i.e. while the SDDL[2:0] bits in ICMR2 are set to any value other than 000b), the DLCS bit in ICMR2 selects the clock source for counting by the SDA output delay counter as the internal base clock (IICϕ) for the RIIC module or as a clock signal derived by dividing the frequency of the internal base clock by two (IICϕ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. After counting of the set number of cycles of delay is completed, the RIIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.

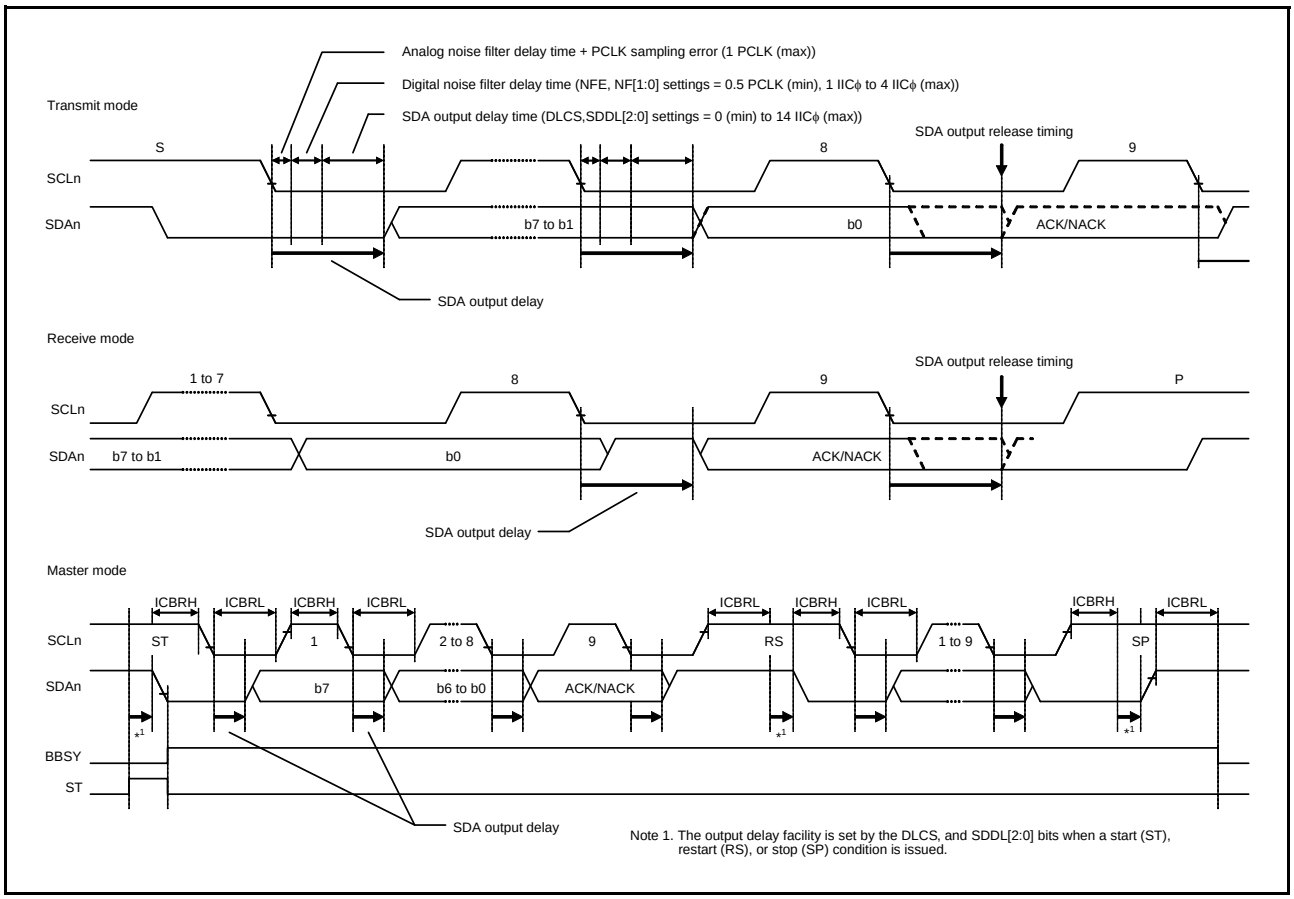


Figure 30.22 SDA Output Delay Facility

30.6 Digital Noise-Filter Circuits

The states of the SCLn and SDAn pins are conveyed to the internal circuitry through analog noise-filter and digital noise-filter circuits. Figure 30.23 is a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of the RIIC consists of four flip-flop circuit stages connected in series and a match-detection circuit.

The number of effective stages in the digital noise filter is selected by the NF[1:0] bits in ICMR3. The selected number of effective stages determines the noise-filtering capability as a period from one to four IICϕ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICϕ signal. When the input signal level matches the output level of the number of effective flip-flop circuit stages as selected by the NF[1:0] bits in ICMR3, the signal level is conveyed to the subsequent stage. If the signal levels do not match, the previous value is retained.

If the ratio between the frequency of the internal operating clock (PCLK) and the transfer rate is small (e.g. data transfer at 400 kbps with PCLK = 4 MHz), the characteristics of the digital noise filter may lead to the elimination of needed signals as noise. In such cases, it is possible to disable the digital noise-filter circuit (by clearing the NFE bit in ICFER) and use only the analog noise-filter circuit.

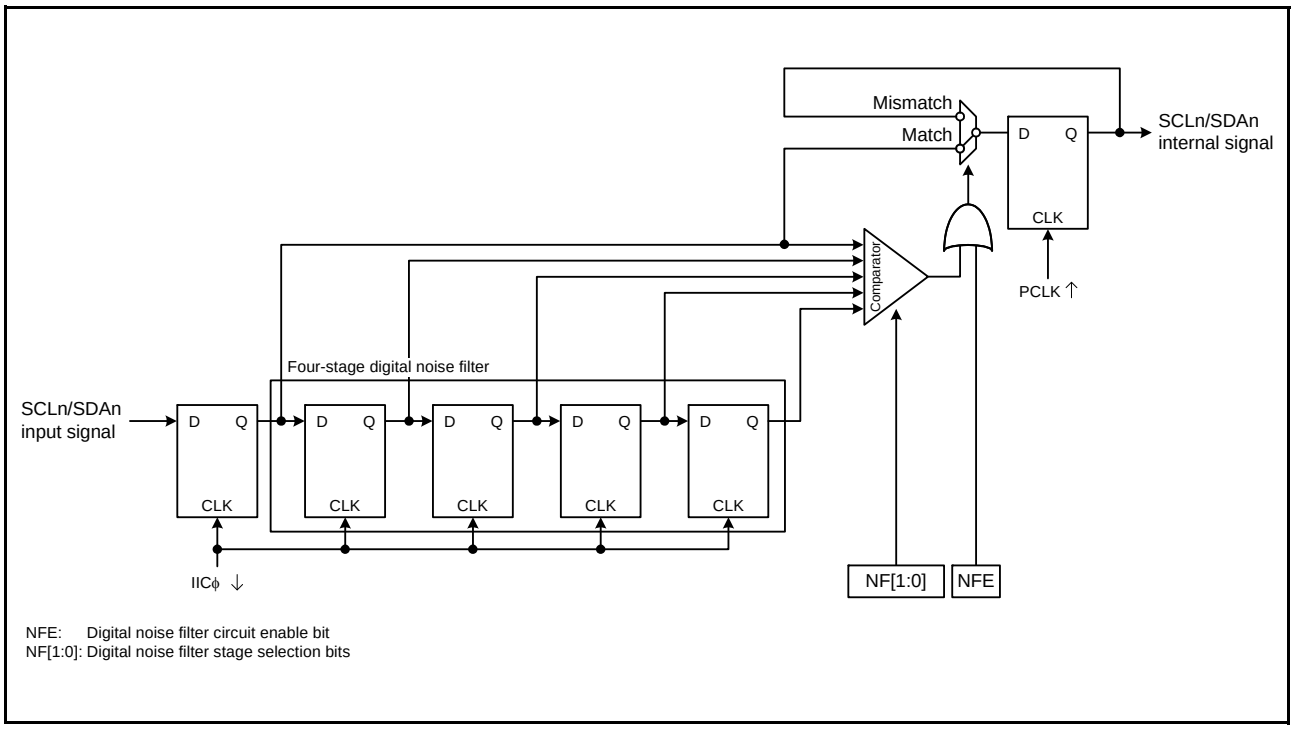


Figure 30.23 Block Diagram of Digital Noise Filter Circuit

30.7 Address Match Detection

The RIIC can set three unique slave addresses in addition to the general call address and host address, and also can set 7-bit or 10-bit slave addresses.

30.7.1 Slave-Address Match Detection

The RIIC can set three unique slave addresses, and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in SARUy and SARLy (y = 0 to 2) can be detected.

When the RIIC detects a match of the set slave address, the corresponding AASy flag (y = 0 to 2) in ICSR1 is set to 1 at the falling edge of the ninth SCL clock cycle, and the RDRF flag in ICSR2 or the TDRE flag in ICSR2 is set to 1 by the following R/W# bit. This causes a receive data full interrupt (ICRXI) or transmit data empty interrupt (ICTXI) to be generated. The AASy flag is used to identify which slave address has been specified.

Figure 30.24 to Figure 30.26 show the AASy flag set timing in three cases.

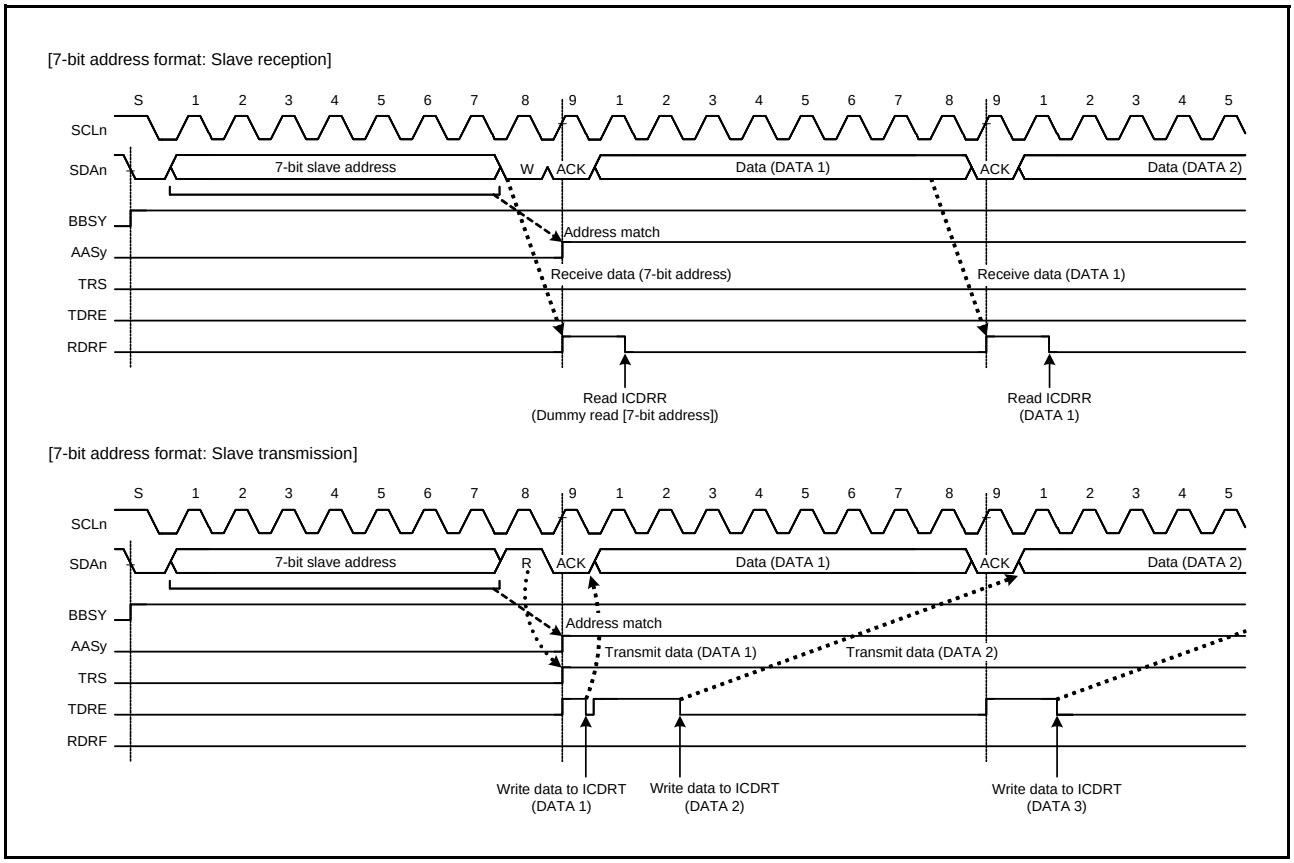


Figure 30.24 AASy Flag Set Timing with 7-Bit Address Format Selected

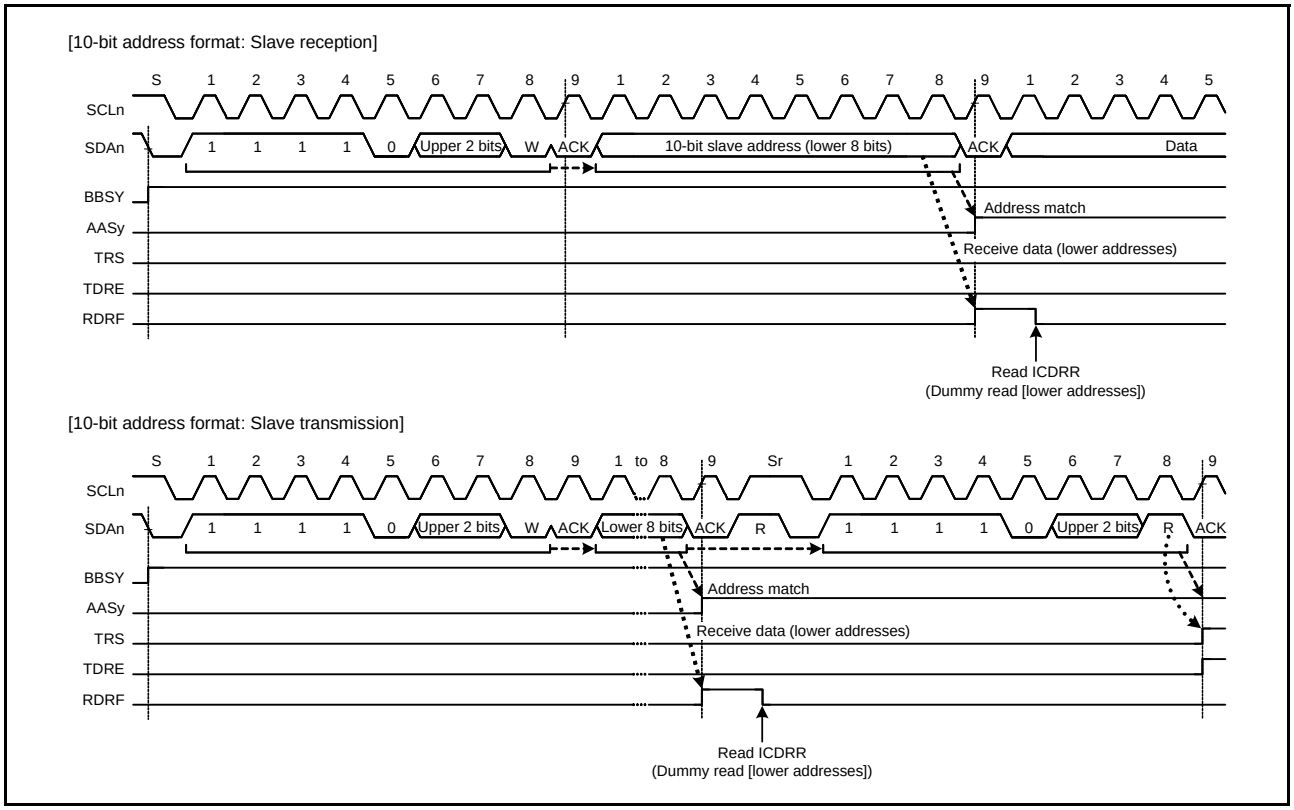


Figure 30.25 AASy Flag Set Timing with 10-Bit Address Format Selected

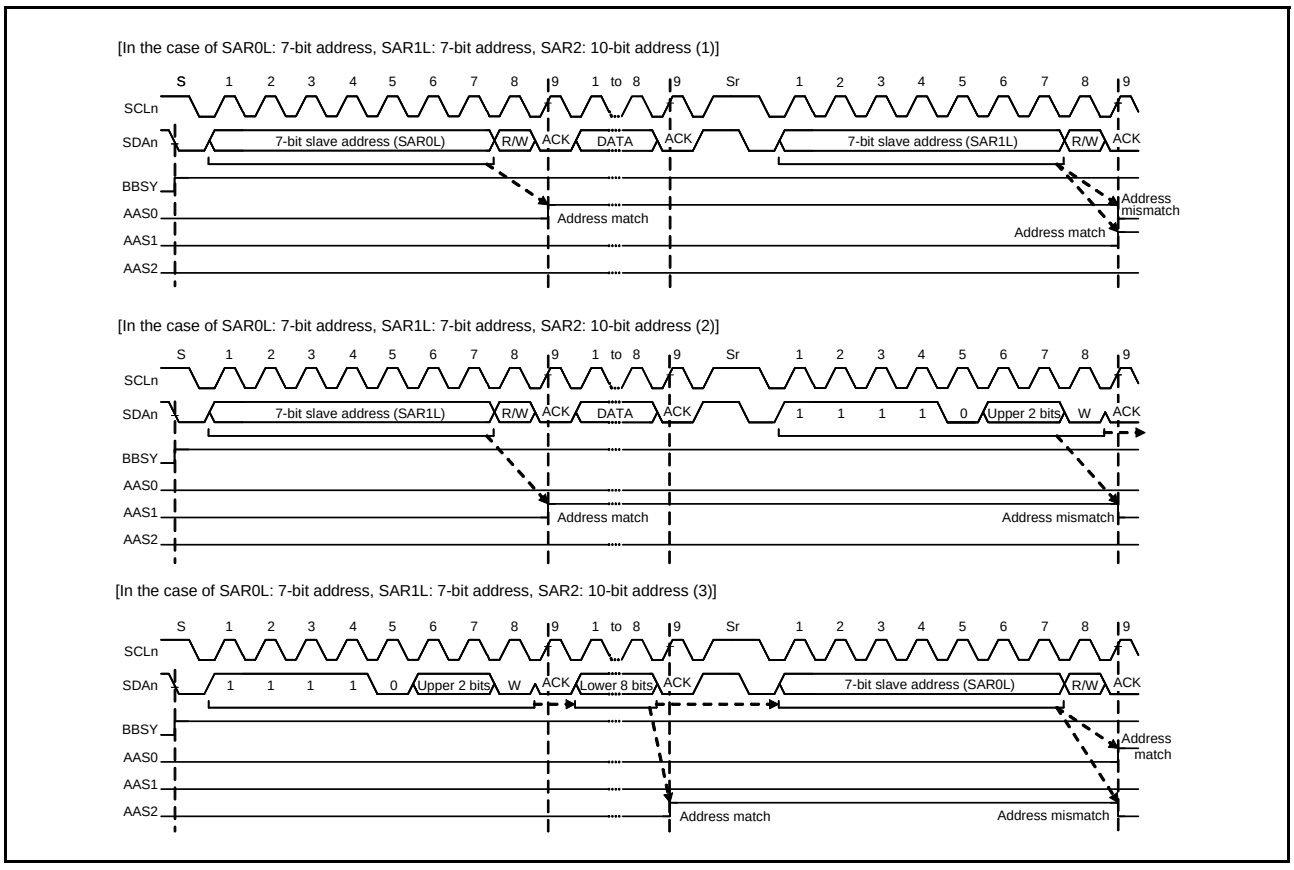


Figure 30.26 AASy Flag Set/Clear Timing with 7-Bit/10-Bit Address Formats Mixed

30.7.2 Detection of the General Call Address

The RIIC has a facility for detecting the general call address (0000 000b + 0 [W]). This is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the RIIC recognizes this as the address of a slave device with an “all-zero” address but not as the general call address.

When the RIIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 are set to 1 on the rising edge of the ninth cycle of SCL clock. This leads to the generation of a receive data full interrupt (ICRXI). The value of the GCA flag can be confirmed to recognize that the general call address has been transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

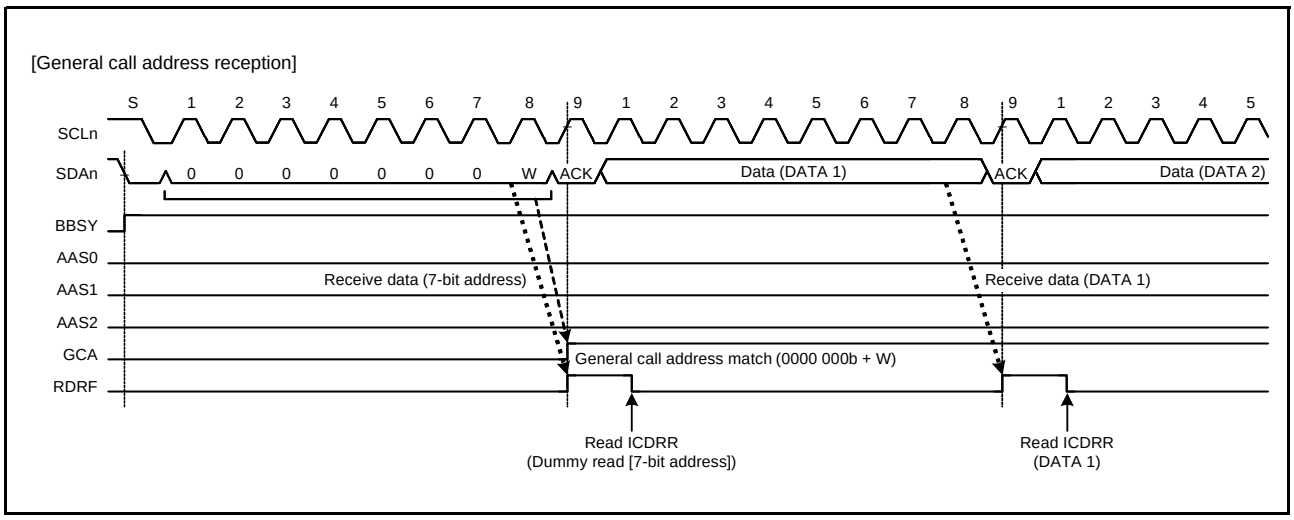


Figure 30.27 Timing of GCA Flag Setting during Reception of General Call Address

30.7.3 Device-ID Address Detection

The RIIC module has a facility for detecting device-ID addresses conformant with the I2C bus specification (Rev. 03).

When the RIIC receives 1111 100b as the first byte after a start condition or restart condition was issued with the DIDE bit in ICSER set to 1, the RIIC recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the eighth SCL clock cycle when the following R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the RIIC sets the corresponding AASy flag (y = 0 to 2) in ICSR1 to 1.

After that, when the first byte received after a start or restart condition is issued matches the device ID address (1111 100b) again and the following R/W# bit is 1, the RIIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device-ID address detection function, the RIIC clears the DID flag to 0 if a match with the RIIC’s own slave address is not obtained or a match with the device ID address is not obtained after a match with the RIIC’s own slave address and the detection of a restart condition. If the first byte after detection of a start or restart condition matches the device ID address (1111 100b) and the R/W# bit is 0, the RIIC sets the DID flag to 1 and compares the second and subsequent bytes with the RIIC’s slave address. If the R/W# bit is 1, the DID flag holds the previous value and the RIIC does not compare the second and subsequent bytes. Therefore, the reception of a device-ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Furthermore, prepare the device-ID fields (three bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal data for transmission. For details of the information that must be included in device-ID fields, contact NXP Semiconductors.

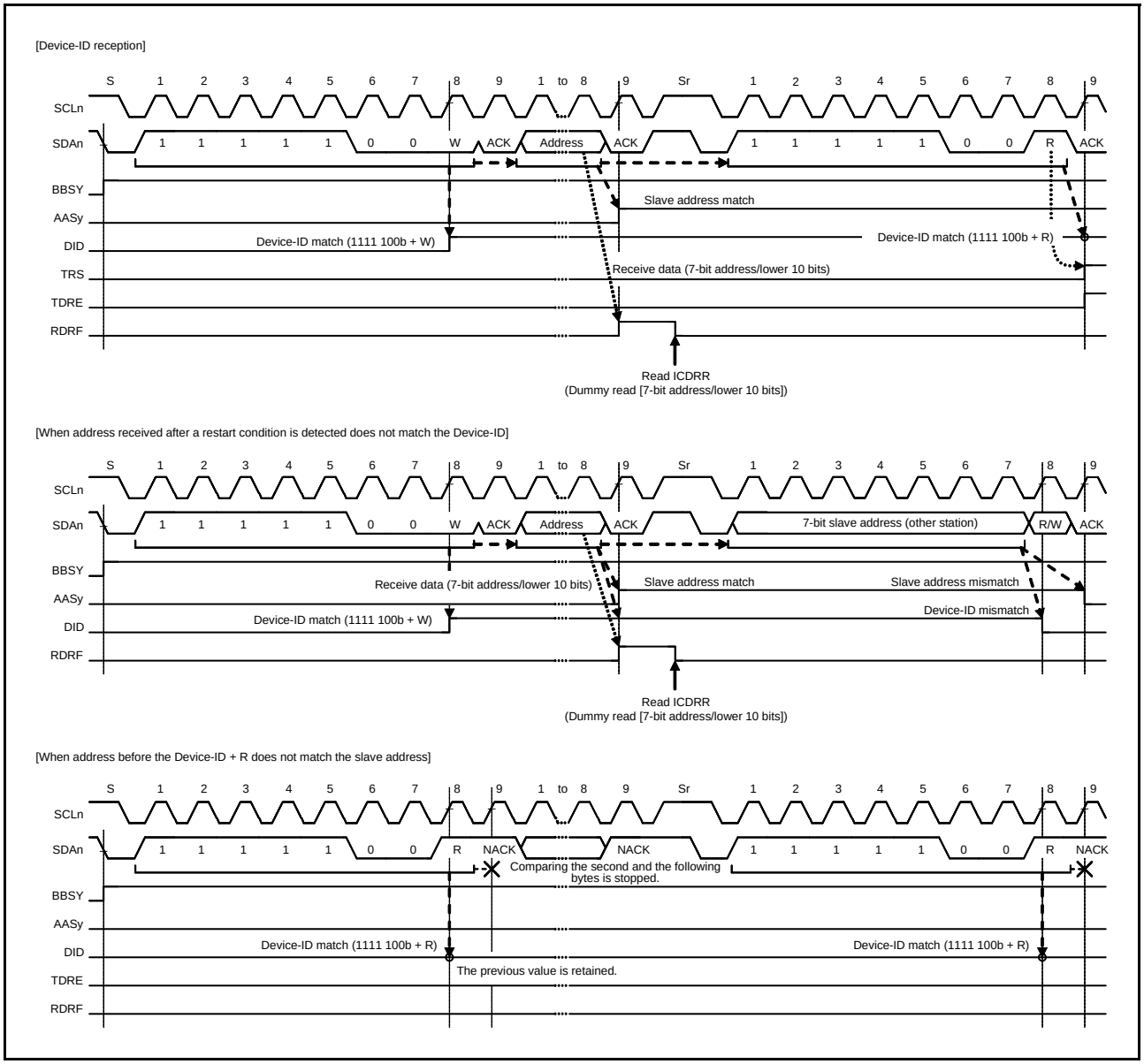


Figure 30.28 AASy/DID Flag Set/Clear Timing during Reception of Device-ID

30.7.4 Host Address Detection

The RIIC has a function to detect the host address while the SMBus is operating. When the HOAE bit in ICSER is set to 1 while the SMBS bit in ICMR3 is 1, the RIIC can detect the host address (0001 000b) in slave receive mode (MST and TRS bits = 00b in ICCR2).

When the RIIC detects the host address, the HOA flag in ICSR1 is set to 1 at the rising edge of the ninth SCL clock cycle, and at the same time, the TDRE flag in ICSR2 is set to 1 when the R/W# bit is 0 (Wr bit). This causes a transmit data empty interrupt (ICTXI) to be generated. The HOA flag is used to recognize that the host address was sent from the smart battery or other devices.

If the bit following the host address (0001 000b) is an Rd bit (R/W# bit = 1), the RIIC can also detect the host address. After the host address is detected, the RIIC operates in the same manner as normal slave operation.

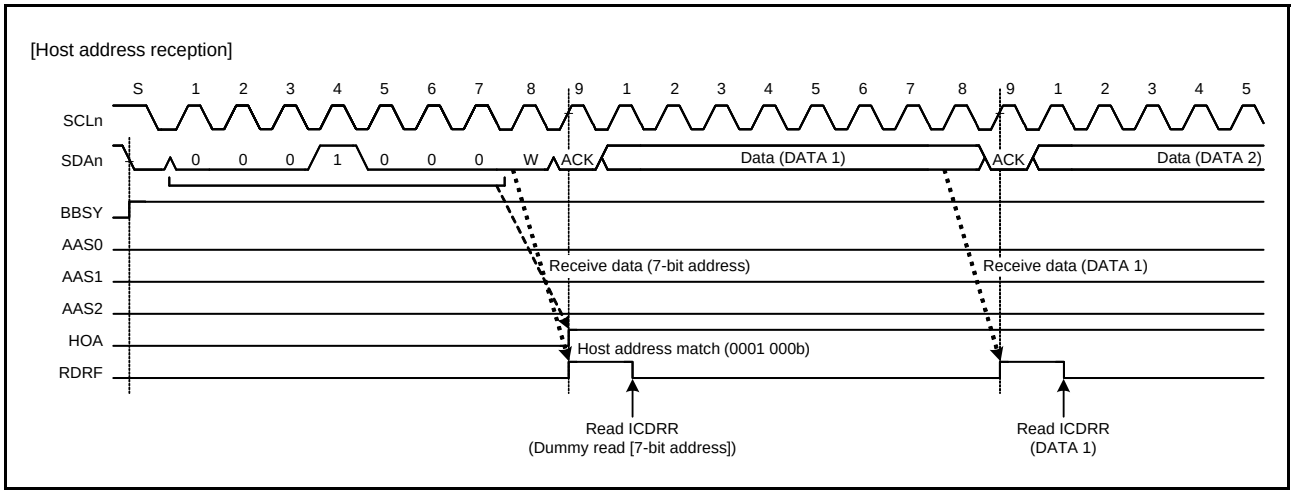


Figure 30.29 HOA Flag Set Timing during Reception of Host Address

30.8 Automatically Low-Hold Function for SCL

30.8.1 Function to Prevent Wrong Transmission of Transmit Data

If the shift register (ICDRS) is empty when data have not been written to the transmit data register (ICDRT) with the RIIC in transmission mode (TRS bit = 1 in ICCR2), the SCLn signal is automatically held at the low level over the intervals shown below. This low-hold period is extended until data for transmission have been written, which prevents the unintended transmission of erroneous data.

<Master transmit mode>

- Low-level interval after a start condition or restart condition is issued
- Low-level interval of one clock cycle between the ninth clock cycle of one transfer and the first clock cycle of the next

<Slave transmit mode>

- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

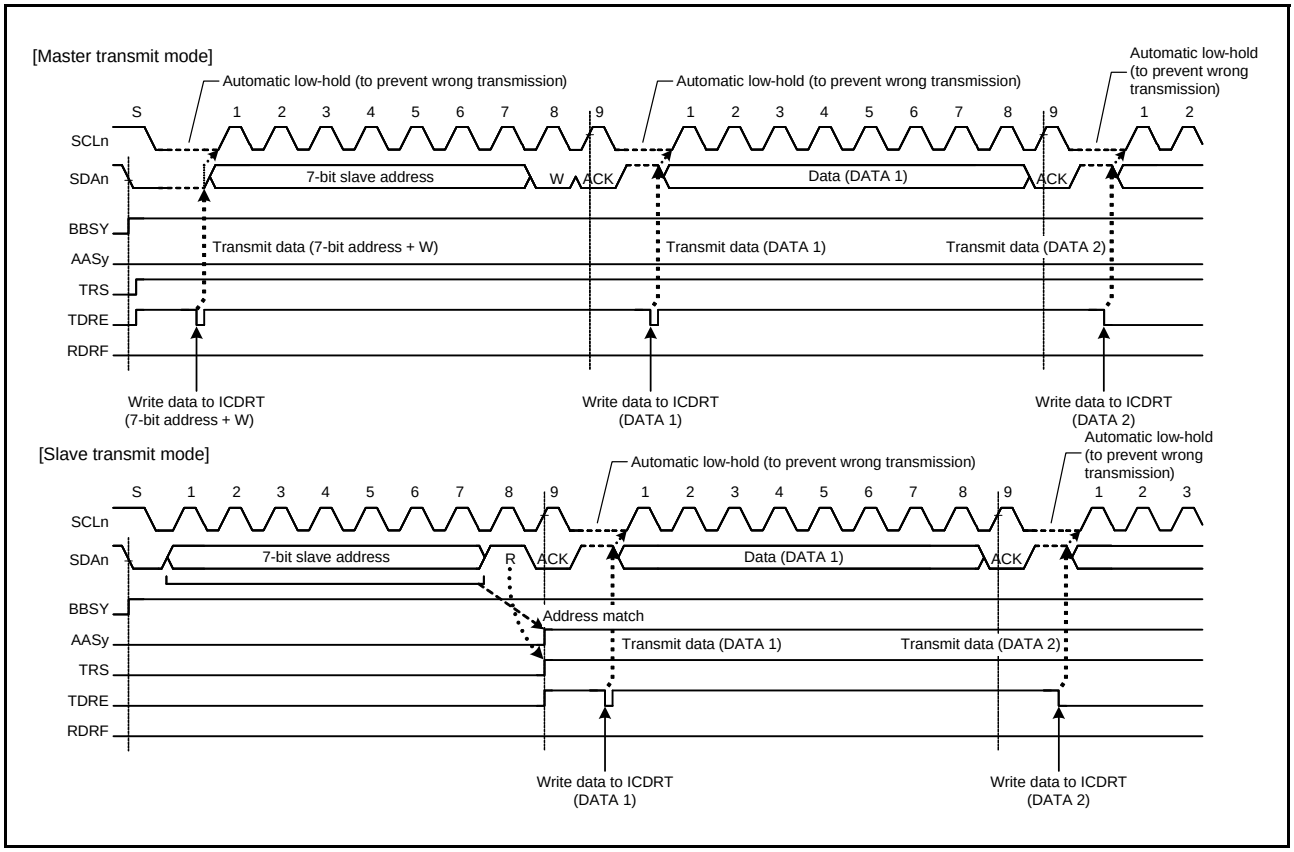


Figure 30.30 Automatic Low-Hold Operation in Transmit Mode

30.8.2 NACK Reception Transfer Suspension Function

The RIIC has a function to suspend transfer operation when NACK is received in transmit mode (TRS bit = 1 in ICCR2). This function is enabled when the NACKE bit in ICFER is set to 1 (transfer suspension enabled). If the next transmit data has already been written (TDRE flag = 0 in ICSR2) when NACK is received, next data transmission at the falling edge of the ninth SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (NACKF flag = 1 in ICSR2), transmit operation and receive operation are discontinued. To restore transmit/receive operation, be sure to clear the NACKF flag to 0. In master transmit mode, clear the NACKF flag to 0, issue a restart or stop condition, and then issue a start condition again.

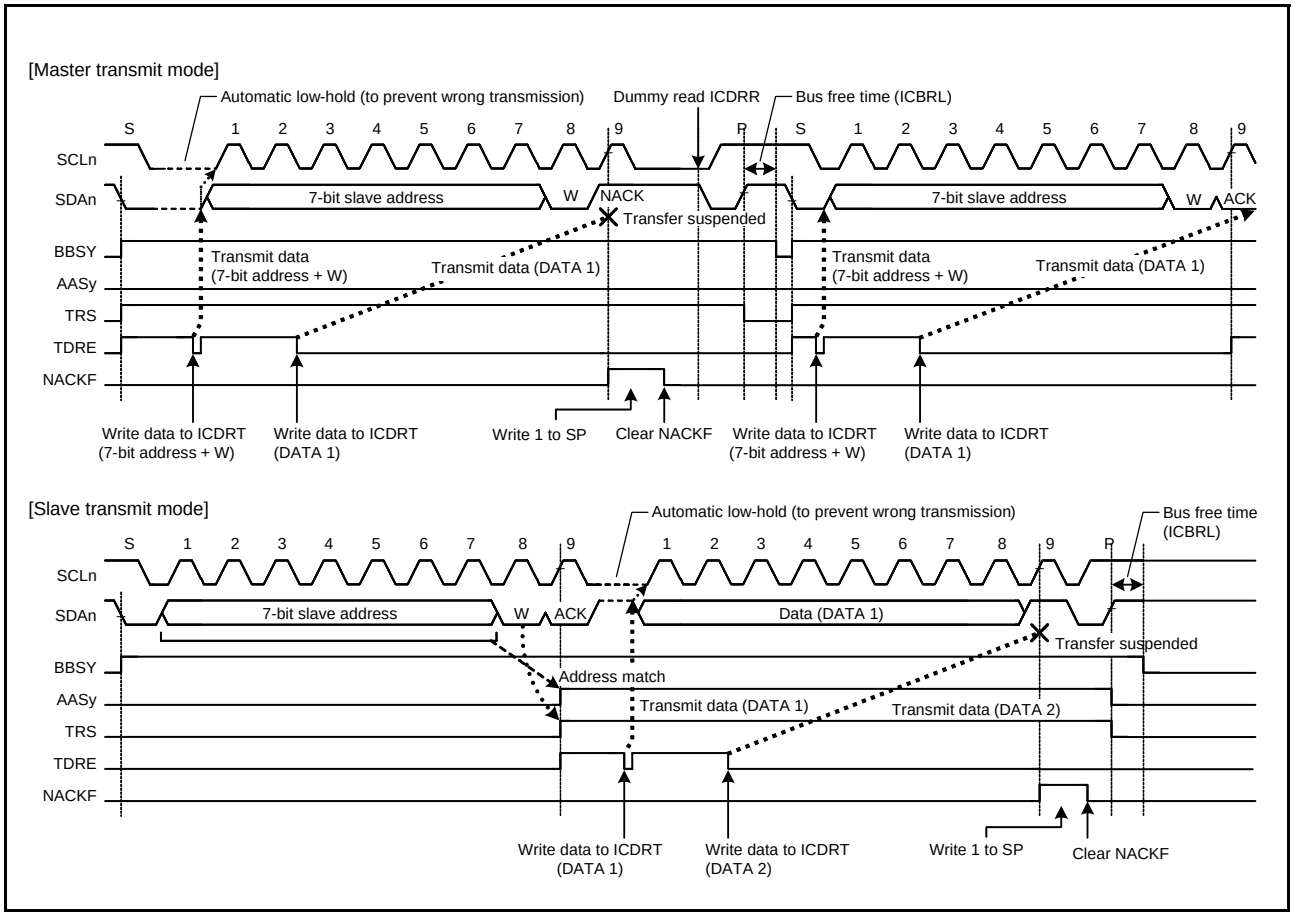


Figure 30.31 Suspension of Data Transfer when NACK is Received (NACKE = 1)

30.8.3 Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (RDRF flag = 1 in ICSR2) in receive mode (TRS = 0 in ICCR2), the RIIC holds the SCLn line low automatically immediately before the next data is received to prevent failure to receive data.

This function to prevent failure to receive data using the automatic low-hold function is also enabled even if the read processing of the final receive data is delayed and, in the meantime, the RIIC's own slave address is designated after a stop condition is issued. This function does not disturb other communication because the RIIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.

Sections in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in ICMR3.

(1) One-Byte Receive Operation and Automatic Low-Hold Function Using the WAIT Bit

When the WAIT bit in ICMR3 is set to 1, the RIIC performs one-byte receive operation using the WAIT bit function. Furthermore, when the ICMR3.RDRFS bit is 0, the RIIC automatically sends the ACKBT bit value in ICMR3 for the acknowledge bit in the period from the falling edge of the eighth SCL clock cycle to the falling edge of the ninth SCL clock cycle, and automatically holds the SCLn line low at the falling edge of the ninth SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from ICDRR, which enables bytewise receive operation.

The WAIT bit function is enabled for receive frames after a match with the RIIC's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

(2) One-Byte Receive Operation (ACK/NACK Transmission Control) and Automatic Low-Hold Function Using the RDRFS Bit

When the RDRFS bit in ICMR3 is set to 1, the RIIC performs one-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the RDRF flag (receive data full) in ICSR2 is set to 1 at the rising edge of the eighth SCL clock cycle, and the SCLn line is automatically held low at the falling edge of the eighth SCL clock cycle. This low-hold is released by writing a value to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation by the ACK/NACK transmission control according to the data received in byte units. The RDRFS bit function is enabled for receive frames after a match with the RIIC's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

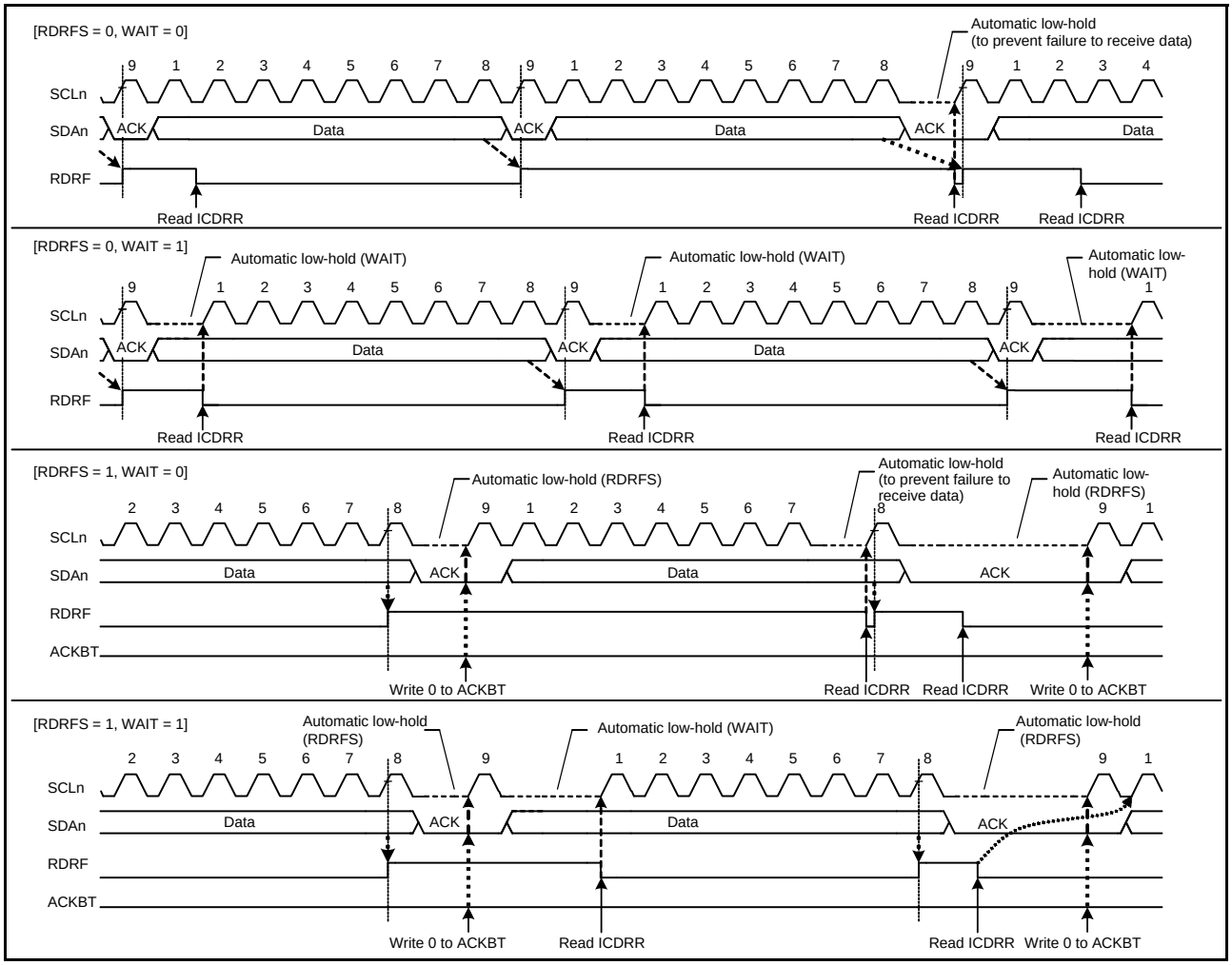


Figure 30.32 Automatic Low-Hold Operation in Receive Mode (Using RDRFS and WAIT Bits)

30.9 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I2C bus standard, the RIIC has functions to prevent double-issue of a start condition, to detect arbitration-lost during transmission of NACK, and to detect arbitration-lost in slave transmit mode.

30.9.1 Master Arbitration-Lost Detection (MALE Bit)

The RIIC drives the SDAn line low to issue a start condition. However, if the SDAn line has already been driven low by another master device issuing a start condition, the RIIC regards its own issuing of a start condition as an error and considers this a loss in arbitration, so priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY flag = 1 in ICCR2), the RIIC regards this as a double-issuing-of-start-condition error and considers itself to have lost in arbitration, thus preventing a failure of transfer due to issuing of a start condition while transfer is in progress.
When a start condition is issued successfully, if the data for transmission including the address bits (i.e. the internal SDA output level) and the level on the SDAn line do not match (the high output as the internal SDA output; i.e. the SDAn pin is in the high-impedance state) and the low level is detected on the SDA line, the RIIC loses in arbitration.
After a loss in arbitration of mastership, the RIIC immediately enters slave receive mode. If a slave address (including the general call address) matches its own address at this time, the RIIC continues in slave operation.
A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER is 1 (master arbitration-lost detection enabled).
[Master arbitration-lost conditions]

- Non-matching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ST bit in ICCR2 to 1 while the BBSY flag in ICCR2 was cleared to 0 (erroneous issuing of a start condition)
- Setting of the ST bit in ICCR2 to 1 (start condition double-issue error) while the BBSY flag is set to 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (MST and TRS bits = 11b in ICCR2)

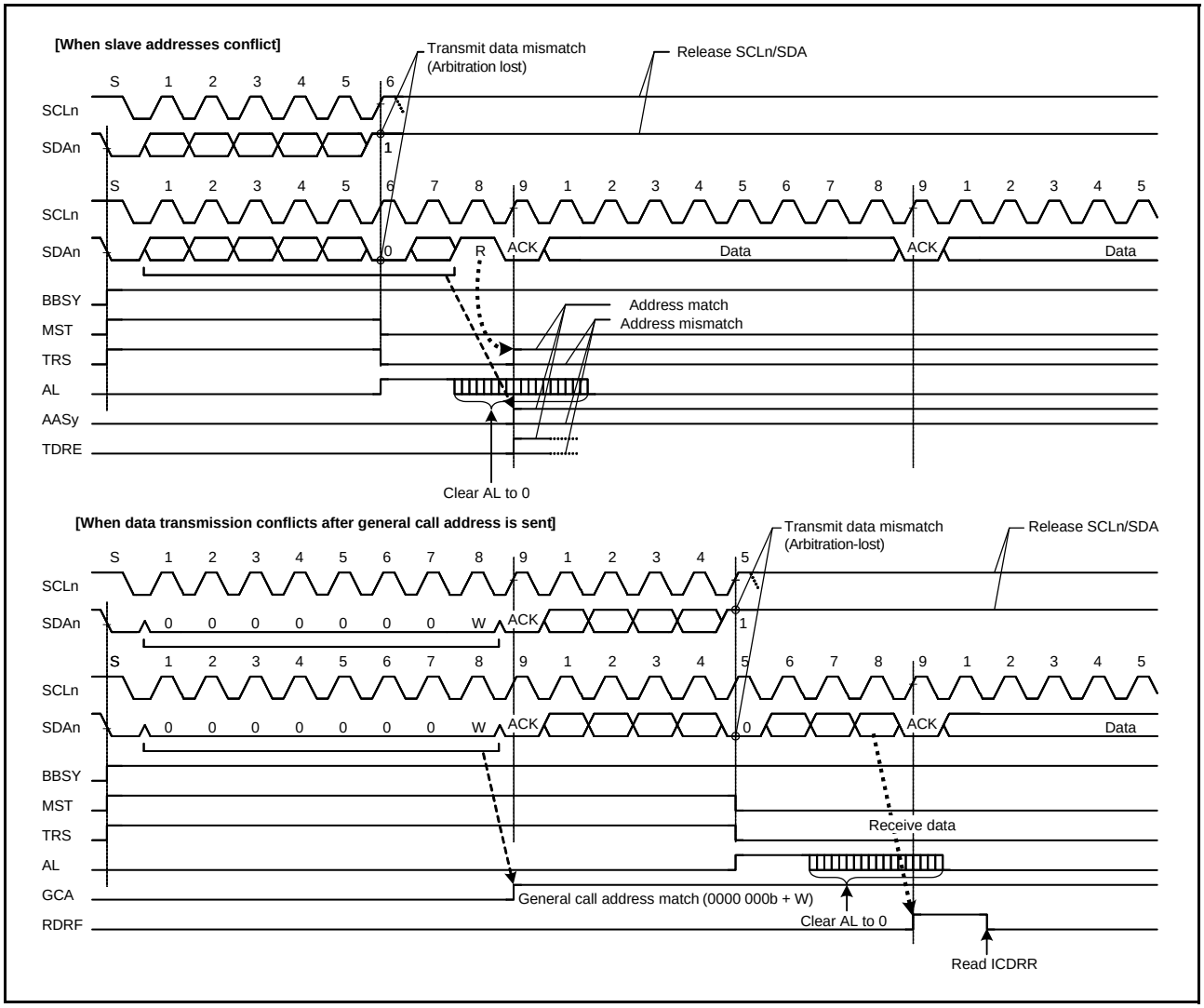


Figure 30.33 Examples of Master Arbitration-Lost Detection (MALE = 1)

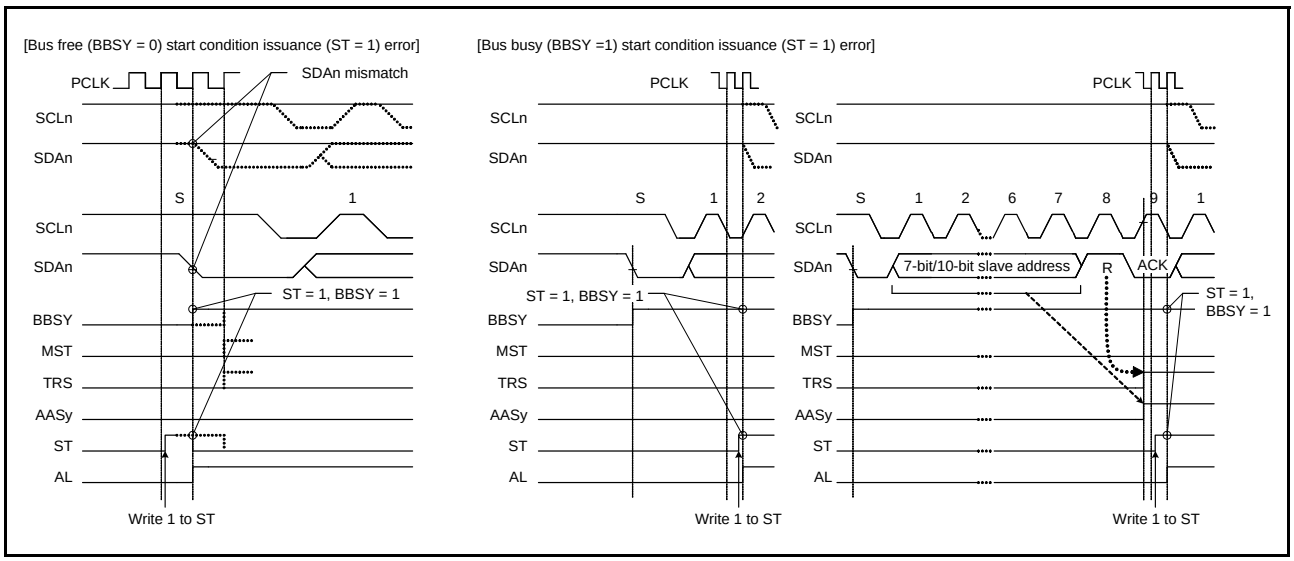


Figure 30.34 Arbitration-Lost when a Start Condition is Issued (MALE = 1)

30.9.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

The RIIC has a function to cause arbitration to be lost if the internal SDA output level does not match the level on the SDAn line (the high output as the internal SDA output; i.e. the SDAn pin is in the high-impedance state) and the low level is detected on the SDA line during transmission of NACK in receive mode. Arbitration is lost due to a conflict of NACK transmission and ACK transmission when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send/receive the same information through a single slave device. Figure 30.35 shows an example of arbitration-lost detection during transmission of NACK.

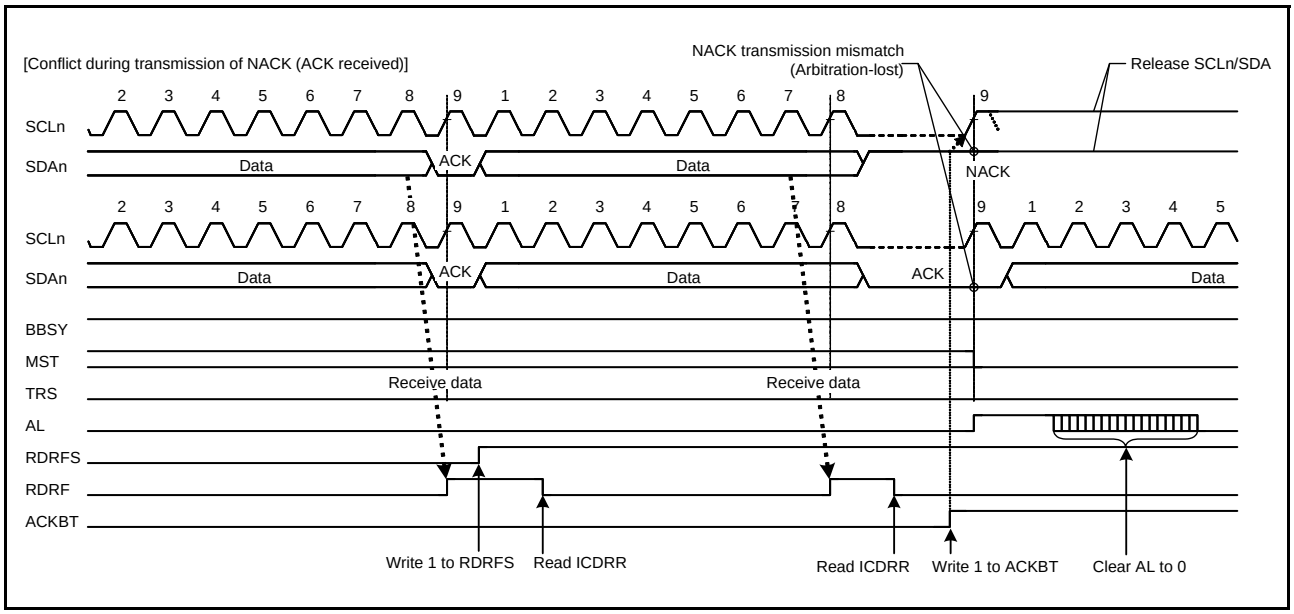


Figure 30.35 Example of Arbitration-Lost Detection during Transmission of NACK (NALE = 1)

The following explains arbitration-lost detection using an example where two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives two bytes of data from the slave device, and master B receives four bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in both master A and master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. Here, master A sends NACK when it has received two final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received necessary four bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like this occurs, master A cannot detect ACK transmitted by master B and issues a stop condition. Therefore, the issuance of the stop condition conflicts with the SCL clock output of master B, which disturbs communication.

When the RIIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost.

If arbitration is lost during transmission of NACK, the RIIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing (such as FFh transmission processing) necessary if the UDID (Unique Device Identifier) of assign address does not match in the Get UDID (general) processing after the Assign address command.

The RIIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKBT bit = 1 in ICMR3)

30.9.3 Slave Arbitration-Lost Detection (SALE Bit)

The RIIC has a function to cause arbitration to be lost if the data for transmission (i.e. the internal SDA output level) and the level on the SDAn line do not match (the high output as the internal SDA output; i.e. the SDAn pin is in the high-impedance state) and the low level is detected on the SDA line in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.
When it loses slave arbitration, the RIIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminates subsequent redundant processing (processing for the transmission of FFh).
The RIIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmit mode (MST and TRS bits = 01b in ICCR2)

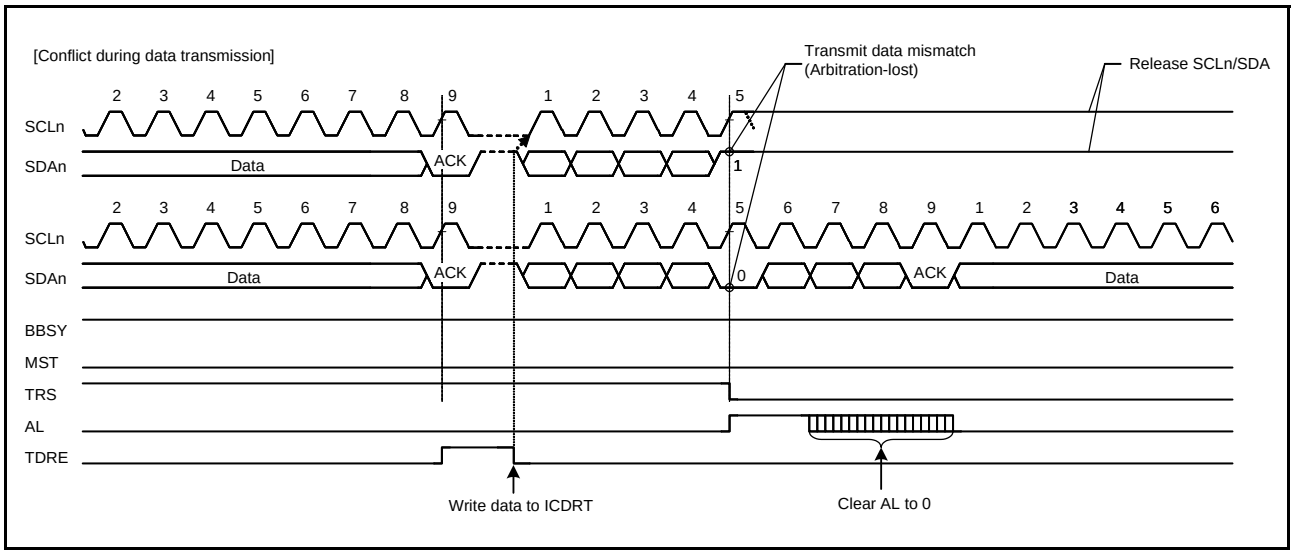


Figure 30.36 Example of Slave Arbitration-Lost Detection (SALE = 1)

30.10 Start Condition/Restart Condition/Stop Condition Issuing Function

30.10.1 Issuing a Start Condition

The RIIC issues a start condition when the ST bit in ICCR2 is set to 1.
When the ST bit is set to 1, a start condition issuance request is made and the RIIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free). When a start condition is issued normally, the RIIC automatically shifts to the master transmit mode.
A start condition is issued in the following sequence.

[Start condition issuance]
(1) Drive the SDAn line low (high level to low level).
(2) Ensure the time set in ICBRH and the start condition hold time.
(3) Drive the SCLn line low (high level to low level).
(4) Detect low level of the SCLn line and ensure the low-level period of SCLn line set in ICBRL.

30.10.2 Issuing a Restart Condition

The RIIC issues a restart condition when the RS bit in ICCR2 is set to 1.
When the RS bit is set to 1, a restart condition issuance request is made and the RIIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy) and the MST bit in ICCR2 is 1 (master mode).
A restart condition is issued in the following sequence.

[Restart condition issuance]
(1) Release the SDAn line.
(2) Ensure the low-level period of SCLn line set in ICBRL.
(3) Release the SCLn line (low level to high level).
(4) Detect a high level of the SCLn line and ensure the time set in ICBRL and the restart condition setup time.
(5) Drive the SDAn line low (high level to low level).
(6) Ensure the time set in ICBRH and the restart condition hold time.
(7) Drive the SCLn line low (high level to low level).
(8) Detect a low level of the SCLn line and ensure the low-level period of SCLn line set in ICBRL.

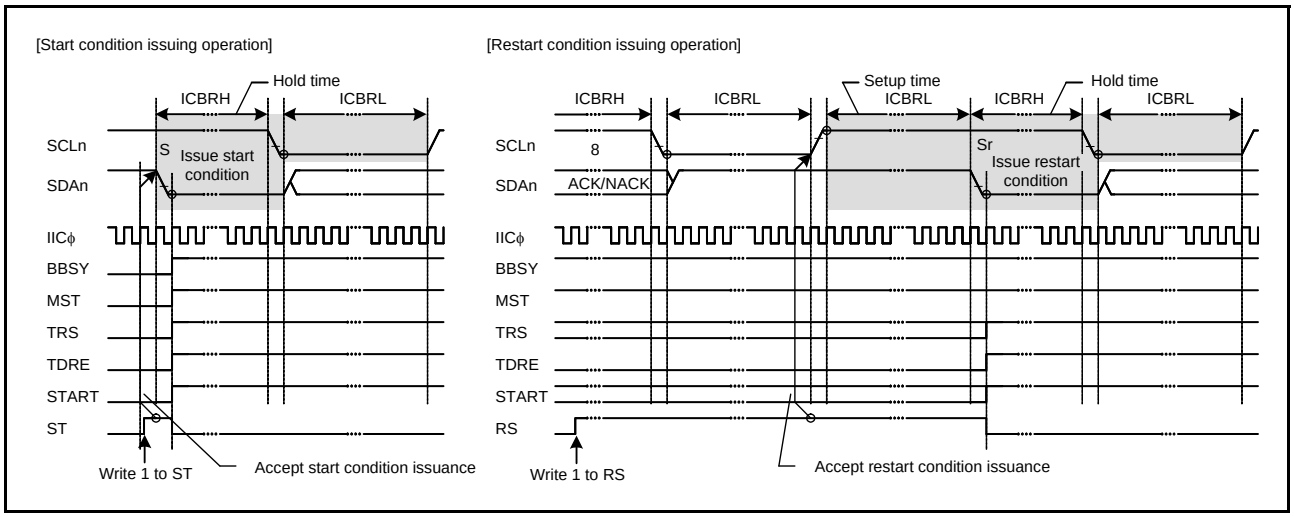


Figure 30.37 Start Condition/Restart Condition Issue Timing (ST and RS Bits)

30.10.3 Issuing a Stop Condition

The RIIC issues a stop condition when the SP bit in ICCR2 is set to 1.
When the SP bit is set to 1, a stop condition issuance request is made and the RIIC issues a stop condition when the BBSY flag in ICCR2 is 1 (bus busy) and the MST bit in ICCR2 is 1 (master mode).
A stop condition is issued in the following sequence.

[Stop condition issuance]

- Drive the SDAn line low (high level to low level).
- Ensure the low-level period of SCLn line set in ICBRL.
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the time set in ICBRH and the stop condition setup time.
- Release the SDAn line (low level to high level).
- Ensure the time set in ICBRL and the bus free time.
- Clear the BBSY flag to 0 (to release the bus mastership).

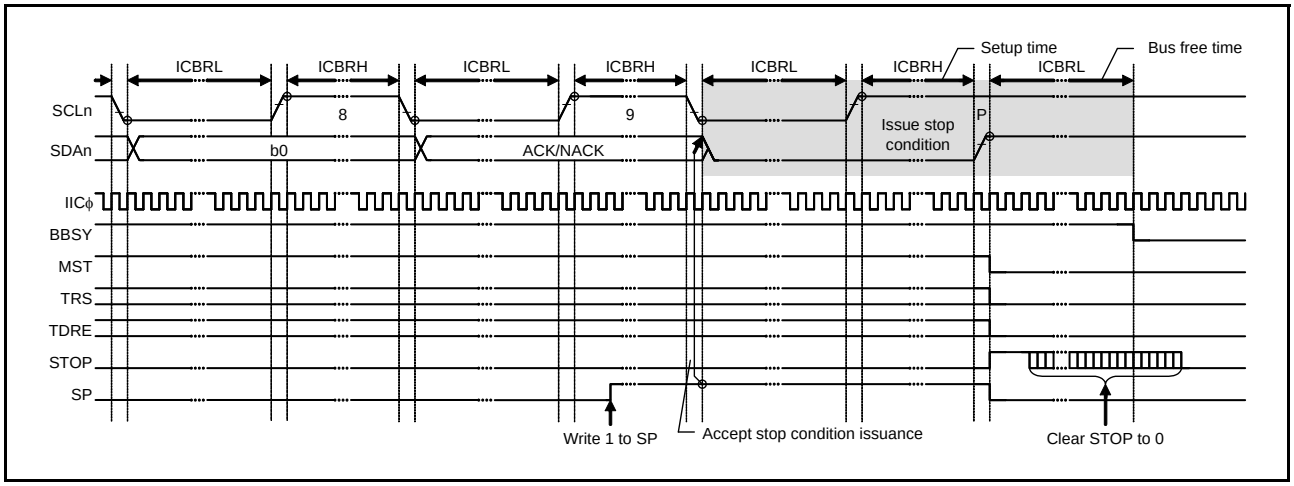


Figure 30.38 Stop Condition Issue Timing (SP Bit)

30.11 Bus Hanging

If the clock signals from the master and slave devices go out of synchronization due to noise or other factors, the I2C bus might hang with a fixed level on the SCLn line and/or SDAn line.
As measures against the bus hanging, the RIIC has a timeout function to detect hanging by monitoring the SCLn line, a function for the output of an extra SCL clock cycle to release the bus from a hung state due to clock signals being out of synchronization, and the RIIC/internal reset function.
By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to see whether the RIIC or its partner in communications is placing the low level on the SCLn or SDAn lines.

30.11.1 Timeout Function

The RIIC has the timeout function to detect an abnormality that the SCLn line is held for a certain period of time. The RIIC can detect an abnormal bus state by monitoring that the SCLn line is held low or high for a predetermined time. The timeout function monitors the SCLn line state and counts the low-level period or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rising or falling), but continues to count unless the SCLn line changes. If the internal counter overflows due to no SCLn line change, the RIIC can detect the timeout and report the bus abnormality.

This timeout function is enabled when the TMOE bit in ICFER is 1. It detects bus hanging on the SCL0n line fixed at low or high during the following period.

- In master mode (ICCR2.MST = 1) and bus busy (ICCR2.BBSY = 1)
- In slave mode (ICCR2.MST = 1), own slave address matched (ICSR2 00h), and bus busy (ICCR2.BBSY = 1)
- Issue of start condition is requested (ICCR2.ST = 1) and bus free (ICCR2.BBSY = 0)

The internal counter of the timeout function works using the internal reference clock (IICϕ) set by the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (TMOS bit = 0 in ICMR2) or a 14-bit counter when short mode is selected (TMOS bit = 1).

The SCLn line level (low/high or both levels) during which this counter is activated can be selected by the setting of the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are cleared to 0, the internal counter does not work.

Note: • When using the timeout detect function, see section 30.2.4, I2C Bus Mode Register 2 (ICMR2), section 30.2.18, Timeout Internal Counter (TMOCNT), and section 30.3.2, Initial Settings.

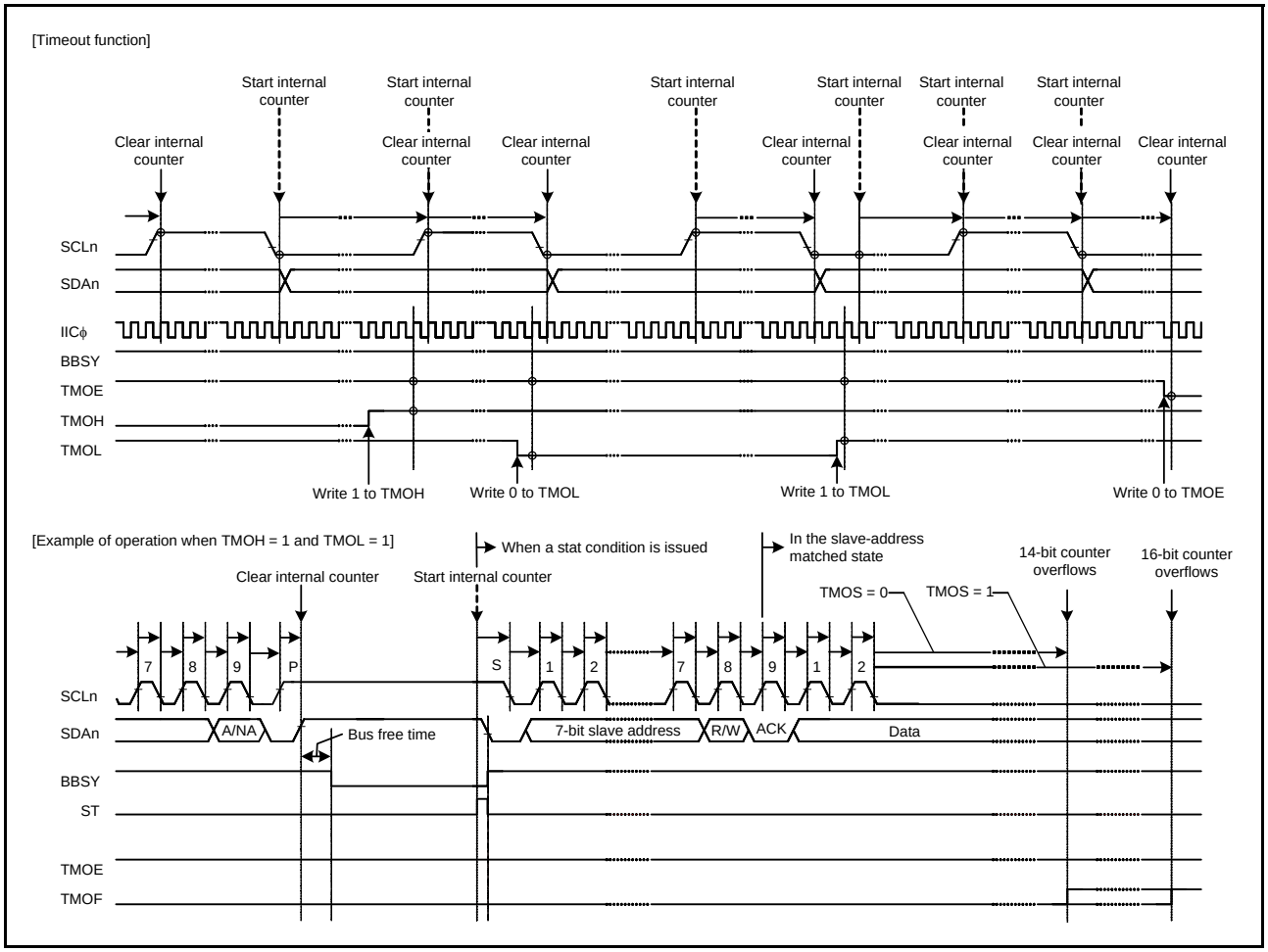


Figure 30.39 Timeout Function (TMOE, TMOS, TMOH, and TMOL Bits)

30.11.2 Extra SCL Clock Cycle Output Function

In master mode, the RIIC module has a facility for the output of extra SCL (clock) cycles to release the SDAn line of the slave device from being held at the low level due to the master being out of synchronization with the slave device.
This function is mainly used in master mode to release the SDAn line of the slave device from the state of being fixed to the low level by including extra cycles of SCLn output from the RIIC with single cycles of the SCL (clock) signal as the unit in the case of a bus error where the RIIC cannot issue a stop condition because the slave device is holding the SDAn line at the low level. Do not use this facility in normal situations. Using it when communications are proceeding correctly will lead to malfunctions.
When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the frequency corresponding to the transfer rate settings (settings of the CKS[2:0] bits in ICMR1, and of the ICBRH and ICBRL registers) is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit is automatically cleared to 0. Therefore, further extra clock cycles can be output consecutively by the software program writing 1 to the CLO bit after having read CLO = 0.
When the RIIC module is in master mode and the slave device is holding the SDAn line at the low level because synchronization with the slave device has been lost due to the effects of noise, etc., the output of a stop condition is not possible. The facility for output of an extra cycle of the SCL (clock) signal can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held at the low level, thus recovering the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming release of the SDAn line by the slave device, complete communications by reissuing the stop condition.
Use this facility with the MALE bit (master arbitration-lost detection disabled) in ICFER cleared to 0. If the MALE bit is set to 1 (master arbitration-lost detection enabled), arbitration is lost when the value of the SDAO bit in ICCR1does not match the state of the SDAn line, so take care on this point.

[Output conditions for using the CLO bit in ICCR1]

- When the bus is free (BBSY flag in ICCR2 = 0) or in master mode (MST bit = 1 and BBSY flag = 1 in ICCR2)
- When the communication device does not hold the SCLn line low

Figure 30.40 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

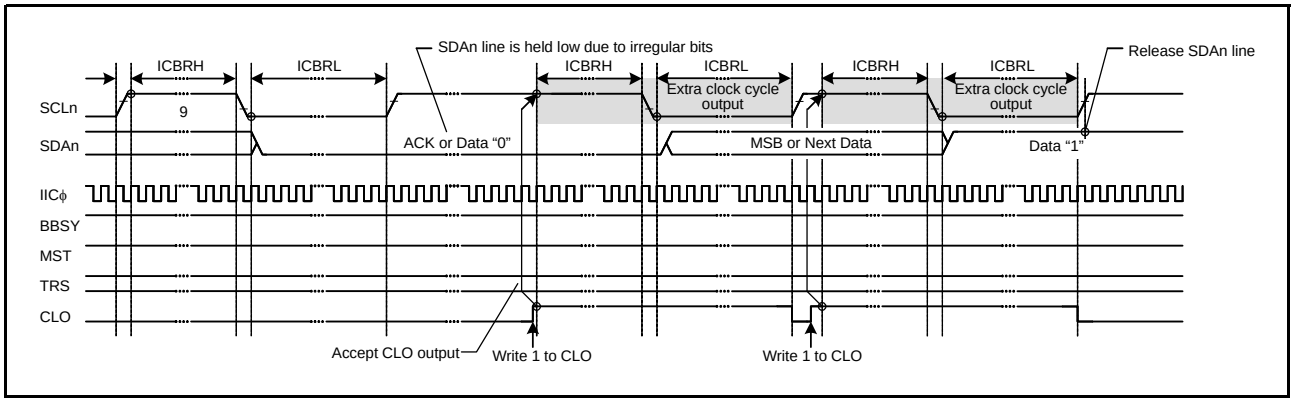


Figure 30.40 Extra SCL Clock Cycle Output Function (CLO Bit)

30.11.3 RIIC Reset and Internal Reset

The RIIC module incorporates a function for resetting itself. There are two types of reset. One is referred to as an RIIC reset; this initializes all registers including the BBSY flag in ICCR2. The other is referred to as an internal reset; this releases the RIIC from the slave-address matched state and initializes the internal counter while retaining other settings. After issuing a reset, be sure to clear the IICRST bit in ICCR1 to 0.
Both types of reset are effective for release from bus-hung states since both restore the output state of the SCLn and SDAn pins to the high impedance state.
Issuing a reset during slave operation may lead to a loss of synchronization between the master device clock and the slave device clock, so avoided this where possible. Note that monitoring of the bus state, such as for the presence of a start condition, is not possible during an RIIC reset (ICE and IICRST bits = 01b in ICCR1).
For a detailed description of the RIIC and internal resets, see section 30.14, Reset States.

30.12 SMBus Operation

The RIIC is available for data communication conforming to the SMBus (Version 2.0). To perform SMBus communication, set the SMBS bit in ICMR3 to 1. To use the transfer rate within a range of 10 kbps to 100 kbps of the SMBus standard, set the CKS[2:0] bits in ICMR1, ICBRH, and ICBRL. In addition, determine the values of the DLCS bit in ICMR2 and the SDDL[2:0] bits in ICMR2 to meet the data hold time specification of 300 ns or more. If the RIIC is used only as a slave device, the transfer rate setting is not necessary. When the RIIC is used only as a slave device, the transfer rate setting is not necessary, whereas the ICBRL needs to be set to a value longer than the data setup time (250 ns).
For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (SARL0, SARL1, and SARL2), and set the corresponding FS bit (7-bit/10-bit address format select) in SARUy (y = 0 to 2) to 0 (7-bit address format).
When transmitting the UDID (Unique Device Identifier), set the SALE bit in ICFER to 1 to enable the slave arbitration-lost detection function.

30.12.1 SMBus Timeout Measurement

(1) Measuring timeout of slave device

The following period (timeout interval: $T_{LOW:\,SEXT}$) must be measured for slave devices in SMBus communication.

- From start condition to stop condition

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with the timer using a start condition detection interrupt (STI) and stop condition detection interrupt (SPI) of the RIIC. The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW:\,SEXT}$: 25 ms (max.) of the SMBus standard.
If the time measured with the timer exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus standard, the slave device must release the bus by writing 1 to the IICRST bit in ICCR1 to issue an internal reset of the RIIC. When an internal reset is issued, the RIIC stops driving the bus for the SCLn pin and SDAn pin and make the SCLnn/SDAn pin outputs high impedance, which releases the bus.

(2) Measuring timeout of master device

The following periods (timeout interval: TLOW: MEXT) must be measured for master devices in SMBus communication.

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition

To measure timeout for master devices, measure these periods with the timer using a start condition detection interrupt (STI), stop condition detection interrupt (SPI), and transmit end interrupt (ICTEI) or receive data full interrupt (ICRXI) of the RIIC. The measured timeout period must be within the total clock low-level extended period [master device] $T_{LOW: MEXT}$: 10 ms (max.) of the SMBus standard, and the total of all $T_{LOW: MEXT}$ from start condition to stop condition must be within $T_{LOW: SEXT}$: 25 ms (max.).

For the ACK receive timing (rising edge of the ninth SMBCLK clock cycle), monitor the TEND flag in ICSR2 in master transmit mode (master transmitter) and the RDRF flag in ICSR2 in master receive mode (master receiver). For this reason, perform bytewise transmit operation in master transmit mode, and hold the RDRFS bit in ICMR3 0 until the byte just before reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 at the rising edge of the ninth SMBCLK clock cycle.

If the period measured with the timer exceeds the total clock low-level extended period [master device] $T_{LOW: MEXT}$: 10 ms (max.) of the SMBus standard or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus standard, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (writing data to ICDRT).

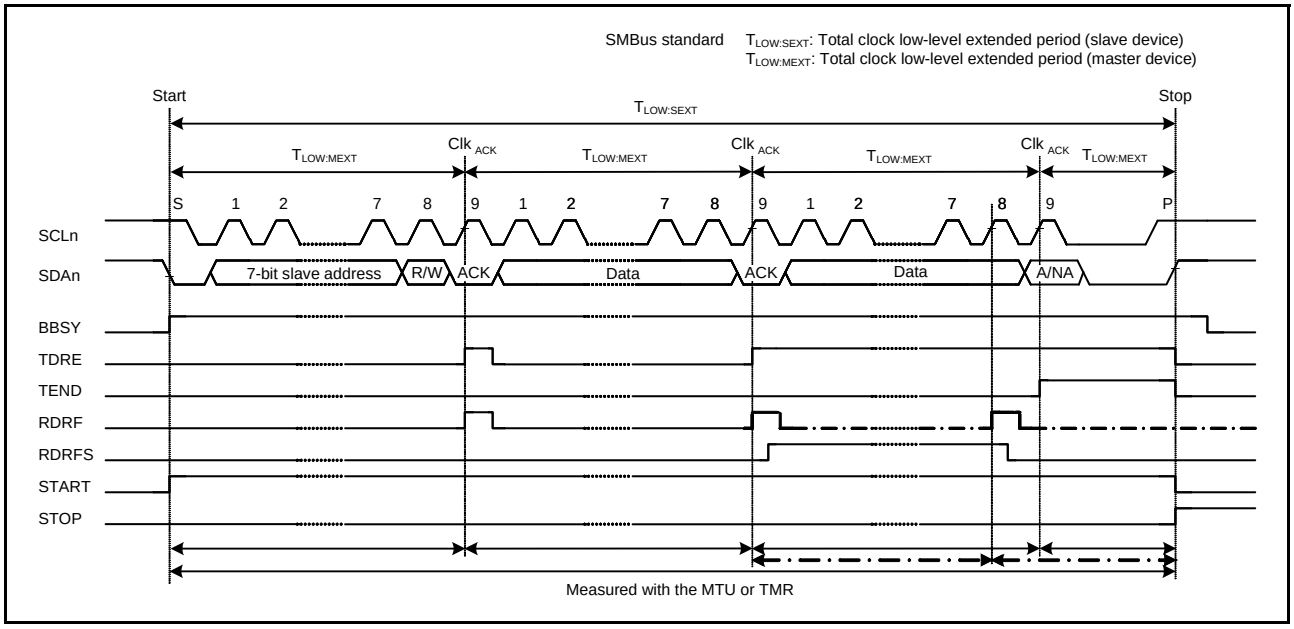


Figure 30.41 SMBus Timeout Measurement

30.12.2 Packet Error Code (PEC)

This MCU incorporates a CRC calculator. The CRC calculator enables transmission of a packet error code (PEC) or checking the received data of the SMBus in data communication of the RIIC. For the CRC generating polynomials of the CRC calculator, see section 33, CRC Calculator (CRC).

The PEC data in master transmit mode (master transmitter) can be generated by writing all transmit data to the CRC data input register (CRCDIR) in the CRC calculator.

The PEC data in master receive mode (master receiver) can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC data output register (CRCDOR) with the received PEC data.

To send ACK or NACK according to the match or mismatch result when the final byte is received as a result of the PEC code check, set the RDRFS bit in ICMR3 to 1 before the rising edge of the eighth SMBCLK clock cycle during reception of the final byte, and hold the SCLn line low at the falling edge of the eighth clock cycle.

30.12.3 SMBus Host Notification Protocol/Notify ARP Master

In communications over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of (or request the SMBus host for) its own slave address or to request its own slave address from the SMBus host.

For a product of this MCU to operate as an SMBus host (or ARP master), the host address (0001 000b) sent from the slave device must be detected as a slave address, so the RIIC has a function for detecting the host address. To detect the host address as a slave address, set the SMBS bit in ICMR3 and the HOAE bit in ICSER to 1. Operation after the host address has been detected is the same as normal slave operation.

30.13 Interrupt Request

The RIIC issues four types of interrupt request: transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start condition detection, and stop condition detection), receive end, transmit data empty, and transmit end.

Table 30.7 lists details of the several interrupt requests. The receive data full and transmit data empty are both capable of launching data transfer by the DTC or DMAC.

Table 30.7 Interrupt Sources

Symbol	Interrupt Source	Interrupt Flag	DTC Launching	DMACA Launching	Priority	Interrupt Condition
EEI	Transfer Error/ Event Generation	AL	Not possible	Not possible	High	AL = 1 • ALIE = 1
		NACKF				NACKF = 1 • NAKIE = 1
		TMOF				TMOF = 1 • TMOIE = 1
		START				START = 1 • STIE = 1
		STOP				STOP = 1 • SPIE = 1
RXI	Receive End	—	Possible	Possible		RDRF = 1 • RIE = 1
TXI	Transmit Data Empty	—	Possible	Possible		TDRE = 1 • TIE = 1
TEI	Transmit End	TEND	Not possible	Not possible	Low	TEND = 1 • TEIE = 1

Clear or mask the each flag during interrupt handling.

Notes on interrupt processing:

1. There is a latency (delay) between the execution of a write instruction for a peripheral module by the CPU and actual writing to the module. Thus, when an interrupt flag has been cleared or masked, read the relevant flag again to check whether clearing or masking has been completed, and then return from interrupt processing. Returning from interrupt processing without checking that writing to the module has been completed creates a possibility of repeated processing of the same interrupt.
2. Since ICTXI is an edge-detected interrupted, it does not require clearing. Furthermore, the TDRE flag in ICSR2 (a condition for ICTXI) is automatically cleared to 0 when data for transmission are written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).
3. Since ICRXI is an edge-detected interrupted, it does not require clearing. Furthermore, the RDRF flag in ICSR2 (a condition for ICRXI) is automatically cleared to 0 when data are read from ICDRR.
4. When using the ICTEI interrupt, clear the TEND flag in ICSR2 in the ICTEI interrupt processing.
   Note that the TEND flag in ICSR2 is automatically cleared to 0 when data for transmission are written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).

30.13.1 Buffer Operation for ICTXI and ICRXI Interrupts

For the ICTXI and ICRXI interrupts, as well as the ICU.IRn.IR flag having the value 1 being a condition for issuing the interrupts, the interrupt request is retained within and not output by the ICU (the capacity for internally retaining the interrupts is one request per source).

An interrupt request that was being retained within the ICU is output when the value of the ICU.IRn.IR flag becomes 0.

Internally retained interrupt requests are automatically cleared under normal conditions of usage.

Internally retained interrupt requests can also be cleared by writing 0 to the interrupt enable bit within the given peripheral module.

30.14 Reset States

The RIIC has chip reset, RIIC reset, and internal reset functions. Table 30.8 lists the scope of each reset and reset conditions.

Table 30.8 Reset Conditions

		Chip Reset	RIIC Reset (ICE = 0, IICRST = 1)	Internal Reset (ICE = 1, IICRST = 1)	Start Condition/ Restart Condition Detection	Stop Condition Detection
ICCR1	ICE, IICRST	At a reset	Retained	Retained	Operation (retained)	Operation (retained)
	SCLO, SDAO		At a reset	At a reset		
	Others			Retained		
ICCR2	BBSY	At a reset	At a reset	Operation	Operation	Operation
	ST			At a reset	At a reset	Operation (retained)
	Others					At a reset
ICMR1	BC[2:0]	At a reset	At a reset	At a reset	At a reset	Operation (retained)
	Others			Retained	Operation (retained)	
ICMR2		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICMR3		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICFER		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICSER		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICIER		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICSR1		At a reset	At a reset	At a reset	Operation (retained)	At a reset
ICSR2	TDRE, TEND	At a reset	At a reset	At a reset	Operation (retained)	At a reset
	START				Operation	
	STOP				Operation (retained)	Operation
	Others					Operation (retained)
SARL0, 1, 2 SARU0, 1, 2		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICBRH, ICBRL		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICDRT		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICDRR		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICDRS		At a reset	At a reset	At a reset	Operation (retained)	Operation (retained)
Timeout function		At a reset	At a reset	Operation	Operation	Operation
Bus free time measurement		At a reset	At a reset	Operation	Operation	Operation

30.15 Usage Notes

30.15.1 Setting Module-Stop Function

Module-stop control register B (MSTPCRB) enables and disables RIIC operation. RIIC is stopped at the initial value. Register access is enabled by clearing module-stop state. For details of the module stop control register B, see section 12, Low Power Consumption.

30.15.2 Points to Note on Starting Transfer

If the ICU.IRn.IR flag is 1 at the time transfer is to be started (by setting the ICCR1.ICE bit to 1), follow the procedure below to clear interrupts before enabling operations. Starting transfer with the ICU.IRn.IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally retained after transfer starts, and this can lead to unanticipated behavior of the ICU.IRn.IR flag.

(1) Confirm that the ICCR1.ICE bit is 0.
(2) Clear the relevant interrupt enable bits (ICIER.TIE, etc.) on the peripheral function side to 0.
(3) Read the relevant interrupt enable bits (ICIER.TIE, etc.) on the peripheral function side and confirm that its value is 0.
(4) Clear the ICU.IRn.IR flag to 0.

31. CAN Module (CAN)

31.1 Overview

The RX63T Group implements three channels of the CAN (Controller Area Network) module that complies with the ISO11898-1 Specifications. The CAN module transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier is hereafter referred to as ID) and extended ID (29 bits).
Table 31.1 lists the specifications of the CAN module, and Figure 31.1 shows a block diagram of the CAN module (i = 1).
Connect the CAN bus transceiver externally.

Table 31.1 Specifications of CAN Module

Item	Description
Protocol	• ISO11898-1 compliant (standard and extended frames)
Bit rate	• Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	• 32 mailboxes: Two selectable mailbox modes Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.
Transmission	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	• Mode transition for the recovery from the bus-off state can be selected: ISO11898-1 Specifications compliant Automatic entry to CAN halt mode at bus-off entry Automatic entry to CAN halt mode at bus-off end Entry to CAN halt mode by a program Transition into error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	• Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)
CAN sleep mode	• Current consumption can be reduced by stopping the CAN clock.
Software support unit	• Three software support units: Acceptance filter support Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) Channel search support
CAN clock source	Peripheral module clock (PCLK) or CANMCLK
Test mode	• Three test modes available for user evaluation Listen-only mode Self-test mode 0 (external loopback) Self-test mode 1 (internal loopback)
Power consumption reducing function	Module-stop state can be set.

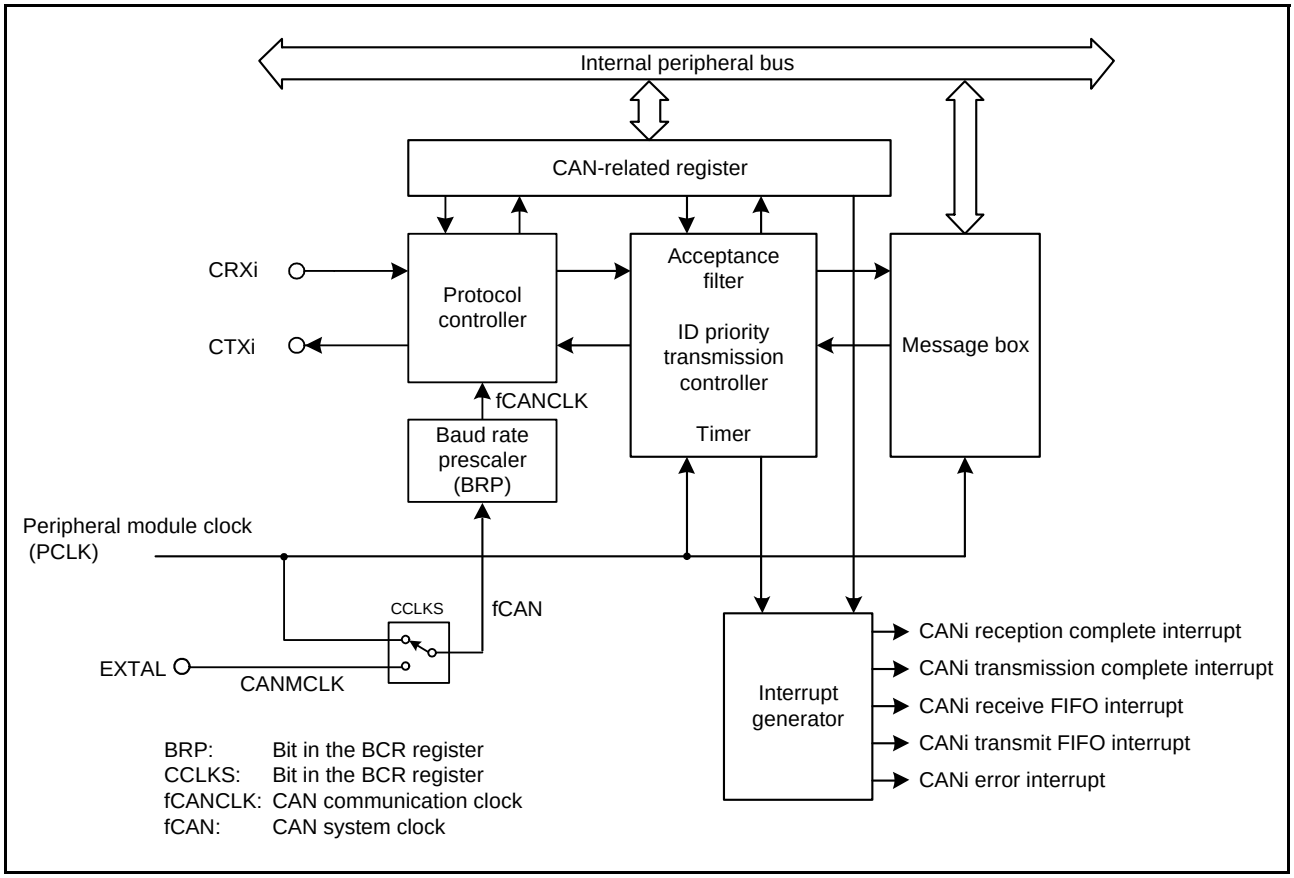


Figure 31.1 Block Diagram of CAN Module (i = 1)

- CRXi and CTXi (i = 1)
  CAN input and output pins
- Protocol controller
  Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Message box
  Consists of 32 mailboxes which can be configured as either transmit or receive mailboxes. Each mailbox has an individual ID, data length code, a data field (8 bytes), and a time stamp.
- Acceptance filter
  Performs filtering of received messages. MKR0 to MKR7 are used for the filtering process.
- Timer
  Used for the time stamp function. The timer value when a message is stored into the mailbox is written as the time stamp value.
- Interrupt generator:
  Generates the following five types of interrupts:
  CANi reception complete interrupt
  CANi transmission complete interrupt
  CANi receive FIFO interrupt
  CANi transmit FIFO interrupt
  CANi error interrupt

Table 31.2 lists the CAN module pins.
The CAN functions should be selected for the pins multiplexed with other signals. For details, see section 20, I/O Ports.

Table 31.2 Pin Configuration

Pin Name	I/O	Function
CRX1	Input	Pin for receiving data
CTX1	Output	Pin for transmitting data

31.2 Register Descriptions

31.2.1 Control Register (CTLR)

Address(es): CAN1.CTLR 0009 1840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MBM	CAN Mailbox Mode Select*1	0: Normal mailbox mode 1: FIFO mailbox mode	R/W
b2, b1	IDFM[1:0]	ID Format Mode Select*1	b2 b1 0 0: Standard ID mode All mailboxes (including FIFO mailboxes) handle only standard Ids. 0 1: Extended ID mode All mailboxes (including FIFO mailboxes) handle only extended IDs. 1 0: Mixed ID mode All mailboxes (including FIFO mailboxes) handle both standard IDs and extended IDs. Standard IDs or extended IDs are specified by using the IDE bit in the corresponding mailbox in normal mailbox mode. In FIFO mailbox mode, the IDE bit in the corresponding mailbox is used for mailboxes [0] to [23], the IDE bits in FIDCR0 and FIDCR1 are used for the receive FIFO, and the IDE bit in mailbox [24] is used for the transmit FIFO. 1 1: Do not use this combination	R/W
b3	MLM	Message Lost Mode Select*2	0: Overwrite mode 1: Overrun mode	R/W
b4	TPM	Transmission Priority Mode Select*2	0: ID priority transmit mode 1: Mailbox number priority transmit mode	R/W
b5	TSRC	Time Stamp Counter Reset Command*4	0: Nothing occurred 1: Reset*3	R/W
b7, b6	TSPS[1:0]	Time Stamp Prescaler Select*1	b7 b6 0 0: Every bit time 0 1: Every 2-bit time 1 0: Every 4-bit time 1 1: Every 8-bit time	R/W
b9, b8	CANM[1:0]	CAN Operating Mode Select*5	b9 b8 0 0: CAN operation mode 0 1: CAN reset mode 1 0: CAN halt mode 1 1: CAN reset mode (forcible transition)	R/W
b10	SLPM	CAN Sleep Mode*5,*6	0: Other than CAN sleep mode 1: CAN sleep mode	R/W

Bit	Symbol	Bit Name	Description	R/W
b12, b11	BOM[1:0]	Bus-Off Recovery Mode*1	b12 b11 0 0: Normal mode (ISO11898-1 compliant) 0 1: Entry to CAN halt mode automatically at bus-off entry 1 0: Entry to CAN halt mode automatically at bus-off end 1 1: Entry to CAN halt mode (during bus-off recovery period) by a program request	R/W
b13	RBOC	Forcible Return From Bus-Off*2	0: Nothing occurred 1: Forcible return from bus-off*3	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Write to the BOM[1:0], TSPS[1:0], TPM, MLM, IDFM[1:0], and MBM bits in CAN reset mode.
Note 2. Set the RBOC bit to 1 in the bus-off state.
Note 3. This bit is automatically set back to 0 after being set to 1. It should be read as 0.
Note 4. Set the TSRC bit to 1 in CAN operation mode.
Note 5. When the CANM[1:0] and SLPM bits are changed, check STR to ensure that the mode has been switched. Do not change the CANM[1:0] bits or SLPM bit until the mode has been switched.
Note 6. Write to the SLPM bit in CAN reset mode or CAN halt mode. When changing the SLPM bit, write 0 or 1 to only the SLPM bit.

MBM Bit (CAN Mailbox Mode Select)

When the MBM bit is 0 (normal mailbox mode), mailboxes [0] to [31] are configured as transmit or receive mailboxes.
When the MBM bit is 1 (FIFO mailbox mode), mailboxes [0] to [23] are configured as transmit or receive mailboxes. Mailboxes [24] to [27] are configured as a transmit FIFO and mailboxes [28] to [31] as a receive FIFO.
Transmit data is written into mailbox [24] (mailbox [24] is a window mailbox for the transmit FIFO). Receive data is read from mailbox [28] (mailbox [28] is a window mailbox for the receive FIFO).
Table 31.3 lists the mailbox configuration.

IDFM[1:0] Bits (ID Format Mode Select)

The IDFM[1:0] bits specify the ID format.

MLM Bit (Message Lost Mode Select)

The MLM bit specifies the operation when a new message is captured in the unread mailbox. Overwrite mode or overrun mode can be selected. All mailboxes (including the receive FIFO) are set to either overwrite mode or overrun mode.
When the MLM bit is 0, all mailboxes are set to overwrite mode and the new message is overwriting the old message.
When the MLM bit is 1, all mailboxes are set to overrun mode and the new message is discarded.

TPM Bit (Transmission Priority Mode Select)

The TPM bit specifies the priority of modes when transmitting messages.
ID priority transmit mode or mailbox number transmit mode can be selected. All mailboxes are set for either ID priority transmission or mailbox number priority transmission.
When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO11898-1 Specifications. In ID priority transmit mode, mailboxes [0] to [31] (in normal mailbox mode), and mailboxes [0] to [23] (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.
Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a transmit FIFO message is being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.

When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (mailboxes [0] to [23]).

TSRC Bit (Time Stamp Counter Reset Command)

The TSRC bit is used to reset the time stamp counter. When the TSRC bit is set to 1, TSR is set to 0000h. This bit is automatically set to 0.

TSPS[1:0] Bits (Time Stamp Prescaler Select)

The TSPS[1:0] bits select the prescaler for the time stamp. The reference clock for the time stamp can be selected to be either 1-, 2-, 4- or 8-bit time periods.

CANM[1:0] Bits (CAN Operating Mode Select)

The CANM[1:0] bits select one of the following modes for the CAN module: CAN operation mode, CAN reset mode, or CAN halt mode. CAN sleep mode is set by the SLPM bit. For details, refer to section 31.3, Operating Mode.
When the CAN module enters CAN halt mode according to the setting of the BOM[1:0] bits, the CANM[1:0] bits are automatically set to 10b.

SLPM Bit (CAN Sleep Mode)

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode. When the SLPM bit is set to 0, the CAN module exits CAN sleep mode. For details, refer to section 31.3, Operating Mode.

BOM[1:0] Bits (Bus-Off Recovery Mode)

The BOM[1:0] bits are used to select bus-off recovery mode for the CAN module.
When the BOM[1:0] bits are 00b, the recovery from bus-off is compliant with the ISO11898-1 Specifications, i.e. the CAN module reenters CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off.
When the BOM[1:0] bits are 01b and the CAN module reaches the bus-off state, the CANM[1:0] bits in CTLR are set to 10b (CAN halt mode) to enter CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off, and TECR and RECR are set to 00h.
When the BOM[1:0] bits are 10b, the CANM[1:0] bits are set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, i.e. after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off, and TECR and RECR are set to 00h.
When the BOM[1:0] bits are 11b, the CAN module enters CAN halt mode by setting the CANM[1:0] bits to 10b while the CAN module is still in the bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and TECR and RECR are set to 00h. However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM[1:0] bits are set to 10b, a bus-off recovery interrupt request is generated.
If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM[1:0] bits are 01b, or at bus-off end when the BOM[1:0] bits are 10b), then the CPU request to enter CAN reset mode has higher priority.

RBOC Bit (Forcible Return From Bus-Off)

When the RBOC bit is set to 1 (force return from bus-off) in the bus-off state, the CAN module forcibly returns from the bus-off state. This bit is automatically set to 0. The error state changes from bus-off to error-active. When the RBOC bit is set to 1, RECR and TECR are set to 00h and the BOST bit in STR is set to 0 (the CAN module is not in bus-off state). The other registers remain unchanged even when the RBOC bit is set to 1. No bus-off recovery interrupt request is generated by this recovery from the bus-off state. Use the RBOC bit only when the BOM[1:0] bits are 00b (normal mode).

Table 31.3 Mailbox Configuration

Mailbox	MBM Bit = 0 (Normal Mailbox Mode)	MBM Bit = 1 (FIFO Mailbox Mode)
Mailboxes [0] to [23]	Normal mailbox	Normal mailbox
Mailboxes [24] to [27]		Transmit FIFO
Mailboxes [28] to [31]		Receive FIFO

Points 1 to 5 below should be considered when the CTLR.MBM bit is set to 1.
Note 1. Transmit FIFO is controlled by TFCR. MCTLj of mailboxes [24] to [27] is disabled.
MCTL24 to MCTL27 cannot be used by the transmit FIFO.
Note 2. Receive FIFO is controlled by RFCR. MCTLj of mailboxes [28] to [31] is disabled.
MCTL28 to MCTL31 cannot be used by the receive FIFO.
Note 3. Refer to MIER about the FIFO interrupts.
Note 4. The corresponding bits in MKIVLR for mailboxes [24] to [31] are disabled. Set 0 to these bits.
Note 5. Transmit/receive FIFOs can be used for both data frames and remote frames.

31.2.2 Bit Configuration Register (BCR)

Address(es): CAN1.BCR 0009 1844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSEG1[3:0]				—	—	BRP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SJW[1:0]		—	TSEG2[2:0]			—	—	—	—	—	—	—	CCLKS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CCLKS	CAN Clock Source Selection	0: PCLK (generated by the PLL clock) 1: CANCLK (generated by the main clock)	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	TSEG2[2:0]	Time Segment 2 Control	b10 b8 0 0 0: Setting prohibited 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	SJW[1:0]	Resynchronization Jump Width Control	b13 b12 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25 to b16	BRP[9:0]	Prescaler Division Ratio Select *1	These bits set the frequency of the CAN communication clock (fCANCLK).	R/W
b26	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to 28	TSEG1[3:0]	Time Segment 1 Control	b31 b28 0 0 0 0: Setting prohibited 0 0 0 1: Setting prohibited 0 0 1 0: Setting prohibited 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq	R/W

Tq: Time Quantum

Note 1. Do not set the value 1 or below when the SCKCR3.CKSEL[2:0] bits are 10b (main clock oscillator is selected).

For bit timing setting, refer to section 31.4, CAN Communication Speed Setting.
Set BCR before entering CAN halt mode or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode.
BCR consists of 24 bits. A 32-bit read/write access should be performed carefully not to rewrite bits b0 to b7.

CCLKS Bit (CAN Clock Source Selection)

When the CCLKS bit is 0, the peripheral clock (PCLK) produced by the PLL frequency synthesizer is used as the CAN clock source (fCAN).
When the CCLKS bit is 1, the CANMCLK signal produced externally on the EXTAL pins is used as the CAN clock source (fCAN) without being processed by the PLL frequency synthesizer.

TSEG2[2:0] Bits (Time Segment 2 Control)

The TSEG2[2:0] bits are used to specify the length of the phase buffer segment 2 (PHASE_SEG2) with a Tq value. A value from 2 to 8 Tq can be set. Set a value smaller than that of the TSEG1[3:0] bits.

SJW[1:0] Bits (Resynchronization Jump Width Control)

The SJW[1:0] bits are used to specify the resynchronization jump width with a Tq value. A value from 1 to 4 Tq can be set. Set a value smaller than or equal to that of the TSEG2[2:0] bits.

BRP[9:0] Bits (Prescaler Division Ratio Select)

The BRP[9:0] bits are used to set the frequency of the CAN communication clock (fCANCLK). The fCANCLK cycle is 1 Tq. If the setting is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.

TSEG1[3:0] Bits (Time Segment 1 Control)

The TSEG1[3:0] bits are used to specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with a time quantum (Tq) value.
A value from 4 to 16 Tq can be set.

31.2.3 Mask Register k (MKRk) (k = 0 to 7)

Address(es): CAN1.MKR0 0009 1400h, CAN1.MKR1 0009 1404h, CAN1.MKR2 0009 1408h, CAN1.MKR3 0009 140Ch, CAN1.MKR4 0009 1410h, CAN1.MKR5 0009 1414h, CAN1.MKR6 0009 1418h, CAN1.MKR7 0009 141Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	0: Corresponding EID[17:0] bit is not compared 1: Corresponding EID[17:0] bit is compared	R/W
b28 to b18	SID[10:0]	Standard ID	0: Corresponding SID[10:0] bit is not compared 1: Corresponding SID[10:0] bit is compared	R/W
b31 to b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W

For the mask function in FIFO mailbox mode, refer to section 31.6, Acceptance Filtering and Masking Functions.
Write to MKR0 to MKR7 in CAN reset mode or CAN halt mode.

EID[17:0] Bits (Extended ID)

The EID[17:0] bits are the filter mask bits for the CAN extended ID bits.
These bits are used to receive extended ID messages.
When the EID[17:0] bit is set to 0, the received ID is not compared with the mailbox ID for the corresponding EID[17:0] bit.
When the EID[17:0] bit is set to 1, the received ID is compared with the mailbox ID for the corresponding EID[17:0] bit.

SID[10:0] Bits (Standard ID)

The SID[10:0] bits are the filter mask bits corresponding to the CAN standard ID bits.
These bits are used to receive both standard ID and extended ID messages.
When the SID[10:0] bit is set to 0, the received ID is not compared with the mailbox ID for the corresponding SID[10:0] bit.
When the SID[10:0] bit is set to 1, the received ID is compared with the mailbox ID for the corresponding SID[10:0] bit.

31.2.4 FIFO Received ID Compare Registers 0 and 1 (FIDCR0 and FIDCR1)

Address(es): CAN1.FIDCR0 0009 1420h, CAN1.FIDCR1 0009 1424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	0: Corresponding EID[17:0] bits are 0 1: Corresponding EID[17:0] bits are 1	R/W
b28 to b18	SID[10:0]	Standard ID	0: Corresponding SID[10:0] bits are 0 1: Corresponding SID[10:0] bits are 1	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame	R/W
b31	IDE	ID Extension*1	0: Standard ID 1: Extended ID	R/W

Note 1. When the IDFM[1:0] bits are not 10b, the IDE bit should be written with 0 and read as 0.

FIDCR0 and FIDCR1 are enabled when the MBM bit in CTLR is set to 1 (FIFO mailbox mode). Bits EID[17:0], SID[10:0], RTR, and IDE in MB28 to MB31 are disabled.
For the usage of FIDCR0 and FIDCR1, refer to section 31.6, Acceptance Filtering and Masking Functions.
Write to FIDCR0 and FIDCR1 in CAN reset mode or CAN halt mode.

EID[17:0] Bits (Extended ID)

The EID[17:0] bits set the extended ID of data frames and remote frames.
These bits are used to receive extended ID messages.

SID[10:0] Bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames.
These bits are used to receive both standard ID and extended ID messages.

RTR Bit (Remote Transmission Request)

The RTR bit sets the specified frame format of data frames or remote frames.

- When both RTR bits in FIDCR0 and FIDCR1 are set to 0, only data frames can be received.
- When both RTR bits in FIDCR0 and FIDCR1 are set to 1, only remote frames can be received.
- When the RTR bits in FIDCR0 and FIDCR1 are set to 0 or 1 individually, both data frames and remote frames can be received.

IDE Bit (ID Extension)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).

- When both IDE bits in FIDCR0 and FIDCR1 are set to 0, only standard ID frames can be received.
- When both IDE bits in FIDCR0 and FIDCR1 are set to 1, only extended ID frames can be received.
- When the IDE bits in FIDCR0 and FIDCR1 are set to 0 or 1 individually, both standard ID and extended ID frames can be received.

31.2.5 Mask Invalid Register (MKIVLR)

Address(es): CAN1.MKIVLR 0009 1428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	MB31 to MB0	Mask Invalid	0: Mask valid 1: Mask invalid	R/W

Each bit in MKIVLR corresponds to a mailbox.
The correspondence between the bits and mailboxes is shown below.
Bit 0 in MKIVLR corresponds to mailbox 0 (MB0) and bit 31 corresponds to mailbox 31 (MB31).*1
When a bit is set to 1, the relevant acceptance mask register becomes invalid for the corresponding mailbox. When a mask invalid bit is set to 1, a message is received by the corresponding mailbox only if the receive message ID matches the mailbox ID exactly.
Write to MKIVLR in CAN reset mode or CAN halt mode.

Note 1. Set bits 31 to 24 to 0 in FIFO mailbox mode.

31.2.6 Mailbox Register j (MBj) (j = 0 to 31)

Table 31.4 lists the CAN1 mailbox memory mapping, and Table 31.5 lists the CAN data frame configuration.
The value after reset of the CAN1 mailbox is undefined.
Write to MBj only when the related MCTLj (j = 0 to 31) is 00h and the corresponding mailbox is not processing an abort request.
See Table 31.4 for detailed register addresses.

Table 31.4 CANi Mailbox Memory Mapping

Address	Message Content
CAN1	**Memory Mapping**
0009 1200h + 16 × j + 0	IDE, RTR, SID10 to SID6
0009 1200h + 16 × j + 1	SID5 to SID0, EID17, EID16
0009 1200h + 16 × j + 2	EID15 to EID8
0009 1200h + 16 × j + 3	EID7 to EID0
0009 1200h + 16 × j + 4	—
0009 1200h + 16 × j + 5	Data length code (DLC[3:0])
0009 1200h + 16 × j + 6	Data byte 0
0009 1200h + 16 × j + 7	Data byte 1
0009 1200h + 16 × j + 8	Data byte 2
0009 1200h + 16 × j + 9	Data byte 3
0009 1200h + 16 × j + 10	Data byte 4
0009 1200h + 16 × j + 11	Data byte 5
0009 1200h + 16 × j + 12	Data byte 6
0009 1200h + 16 × j + 13	Data byte 7
0009 1200h + 16 × j + 14	Time stamp upper byte
0009 1200h + 16 × j + 15	Time stamp lower byte

Table 31.5 CAN Data Frame Configuration

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC0	DATA0	DATA1	…	DATA7

The previous value of each mailbox is retained unless a new message is received.

Address(es): CAN1.MB0 to CAN1.MB63 0009 1200h to 0009 13FFh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b17 to b0	EID[17:0]	Extended ID*1	0: Corresponding EID[17:0] bits are 0 1: Corresponding EID[17:0] bits are 1	R/W
b28 to b18	SID[10:0]	Standard ID	0: Corresponding SID[10:0] bits are 0 1: Corresponding SID[10:0] bits are 1	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Frame Request	0: Data frame 1: Remote frame	R/W
b31	IDE	ID Extension*2	0: Standard ID 1: Extended ID	R/W

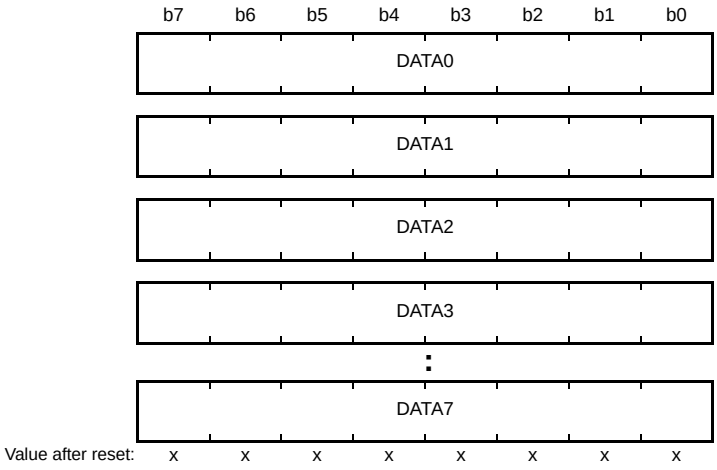
Note 1. If the mailbox has received a standard ID message, the EID bits in the mailbox are undefined.
Note 2. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode). When the IDFM[1:0] bits are not 10b, it should be written with 0 and read as 0.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	DLC[3:0]	Data Length Code*1	b3 b0 0 0 0 0: Data length = 0 byte 0 0 0 1: Data length = 1 byte 0 0 1 0: Data length = 2 bytes 0 0 1 1: Data length = 3 bytes 0 1 0 0: Data length = 4 bytes 0 1 0 1: Data length = 5 bytes 0 1 1 0: Data length = 6 bytes 0 1 1 1: Data length = 7 bytes 1 x x x: Data length = 8 bytes x: Represents any value.	R/W
b15 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W

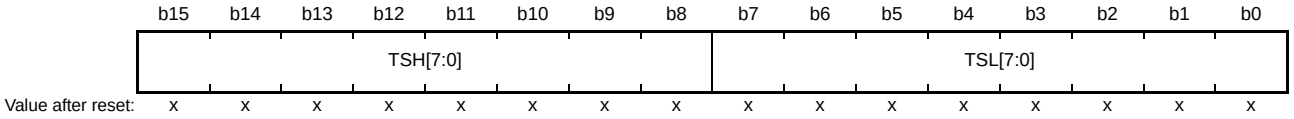
Note 1. If the mailbox has received a message whose data length set by the DLC[3:0] bits is less than 8 bytes, the values of DATA larger than the data length set by the DLC[3:0] bits in the mailbox are undefined.



x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	DATA0 to DATA7	Data Bytes 0 to 7*1,*2	DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB first, and transmission or reception starts from bit 7.	R/W

Note 1. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.
Note 2. If the mailbox has received a remote frame, the previous values of DATA0 to DATA7 in the mailbox are retained.



x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TSL[7:0]	Time Stamp Lower Byte	Bits TSH[7:0] and TSL[7:0] store the counter value of the time stamp when received messages are stored in the mailbox.	R/W
b15 to b8	TSH[7:0]	Time Stamp Higher Byte		R/W

EID[17:0] Bits (Extended ID)

The EID[17:0] bits set the extended ID of data frames and remote frames.
These bits are used to transmit or receive extended ID messages.

SID[10:0] Bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames.
These bits are used to transmit or receive both standard ID and extended ID messages.

RTR Bit (Remote Frame Request)

The RTR bit sets the frame format of data frames or remote frames.

- Receive mailbox receives only frames with the format specified by the RTR bit.
- Transmit mailbox transmits according to the frame format specified by the RTR bit.
- Receive FIFO mailbox receives the data frame, remote frame, or both frames specified by the RTR bit in FIDCR0 and FIDCR1.
- Transmit FIFO mailbox transmits the data frame or remote frame specified by the RTR bit in the relevant transmit message.

IDE Bit (ID Extension)

The IDE bit sets the ID format of standard IDs or extended IDs. The IDE bit is enabled when the IDFM[1:0] bits in CTLR is 10b (mixed ID mode).

- Receive mailbox receives only the ID format specified by the IDE bit.
- Transmit mailbox transmits with the ID format specified by the IDE bit.
- Receive FIFO mailbox receives messages with the standard ID and extended ID specified by the IDE bit in FIDCR0 and FIDCR1.
- Transmit FIFO mailbox transmits messages with the standard ID or extended ID specified by the IDE bit in the relevant transmit message.

DLC[3:0] Bits (Data Length Code)

The DLC[3:0] bits specify the number of bytes of data to be transmitted in data frames. When a remote frame is used to request data, this field specifies the requested number of bytes of data.
When a data frame is received, the number of bytes received is stored in this field. When a remote frame is received, this field is used to store the number requested by the frame.

31.2.7 Mailbox Interrupt Enable Register (MIER)

Address(es): CAN1.MIER 0009 142Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

- Normal mailbox mode

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	MB31 to MB0	Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled Bit 31 corresponds to mailbox 31 (MB31), and bit 0 corresponds to mailbox 0 (MB0).	R/W

- FIFO mailbox mode

Bit	Symbol	Bit Name	Description	R/W
b23 to b0	MB23 to MB0	Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled Bit 23 corresponds to mailbox 23 (MB23), and bit 0 corresponds to mailbox 0 (MB0).	R/W
b24	MB24	Transmit FIFO Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled	R/W
b25	MB25	Transmit FIFO Interrupt Generation Timing Control	0: Every time transmission is completed 1: When the transmit FIFO becomes empty due to completion of transmission	R/W
b27, b26	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b28	MB28	Receive FIFO Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled	R/W
b29	MB29	Receive FIFO Interrupt Generation Timing Control*1	0: Every time reception is completed 1: When the receive FIFO becomes buffer warning by completion of reception	R/W
b31, b30	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. No interrupt request is generated when the receive FIFO becomes buffer warning from full. “Buffer warning” indicates a state in which the third message is stored in the receive FIFO.

MIER can individually enable interrupts for each mailbox.

In normal mailbox mode (all bits) and in FIFO mailbox mode (bits 24 to 0 in MIER), each bit corresponds to the mailbox with the related number. These bits enable or disable transmission/reception complete interrupts for the corresponding mailboxes.

- Bit 0 in MIER corresponds to mailbox 0 (MB0).
- Bit 31 in MIER corresponds to mailbox 31 (MB31).

In FIFO mailbox mode, bits 29, 28, 25, and 24 of MIER specify whether transmit/receive FIFO interrupts are enabled/disabled and the timing when interrupt requests are generated.

Write to MIER only when the related MCTLj (j = 0 to 31) is 00h and the corresponding mailbox is not processing a transmission or reception abort request. In FIFO mailbox mode, change the bits in MIER for the related FIFO only when the TFE bit in TFCR is 0 and the TFEST bit is 1, and the RFE bit in RFCR is 0 and the RFEST bit in RFCR is 1.

31.2.8 Message Control Register j (MCTLj) (j = 0 to 31)

Address(es): CAN1.MCTL0 to CAN1.MCTL310009 1820h to 0009 183Fh

- Transmit mode (when the TRMREQ bit is 1 and the RECREQ bit is 0)

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
Value after reset:	0	0	0	0	0	0	0	0

- Receive mode (when the TRMREQ bit is 0 and the RECREQ bit is 1)

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SENTDATA	Transmission Complete Flag*1,*2	0: Transmission is not completed 1: Transmission is completed	R/W
	NEWDATA	Reception Complete Flag*1,*2	0: No data has been received or 0 is written to the NEWDATA bit 1: A new message is being stored or has been stored to the mailbox	R/W
b1	TRMACTIVE	Transmission-in-Progress Status Flag	(Transmit mailbox setting enabled) 0: Transmission is pending or transmission is not requested 1: From acceptance of transmission request to completion of transmission, or error/arbitration-lost	R
	INVALDATA	Reception-in-Progress Status Flag	(Receive mailbox setting enabled) 0: Message valid 1: Message being updated	R
b2	TRMABT	Transmission Abort Complete Flag*1,*2	(Transmit mailbox setting enabled) 0: Transmission has started, transmission abort failed because transmission is completed, or transmission abort is not requested 1: Transmission abort is completed	R/W
	MSGLOST	Message Lost Flag*1,*2	(Receive mailbox setting enabled) 0: Message is not overwritten or overrun 1: Message is overwritten or overrun	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*3	0: One-shot reception or one-shot transmission disabled 1: One-shot reception or one-shot transmission enabled	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Not configured for reception 1: Configured for reception	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Not configured for transmission 1: Configured for transmission	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing 0 to bits NEWDATA, SENTDATA, MSGLOST, TRMABT, RECREQ, and TRMREQ by a program, do not use the logic operation instruction (AND). Write 0 to only the specified bit and write 1 to the other bits before using the transfer (MOV) instruction.
Note 3. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1.
To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the RECREQ bit and confirming that it has been set to 0.
To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1.
To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message has been transmitted or aborted.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set bits MSGLOST, NEWDATA, and RECREQ to 0 simultaneously.

Write to the MCTLj in CAN operation mode or CAN halt mode.
Do not use MCTL24 to MCTL31 in FIFO mailbox mode.

SENTDATA Flag (Transmission Complete Flag)

The SENTDATA flag is set to 1 when data transmission from the corresponding mailbox is completed. The SENTDATA flag is set to 0 by writing 0 by a program.
To set the SENTDATA flag to 0, first set the TRMREQ bit to 0. Bits SENTDATA and TRMREQ cannot be set to 0 simultaneously. To transmit a new message from the corresponding mailbox, set the SENTDATA flag to 0.

NEWDATA Flag (Reception Complete Flag)

The NEWDATA flag is set to 1 when a new message is being stored or has been stored to the mailbox. The timing for setting this bit to 1 is simultaneous with the INVALDATA bit. The NEWDATA flag is set to 0 by writing 0 by a program. The NEWDATA flag cannot be set to 0 by writing 0 by a program while the related INVALDATA bit is 1.

TRMACTIVE Bit (Transmission-in-Progress Status Flag)

The TRMACTIVE bit is set to 1 when the corresponding mailbox of the CAN module begins transmitting a message. The TRMACTIVE is set to 0 when the CAN module has lost CAN bus arbitration, a CAN bus error occurs, or data transmission is completed.

INVALDATA Bit (Reception-in-Progress Status Flag)

After the completion of a message reception, the INVALDATA bit is set to 1 while the received message is being updated into the corresponding mailbox. The INVALDATA bit is set to 0 immediately after the message has been stored. If the mailbox is read while the INVALDATA bit is 1, the data is undefined.

TRMABT Flag (Transmission Abort Complete Flag)

The TRMABT flag is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort is completed before starting transmission.
- Following a transmission abort request, when the CAN module detects CAN bus arbitration-lost or a CAN bus error.
- In one-shot transmission mode (RECREQ bit = 0, TRMREQ bit = 1, and ONESHOT bit = 1), when the CAN module detects CAN bus arbitration-lost or a CAN bus error.

The TRMABT flag is not set to 1 when data transmission is completed. In this case, the SENTDATA flag is set to 1. The TRMABT flag is set to 0 by writing 0 by a program.

MSGLOST Flag (Message Lost Flag)

The MSGLOST flag is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA flag is 1. The MSGLOST flag is set to 1 at the end of the 6th bit of EOF. The MSGLOST flag is set to 0 by writing 0 by a program.
In both overwrite and overrun modes, the MSGLOST flag cannot be set to 0 by writing 0 by a program during five peripheral module clock (PCLK) cycles following the sixth bit of EOF.

ONESHOT Bit (One-Shot Enable)

The ONESHOT bit can be used in the following two ways, receive mode and transmit mode.

- One-shot receive mode
  When the ONESHOT bit is set to 1 in receive mode (RECREQ bit = 1 and TRMREQ bit = 0), the mailbox receives a message only one time. (The mailbox does not behave as a receive mailbox after having received a message one time.) The behavior of bits NEWDATA and INVALDATA is the same as in normal receive mode. In one-shot receive mode, the MSGLOST flag is not set to 1. To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it has been set to 0.
- One-shot transmit mode
  When the ONESHOT bit is set to 1 in transmit mode (RECREQ bit = 0 and TRMREQ bit = 1), the CAN module transmits a message only one time. (The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration-lost occurs.) When transmission is completed, the SENTDATA flag is set to 1. If transmission is not completed due to a CAN bus error or CAN bus arbitration-lost, the TRMABT flag is set to 1. Set the ONESHOT bit to 0 after the SENTDATA or TRMABT bit is set to 1.

RECREQ Bit (Receive Mailbox Request)

The RECREQ bit selects receive modes listed in Table 31.10.
When the RECREQ bit is set to 1, the corresponding mailbox is configured for reception of a data frame or a remote frame.
When the RECREQ bit is set to 0, the corresponding mailbox is not configured for reception of a data frame or a remote frame.
Due to hardware protection, the RECREQ bit cannot be set to 0 by writing 0 by a program during the following period.

- Hardware protection is started
  From the acceptance filter processing (the beginning of CRC field)

- Hardware protection is released
  – For the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox or a CAN bus error occurs (i.e. maximum period of hardware protection is from the beginning of CRC field to the end of the 7th bit of EOF)
  – For the other mailboxes, after the acceptance filter processing
  – If no mailbox is specified to receive the message, after the acceptance filter processing
  When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set bits SENTDATA and TRMABT to 0 before changing to reception.

TRMREQ Bit (Transmit Mailbox Request)

The TRMREQ bit selects transmit modes listed in Table 31.10.
When the TRMREQ bit is set to 1, the corresponding mailbox is configured for transmission of a data frame or a remote frame.
When the TRMREQ bit is set to 0, the corresponding mailbox is not configured for transmission of a data frame or a remote frame.
If the TRMREQ bit is changed from 1 to 0 to cancel the corresponding transmission request, either the TRMABT or SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception and then set bits NEWDATA and MSGLOST to 0 before changing to transmission.

31.2.9 Receive FIFO Control Register (RFCR)

Address(es): CAN1.RFCR 0009 1848h

	b7	b6	b5	b4	b3	b2	b1	b0
	RFEST	RFWST	RFFST	RFMLF	RFUST[2:0]			RFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RFE	Receive FIFO Enable	0: Receive FIFO disabled 1: Receive FIFO enabled	R/W
b3-b1	RFUST[2:0]	Receive FIFO Unread Message Number Status	b3 b2 b1 0 0 0: No unread message 0 0 1: 1 unread message 0 1 0: 2 unread messages 0 1 1: 3 unread messages 1 0 0: 4 unread messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b4	RFMLF	Receive FIFO Message Lost Flag	0: No receive FIFO message lost has occurred 1: Receive FIFO message lost has occurred	R/W
b5	RFFST	Receive FIFO Full Status Flag	0: Receive FIFO is not full 1: Receive FIFO is full (4 unread messages)	R
b6	RFWST	Receive FIFO Buffer Warning Status Flag	0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages)	R
b7	RFEST	Receive FIFO Empty Status Flag	0: Unread message in receive FIFO 1: No unread message in receive FIFO	R

Write to RFCR in CAN operation mode or CAN halt mode.

RFE Bit (Receive FIFO Enable)

When the RFE bit is set to 1, the receive FIFO is enabled.

When the RFE bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST bit = 1). Write 0 to the RFE bit simultaneously with setting the RFMLF bit.

Do not set this bit to 1 in normal mailbox mode (MBM bit in CTLR = 0). Due to hardware protection, the RFE bit is not set to 0 by writing 0 by a program during the following period.

- Hardware protection is started
  - From the acceptance filter processing (the beginning of CRC field)
- Hardware protection is released
  - If the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs (i.e. maximum period of hardware protection is from the beginning of CRC field to the end of 7th bit of EOF)
  - If the receive FIFO is not specified to receive the message, after the acceptance filter processing

RFUST[2:0] Bits (Receive FIFO Unread Message Number Status)

The RFUST[2:0] bits indicate the number of unread messages in the receive FIFO.

The value of the RFUST[2:0] bits is initialized to 000b when the RFE bit is set to 0.

RFMLF Flag (Receive FIFO Message Lost Flag)

The RFMLF bit is set to 1 (receive FIFO message lost has occurred) when the receive FIFO receives a new message and the receive FIFO is full. The timing for setting this bit to 1 is at the end of the 6th bit of EOF.
The RFMLF bit is set to 0 by writing 0 by a program (writing 1 has no effect). In both overwrite and overrun modes, the RFMLF bit cannot be set to 0 (receive FIFO message lost has not occurred) by writing 0 by a program due to hardware protection during five peripheral module clock (PCLK) cycles following the sixth bit of EOF, if the receive FIFO is full and determined to receive a message.

RFFST Flag (Receive FIFO Full Status Flag)

The RFFST bit is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. The RFFST bit is 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. The RFFST bit is set to 0 when the RFE bit is 0.

RFWST Flag (Receive FIFO Buffer Warning Status Flag)

The RFWST bit is set to 1 (receive FIFO is buffer warning) when the number of unread messages in the receive FIFO is 3. The RFWST bit is 0 (receive FIFO is not buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. The RFWST bit is set to 0 when the RFE bit is 0.

RFEST Flag (Receive FIFO Empty Status Flag)

The RFEST bit is set to 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. The RFEST bit is set to 1 when the RFE bit is set to 0. The RFEST bit is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.

Figure 31.2 shows the receive FIFO mailbox operation.

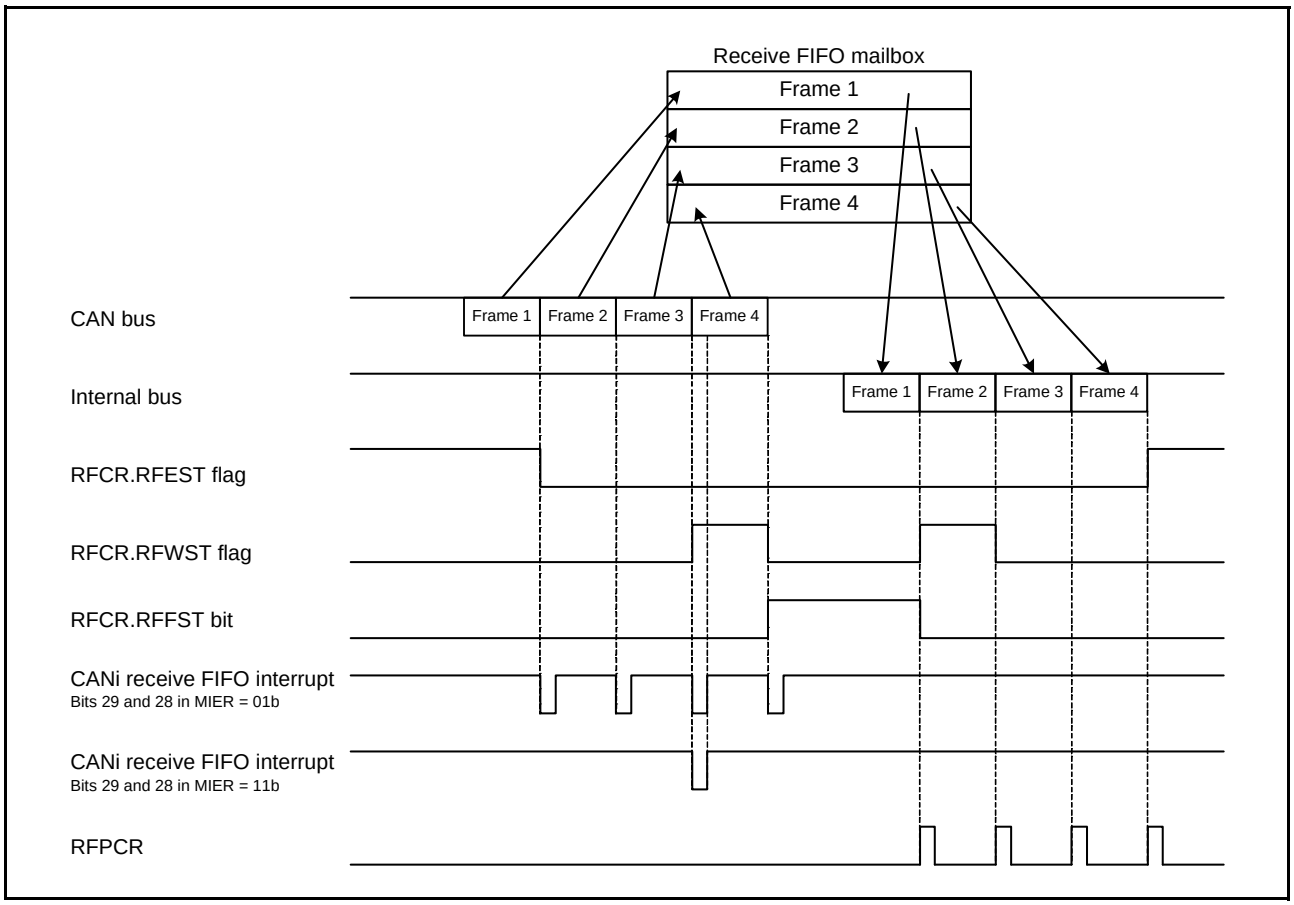


Figure 31.2 Receive FIFO Mailbox Operation (Bits 29 and 28 in MIER = 01b or 11b)

31.2.10 Receive FIFO Pointer Control Register (RFPCR)

Address(es): CAN1.RFPCR 009 1849h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU-side pointer for the receive FIFO is incremented by writing FFh to RFPCR.	W

When the receive FIFO is not empty, write FFh to RFPCR by a program to increment the CPU-side pointer for the receive FIFO to the next mailbox location.
Do not write to RFPCR when the RFE bit in RFCR is 0 (receive FIFO disabled).
Both the CAN-side pointer and the CPU-side pointer are incremented when a new message is received and the RFFST bit is 1 (receive FIFO is full) in overwrite mode. When the RFMLF bit is 1 in this condition, the CPU-side pointer cannot be incremented by writing to RFPCR by a program.

31.2.11 Transmit FIFO Control Register (TFCR)

Address(es): CAN1.TFCR 0009 184Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	TFEST	TFFST	—	—	TFUST[2:0]			TFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TFE	Transmit FIFO Enable	0: Transmit FIFO disabled 1: Transmit FIFO enabled	R/W
b3 to b1	TFUST[2:0]	Transmit FIFO Unsent Message Number Status	b3 b2 b1 0 0 0: No unsent message 0 0 1: 1 unsent message 0 1 0: 2 unsent messages 0 1 1: 3 unsent messages 1 0 0: 4 unsent messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	TFFST	Transmit FIFO Full Status	0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages)	R
b7	TFEST	Transmit FIFO Empty Status	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO	R

Write to TFCR in CAN operation mode or CAN halt mode.

TFE Bit (Transmit FIFO Enable)

When the TFE bit is set to 1, the transmit FIFO is enabled.
When the TFE bit is set to 0, the transmit FIFO becomes empty (TFEST bit = 1) and then unsent messages from the transmit FIFO are lost as described below:

- Immediately if a message from the transmit FIFO is not scheduled for the next transmission or during transmission
- Following the completion of transmission, a CAN bus error, CAN bus arbitration-lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already during transmission

Before setting the TFE bit to 1 again, ensure that the TFEST bit has been set to 1. After setting the TFE bit to 1, write transmit data into MB24.
Do not set the TFE bit to 1 in normal mailbox mode (MBM bit in CTLR = 0).

TFUST[2:0] Bits (Transmit FIFO Unsent Message Number Status)

The TFUST[2:0] bits indicate the number of unsent messages in the transmit FIFO.
The TFUST[2:0] bits are set to 000b after TFE bit is cleared to 0 and transmission is aborted or completed.

TFFST Bit (Transmit FIFO Full Status)

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. The TFFST bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. The TFFST bit is set to 0 when transmission from the transmit FIFO has been aborted.

TFEST Bit (Transmit FIFO Empty Status)

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. The TFEST bit is set to 1 when transmission from the transmit FIFO has been aborted. The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

Figure 31.3 shows the transmit FIFO mailbox operation.

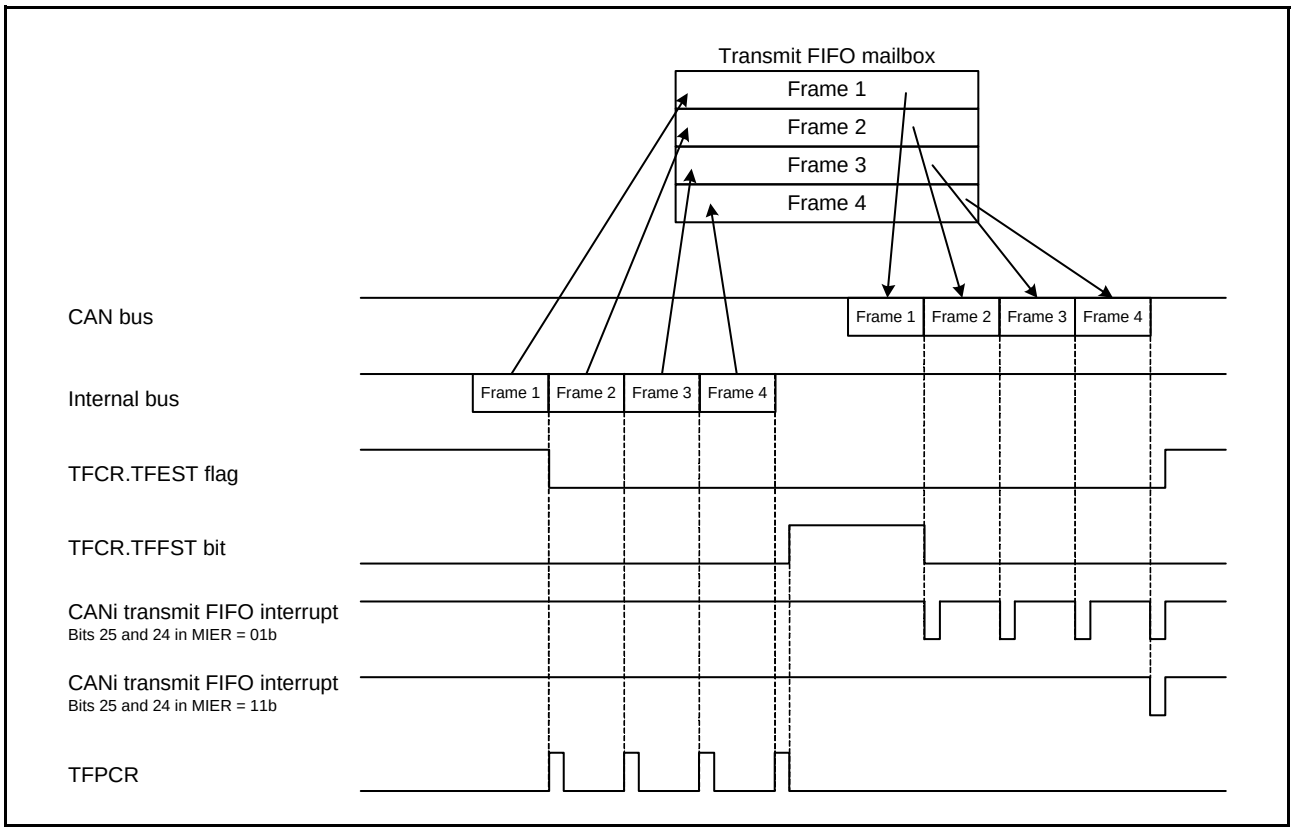


Figure 31.3 Transmit FIFO Mailbox Operation (Bits 25 and 24 in MIER = 01b or 11b)

31.2.12 Transmit FIFO Pointer Control Register (TFPCR)

Address(es): CAN1.TFPCR 0009 184Bh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU-side pointer for the transmit FIFO is incremented by writing FFh to TFPCR.	W

When the transmit FIFO is not full, write FFh to TFPCR by a program to increment the CPU-side pointer for the transmit FIFO to the next mailbox location.
Do not write to TFPCR when the TFE bit in TFCR is 0 (transmit FIFO disabled).

31.2.13 Status Register (STR)

Address(es): CAN1.STR 0009 1842h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	NDST	NEWDATA Status Flag	0: No mailbox with NEWDATA bit = 1 1: Mailbox(es) with NEWDATA bit = 1	R
b1	SDST	SENTDATA Status Flag	0: No mailbox with SENTDATA bit = 1 1: Mailbox(es) with SENTDATA bit = 1	R
b2	RFST	Receive FIFO Status Flag	0: No message in receive FIFO (empty) 1: Message in receive FIFO	R
b3	TFST	Transmit FIFO Status Flag	0: Transmit FIFO is full 1: Transmit FIFO is not full	R
b4	NMLST	Normal Mailbox Message Lost Status Flag	0: No mailbox with MSGLOST bit = 1 1: Mailbox(es) with MSGLOST bit = 1	R
b5	FMLST	FIFO Mailbox Message Lost Status Flag	0: RFMLF bit = 0 1: RFMLF bit = 1	R
b6	TABST	Transmission Abort Status Flag	0: No mailbox with TRMABT bit = 1 1: Mailbox(es) with TRMABT bit = 1	R
b7	EST	Error Status Flag	0: No error occurred 1: Error occurred	R
b8	RSTST	CAN Reset Status Flag	0: Not in CAN reset mode 1: In CAN reset mode	R
b9	HLTST	CAN Halt Status Flag	0: Not in CAN halt mode 1: In CAN halt mode	R
b10	SLPST	CAN Sleep Status Flag	0: Not in CAN sleep mode 1: In CAN sleep mode	R
b11	EPST	Error-Passive Status Flag	0: Not in error-passive state 1: In error-passive state	R
b12	BOST	Bus-Off Status Flag	0: Not in bus-off state 1: In bus-off state	R
b13	TRMST	Transmit Status Flag (transmitter)	0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state	R
b14	RECST	Receive Status Flag (receiver)	0: Bus idle or transmission in progress 1: Reception in progress	R
b15	—	Reserved	The read value is 0.	R

NDST Flag (NEWDATA Status Flag)

The NDST bit is set to 1 when at least one NEWDATA bit in MCTLj (j = 0 to 31) is 1 regardless of the value of MIER. The NDST bit is set to 0 when all NEWDATA bits are 0.

SDST Flag (SENTDATA Status Flag)

The SDST bit is set to 1 when at least one SENTDATA bit in MCTLj (j = 0 to 31) is 1 regardless of the value of MIER. The SDST bit is set to 0 when all SENTDATA bits are 0.

RFST Flag (Receive FIFO Status Flag)

The RFST bit is set to 1 when the receive FIFO is not empty. The RFST bit is set to 0 when the receive FIFO is empty or normal mailbox mode is selected.

TFST Flag (Transmit FIFO Status Flag)

The TFST bit is set to 1 when the transmit FIFO is not full. The TFST bit is set to 0 when the transmit FIFO is full or normal mailbox mode is selected.

NMLST Flag (Normal Mailbox Message Lost Status Flag)

The NMLST bit is set to 1 when at least one MSGLOST bit in MCTLj (i = 0 to 2, j = 0 to 31) is 1 regardless of the value of MIER. The NMLST bit is set to 0 when all MSGLOST bits are 0.

FMLST Flag (FIFO Mailbox Message Lost Status Flag)

The FMLST bit is set to 1 when the RFMLF bit in RFCR is 1 regardless of the value of MIER. The FMLST bit is set to 0 when the RFMLF bit is 0.

TABST Flag (Transmission Abort Status Flag)

The TABST bit is set to 1 when at least one TRMABT bit in MCTLj (i = 0 to 2, j = 0 to 31) is 1 regardless of the value of MIER. The TABST bit is set to 0 when all TRMABT bits are 0.

EST Flag (Error Status Flag)

The EST bit is set to 1 when at least one error is detected by EIFR regardless of the value of EIER. The EST bit is set to 0 when no error is detected by EIFR.

RSTST Flag (CAN Reset Status Flag)

The RSTST bit is set to 1 when the CAN module is in CAN reset mode. The RSTST bit is 0 when the CAN module is not in CAN reset mode. Even when the state is changed from CAN reset mode to CAN sleep mode, the RSTST bit remains 1.

HLTST Flag (CAN Halt Status Flag)

The HLTST bit is set to 1 when the CAN module is in CAN halt mode. The HLTST bit is set to 0 when the CAN module is not in CAN halt mode. Even when the state is changed from CAN halt mode to CAN sleep mode, the HLTST bit remains 1.

SLPST Flag (CAN Sleep Status Flag)

The SLPST bit is set to 1 when the CAN module is in CAN sleep mode. The SLPST bit is set to 0 when the CAN module is not in CAN sleep mode.

EPST Flag (Error-Passive Status Flag)

The EPST bit is set to 1 when the value of TECR or RECR exceeds 127 and the CAN module is in the error-passive state ($128 \leq TEC < 256$ or $128 \leq REC < 256$). The EPST bit is set to 0 when the CAN module is not in the error-passive state.

BOST Flag (Bus-Off Status Flag)

The BOST bit is set to 1 when the value of TECR exceeds 255 and the CAN module is in the bus-off state ($TEC \geq 256$). The BOST bit is set to 0 when the CAN module is not in the bus-off state.

TRMST Flag (Transmit Status Flag) (transmitter)

The TRMST bit is set to 1 when the CAN module performs as a transmitter node or is in the bus-off state. The TRMST bit is set to 0 when the CAN module performs as a receiver node or is in the bus-idle state.

RECST Flag (Receive Status Flag) (receiver)

The RECST bit is set to 1 when the CAN module performs as a receiver node. The RECST bit is set to 0 when the CAN module performs as a transmitter node or is in the bus-idle state.

31.2.14 Mailbox Search Mode Register (MSMR)

Address(es): CAN1.MSMR 0009 1853h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MBSM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	MBSM[1:0]	Mailbox Search Mode Select	b1 b0 0 0: Receive mailbox search mode 0 1: Transmit mailbox search mode 1 0: Message lost search mode 1 1: Channel search mode	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Write to MSMR in CAN operation mode or CAN halt mode.

MBSM[1:0] Bits (Mailbox Search Mode Select)

The MBSM[1:0] bits select the search mode for the mailbox search function.

When the MBSM[1:0] bits are 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA bit in MCTLj (j = 0 to 31) for the normal mailbox and the RFEST bit in RFCR.

When the MBSM[1:0] bits are 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA bit in MCTLj.

When the MBSM[1:0] bits are 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST bit in MCTLj for the normal mailbox and the RFMLF bit in RFCR.

When the MBSM[1:0] bits are 11b, channel search mode is selected. In this mode, the search target is CSSR. Refer to section 31.2.16, Channel Search Support Register (CSSR).

31.2.15 Mailbox Search Status Register (MSSR)

Address(es): CAN1.MSSR 0009 1852h

	b7	b6	b5	b4	b3	b2	b1	b0
	SEST	—	—	MBNST[4:0]				
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	MBNST[4:0]	Search Result Mailbox Number Status	These bits output the smallest mailbox number that is searched in each mode of MSMR.	R
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SEST	Search Result Status	0: Search result found 1: No search result	R

MBNST[4:0] Bits (Search Result Mailbox Number Status)

The MBNST[4:0] bits output the smallest mailbox number that is searched in each mode of MSMR. In receive mailbox search mode, transmit mailbox search mode, and message lost search mode, the value of the mailbox i.e., the search result to be output, is updated as described below:

- When the NEWDATA, SENTDATA or MSGLOST bit for the output mailbox is set to 0
- When the NEWDATA, SENTDATA or MSGLOST bit for a higher-priority mailbox is set to 1

If the MBSM[1:0] bits are set to 00b (receive mailbox search mode) or 10b (message lost search mode), the receive FIFO (mailbox [28]) is output when the receive FIFO is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (mailboxes [0] to [23]). If the MBSM[1:0] bits are set to 01b (transmit mailbox search mode), the transmit FIFO (mailbox [24]) is not output. Table 31.6 lists the behavior of the MBNST[4:0] bits in FIFO mailbox mode.

In channel search mode, the MBNST[4:0] bits output the corresponding channel number. After MSSR is read by a program, the next target channel number is output.

SEST Bit (Search Result Status)

The SEST bit is set to 1 (no search result) when no corresponding mailbox is found after searching all mailboxes. For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA bit for mailboxes is 1. The SEST bit is set to 0 when at least one SENTDATA bit is 1. When the SEST bit is 1, the value of the MBNST[4:0] bits is undefined.

Table 31.6 Behavior of MBNST[4:0] Bits in FIFO Mailbox Mode

MBSM[1:0] Bits	Mailbox [24] (Transmit FIFO)	Mailbox [28] (Receive FIFO)
00b	Mailbox [24] is not output.	Mailbox [28] is output when no MCTLj.NEWDATA bit for the normal mailboxes is set to 1 (new message is being stored or has been stored to the mailbox) and the receive FIFO is not empty.
01b		Mailbox [28] is not output.
10b		Mailbox [28] is output when no MCTLj.MSGLOST bit for the normal mailboxes is set to 1 (message is overwritten or overrun) and the RFCR.RFMLF bit is set to 1 (receive FIFO message lost has occurred) in the receive FIFO.
11b		Mailbox [28] is not output.

31.2.16 Channel Search Support Register (CSSR)

Address(es): CAN1.CSSR 0009 1851h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	When the value for the channel search is input, the channel number is output to MSSR.	R/W

The bits in CSSR, which are set to 1, are encoded by an 8/3 encoder (the LSB position has the higher priority) and output to the MBNST[4:0] bits in MSSR.
MSSR outputs the updated value whenever MSSR is read by a program.
Write to CSSR only when the MSMR.MBSM[1:0] bits are 11b (channel search mode). Write to CSSR in CAN operation mode or CAN halt mode.

Figure 31.4 shows the write and read of CSSR and MSSR.

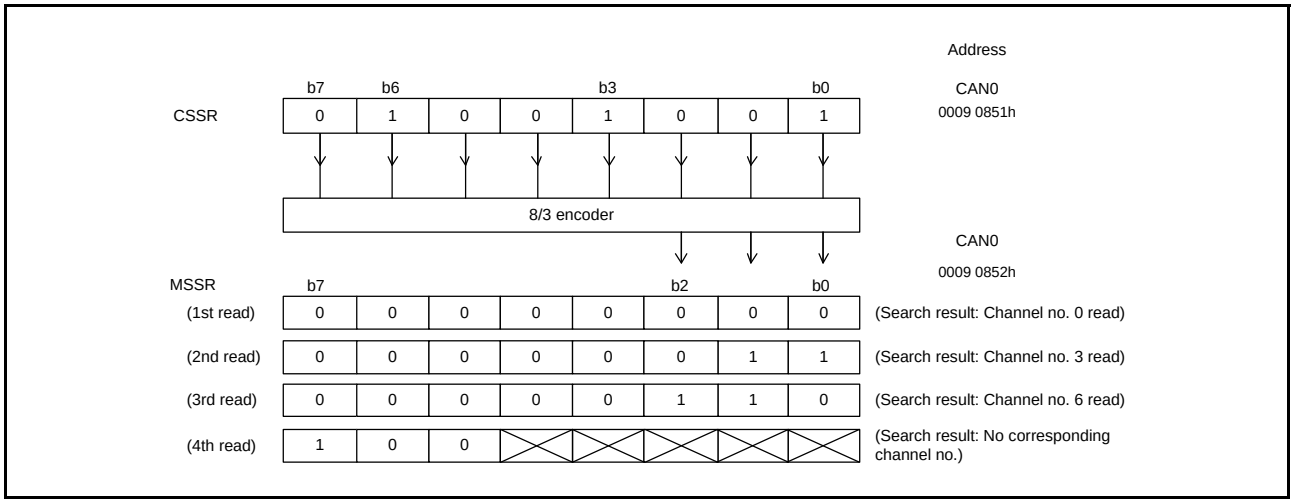


Figure 31.4 Write and Read of CSSR and MSSR

The value of CSSR is also updated whenever MSSR is read. When read, the value prior to conversion by the 8/3 encoder can be read.

31.2.17 Acceptance Filter Support Register (AFSR)

Address(es): CAN1.AFSR 0009 1856h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

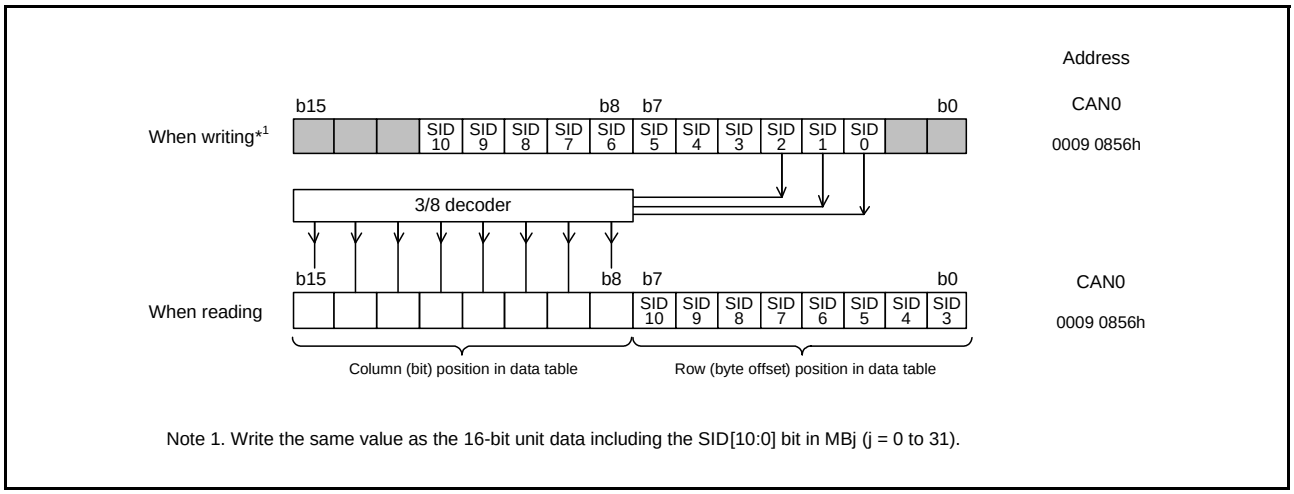
Bit	Description	R/W
b15 to b0	After the standard ID of a received message is written, the value converted for data table search can be read.	R/W

Note: • Write to AFSR in CAN operation mode or CAN halt mode.

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs created by the user are set to be valid/invalid in bit units. When AFSR is written with data in 16-bit units including the SID[10:0] bit in MBj (j = 0 to 31), in which a received standard ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.
The ASU is enabled in the following cases:

- When the ID to receive cannot be masked by the acceptance filter
  (Example) IDs to receive: 078h, 087h, and 111h
- When there are too many IDs to receive and software filtering time is expected to be shortened
  It should be noted that AFSR cannot be set in CAN reset mode.

Figure 31.5 shows the write and read of AFSR.



Note 1. Write the same value as the 16-bit unit data including the SID[10:0] bit in MBj (j = 0 to 31).

Figure 31.5 Write and Read of AFSR

31.2.18 Error Interrupt Enable Register (EIER)

Address(es): CAN1.EIER 0009 184Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BEIE	Bus Error Interrupt Enable	0: Bus error interrupt disabled 1: Bus error interrupt enabled	R/W
b1	EWIE	Error-Warning Interrupt Enable	0: Error-warning interrupt disabled 1: Error-warning interrupt enabled	R/W
b2	EPIE	Error-Passive Interrupt Enable	0: Error-passive interrupt disabled 1: Error-passive interrupt enabled	R/W
b3	BOEIE	Bus-Off Entry Interrupt Enable	0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled	R/W
b4	BORIE	Bus-Off Recovery Interrupt Enable	0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled	R/W
b5	ORIE	Overrun Interrupt Enable	0: Receive overrun interrupt disabled 1: Receive overrun interrupt enabled	R/W
b6	OLIE	Overload Frame Transmit Interrupt Enable	0: Overload frame transmit interrupt disabled 1: Overload frame transmit interrupt enabled	R/W
b7	BLIE	Bus Lock Interrupt Enable	0: Bus lock interrupt disabled 1: Bus lock interrupt enabled	R/W

EIER is used to enable or disable the error interrupt individually for each error interrupt source in EIFR.
Write to EIER in CAN reset mode.

BEIE Bit (Bus Error Interrupt Enable)

When the BEIE bit is 0, no error interrupt request is generated even if the BEIF bit in EIFR is set to 1. When the BEIE bit is 1, an error interrupt request is generated if the BEIF bit is set to 1.

EWIE Bit (Error-Warning Interrupt Enable)

When the EWIE bit is 0, no error interrupt request is generated even if the EWIF bit in EIFR is set to 1. When the EWIE bit is 1, an error interrupt request is generated if the EWIF bit is set to 1.

EPIE Bit (Error-Passive Interrupt Enable)

When the EPIE bit is 0, no error interrupt request is generated even if the EPIF bit in EIFR is set to 1. When the EPIE bit is 1, an error interrupt request is generated if the EPIF bit is set to 1.

BOEIE Bit (Bus-Off Entry Interrupt Enable)

When the BOEIE bit is 0, no error interrupt request is generated even if the BOEIF bit in EIFR is set to 1. When the BOEIE bit is 1, an error interrupt request is generated if the BOEIF bit is set to 1.

BORIE Bit (Bus-Off Recovery Interrupt Enable)

When the BORIE bit is 0, an error interrupt request is not generated even if the BORIF bit in EIFR is set to 1. When the BORIE bit is set to 1, an error interrupt request is generated if the BORIF bit is set to 1.

ORIE Bit (Overrun Interrupt Enable)

When the ORIE bit is 0, an error interrupt request is not generated even if the ORIF bit in EIFR is set to 1. When the ORIE bit is 1, an error interrupt request is generated if the ORIF bit is set to 1.

OLIE Bit (Overload Frame Transmit Interrupt Enable)

When the OLIE bit is 0, no error interrupt request is generated even if the OLIF bit in EIFR is set to 1. When the OLIE bit is 1, an error interrupt request is generated if the OLIF bit is set to 1.

BLIE Bit (Bus Lock Interrupt Enable)

When the BLIE bit is 0, no error interrupt request is generated even if the BLIF bit in EIFR is set to 1. When the BLIE bit is 1, an error interrupt request is generated if the BLIF bit is set to 1.

31.2.19 Error Interrupt Factor Judge Register (EIFR)

Address(es): CAN1.EIFR 0009 184Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BEIF	Bus Error Detect Flag	0: No bus error detected 1: Bus error detected	R/W
b1	EWIF	Error-Warning Detect Flag	0: No error-warning detected 1: Error-warning detected	R/W
b2	EPIF	Error-Passive Detect Flag	0: No error-passive detected 1: Error-passive detected	R/W
b3	BOEIF	Bus-Off Entry Detect Flag	0: No bus-off entry detected 1: Bus-off entry detected	R/W
b4	BORIF	Bus-Off Recovery Detect Flag	0: No bus-off recovery detected 1: Bus-off recovery detected	R/W
b5	ORIF	Receive Overrun Detect Flag	0: No receive overrun detected 1: Receive overrun detected	R/W
b6	OLIF	Overload Frame Transmission Detect Flag	0: No overload frame transmission detected 1: Overload frame transmission detected	R/W
b7	BLIF	Bus Lock Detect Flag	0: No bus lock detected 1: Bus lock detected	R/W

If an event corresponding to each bit occurs, the corresponding bit in EIFR is set to 1 regardless of the setting of EIER. To set each bit to 0, write 0 by a program. If the set timing occurs simultaneously with the clear timing by the program, the bit becomes 1.

When a single bit is set to 0 by a program, do not use the logic operation instruction (AND) – use the transfer instruction (MOV) to ensure that only the specified bit is set to 0 and the other bits are set to 1. Writing 1 has no effect to these bit values.

BEIF Flag (Bus Error Detect Flag)

The BEIF bit is set to 1 when a bus error is detected.

EWIF Flag (Error-Warning Detect Flag)

The EWIF bit is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95. The EWIF bit is set to 1 only when the REC or TEC initially exceeds 95. Thus, if 0 is written to the EWIF bit by a program while the REC or TEC remains greater than 95, the EWIF bit is not set to 1 until the REC and TEC go below 95 and then REC or TEC exceeds 95 again.

EPIF Flag (Error-Passive Detect Flag)

The EPIF bit is set to 1 when the CAN error state becomes error-passive (the REC (receive error counter) or TEC (transmit error counter) value exceeds 127).
The EPIF bit is set to 1 only when the REC or TEC initially exceeds 127. Thus, if 0 is written by a program while the REC or TEC remains greater than 127, the EPIF bit is not set to 1 until the REC and TEC go below 127 and then REC or TEC exceeds 127 again.

BOEIF Flag (Bus-Off Entry Detect Flag)

The BOEIF bit is set to 1 when the CAN error state becomes bus-off (the TEC (transmit error counter) value exceeds 255). The BOEIF bit is also set to 1 when the BOM[1:0] bits in CTLR are 01b (entry to CAN halt mode automatically at bus-off entry) and the CAN module becomes the bus-off state.

BORIF Flag (Bus-Off Recovery Detect Flag)

The BORIF bit is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive bits 128 times in the following conditions:

- When the BOM[1:0] bits in CTLR are 00b
- When the BOM[1:0] bits in CTLR are 10b
- When the BOM[1:0] bits in CTLR are 11b

However, the BORIF bit is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:

- When the CANM[1:0] bits in CTLR are set to 01b or 11b (CAN reset mode)
- When the RBOC bit in CTLR is set to 1 (forcible return from bus-off)
- When the BOM[1:0] bits in CTLR are set to 01b
- When the BOM[1:0] bits in CTLR are set to 11b and the CANM[1:0] bits in CTLR are set to 10b (CAN halt mode) before normal recovery occurs

ORIF Flag (Receive Overrun Detect Flag)

The ORIF bit is set to 1 when a receive overrun occurs. This bit is not to set to 1 in overwrite mode.
In overwrite mode, a reception complete interrupt request is generated if an overwrite condition occurs and the ORIF bit is not set to 1.
In normal mailbox mode, if an overrun occurs in any of mailboxes [0] to [31] in overrun mode, this bit is set to 1. In FIFO mailbox mode, if an overrun occurs in any of mailboxes [0] to [23] or the receive FIFO in overrun mode, this bit is set to 1.

OLIF Flag (Overload Frame Transmission Detect Flag)

The OLIF bit is set to 1 if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception.

BLIF Flag (Bus Lock Detect Flag)

The BLIF flag is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the BLIF flag is set to 1, bus lock is detected again under either of the following conditions:

- After this flag is set to 0 from 1, recessive bits are detected
- After this flag is set to 0 from 1, the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again (internal reset).

Table 31.7 lists the behavior of bits BOEIF and BORIF according to the CTLR.BOM[1:0] bit setting.

Table 31.7 Behavior of BOEIF and BORIF Flags according to CTLR.BOM[1:0] Bit Setting

BOM[1:0] Bits	BOEIF Bit	BORIF Bit
00b	Set to 1 on entry to the bus-off state.	Set to 1 on exit from the bus-off state.
01b		Do not set to 1.
10b		Set to 1 on exit from the bus-off state.
11b		Set to 1 if normal bus-off recovery occurs before the CANM[1:0] bits are set to 10b (CAN halt mode).

31.2.20 Receive Error Count Register (RECR)

Address(es): CAN1.RECR 0009 184Eh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Receive error count function CiRECR increments or decrements the counter value according to the error status of the CAN module during reception.	R

RECR indicates the value of the receive error counter.

Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the receive error counter.

The value of RECR in the bus-off state is undefined.

31.2.21 Transmit Error Count Register (TECR)

Address(es): CAN1.TECR 0009 184Fh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Transmit error count function CiTECR increments or decrements the counter value according to the error status of the CAN module during transmission.	R

TECR indicates the value of the transmit error counter.
Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the transmit error counter.
The value of TECR in the bus-off state is undefined.

31.2.22 Error Code Store Register (ECSR)

Address(es): CAN1.ECSR 0000 1850h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SEF	Stuff Error Flag*1,*2	0: No stuff error detected 1: Stuff error detected	R/W
b1	FEF	Form Error Flag*1,*2	0: No form error detected 1: Form error detected	R/W
b2	AEF	ACK Error Flag*1,*2	0: No ACK error detected 1: ACK error detected	R/W
b3	CEF	CRC Error Flag*1,*2	0: No CRC error detected 1: CRC error detected	R/W
b4	BE1F	Bit Error (recessive) Flag*1,*2	0: No bit error (recessive) detected 1: Bit error (recessive) detected	R/W
b5	BE0F	Bit Error (dominant) Flag*1,*2	0: No bit error (dominant) detected 1: Bit error (dominant) detected	R/W
b6	ADEF	ACK Delimiter Error Flag*1,*2	0: No ACK delimiter error detected 1: ACK delimiter error detected	R/W
b7	EDPM	Error Display Mode Select*3,*4	0: Output of first detected error code 1: Output of accumulated error code	R/W

Note 1. Writing 1 has no effect to these bit values.
Note 2. To write 0 to bits SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF, do not use the logic operation instruction (AND). Use the transfer (MOV) instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
Note 3. Write to the EDPM bit in CAN reset mode or CAN halt mode.
Note 4. If more than one error condition is detected simultaneously, all related bits are set to 1.

ECSR can be used to monitor whether an error has occurred on the CAN bus.
Refer to the CAN Specifications (ISO11898-1) to check the generation conditions of each error.
To set each bit except for the EDPM bit to 0, write 0 by a program. If the timing at which each bit is set to 1 and the timing at which 0 is written by a program are the same, the relevant bit is set to 1.

SEF Flag (Stuff Error Flag)

The SEF bit is set to 1 when a stuff error is detected.

FEF Flag (Form Error Flag)

The FEF bit is set to 1 when a form error is detected.

AEF Flag (ACK Error Flag)

The AEF bit is set to 1 when an ACK error is detected.

CEF Flag (CRC Error Flag)

The CEF bit is set to 1 when a CRC error is detected.

BE1F Flag (Bit Error (recessive) Flag)

The BE1F bit is set to 1 when a recessive bit error is detected.

BE0F Flag (Bit Error (dominant) Flag)

The BE0F bit is set to 1 when a dominant bit error is detected.

ADEF Flag (ACK Delimiter Error Flag)

The ADEF bit is set to 1 when a form error is detected with the ACK delimiter during transmission.

EDPM Bit (Error Display Mode Select)

The EDPM bit selects the output mode of ECSR. When the EDPM bit is set to 0, ECSR outputs the first error code. When the EDPM bit is set to 1, ECSR outputs the accumulated error code.

31.2.23 Time Stamp Register (TSR)

Address(es): CAN1.TSR 0009 1854h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	R/W
b15 to b0	Free-running counter value for the time stamp function	R

Note: • Read TSR in 16-bit units.

When TSR is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read.
The value of the time stamp counter reference clock is a multiple of 1 bit time, as configured by the TSPS[1:0] bits in CTLR.
The time stamp counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode.
The time stamp counter value is stored to bits TSL[7:0] and TSH[7:0] in MBj when a received message is stored in a receive mailbox.

31.2.24 Test Control Register (TCR)

Address(es): CAN1.TCR 0009 1858h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSTM[1:0]		TSTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSTE	CAN Test Mode Enable	0: CAN test mode disabled 1: CAN test mode enabled	R/W
b2, b1	TSTM[1:0]	CAN Test Mode Select	b2 b1 0 0: Other than CAN test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback) 1 1: Self-test mode 1 (internal loopback)	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TCR controls the CAN test mode. Write to TCR in CAN halt mode only.

(1) Listen-Only Mode

The CAN Specifications (ISO11898-1) recommend an optional bus monitoring mode. In listen-only mode, valid data frames and valid remote frames can be received. However, only recessive bits can be sent on the CAN bus, and the ACK bit, overload flag, and active error flag cannot be sent.

Listen-only mode can be used for baud rate detection.

Do not request transmission from any mailboxes in listen-only mode.

Figure 31.6 shows the connection when listen-only mode is selected (i = 1).

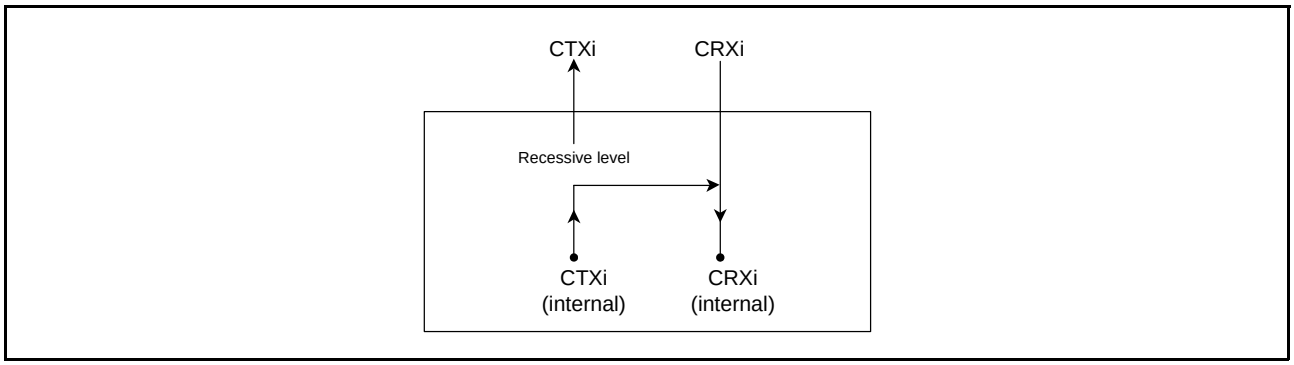


Figure 31.6 Connection when Listen-Only Mode is Selected (i = 1)

(2) Self-Test Mode 0 (External Loopback))

Self-test mode 0 is provided for CAN transceiver tests.
In self-test mode 0, the protocol controller treats its own transmitted messages as messages received via the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.
Connect the CTXi and CRXi pins to the transceiver.
Figure 31.7 shows the connection when self-test mode 0 is selected (i = 1).

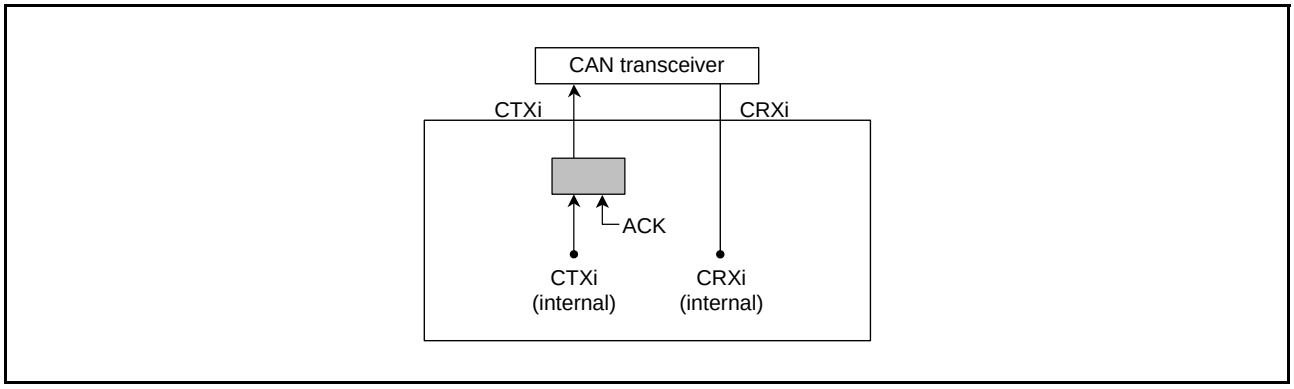


Figure 31.7 Connection when Self-Test Mode 0 is Selected (i = 1)

(3) Self-Test Mode 1 (Internal Loopback)

Self-test mode 1 is provided for self-test functions.
In self-test mode 1, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.
In self-test mode 1, the protocol controller performs an internal feedback from the internal CTXi pin to the internal CRXi pin. The input value of the external CRXi pin is ignored. The external CTXi pin outputs only recessive bits. The CTXi and CRXi pins do not need to be connected to the CAN bus or any external device.
Figure 31.8 shows the connection when self-test mode 1 is selected (i = 1).

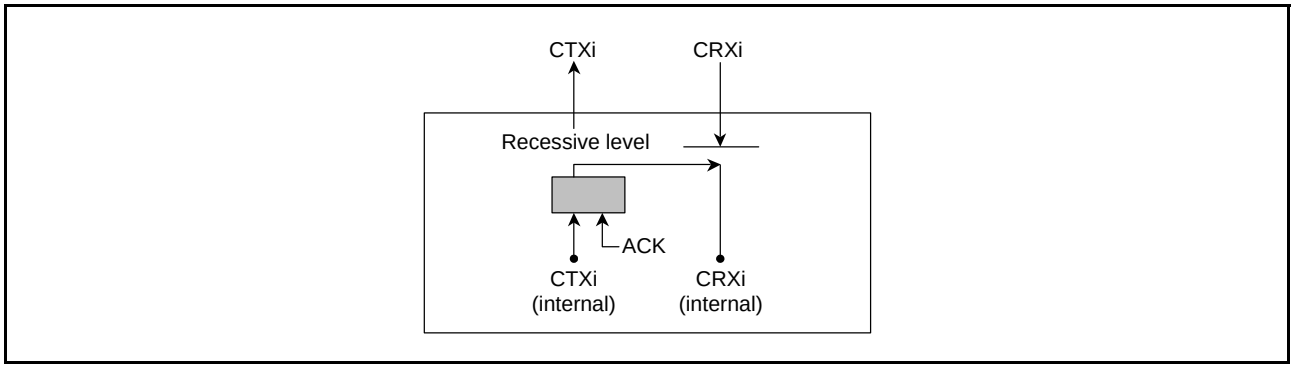


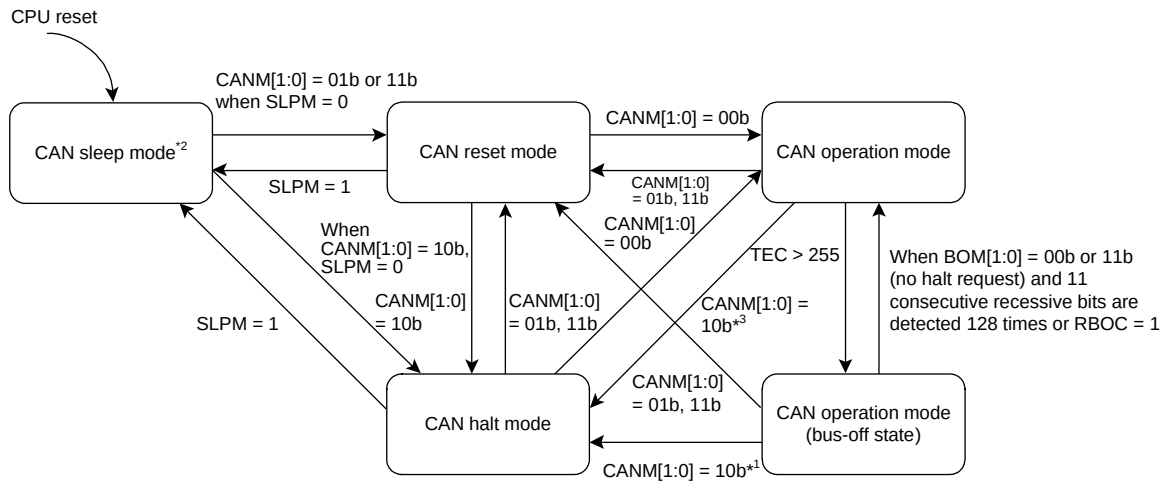
Figure 31.8 Connection when Self-Test Mode 1 is Selected (i = 1)

31.3 Operating Mode

The CAN module has the following four operating modes.

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode

Figure 31.9 shows the transition between CAN operating modes.



CANM, SLPM, BOM, RBOC: Bits in CTLR

Note 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the CTLR.BOM[1:0] bits.
When the CTLR.BOM[1:0] bits are 01b, the state transition timing is immediately after entering the bus-off state.
When the CTLR.BOM[1:0] bits are 10b, the state transition timing is at the end of the bus-off state.
When the CTLR.BOM[1:0] bits are 11b, the state transition timing is at the setting of the CTLR.CANM[1:0] bits to 10b (CAN halt mode).
Note 2. Write 0 only to the CTLR.SLPM bit to set or cancel CAN sleep mode.
Transition from sleep mode to CAN Halt mode is only allowed after transition from CAN Halt mode to sleep mode.
Note 3. CAN Halt mode cannot be entered while CAN bus is locked at dominant level. In such case, make a transition to CAN reset mode.

Figure 31.9 Transition between CAN Operating Modes

31.3.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration.
When the CTLR.CANM[1:0] bits are set to 01b or 11b, the CAN module enters CAN reset mode. Then, the STR.RSTST bit is set to 1. Do not change the CTLR.CANM[1:0] bits until the RSTST bit is set to 1. Set BCR before exiting CAN reset mode to any other modes.
The following registers are initialized to their reset values after entering CAN reset mode, and their initial values are retained during CAN reset mode:

- MCTLj
- STR (except for the SLPST and TFST bits)
- EIFR
- RECR
- TECR
- TSR
- MSSR
- MSMR

- RFCR
- TFCR
- TCR
- ECSR (except for the EDPM bit)

The following registers retain their previous values even after entering CAN reset mode.

- CTLR
- STR (only the SLPST and TFST bits)
- MIER
- EIER
- BCR
- CSSR
- ECSR (only the EDPM bit)
- MBj
- MKR0 to MKR7
- FIDCR0 and FIDCR1
- MKIVLR
- AFSR
- RFPCR
- TFPCR

31.3.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.
When the CTLR.CANM[1:0] bits are set to 10b, CAN halt mode is selected. Then the STR.HLTST bit is set to 1. Do not change the CTLR.CANM[1:0] bits until the HLTST bit is set to 1.
See Table 31.8 for the state transition conditions when transmitting or receiving.
All registers except for bits RSTST, HLTST, and SLPST in STR remain unchanged when the CAN enters CAN halt mode.
Do not change CTLR (except for bits CANM[1:0] and SLPM) and EIER in CAN halt mode. BCR can be changed in CAN halt mode only when listen-only mode is selected for automatic baud rate detection.

Table 31.8 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode (forcible transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission.*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception.*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission.*1,*2,*4	[When the BOM[1:0] bits are 00b] A halt request from a program will be accepted only after bus-off recovery. [When the BOM[1:0] bits are 01b] CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 10b] CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

CANM[1:0], BOM[1:0]: Bits in CTLR

Note 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

Note 2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the EIFR.BLIF flag. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

31.3.3 CAN Sleep Mode

CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After a RES# pin reset or software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in CTLR is set to 1, the CAN module enters CAN sleep mode. Then, the SLPST bit in STR is set to 1. Do not change the value of the SLPM bit until the SLPST bit is set to 1. The other registers remain unchanged when the CAN module enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any registers (except for the SLPM bit) during CAN sleep mode. Read operation is still allowed.

When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

31.3.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.
When the CANM[1:0] bits in CTLR are set to 00b, the CAN module enters CAN operation mode.
Then bits RSTST and HLTST in STR are set to 0. Do not change the value of the CANM[1:0] bits until bits RSTST and HLTST are set to 0.
If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network, thus enabling transmission and reception of CAN messages.
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three sub-modes, depending on the status of the CAN bus.

- Idle mode: Transmission or reception is not being performed.
- Receive mode: A CAN message sent by another node is being received.
- Transmit mode:A CAN message is being transmitted. The CAN module receives a message transmitted by the local node simultaneously when self-test mode 0 (TSTM[1:0] bits in TCR = 10b) or self-test mode 1 (TSTM[1:0] bits = 11b) is selected.

Figure 31.10 shows the sub-modes of CAN operation mode.

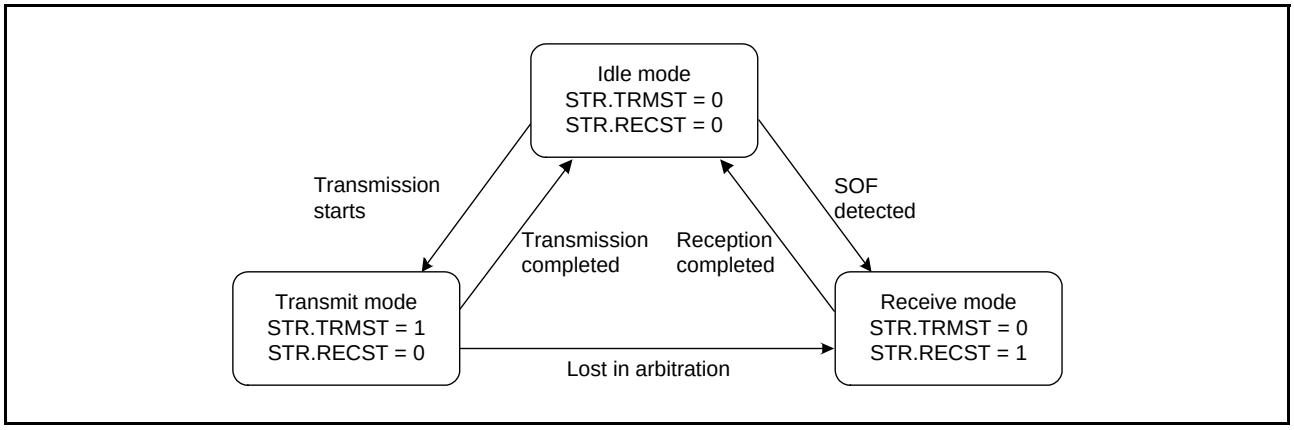


Figure 31.10 Sub-Modes of CAN Operation Mode

31.3.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state according to the increment/decrement rules for the transmit/error counters in the CAN Specifications.
The following cases apply when the CAN module is recovering from the bus-off state. When the CAN module is in the bus-off state, the values of the CAN-related registers, except for STR, EIFR, RECR, TECR and TSR, remain unchanged.

(1) When bits BOM[1:0] in CTLR are 00b (normal mode)

The CAN module enters the error-active state after it has completed the recovery from the bus-off state and CAN communication is enabled. The BORIF flag in EIFR is set to 1 (bus-off recovery detected) at this time.

(2) When bit RBOC in CTLR is set to 1 (forcible return from bus-off)

The CAN module enters the error-active state when it is in the bus-off state and the RBOC bit is set to 1. CAN communication is enabled again after 11b consecutive recessive bits are detected. The BORIF bit is not set to 1 at this time.

(3) When bits BOM[1:0] are 01b (automatic transition to CAN halt mode at bus-off entry)

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF bit is not set to 1 at this time.

(4) When bits BOM[1:0] are 10b (automatic transition to CAN halt mode at bus-off end)

The CAN module enters CAN halt mode when it has completed the recovery from bus-off. The BORIF bit is set to 1 at this time.

(5) When bits BOM[1:0] are 11b (automatic transition to CAN halt mode by a program) and bits CANM[1:0] in CTLR are set to 10b (CAN halt mode) during bus-off state

The CAN module enters CAN halt mode when it is in the bus-off state and the CANM[1:0] bits are set to 10b (CAN halt mode). The BORIF bit is not set to 1 at this time.
If the CANM[1:0] bits are not set to 10b during bus-off, the same behavior as (1) applies.

31.4 CAN Communication Speed Setting

The following description explains about CAN communication speed setting.

31.4.1 CAN Clock Setting

The CAN module has a CAN clock selector.
The CAN clock can be set by the CCLKS bit and the BRP[9:0] bits in BCR.
Figure 31.11 shows a block diagram of the CAN clock generator.

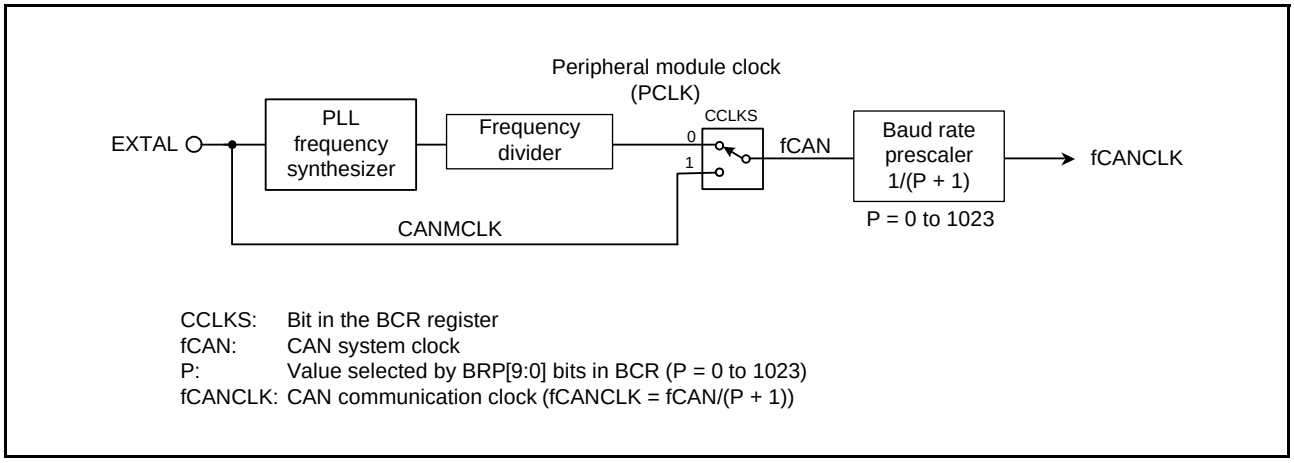


Figure 31.11 Block Diagram of CAN Clock Generator

31.4.2 Bit Timing Setting

The bit time consists of the following three segments.
Figure 31.12 shows the bit timing.

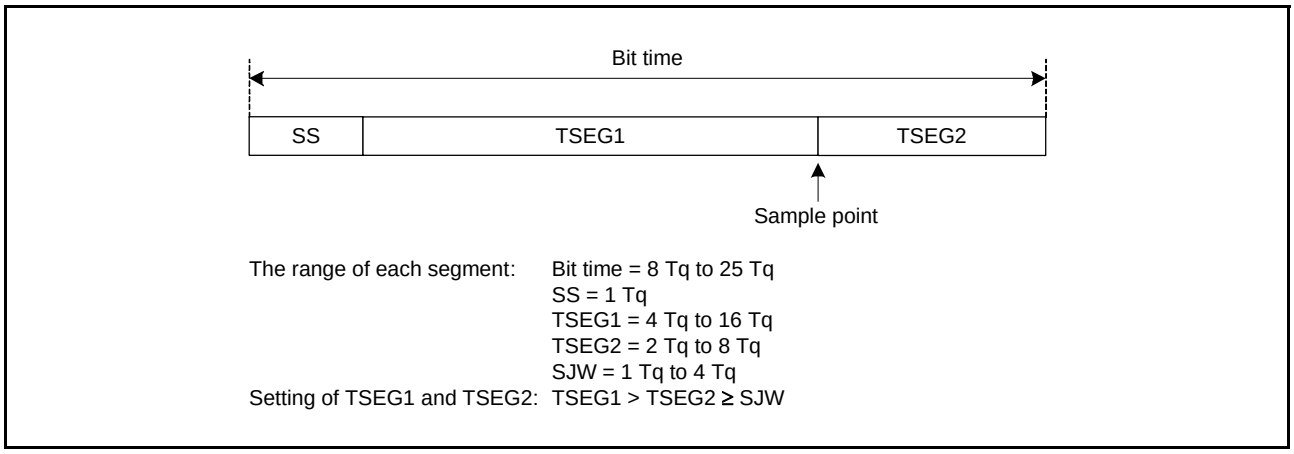


Figure 31.12 Bit Timing

31.4.3 Bit Rate

The bit rate depends on the division value of fCAN (CAN clock), the division value of the baud rate prescaler, and the number of Tq of 1 bit time.

$$\text{Bit rate [bps]} = \frac{\text{fCAN}}{\text{Baud rate prescaler division value}^{*1} \times \text{number of Tq of 1 bit time}} = \frac{\text{fCANCLK}}{\text{Number of Tq of 1 bit time}}$$

Note 1. Division value of baud rate prescaler = P + 1 (P: 0 to 1023)
P: Setting of the BRP[9:0] bits in BCR

Table 31.9 lists bit rate examples.

Table 31.9 Bit Rate Examples

fCAN	50 MHz		48 MHz		40 MHz		32 MHz	
Bit Rate	Number of Tq	P + 1	Number of Tq	P + 1	Number of Tq	P + 1	Number of Tq	P + 1
1 Mbps	10Tq 25Tq	5 2	8Tq 12Tq 16Tq	6 4 3	10Tq 20Tq	4 2	8Tq 16Tq	4 2
500 kbps	10Tq 25Tq	10 4	8Tq 12Tq 16Tq	12 8 6	10Tq 20Tq	8 4	8Tq 16Tq	8 4
250 kbps	10Tq 25Tq	20 8	8Tq 12Tq 16Tq	24 16 12	10Tq 20Tq	16 8	8Tq 16Tq	16 8
125 kbps	10Tq 25Tq	40 16	8Tq 12Tq 16Tq	48 32 24	10Tq 20Tq	32 16	8Tq 16Tq	32 16
83.3 kbps	10Tq 25Tq	60 24	8Tq 12Tq 16Tq	72 48 36	8Tq 10Tq 16Tq 20Tq	60 48 30 24	8Tq 16Tq	48 24
33.3 kbps	10Tq 25Tq	150 60	8Tq 12Tq 16Tq	180 120 90	8Tq 10Tq 20Tq	150 120 60	8Tq 10Tq 16Tq 20Tq	120 96 60 48

31.5 Mailbox and Mask Register Structure

Figure 31.13 shows the structure of MBj.
There are 32 mailboxes with the same structure.

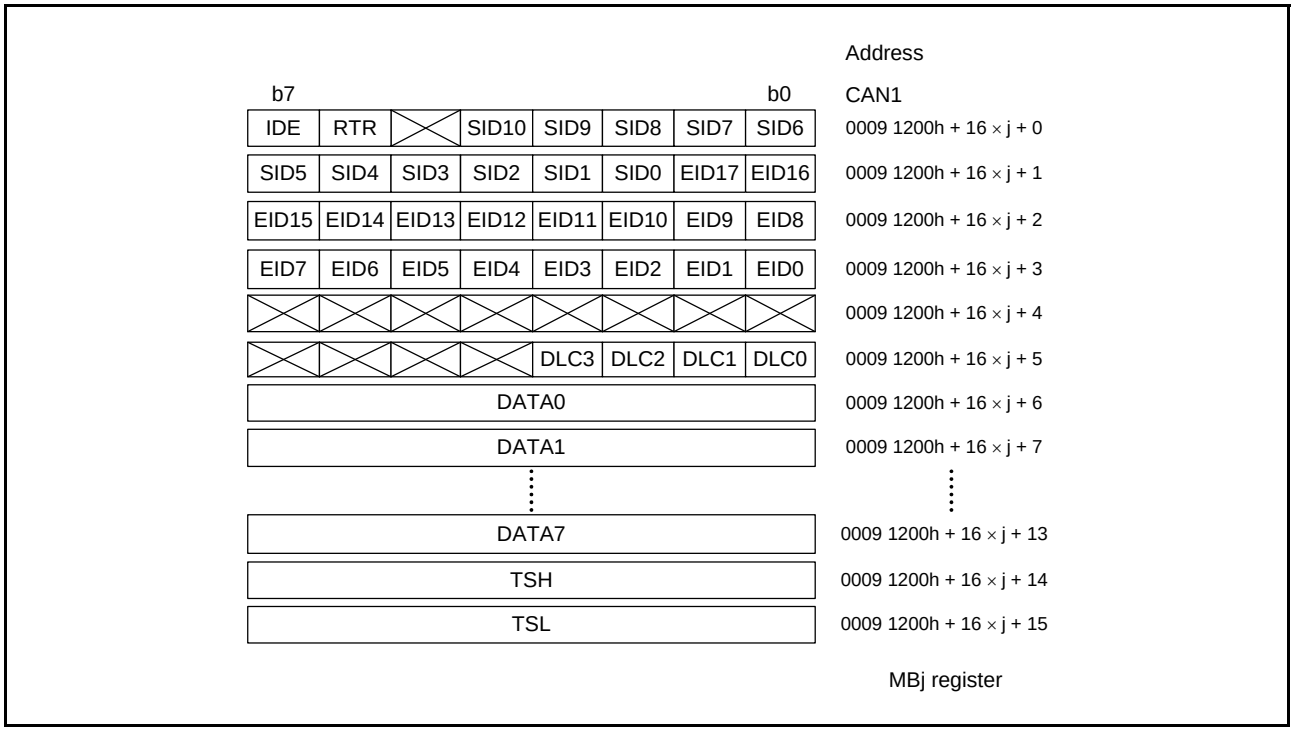


Figure 31.13 Structure of MBj (j = 0 to 31)

Figure 31.14 shows the structure of MKRk.
There are eight mask registers with the same structure.

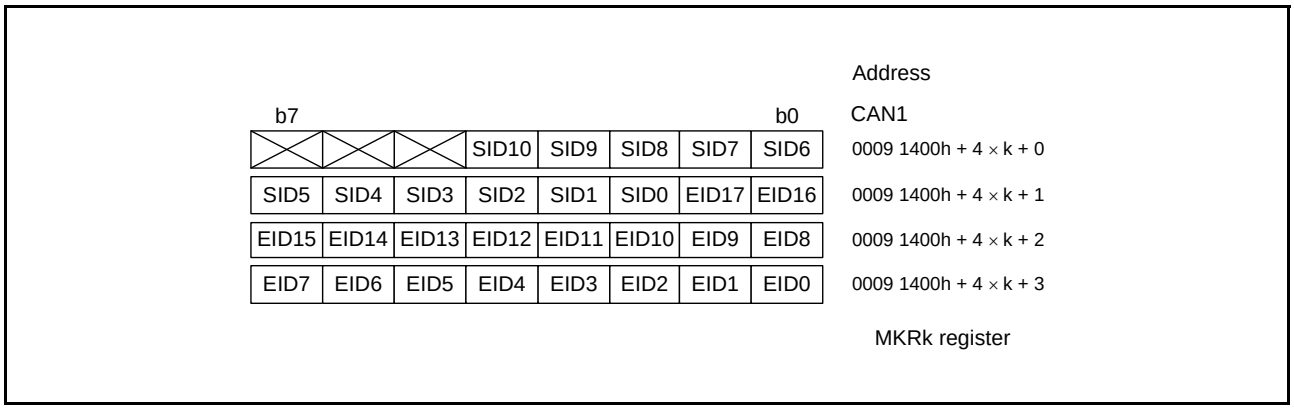


Figure 31.14 Structure of MKRk (k = 0 to 7)

Figure 31.15 shows the structure of FIDCR0 and FIDCR1.
There are two FIFO received ID compare registers with the same structure.

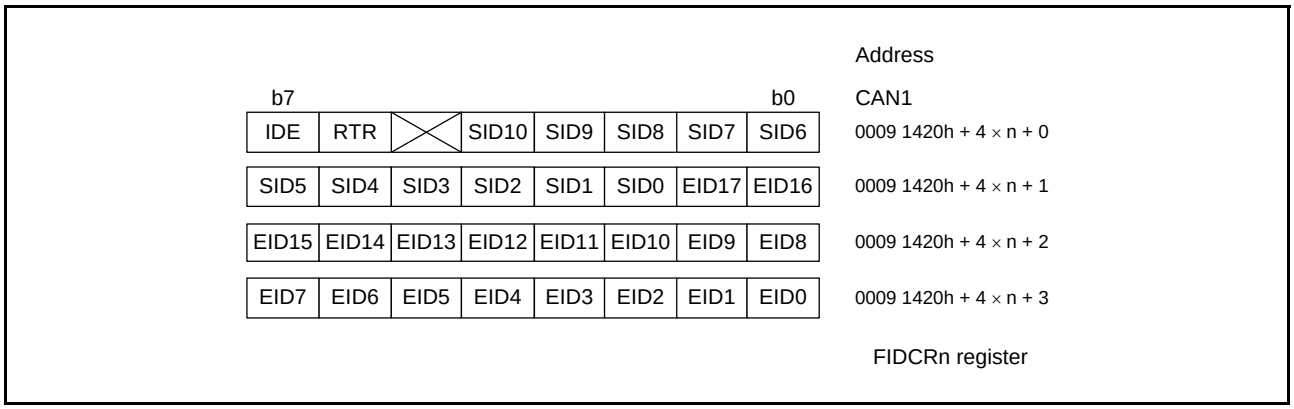


Figure 31.15 Structure of FIDCRn (n = 0, 1)

31.6 Acceptance Filtering and Masking Functions

The acceptance filtering function and masking function allows the user to select and receive messages with a specified range of multiple IDs for mailboxes.
Registers MKR0 to MKR7 can perform masking of the standard ID and the extended ID of 29 bits.

- MKR0 corresponds to mailboxes [0] to [3]
- MKR1 corresponds to mailboxes [4] to [7]
- MKR2 corresponds to mailboxes [8] to [11]
- MKR3 corresponds to mailboxes [12] to [15]
- MKR4 corresponds to mailboxes [16] to [19]
- MKR5 corresponds to mailboxes [20] to [23]
- MKR6 corresponds to mailboxes [24] to [27] in normal mailbox mode and the receive FIFO mailboxes [28] to [31] in FIFO mailbox mode.
- MKR7 corresponds to mailboxes [28] to [31] in normal mailbox mode and the receive FIFO mailboxes [28] to [31] in FIFO mailbox mode.

MKIVLR disables acceptance filtering individually for each mailbox.
The IDE bit in MBj is valid when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).
The RTR bit in MBj selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes (mailboxes [0] to [23]) use the single corresponding register among MKR0 to MKR5 for acceptance filtering. Receive FIFO mailboxes (mailboxes [28] to [31]) use two registers MKR6 and MKR7 for acceptance filtering.
Also, the receive FIFO uses two registers FIDCR0 and FIDCR1 for ID comparison. Bits EID[17:0], SID[10:0], RTR, and IDE in MB28 to MB31 for the receive FIFO are disabled. As acceptance filtering depends on the result of two logic AND operations, two ranges of IDs can be received into the receive FIFO.
MKIVLR is disabled for the receive FIFO.

If both the standard ID and extended ID are set in the IDE bits in FIDCR0 and FIDCR1 individually, both ID formats are received.
If both the data frame and remote frame are set in the RTR bits in FIDCR0 and FIDCR1 individually, both data and remote frames are received.
When combination with two ranges of IDs is not necessary, set the same mask value and the same ID into both the FIFO ID and mask register.
Figure 31.16 shows the correspondence between mask registers and mailboxes. Figure 31.17 shows acceptance filtering.

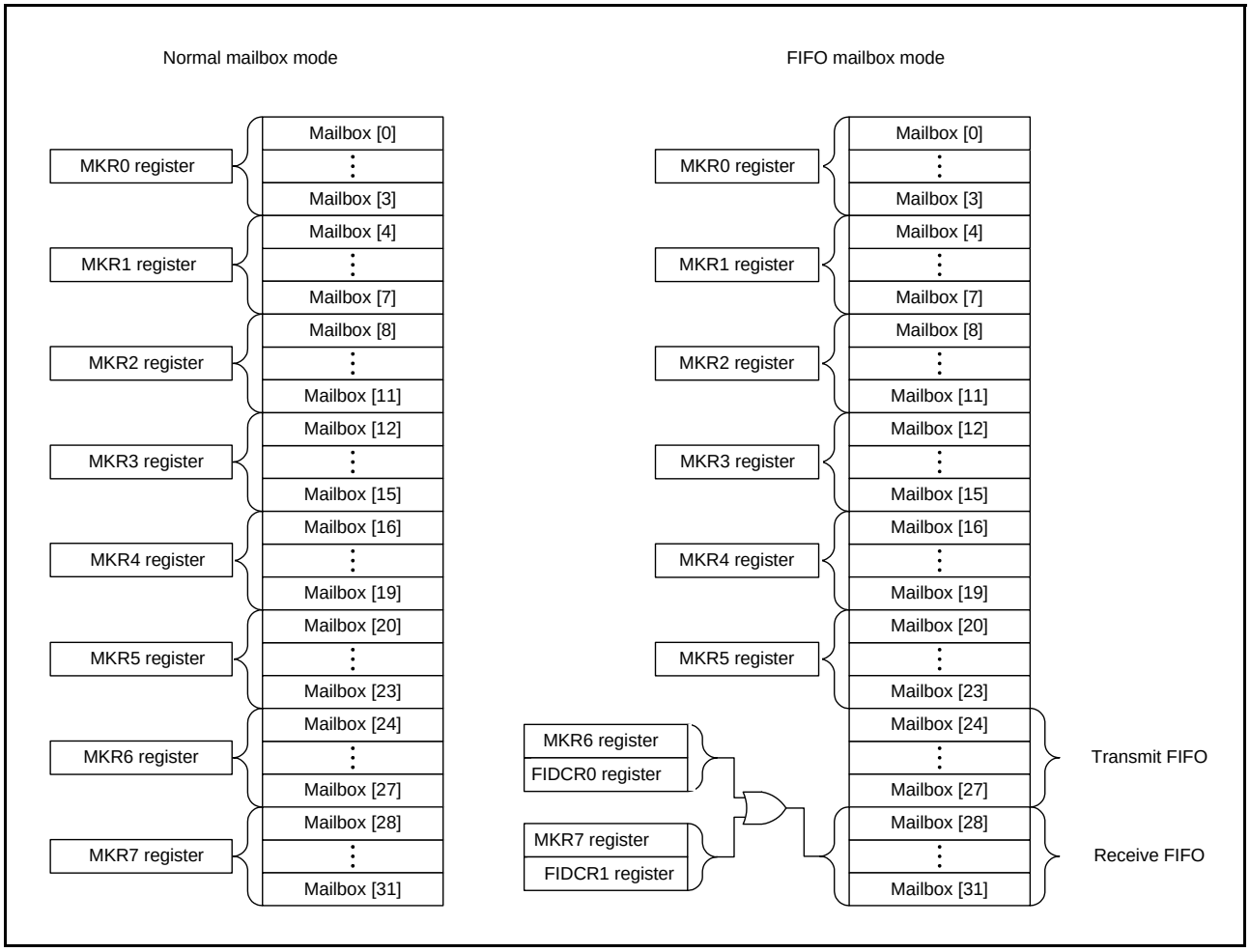
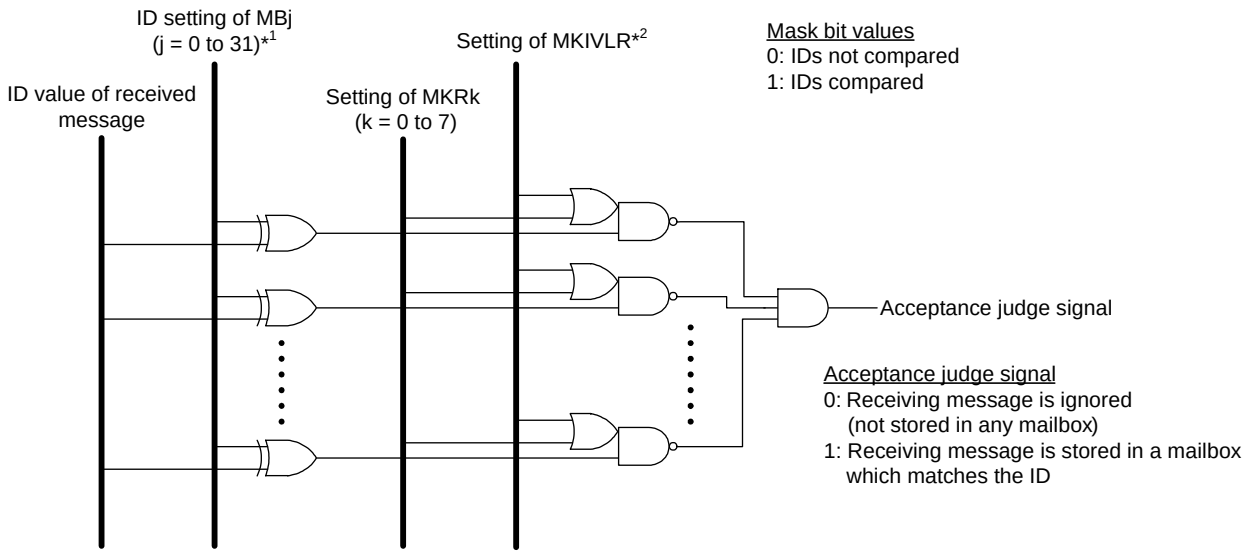


Figure 31.16 Correspondence between Mask Registers and Mailboxes



Note 1. The settings of FIDCR0 and FIDCR1 are used in FIFO mailbox mode.
Note 2. Invalid in FIFO mailboxes.

Figure 31.17 Acceptance Filtering

31.7 Reception and Transmission

Table 31.10 lists how to make the CAN communication mode settings.

Table 31.10 Setting of CAN Receive Mode and CAN Transmit Mode

MCTLj. TRMREQ	MCTLj. RECREQ	MCTLj. ONESHOT	Communication Mode of Mailbox
0	0	0	Mailbox disabled or transmission being aborted.
0	0	1	Can be configured only when transmission or reception from a mailbox programmed in one-shot mode is aborted.
0	1	0	Configured as a receive mailbox for a data frame or a remote frame.
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame.
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

j = 0 to 31

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, note the following:

1. Before a mailbox is configured as a receive mailbox or a one-shot receive mailbox, set MCTLj to 00h.
2. A received message is stored into the first mailbox that matches the condition according to the result of receive mode setting and acceptance filtering. Upon deciding the mailbox to store the received message, the mailbox with the smaller number has higher priority.
3. In CAN operation mode, when the CAN module transmits a message whose ID matches with the ID/mask set of a mailbox configured to receive messages, the CAN module never receives the transmitted data. In self-test mode, however, the CAN module will receive its transmitted data. In this case, the CAN module returns ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, note the following:

4. Before a mailbox is configured as a transmit mailbox or a one-shot transmit mailbox, ensure that MCTLj is 00h and that there is no pending abort process.

31.7.1 Reception

Figure 31.18 shows an operation example of data frame reception in overwrite mode.
This example shows the operation of overwriting the first message when the CAN module receives two consecutive CAN messages which match the receiving conditions of MCTLj (j = 0 to 31).

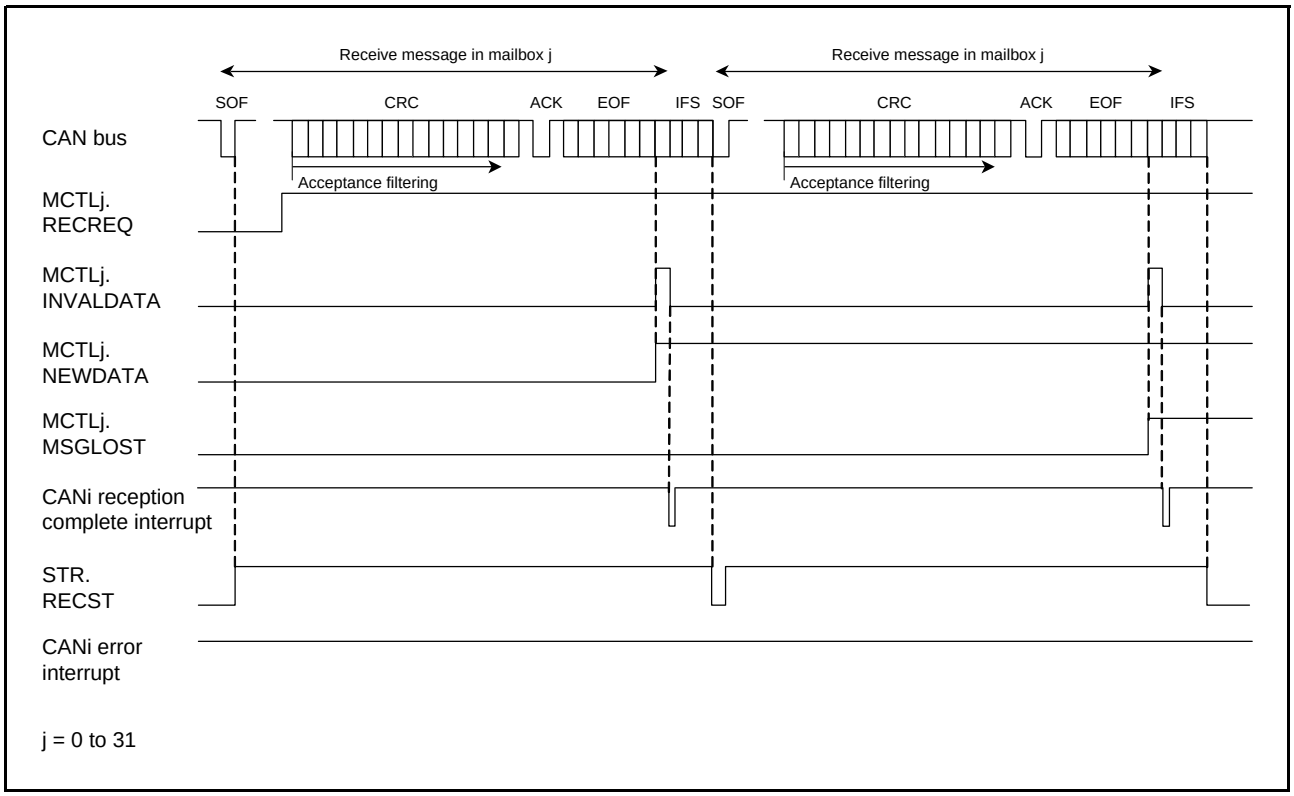


Figure 31.18 Operation Example of Data Frame Reception in Overwrite Mode

1. When an SOF is detected on the CAN bus, the RECST bit in STR is set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
2. The acceptance filter processing starts at the beginning of the CRC field to select the receive mailbox.
3. After a message has been received, the NEWDATA bit in MCTLj for the receive mailbox is set to 1 (new message is being stored or has been stored to the mailbox). The INVALDATA bit in MCTLj is set to 1 (message is being updated) at the same time, and then the INVALDATA bit is set to 0 (message valid) again after the complete message is transferred to the mailbox.
4. When the interrupt enable bit in MIER for the receive mailbox is 1 (interrupt enabled), the CANi reception complete interrupt request is generated. This interrupt (CANi reception complete interrupt) is generated when the INVALDATA bit is set to 0.
5. After reading the message from the mailbox, the NEWDATA bit needs to be set to 0 by a program.
6. In overwrite mode, if the next CAN message has been received into a mailbox whose NEWDATA bit is still set to 1, the MSGLOST bit in MCTLj is set to 1 (message has been overwritten). The new received message is transferred to the mailbox. The CANi reception complete interrupt request is generated the same as in 4.

Figure 31.19 shows the operation example of data frame reception in overrun mode.
This example shows the operation of overrunning the second message when the CAN module receives two consecutive CAN messages which match the receiving conditions of MCTLj (j = 0 to 31).

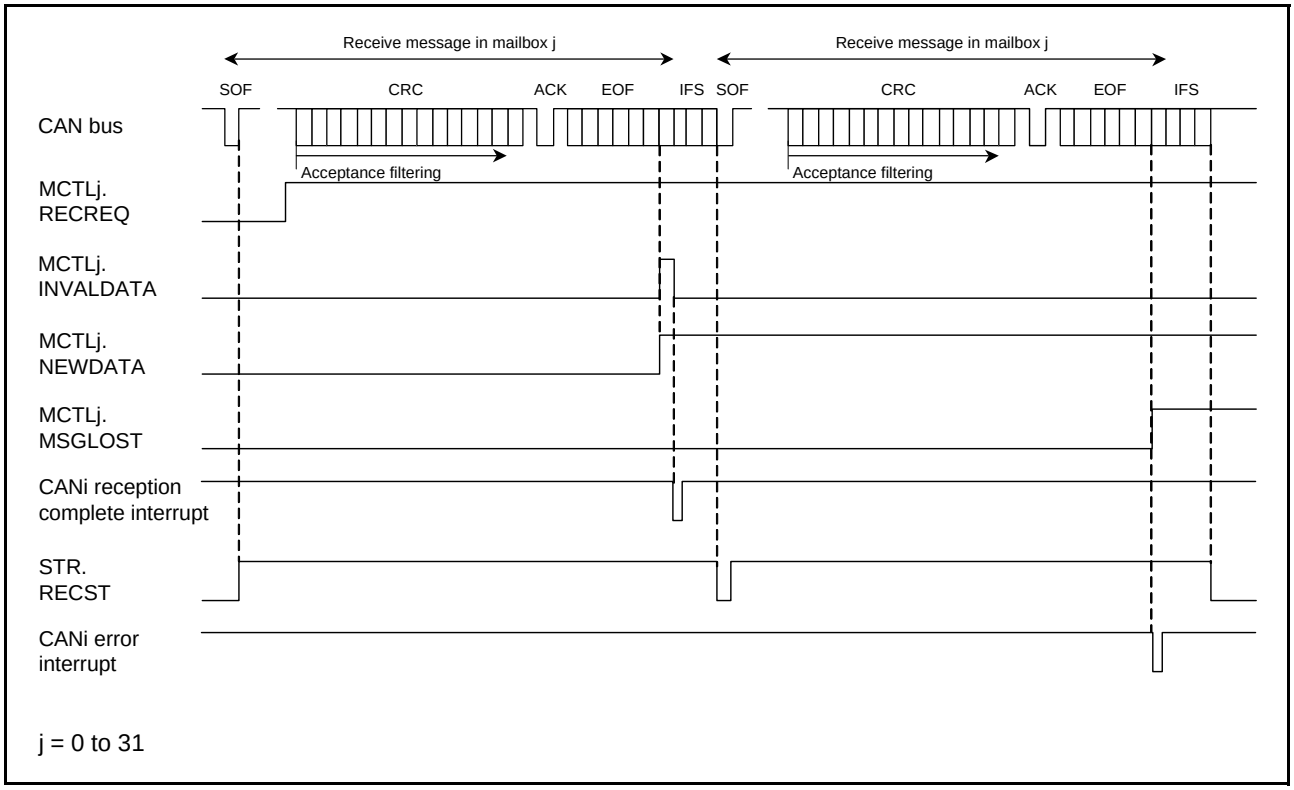


Figure 31.19 Operation Example of Data Frame Reception in Overrun Mode

1. to 5. are the same as in overwrite mode.

6. In overrun mode, if the next CAN message has been received before the NEWDATA bit in MCTLj is set to 0, the MSGLOST bit in MCTLj is set to 1 (message has been overrun). The new received message is discarded and a CANi error interrupt request is generated if the corresponding interrupt enable bit in EIER is set to 1 (interrupt enabled).

31.7.2 Transmission

Figure 31.20 shows an operation example of data frame transmission.

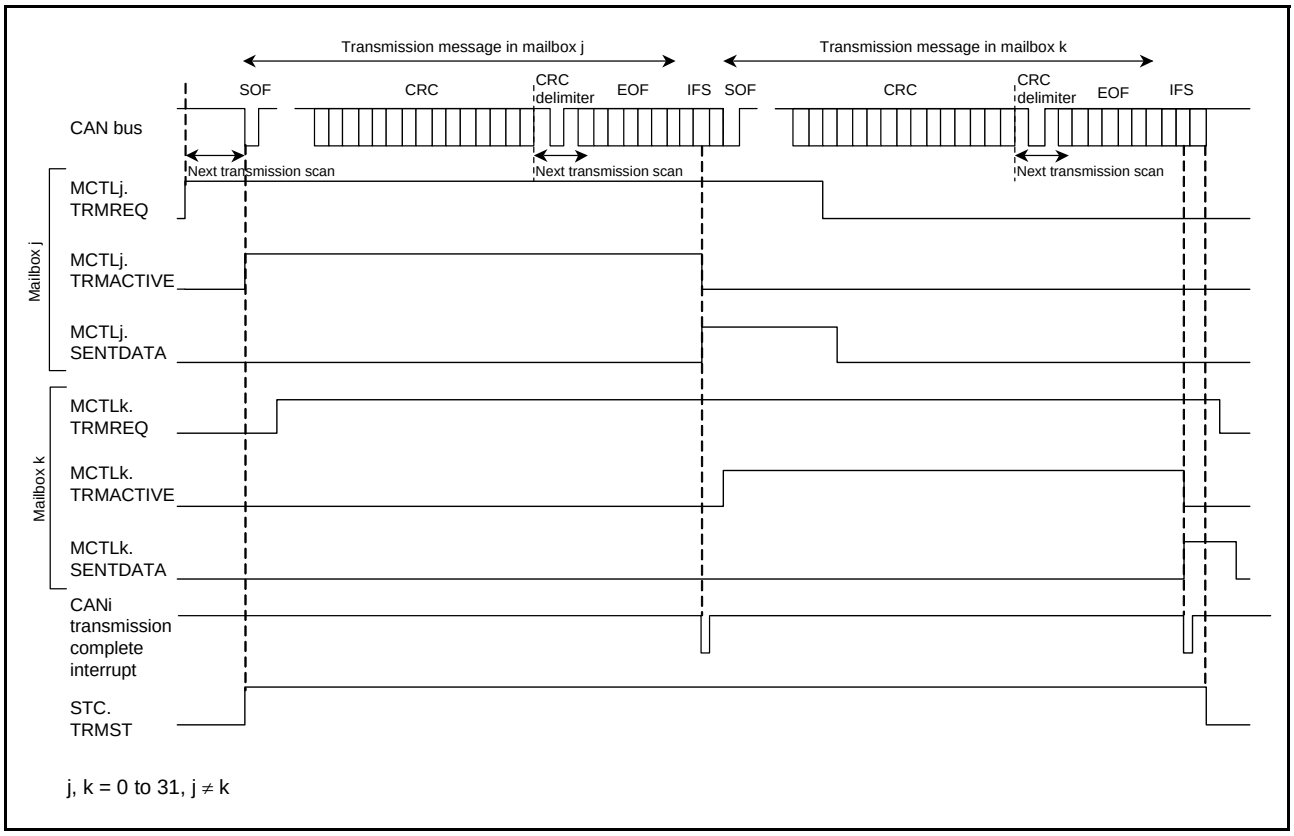


Figure 31.20 Operation Example of Data Frame Transmission

1. When a TRMREQ bit in MCTLj (j = 0 to 31) is set to 1 (transmit mailbox) in the bus-idle state, the mailbox scan processing starts to decide the highest-priority mailbox for transmission. Once the transmit mailbox is decided, the TRMACTIVE bit in MCTLj is set to 1 (from acceptance of transmission request to completion of transmission, or error/arbitration-lost), the TRMST bit in STR is set to 1 (transmission in progress), and the CAN module starts transmission.*1
2. If other TRMREQ bits are set, the transmission scan processing starts with the CRC delimiter for the next transmission.
3. If transmission is completed without losing arbitration, the SENTDATA bit in MCTLj is set to 1 (transmission completed) and the TRMACTIVE bit is set to 0 (transmission is pending or transmission is not requested). If the interrupt enable bit in MIER is 1 (interrupt enabled), the CANi transmission complete interrupt request is generated.
4. When requesting the next transmission from the same mailbox, set bits SENTDATA and TRMREQ to 0, then set the TRMREQ bit to 1 after checking that bits SENTDATA and TRMREQ have been set to 0.

Note 1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE bit is set to 0. The transmission scan processing is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following the arbitration-lost, the transmission scan processing is performed again to search for the highest-priority transmit mailbox from the start of the error delimiter.

31.8 CAN Interrupt

The CAN module provides the following CAN interrupts for each channel. Table 31.11 lists CAN interrupts.

- CAN reception complete interrupt (mailboxes 0 to 31) [RXMi]
- CAN transmission complete interrupt (mailboxes 0 to 31) [TXMi]
- CAN receive FIFO interrupt [RXFi]
- CAN transmit FIFO interrupt [TXFi]
- CAN error interrupt [ERSi]

There are eight types of interrupt sources for the CANi error interrupts. These sources can be determined by checking EIFR.

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock

Table 31.11 CAN Interrupts

Module	Interrupt Symbol	Interrupt Source	Source Flag
CANi	ERSi	Bus lock detected	EIFR.BLIF
		Overload frame transmission detected	EIFR.OLIF
		Overrun detected	EIFR.ORIF
		Bus-off recovery detected	EIFR.BORIF
		Bus-off entry detected	EIFR.BOEIF
		Error-passive detected	EIFR.EPIF
		Error-warning detected	EIFR.EWIF
		Bus error detected	EIFR.BEIF
	RXFi	Receive FIFO message received (MIER[29] = 0)	RFCR.RFUST[2:0]
		Receive FIFO warning (MIER[29] = 1)	
	TXFi	Transmit FIFO message transmission completed (MIER[25] = 0)	TFCR.TFUST[2:0]
		FIFO last message transmission completed (MIER[25] = 1)	
	RXMi	Mailbox 0 to 31 message received	MCTL0.NEWDATA to MCTL31.NEWDATA
	TXMi	Mailbox 0 to 31 message transmission completed	MCTL0.SENTDATA to MCTL31.SENTDATA

i = 2

31.9 Usage Notes

31.9.1 Setting for the Module-Stop State

Module stop control register B (MSTPCRB) can be used to enable or disable operation of the CAN module. The CAN module is stopped at the initial value. The registers become accessible on release from the module-stop state. For details, refer to section 12, Low Power Consumption.

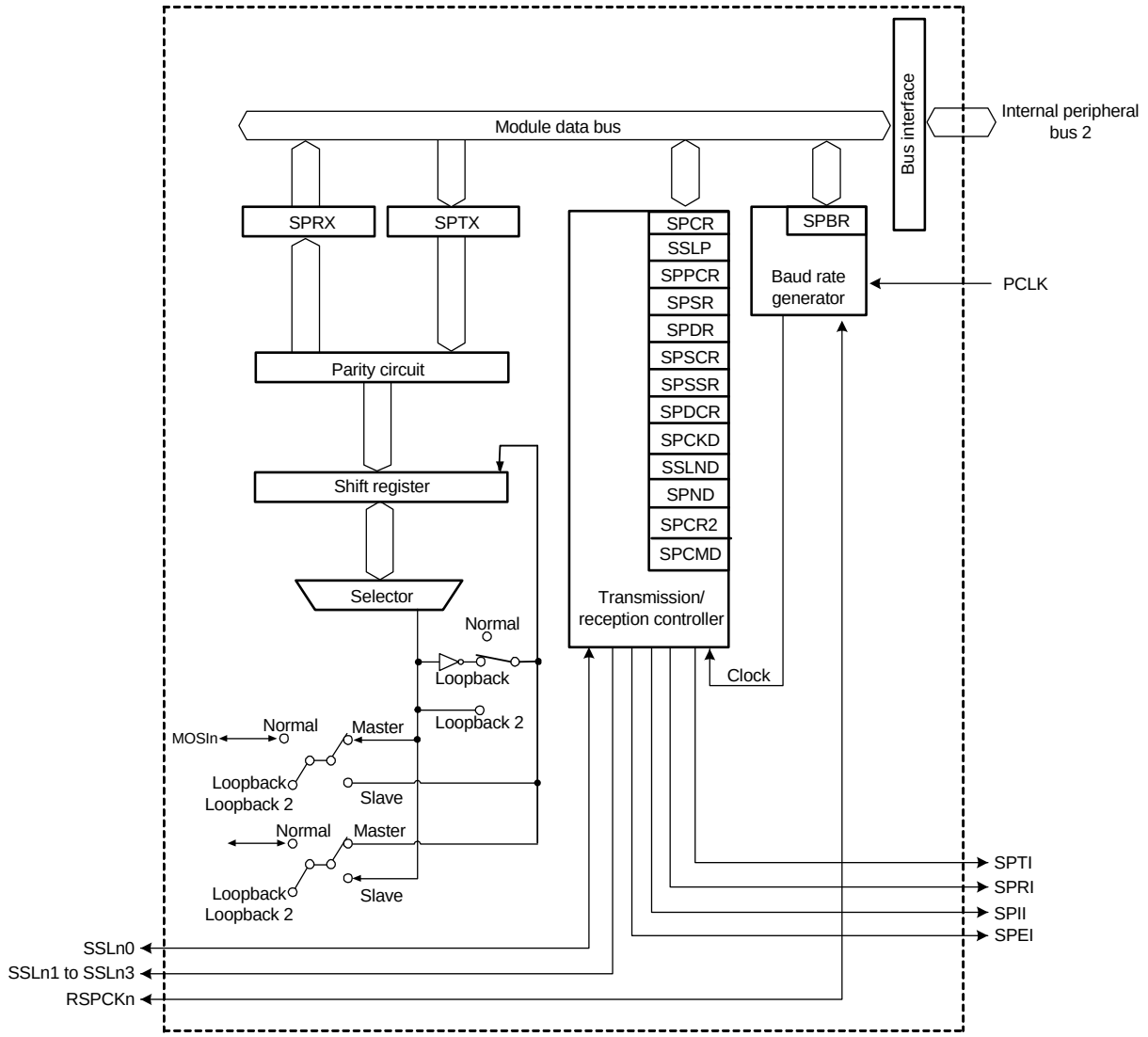
32. Serial Peripheral Interface (RSPI)

32.1 Overview

This MCU Group includes two independent channels of Serial Peripheral Interface (RSPI).
The RSPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices.
Table 32.1 lists the specifications of the RSPI, and Figure 32.1 shows a block diagram of the RSPI.
Furthermore, n in this section indicates A or B, and i indicates 0 to 3. Also, m as used with the RSPI command registers (SPCMDm) indicates 0 to 7.

Table 32.1 Specifications of RSPI

Item	Description
Number of channels	Two channels
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Transmit-only operation is available. • Capable of serial communications in master/slave mode • Switching of the polarity of the serial transfer clock • Switching of the phase of the serial transfer clock
Data format	• MSB-first/LSB-first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (Division ratio: 2 to 4096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is that of PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK
Buffer configuration	Double buffer configuration for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection
SSL control function	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 signals are output. • In multi-master mode: SSLn0 signal for input, and SSLn1 to SSLn3 signals for either output or unused. • In slave mode: SSLn0 signal for input, and SSLn1 to SSLn3 signals for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation
Interrupt sources	• Maskable interrupt sources RSPI receive interrupt (receive buffer full) RSPI transmit interrupt (transmit buffer empty) RSPI error interrupt (mode fault, overrun, parity error) RSPI idle interrupt (RSPI idle)
Others	• Function for initializing the RSPI • Loopback mode
Power consumption reducing function	Module-stop state can be set.



SPCR: RSPI control register
SPCR2: RSPI control register 2
SSLP: RSPI slave select polarity register
SPPCR: RSPI pin control register
SPSR: RSPI status register
SPDR: RSPI data register
SPSCR: RSPI sequence control register
SPSSR: RSPI sequence status register
SPDCR: RSPI data control register
SPCKD: RSPI clock delay register
SSLND: RSPI slave select negation delay register
SPND: RSPI next-access delay register
SPCMD: RSPI command registers 0 to 7 (eight registers)
SPBR: RSPI bit rate register
SPTX: RSPI transmit buffer
SPRX: RSPI receive buffer
SPTI: RSPI transmit interrupt
SPRI: RSPI receive interrupt
SPII: SPI idle interrupt
SPEI: RSPI error interrupt

Figure 32.1 Block Diagram of RSPI

Table 32.2 lists the input and output pins used in the RSPI.
The RSPI automatically switches the input/output direction of the SSLn0 pin (n = A or B). SSLn0 is set as an output when the RSPI is a single master and as an input when the RSPI is a multi-master or a slave. Pins RSPCKn, MOSIn, and MISOn (n = A or B) are automatically set as inputs or outputs according to the setting of master or slave and the level input on the SSLn0 pin (see section 32.3.2, Controlling RSPI Pins).

Table 32.2 RSPI Pin Configuration

Channel	Pin Name	I/O	Function
RSPI0	RSPCKA	I/O	Clock I/O pin
	MOSIA	I/O	Master transmit data I/O pin
	MISOA	I/O	Slave transmit data I/O pin
	SSLA0	I/O	Slave selection I/O pin
	SSLA1	Output	Slave selection output pin
	SSLA2	Output	Slave selection output pin
	SSLA3	Output	Slave selection output pin
RSPI1	RSPCKB	I/O	Clock I/O pin
	MOSIB	I/O	Master transmit data I/O pin
	MISOB	I/O	Slave transmit data I/O pin
	SSLB0	I/O	Slave selection I/O pin
	SSLB1	Output	Slave selection output pin
	SSLB2	Output	Slave selection output pin
	SSLB3	Output	Slave selection output pin

32.2 Register Descriptions

32.2.1 RSPI Control Register (SPCR)

Address(es): RSPI0.SPCR 0008 8380h, RSPI1.SPCR 0008 83A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPMS	RSPI Mode Select	0: SPI operation (four-wire method) 1: Clock synchronous operation (three-wire method)	R/W
b1	TXMD	Communications Operating Mode Select	0: Full-duplex synchronous serial communications 1: Serial communications consisting of only transmit operations	R/W
b2	MODFEN	Mode Fault Error Detection Enable	0: Disables the detection of mode fault error 1: Enables the detection of mode fault error	R/W
b3	MSTR	RSPI Master/Slave Mode Select	0: Slave mode 1: Master mode	R/W
b4	SPEIE	RSPI Error Interrupt Enable	0: Disables the generation of RSPI error interrupt requests 1: Enables the generation of RSPI error interrupt requests	R/W
b5	SPTIE	RSPI Transmit Buffer Empty Interrupt Enable	0: Disables the generation of RSPI transmit interrupt requests 1: Enables the generation of RSPI transmit interrupt requests	R/W
b6	SPE	RSPI Function Enable	0: Disables the RSPI function 1: Enables the RSPI function	R/W
b7	SPRIE	RSPI Receive Buffer Full Interrupt Enable	0: Disables the generation of RSPI receive interrupt requests 1: Enables the generation of RSPI receive interrupt requests	R/W

If the SPCR.MSTR, SPCR.MODFEN, and SPCR.TXMD bits are changed while the SPCR.SPE bit is 1, subsequent operations cannot be guaranteed.

SPMS Bit (RSPI Mode Select)

The SPMS bit selects SPI operation (four-wire method) or clock synchronous operation (three-wire method).
The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The three pins RSPCKn, MOSIn, and MISOn handle communications. If clock-synchronous operation is to proceed in master mode (SPCR.MSTR = 1), the SPCMDm.CPHA bit can be set to either 0 or 1. Set the CPHA bit to 1 if clock-synchronous operation is to proceed in slave mode (SPCR.MSTR = 0). Operation is not guaranteed if the CPHA bit is set to 0 when clock-synchronous operation is to proceed in slave mode (SPCR.MSTR = 0).

TXMD Bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit operations only.
When performing communications with the TXMD bit set to 1, the RSPI performs only transmit operations and not receive operations (see section 32.3.6, Communications Operating Mode).
When the TXMD bit is set to 1, receive buffer full interrupt requests cannot be used.

MODFEN Bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault error (see section 32.3.8, Error Detection). In addition, the RSPI determines the input/output direction of the SSLn0 to SSLn3 pins based on combinations of the MODFEN and MSTR bits (see section 32.3.2, Controlling RSPI Pins).

MSTR Bit (RSPI Master/Slave Mode Select)

The MSTR bit selects master/slave mode of the RSPI. According to MSTR bit settings, the RSPI determines the direction of pins RSPCKn, MOSIn, MISOn, and SSLn0 to SSLn3.

SPEIE Bit (RSPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of RSPI error interrupt requests when the RSPI detects a mode fault error and sets the SPSR.MODF flag to 1, when the RSPI detects an overrun error and sets the SPSR.OVRF flag to 1, or when the RSPI detects a parity error and sets the SPSR.PERF flag to 1 (see section 32.3.8, Error Detection).

SPTIE Bit (RSPI Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of RSPI transmit buffer empty interrupt requests when the RSPI detects transmit buffer empty.

At the beginning of transmission, the transmit buffer empty interrupt requests are generated by setting the SPE bit to 1 at the same time or after the SPTIE bit has been set to 1.

Therefore, note that even while the RSPI function is disabled (SPE bit is 0), setting the SPTIE bit to 1 will generate an RSPI transmit buffer empty interrupt request.

SPE Bit (RSPI Function Enable)

The SPE bit enables or disables the RSPI function.

When the SPSR.MODF bit is 1, the SPE bit cannot be set to 1. For details, refer to section 32.3.8, Error Detection.

Setting the SPE bit to 0 disables the RSPI function, and initializes a part of the module function. For details, refer to section 32.3.9, Initializing RSPI. Furthermore, an RSPI transmission interrupt request is generated by the state of the SPE bit changing from 0 to 1 or from 1 to 0.

SPRIE Bit (RSPI Receive Buffer Full Interrupt Enable)

If the RSPI has detected a receive buffer full write after completion of a serial transfer, the SPRIE bit enables or disables the generation of an RSPI receive buffer full interrupt request.

32.2.2 RSPI Slave Select Polarity Register (SSLP)

Address(es): RSPI0.SSLP 0008 8381h, RSPI1.SSLP 0008 83A1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SSL0P	SSL0 Signal Polarity Setting	0: SSL0 signal is active low 1: SSL0 signal is active high	R/W
b1	SSL1P	SSL1 Signal Polarity Setting	0: SSL1 signal is active low 1: SSL1 signal is active high	R/W
b2	SSL2P	SSL2 Signal Polarity Setting	0: SSL2 signal is active low 1: SSL2 signal is active high	R/W
b3	SSL3P	SSL3 Signal Polarity Setting	0: SSL3 signal is active low 1: SSL3 signal is active high	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not execute the subsequent operations if the contents of SSLP are changed while the SPCR.SPE bit is 1.

32.2.3 RSPI Pin Control Register (SPPCR)

Address(es): RSPI0.SPPCR 0008 8382h, RSPI1.SPPCR 0008 83A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	SPOM	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPLP	RSPI Loopback	0: Normal mode 1: Loopback mode (reversed transmit data = receive data)	R/W
b1	SPLP2	RSPI Loopback 2	0: Normal mode 1: Loopback mode (transmit data = receive data)	R/W
b2	SPOM	RSPI Output Pin Mode	[In 144-, 120-, 112-, and 100-pin versions] 0: CMOS output 1: Open-drain output [In 64- and 48-pin versions] 0: CMOS output 1: Setting prohibited	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: The level output on the MOSIn pin during MOSI idling is low. 1: The level output on the MOSIn pin during MOSI idling is high.	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: MOSI output value equals final data from previous transfer 1: MOSI output value equals the value set in the MOIFV bit	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not execute the subsequent operations if the contents of SPPCR are changed while the SPCR.SPE bit is 1.

SPLP Bit (RSPI Loopback)

The SPLP bit selects the mode of the RSPI pins.

When the SPLP bit is set to 1, the RSPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects (reverses) the input path and output path for the shift register (loopback mode).

SPLP2 Bit (RSPI Loopback 2)

The SPLP2 bit selects the mode of the RSPI pins.

When the SPLP2 bit is set to 1, the RSPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path for the shift register (loopback mode).

SPOM Bit (RSPI Output Pin Mode)

For 144-, 120-, 112-, and 100-pin products, the SPOM bit selects CMOS output or open-drain output as the form of output from the RSPI pin. For 64- and 48-pin products, leave this bit at its initial value.

MOIFV Bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIn pin output value during the SSL negation period (including the SSL retention period during a burst transfer).

MOIFE Bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the RSPI in master mode is in an SSL negation period (including the SSL retention period during a burst transfer). When the MOIFE bit is 0, the RSPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the RSPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

32.2.4 RSPI Status Register (SPSR)

Address(es): RSPI0.SPSR 0008 8383h, RSPI1.SPSR 0008 83A3h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	—	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OVRF	Overrun Error Flag	0: No overrun error occurs 1: An overrun error occurs	R/(W) *1
b1	IDLNF	RSPI Idle Flag	0: RSPI is in the idle state 1: RSPI is in the transfer state	R
b2	MODF	Mode Fault Error Flag	0: No mode fault error occurs 1: A mode fault error occurs	R/(W) *1
b3	PERF	Parity Error Flag	0: No parity error occurs 1: A parity error occurs	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	SPTEF	Transmit Buffer Empty Flag	0: Transmit buffer has valid data 1: Transmit buffer has no valid data	R/W*2
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	SPRF	Receive Buffer Full Flag	0: Receive buffer has no valid data 1: Receive buffer has valid data	R/W*2

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Write 1 when writing is necessary.

OVRF Flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error.

[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the receive buffer holds data that has not yet been read

[Clearing condition]

- When SPSR is read while the OVRF flag is 1, and then writes the value 0 to the OVRF flag.

IDLNF Flag (RSPI Idle Flag)

The IDLNF flag indicates the transfer status of the RSPI.

[Setting condition]

<Master mode>

- Of the conditions in master mode under “Clearing condition” below, condition 1 not being fulfilled or none of the second to fourth clearing conditions (condition 2) being fulfilled.

<Slave mode>

- The SPCR.SPE bit is 1 (RSPI function is enabled)

[Clearing condition]

<Master mode>

- The flag is cleared to 0 when the following first clearing condition (condition 1) is satisfied or all of the second to fourth clearing conditions (condition 2) are satisfied.

1. The SPCR.SPE bit is 0 (RSPI is initialized)
2. The transmit buffer (SPTX) is empty (data for the next transfer is not set)
3. The SPSSR.SPCP[2:0] bits are 000b (beginning of sequence control)
4. The RSPI internal sequencer has entered the idle state (status in which operations up to the next-access delay have finished)

<Slave mode>

- The SPCR.SPE bit is 0 (RSPI is initialized)

MODF Flag (Mode Fault Error Flag)

Indicates the occurrence of a mode fault error.

[Setting condition]

<Multi-master mode>

- When the input level of the SSLni pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), the RSPI detects a mode fault error

<Slave mode>

- When the SSLni pin is negated before the RSPCK cycle necessary for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), the RSPI detects a mode fault error

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSL signal polarity setting bit).
In slave mode, communication should not be started from the master device when no transmit data is written. Otherwise, it may cause the mode fault flag to be set to 1 (mode-fault error).

[Clearing condition]

- When SPSR is read while the MODF flag is 1, and then writes the value 0 to the MODF flag

PERF Flag (Parity Error Flag)

Indicates the occurrence of a parity error.

[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1, the RSPI detects a parity error

[Clearing condition]

- When SPSR is read while the PERF flag is 1, and then writes the value 0 to the PERF flag

SPTEF Flag (Transmit Buffer Empty Flag)

Indicates whether the transmit buffer (SPTX) in RSPI data register has valid data.

[Setting condition]

- When the SPCR.SPE bit is 0 (disables RSPI function)
- When data is transferred from the transmit buffer to the shift register

[Clearing condition]

- When the number of frames of transmit data specified by SPDCR.SPFC[1:0] bits is written to the SPDR register.

The SPDR register can be set only when the SPTEF flag is 1. The data in the transmit buffer is not updated when the SPDR register is set while the SPTEF flag is 0.

SPRF Flag (Receive Buffer Full Flag)

Indicates whether the receive buffer (SPRX) in the RSPI data register has valid data.

[Setting condition]

- When the number of frames of receive data specified by the SPDCR.SPFC[1:0] bits is transferred from shift register to the receive buffer (SPRX) while the SPCR.TXMD bit is 0 (full duplex) and the SPRF flag is 0.
  Note that the SPRF flag does not become 1 when the OVRF flag is 1.

[Clearing condition]

- When all of the received data are read from the SPDR register

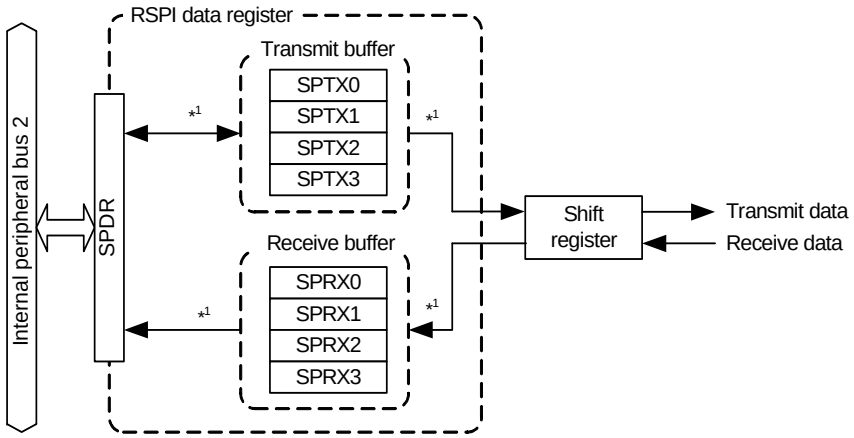
32.2.5 RSPI Data Register (SPDR)

Address(es): RSPI0.SPDR 0008 8384h, RSPI1.SPDR 0008 83A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SPD31	SPD30	SPD29	SPD28	SPD27	SPD26	SPD25	SPD24	SPD23	SPD22	SPD21	SPD20	SPD19	SPD18	SPD17	SPD16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SPD15	SPD14	SPD13	SPD12	SPD11	SPD10	SPD9	SPD8	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDR is the interface with the buffers that hold data for transmission and reception by the RSPI. The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR. Figure 32.2 shows the Configuration of SPDR.



Note 1. The destination buffer and stage for access is automatically switched by hardware

Figure 32.2 Configuration of SPDR

The transmit and receive buffers have four stages each. The number of stages to be used is selectable by the number of frames specification bits in the RSPI data control register (SPDCR.SPFC[1:0]). The eight stages of the buffer are all mapped to the single address of SPDR.

Data written to SPDR are written to a transmit-buffer stage (SPTX0 to SPTX3) and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun is generated.

Furthermore, if the data length is other than 32 bits, bits not referred to in SPTXn (n = 0 to 3) are stored in the corresponding bits in SPRXn. For example, if the data length is nine bits, the SPTXn[31:9] bits are stored in SPRXn[31:9] (and received data are stored in the SPTXn[8:0] bits).

(1) Bus Interface

SPDR is the interface with 32-bit wide transmit and receive buffers, each of which has four stages, for a total of 32 bytes. In other words, the 32 bytes are mapped to the four-byte address space for SPDR. Furthermore, the unit of access for SPDR is selected by the RSPI longword access/word access specification bit in the RSPI data control register (SPDCR.SPLW).
Data for transmission should be flush with the LSB end of the register. Received data are stored flush with the LSB end. Operations involved in writing to and reading from SPDR are described below.

(a) Writing

Value can be written to the transmit buffer (SPTXn) by writing to SPDR.
Unlike reading from SPDR, it is not affected by the SPDCR.SPRDTD bit value.
The transmit buffer includes a transmit buffer write pointer which is automatically indicates the next buffer each time are written to SPDR.
Figure 32.3 shows the configuration of the bus interface with the transmit buffer in the case of writing to SPDR.

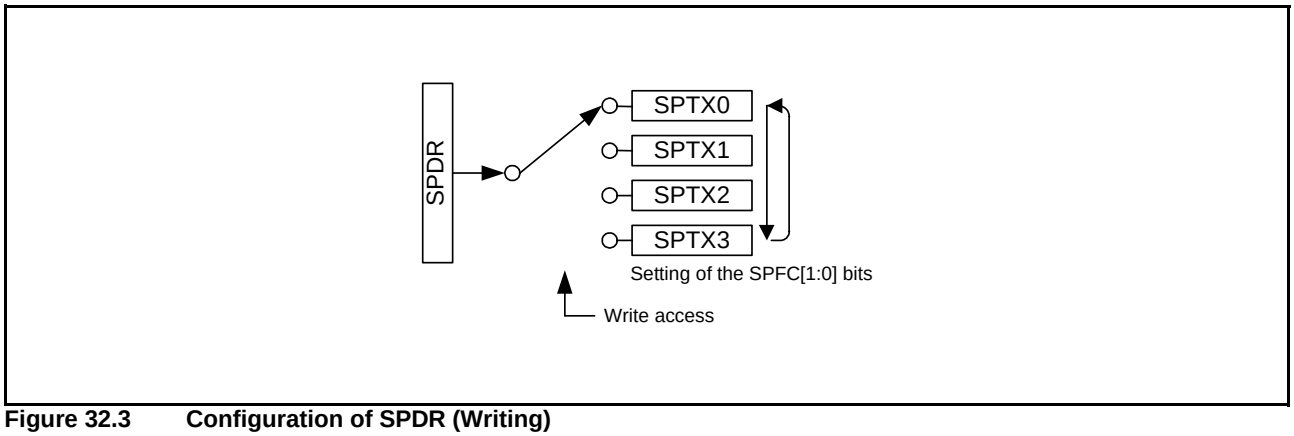


Figure 32.3 Configuration of SPDR (Writing)

The sequence for switching the transmit buffer write pointer differs with the setting of the number of frames specification bits in the RSPI data control register (SPDCR.SPFC[1:0]).

- Settings of the SPFC[1:0] bits and sequence of switching the pointer among SPTX0 to SPTX03.
  When the SPFC[1:0] bits are 00b: SPTX0 → SPTX0 → SPTX0 → …
  When the SPFC[1:0] bits are 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the RSPI function enable bit in the RSPI control register (SPCR.SPE) while the bit's current value is 0, SPTX0 will be the destination the next time writing proceeds.
When writing to the transmit buffer (SPTXn), after generation of the transmit buffer empty interrupt, write the number of frames set by the number of frames specification bits SPFC[1:0] in the RSPI data control register SPDCR.
The value in the transmit buffer (SPTXn) is not updated by writing during the period from completion of writing to a generation of next transmit buffer empty interrupt.

(b) Reading

SPDR can be read to read out the value of a receive buffer (SPRXn; n = 0 to 3) or a transmit buffer (SPTXn; n = 0 to 3). The setting of the RSPI receive/transmit data selection bit in the RSPI data control register (SPDCR.SPRDTD) selects whether reading is of the receive or transmit buffer.

The structure of the SPDR when it is read includes two independent pointers (receive buffer read pointer and transmit buffer read pointer). Reading SPDR causes automatic updating of the pointer so that it indicates the next stage of the buffer.

Figure 32.4 shows the configuration of the bus interface with the receive and transmit buffers in the case of reading from SPDR.

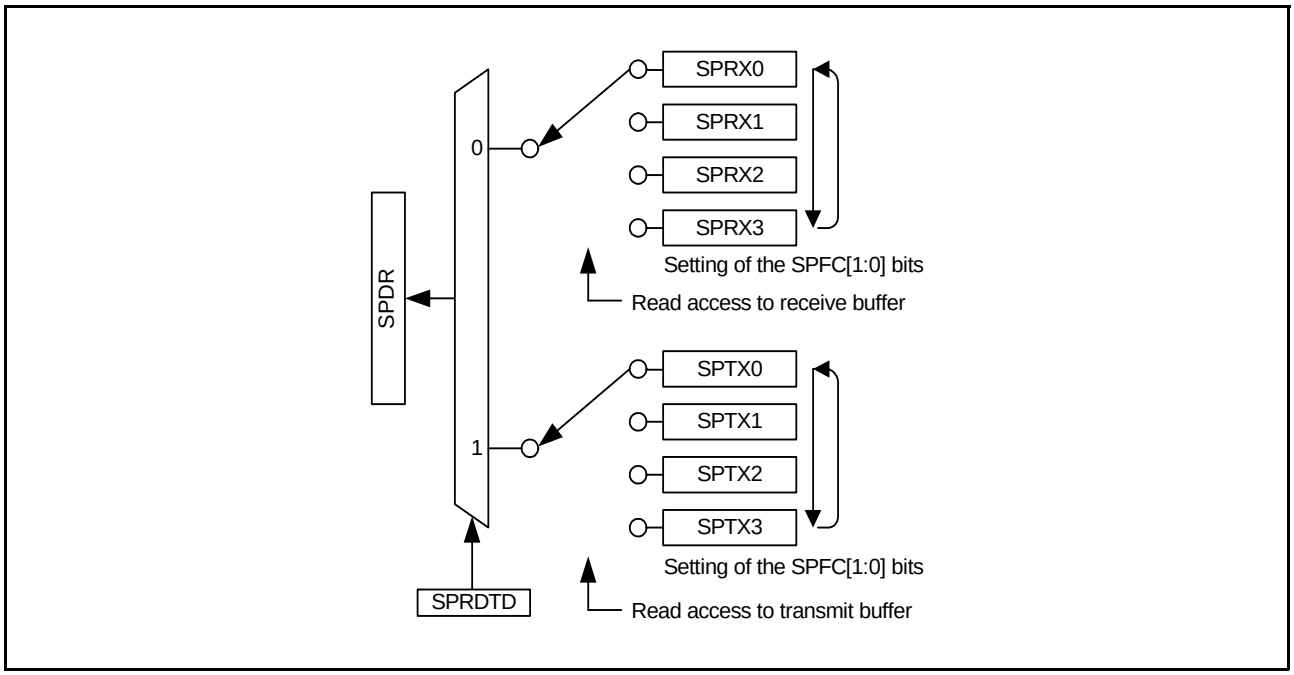


Figure 32.4 Configuration of SPDR (Reading)

After the receive buffer is read, the receive buffer read pointer is automatically switched to point the next buffer.

The sequence for switching the receive buffer read pointer is the same as that for the transmit buffer write pointer.

Note, however, that the next buffer to be read is SPRX0 when 1 is written to the RSPI function enable bit in the RSPI control register (SPCR.SPE) while the current bit value is 0.

The transmit buffer read pointer is updated when writing to SPDR and not updated when reading from the transmit buffer.

When the transmit buffer is read, the last value written to SPDR is returned.

After generation of the RSPI transmit interrupt,

if the transmit buffer is read in the interval after writing of the number of frames of data for transmission specified in the number of frames specification bits (SPFC[1:0]) in the RSPI data control register (SPDCR)

and before the next RSPI transmit interrupt, all bits of the value read out are 0.

32.2.6 RSPI Sequence Control Register (SPSCR)

Address(es): RSPI0.SPSCR 0008 8388h, RSPI1.SPSCR 0008 83A8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPSLN[2:0]	RSPI Sequence Length Specification	b2 b0 Sequence Length — Referenced SPCMD0 to SPCMD7 (No.) 0 0 0: 1 — 0→0→… 0 0 1: 2 — 0→1→0→… 0 1 0: 3 — 0→1→2→0→… 0 1 1: 4 — 0→1→2→3→0→… 1 0 0: 5 — 0→1→2→3→4→0→… 1 0 1: 6 — 0→1→2→3→4→5→0→… 1 1 0: 7 — 0→1→2→3→4→5→6→0→… 1 1 1: 8 — 0→1→2→3→4→5→6→7→0→… SPCMD0 to SPCMD7 to be referenced and the order in which they are referenced are changed according to the sequence length that is set in these bits. The relationship among the setting of these bits, sequence length, and SPCMD0 to SPCMD7 registers referenced by the RSPI is shown above. However, the RSPI in slave mode always references SPCMD0.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPSCR sets the sequence length when the RSPI operates in master mode. When changing the SPSCR.SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, the bits should be changed while the SPSR.IDLNF flag is 0.

SPSLN[2:0] Bits (RSPI Sequence Length Specification)

The SPSLN[2:0] bits specify a sequence length when the RSPI in master mode performs sequential operations. The RSPI in master mode changes SPCMD0 to SPCMD7 registers to be referenced and the order in which they are referenced according to the sequence length that is set in the SPSLN[2:0] bits.
In slave mode, SPCMD0 is always referred to.

32.2.7 RSPI Sequence Status Register (SPSSR)

Address(es): RSPI0.SPSSR 0008 8389h, RSPI1.SPSSR 0008 83A9h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPECM[2:0]			—	SPCP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPCP[2:0]	RSPI Command Pointer	b2 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
b3	—	Reserved	This bit is read as 0.	R
b6 to b4	SPECM[2:0]	RSPI Error Command	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
b7	—	Reserved	This bit is read as 0.	R

SPSSR indicates the sequence control status when the RSPI operates in master mode.
Any writing to SPSSR is ignored.

SPCP[2:0] Bits (RSPI Command Pointer)

The SPCP[2:0] bits indicate SPCMDm that is currently pointed to by the pointer during sequence control by the RSPI. For the RSPI's sequence control, see section 32.3.10.1, Master Mode Operation.

SPECM[2:0] Bits (RSPI Error Command)

The SPECM[2:0] bits indicate SPCMDm that is specified by the SPCP[2:0] bits when an error is detected during sequence control by the RSPI. The RSPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF bits are 0 and there is no error, the values of the SPECM[2:0] bits have no meaning. For the RSPI's error detection function, see section 32.3.8, Error Detection. For the RSPI's sequence control, see section 32.3.10.1, Master Mode Operation.

32.2.8 RSPI Bit Rate Register (SPBR)

Address(es): RSPI0.SPBR 0008 838Ah, RSPI1.SPBR 0008 83AAh

	b7	b6	b5	b4	b3	b2	b1	b0
	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0
Value after reset:	1	1	1	1	1	1	1	1

SPBR sets the bit rate in master mode. If the contents of SPBR are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, subsequent operations cannot be guaranteed.

When the RSPI is used in slave mode, the bit rate depends on the bit rate of the input clock (bit rate satisfying the electrical characteristics should be used) regardless of the settings of SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting bits).
The bit rate is determined by combinations of the SPBR setting and the SPCMDm.BRDV[1:0] bit setting. The equation for calculating the bit rate is given below. In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] bit setting (0, 1, 2, 3).

$$\text{Bit rate} = \frac{f(\text{PCLK})}{2 \times (n + 1)\, 2^{N}}$$

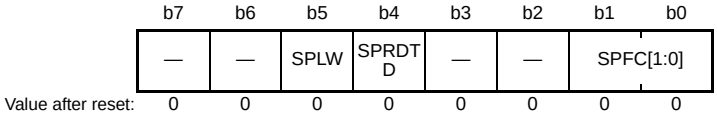
Table 32.3 lists examples of the relationship among the SPBR settings, the BRDV[1:0] settings, and bit rates.

Table 32.3 Relationship among SPBR Settings, BRDV[1:0] Settings, and Bit Rates

SPBR (n)	BRDV[1:0] Bits (N)	Division Ratio	Bit Rate			
			PCLK = 32 MHz	PCLK = 36 MHz	PCLK = 40 MHz	PCLK = 50 MHz
0	0	2	16.0 Mbps	18.0 Mbps	20.0 Mbps	25.0 Mbps
1	0	4	8.00 Mbps	9.00 Mbps	10.0 Mbps	12.5 Mbps
2	0	6	5.33 Mbps	6.00 Mbps	6.67 Mbps	8.33 Mbps
3	0	8	4.00 Mbps	4.50 Mbps	5.00 Mbps	6.25 Mbps
4	0	10	3.20 Mbps	3.60 Mbps	4.00 Mbps	5.00 Mbps
5	0	12	2.67 Mbps	3.00 Mbps	3.33 Mbps	4.16 Mbps
5	1	24	1.33 Mbps	1.50 Mbps	1.67 Mbps	2.08 Mbps
5	2	48	667 kbps	750 kbps	833 kbps	1.04 Mbps
5	3	96	333 kbps	375 kbps	417 kbps	521 kbps
255	3	4096	7.81 kbps	8.80 kbps	9.78 kbps	12.2 kbps

32.2.9 RSPI Data Control Register (SPDCR)

Address(es): RSPI0.SPDCR 0008 838Bh, RSPI1.SPDCR 0008 83ABh



Bit	Symbol	Bit Name	Description	R/W
b1, b0	SPFC[1:0]	Number of Frames Specification	b1 b0 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	RSPI Receive/Transmit Data Selection	0: SPDR values are read from the receive buffer 1: SPDR values are read from the transmit buffer (but only if the transmit buffer is empty)	R/W
b5	SPLW	RSPI Longword Access/ Word Access Specification	0: SPDR is accessed in words 1: SPDR is accessed in longwords	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Up to four frames can be transmitted or received in one round of transmission or reception activation. The amount of data in each transfer is controlled by the combination of the SPCMDm.SPB[3:0] bits, the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits.
When changing the SPDCR.SPFC[1:0] bits while the SPCR.SPE bit is 1, the bits should be changed while the SPSR.IDLNF flag is 0.

SPFC[1:0] Bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR (per transfer activation). Up to four frames can be transmitted or received in one round of transmission or reception, and the amount of data is determined by the combination of the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits. Furthermore, the setting of the SPFC[1:0] bits adjusts the number of frames for generation of RSPI reception interrupts, and start of transmission or generation of RSPI transmission interrupts. Table 32.4 show the frame configurations that can be stored in SPDR and examples of combinations of settings for transmission and reception. Do not execute the subsequent operations if combinations of settings other than those shown in the examples are made.

Table 32.4 Settable Combinations of SPSLN[2:0] Bits and SPFC[1:0] Bits

Setting	SPSLN[2:0]	SPFC[1:0]	Number of Frames in a Single Sequence	Number of Frames at which Receive Buffer Full Interrupt Occurs or Transmit Buffer Holding Data is Recognized
1-1	000	00	1	1
1-2	000	01	2	2
1-3	000	10	3	3
1-4	000	11	4	4
2-1	001	01	2	2
2-2	001	11	4	4
3	010	10	3	3
4	011	11	4	4
5	100	00	5	1
6	101	00	6	1
7	110	00	7	1
8	111	00	8	1

SPRDTD Bit (RSPI Receive/Transmit Data Selection)

The SPRDTD bit selects whether the SPDR reads values from the receive buffer or from the transmit buffer.

If reading is from the transmit buffer, the value written to SPDR register immediately beforehand is read.

When reading the transmit buffer, do so before writing of the number of frames set in the SPFC[1:0] bits is finished and after generation of the RSPI transmission interrupt.

For details, see section section 32.2.5, RSPI Data Register (SPDR).

SPLW Bit (RSPI Longword Access/Word Access Specification)

The SPLW bit specifies the access width for SPDR. Access to SPDR is in words when the SPLW bit is 0 and in longwords when the SPLW bit is 1.

Also, when the SPLW bit is 0, set the SPCMDm.SPB[3:0] bits (RSPI data length setting bits) to 8 to 16 bits. Do not execute an operation when 20, 24, or 32 bits is specified.

32.2.10 RSPI Clock Delay Register (SPCKD)

Address(es): RSPI0.SPCKD 0008 838Ch, RSPI1.SPCKD 0008 83ACh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK Delay Setting	b2 b1 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPCKD sets a period from the beginning of SSLni signal assertion to RSPCK oscillation (RSPCK delay) when the SPCMDm.SCKDEN bit is 1. Do not execute the subsequent operations if the contents of SPCKD are changed while both the SPCR.MSTR and SPCR.SPE bits are 1.

SCKDL[2:0] Bits (RSPCK Delay Setting)

The SCKDL[2:0] bits set an RSPCK delay value when the SPCMDm.SCKDEN bit is 1.
When using the RSPI in slave mode, set the SCKDL[2:0] bits to 000b.

32.2.11 RSPI Slave Select Negation Delay Register (SSLND)

Address(es): RSPI0.SSLND 0008 838Dh, RSPI1.SSLND 0008 83ADh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SLNDL[2:0]	SSL Negation Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SSLND sets a period (SSL negation delay) from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the RSPI in master mode. Do not execute the subsequent operations if the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1.

SLNDL[2:0] Bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits set an SSL negation delay value when the RSPI is in master mode.
When using the RSPI in slave mode, set the SLNDL[2:0] bits to 000b.

32.2.12 RSPI Next-Access Delay Register (SPND)

Address(es): RSPI0.SPND 0008 838Eh, RSPI1.SPND 0008 83AEh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPNDL[2:0]	RSPI Next-Access Delay Setting	b2 b0 0 0 0: 1 RSPCK + 2 PCLK 0 0 1: 2 RSPCK + 2 PCLK 0 1 0: 3 RSPCK + 2 PCLK 0 1 1: 4 RSPCK + 2 PCLK 1 0 0: 5 RSPCK + 2 PCLK 1 0 1: 6 RSPCK + 2 PCLK 1 1 0: 7 RSPCK + 2 PCLK 1 1 1: 8 RSPCK + 2 PCLK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPND sets a non-active period (next-access delay) of the SSLni signal after termination of a serial transfer when the SPCMDm.SPNDEN bit is 1. Do not execute the subsequent operations if the contents of SPND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1.

SPNDL[2:0] Bits (RSPI Next-Access Delay Setting)

The SPNDL[2:0] bits set a next-access delay when the SPCMDm.SPNDEN bit is 1.

When using the RSPI in slave mode, set the SPNDL[2:0] bits to 000b.

32.2.13 RSPI Control Register 2 (SPCR2)

Address(es): RSPI0.SPCR2 0008 838Fh, RSPI1.SPCR2 0008 83AFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPPE	Parity Enable	0: Does not add the parity bit to transmit data and does not check the parity bit of receive data 1: Adds the parity bit to transmit data and checks the parity bit of receive data (when SPCR.TXMD = 0) Adds the parity bit to transmit data but does not check the parity bit of receive data (when SPCR.TXMD = 1)	R/W
b1	SPOE	Parity Mode	0: Selects even parity for use in transmission and reception 1: Selects odd parity for use in transmission and reception	R/W
b2	SPIIE	RSPI Idle Interrupt Enable	0: Disables the generation of idle interrupt requests 1: Enables the generation of idle interrupt requests	R/W
b3	PTE	Parity Self-Testing	0: Disables the self-diagnosis function of the parity circuit 1: Enables the self-diagnosis function of the parity circuit	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not execute the subsequent operations if the SPPE bit or SPOE bit in SPCR2 is changed while the SPCR.SPE bit is 1.

SPPE Bit (Parity Enable)

The SPPE bit enables or disables the parity function.

The parity bit is added to transmit data and parity checking is performed for receive data when the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1.

The parity bit is added to transmit data but parity checking is not performed for receive data when the SPCR.TXMD bit is 1 and the SPCR2.SPPE bit is 1.

SPOE Bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit/receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit/receive character plus the parity bit is odd.

The SPOE bit is valid only when the SPPE bit is 1.

SPIIE Bit (RSPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of RSPI idle interrupt requests when the RSPI being in the idle state is detected and the SPSR.IDLNF flag is cleared to 0.

PTE Bit (Parity Self-Testing)

The PTE bit enables the self-diagnosis function of the parity circuit in order to check whether the parity function is

operating correctly.

32.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7)

Address(es): RSPI0.SPCMD0 0008 8390h, RSPI0.SPCMD1 0008 8392h, RSPI0.SPCMD2 0008 8394h, RSPI0.SPCMD3 0008 8396h, RSPI0.SPCMD4 0008 8398h, RSPI0.SPCMD5 0008 839Ah, RSPI0.SPCMD6 0008 839Ch, RSPI0.SPCMD7 0008 839Eh, RSPI1.SPCMD0 0008 83B0h, RSPI1.SPCMD1 0008 83B2h, RSPI1.SPCMD2 0008 83B4h, RSPI1.SPCMD3 0008 83B6h, RSPI1.SPCMD4 0008 83B8h, RSPI1.SPCMD5 0008 83BAh, RSPI1.SPCMD6 0008 83BCh, RSPI1.SPCMD7 0008 83BEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	CPHA	RSPCK Phase Setting	0: Data sampling on odd edge, data variation on even edge 1: Data variation on odd edge, data sampling on even edge	R/W
b1	CPOL	RSPCK Polarity Setting	0: RSPCK is low when idle 1: RSPCK is high when idle	R/W
b3, b2	BRDV[1:0]	Bit Rate Division Setting	b3 b2 0 0: These bits select the base bit rate 0 1: These bits select the base bit rate divided by 2 1 0: These bits select the base bit rate divided by 4 1 1: These bits select the base bit rate divided by 8	R/W
b6 to b4	SSLA[2:0]	SSL Signal Assertion Setting	b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 1 x x: — (Setting prohibited) x: Don't care	R/W
b7	SSLKP	SSL Signal Level Keeping	0: Negates all SSL signals upon completion of transfer 1: Keeps the SSL signal level from the end of transfer until the beginning of the next access	R/W
b11 to b8	SPB[3:0]	RSPI Data Length Setting	b11 b8 0100 to 0111: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0010, 0011: 32 bits	R/W
b12	LSBF	RSPI LSB First	0: MSB first 1: LSB first	R/W
b13	SPNDEN	RSPI Next-Access Delay Enable	0: A next-access delay of 1 RSPCK + 2 PCLK 1: A next-access delay is equal to the setting of the RSPI next-access delay register (SPND)	R/W
b14	SLNDEN	SSL Negation Delay Setting Enable	0: An SSL negation delay of 1 RSPCK 1: An SSL negation delay is equal to the setting of the RSPI slave select negation delay register (SSLND)	R/W
b15	SCKDEN	RSPCK Delay Setting Enable	0: An RSPCK delay of 1 RSPCK 1: An RSPCK delay is equal to the setting of the RSPI clock delay register (SPCKD)	R/W

SPCMDm register is used to set a transfer format for the RSPI in master mode. Each channel has eight RSPI command registers (SPCMD0 to SPCMD7). Some of the bits in SPCMD0 register is used to set a transfer mode for the RSPI in slave mode. The RSPI in master mode sequentially references SPCMDm register according to the settings in the SPSCR.SPSLN[2:0] bits, and executes the serial transfer that is set in the referenced SPCMDm register.
SPCMDm register should be set while the transmit buffer is empty (data for the next transfer is not set) and before setting of the data that is to be transmitted when that SPCMDm register is referenced.
SPCMDm that is referenced by the RSPI in master mode can be checked by means of the SPSSR.SPCP[2:0] bits. Do not execute the subsequent operations if the contents of SPCMDm are changed while the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1.

CPHA Bit (RSPCK Phase Setting)

The CPHA bit sets an RSPCK phase of the RSPI in master mode or slave mode. Data communications between RSPI modules require the same RSPCK phase setting between the modules.

CPOL Bit (RSPCK Polarity Setting)

The CPOL bit sets an RSPCK polarity of the RSPI in master mode or slave mode. Data communications between RSPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] Bits (Bit Rate Division Setting)

The BRDV[1:0] bits are used to determine the bit rate. A bit rate is determined by combinations of the settings in the BRDV[1:0] bits and SPBR (see section 32.2.8, RSPI Bit Rate Register (SPBR)). The settings in SPBR determine the base bit rate. The settings in the BRDV[1:0] bits are used to select a bit rate which is obtained by dividing the base bit rate by 1, 2, 4, or 8. In SPCMDm register, different BRDV[1:0] bit settings can be specified. This permits the execution of serial transfers at a different bit rate for each command.

SSLA[2:0] Bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the RSPI performs serial transfers in master mode.
Setting the SSLA[2:0] bits controls the assertion for the SSLni signal. When an SSLni signal is asserted, its polarity is determined by the set value in the corresponding SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state (as the SSLn0 pin acts as input).
When using the RSPI in slave mode, set the SSLA[2:0] bits to 000b.

SSLKP Bit (SSL Signal Level Keeping)

When the RSPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLni signal level for the current command is to be kept or negated between the SSL negation timing associated with the current command and the SSL assertion timing associated with the next command.
When using the RSPI in slave mode, the SSLKP bit should be set to 0.

SPB[3:0] Bits (RSPI Data Length Setting)

The SPB[3:0] bits set a transfer data length for the RSPI in master mode or slave mode.

LSBF Bit (RSPI LSB First)

The LSBF bit sets the data format of the RSPI in master mode or slave mode to MSB first or LSB first.

SPNDEN Bit (RSPI Next-Access Delay Enable)

The SPNDEN bit sets the period from the time the RSPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the RSPI enables the SSLni signal assertion for the next access (next-access delay). If the SPNDEN bit is 0, the RSPI sets the next-access delay to 1 RSPCK + 2 PCLK. If the SPNDEN bit is 1, the RSPI inserts a next-access delay in compliance with the SPND setting.

When using the RSPI in slave mode, the SPNDEN bit should be set to 0.

SLNDEN Bit (SSL Negation Delay Setting Enable)

The SLNDEN bit sets the period from the time the RSPI in master mode stops RSPCK oscillation until the RSPI sets the SSLni signal inactive (SSL negation delay). If the SLNDEN bit is 0, the RSPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the RSPI negates the SSL signal at an SSL negation delay in compliance with the SSLND setting.

When using the RSPI in slave mode, the SLNDEN bit should be set to 0.

SCKDEN Bit (RSPCK Delay Setting Enable)

The SCKDEN bit sets the period from the point when the RSPI in master mode activates the SSLni signal until the RSPCK starts oscillation (RSPI clock delay). If the SCKDEN bit is 0, the RSPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the RSPI starts the oscillation of RSPCK at an RSPCK delay in compliance with the SPCKD setting.

When using the RSPI in slave mode, the SCKDEN bit should be set to 0.

32.3 Operation

In this section, the serial transfer period means a period from the beginning of driving valid data to the fetching of the final valid data.

32.3.1 Overview of RSPI Operations

The RSPI is capable of synchronous serial transfers in slave mode (SPI operation), single-master mode (SPI operation), multi-master mode (SPI operation), slave mode (clock synchronous operation), and master mode (clock synchronous operation). A particular mode of the RSPI can be selected by using the MSTR, MODFEN, and SPMS bits in SPCR. Table 32.5 lists the relationship between RSPI modes and SPCR settings, and a description of each mode.

Table 32.5 Relationship between RSPI Modes and SPCR Settings and Description of Each Mode

Mode	Slave (SPI Operation)	Single-Master (SPI Operation)	Multi-Master (SPI Operation)	Slave (Clock Synchronous Operation)	Master (Clock Synchronous Operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn signal	Input	Output	Output/Hi-Z	Input	Output
MOSIn signal	Input	Output	Output/Hi-Z	Input	Output
MISOn signal	Output/Hi-Z	Input	Input	Output	Input
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity modification function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLK/8	Up to PCLK/2	Up to PCLK/2	Up to PCLK/8	Up to PCLK/2
Clock source	RSPCK input	On-chip baud rate generator	On-chip baud rate generator	RSPCK input	On-chip baud rate generator
Clock polarity	Two	Two	Two	Two	Two
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB	MSB/LSB	MSB/LSB	MSB/LSB	MSB/LSB
Transfer data length	8 to 32 bits	8 to 32 bits	8 to 32 bits	8 to 32 bits	8 to 32 bits
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0,1)	Possible (CPHA = 0,1)	—	—
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer activation method	SSL input active or RSPCK oscillation	Transmit buffer is written to at generation of a transmit buffer empty interrupt request	Transmit buffer is written to at generation of a transmit buffer empty interrupt request	RSPCK oscillation	Transmit buffer is written to at generation of a transmit buffer empty interrupt request
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmit buffer empty detection	Supported	Supported	Supported	Supported	Supported
Receive buffer full detection	Supported*2	Supported*2	Supported*2	Supported*2	Supported*2
Overrun error detection	Supported*2	Supported*2	Supported*2	Supported*2	Supported*2
Parity error detection	Supported*2,*3	Supported*2,*3	Supported*2,*3	Supported*2,*3	Supported*2,*3
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, receiver buffer full detection, overrun error detection, and parity error detection are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.

32.3.2 Controlling RSPI Pins

The RSPI can switch pin states is response to the settings of the MSTR, MODFEN, and SPMS bits in SPCR and the SPOM bit in SPPCR. Setting the SPOM bit in SPPCR to 0 selects CMOS output; setting it to 1 selects open-drain output. Table 32.6 lists the relationship between pin states and bit settings. In 64- and 48-pin products, only the CMOS output mode is supported, so do not set the SPOM bit in SPPCR to 1.

Table 32.6 Relationship between Pin States and Bit Settings

Mode	Pin	Pin State*2	
		SPPCR.SPOM = 0	SPPCR.SPOM = 1*6
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (Clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (Clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. RSPI settings are not reflected in the multiplexed pins for which the RSPI function is not selected.
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z.
Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is cleared (= 0), the pin state is Hi-Z.
Note 5. These pins are available for use as I/O port pins.
Note 6. Open-drain output is only selectable in 144-, 120-, 112-, and 100-pin products. In 64- and 48-pin products, do not set the SPOM bit in SPPCR to 1.

The RSPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) according to MOIFE and MOIFV bit settings in SPPCR, as listed in Table 32.7.

Table 32.7 MOSI Signal Value Determination during SSL Negation Period

MOIFE Bit	MOIFV Bit	MOSIn Signal Value during SSL Negation Period
0	0, 1	Final data from previous transfer
1	0	Always low
1	1	Always high

32.3.3 RSPI System Configuration Examples

32.3.3.1 Single Master/Single Slave (with This MCU Acting as Master)

Figure 32.5 shows a single-master/single-slave RSPI system configuration example when this MCU is used as a master. In the single-master/single-slave configuration, the SSLn0 to SSLn3 output of this MCU (master) are not used. The SSL input of the RSPI slave is fixed to the low level, and the RSPI slave is always maintained in a select state.*1
This MCU (master) always drives the RSPCKn and MOSIn. The RSPI slave always drives the MISO.

Note 1. In the transfer format corresponding to the case where the SPCMDm.CPHA bit is 0, there are slave devices for which the SSL signal cannot be fixed to the active level. In situations where the SSL signal cannot be fixed, the SSLni output of this MCU should be connected to the SSL input of the slave device.

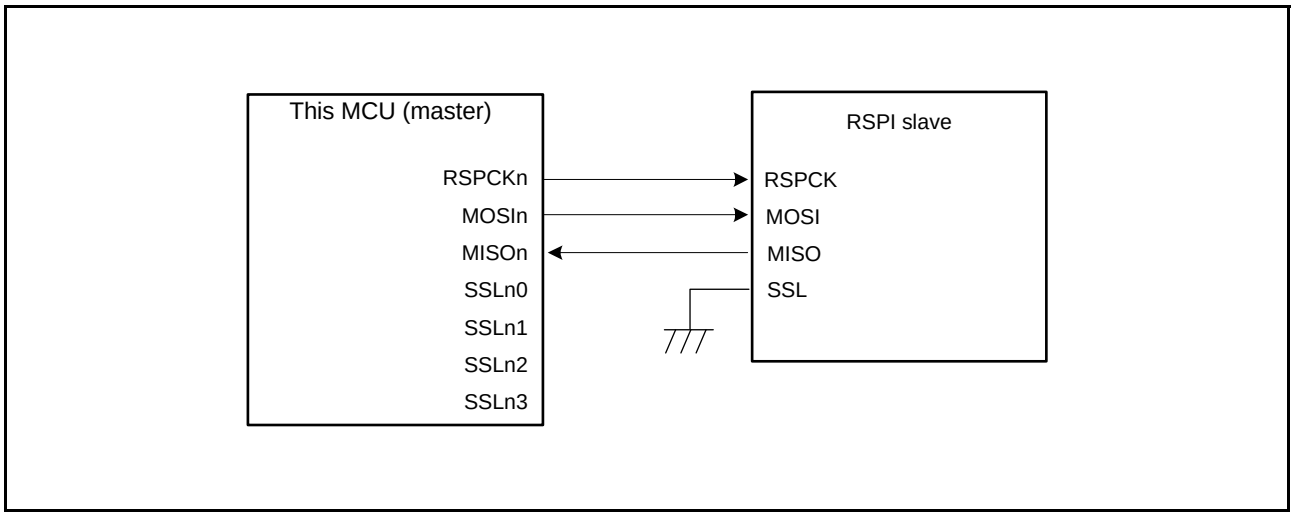


Figure 32.5 Single-Master/Single-Slave Configuration Example (This MCU = Master)

32.3.3.2 Single Master/Single Slave (with This MCU Acting as Slave)

Figure 32.6 shows a single-master/single-slave RSPI system configuration example when this MCU is used as a slave. When this MCU is to operate as a slave, the SSLn0 pin is used as SSL input. The RSPI master always drives the RSPCK and MOSI. This MCU (slave) always drives the MISOn.*1

In the single-slave configuration in which the SPCMDm.CPHA bit is set to 1, the SSLn0 input of this MCU (slave) is fixed to the low level, this MCU (slave) is always maintained in a select state, and in this manner it is possible to execute serial transfer (Figure 32.7).

Note 1. When SSLn0 is at the non-active level, the pin state is Hi-Z.

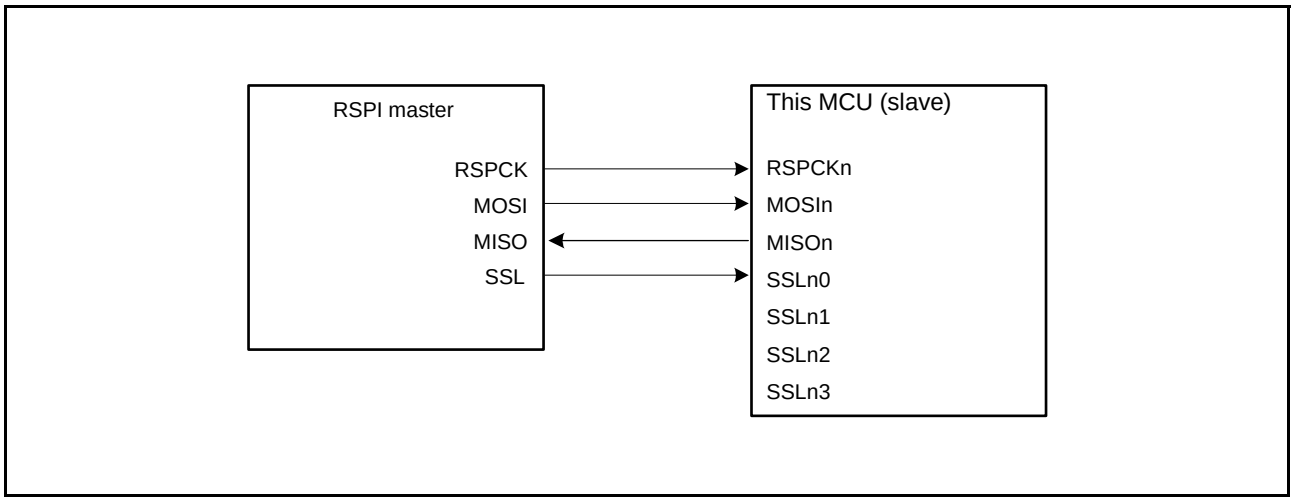


Figure 32.6 Single-Master/Single-Slave Configuration Example (This MCU = Slave, CPHA = 0)

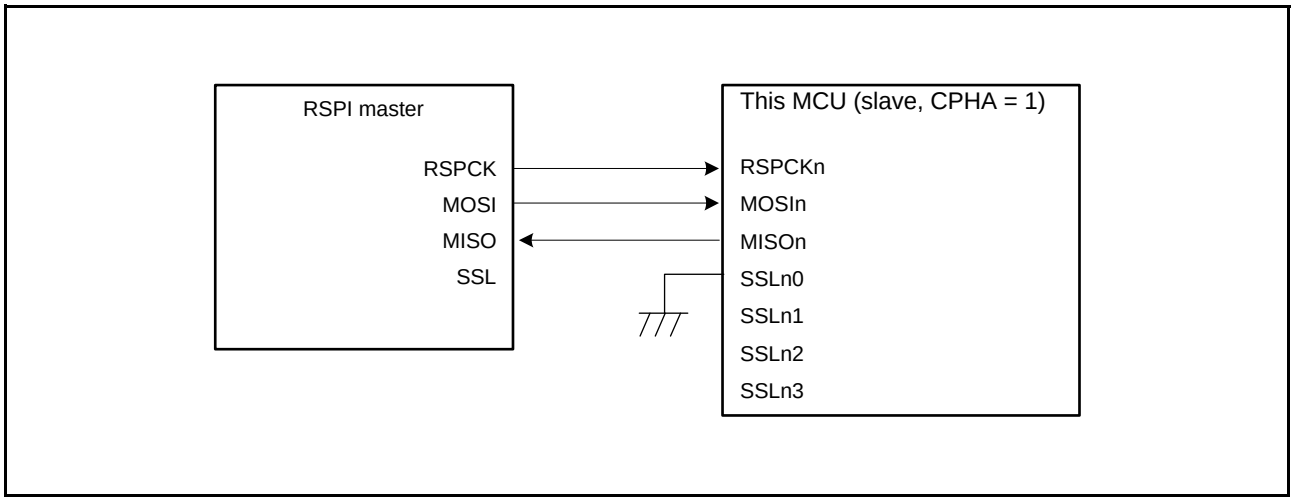


Figure 32.7 Single-Master/Single-Slave Configuration Example (This MCU = Slave, CPHA = 1)

32.3.3.3 Single Master/Multi-Slave (with This MCU Acting as Master)

Figure 32.8 shows a single-master/multi-slave RSPI system configuration example when this MCU is used as a master. In the example of Figure 32.8, the RSPI system is comprised of this MCU (master) and four slaves (RSPI slave 0 to RSPI slave 3).

The RSPCKn and MOSIn outputs of this MCU (master) are connected to the RSPCK and MOSI inputs of RSPI slave 0 to RSPI slave 3. The MISO outputs of RSPI slave 0 to RSPI slave 3 are all connected to the MISOn input of this MCU (master). SSLn0 to SSLn3 outputs of this MCU (master) are connected to the SSL inputs of RSPI slave 0 to RSPI slave 3, respectively.

This MCU (master) always drives RSPCK, MOSI, and SSLn0 to SSLn3. Of the RSPI slave 0 to RSPI slave 3, the slave that receives low-level input into the SSL input drives MISO.

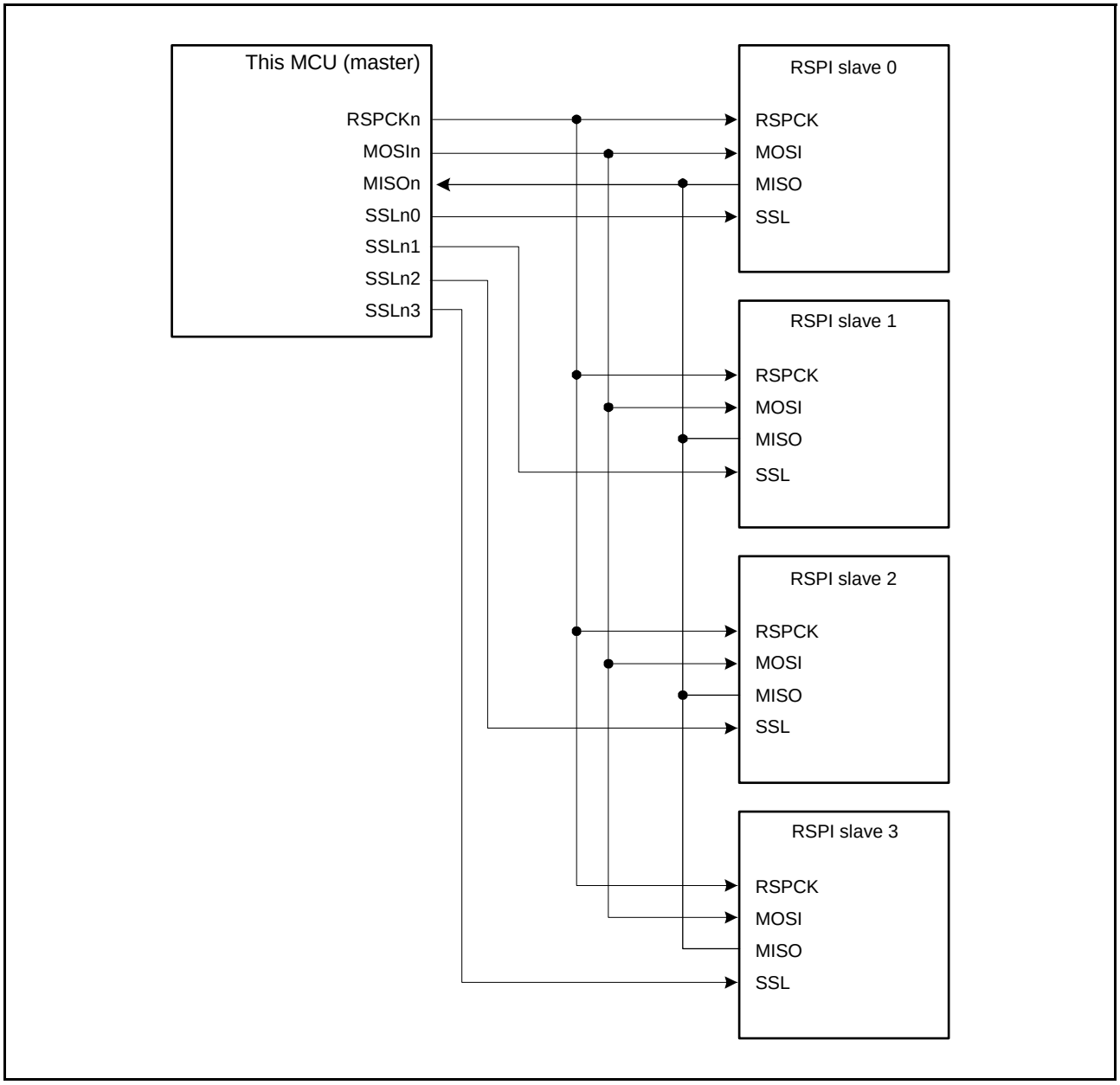


Figure 32.8 Single-Master/Multi-Slave Configuration Example (This MCU = Master)

32.3.3.4 Single Master/Multi-Slave (with This MCU Acting as Slave)

Figure 32.9 shows a single-master/multi-slave RSPI system configuration example when this MCU is used as a slave. In the example of Figure 32.9, the RSPI system is comprised of an RSPI master and two MCUs (slave X and slave Y). The RSPCK and MOSI outputs of the RSPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slave X and slave Y). The MISOn outputs of the MCUs (slave X and slave Y) are all connected to the MISO input of the RSPI master. SSLX and SSLY outputs of the RSPI master are connected to the SSLn0 inputs of the MCUs (slave X and slave Y), respectively.
The RSPI master always drives RSPCK, MOSI, SSLX, and SSLY. Of the MCUs (slave X and slave Y), the slave that receives low-level input into the SSLn0 input drives MISOn.

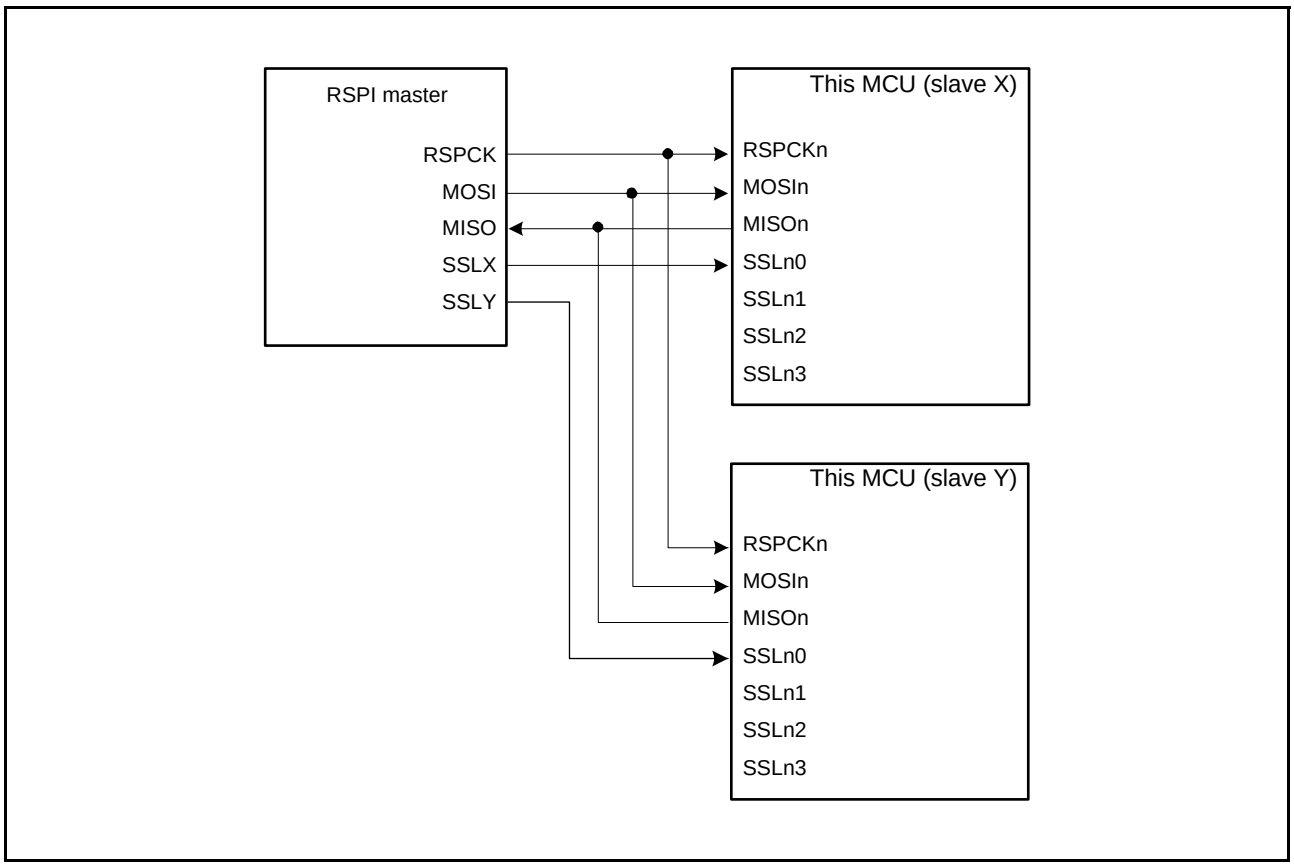


Figure 32.9 Single-Master/Multi-Slave Configuration Example (This MCU = Slave)

32.3.3.5 Multi-Master/Multi-Slave (with This MCU Acting as Master)

Figure 32.10 shows a multi-master/multi-slave RSPI system configuration example when this MCU is used as a master. In the example of Figure 32.10, the RSPI system is comprised of two MCUs (master X and master Y) and two RSPI slaves (RSPI slave 1 and RSPI slave 2).

The RSPCKn and MOSIn outputs of the MCUs (master X and master Y) are connected to the RSPCK and MOSI inputs of RSPI slaves 1 and 2. The MISO outputs of RSPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (master X and master Y). Any generic port Y output from this MCU (master X) is connected to the SSLn0 input of this MCU (master Y). Any generic port X output of this MCU (master Y) is connected to the SSLn0 input of this MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (master X and master Y) are connected to the SSL inputs of the RSPI slaves 1 and 2. In this configuration example, since the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of this MCU is not required.

This MCU drives RSPCKn, MOSIn, SSLn1, and SSLn2 when the SSLn0 input level is high. When the SSLn0 input level is low, this MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the RSPI bus right to the other master. Of the RSPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives MISO.

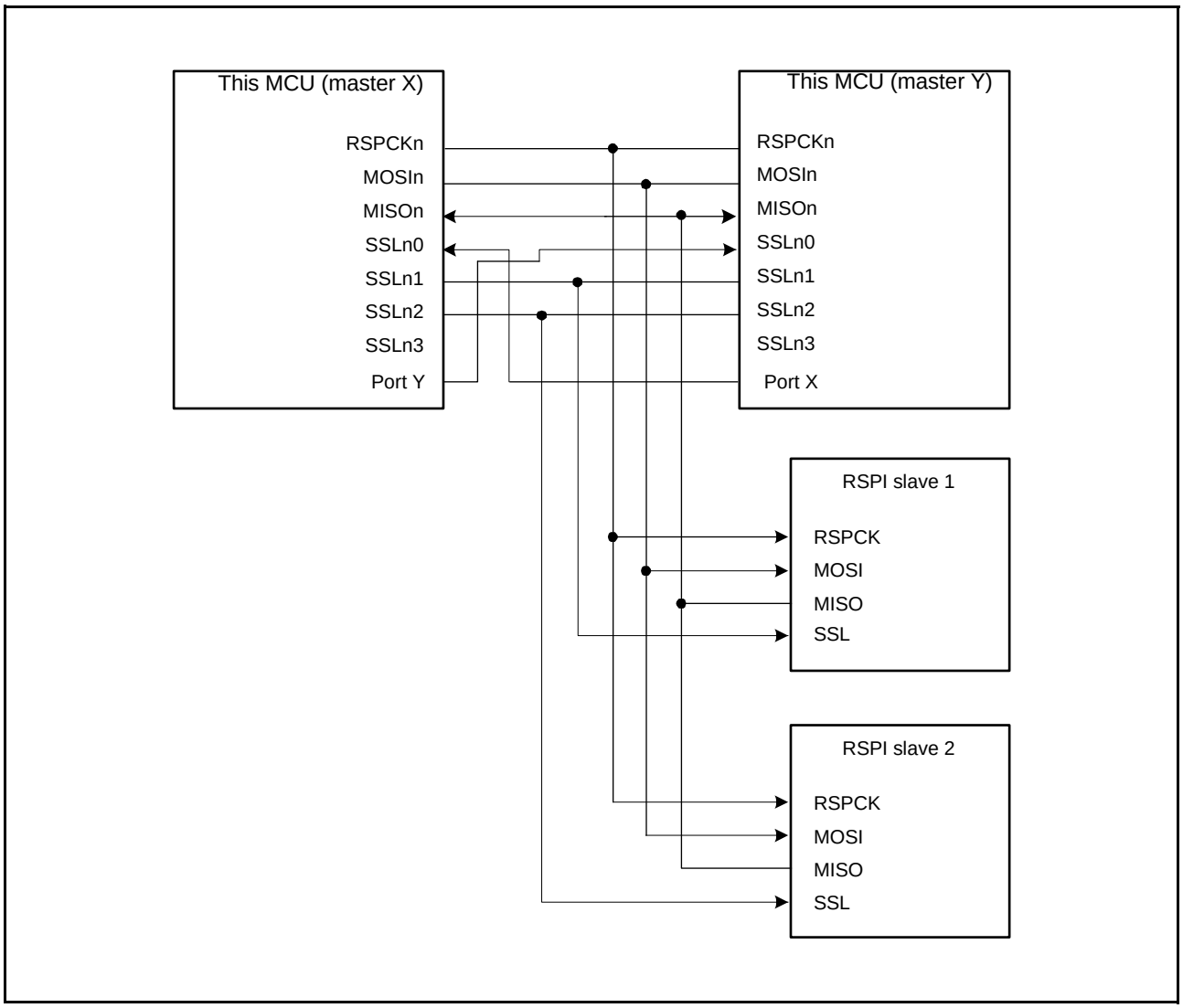


Figure 32.10 Multi-Master/Multi-Slave Configuration Example (This MCU = Master)

32.3.3.6 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) (with This MCU Acting as Master)

Figure 32.11 shows a master (clock synchronous operation)/slave (clock synchronous operation) RSPI system configuration example when this MCU is used as a master. In the master (clock synchronous operation)/slave (clock synchronous operation) configuration, SSLn0 to SSLn3 of this MCU (master) are not used.
This MCU (master) always drives the RSPCKn and MOSIn. The RSPI slave always drives the MISO.

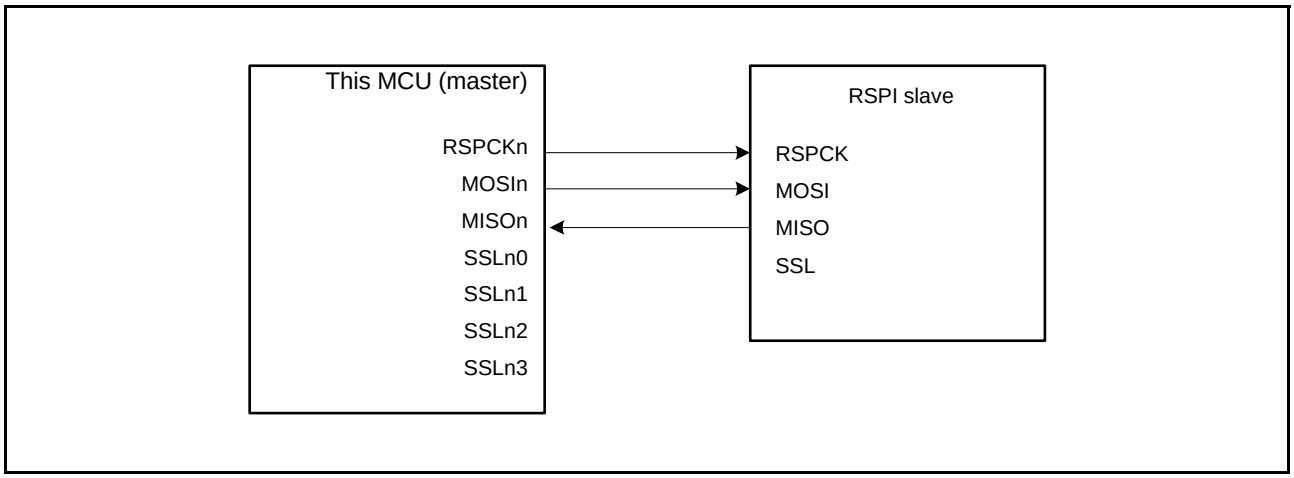


Figure 32.11 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) Configuration Example (This MCU = Master)

32.3.3.7 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) (with This MCU Acting as Slave)

Figure 32.12 shows a master (clock synchronous operation)/slave (clock synchronous operation) RSPI system configuration example when this MCU is used as a slave. When this MCU is to operate as a slave (clock synchronous operation), this MCU (slave) always drives the MISOn and the RSPI master always drives the RSPCK and MOSI. In addition, SSLn0 to SSLn3 of this MCU (slave) are not used.
Only in the single-slave configuration in which the SPCMDm.CPHA bit is set to 1, this MCU (slave) can execute serial transfer.

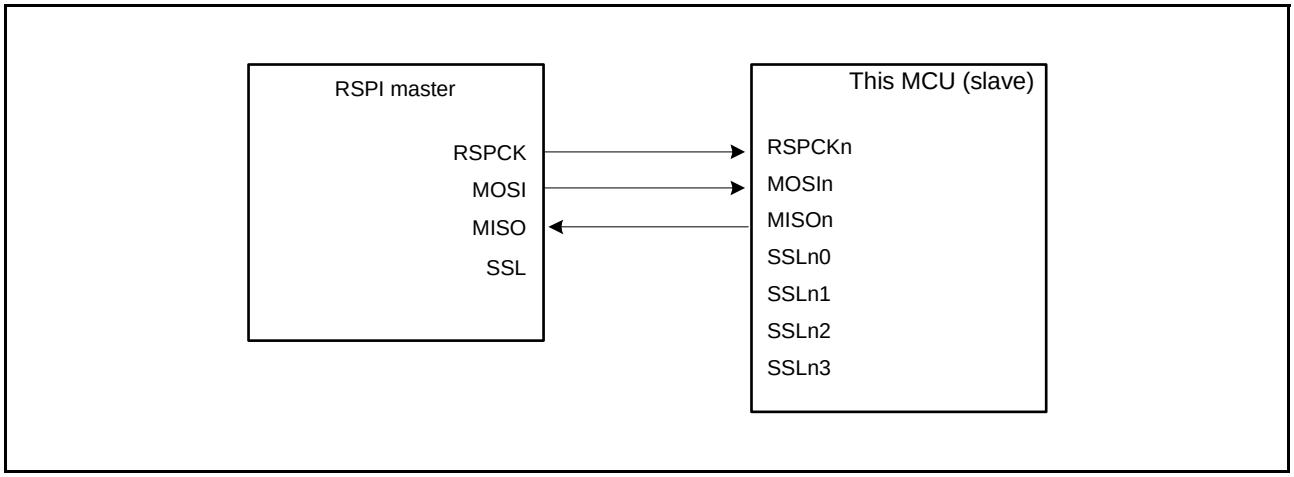


Figure 32.12 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) Configuration Example (This MCU = Slave, CPHA = 1)

32.3.4 Data Format

The RSPI's data format depends on the settings in the RSPI command register m (SPCMDm) (m = 0 to 7) and the parity enable bit of RSPI control register 2 (SPCR2.SPPE). Regardless of whether the MSB or LSB is first, the RSPI treats the range from the LSB bit of the RSPI data register (SPDR) to the selected data length as transfer data.
The format of one frame of data before or after transfer is shown below.

(a) With Parity Disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the RSPI data length setting bits in the RSPI command register m (SPCMDm.SPB[3:0]).

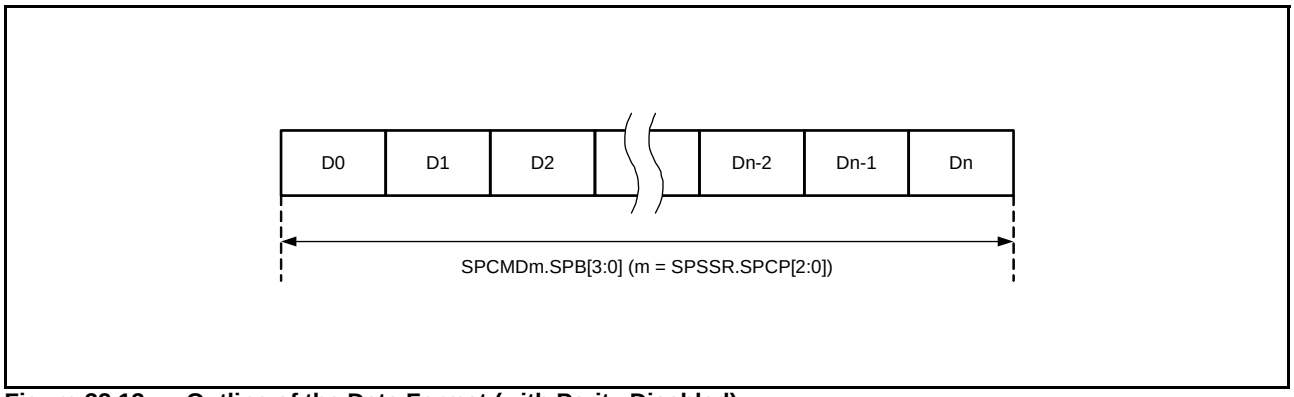


Figure 32.13 Outline of the Data Format (with Parity Disabled)

(b) With Parity Enabled

When parity is enabled, transmission or reception of data also proceeds with the length in bits selected in the SPCMDm.SPB[3:0] bits. In this case, however, the last bit is a parity bit.

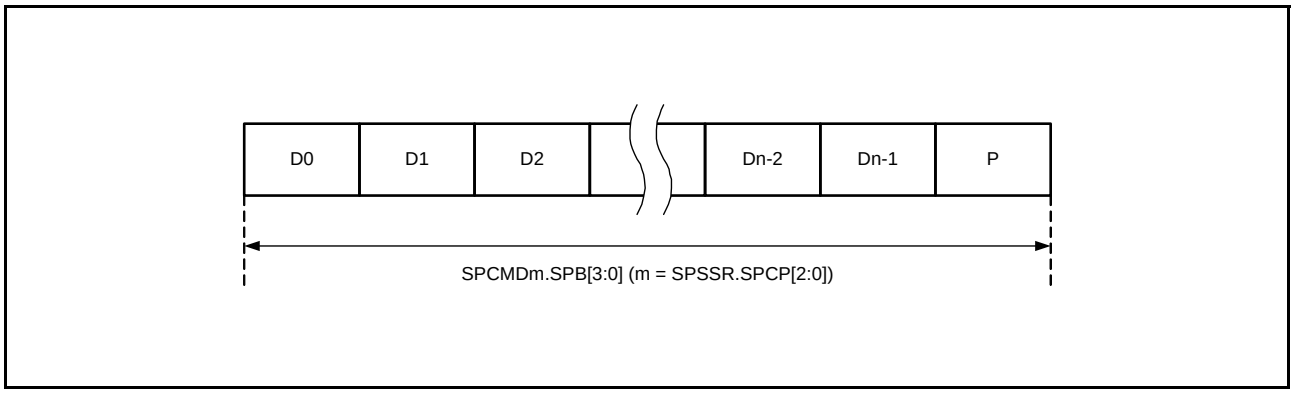


Figure 32.14 Outline of the Data Format (with Parity Enabled)

32.3.4.1 When Parity is Disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission are copied to the shift register with no prior processing. A description of the connection between the RSPI data register (SPDR) and the shift register in terms of the combination of MSB- or LSB-first and data length is given below.

(1) MSB-First Transfer (32-Bit Data)

Figure 32.15 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, an RSPI data length of 32 bits, and MSB-first selected.
In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission are shifted out from the shift register in order from T31, through T30, and so on to T00.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R31 to R00 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer.

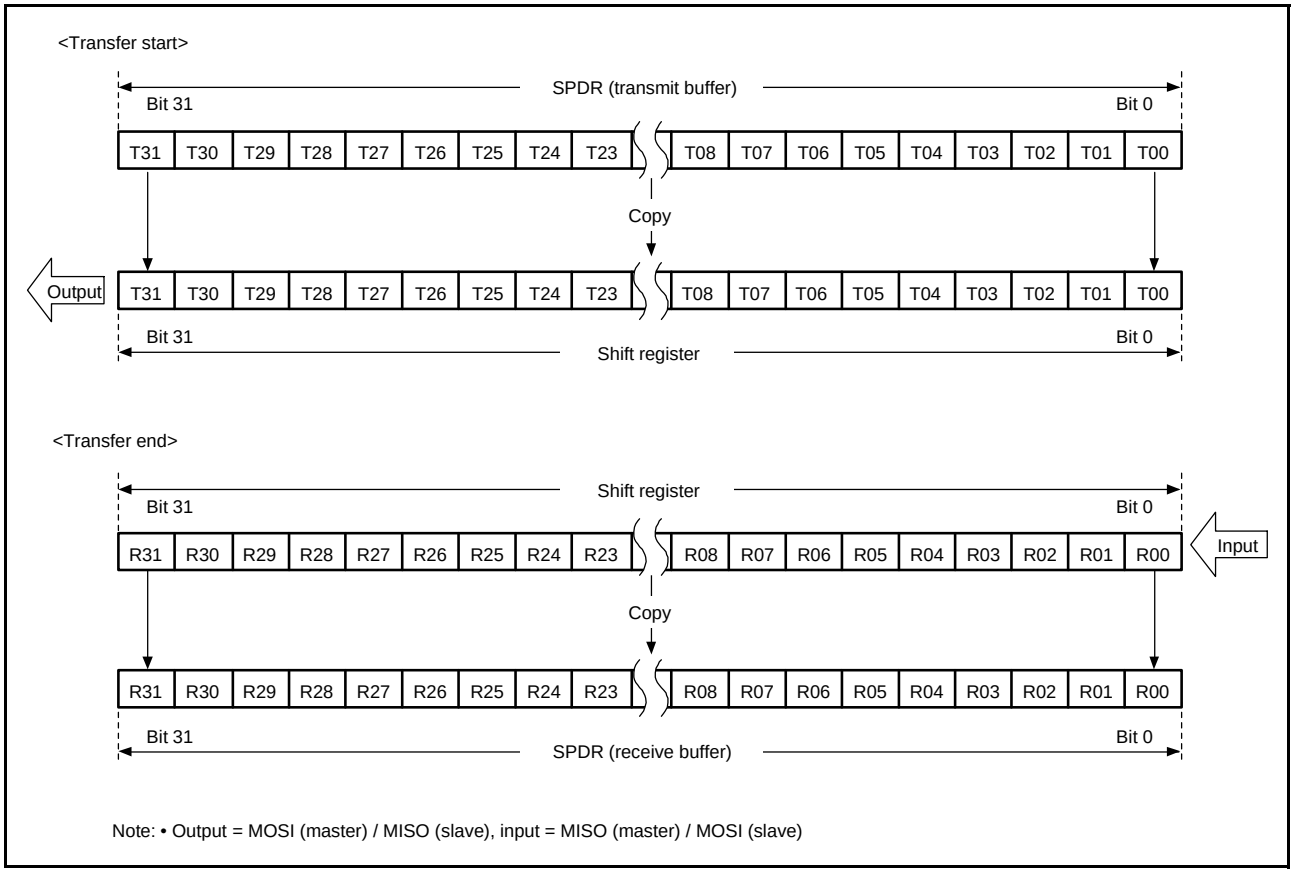


Figure 32.15 MSB-First Transfer (32-Bit Data, Parity Disabled)

(2) MSB-First Transfer (24-Bit Data)

Figure 32.16 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, 24 bits as the RSPI data length for an example that is not 32 bits, and MSB-first selected.
In transmission, the lower-order 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission are shifted out from the shift register in order from T23, through T22, and so on to T00.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R23 to R00 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. At this time, the higher-order eight bits of the transmit buffer are stored in the higher-order eight bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order eight bits of the receive buffer.

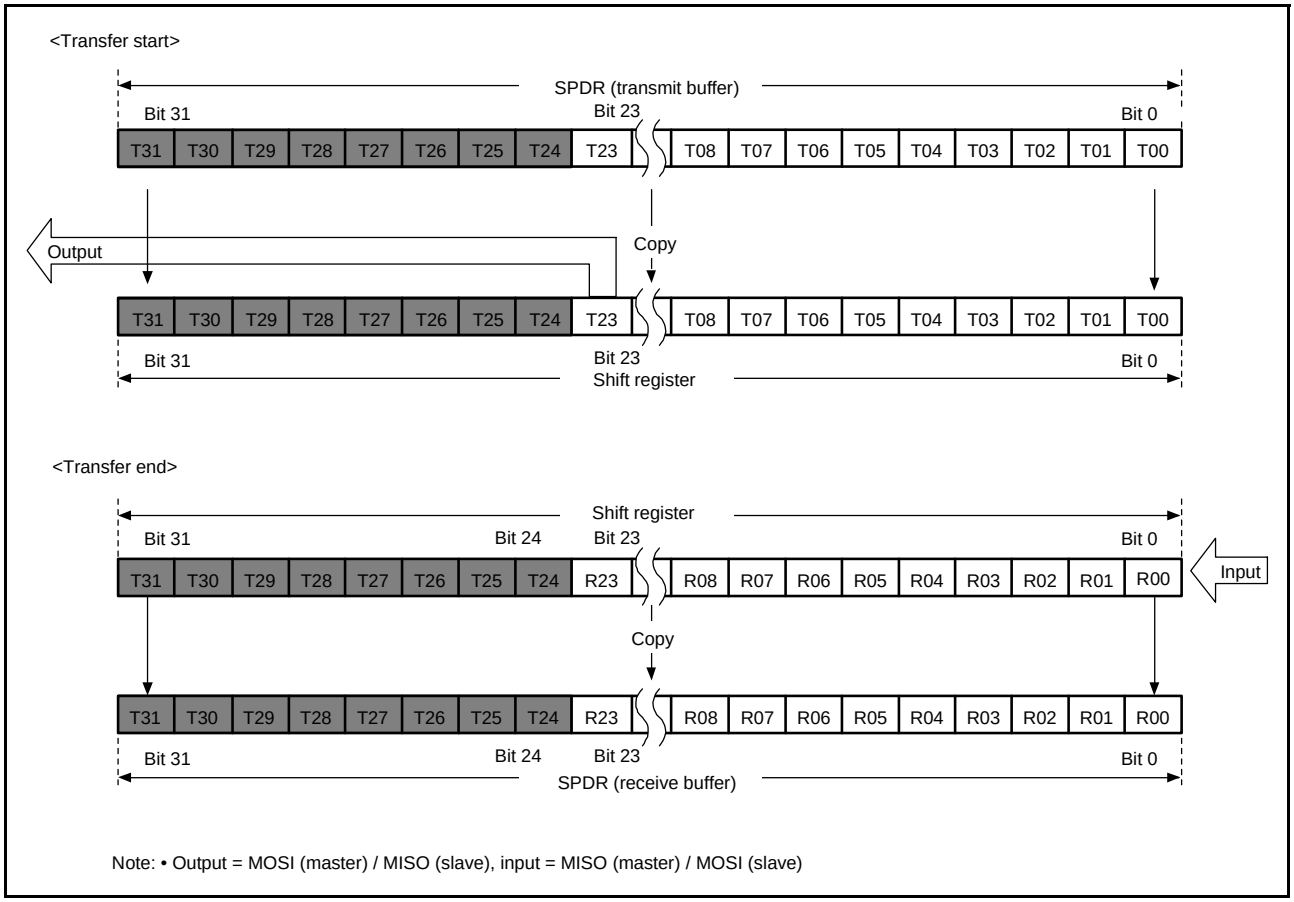


Figure 32.16 MSB-First Transfer (24-Bit Data, Parity Disabled)

(3) LSB-First Transfer (32-Bit Data)

Figure 32.17 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, an RSPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission are shifted out from the shift register in order from T00, through T01, and so on to T31.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R00 to R31 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer.

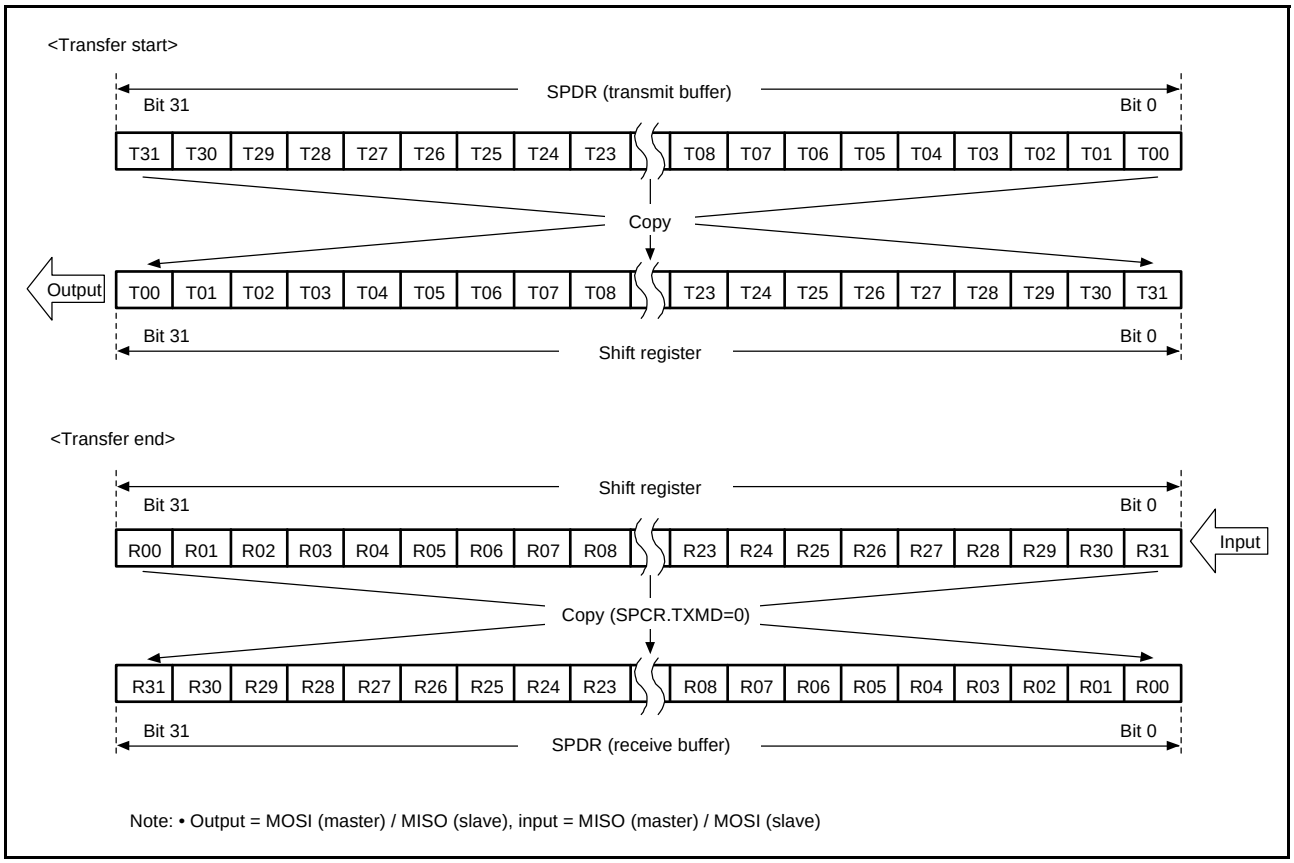


Figure 32.17 LSB-First Transfer (32-Bit Data, Parity Disabled)

(4) LSB-First Transfer (24-Bit Data)

Figure 32.18 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, 24 bits as the RSPI data length for an example that is not 32 bits, and LSB-first selected.

In transmission, the lower-order 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission are shifted out from the shift register in order from T00, through T01, and so on to T23.

In reception, received data are shifted in bit by bit through bit 8 of the shift register. When bits R00 to R23 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer.

At this time, the higher-order eight bits of the transmit buffer are stored in the higher-order eight bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order eight bits of the receive buffer.

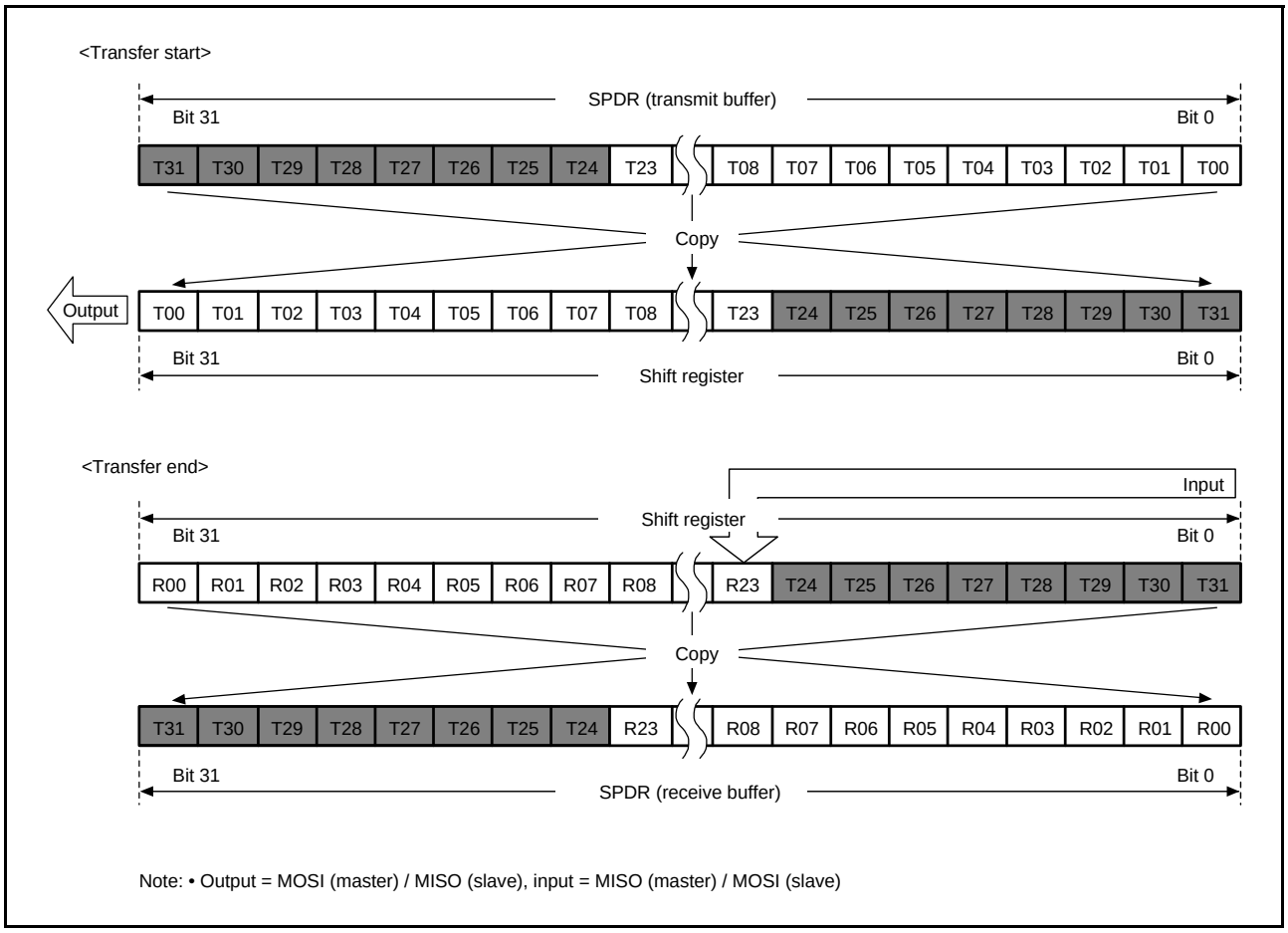


Figure 32.18 LSB-First Transfer (24-Bit Data, Parity Disabled)

32.3.4.2 When Parity is Enabled (SPCR2.SPPE = 1)

When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-First Transfer (32-Bit Data)

Figure 32.19 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, an RSPI data length of 32 bits, and MSB-first selected.
In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data are transmitted in the order T31, T30, …, T01, and P.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R31 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R31 to P are checked by judging the parity.

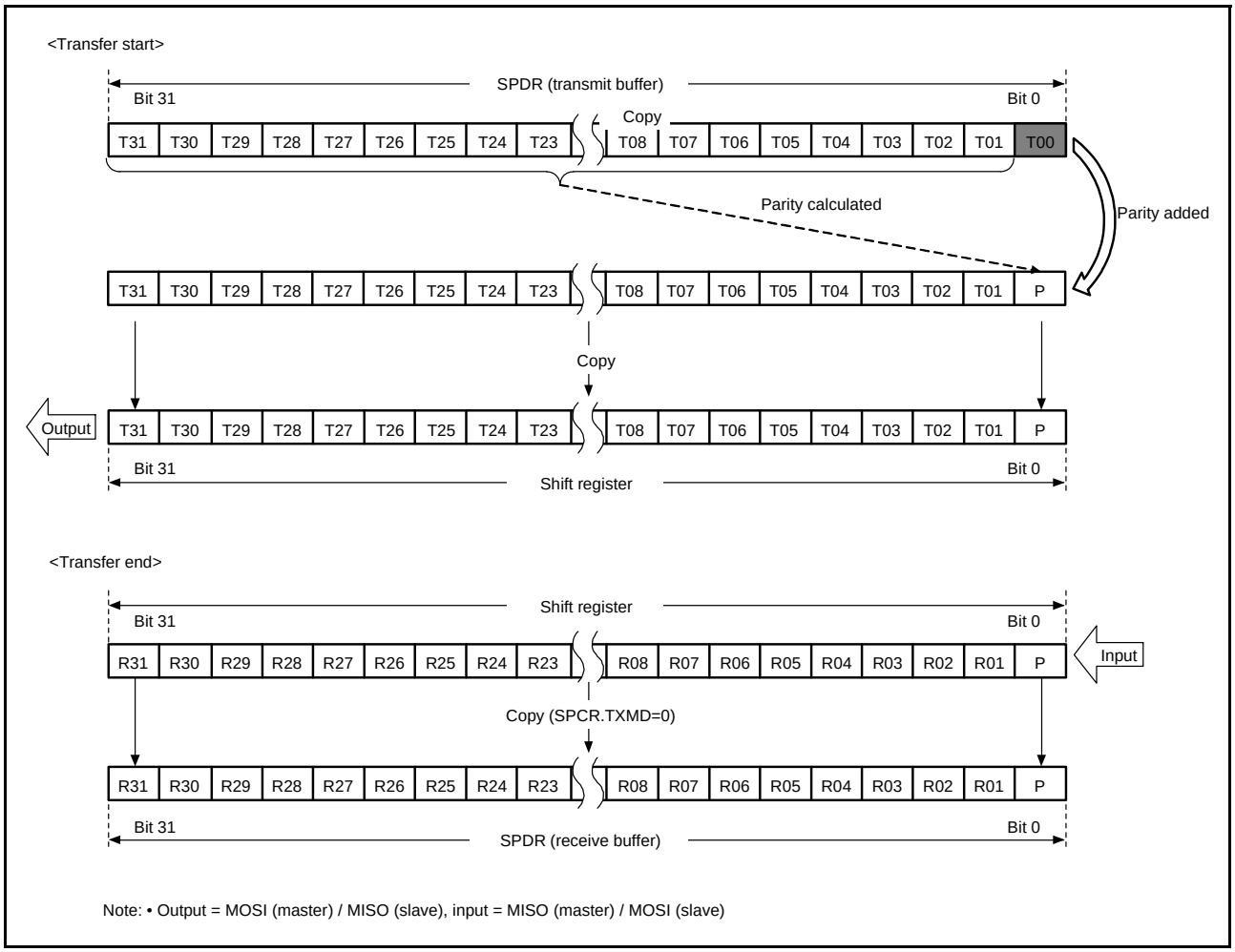


Figure 32.19 MSB-First Transfer (32-Bit Data, Parity Enabled)

(2) MSB-First Transfer (24-Bit Data)

Figure 32.20 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, 24 bits as the RSPI data length for an example that is not 32 bits, and MSB-first selected.
In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data are transmitted in the order T23, T22, …, T01, and P.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R23 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R23 to P are checked by judging the parity. At this time, the higher-order eight bits of the transmit buffer are stored in the higher-order eight bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order eight bits of the receive buffer.

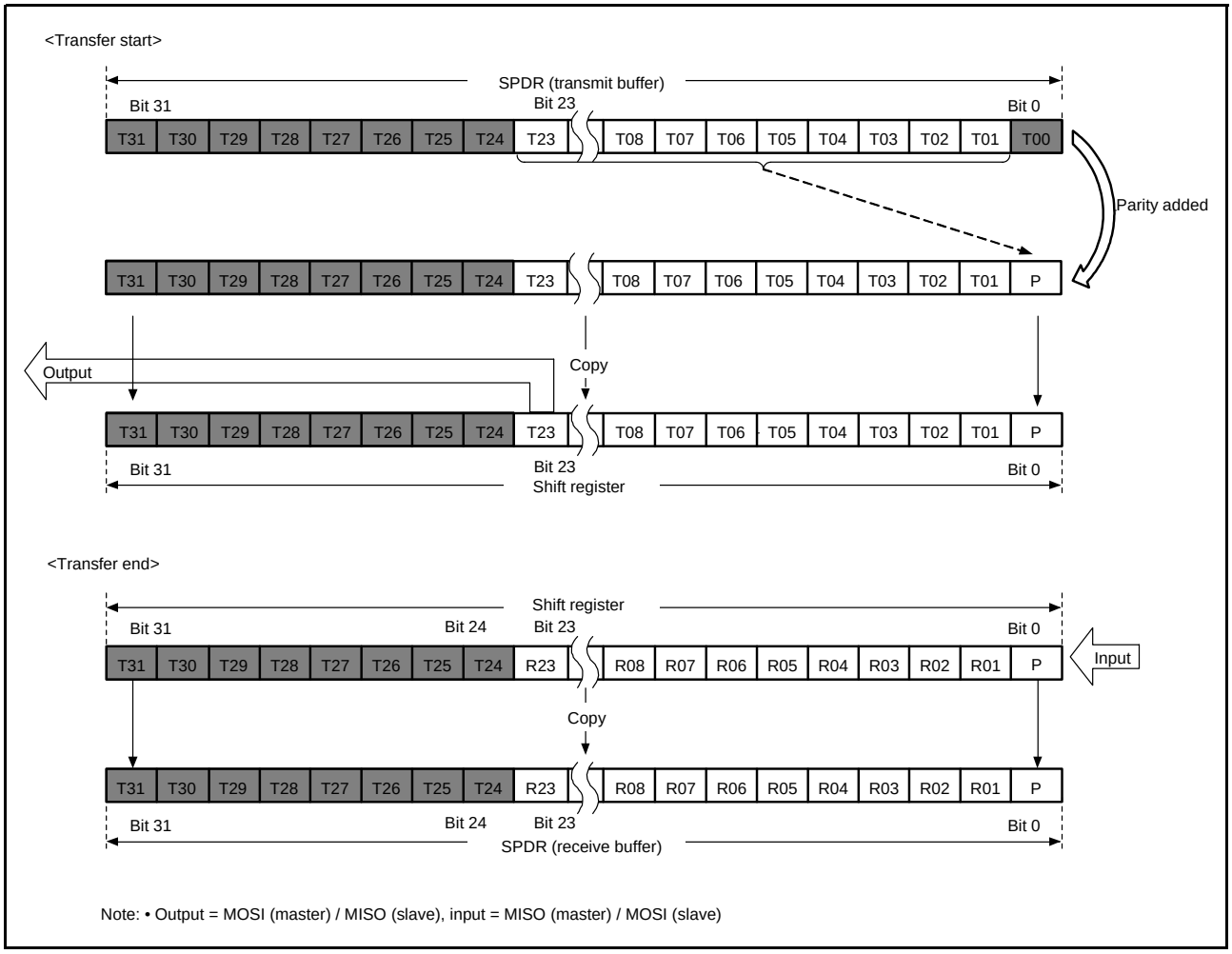


Figure 32.20 MSB-First Transfer (24-Bit Data, Parity Enabled)

(3) LSB-First Transfer (32-Bit Data)

Figure 32.21 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, an RSPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole is copied to the shift register. Data are transmitted in the order T00, T01, …, T30, and P.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R00 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P are checked by judging the parity.

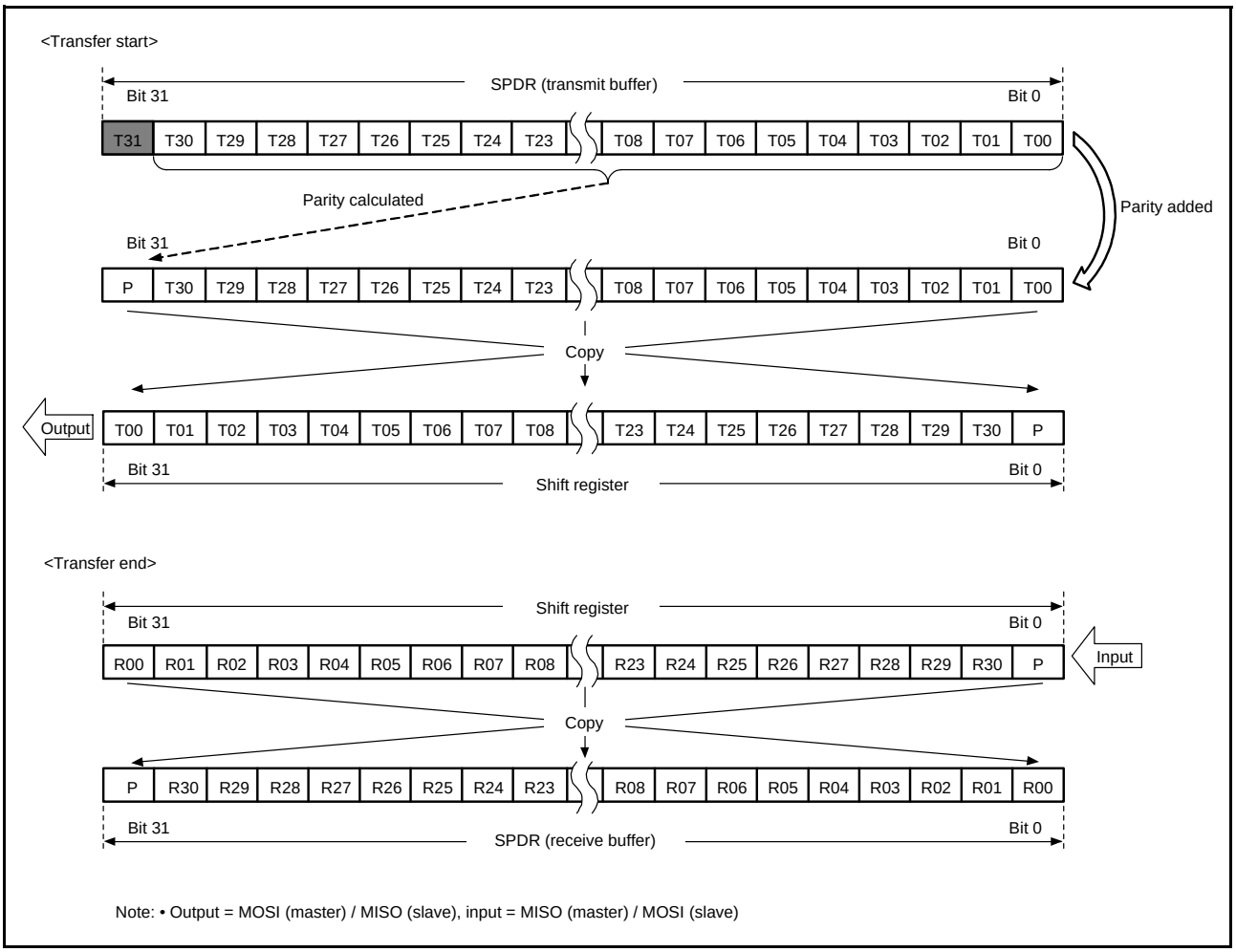


Figure 32.21 LSB-First Transfer (32-Bit Data, Parity Enabled)

(4) LSB First Transfer (24-Bit Data)

Figure 32.22 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, 24 bits as the RSPI data length for an example that is not 32 bits, and LSB-first selected.
In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole is copied to the shift register. Data are transmitted in the order T00, T01, …, T22, and P.
In reception, received data are shifted in bit by bit through bit 8 of the shift register. When bits R23 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P are checked by judging the parity. At this time, the higher-order eight bits of the transmit buffer are stored in the higher-order eight bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order eight bits of the receive buffer.

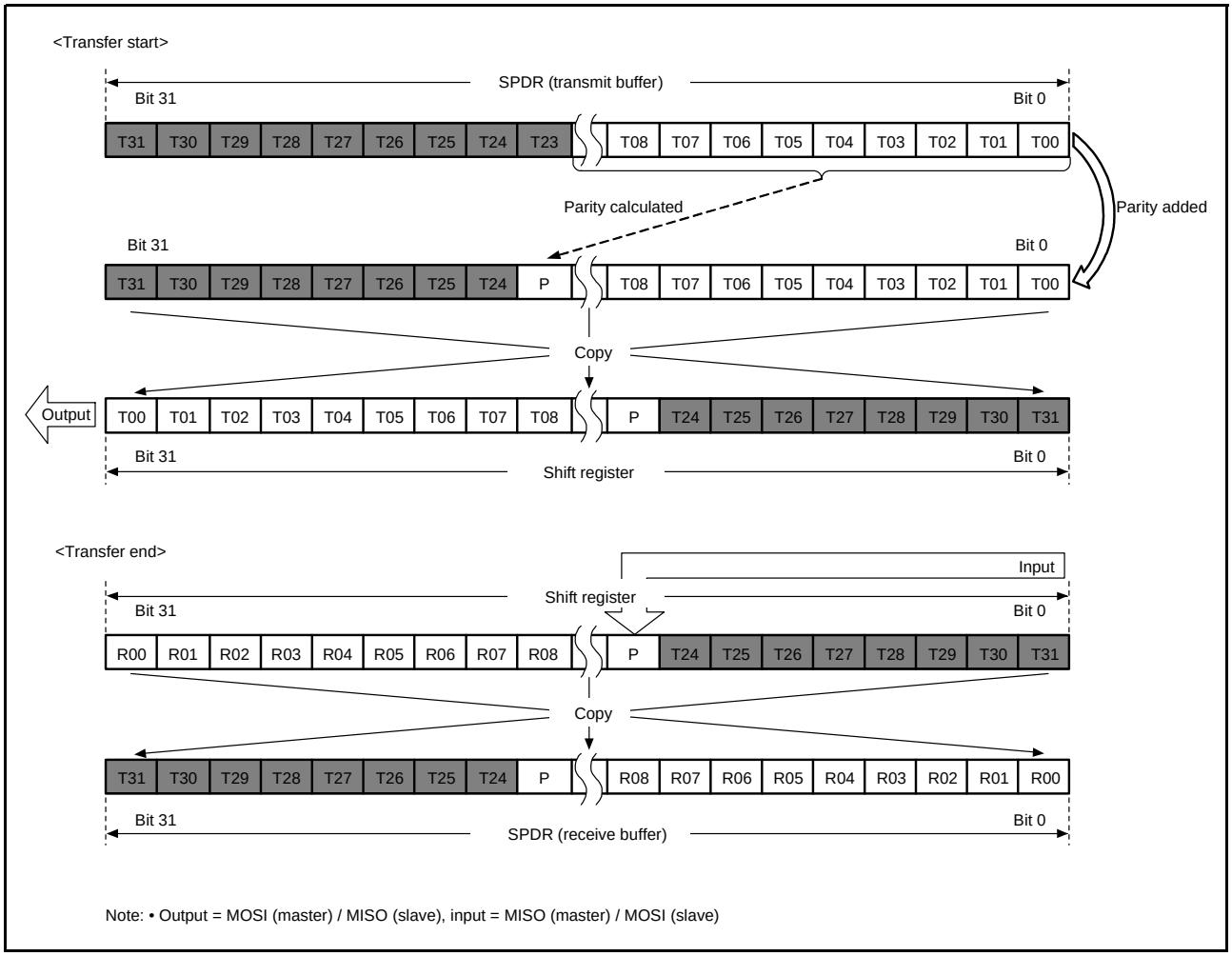


Figure 32.22 LSB-First Transfer (24-Bit Data, Parity Enabled)

32.3.5 Transfer Format

32.3.5.1 CPHA = 0

Figure 32.23 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Note that clock synchronous operation (the SPCR.SPMS bit is 1) is not guaranteed when the RSPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 32.23, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0; RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the RSPI fetches serial transfer data into the shift register. The input/output directions of the signals depend on the RSPI settings. For details, see section 32.3.2, Controlling RSPI Pins.

When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals commences at an SSLni signal assertion timing. The first RSPCKn signal change timing that occurs after the SSLni signal assertion becomes the first transfer data fetch timing. After this timing, data is sampled at every 1 RSPCK cycle. The change timing for MOSIn and MISOn signals is always 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing; it only affects the signal polarity.

t1 denotes a period from an SSLni signal assertion to RSPCKn oscillation (RSPCK delay). t2 denotes a period from the termination of RSPCKn oscillation to an SSLni signal negation (SSL negation delay). t3 denotes a period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer (next-access delay). t1, t2, and t3 are controlled by a master device running on the RSPI system. For a description of t1, t2, and t3 when the RSPI of this MCU is in master mode, see section 32.3.10.1, Master Mode Operation.

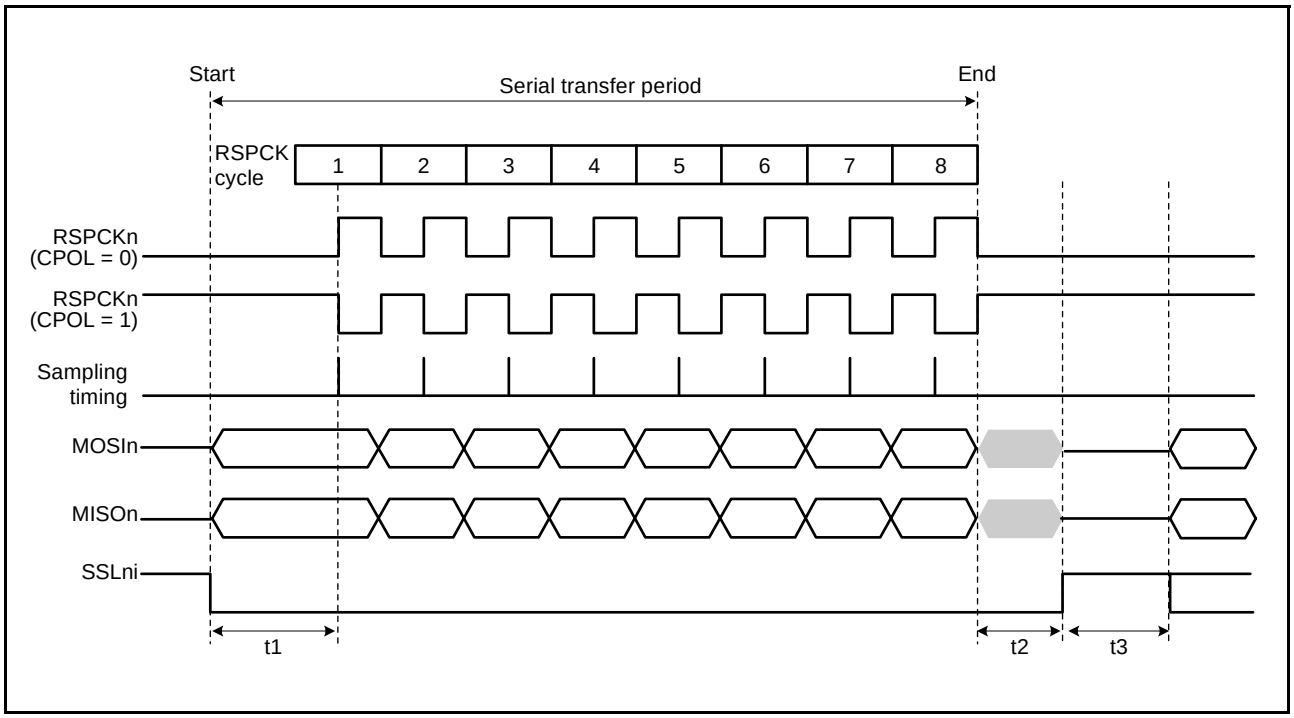


Figure 32.23 RSPI Transfer Format (CPHA = 0)

32.3.5.2 CPHA = 1

Figure 32.24 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three signals RSPCKn, MOSIn, and MISOn handle communications. In Figure 32.24, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0; RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the RSPI fetches serial transfer data into the shift register. The input/output directions of the signals depend on the RSPI mode (master or slave). For details, see section 32.3.2, Controlling RSPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOn signal commences at an SSLni signal assertion timing. The output of valid data to the MOSIn and MISOn signals commences at the first RSPCKn signal change timing that occurs after the SSLni signal assertion. After this timing, data is updated at every 1 RSPCK cycle. The transfer data fetch timing is always 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKn signal operation timing; it only affects the signal polarity.

t1, t2, and t3 are the same as those in the case of CPHA = 0. For a description of t1, t2, and t3 when the RSPI of this MCU is in master mode, see section 32.3.10.1, Master Mode Operation.

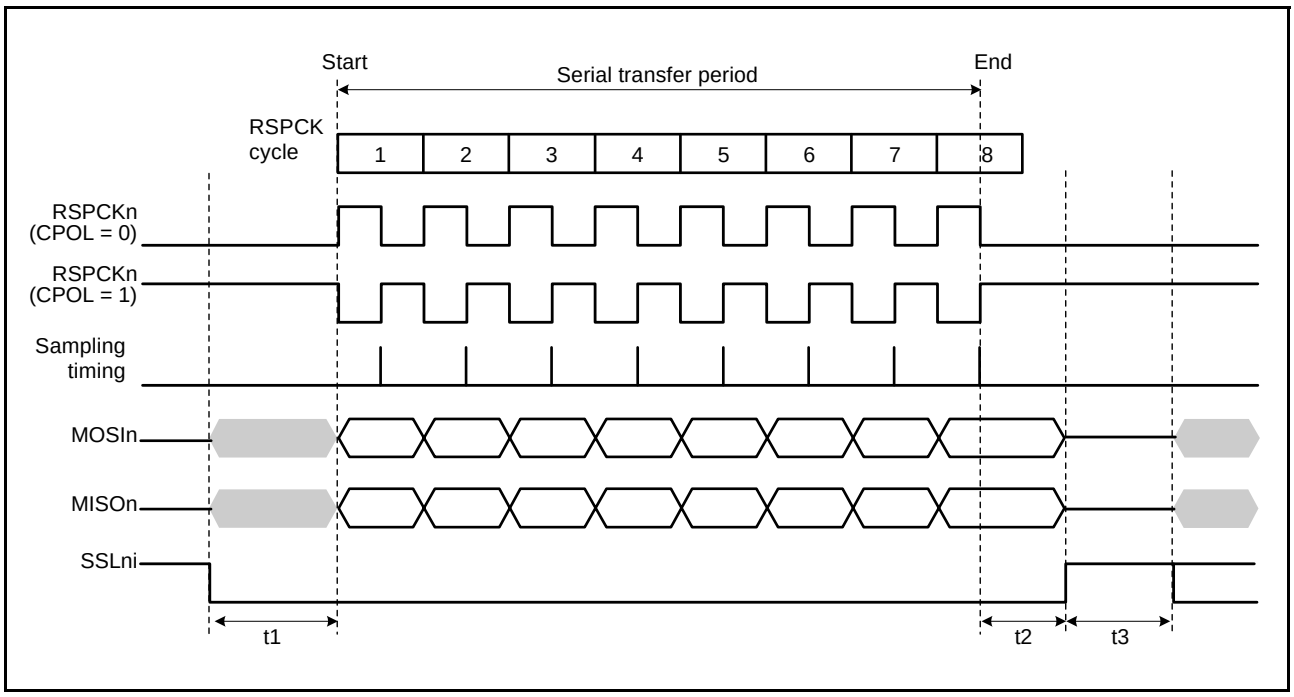


Figure 32.24 RSPI Transfer Format (CPHA = 1)

32.3.6 Communications Operating Mode

Full-duplex synchronous serial communications or transmit operations only can be selected by the communications operating mode select bit (SPCR.TXMD). The SPDR access shown in Figure 32.25 and Figure 32.26 indicates the condition of access to the SPDR register, where W denotes a write cycle.

32.3.6.1 Full-Duplex Synchronous Serial Communications (SPCR.TXMD = 0)

Figure 32.25 shows an example of operation when the communications operating mode select bit (SPCR.TXMD) is set to 0. In the example in Figure 32.25, the RSPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKn waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

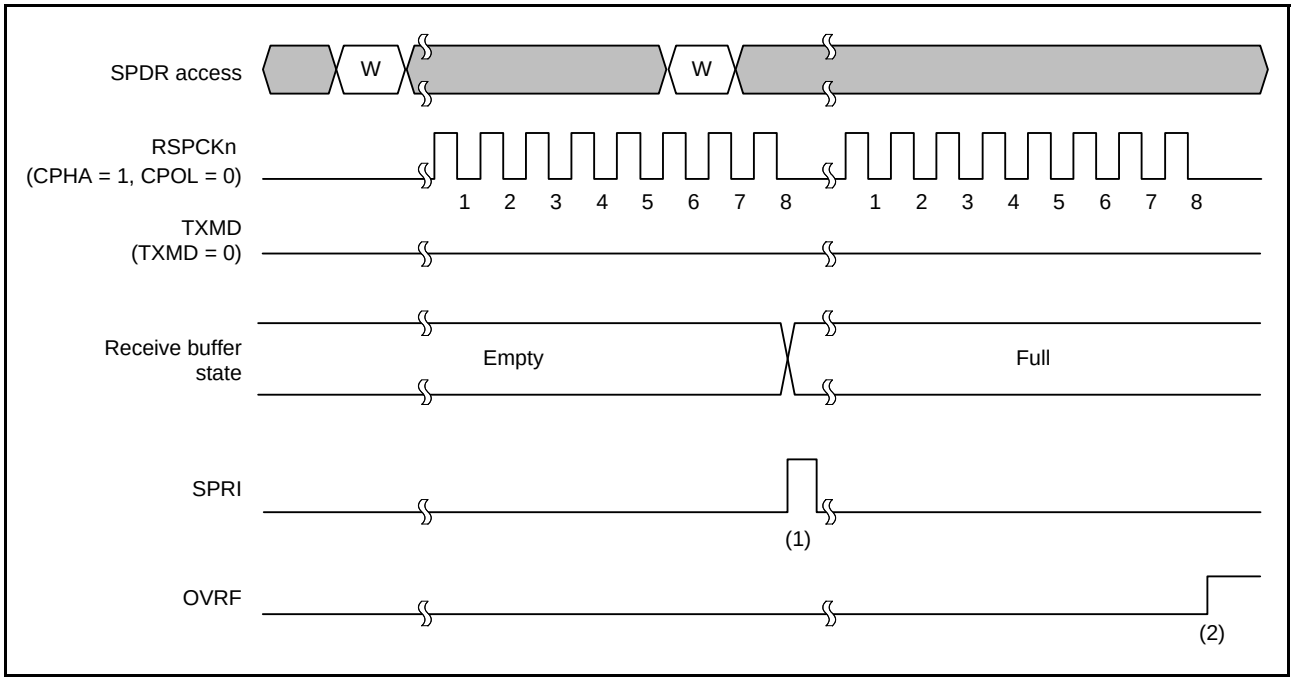


Figure 32.25 Operation Example of SPCR.TXMD = 0

The operation of the flags at timings shown in steps (1) and (2) in the figure is described below.

(1) When a serial transfer ends with the receive buffer of SPDR empty, the RSPI generates a receive buffer full interrupt request (SPRI) and copies the received data in the shift register to the receive buffer.

(2) When a serial transfer ends with the receive buffer of SPDR holding data that was received in the previous serial transfer, the RSPI sets the SPSR.OVRF flag to 1 and discards the received data in the shift register.

32.3.6.2 Transmit Operations Only (SPCR.TXMD = 1)

Figure 32.26 shows an example of operation when the communications operating mode select bit (SPCR.TXMD) is set to 1. In the example in Figure 32.26, the RSPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKn waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

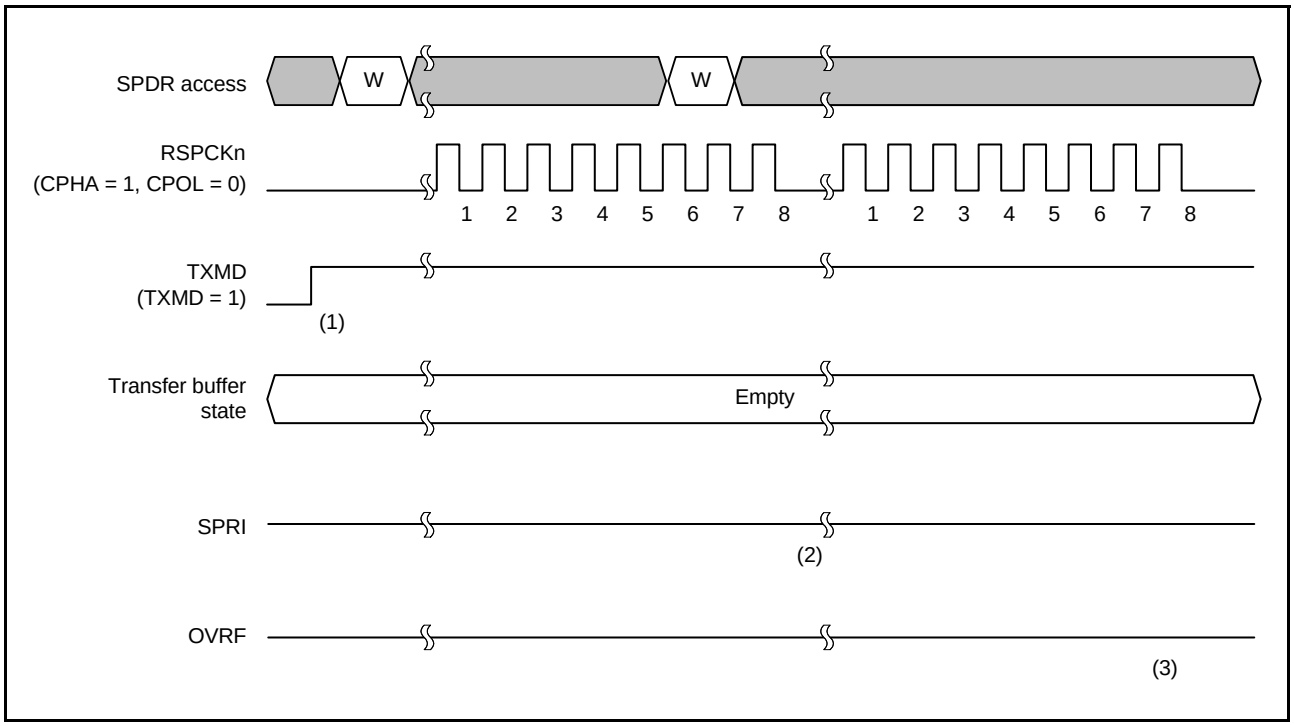


Figure 32.26 Operation Example of SPCR.TXMD = 1

The operation of the flags at timings shown in steps (1) to (3) in the figure is described below.

(1) Make sure there is no data left in the receive buffer and the SPSR.OVRF flag is 0 before entering the mode of transmit operations only (SPCR.TXMD = 1).

(2) When a serial transfer ends with the receive buffer of SPDR empty, if the mode of transmit operations only is selected (SPCR.TXMD = 1), the RSPI does not copy the data in the shift register to the receive buffer.

(3) Since the receive buffer of SPDR does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

When performing transmit operations only (SPCR.TXMD = 1), the RSPI transmits transmit data but does not receive received data. Therefore, the SPSR.OVRF flag remains cleared to 0 at the timings of (1) to (3).

32.3.7 Transmit Buffer Empty/Receive Buffer Full Interrupts

Figure 32.27 shows an example of operation of the RSPI transmit buffer empty interrupt (SPTI) and the RSPI receive buffer full interrupt (SPRI). The SPDR register access shown in Figure 32.27 indicates the condition of access to the SPDR register, where W denotes a write cycle, and R a read cycle. In the example in Figure 32.27, the RSPI performs an 8-bit serial transfer in which the SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKn waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

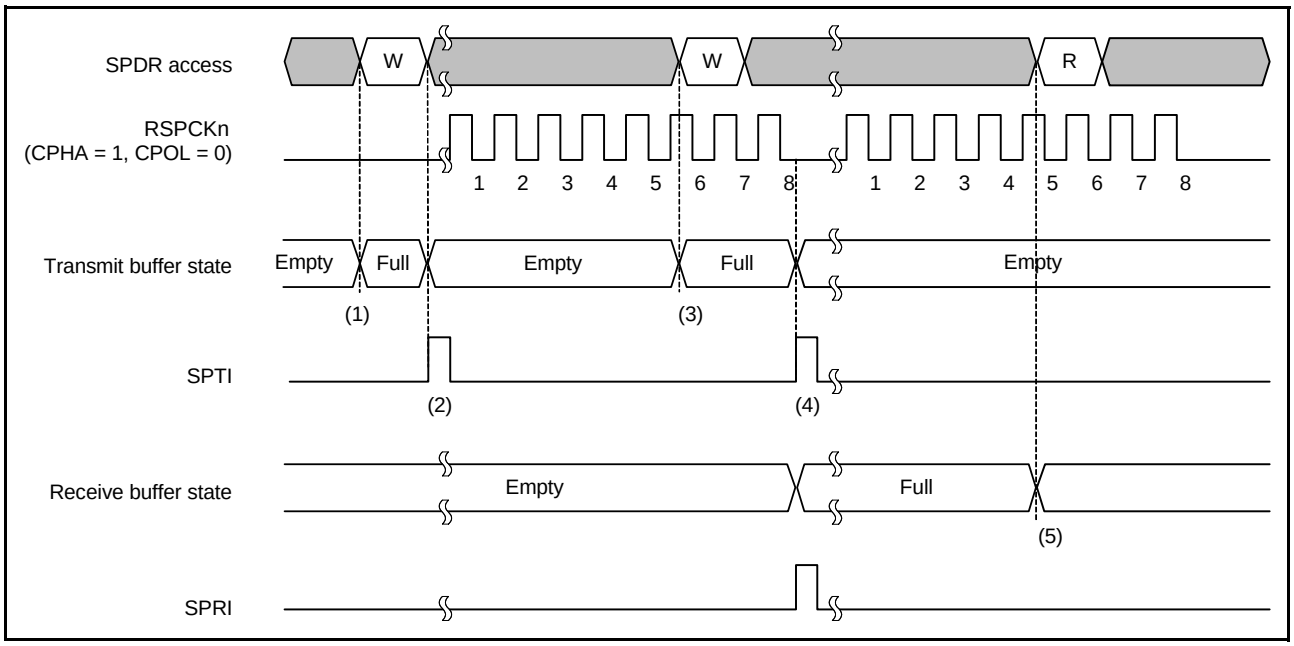


Figure 32.27 Operation Example of SPTI and SPRI Interrupts

The operation of the interrupts at timings shown in steps (1) to (5) in the figure is described below.

1. When transmit data is written to SPDR when the transmit buffer of SPDR is empty (data for the next transfer is not set), the RSPI writes data to the transmit buffer.
2. If the shift register is empty, the RSPI copies the data in the transmit buffer to the shift register and generates a transmit buffer empty interrupt request (SPTI). How a serial transfer is started depends on the mode of the RSPI. For details, see section 32.3.10, SPI Operation, and section 32.3.11, Clock Synchronous Operation.
3. When transmit data is written to SPDR by the transmit buffer empty interrupt routine, the data is transferred to the transmit buffer. Because the data being transferred serially is stored in the shift register, the RSPI does not copy the data in the transmit buffer to the shift register.
4. When the serial transfer ends with the receive buffer of SPDR being empty, the RSPI copies the receive data in the shift register to the receive buffer and generates a receive buffer full interrupt request (SPRI). Since the shift register becomes empty upon completion of serial transfer, when the transmit buffer had been full before the serial transfer ended, the RSPI copies the data in the transmit buffer to the shift register. Even when received data is not copied from the shift register to the receive buffer in an overrun error status, upon completion of the serial transfer, the RSPI determines that the shift register is empty, thus data transfer from the transmit buffer to the shift register is enabled.
5. When SPDR is read by the receive buffer full interrupt routine, the receive data can be read.

If SPDR is written to when the transmit buffer holds data that has not yet been transmitted, the RSPI does not update the data in the transmit buffer. When writing to SPDR, make sure to use a transmit buffer empty interrupt request. To use an RSPI transmit interrupt, set the SPTIE bit in SPCR to 1.
If the RSPI function is disabled (the SPE bit in SPCR being 0), set the SPTIE bit to 0.
When serial transfer ends with the receive buffer being full, the RSPI does not copy data from the shift register to the receive buffer, and detects an overrun error (see section 32.3.8, Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an RSPI receive interrupt, set the SPCR.SPRIE bit to 1.
Transmission and reception interrupts or the corresponding IRn.IR flags (where n is the vector number) in ICU can be used to confirm the states of the transmission and reception buffers. See section 15, Interrupt controller (ICUb), for the vector numbers.

32.3.8 Error Detection

In the normal RSPI serial transfer, the data written to the transmit buffer of SPDR is serially transmitted, and the serially received data can be read from the receive buffer of SPDR. If access is made to SPDR, depending on the status of the transmit/receive buffer or the status of the RSPI at the beginning or end of serial transfer, in some cases non-normal transfers can be executed.

If a non-normal transfer operation occurs, the RSPI detects the event as an overrun error, parity error, or mode fault error. Table 32.8 lists the relationship between non-normal transfer operations and the RSPI's error detection function.

Table 32.8 Relationship between Non-Normal Transfer Operations and RSPI Error Detection Function

	Occurrence Condition	RSPI Operation	Error Detection
A	SPDR is written when the transmit buffer is full.	• The contents of the transmit buffer are kept. • Missing write data.	None
B	Serial transfer is started in slave mode when transmit data is still not loaded on the shift register.	Data received in previous serial transfer is serially transmitted.	None
C	SPDR is read when the receive buffer is empty.	Previously received serial data is output.	None
D	Serial transfer terminates when the receive buffer is full.	• The contents of the receive buffer are kept. • Missing serial receive data.	Overrun error
E	An incorrect parity bit is received when performing full-duplex synchronous serial communications with the parity function enabled.	The parity error flag is asserted.	Parity error
F	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode.	• Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped. • RSPI function is disabled.	Mode fault error
G	The SSLn0 input signal is asserted during serial transfer in multi-master mode.	• Serial transfer is suspended. • Missing transmit/receive data. • Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped. • RSPI function is disabled.	Mode fault error
H	The SSLn0 input signal is negated during serial transfer in slave mode.	• Serial transfer is suspended. • Missing transmit/receive data. • Driving of the MISOn output signal is stopped. • RSPI function is disabled.	Mode fault error

On operation A described in Table 32.8, the RSPI does not detect an error. To prevent data omission during the writing to SPDR, write operations to SPDR should be executed using a transmit interrupt request.

Likewise, the RSPI does not detect an error on operation B. In a serial transfer that was started before the shift register was updated, the RSPI sends the data that was received in the previous serial transfer, and does not treat the operation indicated in B as an error. Note that the received data from the previous serial transfer is retained in the receive buffer of SPDR, thus it can be correctly read (if SPDR is not read before the end of the serial transfer, an overrun error may occur).

Similarly, the RSPI does not detect an error on operation C. To prevent extraneous data from being read, SPDR read operation should be executed using a receive interrupt request.

An overrun error shown in D is described in section 32.3.8.1, Overrun Error. A parity error shown in E is described in section 32.3.8.2, Parity Error. A mode fault error shown in F to H is described in section 32.3.8.3, Mode Fault Error.

For the transmit and receive interrupts, refer to section 32.3.7, Transmit Buffer Empty/Receive Buffer Full Interrupts.

32.3.8.1 Overrun Error

If a serial transfer ends when the receive buffer of SPDR is full, the RSPI detects an overrun error, and sets the OVRF flag in SPSR to 1. When the OVRF flag is 1, the RSPI does not copy data from the shift register to the receive buffer so that the data prior to the occurrence of the error is retained in the receive buffer. To set the OVRF flag to 0, write 0 to the OVRF flag after the CPU has read SPSR with the OVRF flag set to 1.

Figure 32.28 shows an example of operation of the OVRF flag. The SPSR and SPDR accesses shown in Figure 32.28 indicate the condition of accesses to SPSR and SPDR, respectively, where W denotes a write cycle, and R a read cycle. In the example in Figure 32.28, the RSPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKn waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

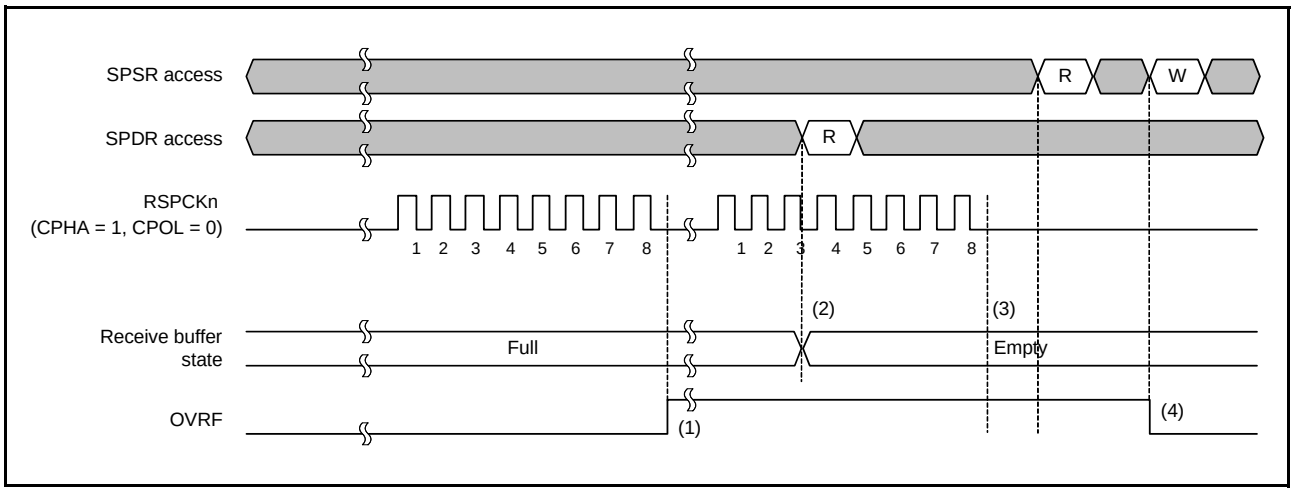


Figure 32.28 Operation Example of OVRF Flag

The operation of the flags at the timing shown in steps (1) to (4) in the figure is described below.

1. If a serial transfer terminates with the receive buffer full, the RSPI detects an overrun error, and sets the OVRF flag to 1. The RSPI does not copy the data in the shift register to the receive buffer. Even if the SPPE bit is 1, parity errors are not detected. In master mode, the RSPI copies the pointer value to SPCMDm register to the SPSSR.SPECM[2:0] bits.
2. When SPDR is read, the RSPI outputs the data in the receive buffer can be read. The receive buffer becoming empty does not clear the OVRF flag.
3. If the serial transfer ends with the OVRF flag being 1 (an overrun error), the RSPI does not copy the data in the shift register to the receive buffer. A reception-buffer interrupt is not generated. Even if the SPPE bit is 1, parity errors are not detected. When in master mode, the RSPI does not update the SPSSR.SPECM[2:0] bits. When in an overrun error state and the RSPI does not copy the received data from the shift register to the receive buffer, upon termination of the serial transfer, the RSPI determines that the shift register is empty; in this manner, data transfer from the transmit buffer to the shift register is enabled.
4. If the value 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, OVRF flag is cleared to 0.

The occurrence of an overrun can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. When executing a serial transfer, measures should be taken to ensure the early detection of overrun errors, such as reading SPSR immediately after SPDR is read. When the RSPI is used in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

If an overrun error occurs and the OVRF flag is set to 1, normal reception operations cannot be performed until the OVRF flag is cleared.

32.3.8.2 Parity Error

If full-duplex synchronous serial communications is performed with the SPCR.TXMD bit cleared to 0 and the SPCR2.SPPE bit set to 1, when serial transfer ends, the RSPI checks whether there are parity errors. Upon detecting a parity error in the received data, the RSPI sets the SPSR.PERF flag to 1. Since the RSPI does not copy the data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after SPSR register is read with the PERF flag set to 1. Figure 32.29 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 32.29 indicates the condition of access to SPSR register, where W denotes a write cycle, and R a read cycle. In the example of Figure 32.29, full-duplex synchronous serial communications is performed while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The RSPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKn waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

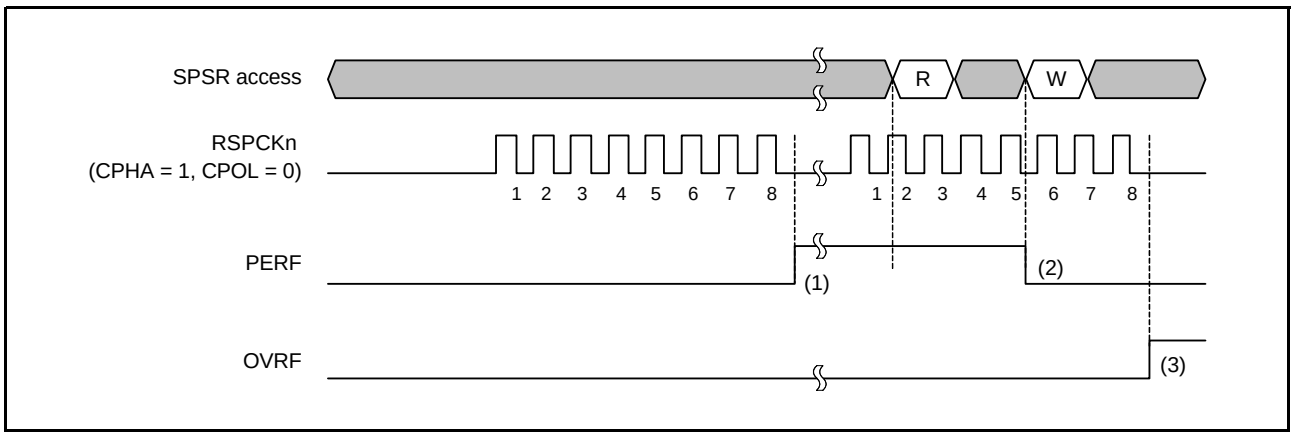


Figure 32.29 Operation Example of PERF Flag

The operation of the flags at the timing shown in steps (1) to (3) in the figure is described below.

1. If a serial transfer terminates with the RSPI not detecting an overrun error, the RSPI copies the data in the shift register to the receive buffer. The RSPI judges the received data at this timing, and sets the PERF flag to 1 if a parity error is detected. In master mode, the RSPI copies the pointer value to SPCMDm register to the SPSSR.SPECM[2:0] bits.
2. If the value 0 is written to the PERF flag after SPSR register is read when the PERF flag is 1, the OVRF flag is cleared to 0.
3. When the RSPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The RSPI does not perform parity error detection at this timing.

The occurrence of a parity error can be checked either by reading SPSR register or by using an RSPI error interrupt and reading SPSR register. When executing a serial transfer, measures should be taken to ensure the early detection of parity errors, such as reading SPSR. When the RSPI is used in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

32.3.8.3 Mode Fault Error

The RSPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input with respect to the SSLn0 input signal of the RSPI in multi-master mode, the RSPI detects a mode fault error irrespective of the status of the serial transfer, and sets the MODF bit in the RSPI status register (SPSR) to 1. Upon detecting the mode fault error, the RSPI copies the value of the pointer to SPCMDm to the SPSSR.SPECM[2:0] bits. The active level of the SSLn0 signal is determined by the SSL0P bit in the RSPI slave select polarity register (SSLP).

When the MSTR bit is 0, the RSPI operates in slave mode. The RSPI detects a mode fault error if the MODFEN bit in the RSPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

Upon detecting a mode fault error, the RSPI stops driving of the output signals and clears the SPCR.SPE bit to 0 (see section 32.3.9, Initializing RSPI). In the case of multi-master configuration, detection of a mode fault error is used to stop driving of the output signals and the RSPI function, which allows the master right to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. Detecting mode-fault errors without utilizing the RSPI error interrupt requires polling of SPSR. When using the RSPI in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF bit is 1, writing of the value 1 to the SPE bit is ignored by the RSPI. To enable the RSPI function after the detection of a mode fault error, the MODF bit must be set to 0.

32.3.9 Initializing RSPI

If the value 0 is written to the SPE bit in the RSPI control register (SPCR) or the RSPI clears the SPE bit to 0 because of the detection of a mode fault error, the RSPI disables the RSPI function, and initializes some of the module functions. When a system reset is generated, the RSPI initializes all of the module functions. The following describes initialization by the clearing of the SPE bit in SPCR and initialization by a system reset.

32.3.9.1 Initialization by Clearing the SPE Bit

When the SPE bit in SPCR is cleared, the RSPI performs the following initialization:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the RSPI
- Initializing the transmit buffer of the RSPI

Initialization by the clearing of the SPE bit does not initialize the control bits of the RSPI. For this reason, the RSPI can be started in the same transfer mode as prior to the initialization if the SPE bit is set to 1 again.
The OVRF and MODF flags in SPSR are not initialized, nor is the value of the RSPI sequence status register (SPSSR) initialized. For this reason, even after the RSPI is initialized, data from the receive buffer can be read in order to check the status of error occurrence during an RSPI transfer.
The transmit buffer is initialized to an empty state. Therefore, if the SPTIE bit in SPCR is set to 1 after RSPI initialization, an RSPI transmit interrupt is generated. When the RSPI is initialized by the CPU, in order to disable any RSPI transmit interrupt, the value 0 should be written to the SPTIE bit simultaneously with the writing of the value 0 to the SPE bit. To disable any RSPI transmit interrupt after a mode fault error is detected, use an error handling routine to write the value 0 to the SPTIE bit.

32.3.9.2 System Reset

The initialization by a system reset completely initializes the RSPI through the initialization of all bits for controlling the RSPI, initialization of the status bits, and initialization of data registers, in addition to the requirements described in section 32.3.9.1, Initialization by Clearing the SPE Bit.

32.3.10 SPI Operation

32.3.10.1 Master Mode Operation

The only difference between single-master mode operation and multi-master mode operation lies in mode fault error detection (see section 32.3.8, Error Detection). When operating in single-master mode, the RSPI does not detect mode fault errors whereas the RSPI running in multi-master mode does detect mode fault errors. This section explains operations that are common to single-master mode and multi-master mode.

(1) Starting a Serial Transfer

The RSPI updates the data in the transmit buffer (SPTX) when data is written to the RSPI data register (SPDR) with the RSPI transmit buffer being empty (data for the next transfer is not set). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR, the RSPI copies data from the transmission buffer to the shift register and starts serial transfer. Upon copying transmit data to the shift register, the RSPI changes the status of the shift register to “full”, and upon termination of serial transfer, it changes the status of the shift register to “empty”. The status of the shift register cannot be referenced.
For details on the RSPI transfer format, see section 32.3.5, Transfer Format. The polarity of the SSLni output pins depends on the SSLP register settings.

(2) Terminating a Serial Transfer

Irrespective of the CPHA bit in the RSPI command register (SPCMDm), the RSPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the final sampling timing. If free space is available in the receive buffer (SPRX), upon termination of serial transfer, the RSPI copies data from the shift register to the receive buffer of the RSPI data register (SPDR).
It should be noted that the final sampling timing varies depending on the bit length of transfer data. In master mode, the RSPI data length depends on the SPCMDm.SPB[3:0] bit setting. The polarity of the SSLni output pin depends on the SSLP register settings.
For details on the RSPI transfer format, see section 32.3.5, Transfer Format.

(3) Sequence Control

The transfer format that is employed in master mode is determined by SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.
SPSCR is a register used to determine the sequence configuration for serial transfers that are executed by the RSPI in master mode. The following items are set in SPCMDm register: SSLni pin output signal value, MSB/LSB first, data length, some of the bit rate settings, RSPCK polarity/phase, whether SPCKD is to be referenced, whether SSLND is to be referenced, and whether SPND is to be referenced. SPBR holds some of the bit rate settings; SPCKD, an RSPI clock delay value; SSLND, an SSL negation delay; and SPND, a next-access delay value.
According to the sequence length that is assigned to SPSCR, the RSPI makes up a sequence comprised of a part or all of SPCMDm register. The RSPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the RSPI function is enabled, the RSPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The RSPI increments the pointer each time the next-access delay period for a data transfer ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, the RSPI sets the pointer in SPCMD0, and in this manner the sequence is executed repeatedly.

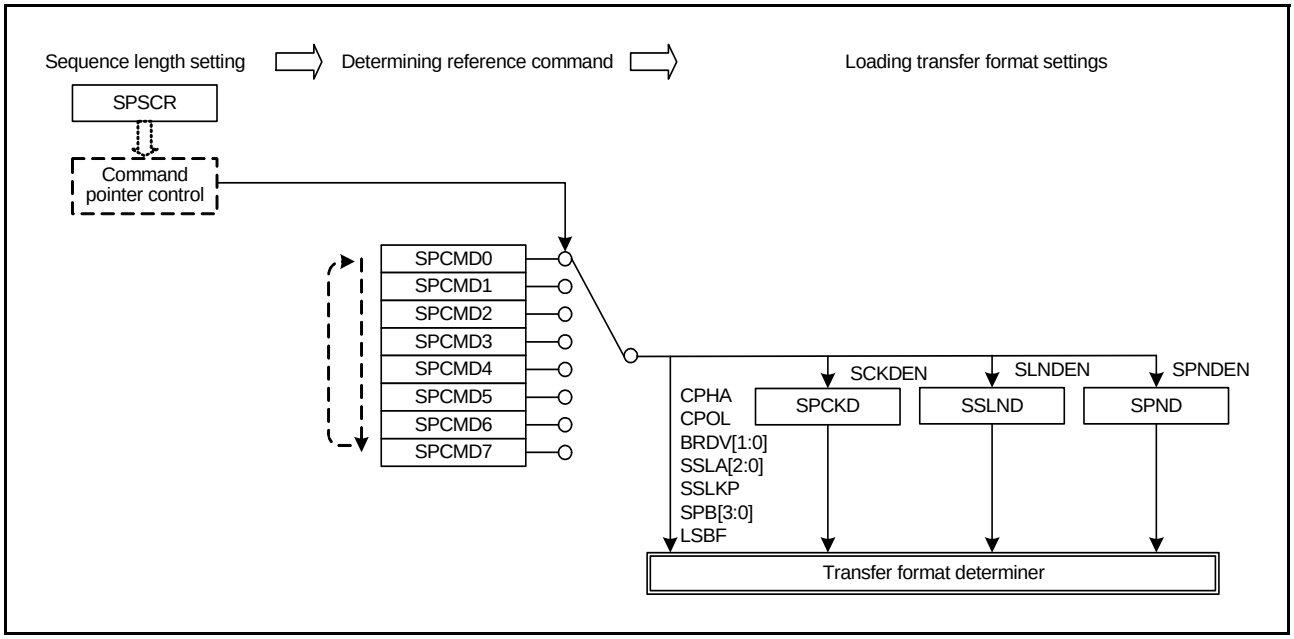


Figure 32.30 Procedure for Determining the Form of Serial Transmission in Master Mode

In this section, a frame is the combination of the data (SPDR) and the settings (SPCMDm).

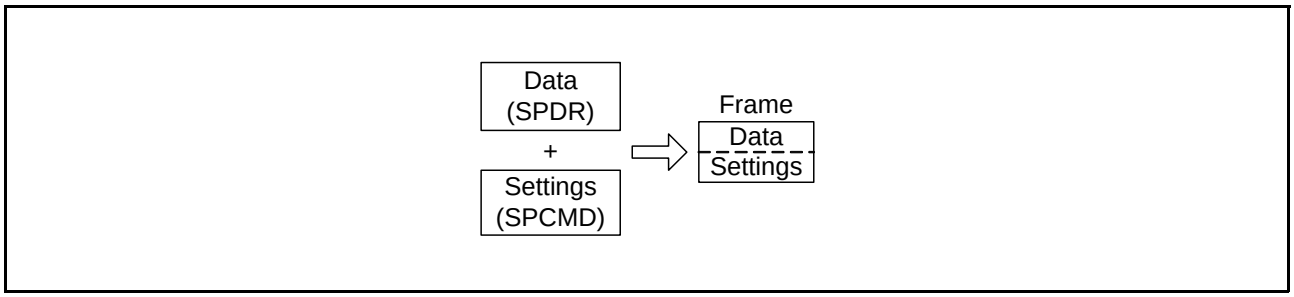


Figure 32.31 Concept of a Frame

Figure 32.32 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 32.4.

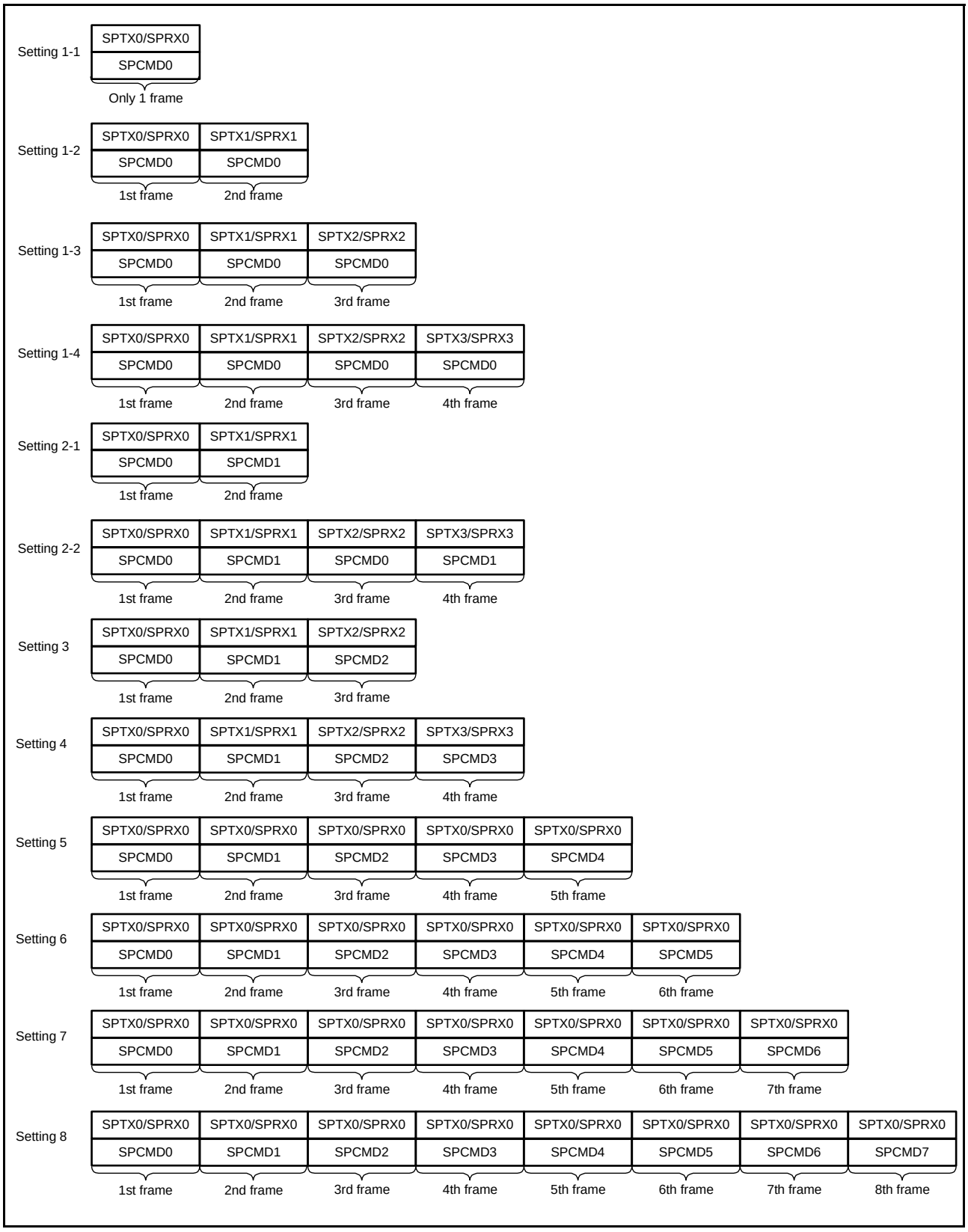


Figure 32.32 Correspondence between the RSPI Command Register and Transmit/Receive Buffers in Sequence Operations

(4) Burst Transfer

If the SSLKP bit in the RSPI command register (SPCMDm) that the RSPI references during the current serial transfer is 1, the RSPI keeps the SSLni signal level during the serial transfer until the beginning of the SSLni signal assertion for the next serial transfer. If the SSLni signal level for the next serial transfer is the same as the SSLni signal level for the current serial transfer, the RSPI can execute continuous serial transfers while keeping the SSLni signal assertion status (burst transfer).

Figure 32.33 shows an example of an SSLni signal operation for the case where a burst transfer is implemented using SPCMD0 and SPCMD1 register settings. The text below explains the RSPI operations (1) to (7) as shown in Figure 32.33. It should be noted that the polarity of the SSLni output signal depends on the SSLP register settings.

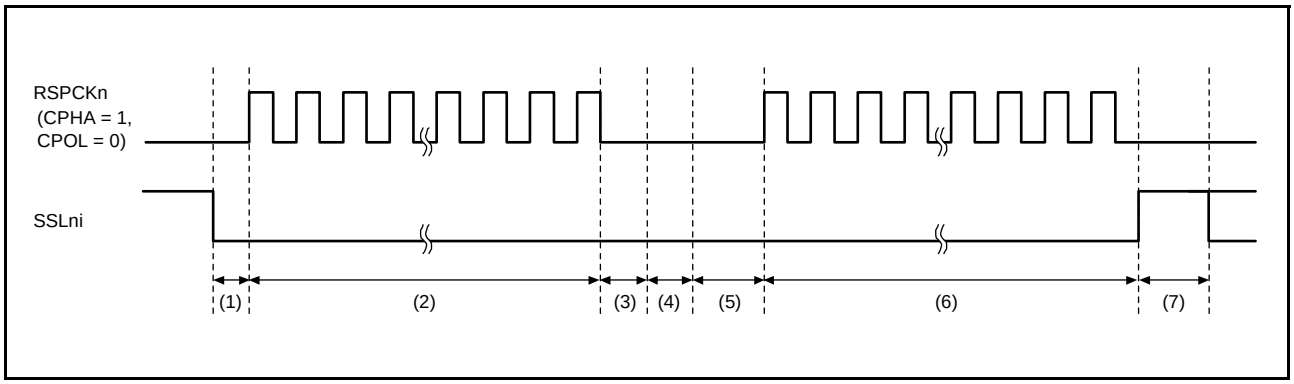


Figure 32.33 Example of Burst Transfer Operation using SSLKP Bit

(1) Based on SPCMD0, the RSPI asserts the SSLni signal and inserts RSPCK delays.
(2) The RSPI executes serial transfers according to SPCMD0.
(3) The RSPI inserts SSL negation delays.
(4) Since the SPCMD0.SSLKP bit is 1, the RSPI keeps the SSLni signal value on SPCMD0. This period is sustained, at the shortest, for a period equal to the next-access delay of SPCMD0. If the shift register is empty after the passage of a minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
(5) Based on SPCMD1, the RSPI asserts the SSLni signal and inserts RSPCK delays.
(6) The RSPI executes serial transfers according to SPCMD1.
(7) Because the SPCMD1.SSLKP bit is 0, the RSPI negates the SSLni signal. In addition, a next-access delay is inserted according to SPCMD1.

If the SSLni signal output settings in the SPCMDm register in which 1 is assigned to the SSLKP bit are different from the SSLni signal output settings in the SPCMDm register to be used in the next transfer, the RSPI switches the SSLni signal status to SSLni signal assertion ((5) in Figure 32.33) corresponding to the command for the next transfer. Note that if such an SSLni signal switching occurs, the slaves that drive the MISOn signal compete, and collision of signal levels may occur.

The RSPI in master mode references the SSLni signal operation within the module for the case where the SSLKP bit is not used. Even when the SPCMDm.CPHA bit is 0, the RSPI can accurately start serial transfers by using the SSLni signal assertion for the next transfer that is detected internally. For this reason, burst transfers in master mode can be executed irrespective of CPHA bit settings (see section 32.3.10, SPI Operation).

(5) RSPCK Delay (t1)

The RSPCK delay value of the RSPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD register setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines an RSPCK delay value during serial transfer by using the SPCMDm.SCKDEN bit and SPCKD, as listed in Table 32.9. For a definition of RSPCK delay, see section 32.3.5, Transfer Format.

Table 32.9 Relationship among SCKDEN Bit, SPCKD, and RSPCK Delay Value

SPCMDm.SCKDEN Bit	SPCKD.SCKDL[2:0] Bits	RSPCK Delay Value
0	000 to 111	1 RSPCK
1	000	1 RSPCK
	001	2 RSPCK
	010	3 RSPCK
	011	4 RSPCK
	100	5 RSPCK
	101	6 RSPCK
	110	7 RSPCK
	111	8 RSPCK

(6) SSL Negation Delay (t2)

The SSL negation delay value of the RSPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND register setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines an SSL negation delay value during serial transfer by using the SPCMDm.SLNDEN bit and SSLND, as listed in Table 32.10. For a definition of SSL negation delay, see section 32.3.5, Transfer Format.

Table 32.10 Relationship among SLNDEN Bit, SSLND, and SSL Negation Delay Value

SPCMDm.SLNDEN Bit	SSLND.SLNDL[2:0] Bits	SSL Negation Delay Value
0	000 to 111	1 RSPCK
1	000	1 RSPCK
	001	2 RSPCK
	010	3 RSPCK
	011	4 RSPCK
	100	5 RSPCK
	101	6 RSPCK
	110	7 RSPCK
	111	8 RSPCK

(7) Next-Access Delay (t3)

The next-access delay value of the RSPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines a next-access delay value during serial transfer by using the SPCMDm.SPNDEN bit and SPND, as listed in Table 32.11. For a definition of next-access delay, see section 32.3.5, Transfer Format.

Table 32.11 Relationship among SPNDEN Bit, SPND, and Next-Access Delay Value

SPCMDm.SPNDEN Bit	SPND.SPNDL[2:0] Bits	Next-Access Delay Value
0	000 to 111	1 RSPCK + 2 PCLK
1	000	1 RSPCK + 2 PCLK
	001	2 RSPCK + 2 PCLK
	010	3 RSPCK + 2 PCLK
	011	4 RSPCK + 2 PCLK
	100	5 RSPCK + 2 PCLK
	101	6 RSPCK + 2 PCLK
	110	7 RSPCK + 2 PCLK
	111	8 RSPCK + 2 PCLK

(8) Initialization Flowchart

Figure 32.34 is a flowchart illustrating an example of initialization in SPI operation when the RSPI is used in master mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, see the descriptions given in the individual blocks.

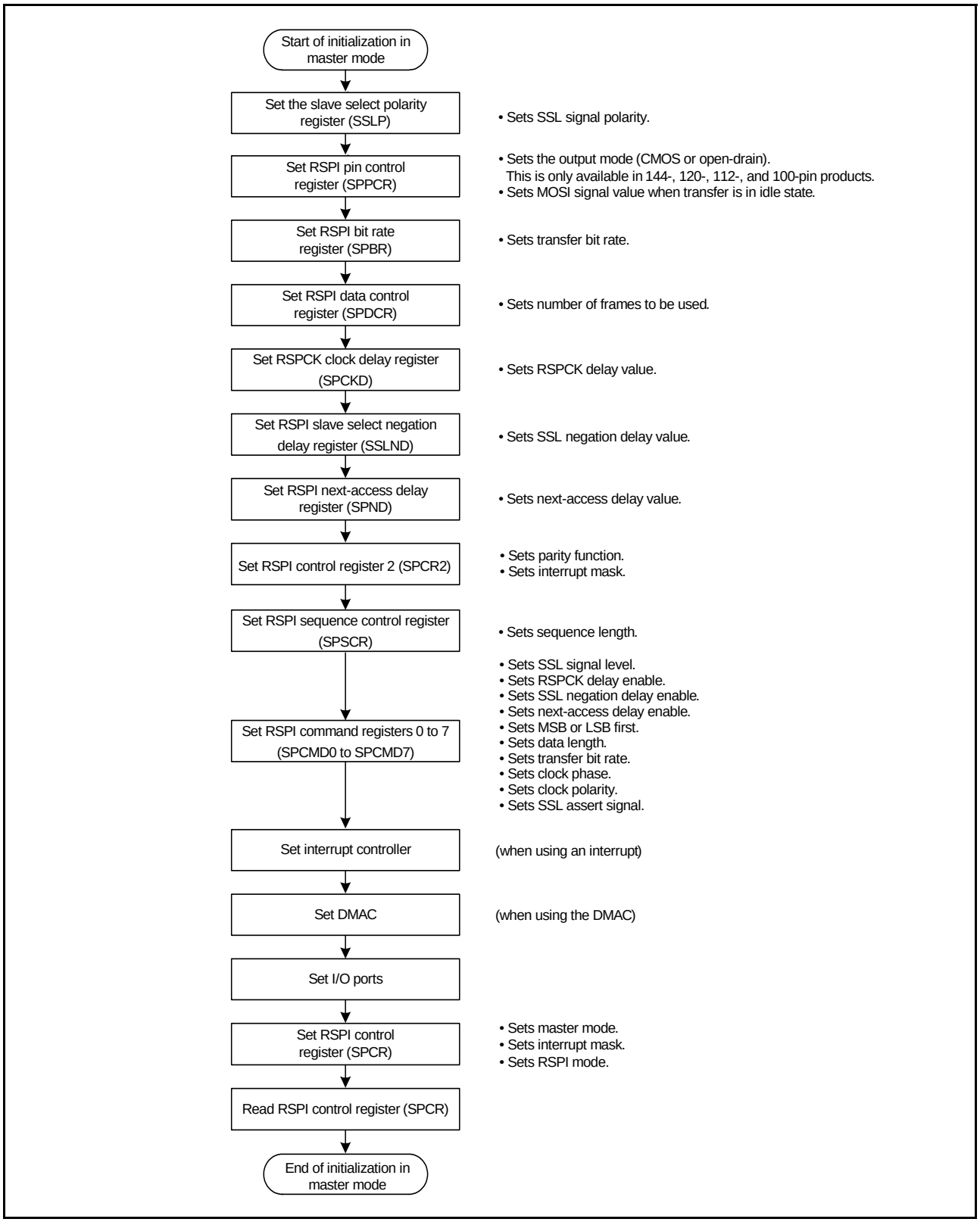


Figure 32.34 Example of Initialization Flowchart in Master Mode (SPI Operation)

(9) Software Processing Flow

Figure 32.35 to Figure 32.37 show examples of the flow of software processing.

(a) Transmit Processing Flow

When transmitting data, the CPU will be notified of the completion of data transmission after the last writing of data for transmission if the SPII interrupt is enabled.
The completion of data transmission can also be checked by polling to see if the SPSR.IDLNF flag has become 0, instead of using the SPII interrupt. However, one cycle of PCLK is required for the time from when data for transmission is written in the SPDR register to when the IDLNF flag becomes 1. After the last data is written in the SPDR register, discard the value of the SPSR register once not to judge the condition with the IDLNF flag which has not yet become 1, and read and use the value of the SPSR.IDLNF flag to confirm the completion of data transmission.

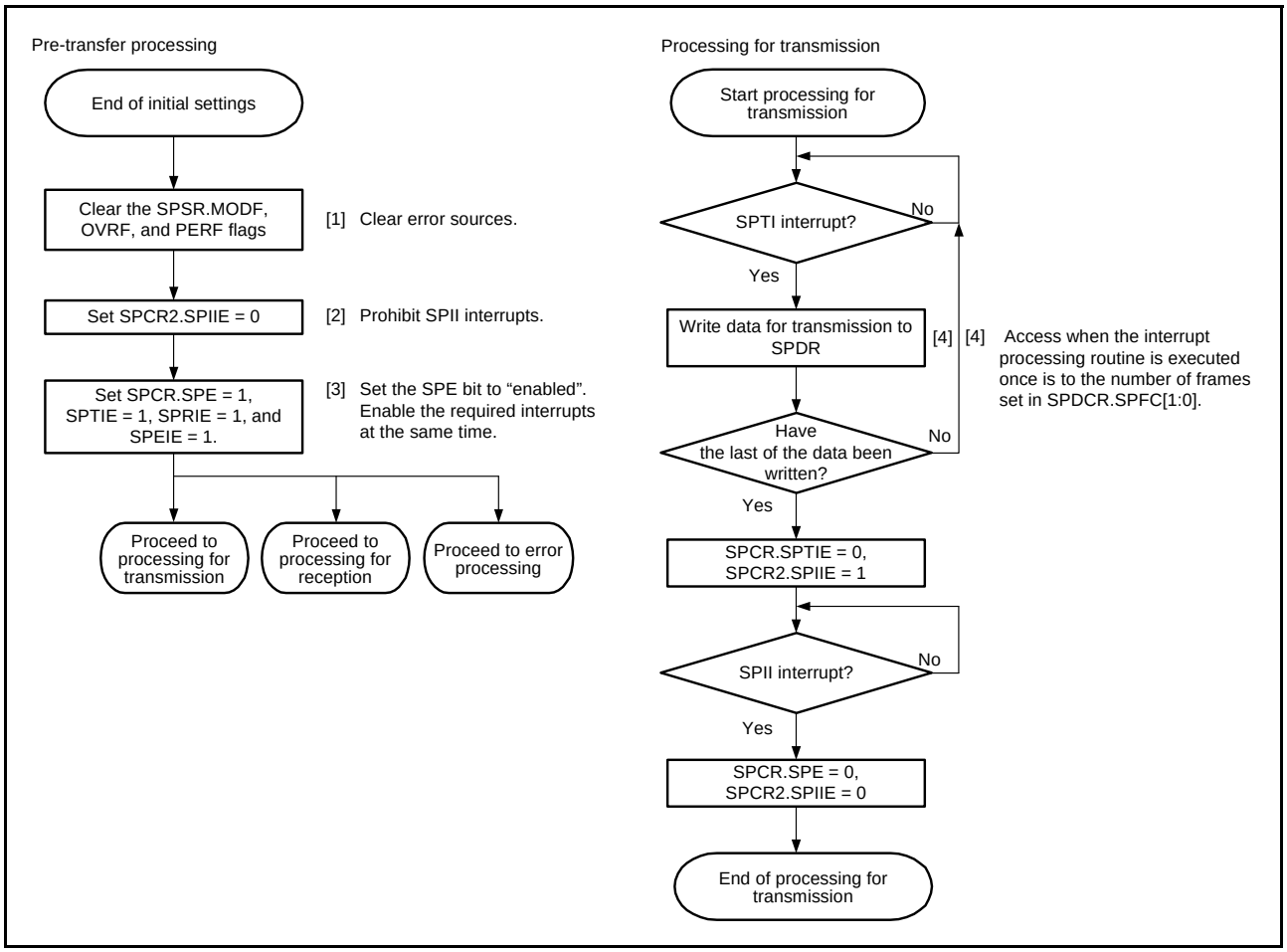


Figure 32.35 Flowchart in Master Mode (Transmission)

(b) Receive Processing Flow

The RSPI does not handle receive-only operation, so processing for transmission is required if reception is to proceed.

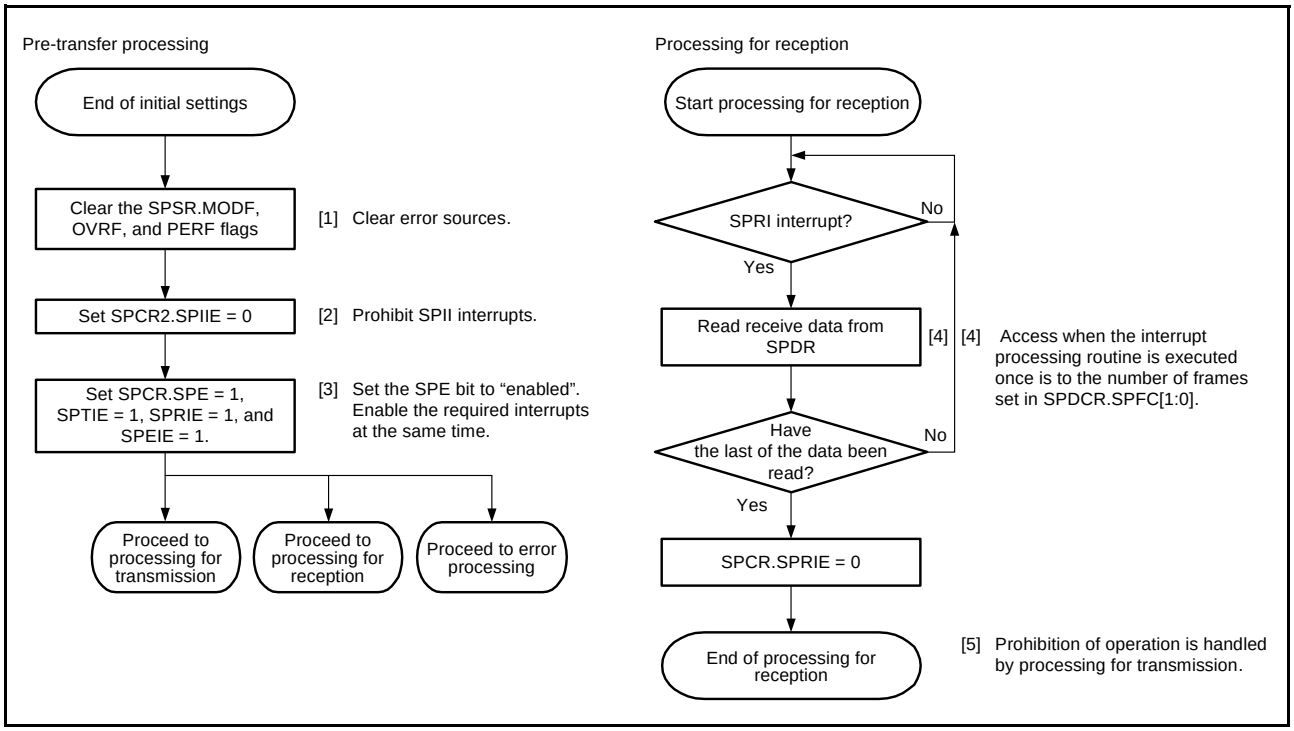


Figure 32.36 Flowchart in Master Mode (Reception)

(c) Flow of error processing

The RSPI has three types of error. When a mode-fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, however, the SPCR.SPE bit is not cleared and operations for transmission and reception continue; accordingly, we recommend clearing of the SPCR.SPE bit to stop operations in the case of errors other than mode-fault errors. Not doing so will lead to updating of the SPSSR.SPECM[2:0] bits.

When an error occurs, clear the ICU.IRn.IR flag from within the error processing routine. If this is not done, the ICU.IRn.IR flag may continue to indicate the SPTI interrupt or SPRI interrupt request. If SPRI interrupt request is retained, read the receive buffer to initialize the RSPI internal sequencer.

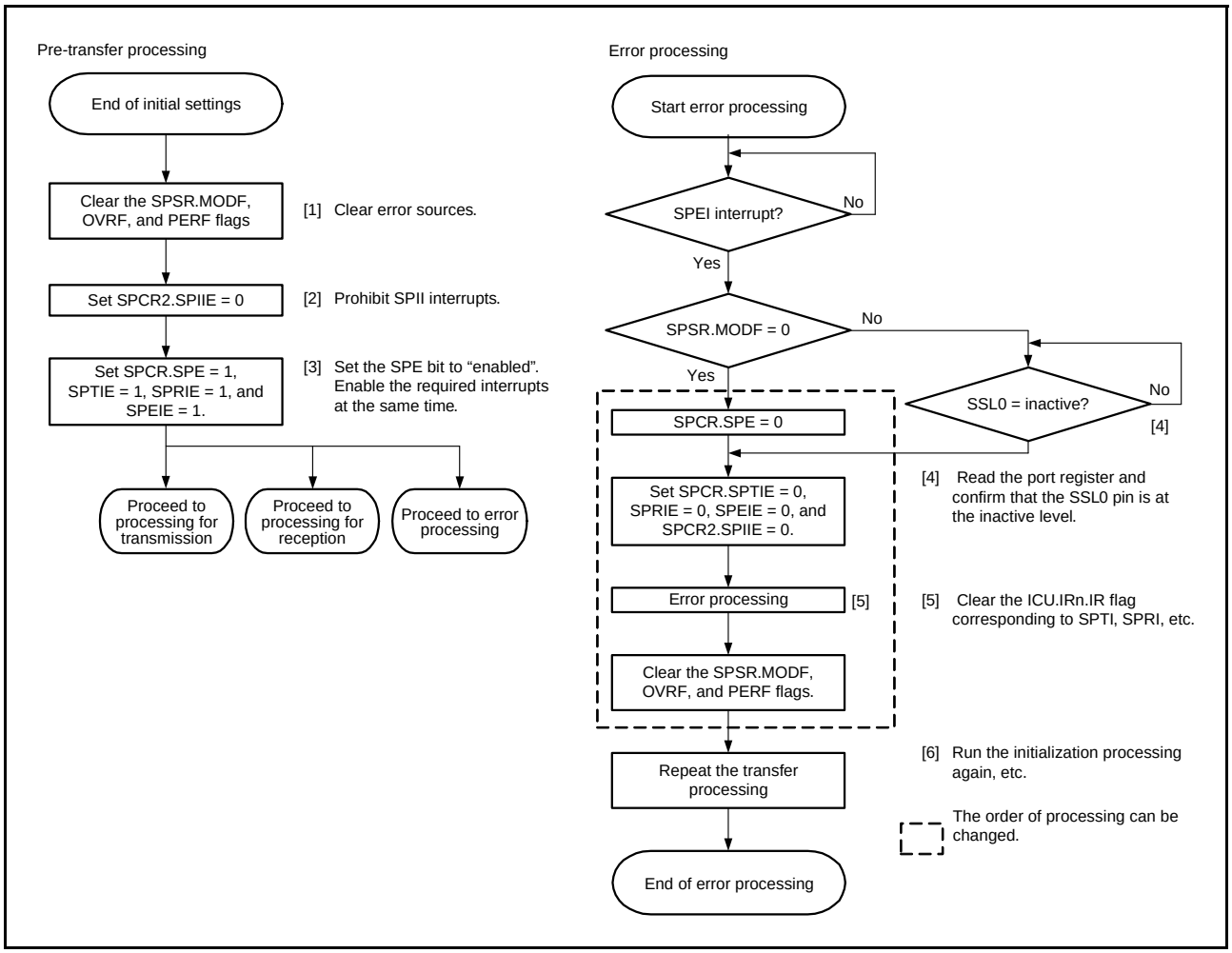


Figure 32.37 Flowchart for Master Mode (Error Processing)

32.3.10.2 Slave Mode Operation

(1) Starting a Serial Transfer

If the SPCMD0.CPHA bit is 0, when detecting an SSLn0 input signal assertion, the RSPI needs to start driving valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.
If the CPHA bit is 1, when detecting the first RSPCKn edge in an SSLn0 signal asserted condition, the RSPI needs to start driving valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.
When detecting the start of a serial transfer in a condition in which the shift register is empty, the RSPI changes the status of the shift register to “full”, so that data cannot be copied from the transmit buffer to the shift register when serial transfer is in progress. If the shift register was full before the serial transfer started, the RSPI leaves the status of the shift register unchanged, in the full state.
Irrespective of CPHA bit setting, the timing at which the RSPI starts driving of the MISOn output signal is the SSLn0 signal assertion timing. The data which is output by the RSPI is either valid or invalid, depending on the CPHA bit setting.
For details on the RSPI transfer format, see section 32.3.5, Transfer Format. The polarity of the SSLn0 input signal depends on the setting of the SSL0P bit in the RSPI slave select polarity register (SSLP).

(2) Terminating a Serial Transfer

Irrespective of the SPCMD0.CPHA bit, the RSPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer, upon termination of serial transfer the RSPI copies received data from the shift register to the receive buffer of the RSPI data register (SPDR).
Upon termination of a serial transfer the RSPI changes the status of the shift register to “empty”, regardless of the receive buffer state. A mode fault error occurs if the RSPI detects an SSLn0 input signal negation from the beginning of serial transfer to the end of serial transfer (see section 32.3.8, Error Detection).
The final sampling timing changes depending on the bit length of transfer data. In slave mode, the RSPI data length depends on the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P bit setting.
For details on the RSPI transfer format, see section 32.3.5, Transfer Format.

(3) Notes on Single-Slave Operations

If the SPCMD0.CPHA bit is 0, the RSPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the type of configuration shown in Figure 32.7 as an example, if the RSPI is used in single-slave mode, the SSLn0 signal is always fixed at the active state. Therefore, when the CPHA bit is set to 0, the RSPI cannot correctly start a serial transfer. To correctly execute transmit/receive operations by the RSPI in slave mode in a configuration in which the SSLn0 input signal is fixed at the active state, the CPHA bit should be set to 1. If there is a need for setting the CPHA bit to 0, the SSLn0 input signal should not be fixed.

(4) Burst Transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. If the CPHA bit is 1, the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state corresponds to a serial transfer period. Even when the SSLn0 input signal remains at the active level, the RSPI can accommodate burst transfers because it can detect the start of an access.
If the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization Flowchart

Figure 32.38 is a flowchart illustrating an example of initialization in SPI operation when the RSPI is used in slave mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, see the descriptions given in the individual blocks.

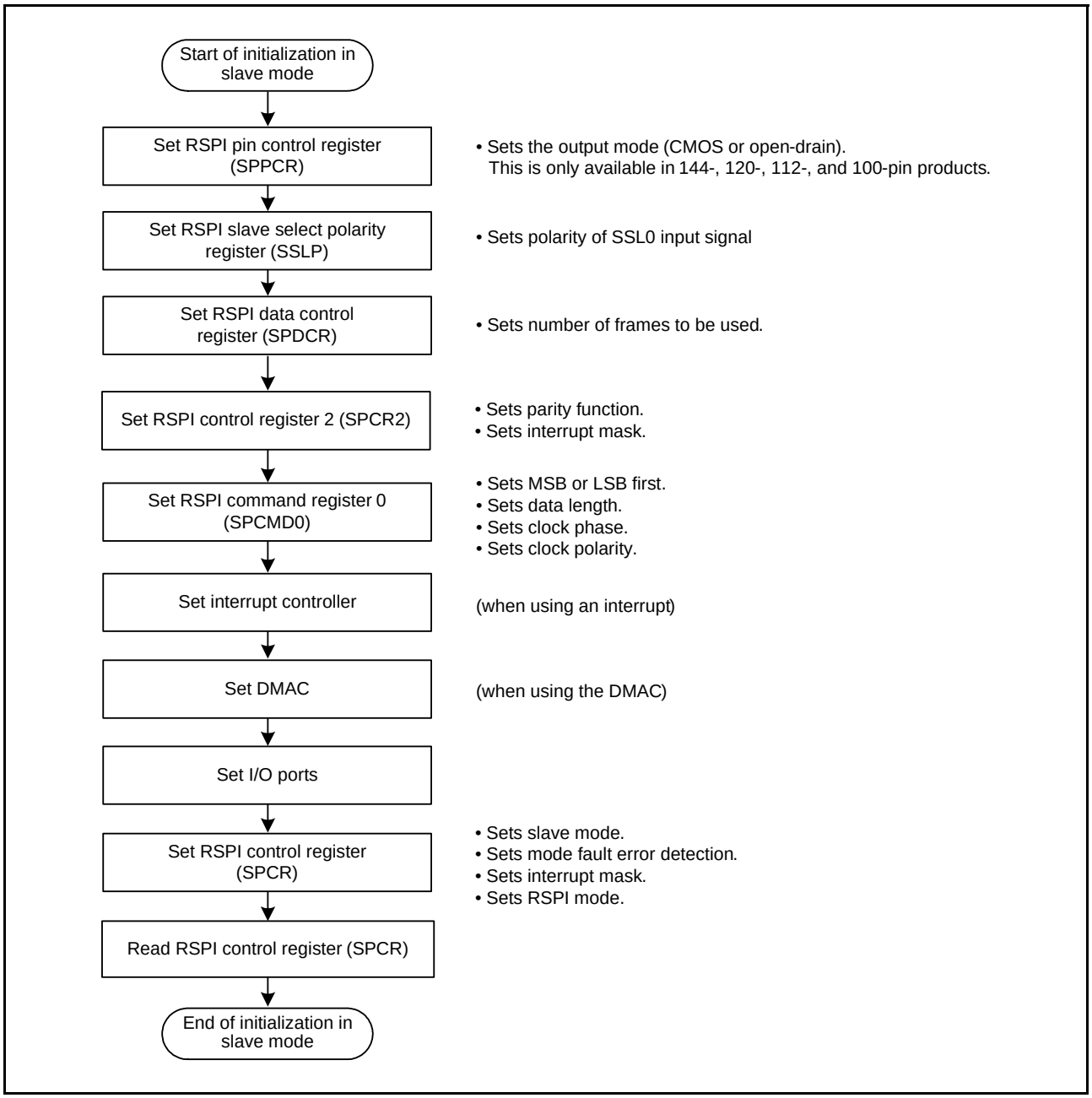


Figure 32.38 Example of Initialization Flowchart in Slave Mode (SPI Operation)

(6) Flow of Software Processing

Figure 32.39 to Figure 32.41 show examples of the flow of software processing.

(a) Flow of processing for transmission

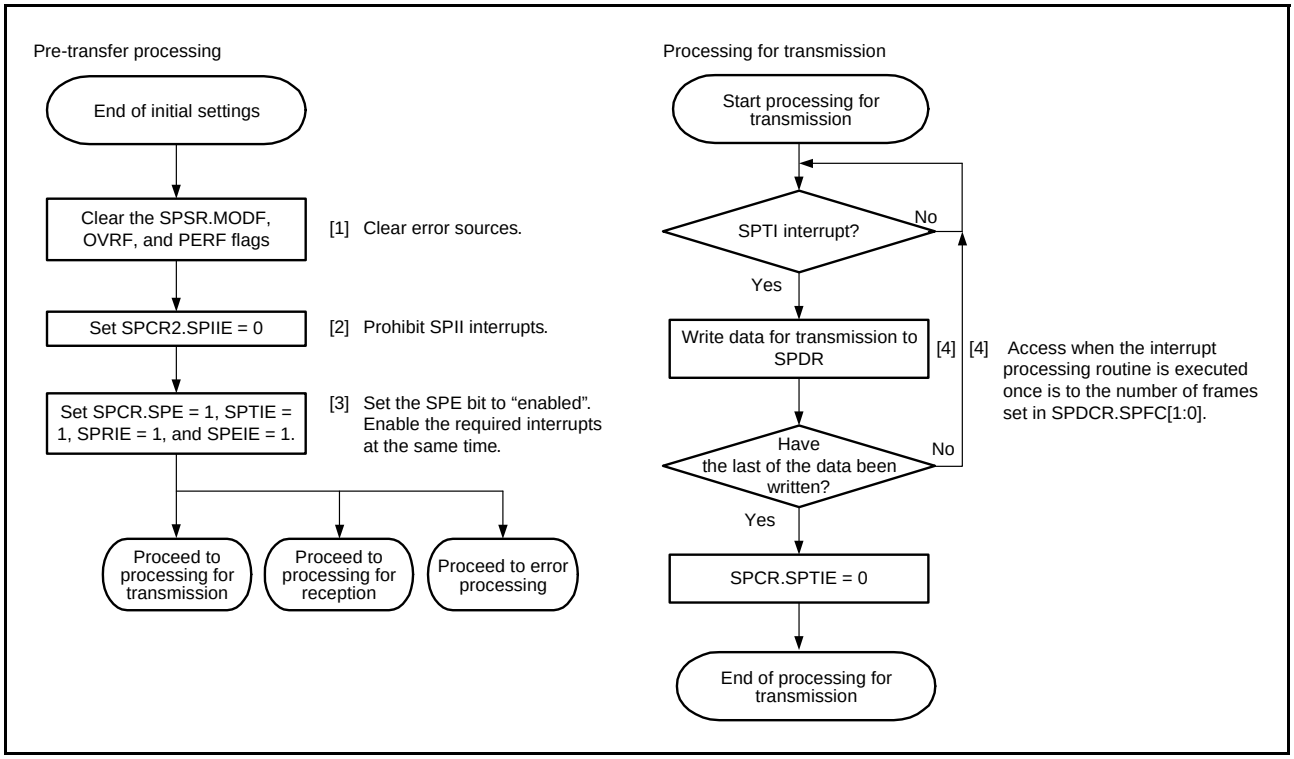


Figure 32.39 Flowchart for Slave Mode (Transmission)

(b) Flow of processing for reception

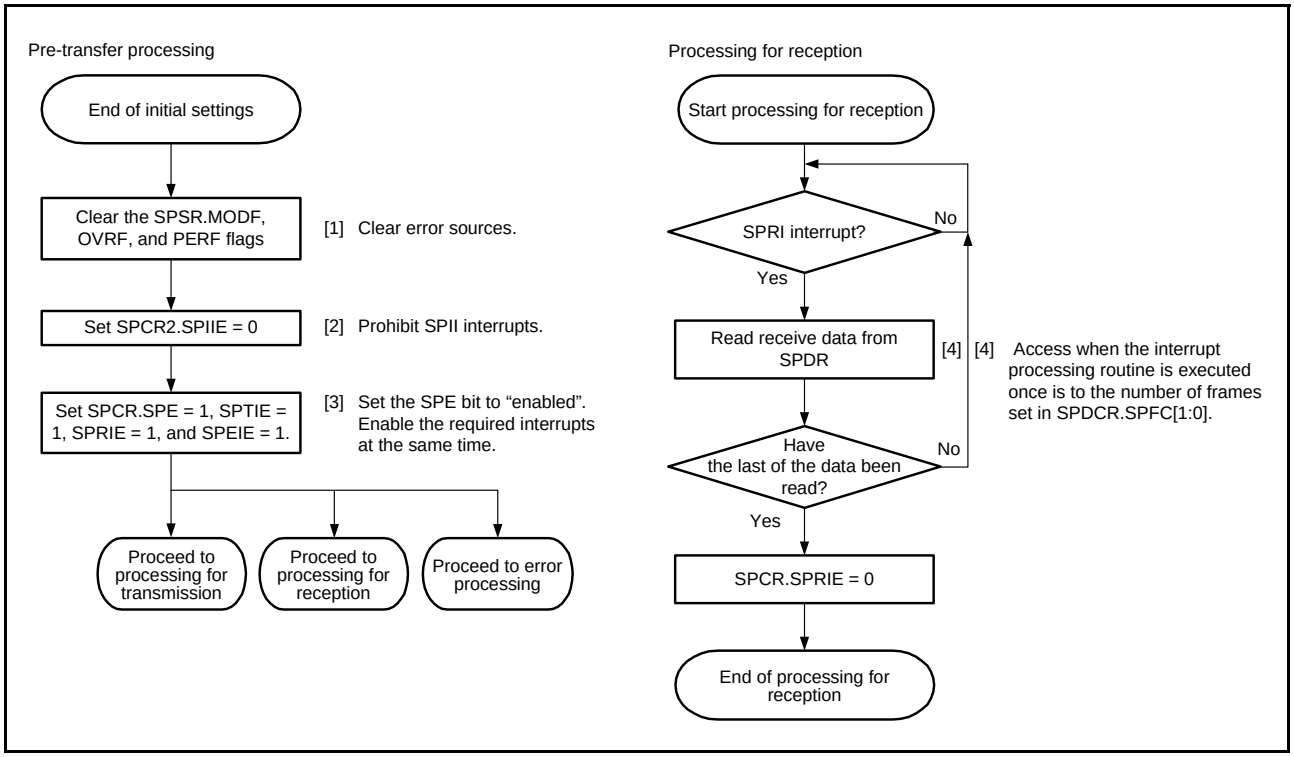


Figure 32.40 Flowchart for Slave Mode (Reception)

(c) Flow of error processing

In slave operation, even when a mode-fault error is generated, the SPSR.MODF flag can be cleared without de-asserting the pin. When an error occurs, clear the ICU.IRn.IR flag from within the error processing routine. If this is not done, the ICU.IRn.IR flag may continue to indicate the SPTI interrupt or SPRI interrupt request. If SPRI interrupt request is retained, read the receive buffer to initialize the RSPI internal sequencer.

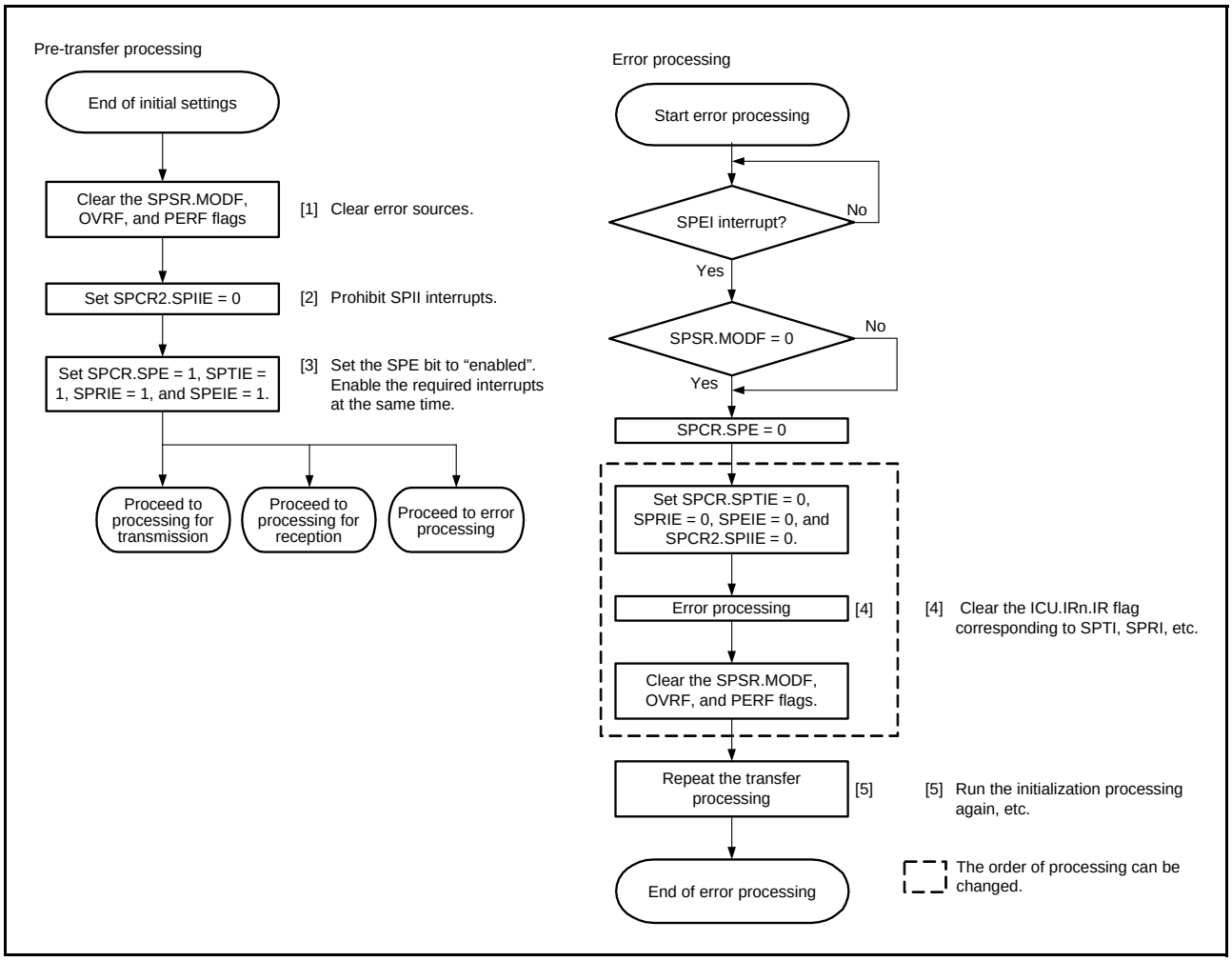


Figure 32.41 Flowchart for Slave Mode (Error Processing)

32.3.11 Clock Synchronous Operation

Setting the SPMS bit in the RSPI control register (SPCR) to 1 selects clock synchronous operation of the RSPI. In clock synchronous operation, the SSLni pin is not used, and the three pins of RSPCKn, MOSIn, and MISOn handle communications. The SSLni pin is available as I/O port pins.
Although clock synchronous operation does not require use of the SSLni pin, operation of the module is the same as in SPI operation. That is, in both master and slave operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected because the SSLni pin is not used.
Furthermore, in clock synchronous operation, do not execute an operation when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

32.3.12 Master Mode Operation

(1) Starting a Serial Transfer

The RSPI updates the data in the transmit buffer (SPTX) of SPDR when data is written to the RSPI data register (SPDR) with the transmit buffer being empty (data for the next transfer is not set). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR, the RSPI copies data from the transmission buffer to the shift register and starts serial transmission. Upon copying transmit data to the shift register, the RSPI changes the status of the shift register to “full”, and upon termination of serial transfer, it changes the status of the shift register to “empty”. The status of the shift register cannot be referenced.
For details on the RSPI transfer format, see section 32.3.5, Transfer Format.

(2) Terminating a Serial Transfer

The RSPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the sampling timing. If free space is available in the receive buffer, upon termination of serial transfer, the RSPI copies data from the shift register to the receive buffer of the RSPI data register (SPDR).
It should be noted that the final sampling timing varies depending on the bit length of transfer data. In master mode, the RSPI data length depends on the SPCMDm.SPB[3:0] bit setting.
For details on the RSPI transfer format, see section 32.3.5, Transfer Format.
However, transfer in clock-synchronous operation is conducted without the SSLn0 output signal.

(3) Sequence Control

The transfer format employed in master mode is determined by SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.
SPSCR is a register used to determine the sequence configuration for serial transfers that are executed by the RSPI in master mode. The following items are set in SPCMDm register: SSLni output signal value, MSB/LSB first, data length, some of the bit rate settings, RSPCKn polarity/phase, whether SPCKD is to be referenced, whether SSLND is to be referenced, and whether SPND is to be referenced. SPBR holds some of the bit rate settings; SPCKD, an RSPI clock delay value; SSLND, an SSL negation delay; and SPND, a next-access delay value.
According to the sequence length that is assigned to SPSCR, the RSPI makes up a sequence comprised of a part or all of SPCMDm register. The RSPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPE bit in the RSPI control register (SPCR) is set to 1 and the RSPI function is enabled, the RSPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer.
The RSPI increments the pointer each time the next-access delay period for a data transfer ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, the RSPI sets the pointer in SPCMD0 register, and in this manner the sequence is executed repeatedly.

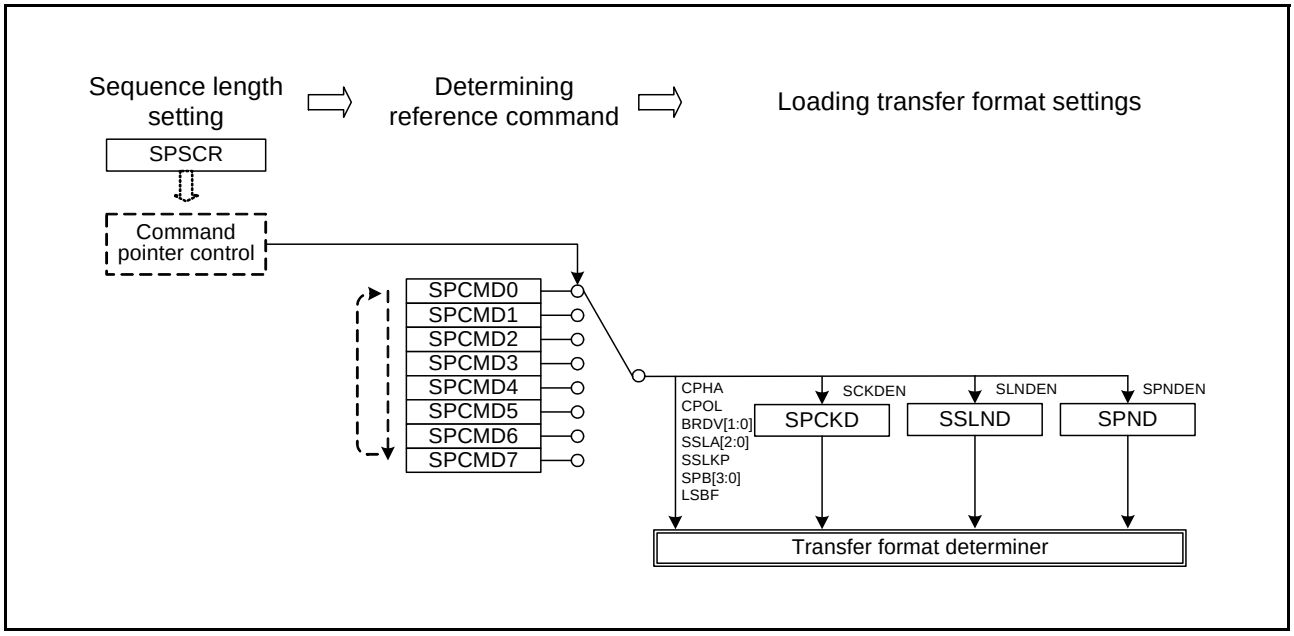


Figure 32.42 Procedure for Determining the Form of Serial Transmission in Master Mode

In this section, a frame is the combination of the data (SPDR) and the settings (SPCMDm).

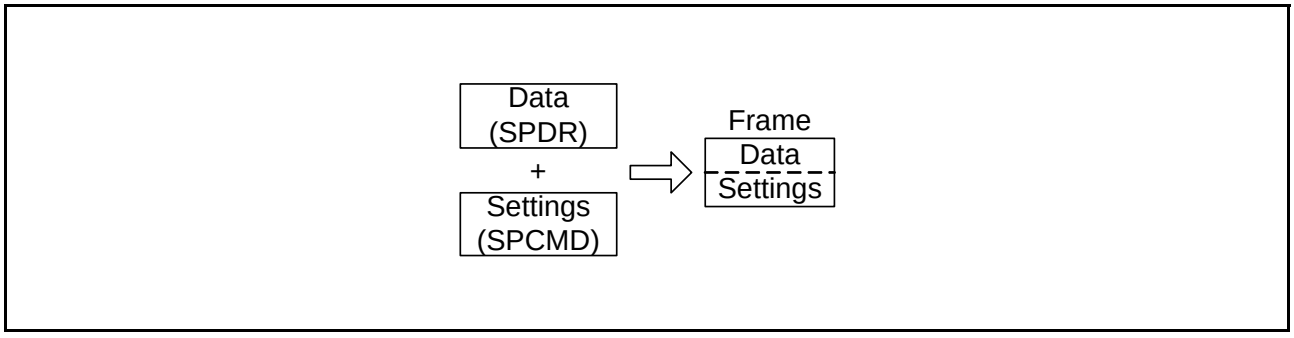


Figure 32.43 Concept of a Frame

Figure 32.44 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 32.4.

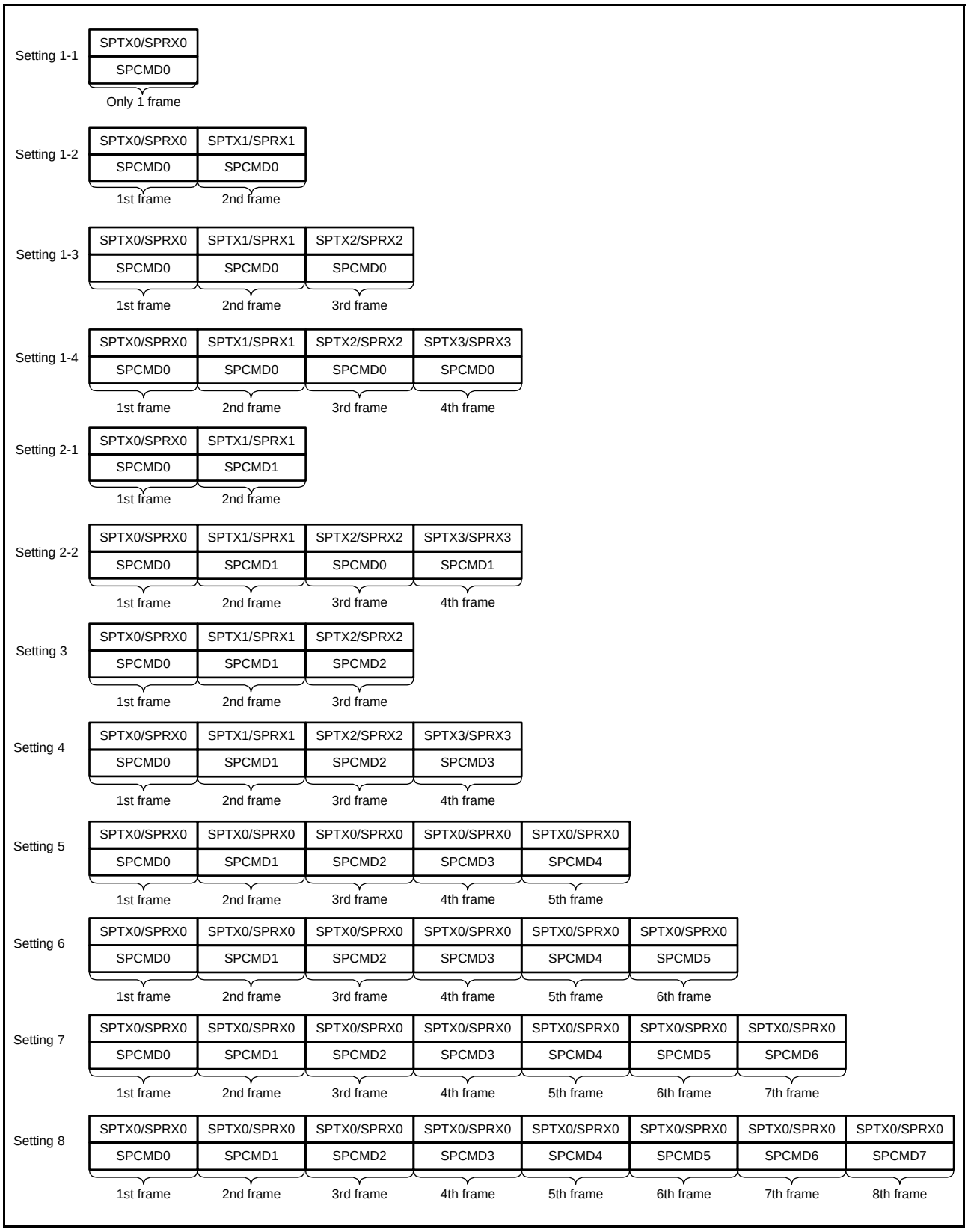


Figure 32.44 Correspondence between the RSPI Command Register and Transmit/Receive Buffers in Sequence Operations

(4) Initialization Flowchart

Figure 32.45 is a flowchart illustrating an example of initialization in clock synchronous operation when the RSPI is used in master mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, see the descriptions given in the individual blocks.

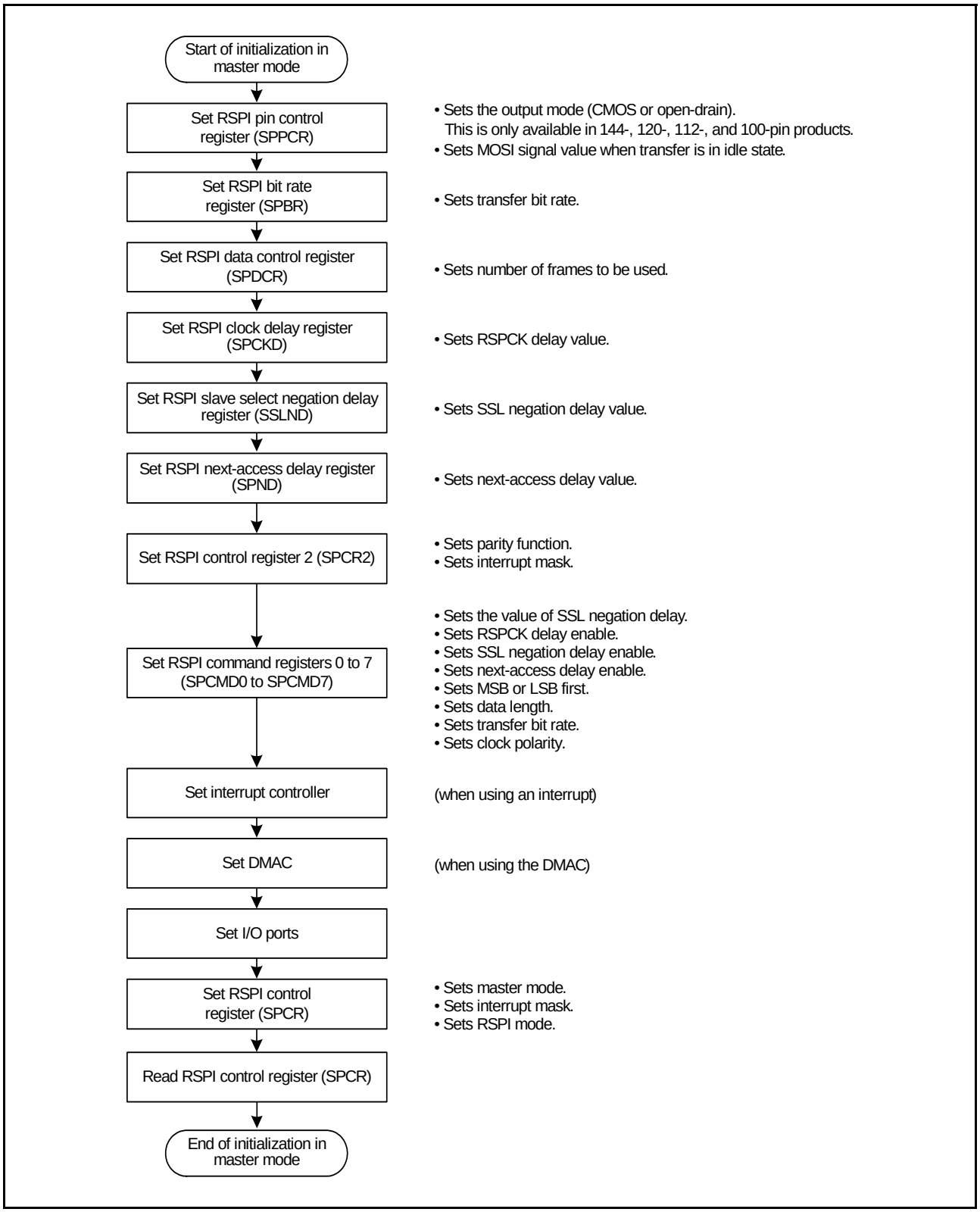


Figure 32.45 Example of Initialization Flowchart in Master Mode (Clock Synchronous Operation)

(5) Flow of Software Processing

Software processing during clock-synchronous master operation is the same as that for SPI master operation. For details, see 32.3.10.1, (9) Software Processing Flow. Note that mode-fault errors will not occur.

32.3.13 Slave Mode Operation

(1) Starting a Serial Transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the RSPI. When detecting the start of a serial transfer in a condition in which the shift register is empty, the RSPI changes the status of the shift register to “full”, so that data cannot be copied from the transmit buffer to the shift register when serial transfer is in progress. If the shift register was full before the serial transfer started, the RSPI keeps the status of the shift register unchanged, in the full state. When the SPMS bit is 1, the RSPI always drives the MISOn output signal.
For details on the RSPI transfer format, see section 32.3.5, Transfer Format. It should be noted that the SSL0 input signal is not used in clock synchronous operation.

(2) Terminating a Serial Transfer

The RSPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer, upon termination of serial transfer the RSPI copies received data from the shift register to the receive buffer of the RSPI data register (SPDR).
Upon termination of a serial transfer the RSPI changes the status of the shift register to “empty”. The final sampling timing changes depending on the bit length of transfer data. In slave mode, the RSPI data length depends on the SPCMD0.SPB[3:0] bit setting. For details on the RSPI transfer format, see section 32.3.5, Transfer Format.

(3) Initialization Flowchart

Figure 32.46 is a flowchart illustrating an example of initialization in clock synchronous operation when the RSPI is used in slave mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, see the descriptions given in the individual blocks.

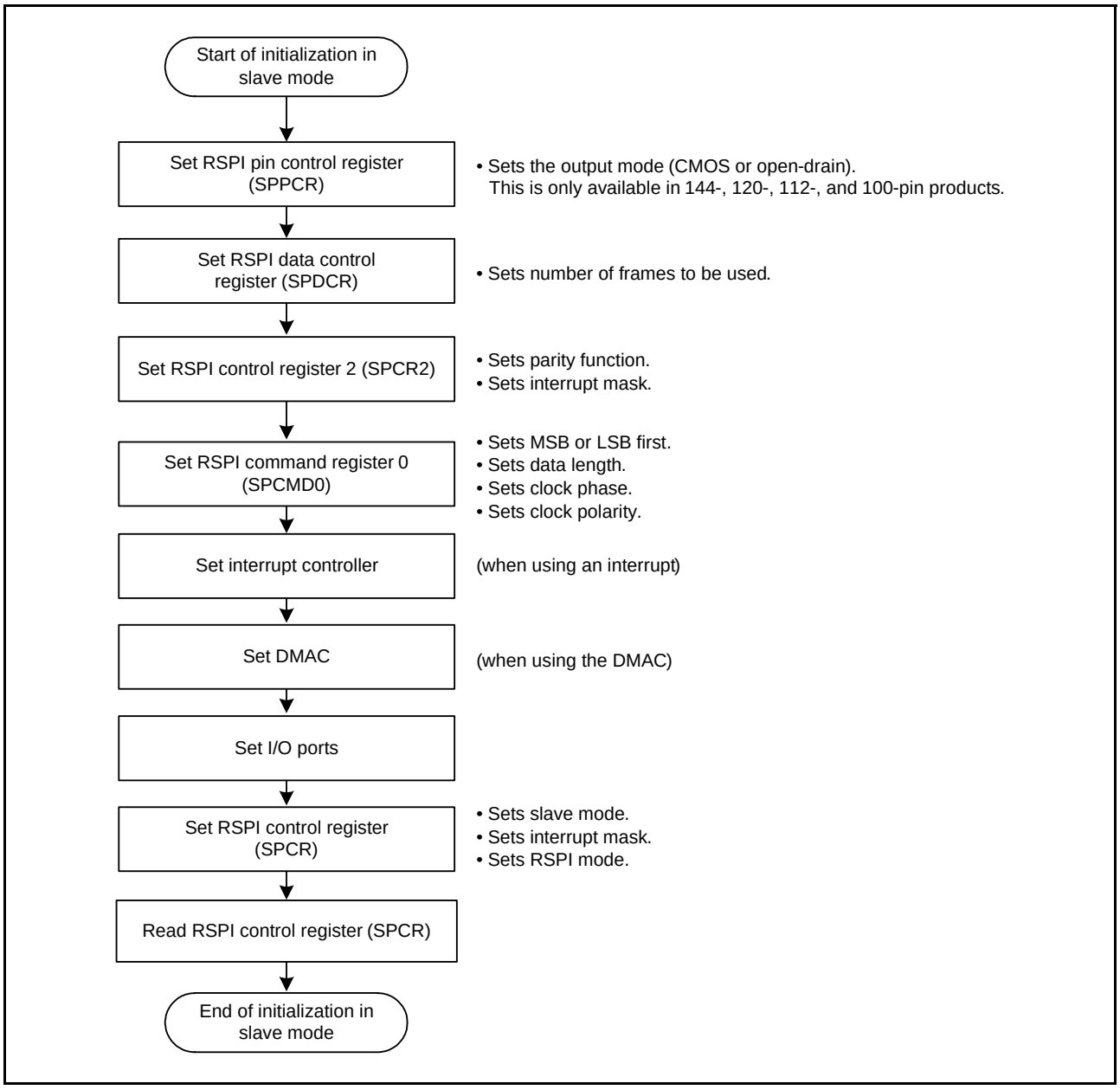


Figure 32.46 Example of Initialization Flowchart in Slave Mode (Clock Synchronous Operation)

(4) Flow of Software Processing

Software processing during clock-synchronous slave operation is the same as that for SPI slave operation. For details, see 32.3.10.2, (6) Flow of Software Processing. Note that mode-fault errors will not occur.

32.3.14 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the RSPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path of the shift register. The RSPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, and between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the RSPI or the reversed transmit data becomes the received data for the RSPI.
Table 32.12 lists the relationship among the SPLP2 and SPLP bits and the received data. Figure 32.47 shows the configuration of the shift register I/O paths for the case where the RSPI in master mode is set in loopback mode (SPPCR.SPLP2 = 0, SPPCR.SPLP = 1).

Table 32.12 SPLP2 and SPLP Bit Settings and Received Data

SPPCR.SPLP2 Bit	SPPCR.SPLP Bit	Received Data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Reversed transmit data
1	0	Transmit data
1	1	Transmit data

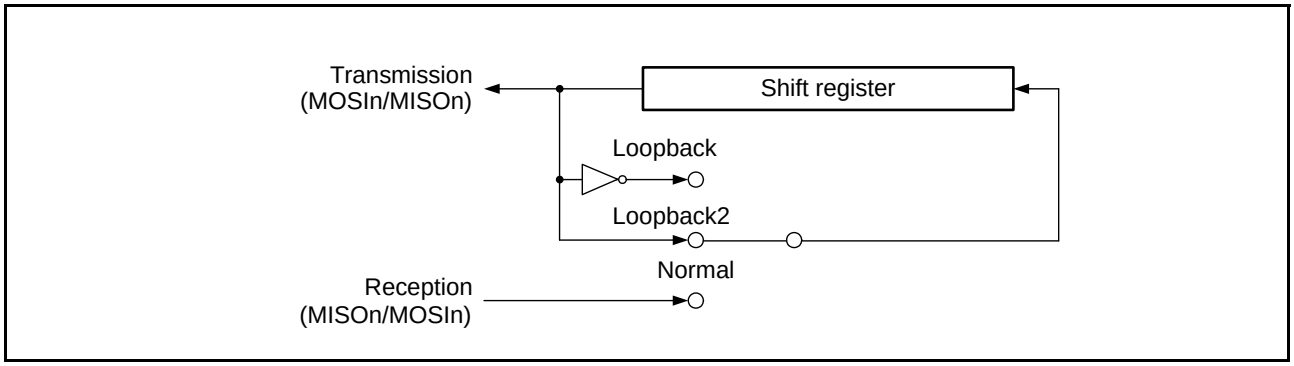


Figure 32.47 Configuration of Shift Register I/O Paths in Loopback Mode (Master Mode)

32.3.15 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. In order to detect defects in the parity bit adding unit and error detecting unit of the parity circuit, self-diagnosis is executed for the parity circuit following the flowchart shown in Figure 32.48.

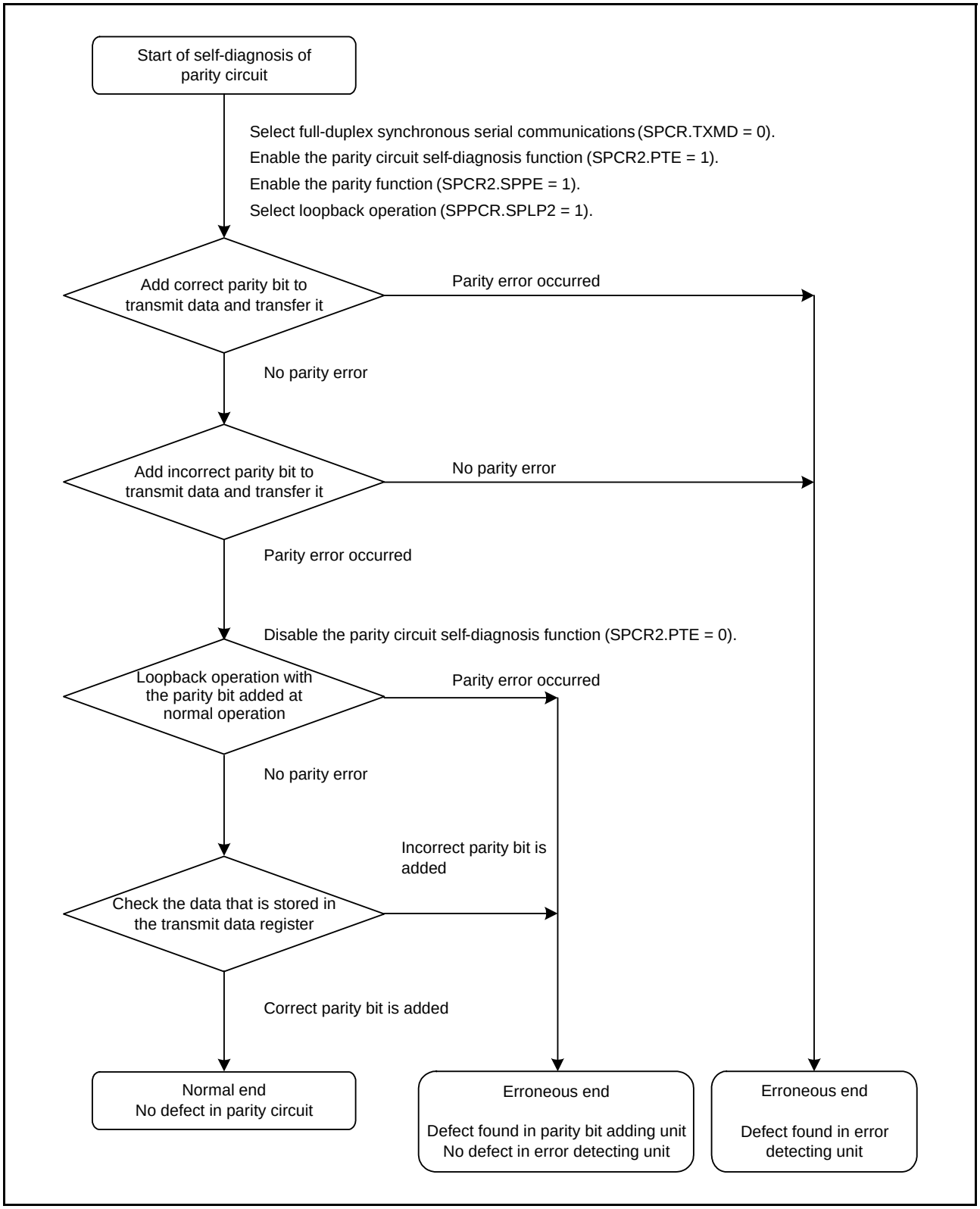


Figure 32.48 Flowchart for Self-Diagnosis of Parity Circuit

32.3.16 Interrupt Sources

The RSPI has interrupt sources of receive buffer full, transmit buffer empty, mode fault, overrun, parity error, and RSPI idle. In addition, the DTC or DMAC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Since the vector address for SPEI is allocated to interrupt requests due to mode-fault, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the RSPI are listed in Table 32.13. An interrupt is generated on satisfaction of an interrupt condition in Table 32.13. Clear the receive buffer full and transmit buffer empty sources through data transfer.

When using the DTC or DMAC to perform data transmission/reception, the DTC or DMAC must be set up first to be in a status in which transfer is enabled before making the RSPI settings. For the method for setting the DTC or DMAC, refer to section 18, DMA Controller (DMACA), or section 19, Data Transfer Controller (DTCa).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt are generated while the ICU.IRn.IR flag is 1, the interrupt is not output as a request for ICU but is retained internally (the capacity for retention is one request per source). A retained interrupt request to ICU is output when the ICU.IRn.IR flag becomes 0. A retained interrupt request is automatically discarded once it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally retained interrupt request can also be cleared to 0.

Table 32.13 Interrupt Sources of RSPI

Interrupt Source	Symbol	Interrupt Condition	DMAC/DTC Activation
Receive buffer full	SPRI	The receive buffer becomes full while the SPCR.SPRIE bit is 1.	Possible
Transmit buffer empty	SPTI	The transmit buffer becomes empty while the SPCR.SPTIE bit is 1.	Possible
RSPI errors (mode fault, overrun, and parity error)	SPEI	The SPSR.MODF, OVRF, or PERF flag is set to 1 while the SPCR.SPEIE bit is 1.	Impossible
RSPI idle	SPII	The SPSR.IDLNF flag is set to 0 while the SPCR2.SPIIE bit is 1.	Impossible

32.4 Usage Note

32.4.1 Setting Module-Stop Function

Module stop control register B (MSTPCRB) and module stop control register C (MSTPCRC) can used to enable or disable operation of the RSPI. The RSPI is stopped at the initial value. The registers become accessible on release from the module-stop state. For details, refer to section 12, Low Power Consumption.

32.4.2 Cautionary Note on the Low Power Consumption Functions

When a low power consumption function is to be used to lower power consumption by the RSPI, use the low power consumption function after the SPCR.SPE bit is set to 0 and transfer ends.

32.4.3 Points to Note on Starting Transfer

If the ICU.IRn.IR flag is 1 at the time transfer is to be started, an interrupt request is internally retained after transfer starts, and this can lead to unanticipated behavior of the ICU.IRn.IR flag.
When the ICU.IRn.IR flag is 1 at the time transfer is to start, follow the procedure below to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1).

1. Confirm that transfer has stopped (i.e. that the SPCR.SPE bit is 0).
2. Clear the relevant interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) to 0.
3. Read the relevant interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) and confirm that its value is 0.
4. Clear the ICU.IRn.IR flag to 0.

33.CRC Calculator (CRC)

The CRC (Cyclic Redundancy Check) calculator generates CRC codes.

33.1 Overview

Table 33.1 lists the specifications of the CRC calculator, and Figure 33.1 shows a block diagram of the CRC calculator.

Table 33.1 Specifications of CRC

Item	Description
Data for CRC calculation*1	CRC code generated for any desired data in 8n-bit units (where n is a whole number)
Data block size	8 bits
CRC processor unit	Operation executed on eight bits in parallel
CRC generating polynomial	One of three generating polynomials selectable • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$
CRC calculation switching	CRC code generation for LSB-first or MSB-first communication selectable
Low-power consumption function	Module-stop state can be set

Note 1. The circuit does not have functionality to divide data for calculation into a data-block size. Write data in 8-bit units.

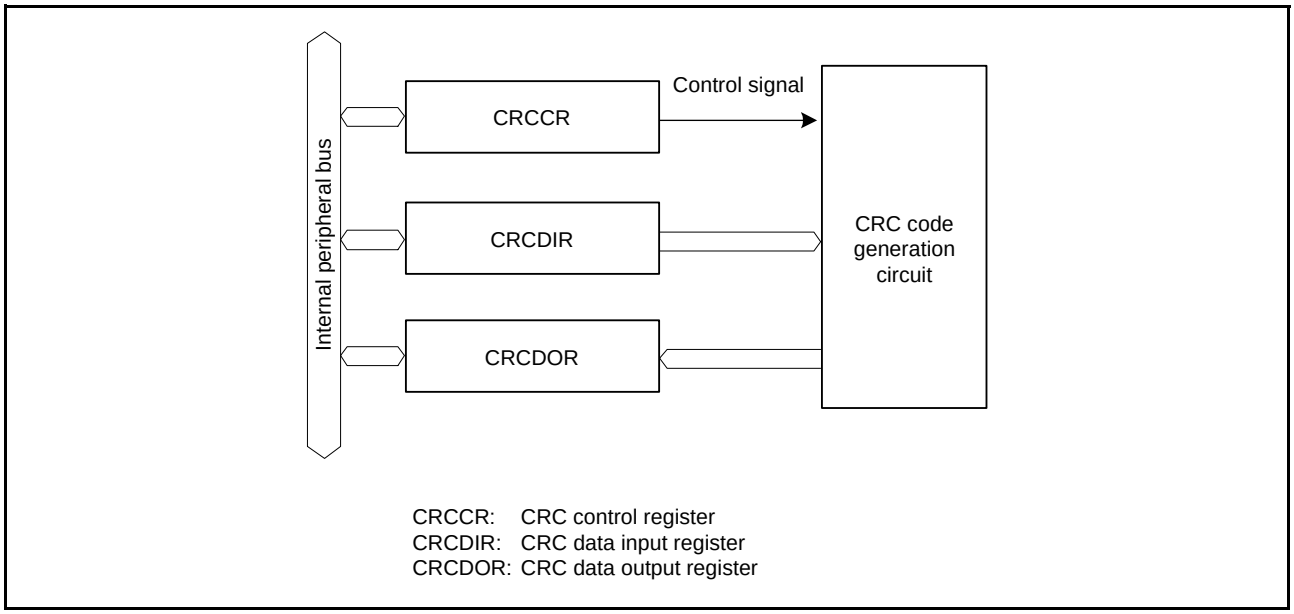


Figure 33.1 Block Diagram of CRC Calculator

33.2 Register Descriptions

33.2.1 CRC Control Register (CRCCR)

Address(es): 0008 8280h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	—	—	—	—	LMS	GPS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	GPS[1:0]	CRC Generating Polynomial Switching	b1 b0 0 0: No calculation is executed. 0 1: $X^8 + X^2 + X + 1$ 1 0: $X^{16} + X^{15} + X^2 + 1$ 1 1: $X^{16} + X^{12} + X^5 + 1$	R/W
b2	LMS	CRC Calculation Switching	0: Generate CRC for LSB first communication. 1: Generate CRC for MSB first communication.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DORCLR	CRCDOR Register Clear	1: Clear the CRCDOR register*1 This bit is read as 0.	W

Note 1. Only 1 can be written.

DORCLR Bit (CRCDOR Register Clear)

Write 1 to this bit so that the CRCDOR register is cleared to 0000h.
This bit is read as 0. Only 1 can be written.

LMS Bit (CRC Calculation Switching)

This bit selects the bit order for the 16-bit CRC code generated.
Transmit data from the lower-order bytes of the CRC code (b7 to b0) for LSB first communication and transmit data from the higher-order bytes of the CRC code (b15 to b8) for MSB first communication.
For transmission and reception of the CRC code, see section 33.3, Operation.

33.2.2 CRC Data Input Register (CRCDIR)

Address(es): 0008 8281h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

CRCDIR is a readable/writable register, to which the bytes to be CRC-operated are written.

33.2.3 CRC Data Output Register (CRCDOR)

Address(es): 0008 8282h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDOR is a readable/writable register. The initial value is 0000h.
For operation using the value other than the initial value, rewrite CRCDOR.
When data is written to CRCDIR, the operation result is stored in CRCDOR. The communication data is verified when the following CRC code calculation result is 0000h.
When an 8-bit CRC ($X^8 + X^2 + X + 1$ polynomial) is in use, the valid CRC code is obtained in the lower-order byte (b7 to b0). The higher-order byte (b15 to b8) is not updated.

33.3 Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfer.
The following figures show examples in which the CRCCR.GPS[1:0] bits are set to 11b so the CRC code is calculated by using a 16-bit CRC (with the polynomial $X^{16} + X^{12} + X^5 + 1$), and the CRC code is calculated for the value “F0h”.
When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in the lower-order byte of CRCDOR.

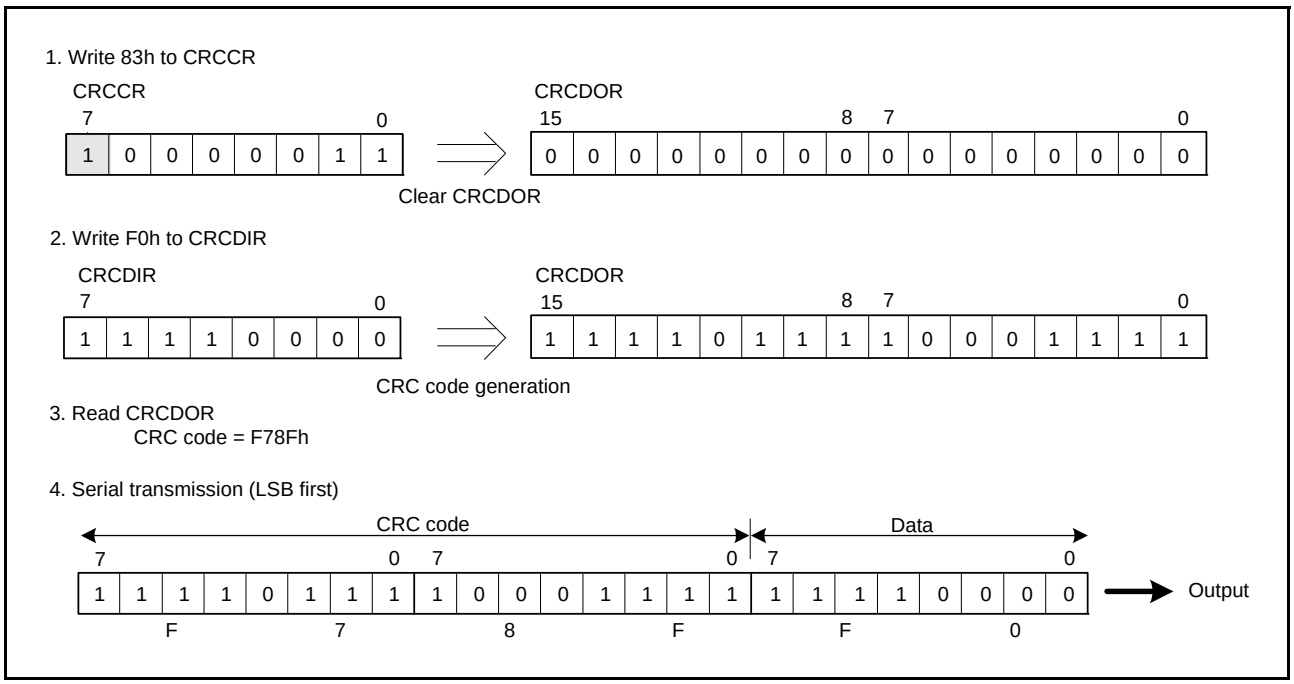


Figure 33.2 LSB-First Data Transmission

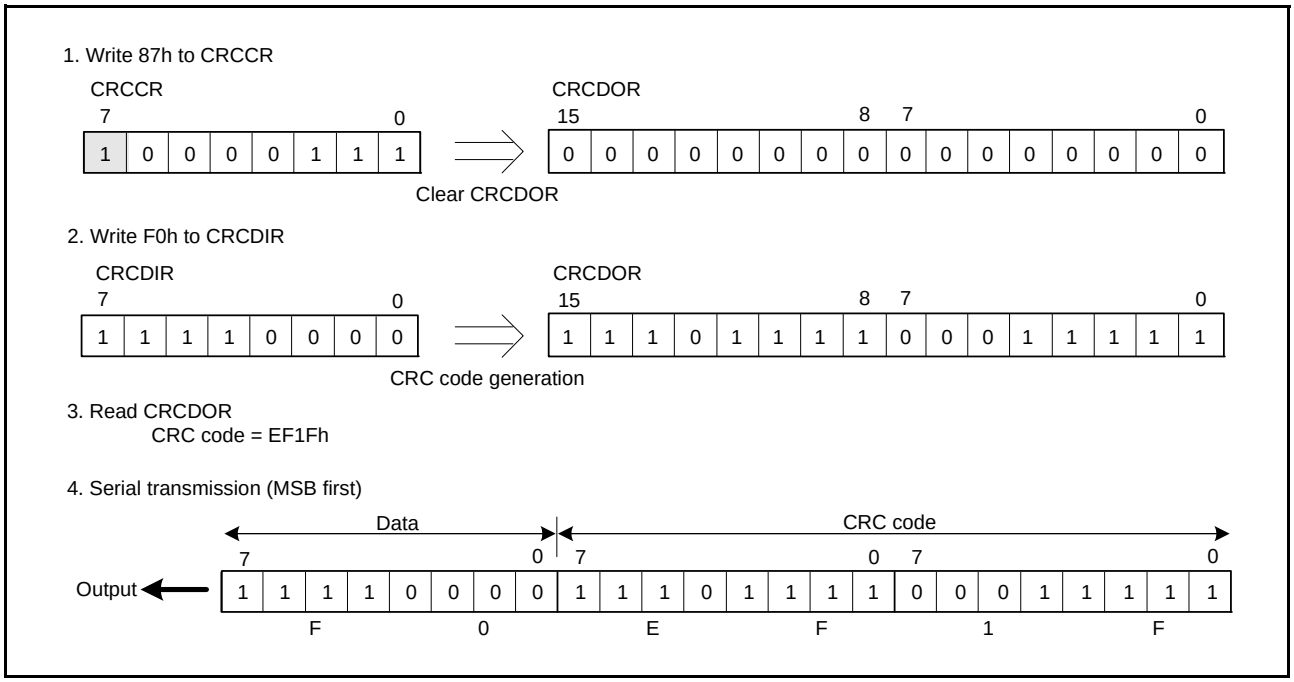


Figure 33.3 MSB-First Data Transmission

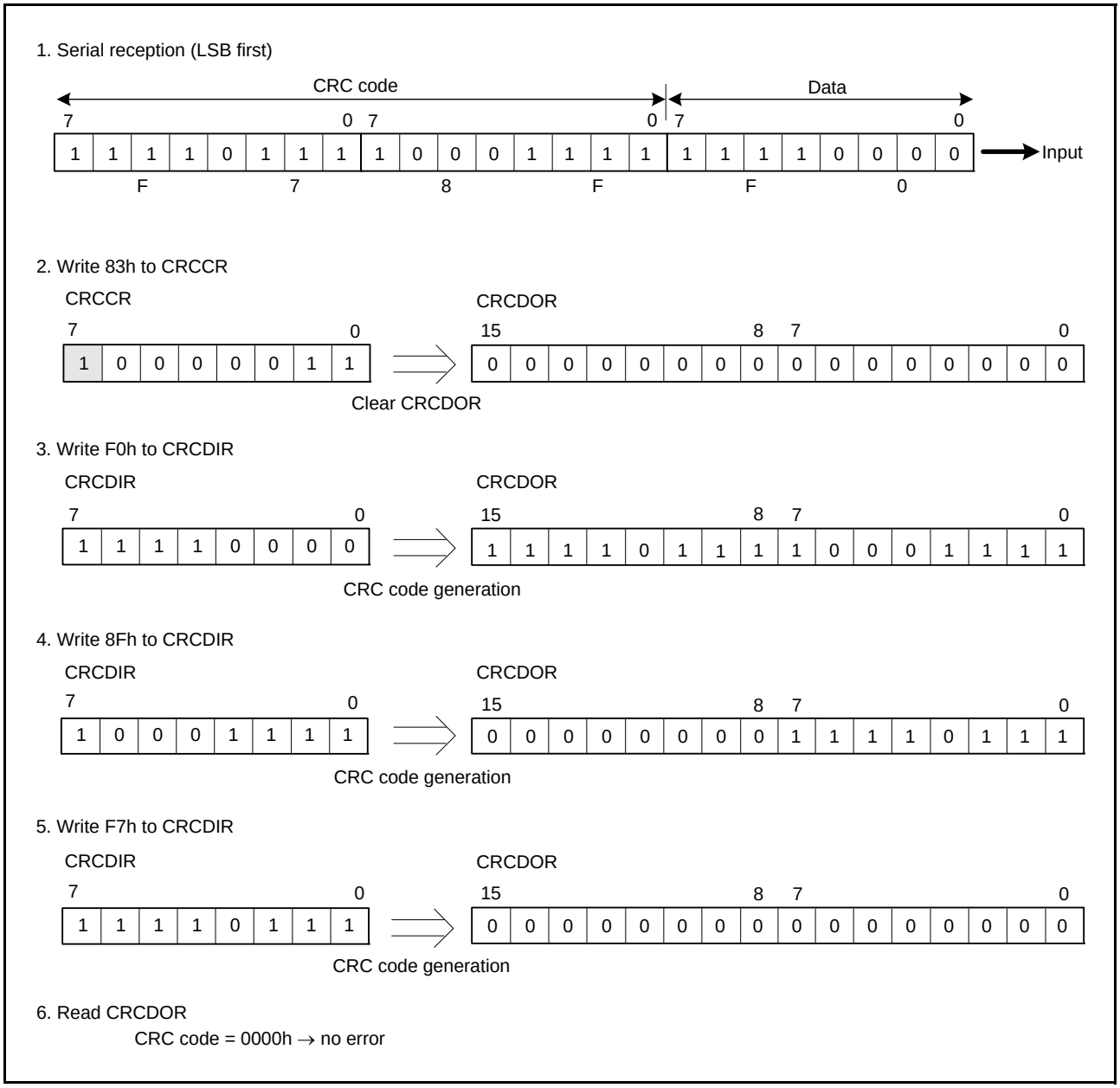


Figure 33.4 LSB-First Data Reception

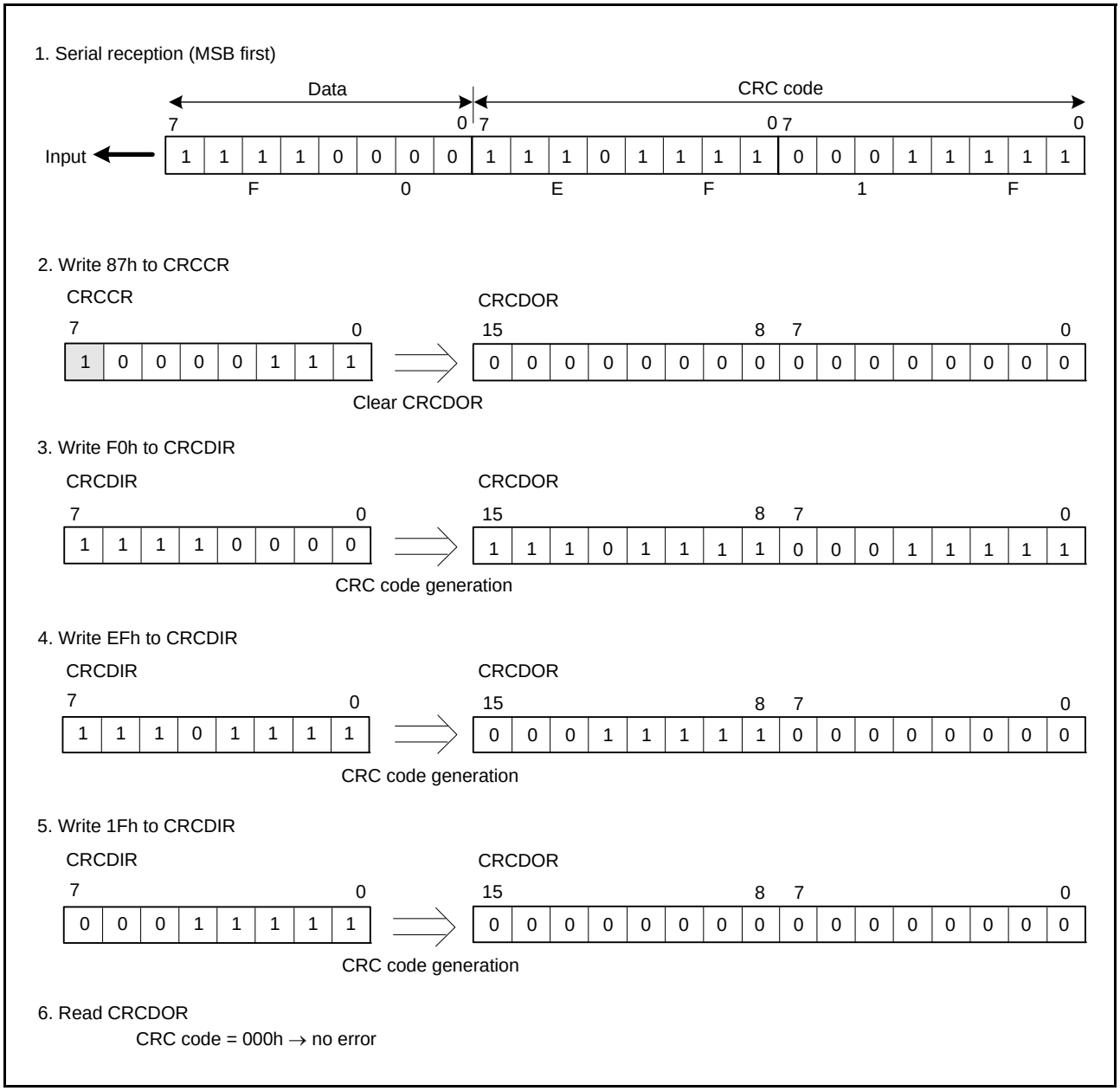


Figure 33.5 MSB-First Data Reception

33.4 Usage Notes

33.4.1 Module-Stop Function Setting

Operation of the CRC calculator can be disabled or enabled using the module stop control register B (MSTPCRB). The CRC calculator is stopped at the initial value. Register access is enabled by clearing the module-stop state. For details, see section 12, Low Power Consumption.

33.5 Note on Transmission

Note that the sequence of transmission for the CRC code differs according to whether transmission is LSB-first or MSB-first.

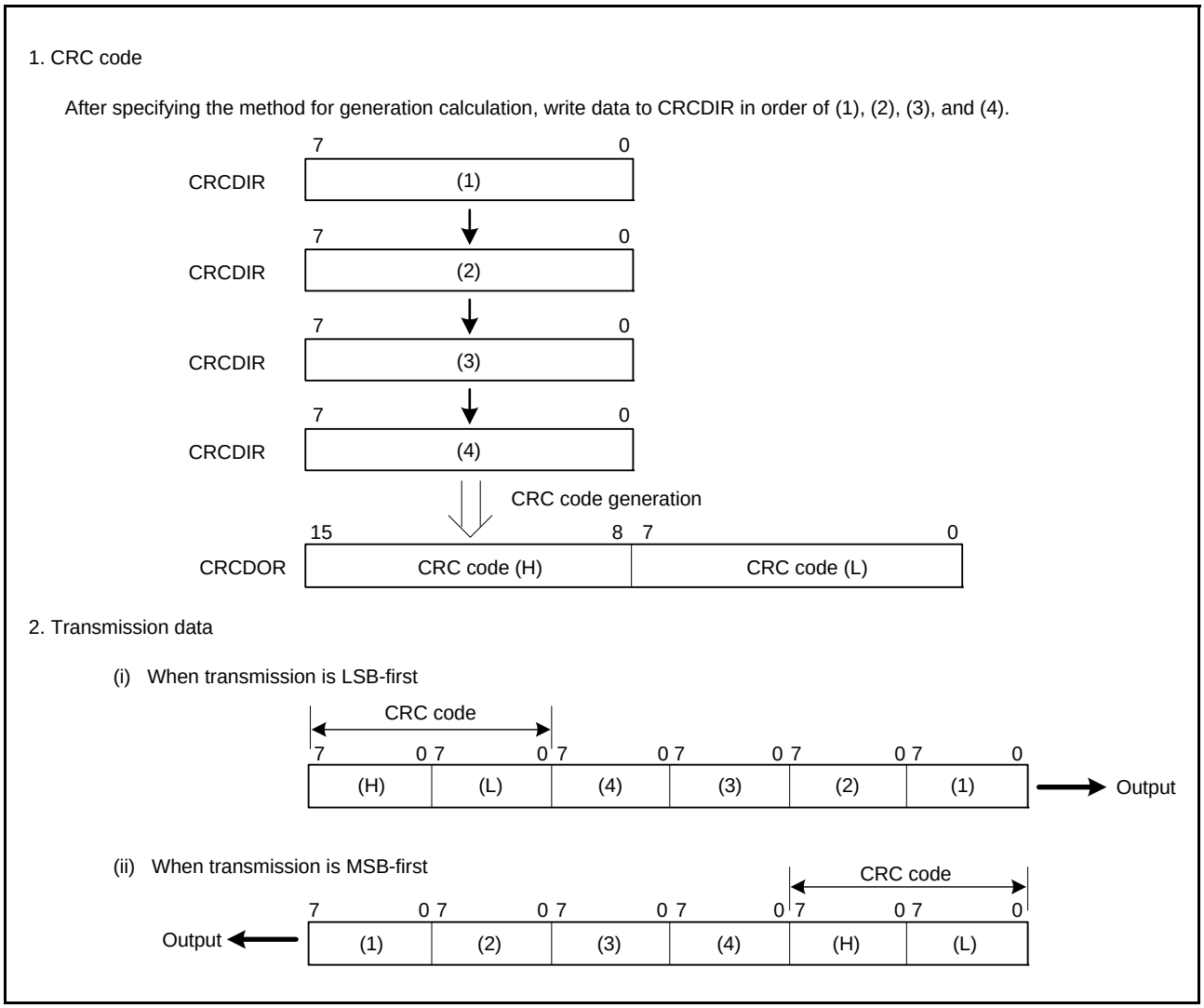


Figure 33.6 LSB-First and MSB-First Data Transmission

34. 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions]

34.1 Overview

Products of this MCU Group incorpoate two units of 12-bit successive approximation A/D converter. Up to four analog input channels are selectable for each unit.

The 12-bit A/D converter converts a maximum of four selected channels of analog inputs into a 12-bit digital value through successive approximation.

The A/D converter has three operating modes: single-cycle scan mode in which the analog inputs of up to four arbitrarily selected channels are converted for only once in ascending channel order; and continuous scan mode in which the analog inputs of up to four arbitrarily selected channels are continuously converted in ascending channel order; and group scan mode in which up to four channels of the analog inputs are arbitrarily divided into two groups (group A and group B) and converted in ascending channel order in each group.

In group scan mode, the scan start conditions of group A and group B can be independently selected, thus allowing A/D conversion of group A and group B to be started independently.When group A priority control is selected, along with operation as described above, if a request to start scanning for group A is received during A/D conversion operations for group B, conversion operations for group B are discontinued and conversion for group A starts, i.e. is given priority.

In double trigger mode, one arbitrarily selected analog input channel is converted in single-cycle scan mode or group scan mode (group A), and the resulting data of A/D conversion started by the first and second triggers are stored into separate registers (duplication of A/D conversion data).

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages internally generated in the 12-bit A/D converter is converted.

Table 34.1 lists the specifications of the 12-bit A/D converter and Table 34.2 indicates the functions of the 12-bit A/D converter. Figure 34.1 shows a block diagram of the 12-bit A/D converter.

Table 34.1 Specifications of 12-Bit A/D Converter (1/2)

Item	Specifications
Number of units	Two units (S12ADB0/S12ADB1)
Input channels	Eight channels (four channels × two units)
A/D conversion method	Successive approximation method
Resolution	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock ADCLK = 50 MHz)
A/D conversion clock	Peripheral module clock PCLKB*1 and A/D conversion clock ADCLK*1 can be set so that the frequency division ratio should be one of the following. PCLKB to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8 ADCLK is set using the clock generation circuit (CPG).
Data registers	• Eight registers for analog input, one for A/D-converted data duplication in double-trigger mode, and two for A/D-converted data duplication during extended operation in double-trigger mode. • The results of A/D conversion are stored in 12-bit A/D data registers. • 8, 10, and 12-bit accuracy output for the results of A/D conversion (selectable between 2 and 4-bit right shifts for output of conversion results). • An accumulation of A/D conversion results is stored as a 14-bit value in A/D data registers in cumulative mode. • Double trigger mode (selectable in single cycle scan and group scan modes). The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers). A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Table 34.1 Specifications of 12-Bit A/D Converter (2/2)

Item	Specifications
Operating modes	• Single-cycle scan mode: A/D conversion is performed for only once on the analog inputs of up to four arbitrarily selected channels. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to four arbitrarily selected channels. • Group scan mode: Up to four channels of analog inputs are divided into group A and group B and A/D conversion is performed only once on all the selected channels on a group basis. The scan start conditions of group A and group B can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. After the A/D conversion on group A is completed, the A/D conversion on group B is restarted (rescan).
Conditions of A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU3) or the general-purpose PWM timer (GPT). • Asynchronous trigger A/D conversion can be triggered by the external trigger pin ADTRGn#.
Function	• Sample-and-hold function • Channel-dedicated sample-and-hold function (three channels/unit) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode • Discharge function • Double trigger mode (duplication of A/D conversion data) • Input signal amplification function provided through programmable gain amplifier (three channels per unit) • Window-comparator function (three channels/unit) • Input signal amplification using a programmable gain amplifier (three channels per unit)
Interrupt source	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt (S12ADI) request can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt (S12ADI, S12ADI1) request can be generated on completion of double scan. • In group scan mode, A/D scan end interrupt (S12ADI, S12ADI1) request can be generated on completion of group A scan, whereas A/D scan end interrupt specially for group B (S12GBADI, S12GBADI1) request can be generated on completion of group B scan. • In group scan mode with double trigger mode, A/D scan end interrupt (S12ADI, S12ADI1) request can be generated on completion of double scan of group A, whereas A/D scan end interrupt specially for group B (S12GBADI, S12GBADI1) request can be generated on completion of group B scan. • An interrupt request (CMP0 to CMP2, CMP4 to CMP6) is generated (and can be used as a POE source) in response to detection by the comparator. • The S12ADI, S12GBADI, S12ADI1, S12GBADI1 and CMP0 to CMP2, CMP4 to CMP6 interrupts are capable of activating the DMA controller (DMAC) or the data-transfer controller (DTC).
Low power consumption function	• Module stop state can be specified.*2

Note 1. Peripheral module clock PCLKB is set according to the setting of the SCKCR.PCKB[3:0] bits and A/D conversion clock ADCLK is set according to the setting of the SCKCR.PCKB[3:0] bits.

Note 2. For details, refer to section 12, Low Power Consumption.

Table 34.2 Functions of 12-Bit A/D Converter (1/2)

Item			Function	
			Unit 0 (S12AD)	Unit 1 (S12AD1)
Analog input channel			AN000 to AN003	AN100 to AN103
A/D conversion start conditions	Software	Software trigger	Enabled	Enabled
	External trigger	Trigger input pin	ADTRG0#	ADTRG1#
	Triggers from MTU3	Input capture to or compare match with MTU0.TGRA	TRGA0N	TRGA0N
		Input capture to or compare match with MTU1.TGRA	TRGA1N	TRGA1N
		Input capture to or compare match with MTU2.TGRA	TRGA2N	TRGA2N
		Input capture to or compare match with MTU3.TGRA	TRGA3N	TRGA3N
		Input capture to or compare match with MTU4.TGRA or, in complementary PWM mode, an underflow of MTU4.TCNT (in the trough)	TRGA4N	TRGA4N
		Input capture to or compare match with MTU0.TGRA	TRGA6N	TRGA6N
		Input capture to or compare match with MTU7.TGRA or, in complementary PWM mode, an underflow of MTU7.TCNT (in the trough)	TRGA7N	TRGA7N
		Compare match between MTU4.TADCORA and MTU4.TCNT	TRG0AN	TRG0AN
		Compare match between MTU4.TADCORB and MTU4.TCNT	TRG4AN	TRG4AN
		Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT	TRG4BN	TRG4BN
		Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	TRG4AN or TRG4BN	TRG4AN or TRG4BN
		Compare match between MTU7.TADCORA and MTU7.TCNT	TRG4ABN	TRG4ABN
		Compare match between MTU7.TADCORB and MTU7.TCNT	TRG7AN	TRG7AN
		Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT	TRG7BN	TRG7BN
		Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	TRG7AN or TRG7BN	TRG7AN or TRG7BN
		Compare match between MTU4.TADCORA and MTU4.TCNT	TRG7ABN	TRG7ABN
	Triggers from GPT	Compare match with GPT0.GTADTRA	GTADTRA0N	GTADTRA0N
		Compare match with GPT0.GTADTRB	GTADTRB0N	GTADTRB0N
		Compare match with GPT1.GTADTRA	GTADTRA1N	GTADTRA1N
		Compare match with GPT1.GTADTRB	GTADTRB1N	GTADTRB1N
		Compare match with GPT2.GTADTRA	GTADTRA2N	GTADTRA2N
		Compare match with GPT2.GTADTRB	GTADTRB2N	GTADTRB2N
		Compare match with GPT3.GTADTRA	GTADTRA3N	GTADTRA3N
		Compare match with GPT3.GTADTRB	GTADTRB3N	GTADTRB3N
		Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	GTADTRA0N or GTADTRB0N	GTADTRA0N or GTADTRB0N
		Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	GTADTRA1N or GTADTRB1N	GTADTRA1N or GTADTRB1N
		Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	GTADTRA2N or GTADTRB2N	GTADTRA2N or GTADTRB2N

Table 34.2 Functions of 12-Bit A/D Converter (2/2)

Item			Function	
			Unit 0 (S12AD)	Unit 1 (S12AD1)
A/D conversion start conditions	Triggers from GPT	Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	GTADTRA3N or GTADTRB3N	GTADTRA3N or GTADTRB3N
		Compare match with GPT4.GTADTRA	GTADTRA4N	GTADTRA4N
		Compare match with GPT4.GTADTRB	GTADTRB4N	GTADTRB4N
		Compare match with GPT5.GTADTRA	GTADTRA5N	GTADTRA5N
		Compare match with GPT5.GTADTRB	GTADTRB5N	GTADTRB5N
		Compare match with GPT6.GTADTRA	GTADTRA6N	GTADTRA6N
		Compare match with GPT6.GTADTRB	GTADTRB6N	GTADTRB6N
		Compare match with GPT7.GTADTRA	GTADTRA7N	GTADTRA7N
		Compare match with GPT7.GTADTRB	GTADTRB7N	GTADTRB7N
		Compare match with GPT4.GTADTRA or with GPT4.GTADTRB	GTADTRA4N or GTADTRB4N	GTADTRA4N or GTADTRB4N
		Compare match with GPT5.GTADTRA or with GPT5.GTADTRB	GTADTRA5N or GTADTRB5N	GTADTRA5N or GTADTRB5N
		Compare match with GPT6.GTADTRA or with GPT6.GTADTRB	GTADTRA6N or GTADTRB6N	GTADTRA6N or GTADTRB6N
		Compare match with GPT7.GTADTRA or with GPT7.GTADTRB	GTADTRA7N or GTADTRB7N	GTADTRA7N or GTADTRB7N
Channels with dedicated independent sample-and-hold function	Target channel		AN000 to AN002	AN100 to AN102
Programmable gain amplifier	Target channel		AN000 to AN002	AN100 to AN102
	Gain setting		×2.0, ×2.5, ×3.077, ×3.636, ×4.0, ×4.444, ×5.0, ×5.714, ×6.667, ×10.0, ×13.333 (11 steps in total)	
Window comparator	Target channel		AN000 to AN002	AN100 to AN102
	Reference voltage and setting standard	Specified by external pins	CVREFL: AN003	CVREFH: AN103
		Internally generated	1/8AVCC0, 2/8AVCC0, 3/8AVCC0, 4/8AVCC0, 5/8AVCC0, 6/8AVCC0, 7/8AVCC0	
	Noise cancellation		Samples 16 results of detection by the comparator at PCLK, PCLK/2, PCLK/4, PCLK/8, PCLK/16, or PCLK/128.	
Interrupt			S12ADI S12GBADI CMP0 to CMP2	S12ADI1 S12GBADI1 CMP4 to CMP6
Module stop function setting*1			MSTPCRA. MSTPA17 bit	MSTPCRA. MSTPA16 bit

Note 1. For details, see section 12, Low Power Consumption.

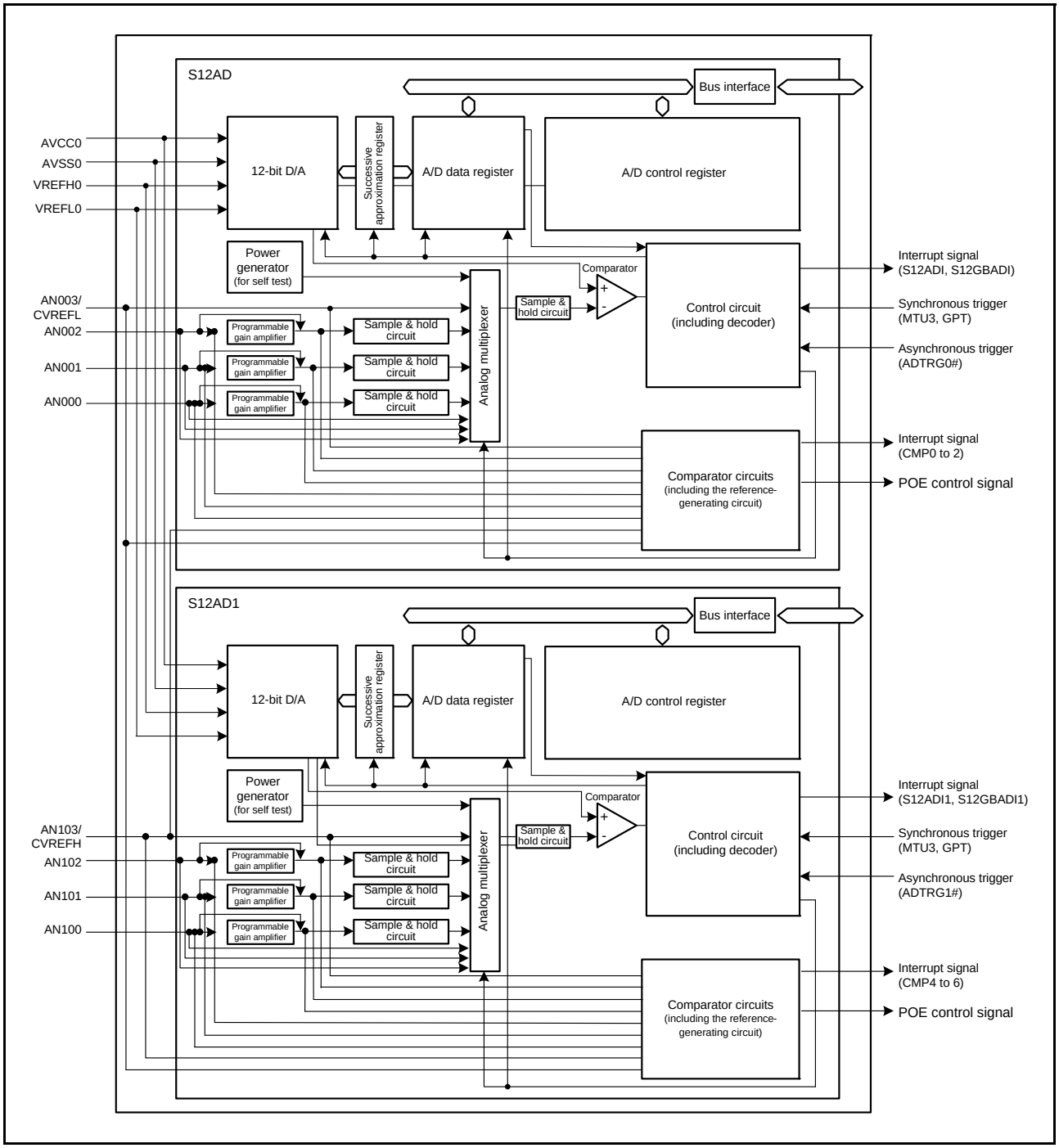


Figure 34.1 Block Diagram of 12-Bit A/D Converter

Table 34.3 indicates the input pins of the 12-bit A/D converter.

Table 34.3 Input Pins of 12-Bit A/D Converter

Unit	Pin Name	I/O	Function	On-Chip PGA	On-Chip Comparator
Unit 0 (S12AD)	AN000	Input	Analog input pin 0	Incorporated	Incorporated
	AN001	Input	Analog input pin 1	Incorporated	Incorporated
	AN002	Input	Analog input pin 2	Incorporated	Incorporated
	AN003/ CVREFL	Input	Analog input pin 3/comparator low-side reference-voltage pin (The pin serves as the comparator low-side reference-voltage pin when the comparator is operating and the application of reference voltages to external pins is selected.)	—	—
	ADTRG0#	Input	External trigger input pin for starting A/D conversion	—	—
Unit 1 (S12AD1)	AN100	Input	Analog input pin 4	Incorporated	Incorporated
	AN101	Input	Analog input pin 5	Incorporated	Incorporated
	AN102	Input	Analog input pin 6	Incorporated	Incorporated
	AN103/ CVREFH	Input	Analog input pin 7/comparator high-side reference-voltage pin (The pin serves as the comparator high-side reference-voltage pin when the comparator is operating and the application of reference voltages to external pins is selected.)	—	—
	ADTRG1#	Input	External trigger input pin for starting A/D conversion	—	—
Common to both units	AVCC0	Input	Analog block power supply pin	—	—
	AVSS0	Input	Analog block ground pin	—	—
	VREFH0	Input	Reference power supply pin	—	—
	VREFL0	Input	Reference power supply ground pin	—	—

34.2 Register Descriptions

34.2.1 A/D Data Registers y (ADDRy; y = 0 to 3), A/D Data-Doubling Register (ADDBLDR), A/D Data-Doubling Register A (ADDBLDRA), and A/D Data-Doubling Register B (ADDBLDRB)

The ADDRy registers are 16-bit read-only registers for storing the results of A/D conversion. Register ADDBLDR is a 16-bit read-only register for storing the result of A/D conversion in response to the second trigger in double-trigger mode. Registers ADDBLDRA and ADDBLDRB are 16-bit read-only registers for storing the result of A/D conversion in response to the respective triggers during extended operation in double-trigger mode.
The formats for data in the ADDRy, ADDBLDR, ADDBLDRA, and ADDBLDRB registers vary according to the following conditions.

- The setting of the A/D data register format selection bit (determining whether the data are flush-left or flush-right in the registers)
- The setting of the A/D data register bit-precision specification bits (for eight, 10, or 12 bits)
- The setting of the A/D-converted value cumulative mode selection register (determining whether A/D-converted value cumulative mode is or is not selected)

The conditions are given above each of the descriptions below.

- The settings are for flush-right data with 12-bit precision)

Address: S12AD: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h
S12AD1: ADDR0 0008 9120h, ADDR1 0008 9122h, ADDR2 0008 9124h, ADDR3 0008 9126h, ADDBLDR 0008 9118h, ADDBLDRA 0008 9184h, ADDBLDRB 0008 9186h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	AD[11:0]	Converted value 11 to 0	12-bit A/D-converted value	R
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings are for flush-right data with 10-bit precision

Address: S12AD: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h
S12AD1: ADDR0 0008 9120h, ADDR1 0008 9122h, ADDR2 0008 9124h, ADDR3 0008 9126h, ADDBLDR 0008 9118h, ADDBLDRA 0008 9184h, ADDBLDRB 0008 9186h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[11:2]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	AD[11:2]	Converted value 11 to 2	10 higher-order bits of the 12-bit A/D converted value	R
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings are for flush-right data with eight-bit precision.

Address
S12AD: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h
S12AD1: ADDR0 0008 9120h, ADDR1 0008 9122h, ADDR2 0008 9124h, ADDR3 0008 9126h, ADDBLDR 0008 9118h, ADDBLDRA 0008 9184h, ADDBLDRB 0008 9186h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	AD[11:4]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	AD[11:4]	Converted value 11 to 4	Eight higher-order bits of the 12-bit A/D converted value	R
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings are for flush-left data with 12-bit precision

Address
S12AD: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h
S12AD1: ADDR0 0008 9120h, ADDR1 0008 9122h, ADDR2 0008 9124h, ADDR3 0008 9126h, ADDBLDR 0008 9118h, ADDBLDRA 0008 9184h, ADDBLDRB 0008 9186h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b4	AD[11:0]	Converted value 11 to 0	12-bit A/D-converted value	R

- The settings are for flush-left data with 10-bit precision.

Address
S12AD: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h
S12AD1: ADDR0 0008 9120h, ADDR1 0008 9122h, ADDR2 0008 9124h, ADDR3 0008 9126h, ADDBLDR 0008 9118h, ADDBLDRA 0008 9184h, ADDBLDRB 0008 9186h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:2]										—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b6	AD[11:2]	Converted value 11 to 2	10 higher-order bits of the 12-bit A/D converted value	R

- The settings are for flush-left data with eight-bit precision.

Address
S12AD: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h
S12AD1: ADDR0 0008 9120h, ADDR1 0008 9122h, ADDR2 0008 9124h, ADDR3 0008 9126h, ADDBLDR 0008 9118h, ADDBLDRA 0008 9184h, ADDBLDRB 0008 9186h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:4]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	AD[11:4]	Converted value 11 to 4	Eight higher-order bits of the 12-bit A/D converted value	R

- When A/D-converted value addition mode is selected

Address
S12AD: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h
S12AD1: ADDR0 0008 9120h, ADDR1 0008 9122h, ADDR2 0008 9124h, ADDR3 0008 9126h, ADDBLDR 0008 9118h, ADDBLDRA 0008 9184h, ADDBLDRB 0008 9186h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[13:0]														—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b2	AD[13:0]	—	14-bit A/D-converted value addition result	R

When A/D-converted value addition mode is selected, the AD[13:0] bits show the value that is obtained by adding up A/D-converted values on a specific channel. In A/D-converted value addition mode, the value obtained by adding up A/D conversion results is stored left-justified as a 14-bit value in the A/D data register. The settings of the ADCER.ADPRC[1:0] and ADCER.ADRFMT bits become invalid.

34.2.2 A/D Self-Diagnosis Data Register (ADRD)

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the 12-bit A/D converter's self-diagnosis.

The following different formats are used depending on the setting of the A/D data register format select bit (ADRFMT) in ADCER. ADRD cannot be set to A/D-converted value addition mode.

- ADCER.ADRFMT = 0 (Setting for right-alignment)

Address: S12AD: ADRD 0008 901Eh
S12AD1: ADRD 0008 911Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	AD[11:0]	—	12-bit A/D-converted value	R
b13, b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREFH0 × 0 has been executed. 1 0: Self-diagnosis using VREFH0 × 1/2 has been executed. 1 1: Self-diagnosis using VREFH0 × 1 has been executed. For details of self-diagnosis, see section 34.2.8, A/D Control Extended Register (ADCER).	R

- ADCER.ADRFMT = 1 (Setting for left-alignment)

Address: S12AD: ADRD 0008 901Eh
S12AD1: ADRD 0008 911Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREFH0 × 0 has been executed. 1 0: Self-diagnosis using VREFH0 × 1/2 has been executed. 1 1: Self-diagnosis using VREFH0 × 1 has been executed. For details of self-diagnosis, see section 34.2.8, A/D Control Extended Register (ADCER).	R
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b4	AD[11:0]	—	12-bit A/D-converted value	R

34.2.3 A/D Control Register (ADCSR)

Address: S12AD: ADCSR 0008 9000h
S12AD1: ADCSR 0008 9100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		ADIE	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	DBLANS[4:0]	Double-trigger channel select	These bits select the analog input on one of the four channels for double-triggered operation. The setting is only effective while double-trigger mode is selected.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	GBADIE	Group B Scan End Interrupt Enable	0: Disables S12GBADI interrupt generation upon group B scan completion. 1: Enables S12GBADI interrupt generation upon group B scan completion.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselects double trigger mode. 1: Selects double trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: A/D conversion is started by the synchronous trigger (MTU3, GPT). 1: A/D conversion is started by the asynchronous trigger (ADTRGn#).	R/W
b9	TRGE	Trigger Start Enable	0: Disables A/D conversion to be started by the synchronous or asynchronous trigger. 1: Enables A/D conversion to be started by the synchronous or asynchronous trigger.	R/W
b10, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	ADIE	Scan End Interrupt Enable	0: Disables S12ADI interrupt generation upon scan completion. 1: Enables S12ADI interrupt generation upon scan completion.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single-cycle scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited	R/W
b15	ADST	A/D Conversion Start	0: Stops A/D conversion process. 1: Starts A/D conversion process.	R/W

Note 1. Starting A/D conversion using an external pin (asynchronous trigger)
If 1 is written to both the TRGE and EXTRG bits in ADCSR when a high-level signal is input to the external pin (ADTRGn#), and then if the ADTRGn# signal is driven low, the falling edge of ADTRGn# is detected and the scan conversion process is started. In this case, the pulse width of the low-level input must be at least 1.5 PCLK clock cycles.

ADCSR sets double trigger mode, A/D conversion start trigger; enables/disables scan end interrupt; selects the scan mode; and starts or stops A/D conversion.

DBLANS[4:0] Bits (Double-trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double trigger mode. The A/D conversion results of the analog input of the selected channel are stored into A/D data register y when conversion is started by the first trigger, and into the A/D data duplication register when started by the second trigger. Selection of the channel for double-triggered operation is described in Table 34.4. A/D-converted value addition mode with double trigger mode can be set by selecting the channel selected by the DBLANS[4:0] bits using the ADADS register. If double trigger mode is selected, the channel selected by the ADANSA register is invalid, and the channel selected by the DBLANS [4:0] bits is subjected to A/D conversion instead.
The DBLANS[4:0] bits should be set while the ADST bit is 0 (they should not be set simultaneously when 1 is written to the ADST bit.)

Table 34.4 Relationship between DBLANS Bit Settings and Double Trigger Enabled Channels

	Duplication Channel	
DBLANS[4:0]	S12AD	S12AD1
00000	AN000	AN100
00001	AN001	AN101
00010	AN002	AN102
00011	AN003	AN103

GBADIE Bit (Group B Scan End Interrupt Enable)

The GBADIE bit enables or disables group B scan end interrupt (S12GBADI) in group scan mode.

DBLE Bit (Double Trigger Mode Select)

In double trigger mode, the following operation is performed after scanning is started by the MTU3 or GPT trigger selected by the TRSA[5:0] bits in ADSTRGR.

1. When the ADIE bit is 1, a scan end interrupt is not generated upon first scan completion but is generated upon second scan completion.
2. The A/D conversion results of the analog input of the channel selected by the DBLANS[4:0] are stored into A/D data register y for the first time, and into the A/D data duplication register for the second time.

Setting the DBLE bit to 1 invalidates the channel selected by the ADANSA register. In continuous scan mode, double trigger mode should not be selected. In double trigger mode, software trigger should not be selected. The DBLE bit should be set while ADST bit is 0 (it should not be set simultaneously when 1 is written to the ADST bit.)

EXTRG Bit (Trigger Select)

The EXTRG bit selects the synchronous trigger or the asynchronous trigger as the trigger for starting A/D conversion.

TRGE Bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous trigger and the asynchronous trigger. This bit should be set to 1 in group scan mode.

ADIE Bit (Scan End Interrupt Enable)

The ADIE bit enables or disables the A/D scan end interrupt (S12ADI) in scans except for group B scan in group scan mode.

With double trigger mode deselected, the S12ADI interrupt is generated when the first scan is completed if the ADIE bit is set to 1.

With double trigger mode selected, the S12ADI interrupt is generated when the second scan is completed if the ADIE bit is set to 1 as long as the scan is started by the MTU3 or GPT trigger selected by the TRSA[5:0] bits in ADSTRGR.

ADCS[1:0] Bits (Scan Mode Select)

The ADCS bit selects the scan mode.
In single-cycle scan mode, A/D conversion is performed for the analog inputs of a maximum of four channels selected with the ADANSA register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, scan conversion is stopped.
In continuous scan mode, while the ADST bit in ADCSR is 1, A/D conversion is performed for the analog inputs of a maximum of four channels selected with the ADANSA register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is repeated beginning at the first channel. A/D conversion is repeated until the ADST bit in ADCSR is set to 0.
In group scan mode, A/D conversion is performed for the analog inputs (group A) of a maximum of four channels selected with the ADANSA register in the ascending order of the channel number after scanning is started by the MTU3 or GPT trigger selected by the TRSA[5:0] bits in ADSTRGR, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is stopped. A/D conversion is also performed for the analog inputs (group B) of a maximum of eight channels selected with the ADANSB register in the oscending order of the channel number after scanning is started by the MTU3 or GPT trigger celected by the TRSB[4:0] bits in ADSTRGR, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is stopped. In group scan mode, different channels and triggers should be selected for group A and group B.
The ADCS bit should be set while the ADST bit is 0 (it should not be set simultaneously when 1 is written to the ADST bit.)

ADST Bit (A/D Conversion Start)

The ADST bit starts or stops A/D conversion process.
Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and conversion target analog input.
[Setting conditions]

- 1 is written by software.
- The synchronous trigger (MTU3 or GPT, or temperature sensor) selected by the ADSTRGR.TRSA[5:0] bits is detected with ADCSR.EXTRG and ADCSR.TRGE bits being set to 0 and 1, respectively.
- A synchronous trigger (MTU3 or GPT) selected by the ADSTRGR.TRSB[5:0] bits is detected with the ADCSR.TRGE bit being set to 1 in group scan mode.
- The asynchronous trigger is detected with the ADCSR.TRGE and ADCSR.EXTRG bits being set to 1 and the ADSTRGR.TRSA[5:0] bits being set to “000000b”.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), a group B trigger is detected and A/D conversion of group B is started.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), a group B trigger is detected and A/D conversion of group B is started.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), the ADGSPCR.GBRP bit is set to 1 and A/D conversion of group B is started.

[Clearing conditions]

- 0 is written by software.
- The A/D conversion of all the channels selected is completed in single-cycle scan mode.
- Group A scan is completed in group scan mode.
- Group B scan is completed in group scan mode.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), a group A trigger is detected during A/D conversion of group B and the scanning of group B is stopped.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), the ADGSPCR.GBRP bit is set to 1 and the scanning of group B by a resumption trigger is completed.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1),

the ADGSPCR.GBRSCN bit is set to 1 and the scanning of group B by a trigger is completed.

Note 1. When group-A priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), do not set the ADST bit to 1.

Note 2. When group-A priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1) and ADGSPCR.GBRP = 1, do not set the ADST bit to 0. When terminating A/D conversion, follow the procedure for clearing the ADST bit.

34.2.4 A/D Channel Select Register A (ADANSA)

Address: S12AD: ADANSA 0008 9004h
S12AD1: ADANSA 0008 9104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	PG002 SEL	PG001 SEL	PG000 SEL	—	PG002 EN	PG001 EN	PG000 EN	—	—	—	—	ANSA[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	ANSA[3:0]	A/D Conversion Channels Select	0: AN000 to AN003 and AN100 to AN103 are not subjected to conversion. 1: AN000 to AN003 and AN100 to AN103 are subjected to scan conversion.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PG000EN	Programmable Gain Amplifier for AN000 Enable	0: Programmable Gain Amplifier operation is disabled 1: Programmable Gain Amplifier operation is enabled	R/W
b9	PG001EN	Programmable Gain Amplifier for AN001 Enable	0: Programmable Gain Amplifier operation is disabled 1: Programmable Gain Amplifier operation is enabled	R/W
b10	PG002EN	Programmable Gain Amplifier for AN002 Enable	0: Programmable Gain Amplifier operation is disabled 1: Programmable Gain Amplifier operation is enabled	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	PG000SEL	Programmable Gain Amplifier for AN000 Select	0: Not use (bypass) the Programmable Gain Amplifier 1: Use the Programmable Gain Amplifier	R/W
b13	PG001SEL	Programmable Gain Amplifier for AN001 Select	0: Not use (bypass) the Programmable Gain Amplifier 1: Use the Programmable Gain Amplifier	R/W
b14	PG002SEL	Programmable Gain Amplifier for AN002 Select	0: Not Use (bypass) the Programmable Gain Amplifier 1: Use the Programmable Gain Amplifier	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

ADANSA is used to select analog input channels for A/D conversion from among AN000 to AN003 and AN100 to AN103, use or not use Programmable Gain Amplifier for AN000 to AN002 and AN100 to AN102, disable or enable Programmable Gain Amplifier for AN000 to AN002 and AN100 to AN102.

ANSA[3:0] Bits (A/D Conversion Channel Select)

The ANSA[15:0] bits select analog input channels for A/D conversion from among AN000 to AN003 and AN100 to AN103. The channels to be selected and the number of channels can be arbitrarily set. The ANSA[0] bit corresponds to AN000 and the AN100.

In group scan mode, group A channels are to be selected.

When double trigger mode is selected, the channel selected by the ANSA[3:0] bits is invalid, and the channel selected by the ADCSR.DBLANS[4:0] bits is selected in group A instead.

The ANSA[3:0] bits should be set while the ADCSR.ADST bit is 0.

PGnEN Bit (Programmable Gain Amplifier for ANn Enable) (n=000 to 002, 100 to 102)

This bit sets disables or enables for Programmable Gain Amplifier operation.

PGnSEL Bit (Programmable Gain Amplifier for ANn Select) (n=000 to 002, 100 to 102)

This bit sets use or not use for Programmable Gain Amplifier operation.

34.2.5 A/D Channel Select Register B (ADANSB)

Address: S12AD: ADANSB 0008 9014h
S12AD1: ADANSB 0008 9114h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSB[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	ANSB[3:0]	A/D Conversion Channels Select	0: AN000 to AN003 and AN100 to AN103 are not subjected to conversion. 1: AN000 to AN003 and AN100 to AN103 are subjected to scan conversion.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADANSB selects channels for A/D conversion in group B from among AN000 to AN003 and AN100 to AN103 in group scan mode. ADANSB is not used in any other scan mode. The channels for conversion can be selected from among the channels other than group A channels, which are selected by the ADANSA register or ADCSR.DBLANS[4:0] bits in double trigger mode. The ANSB[0] bit corresponds to AN000 and AN100 bit corresponds to AN007.
The ANSB[3:0] bits should be set while the ADST bit is 0.

34.2.6 A/D-Converted Value Addition Mode Select Register (ADADS)

Address: S12AD: ADADS 0008 9008h
S12AD1: ADADS 0008 9108h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ADS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	ADS[3:0]	A/D-Converted Value Addition Channel Select	0: A/D-converted value addition mode for AN000 to AN007 and AN100 to AN103 is not selected. 1: A/D-converted value addition mode for AN000 to AN007 and AN100 to AN103 is selected.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADADS selects the channels AN000 to AN003 and AN100 to AN103 on which A/D conversion is performed successively 2 to 4 times and then converted values are added (integrated).

ADS[3:0] Bits (A/D-Converted Value Addition Channels 0 to 3 Select)

When the ADS[n] bit of the number that is the same as that of A/D converted channel selected by ANSA[n] bits (n = 0 to 3) in ADANSA or DBLANS[4:0] bits in ADCSR and ANSB[n] bits (n = 0 to 3) in ADANSB is set to 1, these bits perform A/D conversion of analog input of the selected channels successively 2 to 4 times that is set with the ADC[1:0] bits in ADADC and returns the added (integrated) conversion results to the A/D data register. For the channel for which the A/D conversion is performed and addition mode is not selected, a normal one-time conversion is performed and the conversion result is returned to the A/D data register.
The ADS[3:0] bits should be set while the ADCSR.ADST bit is 0.

Figure 34.2 shows a scanning operation sequence in which both the ADS[2] and ADS[6] bits are set to 1.
In continuous scan mode (ADCSR.ADCS = 10b), it is assumed that the addition count is set to 4 (ADADC.ADC[1:0] = 11b) and the channels AN000 to AN003 are selected (ADANSA.ANSA[3:0] = FFh). The conversion process begins with AN000. The AN002 conversion is performed successively 4 times, and the added (integrated) value is returned to the A/D data register 2. After that the AN003 conversion process is started. The AN006 conversion is performed successively 4 times and the added (integrated) value is returned to the A/D data register 6. After conversion of AN007, the conversion operation is once again performed in the same sequence from AN000.
For the channel for which the addition mode is not selected, the A/D data register format is determined by the ADRFMT bit in ADCER (right-alignment or left-alignment).

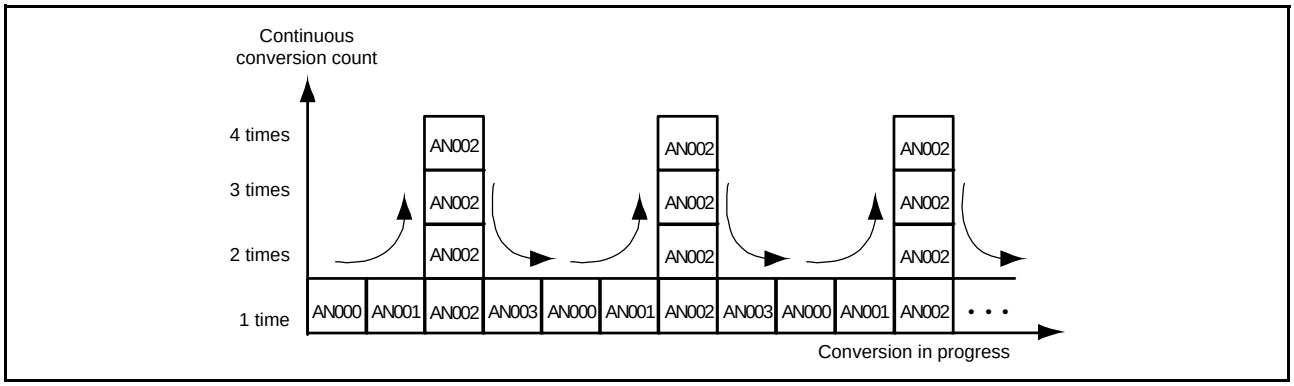


Figure 34.2 Scan Conversion Sequence with ADADC.ADC[1:0] and ADS[2] = 1 and ADS[6] = 1

34.2.7 A/D-Converted Value Addition Count Select Register (ADADC)

Address: S12AD: ADADC 0008 900Ch
S12AD1: ADADC 0008 910Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ADC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	ADC[1:0]	Addition Count Select	b1 b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADADC sets the addition count for the channels for which A/D-converted value addition mode is selected, and for A/D conversion.

ADC[1:0] Bits (Addition Count Select)

The ADC[1:0] bits set the addition count common to the channels for which A/D conversion or A/D-converted value addition mode is selected, including the channels selected in double trigger mode (by ADCSR.DBLANS[4:0] bits), and to A/D conversion.

The ADC[1:0] bits should be set while the ADCSR.ADST bit is 0.

34.2.8 A/D Control Extended Register (ADCER)

Address: S12AD: ADCER 0008 900Eh
S12AD1: ADCER 0008 910Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	DCE	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2, b1	ADPRC[1:0]	A/D data-register bit-precision specification bit	00: Values are stored with 12-bit precision in the A/D data registers. 01: Values are stored with 10-bit precision in the A/D data registers. 10: Values are stored with 8-bit precision in the A/D data registers. 11: Do not make this setting.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DCE	DCE discharge enable bit	0: Discharging does not proceed on completion of A/D conversion. 0: Discharging proceeds on completion of A/D conversion.	R/W
b5	ACE	Automatic Clearing Enable	0: Disables automatic clearing. 1: Enables automatic clearing.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Conversion Voltage Select for Self-Diagnosis	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: Uses VREFH0 × 0 for self-diagnosis. 1 0: Uses VREFH0 × 1/2 for self-diagnosis. 1 1: Uses VREFH0 × 1 for self-diagnosis.	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Rotation mode for self-diagnosis voltage 1: Fixed mode for self-diagnosis voltage	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Disables self-diagnosis of 12-bit A/D converter. 1: Enables self-diagnosis of12-bit A/D converter.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Right-alignment is selected for the A/D data register format. 1: Left-alignment is selected for the A/D data register format.	R/W

ADCER sets the parameters related to self-diagnosis, format of the A/D data registers y (ADDRy), and enables/disables automatic clearing of registers.

ADPRC Bits (A/D Data Register Bit-Precision Specification)

These bits select storage of the results of A/D conversion with eight-, 10-, or 12-bit precision in the ADDRy, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.

DCE Bit (Discharge Enable)

This bit selects whether discharging of analog pins involved in conversion proceeds or does not proceed on completion of A/D conversion. If a failure leads to an input pin becoming open circuit, when discharging proceeds several times and the result of conversion approaches 0000h, the open circuit state of the pin is detectable.

ACE Bit (Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (All “0”) of ADDRy, ADRD,ADDBLDR, ADDBLDRA, and ADDBLDRB after the register has been read by the CPU, DTC, or DMACA. This function enables update failures of ADDRy, ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB to be detected.

DIAGVAL[1:0] Bits (Conversion Voltage Select for Self-Diagnosis)

For details, refer to the ADCER.DIAGLD bit description.
Self-diagnosis should not be executed by setting the ADCER.DIAGLD bit to 1 with these bits set to 00b.

DIAGLD Bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis. Setting this bit to 0 allows conversion of the voltages in rotation mode where VREFH0 × 0, VREFH0 × 1/2, and VREFH0 × 1 are converted in this order. After reset, VREFH0 × 0 is first converted if rotation mode is selected whereas the fixed voltage specified by the ADCER.DIAGVAL[1:0] bits is converted if fixed mode is selected. In rotation mode, the self-diagnosis voltage value does not return to VREFH0 × 0 when scan conversion is completed; when scan conversion is restarted, rotation starts at the voltage value following the previous value. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.
The DIAGLD bit should be set while the ADST bit is 0.

DIAGM Bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.
Self-diagnosis is used to detect a failure of the 12-bit A/D converter. Specifically, one of the internally generated voltage values VREFH0 × 0, VREFH0 × 1/2, and VREFH0 × 1 is converted. When conversion is completed, information of the converted voltage and the conversion result is stored into the self-diagnosis data register (ADRD). ADRD can then be read out by software to determine whether the conversion result falls within the normal range (normal) or not (abnormal). Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. The execution time of self-diagnosis equals to the A/D conversion time of one channel. If selected, self-diagnosis is not executed. When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.
The DIAGM bit should be set while the ADST bit is 0.

ADRFMT Bit (A/D Data Register Format Select)

The ADRFMT bit specifies left-alignment or right-alignment for the data to be stored in ADDRy, ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.
When the A/D converted value addition mode is selected, the format of each data register is fixed to left-alignment, irrespective of the ADCER.ADRFMT bit value.

For details on the format of the data registers, see section 34.2.1, A/D Data Registers y (ADDRy; y = 0 to 3), A/D Data-Doubling Register (ADDBLDR), A/D Data-Doubling Register A (ADDBLDRA), and A/D Data-Doubling Register B (ADDBLDRB), and section 34.2.2, A/D Self-Diagnosis Data Register (ADRD).

34.2.9 A/D Start Trigger Select Register (ADSTRGR)

Address: S12AD: ADSTRGR 0008 9010h
S12AD1: ADSTRGR 0008 9110h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B	Select the A/D conversion start trigger for group B in group scan mode.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	Select the A/D conversion start trigger in single-cycle scan mode and continuous mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSTRGR selects the A/D conversion start trigger.

TRSB[5:0] Bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits require to be set only in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B, setting software trigger or asynchronous trigger is prohibited. Therefore, the TRSB[5:0] bits should be set to the value other than 000000 and the ADCSR.TRGE bit should be set to 1 in group scan mode.When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single cycle scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 1Fh. Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger may become invalid.
Table 34.5 shows the A/D conversion startup sources selected by TRSB[5:0] bits.

TRSA[5:0] Bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single-cycle scan mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in group A is selected. For scan execution in group scan mode or double trigger mode, software trigger or asynchronous trigger cannot be used.

- When using the A/D conversion startup source of the synchronous trigger (MTU3, GPT), set the TRGE bit in ADCSR to 1 and set the EXTRG bit in ADCSR to 0.
- When using the asynchronous trigger (ADTRGn#), set the TRGE bit in ADCSR to 1 and set the EXTRG bit in ADCSR to 1.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, and the TRSA[5:0] bits.
  Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger may become invalid.
  Table 34.6 shows the A/D conversion startup sources selected by TRSA[5:0] bits

Table 34.5 Selection of A/D Activation Sources by the TRSB[5:0] Bits (1/2)

Module	Source	Remarks	TRSB [5]	TRSB [4]	TRSB [3]	TRSB [2]	TRSB [1]	TRSB [0]
Trigger source de-selection state			1	1	1	1	1	1
MTU3	TRGA0N	Input capture to or compare match with MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Input capture to or compare match with MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Input capture to or compare match with MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Input capture to or compare match with MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Input capture to or compare match with MTU4.TGRA or, in complementary PWM mode, an underflow of MTU4.TCNT (in the trough)	0	0	0	1	0	1
	TRGA6N	Input capture to or compare match with MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Input capture to or compare match with MTU7.TGRA, or in complementary PWM mode, an underflow of MTU7.TCNT (in the trough)	0	0	0	1	1	1
	TRG0AN	Compare match with MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT and between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	0	1	0	0	0	0

Table 34.5 Selection of A/D Activation Sources by the TRSB[5:0] Bits (2/2)

Module	Source	Remarks	TRSB [5]	TRSB [4]	TRSB [3]	TRSB [2]	TRSB [1]	TRSB [0]
GPT to GPT3	GTADTRA0N	Compare match with GPT0.GTADTRA	0	1	0	0	0	1
	GTADTRB0N	Compare match with GPT0.GTADTRB	0	1	0	0	1	0
	GTADTRA1N	Compare match with GPT1.GTADTRA	0	1	0	0	1	1
	GTADTRB1N	Compare match with GPT1.GTADTRB	0	1	0	1	0	0
	GTADTRA2N	Compare match with GPT2.GTADTRA	0	1	0	1	0	1
	GTADTRB2N	Compare match with GPT2.GTADTRB	0	1	0	1	1	0
	GTADTRA3N	Compare match with GPT3.GTADTRA	0	1	0	1	1	1
	GTADTRB3N	Compare match with GPT3.GTADTRB	0	1	1	0	0	0
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	0	1	1	0	0	1
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	0	1	1	0	1	0
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	0	1	1	0	1	1
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	0	1	1	1	0	0
GPT4 to GPT7	GTADTRA4N	Compare match with GPT4.GTADTRA	0	1	1	1	0	1
	GTADTRB4N	Compare match with GPT4.GTADTRB	0	1	1	1	1	0
	GTADTRA5N	Compare match with GPT5.GTADTRA	0	1	1	1	1	1
	GTADTRB5N	Compare match with GPT5.GTADTRB	1	0	0	0	0	0
	GTADTRA6N	Compare match with GPT6.GTADTRA	1	0	0	0	0	1
	GTADTRB6N	Compare match with GPT6.GTADTRB	1	0	0	0	1	0
	GTADTRA7N	Compare match with GPT7.GTADTRA	1	0	0	0	1	1
	GTADTRB7N	Compare match with GPT7.GTADTRB	1	0	0	1	0	0
	GTADTRA4N or GTADTRB4N	Compare match with GPT4.GTADTRA or with GPT4.GTADTRB	1	0	0	1	0	1
	GTADTRA5N or GTADTRB5N	Compare match with GPT5.GTADTRA or with GPT5.GTADTRB	1	0	0	1	1	0
	GTADTRA6N or GTADTRB6N	Compare match with GPT6.GTADTRA or with GPT6.GTADTRB	1	0	0	1	1	1
	GTADTRA7N or GTADTRB7N	Compare match with GPT7.GTADTRA or with GPT7.GTADTRB	1	0	1	0	0	0

Table 34.6 Selection of A/D Activation Sources by the TRSA[5:0] Bits (1/2)

Module	Source	Remarks	TRSA [5]	TRSA [4]	TRSA [3]	TRSA [2]	TRSA [1]	TRSA [0]
Trigger source de-selection state			1	1	1	1	1	1
External pin	ADTRG0#	Input pin for the ADTRG0# trigger	0	0	0	0	0	0
	ADTRG1#	Input pin for the ADTRG1# trigger	0	0	0	0	0	0
MTU3	TRGA0N	Input capture to or compare match with MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Input capture to or compare match with MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Input capture to or compare match with MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Input capture to or compare match with MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Input capture to or compare match with MTU4.TGRA or, in complementary PWM mode, an underflow of MTU4.TCNT (in the trough)	0	0	0	1	0	1
	TRGA6N	Input capture to or compare match with MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Input capture to or compare match with MTU7.TGRA, or in complementary PWM mode, an underflow of MTU7.TCNT (in the trough)	0	0	0	1	1	1
	TRG0AN	Compare match with MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT and between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	0	1	0	0	0	0

Table 34.6 Selection of A/D Activation Sources by the TRSA[5:0] Bits (2/2)

Module	Source	Remarks	TRSA [5]	TRSA [4]	TRSA [3]	TRSA [2]	TRSA [1]	TRSA [0]
GPT0 to GPT3	GTADTRA0N	Compare match with GPT0.GTADTRA	0	1	0	0	0	1
	GTADTRB0N	Compare match with GPT0.GTADTRB	0	1	0	0	1	0
	GTADTRA1N	Compare match with GPT1.GTADTRA	0	1	0	0	1	1
	GTADTRB1N	Compare match with GPT1.GTADTRB	0	1	0	1	0	0
	GTADTRA2N	Compare match with GPT2.GTADTRA	0	1	0	1	0	1
	GTADTRB2N	Compare match with GPT2.GTADTRB	0	1	0	1	1	0
	GTADTRA3N	Compare match with GPT3.GTADTRA	0	1	0	1	1	1
	GTADTRB3N	Compare match with GPT3.GTADTRB	0	1	1	0	0	0
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	0	1	1	0	0	1
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	0	1	1	0	1	0
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	0	1	1	0	1	1
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	0	1	1	1	0	0
GPT4 to GPT7	GTADTRA4N	Compare match with GPT4.GTADTRA	0	1	1	1	0	1
	GTADTRB4N	Compare match with GPT4.GTADTRB	0	1	1	1	1	0
	GTADTRA5N	Compare match with GPT5.GTADTRA	0	1	1	1	1	1
	GTADTRB5N	Compare match with GPT5.GTADTRB	1	0	0	0	0	0
	GTADTRA6N	Compare match with GPT6.GTADTRA	1	0	0	0	0	1
	GTADTRB6N	Compare match with GPT6.GTADTRB	1	0	0	0	1	0
	GTADTRA7N	Compare match with GPT7.GTADTRA	1	0	0	0	1	1
	GTADTRB7N	Compare match with GPT7.GTADTRB	1	0	0	1	0	0
	GTADTRA4N or GTADTRB4N	Compare match with GPT4.GTADTRA or with GPT4.GTADTRB	1	0	0	1	0	1
	GTADTRA5N or GTADTRB5N	Compare match with GPT5.GTADTRA or with GPT5.GTADTRB	1	0	0	1	1	0
	GTADTRA6N or GTADTRB6N	Compare match with GPT6.GTADTRA or with GPT6.GTADTRB	1	0	0	1	1	1
	GTADTRA7N or GTADTRB7N	Compare match with GPT7.GTADTRA or with GPT7.GTADTRB	1	0	1	0	0	0

34.2.10 A/D Sampling State Register n (ADSSTRn) (n = 0 to 3)

Address: S12AD: ADSSTR0 0008 9060h, ADSSTR1 0008 9073h, ADSSTR2 0008 9074h, ADSSTR3 0008 9075h
S12AD1: ADSSTR0 0008 9160h, ADSSTR1 0008 9173h, ADSSTR2 0008 9174h, ADSSTR3 0008 9175h

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	These bits set the sampling time in the range from 13 to 255 states.	R/W

The ADSSTRn register sets the sampling time for analog input.
If one state is one ADCLK (A/D conversion clock) cycle and the ADCLK clock is 50 MHz, one state is 20 ns. The initial value is 20 states. If the impedance of analog input signal source is too high to secure sufficient sampling time or if the ADCLK clock is slow, the sampling time can be adjusted. When any bit of this register is to be set, ADCSR.ADST must be 0. The sampling time must be set to a value that is 13 states or more and is 255 or less. In addition, the sampling time must be 0.4 µs or more. Table 34.7 shows the relationship between the A/D sampling state register and the relevant channels.
For details, refer to section 34.3.5, Analog Input Sampling and Scan Conversion Time.

Table 34.7 Relationship between A/D Sampling State Register and Relevant Channels

	Corresponding Channels	
Bit Name	**S12ADB0**	**S12ADBl**
ADSSTR0.SST[7:0] bits	AN000/self-diagnosis	AN100/self-diagnosis
ADSSTR1.SST[7:0] bits	AN001	AN101
ADSSTR2.SST[7:0] bits	AN002	AN102
ADSSTR3.SST[7:0] bits	AN003	AN103

34.2.11 A/D Sample and Hold Circuit Control Register (ADSHCR)

Address: S12AD: ADSHCR 0008 9066h
S12AD1: ADSHCR 0008 9166h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SHANS[2:0]			SSTSH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SSTSH[7:0]	Sampling Time Sample-and-Hold Circuit Setting	Set the sampling time (4 to 255 states).	R/W
b10 to b8	SHANS[2:0]	Channel-Dedicated Sample-and-Hold Circuit Bypass Select	Select whether to use or not use (bypass) AN000 to AN002 and AN100 to AN102 channel-dedicated sample-and-hold circuits. 0: Bypass the channel-dedicated sample-and-hold circuits. 1: Use the channel-dedicated sample-and-hold circuits.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSHCR sets the parameters related to channel-dedicated sample-and-hold circuits.

SSTSH[7:0] Bits (Sampling Time Sample-and-Hold Circuit Setting)

The SSTSH[7:0] bits set the sampling time for the channel-dedicated sample-and-hold circuits. One state is one ADCLK (A/D conversion clock) cycle. When the ADCLK is 50 MHz, one state is 20 ns. The initial value is 20 states. If the impedance of the analog input signal source is too high to secure sufficient sampling time or if the ADCLK is slow, the sampling time can be adjusted. The SSTSH[7:0] bits should be set while the ADST bit in ADCSR is 0. The set value for sampling time should be 4 or more states and 255 or less states. The sampling time should be 0.4 μs or longer. For example, when the ADCLK is 25 MHz, the lower limit of the set value for sampling states is 10 states.

SHANS[2:0] Bits (Channel-Dedicated Sample-and-Hold Circuit Bypass Select)

The SHANS[2:0] bits select whether to use or not use (bypass) AN000 to AN002 and AN100 to AN102 channel-dedicated sample-and-hold circuits. The SHANS[0] bit selects AN000 and AN100, SHANS[1] bit selects AN001 and AN101, and SHANS[2] bit selects AN002 and AN102. The SHANS[2:0] bits should be set while the ADST bit in ADCSR is 0.

If any channel from among AN000 to AN002 and AN100 to AN102 is selected for group B while operation is in group scan mode under group A priority control, make the setting to bypass the channel's dedicated sample-and-hold circuit.

34.2.12 A/D Group Scan Priority Control Register (ADGSPCR)

Address: S12AD: ADGSPCR 0008 9080h
S12AD1: ADGSPCR 0008 9180h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PGS	Group-A priority control setting bit*1	0: Operation is without group A priority control 1: Operation is with group A priority control	R/W
b1	GBRSCN	Group B restart setting bit	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Scanning for group B is not restarted after having been discontinued due to group A priority control. 1: Scanning for group B is restarted after having been discontinued due to group A priority control.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Single-cycle scan continuous activation bit for Group B*2	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Single-cycle scans through group B are not continuously activated. 1: Single-cycle scans through group B are continuously activated.	R/W

Note 1. When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be 01b (group scan mode). If the bits are set to any other values, operation is not guaranteed.
Note 2. When the GBRP bit has been set to 1, single-cycle scan is performed continuously on group B regardless of the setting of the GBRSCN bit.

Register ADGSPCR is used to make settings for priority control of A/D conversion in group-scan mode under group A priority control.

PGS Bit (Group A Priority Control Setting)

This bit sets the priority of operation on group A. Set this bit to 1 when giving priority to operation on group A.
When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode). If the bits are set to any other values, operation is not guaranteed.
When the PGS bit has been set to 0, clear operation must be performed by software according to section 34.6.2, Notes on Stopping A/D Conversion. When the PGS bit has been set to 1, make settings according to section 34.3.4.4, Operation under Group-A Priority Control.
When operating under group-A priority control in the group-scan mode, set to 1 to the PGSC bit of the ADGSPMR register, or specify the frequency ratio between the peripheral module clock (PCLKB) and A/D conversion clock, ADCLK (=PCLKD) as indicated below.

(a) PCLKB = PCLKD (Set the same value to the SCKCR. PCKB [3:0] and SCKCR. PCKD[3:0])
(b) PCLKB/2 = PCLKD (Set a value which +1 is added to the one set to the SCKCR. PCKB [3:0] to the SCKCR. PCKD[3:0])

GBRSCN Bit (Group B Restart Setting)

This bit controls the restarting of scan operation on group B when operation on group A is given priority.
If a scan operation on group B has been stopped by a group A trigger input with the GBRSCN bit set to 1, the scan operation is restarted on completion of the A/D conversion on group A. Also, if a group B trigger is input during A/D conversion on group A, the scan operation on group B is restarted on completion of the A/D conversion on group A. However, if group A triggers are input continuously, the scan operation on group B is not restarted.
If the GBRSCN bit has been set to 0, triggers that are input during A/D conversion are ignored. Also, the ADCSR.ADST bit must be 0 when the GBRSCN bit is to be set.

The setting of the GBRSCN bit becomes valid when the PGS bit is set to 1.

GBRP Bit (Single-Cycle Scan Continuous Activation for Group B)

This bit is set when a single-cycle scan operation is to be performed continuously on group B.
Setting the GBRP bit to 1 starts a single-cycle scan on group B. On completion of the scan, another single-cycle scan on group B is automatically started. If an A/D conversion on group B has been stopped due to an operation on group A that takes priority, single-cycle scan on group B is automatically restarted on completion of the A/D conversion on group A.
Disable group B trigger input before setting the GBRP bit to 1. Setting the GBRP bit to 1 invalidates the setting of the GBRSCN bit.
The ADCSR.ADST bit must be 0 when the GBRP bit is to be set.
The setting of the GBRP bit is valid when the PGS bit is 1.

34.2.13 Comparator Operating Mode Selection Register 0 (ADCMPMD0)

Address: S12AD: ADCMPMD0 0008 90E0h
S12AD1: ADCMPMD0 0008 91E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CEN002[1:0]		CEN001[1:0]		CEN000[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CEN000[1:0]	Comparator selection bits for AN000/AN100	b1 b0 0 0: The comparator is not in use. 0 1: The comparator is in use for comparison with the low level (detection of input voltages that are lower than the low-side reference voltage). 1 0: The comparator is in use for comparison with the high level (detection of input voltages that are higher than the high-side reference voltage). 1 1: The comparator is in use as a window comparator (detecting input voltages that are beyond the range from the low-side reference voltage to the high-side reference voltage).	R/W
b2, b3	CEN001[1:0]	Comparator selection bits for AN001/AN101	b2 b3 0 0: The comparator is not in use. 0 1: The comparator is in use for comparison with the low level (detection of input voltages that are lower than the low-side reference voltage). 1 0: The comparator is in use for comparison with the high level (detection of input voltages that are higher than the high-side reference voltage). 1 1: The comparator is in use as a window comparator (detecting input voltages that are beyond the range from the low-side reference voltage to the high-side reference voltage).	R/W
b5, b4	CEN002[1:0]	Comparator selection bits for AN002/AN102	b5 b4 0 0: The comparator is not in use. 0 1: The comparator is in use for comparison with the low level (detection of input voltages that are lower than the low-side reference voltage). 1 0: The comparator is in use for comparison with the high level (detection of input voltages that are higher than the high-side reference voltage). 1 1: The comparator is in use as a window comparator (detecting input voltages that are beyond the range from the low-side reference voltage to the high-side reference voltage).	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The setting of the ADCMPMD0 register determines whether or not the comparator is in use.

CENn[1:0] Bits (ANn Comparator Selection) (n = 000 to 002)

These bits determine whether or not the given comparator is in use and if it is, its mode of operation.

34.2.14 Comparator Operating-Mode Selection Register 1 (ADCMPMD1)

Address: S12AD: ADCMPMD1 0008 90E2h
S12AD1: ADCMPMD1 0008 91E2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VSELL0	VSELH0	CSEL0	—	REFH[2:0]			—	REFL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	REFL[2:0]	Comparator Low-Side Reference-Voltage Internal-Voltage Selection	b2 b1 b0 0 0 0: Disabled 0 0 1: AVCC0 × 1/8 0 1 0: AVCC0 × 2/8 0 1 1: AVCC0 × 3/8 1 0 0: AVCC0 × 4/8 1 0 1: AVCC0 × 5/8 1 1 0: AVCC0 × 6/8 1 1 1: AVCC0 × 7/8	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	REFH[2:0]	Comparator High-Side Reference-Voltage Internal-Voltage Selection	b6 b5 b4 0 0 0: Disabled 0 0 1: AVCC0 × 1/8 0 1 0: AVCC0 × 2/8 0 1 1: AVCC0 × 3/8 1 0 0: AVCC0 × 4/8 1 0 1: AVCC0 × 5/8 1 1 0: AVCC0 × 6/8 1 1 1: AVCC0 × 7/8	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	CSEL0	Comparator input selection bit	0: Use the signal before it is amplified by the programmable gain amplifier as comparator input. 1: Use the signal after it is amplified by the programmable gain amplifier as comparator input.	R/W
b9	VSELH0	Comparator High-Side Reference-Voltage Selection	0: The voltage on the AN103 pin is input as the high-side reference-voltage. 1: The internal voltage selected by the REFH[2:0] bits is input as the high-side reference-voltage.	R/W
b10	VSELL0	Comparator Low-Side Reference-Voltage Selection Bit	0: The voltage on the AN003 pin is input as the high-side reference-voltage. 1: The internal voltage selected by the REFL[2:0] bits is input as the high-side reference-voltage.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADCMPMD1 register is used to set the inputs for the comparator and the reference voltages.

REFL[2:0] Bits (Comparator Low-Side Reference-Voltage Internal-Voltage Selection)

These bits are used to set the internal-voltage to be used as the low-side reference-voltage for the comparator. The range of usable settings differs with the conditions of usage, so see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions], regarding the range of REFL voltage.

CSEL0 Bit (AN000 to AN002 and AN100 to AN102 Comparator Input Selection)

This bit selects comparator input for AN000 to AN002 and AN100 to AN102

REFH[2:0] Bits (Comparator High-Side Reference-Voltage Internal-Voltage Selection)

These bits are used to set the internal-voltage to be used as the high-side reference-voltage for the comparator. The range of usable settings differs with the conditions of usage, so see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions], regarding the range of REFL voltage.

VSELH0 Bit (Comparator High-Side Reference-Voltage Selection)

This bit selects how the high-side reference voltage for the comparator is input.

VSELL0 Bit (Comparator High-Side Reference-Voltage Selection)

This bit selects how the low-side reference voltage for the comparator is input.

34.2.15 Comparator Filter-Mode Register (ADCMPNR0)

Address: S12AD: ADCMPNR0 0008 90E4h
S12AD1: ADCMPNR0 0008 91E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	C002NR[3:0]				C001NR[3:0]				C000NR[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	C000NR[3:0]	Comparator Noise-Cancelling Filter Mode Selection Bits for AN000/ AN100	b3 b0 0 0 0 0: Results of detection by the comparator are not sampled. 1 0 0 0: Results of detection by the comparator are sampled 16 times at PCLK. 1 0 0 1: Results of detection by the comparator are sampled 16 times at PCLK/2. 1 0 1 0: Results of detection by the comparator are sampled 16 times at PCLK/4. 1 0 1 1: Results of detection by the comparator are sampled 16 times at PCLK/8. 1 1 0 0: Results of detection by the comparator are sampled 16 times at PCLK/16. 1 1 0 1: Results of detection by the comparator are sampled 16 times at PCLK/128. Do not make settings other than those listed above.	R/W
b7 to b4	C001NR[3:0]	Comparator Noise-Cancelling Filter Mode Selection Bits for AN001/ AN101	b7 b4 0 0 0 0: Results of detection by the comparator are not sampled. 1 0 0 0: Results of detection by the comparator are sampled 16 times at PCLK. 1 0 0 1: Results of detection by the comparator are sampled 16 times at PCLK/2. 1 0 1 0: Results of detection by the comparator are sampled 16 times at PCLK/4. 1 0 1 1: Results of detection by the comparator are sampled 16 times at PCLK/8. 1 1 0 0: Results of detection by the comparator are sampled 16 times at PCLK/16. 1 1 0 1: Results of detection by the comparator are sampled 16 times at PCLK/128. Do not make settings other than those listed above.	R/W
b11 to b8	C002NR[3:0]	Comparator Noise-Cancelling Filter Mode Selection Bits for AN002/ AN102	b11 b8 0 0 0 0: Results of detection by the comparator are not sampled. 1 0 0 0: Results of detection by the comparator are sampled 16 times at PCLK. 1 0 0 1: Results of detection by the comparator are sampled 16 times at PCLK/2. 1 0 1 0: Results of detection by the comparator are sampled 16 times at PCLK/4. 1 0 1 1: Results of detection by the comparator are sampled 16 times at PCLK/8. 1 1 0 0: Results of detection by the comparator are sampled 16 times at PCLK/16. 1 1 0 1: Results of detection by the comparator are sampled 16 times at PCLK/128. Do not make settings other than those listed above.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Register ADCMPNR0 is used to make settings for processing by the noise filter of the results of detection by the comparator.

CnNR[3:0] Bits (ANn Comparator Noise-Cancelling Filter Mode Selection) (n = 000 to 002)

These bits set the operation of the noise filter for the results of detection by the ANn comparator. The corresponding ADCMPFR.CnFLAG is set if “detected” is the result from all samples of the results of detection by the comparator in accord with the specified conditions. At this time, an activation request in the form of a comparator interrupt (CMP0 to CMP2, CMP4 to CMP6) or port-output enable 3 signal can be produced in accord with the setting in the ADCMPSEL register.

34.2.16 Comparator Detection Flag Register (ADCMPFR)

Address: S12AD: ADCMPFR 0008 90E8h
S12AD1: ADCMPFR 0008 91E8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	C002FLAG	C001FLAG	C000FLAG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C000FLAG	Comparator Detection Flag for AN000/AN100	0: The comparator has not detected the condition. 1: The comparator has detected the condition.	R/W*1
b1	C001FLAG	Comparator Detection Flag for AN001/AN101	0: The comparator has not detected the condition. 1: The comparator has detected the condition.	R/W*1
b2	C002FLAG	Comparator Detection Flag for AN002/AN102	0: The comparator has not detected the condition. 1: The comparator has detected the condition.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The only writable value is 0, which clears the flag. When clearing theC000FLAG, C001FLAG, or C002FLAG bits, be sure to clear only the target bit or bits for clearing and to write 1 to the other bits.

The ADCMPFR register contains flags that indicate the state (detection or non-detection) of the comparators.

CnFLAG flags (Comparator Detection Flag for ANn; n = 000 to 002)

Each flag indicates the state of a comparator in terms of detection or non-detection.
[Setting condition]

- Detection of a change in the input voltage to a voltage above the low-side threshold.
- Detection of a change in the input voltage to a voltage below the high-side threshold.

[Clearing condition]

- Software writing 0 to the flag.

34.2.17 Comparator Interrupt Selection Register (ADCMPSEL)

Address: S12AD: ADCMPSEL 0008 90EAh
S12AD1: ADCMPSEL 0008 91EAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	POERQ002	POERQ001	POERQ000	—	—	—	—	—	IE002	IE001	IE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IE000	Comparator Detection-Interrupt (CMP0/CMP4) Enable for AN000/AN100	0: Interrupt generation is disabled. 1: Interrupt generation is enabled.	R/W
b1	IE001	Comparator Detection-Interrupt (CMP1/CMP5) Enable for AN001/AN101	0: Interrupt generation is disabled. 1: Interrupt generation is enabled.	R/W
b2	IE002	Comparator Detection-Interrupt (CMP2/CMP6) Enable for AN002/AN102	0: Interrupt generation is disabled. 1: Interrupt generation is enabled.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	POERQ000	POE Request Generation on Comparator Detection Setting for AN000/AN100	0: POE request generation on comparator detection is disabled for AN000. 1: POE request generation on comparator detection is enabled for AN000.	R/W
b9	POERQ001	POE Request Generation on Comparator Detection Setting for AN001/AN101	0: POE request generation on comparator detection is disabled for AN001. 1: POE request generation on comparator detection is enabled for AN001.	R/W
b10	POERQ002	POE Request Generation on Comparator Detection Setting Bit for AN002/AN102	0: POE request generation on comparator detection is disabled for AN002. 1: POE request generation on comparator detection is enabled for AN002.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Settings in ADCMPSEL determine if the comparator detection flags act as sources for CPU interrupts or POE signals.

IEn (ANn Comparator Detection-Interrupt Enable) Bit (n = 000 to 002)

Each bit disables or enables the generation of an interrupt (CMP0 to CMP2, CMP4 to CMP6) in response to detection by the corresponding comparator.

POERQn Bit (ANn POE Request Generation on Comparator Detection Setting) (n = 000 to 002)

Each bit disables or enables the generation of a POE request in response to detection by the corresponding comparator. The POE request signal is the logical OR of the detection signals from comparators selected by the POERQn bits.

34.2.18 A/D Programmable Gain Amplifier Register (ADPG)

Address: S12AD: ADPG 0008 908Ah
S12AD1: ADPG 0008 918Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	PG2GAIN				PG1GAIN				PG0GAIN			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	PG0GAIN	Programmable Gain Amplifier 0 Gain Select	b3 b0 0 0 0 0: × 2.0 0 0 0 1: × 2.5 0 0 1 0: setting prohibited 0 0 1 1: setting prohibited 0 1 0 0: × 3.077 0 1 0 1: setting prohibited 0 1 1 0: × 3.636 0 1 1 1: × 4.0 1 0 0 0: × 4.444 1 0 0 1: × 5.0 1 0 1 0: × 5.714 1 0 1 1: × 6.667 1 1 0 0: setting prohibited 1 1 0 1: × 10.0 1 1 1 0: × 13.333 1 1 1 1: setting prohibited	R/W
b7 to b4	PG1GAIN	Programmable Gain Amplifier 1 Gain Select	b7 b4 0 0 0 0: × 2.0 0 0 0 1: × 2.5 0 0 1 0: setting prohibited 0 0 1 1: setting prohibited 0 1 0 0: × 3.077 0 1 0 1: setting prohibited 0 1 1 0: × 3.636 0 1 1 1: × 4.0 1 0 0 0: × 4.444 1 0 0 1: × 5.0 1 0 1 0: × 5.714 1 0 1 1: × 6.667 1 1 0 0: setting prohibited 1 1 0 1: × 10.0 1 1 1 0: × 13.333 1 1 1 1: setting prohibited	R/W
b11 to b8	PG2GAIN	Programmable Gain Amplifier 2 Gain Select	b11 b8 0 0 0 0: × 2.0 0 0 0 1: × 2.5 0 0 1 0: setting prohibited 0 0 1 1: setting prohibited 0 1 0 0: × 3.077 0 1 0 1: setting prohibited 0 1 1 0: × 3.636 0 1 1 1: × 4.0 1 0 0 0: × 4.444 1 0 0 1: × 5.0 1 0 1 0: × 5.714 1 0 1 1: × 6.667 1 1 0 0: setting prohibited 1 1 0 1: × 10.0 1 1 1 0: × 13.333 1 1 1 1: setting prohibited	R/W
b15 to b12	—	Reserved	These bits are read as 0.	R

PG0GAIN Bit (Programmable Gain Amplifier Gain Select for AN000 and AN100)
PG1GAIN Bit (Programmable Gain Amplifier Gain Select for AN001 and AN101)
PG2GAIN Bit (Programmable Gain Amplifier Gain Select for AN002 and AN102)

This register sets gain for programmable gain amplifier.

34.2.19 A/D Group Scan Priority Control Register (ADGSPMR)

Address: S12AD: ADGSPMR 0008 90FCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PGSC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	PGSC	Clock frequency setting bit when operating under group-A priority control	0: When operating under group-A priority control, frequency ratio between PCLK and ADCLK is 2:1 or 1:1. 1: When operating under group-A priority control, frequency ratio between PCLK and ADCLK is 4:1 or over.	R/W

ADGSPMR should always be accessed in 16-bits.

34.3 Operation

34.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.
A scan conversion is performed in three operating modes: single-cycle scan mode, continuous scan mode, and group scan mode. In single-cycle scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until the ADST bit in ADCSR is cleared to 0 from 1 by software. In group scan mode, the selected channels of group A and the selected channels of group B are scanned once after starting to be scanned according to the respective triggers.
In single-cycle scan mode and continuous scan mode, A/D conversion is performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for ANn channels of group A and group B selected by the ADANSA and ADANSB registers, respectively, starting from the channel with the smallest number n.
When self-diagnosis is selected, it is executed once at the beginning of each scan, and one of the three voltages internally generated in the 12-bit A/D converter is converted.
Double trigger mode is to be used with single-cycle scan mode or group scan mode. With double trigger mode being enabled, A/D conversion data of a channel selected by the DBLANS[4:0] bits in ADCSR is duplicated only if the conversion is started by any of the MTU3, GPT triggers selected by TRSA[5:0] bits in ADSTRGR.
When any of AN000 to AN002 or AN100 to AN102 channels is set by the SHANS[2:0] bits in ADSHCR so that the channel uses a channel-dedicated sample-and-hold circuit, the set analog input is sampled and held before the first A/D conversion of each scan.

34.3.2 Single-Cycle Scan Mode

34.3.2.1 Basic Operation (Channel-Dedicated Sample-and-Hold Circuits not Used)

In basic operation of single-cycle scan mode, A/D conversion is performed once on the analog input of the specified channels as below.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3, GPT), or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(3) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled).

(4) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

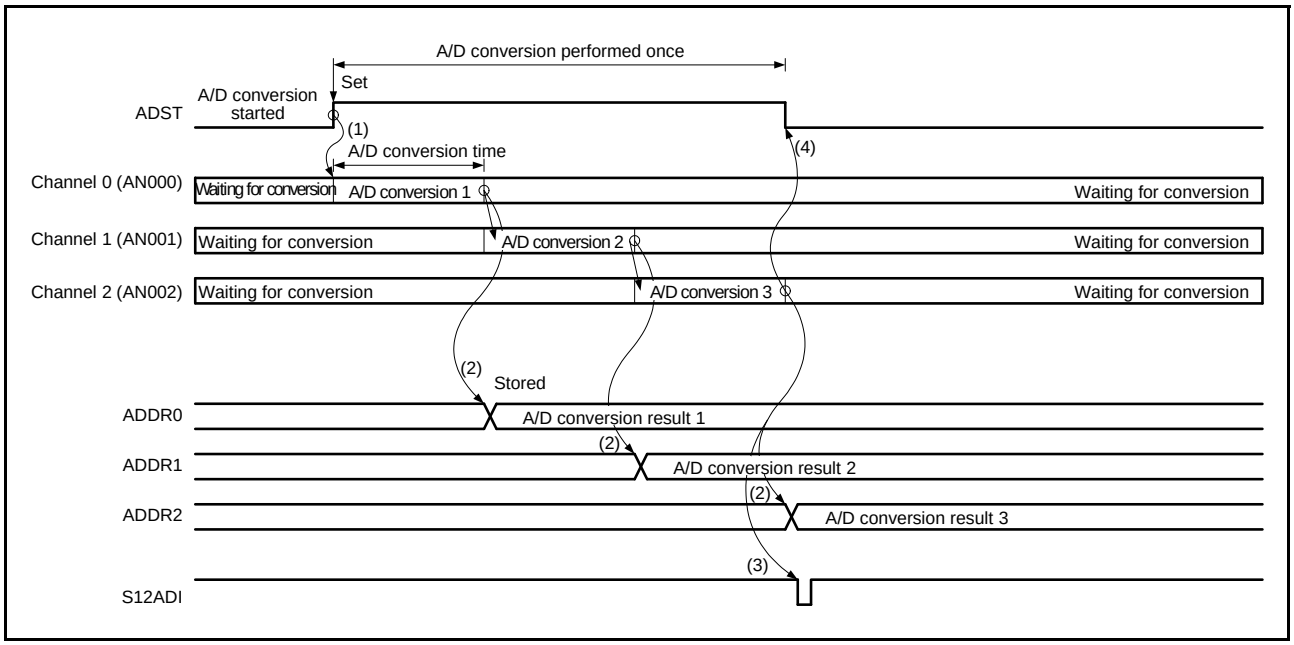


Figure 34.3 Example of Operation in Single-Cycle Scan Mode (Basic Operation: AN000 to AN002 Selected)

34.3.2.2 Basic Operation (Channel-Dedicated Sample-and-Hold Circuits Used)

When the channel-dedicated sample-and-hold circuit is used, sample-and-hold operation is first performed, and then A/D conversion is performed once on the analog input of all the selected channels as below. The channels whose channel-dedicated sample-and-hold circuit is to be used can be selected by SHANS[2:0] bits in ADSHCR.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3, GPT), or asynchronous trigger input.

(2) After sample-and-hold operation, A/D conversion is performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled).

(5) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

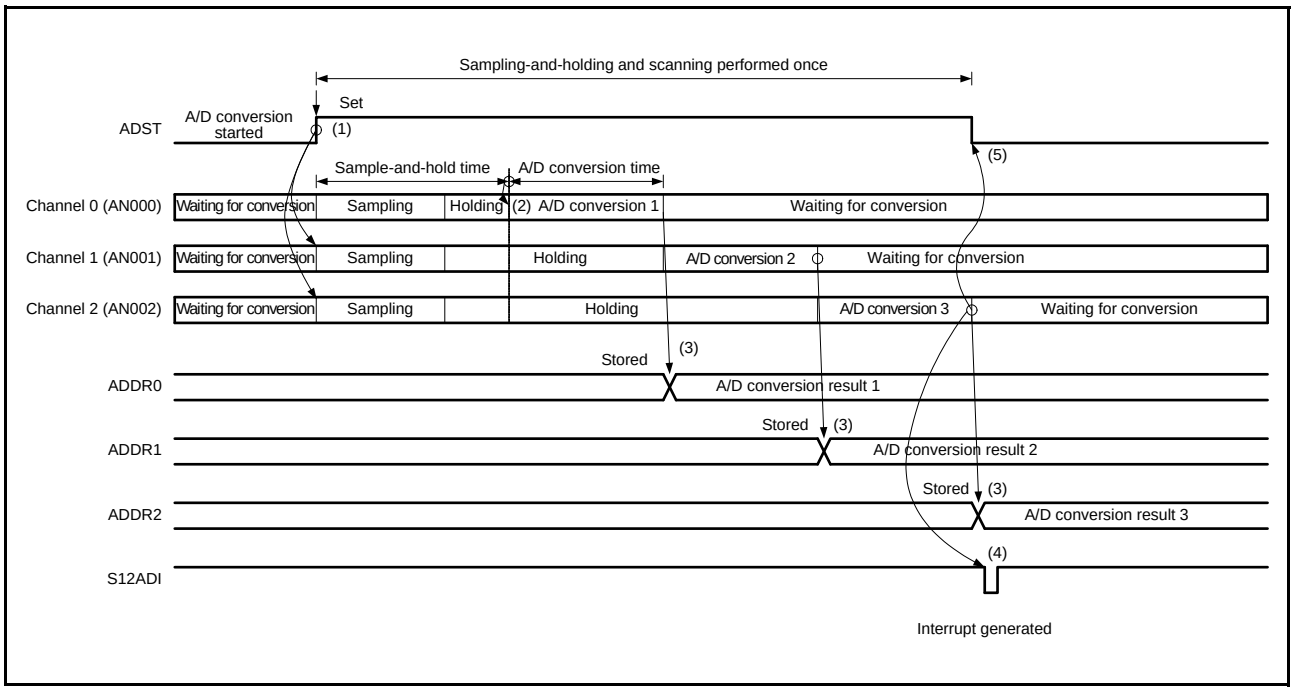


Figure 34.4 Example of Operation in Single-Cycle Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used)

34.3.2.3 Channel Selection and Self-Diagnosis (Channel-Dedicated Sample-and-Hold Circuits not Used)

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the A/D converter, and then A/D conversion is performed once on the analog input of the selected channels as below.

(1) A/D conversion for self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3, GPT), or asynchronous trigger input.

(2) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled).

(5) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

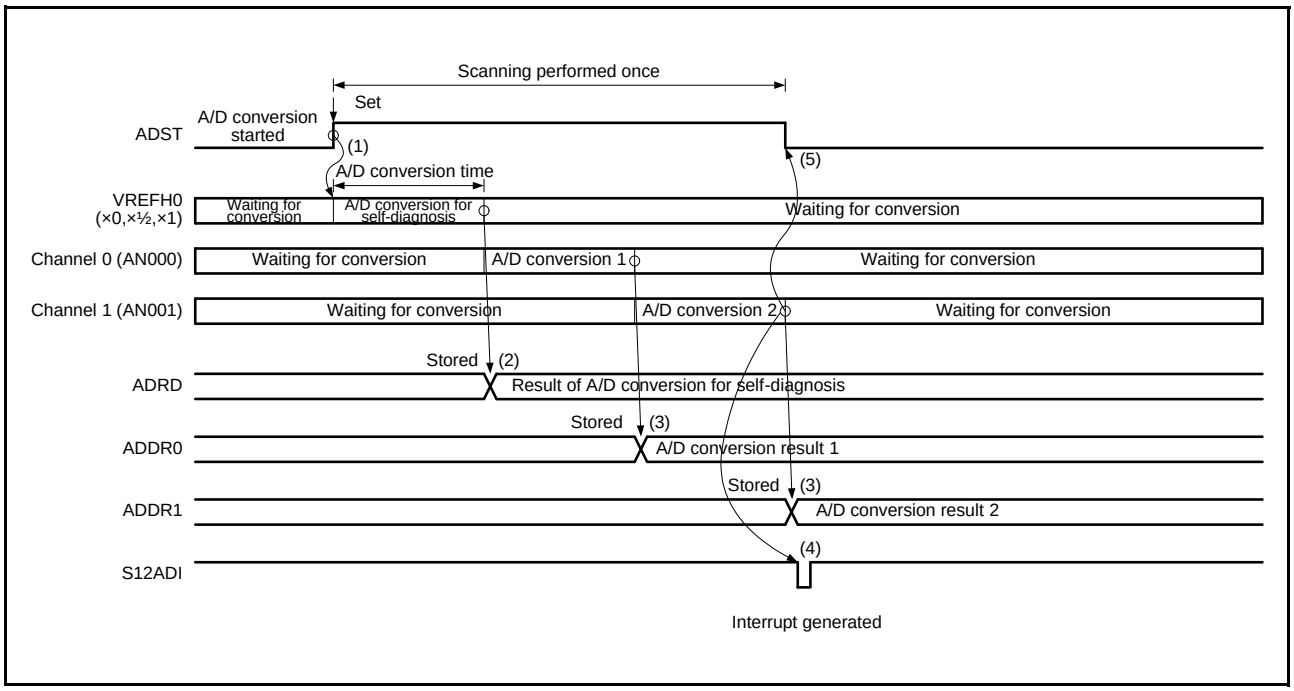


Figure 34.5 Example of Operation in Single-Cycle Scan Mode (Basic Operation + Self-Diagnosis)

34.3.2.4 Channel Selection and Self-Diagnosis (Channel-Dedicated Sample-and-Hold Circuits Used)

When the channel-dedicated sample-and-hold circuit is used and channels and self-diagnosis are selected, sample-and-hold operation is first performed, and then A/D conversion is performed once for the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the 12-bit A/D converter as below. After that, A/D conversion is performed only once on the analog input of the selected channels.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3, GPT), or asynchronous trigger input.

(2) After sample-and-hold operation, A/D conversion for self-diagnosis is started.

(3) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(4) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(5) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled).

(6) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

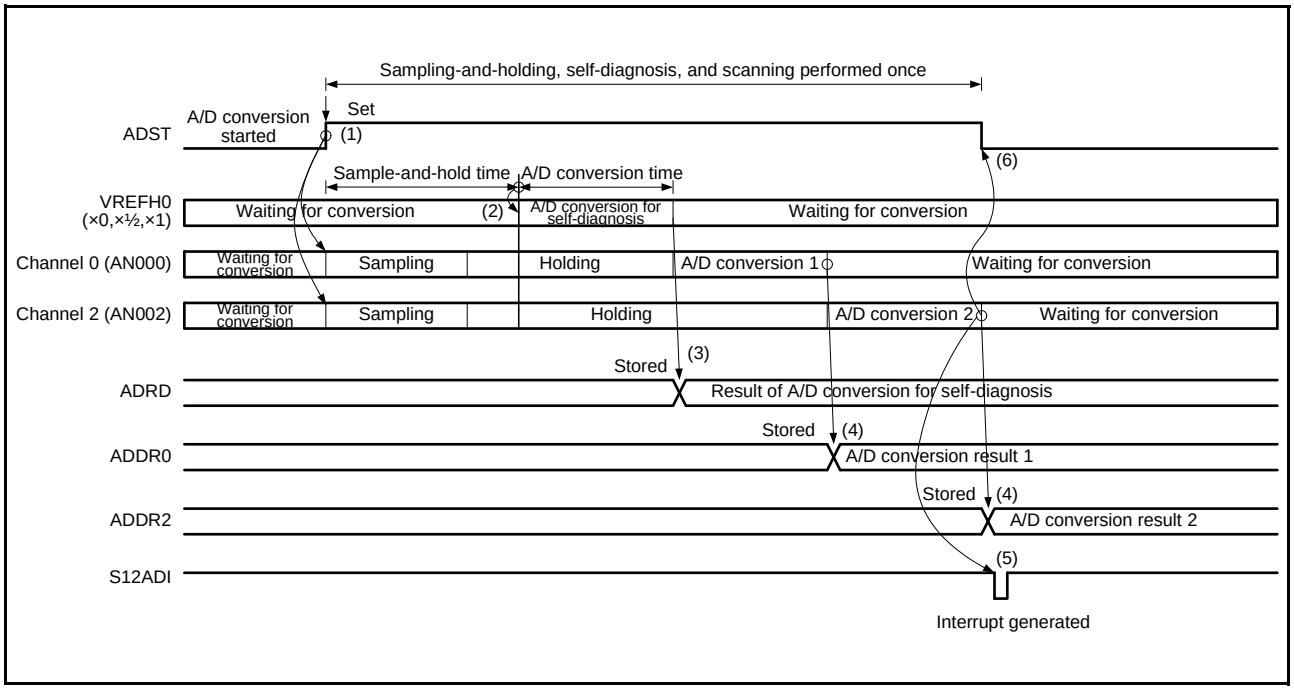


Figure 34.6 Example of Operation in Single-Cycle Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used + Self-Diagnosis)

34.3.2.5 A/D Conversion in Double Trigger Mode

In single-cycle scan mode with double trigger mode, two rounds of single-cycle scan operation started by a trigger from the MTU3, GPT are performed as a sequence as shown below.
Self-diagnosis should be deselected.
Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the DBLANS[4:0] bits in ADCSR and setting the DBLE bit in ADCSR to 1. When the DBLE bit in ADCSR is set to 1, channel selection using the ADANSA register is invalid. In double trigger mode, MTU3, GPT triggers should be selected using the TRSA[5:0] bits in ADSTRGR; the EXTRG bit and TRGE bit in ADCSR should be set to 0 and 1, respectively. Software trigger should not be used.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by the MTU3, GPT trigger input, A/D conversion is started on the single channel selected by the DBLANS[4:0] bits in ADCSR.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) The ADST bit is automatically cleared to 0 and the 12-bit A/D converter enters a wait state. Here, an S12ADI interrupt request is not generated irrespective of the ADIE (S12ADI interrupt upon scanning completion enabled) bit setting in ADCSR.
(4) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by the second trigger input, A/D conversion is started on the single channel selected by the DBLANS[4:0] bits in ADCSR.
(5) When A/D conversion is completed, the A/D conversion result is stored into the A/D data duplication register (ADDBLDR), which is exclusively used in double trigger mode.
(6) If the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled), an S12ADI interrupt request is generated.
(7) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion is completed. Then the 12-bit A/D converter enters a wait state.

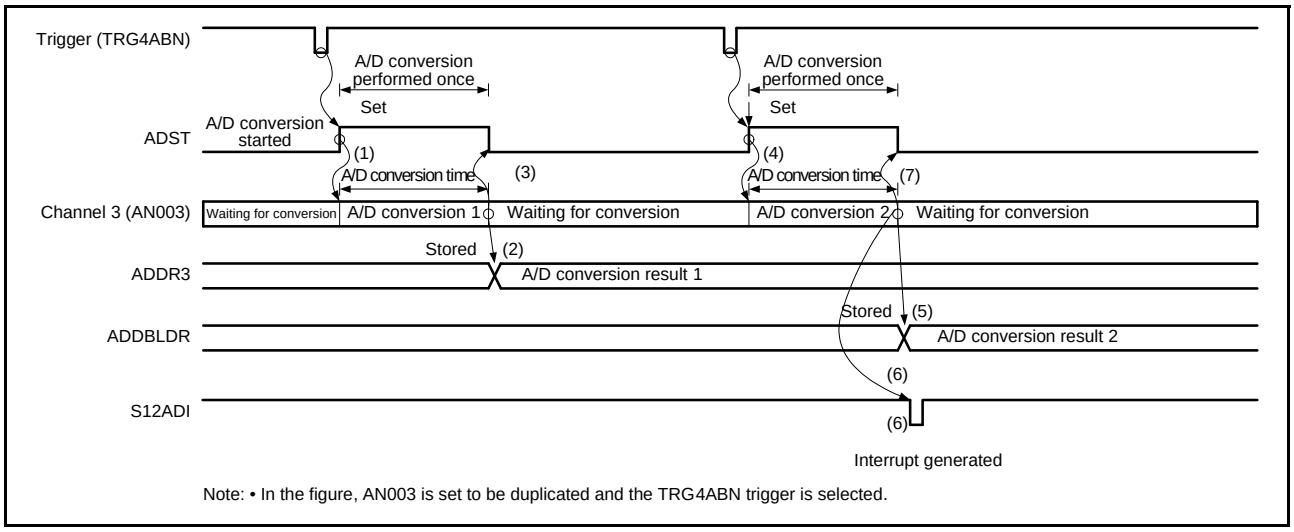


Figure 34.7 Example of Operation in Single-Cycle Scan Mode (Double Trigger Mode Selected; AN003 Duplicated)

34.3.2.6 Extended Operations When Double-Trigger Mode is Selected

If double-trigger mode is selected while the A/D converter is in single-cycle scan mode, and, as an A/D conversion start trigger, a synchronous trigger TRGnAN or TRGnBN (n = 4, 7) is selected (0Bh or 0Fh is set to ADSTRGR.TRSA[5:0]), or GTADTRAmN or GTADTRBmN (m = 0 to 7) is selected (19h, 1Ah, 1Bh, 1Ch, 25h, 26h, 27h, or 28h is set to ADSTRGR.TRSA[5:0]), the following operations are included with the operations described when double-trigger mode is selected.

When A/D conversion is started by a synchronous trigger TRGnAN (n = 4, 7) or GTADTRAmN (m = 0 to 7), the results of A/D conversion are stored in A/D data-doubling register A (ADDBLDRA).
When A/D conversion is started by a synchronous trigger TRGnBN (n = 4, 7) or GTADTRBmN (m = 0 to 7), the results of A/D conversion are stored in A/D data-doubling register B (ADDBLDRB). With the correspondence between synchronous triggers determined in this way, the target register for storing the results of A/D conversion does not depend on the order of trigger input. Results of A/D conversion are also stored in the A/D data register (ADDRy) and the A/D data-doubling register (ADDBLDR) at the same time, and this depends on the order of trigger input.

In extended double trigger mode, if two types of triggers have occurred simultaneously with TRGnAN or TRGnBN (n = 4, 7) or GTADTRAmN or GTADTRBmN (m = 0 to 7) selected, results are not sorted by the trigger sources and are stored in A/D data-doubling register B (ADDBLDRB).
Note that if a trigger source is input during A/D conversion caused by another trigger source, the former trigger source is ignored and sorting is performed by the latter trigger source.

Described below are operations performed if the first trigger is TRG4AN with the synchronous trigger TRG4AN or TRG4BN selected.

(1) A/D conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts when the TRG4AN input sets the ADCSR.ADST bit to 1 (starting A/D conversion).
(2) The result is stored in A/D data-doubling register A (ADDBLDRA) and in the corresponding A/D data register (ADDRy) on completion of the A/D conversion for the channel.
(3) The ADST bit is automatically cleared and the A/D converter enters the waiting state. An S12ADI interrupt is not generated at this time, regardless of the setting of the ADCSR.ADIE bit (i.e. whether or not this is set to enable S12ADI interrupts in response to scan completion).
(4) When the TRG4BN input sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts.
(5) The result is stored in A/D data-doubling register B (ADDBLDRB) and in the A/D data-doubling register (ADDBLDR) on completion of A/D conversion.
(6) An S12ADI interrupt request is generated if the setting of the ADCSR.ADIE bit is 1.
(7) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is cleared on completion of conversion, after which the A/D converter enters the waiting state.

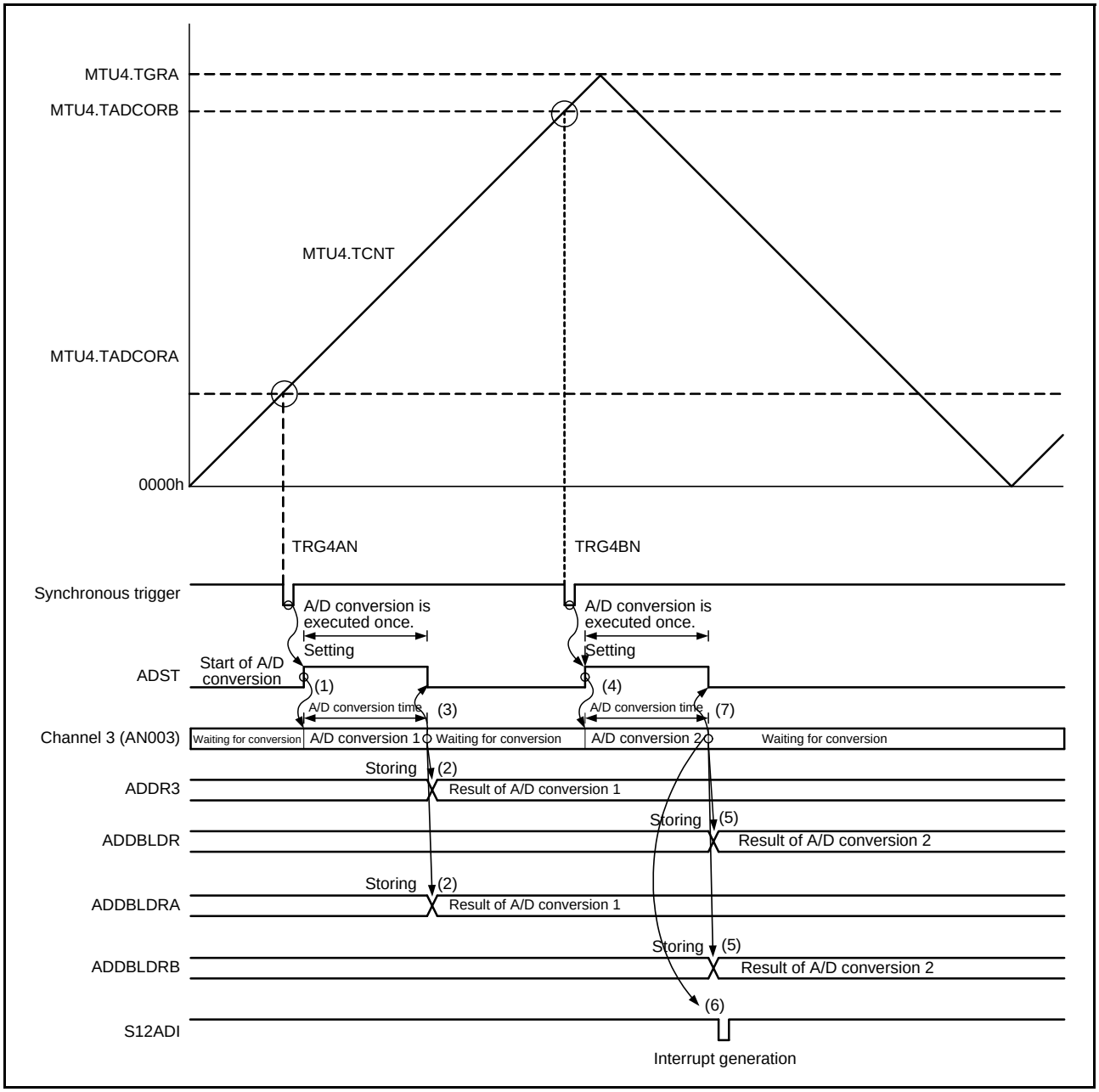


Figure 34.8 Example of Extended Operation in Double-Trigger Mode (1)
(Doubling Selected for AN003, TRG4AN or TRG4BN Selected, First Trigger is TRG4AN)

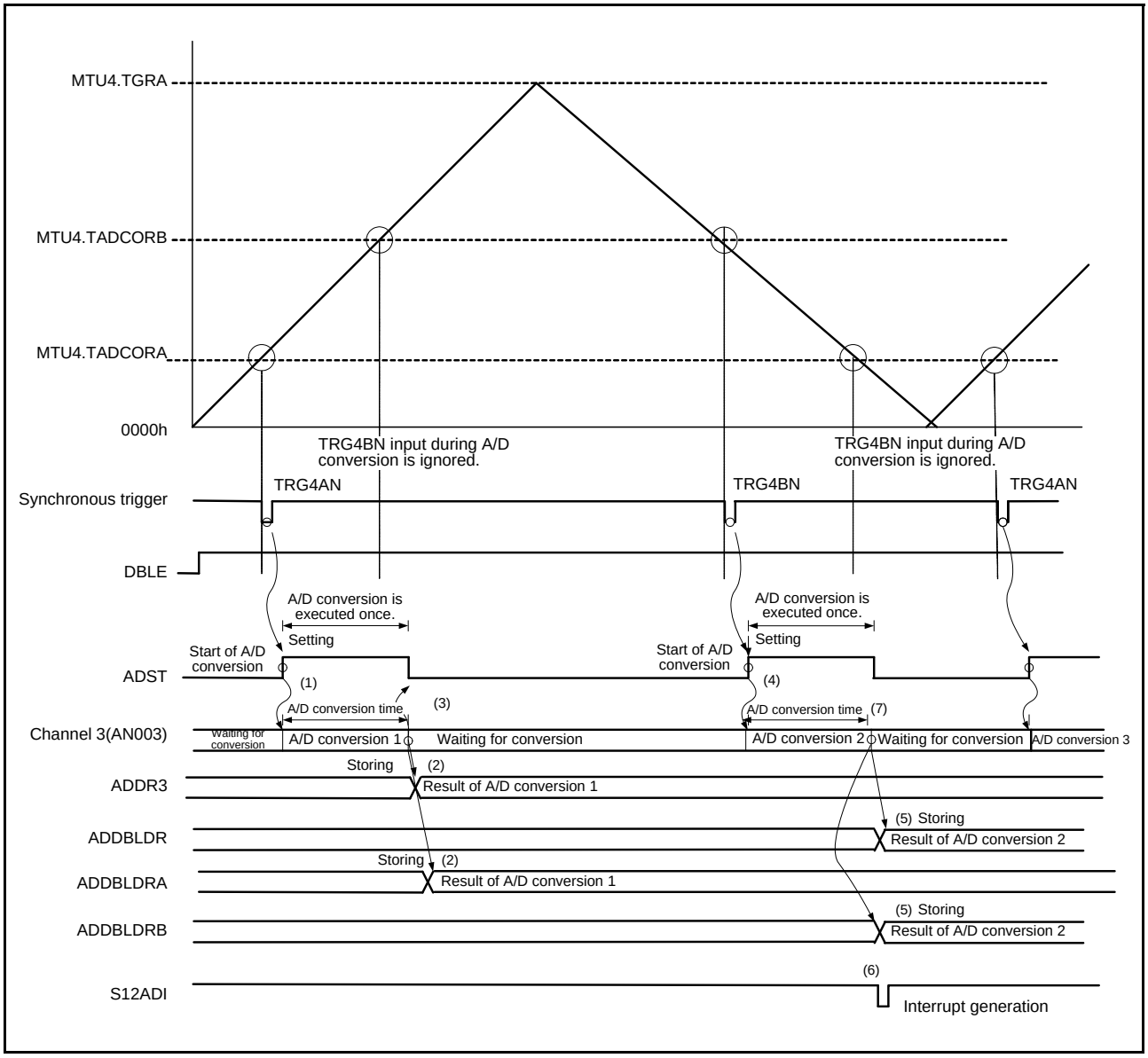


Figure 34.9 Example of Extended Operation in Double-Trigger Mode (2)
(Doubling Selected for AN003, TRG4AN and TRG4BN Selected, First Trigger is TRG4BN)

Below is a description of operations in response to TRG4BN as the first trigger, again in the case where TRGnAN or TRGnBN is selected as the synchronous trigger for the start of A/D conversion.

(1) When the TRG4BN input sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts.
(2) On completion of A/D conversion, the result is stored in A/D data-doubling register B (ADDBLDRB) and in the corresponding A/D data register (ADDRy).
(3) ADST is automatically cleared and the A/D converter enters the waiting state. An S12ADI interrupt is not generated at this time, regardless of the setting of the ADCSR.ADIE bit (i.e. whether or not this is set to enable S12ADI interrupts in response to scan completion).
(4) When the TRG4AN input sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts.
(5) On completion of A/D conversion, the result is stored in A/D data-doubling register A (ADDBLDRA) and in the A/D data-doubling register (ADDBLDR).
(6) An S12ADI interrupt request is generated if the setting of the ADCSR.ADIE bit is 1.
(7) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is cleared on completion of conversion, after which the A/D converter enters the waiting state.

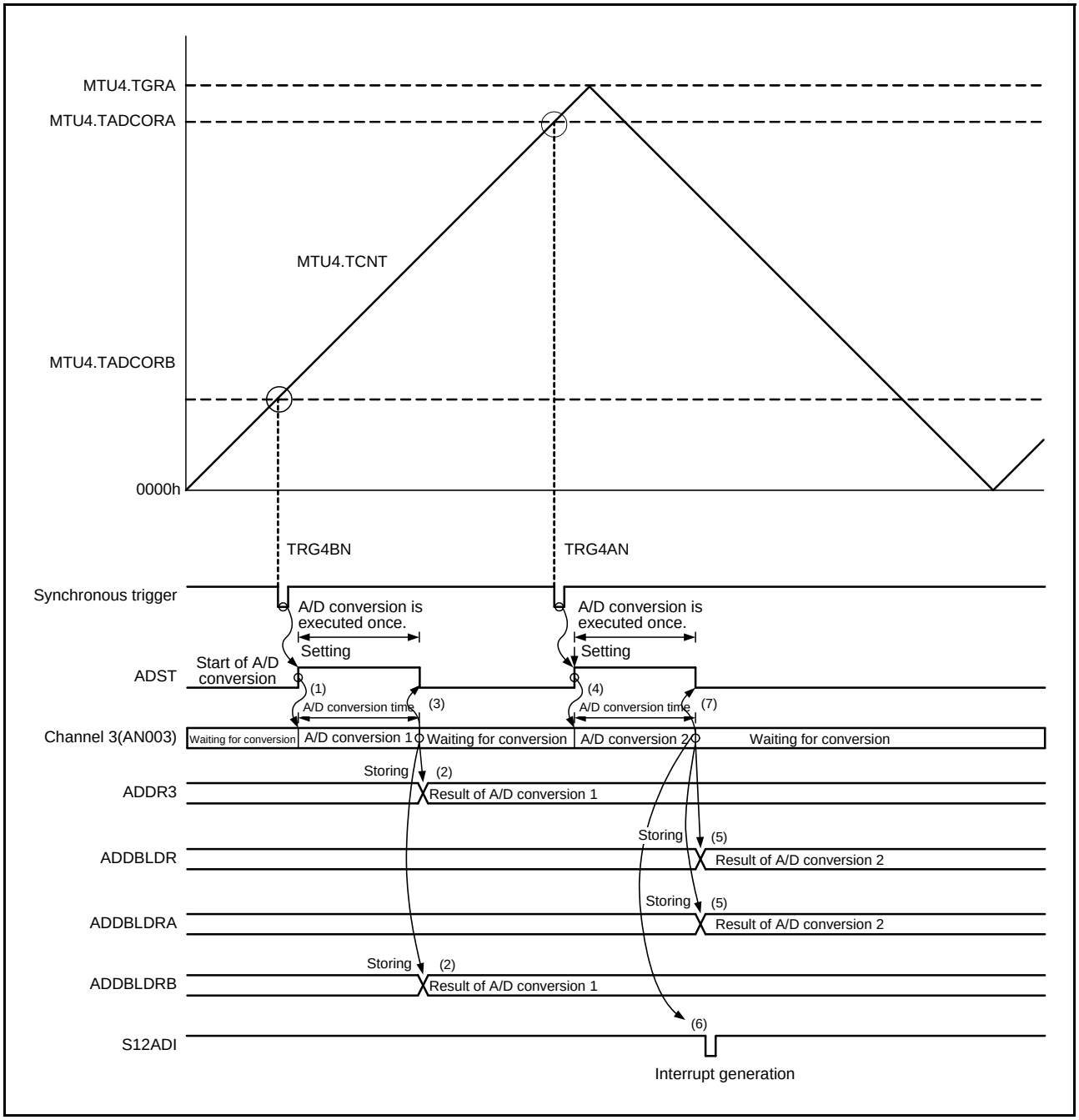


Figure 34.10 Example of Extended Operation in Double-Trigger Mode (Doubling Selected for AN003, TRG4AN and TRG4BN Selected, First Trigger is TRG4BN)

Described below are operations performed if two types of trigger sources occur with the synchronous trigger GTADTRA0N or GTADTRB0N selected as an A/D conversion trigger.

(1) The first A/D conversion on the single channel in group A selected by the ADCSR.DBLANS[4:0] bits starts when the first simultaneous input of the two trigger sources GTADTRA0N and GTADTRB0N sets the ADCSR.ADST bit to 1 (starting A/D conversion).
(2) The result is stored in A/D data-doubling register B (ADDBLDRB) and in the corresponding A/D data register (ADDRy) on completion of the A/D conversion on the channel.
(3) The ADST bit is automatically cleared and the A/D converter enters the waiting state. An S12ADI interrupt is not generated at this time, regardless of the setting of the ADCSR.ADIE bit (i.e. whether or not this is set to enable S12ADI interrupts in response to scan completion).
(4) The second A/D conversion on the single channel in group A selected by the ADCSR.DBLANS[4:0] bits starts when the second simultaneous input of the two trigger sources GTADTRA0N and GTADTRB0N sets the ADCSR.ADST bit to 1 (starting A/D conversion).
(5) The result is stored in A/D data-doubling register B (ADDBLDRB) and in A/D data-doubling register (ADDBLDR) on completion of the A/D conversion.
(6) An S12ADI interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt).
(7) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is cleared on completion of conversion, after which the converter enters the waiting state.

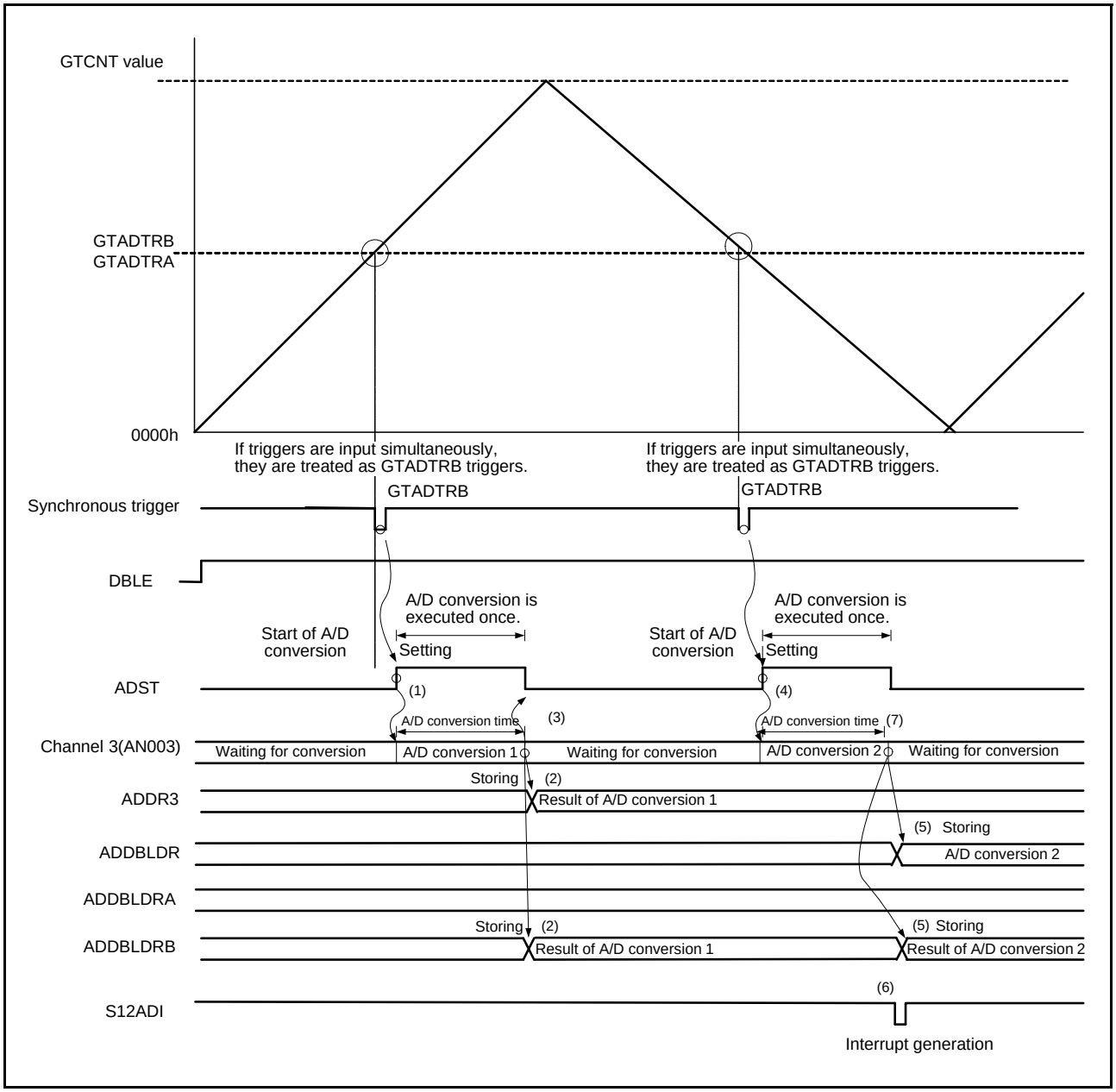


Figure 34.11 Example of Extended Operation in Double-Trigger Mode (Doubling Selected for AN003, GTADTRA0N and GTADTRB0N Selected, Two Trigger Sources Occurred Simultaneously)

34.3.3 Continuous Scan Mode

34.3.3.1 Basic Operation (Channel-Dedicated Sample-and-Hold Circuits not Used)

In basic operation of continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels as below.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3,GPT), or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(3) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion enabled).
The 12-bit A/D converter sequentially starts A/D conversion for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(4) The ADST bit in ADCSR is not automatically cleared and steps 2 and 3 are repeated as long as the bit remains 1 (A/D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.

(5) When the ADST bit is later set to 1 (A/D conversion start), A/D conversion is started again for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

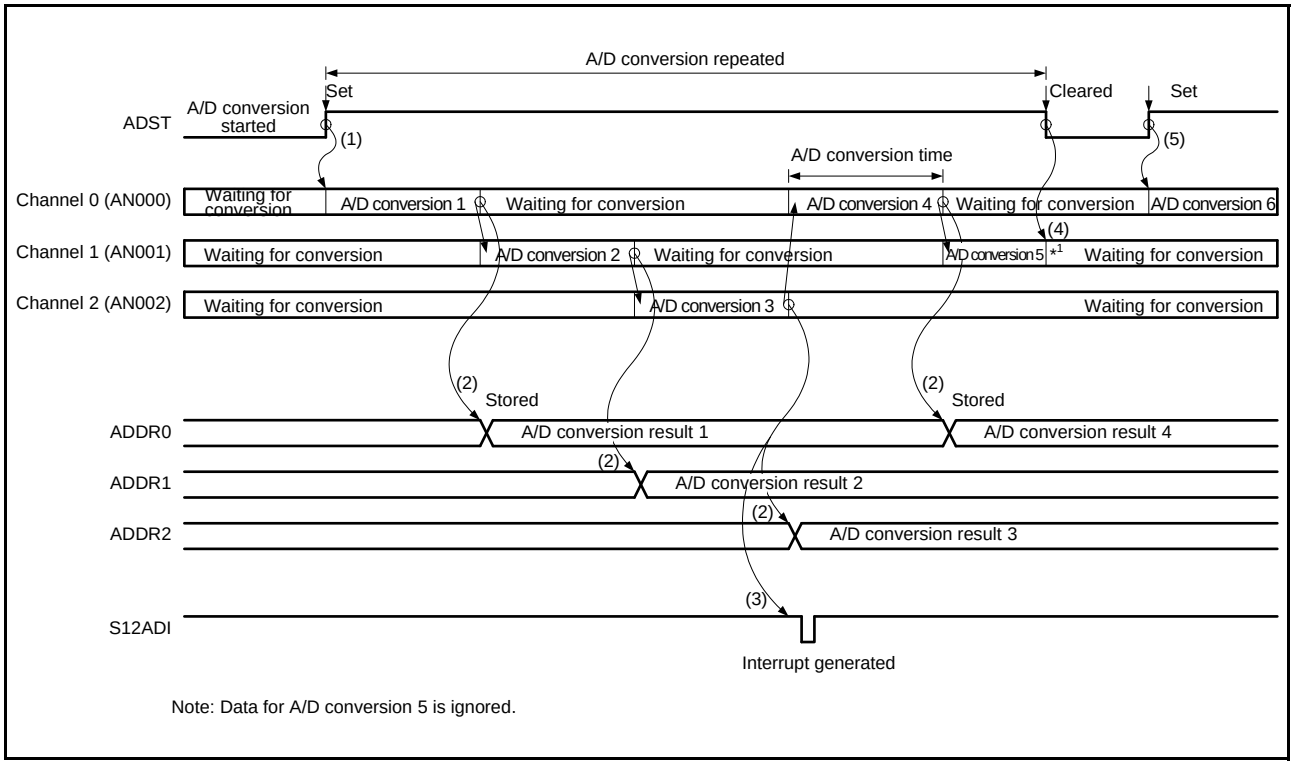


Figure 34.12 Example of Operation in Continuous Scan Mode (Basic Operation: AN000 to AN002 Selected)

34.3.3.2 Basic Operation (Channel-Dedicated Sample-and-Hold Circuits Used)

When the channel-dedicated sample-and-hold circuit is used, sample-and-hold operation is first performed, and then A/D conversion is repeated on the analog input of all the selected channels as below. The channels whose channel-dedicated sample-and-hold circuit is to be used can be selected by the SHANS[2:0] bits in ADSHCR.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software or synchronous trigger (MTU3, GPT) input.

(2) After sample-and-hold operation, A/D conversion is performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion enabled). At the same time, analog input sampling is started for all the channels whose channel-dedicated sample-and-hold circuit is to be used.

(5) The ADST bit is not automatically cleared and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.

(6) When the ADST bit is later set to 1 (A/D conversion start), analog input sampling is started again for all the channels whose channel-dedicated sample-and-hold circuit is to be used.

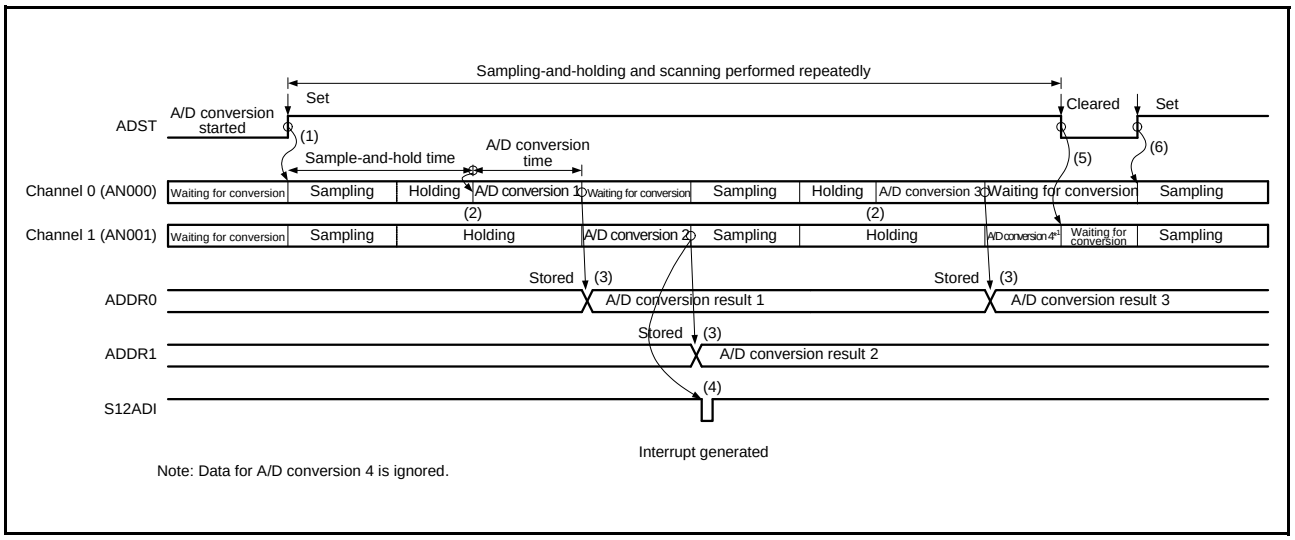


Figure 34.13 Example of Operation in Continuous Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used)

34.3.3.3 Channel Selection and Self-Diagnosis (Channel-Dedicated Sample-and-Hold Circuits not Used)

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the 12-bit A/D converter, and then A/D conversion is performed on the analog input of the selected channels, which sequence is repeated as below.

(1) A/D conversion for self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3, GPT), or asynchronous trigger input.

(2) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion enabled). At the same time, the 12-bit A/D converter starts A/D conversion for self-diagnosis and then starts A/D conversion on ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(5) The ADST bit is not automatically cleared and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.

(6) When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.

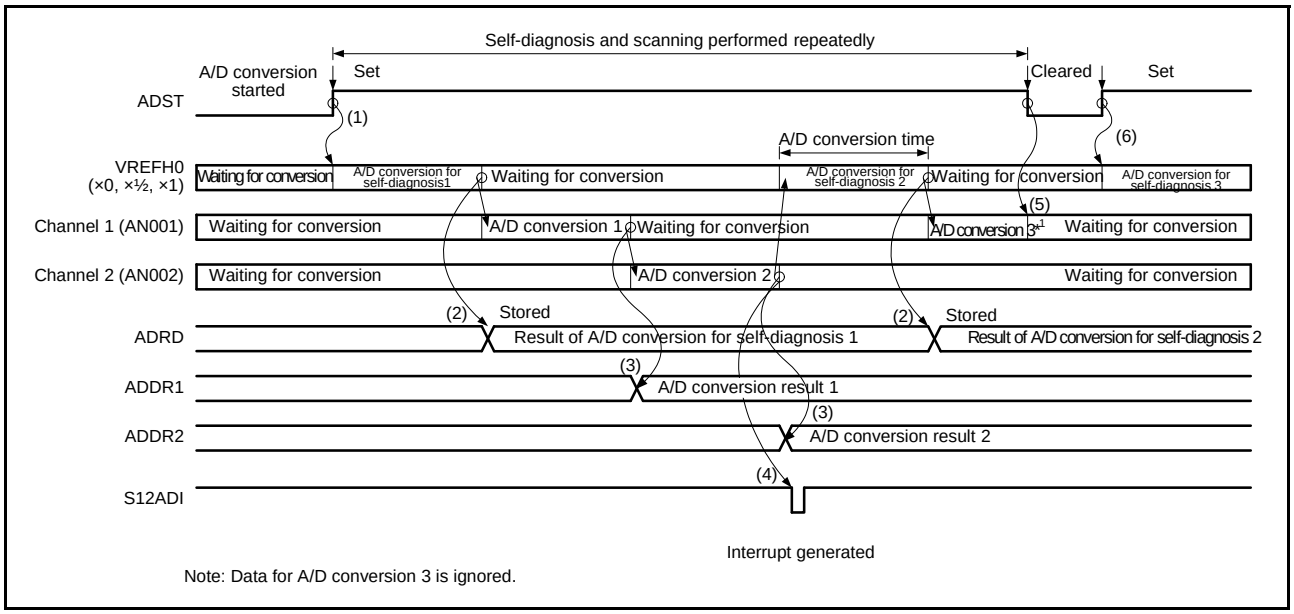


Figure 34.14 Example of Operation in Continuous Scan Mode (Basic Operation + Self-Diagnosis)

34.3.3.4 Channel Selection and Self-Diagnosis (Channel-Dedicated Sample-and-Hold Circuits Used)

When the channel-dedicated sample-and-hold circuit is used and channels and self-diagnosis are selected, sample-and-hold operation is first performed, and then A/D conversion is performed for the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the 12-bit A/D converter, and A/D conversion is performed on the analog input of the selected channels, which sequence is repeated as below.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3, GPT), or asynchronous trigger input.

(2) After sample-and-hold operation, A/D conversion for self-diagnosis is started.

(3) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(4) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(5) When A/D conversion of all the selected channels is completed, an S12ADI interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled). At the same time, analog input sampling is started for all the channels whose channel-dedicated sample-and-hold circuit is to be used.

(6) The ADST bit is not automatically cleared and steps 2 to 5 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.

(7) When the ADST bit is later set to 1 (A/D conversion start), analog input sampling is started again for all the channels whose channel-dedicated sample-and-hold circuit is to be used.

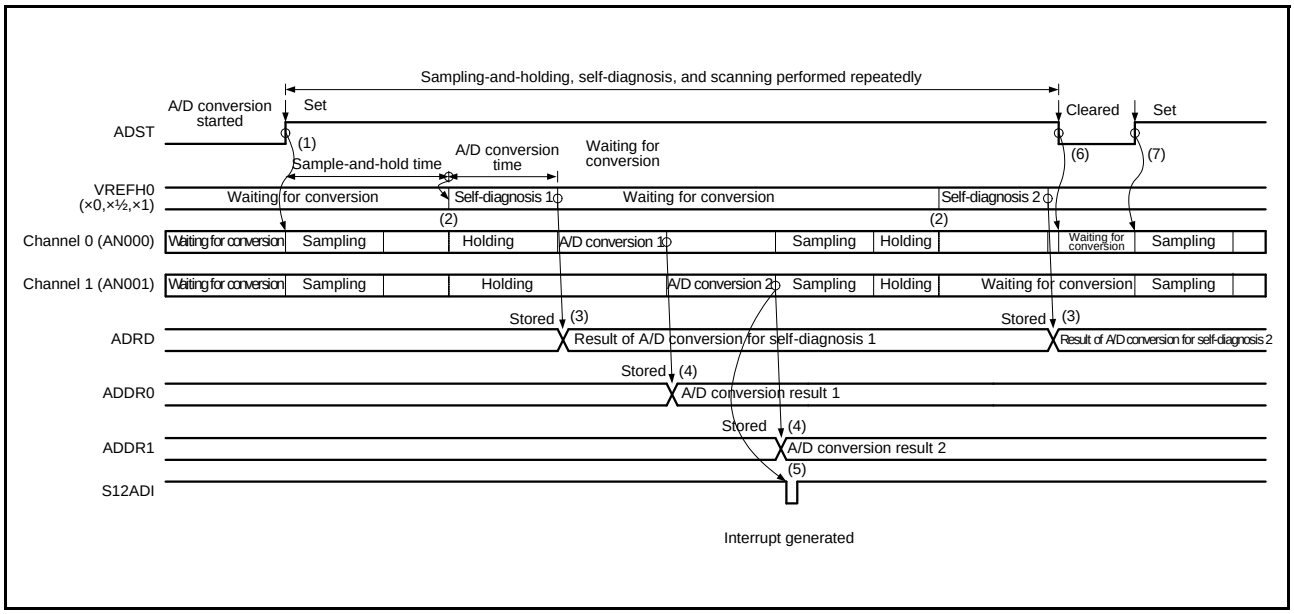


Figure 34.15 Example of Operation in Continuous Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used + Self-Diagnosis)

34.3.4 Group Scan Mode

34.3.4.1 Basic Operation

In basic operation of group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in group A and group B after scanning is started by the MTU3, GPT trigger as below. Scan operation of each group is similar to the scan operation in single-cycle scan mode.
The group A trigger and group B trigger can be selected using the TRSA[5:0] and TRSB[5:0] bits in ADSTRGR, respectively. The different triggers should be used for group A and group B to prevent simultaneous A/D conversion of group A and group B. Software trigger should not be used.
The group A and group B channels to be A/D-converted are selected using the ADANSA register and ADANSB register, respectively. Group A and group B cannot use the same channels. Channels with dedicated sample-and-hold circuits and with programmable gain amplifiers are not selectable for group B.
When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.
The following describes operation in group scan mode using a trigger from the MTU3. Specifically, the TRG4AN and TRG4BN triggers from the MTU3 are assumed to be used to start conversion of group A and group B, respectively.

(1) Scanning of group A is started by the TRG4AN trigger from the MTU3.
(2) When group A scanning is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt enabled).
(3) Scanning of group B is started by the TRG4BN trigger from the MTU3.
(4) When group B scanning is completed, an S12GBADI interrupt is generated if the GBADIE bit in ADCSR is 1 (S12GBADI interrupt enabled).

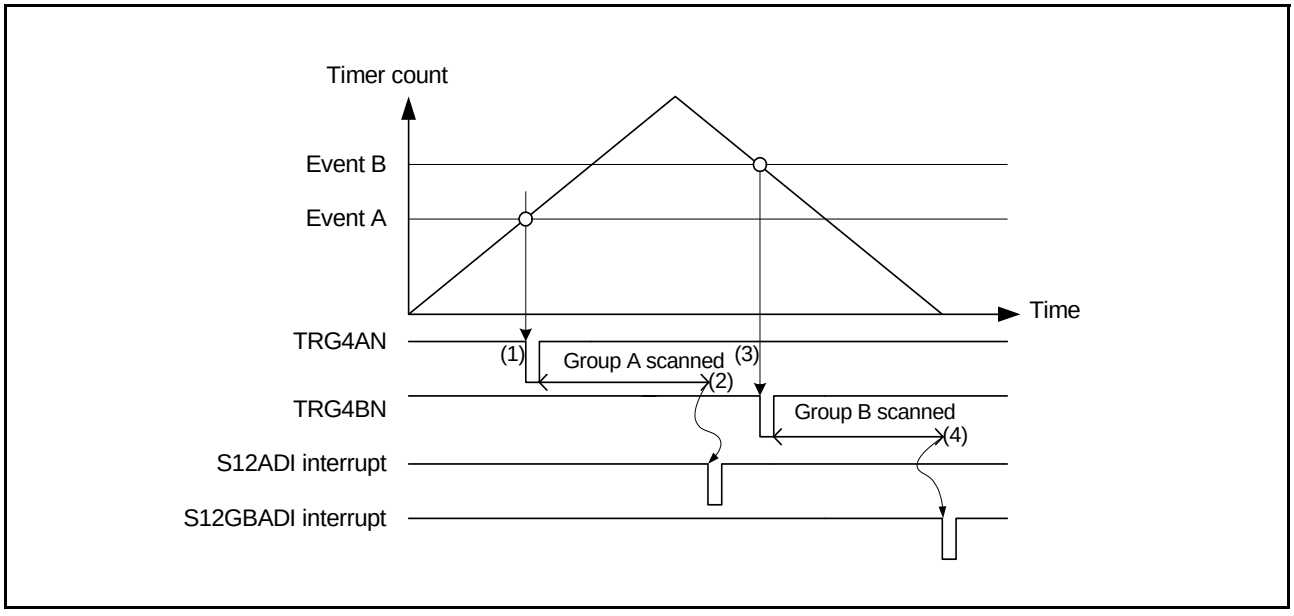


Figure 34.16 Example of Operation in Group Scan Mode (Basic Operation: MTU3 Triggers Used)

34.3.4.2 A/D Conversion in Double Trigger Mode

In group scan mode with double trigger mode, two rounds of single-cycle scan operation started by a trigger from the MTU3 or the GPT are performed as a sequence for group A. For group B, single-cycle scan operation started by a trigger from the MTU3 or the GPT is performed once.

In group scan mode, the group A trigger and group B trigger can be selected using the TRSA[5:0] and TRSB[5:0] bits in ADSTRGR, respectively. The different triggers should be used for group A and group B to prevent simultaneous A/D conversion of group A and group B. Software trigger, or asynchronous trigger (ADTRGn#) should not be used.

The group A and group B channels to be A/D-converted are selected using the DBLANS[4:0] bits in ADCSR register and ADANSB register, respectively. The same channels cannot be selected for both groups. Channels with dedicated sample-and-hold circuits and with programmable gain amplifiers are not selectable for group B.

In group scan mode with double trigger mode, self-diagnosis cannot be selected.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the DBLANS[4:0] bits in ADCSR and setting the DBLE bit in ADCSR to 1.

The following describes operation in group scan mode with double trigger mode using a trigger from the MTU3. Specifically, the TRG4ABN and TRG0AN triggers from the MTU3 are assumed to be used to start conversion of group A and group B, respectively.

(1) Scanning of group B is started by the TRG0AN trigger from the MTU3.
(2) When group B scanning is completed, an S12GBADI interrupt is generated if the GBADIE bit in ADCSR is 1 (S12GBADI interrupt enabled).
(3) The first scanning of group A is started by the first TRG4ABN trigger from the MTU3.
(4) When the first scanning of group A is completed, the conversion result is stored into ADDRy; an S12ADI interrupt request is not generated irrespective of the ADIE bit setting in ADCSR.
(5) The second scanning of group A is started by the second TRG4ABN trigger from the MTU3.
(6) When the second scanning of group A is completed, the conversion result is stored into ADDBLDR. An S12ADI interrupt is generated if the ADIE bit is 1 (S12ADI interrupt enabled).

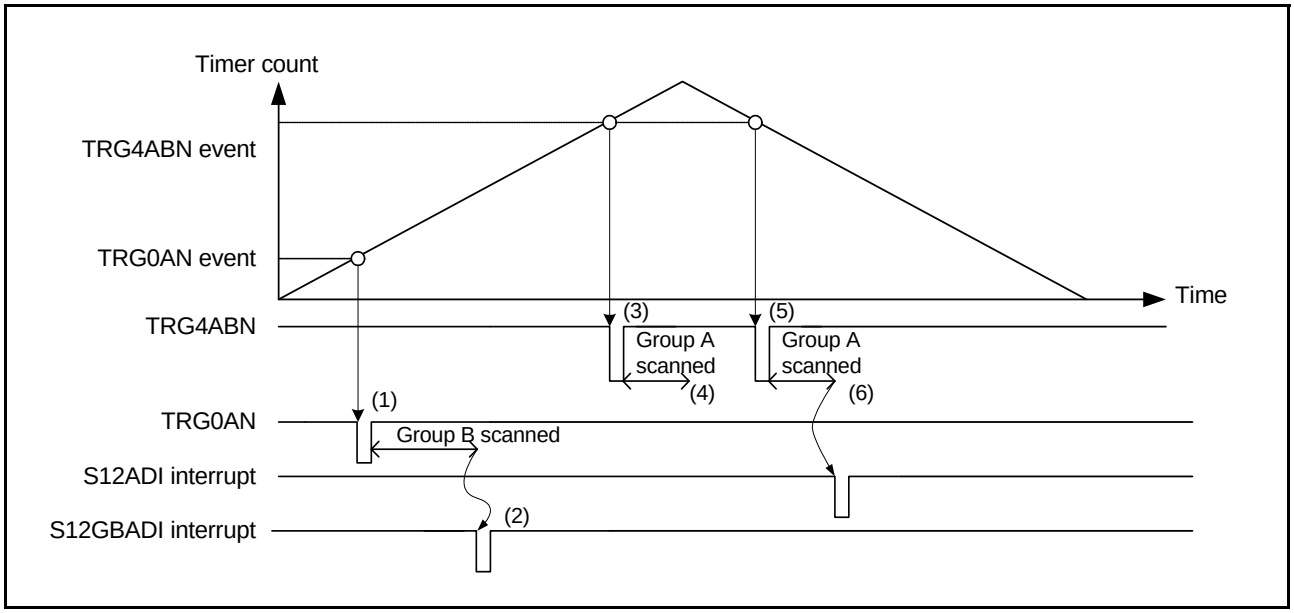


Figure 34.17 Example of Operation in Group Scan Mode with Double Trigger Mode (Basic Operation: MTU Triggers Used)

34.3.4.3 Notes on Using the Software Trigger

When a software trigger is input in double-trigger mode and scanning proceeds with the ADCSR.ADIE bit set to 1 (enabling ADI interrupts), an S12ADI interrupt is generated regardless of whether the scan is first or second in the overall order. Furthermore, doubling does not proceed in response to a software trigger, even in a case where the scan is second in the order. Figure 34.18 shows an example of why care is required in case a software trigger is input while a scan in double-trigger mode has already been started by another trigger.

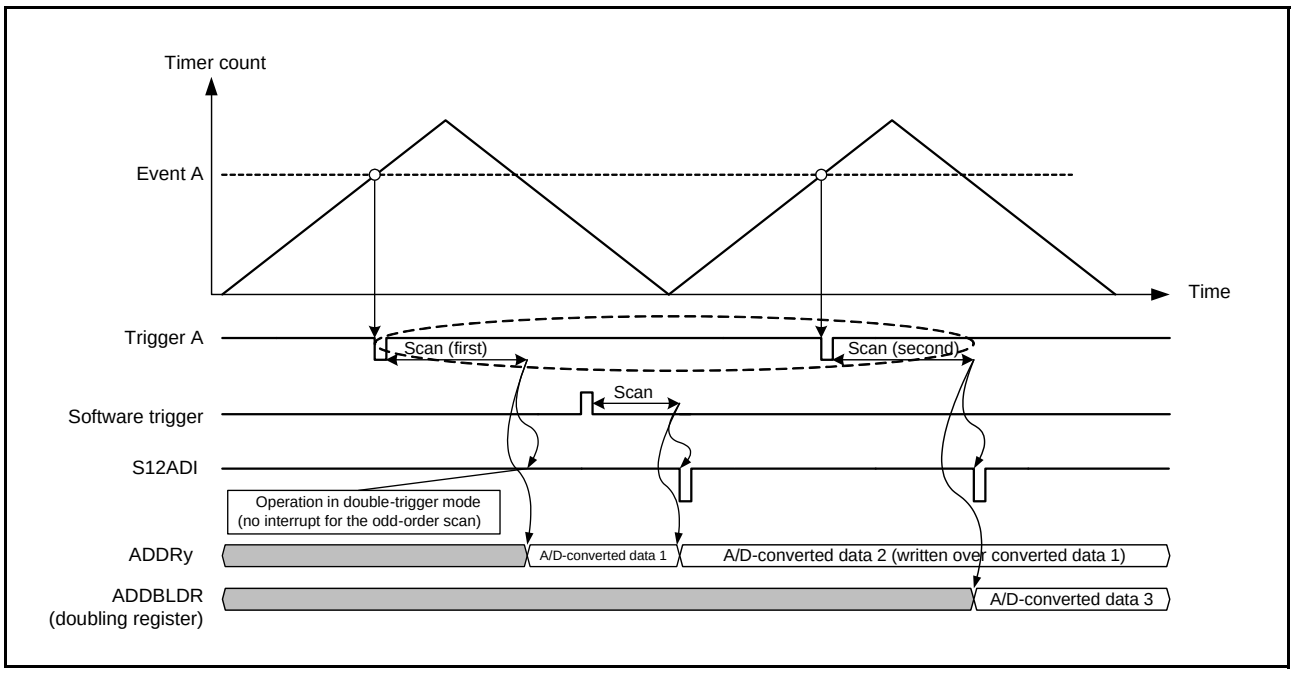


Figure 34.18 Example of Why Care is Required in Case a Software Trigger is Input During Double-Trigger Operation

34.3.4.4 Operation under Group-A Priority Control

Setting the ADGSPCR.PGS bit to 1 in group-scan mode makes operation proceed under group-A priority control. When setting the PGS bit in the ADPGSCR register to 1, follow the procedure described in Figure 34.20. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.
In operation in basic group-scan mode, input of the trigger for the other group during operation for A/D conversion in group A or group B is ignored. Under group-A priority control, if a group-A trigger is input during A/D conversion for group B, A/D conversion for group B is discontinued and A/D conversion for group A proceeds. If the setting of the ADGSPCR.GBRSCN bit is 0, the converter enters the waiting state on completion of the A/D conversion for group A. If the setting of the ADGSPCR.GBRSCN bit is 1, the converter automatically restarts scanning for group B from the head of the group. Table 34.8 describes operations in response to the input of a trigger during A/D conversion with the two settings of the ADGSPCR.GBRSCN bit.

Scan operations in group A or group B are the same in single-cycle scan mode. Furthermore, single-cycle scanning continues to proceed if the ADGSPCR.GBRP bit is set to 1 during scanning operations for group B.

For the trigger settings in group-scan mode, select a synchronous trigger for group A using the ADSTRGR.TRSA[5:0] bits and select a synchronous trigger different from that of group A for group B using the ADSTRGR.TRSB[5:0] bits. Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting the ADGSPCR.GBRP bit to 1. Furthermore, as targets for A/D conversion, select channels for group A using the ADANSA register, and for group B, select channels different from those for group A using the ADANSB register.

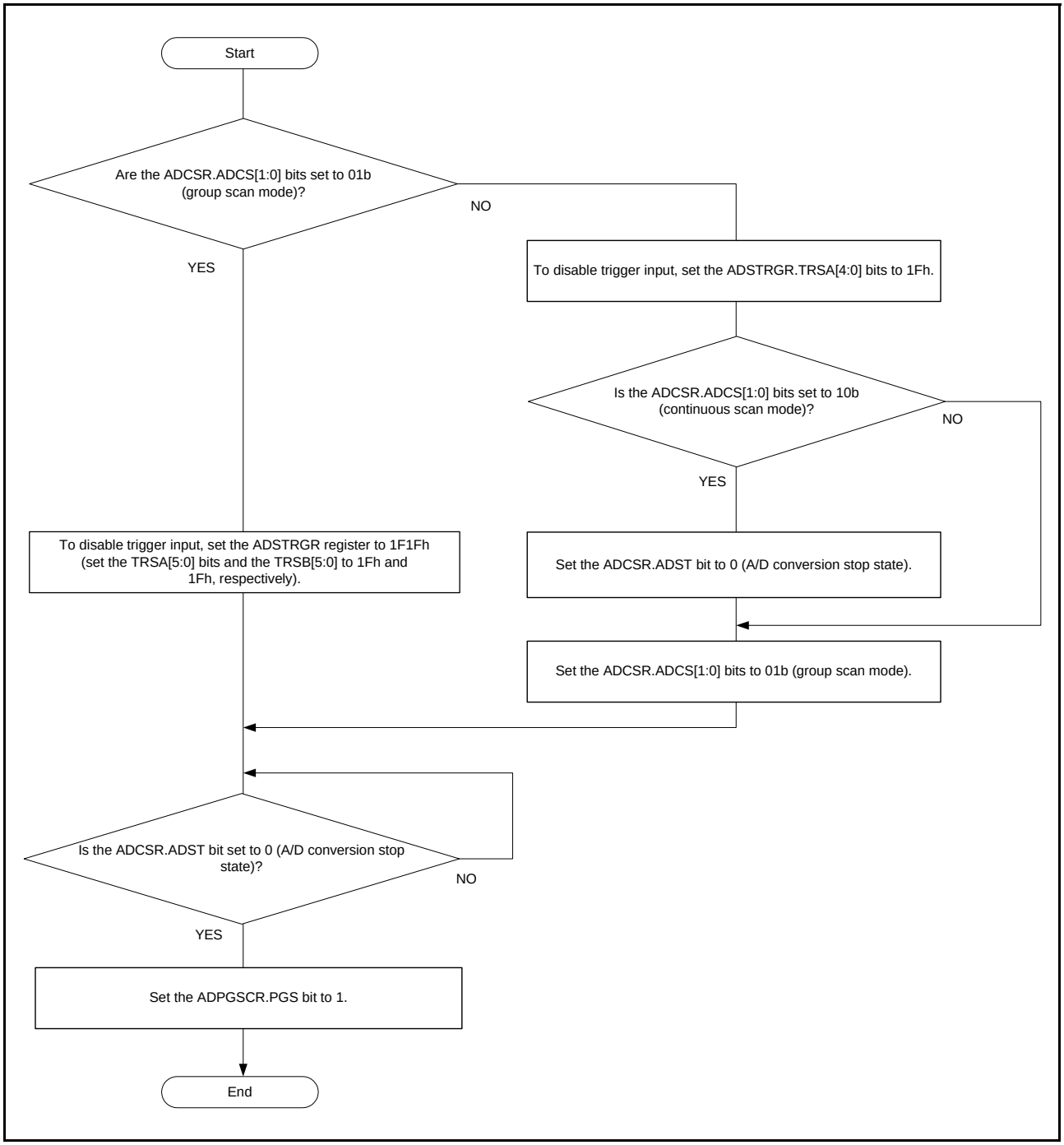


Figure 34.19 Flow of Setting the ADPGSCR.PGS Bit

Table 34.8 Control of A/D Conversion Operations According to the Settings of the ADGSPCR.GBRSCN Bit

Bit name	Trigger Input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group B	Trigger input is ineffective.	A/D conversion is performed on group B after A/D conversion on group A is completed. However, if group A triggers are input continuously, rescanning of group B is cancelled for group A and is not performed.*1
When A/D conversion for group B is in progress	Input of trigger for group A	Conversion for group B that is in progress is discontinued and conversion for group A starts.	• Conversion in progress for group B is discontinued and conversion for group A starts. • Conversion for group B starts after conversion for group A is completed.
	Input of trigger for group B	Trigger input is ineffective.	Trigger input is ineffective.

Note 1. In order to guarantee rescanning operation on group B, as the minimum interval between group A triggers, secure intervals each equal to the sum of the group A scan time (tSCAN [GrA]) and the group B scan time (tSCAN [GrB]), which total a time for two rounds of scan.
As the minimum interval between group B triggers, secure intervals each equal to the sum of the group A scan time (tSCAN [GrA]) and a time twice as long as the group B scan time (tSCAN [GrB]), which total a time for three rounds of scan.
If A/D conversion on group B is to be restarted for rescanning during A/D conversion on group A, rescanning operation is cancelled. Also, if group B is activated for rescanning at the same time when group B is activated by a trigger request, secure the trigger intervals mentioned above because the trigger request is invalidated.

Below is a description of operations in group-scan mode under group-A priority control (i.e. ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

(1) When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion, the result is stored in the corresponding A/D data register (ADDRy).
(3) The ADCSR.ADST bit is cleared on the input of a trigger for group A while operation for A/D conversion in group B is in progress, and the latter is discontinued. After that, the ADCSR.ADST bit is set to 1 (starting A/D conversion), and conversion for the ANn channels selected in the ADANSA register starts in order from the channel with the lowest number.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An ADI interrupt request (S12ADI) is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt).
(6) After the ADST bit is automatically cleared, again, the bit is automatically set to 1 (starting A/D conversion) and conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(8) An ADI interrupt request (S12GBADI) is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12GBADI interrupt).
(9) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is automatically cleared on completion of conversion, after which the A/D converter enters the waiting state.

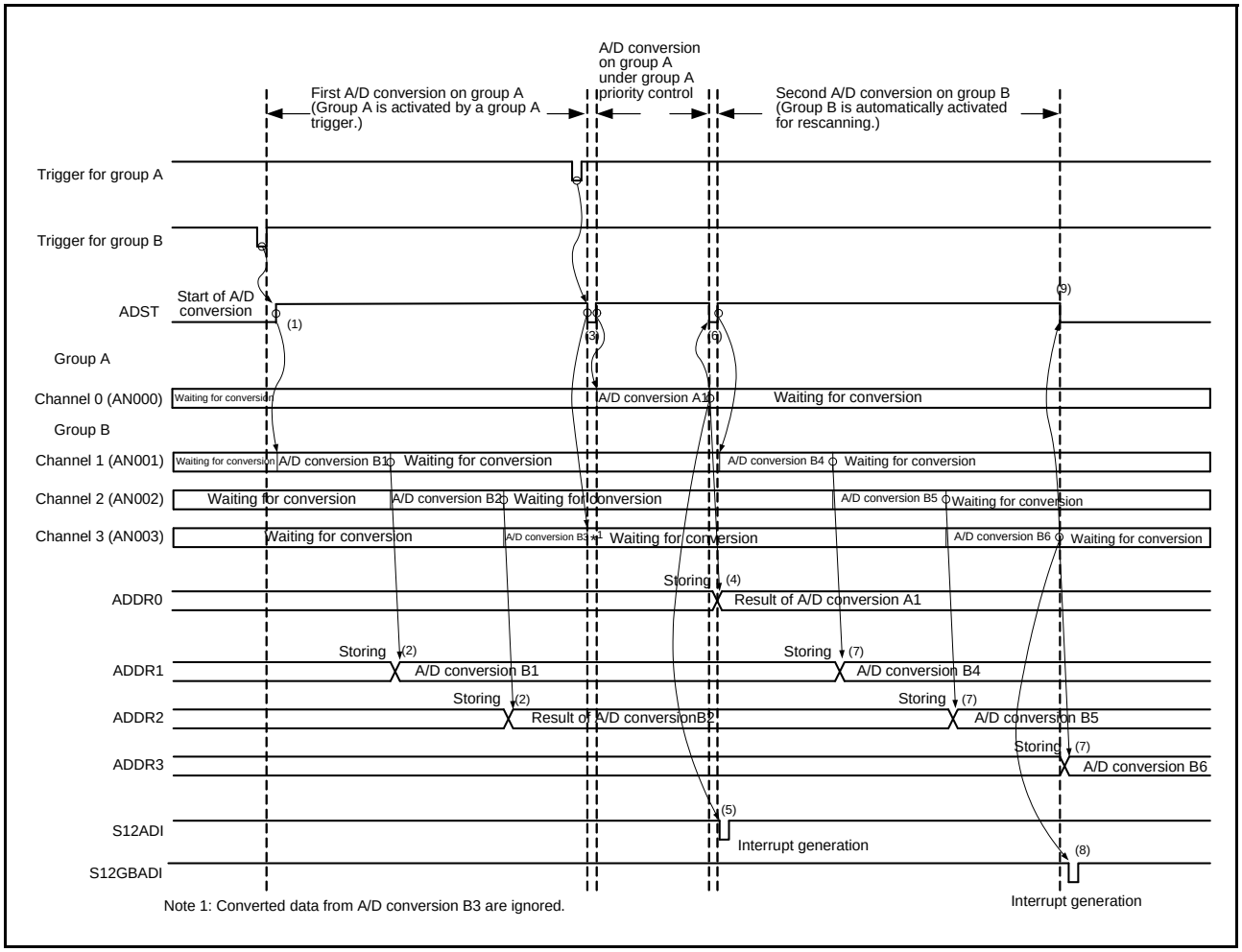


Figure 34.20 Example of Operations under Group-A Priority Control (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) (1)

Described below is an example of a rescanning operation in which a group B trigger is input during A/D conversion on group A. In this example, channels 1 to 3 are selected for group A and channel 0 is selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

(1) When input of a trigger for group A sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channels selected in the ADANSA register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group B trigger is input during A/D conversion on group A, A/D conversion on group B can be performed after the A/D conversion on group A is completed. (However, if group A triggers are input continuously, the scan operation on group B is cancelled for group A and is not performed.)
(4) On completion of the A/D conversion on the group A, an S12ADI interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt).
(5) On completion of the A/D conversion on the group A, activation of group B for rescanning sets the ADCSR.ADST bit to 1 automatically.

After that, conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number.

(6) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(7) On completion of the rescanning operation on the group B, an S12GBADI interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (enabling S12GBADI interrupt).
(8) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is automatically cleared on completion of conversion, after which the A/D converter enters a waiting state.

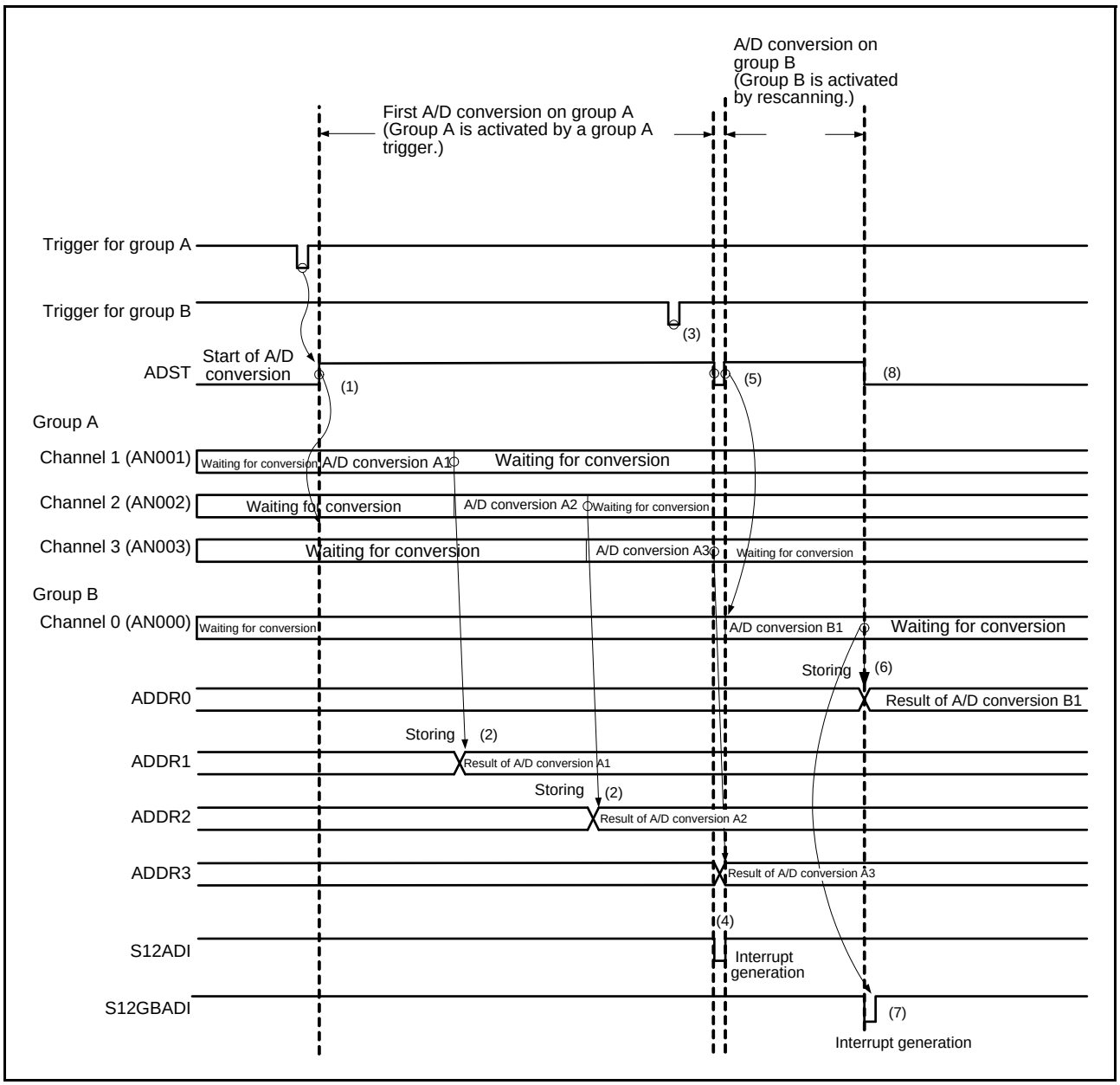
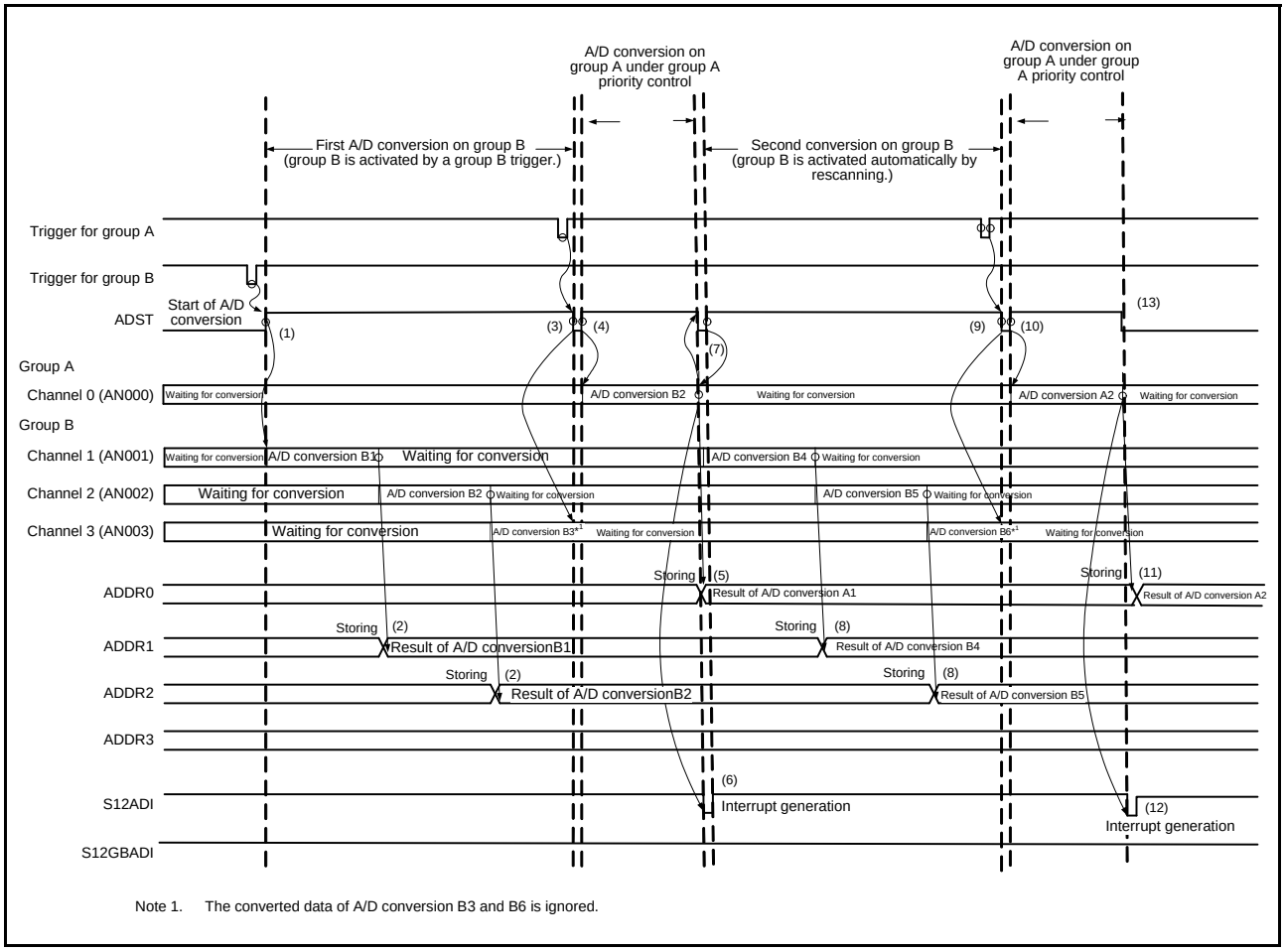


Figure 34.21 Example of Operations under Group-A Priority Control (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) (2)

Described below is an example of a rescanning operation that cannot be performed. In the example, channel 0 is selected for group A and channels 1 to 3 are selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

(1) When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group A trigger is input during A/D conversion on group B, the ADCSR.ADST bit is set to 0 (stopping A/D conversion) and the ongoing A/D conversion on group B is stopped.
(4) After that, the ADCSR.ADST bit is automatically set to 1, and conversion for the ANn channels selected in the ADANSA register starts in order from the channel with the lowest number.
(5) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(6) An S12ADI interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt).
(7) On completion of A/D conversion on the group A, rescanning operation on group B sets the ADCSR.ADST bit to 1 automatically if the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning operation). After that, A/D conversion for the ANn group B channels selected in the ADANSB register starts again in order from the channel with the lowest number.
(8) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(9) If a group A trigger is input during A/D conversion on group B for rescanning, the ADCSR.ADST bit is cleared to 0 (stopping A/D conversion) and the ongoing A/D conversion on group B is stopped.
(10) After that, the ADCSR.ADST bit is set to 1 automatically and A/D conversion for the ANn group A channels selected in the ADANSA register starts in order from the channel with the lowest number.
(11) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(12) An S12ADI interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt).
(13) After that, the ADST bit is cleared automatically and the A/D conversion is stopped. The rescanning operation on group B that has been cancelled for conversion on group A is not performed again.



Note 1. The converted data of A/D conversion B3 and B6 is ignored.

Figure 34.22 Example of Operations under Group-A Priority Control (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) (3)

Described below is an example of operation under group-A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSCR.GBRSCN = 0, ADGSCR.GBRP = 0).

(1) When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number.

(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(3) If a group A trigger is input during A/D conversion on group B, the ADCSR.ADST bit is cleared to 0 and the ongoing A/D conversion on group B is stopped. After that, the ADCSR.ADST bit is set to 1 (starting A/D conversion) and conversion for the ANn channels selected in the ADANSA register starts in order from the channel with the lowest number.

(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(5) An ADI interrupt request (S12ADI) is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt).

(6) The ADCSR.ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is cleared on completion of conversion, after which the A/D converter enters the waiting state.

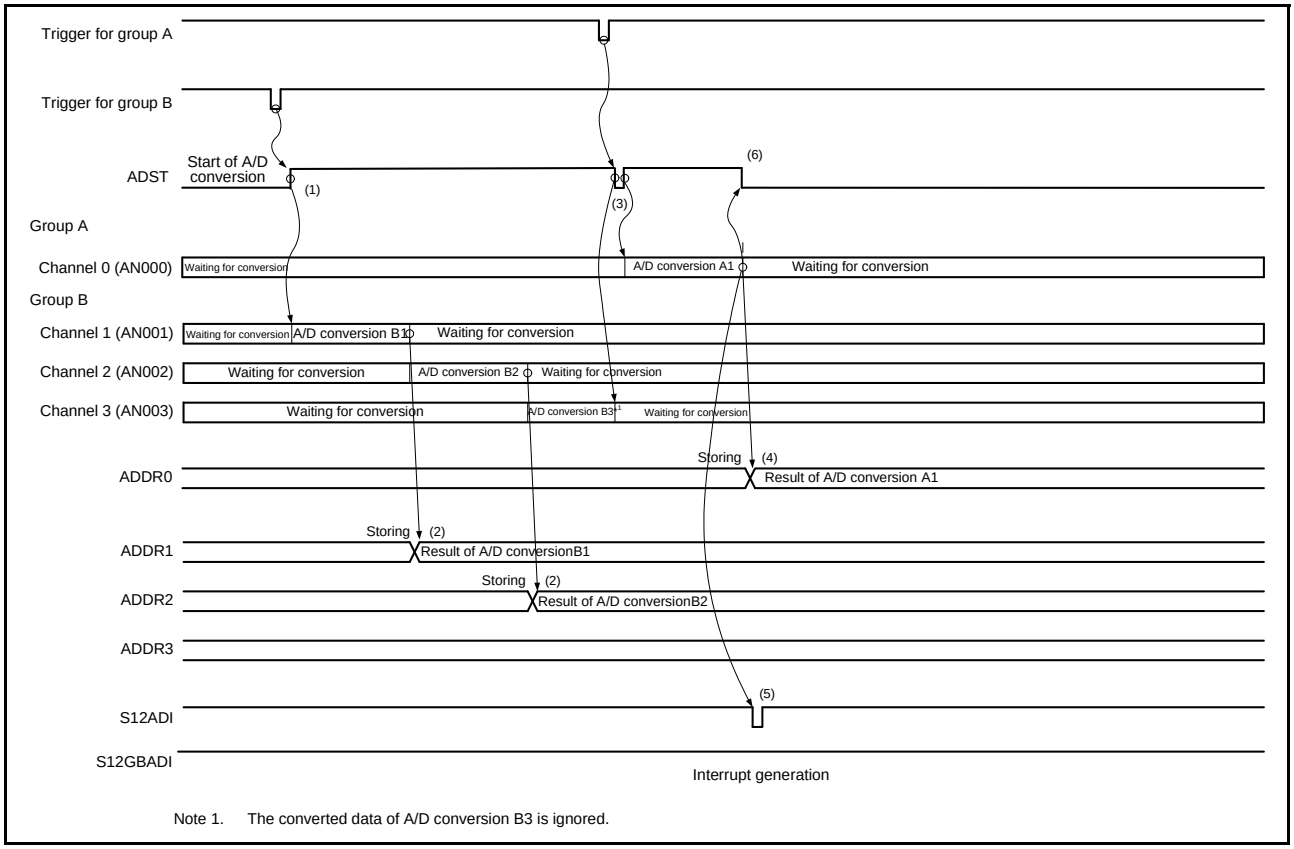


Figure 34.23 Example of Operation under Group-A Priority Control (when ADGSPCR.GBRSCN = 0 and ADGSPCR.GBRP = 0)

Described below is an example of operation under group A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSCR.GBRP = 1).

(1) The ADCSR.ADST bit is set to 1 (starting A/D conversion) when ADGSPCR.GBRP is set to 1, and conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group A trigger is input during A/D conversion on group B, the ADCSR.ADST bit is cleared to 0 and the ongoing A/D conversion on group B is stopped. After that, the ADCSR.ADST bit is set to 1 (starting A/D conversion) and conversion for the ANn channels selected in the ADANSA register starts in order from the channel with the lowest number.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An ADI interrupt request (S12ADI) is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt).
(6) After the ADST bit is automatically cleared, again, the bit is automatically set to 1 (starting A/D conversion) and conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(8) An ADI interrupt request (S12GBADI) is generated if the setting of the ADCSR. GBADIE bit is 1.

(9) After the ADST bit is automatically cleared, again, the bit is automatically set to 1 (starting A/D conversion) and conversion for the ANn channels selected in the ADANSB register starts in order from the channel with the lowest number. Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1.
Clearing of the ADCSR.ADST bit is prohibited while the ADGSPCR.GBRP bit is set to 1.
Follow the procedure for clear operation by software through the ADCSR.ADST bit, shown in Figure 34.32, if you wish to forcibly stop A/D conversion while ADGSPCR.GBRP = 1.

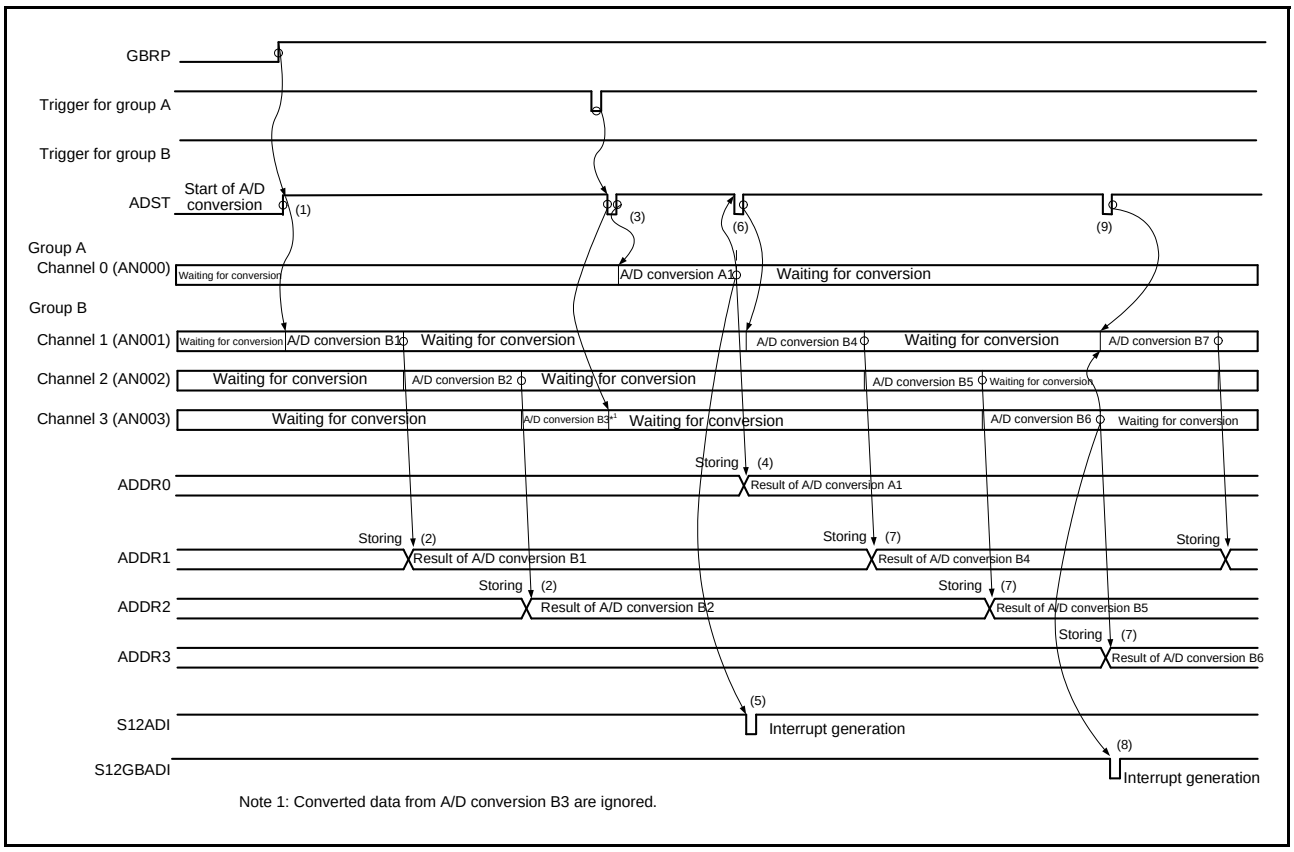


Figure 34.24 Example of Operation under Group-A Priority Control (when ADGSPCR.GBRP = 1)

34.3.5 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by software trigger; the triggers from the MTU3, GPT; or ADTRGn# (external trigger). After start-of-scanning-delay time (t_D) has passed, the A/D converter samples the channel-dedicated sample-and-hold circuits, the conversion process for self-diagnosis, and then starts the A/D conversion process.

Figure 34.25 shows the scan conversion timing in single-cycle scan mode, in which scan conversion is activated by software trigger or triggers from the MTU3, GPT. Figure 34.26 shows the scan conversion timing in single-cycle scan mode, in which scan conversion is activated by ADTRGn# (external trigger). The scan conversion time (t_{SCAN}) includes start-of-scanning-delay time (t_D), channel-dedicated sample-and-hold circuit processing time (t_{SPLSH})*1, self-diagnosis A/D conversion processing time (t_{DIAG})*2, A/D conversion processing time (t_{CONV}), channel-dedicated sample-and-hold circuit end time (t_{SHED})*3, and end-of-scanning-delay time (t_{ED}). Channel-dedicated sample-and-hold circuit processing time (t_{SPLSH}) consists of sampling time (t_{SH}) and wait time between sampling and A/D conversion (t_w). The A/D conversion processing time (t_{CONV}) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}).

The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTRn (n = 0 to 3) register.

The time for conversion by successive approximation (t_{SAM}) is fixed at 30 ADCLK states. An example of setting the ADSSTR register is provided in Table 34.10, and the scan conversion time is shown in Table 34.11.

The scan conversion time (t_{SCAN}) in single-cycle scan mode for which the number of selected channels is n can be determined as follows:

$t_{SCAN} = t_D + t_{SPLSH} + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single-cycle scan minus t_{ED} plus t_{SHED}.

The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed to $t_{SPLSH} + t_{DIAG} + (t_{CONV} \times n) + t_{SHED}$.

Note 1. When no channel-dedicated sample-and-hold circuits are used, $t_{SPLSH} = 0$.

Note 2. When the self-diagnosis function is not used, $t_{DIAG} = 0$.

Note 3. When no channel-dedicated sample-and-hold circuits are used, $t_{SHED} = 0$. Here, continuous scan mode is assumed. In single-cycle scan mode and group scan mode, t_{SHED} is included in the end-of-scanning-delay time (t_{ED}).

Table 34.9 Example of Setting the ADSSTRn Register

Use	Setting Range	Sampling Time*1
Standard (initial value)	14h	0.4µs (For PCLK = ADCLK = 50 MHz)
Use this range if there is not sufficient sampling time due to the high impedance of an analog input signal source.	15h to FF	Example: FFh 5.1µs (For PCLK = ADCLK = 50 MHz)
Use this range if ADCLK is less than 50 MHz and the sampling time needs to be less than the initial value.	0Dh to 13	Example: 10h 0.4µs (For PCLK = ADCLK = 40 MHz)

Note 1. Set the sampling time so that it is 0.4 µs or more. The sampling time is determined by the following formula.

$$\text{Sampling time (µs)} = \frac{\text{ADSSTRn register setting}}{\text{ADCLK (MHz)}}$$

Table 34.10 Times for Conversion During Scanning (in Numbers of Cycles of the ADCLK and PCLK)

Item			Symbol		Type/Conditions: Synchronous Trigger	Type/Conditions: Asynchronous Trigger	Type/Conditions: Software Trigger	Unit
Scan start processing time*1*2	A/D conversion on group A under group A priority control.	Group B is to be stopped. (Group A is activated after group B is stopped due to an A/D conversion source of group A.)	t_D		6 PCLK + 4 ADCLK	—	—	Cycle
		Group B is not to be stopped. (Activation by an A/D conversion source of group A.)			3 PCLK + 4 ADCLK	—	—	
	Other than above				2 PCLK + 4 ADCLK	4 PCLK + 4 ADCLK	2 PCLK + 4 ADCLK	
Channel-dedicated sample-and-hold processing time*1	Sampling time		t_{SPLSH}	t_{SH}	The setting of ADSHCRn.SSTSH[7:0] (initial value 14h) x ADCLK			
	Wait time between sampling and A/D Conversion			t_W	10 ADCLK			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	The setting of ADSSTRn.SSTSH[7:0] (initial value 14h) x ADCLK			
	Time for conversion by successive approximation			t_{SAM}	30 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	The setting of ADSSTRn.SSTSH[7:0] (initial value 14h) x ADCLK			
	Time for conversion by successive approximation			t_{SAM}	30 ADCLK			
Channel-dedicated sample-and-hold end processing time			t_{SHED}		2 ADCLK			
Scan end processing time *1			t_{ED}		1 PCLK + 3 ADCLK			

Note 1. Refer to Figure 34.27 and Figure 34.28 for illustration of times tD, tSPLSH, tDIAG, tCONV, and tED.
Note 2. This is the time required for execution in continuous scan mode. The time to end scanning must also be included if execution is in single-cycle scan mode or in group-scan mode. The maximum value is three cycles of the ADCLK.

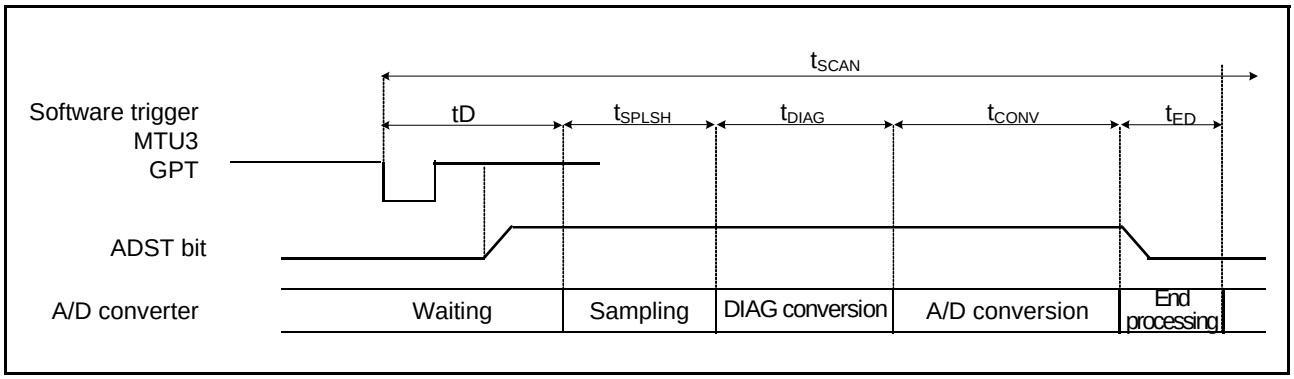


Figure 34.25 Scan Conversion Timing (Activated by Software, or Triggers from the MTU3, GPT)

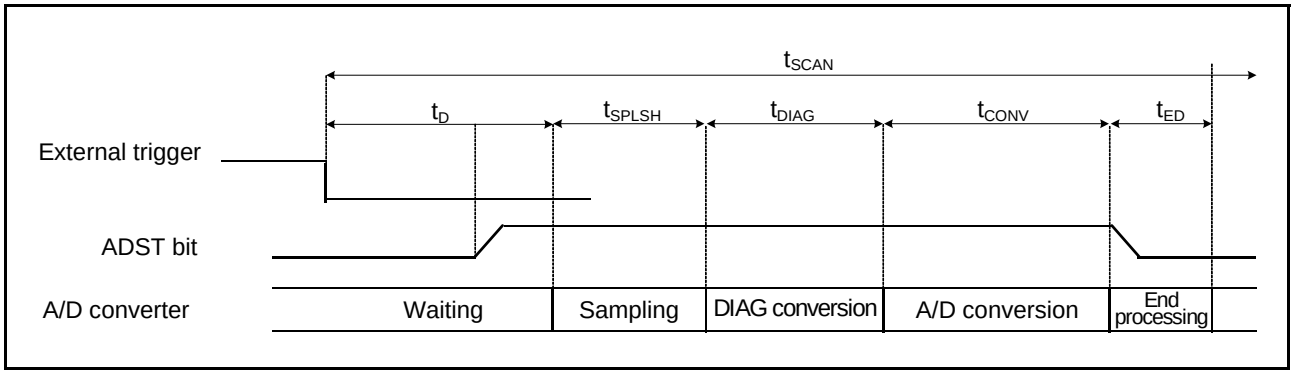


Figure 34.26 Scan Conversion Timing (Activated by ADTRG#)

34.3.6 Usage Example of Automatic Register Clearing Function

Setting the ACE bit in ADCER to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB) to 0000h when the A/D data registers are read by the CPU, DTC/DMAC tranfser. This function enables detection of update failures of the A/D data registers. The following describes the examples in which the function to automatically clear the ADDRy register is enabled and disabled.

In a case where the ACE bit in ADCER is 0 (automatic clearing is disabled), if the A/D conversion result (0222h) is not written to the ADDRy register for some reason, the old data (0111h) will be the ADDRy value. Furthermore, if this ADDRy value is written to a general register using an A/D scan end interrupt, the old data (0111h) can be saved in the general register. When checking whether there is an update failure, it is necessary to frequently save the old data in the RAM or a general register.

In a case where the ACE bit in ADCER is 1 (automatic clearing is enabled), when ADDRy = 0111h is read by the CPU, DTC, or DMACA, ADDRy is automatically cleared to 0000h. After that, if the A/D conversion result 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general register using an A/D scan end interrupt at this point, 0000h will be saved in the general register. Occurrence of an ADDRy update failure can be determined by simply checking that the read data value is 0000h.

34.3.7 A/D-Converted Value Addition Function

The same channel is A/D converted two to four consecutive times and the sum of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.

34.3.8 Discharging the Analog Pins

Discharging of the analog pins at the time of A/D conversion can be used to detect a target analog pin being open-circuit.

When the ADCER.DCE bit is set to 1, an analog pin for which conversion is in progress is only discharged after the end of sampling from the pin. If an analog pin has become open-circuit due to a malfunction, breakage, etc., the result of conversion for the pin will be 0000h after it has been discharged several times, so a pin being open-circuit is detectable.

34.3.9 Starting A/D Conversion with Asynchronous Trigger

The A/D conversion can be started by the input of an asynchronous trigger. To start up the A/D converter by an asynchronous trigger, the A/D conversion start trigger select bits (ADSTRGR.TRGA[5:0]) should be set to 00000b and a high-level signal should be input to the asynchronous trigger (ADTRG0# pin), and both the ADCSR.TRGE and ADCSR.EXTRG bits should be set to 1. Figure 34.27 shows a timing of the asynchronous trigger input.
For the time between setting the ADST bit and starting A/D conversion, refer to section 34.6.3, A/D Conversion Restarting Timing and Termination Timing.

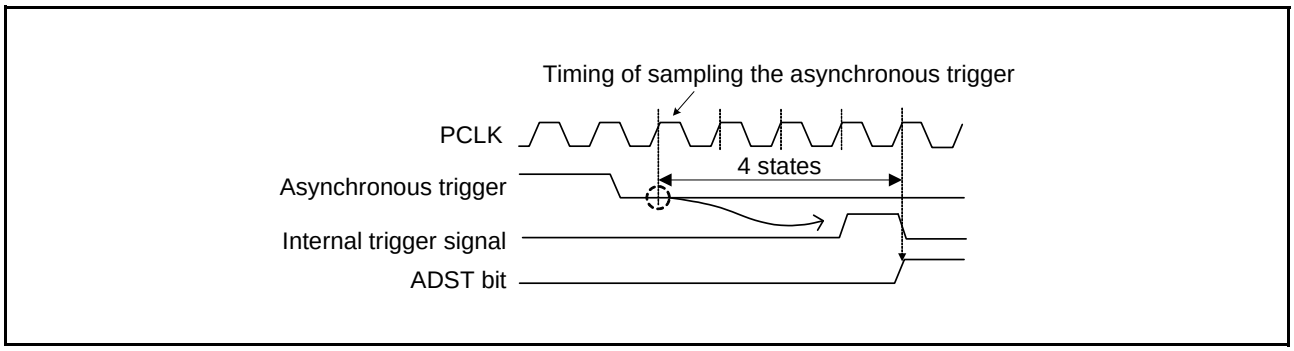


Figure 34.27 Asynchronous Trigger Input Timing

34.3.10 Starting A/D Conversion with Synchronous Trigger from Peripheral Modules

The A/D conversion can be started by a synchronous trigger of the MTU3, GPT. To start the A/D conversion by a synchronous trigger, the ADCSR.TRGE bit should be set to 1, the ADCSR.EXTRG bit should be cleared to 0, and the relevant source should be selected by ADSTRGR.TRSA[5:0] and TRSB[5:0] bits.

34.3.11 Window Comparator

The circuits for some ANn pins (those with n = 000 to 002 and 100 to 102) incorporate a window comparator. Along with the window comparator, which is capable of detecting the application to an ANn pin of voltages beyond the range from the low-side reference-voltage to the high-side reference-voltage, operation as a low-level comparator for detecting the application of any voltage lower than the low-side reference-voltage or as a high-level comparator for detecting the application of any voltage higher than the high-side reference-voltage can be selected. The operating mode of the window comparator is selected by the setting of the ADCMPMD0.CENn[1:0] bits (n = 000 to 002). Voltages that are externally supplied through the AN003/CVREFL pin for the low side and the AN103/CVREFH pin for the high side, or an internally generated reference voltage (of the form 1/8 × AVCC0 to 7/8 × AVCC0) are selectable as the reference voltages for the window comparator. A noise-cancelling filter for the detection signal from the window comparator is available for suppressing the output of false detection signals due to noise. An interrupt request for the CPU (CMPI0 to CMPI2) for the CPU or a POE signal (to place a complementary PWM output pin from the MTU3 module or a GPT output pin in the high impedance state) can be generated in response to detection by the comparator. The detection signal from the comparator is usable as a trigger to control counting by or as a source of requests for negation of an output from the general PWM timer (GPT). For details, refer to section 24, General PWM Timer (GPT).

An example of settings for the window comparator is described below.

1. Set the VSELL0 and VSELH0 bits in register ADCMPMD1 to select how the reference voltages are to be applied. When the internally generated reference voltage is selected, set the low- or high-side reference voltage by setting the REFL[2:0] and REFH[2:0] bits in ADCMPMD1.
2. Set the ADCMPNR0.CnNR[3:0] bits for the given comparator (n = 000 to 002) to determine whether or not the noise-cancelling filter will be used on the result of detection by the comparator.
3. Set the ADCMPSEL.IEn bits (n = 000 to 002) as required if an interrupt request for the CPU (CMPI0 to CMPI2) is to be generated in response to the detection signal from the comparator. Also set the ADCMPSEL.POERQm (n = 000 to 002) bits as required if a POE request is to be generated in response to the detection signal from the comparator. The POE request is generated as the logical OR of the detection signals selected by the POERQm bits.
4. Set the ADCMPMD0.CENn[1:0] (n = 000 to 002) bits to select the operating mode of the pin for use in detection and of the window comparator.

Figure 34.28 to Figure 34.30 depict examples of operation of the window comparator.

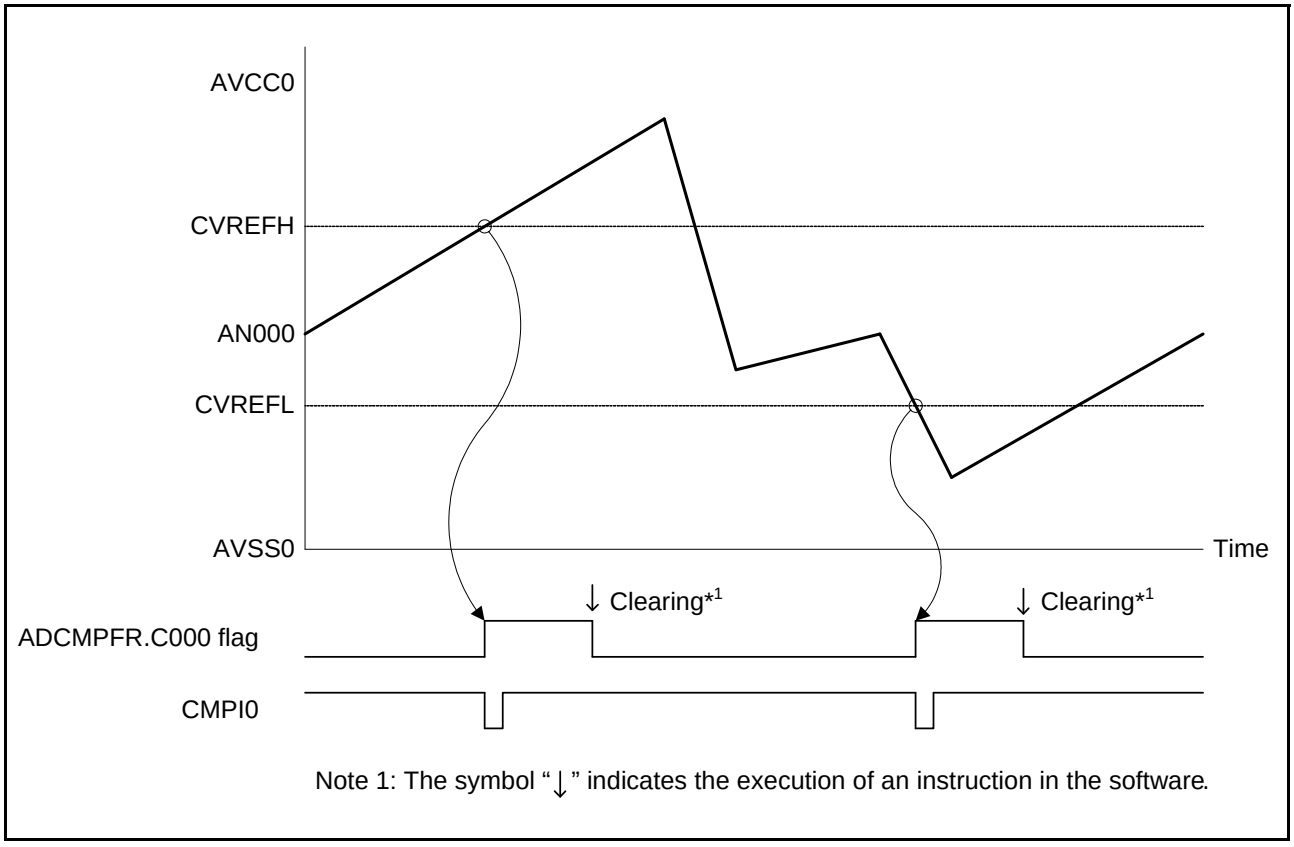


Figure 34.28 Example 1 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 11b)

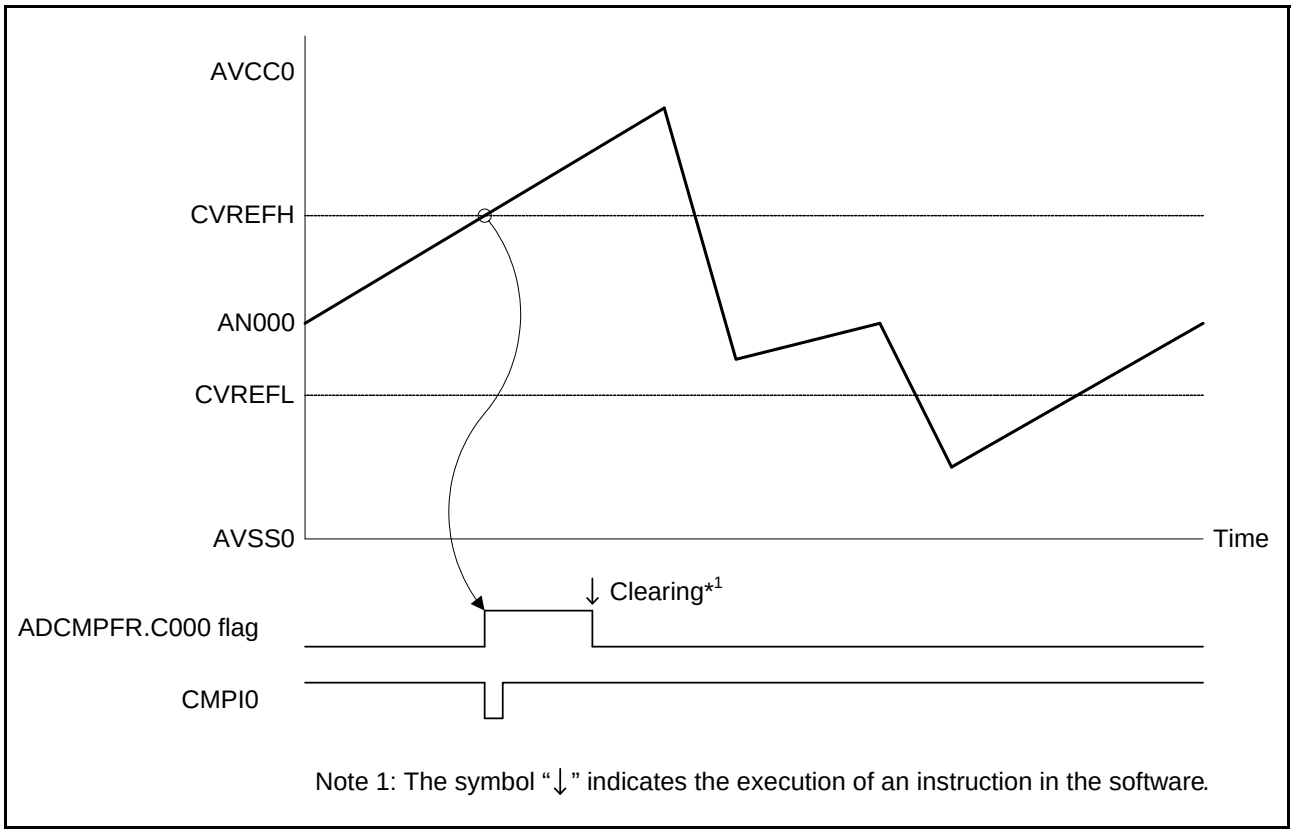


Figure 34.29 Example 2 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 10b)

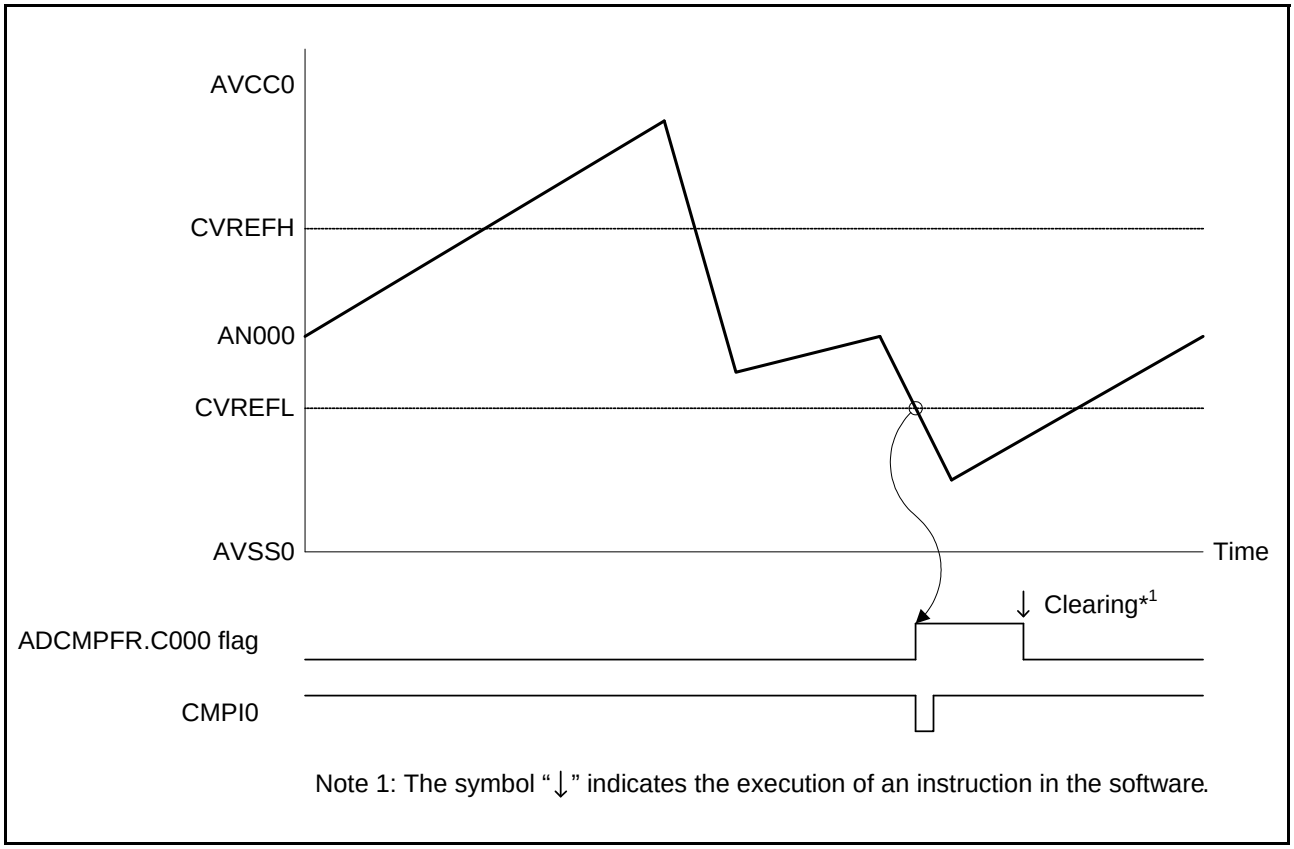


Figure 34.30 Example 3 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 01b)

34.3.12 Programmable Gain Amplifier

AN000 to AN002 and AN100 to AN102 pins incorporate a programmable gain amplifier.

Gain is selected by ADPG.PGnGAIN[3:0] bits (n = 000 to 002 and 100 to 102), and operational amplifier to be used for ADANSA.PgnEN bit and ADANSA.PGnSEL bit are selected.

To use the programmable gain amplifier, the corresponding bit of ADSHCR.SHANS[2:0] must be set to 1 (use sample-and-hold circuit).

34.4 Interrupt Sources and DMA Transfer Requests

34.4.1 Interrupt Request on Completion of Each Scanning Conversion

The 12-bit A/D converter can send scan end interrupt requests S12ADI and S12GBADI to the CPU.
Setting the ADCSR.ADIE bit to 1 and 0 enables and disables an S12ADI interrupt, respectively; similarly, setting the ADCSR.GBADIE bit to 1 and 0 enables and disables an S12GBADI interrupt, respectively.
In addition, the DTC or DMACA can be started up when an S12ADI or an S12GBADI interrupt is generated. Using an S12ADI or an S12GBADI interrupt to allow the DTC or DMACA to read the converted data enables continuous conversion without burden on software.
For details on DTC settings, see section 19, Data Transfer Controller (DTCa), and for details on DMACA settings, see section 18, DMA Controller (DMACA).

34.4.2 Interrupt Requests at the Time of Detection by the Comparator

The comparator is capable of generating interrupt requests for the CPU (CMPm, where m = 0 to 2, 4 to 6) in response to detection. Setting the ADCMPSEL.IEn (n = 000 to 002) to 1 or 0 respectively enables or disables the CMPm interrupt. Furthermore, the DTC or DMACA can be activated at the time of CMPm interrupt. See section 19, Data Transfer Controller (DTCa), for the DTC settings and section 18, DMA Controller (DMACA), for the DMACA settings.

34.5 A/D Conversion Accuracy Definitions

The RX63T Group's A/D conversion accuracy is defined as below:

- Resolution
  The number of 12-bit A/D converter digital output codes
- Offset error
  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 000000000000 to 000000000001, excluding quantization error. (Figure 34.31)
- Full-scale error
  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 111111111110 to 111111111111, excluding quantization error. (Figure 34.31)
- Quantization error
  The deviation inherent in the 12-bit A/D converter, given by 1/2 LSB (Figure 34.31)
- Nonlinearity error
  The error with respect to the ideal A/D conversion characteristic between zero voltage and the full-scale error, excluding offset error, full-scale error, and quantization error. (Figure 34.31)
- Absolute accuracy
  The deviation between the digital value and analog input value, including offset error, full-scale error, quantization error, and nonlinearity error.

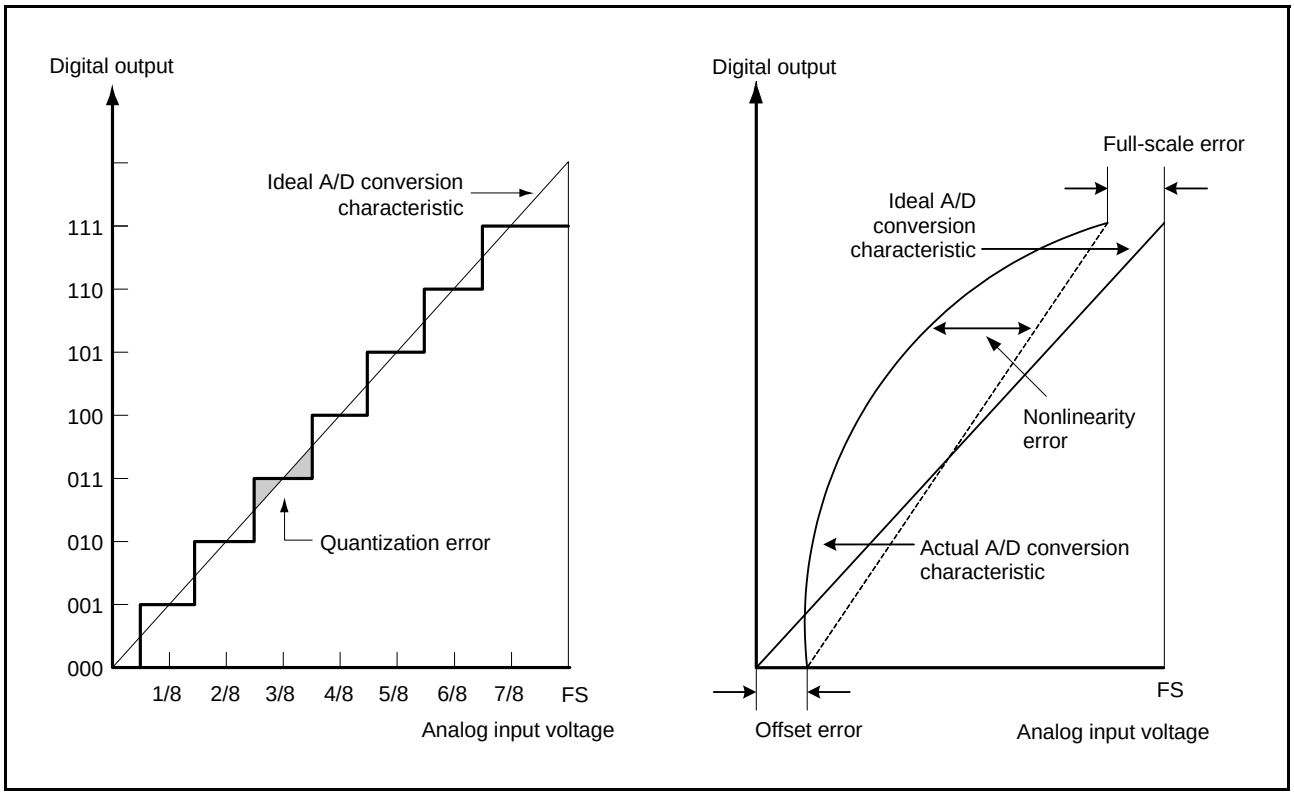


Figure 34.31 Definition of A/D Conversion Accuracy (Example of 3-Bit A/D Converter)

34.6 Usage Notes

34.6.1 Notes on Reading Data registers

The A/D data registers, A/D data duplication register, and A/D self-diagnosis data register should be read in word units. If a register is read twice in byte units, that is, the upper byte and lower byte are separately read, the A/D converted value having been read first may disagree with the A/D converted value having been read for the second time. To prevent this, the data registers should never be read in byte units.

34.6.2 Notes on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger has been selected as the condition for starting A/D conversion, follow the procedure in Figure 34.32.

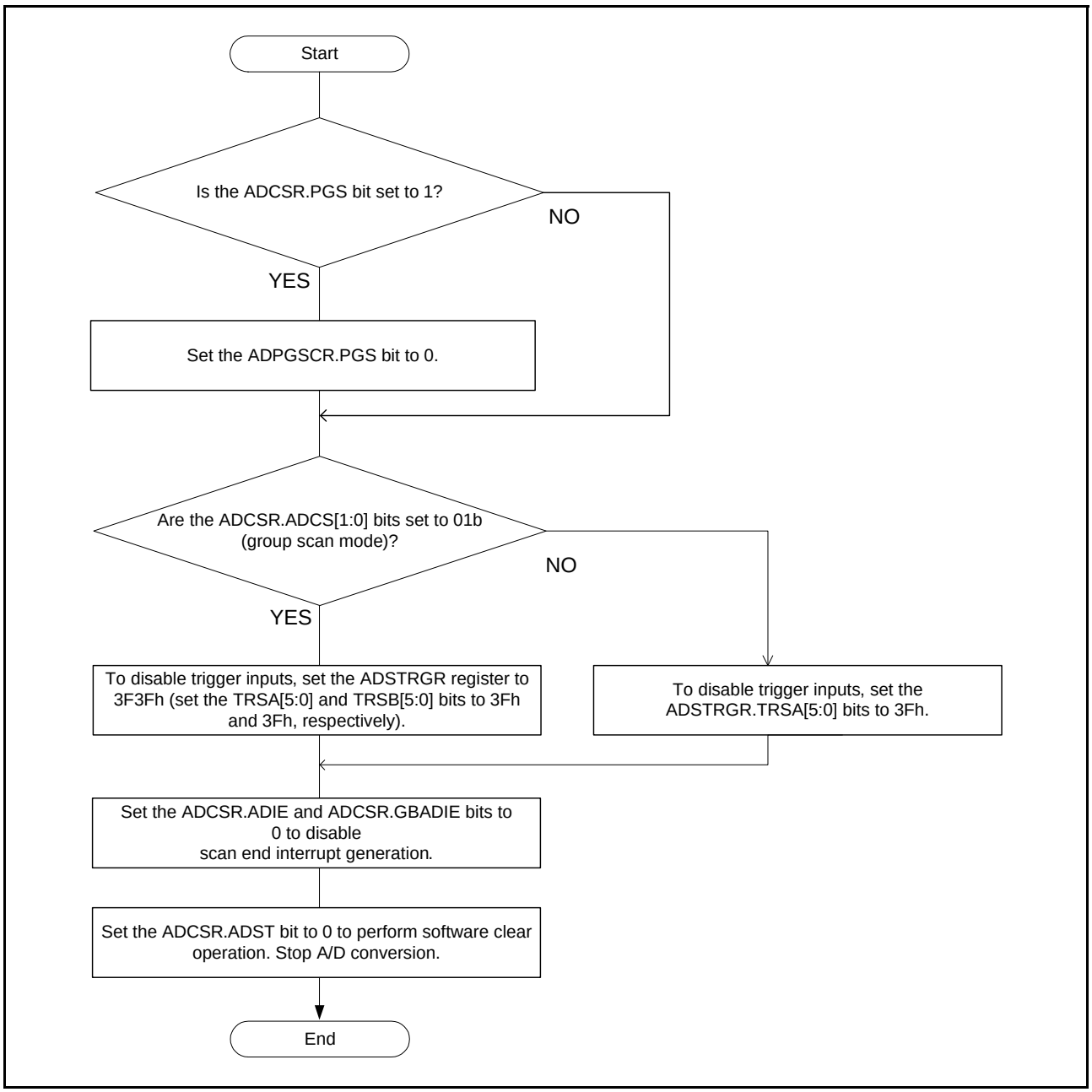


Figure 34.32 Procedures for Clear Operation by Software through the ADCSR.ADST Bit

34.6.3 A/D Conversion Restarting Timing and Termination Timing

It takes a maximum of four ADCLK cycles for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADST bit in ADCSR to 1. It takes a maximum of two ADCLK cycles for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADST bit in ADCSR to 0.

34.6.4 Notes on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D converted data is overwritten with the second A/D converted data in the case that the CPU does not complete reading out the A/D converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

34.6.5 Module Stop Function Setting

Operation of the 12-bit A/D converter can be disabled or enabled using the module stop control register. The 12-bit A/D converter is stopped at the initial value.
After the module stop state is canceled, wait for 1 µs to start A/D conversion. For details, see section 12, Low Power Consumption.

34.6.6 Notes on Entering Low Power Consumption States

Before entering module stop mode or software standby mode, make sure to stop A/D conversion. Here, set the ADST bit in ADCSR to 0, and allow time for stopping the analog unit of the 12-bit A/D converter.
Follow the procedure given below to secure this time.
Follow the procedure for clear operation by software through the ADCSR.ADST bit, shown in Figure 34.32, to set the ADCSR.ADST bit to 0. After confirming that the A/D converter has been stopped, place the MCU in the module stop state mode or software standby mode.
Furthermore, sections of the 12-bit A/D converter enter the state of waiting to operate when the converter is placed in module-stop mode, on software standby, or on deep software standby. Setting the MSTPCRA.MSTPA24 to 1 fully places the 12-bit A/D converter on standby. In this case, wait for a further 10 ms to start A/D conversion after release from the module-stop mode, software standby, or deep software standby.

34.6.7 Allowable Impedance of Signal Source

To achieve high-speed conversion of 1.0 µs, the analog input pins of this MCU are designed so that the conversion accuracy is guaranteed if the impedance of the input signal source is 1 kΩ or less. If an external capacitor of large capacitance is attached in the application in which only a single pin input is converted in single-cycle scan mode, the only load on input is virtually 10 kΩ of the internal input resistor; therefore, the impedance of the signal source can be ignored. Being a low-pass filter, however, an analog input circuit may not follow the analog signal with a large differential coefficient (e. g., larger than 5 mV/µs) as shown in Figure 34.33. When high-speed analog signals are to be converted or multiple pins are to be converted in scan mode, a low-impedance buffer should be used.

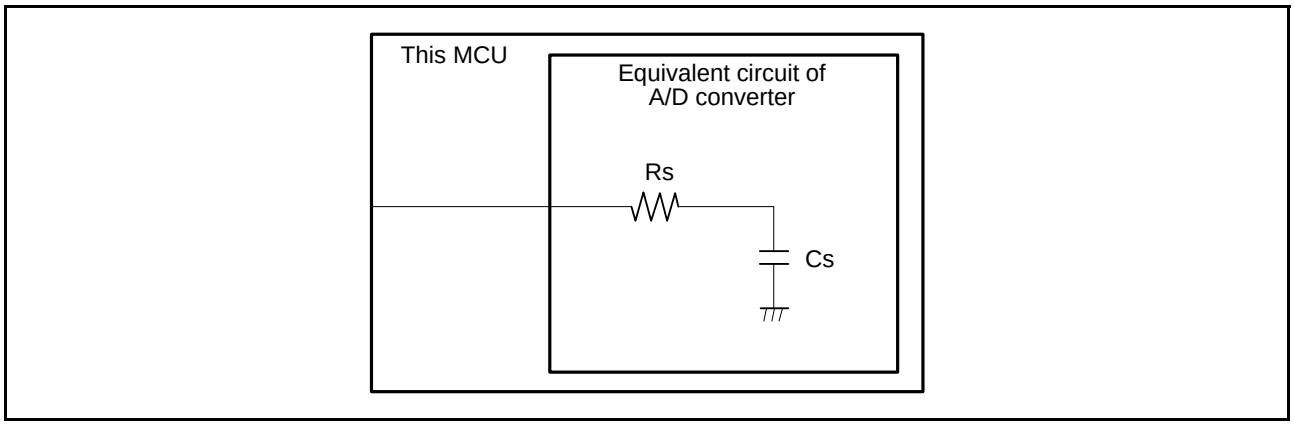


Figure 34.33 Internal Equivalent Circuit of Analog Input Pin

Table 34.11 Specifications of Analog Input Pins

Item		Min.	Max.	Unit
Allowable signal source impedance*1		—	1	kΩ
Internal equivalent circuit of a pin	Rs	—	10	kΩ
	Cs	—	10	pF

Note 1. The value differs depending on the analog power supply voltage and analog input pins to be used. For details, see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions].

34.6.8 Influence on Absolute Accuracy

Attaching a capacitor creates coupling with GND and may affect the absolute accuracy when noisy GND is used; therefore, a capacitor should be connected to electrically stable GND such as AVSS0.
The filter circuit should be designed so that it does not interfere digital signals or it does not serve as an antenna on the circuit board.

34.6.9 Voltage Range of Analog Power Supply Pins

If this MCU is used with the voltages outside the following ranges, the reliability of the MCU may be affected.

- Analog input voltage range
  Voltage (VAN) applied to analog input pins ANn: VREFL0 ≤ VAN ≤ VREFH0
- Relationship between power supply pin pairs (AVCC0–AVSS0, VREFH0–VREFL0, VCC–VSS)
  AVSS0 = VSS
  A 0.1-µF capacitor should be connected between each pair of power supply pins to create a closed loop with the shortest rout possible as shown in Figure 34.34, and connection should be made so that the following conditions are satisfied at the supply side.
  VREFL0 = AVSS0 = VSS
  When the A/D converter is not used, the following conditions should be satisfied.
  VREFH0 = AVCC0 = VCC and VREFL0 = AVSS0 = VSS
- Setting ranges of VREFH0 and VREFL0
  Specify a reference voltage through the VREFH0 pin so that VREFH0 is less than or equal to AVCC0.
  Configure the VREFL0 pin so that VREFL0 is equal to AVSS0 and VSS.

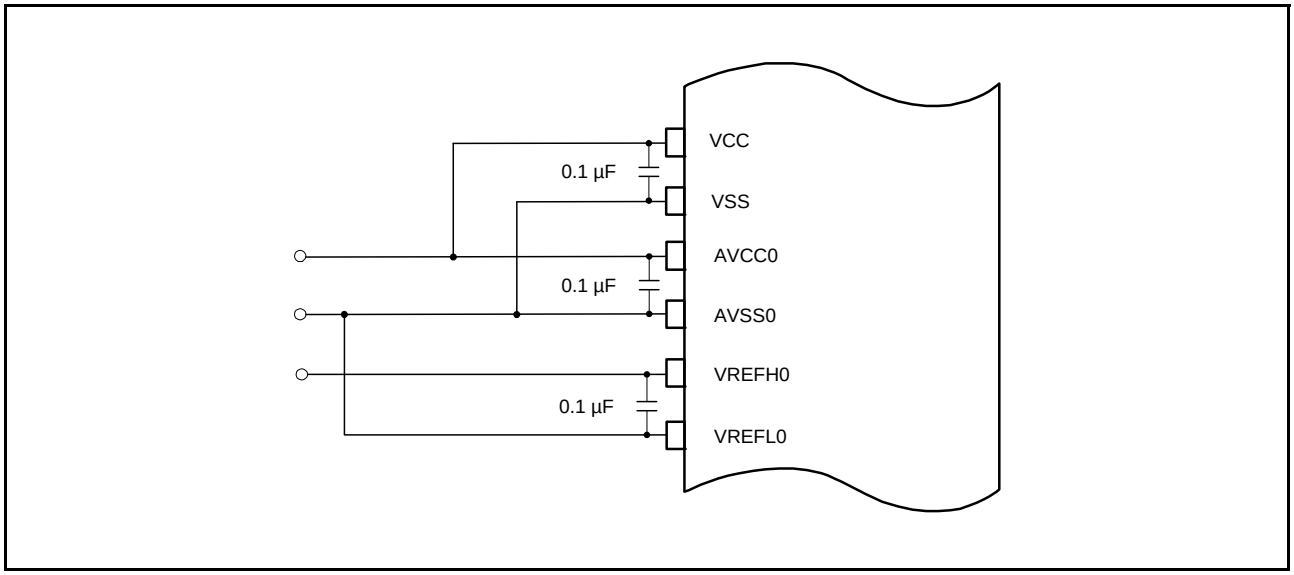


Figure 34.34 Example of Connecting Power Supply Pins

34.6.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or placed near each other. If these rules are not followed, noise will be produced on analog signals and A/D conversion accuracy will be affected. The analog input pins (AN000 to AN003 and AN100 to AN103), analog reference voltages (VREFH0 and VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

34.6.11 Notes on Noise Prevention

To prevent the analog input pins (AN000 to AN003 and AN100 to AN103) from being destroyed by abnormal voltage such as excessive surge, a capacitor should be inserted between AVCC0 and AVSS0 and between VREFH0 and VREFL0, and a protection circuit should be connected to protect the analog input pins (AN000 to AN003 and AN100 to AN103) as shown Figure 34.35.
Moreover, connect the filter capacitor to be connected to analog input pins (AN000 to AN003 and AN100 to AN103) to VREFL0. The 0.1 µF capacitor shown in Figure 34.35 must be placed as close as possible to the pin.
Note that an error may occur when the filter capacitor is connected as shown in Figure 34.35, because the input voltages of the analog input pins (AN000 to AN003 and AN100 to AN103) are averaged. Accordingly, determine circuit constant upon careful consideration.

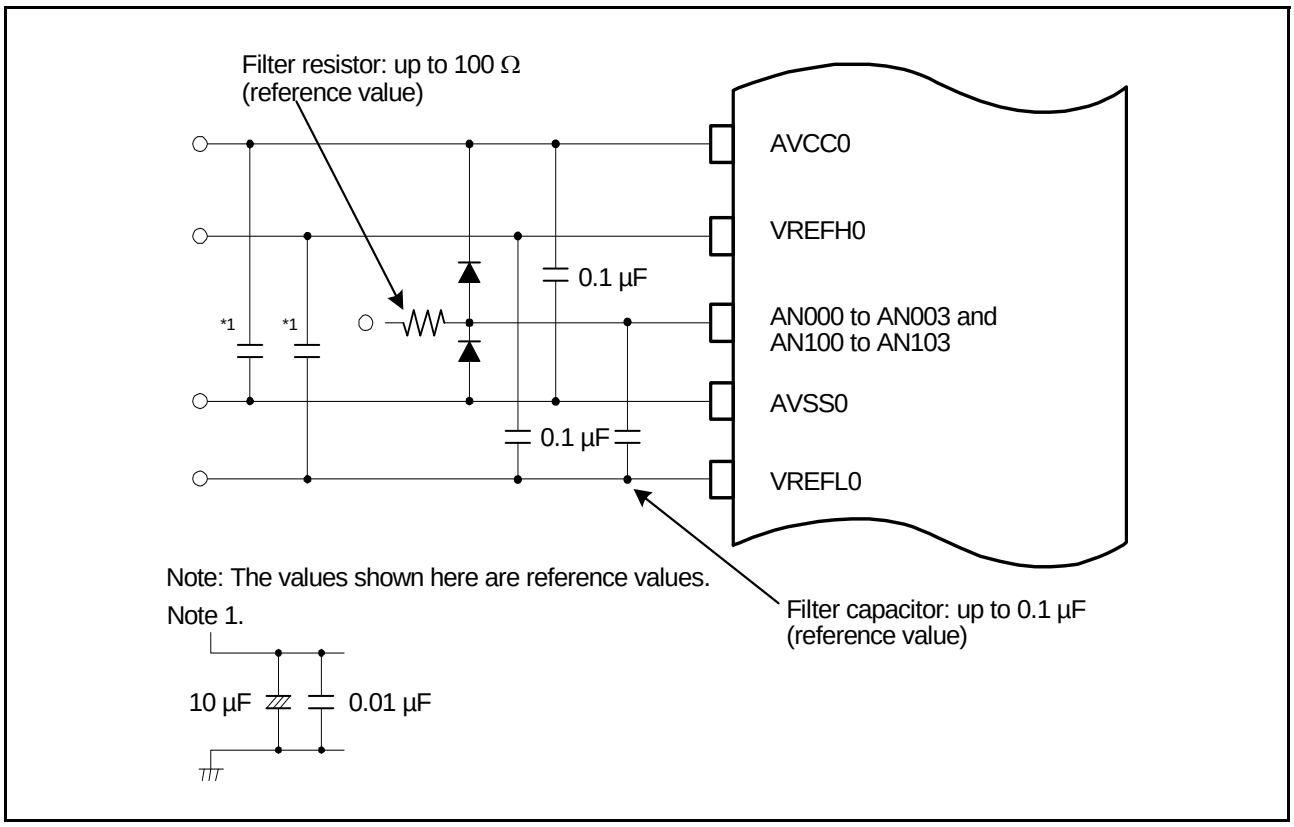


Figure 34.35 Sample Protection Circuit for Analog Inputs

34.6.12 Notes on Using the External Bus

When A/D conversion is done during access to the external bus, the accuracy may degrade.
In this case, repeat conversion several times and calculate by software the average of the converted values, excluding the maximum and minimum values.

35. 12-Bit A/D Converter (S12ADB) [64- and 48-Pin Versions]

35.1 Overview

Products of this MCU incorporate a 12-bit successive approximation A/D converter. Up to eight analog input channels are selectable.

The 12-bit A/D converter converts a maximum of eight selected channels of analog inputs into a 12-bit digital value through successive approximation.

The A/D converter has three operating modes: single-cycle scan mode in which the analog inputs of up to eight arbitrarily selected channels are converted for only once in ascending channel order; and continuous scan mode in which the analog inputs of up to eight arbitrarily selected channels are continuously converted in ascending channel order; and group scan mode in which up to eight channels of the analog inputs are arbitrarily divided into two groups (group A and group B) and converted in ascending channel order in each group.

In group scan mode, the scan start conditions of group A and group B can be independently selected, thus allowing A/D conversion of group A and group B to be started independently.When group A priority control is selected, along with operation as described above, if a request to start scanning for group A is received during A/D conversion operations for group B, conversion operations for group B are discontinued and conversion for group A starts, i.e. is given priority.

In double trigger mode, one arbitrarily selected analog input channel is converted in single-cycle scan mode or group scan mode (group A), and the resulting data of A/D conversion started by the first and second triggers are stored into separate registers (duplication of A/D conversion data).

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages internally generated in the 12-bit A/D converter is converted.

Table 35.1 lists the specifications of the 12-bit A/D converter and Table 35.2 indicates the functions of the 12-bit A/D converter. Figure 35.1 shows a block diagram of the 12-bit A/D converter.

Table 35.1 Specifications of 12-Bit A/D Converter (1/2)

Item	Specifications
Number of units	One unit
Input channels	Up to eight channels
A/D conversion method	Successive approximation method
Resolution	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock ADCLK = 50 MHz)
A/D conversion clock	Peripheral module clock PCLKB*1 and A/D conversion clock ADCLK*1 can be set so that the frequency division ratio should be one of the following. PCLKB to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8 ADCLK is set using the clock generation circuit (CPG).
Data registers	• Eight registers for analog input, one for A/D-converted data duplication in double-trigger mode, and two for A/D-converted data duplication during extended operation in double-trigger mode. • The results of A/D conversion are stored in 12-bit A/D data registers. • 8, 10, and 12-bit accuracy output for the results of A/D conversion (selectable between 2 and 4-bit right shifts for output of conversion results). • An accumulation of A/D conversion results is stored as a 14-bit value in A/D data registers in cumulative mode. • Double trigger mode (selectable in single cycle scan and group scan modes). The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers). A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Table 35.1 Specifications of 12-Bit A/D Converter (2/2)

Item	Specifications
Operating modes	• Single-cycle scan mode: A/D conversion is performed for only once on the analog inputs of up to eight arbitrarily selected channels. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to eight arbitrarily selected channels. • Group scan mode: Up to eight channels of analog inputs are divided into group A and group B and A/D conversion is performed only once on all the selected channels on a group basis. The scan start conditions of group A and group B can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. After the A/D conversion on group A is completed, the A/D conversion on group B is restarted (rescan).
Conditions of A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU3) or the general-purpose PWM timer (GPT). • Asynchronous trigger A/D conversion can be triggered by the external trigger pin ADTRG0#.
Function	• Sample-and-hold function • Channel-dedicated sample-and-hold function (for thee channels) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode • Discharge function • Double trigger mode (duplication of A/D conversion data) • Window-comparator function (for three channels)
Interrupt source	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt (S12ADI) request can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt (S12ADI) request can be generated on completion of double scan. • In group scan mode, A/D scan end interrupt (S12ADI) request can be generated on completion of group A scan, whereas A/D scan end interrupt specially for group B (S12GBADI) request can be generated on completion of group B scan. • In group scan mode with double trigger mode, A/D scan end interrupt (S12ADI) request can be generated on completion of double scan of group A, whereas A/D scan end interrupt specially for group B (S12GBADI) request can be generated on completion of group B scan. • An interrupt request (CMP0 to CMP2) is generated (and can be used as a POE source) in response to detection by the comparator. • The S12ADI, S12GBADI, and CMP0 to CMP2 interrupts are capable of activating the DMA controller (DMAC) or the data-transfer controller (DTC).
Low power consumption function	• Module stop state can be specified.*2

Note 1. Peripheral module clock PCLKB is set according to the setting of the SCKCR.PCKB[3:0] bits and A/D conversion clock ADCLK is set according to the setting of the SCKCR.PCKB[3:0] bits.
Note 2. For details, refer to section 12, Low Power Consumption.

Table 35.2 Functions of 12-Bit A/D Converter (1/2)

Item			Function
Analog input channel			AN000 to AN007
A/D conversion start conditions	Software	Software trigger	Enabled
	External trigger	Trigger input pin	ADTRG0#
	Triggers from MTU3	Input capture to or compare match with MTU0.TGRA	TRGA0N
		Input capture to or compare match with MTU1.TGRA	TRGA1N
		Input capture to or compare match with MTU2.TGRA	TRGA2N
		Input capture to or compare match with MTU3.TGRA	TRGA3N
		Input capture to or compare match with MTU4.TGRA or, in complementary PWM mode, an underflow of MTU4.TCNT (in the trough)	TRGA4N
		Input capture to or compare match with MTU6.TGRA	TRGA6N
		Input capture to or compare match with TRGA6N MTU7.TGRA, or in complementary PWM mode, an underflow of MTU7.TCNT (in the trough)	TRGA7N
		Compare match with MTU0.TGRE	TRG0AN
		Compare match between MTU4.TADCORA and MTU4.TCNT	TRG4AN
		Compare match between MTU4.TADCORB and MTU4.TCNT	TRG4BN
		Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT	TRG4ANor TRG4BN
		Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	TRG4ABN
		Compare match between MTU7.TADCORA and MTU7.TCNT	TRG7AN
		Compare match between MTU7.TADCORB and MTU7.TCNT	TRG7BN
		Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT	TRG7AN or TRG7BN
		Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	TRG7ABN
	Triggers from GPT	Compare match with GPT0.GTADTRA	GTADTRA0N
		Compare match with GPT0.GTADTRB	GTADTRB0N
		Compare match with GPT1.GTADTRA	GTADTRA1N
		Compare match with GPT1.GTADTRB	GTADTRB1N
		Compare match with GPT2.GTADTRA	GTADTRA2N
		Compare match with GPT2.GTADTRB	GTADTRB2N
		Compare match with GPT3.GTADTRA	GTADTRA3N
		Compare match with GPT3.GTADTRB	GTADTRB3N
		Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	GTADTRA0N or GTADTRB0N
		Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	GTADTRA1N or GTADTRB1N
		Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	GTADTRA2N or GTADTRB2N
		Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	GTADTRA3N or GTADTRB3N

Table 35.2 Functions of 12-Bit A/D Converter (2/2)

Item			Function
Channels with dedicated independent sample-and-hold function	Target channel		AN000 to AN002
Window comparator	Target channel		AN000 to AN002
	Reference voltage and setting standard	Specified by external pins	CVREFL: AN003, CVREFH: AN007
		Internally generated	1/8 AVCC0, 2/8 AVCC0, 3/8 AVCC0, 4/8 AVCC0, 5/8 AVCC0, 6/8 AVCC0, 7/8 AVCC0
	Noise cancellation		Samples 16 results of detection by the comparator at PCLK, PCLK/2, PCLK/4, PCLK/8, PCLK/16, or PCLK/128.
Interrupt			S12ADI S12GBADI CMP0 to CMP2
Module stop function setting*1			MSTPCRA.MSTPA17 bit

Note 1. For details, see section 12, Low Power Consumption.

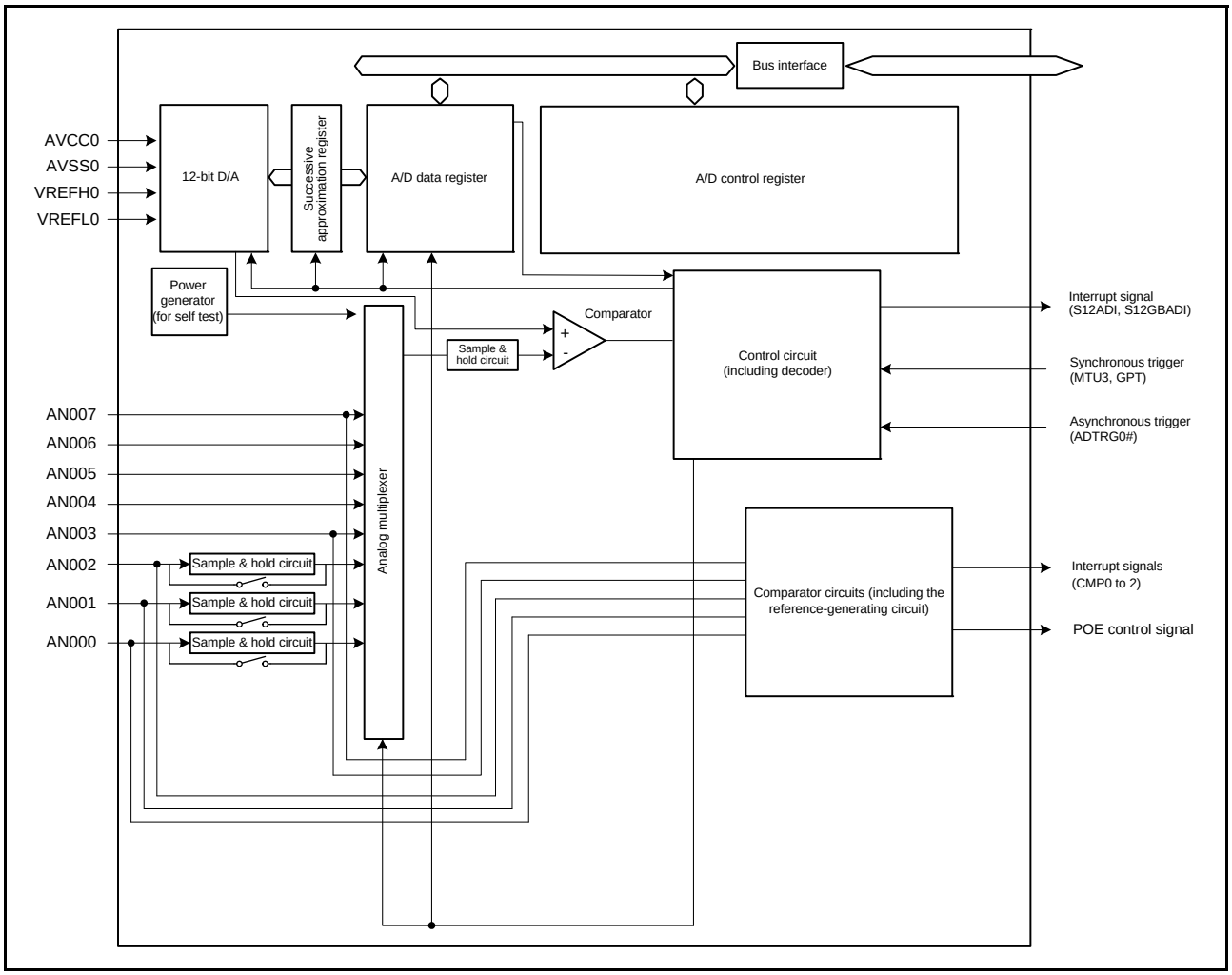


Figure 35.1 Block Diagram of 12-Bit A/D Converter

Table 35.3 indicates the input pins of the 12-bit A/D converter.

Table 35.3 Input Pins of 12-Bit A/D Converter

Pin Name	Input	Function
AVCC0	Input	Analog block power supply pin
AVSS0	Input	Analog block ground pin
VREFH0	Input	Reference power supply pin
VREFL0	Input	Reference power supply ground pin
AN000	Input	Analog input pin 0
AN001	Input	Analog input pin 1
AN002	Input	Analog input pin 2
AN003/CVREFL	Input	Analog input pin 3/comparator low-side reference-voltage pin (The pin serves as the comparator low-side reference-voltage pin when the comparator is operating and the application of reference voltages to external pins is selected.)
AN004	Input	Analog input pin 4
AN005	Input	Analog input pin 5
AN006	Input	Analog input pin 6
AN007/CVREFH	Input	Analog input pin 7/comparator high-side reference-voltage pin (The pin serves as the comparator high-side reference-voltage pin when the comparator is operating and the application of reference voltages to external pins is selected.)
ADTRG0#	Input	External trigger input pin for starting A/D conversion

35.2 Register Descriptions

35.2.1 A/D Data Registers y (ADDRy; y = 0 to 7), A/D Data-Doubling Register (ADDBLDR), A/D Data-Doubling Register A (ADDBLDRA), and A/D Data-Doubling Register B (ADDBLDRB)

The ADDRy registers are 16-bit read-only registers for storing the results of A/D conversion. Register ADDBLDR is a 16-bit read-only register for storing the result of A/D conversion in response to the second trigger in double-trigger mode. Registers ADDBLDRA and ADDBLDRB are 16-bit read-only registers for storing the result of A/D conversion in response to the respective triggers during extended operation in double-trigger mode.
The formats for data in the ADDRy, ADDBLDR, ADDBLDRA, and ADDBLDRB registers vary according to the following conditions.

- The setting of the A/D data register format selection bit (determining whether the data are flush-left or flush-right in the registers)
- The setting of the A/D data register bit-precision specification bits (for eight, 10, or 12 bits)
- The setting of the A/D-converted value cumulative mode selection register (determining whether A/D-converted value cumulative mode is or is not selected)

The conditions are given above each of the descriptions below.

- The settings are for flush-right data with 12-bit precision)

Address: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDR4 0008 9028h, ADDR5 0008 902Ah, ADDR6 0008 902Ch, ADDR7 0008 902Eh, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	AD[11:0]	Converted value 11 to 0	12-bit A/D-converted value	R
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings are for flush-right data with 10-bit precision

Address(es): ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDR4 0008 9028h, ADDR5 0008 902Ah, ADDR6 0008 902Ch, ADDR7 0008 902Eh, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[11:2]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	AD[11:2]	Converted value 11 to 2	10 higher-order bits of the 12-bit A/D converted value	R
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings are for flush-right data with eight-bit precision.

Address(es): ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDR4 0008 9028h, ADDR5 0008 902Ah, ADDR6 0008 902Ch, ADDR7 0008 902Eh, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	AD[11:4]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	AD[11:4]	Converted value 11 to 4	Eight higher-order bits of the 12-bit A/D converted value	R
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings are for flush-left data with 12-bit precision

Address: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDR4 0008 9028h, ADDR5 0008 902Ah, ADDR6 0008 902Ch, ADDR7 0008 902Eh, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b4	AD[11:0]	Converted value 11 to 0	12-bit A/D-converted value	R

- The settings are for flush-left data with 10-bit precision.

Address(es): ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDR4 0008 9028h, ADDR5 0008 902Ah, ADDR6 0008 902Ch, ADDR7 0008 902Eh, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:2]										—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b6	AD[11:2]	Converted value 11 to 2	10 higher-order bits of the 12-bit A/D converted value	R

- The settings are for flush-left data with eight-bit precision.

Address(es): ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDR4 0008 9028h, ADDR5 0008 902Ah, ADDR6 0008 902Ch, ADDR7 0008 902Eh, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:4]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	AD[11:4]	Converted value 11 to 4	Eight higher-order bits of the 12-bit A/D converted value	R

- When A/D-converted value addition mode is selected

Address: ADDR0 0008 9020h, ADDR1 0008 9022h, ADDR2 0008 9024h, ADDR3 0008 9026h, ADDR4 0008 9028h, ADDR5 0008 902Ah, ADDR6 0008 902Ch, ADDR7 0008 902Eh, ADDBLDR 0008 9018h, ADDBLDRA 0008 9084h, ADDBLDRB 0008 9086h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[13:0]														—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b2	AD[13:0]	—	14-bit A/D-converted value addition result	R

When A/D-converted value addition mode is selected, the AD[13:0] bits show the value that is obtained by adding up A/D-converted values on a specific channel. In A/D-converted value addition mode, the value obtained by adding up A/D conversion results is stored left-justified as a 14-bit value in the A/D data register. The settings of the ADCER.ADPRC[1:0] and ADCER.ADRFMT bits become invalid.

35.2.2 A/D Self-Diagnosis Data Register (ADRD)

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the 12-bit A/D converter's self-diagnosis.
The following different formats are used depending on the setting of the A/D data register format select bit (ADRFMT) in ADCER. ADRD cannot be set to A/D-converted value addition mode.

- ADCER.ADRFMT = 0 (Setting for right-alignment)

Address: 0008 901Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	AD[11:0]	—	12-bit A/D-converted value	R
b13, b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREFH0 × 0 has been executed. 1 0: Self-diagnosis using VREFH0 × 1/2 has been executed. 1 1: Self-diagnosis using VREFH0 × 1 has been executed. For details of self-diagnosis, see section 35.2.8, A/D Control Extended Register (ADCER).	R

- ADCER.ADRFMT = 1 (Setting for left-alignment)

Address: 0008 901Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREFH0 × 0 has been executed. 1 0: Self-diagnosis using VREFH0 × 1/2 has been executed. 1 1: Self-diagnosis using VREFH0 × 1 has been executed. For details of self-diagnosis, see section 35.2.8, A/D Control Extended Register (ADCER).	R
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b4	AD[11:0]	—	12-bit A/D-converted value	R

35.2.3 A/D Control Register (ADCSR)

Address: 0008 9000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		ADIE	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	DBLANS[4:0]	Double-trigger channel select	These bits select the analog input on one of the eight channels for double-triggered operation. The setting is only effective while double-trigger mode is selected.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	GBADIE	Group B Scan End Interrupt Enable	0: Disables S12GBADI interrupt generation upon group B scan completion. 1: Enables S12GBADI interrupt generation upon group B scan completion.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselects double trigger mode. 1: Selects double trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: A/D conversion is started by the synchronous trigger (MTU3, GPT). 1: A/D conversion is started by the asynchronous trigger (ADTRG0#).	R/W
b9	TRGE	Trigger Start Enable	0: Disables A/D conversion to be started by the synchronous or asynchronous trigger. 1: Enables A/D conversion to be started by the synchronous or asynchronous trigger.	R/W
b10, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	ADIE	Scan End Interrupt Enable	0: Disables S12ADI interrupt generation upon scan completion. 1: Enables S12ADI interrupt generation upon scan completion.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single-cycle scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited	R/W
b15	ADST	A/D Conversion Start	0: Stops A/D conversion process. 1: Starts A/D conversion process.	R/W

Note 1. Starting A/D conversion using an external pin (asynchronous trigger)
If 1 is written to both the TRGE and EXTRG bits in ADCSR when a high-level signal is input to the external pin (ADTRG0#), and then if the ADTRG0# signal is driven low, the falling edge of ADTRG0# is detected and the scan conversion process is started. In this case, the pulse width of the low-level input must be at least 1.5 PCLK clock cycles.

ADCSR sets double trigger mode, A/D conversion start trigger; enables/disables scan end interrupt; selects the scan mode; and starts or stops A/D conversion.

DBLANS[4:0] Bits (Double-trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double trigger mode. The A/D conversion results of the analog input of the selected channel are stored into A/D data register y when conversion is started by the first trigger, and into the A/D data duplication register when started by the second trigger. Selection of the channel for double-triggered operation is described in Table 35.4. A/D-converted value addition mode with double trigger mode can be set by selecting the channel selected by the DBLANS[4:0] bits using the ADADS register. If double trigger mode is selected, the channel selected by the ADANSA register is invalid, and the channel selected by the DBLANS [4:0] bits is subjected to A/D conversion instead.
The DBLANS[4:0] bits should be set while the ADST bit is 0 (they should not be set simultaneously when 1 is written to the ADST bit.)

Table 35.4 Relationship between DBLANS Bit Settings and Double Trigger Enabled Channels

DBLANS[4:0]	Duplication Channel
00000	AN000
00001	AN001
00010	AN002
00011	AN003
00100	AN004
00101	AN005
00110	AN006
00111	AN007

GBADIE Bit (Group B Scan End Interrupt Enable)

The GBADIE bit enables or disables group B scan end interrupt (S12GBADI) in group scan mode.

DBLE Bit (Double Trigger Mode Select)

In double trigger mode, the following operation is performed after scanning is started by the MTU3 or GPT trigger selected by the TRSA[4:0] bits in ADSTRGR.

1. When the ADIE bit is 1, a scan end interrupt is not generated upon first scan completion but is generated upon second scan completion.
2. The A/D conversion results of the analog input of the channel selected by the DBLANS[4:0] are stored into A/D data register y for the first time, and into the A/D data duplication register for the second time.

Setting the DBLE bit to 1 invalidates the channel selected by the ADANSA register. In continuous scan mode, double trigger mode should not be selected. In double trigger mode, software trigger should not be selected. The DBLE bit should be set while ADST bit is 0 (it should not be set simultaneously when 1 is written to the ADST bit.)

EXTRG Bit (Trigger Select)

The EXTRG bit selects the synchronous trigger or the asynchronous trigger as the trigger for starting A/D conversion.

TRGE Bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous trigger and the asynchronous trigger. This bit should be set to 1 in group scan mode.

ADIE Bit (Scan End Interrupt Enable)

The ADIE bit enables or disables the A/D scan end interrupt (S12ADI) in scans except for group B scan in group scan mode.

With double trigger mode deselected, the S12ADI interrupt is generated when the first scan is completed if the ADIE bit is set to 1.

With double trigger mode selected, the S12ADI interrupt is generated when the second scan is completed if the ADIE bit is set to 1 as long as the scan is started by the MTU3 or GPT trigger selected by the TRSA[4:0] bits in ADSTRGR.

ADCS[1:0] Bits (Scan Mode Select)

The ADCS bit selects the scan mode.
In single-cycle scan mode, A/D conversion is performed for the analog inputs of a maximum of eight channels selected with the ADANSA register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, scan conversion is stopped.
In continuous scan mode, while the ADST bit in ADCSR is 1, A/D conversion is performed for the analog inputs of a maximum of eight channels selected with the ADANSA register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is repeated beginning at the first channel. A/D conversion is repeated until the ADST bit in ADCSR is set to 0.
In group scan mode, A/D conversion is performed for the analog inputs (group A) of a maximum of eight channels selected with the ADANSA register in the ascending order of the channel number after scanning is started by the MTU3 or GPT trigger selected by the TRSA[4:0] bits in ADSTRGR, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is stopped. A/D conversion is also performed for the analog inputs (group B) of a maximum of eight channels selected with the ADANSB register in the oscending order of the channel number after scanning is started by the MTU3 or GPT trigger celected by the TRSB[4:0] bits in ADSTRGR, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is stopped. In group scan mode, different channels and triggers should be selected for group A and group B.
The ADCS bit should be set while the ADST bit is 0 (it should not be set simultaneously when 1 is written to the ADST bit.)

ADST Bit (A/D Conversion Start)

The ADST bit starts or stops A/D conversion process.
Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and conversion target analog input.
[Setting conditions]

- 1 is written by software.
- The synchronous trigger (MTU3 or GPT, or temperature sensor) selected by the ADSTRGR.TRSA[4:0] bits is detected with ADCSR.EXTRG and ADCSR.TRGE bits being set to 0 and 1, respectively.
- A synchronous trigger (MTU3 or GPT) selected by the ADSTRGR.TRSB[4:0] bits is detected with the ADCSR.TRGE bit being set to 1 in group scan mode.
- The asynchronous trigger is detected with the ADCSR.TRGE and ADCSR.EXTRG bits being set to 1 and the ADSTRGR.TRSA[4:0] bits being set to “00000b”.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), a group B trigger is detected and A/D conversion of group B is started.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), a group B trigger is detected and A/D conversion of group B is started.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), the ADGSPCR.GBRP bit is set to 1 and A/D conversion of group B is started.

[Clearing conditions]

- 0 is written by software.
- The A/D conversion of all the channels selected is completed in single-cycle scan mode.
- Group A scan is completed in group scan mode.
- Group B scan is completed in group scan mode.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), a group A trigger is detected during A/D conversion of group B and the scanning of group B is stopped.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), the ADGSPCR.GBRP bit is set to 1 and the scanning of group B by a resumption trigger is completed.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), the ADGSPCR.GBRSCN bit is set to 1 and the scanning of group B by a trigger is completed.

Note 1. When group-A priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1), do not set the ADST bit to 1.
Note 2. When group-A priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS = 1) and ADGSPCR.GBRP = 1, do not set the ADST bit to 0. When terminating A/D conversion, follow the procedure for clearing the ADST bit.

35.2.4 A/D Channel Select Register A (ADANSA)

Address: 0008 9004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	ANSA[7:0]	A/D Conversion Channels Select	0: AN000 to AN007 are not subjected to conversion. 1: AN000 to AN007 are subjected to scan conversion.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADANSA selects analog input channels for A/D conversion from among AN000 to AN007. In group scan mode, group A channels are to be selected.

ANSA[7:0] Bits (A/D Conversion Channel Select)

The ANSA[15:0] bits select analog input channels for A/D conversion from among AN000 to AN007. The channels to be selected and the number of channels can be arbitrarily set. The ANSA[0] bit corresponds to AN000 and the ANSA[7] bit corresponds to AN007.
When double trigger mode is selected, the channel selected by the ANSA[7:0] bits is invalid, and the channel selected by the ADCSR.DBLANS[4:0] bits is selected in group A instead.
The ANSA[7:0] bits should be set while the ADCSR.ADST bit is 0.

35.2.5 A/D Channel Select Register B (ADANSB)

Address: 0008 9014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSB[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	ANSB[7:0]	A/D Conversion Channels Select	0: AN000 to AN007 are not subjected to conversion. 1: AN000 to AN007 are subjected to scan conversion.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADANSB selects channels for A/D conversion in group B from among AN000 to AN007 in group scan mode. ADANSB is not used in any other scan mode. The channels for conversion can be selected from among the channels other than group A channels, which are selected by the ADANSA register or ADCSR.DBLANS[4:0] bits in double trigger mode. The ANSB[0] bit corresponds to AN000 and the ANSB[7] bit corresponds to AN007.
The ANSB[7:0] bits should be set while the ADST bit is 0.

35.2.6 A/D-Converted Value Addition Mode Select Register (ADADS)

Address: 0008 9008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ADS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	ADS[7:0]	A/D-Converted Value Addition Channel Select	0: A/D-converted value addition mode for AN000 to AN007 is not selected. 1: A/D-converted value addition mode for AN000 to AN007 is selected.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADADS selects the channels 0 to 7 on which A/D conversion is performed successively 2 to 4 times and then converted values are added (integrated).

ADS[7:0] Bits (A/D-Converted Value Addition Channel Select)

When the ADS[n] bit of the number that is the same as that of A/D converted channel selected by ANSA[n] bits (n = 0 to 7) in ADANSA or DBLANS[4:0] bits in ADCSR and ANSB[n] bits (n = 0 to 7) in ADANSB is set to 1, these bits perform A/D conversion of analog input of the selected channels successively 2 to 4 times that is set with the ADC[1:0] bits in ADADC and returns the added (integrated) conversion results to the A/D data register. For the channel for which the A/D conversion is performed and addition mode is not selected, a normal one-time conversion is performed and the conversion result is returned to the A/D data register.
The ADS[7:0] bits should be set while the ADCSR.ADST bit is 0.

Figure 35.2 shows a scanning operation sequence in which both the ADS[2] and ADS[6] bits are set to 1.
In continuous scan mode (ADCSR.ADCS = 10b), it is assumed that the addition count is set to 4 (ADADC.ADC[1:0] = 11b) and the channels AN000 to AN007 are selected (ADANSA.ANSA[7:0] = FFh). The conversion process begins with AN000. The AN002 conversion is performed successively 4 times, and the added (integrated) value is returned to the A/D data register 2. After that the AN003 conversion process is started. The AN006 conversion is performed successively 4 times and the added (integrated) value is returned to the A/D data register 6. After conversion of AN007, the conversion operation is once again performed in the same sequence from AN000.
For the channel for which the addition mode is not selected, the A/D data register format is determined by the ADRFMT bit in ADCER (right-alignment or left-alignment).

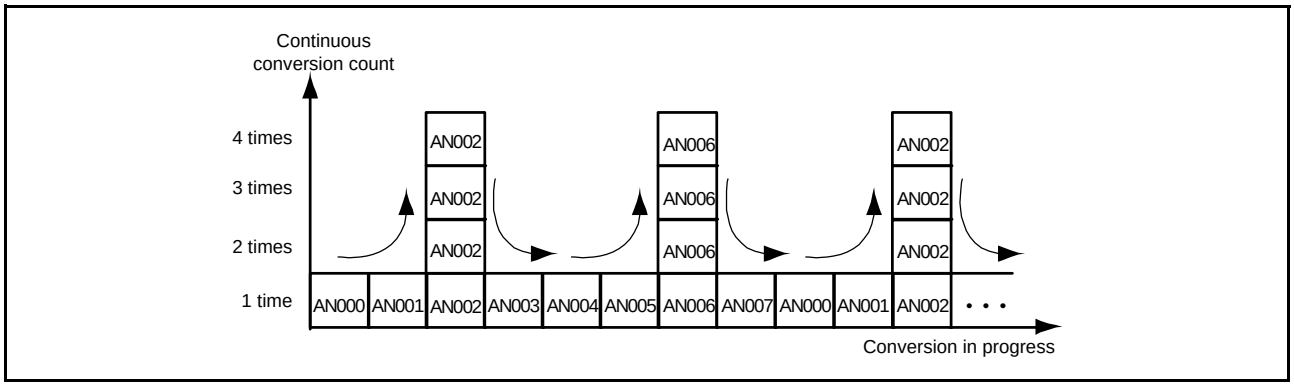


Figure 35.2 Scan Conversion Sequence with ADADC.ADC[1:0] and ADS[2] = 1 and ADS[6] = 1

35.2.7 A/D-Converted Value Addition Count Select Register (ADADC)

Address: 0008 900Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ADC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	ADC[1:0]	Addition Count Select	b1 b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADADC sets the addition count for the channels for which A/D-converted value addition mode is selected, and for A/D conversion.

ADC[1:0] Bits (Addition Count Select)

The ADC[1:0] bits set the addition count common to the channels for which A/D conversion or A/D-converted value addition mode is selected, including the channels selected in double trigger mode (by ADCSR.DBLANS[4:0] bits), and to A/D conversion.

The ADC[1:0] bits should be set while the ADCSR.ADST bit is 0.

35.2.8 A/D Control Extended Register (ADCER)

Address: 0008 900Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	DCE	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2, b1	ADPRC[1:0]	A/D data-register bit-precision specification bit	00: Values are stored with 12-bit precision in the A/D data registers. 01: Values are stored with 10-bit precision in the A/D data registers. 10: Values are stored with 8-bit precision in the A/D data registers. 11: Do not make this setting.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DCE	DCE discharge enable bit	0: Discharging does not proceed on completion of A/D conversion. 0: Discharging proceeds on completion of A/D conversion.	R/W
b5	ACE	Automatic Clearing Enable	0: Disables automatic clearing. 1: Enables automatic clearing.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Conversion Voltage Select for Self-Diagnosis	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: Uses VREFH0 × 0 for self-diagnosis. 1 0: Uses VREFH0 × 1/2 for self-diagnosis. 1 1: Uses VREFH0 × 1 for self-diagnosis.	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Rotation mode for self-diagnosis voltage 1: Fixed mode for self-diagnosis voltage	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Disables self-diagnosis of 12-bit A/D converter. 1: Enables self-diagnosis of12-bit A/D converter.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Right-alignment is selected for the A/D data register format. 1: Left-alignment is selected for the A/D data register format.	R/W

ADCER sets the parameters related to self-diagnosis, format of the A/D data registers y (ADDRy), and enables/disables automatic clearing of registers.

ADPRC Bits (A/D Data Register Bit-Precision Specification)

These bits select storage of the results of A/D conversion with eight-, 10-, or 12-bit precision in the ADDRy, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.

DCE Bit (Discharge Enable)

This bit selects whether discharging of analog pins involved in conversion proceeds or does not proceed on completion of A/D conversion. If a failure leads to an input pin becoming open circuit, when discharging proceeds several times and the result of conversion approaches 0000h, the open circuit state of the pin is detectable.

ACE Bit (Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (All “0”) of ADDRy, ADRD,ADDBLDR, ADDBLDRA, and ADDBLDRB after the register has been read by the CPU, DTC, or DMACA. This function enables update failures of ADDRy, ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB to be detected.

DIAGVAL[1:0] Bits (Conversion Voltage Select for Self-Diagnosis)

For details, refer to the ADCER.DIAGLD bit description.
Self-diagnosis should not be executed by setting the ADCER.DIAGLD bit to 1 with these bits set to 00b.

DIAGLD Bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis. Setting this bit to 0 allows conversion of the voltages in rotation mode where VREFH0 × 0, VREFH0 × 1/2, and VREFH0 × 1 are converted in this order. After reset, VREFH0 × 0 is first converted if rotation mode is selected whereas the fixed voltage specified by the ADCER.DIAGVAL[1:0] bits is converted if fixed mode is selected. In rotation mode, the self-diagnosis voltage value does not return to VREFH0 × 0 when scan conversion is completed; when scan conversion is restarted, rotation starts at the voltage value following the previous value. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.
The DIAGLD bit should be set while the ADST bit is 0.

DIAGM Bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.
Self-diagnosis is used to detect a failure of the 12-bit A/D converter. Specifically, one of the internally generated voltage values VREFH0 × 0, VREFH0 × 1/2, and VREFH0 × 1 is converted. When conversion is completed, information of the converted voltage and the conversion result is stored into the self-diagnosis data register (ADRD). ADRD can then be read out by software to determine whether the conversion result falls within the normal range (normal) or not (abnormal). Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. The execution time of self-diagnosis equals to the A/D conversion time of one channel. If selected, self-diagnosis is not executed. When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.
The DIAGM bit should be set while the ADST bit is 0.

ADRFMT Bit (A/D Data Register Format Select)

The ADRFMT bit specifies left-alignment or right-alignment for the data to be stored in ADDRy, ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.
When the A/D converted value addition mode is selected, the format of each data register is fixed to left-alignment, irrespective of the ADCER.ADRFMT bit value.

For details on the format of the data registers, see section 35.2.1, A/D Data Registers y (ADDRy; y = 0 to 7), A/D Data-Doubling Register (ADDBLDR), A/D Data-Doubling Register A (ADDBLDRA), and A/D Data-Doubling Register B (ADDBLDRB), and section 35.2.2, A/D Self-Diagnosis Data Register (ADRD).

35.2.9 A/D Start Trigger Select Register (ADSTRGR)

Address: 0008 9010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TRSA[4:0]					—	—	—	TRSB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	TRSB[4:0]	A/D Conversion Start Trigger Select for Group B	Select the A/D conversion start trigger for group B in group scan mode.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12 to b8	TRSA[4:0]	A/D Conversion Start Trigger Select	Select the A/D conversion start trigger in single-cycle scan mode and continuous mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSTRGR selects the A/D conversion start trigger.

TRSB[4:0] Bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[4:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[4:0] bits require to be set only in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B, setting software trigger or asynchronous trigger is prohibited. Therefore, the TRSB[4:0] bits should be set to the value other than 00000 and the ADCSR.TRGE bit should be set to 1 in group scan mode.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single cycle scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[4:0] bits to 1Fh. Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger may become invalid.

Table 35.5 shows the A/D conversion startup sources selected by TRSB[4:0] bits.

TRSA[4:0] Bits (A/D Conversion Start Trigger Select)

The TRSA[4:0] bits select the trigger to start A/D conversion in single-cycle san mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in group A is selected. For scan execution in group scan mode or double trigger mode, software trigger or asynchronous trigger cannot be used.

- When using the A/D conversion startup source of the synchronous trigger (MTU3, GPT), set the TRGE bit in ADCSR to 1 and set the EXTRG bit in ADCSR to 0.
- When using the asynchronous trigger (ADTRG0#), set the TRGE bit in ADCSR to 1 and set the EXTRG bit in ADCSR to 1.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, and the TRSA[4:0] bits.
  Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger may become invalid.

Table 35.6 shows the A/D conversion startup sources selected by TRSA[4:0] bits

Table 35.5 Selection of A/D Activation Sources by the TRSB[4:0] Bits (1/2)

Module	Source	Remarks	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source de-selection state			1	1	1	1	1
MTU3	TRGA0N	Input capture to or compare match with MTU0.TGRA	0	0	0	0	1
	TRGA1N	Input capture to or compare match with MTU1.TGRA	0	0	0	1	0
	TRGA2N	Input capture to or compare match with MTU2.TGRA	0	0	0	1	1
	TRGA3N	Input capture to or compare match with MTU3.TGRA	0	0	1	0	0
	TRGA4N	Input capture to or compare match with MTU4.TGRA or, in complementary PWM mode, an underflow of MTU4.TCNT (in the trough)	0	0	1	0	1
	TRGA6N	Input capture to or compare match with MTU6.TGRA	0	0	1	1	0
	TRGA7N	Input capture to or compare match with MTU7.TGRA, or in complementary PWM mode, an underflow of MTU7.TCNT (in the trough)	0	0	1	1	1
	TRG0AN	Compare match with MTU0.TGRE	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT and between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	1	0	0	0	0

Table 35.5 Selection of A/D Activation Sources by the TRSB[4:0] Bits (2/2)

Module	Source	Remarks	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
GPT	GTADTRA0N	Compare match with GPT0.GTADTRA	1	0	0	0	1
	GTADTRB0N	Compare match with GPT0.GTADTRB	1	0	0	1	0
	GTADTRA1N	Compare match with GPT1.GTADTRA	1	0	0	1	1
	GTADTRB1N	Compare match with GPT1.GTADTRB	1	0	1	0	0
	GTADTRA2N	Compare match with GPT2.GTADTRA	1	0	1	0	1
	GTADTRB2N	Compare match with GPT2.GTADTRB	1	0	1	1	0
	GTADTRA3N	Compare match with GPT3.GTADTRA	1	0	1	1	1
	GTADTRB3N	Compare match with GPT3.GTADTRB	1	1	0	0	0
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	1	1	0	0	1
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	1	1	0	1	0
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	1	1	0	1	1
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	1	1	1	0	0

Table 35.6 Selection of A/D Activation Sources by the TRSA[4:0] Bits (1/2)

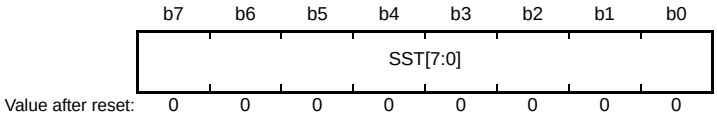
Module	Source	Remarks	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselection state			1	1	1	1	1
External pin	ADTRG0#	Input pin for the ADTRG0# trigger	0	0	0	0	0
MTU3	TRGA0N	Input capture to or compare match with MTU0.TGRA	0	0	0	0	1
	TRGA1N	Input capture to or compare match with MTU1.TGRA	0	0	0	1	0
	TRGA2N	Input capture to or compare match with MTU2.TGRA	0	0	0	1	1
	TRGA3N	Input capture to or compare match with MTU3.TGRA	0	0	1	0	0
	TRGA4N	Input capture to or compare match with MTU4.TGRA or, in complementary PWM mode, an underflow of MTU4.TCNT (in the trough)	0	0	1	0	1
	TRGA6N	Input capture to or compare match with MTU6.TGRA	0	0	1	1	0
	TRGA7N	Input capture to or compare match with MTU7.TGRA, or in complementary PWM mode, an underflow of MTU7.TCNT (in the trough)	0	0	1	1	1
	TRG0AN	Compare match with MTU0.TGRE	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT or between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT or between MTU7.TADCORB and MTU7.TCNT	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT and between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	1	0	0	0	0

Table 35.6 Selection of A/D Activation Sources by the TRSA[4:0] Bits (2/2)

Module	Source	Remarks	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
GPT	GTADTRA0N	Compare match with GPT0.GTADTRA	1	0	0	0	1
	GTADTRB0N	Compare match with GPT0.GTADTRB	1	0	0	1	0
	GTADTRA1N	Compare match with GPT1.GTADTRA	1	0	0	1	1
	GTADTRB1N	Compare match with GPT1.GTADTRB	1	0	1	0	0
	GTADTRA2N	Compare match with GPT2.GTADTRA	1	0	1	0	1
	GTADTRB2N	Compare match with GPT2.GTADTRB	1	0	1	1	0
	GTADTRA3N	Compare match with GPT3.GTADTRA	1	0	1	1	1
	GTADTRB3N	Compare match with GPT3.GTADTRB	1	1	0	0	0
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	1	1	0	0	1
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	1	1	0	1	0
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	1	1	0	1	1
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	1	1	1	0	0

35.2.10 A/D Sampling State Register n (ADSSTRn) (n = 0 to 7)

Address: ADSSTR0 0008 9060h, ADSSTR1 0008 9073h, ADSSTR2 0008 9074h, ADSSTR3 0008 9075h, ADSSTR4 0008 9076h, ADSSTR5 0008 9077h, ADSSTR6 0008 9078h, ADSSTR7 0008 9079h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	These bits set the sampling time in the range from 13 to 255 states.	R/W

The ADSSTRn register sets the sampling time for analog input.
If one state is one ADCLK (A/D conversion clock) cycle and the ADCLK clock is 50 MHz, one state is 20 ns. The initial value is 20 states. If the impedance of analog input signal source is too high to secure sufficient sampling time or if the ADCLK clock is slow, the sampling time can be adjusted. When any bit of this register is to be set, ADCSR.ADST must be 0. The sampling time must be set to a value that is 13 states or more and is 255 or less. In addition, the sampling time must be 0.4 µs or more. Table 35.7 shows the relationship between the A/D sampling state register and the relevant channels.
For details, refer to section 35.3.5, Analog Input Sampling and Scan Conversion Time.

Table 35.7 Relationship between A/D Sampling State Register and Relevant Channels

Bit Name	Corresponding Channels
ADSSTR0.SST[7:0] bits	AN000/self-diagnosis
ADSSTR1.SST[7:0] bits	AN001
ADSSTR2.SST[7:0] bits	AN002
ADSSTR3.SST[7:0] bits	AN003
ADSSTR4.SST[7:0] bits	AN004
ADSSTR5.SST[7:0] bits	AN005
ADSSTR6.SST[7:0] bits	AN006
ADSSTR7.SST[7:0] bits	AN007

35.2.11 A/D Sample and Hold Circuit Control Register (ADSHCR)

Address: 0008 9066h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SHANS[2:0]			SSTSH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SSTSH[7:0]	Sampling Time Sample-and-Hold Circuit Setting	Set the sampling time (4 to 255 states).	R/W
b10 to b8	SHANS[2:0]	Channel-Dedicated Sample-and-Hold Circuit Bypass Select	Select whether to use or not use (bypass) AN000 to AN002 channel-dedicated sample-and-hold circuits. 0: Bypass the channel-dedicated sample-and-hold circuits. 1: Use the channel-dedicated sample-and-hold circuits.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSHCR sets the parameters related to channel-dedicated sample-and-hold circuits.

SSTSH[7:0] Bits (Sampling Time Sample-and-Hold Circuit Setting)

The SSTSH[7:0] bits set the sampling time for the channel-dedicated sample-and-hold circuits. One state is one ADCLK (A/D conversion clock) cycle. When the ADCLK is 50 MHz, one state is 20 ns. The initial value is 20 states. If the impedance of the analog input signal source is too high to secure sufficient sampling time or if the ADCLK is slow, the sampling time can be adjusted. The SSTSH[7:0] bits should be set while the ADST bit in ADCSR is 0. The set value for sampling time should be 4 or more states and 255 or less states. The sampling time should be 0.6 µs or longer. For example, when the ADCLK is 50 MHz, the lower limit of the set value for sampling time is 30 states.

SHANS[2:0] Bits (Channel-Dedicated Sample-and-Hold Circuit Bypass Select)

The SHANS[2:0] bits select whether to use or not use (bypass) AN000 to AN002 channel-dedicated sample-and-hold circuits. The SHANS[0] bit selects AN000, SHANS[1] bit selects AN001, and SHANS[2] bit selects AN002. The SHANS[2:0] bits should be set while the ADST bit in ADCSR is 0.

If any channel from among AN000 to AN002 is selected for group B while operation is in group scan mode under group A priority control, make the setting to bypass the channel's dedicated sample-and-hold circuit.

35.2.12 A/D Group Scan Priority Control Register (ADGSPCR)

Address(es): 0008 9080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PGS	Group-A priority control setting bit*1	0: Operation is without group A priority control 1: Operation is with group A priority control	R/W
b1	GBRSCN	Group B restart setting bit	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Scanning for group B is not restarted after having been discontinued due to group A priority control. 1: Scanning for group B is restarted after having been discontinued due to group A priority control.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Single-cycle scan continuous activation bit for Group B*2	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Single-cycle scans through group B are not continuously activated. 1: Single-cycle scans through group B are continuously activated.	R/W

Note 1. When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be 01b (group scan mode). If the bits are set to any other values, operation is not guaranteed.
Note 2. When the GBRP bit has been set to 1, single-cycle scan is performed continuously on group B regardless of the setting of the GBRSCN bit.

Register ADGSPCR is used to make settings for priority control of A/D conversion in group-scan mode under group A priority control.

PGS Bit (Group A Priority Control Setting)

This bit sets the priority of operation on group A. Set this bit to 1 when giving priority to operation on group A.
When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode). If the bits are set to any other values, operation is not guaranteed.
When the PGS bit has been set to 0, clear operation must be performed by software according to section 35.6.2, Notes on Stopping A/D Conversion. When the PGS bit has been set to 1, make settings according to section 34.3.4.4, Operation under Group-A Priority Control in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

GBRSCN Bit (Group B Restart Setting)

This bit controls the restarting of scan operation on group B when operation on group A is given priority.
If a scan operation on group B has been stopped by a group A trigger input with the GBRSCN bit set to 1, the scan operation is restarted on completion of the A/D conversion on group A. Also, if a group B trigger is input during A/D conversion on group A, the scan operation on group B is restarted on completion of the A/D conversion on group A. However, if group A triggers are input continuously, the scan operation on group B is not restarted.
If the GBRSCN bit has been set to 0, triggers that are input during A/D conversion are ignored. Also, the ADCSR.ADST bit must be 0 when the GBRSCN bit is to be set.
The setting of the GBRSCN bit becomes valid when the PGS bit is set to 1.

GBRP Bit (Single-Cycle Scan Continuous Activation for Group B)

This bit is set when a single-cycle scan operation is to be performed continuously on group B.

Setting the GBRP bit to 1 starts a single-cycle scan on group B. On completion of the scan, another single-cycle scan on group B is automatically started. If an A/D conversion on group B has been stopped due to an operation on group A that takes priority, single-cycle scan on group B is automatically restarted on completion of the A/D conversion on group A. Disable group B trigger input before setting the GBRP bit to 1. Setting the GBRP bit to 1 invalidates the setting of the GBRSCN bit.

The ADCSR.ADST bit must be 0 when the GBRP bit is to be set.

The setting of the GBRP bit is valid when the PGS bit is 1.

35.2.13 Comparator Operating-Mode Selection Register 0 (ADCMPMD0)

Address(es): 0008 90E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CEN002[1:0]		CEN001[1:0]		CEN000[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CEN000[1:0]	Comparator selection bits for AN000	b1 b0 0 0: The comparator is not in use. 0 1: The comparator is in use for comparison with the low level (detection of input voltages that are lower than the low-side reference voltage). 1 0: The comparator is in use for comparison with the high level (detection of input voltages that are higher than the high-side reference voltage). 1 1: The comparator is in use as a window comparator (detecting input voltages that are beyond the range from the low-side reference voltage to the high-side reference voltage).	R/W
b2, b3	CEN001[1:0]	Comparator selection bits for AN001	b2 b3 0 0: The comparator is not in use. 0 1: The comparator is in use for comparison with the low level (detection of input voltages that are lower than the low-side reference voltage). 1 0: The comparator is in use for comparison with the high level (detection of input voltages that are higher than the high-side reference voltage). 1 1: The comparator is in use as a window comparator (detecting input voltages that are beyond the range from the low-side reference voltage to the high-side reference voltage).	R/W
b5, b4	CEN002[1:0]	Comparator selection bits for AN002	b5 b4 0 0: The comparator is not in use. 0 1: The comparator is in use for comparison with the low level (detection of input voltages that are lower than the low-side reference voltage). 1 0: The comparator is in use for comparison with the high level (detection of input voltages that are higher than the high-side reference voltage). 1 1: The comparator is in use as a window comparator (detecting input voltages that are beyond the range from the low-side reference voltage to the high-side reference voltage).	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The setting of the ADCMPMD0 register determines whether or not the comparator is in use.

CENn[1:0] Bits (ANn Comparator Selection) (n = 000 to 002)

These bits determine whether or not the given comparator is in use and if it is, its mode of operation.

35.2.14 Comparator Operating-Mode Selection Register 1 (ADCMPMD1)

Address(es): 0008 90E2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VSEVV 0	VSELH 0	—	—	REFH[2:0]			—	REFL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	REFL[2:0]	Comparator Low-Side Reference-Voltage Internal-Voltage Selection	b2 b1 b0 0 0 0: Disabled 0 0 1: AVCC0 × 1/8 0 1 0: AVCC0 × 2/8 0 1 1: AVCC0 × 3/8 1 0 0: AVCC0 × 4/8 1 0 1: AVCC0 × 5/8 1 1 0: AVCC0 × 6/8 1 1 1: AVCC0 × 7/8	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	REFH[2:0]	Comparator High-Side Reference-Voltage Internal-Voltage Selection	b6 b5 b4 0 0 0: Disabled 0 0 1: AVCC0 × 1/8 0 1 0: AVCC0 × 2/8 0 1 1: AVCC0 × 3/8 1 0 0: AVCC0 × 4/8 1 0 1: AVCC0 × 5/8 1 1 0: AVCC0 × 6/8 1 1 1: AVCC0 × 7/8	R/W
b8, b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	VSELH0	Comparator High-Side Reference-Voltage Selection	0: The voltage on the AN007 pin is input as the high-side reference-voltage. 1: The internal voltage selected by the REFH[2:0] bits is input as the high-side reference-voltage.	R/W
b10	VSEVV0	Comparator Low-Side Reference-Voltage Selection Bit	0: The voltage on the AN003 pin is input as the high-side reference-voltage. 1: The internal voltage selected by the REFL[2:0] bits is input as the high-side reference-voltage.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADCMPMD1 register is used to set the inputs for the comparator and the reference voltages.

REFL[2:0] Bits (Comparator Low-Side Reference-Voltage Internal-Voltage Selection)

These bits are used to set the internal-voltage to be used as the low-side reference-voltage for the comparator. The range of usable settings differs with the conditions of usage, so see section 43, Electrical Characteristics [64- and 48-Pin Versions], regarding the range of REFL voltage.

REFH[2:0] Bits (Comparator High-Side Reference-Voltage Internal-Voltage Selection)

These bits are used to set the internal-voltage to be used as the high-side reference-voltage for the comparator. The range of usable settings differs with the conditions of usage, so see section 43, Electrical Characteristics [64- and 48-Pin Versions], regarding the range of REFL voltage.

VSELH0 Bit (Comparator High-Side Reference-Voltage Selection)

This bit selects how the high-side reference voltage for the comparator is input.

VSELL0 Bit (Comparator High-Side Reference-Voltage Selection)

This bit selects how the low-side reference voltage for the comparator is input.

35.2.15 Comparator Filter-Mode Register (ADCMPNR0)

Address(es): 0008 90E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	C002NR[3:0]				C001NR[3:0]				C000NR[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	C000NR[3:0]	Comparator Noise-Cancelling Filter Mode Selection Bits for AN000	b3 b0 0 0 0 0: Results of detection by the comparator are not sampled. 1 0 0 0: Results of detection by the comparator are sampled 16 times at PCLK. 1 0 0 1: Results of detection by the comparator are sampled 16 times at PCLK/2. 1 0 1 0: Results of detection by the comparator are sampled 16 times at PCLK/4. 1 0 1 1: Results of detection by the comparator are sampled 16 times at PCLK/8. 1 1 0 0: Results of detection by the comparator are sampled 16 times at PCLK/16. 1 1 0 1: Results of detection by the comparator are sampled 16 times at PCLK/128. Do not make settings other than those listed above.	R/W
b7 to b4	C001NR[3:0]	Comparator Noise-Cancelling Filter Mode Selection Bits for AN001	b7 b4 0 0 0 0: Results of detection by the comparator are not sampled. 1 0 0 0: Results of detection by the comparator are sampled 16 times at PCLK. 1 0 0 1: Results of detection by the comparator are sampled 16 times at PCLK/2. 1 0 1 0: Results of detection by the comparator are sampled 16 times at PCLK/4. 1 0 1 1: Results of detection by the comparator are sampled 16 times at PCLK/8. 1 1 0 0: Results of detection by the comparator are sampled 16 times at PCLK/16. 1 1 0 1: Results of detection by the comparator are sampled 16 times at PCLK/128. Do not make settings other than those listed above.	R/W
b11 to b8	C002NR[3:0]	Comparator Noise-Cancelling Filter Mode Selection Bits for AN002	b11 b8 0 0 0 0: Results of detection by the comparator are not sampled. 1 0 0 0: Results of detection by the comparator are sampled 16 times at PCLK. 1 0 0 1: Results of detection by the comparator are sampled 16 times at PCLK/2. 1 0 1 0: Results of detection by the comparator are sampled 16 times at PCLK/4. 1 0 1 1: Results of detection by the comparator are sampled 16 times at PCLK/8. 1 1 0 0: Results of detection by the comparator are sampled 16 times at PCLK/16. 1 1 0 1: Results of detection by the comparator are sampled 16 times at PCLK/128. Do not make settings other than those listed above.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Register ADCMPNR0 is used to make settings for processing by the noise filter of the results of detection by the comparator.

CnNR[3:0] Bits (ANn Comparator Noise-Cancelling Filter Mode Selection) (n = 000 to 002)

These bits set the operation of the noise filter for the results of detection by the ANn comparator. The corresponding ADCMPFR.CnFLAG is set if “detected” is the result from all samples of the results of detection by the comparator in accord with the specified conditions. At this time, an activation request in the form of a comparator interrupt (CMP0 to CMP2) or port-output enable 3 signal can be produced in accord with the setting in the ADCMPSEL register.

35.2.16 Comparator Detection Flag Register (ADCMPFR)

Address(es): 0008 90E8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	C002FLAG	C001FLAG	C000FLAG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C000FLAG	Comparator Detection Flag for AN000	0: The comparator has not detected the condition. 1: The comparator has detected the condition.	R/W*1
b1	C001FLAG	Comparator Detection Flag for AN001	0: The comparator has not detected the condition. 1: The comparator has detected the condition.	R/W*1
b2	C002FLAG	Comparator Detection Flag for AN002	0: The comparator has not detected the condition. 1: The comparator has detected the condition.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The only writable value is 0, which clears the flag.

The ADCMPFR register contains flags that indicate the state (detection or non-detection) of the comparators.

CnFLAG flags (Comparator Detection Flag for ANn; n = 000 to 002)

Each flag indicates the state of a comparator in terms of detection or non-detection.

[Setting condition]

- All samples that are collected from the results of detection operation by the comparator according to the conditions set by the ADCMPNR0.CnNR[3:0] bits (n = 000 to 002) indicate detection.

[Clearing condition]

- Software writing 0 to the flag.

35.2.17 Comparator Interrupt Selection Register (ADCMPSEL)

Address(es): 0008 90EAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	POERQ002	POERQ001	POERQ000	—	—	—	—	—	IE002	IE001	IE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IE000	Comparator Detection-Interrupt (CMP0) Enable for AN000	0: Interrupt generation is disabled. 1: Interrupt generation is enabled.	R/W
b1	IE001	Comparator Detection-Interrupt (CMP1) Enable for AN001	0: Interrupt generation is disabled. 1: Interrupt generation is enabled.	R/W
b2	IE002	Comparator Detection-Interrupt (CMP2) Enable for AN002	0: Interrupt generation is disabled. 1: Interrupt generation is enabled.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	POERQ000	POE Request Generation on Comparator Detection Setting for AN000	0: POE request generation on comparator detection is disabled for AN000. 1: POE request generation on comparator detection is enabled for AN000.	R/W
b9	POERQ001	POE Request Generation on Comparator Detection Setting for AN001	0: POE request generation on comparator detection is disabled for AN001. 1: POE request generation on comparator detection is enabled for AN001.	R/W
b10	POERQ002	POE Request Generation on Comparator Detection Setting Bit for AN002	0: POE request generation on comparator detection is disabled for AN002. 1: POE request generation on comparator detection is enabled for AN002.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Settings in ADCMPSEL determine if the comparator detection flags act as sources for CPU interrupts or POE signals.

IEn (ANn Comparator Detection-Interrupt Enable) Bit (n = 000 to 002)

Each bit disables or enables the generation of an interrupt (CMPn) in response to detection by the corresponding comparator.

POERQn Bit (ANn POE Request Generation on Comparator Detection Setting) (n = 000 to 002)

Each bit disables or enables the generation of a POE request in response to detection by the corresponding comparator. The POE request signal is the logical OR of the detection signals from comparators selected by the POERQn bits.

35.3 Operation

35.3.1 Scanning Operation

See section 34.3.1, Scanning Operation in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.2 Single-Cycle Scan Mode

See section 34.3.2, Single-Cycle Scan Mode in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.3 Continuous Scan Mode

See section 34.3.3, Continuous Scan Mode in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.4 Group Scan Mode

See section 34.3.4, Group Scan Mode in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.5 Analog Input Sampling and Scan Conversion Time

See section 34.3.5, Analog Input Sampling and Scan Conversion Time in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.6 Usage Example of Automatic Register Clearing Function

See section 34.3.6, Usage Example of Automatic Register Clearing Function in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.7 A/D-Converted Value Addition Function

See section 34.3.7, A/D-Converted Value Addition Function in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.8 Discharging the Analog Pins

See section 34.3.8, Discharging the Analog Pins in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.3.9 Starting A/D Conversion with Asynchronous Trigger

The A/D conversion can be started by the input of an asynchronous trigger. To start up the A/D converter by an asynchronous trigger, the A/D conversion start trigger select bits (ADSTRGR.TRGA[4:0]) should be set to 00000b and a high-level signal should be input to the asynchronous trigger (ADTRG0# pin), and both the ADCSR.TRGE and ADCSR.EXTRG bits should be set to 1. Figure 35.3 shows a timing of the asynchronous trigger input.
For the time between setting the ADST bit and starting A/D conversion, refer to section 35.6.3, A/D Conversion Restarting Timing and Termination Timing.

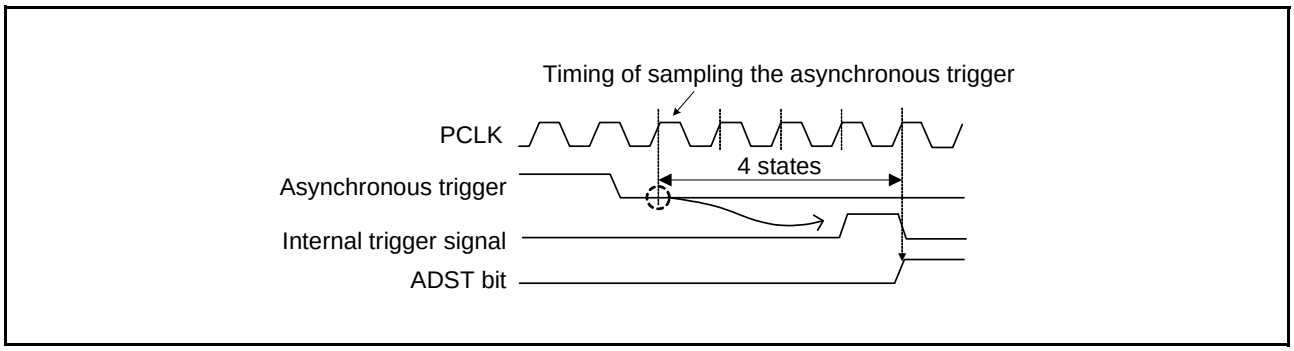


Figure 35.3 Asynchronous Trigger Input Timing

35.3.10 Starting A/D Conversion with Synchronous Trigger from Peripheral Modules

The A/D conversion can be started by a synchronous trigger of the MTU3, GPT. To start the A/D conversion by a synchronous trigger, the ADCSR.TRGE bit should be set to 1, the ADCSR.EXTRG bit should be cleared to 0, and the relevant source should be selected by ADSTRGR.TRSA[4:0] and TRSB[4:0] bits.

35.3.11 Window Comparator

The circuits for some ANn pins (those with n = 000 to 002) incorporate a window comparator. Along with the window comparator, which is capable of detecting the application to an ANn pin of voltages beyond the range from the low-side reference-voltage to the high-side reference-voltage, operation as a low-level comparator for detecting the application of any voltage lower than the low-side reference-voltage or as a high-level comparator for detecting the application of any voltage higher than the high-side reference-voltage can be selected. The operating mode of the window comparator is selected by the setting of the ADCMPMD0.CENn[1:0] bits (n = 000 to 002). Voltages that are externally supplied through the AN003/CVREFL pin for the low side and the AN007/CVREFH pin for the high side, or an internally generated reference voltage (of the form 1/8 × AVCC0 to 7/8 × AVCC0) are selectable as the reference voltages for the window comparator. A noise-cancelling filter for the detection signal from the window comparator is available for suppressing the output of false detection signals due to noise. An interrupt request for the CPU (CMP0 to CMP2) for the CPU or a POE signal (to place a complementary PWM output pin from the MTU3 module or a GPT output pin in the high impedance state) can be generated in response to detection by the comparator. The detection signal from the comparator is usable as a trigger to control counting by or as a source of requests for negation of an output from the general PWM timer (GPT). For details, refer to section 24, General PWM Timer (GPT).

An example of settings for the window comparator is described below.

1. Set the VSELL0 and VSELH0 bits in register ADCMPMD1 to select how the reference voltages are to be applied. When the internally generated reference voltage is selected, set the low- or high-side reference voltage by setting the REFL[2:0] and REFH[2:0] bits in ADCMPMD1.
2. Set the ADCMPNR0.CnNR[3:0] bits for the given comparator (n = 000 to 002) to determine whether or not the noise-cancelling filter will be used on the result of detection by the comparator.
3. Set the ADCMPSEL.IEn bits (n = 000 to 002) as required if an interrupt request for the CPU (CMP0 to CMP2) is to be generated in response to the detection signal from the comparator. Also set the ADCMPSEL.POERQm (n = 000 to 002) bits as required if a POE request is to be generated in response to the detection signal from the comparator. The POE request is generated as the logical OR of the detection signals selected by the POERQm bits.
4. Set the ADCMPMD0.CENn[1:0] (n = 000 to 002) bits to select the operating mode of the pin for use in detection and of the window comparator.

Figure 35.4 to Figure 35.6 depict examples of operation of the window comparator.

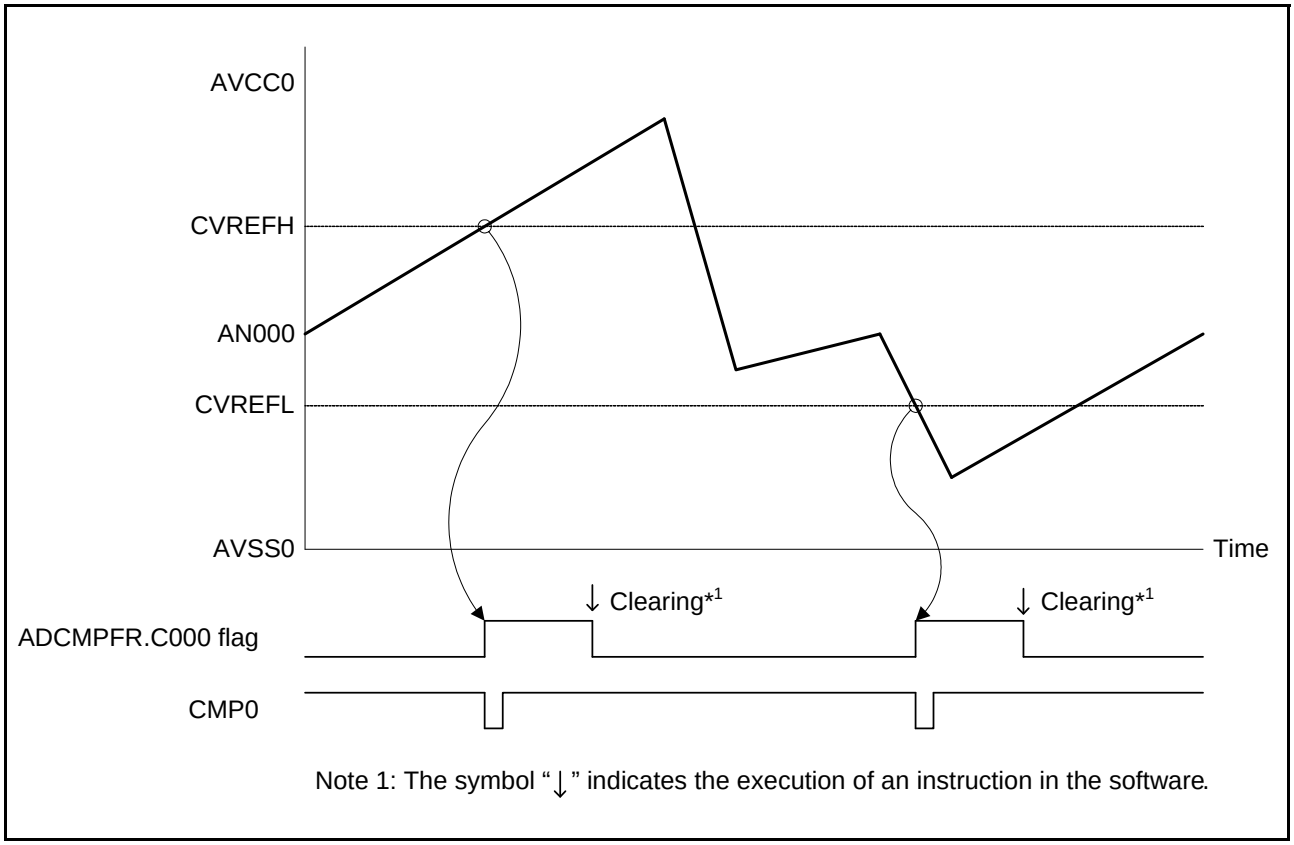


Figure 35.4 Example 1 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 11b)

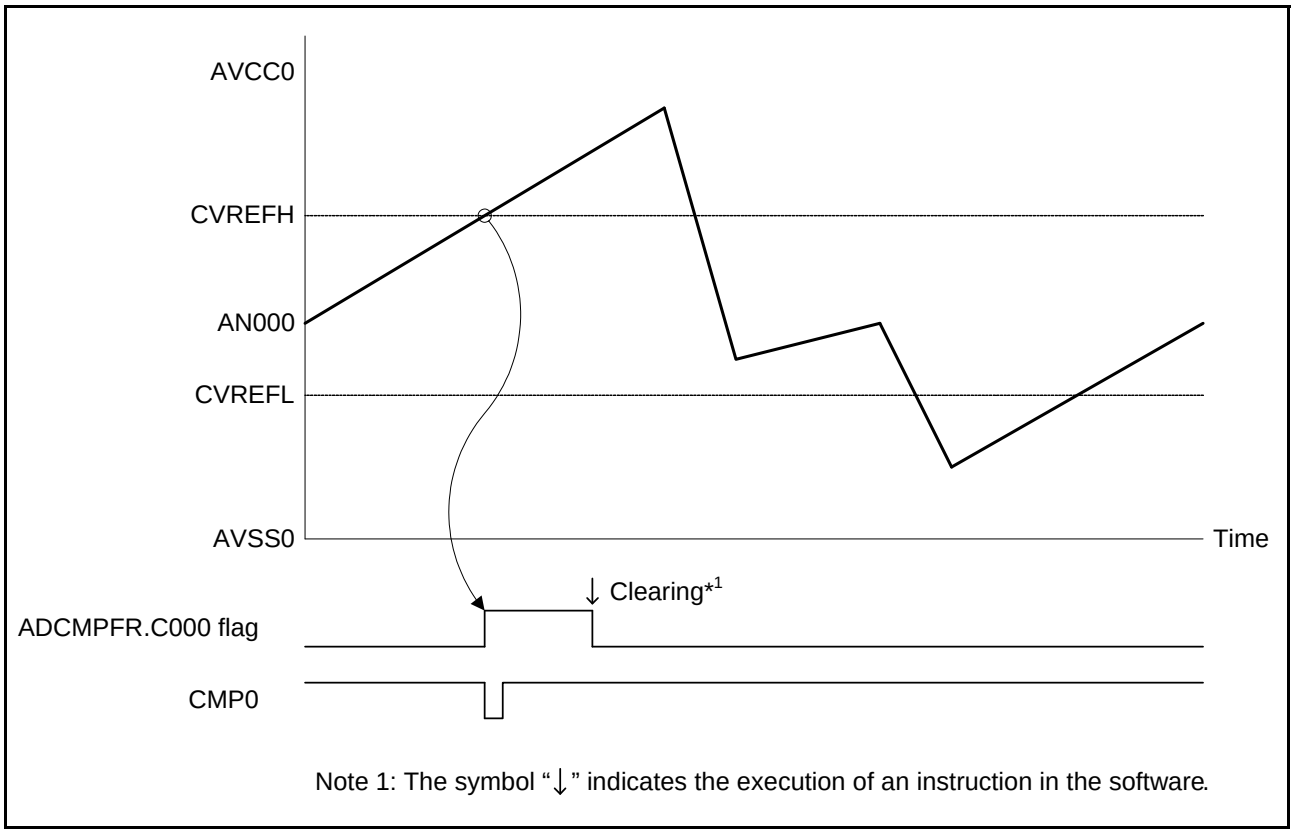


Figure 35.5 Example 2 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 10b)

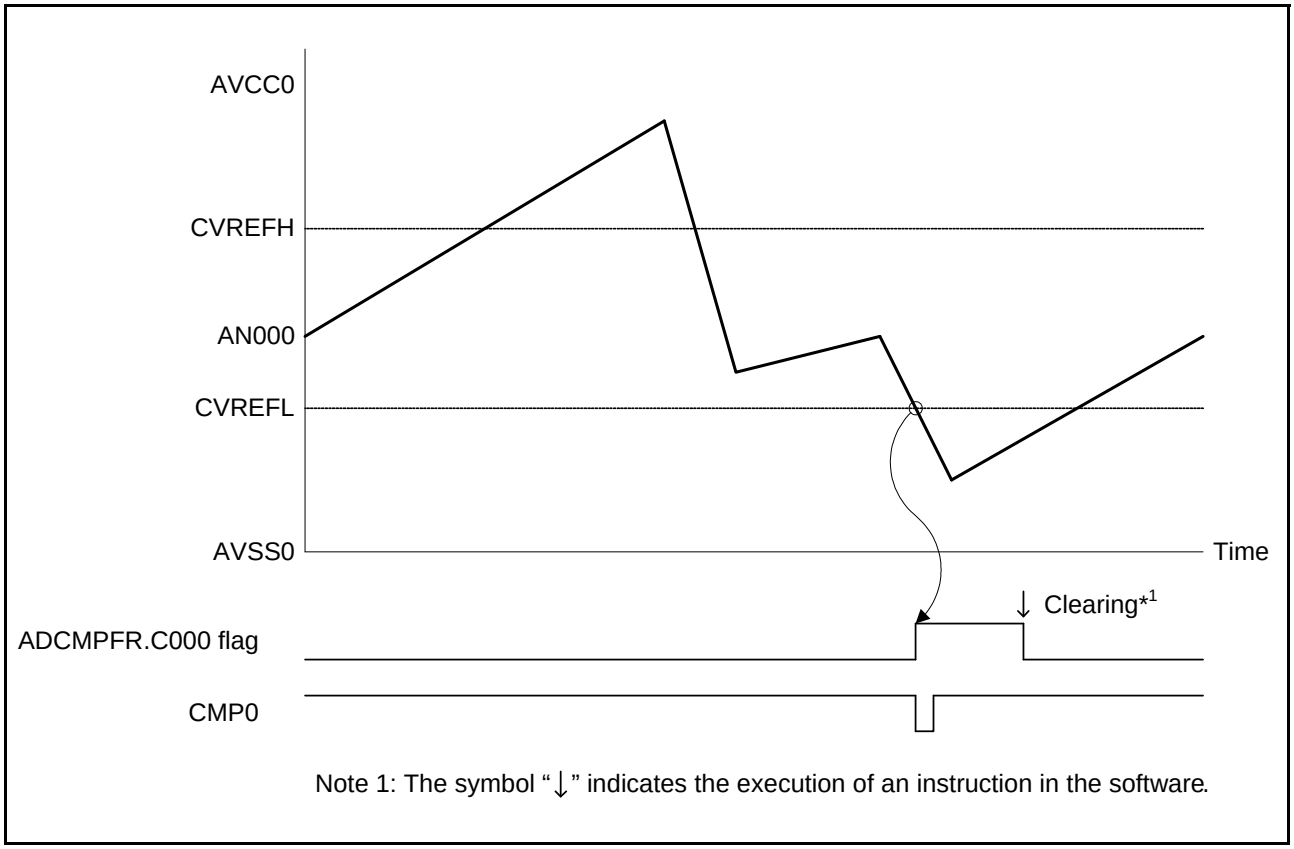


Figure 35.6 Example 3 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 01b)

35.4 Interrupt Sources and DMA Transfer Requests

35.4.1 Interrupt Request on Completion of Each Scanning Conversion

The 12-bit A/D converter can send scan end interrupt requests S12ADI and S12GBADI to the CPU.
Setting the ADCSR.ADIE bit to 1 and 0 enables and disables an S12ADI interrupt, respectively; similarly, setting the ADCSR.GBADIE bit to 1 and 0 enables and disables a S12GBADI interrupt, respectively.
In addition, the DTC or DMACA can be started up when an S12ADI or an S12GBADI interrupt is generated. Using an S12ADI or an S12GBADI interrupt to allow the DTC or DMACA to read the converted data enables continuous conversion without burden on software.
For details on DTC settings, see section 19, Data Transfer Controller (DTCa), and for details on DMACA settings, see section 18, DMA Controller (DMACA).

35.4.2 Interrupt Requests at the Time of Detection by the Comparator

The comparator is capable of generating interrupt requests for the CPU (CMPm, where m = 0 to 2) in response to detection. Setting the ADCMPSEL.IEn (n = 000 to 002) to 1 or 0 respectively enables or disables the CMPm interrupt. Furthermore, the DTC or DMACA can be activated at the time of CMPm interrupt. See section 19, Data Transfer Controller (DTCa), for the DTC settings and section 18, DMA Controller (DMACA), for the DMACA settings.

35.5 A/D Conversion Accuracy Definitions

See section 34.5, A/D Conversion Accuracy Definitions in section 34, 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions].

35.6 Usage Notes

35.6.1 Notes on Reading Data registers

The A/D data registers, A/D data duplication register, and A/D self-diagnosis data register should be read in word units. If a register is read twice in byte units, that is, the upper byte and lower byte are separately read, the A/D converted value having been read first may disagree with the A/D converted value having been read for the second time. To prevent this, the data registers should never be read in byte units.

35.6.2 Notes on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger has been selected as the condition for starting A/D conversion, follow the procedure in Figure 35.7.

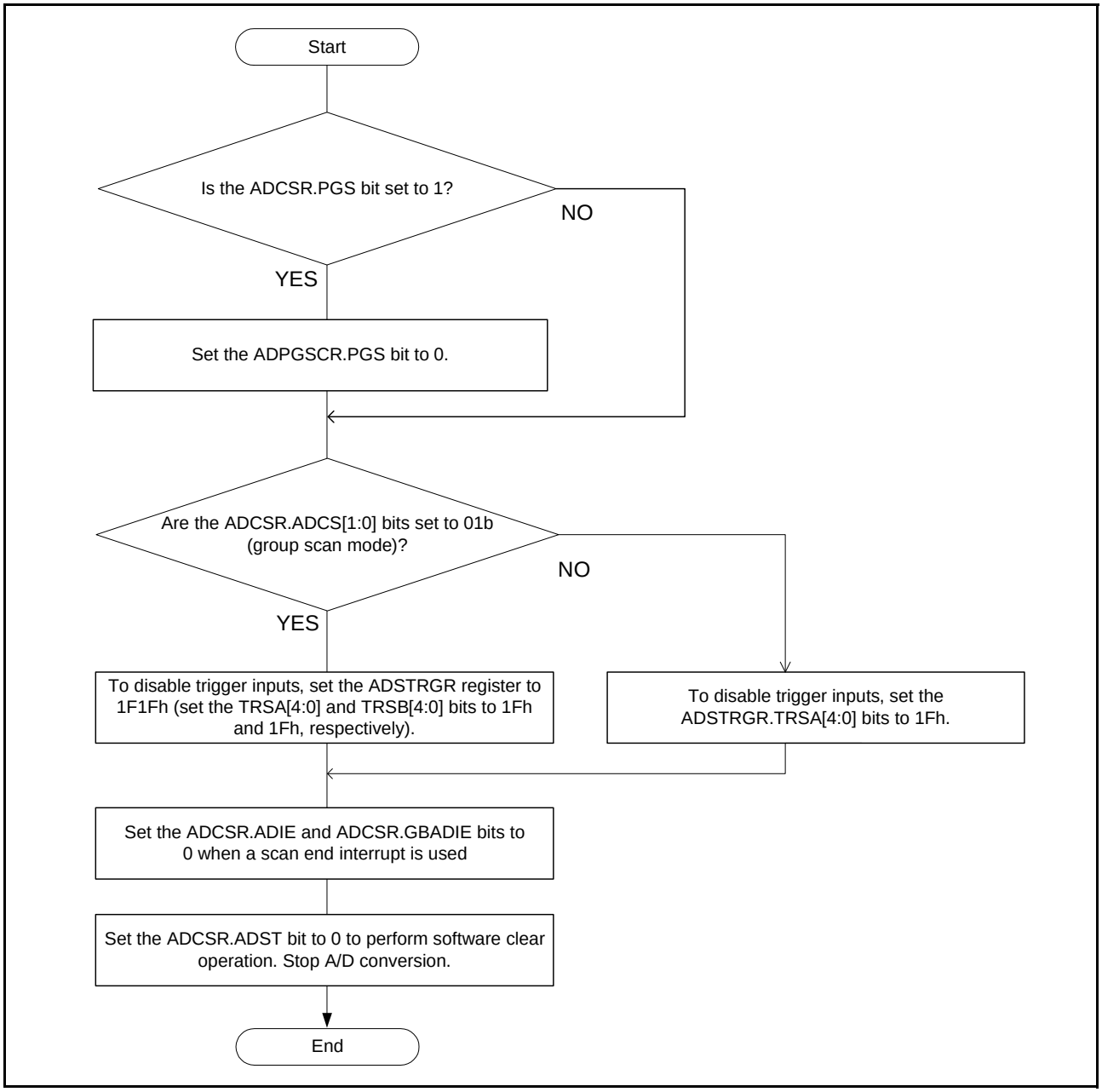


Figure 35.7 Procedures for Clear Operation by Software through the ADCSR.ADST Bit

35.6.3 A/D Conversion Restarting Timing and Termination Timing

It takes a maximum of four ADCLK cycles for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADST bit in ADCSR to 1. It takes a maximum of two ADCLK cycles for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADST bit in ADCSR to 0.

35.6.4 Notes on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D converted data is overwritten with the second A/D converted data in the case that the CPU does not complete reading out the A/D converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

35.6.5 Module Stop Function Setting

Operation of the 12-bit A/D converter can be disabled or enabled using the module stop control register. The 12-bit A/D converter is stopped a the initial value.
After the module stop state is canceled, wait for 1 µs to start A/D conversion. For details, see section 12, Low Power Consumption.

35.6.6 Notes on Entering Low Power Consumption States

Before entering module stop mode or software standby mode, make sure to stop A/D conversion. Here, set the ADST bit in ADCSR to 0, and allow time for stopping the analog unit of the 12-bit A/D converter.
Follow the procedure given below to secure this time.
Follow the procedure for clear operation by software through the ADCSR.ADST bit, shown in Figure 35.7, to set the ADCSR.ADST bit to 0. After confirming that the A/D converter has been stopped, place the MCU in the module stop state mode or software standby mode.
Furthermore, sections of the 12-bit A/D converter enter the state of waiting to operate when the converter is placed in module-stop mode, on software standby, or on deep software standby. Setting the MSTPCRA.MSTPA24 to 1 fully places the 12-bit A/D converter on standby. In this case, wait for a further 10 ms to start A/D conversion after release from the module-stop mode, software standby, or deep software standby.

35.6.7 Allowable Impedance of Signal Source

To achieve high-speed conversion of 1.0 µs, the analog input pins of this MCU are designed so that the conversion accuracy is guaranteed if the impedance of the input signal source is 3 kΩ or less. If an external capacitor of large capacitance is attached in the application in which only a single pin input is converted in single-cycle scan mode, the only load on input is virtually 10 kΩ of the internal input resistor; therefore, the impedance of the signal source can be ignored. Being a low-pass filter, however, an analog input circuit may not follow the analog signal with a large differential coefficient (e. g., larger than 5 mV/µs) as shown in Figure 35.8. When high-speed analog signals are to be converted or multiple pins are to be converted in scan mode, a low-impedance buffer should be used.

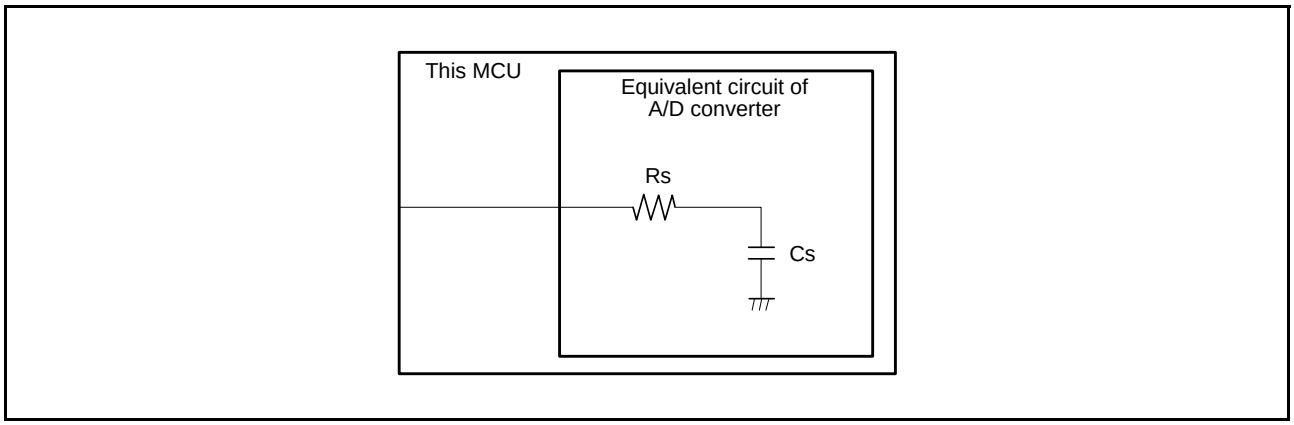


Figure 35.8 Internal Equivalent Circuit of Analog Input Pin

Table 35.8 Specifications of Analog Input Pins

Item		Min.	Max.	Unit
Allowable signal source impedance*1		—	3	kΩ
Internal equivalent circuit of a pin	Rs	—	10	kΩ
	Cs	—	8	pF

Note 1. The value differs depending on the analog power supply voltage and analog input pins to be used. For details, see section 43., Electrical Characteristics [64- and 48-Pin Versions].

35.6.8 Influence on Absolute Accuracy

Attaching a capacitor creates coupling with GND and may affect the absolute accuracy when noisy GND is used; therefore, a capacitor should be connected to electrically stable GND such as AVSS0.
The filter circuit should be designed so that it does not interfere digital signals or it does not serve as an antenna on the circuit board.

35.6.9 Voltage Range of Analog Power Supply Pins

If this MCU is used with the voltages outside the following ranges, the reliability of the MCU may be affected.

- Analog input voltage range
  Voltage (VAN) applied to analog input pins ANn: VREFL0 ≤ VAN ≤ VREFH0
- Relationship between power supply pin pairs (AVCC0–AVSS0, VREFH0–VREFL0, VCC–VSS)
  AVSS0 = VSS
  A 0.1-µF capacitor should be connected between each pair of power supply pins to create a closed loop with the shortest rout possible as shown in Figure 35.9, and connection should be made so that the following conditions are satisfied at the supply side.
  VREFL0 = AVSS0 = VSS
  When the A/D converter is not used, the following conditions should be satisfied.
  VREFH0 = AVCC0 = VCC and VREFL0 = AVSS0 = VSS
- Setting ranges of VREFH0 and VREFL0
  Specify a reference voltage through the VREFH0 pin so that VREFH0 is less than or equal to AVCC0.
  Configure the VREFL0 pin so that VREFL0 is equal to AVSS0 and VSS.

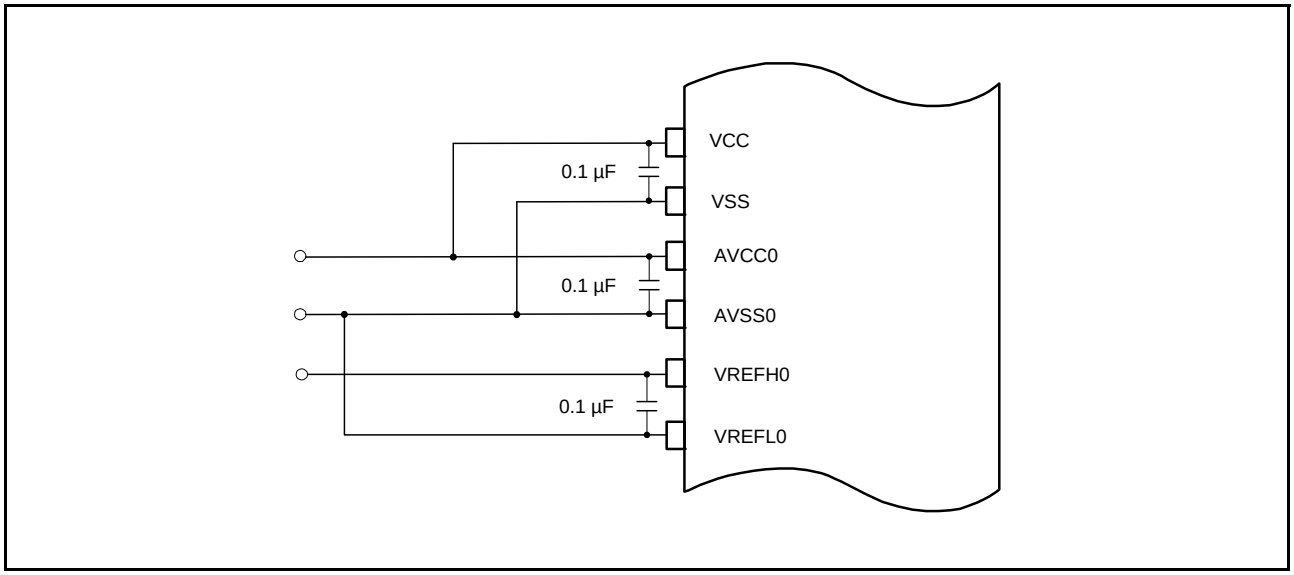


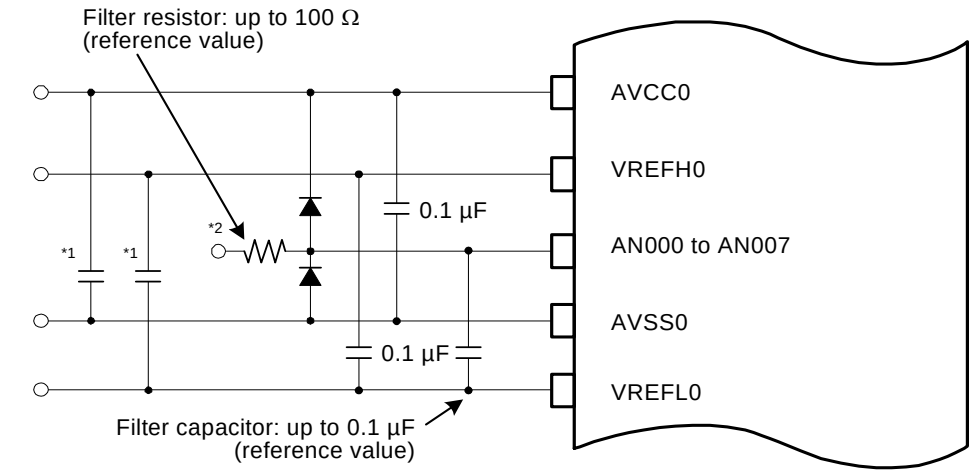
Figure 35.9 Example of Connecting Power Supply Pins

35.6.10 Notes on Board Design

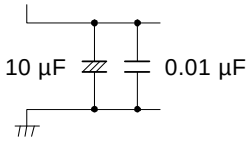
The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or placed near each other. If these rules are not followed, noise will be produced on analog signals and A/D conversion accuracy will be affected. The analog input pins (AN000 to AN007), analog reference voltages (VREFH0 and VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

35.6.11 Notes on Noise Prevention

To prevent the analog input pins (AN000 to AN007) from being destroyed by abnormal voltage such as excessive surge, a capacitor should be inserted between AVCC0 and AVSS0 and between VREFH0 and VREFL0, and a protection circuit should be connected to protect the analog input pins (AN000 to AN007) as shown Figure 35.10.
Moreover, connect the filter capacitor to be connected to analog input pins (AN000 to AN007) to VREFL0. The 0.1 µF capacitor shown in Figure 35.10 must be placed as close as possible to the pin.
Note that an error may occur when the filter capacitor is connected as shown in Figure 35.10, because the input voltages of the analog input pins (AN000 to AN007) are averaged. Accordingly, determine circuit constant upon careful consideration.



Note: The values shown here are reference values.
Note 1.



Note 2. Signal source impedance: up to 3 kΩ

Figure 35.10 Sample Protection Circuit for Analog Inputs

36. 10-Bit A/D Converter (AD)

36.1 Overview

This MCU includes a 10-bit successive approximation A/D converter. Up to 20 channel analog inputs, can be selected. The 10-bit A/D converter converts a maximum of 20 selected channels of analog inputs into a 10-bit digital value through successive approximation.

The A/D converter has two operating modes: single scan mode in which the analog inputs of up to 20 arbitrarily selected channels are converted for only once in ascending channel order; and continuous scan mode in which the analog inputs of up to 20 arbitrarily selected channels are continuously converted in ascending channel order.

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages internally generated in the 10-bit A/D converter is converted.

Table 36.1 lists the specifications of the 10-bit A/D converter and Table 36.2 indicates the functions of the 10-bit A/D converter. Figure 36.1 shows a block diagram of the 10-bit A/D converter.

Table 36.1 Specifications of 10-bit A/D Converter

Item	Specifications
Number of units	One unit
Input channels	20 channels
A/D conversion method	Successive approximation method
Resolution	10 bits
Conversion time	AN0 to AN7: 0.5 µs per channel (when A/D conversion clock ADCLK = 100 MHz) AN8 to AN19: 1.0 µs per channel (when A/D conversion clock ADCLK = 50 MHz)
A/D conversion clock	Peripheral module clock PCLK*1 and A/D conversion clock ADCLK*1 can be set so that the frequency division ratio should be one of the following. PCLK to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuits.
Data registers	For analog input: 20 data registers For self-diagnosis: One data register The A/D conversion result is stored in 10-bit or 8-bit A/D data registers. In addition mode, A/D conversion results are added and stored in A/D data registers as 12-bit data.
Operating modes	• Single Scan Mode: A/D conversion is performed for only once on the analog inputs of up to 20 arbitrarily selected channels. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 20 arbitrarily selected channels.
Conditions of A/D conversion start	• Software trigger • Synchronous trigger Trigger by multi-function timer pulse unit 3 (MTU3) or general PWM timer (GPT) • Asynchronous trigger A/D conversion can be triggered from the ADTRG# pin.
Function	• Sample-and-hold function • Variable sampling state count • Self-diagnosis of 10-bit A/D converter • A/D-converted value addition mode
Interrupt source	• In the modes A/D scan end interrupt (ADI0) request can be generated on completion of single scan. • ADI0 interrupt can activate DMA controller (DMACA) or data transfer controller (DTC).
Low power consumption function	• Module stop state can be specified.

Note 1. Peripheral module clock PCLK is set according to the setting of SCKCR.PCKB[3:0] and A/D conversion clock ADCLK is set according to the setting of SCKCR.PCLKC[3:0].

Table 36.2 Functions of 10-bit A/D Converter

Item			Function
Analog input channel			AN0 to AN19
A/D conversion start conditions	Software	Software trigger	Enabled
	Asynchronous trigger	ADTRG#	Enabled
	Synchronous trigger (MTU3)	TRGA0N	TRGA compare match/input capture from MTU0
		TRGA1N	TRGA compare match/input capture from MTU1
		TRGA2N	TRGA compare match/input capture from MTU2
		TRGA3N	TRGA compare match/input capture from MTU3
		TRGA4N	MTU4.TRGA compare match/input capture or MTU4.TCNT underflow (trough) in complementary PWM mode
		TRGA6N	TRGA compare match/input capture from MTU6
		TRGA7N	MTU7.TRGA compare match/input capture or MTU7.TCNT underflow (trough) in complementary PWM mode
		TRG0AN	TRGE compare match from MTU0
		TRG4AN	MTU4.TADCORA and MTU4.TCNT compare match
		TRG4BN	MTU4.TADCORB and MTU4.TCNT compare match
		TRG4AN or TRG4BN	MTU4.TADCORA and MTU4.TCNT compare match or MTU4.TADCORB and MTU4.TCNT compare match
		TRG4ABN	MTU4.TADCORA and MTU4.TCNT compare match and MTU4.TADCORB and MTU4.TCNT compare match (interrupt skipping function 2)
		TRG7AN	MTU7.TADCORA and MTU7.TCNT compare match
		TRG7BN	MTU7.TADCORB and MTU7.TCNT compare match
		TRG7AN or TRG7BN	MTU7.TADCORA and MTU7.TCNT compare match and MTU7.TADCORB and MTU7.TCNT compare match
		TRG7ABN	MTU7.TADCORA and MTU7.TCNT compare match and MTU7.TADCORB and MTU7.TCNT compare match (interrupt skipping function 2)

Table 36.2 Functions of 10-bit A/D Converter

Item			Function
A/D conversion start conditions	Synchronous trigger (GPT)	GTADTRA0	GPT0.GTADTRA compare match
		GTADTRB0	GPT0.GTADTRB compare match
		GTADTRA1	GPT1.GTADTRA compare match
		GTADTRB1	GPT1.GTADTRB compare match
		GTADTRA2	GPT2.GTADTRA compare match
		GTADTRB2	GPT2.GTADTRB compare match
		GTADTRA3	GPT3.GTADTRA compare match
		GTADTRB3	GPT3.GTADTRB compare match
		GTADTRA0 or GTADTRB0	GPT0.GTADTRA compare match or GPT0.GTADTRB compare match
		GTADTRA1 or GTADTRB1	GPT1.GTADTRA compare match or GPT1.GTADTRB compare match
		GTADTRA2 or GTADTRB2	GPT2.GTADTRA compare match or GPT2.GTADTRB compare match
		GTADTRA3 or GTADTRB3	GPT3.GTADTRA compare match or GPT3.GTADTRB compare match
		GTADTRA4	GPT4.GTADTRA compare match
		GTADTRB4	GPT4.GTADTRB compare match
		GTADTRA5	GPT5.GTADTRA compare match
		GTADTRB5	GPT5.GTADTRB compare match
		GTADTRA6	GPT6.GTADTRA compare match
		GTADTRB6	GPT6.GTADTRB compare match
		GTADTRA7	GPT7.GTADTRA compare match
		GTADTRB7	GPT7.GTADTRB compare match
		GTADTRA4 or GTADTRB4	GPT4.GTADTRA compare match or GPT4.GTADTRB compare match
		GTADTRA5 or GTADTRB5	GPT5.GTADTRA compare match, or GPT5.GTADTRB compare match
		GTADTRA6 or GTADTRB6	GPT6.GTADTRA compare match or GPT6.GTADTRB compare match
		GTADTRA7 or GTADTRB7	GPT7.GTADTRA compare match or GPT7.GTADTRB compare match
Interrupt			ADI0 interrupt
Module stop function setting*1			MSTPCRA.MSTPA23 bit

Note 1. For details, see section 12, Low Power Consumption.

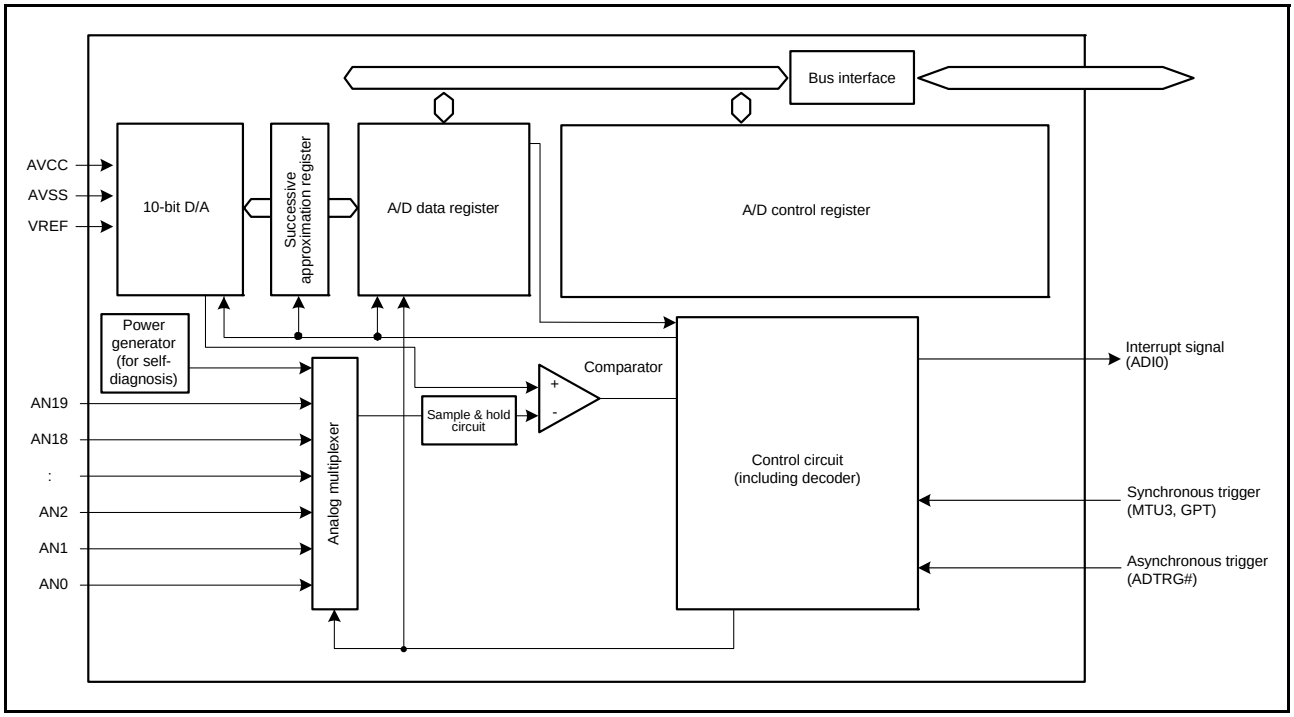


Figure 36.1 Block Diagram of 10-bit A/D Converter

Table 36.3 indicates the input pins of the 10-bit A/D converter.

Table 36.3 Input Pins of 10-bit A/D Converter

Pin Name	Input	Function
AVCC	Input	Analog block power supply pin
AVSS	Input	Analog block ground pin
VREF	Input	Reference power supply pin
AN0 to AN19	Input	Analog input pins
ADTRG#	Input	External trigger input pin for starting A/D conversion

36.2 Register Descriptions

36.2.1 A/D Data Registers y (ADDRy) (y = A to T)

ADDRy registers are 16-bit read-only registers which store the A/D conversion results of channels AN0 to AN19.

The A/D data registers use the following different formats depending on the setting of the A/D data register bit-precision specification bits (ADCER.ADPRC), the A/D data register format select bit (ADCER.ADRFMT), or A/D-converted value addition mode.

- ADCER.ADPRC = 0, ADCER.ADRFMT = 0 (The settings are for flush-right data with 10-bit precision)

Address: ADDRA: 0008 9820h to ADDRT: 0008 9846h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	AD[9:0]	Converted value [9:0]	10-bit A/D-converted value	R
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

- ADCER.ADPRC = 0, ADCER.ADRFMT = 1 (The settings are for flush-left data with 10-bit precision)

Address: ADDRA: 0008 9820h to ADDRT: 0008 9846h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b6	AD[9:0]	Converted value [9:0]	10-bit A/D-converted value	R

- ADCER.ADPRC = 1, ADCER.ADRFMT = 0 (The settings are for flush-right data with 8-bit precision)

Address: ADDRA: 0008 9820h to ADDRT: 0008 9846h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	AD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	AD[7:0]	Converted value [9:2]	8 higher-order bits of the 10-bit A/D converted value	R
b15 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

- ADCER.ADPRC = 1, ADCER.ADRFMT = 1 (The settings are for flush-left data with 8-bit precision)

Address: ADDRA: 0008 9820h to ADDRT: 0008 9846h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b8	AD[7:0]	Converted value [9:2]	8 higher-order bits of the 10-bit A/D converted value	R

- When A/D-converted value addition mode is selected

Address: ADDRA: 00089820h to ADDRT: 00089846h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b4	AD[11:0]	—	12-bit A/D-converted value addition result	R

When A/D-converted value addition mode is selected, the AD[11:0] bits in ADDRy show the value added by the A/D-converted value of the respective channels. In A/D-converted value addition mode, the setting of the ADRFMT bit in ADCER becomes invalid and the format of the register becomes flush-left data with 12-bit precision.

The following minimum and maximum values apply to channels on which A/D-converted value addition mode is selected.

First conversion: 0000h ≤ ADDRy (y = A to T) ≤ 3FF0h
(ADDRy (y = A to T): Bits 15 and 14 = 00b, bits 13 to 4 = AD9 to AD0, bits 3 to 0 = 0000b)
Second conversion: 0000h ≤ ADDRy (y = A to T) ≤ 7FE0h
(ADDRy (y = A to T): Bit 15 = 0, bits 14 to 4 = AD10 to AD0, bits 3 to 0 = 0000b)
Third conversion: 0000h ≤ ADDRy (y = A to T) ≤ BFD0h
(ADDRy (y = A to T): Bits 15 to 4 = AD11 to AD0, bits 3 to 0 = 0000b)
Fourth conversion: 0000h ≤ ADDRy (y = A to T) ≤ FFC0h
(ADDRy (y = A to T): Bits 15 to 4 = AD11 to AD0, bits 3 to 0 = 0000b)

36.2.2 A/D Self-Diagnosis Data Register (ADRD)

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the A/D converter's self-diagnosis. The following different formats are used depending on the setting of the A/D data register bit-precision specification bits (ADCER.ADPRC), or the A/D data register format select bit (ADRFMT) in ADCER. ADRD cannot be set to A/D-converted value addition mode.

- ADCER.ADPRC = 0, ADCER.ADRFMT = 0 (The settings are for flush-right data with 10-bit)

Address: 0008 981Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	—	—	AD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	AD[9:0]	Converted value [9:0]	10-bit A/D-converted value	R
b13 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREF × 0 has been executed. 1 0: Self-diagnosis using VREF × 1/2 has been executed. 1 1: Self-diagnosis using VREF × 1 has been executed. For details of self-diagnosis, see section 36.2.9, A/D Control Extended Register (ADCER).	R

- ADCER.ADPRC = 0, ADCER.ADRFMT = 1 (The settings are for flush-left data with 10-bit)

Address: 0008 981Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREF × 0 has been executed. 1 0: Self-diagnosis using VREF × 1/2 has been executed. 1 1: Self-diagnosis using VREF × 1 has been executed. For details of self-diagnosis, see section 36.2.9, A/D Control Extended Register (ADCER).	R
b5 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b6	AD[9:0]	Converted value [9:0]	10-bit A/D-converted value	R

- ADCER.ADPRC = 1, ADCER.ADRFMT = 0 (The settings are for flush-right data with 8-bit)

Address: 0008 981Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	—	—	—	—	AD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	AD[7:0]	Converted value [9:0]	10-bit A/D-converted value	R
b13 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREF × 0 has been executed. 1 0: Self-diagnosis using VREF × 1/2 has been executed. 1 1: Self-diagnosis using VREF × 1 has been executed. For details of self-diagnosis, see section 36.2.9, A/D Control Extended Register (ADCER).	R

- ADCER.ADPRC = 1, ADCER.ADRFMT = 1 (The settings are for flush-left data with 8-bit)

Address: 0008 981Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using VREF × 0 has been executed. 1 0: Self-diagnosis using VREF × 1/2 has been executed. 1 1: Self-diagnosis using VREF × 1 has been executed. For details of self-diagnosis, see section 36.2.9, A/D Control Extended Register (ADCER).	R
b5 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b6	AD[7:0]	Converted value [9:0]	10-bit A/D-converted value	R

36.2.3 A/D Control Register (ADCSR)

Address: 0008 9800h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS	—	ADIE	—	—	TRGE	EXTRG	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	EXTRG	Trigger Select*1	0: A/D conversion is started by the synchronous trigger (MTU3, GPT). 1: A/D conversion is started by the asynchronous trigger (ADTRG0#).	R/W
b9	TRGE	Trigger Start Enable	0: Disables A/D conversion to be started by the synchronous or asynchronous trigger. 1: Enables A/D conversion to be started by the synchronous or asynchronous trigger.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	ADIE	Scan End Interrupt Enable	0: Disables ADI interrupt generation upon scan completion. 1: Enables ADI interrupt generation upon scan completion.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	ADCS	Scan Mode Select	0: Single scan mode 1: Continuous scan mode	R/W
b15	ADST	A/D Conversion Start	0: Stops A/D conversion process. 1: Starts A/D conversion process.	R/W

Note 1. Starting A/D conversion using an external pin (asynchronous trigger)
If 1 is written to both the TRGE and EXTRG bits in ADCSR when a high-level signal is input to the external pin (ADTRG0#), and then if the ADTRG0# signal is driven low, the falling edge of ADTRG0# is detected and the scan conversion process is started. In this case, the pulse width of the low-level input must be at least 1.5 PCLK clock cycles.

ADCSR sets A/D conversion start trigger; enables/disables scan end interrupt; selects the scan mode; and starts or stops A/D conversion.

EXTRG Bit (Trigger Select)

The EXTRG bit selects the synchronous trigger or the asynchronous trigger as the trigger for starting A/D conversion.

TRGE Bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous trigger and the asynchronous trigger.

ADIE Bit (Scan End Interrupt Enable)

The ADIE bit enables or disables the A/D scan end interrupt (ADI0) in scans.

The ADI0 interrupt is generated when A/D conversion is completed if the ADIE bit is set to 1.

ADCS Bit (Scan Mode Select)

The ADCS bit selects the scan mode.
In single scan mode, A/D conversion is performed for the analog inputs of a maximum of 20 channels selected with the ADANSA0/1 register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, scan conversion is stopped.
In continuous scan mode, while the ADST bit in ADCSR is 1, A/D conversion is performed for the analog inputs of a maximum of 20 channels selected with the ADANSA0/1 register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is repeated beginning at the first channel. A/D conversion is repeated until the ADST bit in ADCSR is set to 0.
Self-diagnosis is executed once at the beginning of each scan (A/D conversion of all the selected channels), and one of the three voltages internally generated in the A/D converter is converted.
The ADCS bit should be set while the ADST bit is 0 (it should not be set simultaneously when 1 is written to the ADST bit.)

ADST Bit (A/D Conversion Start)

The ADST bit starts or stops A/D conversion process.
Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and conversion target analog input.
[Setting conditions]

- 1 is written by software.
- The synchronous trigger (MTU3, GPT) selected by the ADSTRGR.TRSA[5:0] bits is detected with ADCSR.EXTRG and ADCSR.TRGE bits being set to 0 and 1, respectively.
- The asynchronous trigger is detected with the ADCSR.TRGE and ADCSR.EXTRG bits being set to 1 and the ADSTRGR.TRSA[5:0] bits being set to “000000b”.

[Clearing conditions]

- 0 is written by software.
- The A/D conversion of all the channels selected is completed in single-cycle scan mode.

36.2.4 A/D Channel Select Register 0 (ADANSA0)

Address: 0008 9804h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ANSA0[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ANSA0[15:0]	A/D Conversion Channels Select	0: AN0 to AN15 are not subjected to conversion. 1: AN0 to AN15 are subjected to scan conversion.	R/W

ADANSA0 selects analog input channels for A/D conversion from among AN0 to AN15.

ANSA[15:0] Bits (A/D Conversion Channel Select)

The ANSA[15:0] bits select analog input channels for A/D conversion from among AN0 to AN15. The channels to be selected and the number of channels can be arbitrarily set. The ANSA0[0] bit corresponds to AN0 and the ANSA0[15] bit corresponds to AN15.

The ANSA[15:0] bits should be set while the ADCSR.ADST bit is 0.

36.2.5 A/D Channel Select Register 1 (ADANSA1)

Address: 0008 9806h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSA1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	ANSA1[3:0]	A/D Conversion Channels Select	0: AN16 to AN19 are not subjected to conversion. 1: AN16 to AN19 are subjected to scan conversion.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADANSA1 selects analog input channels for A/D conversion from among AN16 to AN19.

ANSA1[3:0] Bits (A/D Conversion Channel Select)

The ANSA1[315:0] bits select analog input channels for A/D conversion from among AN16 to AN19. The channels to be selected and the number of channels can be arbitrarily set. The ANSA1[0] bit corresponds to AN16 and the ANSA1[3] bit corresponds to AN19.

The ANSA1[3:0] bits should be set while the ADCSR.ADST bit is 0.

36.2.6 A/D-Converted Value Addition Mode Select Register0 (ADADS0)

Address: 0008 9808h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADS0[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ADS0[15:0]	A/D-Converted Value Addition Channel Select	0: A/D-converted value addition mode for AN0 to AN15 is not selected. 1: A/D-converted value addition mode for AN0 to AN15 is selected.	R/W

ADADS0 selects analog input channels for A/D conversion from among AN0 to AN15

ADS[15:0] Bits (A/D-Converted Value Addition Channels 0 to 15 Select)

When the ADS0[n] bit of the number that is the same as that of A/D converted channel selected by ADANSA0.ANSA0[n] bits (n = 0 to 15) is set to 1, these bits perform A/D conversion of analog input of the selected channels successively 2 to 4 times that is set with the ADC[1:0] bits in ADADC and returns the added (integrated) conversion results to the A/D data register. For the channel for which the A/D conversion is performed and addition mode is not selected, a normal one-time conversion is performed and the conversion result is returned to the A/D data register.

The ADS0[15:0] bits should be set while the ADCSR.ADST bit is 0.

36.2.7 A/D-Converted Value Addition Mode Select Register1 (ADADS1)

Address: 0008 980Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ADS1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	ADS1[3:0]	A/D-Converted Value Addition Channel Select	0: A/D-converted value addition mode for AN16 to AN19 is not selected. 1: A/D-converted value addition mode for AN16 to AN19 is selected.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADADS1 selects analog input channels for A/D conversion from among AN16 to AN19.

ADS1[3:0] Bits (A/D-Converted Value Addition Channels 16 to 19 Select)

When the ADS1[n] bit of the number that is the same as that of A/D converted channel selected by ADADS1.ANSA1[n] bits (n = 0 to 3) is set to 1, these bits perform A/D conversion of analog input of the selected channels successively 2 to 4 times that is set with the ADC[1:0] bits in ADADC and returns the added (integrated) conversion results to the A/D data register. For the channel for which the A/D conversion is performed and addition mode is not selected, a normal one-time conversion is performed and the conversion result is returned to the A/D data register.

The ADS1[3:0] bits should be set while the ADCSR.ADST bit is 0.

Figure 36.2 shows a scanning operation sequence in which both the ADS0[1] and ADS0[3] bits are set to 1.
In continuous scan mode (ADCSR.ADCS = 1), it is assumed that the addition count is set to 4 (ADADC.ADC[1:0] = 11b) and the channels AN0 to AN3 are selected (ADANSA.ANSA[3:0] = 00FFh). The conversion process begins with AN1. The AN1 conversion is performed successively 4 times, and the added (integrated) value is returned to the A/D data register 1. After that the AN2 conversion process is started. The AN3 conversion is performed successively 4 times and the added (integrated) value is returned to the A/D data register 3. After conversion of AN3, the conversion operation is once again performed in the same sequence from AN0.
For the channel for which the addition mode is not selected, the A/D data register format is determined by the ADRFMT bit in ADCER (right-alignment or left-alignment).

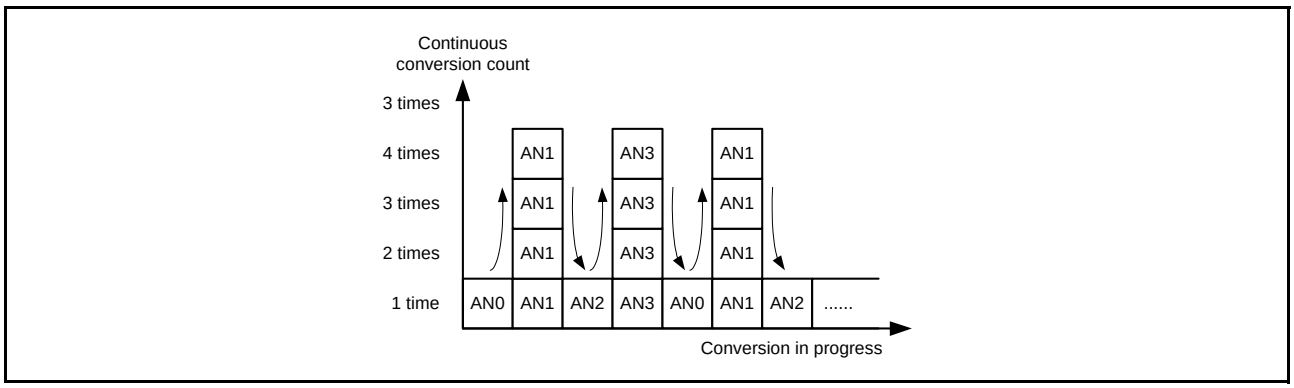


Figure 36.2 Scan Conversion Sequence with ADADC.ADC[1]= 1 and ADS[3] = 1

36.2.8 A/D-Converted Value Addition Count Select Register (ADADC)

Address: 0008 980Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ADC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	ADC[1:0]	Addition Count Select	b1 b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	R/W
b7 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

ADADC sets the addition count for the channels for which A/D-converted value addition mode is selected.

ADC[1:0] Bits (Addition Count Select)

The ADC[1:0] bits set the addition count common to the channels for which A/D conversion or A/D-converted value addition mode is selected.

The ADC[1:0] bits should be set while the ADCSR.ADST bit is 0.

36.2.9 A/D Control Extended Register (ADCER)

Address: 0008 980Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	ADPRC	A/D Data-Register Bit-Precision Specification	0: Values are stored with 10-bit precision in the A/D data registers. 1: Values are stored with 8-bit precision in the A/D data registers.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	ACE	Automatic Clearing Enable	0: Disables automatic clearing. 1: Enables automatic clearing.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Conversion Voltage Select for Self-Diagnosis	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: Uses VREFH0 × 0 for self-diagnosis. 1 0: Uses VREFH0 × 1/2 for self-diagnosis. 1 1: Uses VREFH0 × 1 for self-diagnosis.	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Rotation mode for self-diagnosis voltage 1: Fixed mode for self-diagnosis voltage	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Disables self-diagnosis of 10-bit A/D converter. 1: Enables self-diagnosis of10-bit A/D converter.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Right-alignment is selected for the A/D data register format. 1: Left-alignment is selected for the A/D data register format.	R/W

ADCER sets the parameters related to self-diagnosis, format of the A/D data registers y (ADDRy), and enables/disables automatic clearing of registers.

ADPRC Bits (A/D Data Register Bit-Precision Specification)

These bits select storage of the results of A/D conversion with eight- or 10-bit precision in the ADDRy registers.
When A/D converted value addition function is selected, format of each data register excluding A/D self-diagnosis data register (ADRD) is fixed to 12-bit regardless of the ADPRC bit setting.

Note: • Result of the self-diagnosis cannot be added.

ACE Bit (Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (All “0”) of ADDRy and ADRD after the register has been read by the CPU, DTC, or DMACA. This function enables update failures of ADDRy and ADRD to be detected.

DIAGVAL[1:0] Bits (Conversion Voltage Select for Self-Diagnosis)

For details, refer to the ADCER.DIAGLD bit description.
Self-diagnosis should not be executed by setting the ADCER.DIAGLD bit to 1 with these bits set to 00b.

DIAGLD Bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis.

Setting ADCER.DIAGLD bit to 0 allows conversion of the voltages in rotation mode where VREF × 0, VREF × 1/2, and VREF × 1 are converted in this order. After reset, VREF × 0 is first converted if self-diagnosis rotation mode is selected. If self-diagnosis voltage fixed mode is selected, the fixed voltage specified by the ADCER.DIAGVAL[1:0] bits is converted. In self-diagnosis rotation mode, the self-diagnosis voltage value does not return to VREF × 0 when scan conversion is completed; when scan conversion is restarted, rotation starts at the voltage value following the previous value. If self-diagnosis voltage fixed mode is switched to self-diagnosis voltage rotation mode, rotation starts at the fixed voltage value.
The DIAGLD bit should be set while the ADST bit is 0.

DIAGM Bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.
Self-diagnosis is used to detect a failure of the 10-bit A/D converter. Specifically, one of the three internally generated voltage values VREF × 0, VREF × 1/2, and VREF × 1 is converted. When conversion is completed, information of the converted voltage and the conversion result is stored into the self-diagnosis data register (ADRD). ADRD can then be read out by software to determine whether the conversion result falls within the normal range (normal) or not (abnormal). Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. The execution time of self-diagnosis equals to the A/D conversion time of one channel.
The DIAGM bit should be set while the ADST bit is 0.

ADRFMT Bit (A/D Data Register Format Select)

The ADRFMT bit specifies left-alignment or right-alignment for the data to be stored in ADDRy and ADRD.
When the A/D converted value addition mode is selected, the format of each data register is fixed to left-alignment, irrespective of the ADCER.ADRFMT bit value.

For details on the format of the data registers, see section 36.2.1, A/D Data Registers y (ADDRy) (y = A to T) and section 36.2.2, A/D Self-Diagnosis Data Register (ADRD).

36.2.10 A/D Start Trigger Select Register (ADSTRGR)

Address: 0008 9810h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	Select the A/D conversion start trigger.	R/W
b15 to b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSTRGR selects the A/D conversion start trigger.

TRSA[5:0] Bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion.

- When using the A/D conversion startup source of the synchronous trigger (MTU3 and GPT), set the TRGE bit in ADCSR to 0 and set the EXTRG bit in ADCSR to 0.
- When using the asynchronous trigger (ADTRG#), set the TRGE bit in ADCSR to 1 and set the EXTRG bit in ADCSR to 1.
- Software trigger (ADST bit in ADCSR) is always enabled regardless of the set values of the EXTRG in ADCSR and the TRGA[5:0] bits.

Table 36.4 shows the A/D conversion startup sources selected by TRSA[5:0] bits

Table 36.4 List of A/D Conversion Startup Sources Selected by TRSA[5:0] Bits (1 / 2)

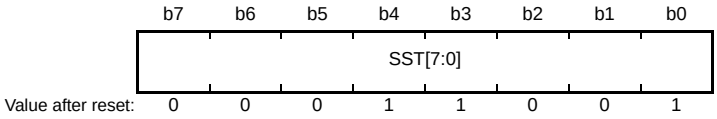
Module	Source	Remarks	TRSA [5]	TRSA [4]	TRSA [3]	TRSA [2]	TRSA [1]	TRSA [0]
ADC	ADST	Software trigger	—	—	—	—	—	—
External input	ADTRG#	A/D conversion start trigger pin	0	0	0	0	0	0
MTU3	TRGA0N	TRGA compare match/input capture from MTU0	0	0	0	0	0	1
	TRGA1N	TRGA compare match/input capture from MTU1	0	0	0	0	1	0
	TRGA2N	TRGA compare match/input capture from MTU2	0	0	0	0	1	1
	TRGA3N	TRGA compare match/input capture from MTU3	0	0	0	1	0	0
	TRGA4N	MTU4.TRGA compare match/input capture or MTU4.TCNT underflow (trough) in complementary PWM mode	0	0	0	1	0	1
	TRGA6N	TRGA compare match/input capture from MTU6	0	0	0	1	1	0
	TRGA7N	MTU7.TRGA compare match/input capture or MTU7.TCNT underflow (trough) in complementary PWM mode	0	0	0	1	1	1
	TRG0AN	TRGE compare match from MTU0	0	0	1	0	0	0
	TRG4AN	MTU4.TADCORA and MTU4.TCNT compare match	0	0	1	0	0	1
	TRG4BN	MTU4.TADCORB and MTU4.TCNT compare match	0	0	1	0	1	0
	TRG4AN or TRG4BN	MTU4.TADCORA and MTU4.TCNT compare match or MTU4.TADCORB and MTU4.TCNT compare match	0	0	1	0	1	1
	TRG4ABN	MTU4.TADCORA and MTU4.TCNT compare match and MTU4.TADCORB and MTU4.TCNT compare match (interrupt skipping function 2)	0	0	1	1	0	0
	TRG7AN	MTU7.TADCORA and MTU7.TCNT compare match	0	0	1	1	0	1
	TRG7BN	MTU7.TADCORB and MTU7.TCNT compare match	0	0	1	1	1	0
	TRG7AN or TRG7BN	MTU7.TADCORA and MTU7.TCNT compare match or MTU7.TADCORB and MTU7.TCNT compare match	0	0	1	1	1	1
	TRG7ABN	MTU7.TADCORA and MTU7.TCNT compare match and MTU7.TADCORB and MTU7.TCNT compare match (interrupt skipping function 2)	0	1	0	0	0	0

Table 36.4 List of A/D Conversion Startup Sources Selected by TRSA[5:0] Bits (2 / 2)

Module	Source	Remarks	TRSA [5]	TRSA [4]	TRSA [3]	TRSA [2]	TRSA [1]	TRSA [0]
GPT	GTADTRA0	GPT0.GTADTRA compare match	0	1	0	0	0	1
	GTADTRB0	GPT0.GTADTRB compare match	0	1	0	0	1	0
	GTADTRA1	GPT1.GTADTRA compare match	0	1	0	0	1	1
	GTADTRB1	GPT1.GTADTRB compare match	0	1	0	1	0	0
	GTADTRA2	GPT2.GTADTRA compare match	0	1	0	1	0	1
	GTADTRB2	GPT2.GTADTRB compare match	0	1	0	1	1	0
	GTADTRA3	GPT3.GTADTRA compare match	0	1	0	1	1	1
	GTADTRB3	GPT3.GTADTRB compare match	0	1	1	0	0	0
	GTADTRA0 or GTADTRB0	GPT0.GTADTRA compare match or GPT0.GTADTRB compare match	0	1	1	0	0	1
	GTADTRA1 or GTADTRB1	GPT1.GTADTRA compare match or GPT1.GTADTRB compare match	0	1	1	0	1	0
	GTADTRA2 or GTADTRB2	GPT2.GTADTRA compare match or GPT2.GTADTRB compare match	0	1	1	0	1	1
	GTADTRA3 or GTADTRB3	GPT3.GTADTRA compare match or GPT3.GTADTRB compare match	0	1	1	1	0	0
	GTADTRA4	GTADTRA4 GPT4.GTADTRA compare match	0	1	1	1	0	1
	GTADTRB4	GTADTRB4 GPT4.GTADTRB compare match	0	1	1	1	1	0
	GTADTRA5	GTADTRA5 GPT5.GTADTRA compare match	0	1	1	1	1	1
	GTADTRB5	GTADTRB5 GPT5.GTADTRB compare match	1	0	0	0	0	0
	GTADTRA6	GTADTRA6 GPT6.GTADTRA compare match	1	0	0	0	0	1
	GTADTRB6	GTADTRB6 GPT6.GTADTRB compare match	1	0	0	0	1	0
	GTADTRA7	GTADTRA7 GPT7.GTADTRA compare match	1	0	0	0	1	1
	GTADTRB7	GTADTRB7 GPT7.GTADTRB compare match	1	0	0	1	0	0
	GTADTRA4 or GTADTRB4	GPT4.GTADTRA compare match or GPT4.GTADTRB compare match	1	0	0	1	0	1
	GTADTRA5 or GTADTRB5	GPT5.GTADTRA compare match or GPT5.GTADTRB compare match	1	0	0	1	1	0
	GTADTRA6 or GTADTRB6	GPT6.GTADTRA compare match or GPT6.GTADTRB compare match	1	0	0	1	1	1
	GTADTRA7 or GTADTRB7	GPT7.GTADTRA compare match or GPT7.GTADTRB compare match	1	0	1	0	0	0

36.2.11 A/D Sampling State Register n (ADSSTRn) (n = 0 to 7)

Address: ADSSTR0: 0008 9860h, ADSSTR1: 0008 9873h, ADSSTR2: 0008 9874h, ADSSTR3: 0008 9875h, ADSSTR4: 0008 9876h, ADSSTR5: 0008 9877h, ADSSTR6: 0008 9878h, ADSSTR7: 0008 9879h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	Sets the sampling time (7 to 255 states).	R/W

ADSSTRn sets the sampling time for analog input (AN0 to AN7) and self-diagnosis.
One state is one ADCLK (A/D conversion clock) cycle. When the ADCLK is 100 MHz, one state is 10 ns. The initial value is 25 states. If the impedance of the analog input signal source is too high to secure sufficient sampling time or if the ADCLK is slow, the sampling time can be adjusted. ADSSTRn should be set while the ADST bit in ADCSR is 0. The set value for sampling time should be 7 or more states and 255 or less states. The sampling time should be 0.25 µs or longer. Table 36.5 shows the A/D sampling state registers and corresponding channels.

Table 36.5 A/D Sampling State Registers and Corresponding Channels

Bit Name	Corresponding Channels
ADSSTR0.SST[7:0]	AN0/self-diagnosis
ADSSTR1.SST[7:0]	AN1
ADSSTR2.SST[7:0]	AN2
ADSSTR3.SST[7:0]	AN3
ADSSTR4.SST[7:0]	AN4
ADSSTR5.SST[7:0]	AN5
ADSSTR6.SST[7:0]	AN6
ADSSTR7.SST[7:0]	AN7

36.2.12 A/D Sampling State Register L (ADSSTRL)

Address: ADSSTRL: 00089861h

	b7	b6	b5	b4	b3	b2	b1	b0
	SST[7:0]							
Value after reset:	0	0	0	1	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	Sets the sampling time (7 to 255 states).	R/W

ADSSTRL sets the sampling time for analog input (AN8 to AN19) and self-diagnosis.
One state is one ADCLK (A/D conversion clock) cycle. When the ADCLK is 100 MHz, one state is 10 ns. The initial value is 50 states. If the impedance of the analog input signal source is too high to secure sufficient sampling time or if the ADCLK is slow, the sampling time can be adjusted. ADSSTRL should be set while the ADST bit in ADCSR is 0. The set value for sampling time should be 7 or more states and 255 or less states. The sampling time should be 0.5 µs or longer.

36.2.13 Digital Power Supply Control Circuit Output Setting Register (ADDPCONR)

Address: 0008 987Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DPCOE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DPCOE	Digital Power Supply Control Circuit Output Enable	0: A/D converted data is not output 1: A/D converted data is output	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADDPCONR sets output of A/D converted data to the digital power supply controller.

36.3 Operation

36.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.
A scan conversion is performed in two operating modes: single scan mode and continuous scan mode. In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until the ADST bit in ADCSR is cleared to 0 from 1 by software.
In single scan mode and continuous scan mode, A/D conversion is performed for ANn channels selected by the ADANSA0/1 register, starting from the channel with the smallest number n.
When self-diagnosis is selected, it is executed once at the beginning of each scan, and one of the three voltages internally generated in the 10-bit A/D converter is converted.

36.3.2 Single scan mode

36.3.2.1 Basic Operation

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as below.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3 or GPT), or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA0/1 register, starting from the channel with the smallest number n.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) When A/D conversion of all the selected channels is completed, an ADI0 interrupt request is generated if the ADIE bit in ADCSR is 1 (ADI0 interrupt upon scanning completion enabled).
(4) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 10-bit A/D converter enters a wait state.

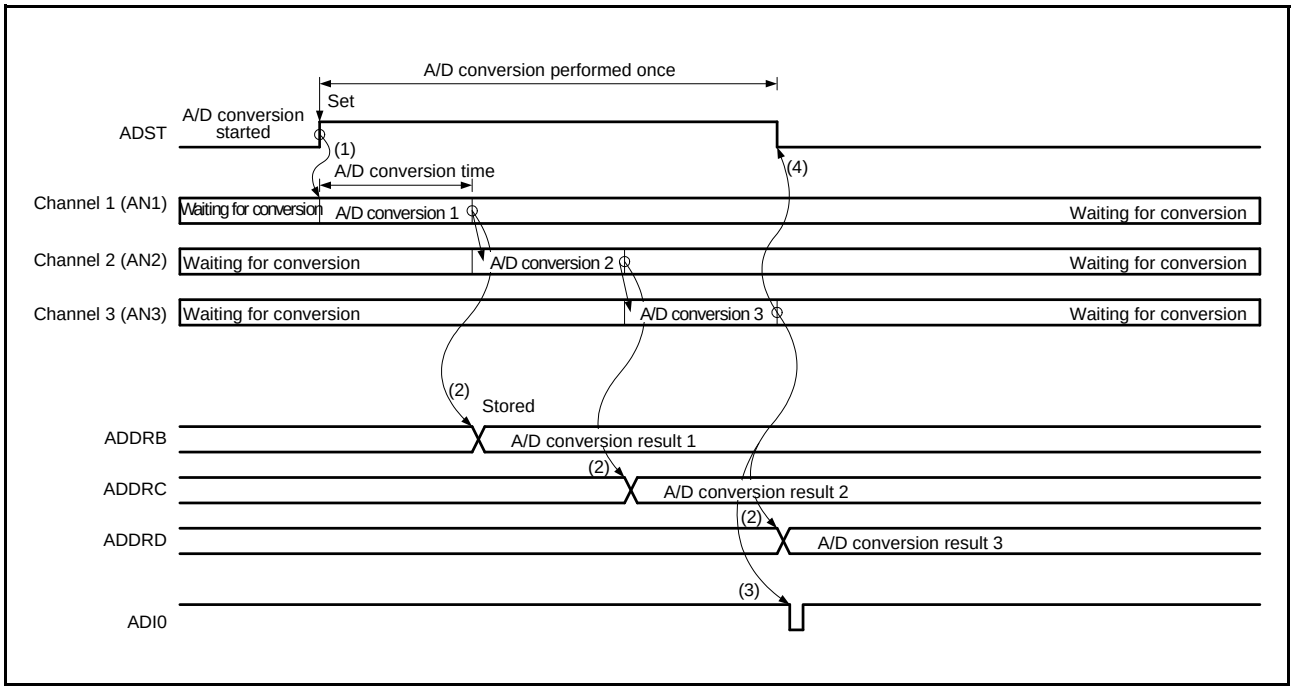


Figure 36.3 Example of Operation in Single Scan Mode (Basic Operation)

36.3.2.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREF (×0, ×1/2, or ×1) supplied to the A/D converter, and then A/D conversion is performed once on the analog input of the selected channels as below.

(1) A/D conversion for self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3 or GPT), or asynchronous trigger input.

(2) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA0/1 register, starting from the channel with the smallest number n.

(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(4) When A/D conversion of all the selected channels is completed, an ADI0 interrupt request is generated if the ADIE bit in ADCSR is 1 (ADI0 interrupt upon scanning completion enabled).

(5) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 10-bit A/D converter enters a wait state.

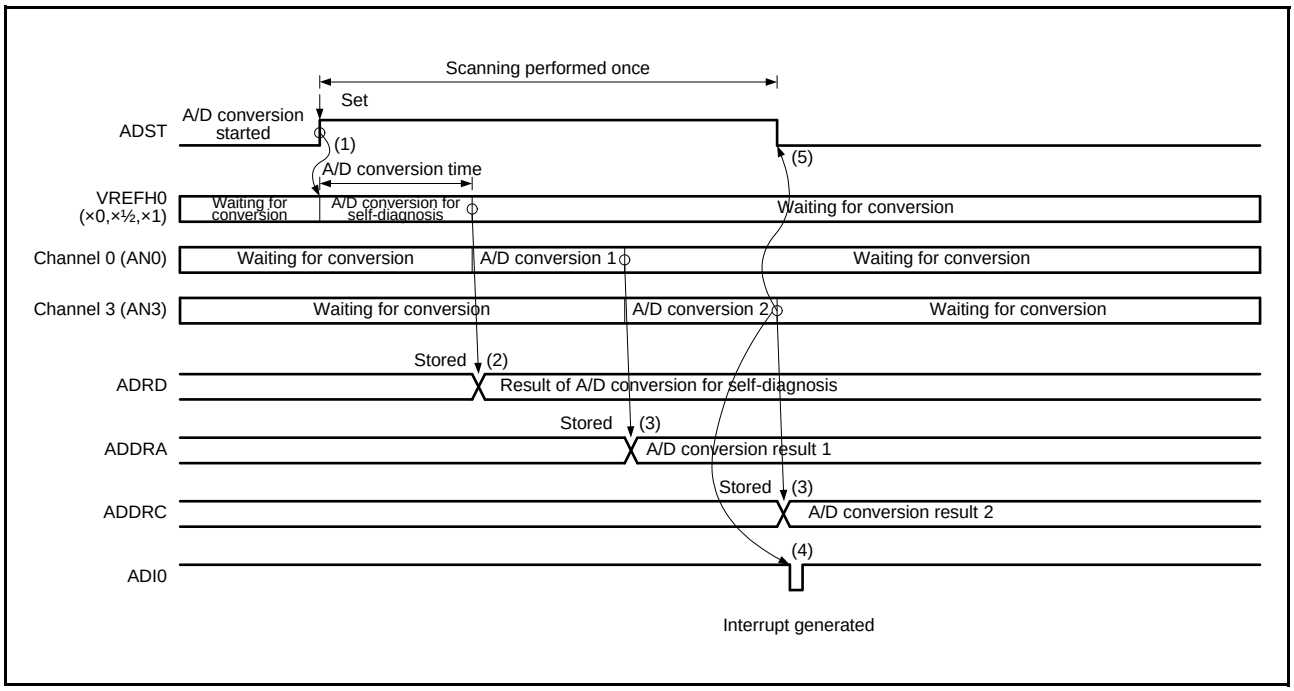


Figure 36.4 Example of Operation in Single Scan Mode (Basic Operation + Self-Diagnosis)

36.3.3 Continuous Scan Mode

36.3.3.1 Basic Operation

In basic operation of continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels as below.

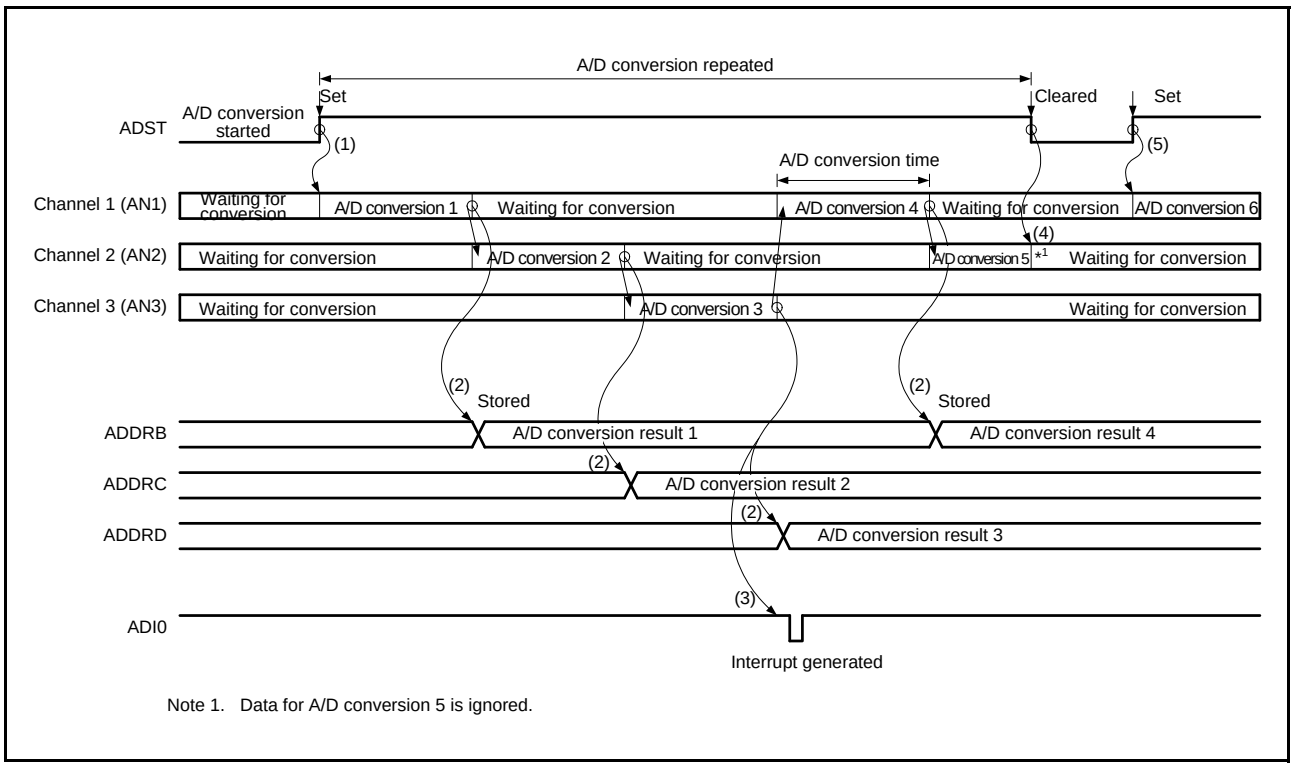
(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3 or GPT), or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA0/1 register, starting from the channel with the smallest number n.

(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(3) When A/D conversion of all the selected channels is completed, an ADI0 interrupt request is generated if the ADIE bit in ADCSR is 1 (ADI0 interrupt upon scanning completion enabled).
The 10-bit A/D converter sequentially starts A/D conversion for ANn channels selected by the ADANSA0/1 register, starting from the channel with the smallest number n.

(4) The ADST bit in ADCSR is not automatically cleared to 0 and steps 2 and 3 are repeated as long as the bit remains 1 (A/D conversion start). When the ADST bit in ADCSR is set to 0 (A/D conversion stop), A/D conversion stops and the 10-bit A/D converter enters a wait state.

(5) When the ADST bit is later set to 1 (A/D conversion start), A/D conversion is started again for ANn channels selected by the ADANSA0/1 register, starting from the channel with the smallest number n.



Note 1. Data for A/D conversion 5 is ignored.

Figure 36.5 Example of Operation in Continuous Scan Mode (Basic Operation: AN000 to AN002 Selected)

36.3.3.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREF (×0, ×1/2, or ×1) supplied to the 10-bit A/D converter, and then A/D conversion is performed on the analog input of the selected channels, which sequence is repeated as below.

(1) A/D conversion for self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by software, synchronous trigger (MTU3 or GPT), or asynchronous trigger input.

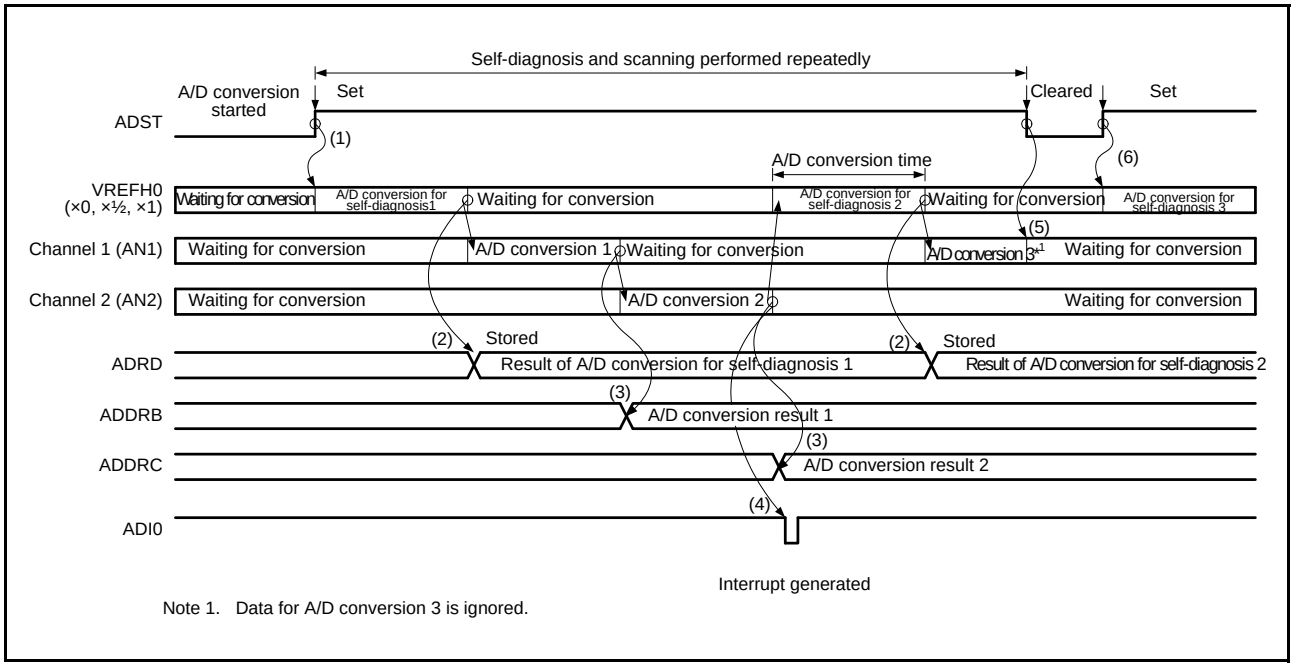
(2) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA0/1 register, starting from the channel with the smallest number n.

(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(4) When A/D conversion of all the selected channels is completed, an ADI0 interrupt request is generated if the ADIE bit in ADCSR is 1 (ADI0 interrupt upon scanning completion enabled). At the same time, the 10-bit A/D converter starts A/D conversion for self-diagnosis and then starts A/D conversion on ANn channels selected by the ADANSA register, starting from the channel with the smallest number n.

(5) The ADST bit is not automatically cleared to 0 and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 10-bit A/D converter enters a wait state.

(6) When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.



Note 1. Data for A/D conversion 3 is ignored.

Figure 36.6 Example of Operation in Continuous Scan Mode (Basic Operation + Self-Diagnosis)

36.3.4 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by software trigger; the synchronous triggers from the MTU3 or GPT, or asynchronous trigger (ADTRG#). After start-of-scanning-delay time (t_D) has passed, the conversion process for self-diagnosis is executed, and then the A/D conversion process is started.
Figure 36.5 shows the scan conversion timing in single-cycle scan mode, in which scan conversion is activated by software or synchronous trigger. Figure 36.6 shows the scan conversion timing in single-cycle scan mode, in which scan conversion is activated by asynchronous trigger. The scan conversion time (t_{SCAN}) includes start-of-scanning-delay time (t_D), self-diagnosis conversion processing time (t_{DIAG})*1, A/D conversion processing time (t_{CONV}), and end-of-scanning-delay time (t_{ED}). Table 34.7 shows the specific scanning time.
The scan conversion time (t_{SCAN}) in single-cycle scan mode for which the number of selected channels is n can be determined as follows:

$t_{SCAN} = t_D$?+ t_{DIAG} ?+ ($t_{CONV} \times n$) + t_{ED}

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single-cycle scan minus t_{ED}.
The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed to (tCONV × n) + tDIAG + (tCONV × n).

Self-diagnosis conversion processing time (tDIAG) and A/D conversion processing time (tCONV) are as follows.
The self-diagnosis conversion processing time (t_{DIAG}) is 25 states (fixed) + the value set in the ADSSTR0.SST[7:0] bits.
The A/D conversion processing time (t_{CONV}) is 25 states (fixed) + the value set in the ADSSTn.SST[7:0] bits*3.

Note 1. When the self-diagnosis function is not used, $t_{DIAG} = 0$.
Note 2. Registers in Table 36.5.

Table 36.6 Scan Conversion Time (in Terms of PCLK and ADCLK Cycles)

Item	Symbol	Types/Conditions	Cycles
Start-of-scanning-delay time*1	t_D	MTU3, GPT or software trigger	2 PCLK + 4 ADCLK
		External trigger	4 PCLK + 4 ADCLK
Self-diagnosis conversion processing time*1	t_{DIAG}	Set by ADSSTR0.SST[7:0] bits (initial value 19h)	50 ADCLK
A/D conversion processing time*1	t_{CONV}	Set by ADSSTRn.SST[7:0] bits (initial value 19h)	50 ADCLK
End-of-scanning-delay time*1	t_{ED}	—	1 PCLK + 3 ADCLK
Scan conversion time*2	t_{SCAN}	—	5 PCLK + (50n + 57) ADCLK

Note 1. For t_D, t_{CONV}, and t_{ED}, refer to Figure 36.7 and Figure 36.8.
Note 2. This applies when asynchronous trigger is activated and self-diagnosis conversion and single-cycle scan mode are selected. n indicates the number of channels.

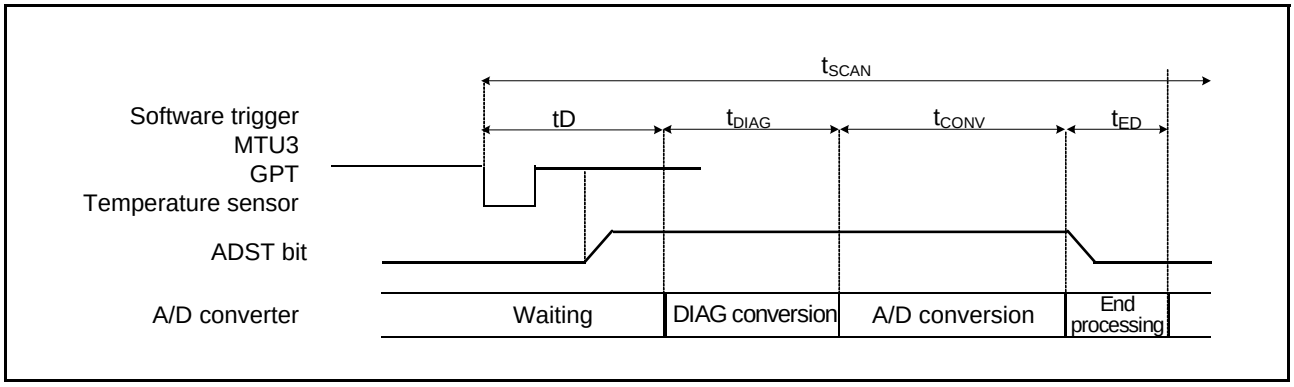


Figure 36.7 Scan Conversion Timing (Activated by Software, or Triggers from the MTU3, GPT)

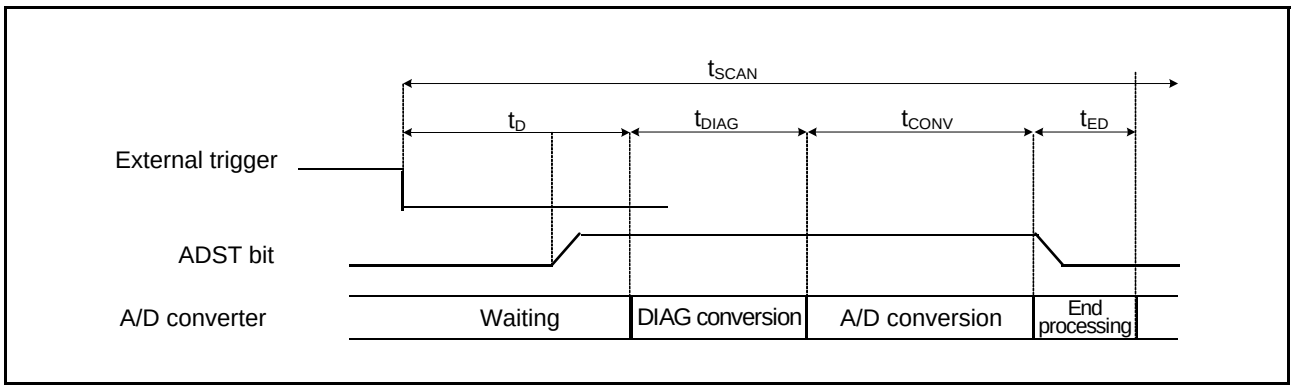


Figure 36.8 Scan Conversion Timing (Activated by ADTRG#)

36.3.5 Usage Example of Automatic Register Clearing Function

Setting the ACE bit in ADCER to 1 automatically clears the A/D data registers (ADDRy and ADRD) to 0000h when the A/D data registers are read by the CPU, DTC, or DMACA. The following describes the examples in which the function to automatically clear the ADDRy register is enabled and disabled.

In a case where the ACE bit in ADCER is 0 (automatic clearing is disabled), if the A/D conversion result (0222h) is not written to the ADDRy register for some reason, the old data (0111h) will be the ADDRy value. This function enables detection of update failures of the ADDRy and ADRD registers. When checking whether there is an update failure, it is necessary to frequently save the old data in the RAM or a general register.

Furthermore, if this ADDRy value is written to a general register using an A/D conversion end interrupt, the old data (0111h) can be saved in the general register. After that, if the A/D conversion result 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. In a case where the ACE bit in ADCER is 1 (automatic clearing is enabled), when ADDRy = 0111h is read by the CPU, DTC, or DMACA, ADDRy is automatically cleared to 0000h. Occurrence of an ADDRy update failure can be determined by simply checking that the read data value is 0000h.

36.3.6 A/D-Converted Value Addition Function

The same channel is A/D converted two to four consecutive times and the sum of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.

A/D converted value addition function can be used for channel-selected analog input A/D conversion.

36.3.7 Starting A/D Conversion with Asynchronous Trigger

The A/D conversion can be started by the input of an asynchronous trigger. To start up the A/D converter by an asynchronous trigger, the A/D conversion start trigger select bits (ADSTRGR.TRGA[5:0]) should be set to 000000b and a high-level signal should be input to the asynchronous trigger (ADTRG# pin), and both the ADCSR.TRGE and ADCSR.EXTRG bits should be set to 1. Figure 36.9 shows a timing of the asynchronous trigger input.
For the time required for the A/D conversion start after the ADCSR.ADST bit is set, refer to section 36.6.3, A/D Conversion Restarting Timing and Termination Timing.

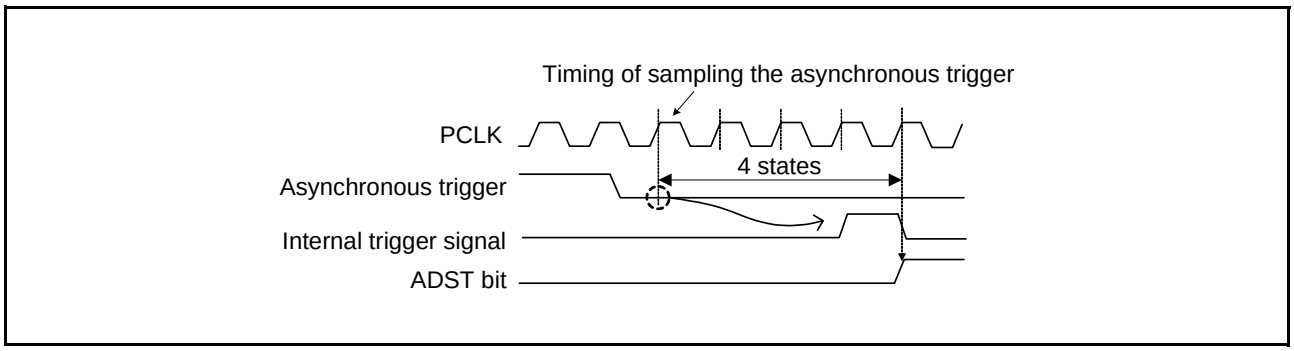


Figure 36.9 Asynchronous Trigger Input Timing

36.3.8 Starting A/D Conversion with Synchronous Trigger from Peripheral Modules

The A/D conversion can be started by a synchronous trigger of the MTU3, GPT. To start the A/D conversion by a synchronous trigger, the ADCSR.TRGE bit should be set to 1, the ADCSR.EXTRG bit should be cleared to 0, and the relevant source should be selected by ADSTRGR.TRSA[5:0] bits.

36.4 Interrupt Sources and DMA Transfer Requests

36.4.1 Interrupt Request on Completion of Each Scanning Conversion

The 10-bit A/D converter can send scan end interrupt requests ADI0 to the CPU.
Setting the ADIE bit in ADCSR to 1 and 0 enables and disables an ADI0 interrupt, respectively.
In addition, the DTC or DMAC can be started up when an ADI0 interrupt is generated. Using an ADI0 interrupt to allow the DTC or DMAC to read the converted data enables continuous conversion without burden on software.
For details on DTC settings, see section 19, Data Transfer Controller (DTCa), and for details on DMAC settings, see section 18, DMA Controller (DMACA).

36.5 A/D Conversion Accuracy Definitions

The RX63T Group's A/D conversion accuracy is defined as below:

- Resolution
  The number of 10-bit A/D converter digital output codes
- Offset error
  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 0000000000 to 0000000001, excluding quantization error.
- Full-scale error
  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 1111111110 to 1111111111, excluding quantization error.
- Quantization error
  The deviation inherent in the 10-bit A/D converter, given by 1/2 LSB
- Nonlinearity error
  The error with respect to the ideal A/D conversion characteristic between zero voltage and the full-scale error, excluding offset error, full-scale error, and quantization error.
- Absolute accuracy
  The deviation between the digital value and analog input value, including offset error, full-scale error, quantization error, and nonlinearity error.

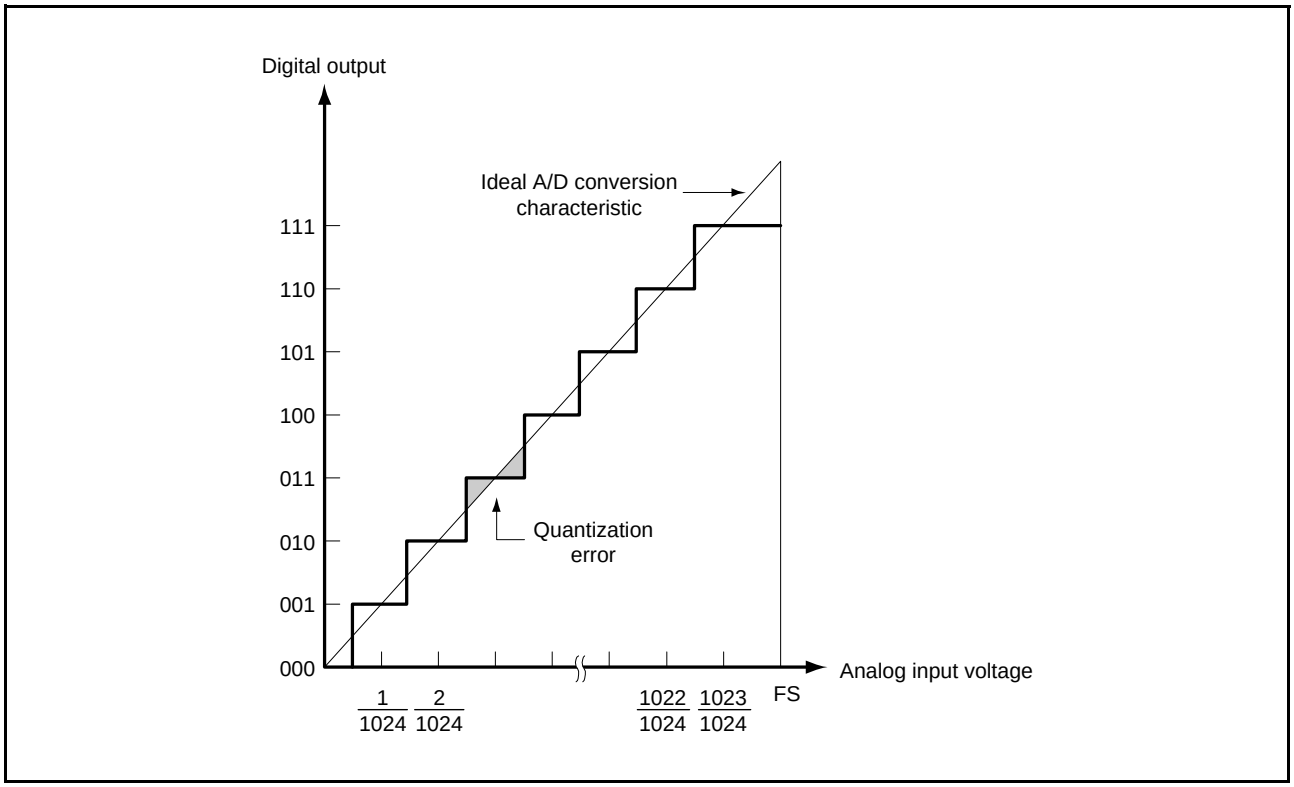


Figure 36.10 A/D Conversion Accuracy Definitions (1)

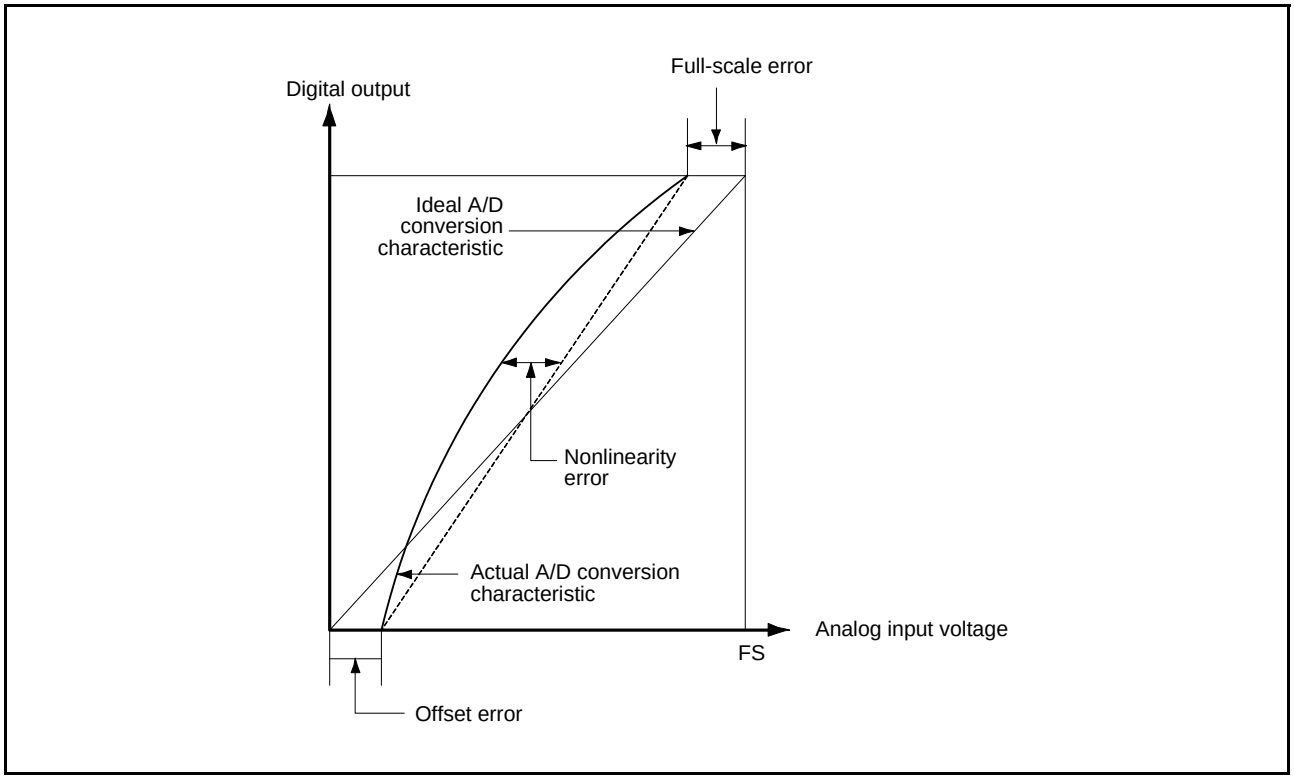


Figure 36.11 A/D Conversion Accuracy Definitions (2)

36.6 Usage Notes

36.6.1 Notes on Reading Data registers

The A/D data registers and A/D self-diagnosis data register should be read in word units. If a register is read twice in byte units, that is, the upper byte and lower byte are separately read, the A/D converted value having been read first may disagree with the A/D converted value having been read for the second time. To prevent this, the data registers should never be read in byte units.

36.6.2 Notes on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger has been selected as the condition for starting A/D conversion, set the TRGE bit in ADCSR to 0 and select the software trigger as the condition for starting A/D conversion, and then set the ADST bit in ADCSR to 0 (to stop A/D conversion).

36.6.3 A/D Conversion Restarting Timing and Termination Timing

It takes a maximum of four ADCLK cycles for the idle analog unit of the 10-bit A/D converter to be restarted by setting the ADST bit in ADCSR to 1. It takes a maximum of two ADCLK cycles for the operating analog unit of the 10-bit A/D converter to be terminated by setting the ADST bit in ADCSR to 0.

36.6.4 Notes on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D converted data is overwritten with the second A/D converted data in the case that the CPU does not complete reading out the A/D converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

36.6.5 Module Stop Function Setting

Operation of the 10-bit A/D converter can be disabled or enabled using the module stop control register. The 10-bit A/D converter is stopped a the initial value. Canceling the module stop state allows registers to be accessed.
For details, see section 12, Low Power Consumption.

36.6.6 Notes on Entering Low Power Consumption States

Before entering module stop mode or software standby mode, make sure to stop A/D conversion. Here, set the ADST bit in ADCSR to 0, and allow time for stopping the analog unit of the 10-bit A/D converter.
Follow the procedure given below to secure this time.
1. Set the ADCSR.TRGE bit to 0 (software trigger).
2. Clear the ADCSR.ADST bit to 0.
3. After confirming that the A/D converter has been stopped, place the MCU in the module stop state mode or software standby mode.

36.6.7 Allowable Impedance of Signal Source

To achieve high-speed conversion of 0.5 µs, the analog input pins of this MCU are designed so that the conversion accuracy is guaranteed if the impedance of the input signal source is 1 kΩ or less. If an external capacitor of large capacitance is attached in the application in which only a single pin input is converted in single scan mode, the only load on input is virtually 2.5 kΩ of the internal input resistor; therefore, the impedance of the signal source can be ignored. Being a low-pass filter, however, an analog input circuit may not follow the analog signal with a large differential coefficient (e. g., larger than 5 mV/µs) as shown in Figure 36.12. When high-speed analog signals are to be converted or multiple pins are to be converted in scan mode, a low-impedance buffer should be used.

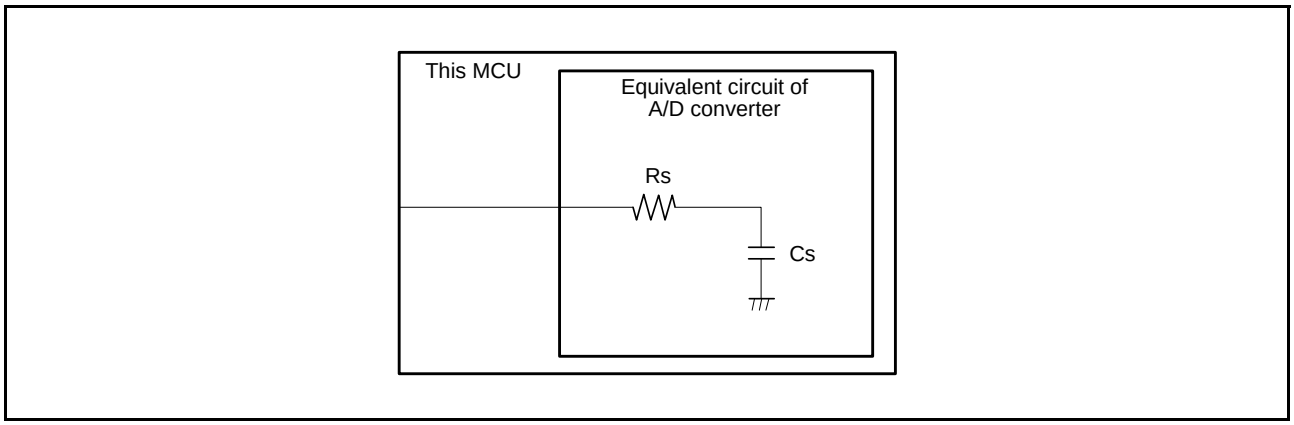


Figure 36.12 Internal Equivalent Circuit of Analog Input Pin

Table 36.7 Specifications of Analog Input Pins

Item		Min.	Max.	Unit
Allowable signal source impedance		—	1	kΩ
Internal equivalent circuit of a pin	Rs	—	8	kΩ
	Cs	—	7	pF

36.6.8 Influence on Absolute Accuracy

Attaching a capacitor creates coupling with GND and may affect the absolute accuracy when noisy GND is used; therefore, a capacitor should be connected to electrically stable GND such as AVSS0.
The filter circuit should be designed so that it does not interfere digital signals or it does not serve as an antenna on the circuit board.

36.6.9 Voltage Range of Analog Power Supply Pins

If this MCU is used with the voltages outside the following ranges, the reliability of the MCU may be affected.

- Analog input voltage range
  Voltage (VAN) applied to analog input pins ANn: AVSS ≤ VAN ≤ VREF
- Relationship between power supply pin pairs (AVCC–AVSS, VCC–VSS)
  AVSS = VSS
  A 0.1-µF capacitor should be connected between each pair of power supply pins to create a closed loop with the shortest route possible as shown in Figure 36.14, and connection should be made so that the following conditions are satisfied at the supply side.
  AVSS = VSS
- VREF range
  The reference voltage range applied to the VREF pin should be VREF ≤ AVCC.

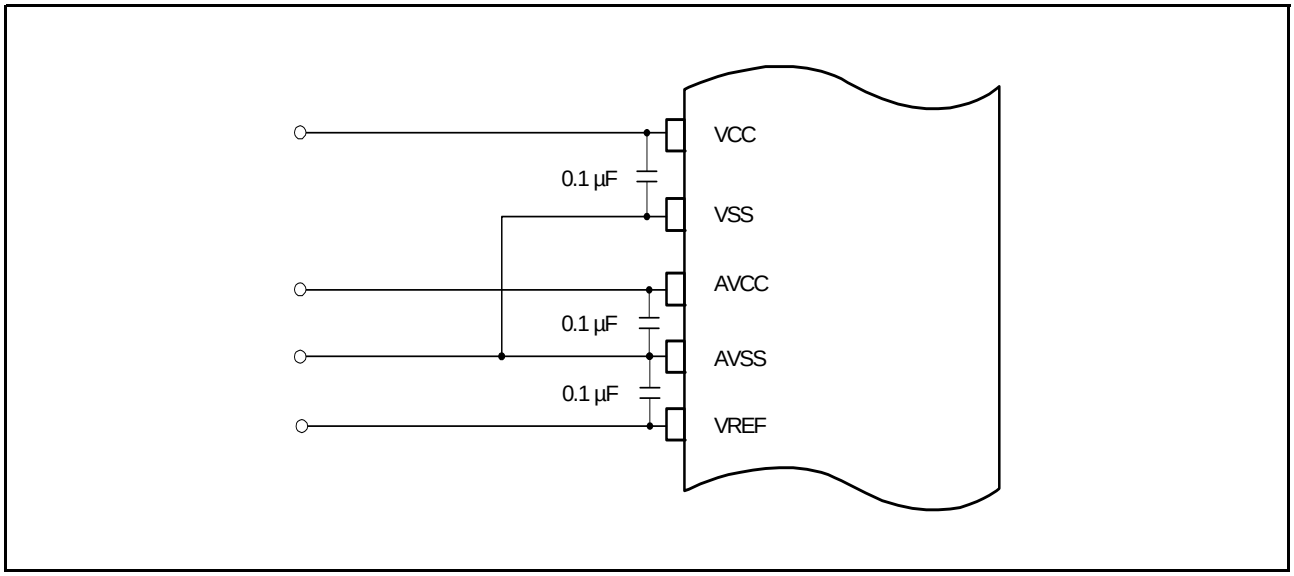


Figure 36.13 Power Supply Pin Connection Example

36.6.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or placed near each other. If these rules are not followed, noise will be produced on analog signals and A/D conversion accuracy will be affected. The analog input pins (AN0 to AN19), analog reference voltage (VREF), and analog power supply (AVCC) should be separated from digital circuits using the analog ground (AVSS). The analog ground (AVSS) should be connected to a stable digital ground (VSS) on the board.

36.6.11 Notes on Noise Prevention

To prevent the analog input pins (AN0 to AN19) from being destroyed by abnormal voltage such as excessive surge, a capacitor should be inserted between AVCC and AVSS and between VREF and AVSS, and a protection circuit should be connected to protect the analog input pins (AN0 to AN19) as shown Figure 36.14.
Moreover, connect the filter capacitor to be connected to analog input pins (AN0 to AN19) to AVSS. The 0.1 µF capacitor shown in Figure 36.14 must be placed as close as possible to the pin.
Note that an error may occur when the filter capacitor is connected as shown in Figure 36.14, because the input voltages of the analog input pins (AN0 to AN19) are averaged. Accordingly, determine circuit constant upon careful consideration.

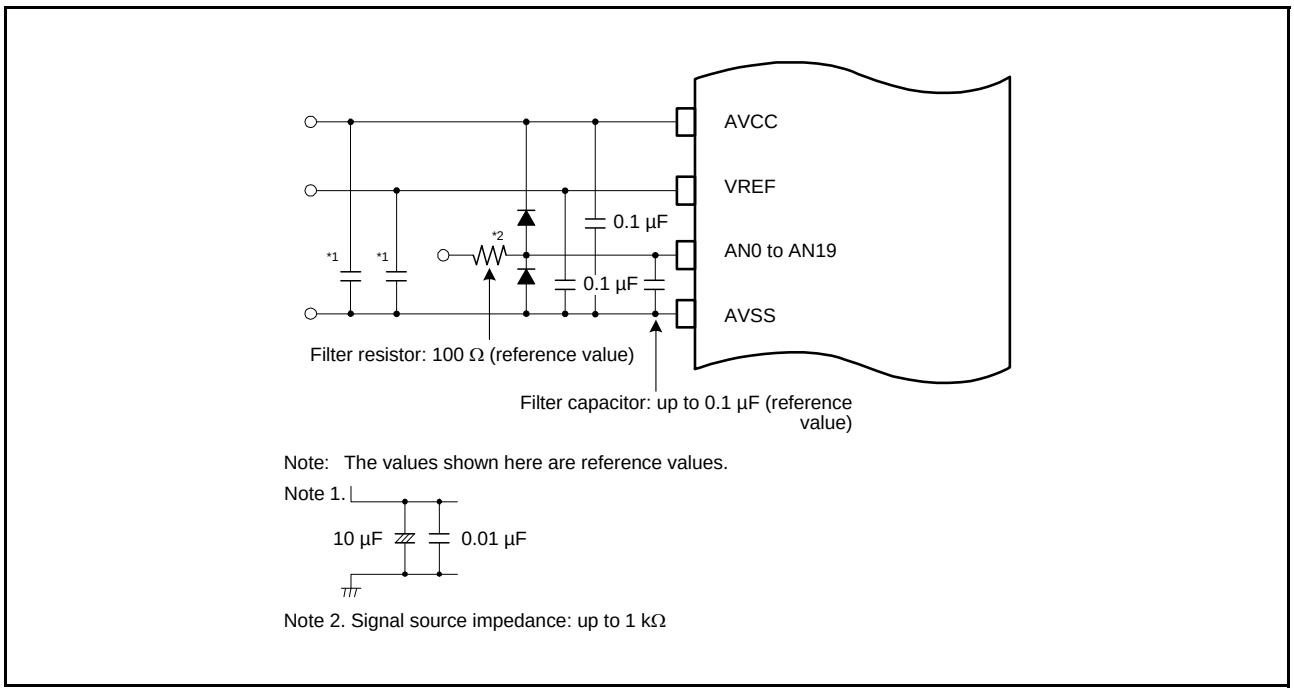


Figure 36.14 Sample Protection Circuit for Analog Inputs

36.6.12 Notes on Using External Bus

When using external bus, 10-bit A/D converter should not be used because analog input pins (AN0 to AN5, AN8 and AN9) share the same pins with the address output pins while external bus is in use.

37. D/A Converter (DAa)

37.1 Overview

This MCU includes two-channels of 10-bit D/A converter.
Table 37.1 lists the specifications of the D/A converter and Figure 37.1 shows a block diagram of the D/A converter.

Table 37.1 Specifications of D/A Converter

Item	Specifications
Resolution	10 bits
Output channels	Two channels
Low-power consumption function	Module-stop state can be set for each unit.
Countermeasure against mutual interference between analog modules	• Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 10-bit A/D converter synchronous D/A conversion enable input signal from the 10-bit A/D converter (degradation of A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal).

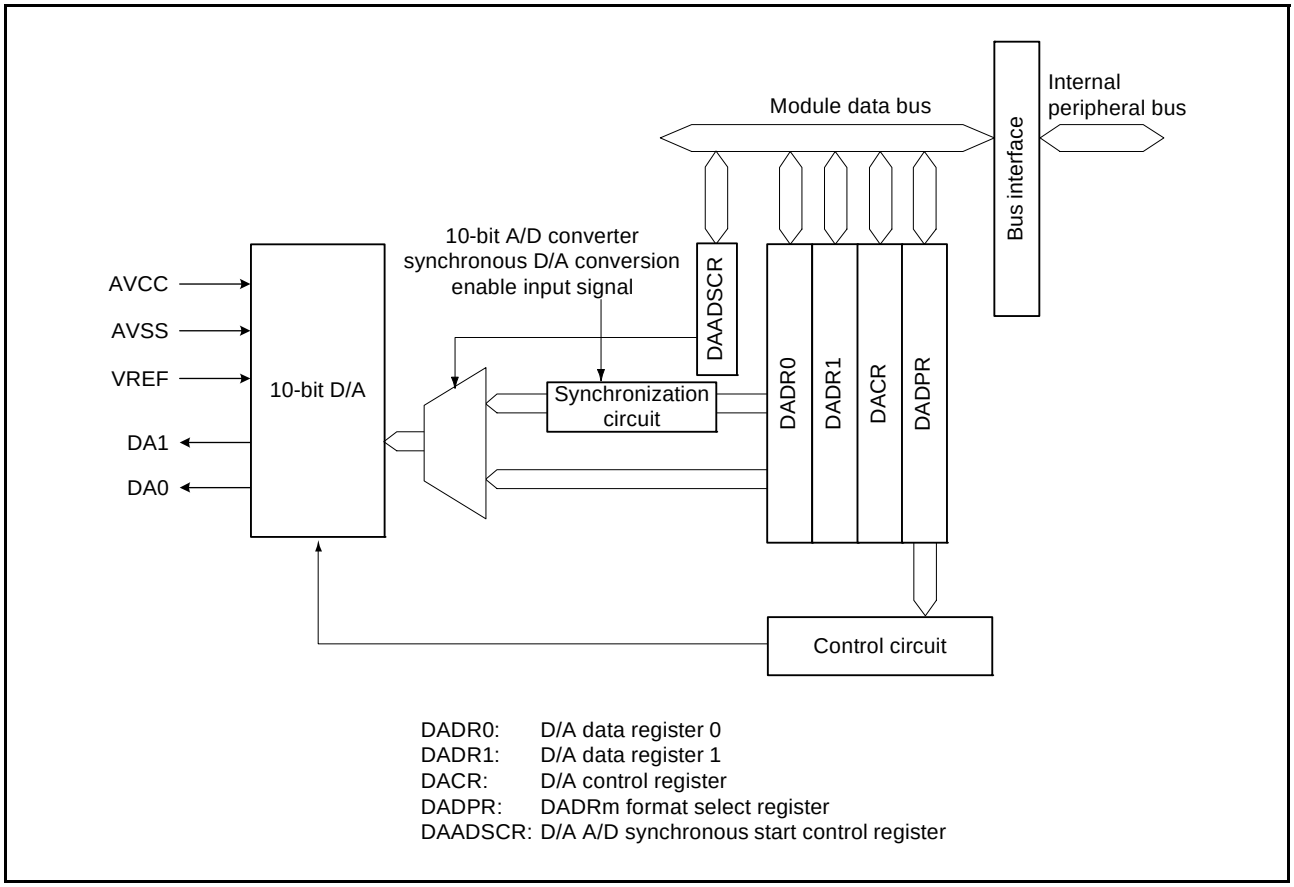


Figure 37.1 Block Diagram of D/A Converter

Table 37.2 lists the pin configuration of the D/A converter.

Table 37.2 Pin Configuration of D/A Converter

Pin Name	I/O	Function
AVCC	Input	Analog power supply pin for the D/A converter
AVSS	Input	Analog ground pin for the D/A converter
VREF	Input	Reference voltage input pin for the 10-bit A/D converter and D/A converter. This pin is also used as an analog power supply pin for each module. Connect to VCC when neither of these modules are used.
DA0	Output	Channel 0 analog output pin
DA1	Output	Channel 1 analog output pin

37.2 Register Descriptions

37.2.1 D/A Data Register m (DADRm) (m = 0, 1)

Address(es): DADR0 0008 80C0h, DADR1 0008 80C2h

• DADPR.DPSEL bit = 0 (data are flush with the right end of the register)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

• DADPR.DPSEL bit = 1 (data are flush with the left end of the register)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
											—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADR registers are 16-bit readable/writable registers, which store data to which D/A conversion is to be performed. Whenever an analog output is enabled, the values in DADR are converted and output to the analog output pins.
10-bit data can be relocated by setting the DPSEL bit in DADPR.
Bits "—" are read as 0. The write value should be 0.

37.2.2 D/A Control Register (DACR)

Address(es): 0008 80C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	DAE*1	D/A Enable	0: D/A conversion is independently controlled on channels 0 and 1. 1: D/A conversion on channels 0 and 1 is enabled as a single whole.	R/W
b6	DAOE0	D/A Output Enable 0	0: Analog output of channel 0 (DA0) is disabled. 1: D/A conversion of channel 0 is enabled. Analog output of channel 0 (DA0) is enabled.*2	R/W
b7	DAOE1	D/A Output Enable 1	0: Analog output of channel 1 (DA1) is disabled. 1: D/A conversion of channel 1 is enabled. Analog output of channel 1 (DA1) is enabled.*2	R/W

Note 1. This bit controls D/A conversion in combination with the DAOEi bit (i = 0, 1). The DAOEi bit controls output of the results of conversion. For details, see Table 37.3.
Note 2. Set the pins for use as analog output to the analog pins with the P54PFS and P55PFS registers. For details, see section 21, Multi-Function Pin Controller (MPC).

Table 37.3 Controlling of D/A Conversion

b5	b7	b6	
DAE	DAOE1	DAOE0	Description
0	0	0	D/A conversion and analog output pins (DA0, DA1) are disabled.*1
		1	D/A conversion of channel 0 is enabled. D/A conversion of channel 1 is disabled. Analog output of channel 0 (DA0) is enabled. Analog output of channel 1 (DA1) is disabled.*1
	1	0	D/A conversion of channel 0 is disabled. D/A conversion of channel 1 is enabled. Analog output of channel 0 (DA0) is disabled.*1 Analog output of channel 1 (DA1) is enabled.
		1	D/A conversion of channels 0 and 1 is enabled. Analog output of channels 0 and 1 (DA0, DA1) is enabled.
1	0	0	D/A conversion of channels 0 and 1 is enabled. Analog output of channels 0 and 1 (DA0, DA1) is disabled.*1
		1	D/A conversion of channels 0 and 1 is enabled.sss Analog output of channel 0 (DA0) is enabled. Analog output of channel 1 (DA1) is disabled.*1
	1	0	D/A conversion of channels 0 and 1 is enabled. Analog output of channel 0 (DA0) is disabled.*1 Analog output of channel 1 (DA1) is enabled.
		1	D/A conversion of channels 0 and 1 is enabled. Analog output of channels 0 and 1 (DA0, DA1) is enabled.

Note 1. When analog output is disabled, the analog output signal is placed in the Hi-Z state.

This register should be set while the 10-bit A/D converter is halted when the DAADSCR.DAADST bit is 1 (enabling the measure against interference between D/A and A/D conversion) (The register should be set while the ADCSR.ADST bit is 0 after the software trigger is selected as the trigger source for the 10-bit A/D converter).

DAE Bit (D/A Enable)

The DAE bit controls D/A conversion in combination with the DAOEi (i = 0 or 1) bit.

When the DAE bit is 0, D/A conversion is independently controlled on channels 0 and 1. When the DAE bit is 1, D/A conversion on channels 0 and 1 is controlled as a single whole. The DAOEi bit controls output of the results of conversion.

When the measure against interference for D/A and A/D conversion is enabled (the DAADSCR.DAADST bit = 1), set this bit while the ADCSR.ADST bit is set to 0. To ensure that the 10-bit A/D converter remains stopped while the setting is made, select the software trigger as the trigger source in advance.

DAOE0 Bit (D/A Output Enable 0)

The DAOE0 bit controls the D/A conversion and analog output.

When the measure against interference between D/A and A/D conversion is enabled (the DAADSCR.DAADST bit = 1), set this bit while the ADCSR.ADST bit is set to 0. To ensure that the 10-bit A/D converter remains stopped while the setting is made, select the software trigger as the trigger source in advance.

DAOE1 Bit (D/A Output Enable 1)

The DAOE1 bit controls the D/A conversion and analog output.

When the measure against interference between D/A and A/D conversion is enabled (the DAADSCR.DAADST bit = 1), set this bit while the ADCSR.ADST bit is set to 0. To ensure that the 10-bit A/D converter remains stopped while the setting is made, select the software trigger as the trigger source in advance.

37.2.3 DADRm Format Select Register (DADPR)

Address(es): 0008 80C5h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSEL	DADRm Format Select	0: Data is flush with the right end of the D/A data register. 1: Data is flush with the left end of the D/A data register.	R/W

37.2.4 D/A A/D Synchronous Start Control Register (DAADSCR)

Address(es): 0008 80C6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0: D/A converter operation does not synchronize with 10-bit A/D converter operation. (measure against interference between D/A and A/D conversion is disabled) 1: D/A converter operation synchronizes with 10-bit A/D converter operation. (measure against interference between D/A and A/D conversion is enabled)	R/W

As a measure against interference between D/A and A/D conversion, DAADSCR switches synchronization of the timing of the start of D/A conversion with the 10-bit A/D converter synchronous D/A conversion enable input signal off or on. This register should be set while the 10-bit A/D converter is halted (while the ADCSR.ADST bit is 0 after selecting software trigger as the 10-bit A/D converter trigger).

DAADST Bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADRm register value to be converted into analog data at any time. Setting the DAADST bit to 1 allows synchronous D/A conversion with the synchronous D/A conversion enable signal from the A/D converter. Therefore, even if the DADRm register value is modified, D/A conversion does not start until the A/D converter completes A/D conversion.

Set this bit while the ADCSR.ADST bit is set to 0. To ensure that the 10-bit A/D converter remains stopped while the setting is made, select the software trigger as the trigger source in advance.

37.3 Operation

The D/A converter includes D/A conversion circuits for two channels, each of which can operate independently.When the DAOEi bit (i = 0, 1) in DACR is set to 1, D/A converter is enabled and the conversion result is output.
An operation example of D/A conversion on channel 0 is shown below. Figure 37.2 shows the timing of this operation.

1. Write the data for conversion to DADR0.
2. Set the DAOE0 bit in DACR to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time tDCONV has elapsed. The conversion result continues to be output until DADR0 is written to again or the DAOE0 bit is cleared to 0. The output value is expressed by the following formula:

$$\frac{\text{Setting value of DADR0}}{1024} \times \text{VREF}$$

3. If DADR0 is written to again, the conversion is immediately started. The conversion result is output after the conversion time tDCONV has elapsed.
   When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), it takes a maximum of one A/D conversion time for D/A conversion to start
4. If the DAOE0 bit is cleared to 0, analog output is disabled.

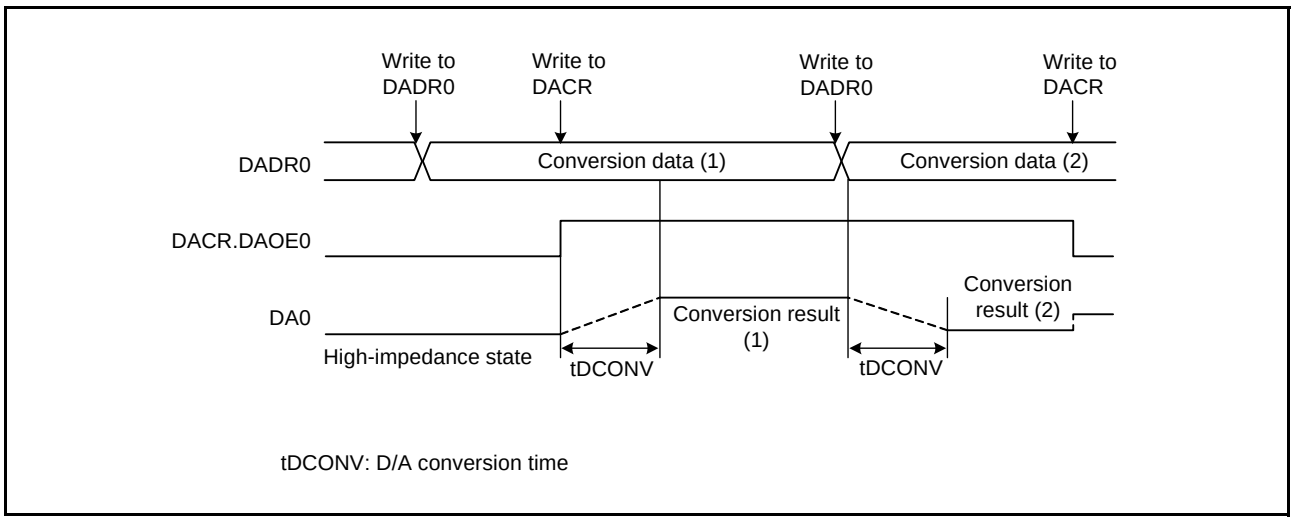


Figure 37.2 Example of D/A Converter Operation

37.3.1 Measure against Interference between D/A and A/D Conversion

When D/A conversion starts, the D/A converter generates inrush current. Since the same analog power supply is shared by the D/A converter and 10-bit A/D converter, the generated inrush current may interfere with 10-bit A/D converter operation.

To prevent such interference, the D/A converter start timing can be synchronized with the 10-bit A/D converter synchronous D/A conversion enable signal.

With the DAADSCR.DAADST bit being 1, even if the DADRm register data is modified during 10-bit A/D converter operation, D/A conversion does not start immediately but starts synchronously with A/D conversion completion. It takes a maximum of one A/D conversion time for the DADRm register data update to be reflected as the D/A conversion circuit input. Before reflection, the DADRm register value does not correspond to the analog output value.

When this function is enabled, it is impossible to check by any software means whether the DADRm register value has been D/A converted or not.

Even with DAADSCR.DAADST being 1, when the DADRm register data is modified while the 10-bit A/D converter is halted, D/A conversion starts in one PCLK clock cycle.

The following describes an example of channel 0 D/A conversion, in which the D/A converter operates synchronously with the 10-bit A/D converter.

(1) Confirm that the 10-bit A/D converter is halted. Set the DAADSCR.DAADST bit to 1.

(2) Confirm that the 10-bit A/D converter is halted. Set the DACR.DAOE0 bit to 1.

(3) Set the DADR0 register.

- If the 10-bit A/D conversion is halted when the DADR0 register is modified, D/A conversion starts in one PCLK cycle.
- If the 10-bit A/D conversion is in progress when the DADR0 register is modified, D/A conversion starts upon A/D conversion completion. If the DADR0 register is modified twice during A/D conversion, the first update may not be converted.

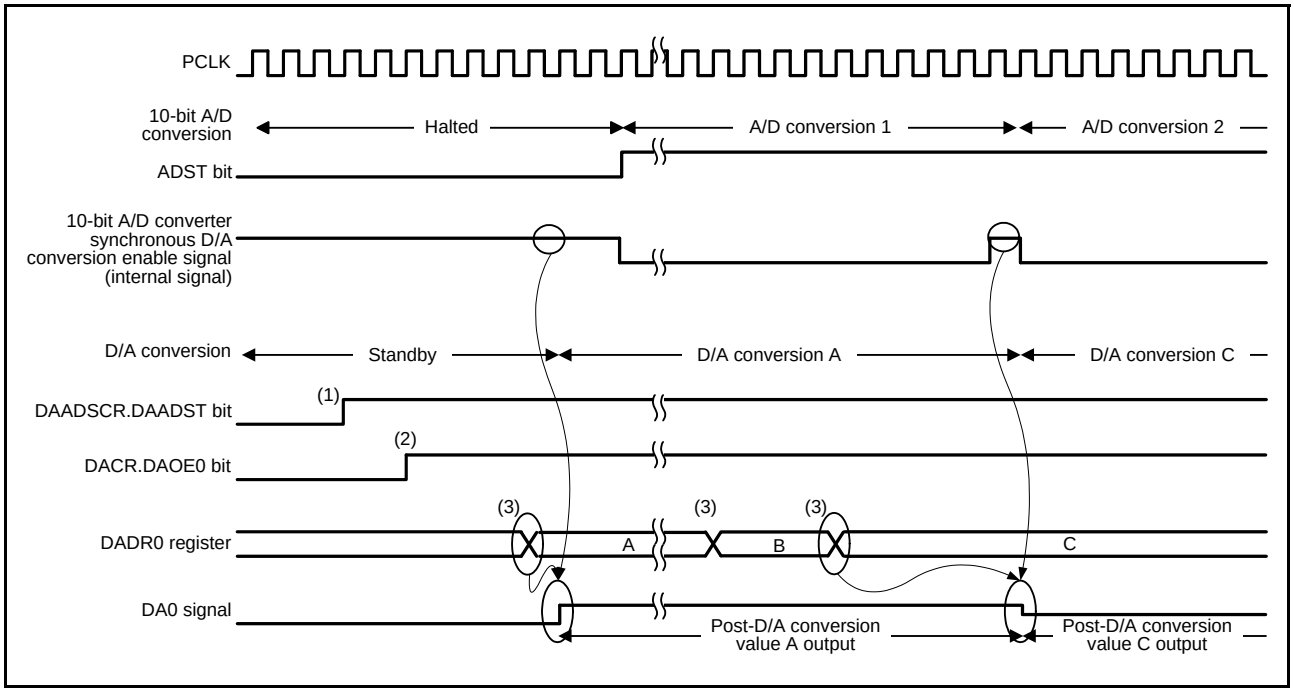


Figure 37.3 Example of Conversion when the D/A Converter is Synchronized with the 10-Bit A/D Converter

37.4 Usage Notes

37.4.1 Module-Stop Function Setting

Operation of the D/A converter can be disabled or enabled by using the module stop control register. The D/A converter is stopped at the initial value. Register access is enabled by clearing the module-stop state. For details, refer to section 12, Low Power Consumption.

37.4.2 Operation of the D/A Converter in Module-Stop State

When this MCU enters the module-stop state with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current has to be reduced in the module-stop state, disable D/A conversion by clearing the DAOE1, DAOE0, and DAE bits in DACR to 0.

37.4.3 Operation of the D/A Converter in Software Standby Mode

When this MCU enters software standby mode with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current has to be reduced in software standby mode, disable D/A conversion by clearing the DAOE1, DAOE0, and DAE bits in DACR to 0.

37.4.4 Note on Entering Deep Software Standby Mode

When this MCU enters deep software standby mode with D/A conversion enabled, the outputs of the D/A converter are placed in a high impedance state.

37.4.5 Note on Usage when Measure against Interference between D/A and A/D Conversion is Enabled

When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), do not place the 10-bit A/D converter into the module-stop state. It may halt D/A conversion in addition to A/D conversion.

38. Data Operation Circuit (DOC)

38.1 Overview

The data operation circuit (DOC) is used to compare, add, and subtract 16-bit data.
Table 38.1 lists the data operation circuit specifications and Figure 38.1 shows a block diagram of the data operation circuit.

- 16-bit data comparison and interrupt generation on a specified condition
- 16-bit data addition
- 16-bit data subtraction

Table 38.1 Specifications of Data Operation Circuit

Function	Description
Data operation function	16-bit data comparison, addition, and subtraction
Power consumption reduction function	Module stop state can be set.

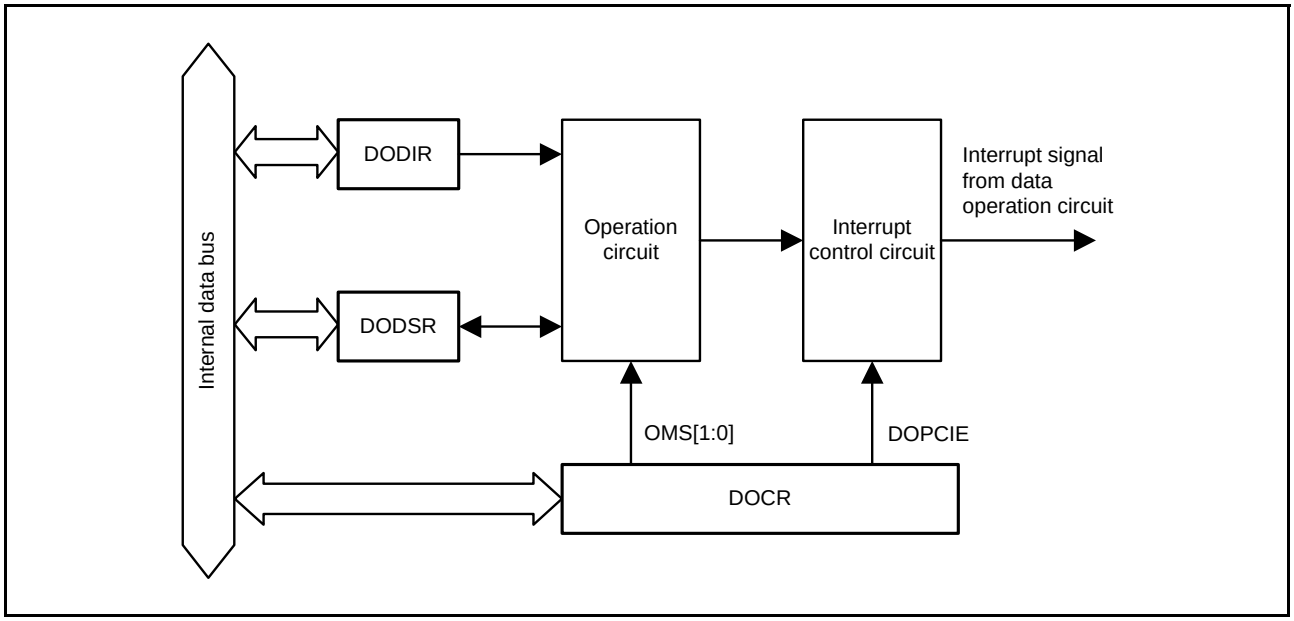


Figure 38.1 Block Diagram of Data Operation Circuit

38.2 Register Descriptions

38.2.1 DOC Control Register (DOCR)

Address: 0008 B080h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	DOPCIE	—	DCSEL	OMS [1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	OMS [1:0]	Operating Mode Select	b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
b2	DCSEL*1	Detection Condition Select	0: Detects mismatch as a result of data comparison. 1: Detects match as a result of data comparison.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DOPCIE	Data Operation Circuit Interrupt Enable	0: Disables interrupts from the data operation circuit. 1: Enables interrupts from the data operation circuit.	R/W
b5	DOPCF	Data Operation Circuit Flag	Indicates the result of an operation.	R
b6	DOPCFCL	DOPCF Clear	0: Maintains the DOPCF flag state. 1: Clears the DOPCF flag.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. This bit is only valid in data comparison mode.

OMS[1:0] Bit (Operating Mode Select)

This bit selects the operating mode of the data operation circuit.

DCSEL Bit (Detection Condition Select)

This bit is only valid in data comparison mode.

This bit selects the condition for detection in data comparison mode.

DOPCIE Bit (Data Operation Circuit Interrupt Enable)

Setting this bit to 1 enables interrupts from the data operation circuit.

DOPCF Flag (Data Operation Circuit Flag)

[Setting conditions]

- The condition selected by the DCSEL bit being met
- A result of data addition being greater than FFFFh
- A result of data subtraction being less than 0000h

[Clearing condition]

- Writing 1 to the DOPCFCL bit

DOPCFCL Bit (DOPCF Clear)

Setting this bit to 1 clears the DOPCF flag.

This bit is read as 0.

38.2.2 DOC Data Input Register (DODIR)

Address: 0008 B082h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR is a 16-bit readable/writable register in which 16-bit data for use in the operations are stored.

38.2.3 DOC Data Setting Register (DODSR)

Address: 0008 B084h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODSR is a 16-bit readable/writable register in which 16-bit data for use as a reference in data comparison mode are stored. This register also stores the results of operations in data addition and data subtraction modes.

38.3 Operation

38.3.1 Data Comparison Mode

Figure 38.2 shows an example of the steps involved in data comparison mode operation by the data operation circuit.

1. Writing 00b to the DOCR.OMS[1:0] bits selects data comparison mode.
2. The 16-bit reference data is set in DODSR.
3. 16-bit data for comparison is written to DODIR.
4. Writing of 16-bit data continues until all data for comparison have been written to DODIR.
5. If a value written to DODIR does not match that in DODSR, the DOCR.DOPCF flag is set to 1. On setting of the DOCR.DOPCIE bit to 1, a data operation circuit interrupt is also generated.

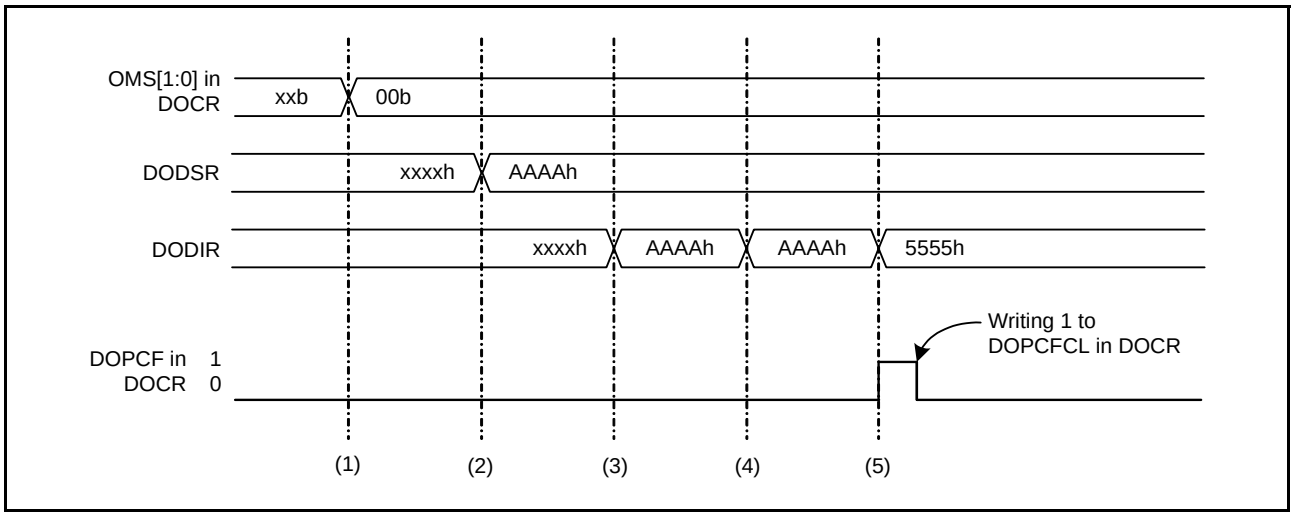


Figure 38.2 Example of Operation in Data Comparison Mode

38.3.2 Data Addition Mode

Figure 38.3 shows an example of the steps involved in data addition mode operation by the data operation circuit.

1. Writing 01b to the DOCR.OMS[1:0] bits selects data addition mode.
2. A 16-bit initial value is set in DODSR.
3. 16-bit data to be added is written to DODIR. The result of the operation is stored in DODSR.
4. Writing of 16-bit data continues until all data for addition have been written to DODIR.
5. If the result of an operation is greater than FFFFh, the DOCR.DOPCF flag is set to 1. On setting of the DOCR.DOPCIE bit to 1, a data operation circuit interrupt is also generated.

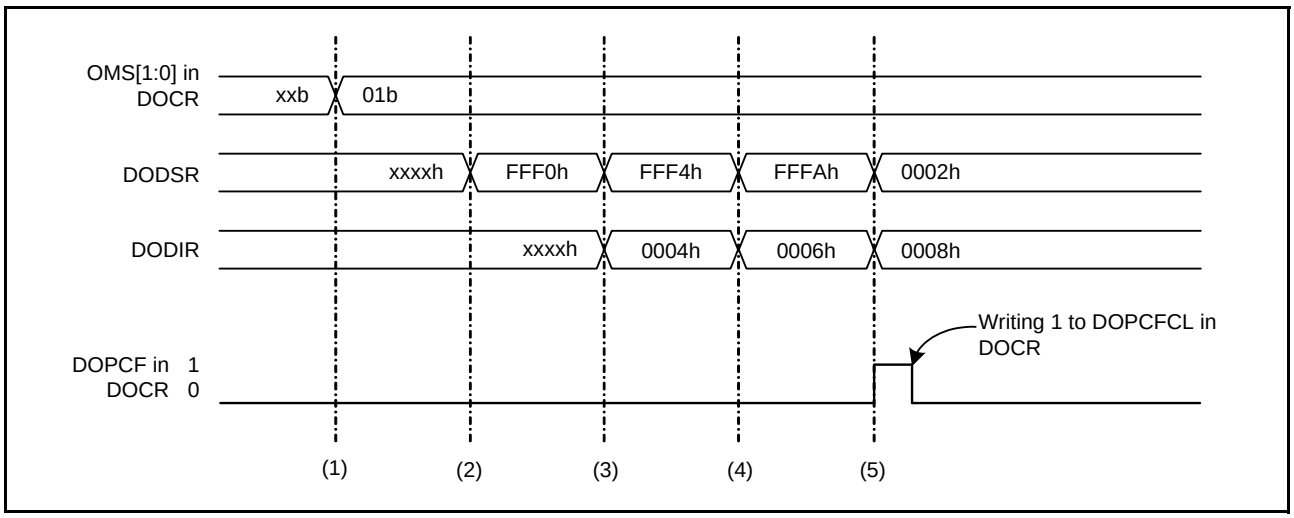


Figure 38.3 Example of Operation in Data Addition Mode

38.3.3 Data Subtraction Mode

Figure 38.4 shows an example of the steps involved in data subtraction mode operation by the data operation circuit.

1. Writing 10b to the DOCR.OMS[1:0] bits selects data subtraction mode.
2. A 16-bit initial value is set in DODSR.
3. 16-bit data to be subtracted is written to DODIR. The result of the operation is stored in DODSR.
4. Writing of 16-bit data continues until all data for subtraction have been written to DODIR.
5. If the result of an operation is less than 0000h, the DOCR.DOPCF flag is set to 1. On setting of the DOCR.DOPCIE bit to 1, a data operation circuit interrupt is also generated.

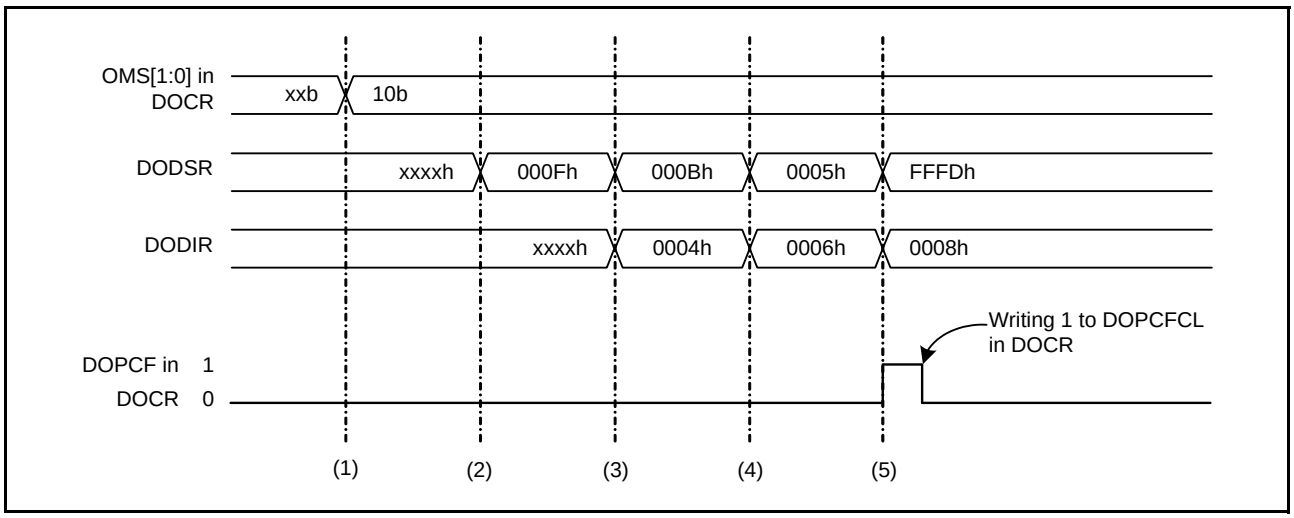


Figure 38.4 Example of Operation in Data Subtraction Mode

38.4 Interrupt Requests

The data operation circuit generates the data operation circuit interrupt as an interrupt request. When an interrupt condition arises, the status flag corresponding to the interrupt is set to 1. Table 38.2 describes the interrupt request.

Table 38.2 Interrupt Request from Data Operation Circuit

Interrupt Request	Status Flag	Interrupt Conditions
Data operation circuit interrupt	DOPCF	• The condition selected by the DOCR.DCSEL bit being met • The result of data addition being greater than FFFFh • The result of data subtraction being less than 0000h

38.5 Usage Note

38.5.1 Module Stop Function Setting

Operation of the data operation circuit can be disabled or enabled by using the module stop control register B (MSTPCRB). The data operation circuit is stopped at the initial value. Register access is enabled by canceling the module stop state. For details, see section 12, Low Power Consumption.

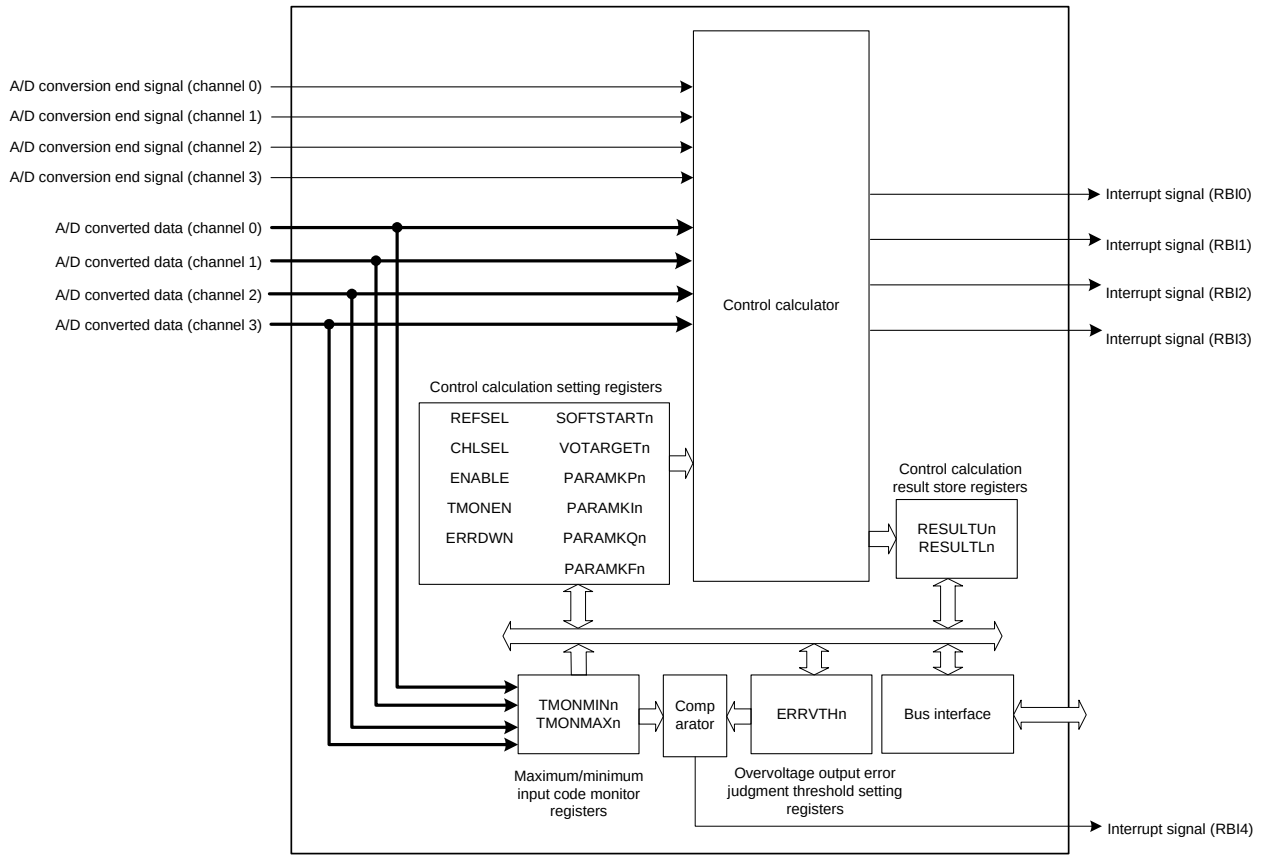
39. Digital Power Supply Controller (DPC)

39.1 Overview

The digital power supply controller (DPC) is a 16-bit fixed-point digital calculator that calculates compensation values for use in the digital control of switched-mode power supplies.
The robust control algorithm adopted for the compensator provides greater stability than a PID (proportional, integral, and derivative) compensator.
The specifications of the digital power controller are described in Table 39.1 and a block diagram is given as Figure 39.1.

Table 39.1 Digital Power Controller Specification

Item	Description
Number of units	One
Number of control channels	Up to four
Control method	Robust control algorithm
Operating precision	16-bit fixed-point
Calculation time	80 ns per control channel (in operation at 100 MHz)
Basic settings	• Internal reference voltage mode See the description of the internal reference voltage setting register. • External reference voltage mode See the description of the external reference voltage setting register.
Software starting time	Variable
Interrupt sources	Five • Four interrupt requests on completion of control calculations for each channel • One interrupt request for overvoltage output errors.
Low power consumption facility	Transitions to the module-stop state are selectable.



n: Channel number from 0 to 3

SOFTSTART0 to 3: Software start setting register 0 to 3
VOTARGET0 to 3: Reference value setting register 0 to 3
REFSEL: Reference value select register
CHLSEL: Control channel setting register
ENABLE: Control enable setting register
PARAMKP0 to 3: Control calculation parameter setting register KP0 to KP3
PARAMKI0 to 3: Control calculation parameter setting register KI0 to KI3
PARAMKQ0 to 3: Control calculation parameter setting register KQ0 to KQ3
PARAMKF0 to 3: Control calculation parameter setting register KF0 to KF3
RESULTU0 to 3: Control calculation result higher-order bits store register 0 to 3
RESULTL0 to 3: Control calculation result lower-order bits store register 0 to 3
TMONEN: Input code monitor enable setting register
TMONMAX0 to 3: Maximum input code monitor registers 0 to 3
TMONMIN0 to 3: Minimum input code monitor registers 0 to 3
ERRVTH0 to 3: Overvoltage output error judgment threshold value setting registers 0 to 3
ERRDWN: PWM shut-down at overvoltage output error setting register

Figure 39.1 DPC Block Diagram

39.2 Registers

39.2.1 Software Start Setting Registers (SOFTSTARTn) (n = 0 to 3)

Address(es): SOFTSTART0 000C 3000h, SOFTSTART1 000C 3004h, SOFTSTART2 000C 3008h, SOFTSTART3 000C 300Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SSEN	SSTM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b7-b0	SSTM[7:0]	Software Stating Time	Set software starting time	R/W
b8	SSEN	Software Start Enable	0: Software start is disabled 1: Software start is enabled	R/W
b15-b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SOFTSTARTn sets parameter to use for software start control (n = 0 to 3).

SSTM[7:0] Bits (Software Starting Time)

These bits set the rising time Tup[us], which is the time the output voltage takes to reach the reference value after PWM waveform output is started and the external elements are controlled to start the generation of output voltages.
Calculation of the value to be set in the SSTM[7:0] bits depends on the value of the REFSEL.RSEL bit.
When the REFSEL.RSEL bit is 0, values to be set in the SSTM[7:0] bits are calculated from the following equation:

$$SSTM[7:0] = (TGVO[9:0] \times Tsw) / (0.015625 \times Tup[us])$$

In the equation, TGVO[9:0] is the reference voltage setting in the reference value setting register (VOTARGETn) (n = 0 to 3), and Tsw is the PWM cycle specified by the value set in the general PWM timer cycle setting register (GTPR) of the general PWM timer GPTa.
Examples of rising-time values are listed in Table 39.2.

Table 39.2 Examples of Rising-Times and Settings

		PWM Cycle		
Time[us]	TGVO[9:0]	GTPR	Tsw[us]	SSTM[7:0]
1000	200h	32h	0.5	11h
		64h	1	21h
		C8h	2	42h
1250	100h	32h	0.5	7h
		64h	1	Eh
		C8h	2	1Bh

When the REFSEL.RSEL bit is 1, the external reference voltage to be input to the 10-bit A/D converter should be a constant value until the external switching elements are controlled and the output voltage starts rising.
Values to be set in the SSTM[7:0] bits are calculated as follows:

$$SSTM[7:0] = (EXREF[9:0] \times Tsw) / (0.015625 \times Tup[us])$$

In the above equation, EXREF[9:0] is the result of A/D conversion of the external reference voltage.

SSEN Bit (Software Start Enable)

This bit enables or disables software starting. When this bit is 0, the rising time is determined by the control calculation response characteristics controlled by the PARMKmn registers (m = P, I, Q, F; n = 0 to 3).
When the SSEN bit is 1, the rising time is determined by the time set in the SSTM bit.

39.2.2 Reference Value Setting Register (VOTARGETn) (n = 0 to 3)

Address(es): VOTARGET0 000C 3010h, VOTARGET1 000C 3014h, VOTARGET2 000C 3018h, VOTARGET3 000C 301Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TGVO[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b9-b0	TGVO[9:0]	Reference Voltage Setting	Set the target output voltage as A/D converted value.	R/W
b15-b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

VOTARGETn sets the reference voltage for the switched-mode power supply system.
The reference voltage, which is the target value for output voltage of the switched-mode power supply system is set in the 10-bit A/D converted value.

39.2.3 Reference Value Select Register (REFSEL)

Address(es): 000C 3020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSEL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RSEL	Reference Voltage Select	0: Internal reference voltage mode 1: External reference voltage mode	R/W
b15-b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

REFSEL selects the value to use as the reference voltage.

RSEL Bit (Reference Voltage Select)

This bit selects the value to use as the reference voltage, which is the target value for the output voltage of the switched-mode power supply system.
When the RSEL bit is 0, the reference voltage is the value corresponding to the setting of the VOTARGETn (n = 0 to 3).
When the RSEL bit is 1, an external input voltage value from the 10-bit A/D converter is used as the reference voltage.
When the RSEL bit is 1, input the reference voltage for control channel 0 to channel 1 of the 10-bit A/D converter and the reference voltage for control channel 2 to channel 3 of the 10-bit A/D converter.
Only these channels (channels 0 and 2) are available for use with the A/D converter; that is, this form of control can be used with no more than two channels.

39.2.4 Control Channel Setting Register (CHLSEL)

Address(es): 000C 3024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b1, b0	CSEL[1:0]	Number of Control Channels Select	(Internal Reference Voltage Mode) 00: One channel (for converted data of the 10-bit A/D converter ch0) 01: Two channels (for converted data of the 10-bit A/D converter ch0 and ch1) 10: Three channels (for converted data of the 10-bit A/D converter ch0 to ch2) 11: Four channels (for converted data of the 10-bit A/D converter ch0 to ch3) (External Reference Voltage Mode) 00: One channel (for converted data of the 10-bit A/D converter ch0) 01: Two channels (for converted data of the 10-bit A/D converter ch0 and ch2) 10: Setting prohibited 11: Setting prohibited	R/W
b15-b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CHLSEL sets the number of control channels.

CSEL[1:0] Bits (Number of Control Channels Select)

These bits select a number of control channels from one to four. When two or more control channels are selected, the results of 10-bit A/D conversion on channels 0 to 3 are applied to control in that sequence. Operate the 10-bit A/D converter in single-cycle scan mode for the relevant channels.

39.2.5 Control Enable Setting Register (ENABLE)

Address(es): 000C 3028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	EN3	EN2	EN1	EN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	EN0	Control Channel 0 Start	0: Control is disabled 1: Control is enabled	R/W
b1	EN1	Control Channel 1 Start	0: Control is disabled 1: Control is enabled	R/W
b2	EN2	Control Channel 2 Start	0: Control is disabled 1: Control is enabled	R/W
b3	EN3	Control Channel 3 Start	0: Control is disabled 1: Control is enabled	R/W
b15-b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ENABLE sets start and stop of compensatory calculation.

ENn Bit (Control Channel n Start) (n = 0 to 3)

These bits start and stop compensatory calculation for each control channel.

39.2.6 Control Calculation Parameter Setting Register Km (PARAMKmn) (m = P, I, Q, F; n = 0 to 3)

Address(es): PARAMKP0 000C 302Ch, PARAMKI0 000C 3030h, PARAMKQ0 000C 3034h, PARAMKF0 000C 3038h
PARAMKP1 000C 303Ch, PARAMKI1 000C 3040h, PARAMKQ1 000C 3044h, PARAMKF1 000C 3048h
PARAMKP2 000C 304Ch, PARAMKI2 000C 3050h, PARAMKQ2 000C 3054h, PARAMKF2 000C 3058h
PARAMKP3 000C 305Ch, PARAMKI3 000C 3060h, PARAMKQ3 000C 3064h, PARAMKF3 000C 3068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMKmn sets control parameter codes.
The four coefficients for the calculator (KP, KI, KQ, and KF) are set as control parameter codes in a 16-bit fixed-point (two's complement) representation. For details of the data format, see section 39.3.1.5, Control Calculation Parameter Setting.

39.2.7 Control Calculation Result Higher-/Lower-Order Bits Store Register (RESULTmn) (m = U, L; n = 0 to 3)

- RESULTUn

Address(es): RESULTU0 000C 306Ch, RESULTU1 000C 3070h, RESULTU2 000C 3074h, RESULTU3 000C 3078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- RESULTLn

Address(es): RESULTL0 000C 306Eh, RESULTL1 000C 3072h, RESULTL2 000C 3076h, RESULTL3 000C 307Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESULTmn stores the control calculation results.

39.2.8 Input Code Monitor Enable Setting Register (TMONEN)

Address(es): 000C 307Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TMEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMEN	Input Code Monitor Enable	0: Monitor is disabled 1: Monitor is enable	R/W
b15-b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TMONEN enables and disables input code monitor function.

TMEN Bit (Input Code Monitor Enable)

Setting this bit to 1 enables the function to store the maximum and minimum values of the target A/D conversion results in TMONMAXn and TMONMINn, respectively.
Setting this bit to 0 clears the value stored in TMONMAXn and TMONMINn.

39.2.9 Maximum Input Code Monitor Register (TMONMAXn) (n = 0 to 3)

Address(es): TMONMAX0 000C 3080h, TMONMAX1 000C 3088h, TMONMAX2 000C 3090h, TMONMAX3 000C 3098h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VMAX[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b9-b0	VMAX[9:0]	Max. A/D-Converted Value	Retains the max. A/D-converted value.	R/W
b15-b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TMONMAXn retains the max. value of the target A/D-converted value when TMONEN.TMEN is set to 1.
The values are updated at the end of A/D conversion of each channel.
Setting TMONEN.TMEN to 0 clears the values stored.

39.2.10 Minimum Input Code Monitor Register (TMONMINn) (n = 0 to 3)

Address(es): TMONMIN0 000C 3084h, TMONMIN1 000C 308Ch, TMONMIN2 000C 3094h, TMONMIN3 000C 309Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VMIN[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b9-b0	VMIN[9:0]	Min. A/D-Converted Value	Retains the min. A/D-converted value.	R/W
b15-b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TMONMINn retains the min. value of the target A/D-converted value when TMONEN.TMEN is set to 1.
The values are updated at the end of A/D conversion of each channel.
Setting TMONEN.TMEN to 0 clears the values stored.

39.2.11 Overvoltage Output Error Judgment Threshold Setting Register (ERRVTHn) (n = 0 to 3)

Address(es): ERRVTH0 000C 30A0h, ERRVTH1 000C 30A4h, ERRVTH2 000C 30A8h, ERRVTH3 000C 30ACh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ERVH[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b9-b0	ERVH[9:0]	Overvoltage Output Error Detecting Threshold	Sets the threshold value to compare with the A/D-converted value for output voltage error judgment.	R/W
b15-b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ERRVTHn sets the threshold to judge an overvoltage error.
When the TMONMAXn value exceeds the ERRVTHn value, it is recognized as an overvoltage output error and an overvoltage output error interrupt request (RBI4) is output.
This function is available only when the TMONEN.TMEN bit is set to 1.

39.2.12 PWM Shut-Down at Overvoltage Output Error Register (ERRDWN)

Address(es): 000C 30D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EPDL	EPDS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	EPDS	Operation Mode Select at Detection of Overvoltage Output Error	0: Shutdown by software 1: Forced shutdown by hardware	R/W
b1	EPDL	PWM Forced Output Level Select at Detection of Overvoltage Output Error	(Enabled when EPDS = 1) 0: Output at low level 1: Output at high level	R/W
b15-b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ERRDWN sets the operation during an overvoltage error.

EPDS Bit (Operation Mode Select at Detection of Overvoltage Output Error)

This bit enables and disables forced writing function to RESULTmn when the output voltage is judged as overvoltage error state.

When this bit is 0, forced writing function to RESULTmn is disabled.

When this bit is 1, a fixed value is written to RESULTmn that stops PWM waveform output.

EPDL Bit (PWM Forced Output Level Select at Detection of Overvoltage Output Error)

When this bit is 1, the value to be written to RESULTmn is selected.

When this bit is 0, 0000h is written to RESULTmn.

When this bit is 1, FFFFh is written to RESULTmn.

39.3 Description of Operation

Figure 39.2 shows the operation flow of digital power controller.

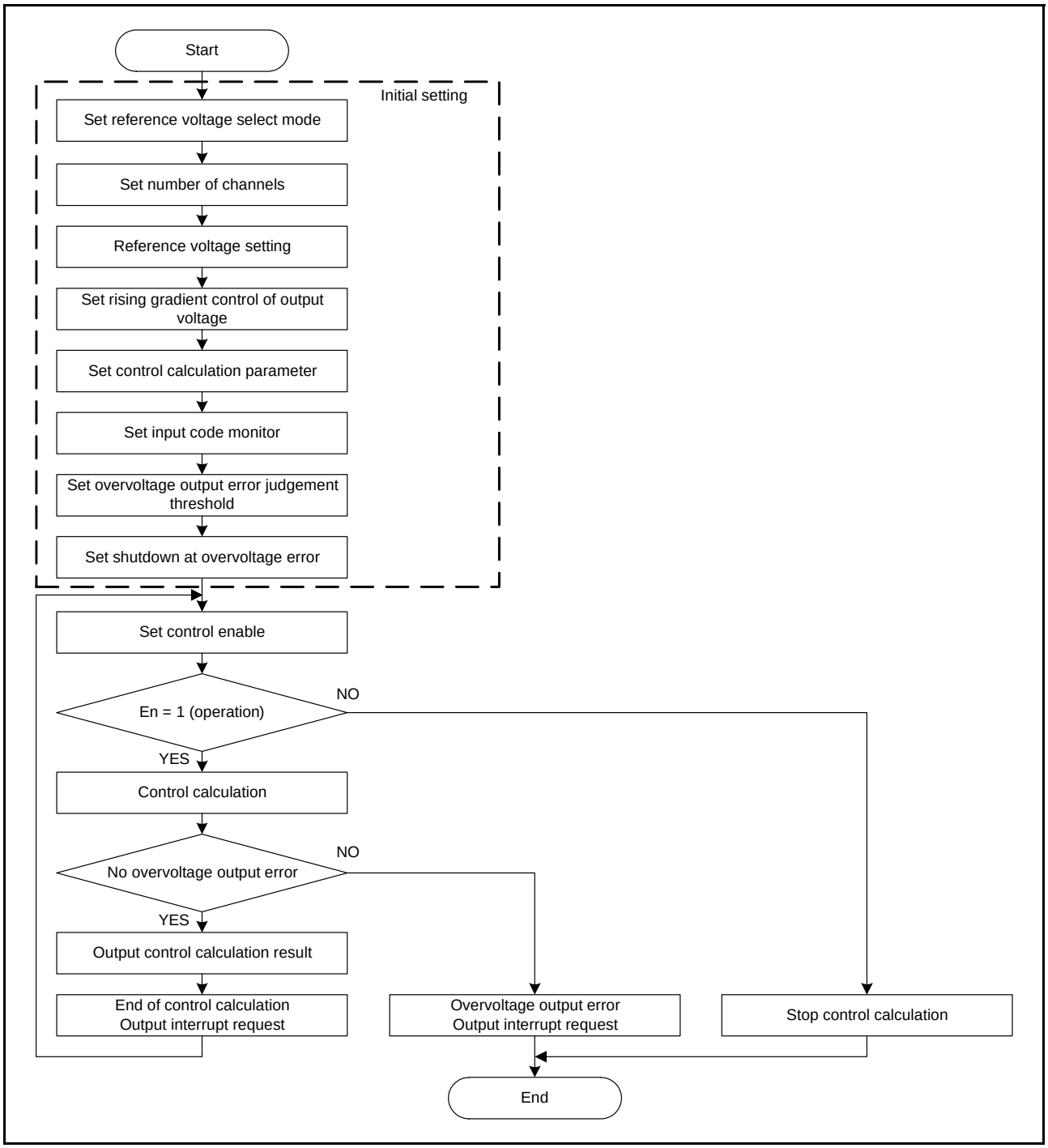


Figure 39.2 Operation Flow

39.3.1 Initial Setting of Internal Reference Voltage Mode

39.3.1.1 Voltage Reference Mode Setting

The reference value that is the target value for output voltage is selected by the REFSEL register. In internal reference voltage mode, set the REFSEL register to 0.

39.3.1.2 Number of Control Channels Setting

In internal reference voltage mode, a number of control channels is selected from one to four. When two or more control channels are selected, the results of 10-bit A/D conversion on channels 0 to 3 are applied to control in that sequence. Operate the 10-bit A/D converter in single-cycle scan mode for the relevant control channels.
The number of control channels is set with the CHLSEL register.

39.3.1.3 Reference Voltage Setting

The reference voltage for each control channel is set with the VOTARGETn register (n = 0 to 3).
The digital power control calculator performs compensatory calculation with the value set in the VOTARGETn register as the reference voltage.
The value to be set in the VOTARGETn register is calculated as follows:

Voltage per A/D converter output code 1d
= A/D converter dynamic range (Vad) / 2^{10} reference voltage (vref)
= Output voltage (Vo) / Voltage per A/D converter output code 1d (V1d)

The value examples set in the VOTARGETn register is explained with the typical reference voltages in Table 39.3.

Table 39.3 Example of VOTARGETn Setting Values

VREF Value of 10-bit A/D converter	Reference Voltage	Value set in VOTARGETn
3.0V	3.0V	3FFh
	2.5V	354h
	2.0V	2A9h
	1.5V	1FFh
	1.0V	154h
	0.5V	0A9h
	0V	000h

39.3.1.4 Software Start Control

The software start control function controls PWM waveform to moderate the rising of the output voltage generated by the external switching element. The aims are to prevent unintended current flows or overshooting of the output voltage when controlling the external switching element to start output voltage generation in response to the PWM waveform output.

When the SOFTSTARTn.SSEN bit (n = 0 to 3) is 1, the control channels are controlled so that the output voltage reaches the reference voltage after the rising time set with the SOFTSTARTn.SSTM[7:0] bits has elapsed.

When the SOFTSTARTn.SSEN bit is 0, the rising time is determined by the control calculator response characteristics controlled by the PARMKmn registers (m = P, I, Q, F; n = 0 to 3).

Examples of software start control settings are given in Table 39.4 and examples of operation are shown in Figure 39.3.

Table 39.4 Software Starting Time Control Setting

	MHz	**0.5**			**1**			**2**		
Switch Cycle	**ns**	**2000**			**1000**			**500**		
SOFTSTARTn[7:0]	8h	1	2	3	1	2	3	1	2	3
Reference value (VOTARGETn)	10'd	341	341	341	341	341	341	341	341	341
Software starting time	ms	43.648	21.824	14.322	21.824	10.912	7.161	10.912	5.456	3.5805

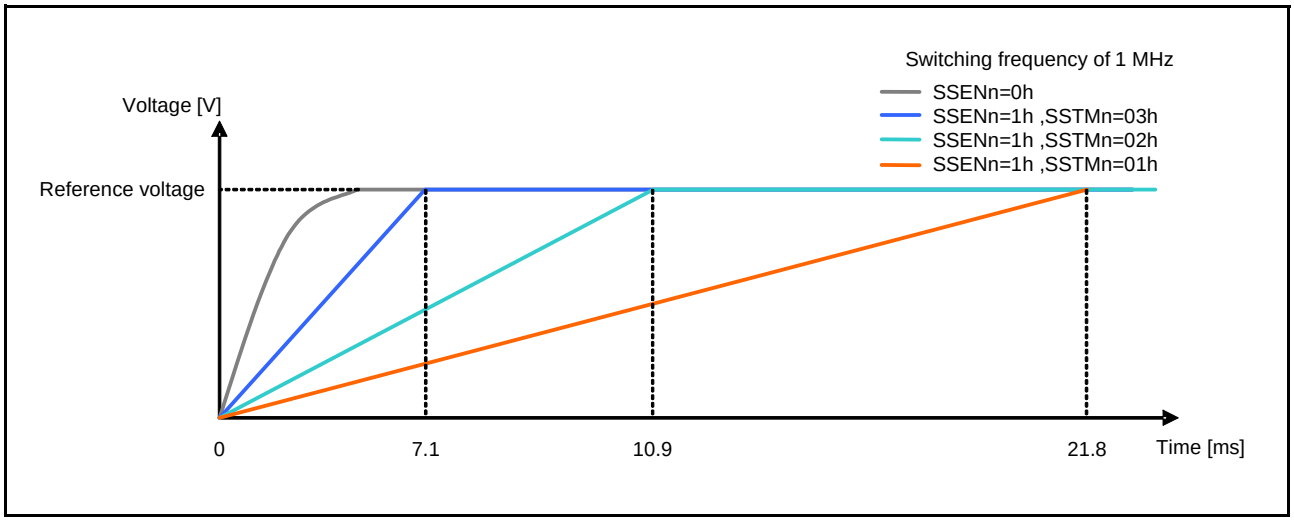
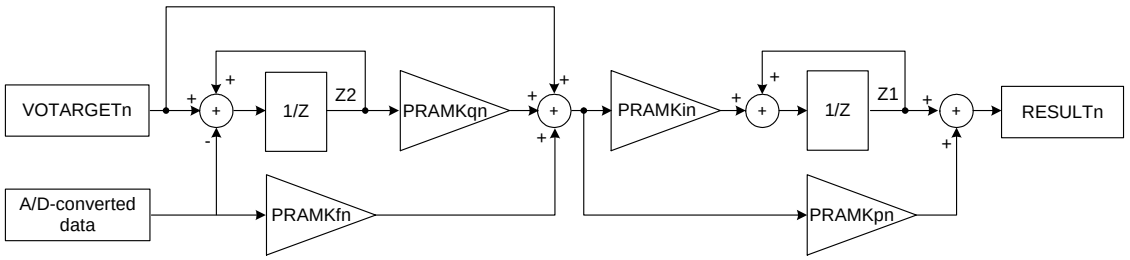


Figure 39.3 Example Operation of Software Starting Time Setting Function

39.3.1.5 Control Calculation Parameter Setting

Figure 39.4 shows the signal flow in calculations for control by the DPC. 1/Z represents the unit delay.
Control calculation is performed on the A/D-converted data with the values set in PARMKmn so that the A/D-converted data matches the value set in VOTARGETn. The result of calculation is output to RESULTmn.



$$RESULTn = Z1 + (Z2 \cdot PARAMKqn + VOTARGETn + PARAMKfn \cdot A/D\text{-}converted\ data) \cdot PARAMKp$$
$$Z1 = Z1 + (Z2 \cdot PARAMKqn + VOTARGETn + PARAMKfn \cdot A/D\text{-}converted\ data) \cdot PARAMKi$$
$$Z2 = Z2 + VOTARGETn - A/D\text{-}converted\ data$$

Figure 39.4 Signal Flow for Control Calculation

The data format for PARAMKmn is 16-bit fixed-point (two's complement) representation. The highest order bit is a sign, the next 5 bits are the integer part and the 10 bits following that are the fractional parts.

MSB(15)		LSB(0)
1 bit Sign part 1: Negative 0: Positive	5 bits Integer part	10 bits Fractional part

Please contact a Renesas Electronics sales office for details on setting the PARAMKmn register.

39.3.1.6 Input Code Monitor Setting

The maximum value and minimum value of the output voltage of each control channels can be monitored.
The maximum and minimum A/D-converted values are stored in TMONMAXn and TMONMINn, respectively.

Input code monitor setting function is enabled by setting the TMONEN.TMEN bit to 1.
The timing to store the A/D-converted value to TMONMAXn and TMONMINn is determined by the setting of REFSEL.
When REFSEL.RSEL is 1, with the A/D converted-value reaches or exceeds the value in VOTARGETn.TGVO[9:0], the maximum and minimum values are stored in TMONMAXn and TMONMINn, respectively.

Once the storing starts, it continues even when the A/D-converted value falls below the value in VOTARGETn.TGVO[9:0].

When REFSEL.RSEL is 0, with the A/D converted-value reaches or exceeds the value converting the external input voltage as the external reference voltage by the 10-bit A/D converter, the maximum and minimum values are stored in TMONMAXn and TMONMINn, respectively.

Once the storing starts, it continues even when the A/D-converted value falls below the value converting the external

input voltage as the external reference voltage by the 10-bit A/D converter

Setting the TMONEN.TMEN bit to 0 clears the values stored in TMONMAXn and TMONMINn.

39.3.1.7 Overvoltage Output Error Detect Function

This function detects overvoltage output state of each control channel.
When the TMONMAXn value exceeds the ERRVTHn value, it is recognized as an overvoltage output error and an overvoltage output error interrupt request (RBI4) is output.
Enable input code monitor function to use overvoltage output error detect function.
Operation at detection of overvoltage output error is selected with the ERRDWN.EPDS bit. When the ERRDWN.EPDS bit is 0, no processing is performed. Change the setting of GPT to stop the PWM output.
When the ERRDWN.EPDS bit is 1, a fixed value is forcedly written to RESULTmn and with this value, the setting value to stop PWM output can be transferred to the GPT that outputs PWM waveform.
The value to be written to RESULTmn is determined by the setting of the ERRDWN.EPDL bit.
When the ERRDWN.EPDL bit is 0, 0000h is written to RESULTmn.
When the ERRDWN.EPDL bit is 1, FFFFh is written to RESULTmn.
Set the ERRDWN.EPDL bit according to the active level of the PWM output generated by the GPT.
Figure 39.5 shows the operation with ERRDWN.EPDS = 1 and ERRDWN.EPDL = 0.

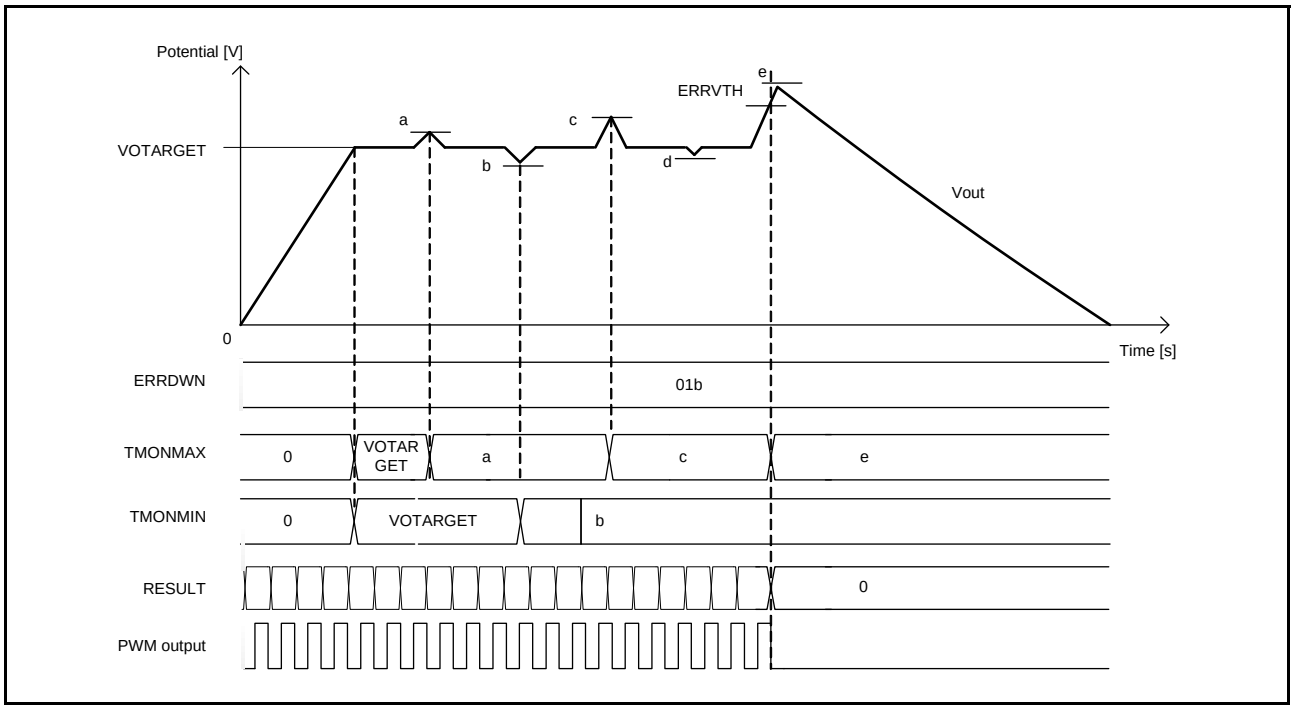


Figure 39.5 Shutdown at Overvoltage Output Error

39.3.2 Operation in Internal Reference Voltage Mode

The DPC operates in combination with the 10-bit A/D converter (AD). Set the 10-bit A/D converter before starting DPC operation.
After the initial settings, set the ENABLE.ENn bit to 1 to start the operation. Setting the ENABLE.ENn bit to 1 initiates control calculation of A/D-converted data in each control channel triggered by A/D conversion end signal. The bits ENABLE.EN0, ENABLE.EN1, ENABLE.EN2, and ENABLE.EN3 corresponds to the 10-bit A/D converter channel 0, 1, 2, and 3, respectively.
After the ENABLE.ENn bit is set to 1, control operation is performed every time the relevant A/D conversion end signal is input. The result of control calculation is stored in RESULTUn and RESULTLn. The result of control calculation is

used for PWM waveform generation at the general PWM timer (GPT). Set the RESULTUn value to the general PWM timer compare capture register (GTCCR) of GPT and the RESULTLn value to the rising output delay register (GTDLYRA, GTDLYRB) of GPT to reflect the calculation result to the PWM waveform. Control calculation end interrupt requests (RBI0 to RBI3) are issued when the control calculation of each control channel ended (calculation result is output to the control calculation result store register). With this RBIn, the RESULTmn value can be transferred to GPT by DMAC or DTC transfer.

After control calculation is started, setting 0 to ENABLE.ENn stops the calculation and outputs 0000h to as the control calculation result of the relevant control channel. When 0 is set to the ENABLE.ENn, control calculation for the relevant control channel is not performed even when a new A/D conversion end signal is input. If 1 is set to the ENABLE.ENn after output of 0000h as the control calculation result of the relevant control channel, control calculation is resumed.

When input code monitor setting is enabled and an overvoltage output error is detected, an overvoltage output error interrupt request signal (RBI4) is output.

39.3.3 Timing Example of Operation in Internal Reference Voltage Mode

39.3.3.1 Internal Reference Voltage Mode (Operation at 2 MHz of Switching Frequency with One Control Channel)

Figure 39.6 shows the waveform at operation in internal reference voltage mode at 2 MHz of switching frequency with one channel.

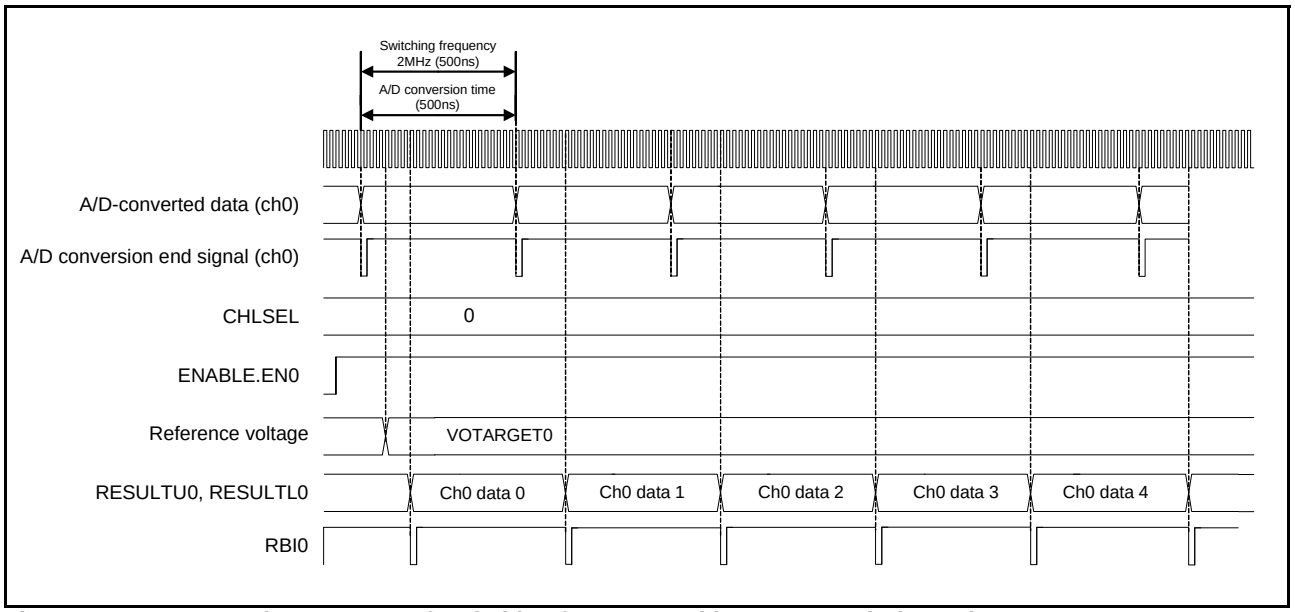


Figure 39.6 Operation at 2 MHz of Switching frequency with One Control Channel

39.3.3.2 Internal Reference Voltage Mode (Simultaneous Operations at 1 MHz of Switching frequency with Two Control Channels)

Figure 39.7 shows the waveform at simultaneous operations in internal reference voltage mode at 1 MHz of switching frequency with two control channels.

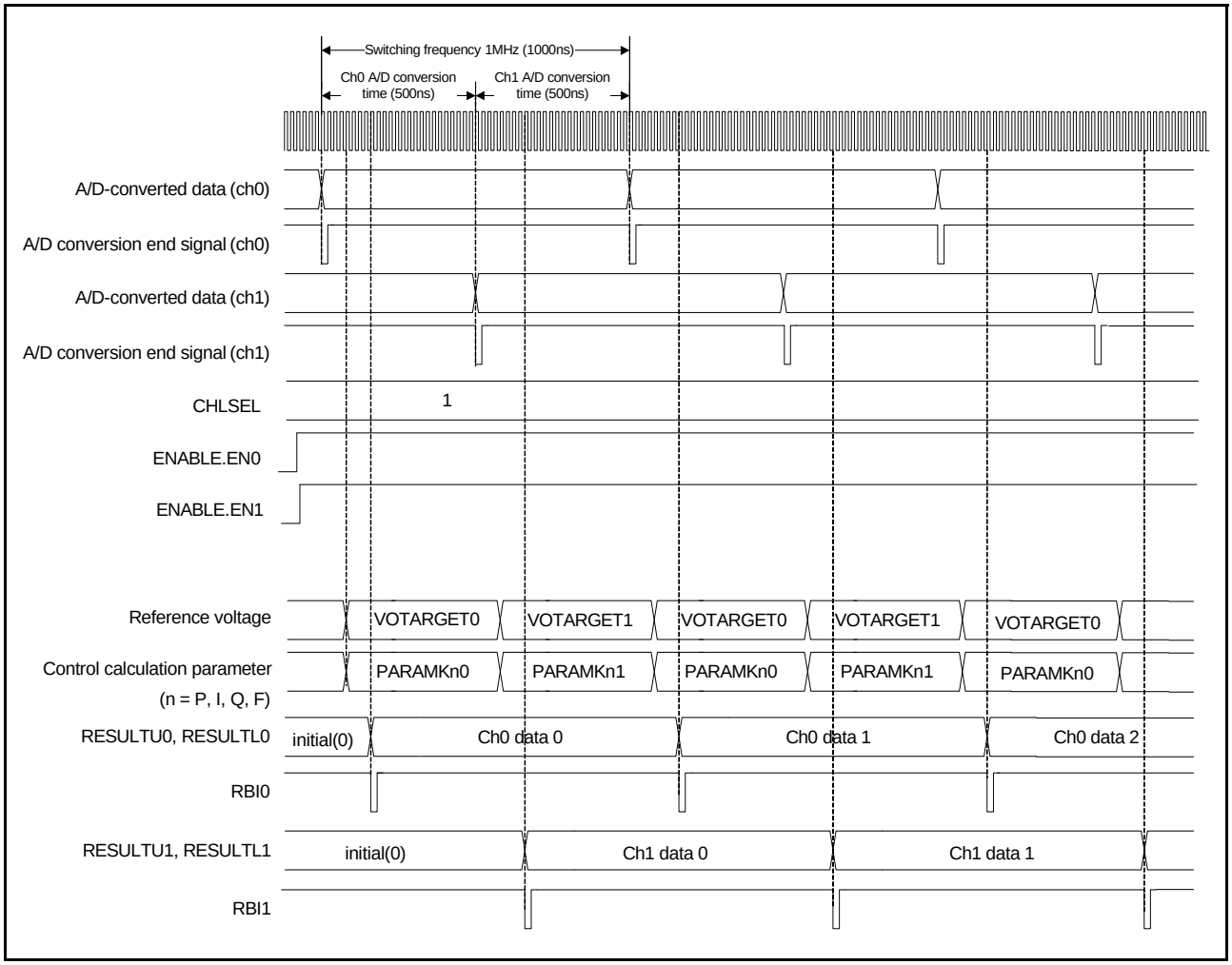


Figure 39.7 Simultaneous Operations at 1 MHz of Switching Frequency with Two Control Channels

39.3.3.3 Internal Reference Voltage Mode (Simultaneous Operations at 500 kHz of Switching frequency with Four Control Channels)

Figure 39.8 shows the waveform at simultaneous operations in internal reference voltage mode at 500 kHz of switching frequency with four control channels.

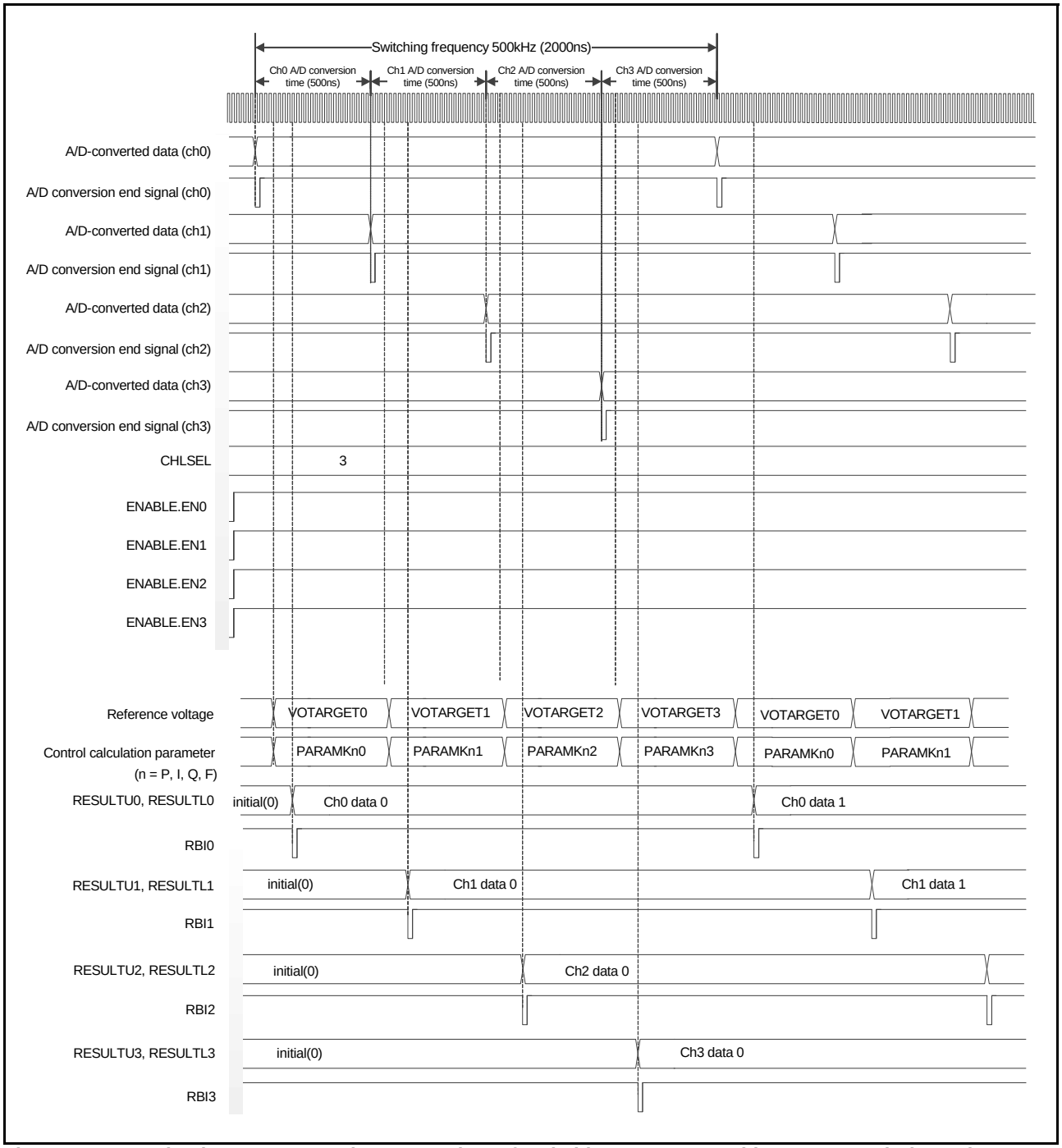


Figure 39.8 Simultaneous Operations at 500 kHz of Switching Frequency with Four Control Channels

Figure 39.9 shows the enable operation waveform at simultaneous operations in internal reference voltage mode at 500 kHz of switching frequency with four PWM channels.

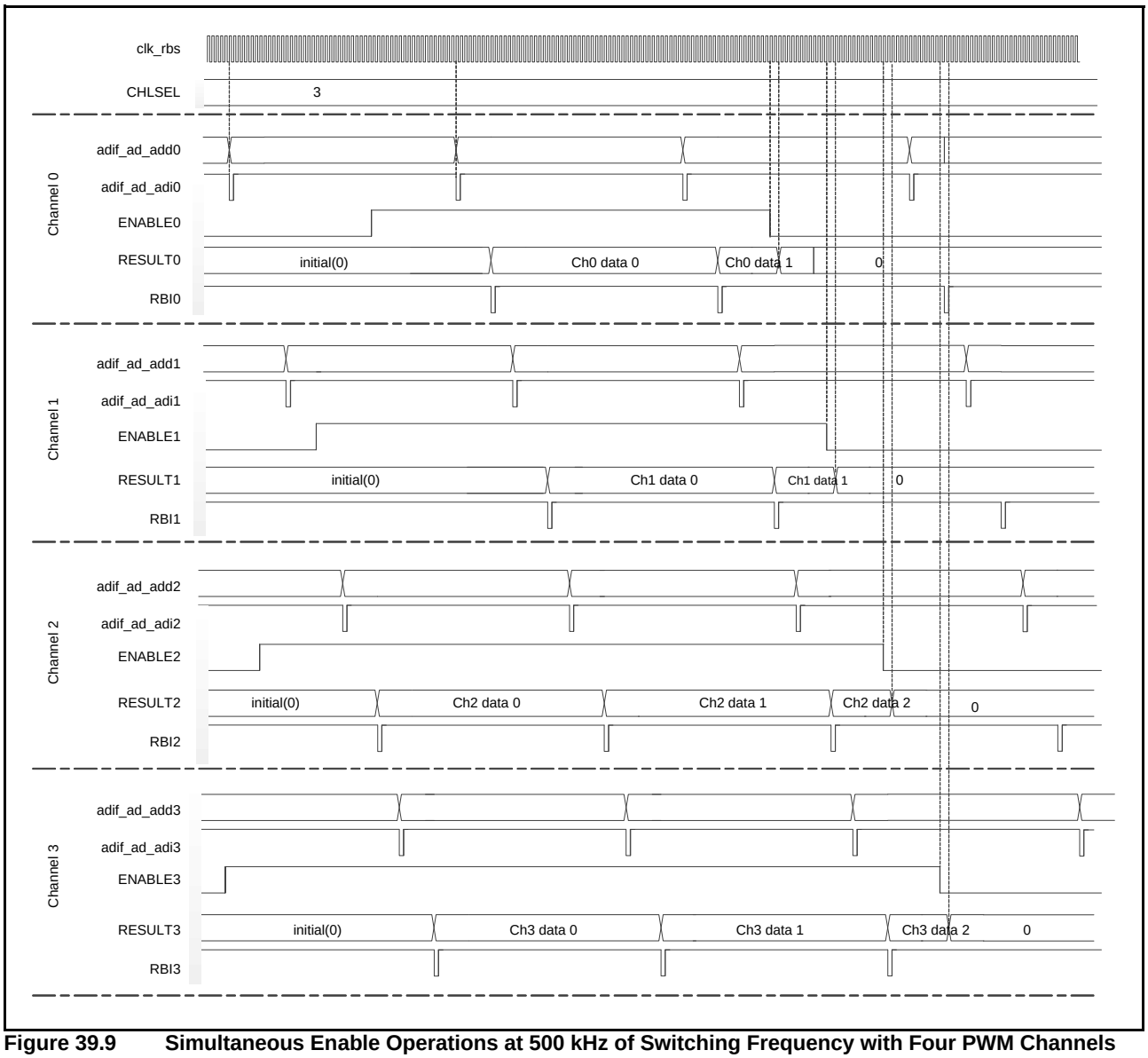


Figure 39.9 Simultaneous Enable Operations at 500 kHz of Switching Frequency with Four PWM Channels

39.3.4 Operation Example of Input Code Monitor Function

Figure 39.10 shows the waveform of input code monitor function. Updates of the TMONMAXn and TMONMINn values starts when the A/D-converted data exceeds the VOTARGETn value.

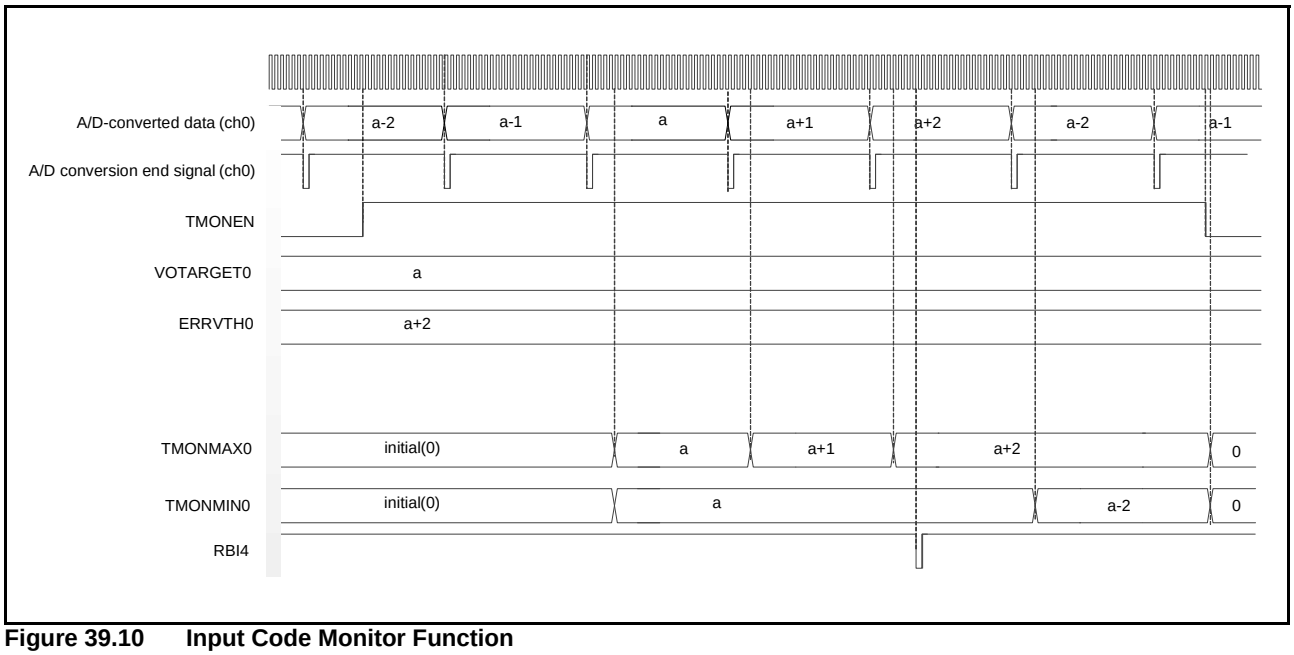


Figure 39.10 Input Code Monitor Function

39.3.5 Initial Setting of Internal Reference Voltage Mode

39.3.5.1 Voltage Reference Mode Setting

The reference value that is the target value for output voltage is selected by the REFSEL register. In external reference voltage mode, set the REFSEL register to 1.

39.3.5.2 Number of Control Channels Setting

In external reference voltage mode, the number of control channels is one or two. When one control channel is selected, the converted result of the 10-bit A/D converter channel 0 is the control channel input and the converted result of the 10-bit A/D converter channel 1 is the reference voltage of channel 0. When two control channels are selected, the converted result of the 10-bit A/D converter channel 0 is the control channel 0 input and the converted result of the 10-bit A/D converter channel 1 is the reference voltage of channel 0. The converted result of the 10-bit A/D converter channel 2 is the control channel 1 input and the converted result of the 10-bit A/D converter channel 3 is the reference voltage of channel 1. The number of control channels is set with the CHLSEL register.

39.3.5.3 Reference Voltage Setting

The reference voltage of control channels are determined by the conversion results of the 10-bit A/D converter channel 1 and channel 3.

39.3.5.4 Software Start Control Setting

See section 39.3.1.4, Software Start Control.

39.3.5.5 Control Calculation Parameter Setting

See section 39.3.1.5, Control Calculation Parameter Setting.

39.3.5.6 Input Code Monitor Setting

See section 39.3.1.6, Input Code Monitor Setting.

39.3.5.7 Overvoltage Output Error Judgment Threshold Setting

See section 39.3.1.7, Overvoltage Output Error Detect Function.

39.3.6 External Reference Voltage Mode

The DPC operates in combination with the 10-bit A/D converter (AD). Set the 10-bit A/D converter before starting DPC operation.

After the initial settings, set the ENABLE.ENn bit to 1 to start the operation. For one control channel, set the ENABLE.EN0 and ENABLE.EN1 bits to 1. For two control channels, set the ENABLE.EN0, ENABLE.EN1, ENABLE.EN2, and ENABLE.EN3 bits to 1.

Setting the ENABLE.ENn bit to 1 initiates control calculation of A/D-converted data in each control channel triggered by A/D conversion end signal. After the ENABLE.ENn bit is set to 1, control operation is performed every time the relevant A/D conversion end signal is input.

After control calculation is started, setting 0 to ENABLE.ENn stops the calculation and outputs 0000h to as the control calculation result of the relevant control channel.

When 0 is set to the ENABLE.ENn, control calculation for the relevant control channel is not performed even when a new A/D conversion end signal is input.

If 1 is set to the ENABLE.ENn after output of 0000h as the control calculation result of the relevant control channel, control calculation is resumed.

Control calculation end interrupt requests (RBI0 or RBI2) are issued when the control calculation of each control channel ended (calculation result is output to the control calculation result store register).

When input code monitor setting is enabled and an overvoltage output error is detected, an overvoltage output error interrupt request signal (RBI4) is output.

39.3.7 Timing Example of Operation in External Reference Voltage Mode

39.3.7.1 External Reference Voltage Mode (Operation at 500 kHz of Switching frequency with Two Channels)

Figure 39.11 shows the waveform at simultaneous operations in internal reference voltage mode at 500 kHz of switching frequency with two PWM channels.

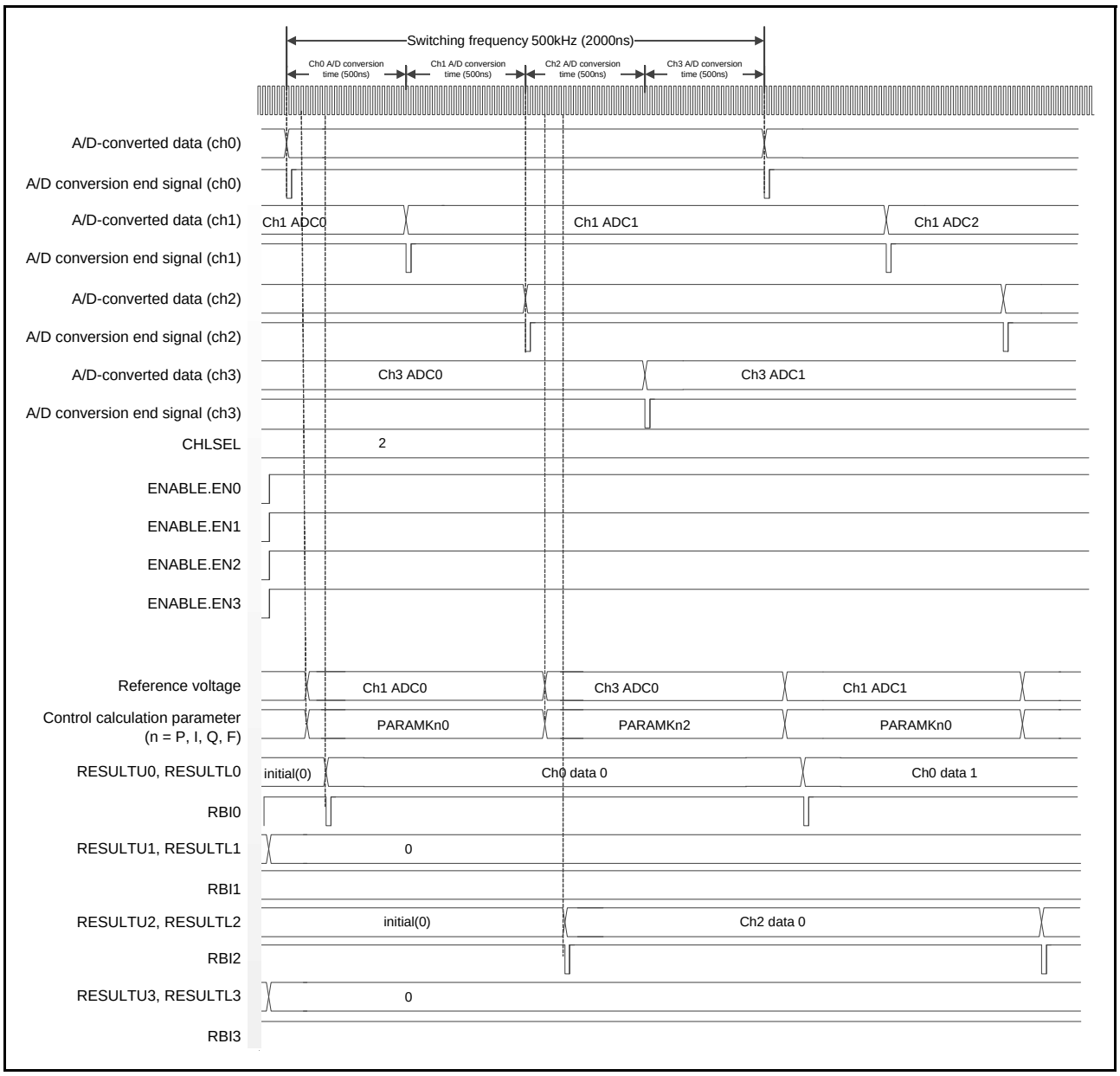


Figure 39.11 Simultaneous Operations at 500 kHz of Switching Frequencies with Two Channels

39.3.7.2 Operation of Input Code Monitor Function

See section 39.2.3, Reference Value Select Register (REFSEL).

39.4 Interrupt Sources

DPC has two interrupt sources, control calculation end interrupt for each control channel and calculation error interrupt With the control calculation end interrupt for each control channel allows data transfer using DTC and DMAC. Table 39.5 lists the interrupt sources for DPC. For data transfer using DTC or DMAC, enable these devices prior to DPC setting. For the settings of DTC and DMAC, see section 18., DMA Controller (DMACA) and section 19., Data Transfer Controller (DTCa).

Table 39.5 DPC Interrupt Sources

Interrupt Source	Symbol	Interrupt Condition	Activation of DTC and DMAC
End of control calculation for channel 0	RBI0	Control calculation result of PWM channel 0 is stored	Enabled
End of control calculation for channel 1	RBI1	Control calculation result of PWM channel 1 is stored	Enabled
End of control calculation for channel 2	RBI2	Control calculation result of PWM channel 2 is stored	Enabled
End of control calculation for channel 3	RBI3	Control calculation result of PWM channel 3 is stored	Enabled
Overvoltage output error	RBI4	TMONEN = 1 and VOTARGETn > ERRVTHn	Disabled

39.5 Usage Notes

39.5.1 Module-Stop Function Setting

DPC operation can be disabled or enabled using the module-stop control register C (MSTPCRC). The DPC module is stopped at the initial value. Register access is enabled by canceling the module-stop state. For details, see section 12., Low Power Consumption.

40. RAM

This MCU has an on-chip high-speed static RAM.

40.1 Overview

Table 40.1 lists the specifications of the RAM.

Table 40.1 Specifications of RAM

Item	Description
RAM capacity	48 Kbytes *2
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.*1
Low-power consumption function	The module-stop state is selectable.

Note 1. Selectable by the RAME bit in SYSCR1. For details on SYSCR1, see section 3.2.4, System Control Register 1 (SYSCR1) or section 4.2.3, System Control Register 1 (SYSCR1).

Note 2. The capacity of RAM differs depending on the products.

RAM Capacity	RAM Address
48 Kbytes	RAM0: 0000 0000h to 0000 BFFFh
32 Kbytes	RAM0: 0000 0000h to 0000 7FFFh
24 Kbytes	RAM0: 0000 0000h to 0000 5FFFh
8 Kbytes	RAM0: 0000 0000h to 0000 1FFFh

40.2 Operation

40.2.1 Low-Power Consumption Function

Power consumption can be reduced by setting module stop control register C (MSTPCRC) to stop supply of the clock signal to RAM.

If the MSTPC0 bit in MSTPCRC is set to 1, supply of the clock signal to RAM0 is stopped.

The module (RAM0) is thus placed in the module-stop state by stopping supply of the clock signals. The RAM operates after a reset.

RAM is not accessible if it is in the module-stop state. A transition to the module-stop state should not be made while access to RAM is in progress.

For details on the MSTPCRC register, see section 12, Low Power Consumption.

41. Flash Memory

This MCU has a maximum 512-Kbyte flash memory for storing code (ROM) and a 32- and 8- Kbyte flash memory for storing data (E2 DataFlash).

41.1 Overview

Table 41.1 lists the specifications of the ROM and E2 DataFlash memory, and Figure 41.1 is a block diagram of the ROM, E2 DataFlash memory, and related modules.
Regarding the configuration of the ROM memory area, refer to section 41.1.1, Configuration of the ROM Area, and for the configuration of the memory area for the E2 DataFlash, refer to section 41.1.3, Configuration of the E2 DataFlash Area.

Table 41.1 Specifications of ROM/E2 DataFlash

Item		ROM	E2 DataFlash
Memory space		User area: Up to 512 Kbytes. User boot area: 16 Kbytes*1	Data area: 32 and 8 Kbytes
Read cycle		A read operation takes one cycle of ICLK	A read operation takes six cycles of FCLK in words or bytes
Programming/erasing method		• The chip incorporates a dedicated sequencer (FCU) for programming of the ROM/E2 DataFlash. • Programming and erasing the ROM/E2 DataFlash are handled by issuing commands to the FCU.	
Value after erasure		FFh	Undefined
BGO (background operation)		• The CPU is able to execute program code from the ROM while the E2 DataFlash memory is being programmed or erased.	
Suspension and resumption		• The CPU is able to execute program code from the ROM during suspension of programming or erasure. • The CPU is able to execute program code from the E2 DataFlash during suspension of programming or erasure. • Programming and erasure of the ROM/E2 DataFlash can be restarted (resumed) after suspension.	
Units of programming and erasure		• Units of programming for the user area or user boot area: 128 bytes • Units of erasure for the user area: In block units • Units of erasure for the user boot area: 16 Kbytes*1	• Unit of programming for the data area: 2 bytes • Unit of erasure for the data area: 32 bytes (1024 or 256 blocks)
On-board programming (four types)		Programming in boot mode • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. • The user boot area can also be programmed. Programming in USB boot mode*2 • USB0 is used. • Dedicated hardware is not required, so direct connection to a PC is possible. Programming in the user boot mode*1 • Able to create original boot programs of the user's making. Programming by a routine for ROM/E2 DataFlash programming within the user program • This allows ROM/E2 DataFlash programming without resetting the system.	
Off-board programming*1		A Flash programmer can be used to program the user area and user boot area.	A Flash programmer cannot be used to program the data area.
Protection	Software-controlled protection	The registers and lock bits can be set to prevent unintentional programming.	• The registers can be used to prevent unintentional programming or reading. • Protection with the registers is performed on a 2-Kbyte basis.
	FCU command-lock	When abnormal operations are detected during programming/erasure, this function disables any further programming/erasure.	

Note 1. Not present in 64- and 48-pin products.
Note 2. Not present in 112-, 100-, 64-, and 48-pin products.

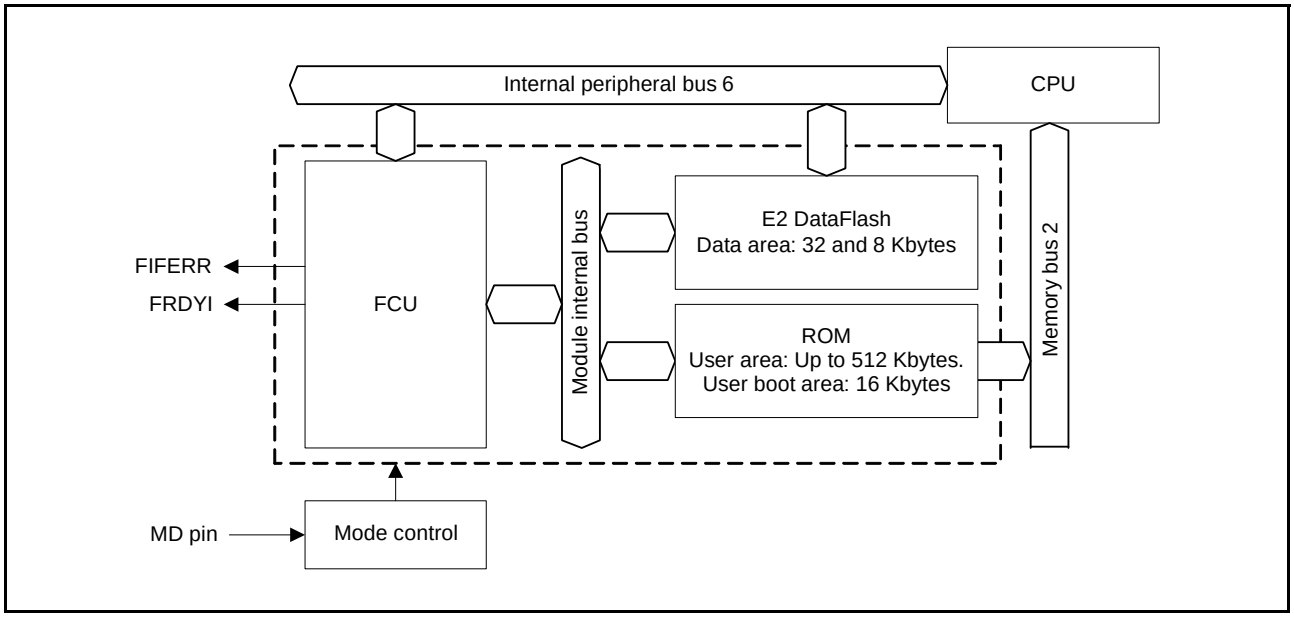


Figure 41.1 Block Diagram of ROM/E2 DataFlash

41.1.1 Configuration of the ROM Area

The ROM of products in this MCU is configured of a maximum 512-Kbyte user area and a 16-Kbyte user boot area. Figure 41.2 shows the address ranges of these areas.

Note that for the user area, the address range for reading differs from the address range for programming and erasure.

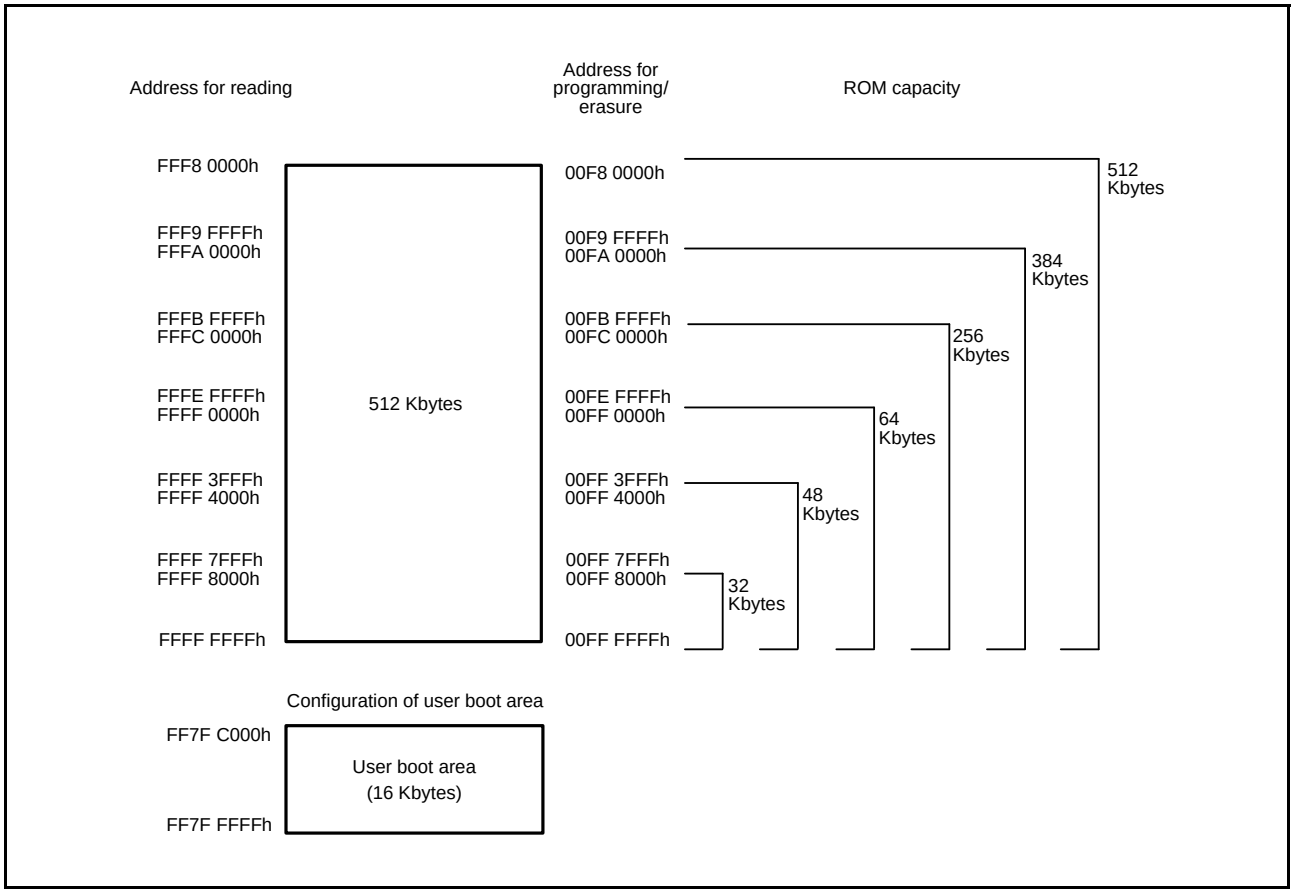


Figure 41.2 Memory Area Configuration of ROM

41.1.2 Block Configuration of the ROM

The user area is divided into blocks, as shown below, depending on the ROM capacity, and erasure proceeds in block units. The configuration of the blocks of the user area is shown in Figure 41.3, and the relations between blocks and addresses of the user area are listed in Table 41.2.

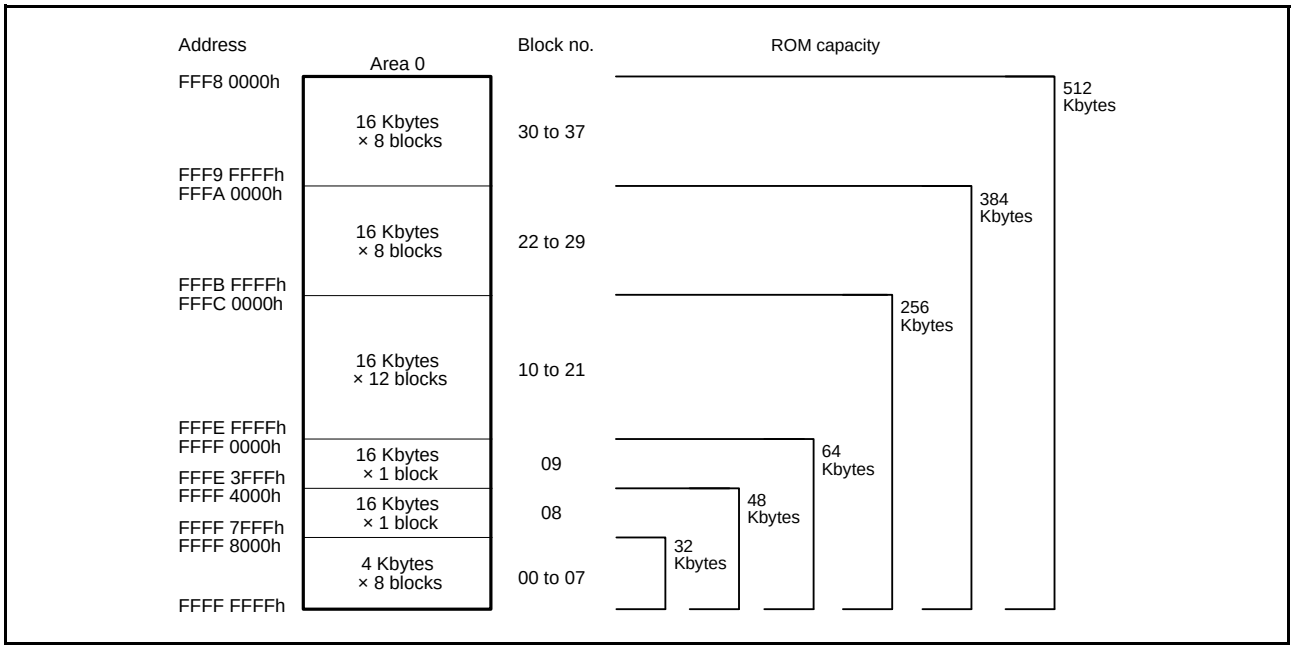


Figure 41.3 Block Configuration of the User Area

Table 41.2 Correspondence between Blocks and Addresses of the User Area

Block No.	Start Address	Block Configuration
37	FFF8 0000h	16 Kbyte x 8 blocks
36	FFF8 4000h	
35	FFF8 8000h	
34	FFF8 C000h	
33	FFF9 0000h	
32	FFF9 4000h	
31	FFF9 8000h	
30	FFF9 C000h	
29	FFFA 0000h	16 Kbyte x 8 blocks
28	FFFA 4000h	
27	FFFA 8000h	
26	FFFA C000h	
25	FFFB 0000h	
24	FFFB 4000h	
23	FFFB 8000h	
22	FFFB C000h	

Block No.	Start Address	Block Configuration
21	FFFC 0000h	16 Kbyte x 12 blocks
20	FFFC 4000h	
19	FFFC 8000h	
18	FFFC C000h	
17	FFFD 0000h	
16	FFFD 4000h	
15	FFFD 8000h	
14	FFFD C000h	
13	FFFE 0000h	
12	FFFE 4000h	
11	FFFE 8000h	
10	FFFE C000h	
9	FFFF 0000h	16 Kbyte x 1 block
8	FFFF 4000h	16 Kbyte x 1 block
7	FFFF 8000h	4 Kbyte x 8 blocks
6	FFFF 9000h	
5	FFFF A000h	
4	FFFF B000h	
3	FFFF C000h	
2	FFFF D000h	
1	FFFF E000h	
0	FFFF F000h	

41.1.3 Configuration of the E2 DataFlash Area

The E2 DataFlash memory of products in this MCU is configured as a 32-Kbyte data area whose addresses range from 0010 0000h to 0010 7FFFh.
Unlike the user area, the address ranges for reading from and programming and erasure of the data area are the same.

41.1.4 Block Configuration of the E2 DataFlash

The data area is divided into 1024 blocks, and erasure is executed in block units. The relations between blocks and addresses of the data area and the corresponding bits to support permission of reading and of programming and erasure are listed in Table 41.3.
The address of block N (address where block N starts) is calculated from the following formula.
Address of block N = (N x 32) + address where the data area starts (0010 0000h).

Table 41.3 Block Configuration of the Data Area

Block No.	Start Address	Reading and Programming/ Erasure Enable Bit
0000 ⋮ 0063	0010 0000h ⋮ 0010 07E0h	DFLRE0.DBRE00 DFLWE0.DBWE00
0064 ⋮ 0127	0010 0800h ⋮ 0010 0FE0h	DFLRE0.DBRE01 DFLWE0.DBWE01
0128 ⋮ 0191	0010 1000h ⋮ 0010 17E0h	DFLRE0.DBRE02 DFLWE0.DBWE02
0192 ⋮ 0255	0010 1800h ⋮ 0010 1FE0h	DFLRE0.DBRE03 DFLWE0.DBWE03
0256 ⋮ 0319	0010 2000h ⋮ 0010 27E0h	DFLRE0.DBRE04 DFLWE0.DBWE04
0320 ⋮ 0383	0010 2800h ⋮ 0010 2FE0h	DFLRE0.DBRE05 DFLWE0.DBWE05
0384 ⋮ 0447	0010 3000h ⋮ 0010 37E0h	DFLRE0.DBRE06 DFLWE0.DBWE06
0448 ⋮ 0511	0010 3800h ⋮ 0010 3FE0h	DFLRE0.DBRE07 DFLWE0.DBWE07
0512 ⋮ 0575	0010 4000h ⋮ 0010 47E0h	DFLRE1.DBRE08 DFLWE1.DBWE08
0576 ⋮ 0639	0010 4800h ⋮ 0010 4FE0h	DFLRE1.DBRE09 DFLWE1.DBWE09
0640 ⋮ 0703	0010 5000h ⋮ 0010 57E0h	DFLRE1.DBRE10 DFLWE1.DBWE10
0704 ⋮ 0767	0010 5800h ⋮ 0010 5FE0h	DFLRE1.DBRE11 DFLWE1.DBWE11
0768 ⋮ 0831	0010 6000h ⋮ 0010 67E0h	DFLRE1.DBRE12 DFLWE1.DBWE12
0832 ⋮ 0895	0010 6800h ⋮ 0010 6FE0h	DFLRE1.DBRE13 DFLWE1.DBWE13
0896 ⋮ 0959	0010 7000h ⋮ 0010 77E0h	DFLRE1.DBRE14 DFLWE1.DBWE14
0960 ⋮ 1023	0010 7800h ⋮ 0010 7FE0h	DFLRE1.DBRE15 DFLWE1.DBWE15

41.2 Register Descriptions

Some registers are common to the ROM and the E2 DataFlash, while others are dedicated to one or the other.

41.2.1 Flash P/E Protection Register (FWEPROR)

Address(es): 0008 C296h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	FLWE[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b1 to b0	FLWE[1:0]	Flash Programming/ Erasure	b1 b0 0 0: Disables programming and erasure of the ROM/E2 DataFlash, programming and erasure of lock bits, reading of lock bits, and blank checking 0 1: Enables programming and erasure of the ROM/E2 DataFlash, programming and erasure of lock bits, reading of lock bits, and blank checking 1 0: Disables programming and erasure of the ROM/E2 DataFlash, programming and erasure of lock bits, reading of lock bits, and blank checking 1 1: Disables programming and erasure of the ROM/E2 DataFlash, programming and erasure of lock bits, reading of lock bits, and blank checking	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Programming and erasure of the ROM or E2 DataFlash memory, programming and erasure of lock bits, reading of lock bits, and blank checking by software are prohibited.

FWEPROR is initialized by a reset due to the signal on the RES# pin, by transitions to software standby and deep software standby, and by the power supply voltage falling below the threshold for detection.

41.2.2 Flash Mode Register (FMODR)

Address(es): 007F C402h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	FRDMD	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	FRDMD	FCU Read Method Select	This bit selects internal processing by the FCU when a 0x71 command is issued. For details, see “FRDMD Bit (FCU Read Method Select)”.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Regarding the FMODR, when a 0x71 command is issued in relation to the FCU, this bit selects internal processing by the FCU. Internal processing by the FCU differs according to the address where the 0x71 command was issued.
This register is common to the ROM and the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 00h and writing is disabled.

FRDMD Bit (FCU Read Method Select)

Table 41.4 shows the relations between the status of the FRDMD bit and internal processing by the FCU when a 0x71 command is issued.

Table 41.4 Correspondence between the FRDMD Bit and 0x71 Command

Where the 0x71 Command is Issued	FRDMD Bit Status	Function	Internal Processing by the FCU
ROM	0	Lock bits are read using the memory area read method (lock bit read 1)	Transition to ROM lock bit read mode
	1	Lock bits are read using the register read method (lock bit read 2)	By going on to issue a 0xD0 command, the lock bit read 2 command is executed.
E2 DataFlash	0	Transition to E2 DataFlash lock bit read mode	The E2 DataFlash memory does not have lock bits. Accordingly, when the E2 DataFlash memory makes a transition to E2 DataFlash lock bit read mode, the values read from the E2 DataFlash area are undefined.
	1	Blank check command	By going on to issue a 0xD0 command, the blank check command is executed.

41.2.3 Flash Access Status Register (FASTAT)

Address(es): 007F C410h

	b7	b6	b5	b4	b3	b2	b1	b0
	ROMAE	—	—	CMDLK	DFLAE	—	DFLRPE	DFLWPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DFLWPE	E2 DataFlash Programming/Erasure Protection Violation Flag	0: No programming/erasure protection violation 1: Programming/erasure protection violation	R/(W) *1
b1	DFLRPE	E2 DataFlash Read Protection Violation Flag	0: No read protection violation 1: Read protection violation	R/(W) *1
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	DFLAE	E2 DataFlash Access Violation Flag	0: No E2 DataFlash access violation 1: E2 DataFlash access violation	R/(W) *1
b4	CMDLK	FCU Command Lock Flag	0: FCU accepts the command 1: FCU does not accept the command	R
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ROMAE	ROM Access Violation Flag	0: No ROM access violation 1: ROM access violation	R/(W) *1

Note 1. Only 0 can be written to clear the flag after reading 1.

This register is common to the ROM and the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 00h and writing is disabled.
When any bit from among the DFLWPE, DFLRPE, DFLAE, and ROMAE bits in FASTAT is set to 1, the FSTATR0.ILGLERR bit is set to 1, which places the FCU in the command-locked state.

DFLWPE Bit (E2 DataFlash Programming/Erasure Protection Violation)

This bit is used to indicate whether or not the programming/erasure protection set by DFLWEy (y = 0, 1) is violated. When the DFLWPE bit is set to 1, the FSTATR0.ILGLERR bit is set to 1, and the CMDLK bit become 1 (command-locked state).

[Setting condition]

- A programming/erasure command is issued for an E2 DataFlash area for which programming or erasure is disabled by DFLWEy (y = 0, 1).

[Clearing condition]

- When 0 is written after reading 1

DFLRPE Bit (E2 DataFlash Read Protection Violation Flag)

This bit is used to indicate whether or not the reading protection set by DFLREy (y = 0, 1) is violated.
When the DFLRPE bit is set to 1, the FSTATR0.ILGLERR bit is set to 1, and the CMDLK bit becomes 1 (command-locked state).

[Setting condition]

- An E2 DataFlash area for which reading is disabled by DFLREy (y=0, 1) is read out.

[Clearing condition]

- When 0 is written after reading 1

DFLAE Bit (E2 DataFlash Access Violation Flag)

This bit indicates whether an E2 DataFlash access violation occurred.
When the DFLAE bit is set to 1, the ILGLERR bit in FSTATR0 is set to 1, and the CMDLK bit becomes 1 (command-locked state).

[Setting conditions]

- An E2 DataFlash area is read in E2 DataFlash P/E normal mode and when the FENTRYD bit in FENTRYR is set to 1.
- An FCU command is issued for an E2 DataFlash area when the FENTRYD bit is set to 0.
- An FCU command is issued for an E2 DataFlash area when the FENTRYR.FENTRY0 bit is set to 1, or the area is read out.

[Clearing condition]

- When 0 is written after reading 1

CMDLK Bit (FCU Command Lock Flag)

This bit is used to indicate whether the FCU can receive commands.
When any bit of the FASTAT register is set to 1, the CMDLK bit is set to 1, and the FCU receives no commands (see section 41.6.2, Command-Locked State). To enable the FCU to receive commands, a status register clear command must be issued to the FCU after setting FASTAT to 10h.

[Setting condition]

- The FCU detects an error, and the CMDLK bit is set to 1 (command-locked state).

[Clearing condition]

- A status register clear command is issued while the FASTAT register is 10h.

ROMAE Bit (ROM Access Violation Flag)

This bit indicates whether a ROM access violation occurred.
When the ROMAE bit is set to 1, the FSTATR0.ILGLERR bit is set to 1, and the CMDLK bit becomes 1 (command-locked state).

[Setting conditions]

- A ROM programming/erasure address is read out when the FCU is in ROM P/E normal mode

ROM Capacity	ROM programming/erasure address ranges
	The FENTRY0 bit is 1
32 Kbytes	00FF 8000h to 00FF FFFFh
48 Kbytes	00FF 4000h to 00FF FFFFh
64 Kbytes	00FF 0000h to 00FF FFFFh
256 Kbytes	00FC 0000h to 00FF FFFFh
384 Kbytes	00FA 0000h to 00FF FFFFh
512 Kbytes	00F8 0000h to 00FF FFFFh

- An FCU command is issued for a ROM programming/erasure address or the address is read out

ROM Capacity	ROM programming/erasure address ranges
	The FENTRY0 bit is 0
32 Kbytes	00FF 8000h to 00FF FFFFh
48 Kbytes	00FF 4000h to 00FF FFFFh
64 Kbytes	00FF 0000h to 00FF FFFFh
256 Kbytes	00FC 0000h to 00FF FFFFh
384 Kbytes	00FA 0000h to 00FF FFFFh
512 Kbytes	00F8 0000h to 00FF FFFFh

- A ROM-reading address is read out while FENTRYR has placed the ROM in ROM P/E mode

ROM Capacity	ROM-reading address ranges
32 Kbytes	FFFF 8000h to FFFF FFFFh
48 Kbytes	FFFF 4000h to FFFF FFFFh
64 Kbytes	FFFF 0000h to FFFF FFFFh
256 Kbytes	FFFC 0000h to FFFF FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh
512 Kbytes	FFF8 0000h to FFFF FFFFh

[Clearing condition]

- When 0 is written after reading 1

41.2.4 Flash Access Error Interrupt Enable Register (FAEINT)

Address(es): 007F C411h

	b7	b6	b5	b4	b3	b2	b1	b0
	ROMAEIE	—	—	CMDLKIE	DFLAEIE	—	DFLRPEIE	DFLWPEIE
Value after reset:	1	0	0	1	1	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	DFLWPEIE	E2 DataFlash Programming/Erasure Protection Violation Interrupt Enable	This bit selects the generation or non-generation of an FIFERR interrupt in response to violations of protection against programming and erasure. 0: The interrupt is not generated. 1: The interrupt is generated.	R/W
b1	DFLRPEIE	E2 DataFlash Read Protection Violation Interrupt Enable	This bit selects the generation or non-generation of an FIFERR interrupt in response to violations of protection against reading. 0: The interrupt is not generated. 1: The interrupt is generated.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	DFLAEIE	E2 DataFlash Access Violation Interrupt Enable	This bit selects the generation or non-generation of an FIFERR interrupt in response to violations of access to the E2 DataFlash. 0: The interrupt is not generated. 1: The interrupt is generated.	R/W
b4	CMDLKIE	FCU Command Lock Interrupt Enable	This bit selects the generation or non-generation of an FIFERR interrupt when the FASTAT.CMDLK bit is set to 1 (command-locked state). 0: The interrupt is not generated. 1: The interrupt is generated.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ROMAEIE	ROM Access Violation Interrupt Enable	This bit selects the generation or non-generation of an FIFERR interrupt in response to violations of access to the ROM. 0: The interrupt is not generated. 1: The interrupt is generated.	R/W

This register is common to the ROM and the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 00h and writing is disabled.

DFLWPEIE Bit (E2 DataFlash Programming/Erasure Protection Violation Interrupt Enable)

This bit is used to enable or disable FIFERR interrupt requests when an E2 DataFlash programming/erasure protection violation occurs and the DFLWPE bit in FASTAT is set to 1.

DFLRPEIE Bit (E2 DataFlash Read Protection Violation Interrupt Enable)

This bit is used to enable or disable FIFERR interrupt requests when an E2 DataFlash read protection violation occurs and the DFLRPE bit in FASTAT is set to 1.

DFLAEIE Bit (E2 DataFlash Access Violation Interrupt Enable)

This bit is used to enable or disable FIFERR interrupt requests when an E2 DataFlash access violation occurs and the DFLAE bit in FASTAT is set to 1.

CMDLKIE Bit (FCU Command Lock Interrupt Enable)

This bit is used to enable or disable FIFERR interrupt requests when the FASTAT.CMDLK bit is set to 1 (command-locked state).

ROMAEIE Bit (ROM Access Violation Interrupt Enable)

This bit is used to enable or disable FIFERR interrupt requests when a ROM access violation occurs and the FASTAT.ROMAE bit is set to 1.

41.2.5 Flash Ready Interrupt Enable Register (FRDYIE)

Address(es): 007F C412h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FRDYIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRDYIE	Flash Ready Interrupt Enable	0: FRDYI interrupt requests disabled 1: FRDYI interrupt requests enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is common to the ROM and the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 00h and writing is disabled.

FRDYIE Bit (Flash Ready Interrupt Enable)

This bit is to enable or disable a flash ready interrupt request when programming/erasure is completed.
If the FRDYIE bit is set to 1, a flash ready interrupt request (FRDYI) is generated when execution of the FCU command has completed (FSTATR0.FRDY bit changes from 0 to 1).

41.2.6 E2 DataFlash Read Enable Register 0 (DFLRE0)

Address(es): 007F C440h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								DBRE07	DBRE06	DBRE05	DBRE04	DBRE03	DBRE02	DBRE01	DBRE00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBRE00	0000-0063 Block Read Enable	0: Read disabled 1: Read enabled	R/W
b1	DBRE01	0064-0127 Block Read Enable		R/W
b2	DBRE02	0128-0191 Block Read Enable		R/W
b3	DBRE03	0192-0255 Block Read Enable		R/W
b4	DBRE04	0256-0319 Block Read Enable		R/W
b5	DBRE05	0320-0383 Block Read Enable		R/W
b6	DBRE06	0384-0447 Block Read Enable		R/W
b7	DBRE07	0448-0511 Block Read Enable		R/W
b15 to b8	KEY[7:0]	Key Code	These bits control permission and prohibition of writing to the DFLRE0 register. To modify the DFLRE0 register, write 2Dh to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W) *1

Note 1. Write data is not retained.

DFLRE0 is a register to enable or disable the 0000 to 0511 blocks of the data area (see Table 41.3) to be read. Reading is enabled or disabled in 2 Kbytes (64 blocks).
This register is dedicated to the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 0000h and writing is disabled.

DBREj Bit (DBj Block Read Enable) (j = 00 to 07)

This bit is used to enable or disable the DB0000 to DB0511 blocks of the data area to be read.

41.2.7 E2 DataFlash Read Enable Register 1 (DFLRE1)

Address(es): 007F C442h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								DBRE15	DBRE14	DBRE13	DBRE12	DBRE11	DBRE10	DBRE09	DBRE08
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBRE08	0512-0575 Block Read Enable	0: Read disabled 1: Read enabled	R/W
b1	DBRE09	0576-0639 Block Read Enable		R/W
b2	DBRE10	0640-0703 Block Read Enable		R/W
b3	DBRE11	0704-0767 Block Read Enable		R/W
b4	DBRE12	0768-0831 Block Read Enable		R/W
b5	DBRE13	0832-0895 Block Read Enable		R/W
b6	DBRE14	0896-0959 Block Read Enable		R/W
b7	DBRE15	0960-1023 Block Read Enable		R/W
b15 to b8	KEY[7:0]	Key Code	These bits control permission and prohibition of writing to the DFLRE1 register. To modify the DFLRE1 register, write D2h to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W) *1

Note 1. Write data is not retained.

DFLRE1 is a register to enable or disable the 0512 to 1023 blocks of the data area (see Table 41.3) to be read. Reading is enabled or disabled in 2 Kbytes (64 blocks).
This register is dedicated to the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 0000h and writing is disabled.

DBREj Bit (Block Read Enable) (j = 08 to 15)

This bit is used to enable or disable the 0512 to 1023 blocks of the data area to be read.

41.2.8 E2 DataFlash P/E Enable Register 0 (DFLWE0)

Address(es): 007F C450h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								DBWE07	DBWE06	DBWE05	DBWE04	DBWE03	DBWE02	DBWE01	DBWE00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBWE00	0000-0063 Block Programming/ Erasure Enable	0: Programming/erasure disabled 1: Programming/erasure enabled	R/W
b1	DBWE01	0064-0127 Block Programming/ Erasure Enable		R/W
b2	DBWE02	0128-0191 Block Programming/ Erasure Enable		R/W
b3	DBWE03	0192-0255 Block Programming/ Erasure Enable		R/W
b4	DBWE04	0256-0319 Block Programming/ Erasure Enable		R/W
b5	DBWE05	0320-0383 Block Programming/ Erasure Enable		R/W
b6	DBWE06	0384-0447 Block Programming/ Erasure Enable		R/W
b7	DBWE07	0448-0511 Block Programming/ Erasure Enable		R/W
b15 to b8	KEY[7:0]	Key Code	These bits control permission and prohibition of writing to the DFLWE0 register. To modify the DFLWE0 register, write 1Eh to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W) *1

Note 1. Write data is not retained.

DFLWE0 is a register to enable or disable the 0000 to 0511 blocks of the data area (see Table 41.3) to be programmed or erased. Programming or erasing is enabled or disabled in 2 Kbytes (64 blocks).
This register is dedicated to the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 0000h and writing is disabled.

DBWEj Bit (Block Programming/Erasure Enable) (j = 00 to 07)

This bit is used to enable or disable the 0000 to 0511 blocks of the data area to be programmed or erased.

41.2.9 E2 DataFlash P/E Enable Register 1 (DFLWE1)

Address(es): 007F C452h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								DBWE15	DBWE14	DBWE13	DBWE12	DBWE11	DBWE10	DBWE09	DBWE08
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBWE08	0512-0575 Block Programming/ Erasure Enable	0: Programming/erasure disabled 1: Programming/erasure enabled	R/W
b1	DBWE09	0576-0639 Block Programming/ Erasure Enable		R/W
b2	DBWE10	0640-0703 Block Programming/ Erasure Enable		R/W
b3	DBWE11	0704-0767 Block Programming/ Erasure Enable		R/W
b4	DBWE12	0768-0831 Block Programming/ Erasure Enable		R/W
b5	DBWE13	0832-0895 Block Programming/ Erasure Enable		R/W
b6	DBWE14	0896-0959 Block Programming/ Erasure Enable		R/W
b7	DBWE15	0960-1023 Block Programming/ Erasure Enable		R/W
b15 to b8	KEY[7:0]	Key Code	These bits control permission and prohibition of writing to the DFLWE1 register. To modify the DFLWE1 register, write E1h to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W) *1

Note 1. Write data is not retained.

DFLWE1 is a register to enable or disable the 0512 to 1023 blocks of the data area (see Table 41.3) to be programmed or erased. Programming or erasing is enabled or disabled in 2 Kbytes (64 blocks).
This register is dedicated to the E2 DataFlash. When the on-chip ROM is disabled, the data read from this register is 0000h and writing is disabled.

DBWEj Bit (Block Programming/Erasure Enable) (j = 08 to 15)

This bit is used to enable or disable the 0512 to 1023 blocks of the data area to be programmed or erased.

41.2.10 Flash Status Register 0 (FSTATR0)

Address(es): 007F FFB0h

	b7	b6	b5	b4	b3	b2	b1	b0
	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PRGSPD	Programming Suspend Status Flag	0: Other than the status described below 1: During programming suspend processing or programming suspended	R
b1	ERSSPD	Erasure Suspend Status Flag	0: Other than the status described below 1: When erasure suspend processing or erasure suspended	R
b2	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b3	SUSRDY	Suspend Ready Flag	0: P/E suspend commands cannot be received 1: P/E suspend commands can be received	R
b4	PRGERR	Programming Error Flag	0: Programming terminates normally 1: An error occurs during programming	R
b5	ERSERR	Erasure Error	0: Erasure terminates normally 1: An error occurs during erasure	R
b6	ILGLERR	Illegal Command Error Flag	0: FCU detects no illegal command or illegal ROM/E2 DataFlash access 1: FCU detects an illegal command or illegal ROM/E2 DataFlash access	R
b7	FRDY	Flash Ready Flag	0: During programming/erasure, During suspending programming/erasure, During the lock bit read 2 command processing, During the peripheral clock notification command processing, During the blank check processing of E2 DataFlash. 1: Processing described above is not performed	R

FSTATR0 is also reset by setting the FRESETR.FRESET bit to 1.
When the on-chip ROM is disabled, the data read from this register is 00h and writing is disabled. This register is common to the ROM and the E2 DataFlash.

PRGSPD Bit (Programming Suspend Status Flag)

This bit is used to indicate that the FCU enters the programming suspend processing state or programming suspended state. For details, see section 41.5, Suspending Operation.

[Setting condition]

- The FCU has initiated a write suspend command.

[Clearing condition]

- The FCU has accepted a resume command.

ERSSPD Bit (Erasure Suspend Status Flag)

This bit is used to indicate that the FCU enters the erasure suspend processing state or erasure suspended state. For details, see section 41.5, Suspending Operation.

[Setting condition]

- The FCU has initiated an erasure suspend command.

[Clearing condition]

- The FCU has accepted a resume command.

SUSRDY Bit (Suspend Ready Flag)

This bit is used to indicate whether the FCU can receive a P/E suspend command.

[Setting condition]

- After starting programming/erasure process, the FCU enters a state in which P/E suspend commands can be received.

[Clearing conditions]

- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FASTAT.CMDLK bit becomes 1 (command-locked state).

PRGERR Bit (Programming Error Flag)

This bit is used to indicate the result of the ROM/E2 DataFlash programming process by the FCU.
When the PRGERR bit is set to 1, the FASTAT.CMDLK bit becomes 1 (command-locked state).

[Setting conditions]

- An error occurs during programming.
- A programming command is issued to areas protected by a lock bit.

[Clearing condition]

- After the FCU processes a status register clear command

ERSERR Bit (Erasure Error Flag)

This bit is used to indicate the result of the ROM/E2 DataFlash erasure process by the FCU.
When the ERSERR bit is set to 1, the FASTAT.CMDLK bit becomes 1 (command-locked state).

[Setting conditions]

- An error occurs during erasure.
- A block erase command is issued to areas protected by a lock bit.

[Clearing condition]

- After the FCU processes a status register clear command

ILGLERR Bit (Illegal Command Error Flag)

This bit is used to indicate that the FCU detects any illegal command or ROM/E2 DataFlash access.
When the ILGLERR bit is set to 1, the FASTAT.CMDLK bit becomes 1 (command-locked state).

[Setting conditions]

- The FCU detects an illegal command.
- The FCU detects an illegal ROM/E2 DataFlash access
  (one of the ROMAE, DFLAE, DFLRPE, and DFLWPE bits in FASTAT is 1).
- The setting of FENTRYR is invalid.

[Clearing condition]

- After a status register clear command has been issued under conditions where FASTAT is set to 10h

41.2.11 Flash Status Register 1 (FSTATR1)

Address(es): 007F FFB1h

	b7	b6	b5	b4	b3	b2	b1	b0
	FCUERR	—	—	FLOCKST	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b4	FLOCKST	Lock Bit Status	0: Protected 1: Not protected	R
b6, b5	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	FCUERR	FCU Error Flag	0: No error occurs in the FCU processing 1: An error occurs in the FCU processing	R

FSTATR1 is also reset by setting the FRESETR.FRESET bit to 1. When the on-chip ROM is disabled, the data read from this register is 00h and writing is disabled. This register is common to the ROM and the E2 DataFlash.

FLOCKST Bit (Lock Bit Status)

This bit is to reflect the read data of a lock bit when using the lock bit read 2 command.
When the FSTATR0.FRDY bit is set to 1 after a lock bit read 2 command is issued, the value of the lock bit status is stored in the FLOCKST bit. The value of the FLOCKST bit is retained until the completion of the next lock bit read 2 command.

FCUERR Bit (FCU Error Flag)

This bit is used to indicate that an error occurs in the FCU internal processing.
When the FCUERR bit is set to 1, set the FRESETR.FRESET bit to 1 to initialize the FCU.

41.2.12 Flash P/E Mode Entry Register (FENTRYR)

Address(es): 007F FFB2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FEKEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRY0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRY0	ROM P/E Mode Entry 0	0: ROM is in ROM read mode. 1: ROM is in ROM P/E mode.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	FENTRYD	E2 DataFlash P/E Mode Entry	0: E2 DataFlash is in read mode. 1: E2 DataFlash is in P/E mode.	R/W
b15 to b8	FEKEY[7:0]	Key Code	These bits control permission and prohibition of writing to the FENTRYR register. To modify the FENTRYR register, write AAh to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W) *1

Note 1. Write data is not retained.

To place the ROM/E2 DataFlash in ROM P/E mode so that the FCU can accept commands, the FENTRYD and FENTRY0 bits must be set to 1. Note that if a value is set other than AA01h and AA80h in FENTRYR, the FSTATR0.ILGLERR bit is set to 1 and the FSATAT.CMDLK bit is set to 1 (command-locked state).
When accessing the FENTRYR register to make a transition to ROM read mode, read the FENTRYR register after writing to it and check that the value has actually been set before reading the ROM.
FENTRYR is also reset when the FRESETR.FRESET bit is set to 1. When on-chip ROM is disabled, the data read from FENTRYR is 0000h and writing is disabled. This register is common to the ROM and the E2 DataFlash.

FENTRY0 Bit (ROM P/E Mode Entry FENTRY0)

This bit is used to place a ROM-reading address and programming/erasure address in P/E mode.

[Writing-enable conditions (when all of the following conditions are met)]

- On-chip ROM is enabled.
- The FSTATR0.FRDY bit is set to 1.
- AAh is written to the FEKEY[7:0] bits in word access.

[Setting condition]

- The writing-enable conditions are met, FENTRYR is set to 0000h, and 1 is written to the FENTRY0 bit.

[Clearing conditions]

- Data is written in byte access.
- Data is written in word access when the FEKEY[7:0] bits are other than AAh.
- When the writing-enable conditions are met, 0 is written to the FENTRY0 bit.
- When the writing-enable conditions are met and FENTRYR is other than 0000h, data is written to FENTRYR.

FENTRYD Bit (E2 DataFlash P/E Mode Entry)

The FENTRYD bit is used to place the E2 DataFlash in P/E mode.

[Writing-enable conditions (when all of the following conditions are met)]

- On-chip ROM is enabled.
- The FRDY bit in FSTATR0 is set to 1
- AAh is written to the FEKEY[7:0] bits in word access.

[Setting condition]

- When the writing-enable conditions are met, FENTRYR is set to 0000h, and 1 is written to the FENTRYD bit

[Clearing conditions]

- Data is written in byte access.
- Data is written in word access when the FEKEY[7:0] bits are other than AAh.
- When the writing-enable conditions are met, 0 is written to the FENTRYD bit.
- When the writing-enable conditions are met and FENTRYR is other than 0000h, data is written to FENTRYR.

41.2.13 Flash Protection Register (FPROTR)

Address(es): 007F FFB4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FPKEY[7:0]								—	—	—	—	—	—	—	FPROTCN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FPROTCN	Lock Bit Protection Cancel	0: Protection with a lock bit enabled 1: Protection with a lock bit disabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	FPKEY[7:0]	Key Code	These bits control permission and prohibition of writing to the FPROTR register. To modify the FPROTR register, write 55h to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W) *1

Note 1. Write data is not retained.

FPROTR is also reset when the FRESETR.FRESET bit is set to 1.
When on-chip ROM is disabled, the data read from FPROTR is 0000h and writing is disabled. This register is dedicated to the ROM.

FPROTCN Bit (Lock Bit Protection Cancel)

This bit is used to enable/disable the programming/erasure protection with a lock bit.

[Setting condition]

- 55h is written to the FPKEY[7:0] bits and 1 is written to the FPROTCN bit in word access when the value of FENTRYR is other than 0000h.

[Clearing conditions]

- Data is written in byte access.
- Data is written in word access when the FPKEY[7:0] bits are other than 55h.
- 55h is written to the FPKEY[7:0] bits and 0 is written to the FPROTCN bit in word access.
- The value of FENTRYR is 0000h.

41.2.14 Flash Reset Register (FRESETR)

Address(es): 007F FFB6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FRKEY[7:0]								—	—	—	—	—	—	—	FRESET
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRESET	Flash Reset	0: FCU is not reset 1: FCU is reset	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	FRKEY[7:0]	Key Code	These bits control permission and prohibition of writing to the FRESETR register. To modify the FRESETR register, write CCh to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W) *1

Note 1. Write data is not retained.

When on-chip ROM is disabled, the data read from FRESETR is 0000h and writing is disabled. This register is common to the ROM and the E2 DataFlash.

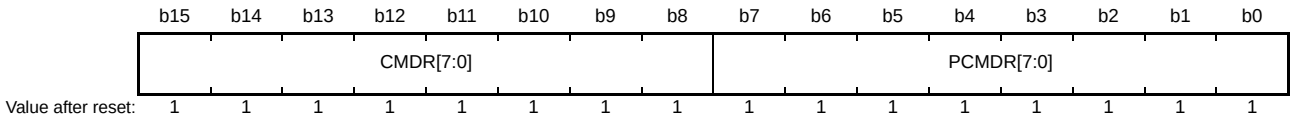
FRESET Bit (Flash Reset)

When the FRESET bit is set to 1, programming/erasure operations for the ROM/E2 DataFlash are forcibly terminated, and the FCU is initialized.

High voltage is applied to the memory of the ROM/E2 DataFlash during programming/erasure. To ensure the time required for dropping the voltage applied to the memory, keep the FRESET bit set to 1 for tFCUR (FCU reset time, see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions]) when initializing the FCU. While the FRESET bit is kept as 1, prohibit the ROM/E2 DataFlash from being read. Additionally, when the FRESET bit is set to 1, the FCU commands cannot be used because FENTRYR is initialized.

41.2.15 FCU Command Register (FCMDR)

Address(es): 007F FFBAh



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCMDR[7:0]	Precommand	Store the command immediately before the last command received by the FCU.	R
b15 to b8	CMDR[7:0]	Command	Store the last command received by the FCU.	R

FCMDR is also initialized when the FRESETR.FRESET bit is set to 1.

Table 41.5 lists the states of FCMDR after receiving each command.

When on-chip ROM is disabled, data read from FCMDR is 0000h and writing is disabled. This register is common to the ROM and the E2 DataFlash.

Table 41.5 States of FCMDR after Receiving Each Command

Command	CMDR[7:0]	PCMDR[7:0]
Normal mode transition	FFh	Previous command
Status read mode transition	70h	Previous command
Lock bit read mode transition (lock bit read 1)	71h	Previous command
Peripheral clock notification	E9h	Previous command
Programming	E8h	Previous command
Block erase	D0h	20h
P/E suspend	B0h	Previous command
P/E resume	D0h	Previous command
Status register clear	50h	Previous command
Lock bit read 2/blank check	D0h	71h
Lock bit programming	D0h	77h

41.2.16 FCU Processing Switching Register (FCPSR)

Address(es): 007F FFC8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ESUSPMD	Erasure Suspend Mode	0: Suspension priority mode 1: Erasure priority mode	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FCPSR is also reset when the FRESETR.FRESET bit is set to 1.
When on-chip ROM is disabled, the data read from FCPSR is 0000h and writing is disabled. This register is common to the ROM and the E2 DataFlash.

ESUSPMD Bit (Erasure Suspend Mode)

This bit is to select the erasure suspend mode for when a P/E suspend command is issued while the FCU executes the erasure processing for the ROM/E2 DataFlash. For details, see section 41.5, Suspending Operation.

41.2.17 E2 DataFlash Blank Check Control Register (DFLBCCNT)

Address(es): 007F FFCAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BCSIZE	—	—	—	—	BCADR[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b10 to b0	BCADR[10:0]	Blank Check Address Setting	Set the address of the area to be checked	R/W
b14 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	BCSIZE	Blank Check Size Setting	0: The size of the area to be blank checked is 2 bytes. 1: The size of the area to be blank checked is 2 Kbytes.	R/W

DFLBCCNT is also reset when the FRESETR.FRESET bit is set to 1.
When on-chip ROM is disabled, the data read from DFLBCCNT is 0000h and writing is disabled. This register is dedicated to the E2 DataFlash.

BCADR[10:0] Bits (Blank Check Address Setting)

These bits are used to set the address of the area to be checked when the size of the area to be checked by a blank check command is 2 bytes (the BCSIZE bit is 0). Set the BCADR[0] bit to 0.
When the BCSIZE bit is 0, the start address of the area to be checked is obtained by adding the DFLBCCNT setting value to the block start address (in 2-Kbyte units) specified at issuance of a blank check command.
When the BCSIZE bit is 1, the setting of the BCADR[10:0] bits will be ignored.

41.2.18 Flash P/E Status Register (FPESTAT)

Address(es): 007F FFCCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PEERRST[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PEERRST[7:0]	P/E Error Status	00h: No error 01h: Programming error against areas protected by a lock bit 02h: Programming error due to sources other than the lock bit protection 11h: Erasure error against areas protected by a lock bit 12h: Erasure error due to sources other than the lock bit protection (Values other than above are reserved)	R
b15 to b8	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

FPESTAT is also reset when the FRESETR.FRESET bit is set to 1.
When on-chip ROM is disabled, the data read from FPESTAT is 0000h and writing is disabled. This register is dedicated to the ROM.

PEERRST[7:0] Bits (P/E Error Status)

These bits are used to indicate the reason of an error that occurs during the programming/erasure processing for the ROM. The value of the PEERRST[7:0] bits is valid only when the FSTATR0.FRDY bit is set to 1 while the FSTATR0.ERSERR bit or FSTATR0.PRGERR bit is 1. The value of the reason of the past error is retained in the PEERRST[7:0] bits when the ERSERR bit and PRGERR bit is 0.

41.2.19 E2 DataFlash Blank Check Status Register (DFLBCSTAT)

Address(es): 007F FFCEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCST	Blank Check Status	0: The area to be blank-checked is erased (blank) 1: 0 or 1 is written in the area to be blank-checked	R
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DFLBCSTAT is also reset when the FRESETR.FRESET bit is set to 1.
When on-chip ROM is disabled, the data read from DFLBCSTAT is 0000h and writing is disabled. This register is dedicated to the E2 DataFlash.

41.2.20 Peripheral Clock Notification Register (PCKAR)

Address(es): 007F FFE8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PCKA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCKA[7:0]	Peripheral Clock Notification	These bits are used to set the FlashIF clock (FCLK) at the programming/erasure for the ROM/E2 DataFlash.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This setting is used to control the programming/erasure time.
PCKAR is also reset when the FRESETR.FRESET bit is set to 1.
When on-chip ROM is disabled, the data read from PCKAR is 0000h and writing is disabled. This register is common to the ROM and the E2 DataFlash.

PCKA[7:0] Bits (Peripheral Clock Notification)

These bits are used to set the FlashIF clock (FCLK) at the programming/erasure for the ROM/E2 DataFlash.
Set the FCLK frequency in the PCKA[7:0] bits and issue a peripheral clock notification command before programming/erasure. Do not change the frequency during programming/erasure for the ROM/E2 DataFlash.
Write a setting to the PCKA[7:0] bits as a binary value that selects the operating frequency in MHz units.
For example, when the operating frequency of the FlashIF clock is 35.9 MHz, the setting value is calculated as follows:

- Round 35.9 off to a whole number.
- Convert 36 to binary and set the upper bits and lower bits of the PCKA[7:0] bits to 00h and 24h (0010 0100b).

Note 1. When the PCKA[7:0] bits are set to values outside the range from 4 to 50 MHz, do not issue a programming command to the ROM/E2 DataFlash.
Note 2. When the PCKA[7:0] bits are set to a frequency that is different from the FCLK, the data of the ROM/E2 DataFlash may be damaged.
Note 3. Note that the programming time depends on the frequency to some extent even if the PCKA[7:0] bits are used.

41.3 Operating Modes Associated with Flash Memory

For information on the relationship between the setting of the level on the MD pin and the operating mode for this MCU, refer to section 3, Operating Modes [144-, 120-, 112- and 100-Pin Versions] or section 4, Operating Modes [64- and 48-Pin Versions].
The ROM and E2 DataFlash can be read, programmed, and erased on board in boot mode, USB boot mode, user boot mode, single-chip mode (with on-chip ROM enabled), or on-chip ROM enabled extended mode.
The area where programming and erasure are permitted, the area from which booting up proceeds, and areas erased at the time of booting up differ with the mode. The differences between modes are indicated in Table 41.6.

Table 41.6 Differences between Modes

Item	Boot Mode	USB Boot Mode	User Boot Mode	Single-Chip Mode (with On-Chip ROM Enabled) or On-chip ROM Enabled Extended Mode
Environment for programming and erasure	On-board programming			
Programmable and erasable area	User area/user boot area/data area	User area/data area	User area/data area	User area/data area
Division into erasure blocks	Possible*1	Possible*1	Possible	Possible
Boot program at a reset	Boot program	USB boot program	User boot program	User program

Note 1. The entire ROM may be erased at the time of booting up. Specified blocks can subsequently be erased. For details, refer to section 41.8.4, ID Code Protection (Boot Mode), section 41.8.2, State Transitions in Boot Mode, and section 41.9.2, State Transitions.

- Programming and erasure of the user boot area are only possible in boot mode.
- In boot mode, a host is able to program, erase, or read the user area, user boot area, or data area via an SCI.
- In boot mode, on-chip RAM is employed for the boot program. Therefore, the data on the on-chip RAM is not retained.
- Booting-up in USB boot mode and user boot mode is from the user boot area. The user boot area of the product as-shipped holds the USB boot program*1, which is capable of reading from or writing to the user area and data area. Furthermore, rewriting of the user boot area in boot mode can enable reading from or writing to the user area and data area via any desired interface.

Note 1. At the time of shipping, the user boot area holds a USB boot program even in the 112-pin and 100-pin products (without the USB function).

41.3.1 Erasure of Areas that are Subject to ID Code Protection

The areas to be erased depend on the operating mode at the time of booting up and the result of reference to the ID code. For a description of the ID code protection, refer to section 41.8.4, ID Code Protection (Boot Mode).

Table 41.7 Connection between areas for erasure, the operating mode, and ID code protection

Operating Mode at the Time of Booting Up	Control Code of ID Code Protection	Matching or non-matching ID codes	User Area	User Boot Area	Data Area
Boot mode	45h	Matching	—	—	—
		Non-matching three times consecutively	Erase	Erase*1	Erase
	52h	Matching or non-matching	—	—	—
	Other than 45h and 52h (ID code protection is disabled)	—	Erase	Erase*1	Erase
USB boot mode	ID code protection is not present in USB boot mode.		Erase		Erase
User boot mode	ID code protection depends on the user boot mode specification.				
Single-chip mode	Erasure does not proceed when booting up is in single-chip mode.				

Note 1. The user boot area is not erased if the user boot program is stored in the user boot area.

41.4 FCU

The ROM and E2 DataFlash operations are performed by issuing commands to a dedicated sequencer (FCU).
The mode transitions of the FCU and the system of commands are described below. The descriptions apply in common to boot mode, USB boot mode, user boot mode, single-chip mode (with on-chip ROM enabled), and on-chip ROM enabled extended mode.

41.4.1 FCU Modes

The FCU has five modes. Transitions between modes are caused by modifying FENTRYR or issuing FCU commands. Since the E2 DataFlash P/E mode is included in ROM read mode, high-speed reading from the ROM is possible in E2 DataFlash P/E mode. Figure 41.4 is a diagram of the FCU mode transitions.

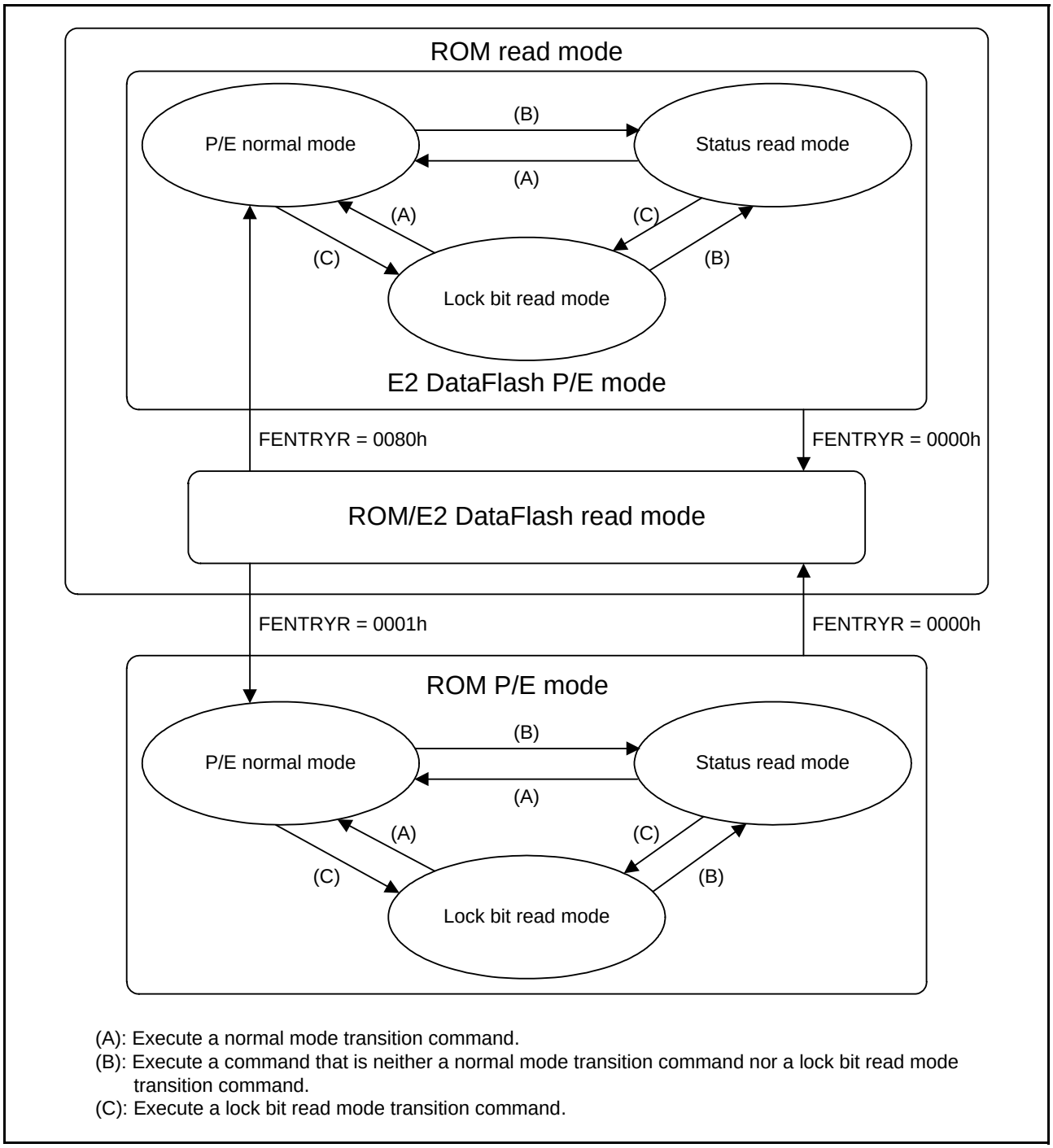


Figure 41.4 Mode Transitions of the FCU

41.4.1.1 ROM Read Modes

The ROM read modes are for high-speed reading of the ROM. Reading out from an address for reading can be accomplished in one cycle of ICLK.
ROM/E2 DataFlash read mode and E2 DataFlash P/E mode are the two kinds of ROM read modes.

41.4.1.2 ROM/E2 DataFlash Read Mode

This mode is for reading the ROM and E2 DataFlash memory. The FCU does not accept FCU commands. The FCU enters this mode when the FENTRYR.FENTRY0 bit is set to 0 with the FENTRYR.FENTRYD bit set to 0.

41.4.1.3 ROM P/E Modes

The ROM P/E modes are for programming and erasure of the ROM. High-speed reading of the ROM is not possible in these modes. Reading out from an address within the range for reading causes a ROM-access violation, and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).
There are three ROM P/E modes.

(1) ROM P/E Normal Mode

The transition to ROM P/E normal mode is the first transition in the process of programming or erasing the ROM. The FCU enters this mode when the FENTRYR.FENTRYD bit is set to 0, with the FENTRYR.FENTRY0 bit set to 1 in ROM read mode, or when the normal mode transition command is received in ROM P/E modes. Table 41.11 lists the acceptable commands in this mode.
Reading out from an address within the range for programming and erasure while the FENTRYR.FENTRY0 bit is set to 1 causes a ROM-access violation, and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).

(2) ROM Status Read Mode

In the ROM status read mode, the state of the ROM can be read. The FCU enters this mode when a status read mode transition command is received, or when a command other than the normal mode transition or lock bit read mode transition command is received in ROM P/E modes.
ROM status read mode encompasses the states where the FSTATR0.FRDY bit is 0 and the FASTAT.CMDLK bit is set to 1 (command-locked state) after an error has occurred. Table 41.11 lists the acceptable commands in this mode.
Reading out from an address within the range for programming and erasure while the FENTRYR.FENTRY0 bit is 1 allows the value of FSTATR0 to be read.

(3) ROM Lock-Bit Read Mode

In the ROM lock-bit read mode, reading the ROM allows the lock bits to be read. The FCU enters this mode when a lock-bit read mode transition command is received in ROM P/E modes. Table 41.11 lists the acceptable commands in this mode.
Reading out from an address within the range for programming and erasure while the FENTRYR.FENTRY0 bit is 1 allows the value of the lock bit of the block including the accessed address to be read from all the read bits.

41.4.1.4 E2 DataFlash P/E Modes

These modes are for programming and erasure of the E2 DataFlash memory. Although high-speed reading from the ROM is possible, reading from the E2 DataFlash is not executable. Although FCU commands for the E2 flash memory are accepted in this mode, FCU commands for the ROM are not. The FCU enters this mode when the FENTRYR.FENTRY0 bit is set to 0 and the FENTRYR.FENTRYD bit is set to 1.
There are three E2 DataFlash P/E modes.

(1) E2 DataFlash P/E Normal Mode

The transition to E2 DataFlash P/E normal mode is the first transition in the process of programming or erasing the E2 DataFlash.
The FCU enters this mode when the FENTRYR.FENTRYD bit is set to 1 and the FENTRYR.FENTRY0 bit is set to 0 in ROM/E2 DataFlash read mode, or when the normal mode transition command is received in E2 DataFlash P/E modes. Table 41.11 lists the acceptable commands in this mode.

(2) E2 DataFlash Status Read Mode

The E2 DataFlash status read mode is for reading information on the state of the E2 DataFlash.
The FCU enters this mode when a status read mode transition command is received, or when a command other than the normal mode transition and lock bit read mode transition command is received in E2 DataFlash P/E modes. E2 DataFlash status read mode encompasses the states where the FRDY bit in FSTATR0 is 0 and the FASTAT.CMDLK bit is set to 1 (command-locked state) after an error has occurred.Table 41.11 lists the acceptable commands in this mode. Reading out from an address within the E2 DataFlash area will actually read the value of the FSTATR0 register. High-speed reading of the ROM is possible.

(3) E2 DataFlash Lock-Bit Read Mode

Since the E2 DataFlash memory does not have lock bits, the lock bits are not read even if a transition to this mode is made. If the E2 DataFlash memory area is read after a transition to this mode, an E2 DataFlash access violation is not generated, but the values read are undefined. High-speed reading of the ROM is possible.
The FCU enters this mode when a lock-bit read mode transition command is received in E2 DataFlash P/E modes. Table 41.11 lists the acceptable commands in this mode.

41.4.2 FCU Commands

FCU commands consist of commands for mode transitions of the FCU and commands for programming and erasure. Table 41.8 lists the FCU commands for use with the ROM and E2 DataFlash.

Table 41.8 FCU Commands

Command	ROM	E2 DataFlash
P/E normal mode transition	Shifts to normal mode (see section 41.4.3, Connections between FCU Modes and Commands)	
Status read mode transition	Shifts to status read mode (see section 41.4.3, Connections between FCU Modes and Commands)	
Lock bit read mode transition (lock bit read 1)	Shifts to lock bit read mode (see section 41.4.3, Connections between FCU Modes and Commands)	
Peripheral clock notification	Sets the FlashIF clock (FCLK)	
Programming	ROM programming (in 128-byte units)	E2 DataFlash programming (in 2-byte units)
Block erase	ROM erasure (in block units, with the lock bit being erased simultaneously)	E2 DataFlash erasure (in block units)
P/E suspend	Suspends programming/erasure	
P/E resume	Resumes programming/erasure	
Status register clear	Clears the ILGLERR, ERSERR and PRGERR bits in FSTATR0 and the FASTAT.CMDLK bit (FCU command lock bit)	
Lock bit read 2	Reads the lock bit of a specified block (the value of the lock bit is reflected in the FSTATR1.FLOCKST bit)	—
Lock bit programming	Programs the lock bit of a specified block	—
Blank checking	—	Checks whether the E2 DataFlash memory is blank

The lock bit read 2 command is for the ROM also used as the blank check command for the E2 DataFlash memory. That is, when a lock bit read 2 command is issued for the E2 DataFlash, blank checking is executed for the E2 DataFlash memory.

Commands for the FCU are issued by writing an FCU command to addresses within the range for ROM programming and erasure or an address in the E2 DataFlash. Table 41.9 lists the formats of the FCU commands. Writing data to addresses listed in Table 41.9 in accordance with certain conditions causes the FCU to execute processing for the corresponding command. An explanation in summary of the FCU command format is given in Table 41.10. Furthermore, although almost all of the FCU commands are in byte units, some of the commands have to be issued in word units.

For details on the conditions for the acceptance of the individual FCU commands, see section 41.4.3, Connections between FCU Modes and Commands. For how to use the FCU commands, see section 41.4.4, FCU Command Usage.

Table 41.9 FCU Command Formats

Command	Number of Bus Cycles	Address / Data	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle	7th to 66th Cycles	67st Cycle
P/E normal mode transition	1	Address	RA	—	—	—	—	—	—	—
		Data	FFh	—	—	—	—	—	—	—
Status read mode transition	1	Address	RA	—	—	—	—	—	—	—
		Data	70h	—	—	—	—	—	—	—
Lock bit read mode transition (lock bit read 1)	1	Address	RA	—	—	—	—	—	—	—
		Data	71h	—	—	—	—	—	—	—
Peripheral clock notification	6	Address	RA	RA	RA	RA	RA	RA	—	—
		Data	E9h	03h	0F0Fh *1	0F0Fh *1	0F0Fh *1	D0h	—	—
Programming (ROM)	67	Address	RA	RA	WA	RA	RA	RA	RA	RA
		Data	E8h	40h	WDn *1	WDn *1	WDn *1	WDn *1	WDn *1	D0h
Programming (E2 DataFlash)	4	Address	RA	RA	WA	RA	—	—	—	—
		Data	E8h	01h	WDn *1	D0h	—	—	—	—
Block erase	2	Address	RA	BA	—	—	—	—	—	—
		Data	20h	D0h	—	—	—	—	—	—
P/E suspend	1	Address	RA	—	—	—	—	—	—	—
		Data	B0h	—	—	—	—	—	—	—
P/E resume	1	Address	RA	—	—	—	—	—	—	—
		Data	D0h	—	—	—	—	—	—	—
Status register clear	1	Address	RA	—	—	—	—	—	—	—
		Data	50h	—	—	—	—	—	—	—
Lock bit read 2 (ROM)	2	Address	RA	BA	—	—	—	—	—	—
		Data	71h	D0h	—	—	—	—	—	—
Blank checking (E2 DataFlash)	2	Address	RA	BA	—	—	—	—	—	—
		Data	71h	D0h	—	—	—	—	—	—
Lock bit programming (ROM)	2	Address	RA	BA	—	—	—	—	—	—
		Data	77h	D0h	—	—	—	—	—	—

Note 1. Write data in word units.

Table 41.10 FCU Commands

Item		ROM	E2 DataFlash
Address	RA	Any address for programming or erasure within the target ROM area*1	Any address within the E2 DataFlash
	WA	Programming-destination address in the range for programming or erasure (128-byte alignment)	Programming-destination address (2-byte alignment)
	BA	Any address for programming or erasure within the target erasure block	Any address within the target erasure block
Data	WDn	nth word of data for programming (n = 1 to 64)	nth word of data for programming (n = 1)
	Others	Command issued to the target address	

Note 1. Addresses that can be used for programming or erasure differ according to the ROM capacity and the settings of the FENTRYR register. For the ROM capacity, see section 41.1.1, Configuration of the ROM Area, and for FENTRYR, see section 41.2.12, Flash P/E Mode Entry Register (FENTRYR).

41.4.3 Connections between FCU Modes and Commands

The sets of FCU commands that can be accepted in each of the FCU modes are fixed. Furthermore, which commands are acceptable in a given FCU mode also depends on the state of the FCU.
Issuing of an FCU command must follow checking of the FCU's state after transitions of the FCU mode.
Commands that are acceptable in the various FCU modes and states are listed in Table 41.11. Issuing a command that is not currently acceptable leads to the FASTAT.CMDLK bit being set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).
Issuing of an FCU command must follow checking of the values of the FRDY, ILGLERR, ERSERR, and PRGERR bits in FSTATR0 and of the FSTATR1.FCUERR bit after transitions of the FCU mode. Furthermore, the FASTAT.CMDLK bit can be checked to see if an error has occurred. The value of the FASTAT.CMDLK bit is the logical OR of the ILGLERR, ERSERR, and PRGERR bits in FSTATR0 and the FSTATR1.FCUERR bit.

Table 41.11 Acceptable Commands and the State and Mode (ROM P/E Mode and E2 DataFlash P/E Mode) of the FCU

	P/E Normal Mode			Status Read Mode										Lock-Bit Read Mode		
	Programming Suspended	Erasure Suspended	Other State	Programming or Erasure	Programming while erasure is suspended	Processing to Suspend Programming or Erasure	Lock Bit Read 2 Processing (ROM)	Blank checking (E2 DataFlash Memory)	Programming Suspended	Erasure Suspended	Command-Locked State (FRDY = 0)	Command-Locked State (FRDY = 1)	Other State	Programming Suspended	Erasure Suspended	Other State
FSTATR0.FRDY bit	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**
FSTATR0.SUSRDY bit	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
FSTATR0.ERSSPD bit	**0**	**1**	**0**	**0**	**1**	**0/1**	**0/1**	**0/1**	**0**	**1**	**0/1**	**0/1**	**0**	**0**	**1**	**0**
FSTATR0.PRGSPD bit	**1**	**0**	**0**	**0**	**0**	**0/1**	**0/1**	**0/1**	**1**	**0**	**0/1**	**0/1**	**0**	**1**	**0**	**0**
FASTAT.CMDLK bit	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**
Normal mode transition	A	A	A	×	×	×	×	×	A	A	×	×	A	A	A	A
Status read transition	A	A	A	×	×	×	×	×	A	A	×	×	A	A	A	A
Lock-bit read transition (lock bit read 1)	A	A	A	×	×	×	×	×	A	A	×	×	A	A	A	A
Peripheral clock notification	×	×	A	×	×	×	×	×	×	×	×	×	A	×	×	A
Programming	×	*	A	×	×	×	×	×	×	*	×	×	A	×	*	A
Block erase	×	×	A	×	×	×	×	×	×	×	×	×	A	×	×	A
P/E suspend	×	×	×	A	×	×	×	×	×	×	×	×	×	×	×	×
P/E resume	A	A	×	×	×	×	×	×	A	A	×	×	×	A	A	×
Status register clear	A	A	A	×	×	×	×	×	A	A	A	A	A	A	A	A
Lock bit read 2 (ROM)	A	A	A	×	×	×	×	×	A	A	×	×	A	A	A	A
Lock bit programming (ROM)	×	*	A	×	×	×	×	×	×	*	×	×	A	×	*	A
Blank checking (E2 DataFlash)	A	A	A	×	×	×	×	×	A	A	×	×	A	A	A	A

A: Acceptable
*: Only programming is acceptable for blocks other than the block where erasure was suspended
×: Not acceptable

41.4.4 FCU Command Usage

The set of FCU commands consists of commands for FCU mode transitions, actually programming or erasing the ROM, error processing, and suspension and resumption. The following passages describe the various commands. For a description of the modes and states where the respective commands are acceptable, see section 41.4.3, Connections between FCU Modes and Commands.

41.4.4.1 Mode Transitions

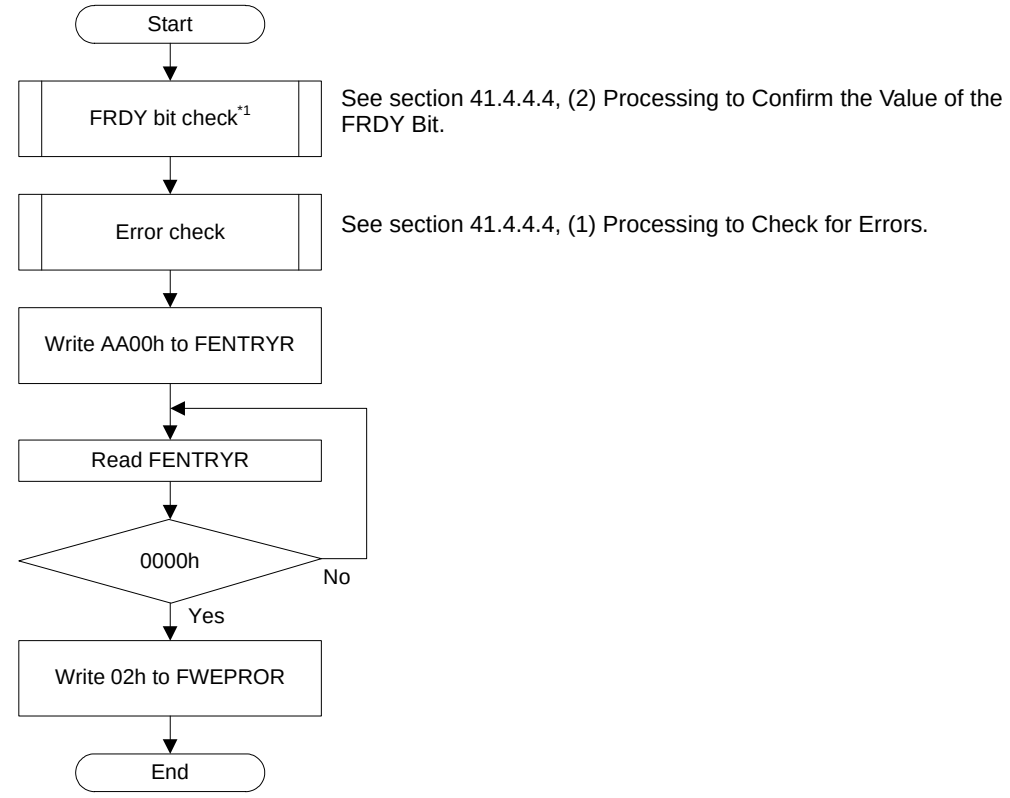
This subsection covers the commands for mode transitions. For an illustration of the various transitions between modes, see Figure 41.4.

(1) Switching to ROM Read Mode or ROM/E2 DataFlash Read Mode

High-speed reading of the ROM requires clearing of the FENTRYR.FENTRY0 bit to 0, which places the FCU in ROM read mode. Writing of 02h as a byte to FWEPROR is also required to disable programming and erasure (see section 41.2.1, Flash P/E Protection Register (FWEPROR)).

Before switching the FCU from ROM P/E mode to read mode, ensure that all processing of FCU commands has been completed and that the FCU has not detected an error.

For a transition to ROM/E2 DataFlash read mode, the FENTRYR.FENTRY0 and FENTRYD bits must be set to 0.



Note 1. tE16K: Erasure time for a 16-Kbyte block (see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions])

Figure 41.5 Procedure for Transition to ROM Read Mode or ROM/E2 DataFlash Read Mode

(2) Switching to P/E Mode

A transition to ROM P/E mode is required before executing an FCU command for programming or erasure of the ROM. Setting the FENTRYR.FENTRY0 bit to 1 causes a transition to ROM
P/E mode for programming and erasure of the corresponding address range.
A transition to E2 DataFlash P/E mode is required before executing an FCU command for programming or erasure of the E2 DataFlash. For a transition to E2 DataFlash P/E mode, set the FENTRYR.FENTRYD bit to 1.
Before actually proceeding to program or erase the ROM, enable programming and erasure by writing 01h as a byte to FWEPROR (see section 41.2.1, Flash P/E Protection Register (FWEPROR)).

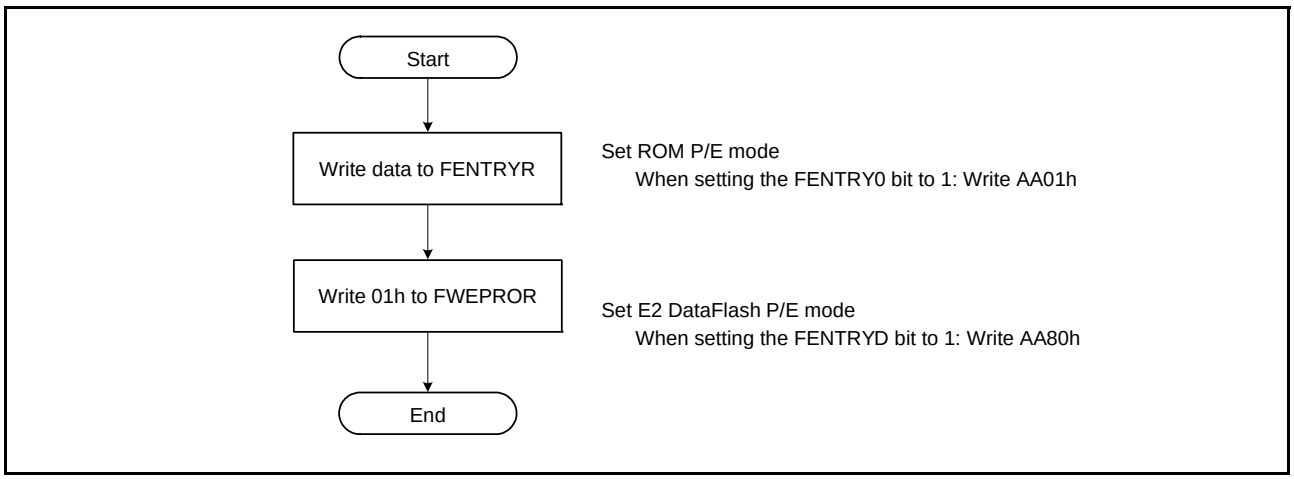


Figure 41.6 Procedure for Transition to ROM P/E Mode or E2 DataFlash P/E Mode

(3) Switching to P/E Normal Mode

Two methods are available for the transition to P/E normal mode: setting FENTRYR while the FCU is in ROM/E2 DataFlash read mode (see section 41.4.1, FCU Modes), or issuing the normal mode transition command while the FCU is in P/E mode (see Figure 41.7). The normal mode transition command is issued by writing FFh to a ROM programming/erasure address or to an E2 DataFlash address.

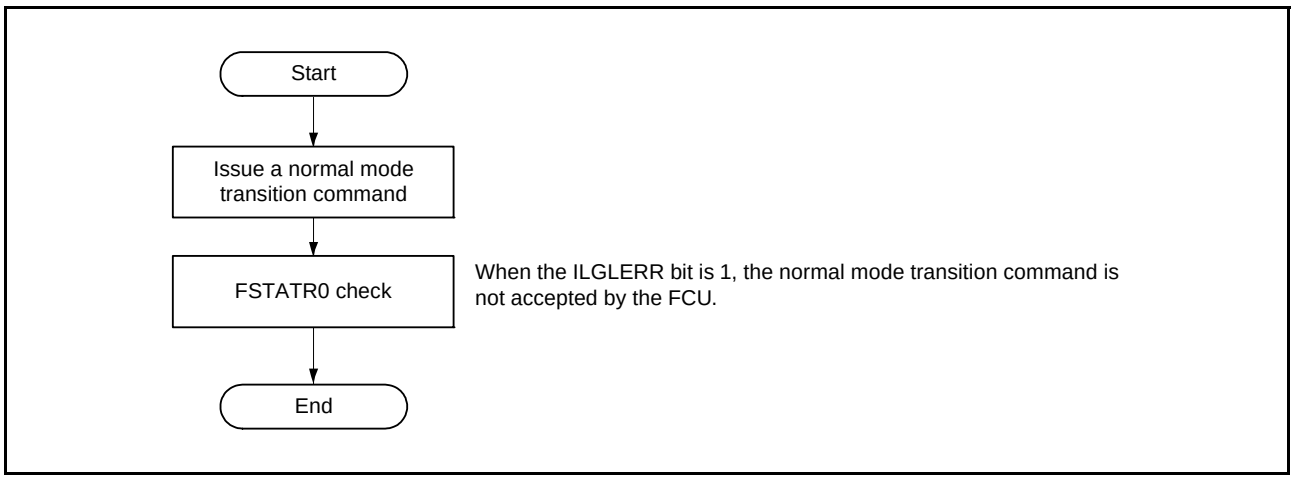


Figure 41.7 Procedure for Transition to ROM P/E Normal Mode

(4) Switching to Status Read Mode

Issuing a status read mode transition command or an FCU command other than a normal mode transition or lock bit read mode transition command places the FCU in status read mode. Figure 41.8 shows the procedure for checking FSTATR0 as an example. In the example, the status read mode transition command is issued to place the FCU in ROM status read mode, and the value of FSTATR0 is obtained by reading out from a ROM programming/erasure address or an E2 DataFlash address and then checked.

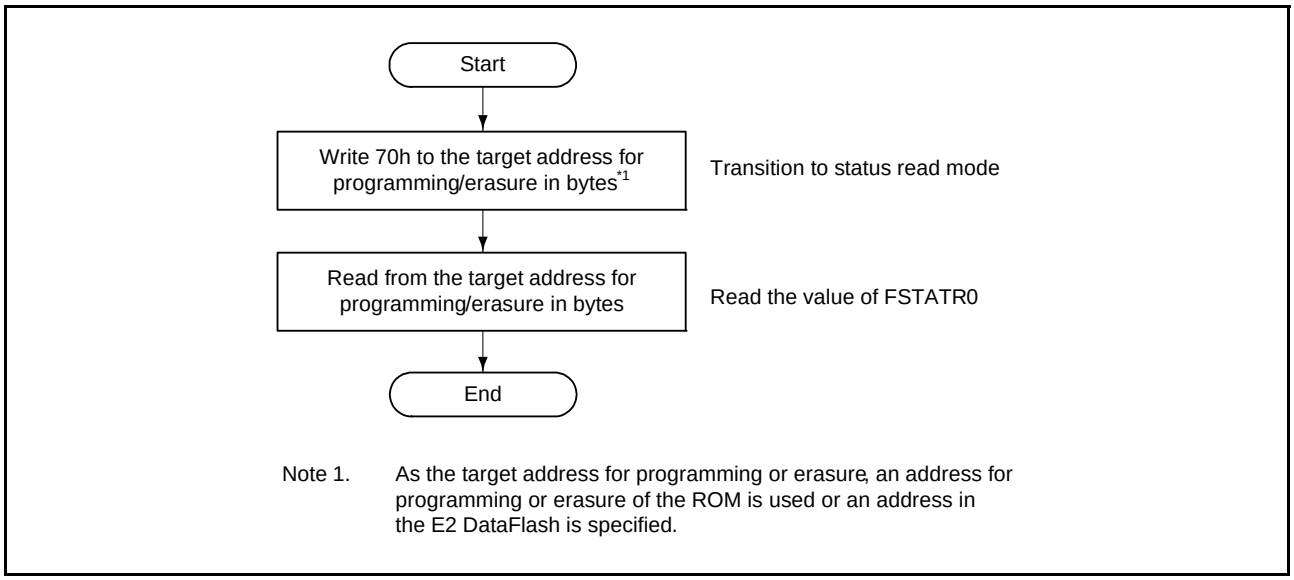


Figure 41.8 Procedure for Transition to ROM Status Read Mode and the Status Checking

(5) Switching to ROM Lock-Bit Read Mode

Clearing the FMODR.FRDMD bit (memory area reading method) issues a lock bit read mode transition (lock bit read 1) command. After the transition to lock bit read mode, the lock bit value is obtained by reading out from a ROM programming/erasure address. All bits of a value thus read have the value of the lock bit of the block that contains the accessed address (Figure 41.9).

Since there are no lock bits for the E2 DataFlash, undefined data are read from the E2 DataFlash area after a transition of the lock bit read mode is made.

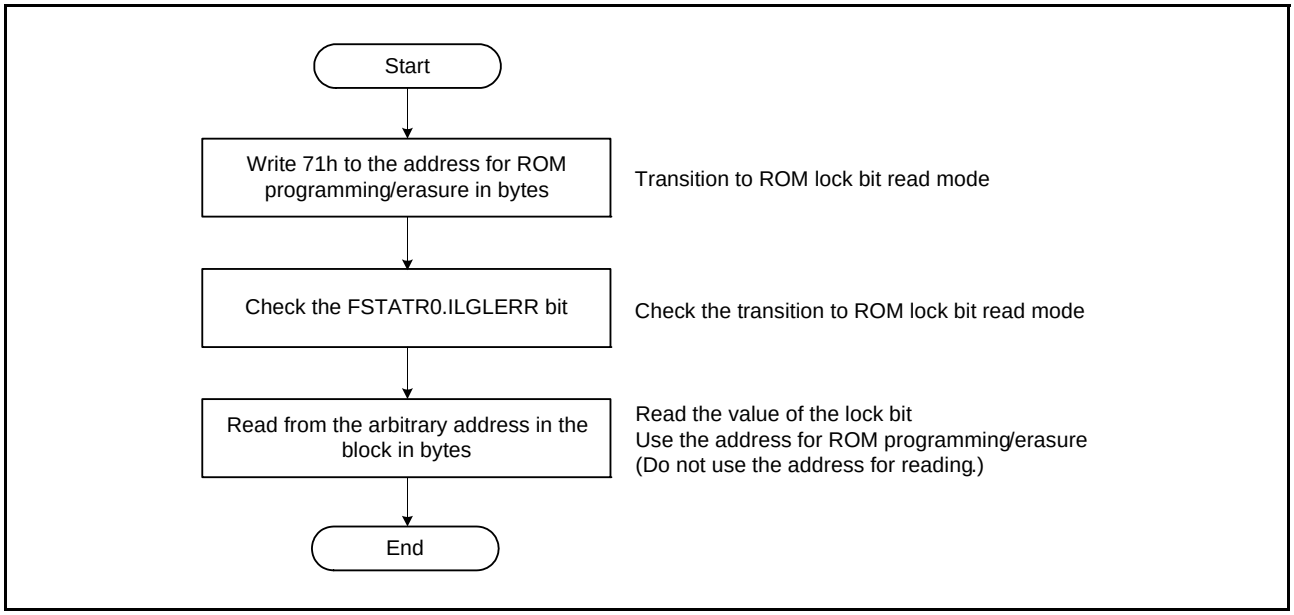
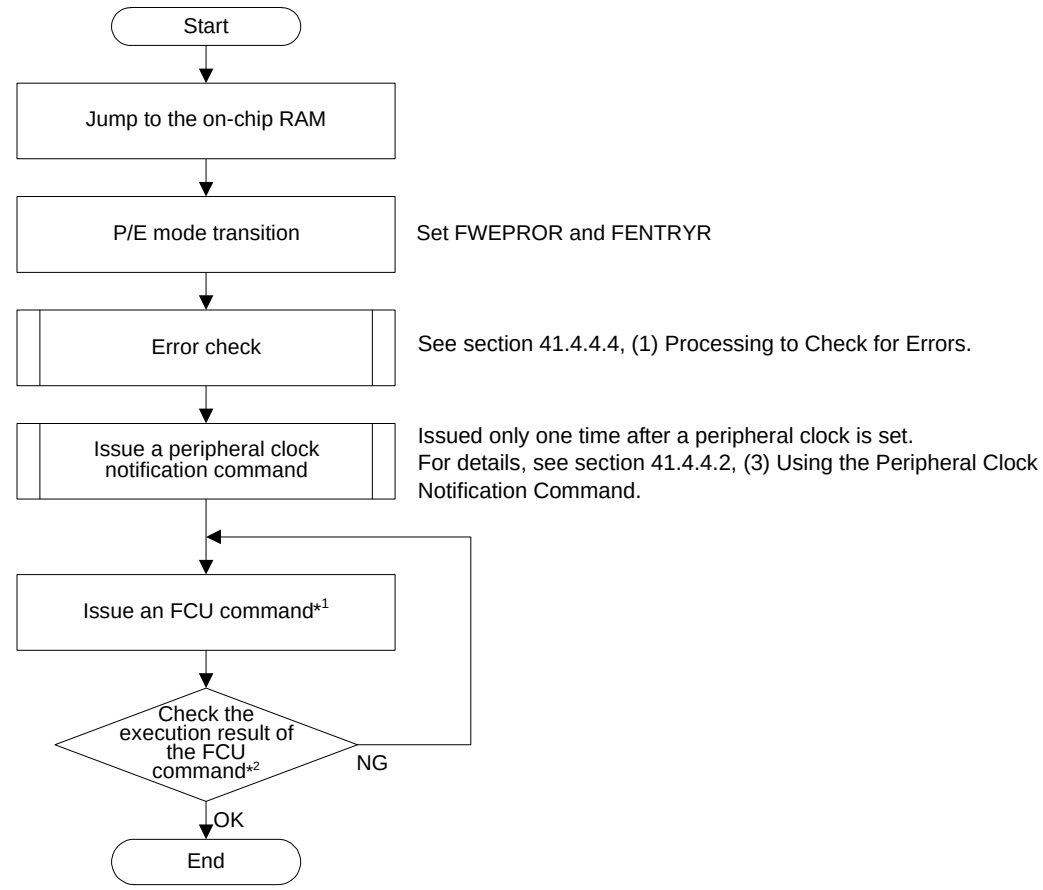


Figure 41.9 Procedure for Transition to ROM Lock-Bit Read Mode and Lock-Bit Reading

41.4.4.2 Programming and Erasure Procedures

The following passages describe the flow of procedures for programming or erasing the ROM or E2 DataFlash. For details on the acceptance of commands by the FCU, see section 41.4.3, Connections between FCU Modes and Commands.
Figure 41.10 is a simple flowchart of the procedure for executing FCU commands.



Note 1. Selected among the programming, block erase, lock bit programming, and lock bit read 2 commands.
Note 2. To check the result of programming/erasure processing, enter ROM read mode or ROM/E2 DataFlash read mode and read data. (see section 41.4.4.1, (1) Switching to ROM Read Mode or ROM/E2 DataFlash Read Mode).

Figure 41.10 Simple Flowchart of the Procedure for Programming and Erasure

(1) Jumping to Locations in On-chip RAM

Since fetching instructions from the ROM is not possible while the ROM is being programmed or erased, instructions have to be fetched from an area other than the ROM. Copy the required program code to on-chip RAM and then make a jump to the address where the code starts in on-chip RAM.

(2) Transition to P/E Mode

The FCU is placed in P/E mode by setting the FENTRYR.FENTRY0 and FENTRYD bits and the FWEPROR register. For details, see section 41.4.4.1, (2) Switching to P/E Mode.

(3) Using the Peripheral Clock Notification Command

The FlashIF clock (FCLK) is used in programming and erasing the ROM or E2 DataFlash, so the frequency of this clock has to be set in PCKAR. Frequencies in the range from 1 to 100 MHz are selectable. If a frequency within this range has not been set, the FCU will detect the error leading the FASTAT.CMDLK bit being set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).

Note that if the PCKA[7:0] bits in the PCKAR register are set to values outside the range from 4 MHz to 50 MHz, do not issue a programming command to the ROM/E2 DataFlash.

The peripheral clock notification command is used after the PCKAR setting has been made. In the first and second cycles for the peripheral clock notification command, respectively, the values E9h and 03h are written to the address range for programming and erasure of the ROM or the address range in the E2 DataFlash. Write 0F0Fh to the address range for programming and erasure of the ROM or the address range in the E2 DataFlash three times in the third to fifth cycles of the command. After 0F0Fh has been written three times (as a word) to the address range for programming and erasure of the ROM or the address range in the E2 DataFlash, the process of the FCU setting the frequency of the peripheral clock starts once the value D0h has been written in the sixth cycle. The FSTATR0.FRDY bit can be used to check whether or not the settings have been completed.

In the case of the ROM, addresses that can be used in the first to sixth cycles differ according to the setting of the FENTRYR.FENTRY0 bit. Ensure that the addresses suit the setting of the FENTRYR.FENTRY0 bit. If issuing of the command is attempted for an address in the area for which P/E mode is disabled by the FENTRYR register, the FCU will detect the error and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).

Furthermore, if the setting for the peripheral clock in use will not be changed from this setting after release from the reset state, the setting by the peripheral clock notification command is also valid for the next FCU command.

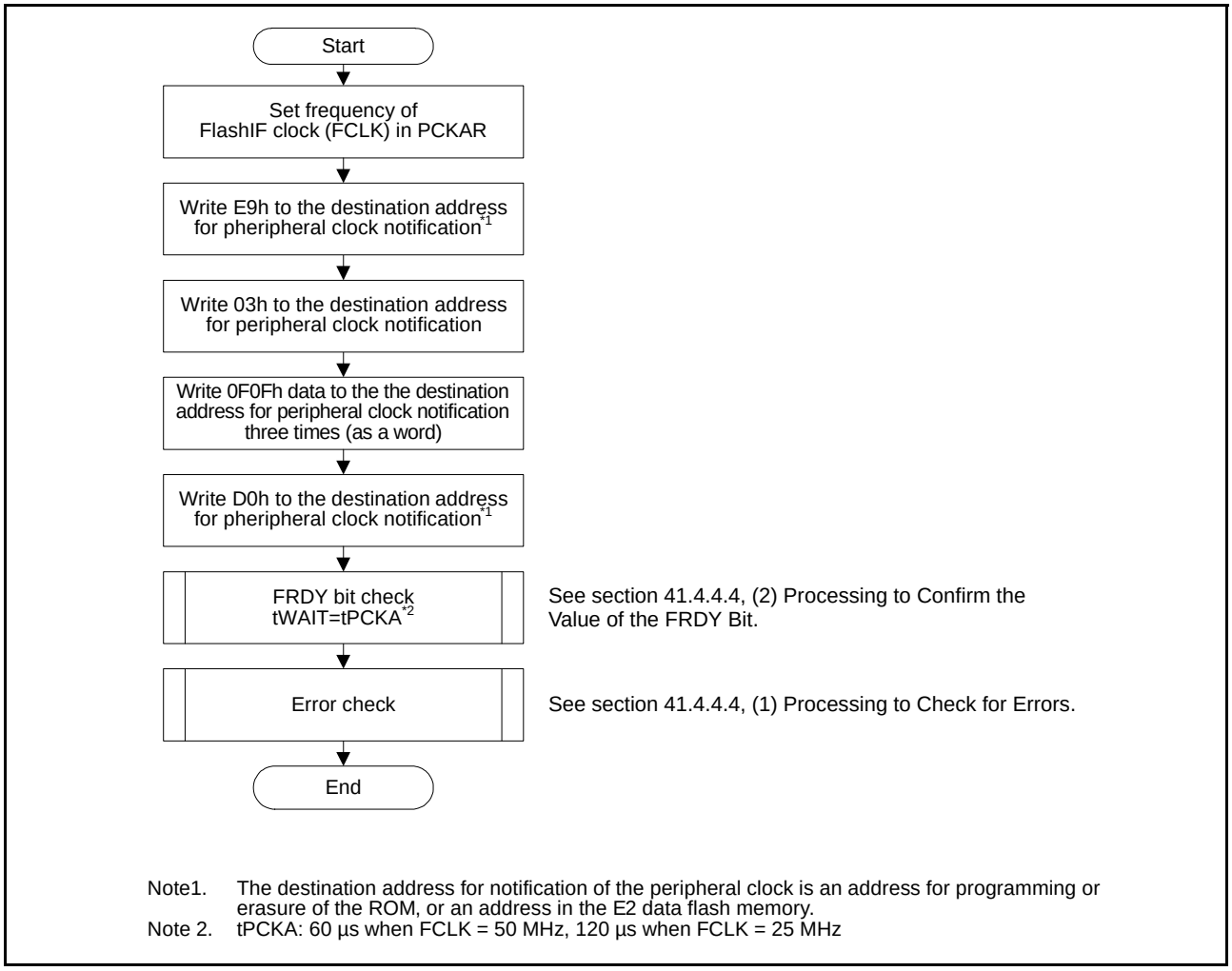


Figure 41.11 Using the Peripheral Clock Notification Command

(4) Programming

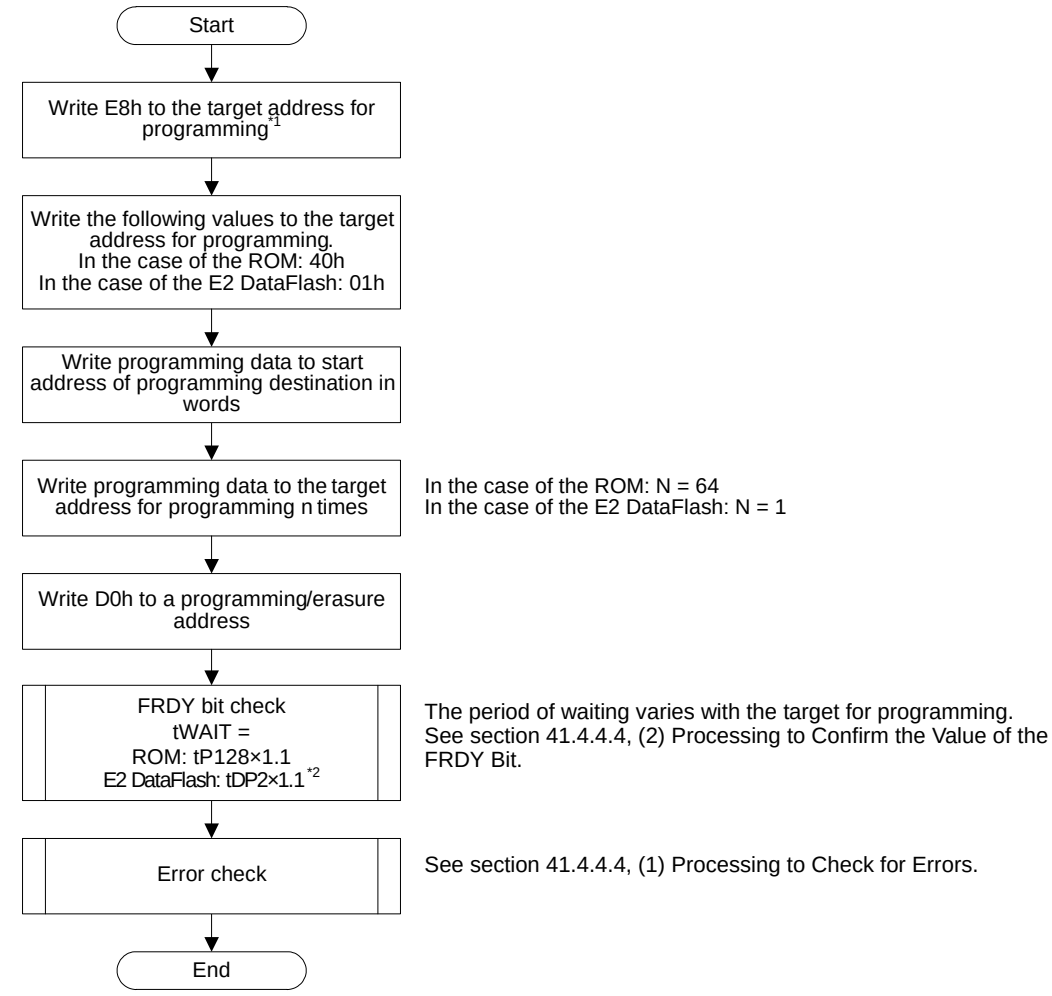
The programming command is used to write data to the ROM or the E2 DataFlash.

- ROM Programming

In the first and second cycles for the programming command, respectively, the values E8h and 40h are written to the address range for programming and erasure of the ROM. In the third cycle, write the actual data to be programmed, as a word unit, to the start address of the target area for programming. For this start address, always use an address that is aligned on a 128-byte boundary. In the fourth to the 66th cycles, write the data for programming in 63 word-unit rounds to the address range for programming and erasure of the ROM. Once the value D0h has been written to the address range for programming and erasure of the ROM in the 67th cycle, the FCU begins the actual process of programming the ROM. The FSTATR0.FRDY bit can be used to check whether or not the programming has been completed.
Addresses that can be used in the first to 67th cycles differ according to the setting of the FENTRYR.FENTRY0 bit. Ensure that the addresses suit the setting of the FENTRYR.FENTRY0 bit. If issuing of the command is attempted for an address in the area for which P/E mode is disabled by the FENTRYR register, the FCU will detect the error leading the FASTAT.CMDLK bit being set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).
In cases where the target range in the third to 66th cycles includes addresses that do not require programming, use FFFFh as the data for programming to those addresses. Furthermore, when a lock is programmed so that protection by the lock bit becomes effective, the FPROTR.FPROTCN bit must be set to 1.

- E2 DataFlash Programming

Write E8h to an address within the E2 DataFlash area in the first cycle of the programming command, and 01h in the second cycle. In the third cycle, write the first word of data for programming to the address where the target area for programming starts. This address must be on a 2-byte boundary.
After writing words to addresses in the E2 DataFlash area one time, write byte D0h to an address within the E2 DataFlash area in the fourth cycle; the FCU will then start actual programming of the E2 DataFlash. Read the FRDY bit in FSTATR0 to confirm the completion of E2 DataFlash programming.
When programming for locking to prohibit programming and erasure according to the setting of the DFLWEy (y = 0, 1) register proceeds, the relevant bit of the DFLWEy (y = 0, 1) register must be set to 1.



Note 1. The target address for programming is an address for programming or erasure of the ROM, or an address in the E2 DataFlash.
Note 2. tP128: Time required for programming 128-byte data
tDP2: Time required for programming 2-byte data
(see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions])

Figure 41.12 Procedure for ROM/E2 DataFlash Programming

(5) Erasure

To erase the ROM/E2 DataFlash, use the block erasure command.
In the first cycle of a block-erasure command, 20h is written to an address for programming or erasure of the ROM or an address in the E2 DataFlash. In the second cycle, when D0h is written to any address within the target block for erasure, the FCU starts processing to erase the ROM or E2 DataFlash. The FSTATR0.FRDY bit can be checked to confirm the completion of erasure. When the CPU reads ROM that has been erased, the value read is FFFF FFFFh. In the case of the E2 DataFlash, values read are undefined. In the case of the ROM, the FPROTR.FPROTCN bit must be set to 1 if protection by the lock bit is in effect for a block to be erased.
Note that the E2 DataFlash has a programming and erasure protection function that is controlled by DFLWEy (y = 0, 1). When erasure for locking to prohibit programming and erasure according to the setting of the DFLWEy (y = 0, 1) register proceeds, the relevant bit of the DFLWEy (y = 0, 1) register must be set to 1.

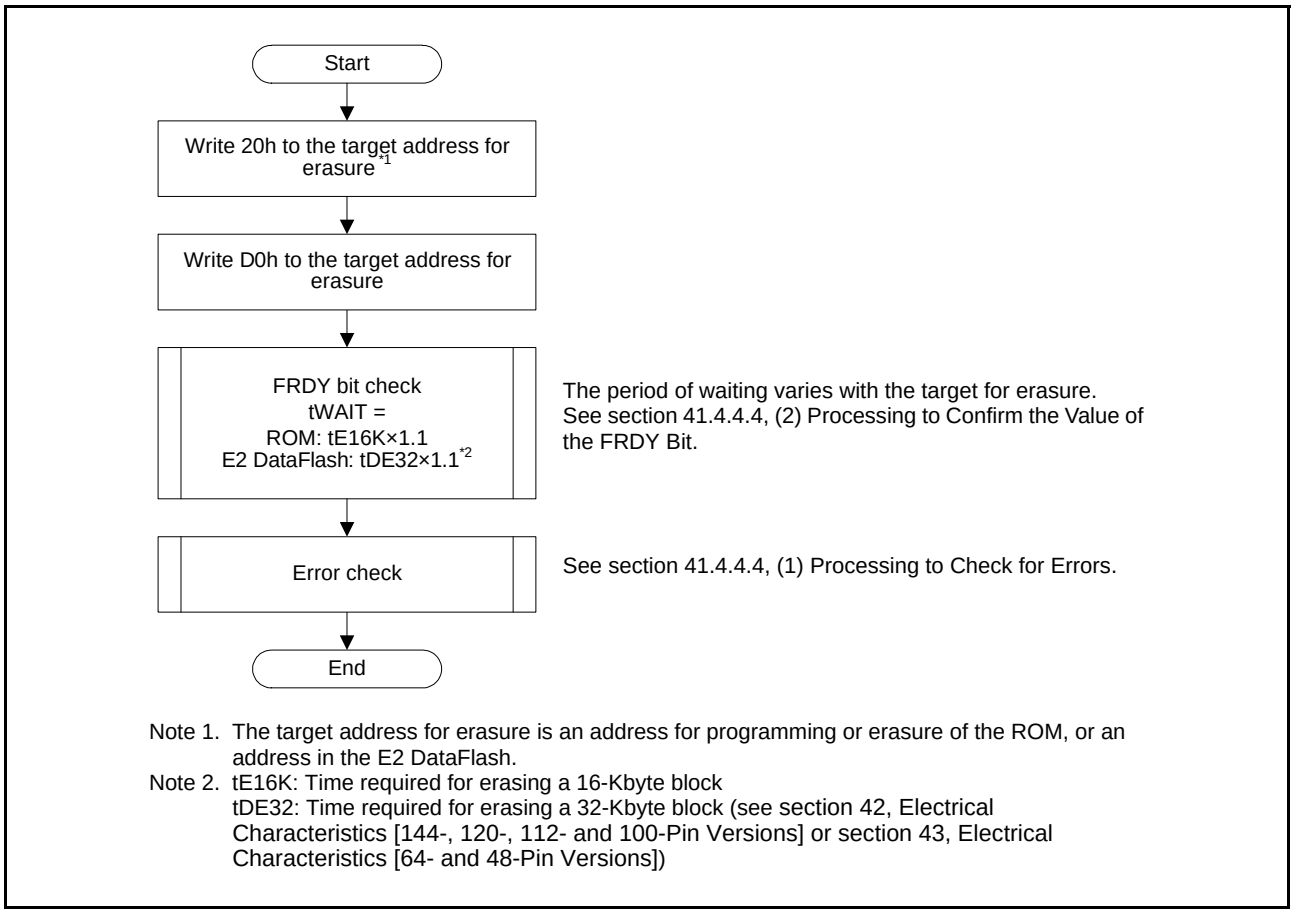
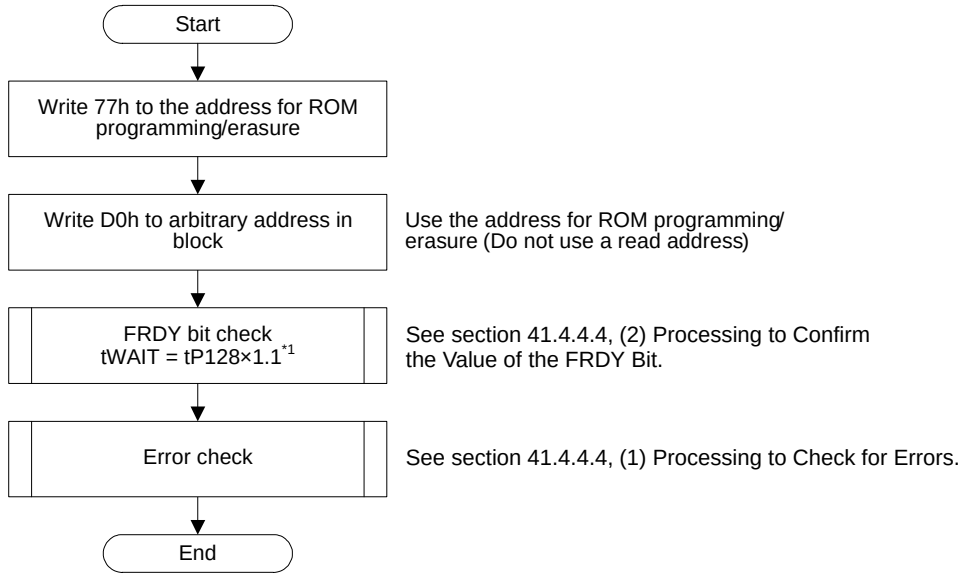


Figure 41.13 Procedure for ROM/E2 DataFlash Erasure

(6) Programming or Erasing Lock Bits

Lock-bit programming can only be executed on the ROM. Each block in the user area includes a lock bit. To write to a lock bit, use the lock bit programming command. In the first cycle of the lock bit programming command, 77h is written to the ROM programming/erasure address. When D0h is written to an arbitrary address in a block whose lock bit is to be written to in the second cycle, the FCU starts the processing to write to the lock bit. Whether writing is completed can be checked with the FSTATR0.FRDY bit.



Note 1. tP128: Time required for programming 128-byte data (see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions])

Figure 41.14 Procedure for Programming the Lock Bit

The block erase command is used to erase lock bits.
When the FPROTR.FPROTCN bit is 0, erasure blocks whose lock bit is set to 0 cannot be erased. When erasing a lock bit, issue a block erase command with the FPROTCN bit set to 1. Using the block erase command erases all data in the block. It is impossible to erase only a lock bit.

(7) Reading Lock Bits

Lock-bit reading can only be executed on the ROM. Lock bits can be read by either reading from a memory area or reading from a register.

The lock bit read 2 command is issued in the case of the register reading method (i.e. when the FMODR.FRDMD bit is set to 1). This command is issued to an address within the block for which the lock bit is to be read; the address range is that for programming and erasing the ROM. In the first and second cycles of the lock bit read 2 command, the values 71h and D0h are written; once these values have been written, the value of the lock bit for the specified block is copied to the FSTATR1.FLOCKST bit.

In the case of the memory area reading method (i.e. when the FMODR.FRDMD bit is 0), the FCU is placed in ROM lock-bit read mode, and the lock bit is obtained by reading from an address within the address range for programming and erasure of the ROM. For details, see Figure 41.9, Procedure for Transition to ROM Lock-Bit Read Mode and Lock-Bit Reading.

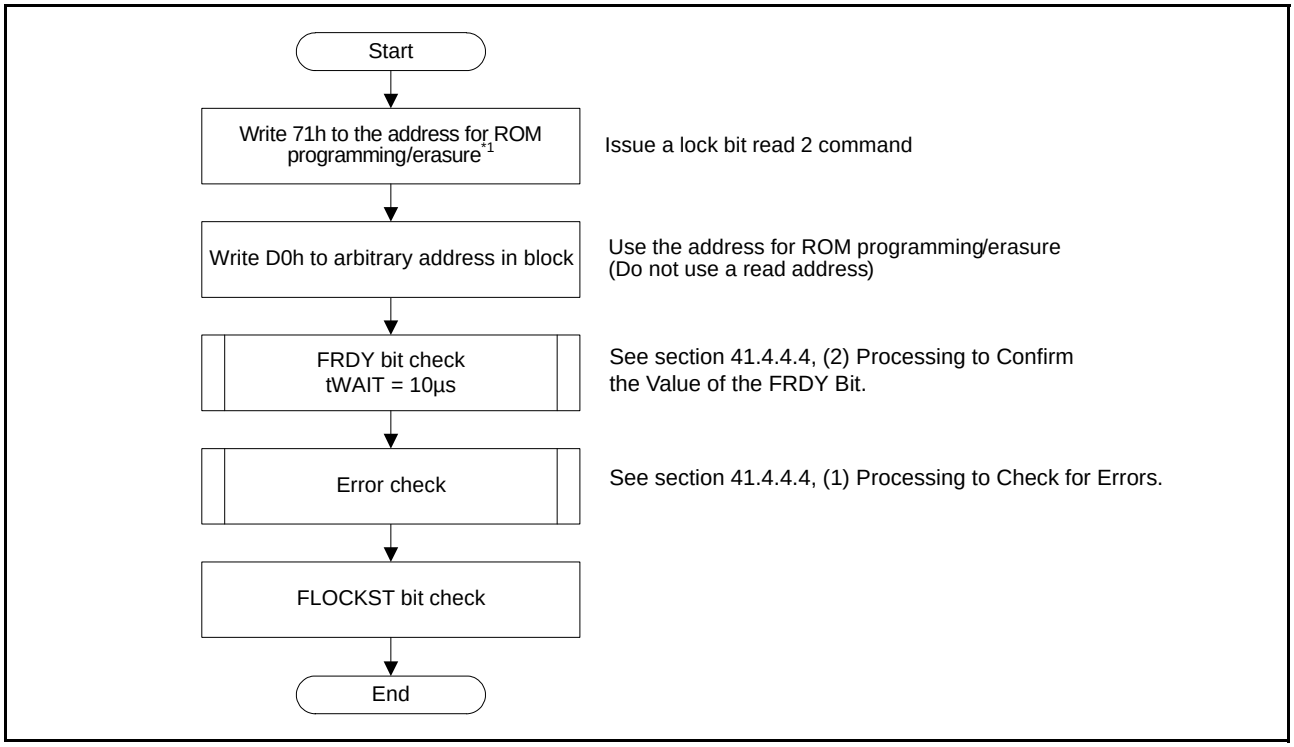
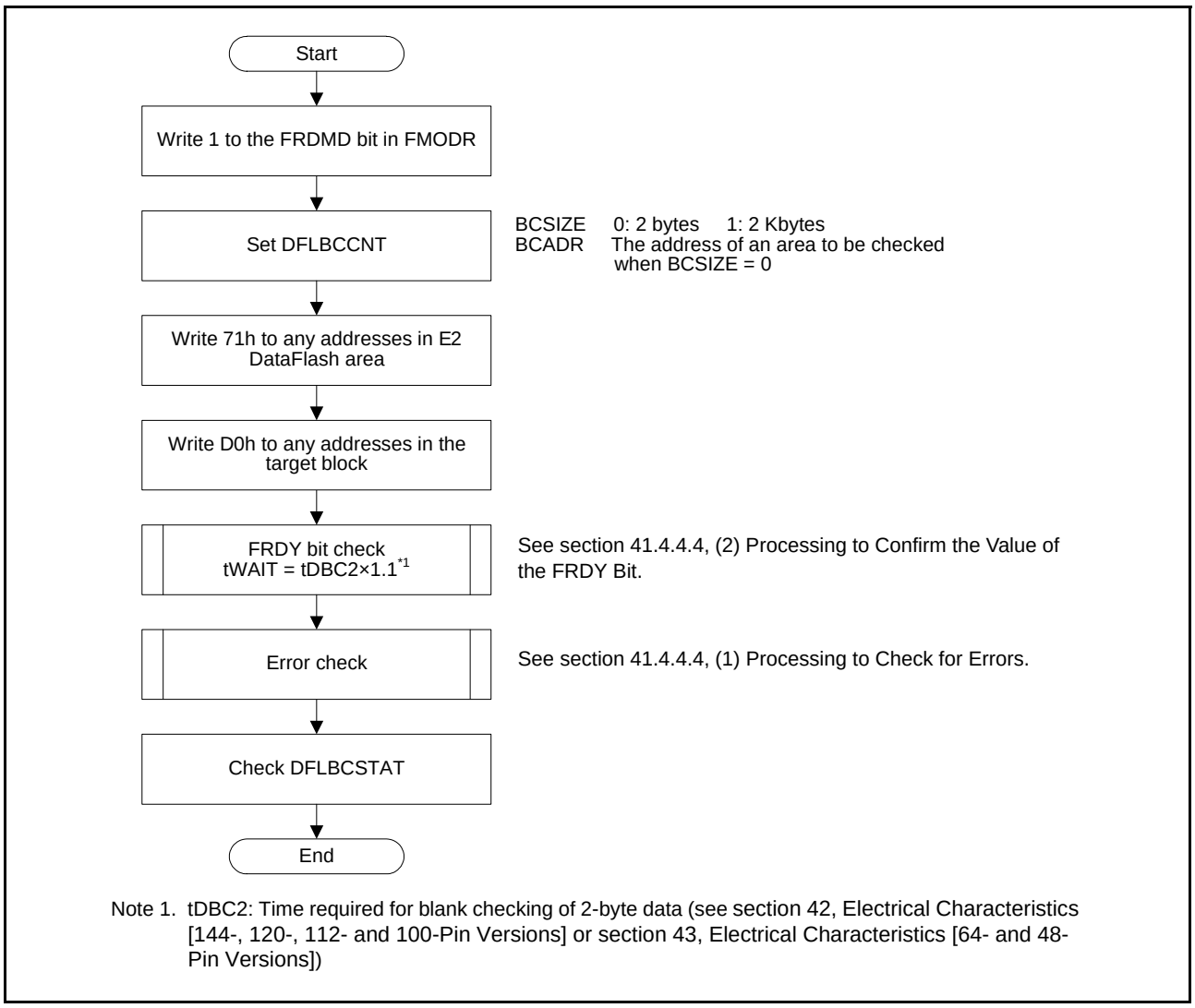


Figure 41.15 Procedure for Reading Lock Bit in Register Read Mode

(8) Blank Checking

Blank checking can only be executed on the E2 DataFlash. Since using the CPU to read erased areas of the E2 DataFlash produces undefined values, the blank checking command should be used to check whether the E2 DataFlash has actually been erased. To make the blank checking command available for use, start by setting the FRDMD bit in FMODR to 1 to enable the command, and then specify the size and start address of the target area in DFLBCCNT. When the DFLBCCNT.BCSIZE bit is 1, checking can be performed on the entire area (2 Kbytes) as specified in the second cycle of the blank check command. When the BCSIZE bit is 0, checking can be performed on the 2-byte range starting from the address obtained by adding the start address of the area as specified in the second cycle of the command and the value held by DFLBCCNT. In the first cycle of the command sequence, the value 71h is written to an address in the E2 DataFlash. In the second cycle, when the value D0h is written to an address in the erasure block within the target area, the FCU starts blank checking of the E2 DataFlash. Test the FRDY bit in the FSTATR0 register to check whether or not the check is complete. On completion of blank checking, check the BCST bit of DFLBCSTAT to see whether the target area has been erased or is filled with 0s and/or 1s.

Figure 41.16 shows the procedure for blank checking of the E2 DataFlash.



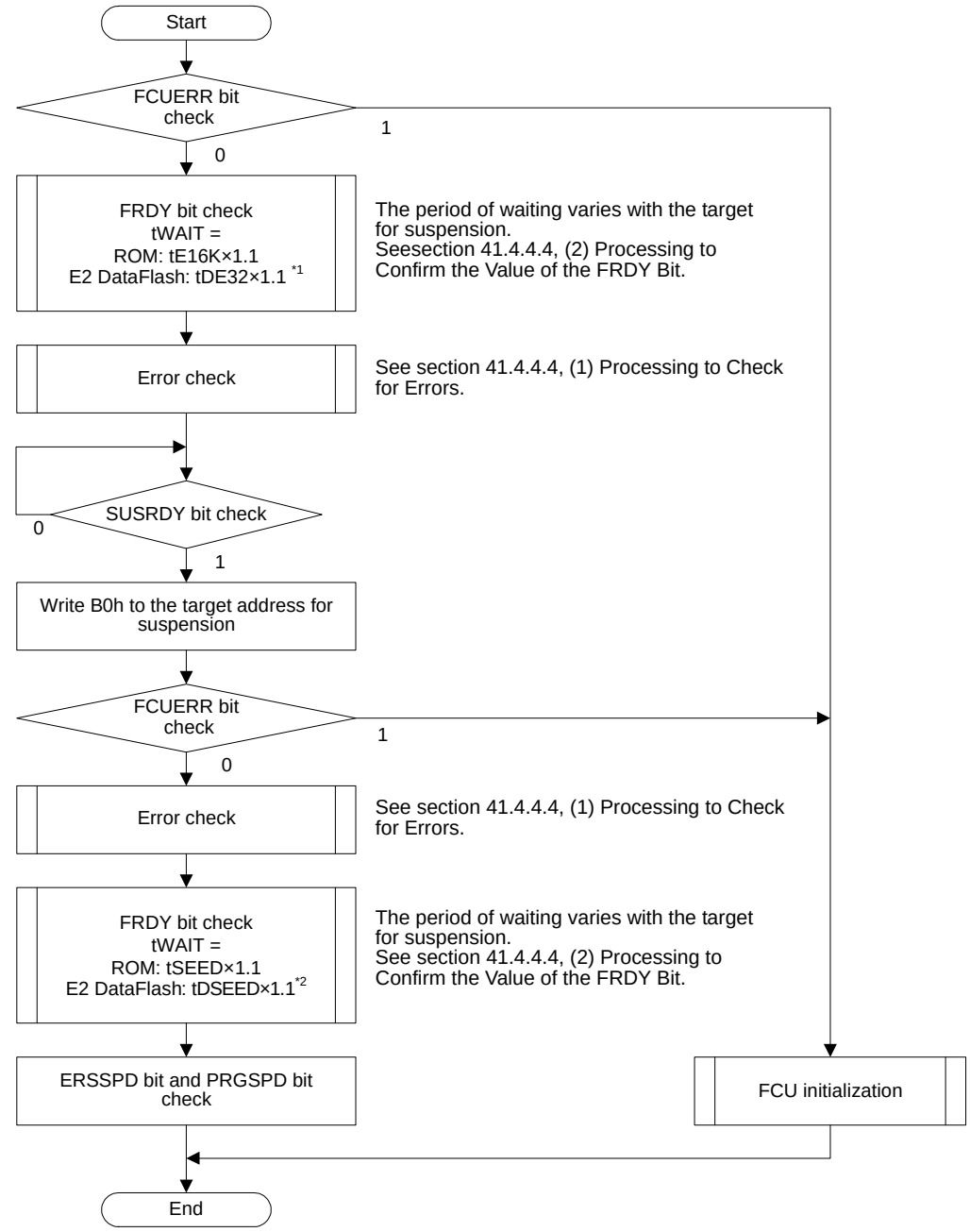
Note 1. tDBC2: Time required for blank checking of 2-byte data (see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions])

Figure 41.16 Procedure for Blank Checking of the E2 DataFlash

41.4.4.3 Suspension and Resumption

(1) Suspending Programming or Erasure

To suspend programming/erasure for the ROM/E2 DataFlash, use the P/E suspend command.
When issuing a P/E suspend command, check that the ILGLERR, ERSERR, and PRGERR bits in FSTATR0 and the FSTATR1.FCUERR bit are 0, and the execution of programming/erasure is normally performed. To confirm that the suspend command can be received, also check that the FSTATR0.SUSRDY bit is 1. After issuing a P/E suspend command, read FSTATR0 and FSTATR1 to confirm that no error occurs.
If an error occurs during programming/erasure, at least one of the ILGLERR, PRGERR, ERSERR, and FCUERR bits is set to 1. When programming/erasure processing has finished during the interval from when the SUSRDY bit is checked as 1 to when a P/E suspend command is received, the ILGLERR bit is set to 1 because the issued P/E suspend command is detected as an illegal command.
When programming/erasure processing has finished simultaneously with the reception of a P/E suspend command, no error occurs and the suspended state is not entered (FSTATR0.FRDY bit is 1 and ERSSPD and PRGSPD bits in FSTATR0 are 0). When a P/E suspend command is received and then the programming/erasure suspend processing finishes normally, the FCU enters the suspended state, the FRDY bit is set to 1, and the ERSSPD or PRGSPD bit is set to 1. After issuing a P/E suspend command, check that the FRDY bit is set to 1, and the ERSSPD or PRGSPD bit is 1 and the FCU enters the suspended state, and then decide the subsequent flow. When issuing a P/E resume command in the subsequent flow although the FCU does not enter the suspended state, an illegal command error occurs and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).
If the erasure suspended state is entered, programming to blocks other than an erasure target can be performed. Additionally, the programming and erasure suspended states can shift to ROM read mode by clearing FENTRYR.
For details on FCU operations at the reception of a P/E suspend command, see section 41.5, Suspending Operation.



Note 1. tE16K: Time required for erasing a 16-Kbyte block
tDE32: Time required for erasing a 32-Kbyte block
(see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions])

Note 2. tSEED: Suspend delay time for the ROM
tDSEED: Suspend delay time for the E2 DataFlash
(see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions])

Figure 41.17 Procedure for Programming/Erasure Suspension

(2) Resuming Programming or Erasure

To resume a suspended programming/erasure processing, use the P/E resume command. When the settings of FENTRYR are changed during suspension, reset FENTRYR to the value immediately before the P/E suspend command was issued, and then issue a P/E resume command.

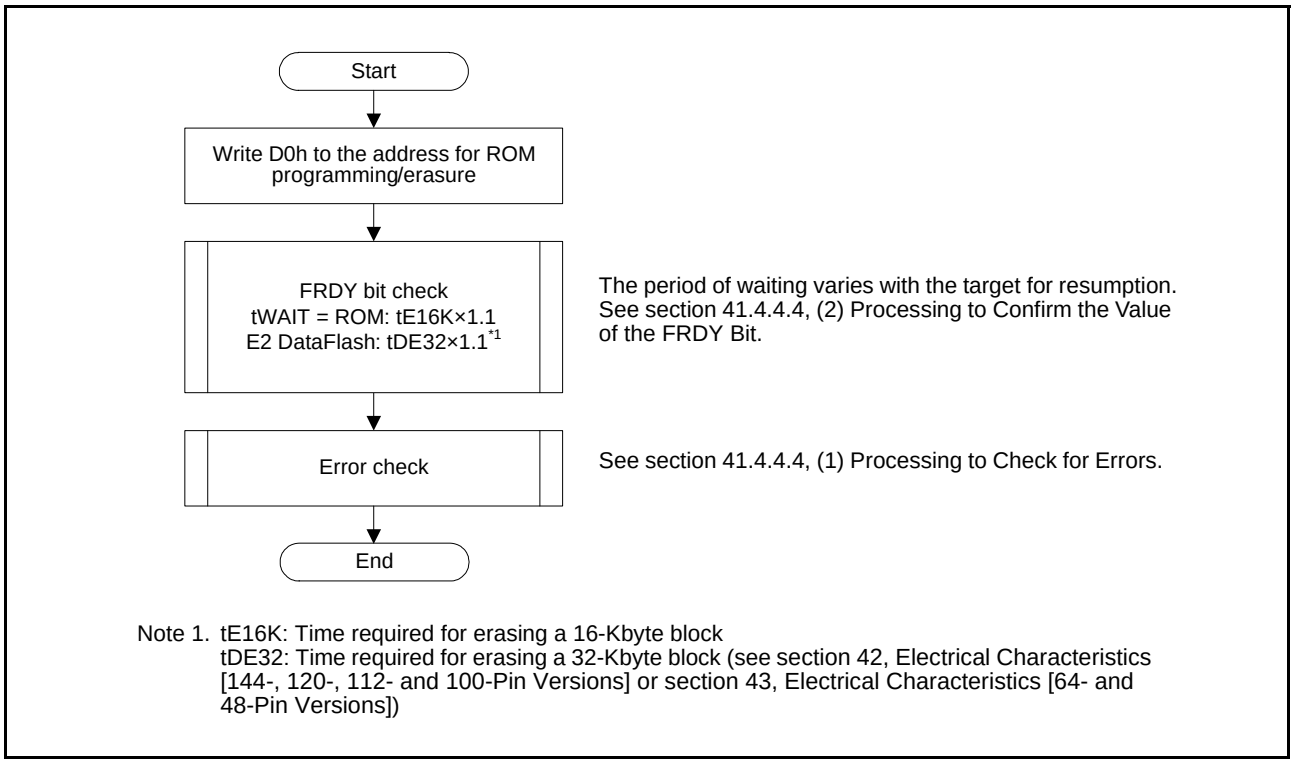


Figure 41.18 Procedure for Resuming Programming or Erasure

41.4.4.4 Processing to Check for Errors and to Confirm the Value of the FRDY Bit

The following passages describe processing to check for errors and processing to confirm the value of the FRDY bit. For details on errors, see section 41.6, Protection.

(1) Processing to Check for Errors

- Checking Flash Status Register 0 (FSTATR0)

To check FSTATR0, read FSTATR0 directly or read the ROM programming/erasure address in ROM status read mode. For the reading in ROM status read mode, see section 41.4.4.1, (4) Switching to Status Read Mode.

- Clearing Flash Status Register 0 (FSTATR0)

To clear the ILGLERR, ERSERR and PRGERR bits in FSTATR0 to 0, use the status register clear command. When one of the ILGLERR, ERSERR and PRGERR bits in FSTATR0 is 1, the FASTAT.CMDLK bit is set to 1 (command-locked state) and the FCU receives no FCU commands other than the status register clear command. If the ILGLERR bit is 1, also check the values of the ROMAE, DFLAE, DFLRPE, and DFLWPE bits in FASTAT. Even if issuing a status register clear command without clearing these bits, the ILGLERR bit is not cleared to 0.
Figure 41.19 shows the flow of processing to check for errors and of the subsequent processing.

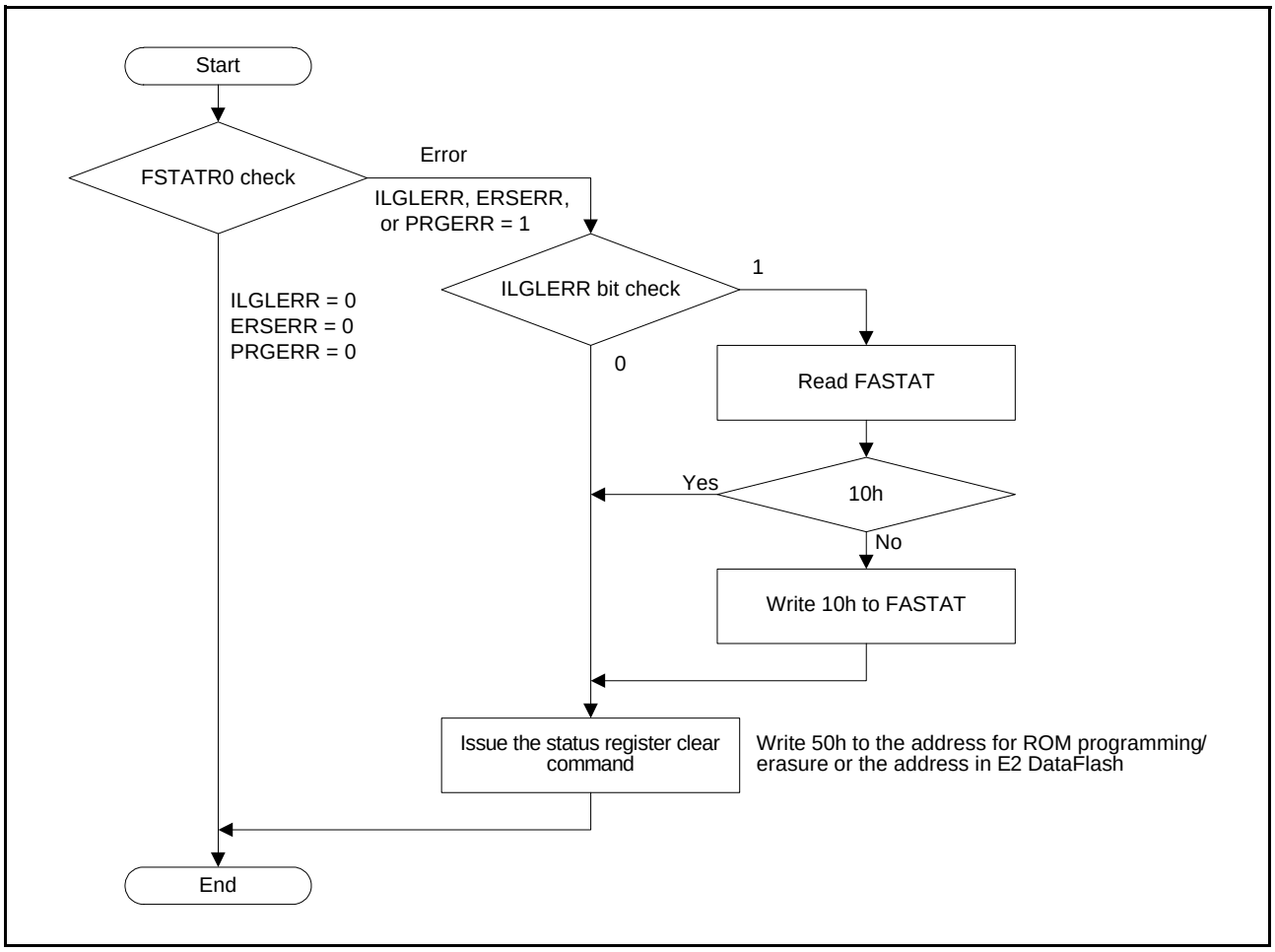


Figure 41.19 Processing to Check for Errors

(2) Processing to Confirm the Value of the FRDY Bit

A period of waiting for processing is required after an FCU command is issued. For details on the period of waiting, see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions]. When a timeout leads to the FSTATR0.FRDY bit not being set to 1, FRESETR must be used to initialize the FCU. For the initialization of the FCU, see section (3), Initializing the FCU.

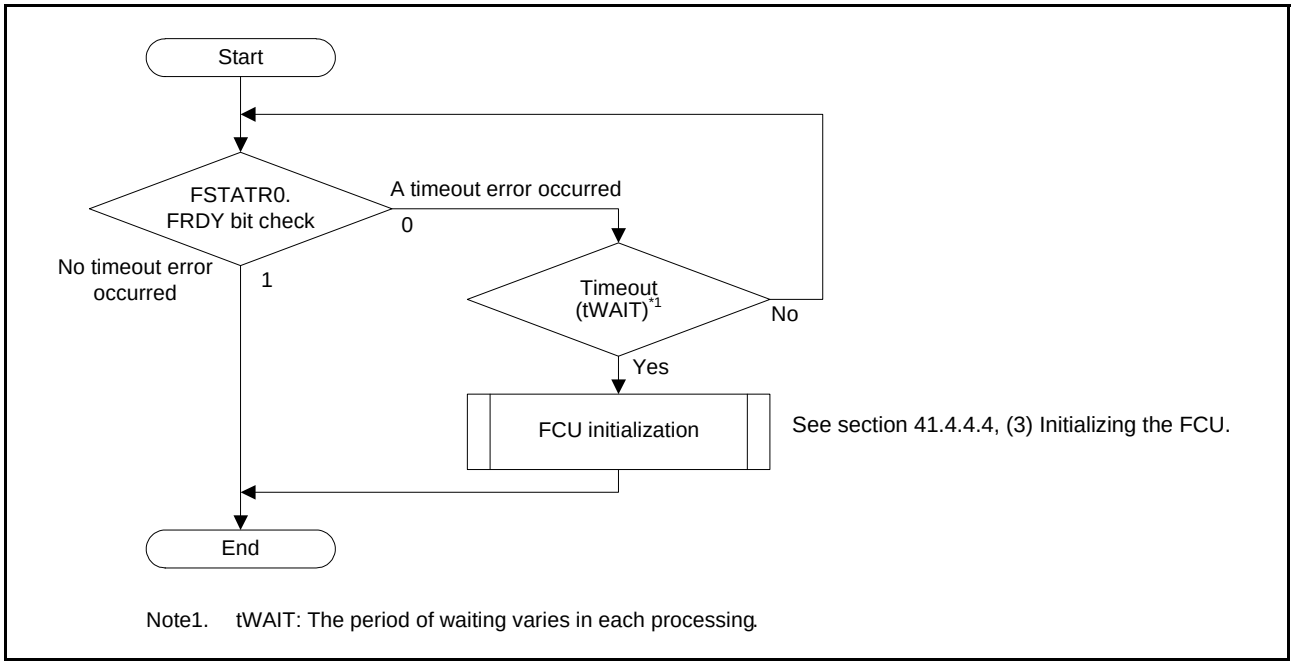


Figure 41.20 Processing to Confirm the Value of the FRDY Bit

(3) Initializing the FCU

If a timeout occurs after an FCU command has been issued, or the FSTATR0.FRDY bit is 1, FRESETR must be used to initialize the FCU. In either case, maintain the FRESETR.FRESET bit set to 1 for a period of tFCR (FCU reset time, see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] or section 43, Electrical Characteristics [64- and 48-Pin Versions]). Disable reading from the ROM and E2 DataFlash memory during this period of keeping the FRESET bit set to 1. In addition, while the FRESET bit is 1, FCU commands are disabled because FENTRYR is initialized. Restart the processing from the start, as shown in Figure 41.10.

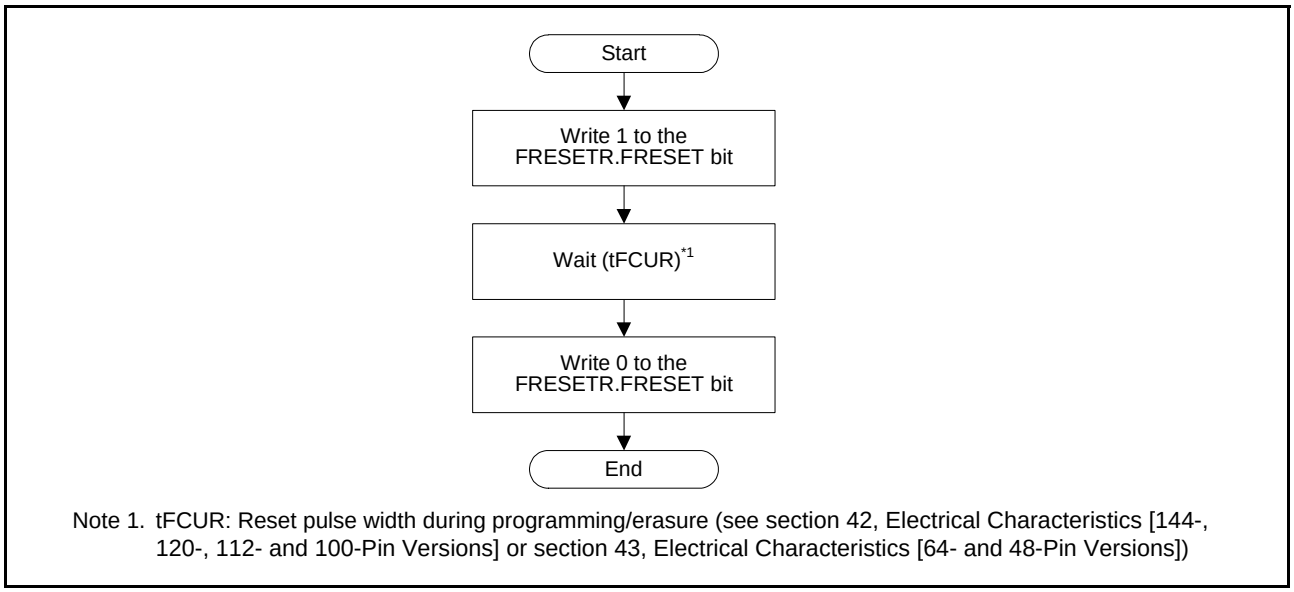


Figure 41.21 FCU Initialization Flow

41.5 Suspending Operation

The ROM/E2 DataFlash cannot be read during programming/erasure. The ROM/E2 DataFlash can be read by suspending the ROM/E2 DataFlash programming/erasure with the P/E suspend command. The P/E suspend command includes one programming mode and two erasure modes (suspension priority mode and erasure priority mode). The P/E resume command that resumes suspended programming/erasure processing is also provided.

41.5.1 Suspension during Programming

When issuing a P/E suspend command during the ROM/E2 DataFlash programming, the FCU suspends programming processing. Figure 41.22 shows the suspend operation of programming.
When receiving a programming-related command, the FCU clears the FSTATR0.FRDY bit to 0 to start programming. If the FCU enters the state in which the P/E suspend command can be received after starting programming, it sets the FSTATR0.SUSRDY bit to 1. When a P/E suspend command is issued, the FCU receives the command and clears the SUSRDY bit to 0. If the FCU receives a P/E suspend command while a programming pulse is being applied, the FCU continues applying the pulse. After the specified pulse application time, the FCU finishes pulse application, and starts the programming suspend processing and sets the FSTATR0.PRGSPD bit to 1. When the suspend processing finishes, the FCU sets the FRDY bit to 1 to enter the programming suspended state. When receiving a P/E resume command in the programming suspended state, the FCU clears the FRDY and PRGSPD bits to 0 and resumes programming.

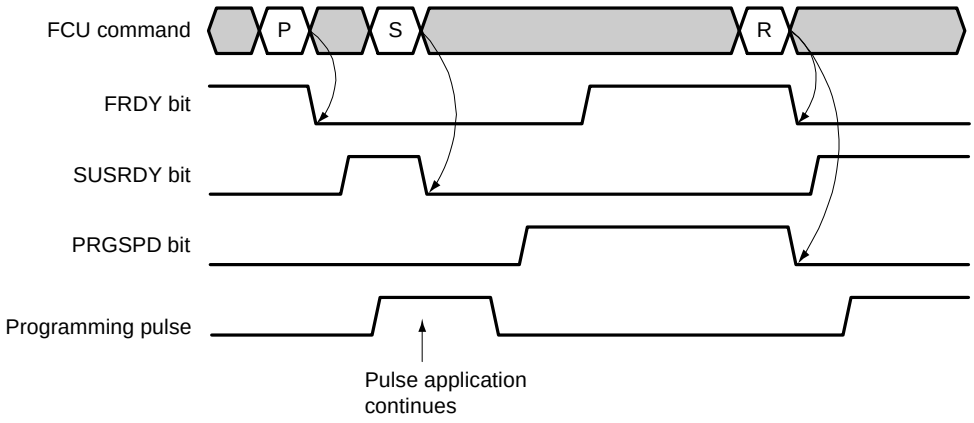


Figure 41.22 Suspension during Programming

41.5.2 Suspension during Erasure (Suspension Priority Mode)

This MCU has a suspension priority mode for the suspension of erasure.

Figure 41.23 shows the suspend operation of erasure when the erasure suspend mode is set to the suspension priority mode (FCPSR.ESUSPMD bit is 0).

When receiving an erasure-related command, the FCU clears the FSTATR0.FRDY bit to 0 to start erasure. If the FCU enters the state in which the P/E suspend command can be received after starting erasure, it sets the FSTATR0.SUSRDY bit to 1. When a P/E suspend command is issued, the FCU receives the command and clears the SUSRDY bit to 0. When receiving a suspend command during erasure, the FCU starts the suspend processing and sets the FSTATR0.ERSSPD bit to 1 even if it is applying an erasure pulse. When the suspend processing finishes, the FCU sets the FRDY bit to 1 to enter the erasure suspended state. When receiving a P/E resume command in the erasure suspended state, the FCU clears the FRDY and ERSSPD bits to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD bits at the suspension and resumption of erasure are the same, regardless of the erasure suspend mode.

The setting of the FCPSR.ESUSPMD bit affects the control method of erasure pulses. In suspension priority mode, when receiving a P/E suspend command while erasure pulse A that has never been suspended in the past is being applied, the FCU suspends the application of erasure pulse A and enters the erasure suspended state. When receiving a P/E suspend command while reapplying erasure pulse A after erasure is resumed by a P/E resume command, the FCU continues applying erasure pulse A. After the specified pulse application time, the FCU finishes erasure pulse application and enters the erasure suspended state. When the FCU receives a P/E resume command next and erasure pulse B starts to be newly applied, and then the FCU receives a P/E suspend command again, the application of erasure pulse B is suspended. In suspension priority mode, delay due to suspension can be minimized because the application of an erasure pulse is suspended one time per pulse and priority is given to the suspend processing.

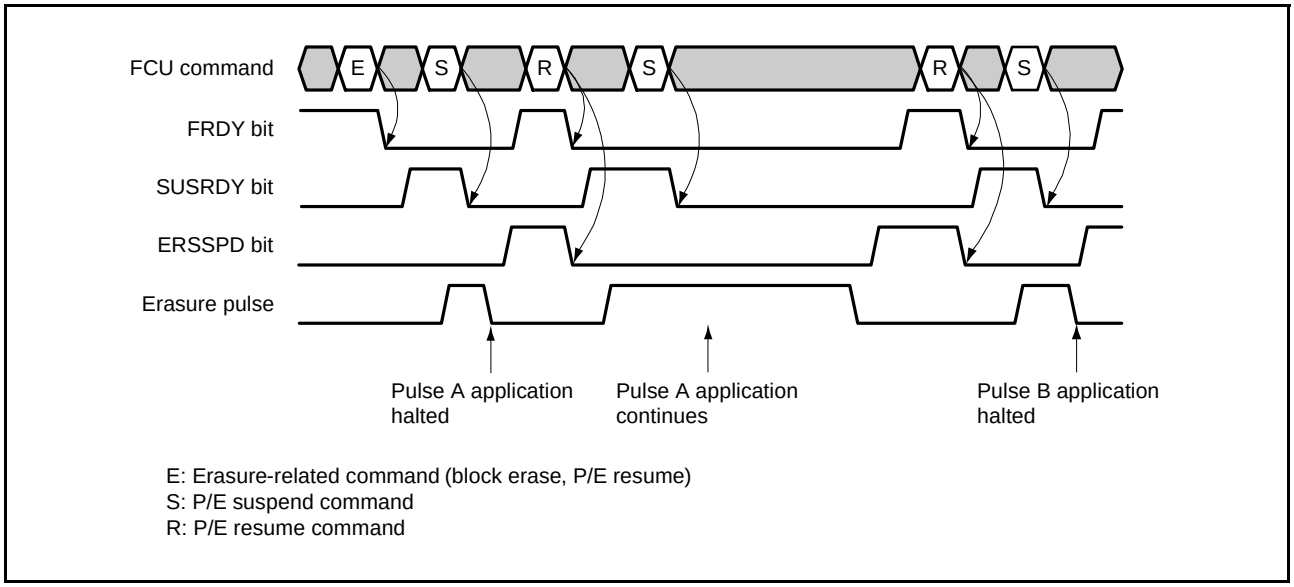


Figure 41.23 Suspension during Erasure (Suspension Priority Mode)

41.5.3 Suspension during Erasure (Erasure Priority Mode)

This MCU has a suspension priority mode for the suspension of erasure.
Figure 41.24 shows the suspend operation of erasure when the erasure suspend mode is set to the erasure priority mode (FCPSR.ESUSPMD bit is 1). The control method of erasure pulses in erasure priority mode is the same as that of programming pulses for the programming suspend processing.
If the FCU receives a P/E suspend command while an erasure pulse is being applied, the FCU definitely continues applying the pulse. In this mode, the required time for the whole erasure processing can be reduced as compared with the suspension priority mode because the reapplication of erasure pulses does not occur when a P/E resume command is issued.

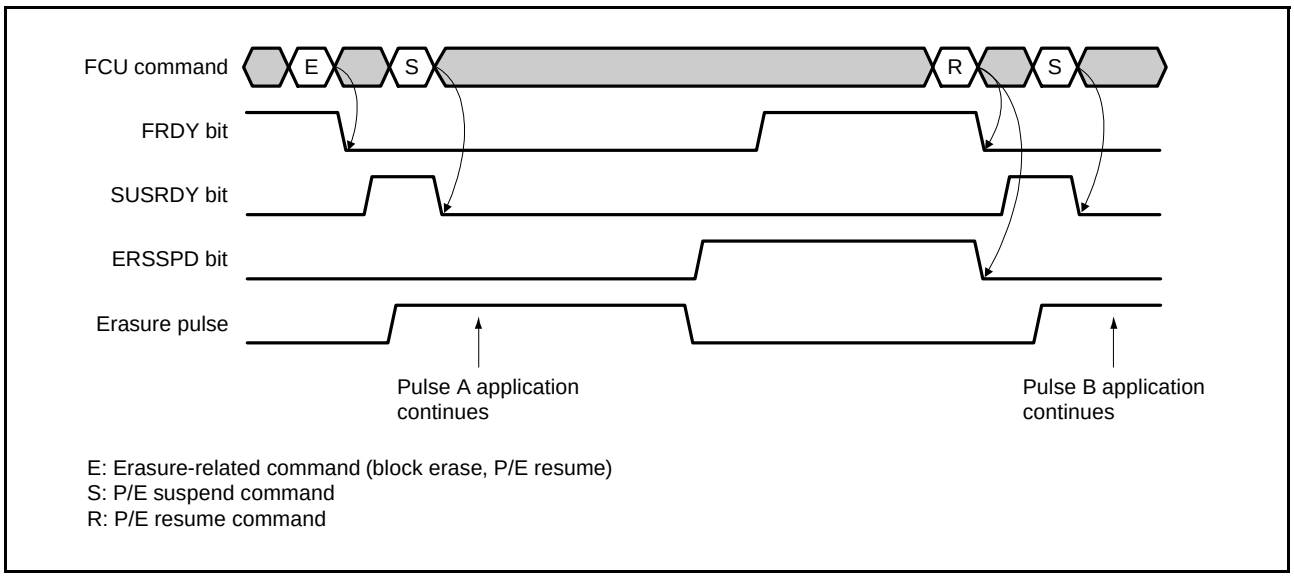


Figure 41.24 Suspension during Erasure (Erasure Priority Mode)

41.6 Protection

Protection against programming/erasure for the ROM/E2 DataFlash includes software protection and the command-locked state.

41.6.1 Software Protection

With the software protection, the ROM/E2 DataFlash programming/erasure is prohibited by the settings of the control registers or user area lock bit. When the software protection is violated and a ROM/E2 DataFlash programming/erasure-related command is issued, the FCU detects an error and the FASTAT.CMDLK bit is set to 1 (command-locked state).

(1) Protection through FWEPROR

If the FWEPROR.FLWE[1:0] bits are not set to 01b, programming cannot be performed in any of the modes.

(2) Protection through FENTRYR

When the FENTRYR.FENTRY0 and FENTRYD bits are both 0, ROM/E2 DataFlash read mode is selected. Because the FCU command cannot be received in ROM/E2 DataFlash read mode, ROM/E2 DataFlash programming/erasure is prohibited. When an FCU command is issued in ROM/E2 DataFlash read mode, the FCU detects an illegal command error and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).

(3) Protection through Lock Bit

Each block in the user area includes a lock bit. When the FPROTR.FPROTCN bit is 0, blocks whose lock bit is set to 0 are prohibited from being programmed/erased. To program or erase blocks whose lock bit is set to 0, set the FPROTCN bit to 1. When the lock bit protection is violated and a ROM programming/erasure-related command is issued, the FCU detects a programming/erasure error and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).

(4) Protection through DFLWEy

When the DBWEj (j = 00 to 15) bit in DFLWEy (y = 0, 1) is 0, programming and erasure of block DBj in the data area is disabled. If an attempt is made to program or erase block DBj while the DBWEj bit is 0, the FCU detects a programming/erasure protection error and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).

(5) Protection through DFLREy

When the DBREj (j = 00 to 15) bit in DFLREy (y = 0, 1) is 0, reading of block DBj in the data area is disabled. If an attempt is made to read block DBj while the DBREj bit is 0, the FCU detects a read protection error and the FASTAT.CMDLK bit is set to 1 (command-locked state) (see section 41.6.2, Command-Locked State).

41.6.2 Command-Locked State

With the command-locked state, the FCU detects malfunctions caused by FCU command issuance errors and prohibited access occurrences, and an FCU command is prohibited from being received.
When any bit from among the status bits (the ILGLERR, ERSERR, and PRGERR bits in FSTATR0, the FSTATR1.FCUERR bit, and the ROMAE, DFLAE, DFLRPE and DFLWPE bits in FASTAT), the FCU will be in the command-locked state (FASTAT.CMDLK bit is set to 1), so programming and erasure of the ROM/E2 DataFlash are prohibited. To clear the command-locked state, a status register clear command must be issued with FASTAT set to 10h. While the interrupt enable bit in FAEINT is 1, if the corresponding bit in FASTAT is set to 1, a flash interface error (FIFERR) interrupt occurs.
Table 41.12 lists the relationship between the error contents and status bit values (FSTATR0.ILGLERR, ERSERR, and PRGERR bits, FSTATR1.FCUERR bit, and FASTAT.ROMAE, DFLAE, DFLRPE, and DFLWPE bits) at error detection.
If a command other than the suspend command is issued during programming/erasure and the FCU enters the command-locked state, it continues programming/erasure. In this state, it is impossible to issue a P/E suspend command and suspend programming/erasure. When a command is issued in the command-locked state, the ILGLERR bit is set to 1.

Table 41.12 Errors and Status Bits

Type	Description	ILGLERR	ERSERR	PRGERR	FCUERR	ROMAE	DFLAE	DFLRPE	DFLWPE
FENTRYR setting error	FENTRYR setting is other than 0001h and 0080h.	1	0	0	0	0	0	0	0
	The FENTRYR setting at suspension disagrees with that at resumption	1	0	0	0	0	0	0	0
Illegal command error (Common to ROM/ E2 DataFlash)	Undefined code is specified in the first cycle of an FCU command	1	0	0	0	0	0	0	0
	Other than D0h is specified in the last cycle of a multi-cycle FCU command	1	0	0	0	0	0	0	0
	The peripheral clock is set to other than 1 to 100 MHz in PCKAR (an error is not detected if the setting is from 1 to 4 MHz or from 50 to 100 MHz)	1	0	0	0	0	0	0	0
	A command other than the suspend command is issued during programming/erasure	1	0	0	0	0	0	0	0
	A suspend command is issued during processing other than programming/ erasure	1	0	0	0	0	0	0	0
	A suspend command is issued in the suspended state	1	0	0	0	0	0	0	0
	A resume command is issued in other than the suspended state	1	0	0	0	0	0	0	0
	A programming/erasure-related command (programming/lock bit programming/block erase) is issued in the programming suspended state	1	0	0	0	0	0	0	0
	A block erase command is issued in the erasure suspended state	1	0	0	0	0	0	0	0
	A programming or lock bit programming command is issued to an erasure suspend target area in the erasure suspended state	1	0	0	0	0	0	0	0
	A command is issued when the FASTAT.CMDLK bit is 1 (in the command-locked state)	1	0/1	0/1	0/1	0/1	0	0	0
Illegal command error (ROM)	Other than 40h is specified in the second cycle of a programming command	1	0	0	0	0	0	0	0
Erasure error	An error occurs during erasure	0	1	0	0	0	0	0	0
	When the FPROTR.FPROTCN bit is 0, a block erase command is issued to an erasure block whose lock bit is set to 0	0	1	0	0	0	0	0	0
Illegal command error (E2 DataFlash)	Other than 01h is specified in the second cycle of a programming command	1	0	0	0	0	0	0	0
	When the FENTRYR.FENTRYD bit is 1, lock bit programming command is issued to the E2 DataFlash area when the FENTRYR.FENTRYD bit is 1	1	0	0	0	0	0	0	0
Programming error	An error occurs during programming	0	0	1	0	0	0	0	0
	When the FPROTR.FPROTCN bit is 0, a programming or lock bit programming command is issued to a block whose lock bit is set to 0	0	0	1	0	0	0	0	0
FCU error	An error occurs during FCU internal processing	0	0	0	1	0	0	0	0
ROM access violation	When the area is in the ROM P/E mode (FENTRYR.FENTRY0 bit = 1), an attempt is made to read a read address in the area*1	1	0	0	0	1	0	0	0
	An FCU command was issued for the address for programming/erasure in the area while the area is in read mode (FENTRYR.FENTRY0 bit = 0)	1	0	0	0	1	0	0	0
	An attempt is made to read the area while in the ROM P/E mode (the FENTRYR register is set)	1	0	0	0	1	0	0	0
E2 DataFlash access error	An attempt is made to read the E2 DataFlash area while in the E2 DataFlash P/E normal mode (FENTRYR.FENTRYD bit = 1)	1	0	0	0	0	1	0	0
	An FCU command is issued for the E2 DataFlash area while FENTRYR.FENTRYD is 0	1	0	0	0	0	1	0	0
	An FCU command is issued for the E2 DataFlash area while the FENTRYR.FENTRY0 bit is 1	1	0	0	0	0	1	0	0
E2 DataFlash read protect error	An attempt is made to read the E2 DataFlash area while it is protected against reading by the DFLREy (y = 0, 1) setting	1	0	0	0	0	0	1	0
E2 DataFlash programming protect error	A programming/erasure command is issued for the E2 DataFlash area while it is protected against programming and erasure by the DFLWEy (y = 0, 1) setting	1	0	0	0	0	0	0	1

Note 1. For the correspondence between ROM capacity and areas, see section 41.1.1, Configuration of the ROM Area.

41.7 User Boot Mode

If the low level is on the MD pin and the high level is on the P00 pin at the time of release from the reset state, the chip starts in user boot mode. The reset vector at this time points to the address FF7F FFFCh of the user boot area. For other vector tables, refer to normal vector table (see section 15, Interrupt controller (ICUb)).
In user boot mode, it is possible to perform programming using a given interface; user area or data area can be programmed or erased by issuing the FCU command. Note that programming to the user boot area should be performed in boot mode.

41.8 Boot Mode

41.8.1 System Configuration

In boot mode, the host sends control commands and data for programming, and the user area, data area, and user boot area are programmed or erased accordingly. An on-chip SCI handles transfer between the host and the MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.
When this MCU is activated in boot mode, the program on the boot area is executed. This program automatically adjusts the bit rate of the SCI and controls programming/erasure by receiving control commands from the host.
Figure 41.25 shows the system configuration for operations in boot mode.
Input and output pins associated with the ROM/E2 DataFlash are listed in Table 41.13.

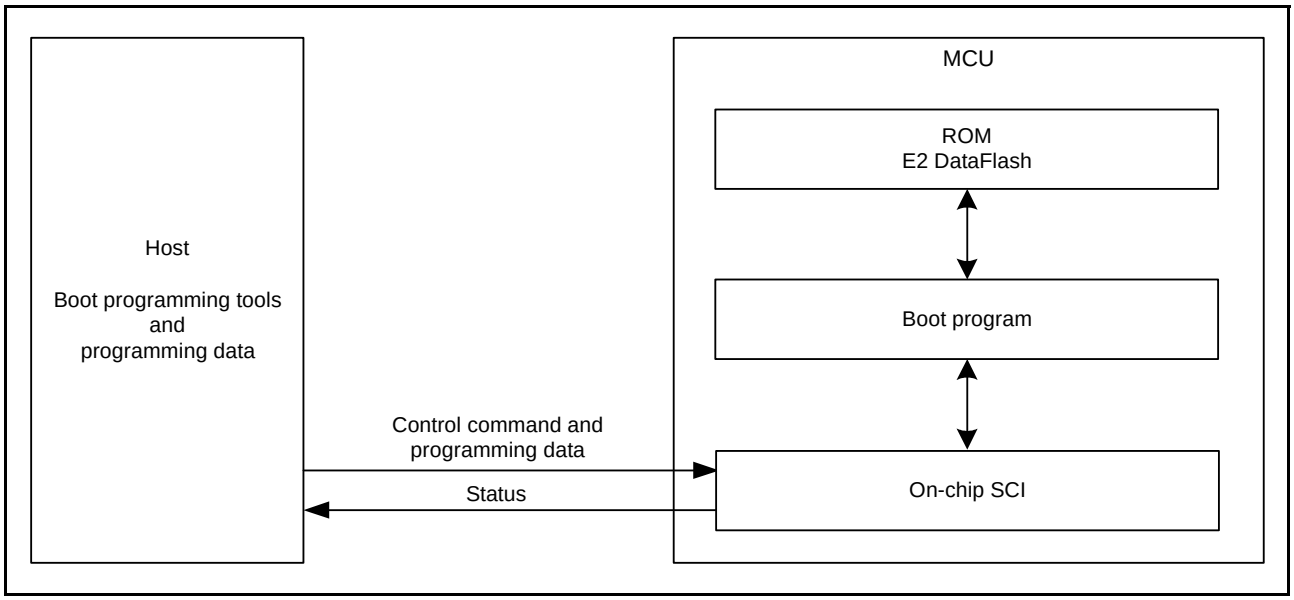


Figure 41.25 System Configuration for Operations in Boot Mode

Table 41.13 Input and Output Pins Associated with the ROM/E2 DataFlash

Pin Name	I/O	Mode to be Used	Use
MD	Input	Boot mode User boot mode USB boot mode	Selection of operation mode
P00	Input		Selection of boot mode (SCI boot), user boot mode, or USB boot mode
TDI/RXD1 (144-pin package)*1 PD5/RXD1 (120/100/64/48-pin packages) PF4/RXD1 (112-pin package)*1	Input	Boot mode	For host communication (to receive data through SCI)
TDO/TXD1 (144-pin package)*1 PD3/TXD1 (120/100/64/48-pin packages) PF2/TXD1 (112-pin package)*1	Output		For host communication (to transmit data through SCI)
USB0_DP, USB0_DM	I/O	USB boot mode	Data input/output of USB
USB0_DPUPE	I/O		Control of pull-up for USB
PE5/USB0_VBUS	Input		Detection of connection and disconnection of USB cables
PE2	Input		Selection of USB bus-power mode or self-power mode

Note 1. Can be used as an SCI pin only in boot mode.

41.8.2 State Transitions in Boot Mode

Figure 41.26 is a diagram of the state transitions in boot mode.

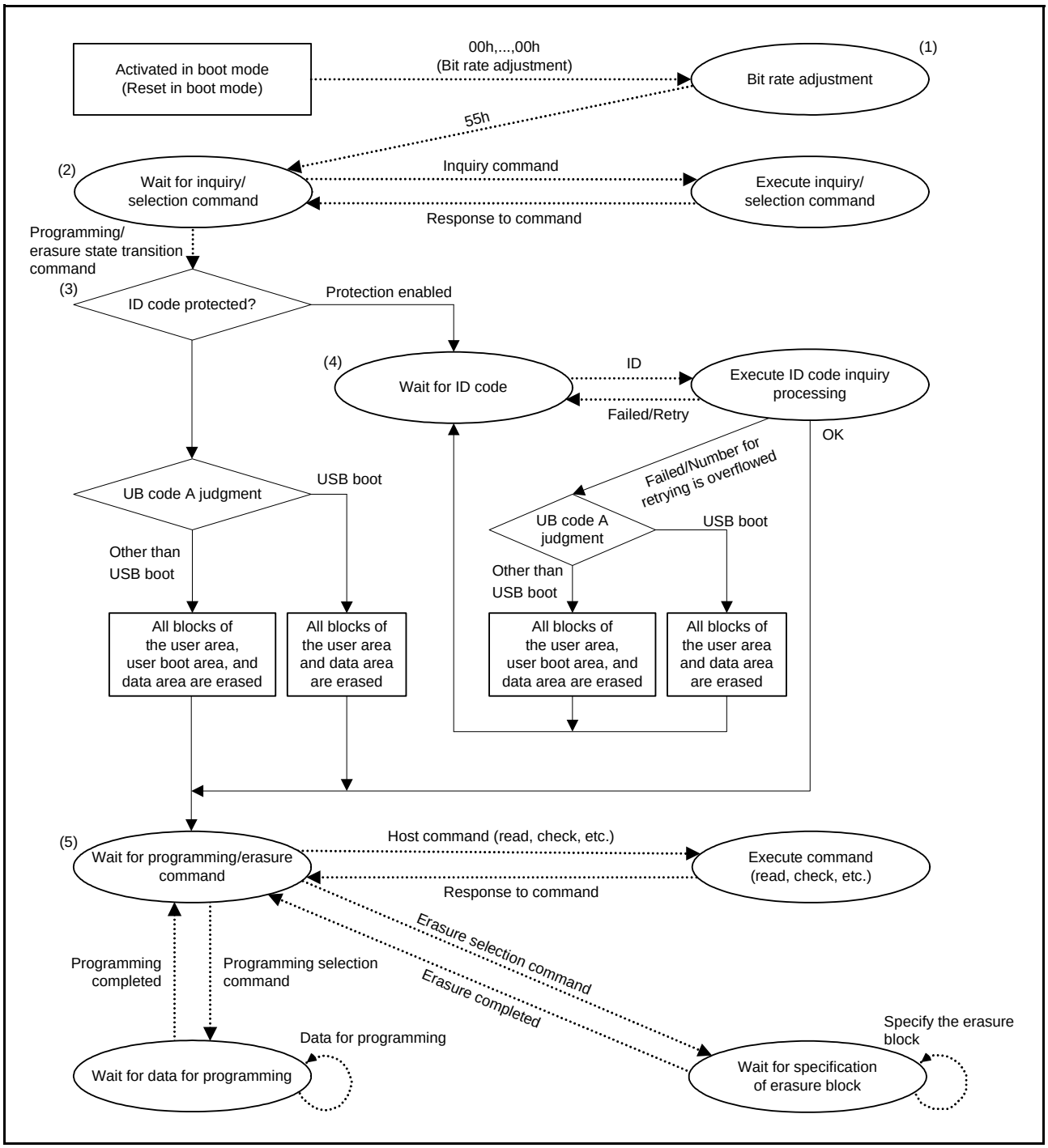


Figure 41.26 State Transitions in Boot Mode

(1) Matching the Bit Rates

When this MCU is activated in boot mode, the bit rate of the SCI is automatically adjusted to match that of the host. On completion of this automatic bit rate adjustment, this MCU transmits the value 00h to the host. On subsequent correct reception of the value 55h sent from the host, this MCU enters the wait for a command for inquiry or selection. For details on matching of the bit rates, see section 41.8.3, Automatic Adjustment of the Bit Rate.

(2) Waiting for a Command for Inquiry or Selection

This state is for inquiries on the area size, the area configuration, the addresses where the areas start, the state of support, etc., and for selection of the device, clock mode, and bit rate. This MCU receives a programming/erasure state transition command issued by the host and then enters the state to determine whether ID code protection is enabled or disabled. For the inquiry/selection commands, see section 41.8.7, Inquiry/Selection Command Wait.

(3) Judging ID Code Protection

This state is for determining whether ID code protection is enabled or disabled. The control code and ID code written in ROM are used to determine whether ID code protection is enabled or disabled. When enabled, the state of waiting for the ID code is entered. When disabled, the user area and data area are completely erased, and the wait for programming and erasure commands is entered. For details on the control code and ID code, see section 41.8.4, ID Code Protection (Boot Mode).

(4) Waiting for an ID Code

This state is for waiting for the control code and ID code to be sent from the host. The control code and ID code sent by the host are compared with the code stored in ROM, and the state of waiting for programming and erasure commands is entered if the two match. If they do not match, the next transition is back to the state of waiting for an ID code. However, if the ID codes fail to match three times in a row and also the state of protection is authentication method 1, the ROM is completely erased, and the state of waiting for an ID code is entered again. Turn the power off and start all over. For details on the control code and ID code, see section 41.8.4, ID Code Protection (Boot Mode).

(5) Waiting for a Command for Programming or Erasure

In this state, programming and erasure proceed in accordance with commands from the host. In response to the reception of a command, this MCU enters the wait for the data to use in programming, the wait for specification of the erasure block to be erased, or the state of executing the processing of commands, such as read and check.
When this MCU receives a programming selection command, it enters the state of waiting for the data to use in programming. After the host has issued the programming selection command, the process continues with the address where programming is to start and then the data for programming. Setting of FFFF FFFFh as the address where programming is to start indicates the completion of programming, and the next transition is from the wait for the data to use in programming to the wait for programming and erasure commands.
When this MCU receives an erasure selection command, it enters the state of waiting for specification of the erasure block to be erased. After the host has issued the erasure selection command, the process continues with the number of the erasure block to be erased. Setting of FFh as the number of the erasure block indicates the completion of erasure, and the next transition is from the wait for specification of the erasure block to the wait for programming and erasure commands. Since the user area, user boot area and data area are all completely erased during the interval between booting up in boot mode and transition to the wait for programming and erasure commands, execution of erasure is not necessary unless data newly programmed in boot mode is to be erased without a further reset.
Other than the programming and erasure commands, commands for execution in this state include those for checksum of the user area and user boot area, blank checking, reading from memory, and acquiring status information.

41.8.3 Automatic Adjustment of the Bit Rate

When this MCU is booted up in boot mode, asynchronous transfer by the SCI is used to measure the periods at low level of consecutive bytes with value 00h that are sent from the host. While the period at low level is being measured, set the host's SCI transfer format to 8-bit data, one stop bit, no parity, and a transfer rate of 9,600 bps or 19,200 bps. This MCU calculates the host's SCI bit rate from the measured periods at low level, adjusts its own bit rate accordingly, and then sends the value 00h to the host.
If reception of the value 00h by the host is successful, the host responds by sending the value 55h to this MCU. If successful reception of 00h by the host is not possible, reboot this MCU in boot mode, and then repeat the process of automatically adjusting the bit rate. If reception of the value 55h by this MCU is successful, it responds by sending E6h to the host, and if successful reception of 55h by this MCU is not possible, it responds by sending FFh to the host.

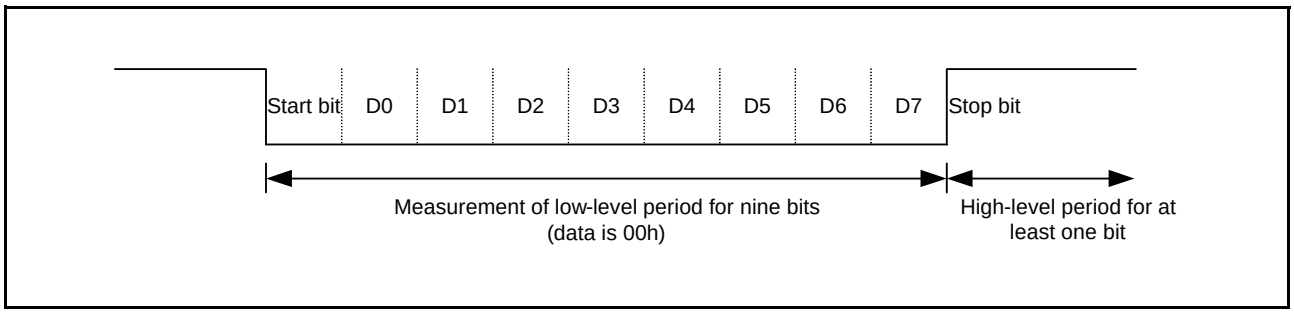


Figure 41.27 Transfer Format Used by SCI in Automatic Adjustment of Bit Rate

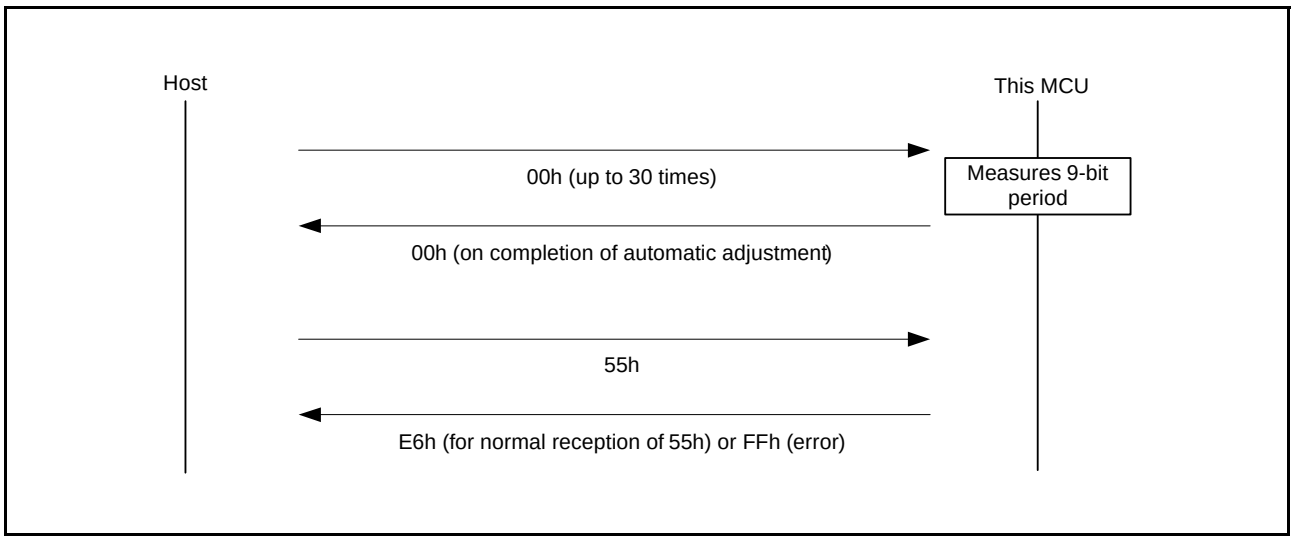


Figure 41.28 Sequence of Transfer between Host and this MCU

Since the bit rate of this MCU depends on the bit rate of SCI communications and the frequency of this MCU's peripheral clock, adjustment to match the bit rate will not be possible under some conditions. Accordingly, ensure that SCI communication is under the conditions given in Table 41.14.

Table 41.14 Conditions for Automatic Bit-Rate Adjustment

Bit Rate of SCI in Host	Frequency Range for EXTAL Signal
9,600 bps	4 to 14 MHz*1
19,200 bps	8 to 14 MHz*1

Note 1. The minimum and maximum frequencies of the resonator are 8 MHz and 12.5 MHz, respectively.

41.8.4 ID Code Protection (Boot Mode)

This function is used to prohibit reading/programming/erasure from the host such as the PC.
After automatic adjustment of the bit rate when booting up in boot mode, the ID code transmitted from the host and the control and ID codes written to the ROM are used to determine disabling or enabling of ID code protection. When ID code protection is enabled, the code sent from the host is compared with the control code and ID code in the ROM to determine whether they match, and reading/programming/erasure will be enabled only when the two match.
The control code and ID code in the ROM consists of four 32-bit words. Figure 41.29 shows the configuration of the control code and ID code. The ID code should be set in 32-bit units.

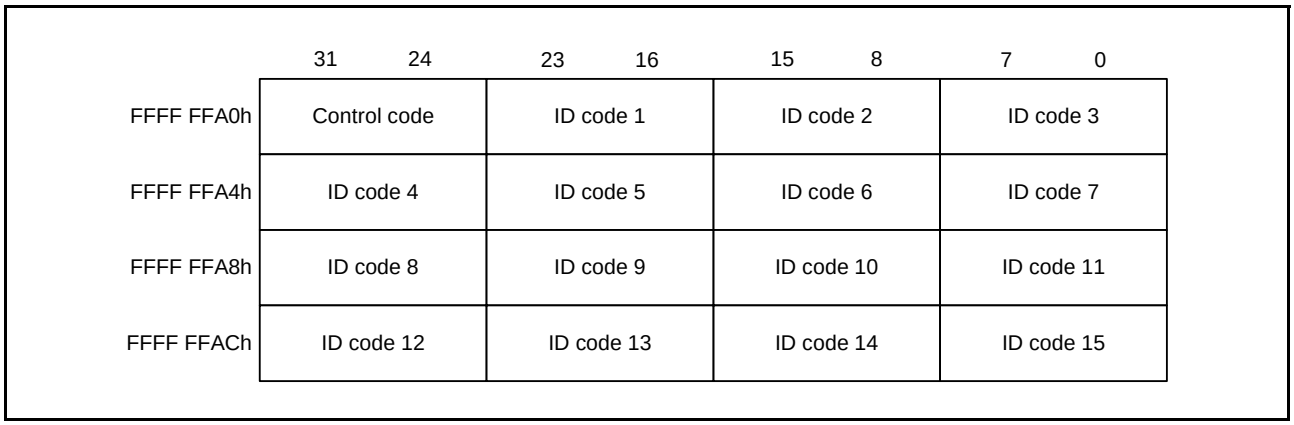


Figure 41.29 Configuration of Control Code and ID Code in ROM

(1) Control Code

The control code determines whether ID code protection is enabled or disabled and the method of authentication to use with the host. Table 41.15 lists how the control code determines the method of authentication.

Table 41.15 Specifications for ID Code Protection

Control Code	ID Code	State of Protection	Operations at the Time of SCI Connection
45h	As desired	Protection enabled (authentication method 1)	Matching ID code: The command wait is entered. Non-matching ID code: The ID code protection wait is entered again. However, if a non-matching ID code is received three times in a row, all blocks are erased.
52h	Sequences other than 50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, ..., FFh	Protection enabled (authentication method 2)	Matching ID code: The command wait is entered. Non-matching ID code: The ID code protection wait is entered again.
	50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, ..., FFh	Protection enabled (authentication method 3)	Always judged to be a non-matching ID code.
Other than above	—	Protection disabled	All blocks are erased.

(2) ID Code

The ID code can be set to any desired value. However, if the control code is 52h and the ID code is 50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, ..., FFh (from the ID code 1 field), there is no determination of matching and the ID code is always considered to be non-matching. Accordingly, reading, programming, and erasure from the host are prohibited.

(3) Program Example for ID Code Setting

The following assembler directives set up a control code of 45h and an ID code of 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh (from the ID code 1 field).

```
.SECTION  ID_CODE,CODE
.ORG  0FFFFFFA0h
.LWORD  45010203h
.LWORD  04050607h
.LWORD  08090A0Bh
.LWORD  0C0D0E0Fh
```

41.8.5 UB Code A

For the UB Code A, see section 8.3, UB Codes.

41.8.6 Configuration of Commands and Responses

Communications between the host and this MCU in boot mode consist of commands sent by the host and responses sent as replies from this MCU.
The notation “SUM” in descriptions of commands means the checksum, in the case of the total of the bytes transmitted by this MCU, and byte data for which the total becomes 00h is indicated. “Size” indicates the size of the command from the byte where it starts, and is the number of bytes transmitted or received other than the SUM byte.

Moreover, if the host has sent an undefined command, this MCU returns a response indicating a command error in the format shown below. The command field holds the first byte of the undefined command sent from the host.

Error response	80h	Command

41.8.7 Inquiry/Selection Command Wait

Table 41.16 lists the commands available in the inquiry/selection command wait. The boot program status inquiry command can also be used in the programming/erasure command wait. The other commands can only be used in the inquiry/selection command wait.

Table 41.16 Inquiry/Selection Commands

Host Command Name	Function
Supported device inquiry	Inquires regarding the device codes and the series name
Device selection	Selects a device code
Clock mode inquiry	Inquires regarding the number of clock modes and their values
Clock mode selection	Notifies the selected clock mode
Multiplication ratio inquiry	Inquires regarding the number of clock types, the number of multiplication/division ratios, and the multiplication /division ratios
Operating frequency inquiry	Inquires regarding the number of clock types and the maximum and minimum operating frequencies
User boot area information inquiry	Inquires regarding the number of user boot area and the start and end addresses
User area information inquiry	Inquires regarding the number of user area and the start and end addresses
Block information inquiry	Inquires regarding the number of blocks and the start and end addresses
Programming size inquiry	Inquires regarding the size of programming data
Data area inquiry	Inquires regarding the availability of data area
Data area information inquiry	Inquires regarding the number of data areas and the start and end addresses
New bit rate selection	Modifies the bit rate of SCI communications between the host and this MCU
Programming/erasure state transition	Enters the state for determining ID code protection
Boot program status inquiry	Inquires regarding the processing state

In the inquiry/selection command wait, send selection commands from the host in the order of device selection, clock mode selection, and new bit rate selection to set up this MCU according to the responses to inquiry commands. Note that the supported device inquiry and clock mode inquiry commands are the only inquiry commands that can be sent before the clock mode selection command; other inquiry commands must not be issued before the clock mode selection command. If commands are issued in an incorrect order, this MCU returns a response indicating a command error. Figure 41.30 shows an example of the procedure to use commands in the inquiry/selection command wait.

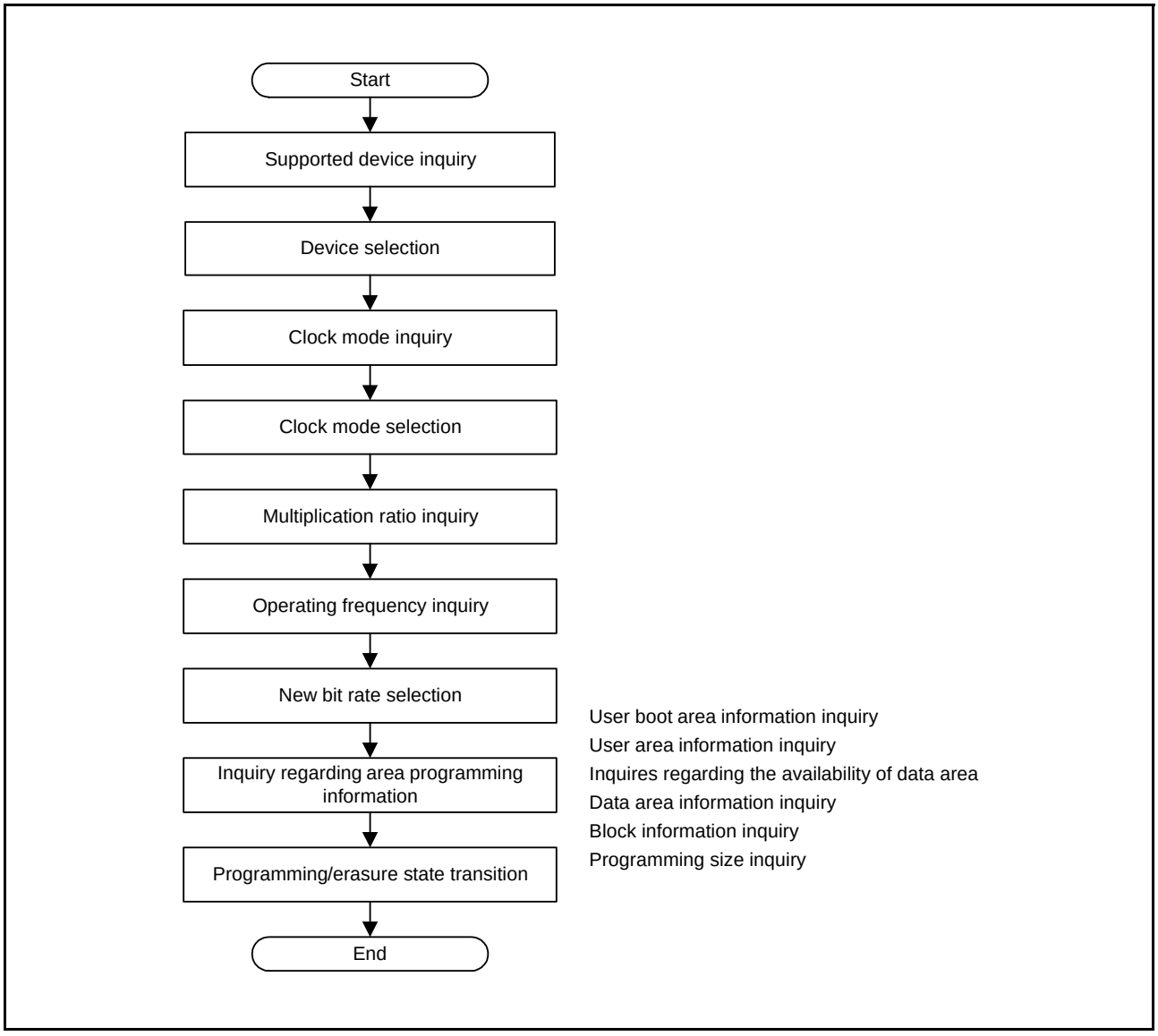


Figure 41.30 Example of Procedure to Use Inquiry/Selection Commands

(1) Supported Device Inquiry

In response to a supported device inquiry command sent from the host, this MCU returns the information concerning the devices supported by the boot program for boot mode. If the supported device inquiry command comes after the host has selected a device, this MCU only returns the information concerning the selected device. In response to supported device inquiry commands, this MCU transmits two sets of device information in turn, one in little endian and the other in big endian.

Command	20h			
Response	30h	Size	Device count	
	Character count	Device code (little endian is specified)		Series name
	Character count	Device code (big endian is specified)		Series name
	SUM			

Size (1 byte):	Total number of bytes in the device count, character count, device code, and series name fields
Device count (1 byte):	Number of device types supported by the boot program for boot mode
Character count (1 byte):	Number of characters included in the device code and series name fields
Device code (4 bytes):	Chip recognition code
Series name (n bytes):	ASCII code for the supported device
SUM (1 byte):	Checksum

(2) Device Selection

In response to a device selection command sent from the host, this MCU checks if the selected device is supported. When the selected device is supported, this MCU and returns a response (06h). If the selected device is not supported or the sent command is illegal, this MCU returns an error response (90h).

Select the device code with the endian specification from the two sets of device information transmitted in response to a supported device inquiry command in accord with the written data.

Command	10h	Size	Device code	SUM
Response	06h			
Error response	90h	Error		

Size (1 byte):	Number of characters in the device code field (fixed at 4)
Device code (4 bytes):	ASCII code for the series name of the chip (same code as the response to the supported device inquiry command)
SUM (1 byte):	Checksum
Error (1 byte):	Error code 11h: Checksum error (illegal command) 21h: Device code error

(3) Clock Mode Inquiry

In response to a clock mode inquiry command sent from the host, this MCU returns the supported clock modes. If the clock mode inquiry command comes after the host has selected a clock mode, this MCU only returns the information concerning the selected clock mode.

Command	21h	
Response	31h	Size
	Mode	
	SUM	

Size (1 byte): Total number of bytes in the mode count and mode fields

Mode (1 byte): Supported clock mode (for example, 01h indicates clock mode 1)

SUM (1 byte): Checksum

(4) Clock Mode Selection

In response to a clock mode selection command sent from the host, this MCU checks if the selected clock mode is supported. When the selected mode is supported, this MCU specifies this clock mode for use and returns a response (06h). If the selected mode is not supported or the sent command is illegal, this MCU returns an error response (91h). Be sure to issue a clock mode selection command only after issuing a device selection command. Even when 00h or 01h has been returned as the number of supported clock modes in response to a clock mode inquiry command, issue a clock mode selection command to specify the clock mode that has been returned as the result of the inquiry.

Command	11h	Size	Mode	SUM
Response	06h			
Error response	91h	Error		

Size (1 byte): Number of characters in the mode field (fixed at 1)

Mode (1 byte): Clock mode (same mode as the response to the clock mode inquiry command)

SUM (1 byte): Checksum

Error (1 byte): Error code
11h: Checksum error (illegal command)
22h: Clock mode error

(5) Multiplication Ratio Inquiry

In response to a multiplication ratio inquiry command sent from the host, this MCU returns the clock types, the number of multiplication/division ratios, and the multiplication division ratios supported.

Command

22h

Response

32h	Size	Clock type count		
Multiplication ratio count	Multiplication ratio	Multiplication ratio	. . .	Multiplication ratio
Multiplication ratio count	Multiplication ratio	Multiplication ratio	. . .	Multiplication ratio
SUM				

Size (1 byte):	Total number of bytes in the clock type count, multiplication ratio count, and multiplication ratio fields
Clock type count (1 byte):	Number of clock types (for example, 02h indicates two clock types; that is, a system clock and a peripheral clock)
Multiplication ratio count (1 byte):	Number of supported multiplication/division ratios (for example, 04h indicates that four multiplication ratios are supported for the system clock (multiplied by 1, multiplied by 2, multiplied by 4, and multiplied by 8)
Multiplication ratio (1 byte):	A positive value indicates a multiplication ratio (for example, 04h = 4 = multiplied by 4) A negative value indicates a division ratio (for example, FEh = –2 = divided by 2)
SUM (1 byte):	Checksum

(6) Operating Frequency Inquiry

In response to an operating frequency inquiry command sent from the host, this MCU returns the minimum and maximum operating frequencies for each clock.

Command

23h

Response

33h	Size	Clock type count
Minimum frequency		Maximum frequency
Minimum frequency		Maximum frequency
SUM		

Size (1 byte):	Total number of bytes in the clock type count, minimum frequency, and maximum frequency fields
Clock type count (1 byte):	Number of clock types (for example, 02h indicates two clock types; that is, a system clock and a peripheral clock)
Minimum frequency (2 bytes):	Minimum value of the operating frequency (for example, 07D0h indicates 20.00 MHz). This value should be calculated by multiplying the frequency value (MHz) to two decimal places by 100.
Maximum frequency (2 bytes):	Maximum value of the operating frequency This value is represented in the same format as the minimum frequency
SUM (1 byte):	Checksum

(7) User Boot Area Information Inquiry

In response to a user boot area information inquiry command sent from the host, this MCU returns the number of user boot areas and their addresses.

Command	24h		
Response	34h	Size	Area count
	Area start address		
	Area end address		
	SUM		

Size (1 byte):	Total number of bytes in the area count, area start address, and area end address fields
Area count (1 byte):	Number of user boot areas (consecutive areas are counted as one area)
Area start address (4 bytes):	Start address of a user boot area
Area end address (4 bytes):	End address of a user boot area
SUM (1 byte):	Checksum

(8) User Area Information Inquiry

In response to a user area information inquiry command sent from the host, this MCU returns the number of user areas and their addresses.

Command	25h		
Response	35h	Size	Area count
	Area start address		
	Area end address		
	SUM		

Size (1 byte):	Total number of bytes in the area count, area start address, and area end address fields
Area count (1 byte):	Number of user areas (consecutive areas are counted as one area)
Area start address (4 bytes):	Start address of a user area
Area end address (4 bytes):	End address of a user area
SUM (1 byte):	Checksum

(9) Block Information Inquiry

In response to a block information inquiry command sent from the host, this MCU returns the number of total erasure blocks in the user area and data area, and their addresses.

Command	26h		
Response	36h	Size	Block count
	Block start address		
	Block end address		
	Block start address		
	Block end address		
	. . .		
	Block start address		
	Block end address		
	SUM		

Size (2 bytes):	Total number of bytes in the block count, block start address, and block end address fields
Block count (1 byte):	Number of erasure blocks in the user area
Block start address (4 bytes):	Start address of an erasure block
Block end address (4 bytes):	End address of an erasure block
SUM (1 byte):	Checksum

(10) Programming Size Inquiry

In response to a programming size inquiry command sent from the host, this MCU returns the programming size.

Command	27h			
Response	37h	Size	Programming size	SUM

Size (1 byte):	Number of characters included in the programming size field (fixed at 2)
Programming size (2 bytes):	Programming unit (bytes)
SUM (1 byte):	Checksum

(11) Data Area Inquiry

In response to a data area inquiry command sent from the host, this MCU returns the information concerning the availability of data areas.

Command	2Ah			
Response	3Ah	Size	Area availability	SUM

Size (1 byte):	Number of characters in the area availability field (fixed at 1)
Area availability (1 byte):	Availability of data areas (fixed at 21h) 21h: Data area is available
SUM (1 byte):	Checksum

(12) Data Area Information Inquiry

In response to a data area information inquiry command sent from the host, this MCU returns the number of data area counts and their addresses.

Command	2Bh		
Response	3Bh	Size	Area count
	Area start address		
	Area end address		
	SUM		

Size (1 byte):	Total number of bytes in the area count, area start address, and area end address fields
Area count (1 byte):	Number of data area counts (consecutive areas are counted as one area)
Area start address (4 bytes):	Start address of a data area
Area end address (4 bytes):	End address of a data area
SUM (1 byte):	Checksum

The information concerning the block configuration in the data area is included in the response to the block information inquiry command (see section 41.8.7, Inquiry/Selection Command Wait).

(13) New Bit Rate Selection

In response to a new bit rate selection command sent from the host, this MCU checks if the on-chip SCI can be set to the selected new bit rate. When the SCI can be set to the new bit rate, this MCU returns a response (06h) and sets the SCI to the new bit rate. If the SCI cannot be set to the new bit rate or the sent command is illegal, this MCU returns an error response (BFh). Upon reception of response 06h, the host waits for a one-bit period in the previous bit rate with which the new bit rate selection command has been sent, and then sets the host's bit rate to the new one. After that, the host sends confirmation data (06h) in the new bit rate, and this MCU returns a response (06h) for the confirmation data.
Be sure to issue a new bit rate selection command only after a clock mode selection command.

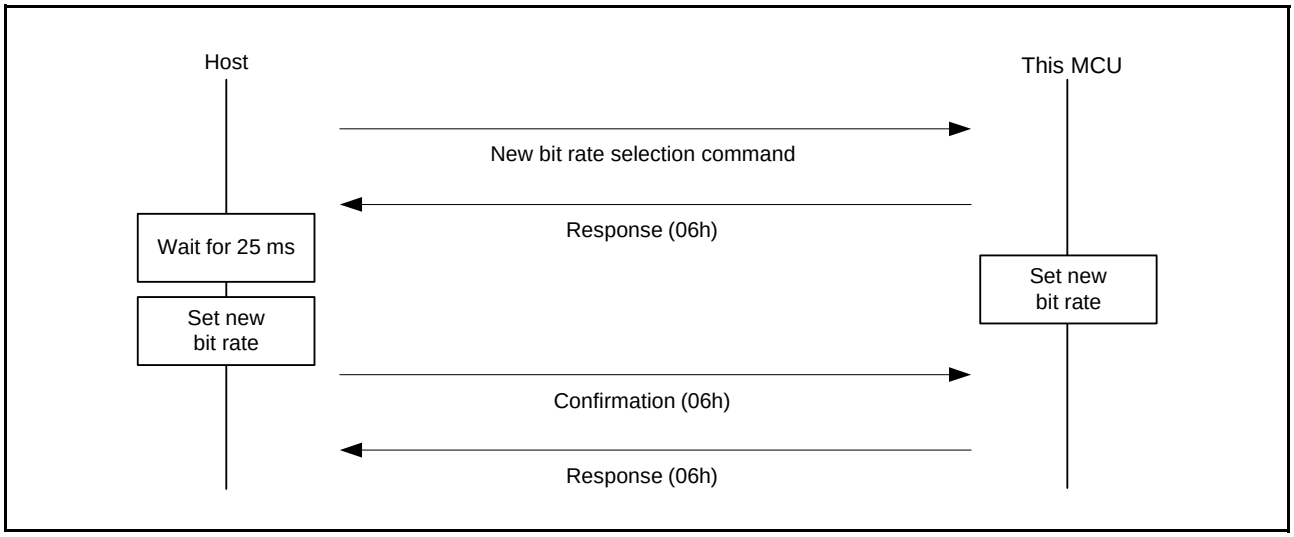


Figure 41.31 New Bit Rate Selection Sequence

Command	3Fh	Size	Bit rate	Input frequency
	Clock type count	Multiplication ratio 1	Multiplication ratio 2	
	SUM			
Response	06h			
Error response	BFh	Error		
Confirmation	06h			
Response	06h			

Size (1 byte):	Total number of bytes in the bit rate, input frequency, clock type count, and multiplication ratio fields
Bit rate (2 bytes):	New bit rate (for example, 00C0h indicates 19200 bps) 1/100 of the new bit rate value should be specified.
Input frequency (2 bytes):	Frequency input to this MCU (for example, 04E2h indicates 12.50 MHz) This value should be calculated by multiplying the input frequency value to two decimal places by 100.
Clock type count (1 byte):	Number of clock types (fixed: 02h indicates two clock types; that is, a system clock and a peripheral clock)
Multiplication ratio 1 (1 byte):	Multiplication/division ratio of the input frequency to obtain the system clock (ICLK) A positive value indicates a multiplication ratio (for example, 04h = 4 = multiplied by 4) A negative value indicates a division ratio (for example, FEh = –2 = divided by 2)
Multiplication ratio 2 (1 byte):	Multiplication/division ratio of the input frequency to obtain the peripheral clock (PCLK) This value is represented in the same format as multiplication ratio 1
SUM (1 byte):	Checksum
Error:	Error code 11h: Checksum error 24h: Bit rate selection error 25h: Input frequency error 26h: Multiplication ratio error 27h: Operating frequency error

- Bit rate selection error

A bit rate selection error occurs when the bit rate selected through a new bit rate selection command cannot be set for the SCI of this MCU within an error of 4%. The bit rate error can be obtained by the following equation from the bit rate (B) selected through a new bit rate selection command, the input frequency (f_{EX}), multiplication ratio 2 ($M_{P\phi}$), the bit rate register (BRR) setting (N) in the SCI, and the CKS[1:0] bit value (n) in the serial mode register (SMR).

$$\text{Error (\%)} = \{ \frac{f_{EX} \times M_{P\phi} \times 10^6}{B \times 64 \times 2^{2n-1} \times (N + 1)} - 1 \} \times 100$$

- Input frequency error

An input frequency error occurs when the input frequency specified through a new bit rate selection command is outside the range from the minimum to maximum input frequencies for the clock mode selected through a clock mode selection command.

- Multiplication ratio error

A multiplication ratio error occurs when the multiplication ratio specified through a new bit rate selection command does not match the clock mode selected through a clock mode selection command. To check the selectable multiplication ratios, issue a multiplication ratio inquiry command.

- Operating frequency error

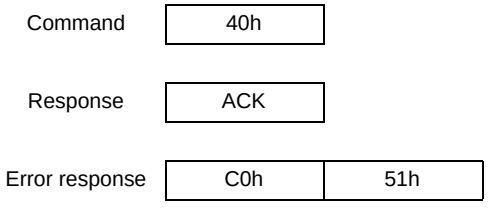
An operating frequency error occurs when this MCU cannot operate at the operating frequencies selected through a new bit rate selection command. This MCU calculates the operating frequencies from the input frequency and multiplication ratios specified through a new bit rate selection command and checks if each calculated frequency is within the range from the minimum to maximum frequencies for the respective clock. To check the minimum and maximum operating frequencies for each clock, issue an operating frequency inquiry command.

(14) Programming/Erasure State Transition

In response to a programming/erasure state transition command sent from the host, this MCU determines whether ID code protection is enabled or disabled using the control code and ID code written in the ROM. When ID code protection is enabled, this MCU returns a response (16h) and waits for the ID code. When ID code protection is disabled, this MCU erases the entire area of each of the user area, user boot area and data area.*1 After completing entire erasure, this MCU returns a response (26h) and waits for a programming/erasure command. If this MCU has failed to complete erasure due to an error, it returns an error response (C0h, and 51h).

Do not issue a programming/erasure state transition command before the device selection, clock mode selection, and new bit rate selection commands.

Note 1. The user-boot area is not erased if it holds a USB boot program.



ACK (1 byte): ACK code
26h: ID code protection is disabled
16h: ID code protection is enabled

(15) Boot Program Status Inquiry

In response to a boot program status inquiry command sent from the host, this MCU returns its current status. The boot program status inquiry command can be issued in both the inquiry/selection command wait and programming/erasure command wait.

Command	4Fh				
Response	5Fh	Size	Status	Error	SUM

Size (1 byte): Total number of bytes in the status and error fields (fixed at 2)
Status (1 byte): Current status of this MCU (see Table 41.17)
Error (1 byte): Error status of this MCU (see Table 41.18)
SUM (1 byte): Check sum

Table 41.17 Status Code

Code	Description
11h	Waiting for device selection
12h	Waiting for clock mode selection
13h	Waiting for bit rate selection
1Fh	Waiting for transition to programming/erasure command wait (bit rate has been selected)
31h	Erasing the user area/user boot area
3Fh	Waiting for a programming/erasure command
4Fh	Waiting for reception of programming data
5Fh	Waiting for erasure block specification

Table 41.18 Error Code

Code	Description
00h	No error
11h	Checksum error
21h	Device code error
22h	Clock mode error
24h	Bit rate selection error
25h	Input frequency error
26h	Multiplication ratio error
27h	Operating frequency error
29h	Block number error
2Ah	Address error
2Bh	Data size error
51h	Erasure error
52h	Incomplete erasure error
53h	Programming error
54h	Selection error
80h	Command error
FFh	Bit rate adjustment confirmation error

41.8.8 ID Code Wait State

Table 41.19 shows the command available in the ID code wait state.

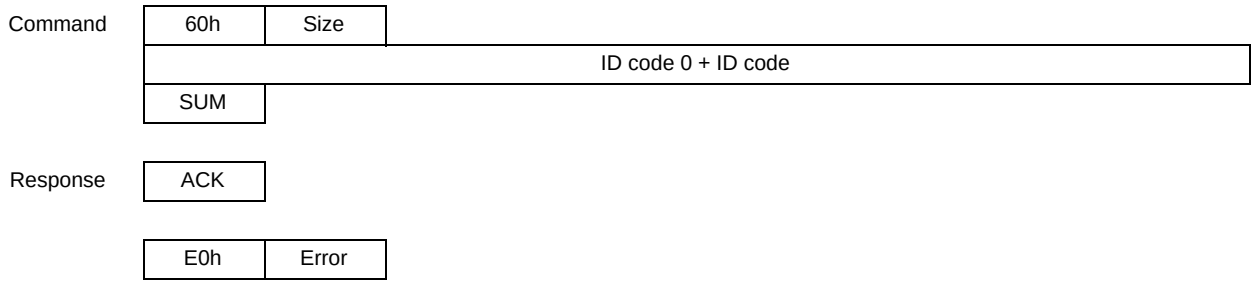
Table 41.19 ID Code Check Command

Command Name	Function
ID code check	Performs the ID code check

If the host has sent an undefined command, this MCU returns a response indicating a command error. For the contents of a command error, see section 41.8.7, Inquiry/Selection Command Wait.

(1) ID Code Check

In response to an ID code check command sent from the host, this MCU compares the code sent from the host with the control code and ID code in the ROM and returns the result.



Size (1 byte): Number of bytes in the ID code field (fixed at 16)

ID code (16 bytes): ID code 0 (1 byte) + ID code (15 bytes)

SUM (1 byte): Checksum

ACK (1 byte): ACK code
26h: Returns the response for a programming/erasure state transition command

Error (1 byte): Error code
11h: Checksum error
61h: ID code mismatch
63h: ID code mismatch (erasure error)
An error has occurred during erasure triggered by an ID code mismatch.

41.8.9 Programming/Erasure Command Wait

Table 41.20 lists the commands available in the programming/erasure command wait.

Table 41.20 Programming/Erasure Commands

Command Name	Function
User boot area programming selection	Selects the program for user boot area programming
User/data area programming selection	Selects the program for user/data area programming
256-byte programming	Programs 256 bytes of data
Erasure selection	Selects the erasure program
Block erase	Erases block data
Memory read	Reads data from memory
User boot area checksum	Performs checksum verification for the user boot area
User area checksum	Performs checksum verification for the user area
Data area checksum	Performs checksum verification for the data area
User boot area blank check	Checks whether the user boot area is blank
User area blank check	Checks whether the user area is blank
Data area blank check	Checks whether the data area is blank
Read lock bit status	Reads from the lock bit
Lock bit program	Writes to the lock bit
Lock bit enable	Enables the lock bit protection
Lock bit disable	Disables the lock bit protection
Boot program status inquiry	Inquires regarding the state of the this MCU

If the host has sent an undefined command, this MCU returns a response indicating a command error. For the contents of a command error, see section 41.8.7, Inquiry/Selection Command Wait.
To program the ROM, issue a programming selection command (user area/data programming selection, user boot area programming selection) and then a 256-byte programming command from the host. To program the DataFlash, issue a user/data area programming selection command and then a 256-byte programming command specifying a data area address as the programming address. Upon reception of a programming selection command, this MCU enters the programming data wait state (see section 41.8.2, State Transitions in Boot Mode). In response to a 256-byte programming command sent from the host in this state, this MCU starts programming the ROM/E2 DataFlash. When the host sends a 256-byte programming command specifying FFFF FFFFh as the programming start address, this MCU detects it as the end of programming and enters the programming/erasure command wait.
To erase the ROM/E2 DataFlash, issue an erasure selection command and then a block erase command from the host. Upon reception of an erasure selection command, this MCU enters the erasure block selection wait state (see section 41.8.2, State Transitions in Boot Mode). In response to a block erase command sent from the host in this state, this MCU erases the specified block in the ROM/E2 DataFlash. When the host sends a block erase command specifying FFh as the block number, this MCU detects it as the end of erasure and enters the programming/erasure command wait.
To read data from the data area, select the user area through a memory read command specifying a data area address as the read address.

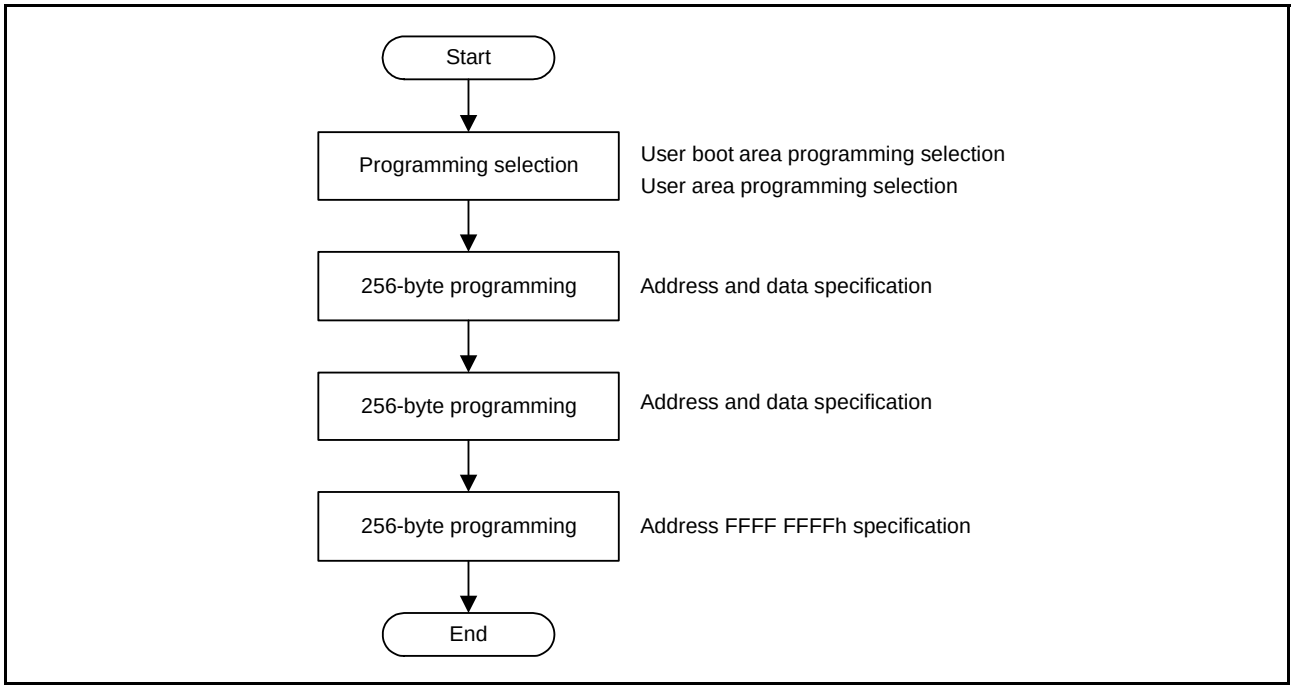


Figure 41.32 Procedure for ROM/E2 DataFlash Programming in Boot Mode

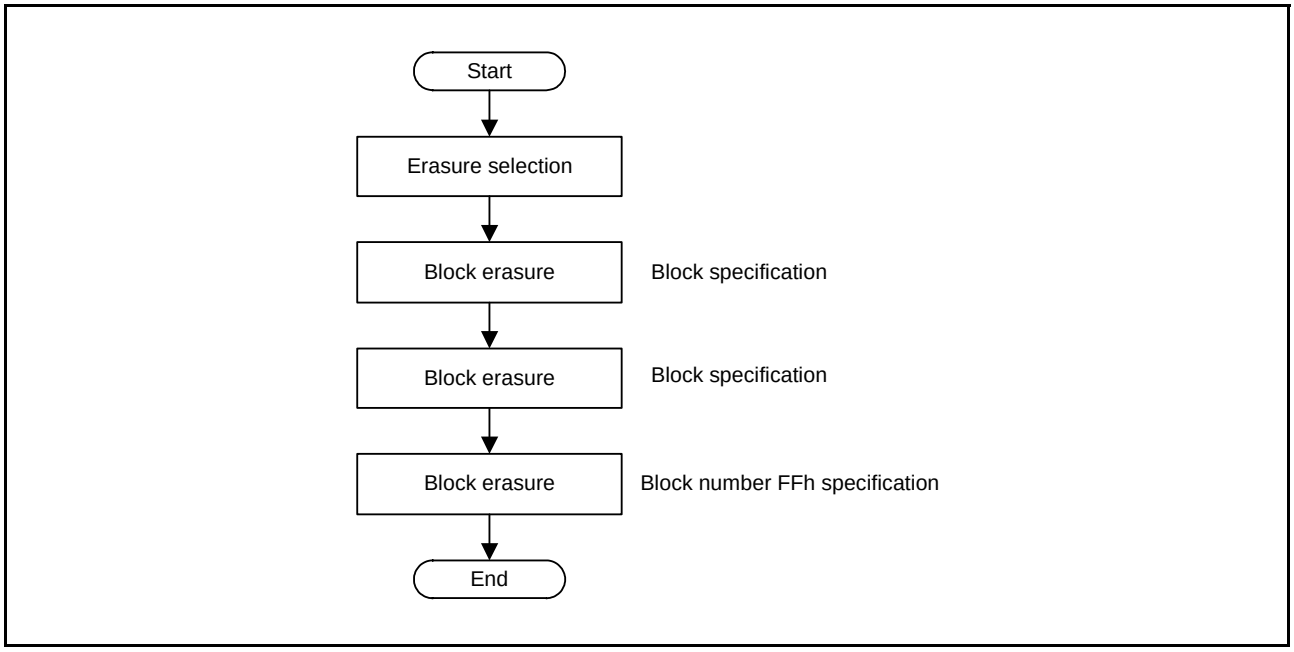


Figure 41.33 Procedure for ROM/E2 DataFlash Erasure in Boot Mode

Each command is described in detail below. The “command” in the description indicates a command sent from the host to this MCU and the “response” indicates a response sent from this MCU to the host. The “checksum” is byte-size data calculated so that the sum of all bytes to be sent by this MCU becomes 00h.

(1) User Boot Area Programming Selection

In response to a user boot area programming selection command sent from the host, this MCU selects the program for user boot area programming and waits for programming data.

Command	42h
Response	06h

(2) User/Data Area Programming Selection

In response to a user/data area programming selection command sent from the host, this MCU selects the program for user area programming and waits for programming data. To program the E2 DataFlash, issue a user/data area programming selection command.

Command	43h
Response	06h

(3) 256-Byte Programming

In response to a 256-byte programming command sent from the host, this MCU programs the ROM/E2 DataFlash. After completing ROM/E2 DataFlash programming successfully, this MCU returns a response (06h). If an error has occurred during ROM programming, this MCU returns an error response (D0h).

Command	50h	Programming address		
	Data	Data	. . .	Data
	SUM			
Response	06h			
Error response	D0h	Error		

Programming address (4 bytes):	Target address of programming To execute programming, a 256-byte boundary address should be specified. To terminate programming, FFFF FFFFh should be specified.
Data (256 bytes):	Programming data FFh should be specified for the bytes that do not need to be programmed. When terminating programming, no data needs to be sent (only the programming address and SUM should be sent in that order).
SUM (1 byte):	Checksum
Error (1 byte):	Error code 11h: Checksum error 2Ah: Address error (the specified address is not in the target area) 53h: Programming cannot be done due to a programming error

(4) Erasure Selection

In response to an erasure selection command sent from the host, this MCU selects the erasure program and waits for erasure block specification.

Command	48h
Response	06h

(5) Block Erasure

In response to a block erase command sent from the host, this MCU erases the ROM/E2 DataFlash. When erasing the user boot area, 80h should be specified as the block number. After completing ROM/E2 DataFlash erasure successfully, this MCU returns a response (06h). If an error has occurred during ROM/E2 DataFlash erasure, this MCU returns an error response (D8h).

Command	58h	Size	Block	SUM
Response	06h			
Error response	D8h	Error		

Size (1 byte):	Number of bytes in the block specification field (fixed at 1)
Block (1 byte):	Block number whose data is to be erased To specify user boot area, 80h should be specified. To terminate erasure, FFh should be specified.
SUM (1 byte):	Checksum
Error (1 byte):	Error code 11h: Checksum error 29h: Block number error (an incorrect block number is specified) 51h: Erasure cannot be done due to an erasure error

(6) Memory Read

In response to a memory read command sent from the host, this MCU reads data from the ROM/E2 DataFlash. After completing ROM/E2 DataFlash reading successfully, this MCU returns the data stored in the address specified by the memory read command. If this MCU has failed to read the ROM/E2 DataFlash, this MCU returns an error response (D2h).

Command	52h	Size	Area	Read start address	
	Reading size			SUM	

Response	52h	Reading size			
	Data	Data	. . .	Data	
	SUM				

Error response	D2h	Error

Size (1 byte):	Total number of bytes in the area, read start address, and reading size fields
Area (1 byte):	Target area to be read 00h: User boot area 01h: User area, data area
Read start address (4 bytes):	Start address of the area to be read
Reading size (4 bytes):	Size of data to be read (bytes)
SUM (1 byte):	Checksum
Data (1 byte):	Data read from the ROM/E2 DataFlash
Error (1 byte):	Error code 11h: Checksum error 2Ah: Address error • The value specified for area selection is neither 00h nor 01h. • The specified read start address is outside the selected area. 2Bh: Data size error • 00h is specified for the reading size. • The reading size is larger than the area. • The end address calculated from the read start address and the reading size is outside the selected area.

(7) User Boot Area Checksum

In response to a user boot area checksum command sent from the host, this MCU sums the user boot area data in byte units and returns the result (checksum).

Command	4Ah			
Response	5Ah	Size	Area checksum	SUM

Size (1 byte):	Number of bytes in the area checksum field (fixed at 4)
Area checksum (4 bytes):	Checksum of the user boot area data
SUM (1 byte):	Checksum (for the response data)

(8) User Area Checksum

In response to a user area checksum command sent from the host, this MCU sums the user area data in byte units and returns the result (checksum).

Command	4Bh			
Response	5Bh	Size	Area checksum	SUM

Size (1 byte): Number of bytes in the area checksum field (fixed at 4)

Area checksum (4 bytes): Checksum of the user area data
The user area also stores the key code for debugging function authentication. Note that the checksum includes this key code value.

SUM (1 byte): Checksum (for the response data)

(9) Data Area Checksum

In response to a data area checksum command sent from the host, this MCU sums the data area data in byte units and returns the result (checksum).

Command	61h			
Response	71h	Size	Area checksum	SUM

Size (1 byte): Number of bytes in the area checksum field (fixed at 4)

Area checksum (4 bytes): Checksum of the data area

SUM (1 byte): Checksum (for the response data)

(10) User Boot Area Blank Check

In response to a user boot area blank check command sent from the host, this MCU checks whether the user boot area is completely erased. When the user boot area is completely erased, this MCU returns a response (06h). If the user boot area has an unerased area, this MCU returns an error response (CCh, 52h).

Command	4Ch	
Response	06h	
Error response	CCh	52h

(11) User Area Blank Check

In response to a user area blank check command sent from the host, this MCU checks whether the user area is completely erased. When the user area is completely erased, this MCU returns a response (06h). If the user area has an unerased area, this MCU returns an error response (CDh, 52h).

Command	4Dh	
Response	06h	
Error response	CDh	52h

(12) Data Area Blank Check

In response to a data area blank check command sent from the host, this MCU checks whether the data area is completely erased. When the data area is completely erased, this MCU returns a response (06h). If the data area has an unerased area, this MCU returns an error response (E2h, 52h).

Command	62h	
Response	06h	
Error response	E2h	52h

(13) Read Lock Bit Status

In response to a read lock bit status command sent from the host, this MCU reads data from the lock bit. After completing the lock bit reading successfully, this MCU returns the data stored in the address specified by the read lock bit status command. If this MCU has failed to read the lock bit, this MCU returns an error response (F1h).

Command	71h	Size	Area	A15 to A8	A23 to A16	A31 to A24	SUM

A15 to A8 (1 byte): The last address in the specified block (bits 15 to 8)
A23 to A16 (1 byte): The last address in the specified block (bits 23 to 16)
A31 to A24 (1 byte): The last address in the specified block (bits 31 to 24)

Response	Status	
Error response	F1h	Error

Size (1 byte):	Total number of bytes in the area, A15 to A8, A23 to A16, and A31 to A24 (fixed at 4 in this MCU)
Area (1 byte):	Target area to be read 01h: User area
A15 to A8 (1 byte):	A15 to A8 of the last address in the specified block (bits 8 to 15)
A23 to A16 (1 byte):	A23 to A16 of the last address in the specified block (bits 16 to 23)
A31 to A24 (1 byte):	A31 to A24 of the last address in the specified block (bits 24 to 31)
SUM (1 byte):	Checksum
Status (1 byte):	Bit 6 locked at 0 Bit 6 unlocked at 1
Error (1 byte):	Error code 11h: Checksum error 2Ah: Address error (the specified address is not in the target area)

(14) Lock Bit Program

In response to a lock bit program command sent from the host, this MCU writes to a lock bit and locks the specified block. After completing the lock bit blocking successfully, this MCU returns a response (06h). If this MCU has failed to lock, this MCU returns an error response (F7h).

Command	77h	Size	Area	Third highest order address	Second highest order address	Highest order address	SUM
Response	06h						
Error response	F7h	Error					

Size (1 byte):	Total number of bytes in the area, third highest order address, second highest order address, and highest order address fields (fixed at 4 in this MCU)
Area (1 byte):	Target area to be locked 01h: User area
Third highest order address (1 byte):	Third highest order address at the specified block's end address (8 to 15 bits)
Second highest order address (1 byte):	Second highest order address at the specified block's end address (16 to 23 bits)
Highest order address (1 byte):	Highest order address at the specified block's end address (24 to 31 bits)
SUM (1 byte):	Checksum
Error (1 byte):	Error code 11h: Checksum error 2Ah: Address error (the specified address is not in the target area) 53h: Lock cannot be done due to a programming error

(15) Lock Bit Enable

In response to a lock bit enable command sent from the host, this MCU enables a lock bit.

Command	7Ah
Response	06h

(16) Lock Bit Disable

In response to a lock bit disable command sent from the host, this MCU disables a lock bit.

Command	75h
Response	06h

(17) Boot Program Status Inquiry

For details, refer to section 41.8.7, Inquiry/Selection Command Wait.

41.9 USB Boot Mode

In USB boot mode, the user area is programmed or erased by control commands and data for programming transmitted from an externally connected host via the USB.

Using USB boot mode requires preparation on the host side of tools for transmitting the control commands and data for programming, and of the data. Figure 41.34 shows the configuration of a system for use in USB boot mode. Interrupt requests generated in USB boot mode are ignored. Ensure that interrupt requests are not generated on the system side.

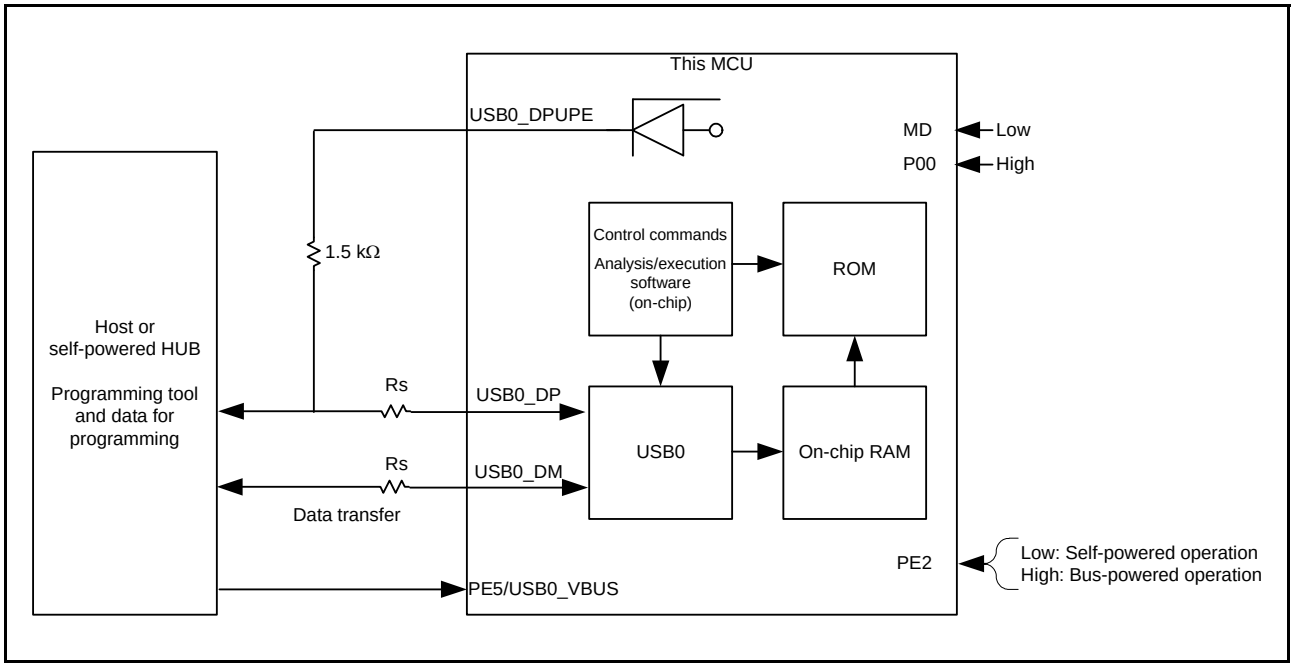


Figure 41.34 System Configuration in USB Boot Mode

41.9.1 Features

- Selection of bus-powered or self-powered mode
- Only the USB0_DPUPE pin is used for control of D+ pull-up connection
- See Table 41.21 for the enumeration information

Table 41.21 Enumeration Information

USB specification	Ver. 2.0 (Full-speed)	
Transfer modes	Control (in/out), Bulk (in/out)	
Maximum current	Self-powered mode (pin PE2 = 0)	100 mA
	Bus-powered mode (pin PE2 = 1)	500 mA
Endpoint configuration	EP0 Control (in out) 8 bytes Configuration1 └─InterfaceNumber0 └─AlternateSetting0 ├─EP1 Bulk (out) 64 bytes └─EP2 Bulk (in) 64 bytes	

41.9.2 State Transitions

State transitions after activation in USB boot mode are shown in Figure 41.35.

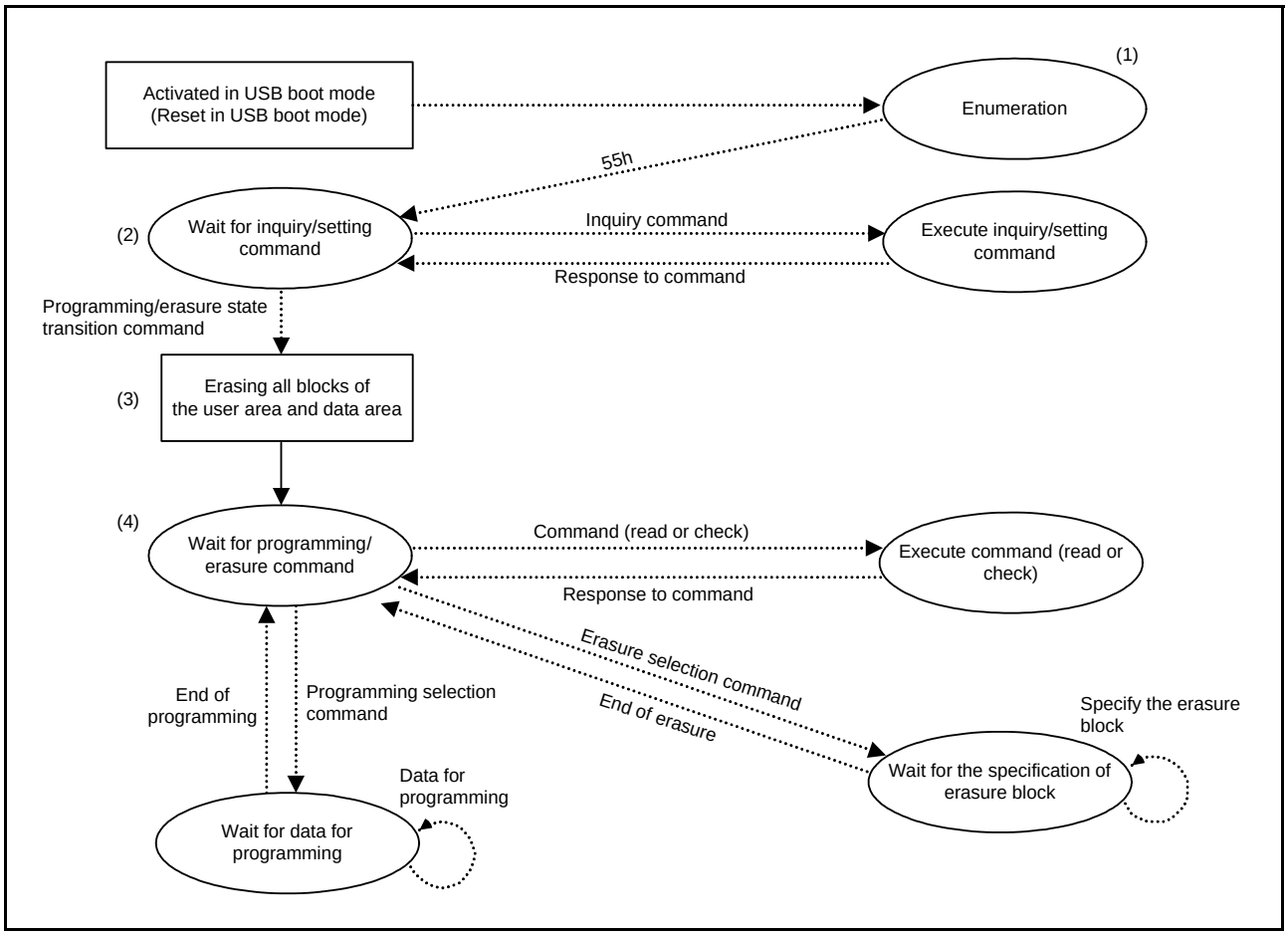


Figure 41.35 State Transitions in USB Boot Mode

(1) The USB boot program the device as shipped contains in the user boot area runs in the case of booting up in USB boot mode. The host sends a single byte with the value 55h to this MCU after enumeration between the host and this MCU. Reset this MCU if it does not send E6h in return.

(2) Inquiry data on the size, structure, first address, state of support, etc. of the user area are sent to the host.

(3) On completion of the inquiries, the whole user area is automatically erased.

(4) After automatic erasure of the user area, the state shifts to waiting for programming and erasure commands. When a programming selection command is received, the state shifts to waiting for data to be programmed. When an erasure-selection command is received, the state shifts to waiting for specification of blocks to be erased.
Other than the programming and erasure commands, commands for the following processes on the user area are also possible: checksum, blank checking, reading memory, and acquiring current status information.

41.9.3 Notes on Program Execution in USB Boot Mode

(1) In USB boot mode, a 12-MHz clock oscillator must be used and a 48-MHz clock signal must be provided to the USB module. Set the frequency of the external clock and clock oscillator so as the USB dedicated clock (UCLK) to be 48 MHz. Clock oscillators running at rates other than 12 MHz cannot be used in USB boot mode. For details, see section 10, Clock Generation Circuit.

(2) Use the USB0_DPUPE pin for controlling D+ pull-up connection.

(3) To ensure that the power supply is stable during programming and erasure of flash memory, do not connect a cable via a bus-powered HUB.

(4) Do not disconnect the USB cable during programming and erasure of flash memory. This may permanently damage the MCU circuit.

(5) Even if the USB bus enters the suspended mode in bus-powered mode, this MCU will not enter software standby mode (low-power consumption mode).

41.10 ID Code Protection on Connection of the On-Chip Debugger

This function is used to prohibit connection with the on-chip debugger. When connecting an on-chip debugger, the control code and ID code that have been written to the ROM are used to determine whether ID code protection on connection of the on-chip debugger is enabled or disabled and to judge ID code protection on connection of the on-chip debugger. When the ID code protection is enabled, the code sent from the on-chip debugger is compared with the control code and ID code in the ROM to determine whether they match. If they match, connection with the on-chip debugger is allowed. If they do not match, the on-chip debugger cannot be connected. However, if the control code is 52h and the ID code is 50h, 72h, 6Fh, 74h, 65h, 63h, and 74h (from the first to the seventh field of the ID code), this is always considered to be a non-match, judgment of the ID code does not proceed, and connection of the on-chip debugger is prohibited.

Furthermore, if all bytes of the control code and ID code have the value FFh, there is no determination of matching, the ID code is always considered to match, and connection of the on-chip debugger is allowed. See Figure 41.29 for the configuration of ID codes in flash memory.

Table 41.22 Specifications for ID Code Protection on Connection of the On-Chip Debugger

Control Code	ID Code	State of Protection	Operations at On-Chip Debugger Connection
FFh	FFh, …, FFh (all bytes FFh)	Protection disabled	The ID code always matches, and connection to the on-chip debugger is permitted.
52h	50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, …, FFh	Protection enabled	The ID code is always non-matching, and connection to the on-chip debugger is prohibited.
Other than above	Other than above	Protection enabled	Matching ID code: Authentication of the on-chip debugger is ended and connection with the on-chip debugger is permitted. Non-matching ID code: The ID code protection waiting state is entered again.

41.11 ROM Code Protection

ROM code protection is a facility for prohibiting a PROM programmer from reading from or programming flash memory. The ROM code in flash memory is a 32-bit code. Figure 41.36 shows the configuration of the ROM code. Set the ROM code in 32-bit units.
For release from ROM code protection, erase the EB00 block of the user area that contains the ROM code in boot mode or by user programming.

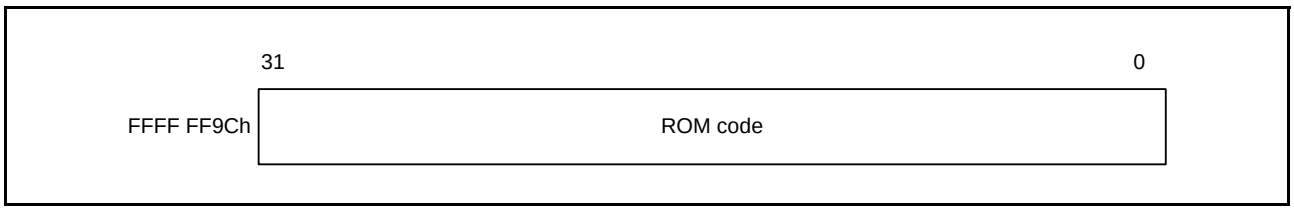


Figure 41.36 Configuration of ROM Code

Table 41.23 Specifications for ROM Code Protection

ROM Code	State of Protection	Operations at the Time of Connection with the PROM Programmer
0000 0000h	Protection enabled (ROM code protection 1)	Access (both reading and writing) to the user area and the user boot area are prohibited.
0000 0001h	Protection enabled (ROM code protection 2)	Reading from the user area and the user boot area are prohibited.
Other than above	Protection disabled	Access (both reading and writing) to the user area and the user boot area are permitted.

41.12 Usage Notes (Common to the ROM/E2 DataFlash Memory)

(1) Areas where Programming or Erasure is Suspended

Data in areas where programming or erasure is suspended are undefined. To avoid malfunctions due to the reading of undefined data, prevent the reading of data and execution of code from areas where programming or erasure is currently suspended.

(2) Suspending Programming or Erasure

If you use the programming/erasure suspension command to suspend the processing of programming or erasure, be sure to use the resume command so that the processing is completed.

(3) Prohibition of Reprogramming

Two or more programming operations cannot be performed for the same address range. If an address range that has already been programmed is to be programmed again, be sure to erase the area in advance of the programming.

(4) Reset during Programming, Erasure, or Blank Check

In case of the generation of a reset by the signal on the RES# pin during programming and erasure or blank checking, only de-assert the reset signal after it has remained within the range of operating voltage stipulated in the electrical characteristics over the period tRESWF (see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] and section 43, Electrical Characteristics [64- and 48-Pin Versions]).
In case of resetting of the FCU by the FRESETR.FRESET bit during programming and erasure or blank checking, maintain the reset state over the period tFCUR (see section 42, Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] and section 43, Electrical Characteristics [64- and 48-Pin Versions]).
During resetting of the FCU, do not read ROM that is the target of programming and erasure or blank checking.
Resets by the watchdog timer and watchdog timer and software resets during programming and erasure or blank checking can be used without securing the above periods.

(5) Prohibition of Non-Maskable Interrupts during Programming or Erasure

If a non-maskable interrupt (NMI pin interrupt, oscillation stop detection interrupt, WDT underflow, refresh error, IWDT underflow/refresh error, voltage-monitoring 1 interrupt or voltage-monitoring 2 interrupt) occurs during programming or erasure, as this will lead to fetching of the vector from the ROM, and the data read out will be undefined. Therefore, avoid a non-maskable interrupt being generated during programming or erasing in the ROM (this prohibition only applies to the ROM).

(6) Interrupt Vector Assignment During Programming, Erasure, or Blank Check

The generation of interrupts during programming, erasure, or blank check may lead to the fetching of vectors from the ROM. To prevent access to the ROM area due to the generation of interrupts, set the interrupt table register (INTB) of the CPU so that the destination for the fetching of interrupt vector is an area outside the ROM.

(7) Abnormal End during Programming, Erasure or Blank Check

In cases where programming and erasure or blank checking is not completed due to the operating voltage rising above the range stipulated in the electrical characteristics, a reset, the FCU being reset by using the FRESETR.FRESET bit, error detection leading to the flash memory being placed in the command-locked state, or one of the prohibitions under item (9), the lock bit may become 0 (indicating the protected state).
In such cases, erase the lock bit by issuing a block-erase command while the FPROTR.FPROTCN is 1. Redo programming that was not completed normally after that.

(8) Actions Prohibited during Programming, Erasure, or Blank Check

During programming, erasure, or blank check, high voltage is applied to the flash memory. In order to prevent damaging the flash memory, the following must be observed.

- Do not allow the input voltage to be below the operating voltage of this MCU.
- Do not change the value of the FWEPROR.FLWE[1:0] bits.
- Do not change the operating mode by the setting of the SYSCR0.ROME bit.
- Do not change the clock-source by setting of the SCKCR3.CKSEL[2:0] bits.
- Do not change the frequency dividing ratio for the FlashIF clock (FCLK).
- Do not make transition to all-module clock-stop mode, software standby mode, or deep software standby mode.

(9) Notes on Flash Programming in Boot Mode or USB Boot Mode

The main clock must be being input for programming of the flash memory in boot mode or USB boot mode. In the case of boot mode, a crystal oscillator within the range indicated in the electrical characteristics, must be connected between the XTAL and EXTAL pins. Connect a 12-MHz oscillator if operation is in USB boot mode.

(10) Handling of the EXTAL Pin in Boot Mode

When operation is in boot mode, provide a clock signal through connection of an external input or crystal oscillator to the EXTAL pin.

(11) Handling of the EXTAL Pin in USB Boot Mode

When operation is in USB boot mode, provide a 12-MHz clock signal through connection of a crystal oscillator to the EXTAL pin.

41.13 Usage Notes (for E2 DataFlash)

(1) Protection of Data Area Immediately after a Reset

As the initial values of DFLREy and DFLWEy (y = 0, 1) are 0000h, programming, erasure, and reading of the data area are disabled after a reset. To read data from the data area, set DFLREy appropriately before accessing the data area. To program or erase the data area, set DFLWEy appropriately before issuing an FCU command for programming or erasure. If an attempt is made to read, program, or erase the data area without setting the registers, the FCU detects the error and the FASTAT.CMDLK bit becomes 1 (the command-locked state).

42. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]

42.1 Absolute Maximum Ratings

Table 42.1 Absolute Maximum Ratings

Conditions: VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, PLLVCC	–0.3 to +6.5	V
USB power supply voltage		VCC_USB*1	–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC*2	–0.3 to +6.5	V
Reference power supply voltage		VREFH0*2	–0.3 to AVCC0 + 0.3	V
		VREF*2	–0.3 to AVCC0 + 0.3	V
Input voltage (except for ports 4 to 6, C, USB0_DP, and USB0_DM)		V_{in}	–0.3 to VCC + 0.3	V
Input voltage (USB0_DP and USB0_DM)		V_{in}	–0.3 to VCC_USB + 0.3	V
Input voltage (port 4)		V_{in}	–0.3 to AVCC0 + 0.3	V
Input voltage (ports 5, 6, and C)		V_{in}	–0.3 to AVCC + 0.3	V
Analog input voltage (port 4)		V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (ports 5, 6, and C)		V_{AN}	–0.3 to AVCC + 0.3	V
Operating temperature	D version product	T_{opr}	–40 to +85	ºC
	G version product	T_{opr}	–40 to +105	ºC
Storage temperature		T_{stg}	–55 to +125	ºC

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. When the USB is not in use, do not leave the VCC_USB and VSS_USB pins open.
Connect the VCC_USB pin to VCC, and the VSS_USB pin to VSS, respectively.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open.
- When the 12-bit A/D converter is not in use
  Connect the AVCC0 pin to AVCC, the VREFH0 pin to VREF, and the AVSS0 and VREFL0 pins to AVSS, respectively.
- When the 10-bit A/D converter is not in use
  Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0, respectively.
- When the 12-bit A/D converter and 10-bit A/D converter are not in use
  Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS, respectively.

42.2 DC Characteristics

Table 42.2 DC Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin GPT input pin RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (IICBus operating)	V_{IH}	VCC × 0.7	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	USB0_VBUS input pin	V_{IH}	VCC × 0.7	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	Port 4*1 (also used as an analog port)	V_{IH}	AVCC0 × 0.8	—	AVCC0 + 0.3		
		V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports 5, 6, and C*1 (also used as an analog port)	V_{IH}	AVCC × 0.8	—	AVCC + 0.3		
		V_{IL}	–0.3	—	AVCC × 0.2		
	Ports 0 to 3*1 Ports 7 to B*1 Ports D to G*1	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#, TCK RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC input pin (SMBus operating)		2.1	—	VCC + 0.3		Conditions 1 and 2
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, WAIT#, TCK RSPI input pin		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		
	RIIC input pin (SMBus operating)		–0.3	—	0.8		Conditions 1 and 2

Note 1. This includes the multiplexed pin functions, except for P25, P26, PB1, or PB2 when the RIIC input functions are in use, P22 to P24, P30, PA3 to PA5, PB0, PD0 to PD2, or PD6 when the RSPI input functions are in use, and PD4 or PF3 when the TCK input function is in use.

Table 42.3 DC Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P52, P53, P60 to P65, P71 to P76, P90 to P95, and USB0_DPUPE)	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
	P52, P53, and P60 to P65		AVCC – 0.5	—	—		I_{OH} = –1 mA
	USB0_DPUPE		VCC_USB – 0.5				I_{OH} = –1 mA
	P71 to P76, and P90 to P95		VCC – 1.0	—	—		I_{OH} = –5 mA
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	P71 to P76, and P90 to P95		—	—	1.1		I_{OL} = 15 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Port 4, Ports P50, P51, P54 to P57, and Port C	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Port 0, Port 1, Ports P20 to P24, Port 3, Ports P52, P53, Ports 6 to A, Ports PB0, PB3 to PB7, and Ports D to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
	Ports P25, P26, PB1, and PB2		—	—	5.0		
Input capacitance	All output pins (except for P25, P26, PB1, and PB2)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 ºC
	Ports P25, P26, PB1, and PB2		—	—	30		

Table 42.4 DC Characteristics (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current *1	During operation	Max. *2	I_{CC}*3	—	—	70	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 100 MHz PCLKD = 50 MHz FCLK = 50 MHz
		Normal *4		—	40	—		
		Increased by BGO operation *5		—	15	—		
	Sleep mode				40	55		
	All-module-clock-stop mode *6				20	30		
	During standby	Software standby mode		—	0.10	3	mA	
		Deep software standby mode		—	20	60	µA	
Analog power supply current	During 12-bit A/D conversion (per unit)		AI_{CC0}	—	1.5	4.2	mA	
	Programmable gain amplifier (per channel)			—	1	1.5	mA	
	Window comparator (per channel)			—	0.5	0.7	mA	
	Waiting for 12-bit A/D conversion (all units)			—	0.1	8	µA	
	During 10-bit A/D conversion (per channel)		AI_{CC}	—	0.9	1.4	mA	
	During D/A conversion (per unit)				0.1	4	µA	
	Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	4	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)		AI_{REFH0}	—	1.6	2.5	mA	
	Waiting for 12-bit A/D conversion (all units)			—	0.1	1.5	µA	
	During 10-bit A/D conversion (per channel)		AI_{REF}	—	0.2	0.3	mA	
	During D/A conversion (per unit)				1	1.5	mA	
	Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	1.2	µA	
VCC rising gradient			SV_{CC}	—	—	20	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
I_{CC} max = 0.6 × f + 10 (max)
I_{CC} typ = 0.3 × f + 10 (normal)
I_{CC} max = 0.45 × f + 10 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

Table 42.5 Permissible Output Currents

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I_{OL}	—	—	2.0	mA
	RIIC pins	I_{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I_{OL}	—	—	15.0	mA
Permissible output low current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I_{OL}	—	—	4.0	mA
	RIIC pins	I_{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I_{OL}	—	—	15.0	mA
Permissible output low current (total)	Total of output pins	ΣI_{OL}	—	—	110	mA
Permissible output high current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and USB0_DPUPE pin)*1	$-I_{OH}$	—	—	2.0	mA
	USB0_DPUPE pin	$-I_{OH}$	—	—	3.0	mA
	P71 to P76, and P90 to P95*2	$-I_{OH}$	—	—	5.0	mA
Permissible output high current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95)*1	$-I_{OH}$	—	—	4.0	mA
	P71 to P76, and P90 to P95*2	$-I_{OH}$	—	—	5.0	mA
Permissible output high current (total)		$\Sigma-I_{OH}$	—	—	35	mA

Note 1. USB0_DP and USB0_DM are not included.

Note 2. For pins P71 to P76 and P90 to P95, I_{OL} = 15 mA (max.) and $-I_{OH}$ = 5 mA (max.). However, if several of the pins are to supply I_{OL} and $-I_{OH}$ of more than 2.0 mA at the same time, the number of pins should be six or less.

Caution: To protect the MCU’s reliability, the output current values should not exceed the values in this table.

Table 42.6 Permissible Power Consumption (G version product only)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = -40 to +105°C. Ta is common to conditions 1 to 3.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Total permissible power consumption*1	Pd	—	345	mW	85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. The total power consumption of the whole chip including output current.

42.3 AC Characteristics

Table 42.7 Operation Frequency Value

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLK) *1		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	AD clock (PCLKC)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	FlashIF clock (FCLK)		—	—	50	
	External bus clock (BCLK)		—	—	50	
	BCLK pin output		—	—	25	
	USB clock (UCLK)		—	—	48	

Note 1. The PCLK must run at a frequency of at least 24 MHz when the USB is in use.

42.3.1 Reset Timing

Table 42.8 Reset Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 42.1
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 42.2
	Software standby mode	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{cyc}	
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{cyc}	

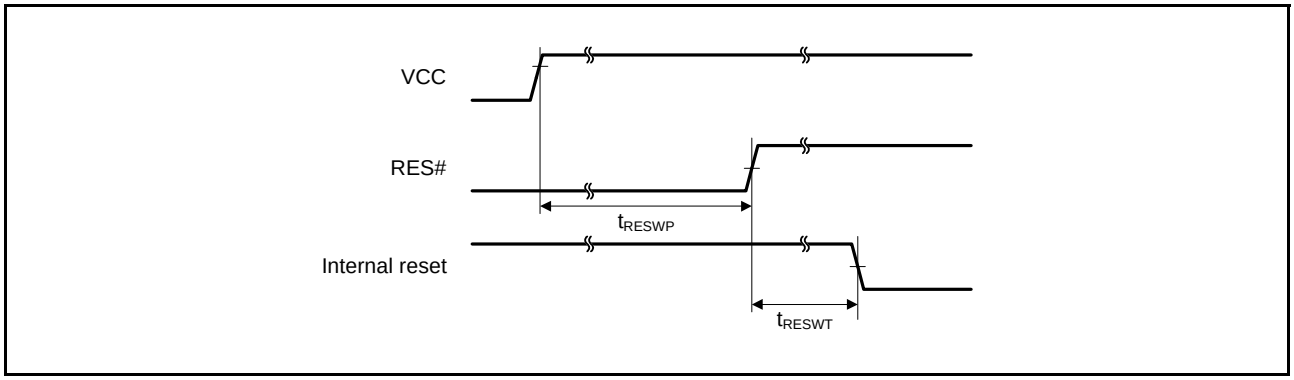


Figure 42.1 Reset Input Timing at Power-On

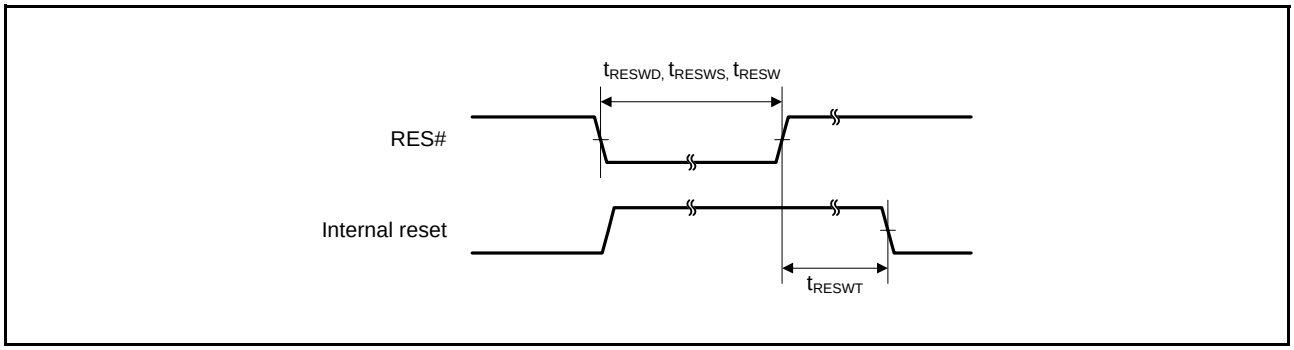


Figure 42.2 Reset Input Timing

42.3.2 Clock Timing

Table 42.9 Clock Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Only condition 3	t_{Bcyc}	20	—	—	ns	Figure 42.3
	Other than condition 3	t_{Bcyc}	40	—	—	ns	
BCLK pin output high pulse width		t_{CH}	5	—	—	ns	
BCLK pin output low pulse width		t_{CL}	5	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
EXTAL external clock input cycle time		t_{EXcyc}	70	—	—	ns	Figure 42.4
EXTAL external clock input high pulse width		t_{EXH}	35	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	35	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	8	—	12.5	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	—	—	*2	ms	Figure 42.5
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	—	—	*3	ms	
LOCO, IWDTCLK clock cycle time		$t_{LOCOCYC}$	6.96	8	9.4	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 42.6
PLL clock frequency		f_{PLL}	104	—	200	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 42.7
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	*4	ms	
PLL clock oscillation stabilization time	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC}$ + t_{PLL1}	ms	Figure 42.8
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).

Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

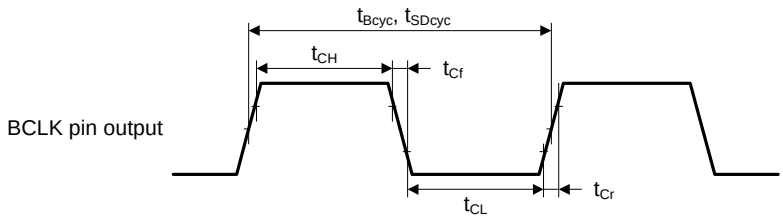
Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

Note 4. This is calculated from the formula below, where n is the number of cycles set by the PLLWTCR.PSTS[4:0] bits.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

Figure 42.3 BCLK Pin Output Timing

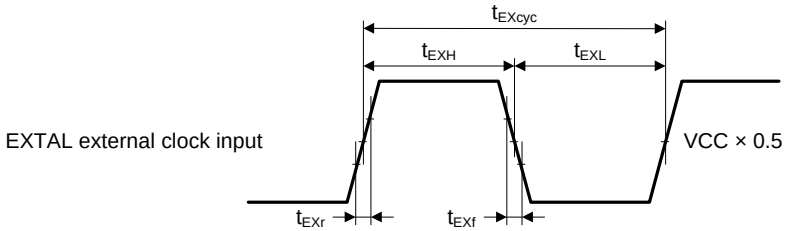


Figure 42.4 EXTAL External Clock Input Timing

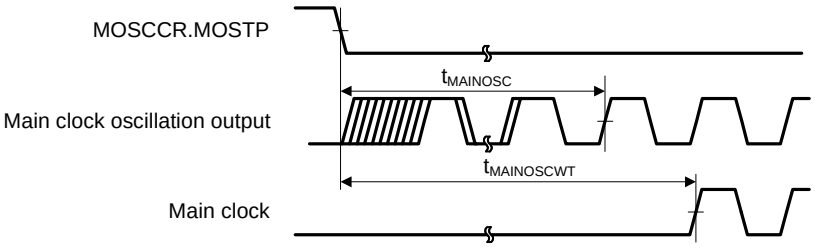


Figure 42.5 Main Clock Oscillation Start Timing

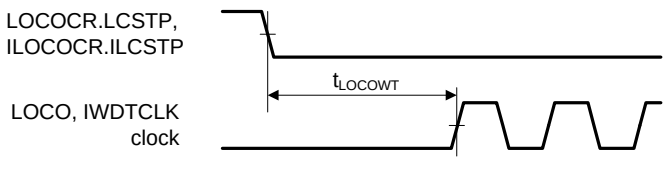


Figure 42.6 LOCO, IWDTCLK Clock Oscillation Start Timing

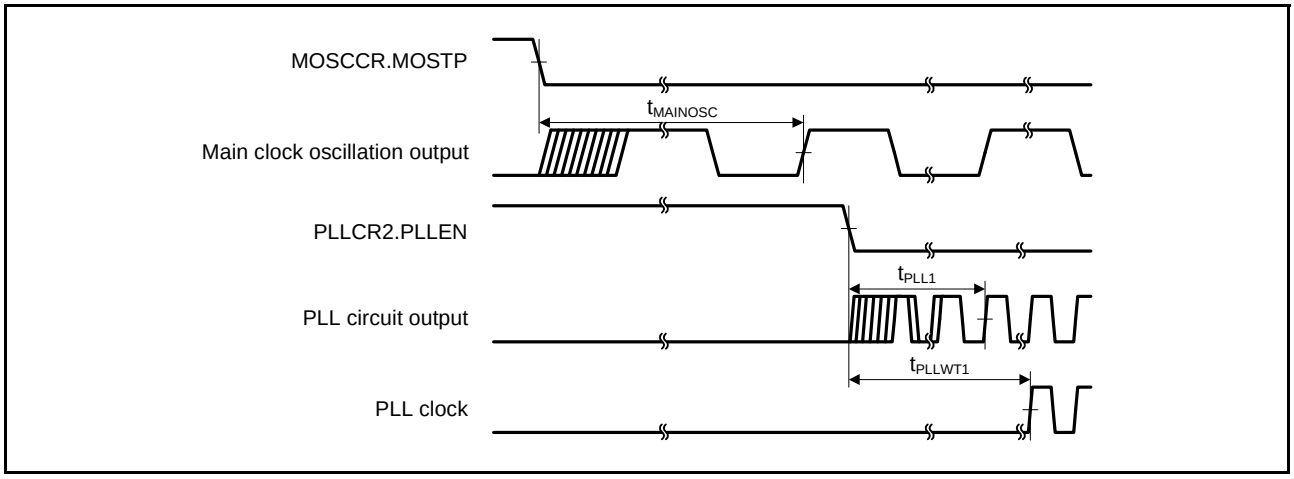


Figure 42.7 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

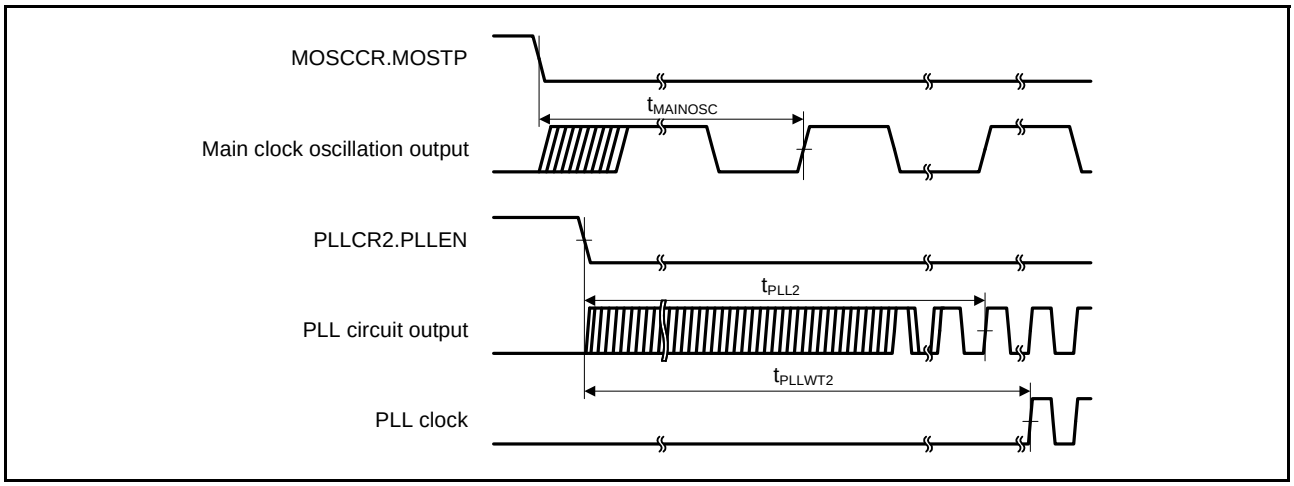


Figure 42.8 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

42.3.3 Timing of Recovery from Low Power Consumption Modes

Table 42.10 Timing of Recovery from Low Power Consumption Modes

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 42.9
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1	ms	Figure 42.10
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

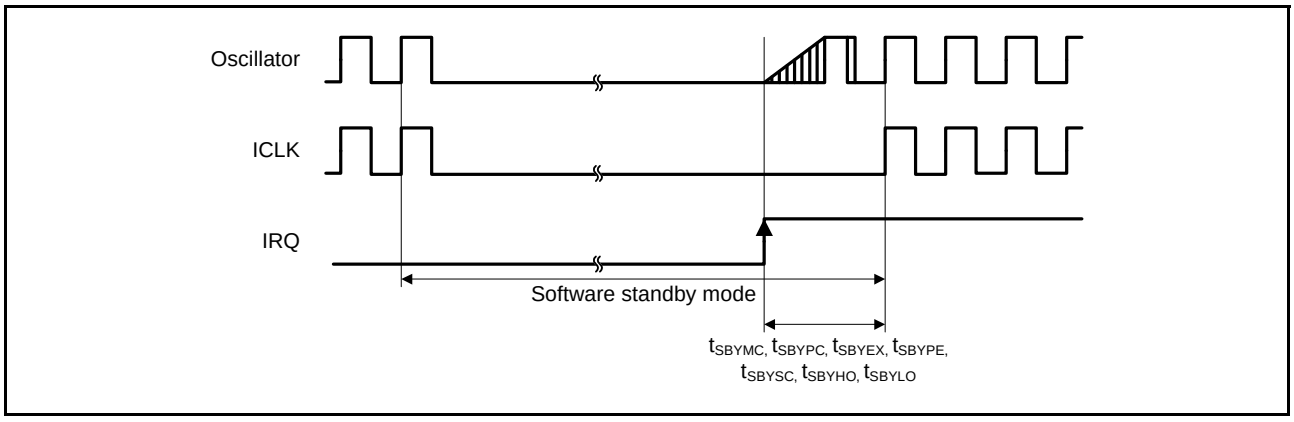


Figure 42.9 Software Standby Mode Cancellation Timing

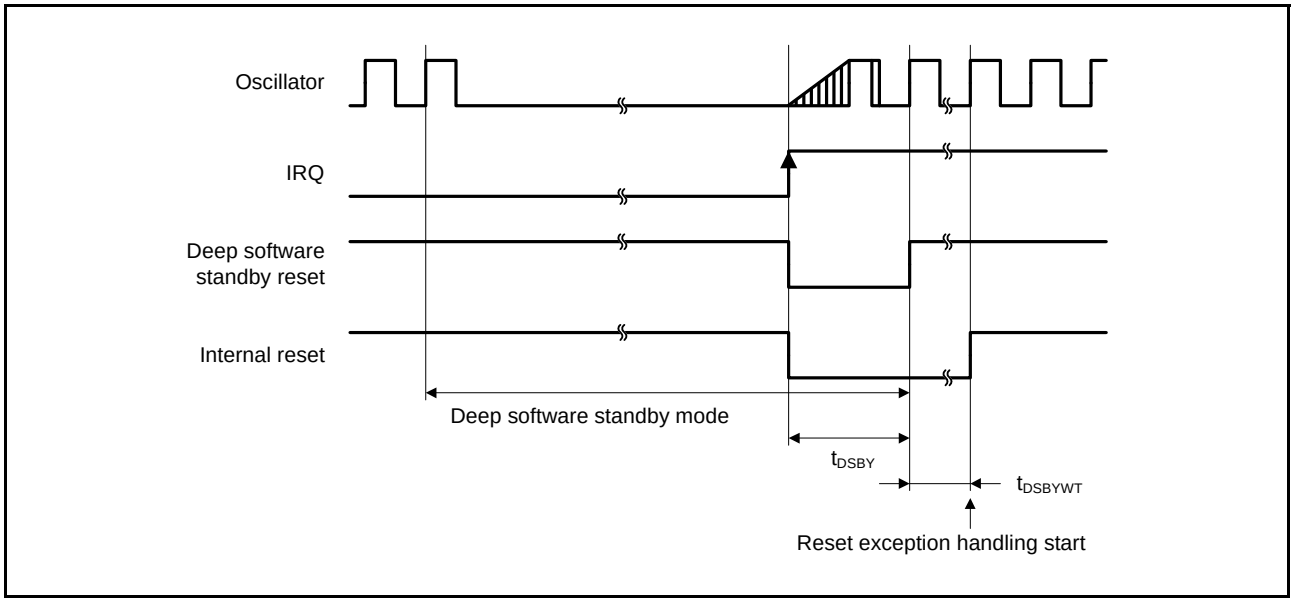


Figure 42.10 Deep Software Standby Mode Cancellation Timing

42.3.4 Control Signal Timing

Table 42.11 Control Signal Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_c(PCLK) × 2 ≤ 200 ns, Figure 42.11
		t_c(PCLK) × 2	—	—	ns	t_c(PCLK) > 200 ns, Figure 42.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_c(PCLK) ≤ 200 ns, Figure 42.12
		t_c(PCLK) × 2	—	—	ns	t_c(PCLK) > 200 ns, Figure 42.12

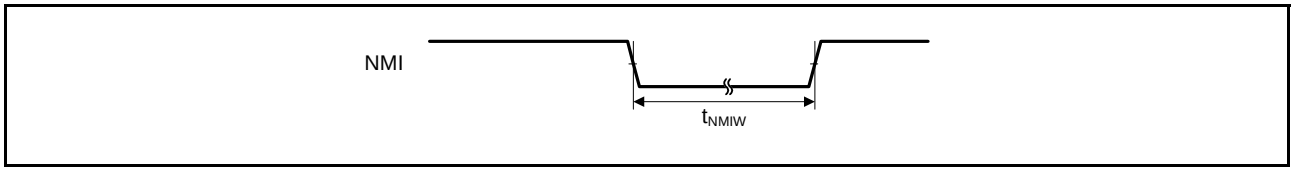


Figure 42.11 NMI Interrupt Input Timing

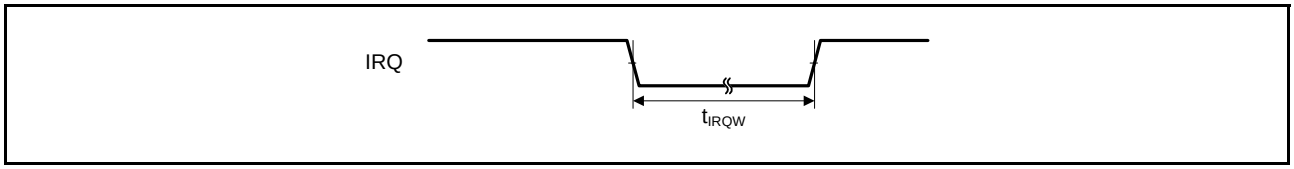


Figure 42.12 IRQ Interrupt Input Timing

42.3.5 Bus Timing

Table 42.12 Bus Timing (1)

Condition: VCC = PLLVCC = VCC_USB = AVCC0 = AVCC = 3.0 to 3.6 V,
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figure 42.13 to Figure 42.16
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 42.17
WAIT# hold time	t_{WTH}	0	—	ns	

Table 42.13 Bus Timing (2)

Condition: VCC = PLLVCC = AVCC0 = AVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V,
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 42.13 to Figure 42.16
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 42.17
WAIT# hold time	t_{WTH}	0	—	ns	

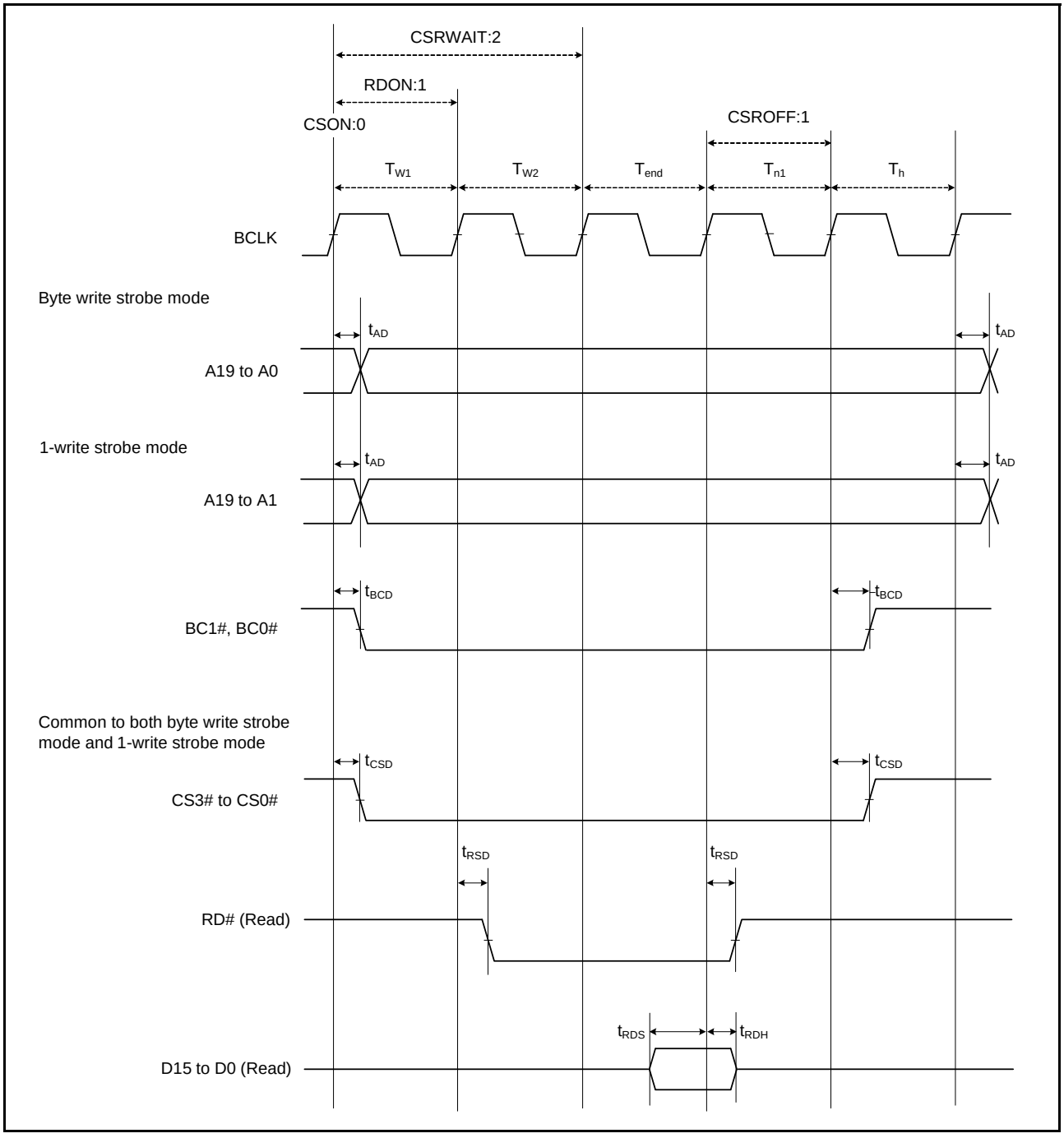
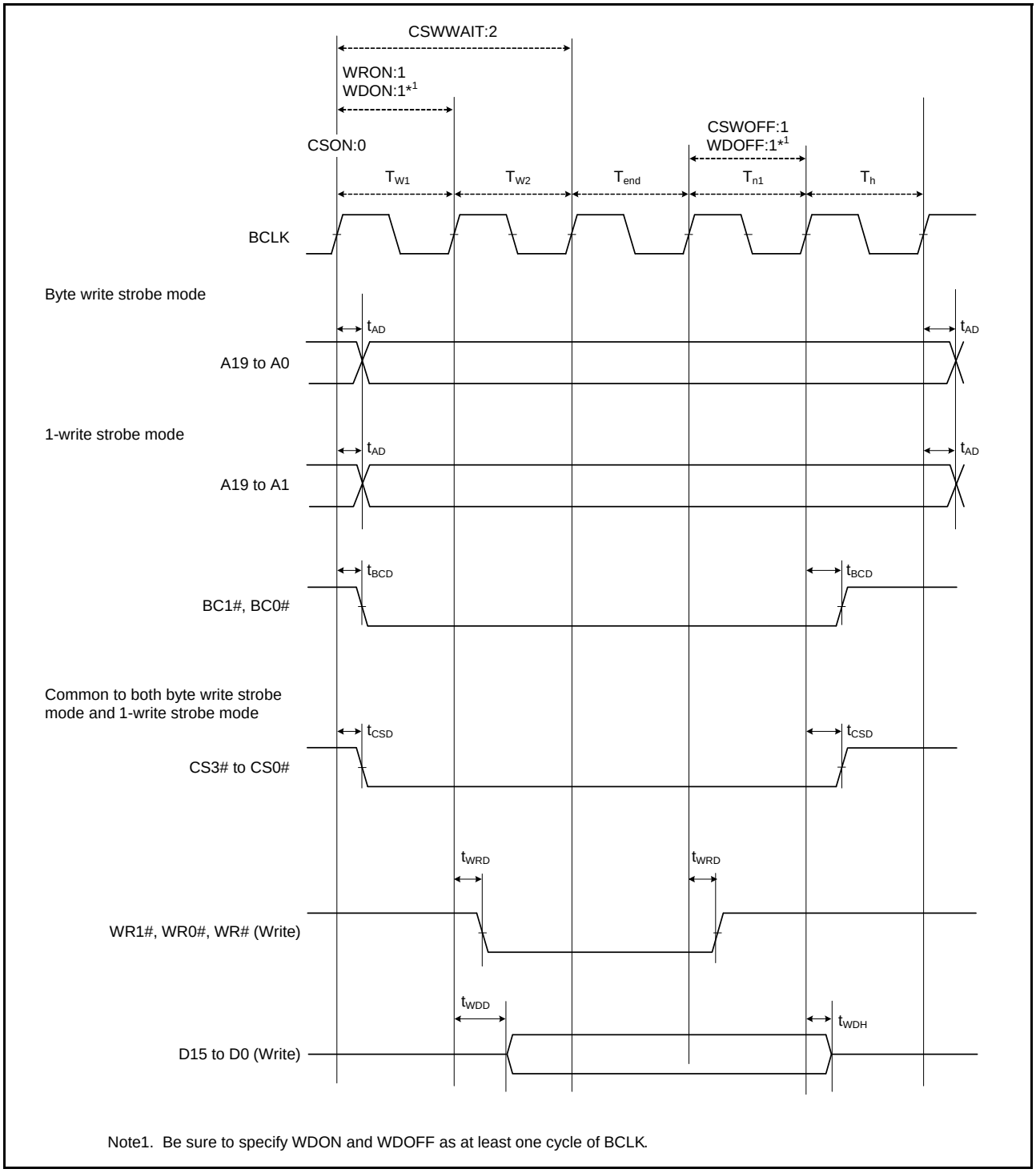


Figure 42.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 42.14 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

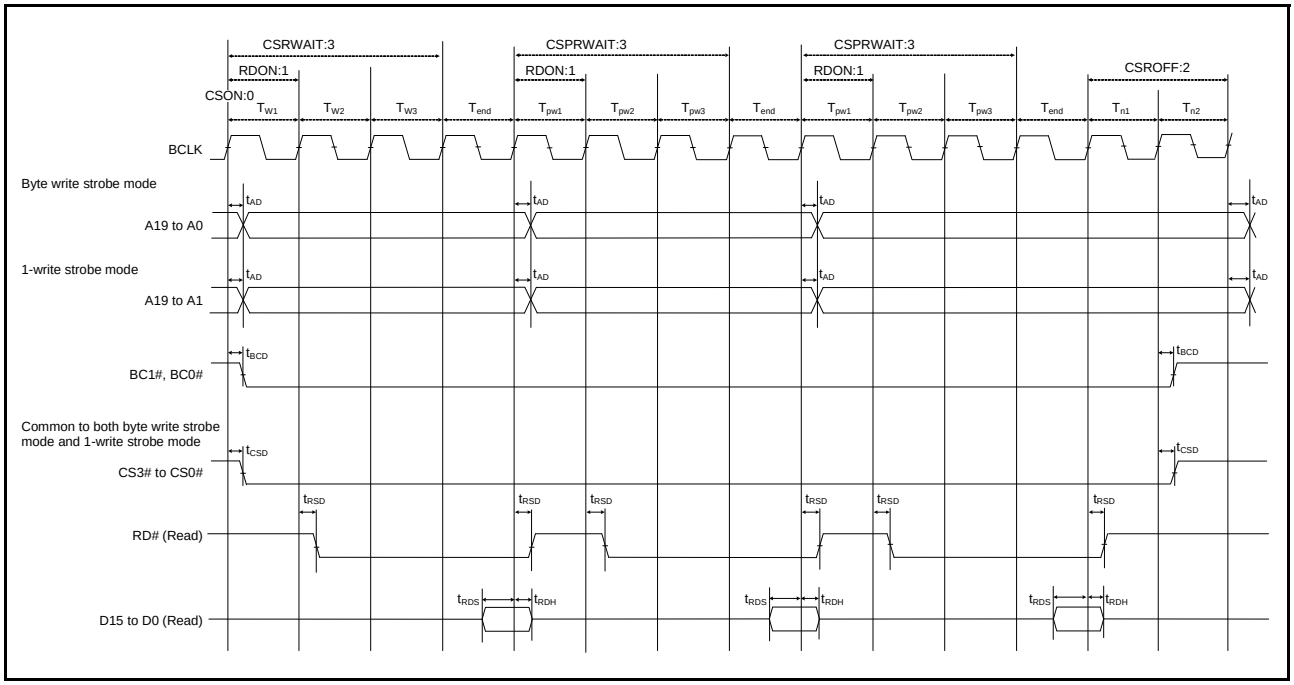
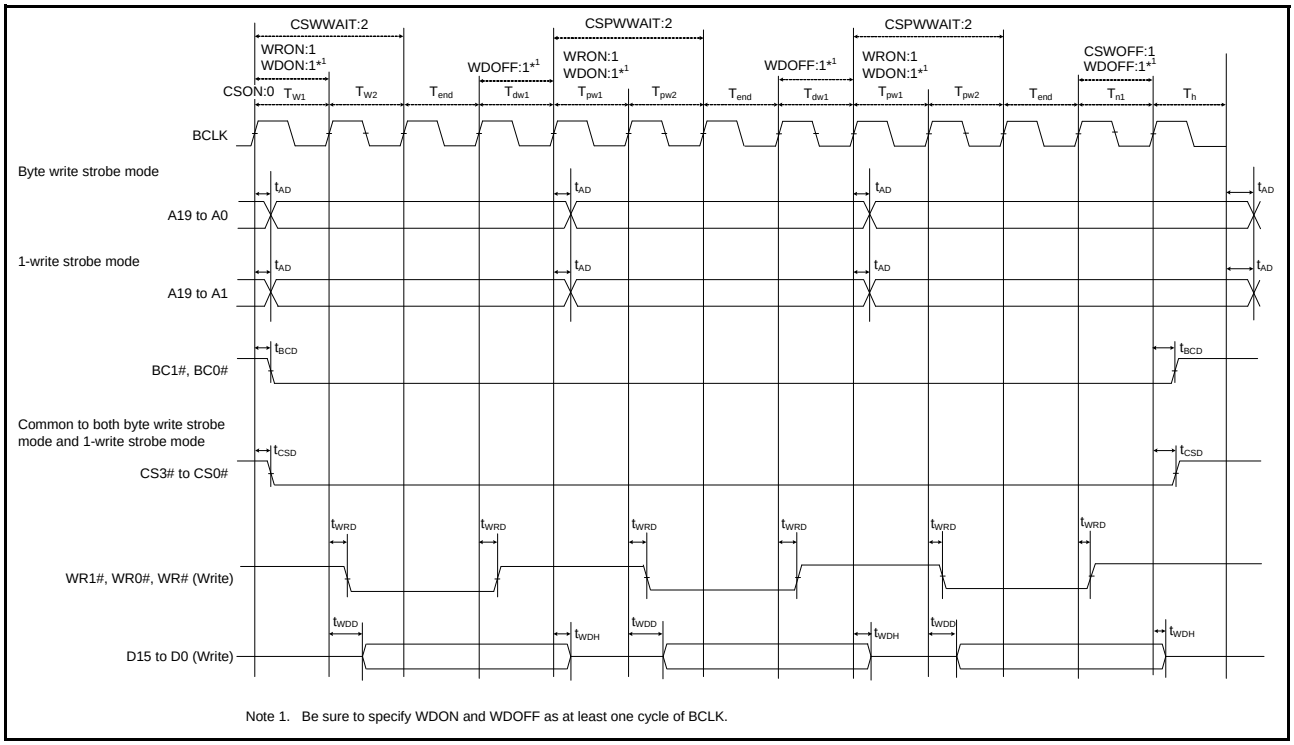


Figure 42.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 42.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

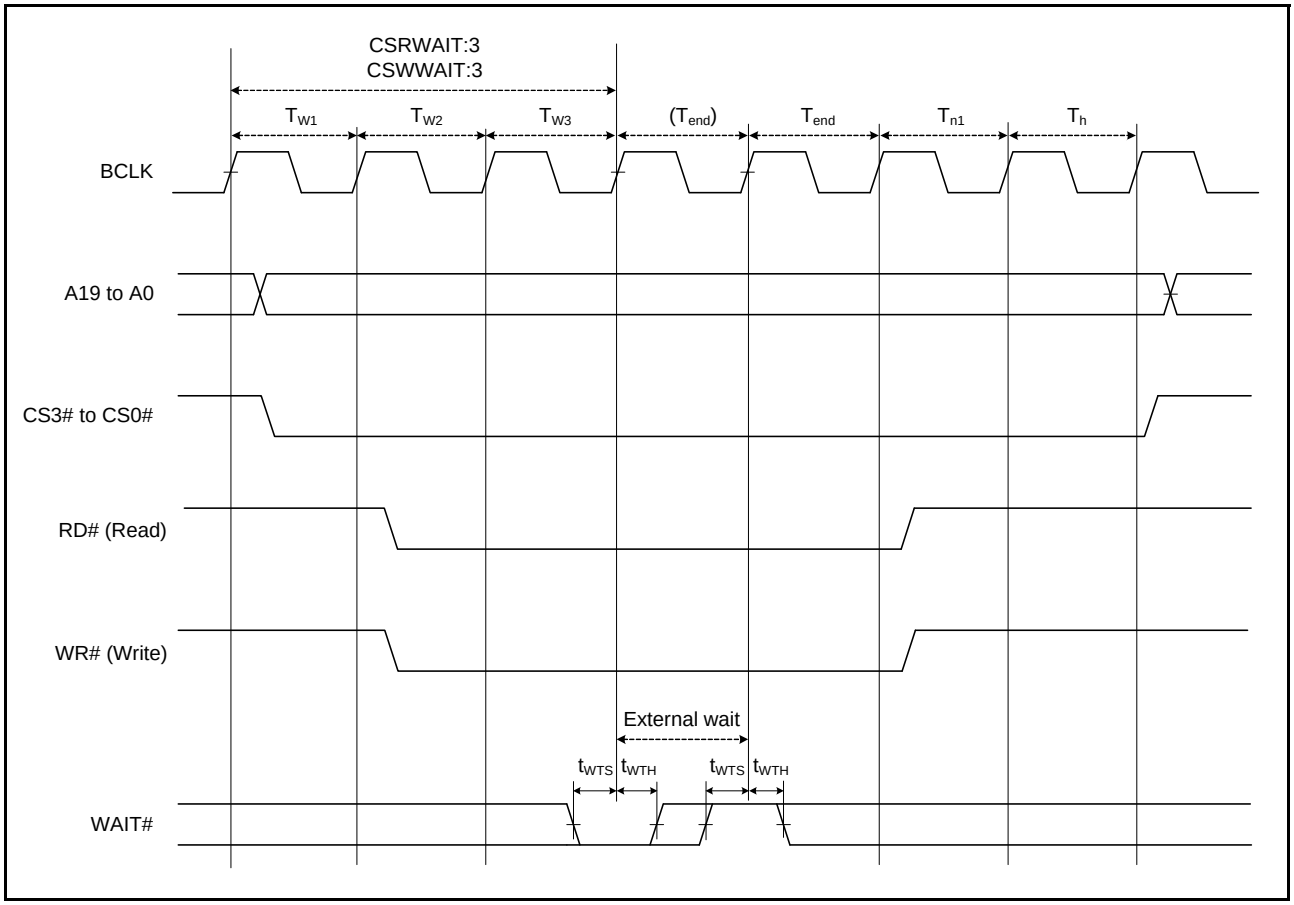


Figure 42.17 External Bus Timing/External Wait Control

Table 42.14 Bus Timing (Multiplexed Bus) (3)

Condition: PLLVCC = VCC_USB = AVCC0 = AVCC = VREF = 3.0 to 3.6 V
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	35	ns	Figure 42.18, Figure 42.19
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
ALE delay time	t_{ALED}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 42.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

Table 42.15 Bus Timing (Multiplexed Bus) (4)

Condition: VCC = PLLVCC = AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 42.18, Figure 42.19
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
RD# delay time	t_{RSD}	—	15	ns	
ALE delay time	t_{ALED}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 42.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

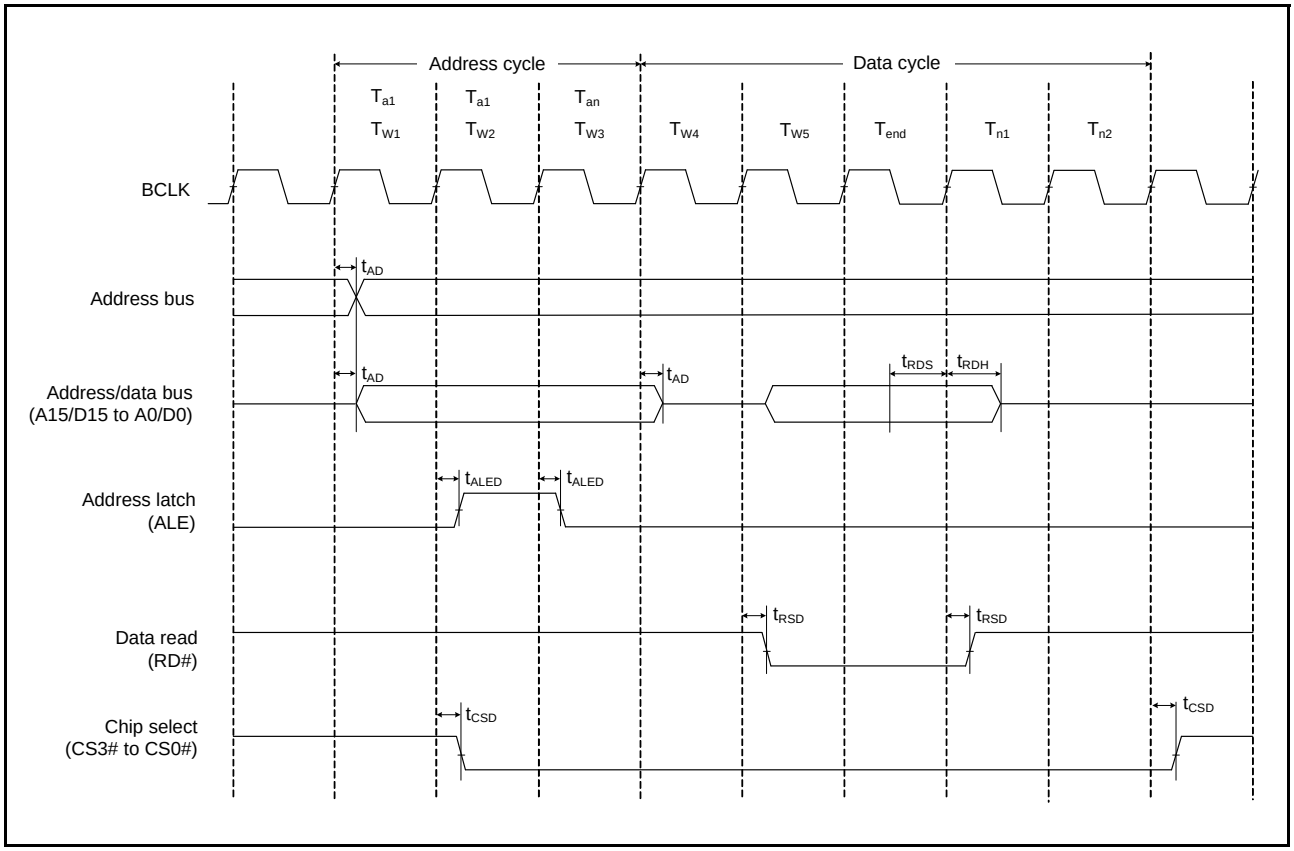


Figure 42.18 Example of External Bus Timing/Read Access Operation (Multiplexed)

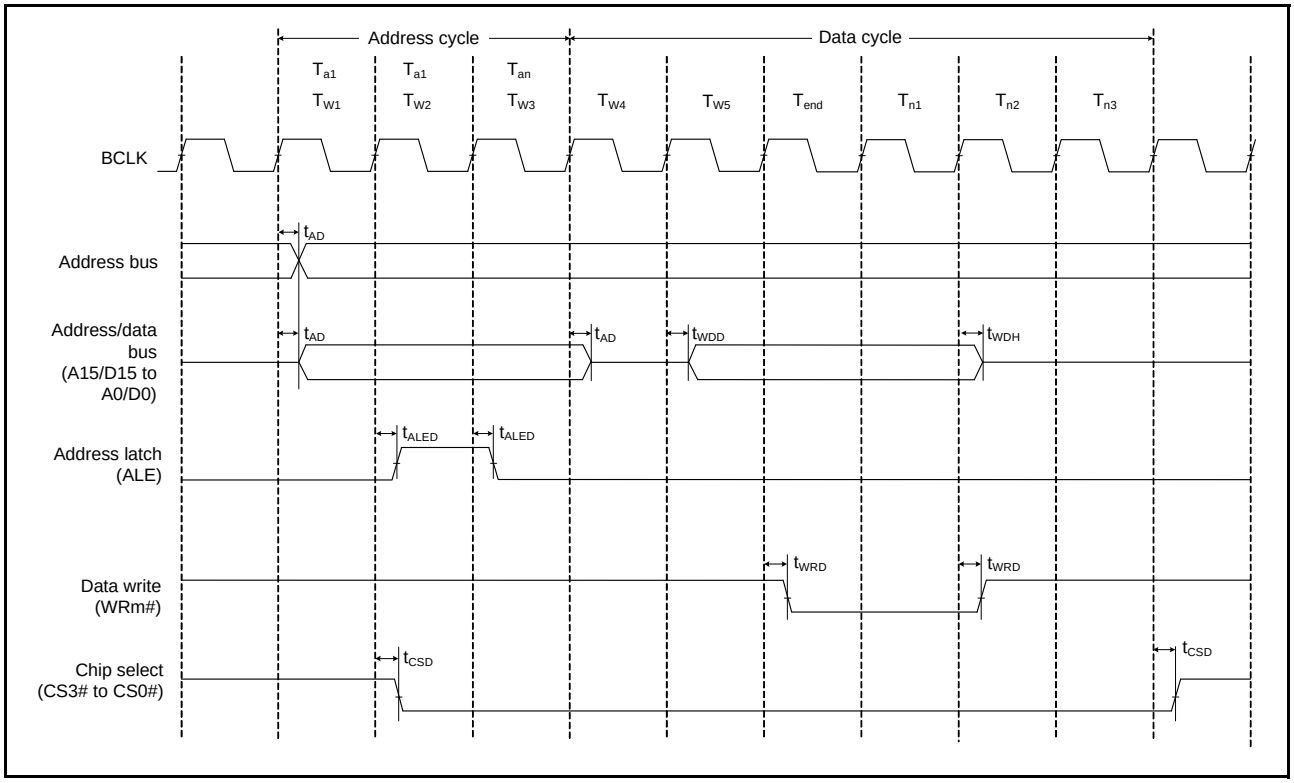


Figure 42.19 Example of External Bus Timing/Write Access Operation (Multiplexed)

42.3.6 Timing of On-Chip Peripheral Modules

Table 42.16 Timing of On-Chip Peripheral Modules (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 42.22
MTU3	Input capture input pulse width	Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 42.23
		Both-edge setting		5	—		
	Input capture input fall time		t_{TICTF}	—	0.1	µs/V	When Input capture at rising edge, or Input capture at both edges is selected.
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 42.25
		Both-edge setting		5	—		
		Phase counting mode		5	—		
	Timer clock input fall time		t_{TCKTF}	—	0.1	µs/V	
POE3	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 42.28
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PAcyc}	Figure 42.26
		Both-edge setting		5	—		
	Input capture input fall time		t_{GTICTF}	—	0.1	µs/V	When Input capture at rising edge, or Input capture at both edges is selected. When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.
	External trigger input pulse width	Single-edge setting	t_{OTETW}	3	—	t_{PAcyc}	Figure 42.27
		Both-edge setting		5	—		
	External trigger input fall time		$t_{GTETRGTF}$	—	0.1	µs/V	When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.

Table 42.16 Timing of On-Chip Peripheral Modules (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	C = 30 pF Figure 42.29
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 42.30
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
	Receive data fall time		t_{TICTF}	—	0.1	µs/V	When Noise Cancellation Function is not used.
A/D converter	10-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 42.31
	12-bit A/D converter trigger input pulse width			1.5	—		
CAC	CACREF input pulse width	$t_{Pcyc} \leq t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}	—	ns	
	CACREF input fall time		$t_{CACREFTF}$	—	0.1	µs/V	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcye}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle.

Table 42.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF, Figure 42.32
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input			—	1	µs	
	RSPCK clock fall time	Input		t_{SPCKF}	—	0.1	µs/V	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF, Figure 42.33 to Figure 42.40
		Slave			20 – t_{Pcyc}	—		
	Data input hold time	Master	PCLKB division ratio set to a value other than 1/2	t_H	t_{Pcyc}	—	ns	
			PCLKB division ratio set to 1/2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	10	ns	
		Slave			—	3 × t_{Pcyc} + 40		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output		t_{DR}, t_{DF}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	15	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 42.39 and Figure 42.40
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 42.16 Timing of On-Chip Peripheral Modules (4)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF, Figure 42.30
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	C = 30 pF, Figure 42.31 to Figure 42.38
	Data input hold time	t_H	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	C = 30 pF, Figure 42.37 and Figure 42.38
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 42.16 Timing of On-Chip Peripheral Modules (5)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 42.36
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.

Table 42.16 Timing of On-Chip Peripheral Modules (6)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	Figure 42.36
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.
Note 3. t_{Pcyc}: PCLK cycle

42.3.7 Timing of PWM Delay Generation Circuit

Table 42.17 Timing of the PWM Delay Generation Circuit

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is common to conditions 1 to 3.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	PCLKA = 100 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

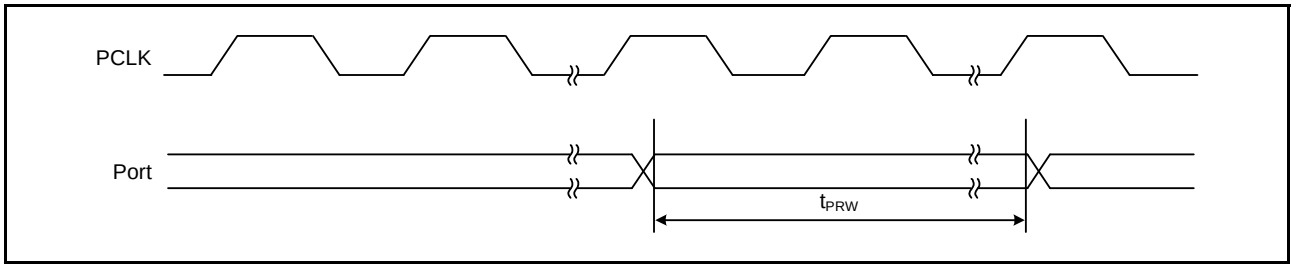


Figure 42.20 I/O port Input Timing

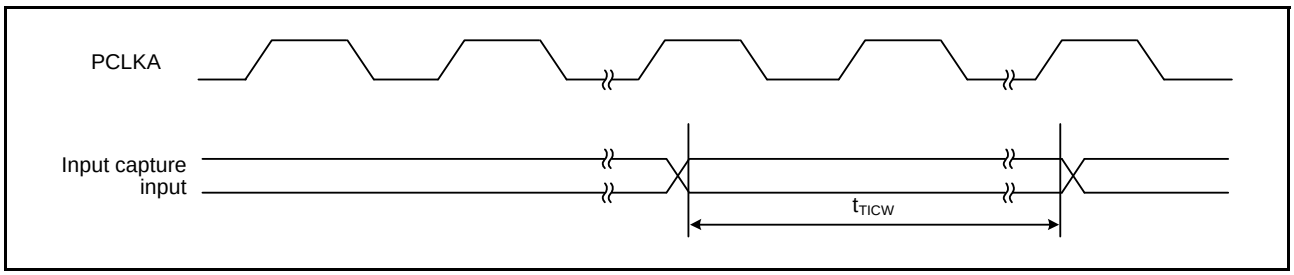


Figure 42.21 MTU3 Input/Output Timing

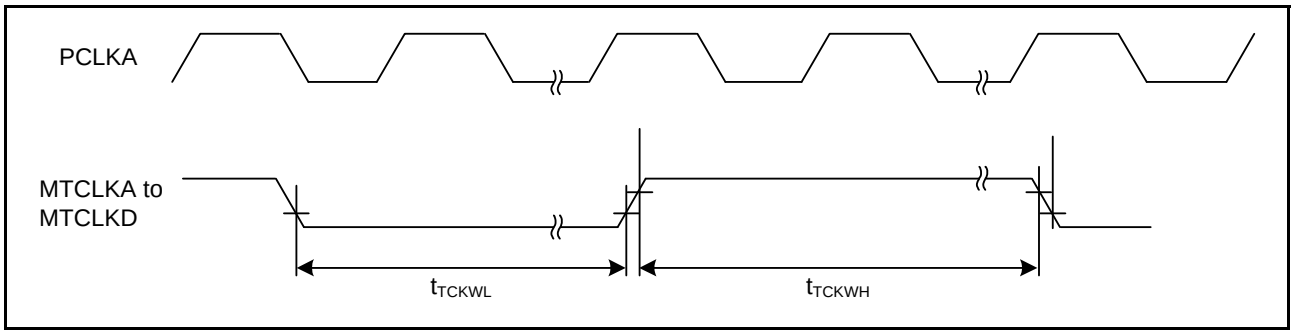


Figure 42.22 MTU3 Clock Input Timing

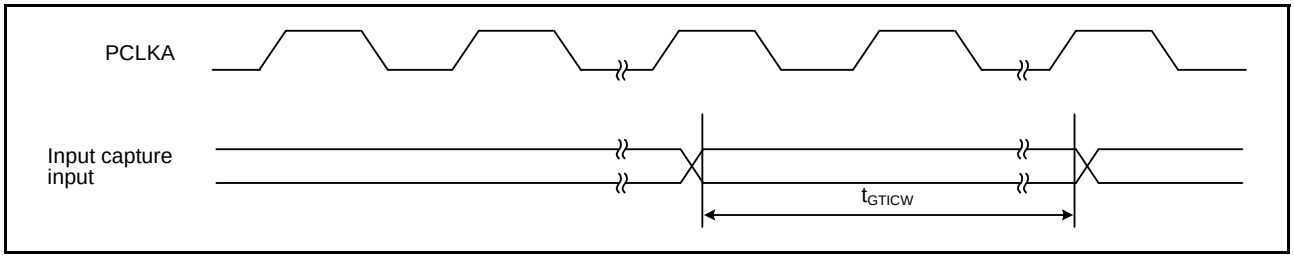


Figure 42.23 GPT Input Capture Input Timing

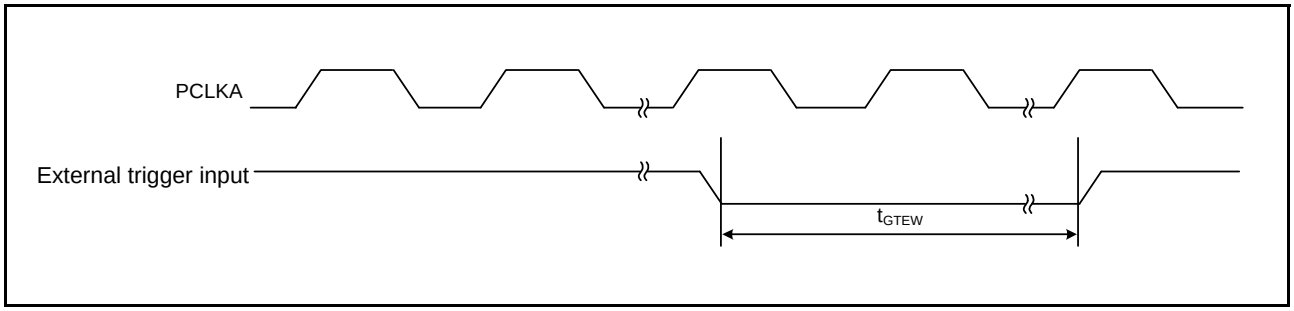


Figure 42.24 GPT External Trigger Input Timing

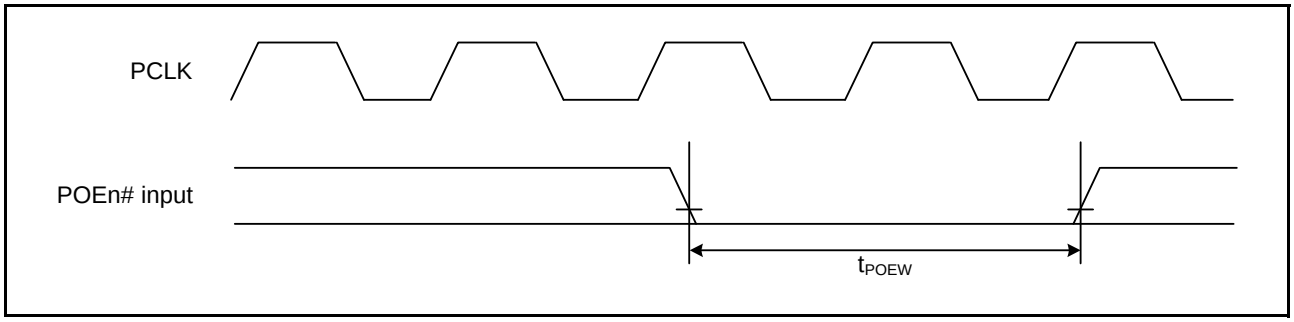


Figure 42.25 POE3# Input Timing

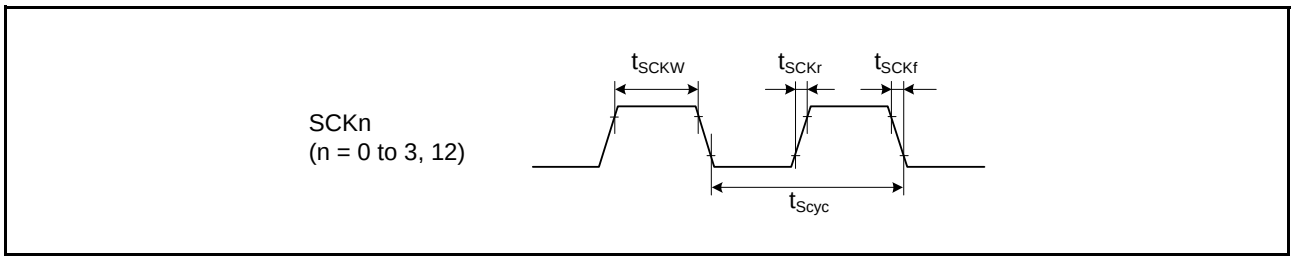


Figure 42.26 SCK Clock Input Timing

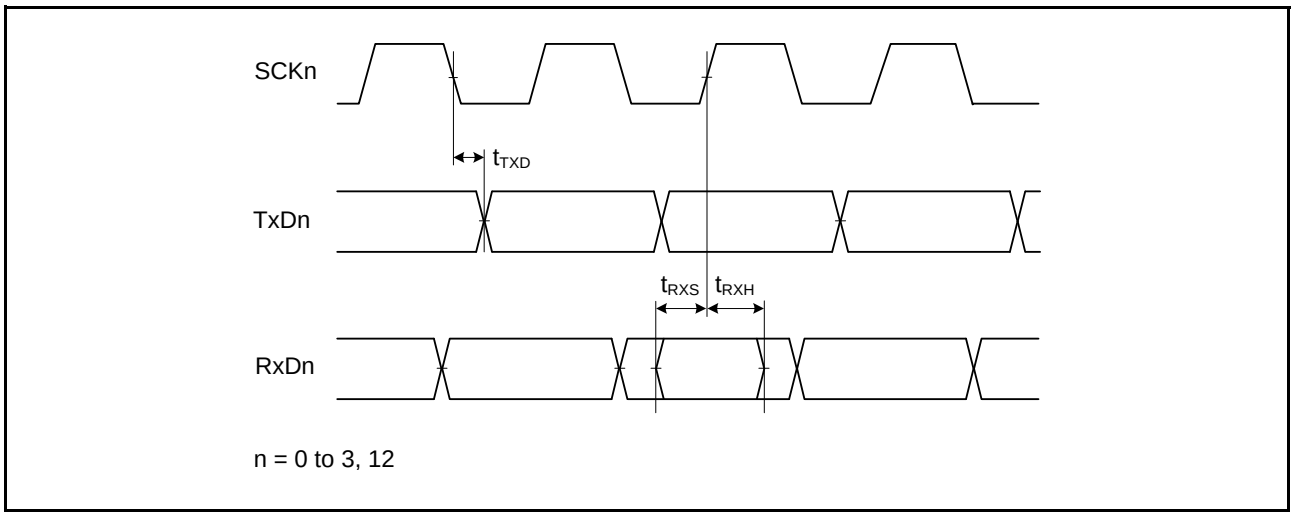


Figure 42.27 SCI Input/Output Timing: Clock Synchronous Mode

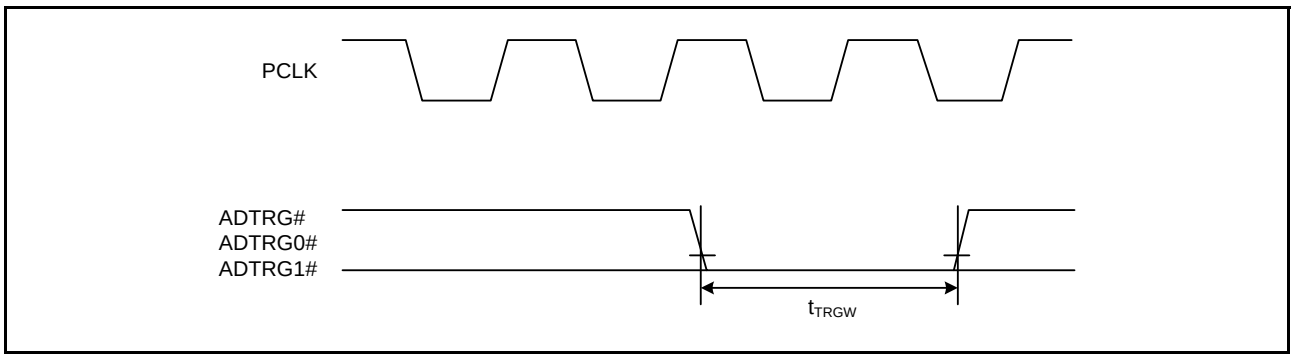


Figure 42.28 AD Converter External Trigger Input Timing

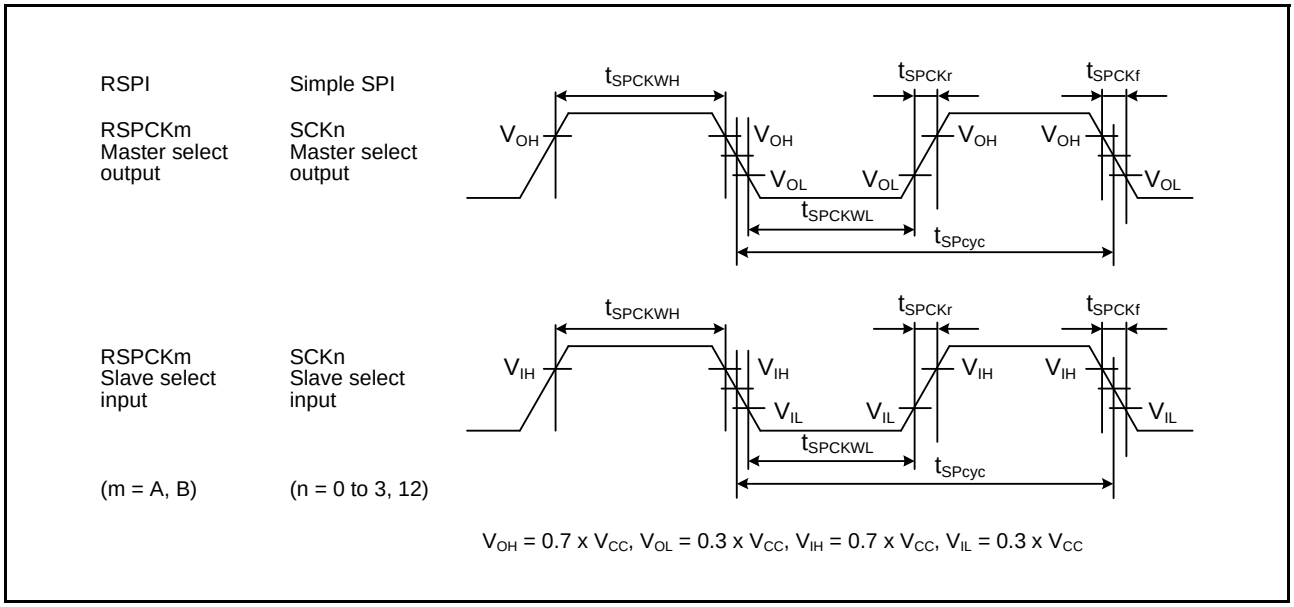


Figure 42.29 RSPI Clock Timing and Simple SPI Clock Timing

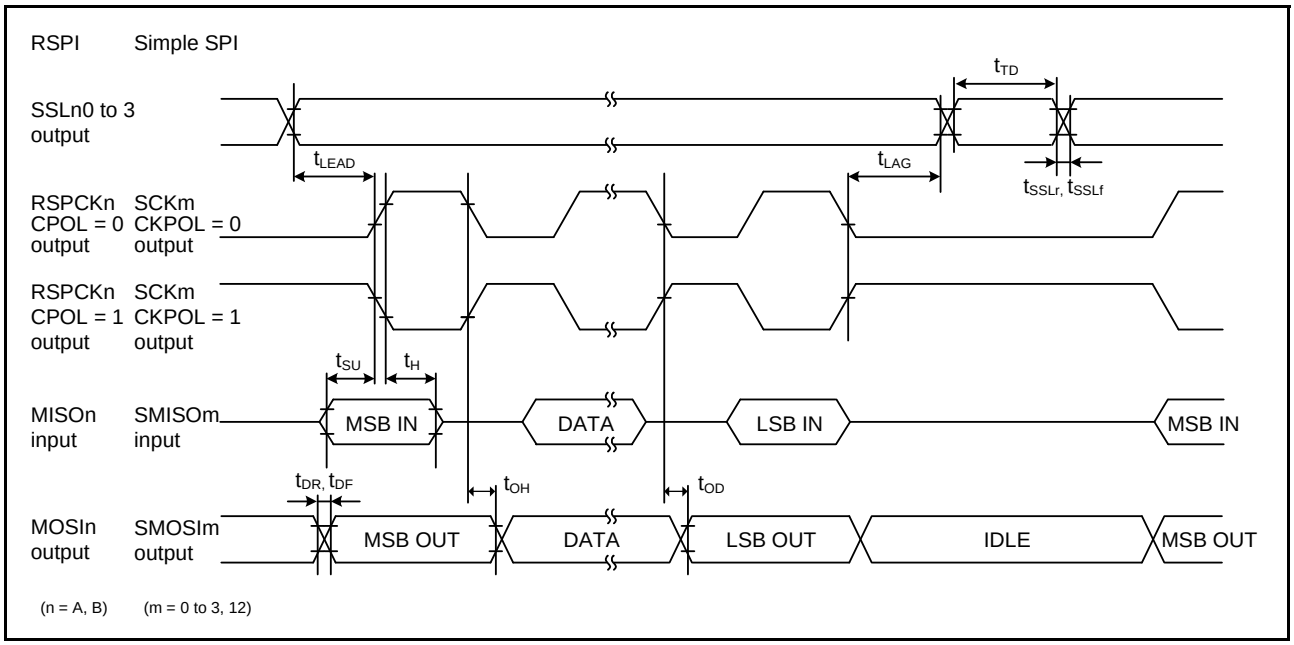


Figure 42.30 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1)

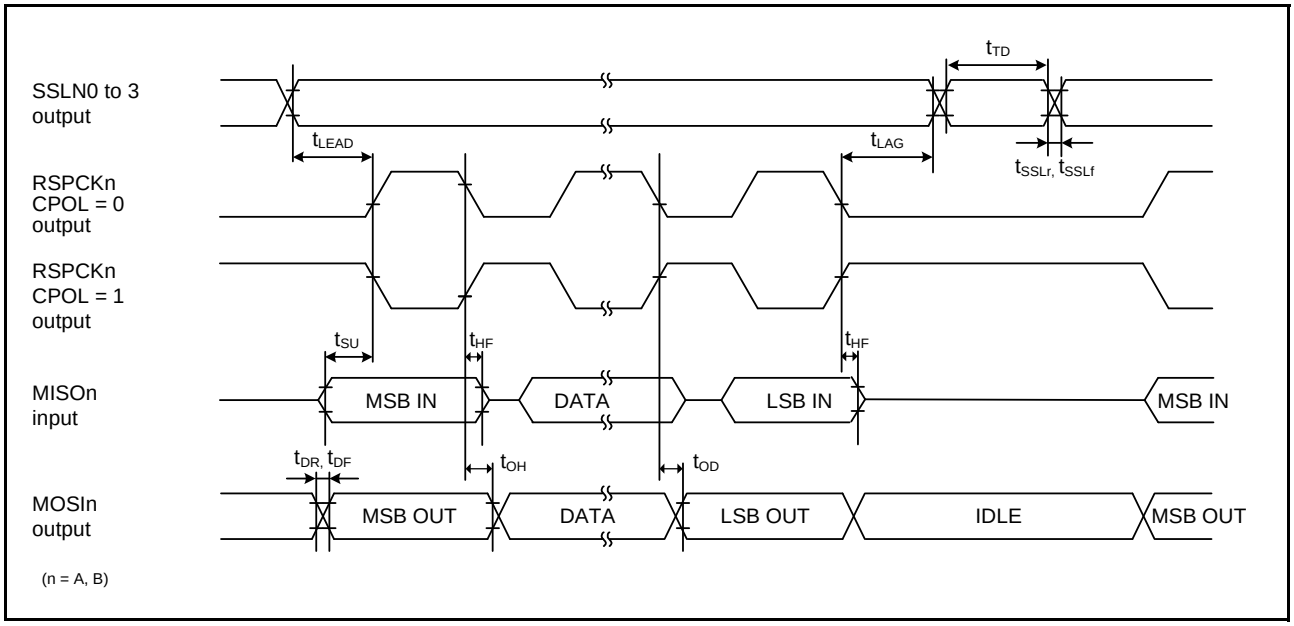


Figure 42.31 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

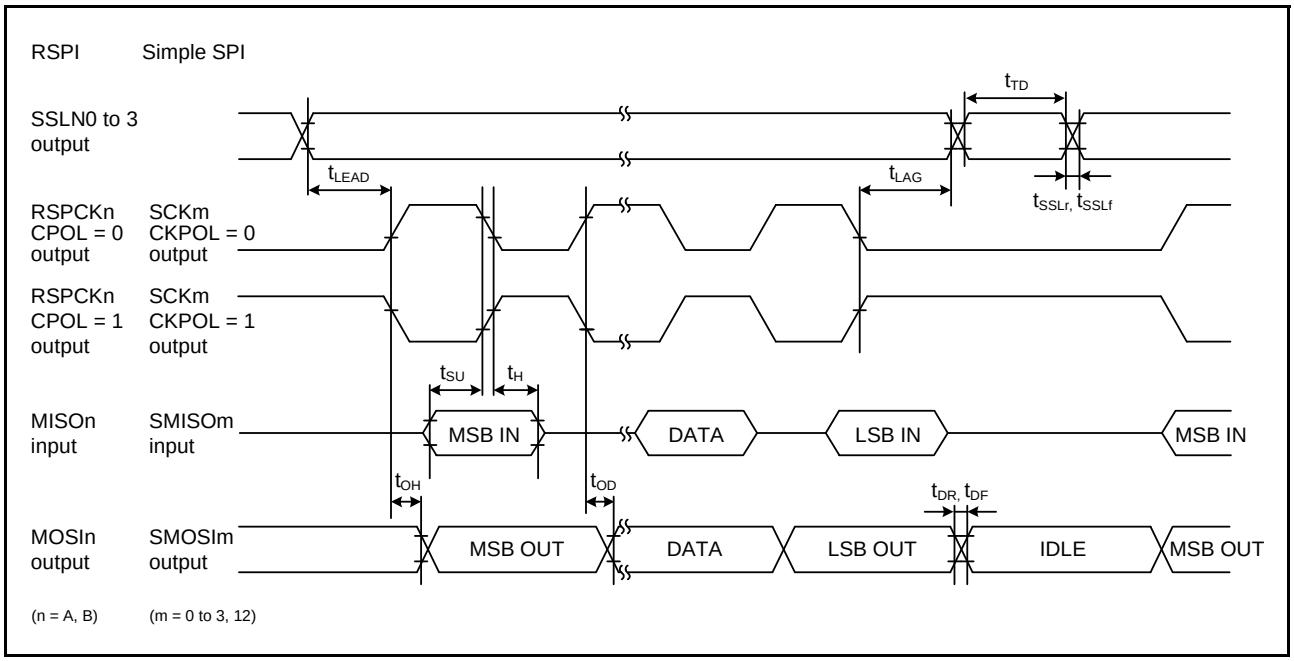


Figure 42.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

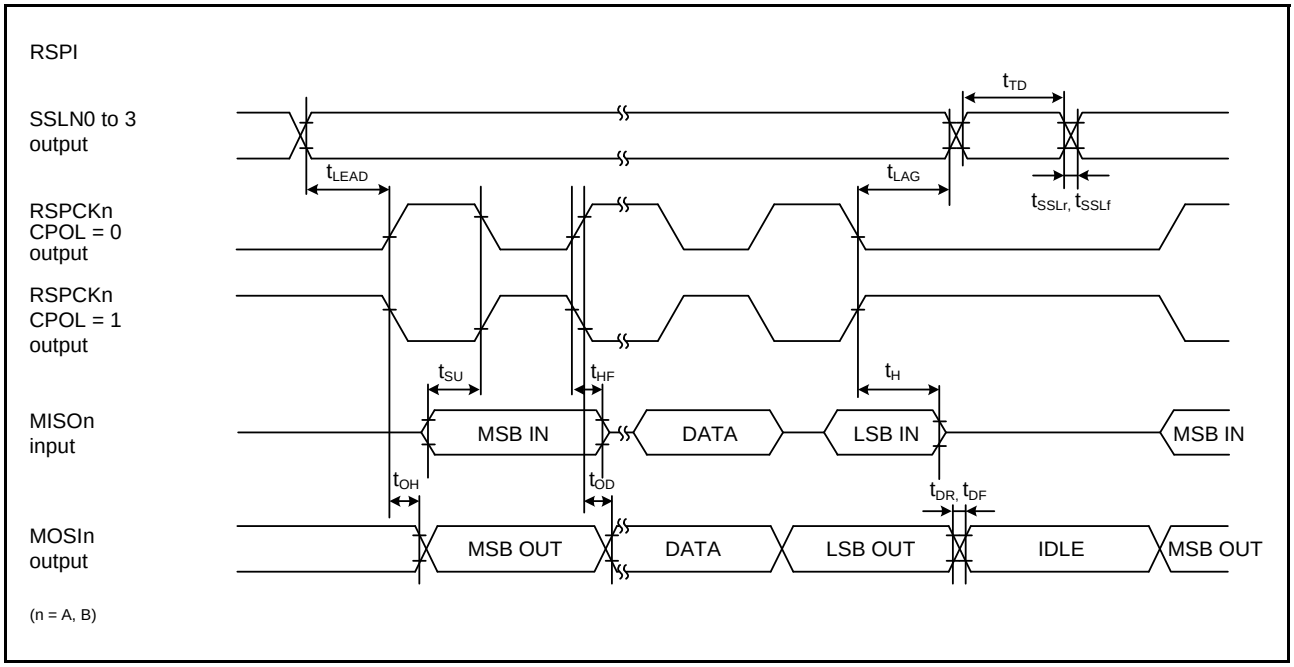


Figure 42.33 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

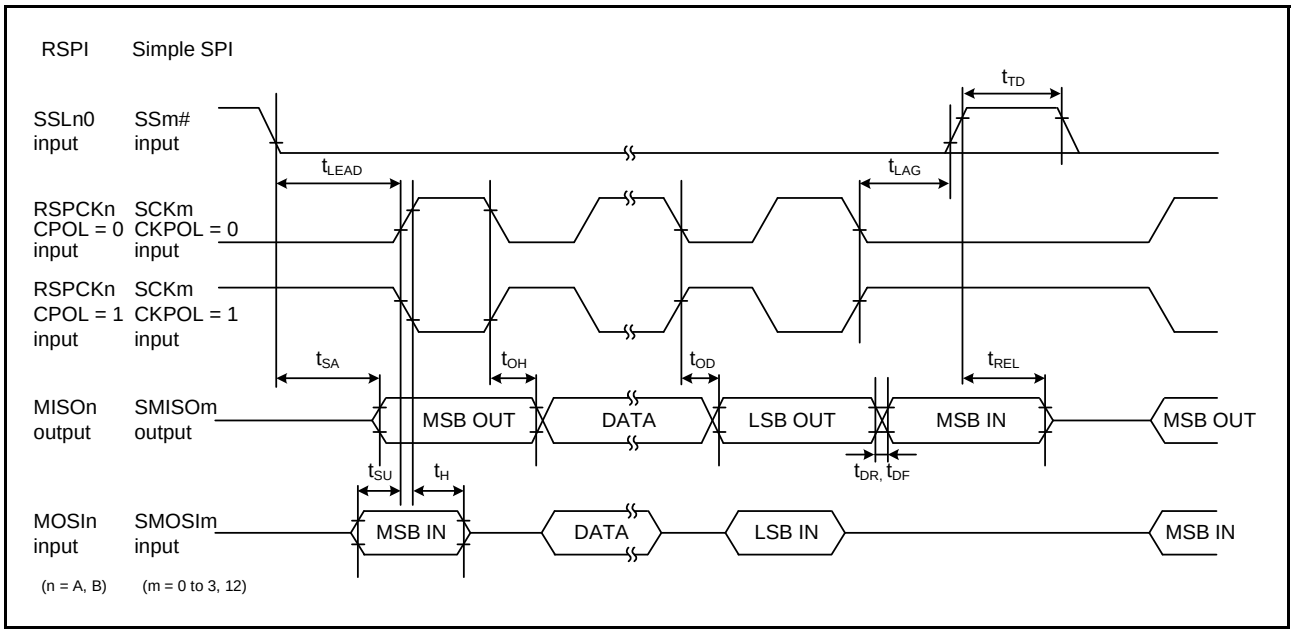


Figure 42.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

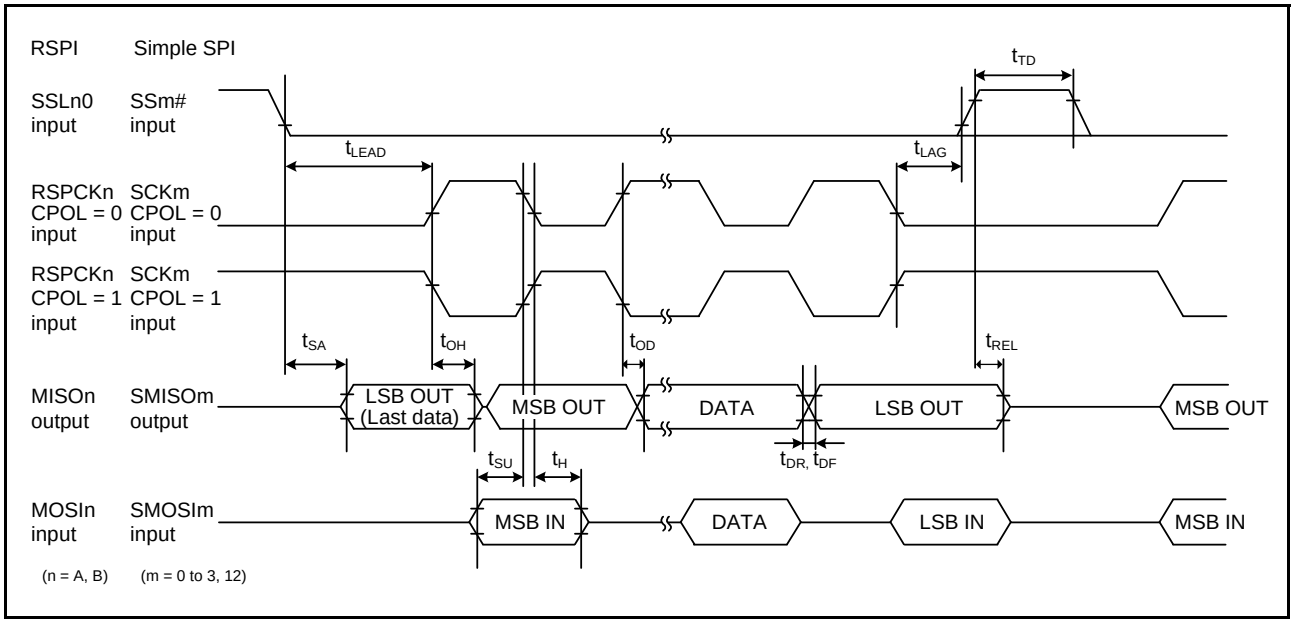


Figure 42.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

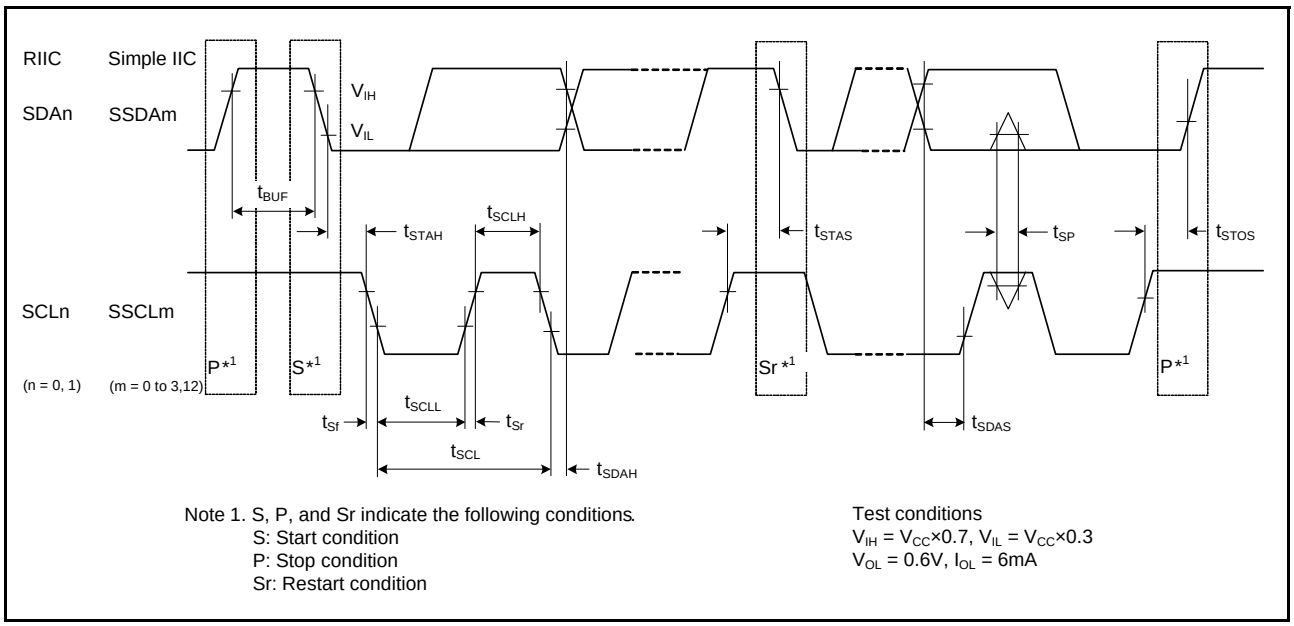


Figure 42.36 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

42.4 USB Characteristics

Table 42.18 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V		Figure 42.37 Figure 42.38
	Input low level voltage	V_{IL}	—	0.8	V		
	Differential input sensitivity	V_{DI}	0.2	—	V	| DP – DM |	
	Differential common mode range	V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V_{OH}	2.8	3.6	V	I_{OH} = –200 µA	
	Output low level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 2 mA	
	Cross-over voltage	V_{CRS}	1.3	2.0	V		
	Rise time	t_{Lr}	4	20	ns		
	Fall time	t_{Lf}	4	20	ns		
	Rise/fall time ratio	t_{Lr} / t_{Lf}	90	111.11	%	t_{Lr} / t_{Lf}	
	Output resistance	Z_{DRV}	28	44	Ω	Rs = 24 Ω included	

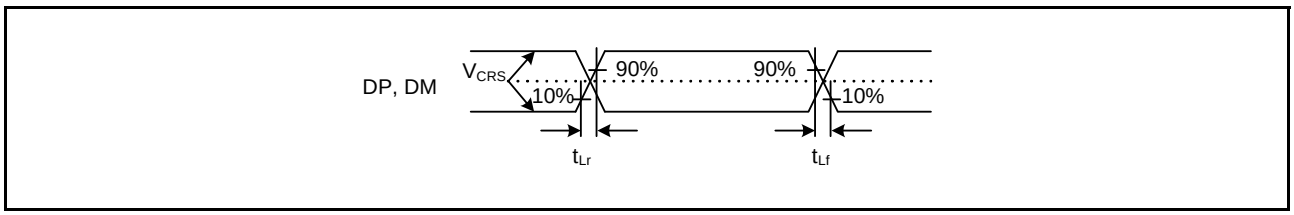


Figure 42.37 DP and DM Output Timing (Full-Speed)

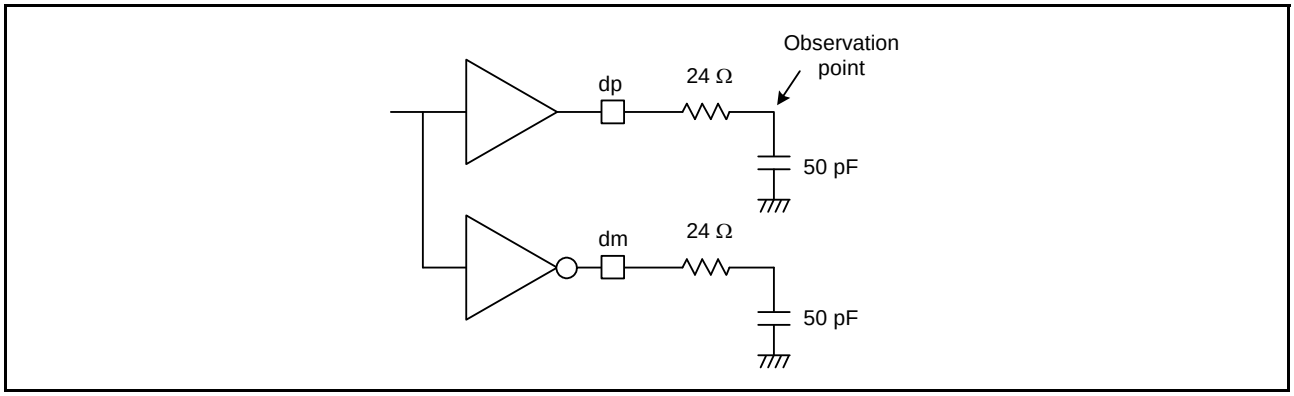


Figure 42.38 Test Circuit (Full-Speed)

42.5 A/D Conversion Characteristics

Table 42.19 10-Bit A/D Conversion Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 100 MHz)	With 0.1-µF external capacitor	AN0 to AN7	0.5	—	—	µs	Sampling in 25 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.6	—	—	µs	Sampling in 35 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±3.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 42.20 10-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$ is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 50 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.8	—	—	µs	Sampling in 15 states
		Other channels	1.0	—	—	µs	Sampling in 25 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±2.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±4.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 42.21 12-Bit A/D Conversion Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

$T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 25 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	2.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	8	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±4.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±4.0	LSB	
	Full-scale error	—	—	±4.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 42.22 12-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 2: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 2 and 3.

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 50 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	1.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	6	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±6.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±6.0	LSB	
	Full-scale error	—	—	±6.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 42.23 Characteristics of the Programmable Gain Amplifier

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		C_{in}	—	—	8	pF	
Input offset voltage		V_{off}	—	—	8	mV	
Input voltage range (V_{in})	Gain × 2.000	V_{in}	0.050 × AVcc	—	0.450 × AVcc	V	
	Gain × 2.500		0.047 × AVcc		0.360 × AVcc		
	Gain × 3.077		0.045 × AVcc		0.292 × AVcc		
	Gain × 3.636		0.042 × AVcc		0.247 × AVcc		
	Gain × 4.000		0.040 × AVcc		0.212 × AVcc		
	Gain × 4.444		0.036 × AVcc		0.191 × AVcc		
	Gain × 5.000		0.033 × AVcc		0.170 × AVcc		
	Gain × 5.714		0.031 × AVcc		0.148 × AVcc		
	Gain × 6.667		0.029 × AVcc		0.127 × AVcc		
	Gain × 10.000		0.025 × AVcc		0.08 × AVcc		
	Gain × 13.333		0.023 × AVcc	—	0.06 × AVcc		
Slew rate		SR	10	—	—	V/µs	
Gain error	Gain × 2.000	—	—	—	1	%	
	Gain × 2.500		—	—	1		
	Gain × 3.077		—	—	1		
	Gain × 3.636		—	—	1.5		
	Gain × 4.000		—	—	1.5		
	Gain × 4.444		—	—	2		
	Gain × 5.000		—	—	2		
	Gain × 5.714		—	—	2		
	Gain × 6.667		—	—	3		
	Gain × 10.000		—	—	4		
	Gain × 13.333		—	—	4		

Table 42.24 Comparator Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	C_{in}	—	—	8	pF	
REFH pin offset voltage	V_{off}	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	V_{in}	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	t_{CR}	—	—	500	ns	VI = VREF±25mV
REFL reply time	t_{CF}	—	—	500	ns	

42.6 D/A Conversion Characteristics

Table 42.25 D/A Conversion Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

42.7 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 42.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.7	V	Figure 42.41
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.82	2.94		Figure 42.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	2.75	2.90	3.05		Figure 42.43
		V_{DET1_9}	2.70	2.85	3.00		
		V_{DET1_A}	2.73	2.88	3.03		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	2.75	2.9	3.05		Figure 42.44
		V_{DET2_9}	2.70	2.85	3.00		
		V_{DET2_A}	2.73	2.88	3.03		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 42.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 42.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 42.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 42.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 42.41 and Figure 42.42
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 42.41 to Figure 42.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

Table 42.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Condition: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 42.41
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 42.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 42.43
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 42.44
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 42.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 42.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 42.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 42.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 42.41 to Figure 42.44
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 42.41 to Figure 42.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

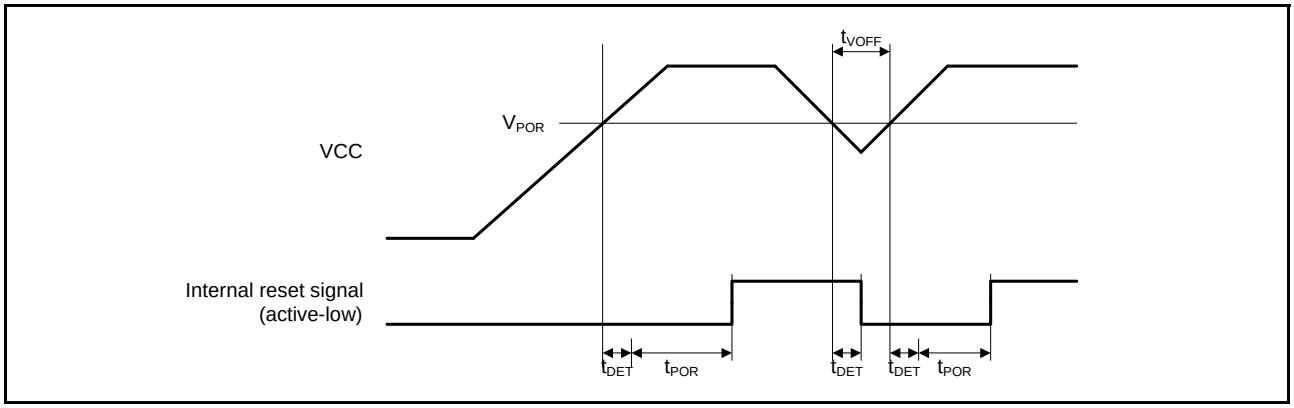


Figure 42.39 Power-on Reset Timing

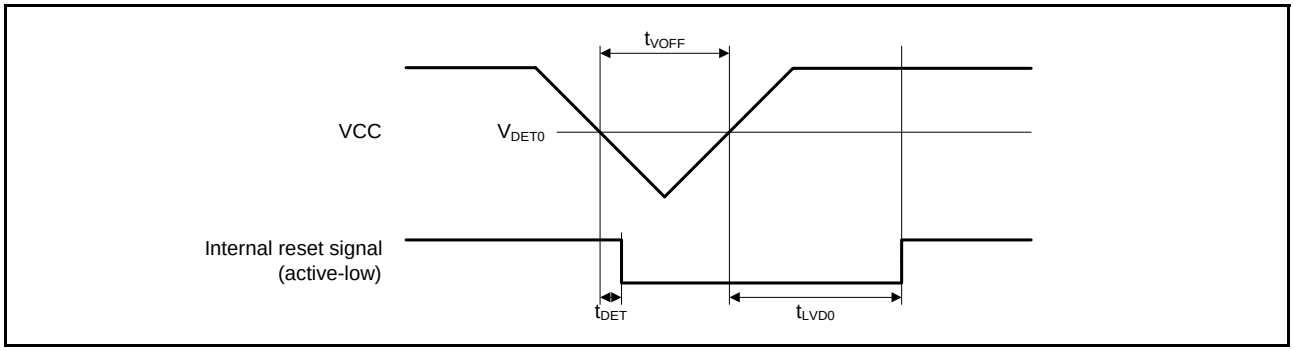


Figure 42.40 Voltage Detection Circuit Timing (V_{DET0})

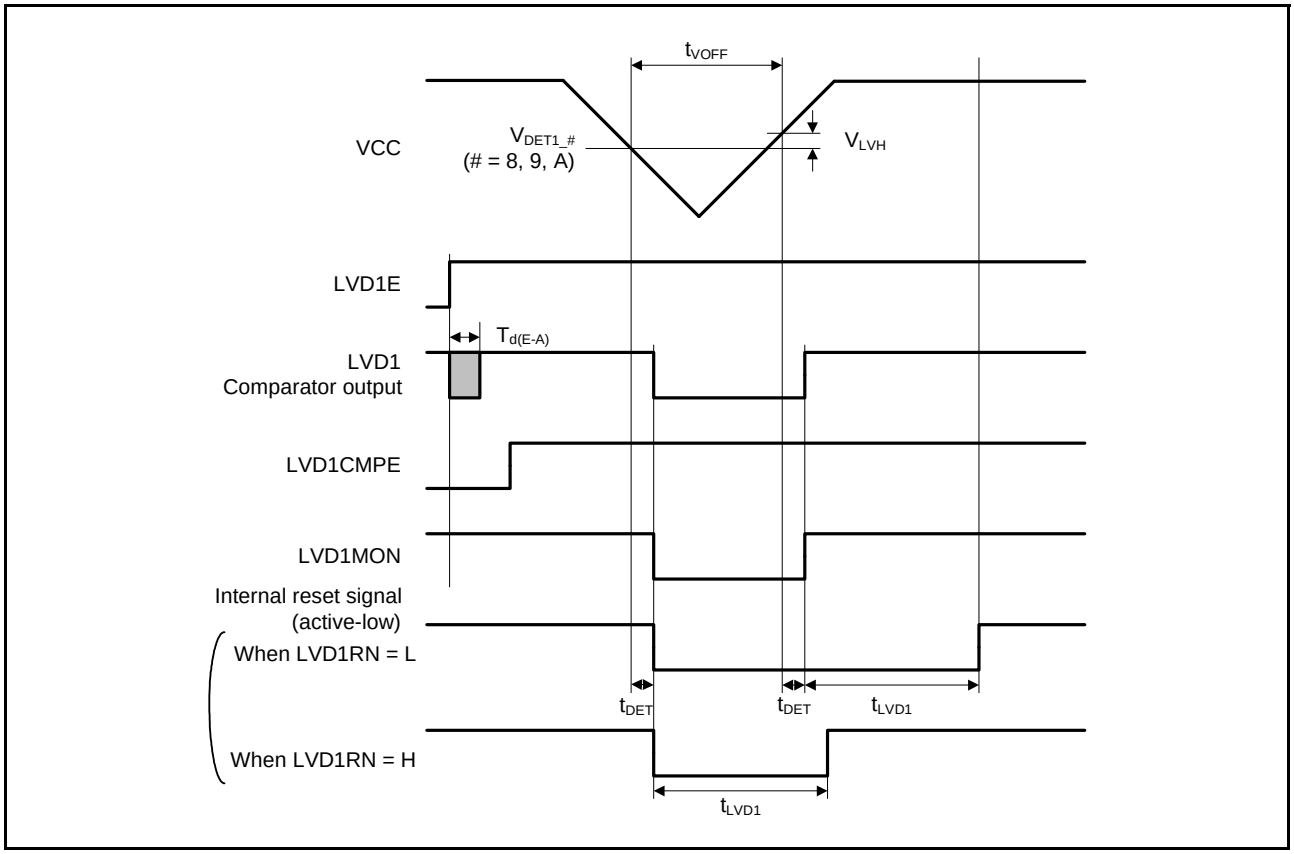


Figure 42.41 Voltage Detection Circuit Timing (V_{DET1})

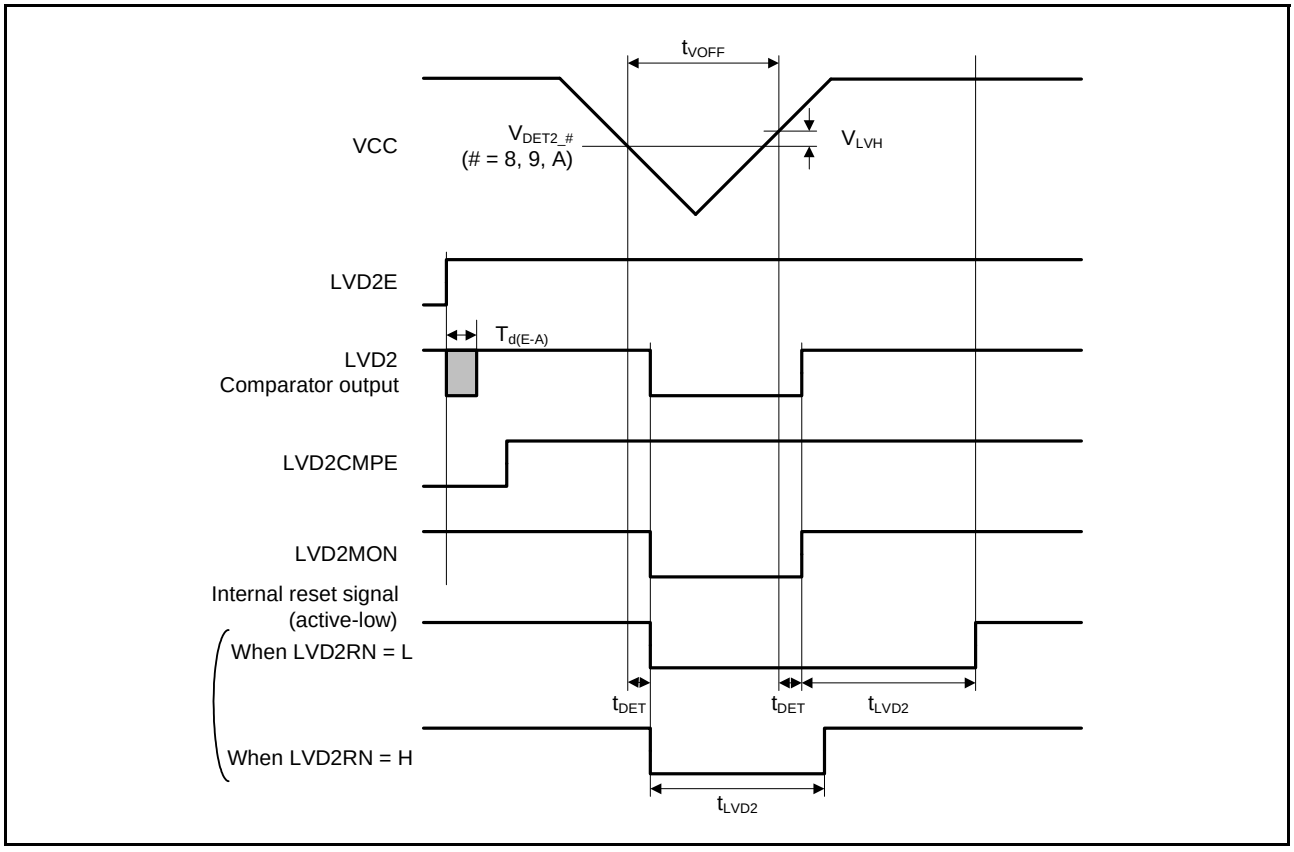


Figure 42.42 Voltage Detection Circuit Timing (V_{DET2})

42.8 Oscillation Stop Detection Circuit Characteristics

Table 42.28 Oscillation Stop Detection Circuit Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 42.43

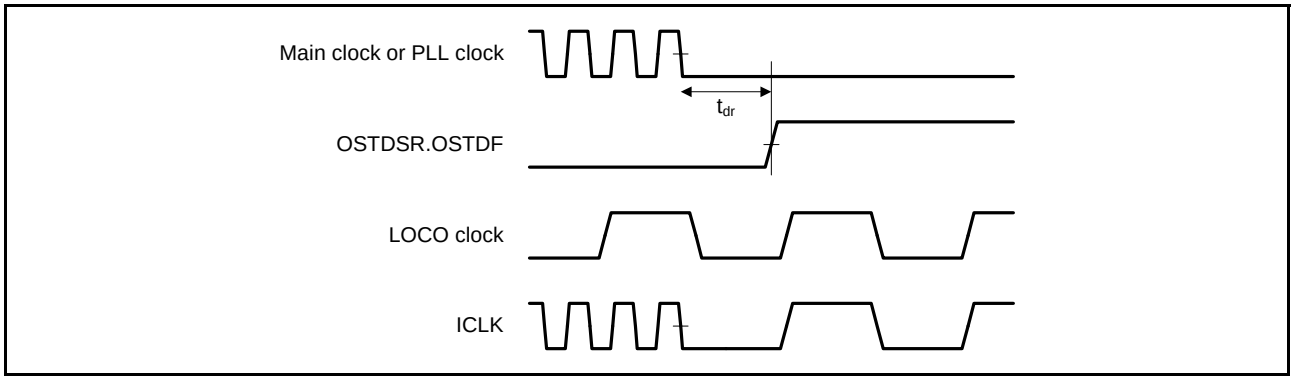


Figure 42.43 Oscillation Stop Detection Timing

42.9 ROM (Flash Memory for Code Storage) Characteristics

Table 42.29 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 42.30 ROM (Flash Memory for Code Storage) Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time $N_{PEC} \leq 100$ times	128 bytes	t_{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t_{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t_{P16K}	—	252	560	—	90	200	ms
Programming time $N_{PEC} > 100$ times	128 bytes	t_{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t_{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t_{P16K}	—	302.4	672	—	108	240	ms
Erasure time $N_{PEC} \leq 100$ times	4 Kbytes	t_{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t_{E16K}	—	200	480	—	100	240	ms
Erasure time $N_{PEC} > 100$ times	4 Kbytes	t_{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t_{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t_{SPD}	—	—	400	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	300	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t_{FCUR}	35	—	—	35	—	—	µs

42.10 E^2 Flash Characteristics

Table 42.31 E^2 Flash Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 42.32 E^2 Flash Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time $N_{DPEC} \leq 100$ times	2 bytes	t_{DP2}	—	0.7	6	—	0.25	2	ms
Programming time $N_{DPEC} > 100$ times	2 bytes	t_{DP2}	—	0.7	6	—	0.25	2	ms
Erasure time $N_{DPEC} \leq 100$ times	32 bytes	t_{DE32}	—	4	40	—	2	20	ms
Erasure time $N_{DPEC} > 100$ times	32 bytes	t_{DE32}	—	7	40	—	4	20	ms
Blank check time	2 bytes	t_{DBC2}	—	—	100	—	—	30	µs
Suspend delay time during programming		t_{DSPD}	—	—	250	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	250	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	500	—	—	300	µs
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	500	—	—	300	µs

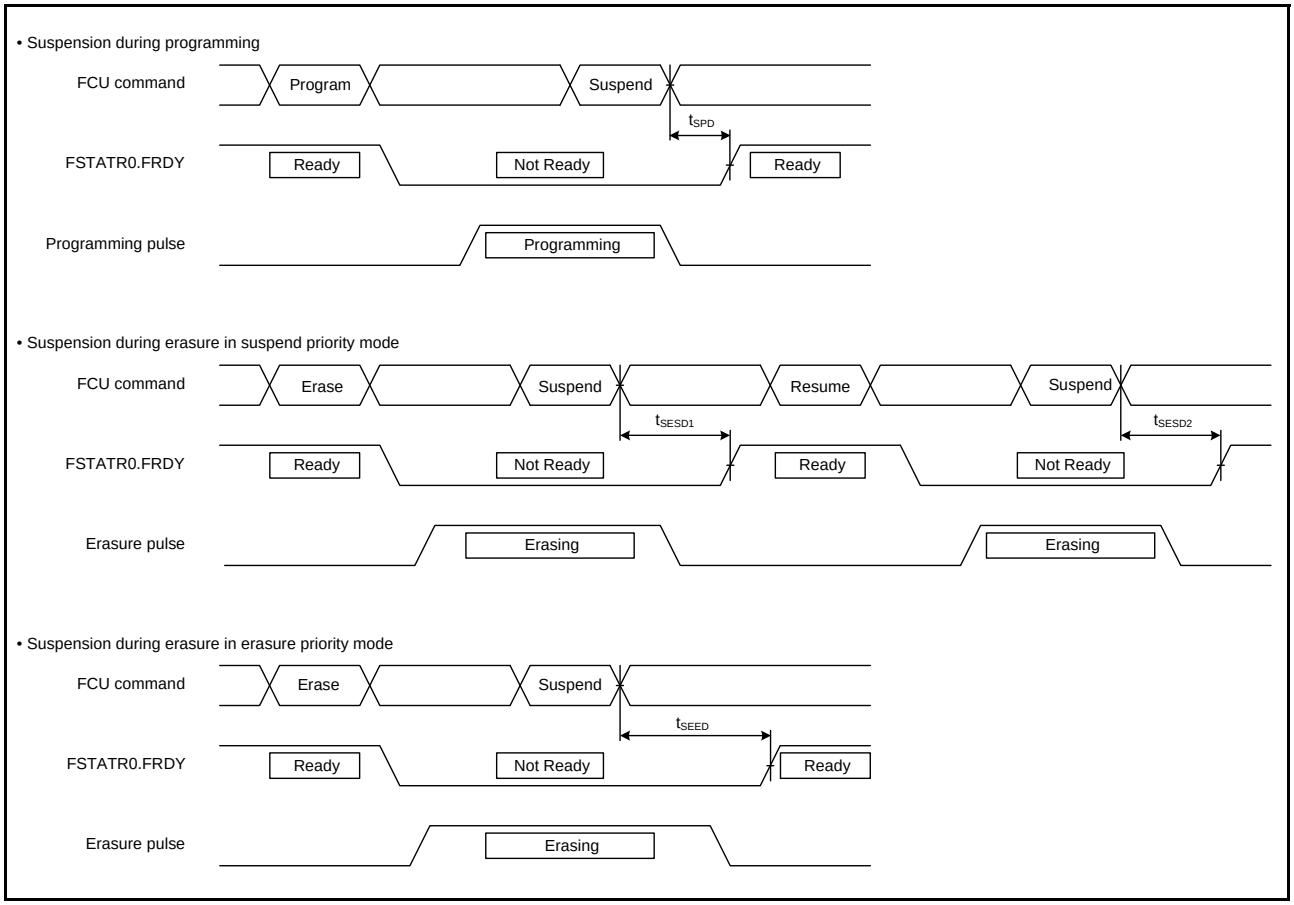


Figure 42.44 Flash Memory Program/Erase Suspend Timing

43. Electrical Characteristics [64- and 48-Pin Versions]

43.1 Absolute Maximum Ratings

Table 43.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1 and port 4)		Vin	–0.3 to VCC+0.3	V
Input voltage (port 4)		Vin	–0.3 to AVCC0+0.3	V
Input voltage (ports for 5 V tolerant)*1		Vin	–0.3 to +5.8	V
Analog power supply voltage		AVCC0*2	–0.3 to +4.6	V
Reference power supply voltage		VREFH0*2	–0.3 to AVCC0+0.3	V
Analog input voltage (port 4)		V_{AN}	–0.3 to AVCC0+0.3	V
Operating temperature	D version product	Topr	–40 to +85	°C
	G version product	Topr	–40 to +105	°C
Storage temperature		Tstg	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, and AVSS0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

43.2 DC Characteristics

Table 43.2 DC Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin GPT input pin RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (IICBus operating)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Port 4 (also used as an analog port)	V_{IH}	AVCC0 × 0.8	—	AVCC0 + 0.3		
		V_{IL}	–0.3	—	AVCC0×0.2		
	Ports for 5 V tolerant*1	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3		
	EXTAL, TCK, RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus operating)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, TCK, RSPI input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus operating)		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Ports 4 and PE2	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0V, V_{in} = VCC
Three-state leakage current (off state)	Ports for 5V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0V, V_{in} = 5.5 V
			—	—	5.0		
Input capacitance	All input pins (except for ports PB1 and PB2)	C_{in}	—	—	15	pF	V_{in} = 0V, f = 1 MHz, T_a = 25ºC
	Ports PB1 and PB2		—	—	30		

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

Table 43.3 DC Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	During operation	Max. *2	I_{CC}*3	—	—	60	mA	ICLK = 100MHz PCLKA = 100MHz PCLKB = 50MHz PCLKD = 50MHz FCLK = 50MHz
		Normal *4		—	25	—		
		Increased by BGO operation*5		—	15	—		
	Sleep mode				25	35		
	All-module-clock-stop mode*6				14	25		
	During standby	Software standby mode		—	0.2	6	mA	
		Deep software standby mode		—	16	40	µA	
Analog power supply current	During 12-bit A/D conversion (sample & hold circuit in use)		AI_{CC0}	—	3	4	mA	
	During 12-bit A/D conversion (sample & hold circuit not in use)			—	2	3	mA	
	Window comparator (1-channel operation)				0.4	1	mA	
	Window comparator (3-channel operation)			—	0.5	1	mA	
	Waiting for 12-bit AD conversion			—	25	32	µA	
Reference power supply current	During 12-bit A/D conversion		AI_{REFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion			—	0.6	0.7	mA	
VCC rising gradient			SrVcc	—	—	20000	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max = 0.45 × f + 15 (Max)
ICC typ = 0.18 × f + 7 (Normal)
ICC max = 0.22 × f + 13 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

Table 43.4 Permissible Output Currents

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	I_{OL}	—	—	2.0*1	mA
Permissible output low current (max. value per pin)	I_{OL}	—	—	4.0*1	mA
Permissible output low current (total)	ΣI_{OL}	—	—	32	mA
Permissible output high current (average value per pin)	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (max. value per pin)	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	$\Sigma-I_{OH}$	—	—	32	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in this table.
Note 1. RIIC pin: IOL = 6 mA (max.)

Table 43.5 Permissible Power Consumption (G version product only)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Total permissible power consumption*1	Pd	—	150	mW	85°C < Ta ≤ 105°C 64-pin version
	Pd	—	120	mW	85°C < Ta ≤ 105 °C 48-pin version

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 1. The total power consumption of the whole chip including output current.

43.3 AC Characteristics

Table 43.6 Operation Frequency Value

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock PCLK		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	Flash clock (FCLK)		—*1	—	50	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

43.3.1 Clock Timing

Table 43.7 Clock Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 43.1
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	4	—	16	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	—	—	—*2	ms	Figure 43.2
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	—	—	—*3	ms	
LOCO, IWDTCLK clock cycle time		t_{cyc}	6.96	8	9.4	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 43.2
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 43.4
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	—*4	ms	
PLL clock oscillation stabilization time PLL	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC}$ + t_{PLL1}	ms	Figure 43.5
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	—*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

Note 4. This is calculated from the formula below, where n is the number of cycles set by the PLLWTCR.PSTS[4:0] bits.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

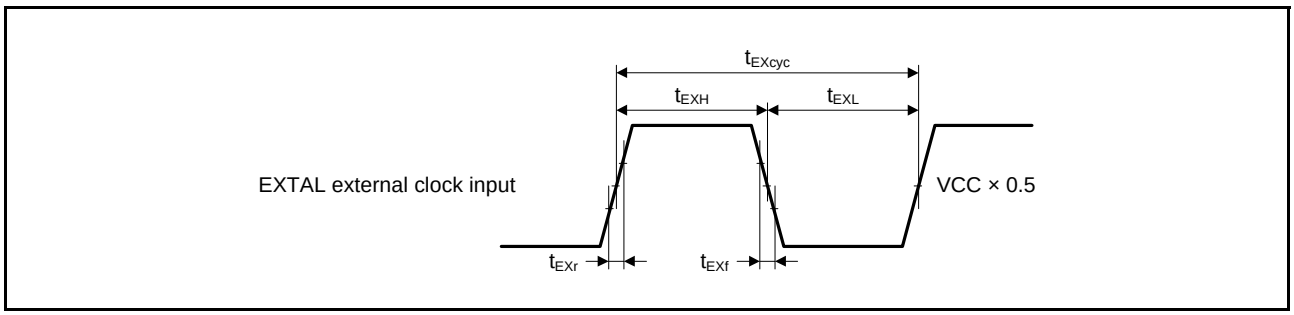


Figure 43.1 EXTAL External Clock Input Timing

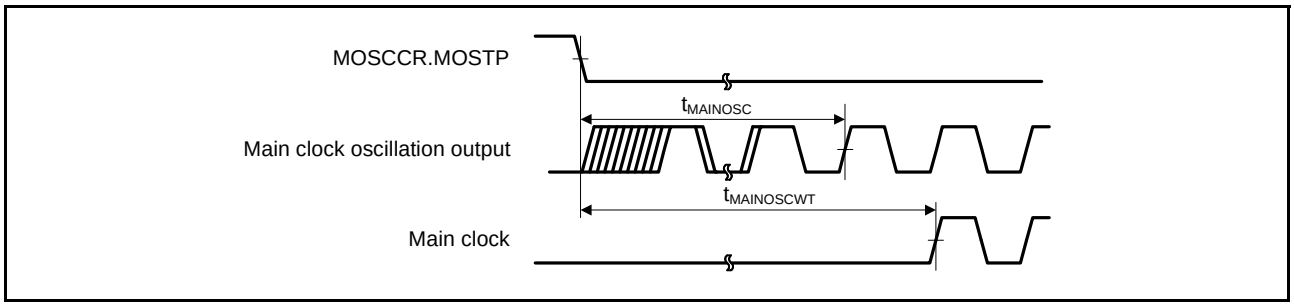


Figure 43.2 Main Clock Oscillation Start Timing

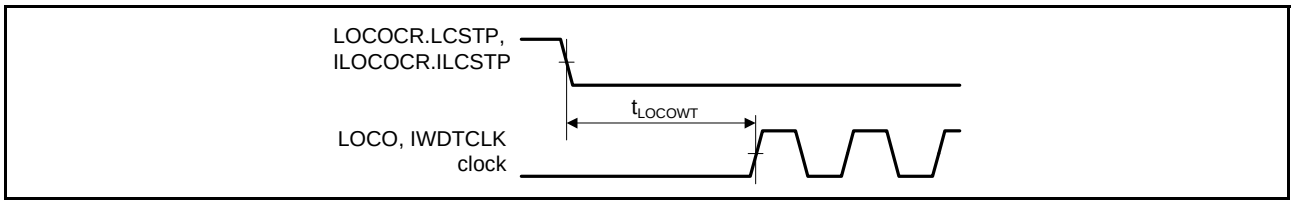


Figure 43.3 LOCO, IWDTCLK Clock Oscillation Start Timing

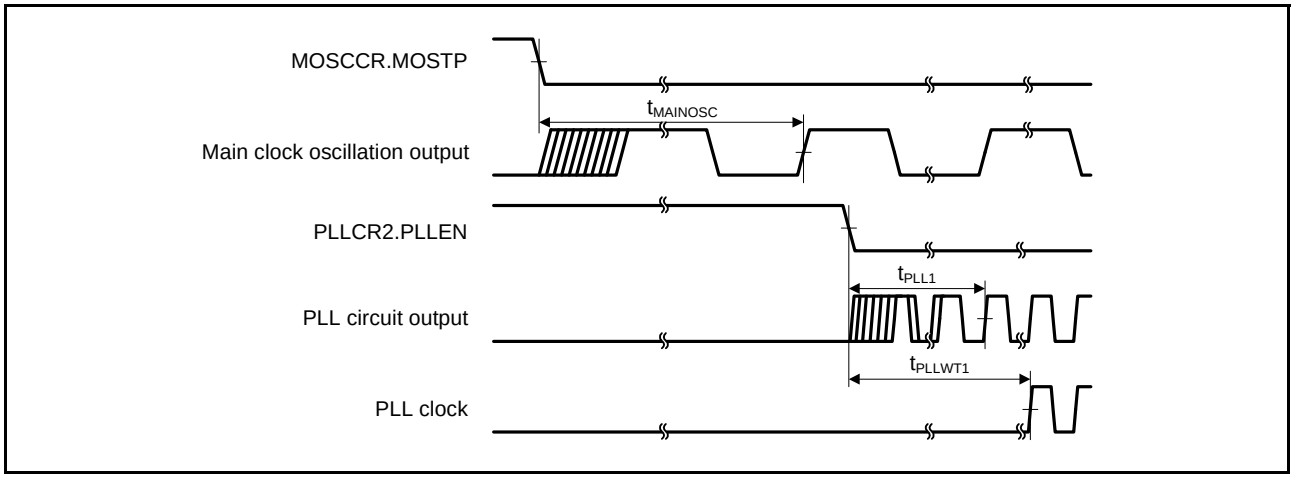


Figure 43.4 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

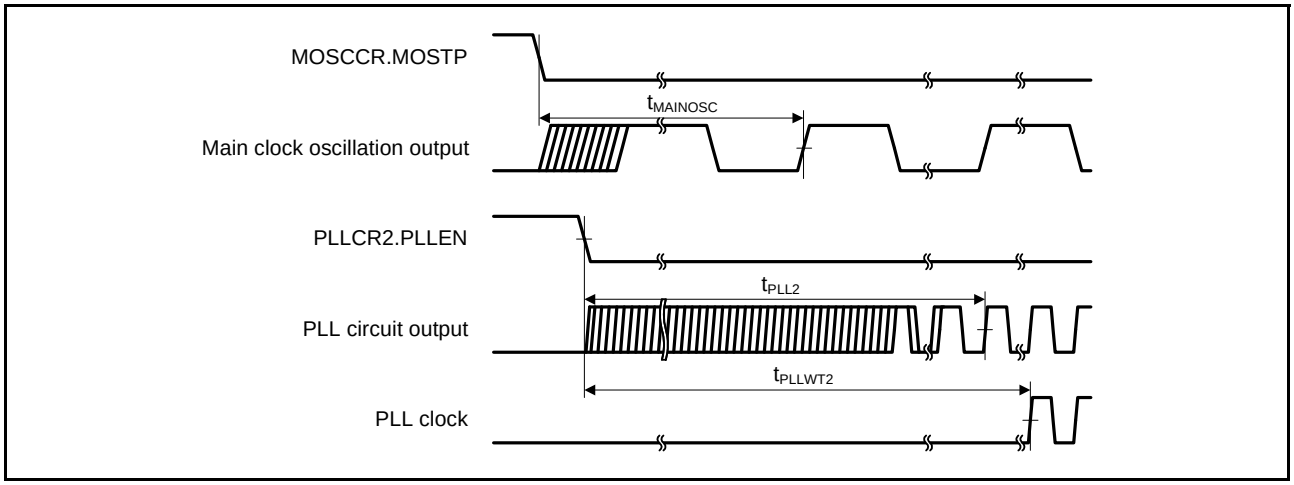


Figure 43.5 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

43.3.2 Reset Timing

Table 43.8 Reset Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 43.6
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 43.7
	Software standby mode	t_{RESWS}	1	—	—	ms	
	Other than above (except for programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory)	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{cyc}	
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{cyc}	

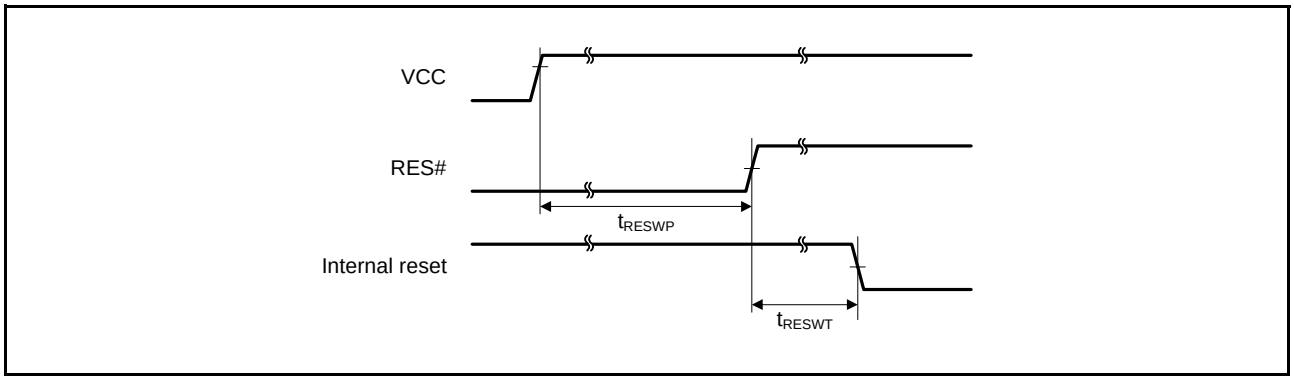


Figure 43.6 Reset Input Timing at Power-On

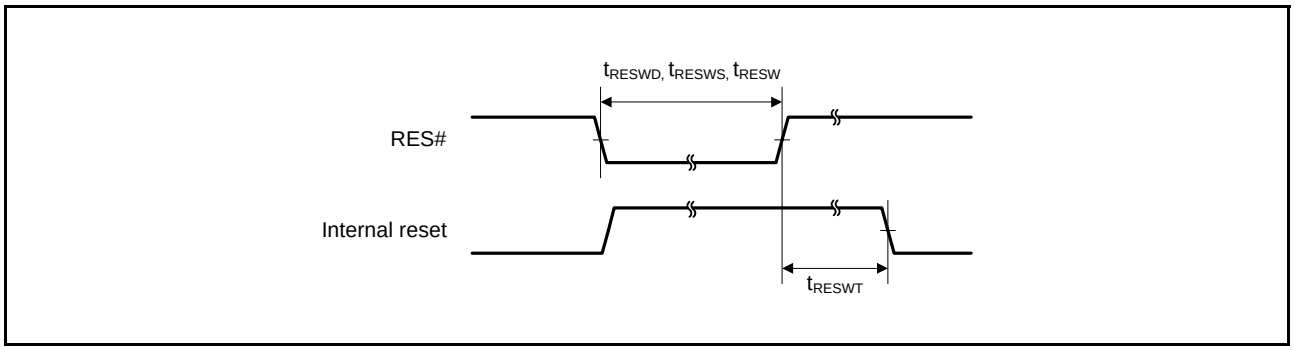


Figure 43.7 Reset Input Timing

43.3.3 Timing of Recovery from Low Power Consumption Modes

Table 43.9 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 43.8
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1	ms	Figure 43.9
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

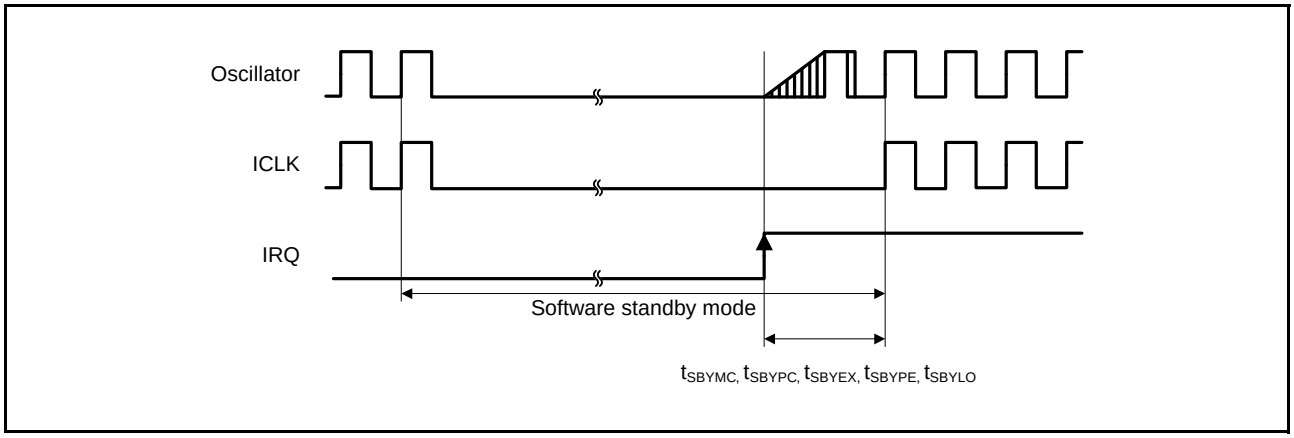


Figure 43.8 Software Standby Mode Cancellation Timing

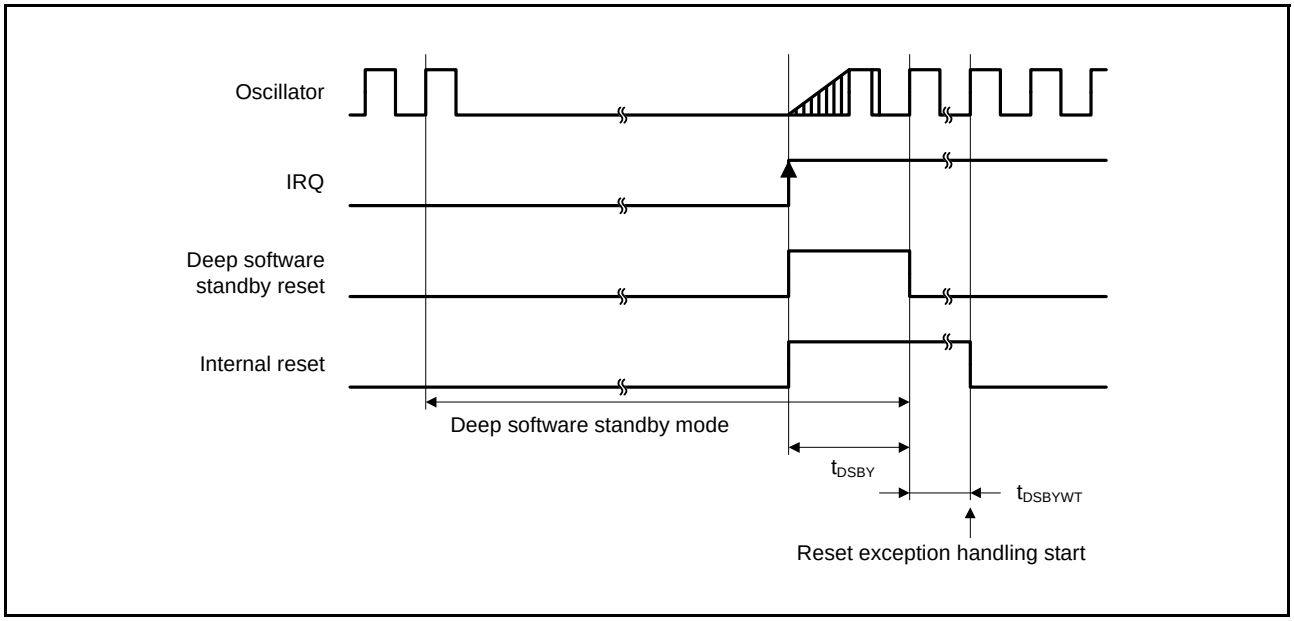


Figure 43.9 Deep Software Standby Mode Cancellation Timing

43.3.4 Control Signal Timing

Table 43.10 Control Signal Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 43.10
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 43.10
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 43.11
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 43.11

Note 1. t_{Pcyc}: PCLK cycle

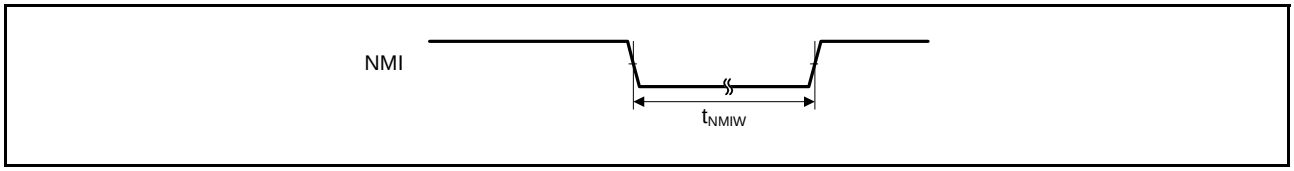


Figure 43.10 NMI Interrupt Input Timing

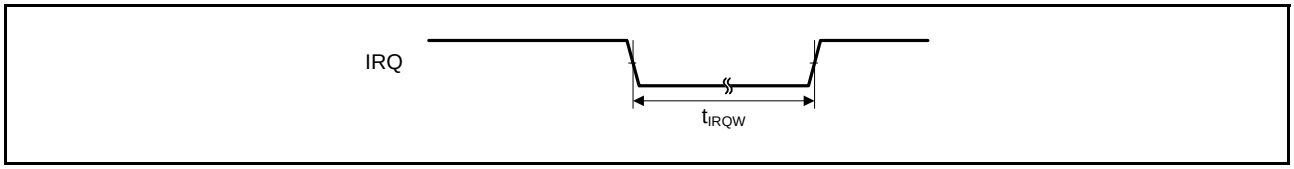


Figure 43.11 IRQ Interrupt Input Timing

43.3.5 Timing of On-Chip Peripheral Modules

Table 43.11 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 43.12
MTU3	Input capture input pulse width	Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 43.13
		Both-edge setting		5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 43.14
		Both-edge setting		5	—		
		Phase counting mode		5	—		
POE3	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 43.16
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PAcyc}	Figure 43.15
		Both-edge setting		5	—		
	External trigger input pulse width	Single-edge setting	t_{OTETW}	3	—	t_{PAcyc}	Figure 43.18
		Both-edge setting		5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 43.17
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 43.18
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 43.19

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcye}: PCLKA cycle

Table 43.12 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 43.20
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input		—	1	µs	
	Data input setup time	Master	t_{SU}	15	—	ns	Figure 43.21 to Figure 43.24
				20	—		
		Slave		$20 - t_{Pcyc}$	—		
	Data input hold time	Master	t_H	0	—	ns	
		Slave		$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	—	18	ns	
		Slave		—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	MISO rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	15	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	4	t_{Pcyc}	Figure 43.23 and Figure 43.24
	Slave output release time		t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 43.13 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 43.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 43.21 to Figure 43.24
	Data input hold time	t_{H}	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 43.23 and Figure 43.24
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 43.14 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 43.25
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle
Note 2. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 3. Cb is the total capacitance of the bus lines.

Table 43.15 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDAinput rise time	t_{Sr}	—	1000	ns	Figure 43.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

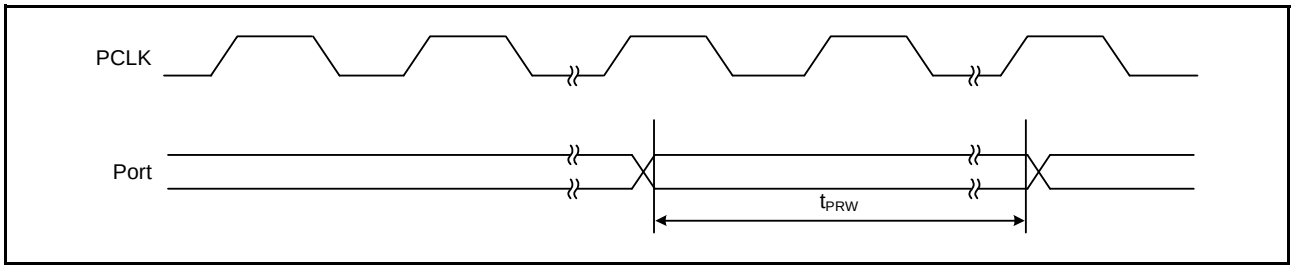


Figure 43.12 I/O port Input Timing

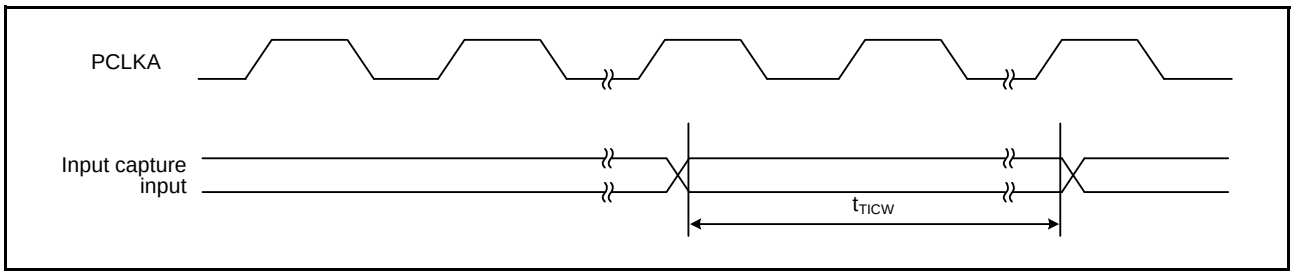


Figure 43.13 MTU3 Input/Output Timing

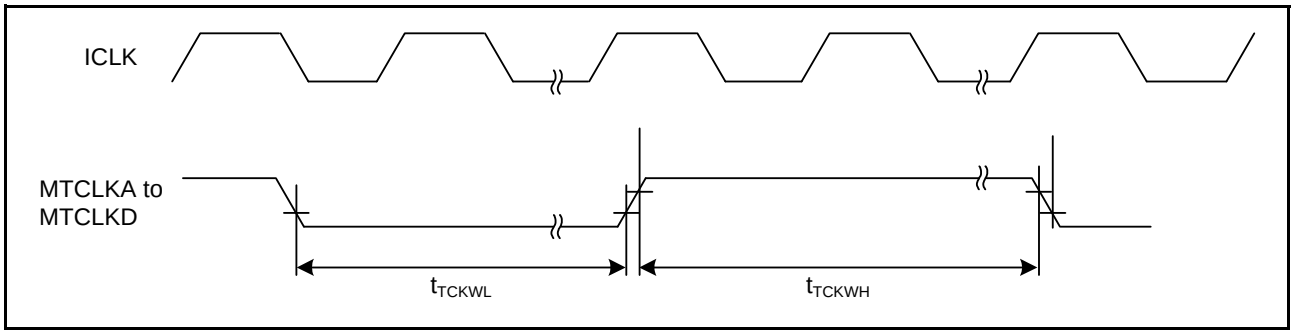


Figure 43.14 MTU3 Clock Input Timing

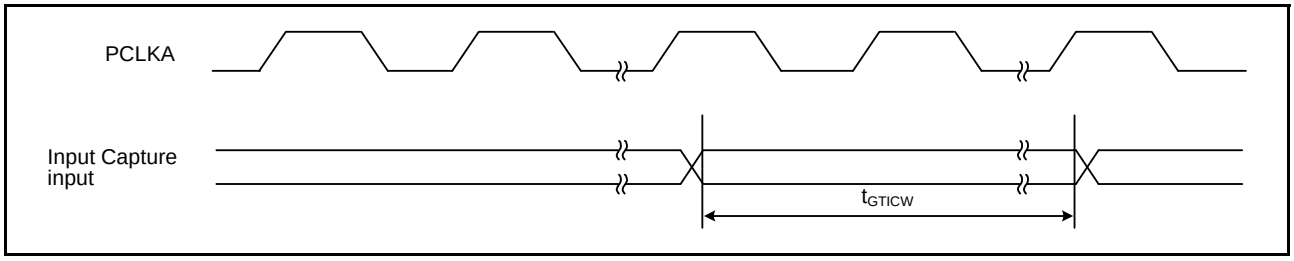


Figure 43.15 GPT Input/Output Timing

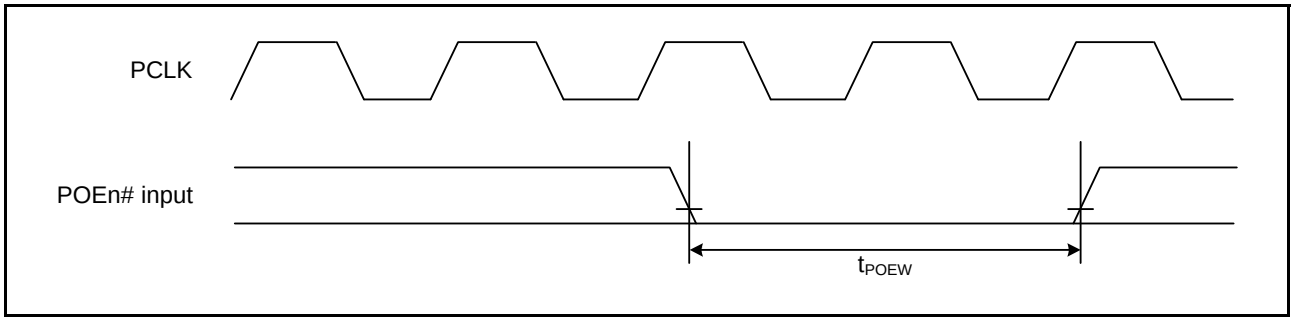


Figure 43.16 POE3# Input Timing

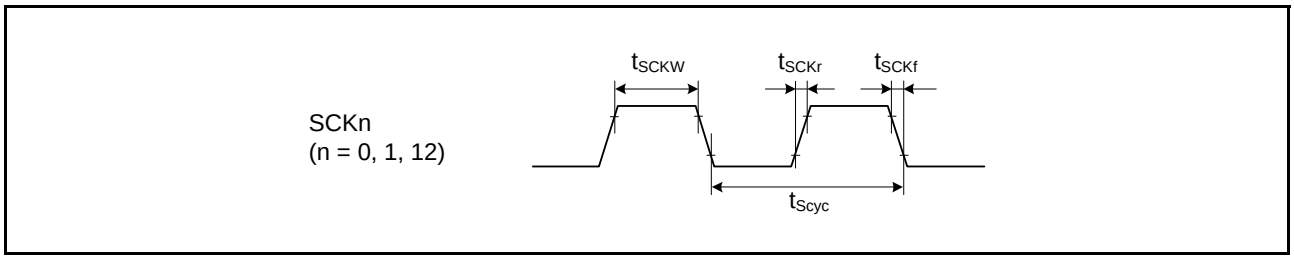


Figure 43.17 SCK Clock Input Timing

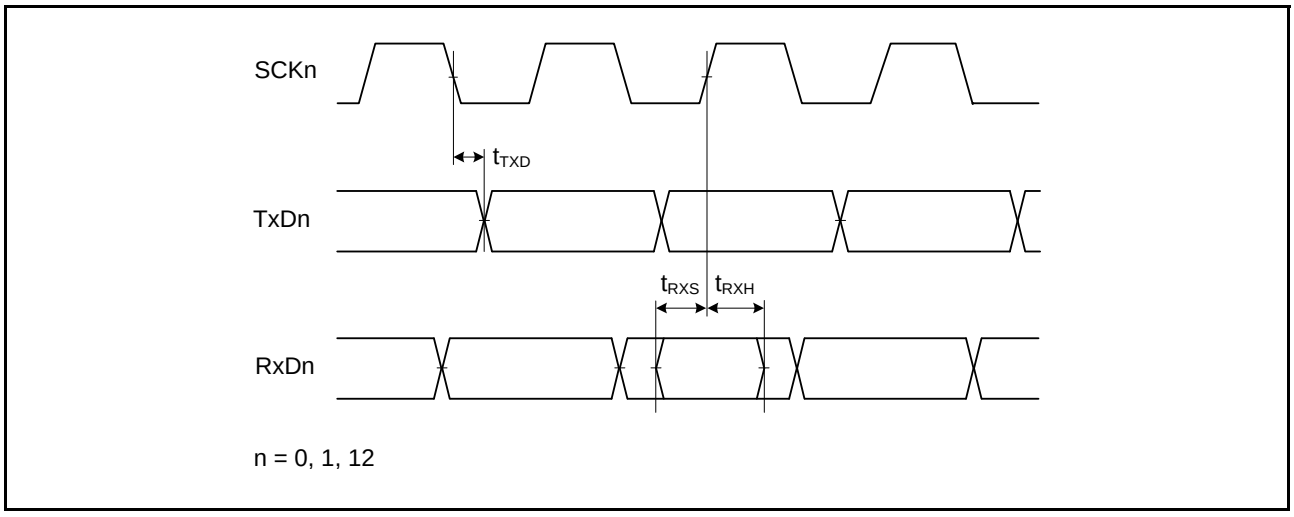


Figure 43.18 SCI Input/Output Timing: Clock Synchronous Mode

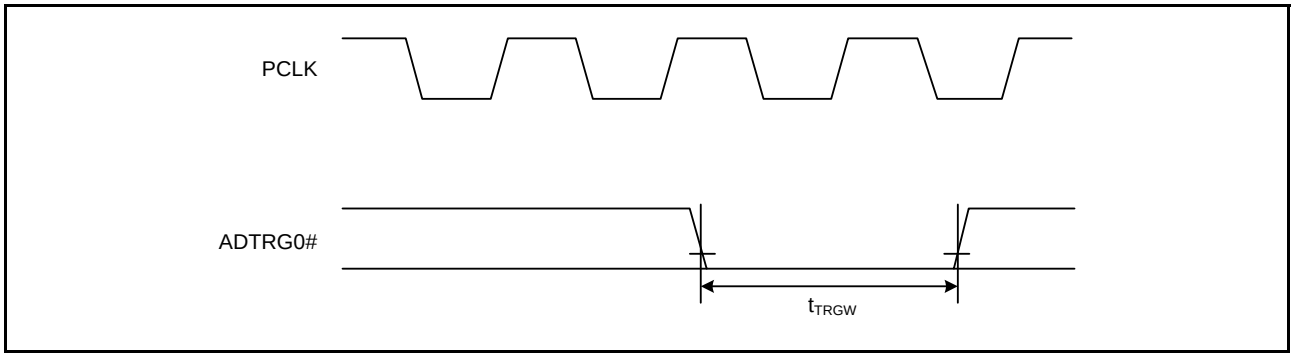


Figure 43.19 AD Converter External Trigger Input Timing

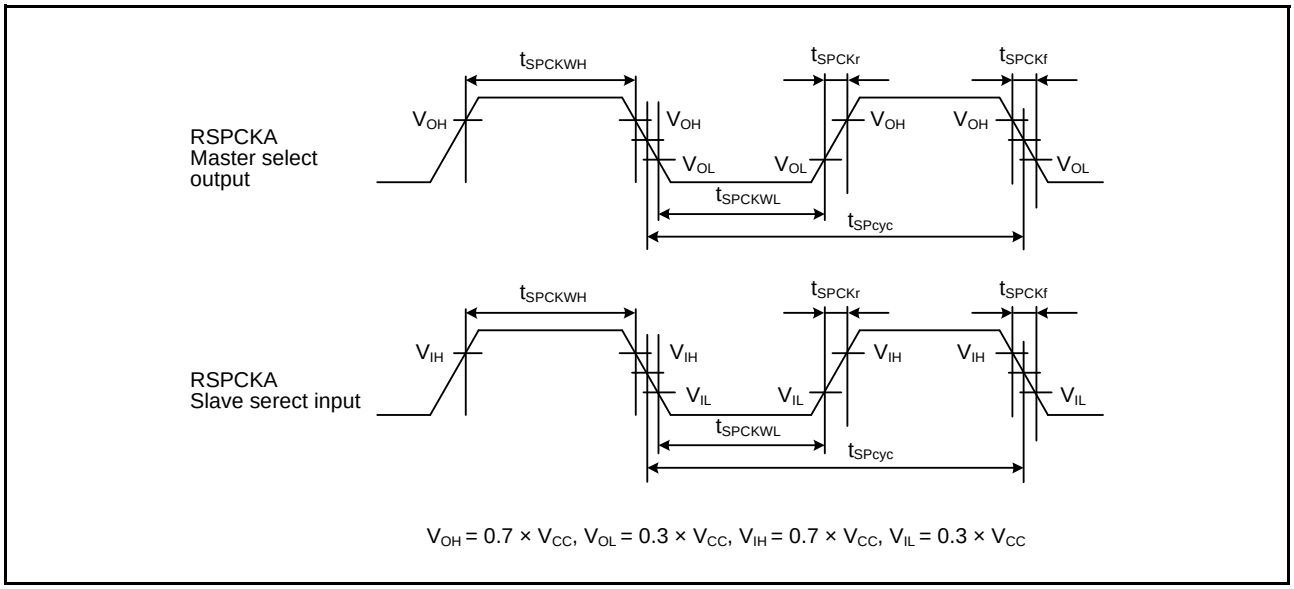


Figure 43.20 RSPI Clock Timing and Simple SPI Clock Timing

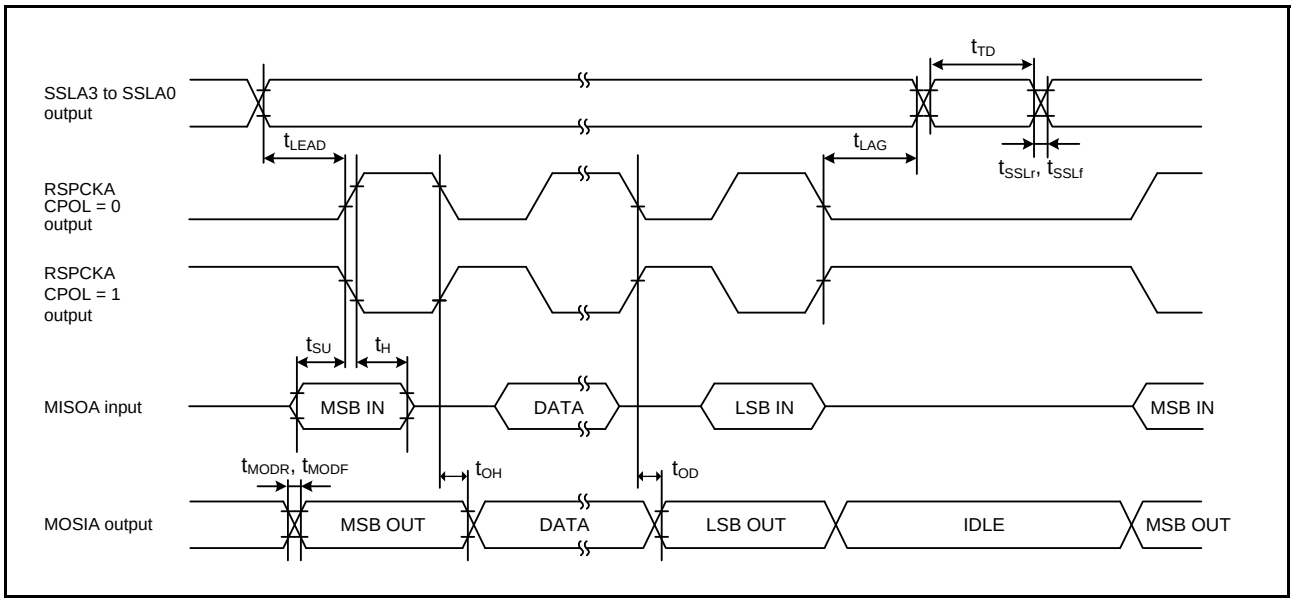


Figure 43.21 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

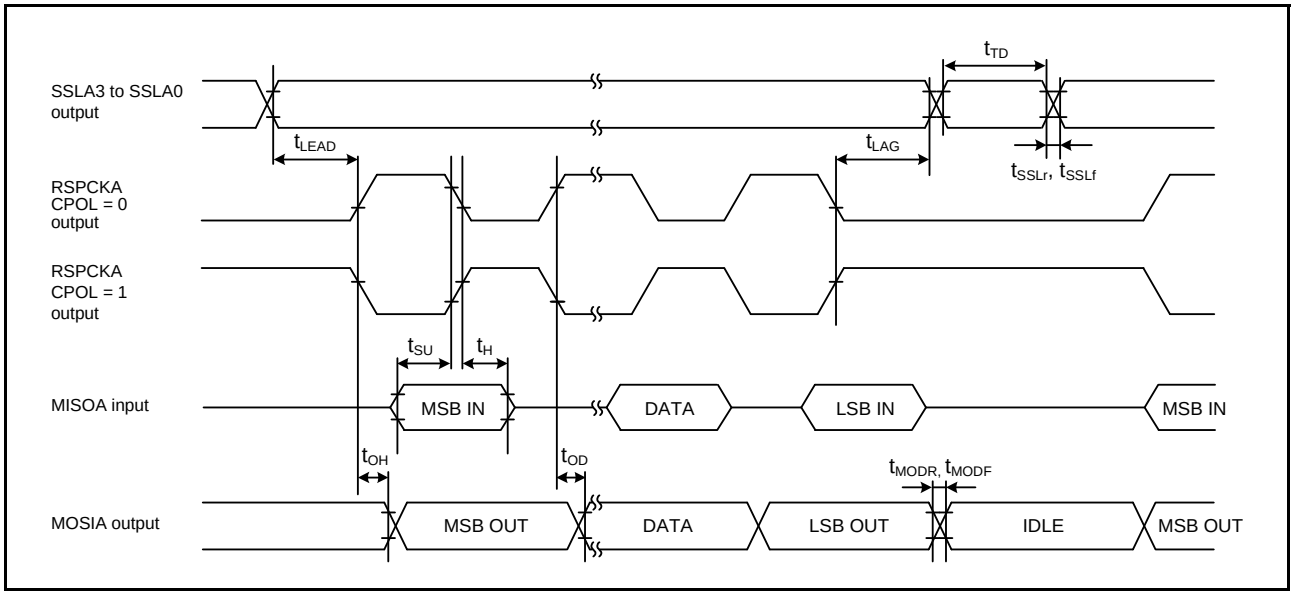


Figure 43.22 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

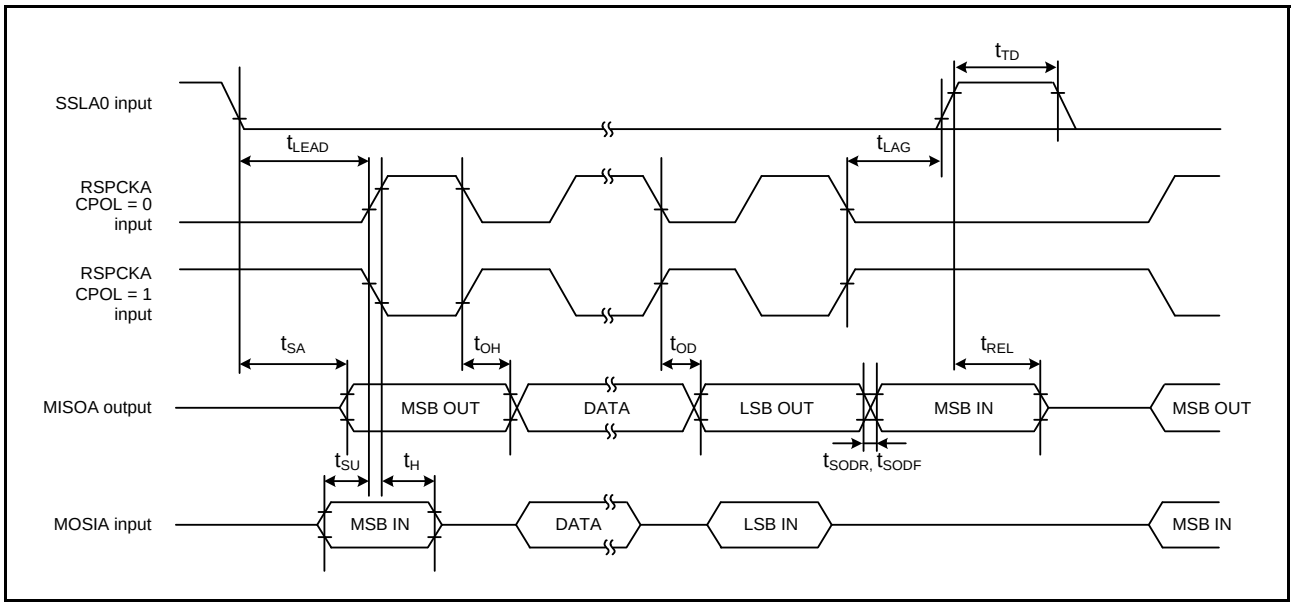


Figure 43.23 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

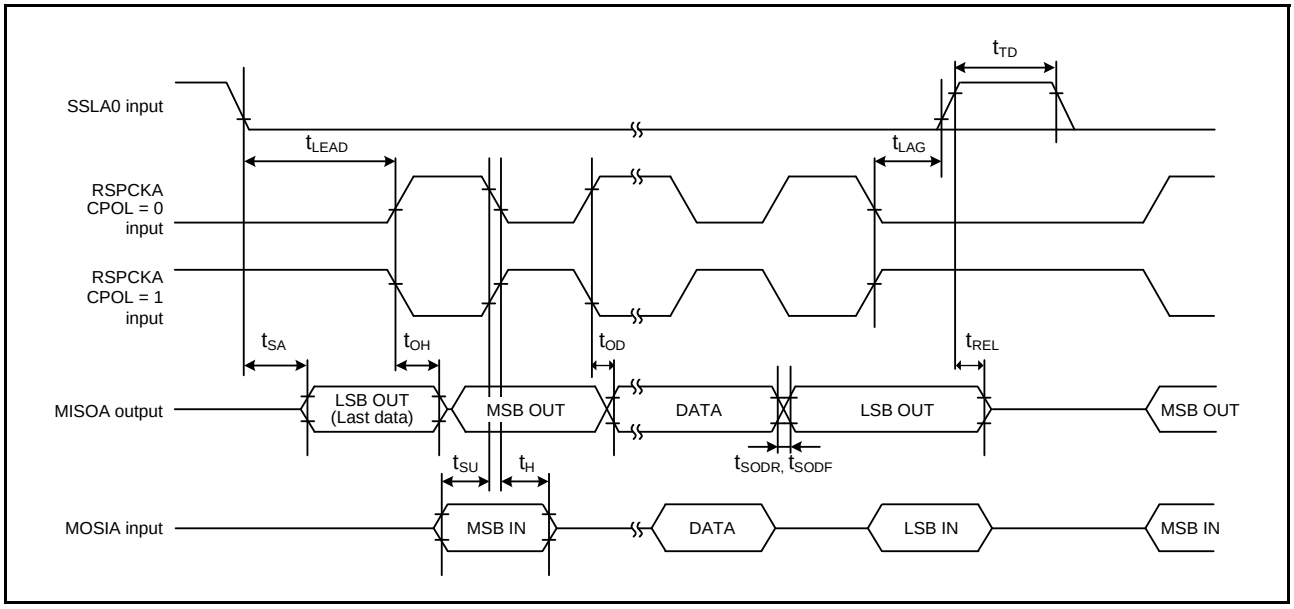
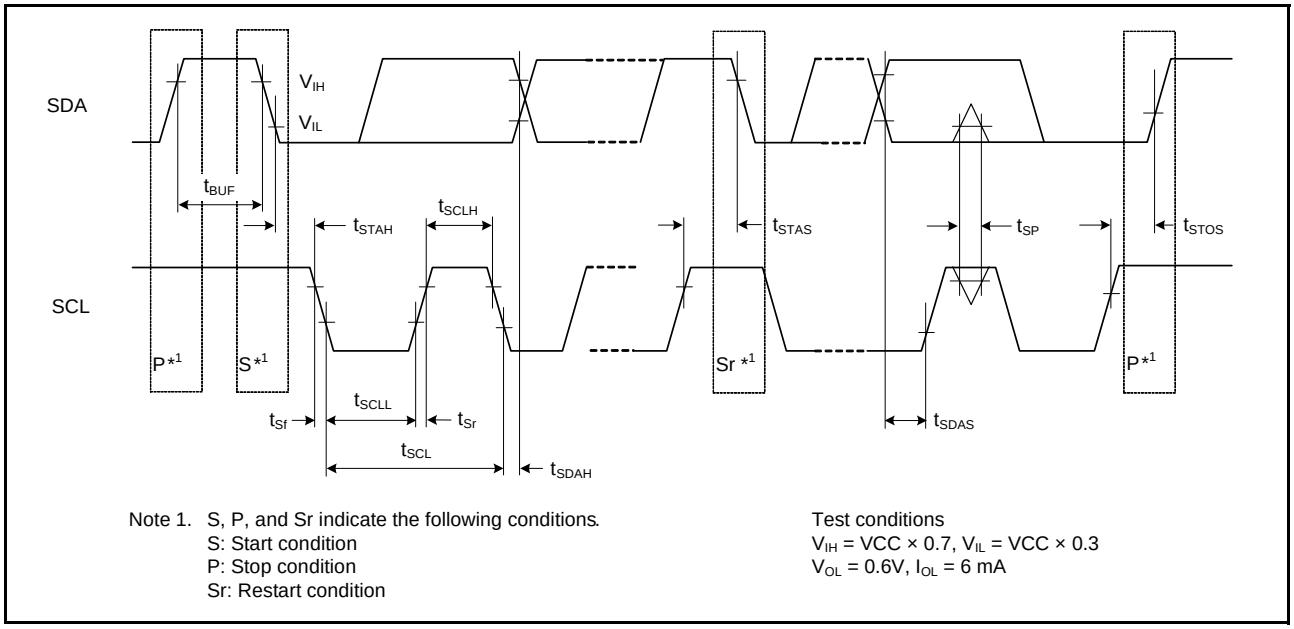


Figure 43.24 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6V, I_{OL} = 6 mA

Figure 43.25 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

43.4 A/D Conversion Characteristics

Table 43.16 12-Bit A/D Conversion Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		min	typ	max	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time *1 (ADCLK = 50 MHz)	When the sample-and-hold circuit is in use per pin	1.6	—	—	µs	Sampling by the sample-and-hold circuit in 30 states. Sampling by the A/D converter in 20 states.
	When the sample-and-hold circuit is not in use per pin	1.0	—	—	µs	Sampling by the A/D converter in 20 states.
Analog input capacitance		—	—	6	pF	
Integral nonlinearity error		—	—	±4.0	LSB	
Offset error		—	—	±7.5	LSB	
Full-scale error		—	—	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample and hold circuit in use	—	—	±8.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Sample and hold circuit not in use	—	—	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		—	—	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 43.17 Comparator Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min	Typ	Max.	Unit	Test Conditions
Analog input capacitance	Cin	—	—	6	pF	
REFH pin offset voltage	Voff	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	Vin	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	tCR	—	—	0.5	µs	
REFL reply time	tCF	—	—	0.5	µs	

43.5 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 43.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.5	2.6	2.7	V	Figure 43.26
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.8	2.9		Figure 43.27
	Voltage detection circuit (LVD1)	V_{DET1}	2.80	2.95	3.10		
	Voltage detection circuit (LVD2)	V_{DET2}	2.80	2.95	3.10		
Internal reset time	Power-on reset (POR)	t_{POR}	—	4.6		ms	Figure 43.26
	Voltage detection circuit (LVD0)	t_{LVD0}	—	4.6			Figure 43.27
	Voltage detection circuit (LVD1)	t_{LVD1}	—	0.9			Figure 43.28
	Voltage detection circuit (LVD2)	t_{LVD2}	—	0.9			Figure 43.29
Minimum VCC down time*1		t_{VOFF}	200	—	—	µs	Figure 43.26, Figure 43.27
Response delay time		t_{det}			200	µs	Figure 43.26 to Figure 43.29
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 43.28 Figure 43.29
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

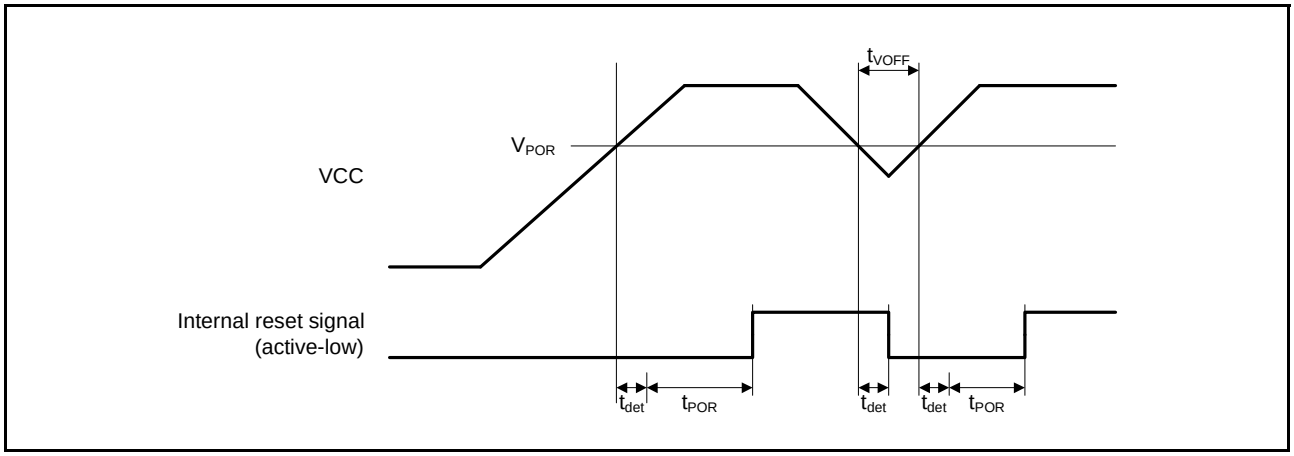


Figure 43.26 Power-on Reset Timing

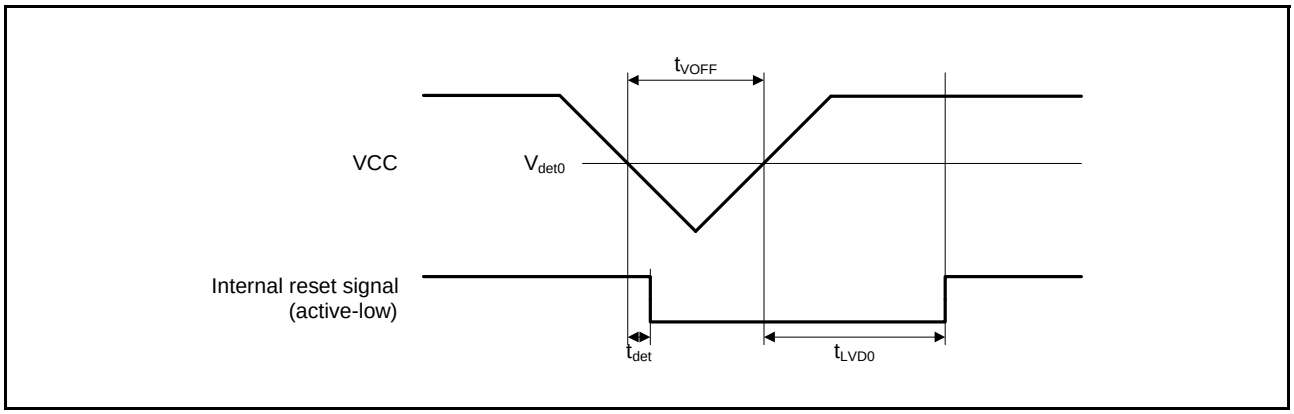


Figure 43.27 Voltage Detection Circuit Timing (V_{det0})

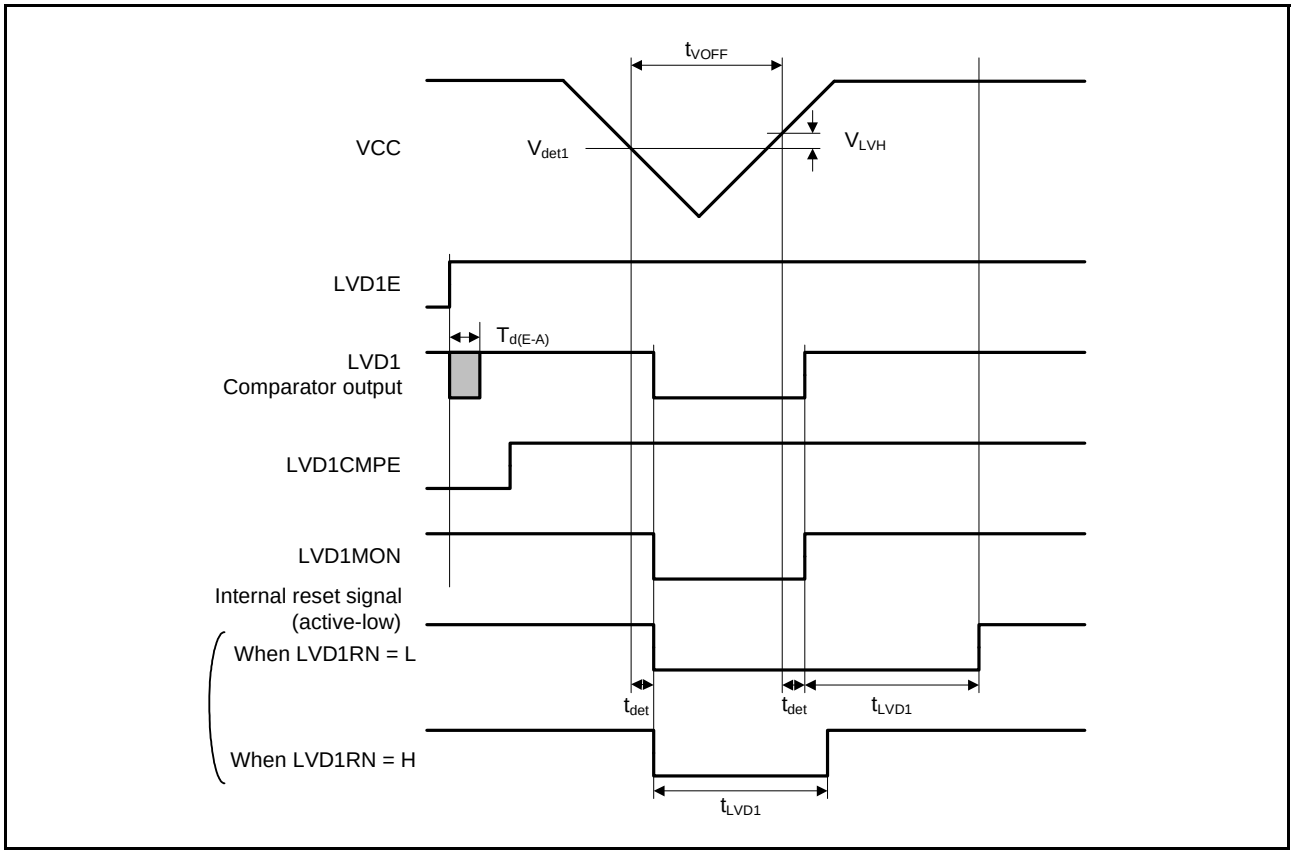


Figure 43.28 Voltage Detection Circuit Timing (V_{det1})

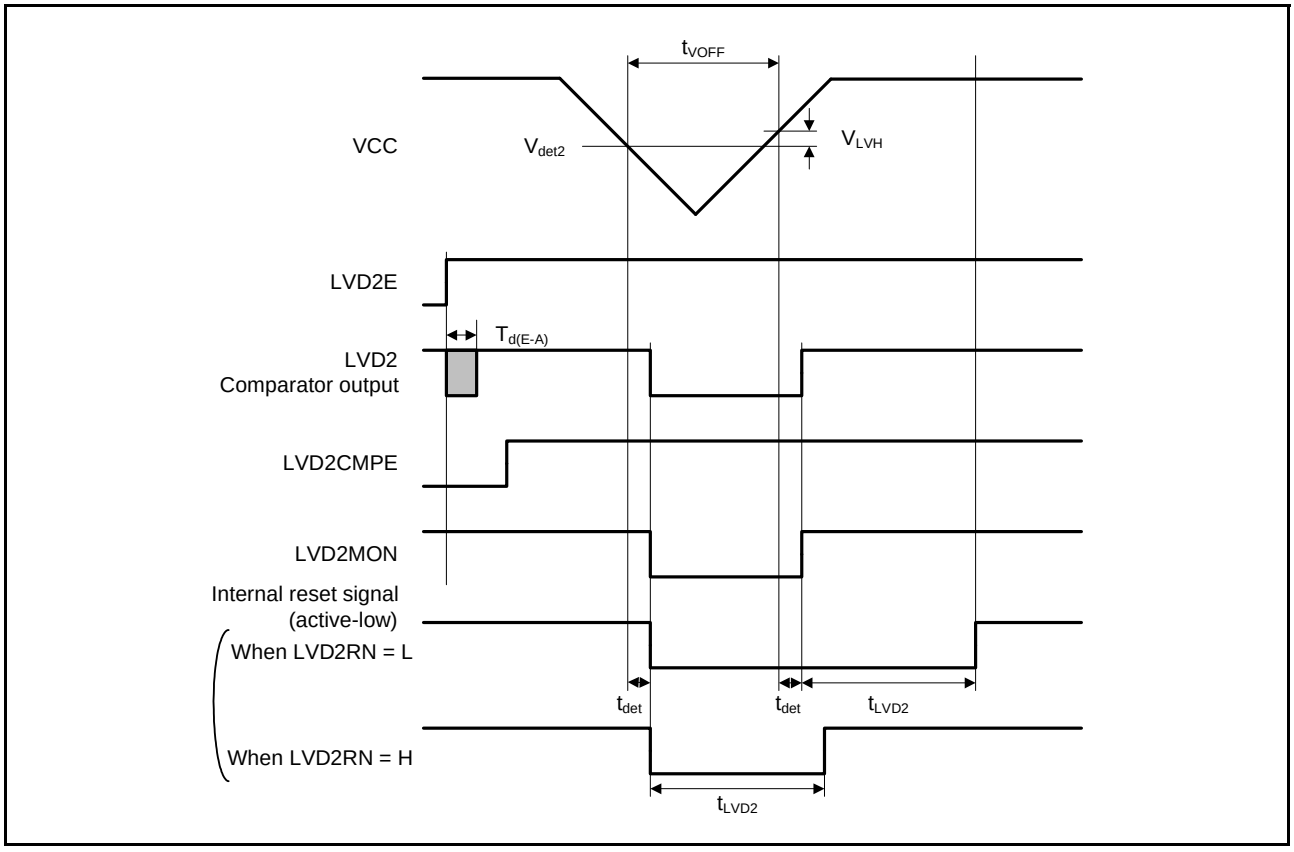


Figure 43.29 Voltage Detection Circuit Timing (V_{det2})

43.6 Oscillation Stop Detection Circuit Characteristics

Table 43.19 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V, AVCC0 = 3.0 to 3.6 V,
VREFH0 = 3.0 V to AVCC0, Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 43.30

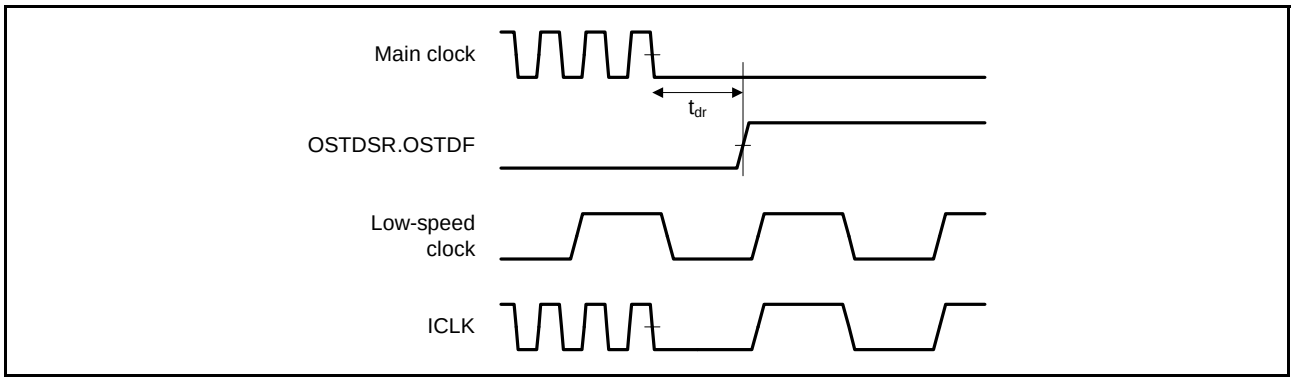


Figure 43.30 Oscillation Stop Detection Timing

43.7 ROM (Flash Memory for Code Storage) Characteristics

Table 43.20 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 43.21 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	min	typ	max	Unit	Test Conditions
Programming time	128 bytes	t_{P128}	—	1	10	ms	FCLK = 50MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	128 bytes	t_{P128}	—	1.2	12	ms	FCLK=50MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	FCLK=50MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	FCLK=50MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during programming		t_{SPD}	—	—	120	µs	Figure 43.31 FCLK = 50MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
FCU reset time		t_{FCUR}	35	—	—	µs	

43.8 E^2 DataFlash Characteristic

Table 43.22 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 43.23 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t_{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t_{DE32}	—	2	20	ms	FCLK = 50 MHz $N_{DPEC} \leq 100$
	32 bytes	t_{DE32}	—	4	20	ms	FCLK = 50 MHz $N_{DPEC} > 100$
Blank check time	2 bytes	t_{DBC2}	—	—	30	µs	FCLK = 50 MHz
Suspend delay time during programming		t_{DSPD}	—	—	120	µs	Figure 43.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	300	µs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	µs	

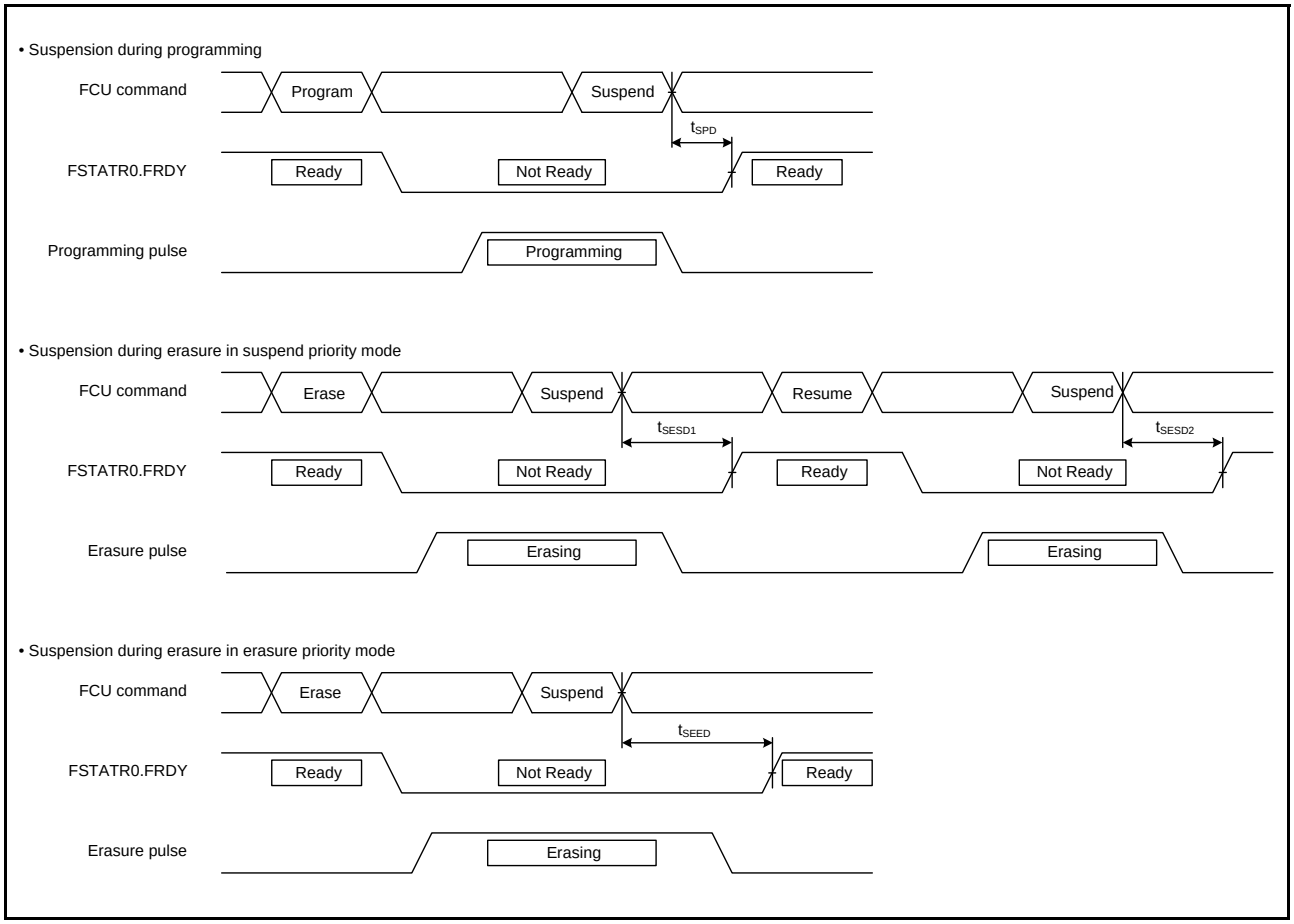


Figure 43.31 Flash Memory Program/Erase Suspend Timing

Appendix 1. Port States in Each Processing Mode

[144-, 120-, 112- and 100-Pin Versions]

Table 1.1 Port States in Each Processing State (1/4)

Port Name Pin Name	Operating Mode According to Registers Setting	Reset	Software Standby Mode		Deep Software Standby Mode IOKEEP = 1/0	After Deep Software Standby Mode is Canceled (Return of Start-up Mode)	
			OPE = 1	OPE = 0		IOKEEP = 1*1	IOKEEP = 0
P00/CS1#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O	[CS output] Hi-Z [Other than the above] Keep-O			
P01/RD#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[RD# output] H	[RD# output] Hi-Z			
P02	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
P03/IRQ7	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
P04, P05	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
P10/IRQ0-DS	All	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
P11/IRQ1-DS/ALE	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[ALE output] L [Other than the above] Keep-O*2	[ALE output] Hi-Z [Other than the above] Keep-O*2			
P12/CS3#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O	[CS output] Hi-Z [Other than the above] Keep-O			
P13, P14	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
P20/IRQ7-DS/D15, P21/IRQ6-DS/D14	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Data output] Hi-Z [Other than the above] Keep-O*2				
P22/D13, P23/D12	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Data output] Hi-Z [Other than the above] Keep-O				
P24/IRQ4/D11	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Data output] Hi-Z [Other than the above] Keep-O*2				
P25/CS1#, P26/CS0#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O	[CS output] Hi-Z [Other than the above] Keep-O			
P30/D10, P31/D9, P32/D8, P33/D7	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Data output] Hi-Z [Other than the above] Keep-O				
P34/IRQ3	All	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
P35	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
Port 4	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
P50, P51	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
P52/A7, P53/A6	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Address output retained [Other than the above] Keep-O*2			

Table 1.1 Port States in Each Processing State (2/4)

Port Name Pin Name	Operating Mode According to Registers Setting	Reset	Software Standby Mode		Deep Software Standby Mode IOKEEP = 1/0	After Deep Software Standby Mode is Canceled (Return of Start-up Mode)	
			OPE = 1	OPE = 0		IOKEEP = 1*1	IOKEEP = 0
P54, P55, P56, P57	All	Hi-Z	Keep-O		Keep	Keep	Hi-Z
P60/A0, P61/A1, P62/A2, P63/A3, P64/A4, P65/A5	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained	[Address output] Hi-Z			
P70/IRQ5-DS/D6	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Data output] Hi-Z [Other than the above] Keep-O*2				
P71/D5, P72/D4, P73/D3, P74/D2, P75/D1, P76/D0	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Data output] Hi-Z [Other than the above] Keep-O				
P80/IRQ5/A9	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Hi-Z [Other than the above] Keep-O*2			
P81/A8	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Hi-Z [Other than the above] Keep-O*2			
P82/IRQ3	All	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
P90 to P95	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
P96/IRQ4-DS/A13	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Hi-Z [Other than the above] Keep-O*2			
PA0 to PA5	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PA6/CS3#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O	[CS output] Hi-Z [Other than the above] Keep-O			
PB0/A14	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O	[Address output] Hi-Z [Other than the above] Keep-O			
PB1/IRQ4	All	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
PB2	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PB3/A15	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O	[Address output] Hi-Z [Other than the above] Keep-O			
PB4/IRQ3-DS/A16	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Hi-Z [Other than the above] Keep-O*2			
PB5/A17	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z

Table 1.1 Port States in Each Processing State (3/4)

Port Name Pin Name	Operating Mode According to Registers Setting	Reset	Software Standby Mode		Deep Software Standby Mode IOKEEP = 1/0	After Deep Software Standby Mode is Canceled (Return of Start-up Mode)	
			OPE = 1	OPE = 0		IOKEEP = 1*1	IOKEEP = 0
PB6/IRQ2/A18	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Hi-Z [Other than the above] Keep-O*2			
PB7/A19	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O	[Address output] Hi-Z [Other than the above] Keep-O			
PC0 to PC5	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PD0/A12	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O	[Address output] Hi-Z [Other than the above] Keep-O			
PD1/CS0#, PD2/CS2#	All	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O	[CS output] Hi-Z [Other than the above] Keep-O			
PD3, PD4	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PD5/IRQ6	All	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
PD6, PD7	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PE0/IRQ7/WR1/BC1/ CRX1-DS	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[WR1#/BC1# output] H [Other than the above] Keep-O*2	[WR1#/BC1# output] Hi-Z [Other than the above] Keep-O*2			
PE1/WR0#/WR#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[WR0#/WR# output] H	[WR0#/WR# output] Hi-Z			
PE2/NMI	All	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
PE3/IRQ2-DS/A11	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O*3	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Hi-Z [Other than the above] Keep-O*2			
PE4/IRQ1/A10	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Address output] Address output retained [Other than the above] Keep-O*2	[Address output] Hi-Z [Other than the above] Keep-O*2			
PE5/IRQ0/BCLK	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[Clock output] H [Other than the above] Keep-O*2				
PF0, PF1	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PF2/IRQ5/CS1#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O*2		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O*2	[CS output] Hi-Z [Other than the above] Keep-O*2			
PF3	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z

Table 1.1 Port States in Each Processing State (4/4)

Port Name Pin Name	Operating Mode According to Registers Setting	Reset	Software Standby Mode		Deep Software Standby Mode IOKEEP = 1/0	After Deep Software Standby Mode is Canceled (Return of Start-up Mode)	
			OPE = 1	OPE = 0		IOKEEP = 1*1	IOKEEP = 0
PF4/CS3#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O	[CS output] Hi-Z [Other than the above] Keep-O			
PG0/IRQ0, PG1/IRQ1, PG2/IRQ2	All	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
PG3	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PG4/IRQ6	All	Hi-Z	Keep-O*2		Keep-O	Keep	Hi-Z
PG5	All	Hi-Z	Keep-O		Keep-O	Keep	Hi-Z
PG6/CS2#	Single-chip mode (EXBE = 0)	Hi-Z	Keep-O		Keep	Keep	Hi-Z
	On-chip ROM enabled/disabled extended (EXBE = 1)		[CS output] H [Other than the above] Keep-O	[CS output] Hi-Z [Other than the above] Keep-O			
USB0_DM	All	Hi-Z	Keep-O		Hi-Z	Hi-Z	
USB0_DP	All	Hi-Z	Keep-O		Hi-Z	Hi-Z	
USB0_DPUPE	All	Hi-Z	Keep-O		Hi-Z	Hi-Z	

H: High-level
L: Low-level
Keep-O: Output pins retain their previous values, and input pins become high-impedance.
Keep: Pin states are retained during periods on software standby.
Hi-Z: High-impedance

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the software standby cancelling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the deep software standby cancelling source.
Note 4. Input is enabled while the pin is used as an input pin.

[64- and 48-Pin Versions]

Table 1.2 Port States in Each Processing State

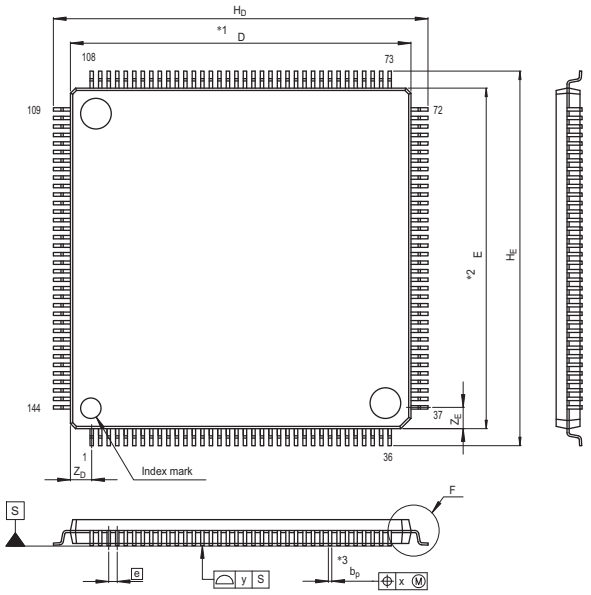
Port Name Pin Name	Operating Mode According to Registers Setting	Reset	Softwere Standby Mode	Deep Software Standby Mode IOKEEP=1/0	After Deep Software Standby Mode is Canceled (Return of start-up Mode)	
					IOKEEP = 1 *1	IOKEEP = 0
P00/IRQ2-DS	All	Hi-Z	Keep-O*2	Keep-O*3	Keep	Hi-Z
P01/IQR4-DS	All	Hi-Z	Keep-O*2	Keep-O*3	Keep	Hi-Z
P10/IRQ0-DS	All	Hi-Z	Keep-O*2	Keep-O*3	Keep	Hi-Z
P11/IRQ1-DS	All	Hi-Z	Keep-O*2	Keep-O*3	Keep	Hi-Z
Port 2	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
Port 3	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
Port 4	All	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
P70/IRQ5-DS	All	Hi-Z	Keep-O*2	Keep-O*3	Keep	Hi-Z
P71 to P76	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
P91, P92	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
P93/IRQ1	All	Hi-Z	Keep-O*2	Keep	Keep	Hi-Z
P94	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
Port A	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
PB0 to PB3	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
PB4/IRQ3-DS	All	Hi-Z	Keep-O*2	Keep-O*3	Keep	Hi-Z
PB5/IRQ0	All	Hi-Z	Keep-O*2	Keep	Keep	Hi-Z
PB6, PB7	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
Port D	All	Hi-Z	Keep-O	Keep	Keep	Hi-Z
PE2/NMI	All	Hi-Z	Hi-Z*2	Hi-Z*3	Hi-Z	Hi-Z

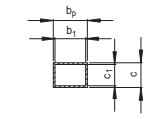
Keep-O: Output pins retain their previous values, and input pins become high-impedance.
Keep: Pin states are retained during periods on software standby.
Hi-Z: High-impedance
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the software standby cancelling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the deep software standby cancelling source.

Appendix 2. Package Dimensions

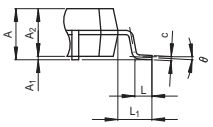
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



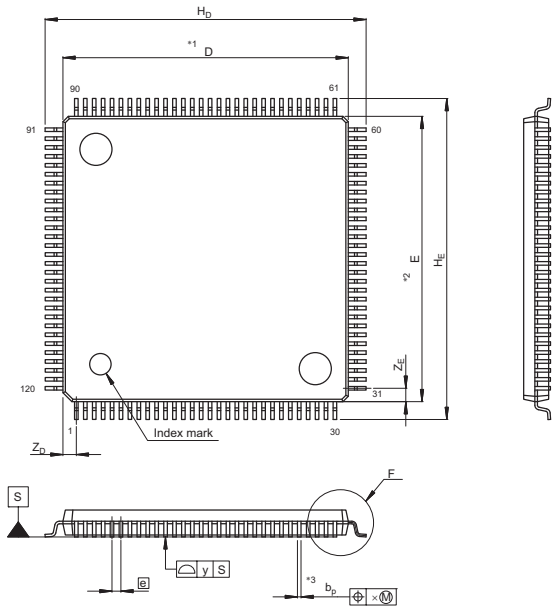
Detail F

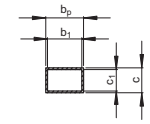
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

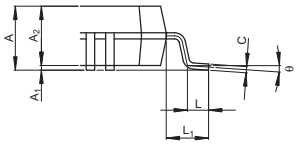
Figure A 144-Pin LQFP (PLQP0144KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP120-16x16-0.50	PLQP0120KA-A	—	0.9g





Terminal cross section



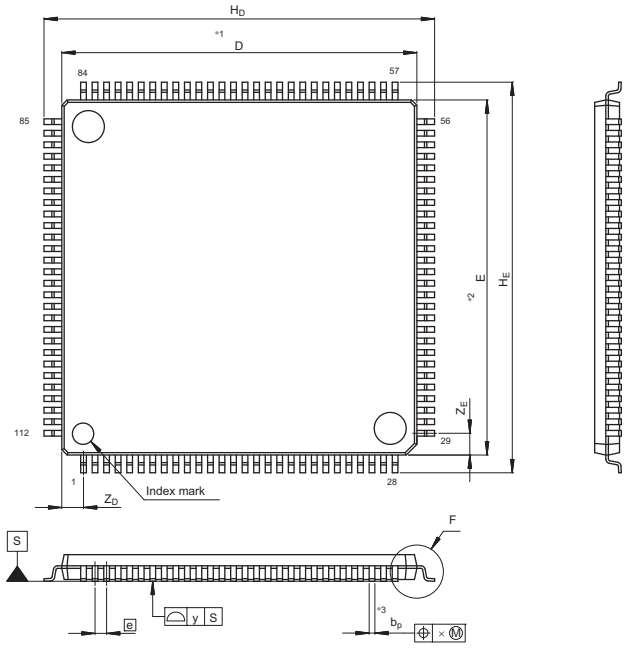
Detail F

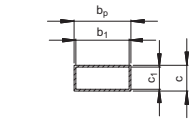
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A_2	—	1.4	—
H_D	17.8	18.0	18.2
H_E	17.8	18.0	18.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

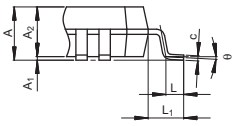
Figure B 120-Pin LQFP (PLQP0120KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E/FP-112EV	1.2g





Terminal cross section



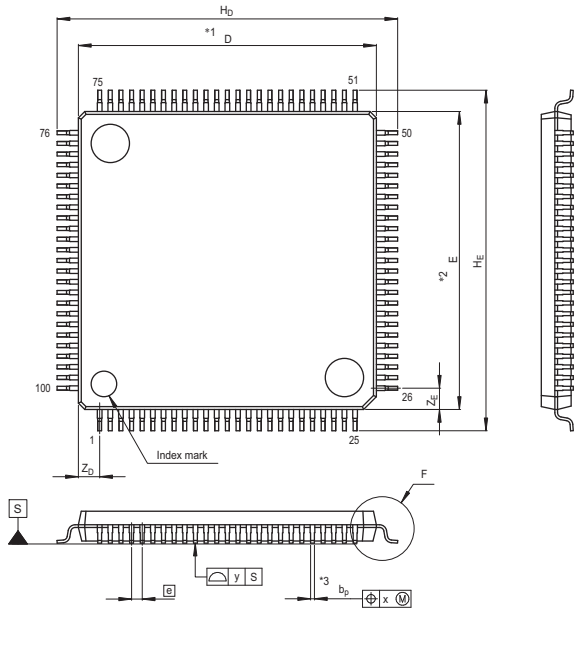
Detail F

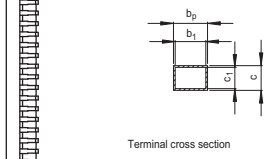
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

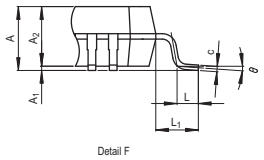
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 112-Pin LQFP (PLQP0112JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





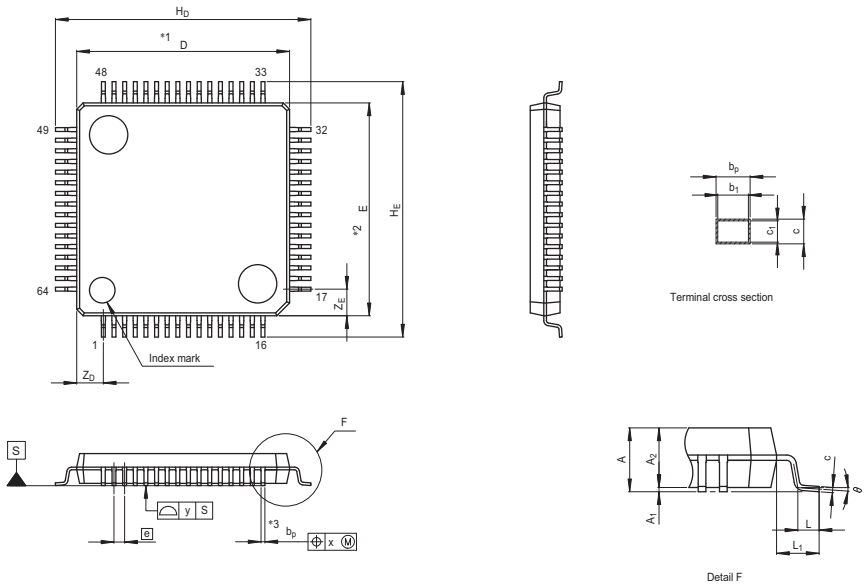


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure D 100-Pin LQFP (PLQP0100KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

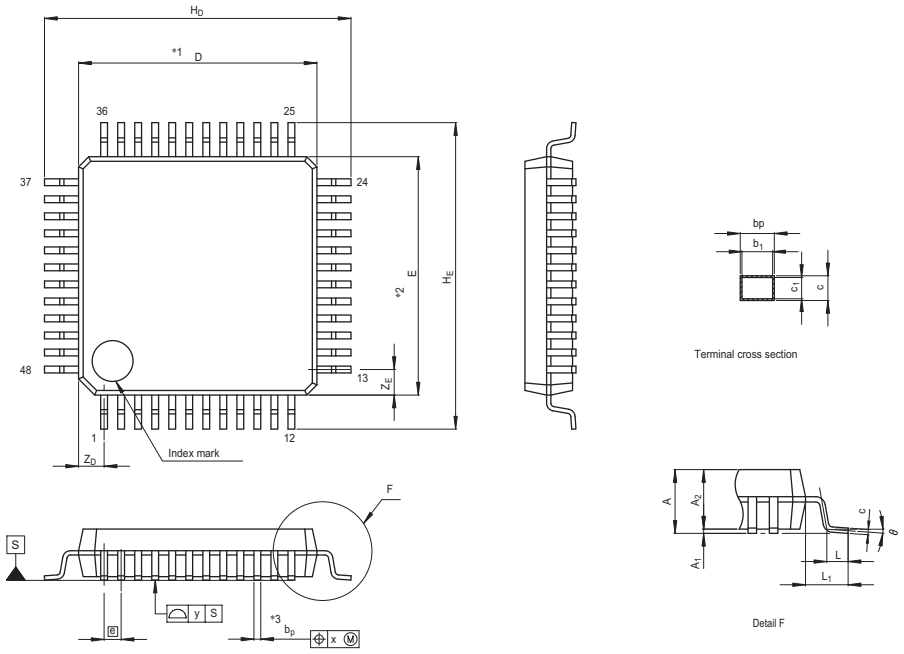


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure E 64-Pin LQFP (PLQP0064KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure F 48-Pin LQFP (PLQP0048KB-A)

REVISION HISTORY	RX63T Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.50	Nov 16, 2011	—	First Edition issued
1.00	May 25, 2012	All	
		—	Memory Protection Unit (MPU) section and related information, added
		—	Corrected terms (description of on-chip ROM and ROM/RAM, host command → command, low/high output → 0/1 output)
		4	How to Use This Manual: Data Sheet, Document Title added; User's manual: Software, Document No. changed
		Features	
		35	Added
		1. Overview	
		36 to 39	Table 1.1 Outline of Specifications, changed
		41	Table 1.3 List of Products: Operating frequency, changed
		42	Figure 1.2 Block Diagram, changed
		43 to 45	Table 1.4 Pin Functions: Input/output of power supply and analog power supply, changed; Description of VCC, changed.
		2. CPU	
		53	2.1 Features, changed
		—	2.5.5 Notes on the Allocation of Instruction Codes, deleted
		70	2.6.1 Fixed Vector Table: "Access exception" added to the description
		70	Figure 2.8 Fixed Vector Table, changed
		3. Operating Modes	
		81	3.1 Operating Mode Types and Selection, changed
		81	Table 3.1 Selection of Operating Modes by the Mode Pin to Table 3.4 Selection of Endian, changed
		82	3.2.1 Mode Monitor Register (MDMONR), changed
		—	3.2.2 Mode Status Register (MDSR), deleted
		83	3.2.2 System Control Register 0 (SYSCR0), changed
		84	3.2.3 System Control Register 1 (SYSCR1), changed
		85	3.3.1 Single-Chip Mode, changed
		85	3.3.2 Boot Mode, changed
		86	Figure 3.1 Mode-Setting Pin Level and Operating Mode, changed
		87	Figure 3.2 Setting of SYSCR0.ROME and EXBE Bits and Operating Modes, changed
		4. Address Space	
		89	Figure 4.1 Memory Map in Each Operating Mode: On-chip RAM (bytes), changed
		5. I/O Registers	
		91	(3) Number of Access Cycles to I/O Registers: Part of description, deleted
		92 to 114	Table 5.1 List of I/O Registers (Address Order), changed
		6. Resets	
		116 to 117	Table 6.2 Targets to be Initialized by Each Reset Source, changed
		118	6.2.1 Reset Status Register 0 (RSTSR0), notes changed
		120 to 121	6.2.3 Reset Status Register 2 (RSTSR2), notes changed
		123	Figure 6.1 Operation Examples During a Power-On Reset and Voltage Monitoring 0 Reset, changed
		124	Figure 6.2 Operation Examples During Voltage Monitoring 1 Reset and Voltage Monitoring 2 Reset, changed
		7. Option-Setting Memory	
		129	7.2.1 Option Function Select Register 0 (OFS0), note deleted
		8. Voltage Detection Circuit (LVDA)	
		135	Table 8.1 Voltage Detection Circuit Specifications, changed
		139	8.2.2 Voltage Monitoring 1 Circuit Status Register (LVD1SR), description changed
		141	8.2.4 Voltage Monitoring 2 Circuit Status Register (LVD2SR), description changed
		147	8.3.2 Monitoring Vdet1, changed
		147	Table 8.2 Procedures for Setting up Monitoring against Vdet1, changed
		147	8.3.3 Monitoring Vdet2, changed
		147	Table 8.3 Procedures for Setting up Monitoring against Vdet2, changed
		148	Figure 8.4 Example of Voltage Monitoring 0 Reset Operation, changed

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	150	Figure 8.5 Example of Voltage Monitoring 1 Interrupt Operation, changed
		152	Figure 8.6 Example of Voltage Monitoring 2 Interrupt Operation, changed
		9. Clock Generation Circuit	
		153	Table 9.1 Specifications of Clock Generation Circuit: Operating frequency, changed, notes added
		154	Figure 9.1 Block Diagram of Clock Generation Circuit, changed
		156	9.2.1 System Clock Control Register (SCKCR), changed
		158	9.2.2 System Clock Control Register (SCKCR3), part of description deleted
		160	9.2.4 PLL Control Register 2 (PLLCR2), description changed
		161	9.2.5 Main Clock Oscillator Control Register (MOSCCR), description changed
		167	Figure 9.2 Example of Crystal Resonator Connection, changed
		167	Table 9.3 Damping Resistance (Reference Values), changed
		167	Table 9.4 Crystal Resonator Characteristics (Reference Values), changed
		170	Figure 9.5 Flow of Recovery from Detection of Oscillator Stop, changed
		171	9.6 Internal Clock, changed
		171	9.6.5 FlashIF Clock, changed
		172	9.7 Pin Settings When an Oscillator is Connected: (1) Main clock, description changed
		10. Clock Frequency Accuracy Measurement Circuit (CAC)	
		174	Table 10.1 Specifications of CAC: Description of Clock frequency measurement, changed
		174	Figure10.1 Block Diagram of CAC, changed
		11. Low Power Consumption	
		185	11.1 Overview, changed
		185	Table 11.1 Specifications of Low Power Consumption Function: Function for lower operating power consumption, deleted
		185	Table 11.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode: Note 3 changed
		187	Figure 11.1 Mode Transitions, changed
		192	11.2.5 Operating Power Control Register (OPCCR), deleted
		—	Table 11.3 Relationship between Operating Power Control Mode, Operating Range, and Power Consumption, deleted
		—	11.2.6 Sleep Mode Return Clock Source Switching Register (RSTCKCR), deleted
		—	11.5 Function for Lower Operating Power Consumption, deleted
		—	11.5.1.3 Sleep Mode Return Clock Source Switching Function, deleted
		203	11.5.2.1 Transition to All-Module Clock Stop Mode, changed
		204	11.5.2.2 Canceling Software Standby Mode, changed
		206	11.5.3.3 Example of Software Standby Mode Application, changed
		208	11.5.4.2 Canceling Deep Software Standby Mode, changed
		210	Figure 11.4 Example of Flowchart to Use Deep Software Standby Mode, changed
		—	11.7.7 Rewrite the Register by DMAC and DTC in Sleep Mode, part of description deleted
		211	11.6.8 Points for Caution on Return from Software Standby, added
		—	11.7.9 Point for Caution when Shifting from Low-Speed Mode to Software Standby Mode deleted
		12. Register Write Protection Function	
		212	Table 12.1 Association between PRCR Bits and Registers to be Protected, changed
		213	12.1.1 Protect Register (PRCR), changed
		13. Exception Handling	
		214	Figure 13.1 Types of Exception Events, changed
		214	13.1.3 Access Exceptions, added
		216	Figure 13.2 Outline of Exception Handling Procedure, changed
		217	Table 13.1 Acceptance Timing and Saved PC Value, changed
		218	Table 13.2 Vector and Site for Saving the Values in the PC and PSW, changed
		219	13.5.3 Access Exceptions, added
		221	Table 13.3 Return from Exception Handling Routine, changed
		221	Table 13.4 Priority of Exception Events, title and table contents changed
		14. Interrupt controller (ICUb)	
		222	Table 14.1 Specifications of Interrupt Controller, changed
		225	14.2.2 Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh), notes changed
		236	14.2.13 Non-Maskable Interrupt Status Clear Register (NMICLR), description changed
		—	14.2.19 Group 12 Interrupt Clear Register (GCR12), deleted
		241	Table 14.3 Interrupt Vector Table: Changed, columns sorted by pin number deleted, notes deleted
		249	Table 14.4 Group 12 Interrupt Requests, changed

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	260	14.7.1 Return from Sleep Mode, changed
		260	14.7.2 Return from All-Module Clock Stop Mode, changed
		261	14.7.3 Return from Software Standby Mode, changed
		15. Buses	
		262	Table 15.1 Bus Specifications, changed
		263	Figure 15.1 Bus Configuration, changed
		264	Table 15.2 Addresses Assigned for Each Bus, changed
		264	15.2.1 CPU Buses, part of description deleted
		265	Table 15.4 Connection of Peripheral Modules to the Internal Peripheral Buses, changed
		266	15.2.5 Write Buffer Function (Internal Peripheral Bus), title added
		269	15.3.3 Bus Error Status Register 1 (BERSR1), changed
		16. Memory-Protection Unit (MPU)	
		274 to 294	Section added
		18. Data Transfer Controller (DTCa)	
		339	18.2.8 DTC Vector Base Register (DTCVBR), changed
		356	18.5 DTC Setting Procedure, changed
		361	18.9.3 Setting the DTC Activation Enable Register (ICU.DTCERn) of the Interrupt Controller, changed
		19. I/O Ports	
		372	Table 19.3 Handling of Unused Pins, changed
		20. Multi-Function Pin Controller (MPC)	
		378	20.2.1 Write-Protect Register (PWPR), changed
		391	20.3.1 Procedure for Specifying Input/Output Pin Function, changed
		391	Table 20.15 Register Settings: Contents changed, notes changed/deleted
		391	20.3.3 Notes on the Use of Analog Functions, added
		21. Multi-Function Timer Pulse Unit 3 (MTU3)	
		392	Table 21.1 Specifications of MTU, changed
		445	21.2.17 Timer Output Master Enable Register (TOER), description added
		447	21.2.18 Timer Output Control Registers 1 (TOCR1A and TOCR1B), notes changed
		449	21.2.19 Timer Output Control Registers 2 (TOCR2A and TOCR2B), notes changed
		458 to 459	21.2.28 Timer Waveform Control Registers (TWCRA and TWCRB), notes changed
		460 to 463	21.2.29 Timer A/D Converter Start Request Control Register (TADCR), notes changed
		488	21.3.4 Cascaded Operation, description added
		491	Figure 21.24 Cascaded Operation Example (c), notes added
		493	21.3.5 PWM Modes, (a) PWM Mode 1, description changed
		511	Figure 21.39 Example of Complementary PWM Mode Setting Procedure, changed
		517	Figure 21.42 Example of Operation without Dead Time (MTU3 and MTU4), changed
		529	Figure 21.57 Timing for Synchronous Counter Clearing (MTU3 and MTU4), changed
		531	Figure 21.59 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 21.57; Bit WRE of TWCRA or TWCRB is 1), changed
		531	Figure 21.60 Example of Synchronous Clearing in Interval Tb at Crest (Timing (6) in Figure 21.57; Bit WRE of TWCRA or TWCRB is 1), changed
		535	Figure 21.65 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 21.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7), changed
		535	Figure 21.66 Example of Synchronous Clearing in Interval Tb at Crest (Timing (6) in Figure 21.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7), changed
		536	Figure 21.67 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 20.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7), changed
		536	Figure 21.68 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 20.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7), changed
		537	Figure 21.69 Example of Counter Clearing Operation by MTU3.TGRA Compare Match, changed
		545	Figure 21.80 Example of Operation when Buffer Transfer is Disabled (BTE[1:0] = 01b), changed
		546	Figure 21.81 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b), changed
		547	Figure 21.82 Relationship between Bits T3AEN and T4VEN in TITCR1A and Buffer Transfer-Enabled Period, changed

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	574	Figure 21.118 TGI Interrupt Timing (Compare Match) (MTU5), changed
		579	21.6.2 Input Clock Restrictions, changed
		579	Figure 21.124 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode, changed
		579	21.6.3 Note on Cycle Setting, changed
		22. Port Output Enable 3 (POE3)	
		—	Description, changed
		—	22.2 Register Descriptions, part of description deleted.
		—	Table 22.4 POE3 Register Configuration, deleted
		625	22.2.2 Output Level Control/Status Register 1 (OCSR1), changed
		626	22.2.3 Active Level Setting Register 1 (ALR1), changed
		631 to 632	22.2.7 Software Port Output Enable Register (SPOER), changed
		633	22.2.8 Port Output Enable Control Register 1 (POECR1), changed
		634	22.2.9 Port Output Enable Control Register 2 (POECR2), changed
		635	22.2.10 Port Output Enable Control Register 3 (POECR3), changed
		636	22.2.11 Port Output Enable Control Register 4 (POECR4), changed
		639	22.2.13 Port Output Enable Control Register 6 (POECR6), changed
		642 to 644	Table 22.4 Target Pins and Conditions for High-Impedance Control, changed
		645	Figure 22.2 Target Pins and Conditions for High-Impedance Control, changed
		649	22.3.7 Release from High-Impedance State, description added
		23. General PWM Timer (GPT)	
		—	Description changed
		650	Table 23.1 Specifications of GPT, changed
		651 to 652	Table 23.2 Functions of GPT: Common interrupt source, changed
		653	Figure 23.1 Block Diagram of GPT, changed
		666 to 667	23.2.11 LOCO Count Control Register (LCCR), changed
		668	23.2.12 LOCO Count Status Register (LCST), changed
		669	23.2.13 LOCO Count Value Register (LCNT), changed
		669	23.2.14 LOCO Count Result Average Register (LCNTA), changed
		669	23.2.15 LOCO Count Result Register n (LCNTn) (n=00 to 15), changed
		670	23.2.16 LOCO Count Upper/Lower Permissible Deviation Register (LCNTDU, LCNTDL), changed
		676 to 677	23.2.19 General PWM Timer Control Register (GTCR), bit function table, changed
		691 to 692	23.2.33 General PWM Timer Dead Time Control Register (GTDTCR), title changed
		757	23.4.1 Interrupt Sources and Priorities, changed
		757	Table 23.5 GPT Interrupt Sources, changed
		767	23.6 IWDTCLK Count Function, changed
		767	Table 23.7 Frequency Setting Example for IWDTCLK Count Function, changed
		768	Figure 23.77 Example of IWDTCLK Count Function Operation, changed
		768	Figure 23.78 Example for Setting IWDTCLK Count Function Operation, changed
		769	Figure 23.79 Example of IWDTCLK Count Skipping Function Operation (Skipping Count: 7, Count Result not Skipped), changed
		769	Figure 23.80 Example of IWDTCLK Count Skipping Function Operation (Skipping Count: 7, Count Result Skipped), changed
		781	23.9.4 Low-Power Consumption Setting when the IWDTCLK Count Function is in Use, changed
		24. Compare Match Timer (CMT)	
		787	24.4.2 Timing of Compare Match Interrupt Generation, changed
		787	Figure 24.4 Timing for the Setting of a Compare Match Interrupt, changed
		27. Serial Communications Interface (SCIc, SCId)	
		820 to 821	Table 27.1 Specifications of SCIc, notes added
		821 to 822	Table 27.2 Specifications of SCId, notes added
		824	Figure 27.2 Block Diagram of SCI12 (SCId), changed
		838	27.2.8 Smart Card Mode Register (SCMR): Bit function table, notes added. SDIR bit, bit description changed
		841	Table 27.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (2), title and columns, added
		842	Table 27.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (3) and (4), title added
		843	Table 27.13 Maximum Bit Rate for Each Operating Frequency (Asynchronous Mode), changed
		843	Table 27.14 Maximum Bit Rate with External Clock Input (Asynchronous Mode), changed

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	844	Table 27.16 Maximum Bit Rate with External Clock Input (Clock Synchronous Mode, Simple SPI Mode), changed
		845	Table 27.17 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372), changed
		845	Table 27.18 Maximum Bit Rate for Each Operating Frequency (Smart Card Interface Mode, S = 372), changed
		846	Table 27.19 BRR Settings for Various Bit Rates (Simple I^2C Mode): (1) and (2), title changed, added
		846	Table 27.20 Minimum Widths at High and Low Level for SCL at Various Bit Rates (Simple I^2C Mode): (1) and (2), title changed, added
		865	27.2.34 Timer Mode Register (TMR), notes changed
		871	Figure 27.6 Sample SCI Initialization Flowchart (Asynchronous Mode), changed
		877	Figure 27.12 Example of Serial Reception Flowchart (2) (Asynchronous Mode), changed
		882	Figure 27.17 Example of Multi-Processor Serial Reception Flowchart (2), changed
		888	Figure 27.24 Example of Serial Reception Flowchart (Clock Synchronous Mode), changed
		910	Table 27.24 States of Pins by Mode and Input Level on the SSn# Pin: State of SMISOn pin, changed
		910	27.8.3 SS Function in Slave Mode, changed
		913	Figure 27.52 Example of Operations at the Time of Start-Frame Transmission, changed
		916	Table 27.25 Structures of Start Frames, changed
		917	Figure 27.55 Example of Operations at the Time of Start-Frame Reception, changed
		919	Figure 27.57 Sample Flowchart for Reception of a Start Frame (2), changed (BDST → SDST)
		921	Figure 27.59 Example of Operations at the Time of Start-Frame Reception (with Priority Interrupts in Use), changed
		922	Figure 27.60 Example of Operations with Bus-Collision Detection, changed
		923	Figure 27.61 Example of Operations with the Digital Filter, changed
		924	Figure 27.62 Example of Operations for Bit-Rate Measurement, changed
		925	Figure 27.63 Timing for Sampling of Data Received through RXDX12, changed
		926	Figure 27.64 Example of Operations in Break Field Low Width Output Mode, changed
		927	Figure 27.65 Example of Operations in Break Field Low Width Determination Mode, changed
		28. I^2C Bus Interface (RIIC)	
		940 to 941	28.2.1 I^2C Bus Control Register 1 (ICCR1), changed
		942 to 944	28.2.4 I^2C Bus Mode Register 2 (ICMR2), changed
		962	28.2.13 I^2C Bus Bit Rate Low-Level Register (ICBRL), changed
		964	Table 28.5 Examples of ICBRH/ICBRL Settings for Transfer Rate: (1) to (3), changed
		966	28.2.18 Timeout Internal Counter (TMOCNT), added
		968	Figure 28.5 Example of RIIC Initialization Flow, changed
		969	28.3.3 Master Transmit Operation: (1), changed
		970	Figure 28.6 Example of Master Transmission Flowchart, changed
		972	28.3.4 Master Receive Operation: (1), changed
		974	Figure 28.10 Example of Master Reception Flowchart (7-Bit Address Format), changed
		975	Figure 28.11 Master Receive Operation Timing (1) (7-Bit Address Format, when RDRFS = 0), changed
		975	Figure 28.12 Master Receive Operation Timing (2) (10-Bit Address Format, when RDRFS = 0), changed
		977	Figure 28.14 Example of Slave Transmission Flowchart, changed
		980	Figure 28.17 Example of Slave Reception Flowchart, changed
		1004	28.13 Interrupt Request, changed
		1004	Table 28.8 Interrupt Sources: ICRXI, changed
		29. Serial Peripheral Interface (RSPI)	
		1007	Table 29.1 Specifications of RSPI: Bit rate, changed
		1012	29.2.2 RSPI Slave Select Polarity Register (SSLP): Bit function table, changed
		1013	29.2.3 RSPI Pin Control Register (SPPCR): Bit function table, MOIFV, changed
		1016	29.2.5 RSPI Data Register (SPDR): Register description, (1) Bus Interface, (a) Writing, changed, (SPRX0 to 3) → (SPRXn)
		1022	29.2.9 RSPI Data Control Register (SPDCR): SPRDTD bit, bit description changed
		1029	29.3.1 Overview of RSPI Operations, changed
		1030	29.3.2 Controlling RSPI Pins, changed
		1031	29.3.3 RSPI System Configuration Examples, changed

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	1040 to 1041	29.3.4.1 When Parity is Disabled (SPCR2.SPPE = 0): (3) LSB-First Transfer (32-Bit Data), changed; (4) LSB-First Transfer (24-Bit Data), changed
		1048	29.3.6.1 Full-Duplex Synchronous Serial Communications (SPCR.TXMD = 0), changed
		1048	Figure 29.25 Operation Example of SPCR.TXMD = 0, changed
		1050	29.3.7 Transmit Buffer Empty/Receive Buffer Full Interrupts, changed
		1052	Table 29.8 Relationship between Non-Normal Transfer Operations and RSPI Error Detection Function: RSPI operation, changed
		1053	29.3.8.1 Overrun Error: 4., changed
		1054	29.3.8.2 Parity Error: 3., changed
		1055	29.3.8.3 Mode Fault Error, changed
		1058	Figure 29.32 Correspondence between the RSPI Command Register and Transmit/Receive Buffers in Sequence Operations, changed
		1061	Table 29.11 Relationship among SPNDEN Bit, SPND, and Next-Access Delay Value: SPCMDm.SPNDEN bit, changed
		—	Figure 29.35 Example of Initialization Flowchart in Master Mode (SPI Operation), deleted
		1063 to 1065	29.3.10.1 Master Mode Operation: (9) Software Processing Flow, changed; (a) Transmit Processing Flow, (b) Receive Processing Flow, (c) Flow of error processing, added
		1063	Figure 29.35 Flowchart in Master Mode (Transmission), added
		1064	Figure 29.36 Flowchart in Master Mode (Reception), added
		1065	Figure 29.37 Flowchart for Master Mode (Error Processing), added
		1068 to 1069	29.3.10.2 Slave Mode Operation: (6) Flow of Software Processing, changed: (a) Flow of processing for transmission, (b) Flow of processing for reception, (c) Flow of error processing, added
		—	Figure 29.40 Example Flowchart for Transfer Operations in Slave Mode (SPI Operation), deleted
		1068	Figure 29.39 Flowchart for Slave Mode (Transmission), added
		1068	Figure 29.40 Flowchart for Slave Mode (Reception), added
		1069	Figure 29.41 Flowchart for Slave Mode (Error Processing), added
		1070	29.3.12 Master Mode Operation: (3) Sequence Control, changed
		1072	Figure 29.44 Correspondence between the RSPI Command Register and Transmit/Receive Buffers in Sequence Operations, changed
		—	29.3.12 Master Mode Operation: (5) Flowchart of Operations, deleted
		—	Figure 29.48 Example Flowchart for Transfer Operations in Master Mode (Clock Synchronous Operation), deleted
		—	29.3.13 Slave Mode Operation: (4), Transfer Operation Flowcharts, deleted
		—	Figure 29.50 Example Flowchart for Transfer Operations in Slave Mode (CPHA = 1) (Clock Synchronous Operation), deleted
		—	29.3.14 Error Handling, deleted
		—	Figure 29.51 Error Handling (Overrun Error), deleted
		—	Figure 29.52 Error Handling (Parity Error), deleted
		—	Figure 29.53 Error Handling (Mode Fault Error), deleted
		1078	Table 29.13 Interrupt Sources of RSPI: RSPI idle, changed (IDINF → IDLNF)
		31. 12-Bit A/D Converter (S12ADB)	
		1086 to 1087	Table 31.1 Specifications of 12-Bit A/D Converter, changed
		1089	Figure 31.1 Block Diagram of 12-Bit A/D Converter, changed
		1110	31.2.11 A/D Sample and Hold Circuit Control Register (ADSHCR), changed
		1115	31.2.15 Comparator Filter-Mode Register (ADCMPNR0), changed
		1117	31.2.17 Comparator Interrupt Selection Register (ADCMPSEL), changed
		1124	31.3.2.6 Extended Operations When Double-Trigger Mode is Selected, changed
		1131	31.3.4.1 Basic Operation (Channel-Dedicated Sample-and-Hold Circuits not Used), changed
		1136	31.3.4.2 A/D Conversion in Double Trigger Mode, changed
		1138	31.3.4.4 Operation under Group-A Priority Control, changed
		1153	31.3.11 Window Comparator, changed
		1154	Figure 31.28 Example 1 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 11b), changed
		1154	Figure 31.29 Example 2 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 10b), changed
		1155	Figure 31.30 Example 3 of Window Comparator Operation (with AN000 Selected and ADCMPMD0.CEN000 = 01b), changed
		1156	31.4.2 Interrupt Requests at the Time of Detection by the Comparator, changed
		1160	31.6.7 Allowable Impedance of Signal Source, changed

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	1160	Table 31.11 Specifications of Analog Input Pins: Internal equivalent circuit of a pin, Max. changed
		1162	31.6.11 Notes on Noise Prevention, changed
		1162	Figure 31.35 Sample Protection Circuit for Analog Inputs, changed
		33. RAM	
		—	Table 33.1 Specifications of on-chip RAM: RAM capacity, changed; Note 2, deleted
		34. ROM (Flash Memory for Code Storage)	
		1171	Table 34.1 Specifications of ROM, changed
		—	Table 34.3 Input and Output Pins Associated with the ROM, deleted
		1173	34.2.1 Flash Write Erase Protection Register (FWEPROR), changed
		1174	34.2.2 Flash Mode Register (FMODR), changed
		1175 1176	34.2.3 Flash Access Status Register (FASTAT), changed
		1178 to 1180	34.2.5 Flash Status Register 0 (FSTATR0), changed
		1180	34.2.6 Flash Status Register 1 (FSTATR1), changed
		1181	34.2.7 Flash Ready Interrupt Enable Register (FRDYIE), changed
		1182	34.2.8 Flash P/E Mode Entry Register (FENTRYR), changed
		1183	34.2.9 Flash Protection Register (FPROTR), changed
		1184	34.2.10 Flash Reset Register (FRESETR), changed
		1185	34.2.11 FCU Command Register (FCMDR), changed
		1186	34.2.12 FCU Processing Switching Register (FCPSR), register description changed
		1186	34.2.13 Flash P/E Status Register (FPESTAT), register description changed
		1187	34.2.14 Peripheral Clock Notification Register (PCKAR), changed
		1188	34.3 Configuration of Memory Areas for the ROM, changed
		1198	Figure 34.7 Procedure for Transition to ROM Read Mode, changed
		1201	Figure 34.11 Simple Flowchart of the Procedure for Programming and Erasure, changed
		1202	34.6.4.2 Programming and Erasure Procedures: (3) Using the Peripheral Clock Notification Command, changed
		1213	34.7.1 Suspension during Programming, changed
		1214	34.7.2 Suspension during Erasure (Suspension Priority Mode), changed
		1215	34.8 Protection, changed
		1216	34.8.2 Command-Locked State, changed
		1216	Table 34.8 Errors that Lead to the Command-Locked State (Types Dedicated to ROM and Types Common to ROM and E2 DataFlash): Title, changed
		1217	Figure 34.23 System Configuration for Operations in Boot Mode, changed
		1218	Table 34.9 Input and Output Pins Associated with the ROM, changed
		1219	Figure 34.24 State Transitions in Boot Mode, changed
		1222	Table 34.11 Specifications for ID Code Protection, changed
		1223	34.9.5 Inquiry/Selection Command Wait, changed
		1229	Figure 34.29 New Bit Rate Selection Sequence, changed
		1223	34.9.6 ID Code Wait State: (1) ID Code Check, changed
		1234	Table 34.16 Programming/Erasure Commands, changed
		1234	34.9.7 Programming/Erasure Command Wait State, changed
		1241	Table 34.17 Specifications for ID Code Protection on Connection of the On-Chip Debugger, changed
		—	34.11 Usage Notes: (4) Reset during Programming or Erasure, changed (5) Prohibition of Non-Maskable Interrupts during Programming or Erasure, changed (7) Programming and Erasure in Low-Speed Operating Modes 1, deleted (8) Programming/Erasure Abnormal End, changed (9) Actions Prohibited during Programming and Erasure, changed
		35. E2 DataFlash Memory (Flash Memory for Data Storage)	
		1244	Table 35.1 Specifications of E2 DataFlash Memory, changed
		1244	35.1 Overview, changed
		—	Table 35.2 Input and Output Pins Associated with the E2 DataFlash, deleted
		1246	35.2.1 Flash Mode Register (FMODR), changed
		1247 to 1248	35.2.2 Flash Access Status Register (FASTAT), changed
		1250	35.2.4 E2 DataFlash Read Enable Register 0 (DFLRE0), changed
		1251	35.2.5 E2 DataFlash Programming/Erasure Enable Register 0 (DFLWE0), changed
		1252	35.2.6 Flash P/E Mode Entry Register (FENTRYR), changed
		1253	35.2.7 E2 DataFlash Blank Check Control Register (DFLBCCNT), changed

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2012	1254	35.2.8 E2 DataFlash Blank Check Status Register (DFLBCSTAT): register description, changed
		1255	35.3 Configuration of Memory Area for the E2 DataFlash Memory, changed
		1261	35.6.4 FCU Command Usage: (2) Programming, changed
		1262	Figure 35.5 Procedure for E2 DataFlash Programming, changed
		1263	35.6.4 FCU Command Usage: (3) Erasure, changed
		1266	35.7.2 Error Protection, changed
		1267	35.8.1 Inquiry/Selection Commands, changed
		1268	35.8.2 Programming/Erasing Commands, changed
		1270	35.9 Usage Notes: (3) Other Points to Note, changed
		36. Electrical Characteristics	
		1272	Table 36.3 DC Characteristics (2), changed
		1275	Table 36.5 Operation Frequency Value, changed
		1275	Table 36.6 Clock Timing, changed
		—	Table 36.8 Reset Timing, notes deleted
		1284	Table 36.13 Timing of On-Chip Peripheral Modules(4), notes changed
		1290	Table 36.16 Comparator Characteristics, changed
		1291	Table 36.17 Power-on Reset Circuit and Voltage Detection Circuit Characteristics, changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	Corrected fluctuation of terms (pin reset, reset from pin → RES# pin reset)	
		Features	
		44	Changed
		1. Overview	
		45	1.1 Outline of Specifications, description changed
		45 to 51	Table 1.1 Outline of Specifications, changed
		52	Table 1.2 Comparison of Functions for Different Packages, changed
		53 to 55	Table 1.3 List of Products, changed
		55	Figure 1.1 How to Read the Product Part Number, changed
		56	Figure 1.2 Block Diagram, changed
		57 to 61	Table 1.4 Pin Functions, changed
		62	Figure 1.3 Pin Assignment (144-Pin LQFP), added
		63	Figure 1.4 Pin Assignment (120-Pin LQFP), added
		64	Figure 1.5 Pin Assignment (112-Pin LQFP), added
		65	Figure 1.6 Pin Assignment (100-Pin LQFP), added
		66	Figure 1.7 Pin Assignment (64-Pin LQFP), notes changed
		67	Figure 1.8 Pin Assignment (48-Pin LQFP), notes changed
		68 to 71	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), added
		72 to 75	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), added
		76 to 79	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), added
		80 to 82	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), added
		2. CPU	
		97	2.4 Data Types, description changed
		—	2.4.1 Integer to 2.4.4 Strings, deleted
		102	2.5.5 Notes on the Allocation of Instruction Codes, added
		3. Operating Modes [144-, 120-, 112- and 100-Pin Versions]	
		114 to 121	Added
		4. Operating Modes [64- and 48-Pin Versions]	
		122	Title changed
		5. Address Space	
		128	Figure 5.1 Memory Map in Each Operating Mode, changed
		129	5.2 External Address Space, added
		6. I/O Registers	
		131	(3) Number of Access Cycles to I/O Registers, description changed
		132 to 184	Table 6.1 List of I/O Registers (Address Order), changed
		7. Resets	
		186	Table 7.2 Targets to be Initialized by Each Reset Source, changed
		187	7.2.1 Reset Status Register 0 (RSTSR0), notes under bit chart and changed
		189	7.2.2 Reset Status Register 1 (RSTSR1), notes under bit chart and bit table changed; description of CWSF flag changed
		189	7.2.3 Reset Status Register 2 (RSTSR2), notes under bit chart and bit table changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	191	7.3.1 RES# Pin Reset, description changed
		193	Figure 7.2 Operation Examples During Voltage Monitoring 1 Reset and Voltage Monitoring 2 Reset, changed
		194	7.3.7 Software Reset, description changed
		8. Option-Setting Memory	
		197	8.1 Overview, description changed
		197	Figure 8.1 Option-Setting Memory Area, changed
		198 to 201	8.2.1 Option Function Select Register 0 (OFS0), changed
		202	8.2.2 Option Function Select Register 1 (OFS1), changed
		203	8.2.3 Endian Select Register B (MDEB), Endian Select Register S (MDES), title and description changed
		204	8.3 UB Codes, added
		204	8.4.1 Setting Example of Option-Setting Memory, description changed
		9. Voltage Detection Circuit (LVDA)	
		208	9.2.2 Voltage Monitoring 1 Circuit Status Register (LVD1SR), Note 1 changed
		209	9.2.4 Voltage Monitoring 2 Circuit Status Register (LVD2SR), Note 1 changed
		211	9.2.6 Voltage Detection Level Select Register (LVDLVLR), bit table for 144-, 120-, 112-, and 100-pin versions added
		212	9.2.7 Voltage Monitoring 1 Circuit Control Register 0 (LVD1CR0), description of LVD1RIE bit changed
		214	9.2.8 Voltage Monitoring 2 Circuit Control Register 0 (LVD2CR0), description of LVD2RIE bit changed
		217	Figure 9.4 Example of Voltage Monitoring 0 Reset Operation, changed
		10. Clock Generation Circuit	
		222	Table 10.1 Specifications of Clock Generation Circuit, changed
		223	Figure 10.1 Block Diagram of Clock Generation Circuit, changed
		224	Table 10.2 Input/Output Pins of Clock Generation Circuit, changed
		225, 226	10.2.1 System Clock Control Register (SCKCR), changed
		227	10.2.2 System Clock Control Register 2 (SCKCR2), added
		228	10.2.3 System Clock Control Register 3 (SCKCR3), description of CKSEL[2:0] bits changed
		229	10.2.4 PLL Control Register (PLLCR), description of PLIDIV[1:0] bits changed
		231	10.2.6 External Bus Clock Control Register (BCKCR), added
		236	10.2.11 Oscillation Stop Detection Status Register (OSTDSR), notes changed
		237	Table 10.3 Damping Resistance (Reference Values), changed
		238	Table 10.4 Crystal Resonator Characteristics (Reference Values), changed
		240	10.4.1 Oscillation Stop Detection and Operation after Detection, description changed
		242	10.6 Internal Clock, changed
		244	10.8.1 Notes on Clock Generation Circuit, description changed
		11. Clock Frequency Accuracy Measurement Circuit (CAC)	
		245	Table11.1 Specifications of CAC, changed
		245	Figure11.1 Block Diagram of CAC, changed
		247	11.2.2 CAC Control Register 1 (CACR1), description of FMCS[2:0] in bit table changed
		248	11.2.3 CAC Control Register 2 (CACR2), description of RSCS[2:0] in bit table and Note 1 changed
		12. Low Power Consumption	
		255	12.1 Overview, description changed
		255	Table 12.1 Specifications of Low Power Consumption Functions, changed
		255, 256	Table 12.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, changed
		257	Figure 12.1 Mode Transitions, changed
		258	12.2.1 Standby Control Register (SBYCR), changed
		259, 260	12.2.2 Module Stop Control Register A (MSTPCRA), changed
		260, 261	12.2.3 Module Stop Control Register B (MSTPCRB), changed
		262	12.2.4 Module Stop Control Register C (MSTPCRC), description of MSTPC0 in bit table and Note 1 changed
		263	12.2.5 Main Clock Oscillator Wait Control Register (MOSCWTCR), description changed
		264, 265	12.2.6 PLL Wait Control Register (PLLWTCR), description changed
		266	12.2.7 Deep Standby Control Register (DPSBYCR), changed
		267	12.2.8 Deep Standby Interrupt Enable Register 0 (DPSIER0), changed
		269	12.2.10 Deep Standby Interrupt Flag Register 0 (DPSIFR0), changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	270	12.2.11 Deep Standby Interrupt Flag Register 2 (DPSIFR2), Note 1 changed
		271	12.2.12 Deep Standby Interrupt Edge Register 0 (DPSIEGR0), changed
		272	12.2.14 Deep Standby Backup Register (DPSBKRy) (y = 0 to 31), description changed
		273	12.3 Reducing Power Consumption by Switching Clock Signals, description changed
		274	12.5.1.2 Canceling Sleep Mode, description changed
		275	12.5.2.1 Transition to All-Module Clock Stop Mode, description and notes changed
		276	12.5.2.2 Canceling All-Module Clock Stop Mode, description and notes changed
		277	12.5.3.1 Transition to Software Standby Mode, description changed
		277, 278	12.5.3.2 Canceling Software Standby Mode, description changed
		279	12.5.3.3 Example of Software Standby Mode Application, description changed
		280	12.5.4.1 Transition to Deep Software Standby Mode, description changed
		281	12.5.4.2 Canceling Deep Software Standby Mode, description changed
		282	12.5.4.4 Example of Deep Software Standby Mode Application, description changed
		283	12.5.4.5 Flowchart to Use Deep Software Standby Mode, description changed
		283	Figure 12.4 Example of Flowchart to Use Deep Software Standby Mode, changed
		284	12.6.5 Input Buffer Control by DIRQnE Bit (n = 0 to 7), title and description changed
		284	12.6.8 Points for Caution on Return from Software Standby, description changed
		13. Register Write Protection Function	
		285	Table 13.1 Association between PRCR Bits and Registers to be Protected, changed
		15. Interrupt controller (ICUb)	
		295	Table 15.1 Specifications of Interrupt Controller, changed
		296	Figure 15.1 Block Diagram of Interrupt Controller, changed
		296	Table 15.2 Pin Configuration of Interrupt Controller, changed
		297, 298	15.2.1 Interrupt Request Register n (IRn) (n = interrupt vector number), description of IR flag changed
		303	15.2.8 IRQ Control Register i (IRQCRi) (i = 0 to 7), title, addresses, description of IRQMD[1:0] bits changed
		304	15.2.9 IRQ Pin Digital Filter Enable Register 0 (IRQFLTE0), changed
		305	15.2.10 IRQ Pin Digital Filter Setting Register 0 (IRQFLTC0), changed
		312, 313	15.2.17 Group m Interrupt Source Register (GRPm) (m: group number), title and description changed
		314, 315	15.2.18 Group m Interrupt Enable Register (GENm) (m = group number), title and description changed
		316	15.2.19 Group m Interrupt Clear Register (GCRm) (m = group number), added
		317	15.3.1 Interrupt Vector Table, description changed
		318 to 325	Table 15.3 Interrupt Vector Table, changed
		326	15.4.1 Interrupt Request Groups, changed
		327	15.5.1 Detecting Interrupts, description changed
		327	15.5.1.1 Operation of Status Flags for Edge-Detected Interrupts, description changed
		331	15.5.1.3 Edge Detection Group Interrupts and Interrupt Status Flags, changed
		333	15.5.1.4 Level Detection Group Interrupts and Interrupt Status Flags, added
		334	15.5.2 Enabling and Disabling Interrupt Sources, description changed
		337	15.5.6 Digital Filter, changed
		338	15.5.7 External Pin Interrupts, description changed
		339	15.7.1 Return from Sleep Mode, description changed
		340	15.7.3 Return from Software Standby Mode, description changed
		340	15.8.2 Note on Using the MUT3 Interrupt, added
		16. Buses	
		343	Table 16.1 Bus Specifications, changed
		344	Figure 16.1 Bus Configuration, changed
		345	Table 16.2 Addresses Assigned for Each Bus, changed
		345	16.2.1 CPU Buses, description changed
		346	16.2.3 Internal Main Buses, description changed
		346	Table 16.4 Connection of Peripheral Modules to the Internal Peripheral Buses, changed
		346	16.2.4 Internal Peripheral Buses, description changed
		348	16.2.6 External Bus, added
		350	16.2.7 Parallel Operation, description changed
		350	Figure 16.5 Example of Parallel Operations, changed
		350	16.2.8 Bus Settings, added

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	350	16.2.9 Restrictions, changed
		351 to 364	16.3.1 CSn Control Register (CSnCR) (n = 0 to 3) to 16.3.6 CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 3), added
		367, 368	16.3.11 Bus Priority Control Register (BUSPRI), changed
		369 to 397	16.4 Endian and Data Alignment, 16.5 Operation of CS Area Controller, added
		398	16.6.1.1 Illegal Address Access, description changed
		398	16.6.1.2 Timeout, description changed
		399	Table 16.11 Types of Bus Errors, changed
		18. DMA Controller (DMACA)	
		422	Figure 18.1 Block Diagram of DMAC, changed
		424	18.2.3 DMA Transfer Count Register (DMCRA), description changed
		454, 455	18.5 Interrupts, description changed
		457	18.7.1 DMA Transfer to External Devices, added
		19. Data Transfer Controller (DTCa)	
		459	Figure 19.1 Block Diagram of DTC, changed
		460	19.2 Register Descriptions, description changed
		465	19.2.8 DTC Vector Base Register (DTCVBR), description changed
		468	19.3.1 Allocating Transfer Data and DTC Vector Table, description changed
		470	19.4 Operation, description changed
		477	Figure 19.8 Chain Transfer Operation, changed
		478 to 480	Figure 19.9 Example (1) of DTC Operation Timing (Short-Address Mode, Normal Transfer Mode, Repeat Transfer Mode) to Figure 19.13 Example of Operation when Transfer Information Skip is Executed (Vector, Transfer Information, and Transfer Destination Data on the On-Chip RAM, and Transfer Source Data on the Peripheral Module), changed
		481	Table 19.8 Execution Cycles of the DTC, notes changed
		483	19.6.1 Normal Transfer, description changed
		484	19.6.2 Chain Transfer when Counter = 0, description changed
		20. I/O Ports	
		488	20.1 Overview, description changed
		488	Table 20.1 Specifications of I/O Ports, changed
		489, 490	Table 20.2 Port Functions [144-, 120-, 112- and 100-Pin Versions], added
		490	Table 20.3 Port Functions [64- and 48-Pin Versions], title and description changed
		491 to 494	20.2.1 144-, 120-, 112, and 100-Pin Versions, added
		495	20.2.2 64- and 48-Pin Versions, title added
		497	20.3.1 Port Direction Register (PDR), changed
		498	20.3.2 Port Output Data Register (PODR), changed
		499	20.3.3 Port Input Data Register (PIDR), changed
		500	20.3.4 Port Mode Register (PMR), changed
		501	20.3.5 Open Drain Control Register 0 (ODR0), changed
		502	20.3.6 Open Drain Control Register 1 (ODR1), changed
		503	20.3.7 Driving Ability Control Register 1 (DSCR1), added
		504	20.3.8 Driving Ability Control Register 2 (DSCR2), added
		505	Table 20.4 Handling of Unused Pins, changed
		505	20.5 Usage Notes, added
		21. Multi-Function Pin Controller (MPC)	
		506	21.1 Overview, description changed
		507 to 514	Table 21.1 Functions Assigned to Each Multiplexed Pin, changed
		515	21.2.1 Write-Protect Register (PWPR), description of PFSWE bit changed
		516	21.2.2 P0n Pin Function Control Register (P0nPFS) (n = 0 to 3), title and description changed
		518	21.2.3 P1n Pin Function Control Registers (P1nPFS) (n = 0 to 4), title and description changed
		519	21.2.4 P2n Pin Function Control Registers (P2nPFS) (n = 0 to 6), title and description changed
		521	21.2.5 P3n Pin Function Control Registers (P3nPFS) (n = 0 to 5), title and description changed
		523	21.2.6 P4n Pin Function Control Registers (P4nPFS) (n = 0 to 7), description deleted
		523	21.2.7 P5n Pin Function Control Registers (P5nPFS) (n = 0 to 7), 21.2.8 P6n Pin Function Control Registers (P6nPFS) (n = 0 or 5), added
		524	21.2.9 P7n Pin Function Control Registers (P7nPFS) (n = 0 to 6), changed
		525	21.2.10 P8n Pin Function Control Registers (P8nPFS) (n = 0 to 2), added
		526	21.2.11 P9n Pin Function Control Registers (P9nPFS) (n = 0 to 6), title and description changed
		527	21.2.12 PAn Pin Function Select Registers (PAnPFS) (n = 0 to 6), title and description changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	529	21.2.13 PBn Pin Function Control Registers (PBnPFS) (n = 0 to 7), changed
		531	21.2.14 PCn Pin Function Control Register (PCnPFSn) (n = 0 to 5), added
		531	21.2.15 PDn Pin Function Control Register (PDnPFS) (n = 0 to 7), title and description changed
		533	21.2.16 PEn Pin Function Control Register (PEnPFS) (n = 0 to 5), title and description changed
		535	21.2.17 PFn Pin Function Select Register (PFnPFS) (n = 2, 3) to 20.2.26 USB0 Control Register (PFUSB0), added
		542	21.3 How to Set the External Bus Interface, added
		544	21.4.1 Procedure for Specifying Input/Output Pin Function, description changed
		544	21.4.2 Notes on MPC Register Setting, description changed
		545	Table 21.40 Register Settings, changed
		545	21.4.3 Notes on the Use of Analog Functions, description changed
		22. Multi-Function Timer Pulse Unit 3 (MTU3)	
		546	Table 22.1 Specifications of MTU, changed
		553, 554	22.2.1 Timer Control Register (TCR), changed
		557	22.2.2 Timer Mode Register 1 (TMDR1), description of MD[3:0] in bit table changed
		588	22.2.8 Timer Buffer Operation Transfer Mode Register (TBTM), description of TTSE bit changed
		599, 600	22.2.17 Timer Output Master Enable Register (TOER), Note 1 for TOERA and TOERB added
		601	22.2.18 Timer Output Control Registers 1 (TOCR1A and TOCR1B), R/W of TOCL in bit table changed
		613	22.2.29 Timer A/D Converter Start Request Control Register (TADCR), Note 4 for TADCR (MTU7) changed
		626, 627	22.2.36 Timer Interrupt Skipping Counters 2 (TITCNT2A and TITCNT2B), changed
		629	Figure 22.7 Periodic Counter Operation, changed
		644	Figure 22.24 Cascaded Operation Example (c), notes changed
		646	22.3.5 PWM Modes, (a) PWM Mode 1, changed
		670	Figure 22.42 Example of Operation without Dead Time (MTU3 and MTU4), changed
		676, 677	Figure 22.47 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1) to Figure 22.49 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3), changed
		682	Figure 22.57 Timing for Synchronous Counter Clearing (MTU3 and MTU4), changed
		684, 685	Figure 22.59 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 22.57; Bit WRE of TWCRA or TWCRB is 1) to Figure 22.62 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 22.57; Bit WRE of TWCRA or TWCRB is 1), changed
		688, 689	Figure 22.65 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 22.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7) to Figure 22.68 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 22.57; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7), changed
		690	(p) Counter Clearing by MTU3.TGRA (MTU6.TGRA) Compare Match, description changed
		690	Figure 22.69 Example of Counter Clearing Operation by MTU3.TGRA Compare Match, changed
		698	Figure 22.80 Example of Operation when Buffer Transfer is Disabled (BTE[1:0] = 01b), changed
		700	Figure 22.82 Relationship between Bits T3AEN and T4VEN in TITCR1A and Buffer Transfer-Enabled Period, changed
		713	Figure 22.99 Example of Motor Control Circuit Configuration, changed
		717	22.4.2 DMAC or DTC Activation, title and description changed
		728, 729	Figure 22.119 TGI Interrupt Timing (Input Capture) (MTU0 to MTU4, MTU6, and MTU7), Figure 22.120 TGI Interrupt Timing (Input Capture) (MTU5), changed
		732	22.6.2 Input Clock Restrictions, description changed
		732	Figure 22.124 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode, changed
		733	Figure 22.125 Contention between TCNT Write and Clear Operations, title changed
		747	22.7.3 Overview of Initialization Procedures and Mode Transitions in Case of Error during Operation, description changed
		751	(4) Operation when Error Occurs in Normal Mode and Operation is Restarted in Phase Counting Mode, notes changed
		773	(29) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Reset-Synchronized PWM Mode, description changed
		23. Port Output Enable 3 (POE3)	
		774	Description, changed
		774	Table 23.1 POE3 Specifications, changed
		775	Figure 23.1 POE3 Block Diagram, changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	776	Table 23.2 POE3 Input/Output Pins, changed
		777	Table 23.3 Pin Combinations, changed
		778	23.2.1 Input Level Control/Status Register 1 (ICSR1), description of POE0F flag changed
		779	23.2.2 Input Level Control/Status Register 2 (ICSR2), added
		780	23.2.3 Output Level Control/Status Register 1 (OCSR1), description of OCF1 flag changed
		781	23.2.4 Output Level Control/Status Register 2 (OCSR2), added
		782, 783	23.2.5 Active Level Setting Register 1 (ALR1), changed
		784	23.2.6 Active Level Setting Register 2 (ALR2), added
		789	23.2.10 Input Level Control/Status Register 7 (ICSR7), added
		790, 791	23.2.11 Software Port Output Enable Register (SPOER), changed
		792	23.2.12 Port Output Enable Control Register 1 (POECR1), description changed
		793, 794	23.2.13 Port Output Enable Control Register 2 (POECR2), changed
		795, 796	23.2.14 Port Output Enable Control Register 3 (POECR3), added
		797 to 799	23.2.15 Port Output Enable Control Register 4 (POECR4), changed
		800, 801	23.2.16 Port Output Enable Control Register 5 (POECR5), changed
		802 to 804	23.2.17 Port Output Enable Control Register 6 (POECR6), changed
		805	23.2.18 Port Output Enable Control Register 7 (POECR7), added
		806	23.2.19 Port Output Enable Control Register 8 (POECR8), added
		809 to 814	Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions], added
		815 to 817	Table 23.5 Target Pins and Conditions for High-Impedance Control [64- and 48-Pin Versions], title changed
		818	Figure 23.2 Target Pins and Conditions for High-Impedance Control, changed
		819	23.3.1 Input Level Detection Operation, description changed
		821	23.3.4 High-Impedance Control through Detection of Stopped Oscillation to 23.3.7 Release from High-Impedance State, description changed
		822	Table 23.6 Interrupt Sources and Conditions, changed
		24. General PWM Timer (GPT)	
		823	Description, changed
		823	Table 24.1 Specifications of GPT, changed
		824, 825	Table 24.2 Functions of GPT (GPT0 to GPT3), title and description changed
		825, 826	Table 24.3 Functions of GPT (GPT4 to GPT7), added
		827	Figure 24.1 Block Diagram of GPT, changed
		828	Table 24.4 I/O Pins of GPT, changed
		829 to 854	24.2.1 General PWM Timer Software Start Register (GTSTR) to 24.2.16 LOCO Count Upper/Lower Permissible Deviation Register (LCNTDU, LCNTDL), address added
		855 to 879	24.2.17 General PWM Timer I/O Control Register (GTIOR) to 24.2.37 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR), addresses added
		835 to 838	24.2.4 General PWM Timer Hardware Start Source Select Register (GTHSSR), changed
		839 to 842	24.2.5 General PWM Timer Hardware Stop/Clear Source Select Register (GTHPSR), changed
		843	24.2.6 General PWM Timer Write-Protection Register (GTWP), changed
		846	24.2.8 General PWM Timer External Trigger Input Interrupt Register (GTETINT), Note 1 and description changed
		850, 851	24.2.11 LOCO Count Control Register (LCCR), changed
		852	24.2.12 LOCO Count Status Register (LCST), Note 1 changed
		853	24.2.15 LOCO Count Result Register n (LCNTn) (n = 00 to 15), description changed
		855, 856	24.2.17 General PWM Timer I/O Control Register (GTIOR), Note 1 and description changed
		864	24.2.22 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC), description of IVTC[1:0] in bit table changed
		866	24.2.23 General PWM Timer Status Register (GTST), Note 1 changed
		869	24.2.24 General PWM Timer Counter (GTCNT), 24.2.31 A/D Converter Start Request Timing Double-Buffer Register m (GTADTDBRm) (m = A, B), description changed
		872 to 875	24.2.32 General PWM Timer Output Negate Control Register (GTONCR), changed
		877	24.2.34 General PWM Timer Dead Time Value Register m (GTDVm) (m = U, D), 24.2.35 General PWM Timer Dead Time Buffer Register m (GTDBm) (m = U, D), description changed
		880	24.3.1 Basic Operation, description changed
		884	24.3.1.2 Waveform Output by Compare Match, changed
		901	24.3.3 PWM Output Operating Mode, (1) Saw-Wave PWM Mode, changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	914	Figure 24.39 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 1, GTDVU and GTDVD Set to Buffer Operation, Active Level: High), changed
		914	Figure 24.40 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 2 or 3, GTDVU and GTDVD Set to Buffer Operation, Active Level: High), changed
		918	24.3.6 Hardware Start/Stop and Clear Operation, description changed
		920	24.3.6.2 Hardware Stop Operation, description changed
		922	Figure 24.48 Example of Count Start/Stop Operation by Hardware Source (Started at Rising Edge of GTETRGn (n = 0, 1) Pin Input, Stopped at Falling Edge of GTETRGn (n = 0, 1) Pin Input), title and description changed
		927	24.3.7.1 Synchronized Clear Operation, description changed
		930	24.3.7.2 Synchronized Start Operation, (1) Simultaneous Start by Software to (4) Phase Start by Hardware Source, description changed
		943, 944	Table 24.6 GPT Interrupt Sources, changed
		946	24.4.1 Interrupt Sources and Priorities, (5) Notes on Using Multiple Interrupt Sources Simultaneously, description changed
		947	24.4.2 DMAC or DTC Activation, title and description changed
		953	24.6 IWDTCLK Count Function, description changed
		956	24.7.1 Write-Protection for Registers, description changed
		963	Figure 24.90 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low), changed
		966	24.9.2 Settings of GTCCRn during Compare Match Operation (n = A, B, C, D, E, F), (3) When automatic dead time setting has been made in saw-wave one-shot pulse mode, description changed
		967	24.9.5 Target Channels for Synchronous Operation, added
		27. Independent Watchdog Timer (IWDTa)	
		990, 991	Table 27.1 Specifications of IWDT, changed
		1001, 1002	27.3.3 Refresh Operation, description changed
		1002, 1003	Figure 27.6 IWDT Refresh Operation Waveforms (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b), Figure 27.7 IWDT Refresh Operation Waveforms (IWDTCR.CKS[3:0] = 0010b, IWDTCR.TOPS[1:0] = 01b), changed
		1004	27.3.7 Reading the Down-Counter Value, description changed
		1004, 1005	Figure 27.8 Processing for Reading IWDT Down-Counter Value (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b), Figure 27.9 Processing for Reading IWDT Down-Counter Value (IWDTCR.CKS[3:0] = 0010b, IWDTCR.TOPS[1:0] = 11b), changed
		28. USB 2.0 Host/Function Module (USBa)	
		1006 to 1110	Added
		29. Serial Communications Interface (SCIc, SCId)	
		1111	Description, changed
		1111	29.1 Overview, description changed
		1111, 1112	Table 29.1 Specifications of SCIc, changed
		1112, 1113	Table 29.2 Specifications of SCId, changed
		1113	Table 29.3 List of Functions of SCI Channels, changed
		1114	Figure 29.1 Block Diagram of SCI0 to SCI3, changed
		1114	Figure 29.2 Block Diagram of SCI12 (SCId), changed
		1115, 1116	Table 29.4 Input and Output Pins of the SCIs (Asynchronous/Clock Synchronous Modes), changed
		1116	Table 29.5 Pin Configuration of SCI (Simple I^2C Mode), changed
		1116	Table 29.6 Pin Configuration of SCI (Simple SPI Mode), changed
		1117, 1118 to 1147	29.2.2 Receive Data Register (RDR), 29.2.3 Transmit Data Register (TDR), 29.2.5 Transmit Data Register (TDR) to 29.2.16 SPI Mode Register (SPMR), addresses added
		1121, 1122	29.2.6 Serial Control Register (SCR), (1) Serial Communications Interface Mode (SMIF in SCMR = 0), changed
		1125, 1126	29.2.7 Serial Status Register (SSR), (1) Serial Communications Interface Mode (SMIF in SCMR = 0), changed
		1131	Table 29.11 Base Clock Settings in Smart Card Interface Mode, changed
		1133	Table 29.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (4), changed
		1134	Table 29.13 Maximum Bit Rate for Each Operating Frequency (Asynchronous Mode), changed
		1134	Table 29.14 Maximum Bit Rate with External Clock Input (Asynchronous Mode), changed
		1135	Table 29.15 BRR Settings for Various Bit Rates (Clock Synchronous Mode, Simple SPI Mode), Note 1 changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	1135	Table 29.16 Maximum Bit Rate with External Clock Input (Clock Synchronous Mode, Simple SPI Mode), changed
		1136	Table 29.18 Maximum Bit Rate for Each Operating Frequency (Smart Card Interface Mode, S = 372), changed
		1138, 1139	29.2.10 Serial Extended Mode Register (SEMR), changed
		1149	29.2.20 Control Register 2 (CR2), changed
		1161	29.3.3 Clock, description changed
		1164	Figure 29.9 Example of Serial Transmission Flowchart in Asynchronous Mode, changed
		1168	Figure 29.13 Example of Serial Reception Flowchart (2) (Asynchronous Mode), changed
		1170	Figure 29.15 Example of Multi-Processor Serial Transmission Flowchart, changed
		1173	Figure 29.18 Example of Multi-Processor Serial Reception Flowchart (2), changed
		1175, 1177, 1180, 1195, 1197, 1199	Figure 29.20 Example of SCI Initialization Flowchart (Clock Synchronous Mode), Figure 29.22 Example of Serial Transmission Flowchart (Clock Synchronous Mode), Figure 29.26 Example of Simultaneous Serial Transmission and Reception Flowchart (Clock Synchronous Mode), Figure 29.44 Example of the Flow of SCI Initialization (for Simple I^2C Mode), Figure 29.47 Example of the Procedure for Master Transmission Operations in Simple I^2C Mode (with Transmission Interrupts and Reception Interrupts in Use), Figure 29.49 Example of the Procedure for Master Reception Operations in Simple I^2C Mode (with Transmission Interrupts and Reception Interrupts in Use), changed
		1179	Figure 29.25 Example of Serial Reception Flowchart (Clock Synchronous Mode), changed
		1190	29.6.8 Clock Output Control, (2) At Mode Switching, description changed
		1201	29.8.3 SS Function in Slave Mode, description changed
		1205	Figure 29.54 Sample Flowchart for Transmission of a Start Frame (1), changed
		1209	Figure 29.57 Sample Flowchart for Reception of a Start Frame (1), changed
		1214	Figure 27.62 Example of Operations with the Digital Filter, changed
		1220	Table 29.26 SCI Interrupt Sources, Note 1 deleted
		1222	29.12.1 Setting the Module-Stop Function, description changed
		1222	29.12.3 The Mark State and Production of Breaks, description changed
		1223	29.12.9 SCI Operations during Low Power Consumption State, (1) Transmission, description changed
		1224	Figure 29.68 Example of Flowchart for Transition to Software Standby Mode during Transmission, changed
		1225	Figure 29.69 Port Pin States during Transition to Software Standby Mode (Internal Clock, Asynchronous Transmission), changed
		1225	Figure 29.70 Port Pin States during Transition to Software Standby Mode (Internal Clock, Clock Synchronous Transmission), changed
		1227	29.12.11 Limitations on Simple SPI Mode, (1) Master Mode, description changed
		30. I^2C Bus Interface (RIIC)	
		1229	Description changed
		1230	Figure 30.1 Block Diagram of RIIC, changed
		1231	Table 30.2 Pin Configuration, changed
		1232 to 1258	30.2.1 I^2C Bus Control Register 1 (ICCR1) to 30.2.18 Timeout Internal Counter (TMOCNT), address added
		1232, 1233	30.2.1 I^2C Bus Control Register 1 (ICCR1), changed
		1234 to 1236	30.2.2 I^2C Bus Control Register 2 (ICCR2), changed
		1237	30.2.3 I^2C Bus Mode Register 1 (ICMR1), changed
		1238, 1239	30.2.4 I^2C Bus Mode Register 2 (ICMR2), changed
		1240, 1241	30.2.5 I^2C Bus Mode Register 3 (ICMR3), changed
		1242, 1243	30.2.6 I^2C Bus Function Enable Register (ICFER), changed
		1249 to 1252	30.2.10 I^2C Bus Status Register 2 (ICSR2), description changed
		1250	Table 30.4 Relationship between Arbitration-Lost Generation Sources and Arbitration-Lost Enable Functions, changed
		1255	30.2.14 I^2C Bus Bit Rate High-Level Register (ICBRH), description changed
		1256	Table 30.5 Examples of ICBRH/ICBRL Settings for Transfer Rate: (1) to (3), notes changed
		1257	30.2.16 I^2C Bus Receive Data Register (ICDRR), description changed
		1257	30.2.17 I^2C Bus Shift Register (ICDRS), description changed
		1258	30.2.18 Timeout Internal Counter (TMOCNT), changed
		1259	Figure 30.4 I^2C Bus Timing (SLA = 7 Bits), description changed
		1260	Figure 30.5 Example of RIIC Initialization Flowchart, changed
		1261	30.3.3 Master Transmit Operation, (2), (4), description changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	1262	Figure 30.6 Example of Master Transmission Flowchart, changed
		1263, 1264	Figure 30.7 Master Transmit Operation Timing (1) (7-Bit Address Format) to Figure 30.9 Master Transmit Operation Timing (3), changed
		1264, 1265	30.3.4 Master Receive Operation, (2), (5), description changed
		1266	Figure 30.10 Example of Master Reception Flowchart (7-Bit Address Format), changed
		1267, 1268	Figure 30.11 Master Receive Operation Timing (1) (7-Bit Address Format, when RDRFS = 0) to Figure 30.13 Master Receive Operation Timing (3) (when RDRFS = 0), changed
		1268	30.3.5 Slave Transmit Operation, (4), (5), description changed
		1269	Figure 30.14 Example of Slave Transmission Flowchart, changed
		1270	Figure 30.15 Slave Transmit Operation Timing (1) (7-Bit Address Format), Figure 30.16 Slave Transmit Operation Timing (2), changed
		1271	30.3.6 Slave Receive Operation, (4), description changed
		1272	Figure 30.17 Example of Slave Reception Flowchart, changed
		1273	Figure 30.18 Slave Receive Operation Timing (1) (7-Bit Address Format, when RDRFS = 0), Figure 30.19 Slave Receive Operation Timing (2) (when RDRFS = 0), changed
		1274	30.4 SCL Synchronization Circuit, description changed
		1274	Figure 30.20 Generation and Synchronization of the SCL Signal from the RIIC, changed
		1276	30.6 Digital Noise-Filter Circuits, description changed
		1277	Figure 30.23 AASy Flag Set Timing with 7-Bit Address Format Selected to Figure 30.25 AASy Flag Set/Clear Timing with 7-Bit/10-Bit Address Formats Mixed, changed
		1279	Figure 30.26 Timing of GCA Flag Setting during Reception of General Call Address, changed
		1280	Figure 30.27 AASy/DID Flag Set/Clear Timing during Reception of Device-ID, changed
		1280	30.7.4 Host Address Detection, description changed
		1281	Figure 30.28 HOA Flag Set Timing during Reception of Host Address, changed
		1281, 1283	30.8.1 Function to Prevent Wrong Transmission of Transmit Data, 30.8.3 Function to Prevent Failure to Receive Data, description changed
		1282 to 1284	Figure 30.29 Automatic Low-Hold Operation in Transmit Mode to Figure 30.31 Automatic Low-Hold Operation in Receive Mode (Using RDRFS and WAIT Bits), changed
		1285	30.9.1 Master Arbitration-Lost Detection (MALE Bit), description changed
		1286	Figure 30.32 Examples of Master Arbitration-Lost Detection (MALE = 1), changed
		1287	30.9.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit), description changed
		1287	Figure 30.34 Example of Arbitration-Lost Detection during Transmission of NACK (NALE = 1), changed
		1288	30.9.3 Slave Arbitration-Lost Detection (SALE Bit), description changed
		1288	Figure 30.35 Example of Slave Arbitration-Lost Detection (SALE = 1), changed
		1289	30.10.1 Issuing a Start Condition, 30.10.2 Issuing a Restart Condition, description changed
		1289	Figure 30.36 Start Condition/Restart Condition Issue Timing (ST and RS Bits), changed
		1290	30.10.3 Issuing a Stop Condition, description changed
		1290	Figure 30.37 Stop Condition Issue Timing (SP Bit), changed
		1291	30.11 Bus Hanging, 30.11.1 Timeout Function to 30.11.3 RIIC Reset and Internal Reset, description changed
		1291	Figure 30.38 Timeout Function (TMOE, TMOS, TMOH, and TMOL Bits), Figure 30.39 Extra SCL Clock Cycle Output Function (CLO Bit), changed
		1293	30.12.1 SMBus Timeout Measurement, description changed
		1294	Figure 30.40 SMBus Timeout Measurement, changed
		1295	30.12.2 Packet Error Code (PEC), description changed
		1298	30.15 Usage Notes, changed
		31. CAN Module (CAN)	
		1299 to 1352	Added
		32. Serial Peripheral Interface (RSPI)	
		1353	32.1 Overview, description changed
		1353	Table 32.1 Specifications of RSPI, changed
		1355	Table 32.2 RSPI Pin Configuration, changed
		1356 to 1375	32.2.1 RSPI Control Register (SPCR) to 32.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7), address added
		1356, 1357	32.2.1 RSPI Control Register (SPCR), description changed
		1359	32.2.3 RSPI Pin Control Register (SPPCR), changed
		1360	32.2.4 RSPI Status Register (SPSR), description changed
		1366	32.2.7 RSPI Sequence Status Register (SPSSR), description changed

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	1369	Table 32.4 Settable Combinations of SPSLN[2:0] Bits and SPFC[1:0] Bits, allocation changed
		1370, 1371	32.2.10 RSPI Clock Delay Register (SPCKD) to 32.2.12 RSPI Next-Access Delay Register (SPND), description changed
		1373 to 1375	32.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7), description changed
		1376	Table 32.5 Relationship between RSPI Modes and SPCR Settings and Description of Each Mode, changed
		1377	32.3.2 Controlling RSPI Pins, description changed
		1377	Table 32.6 Relationship between Pin States and Bit Settings, changed
		1378 to 1383	32.3.3.1 Single Master/Single Slave (with This LSI Acting as Master) to 32.3.3.7 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) (with This LSI Acting as Slave), description changed
		1378 to 1383	Figure 32.5 Single-Master/Single-Slave Configuration Example (This LSI = Master) to Figure 32.12 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) Configuration Example (This LSI = Slave, CPHA = 1), changed
		1385 to 1392	Figure 32.15 MSB-First Transfer (32-Bit Data, Parity Disabled) to Figure 32.22 LSB-First Transfer (24-Bit Data, Parity Enabled), changed
		1393	32.3.5.1 CPHA = 0, 32.3.5.2 CPHA = 1, description changed
		1393, 1394	Figure 32.23 RSPI Transfer Format (CPHA = 0), Figure 32.24 RSPI Transfer Format (CPHA = 1), changed
		1395, 1396	32.3.6.1 Full-Duplex Synchronous Serial Communications (SPCR.TXMD = 0), 32.3.6.2 Transmit Operations Only (SPCR.TXMD = 1), description changed
		1395, 1396	Figure 32.25 Operation Example of SPCR.TXMD = 0, Figure 32.26 Operation Example of SPCR.TXMD = 1, changed
		1397	32.3.7 Transmit Buffer Empty/Receive Buffer Full Interrupts, description changed
		1397	Figure 32.27 Operation Example of SPTI and SPRI Interrupts, changed
		1399	Table 32.8 Relationship between Non-Normal Transfer Operations and RSPI Error Detection Function, changed
		1400	32.3.8.1 Overrun Error to 32.3.8.3 Mode Fault Error, description changed
		1400	Figure 32.28 Operation Example of OVRF Flag, Figure 32.29 Operation Example of PERF Flag, changed
		1404 to 1407	32.3.10.1 Master Mode Operation, (1) Starting a Serial Transfer to (4) Burst Transfer, description changed
		1407	Figure 32.33 Example of Burst Transfer Operation using SSLKP Bit, changed
		1414	32.3.10.2 Slave Mode Operation, (1) Starting a Serial Transfer to (4) Burst Transfer, description changed
		1415	Figure 32.38 Example of Initialization Flowchart in Slave Mode (SPI Operation), changed
		1418	32.3.11 Clock Synchronous Operation, description changed
		1418	32.3.12 Master Mode Operation, (1) Starting a Serial Transfer to (3) Sequence Control, description changed
		1422	32.3.13 Slave Mode Operation, (1) Starting a Serial Transfer and (2) Terminating a Serial Transfer, description changed
		1424	32.3.14 Loopback Mode, description changed
		1424	Table 32.12 SPLP2 and SPLP Bit Settings and Received Data, changed
		1424	Figure 32.47 Configuration of Shift Register I/O Paths in Loopback Mode (Master Mode), changed
		1427	32.4.1 Setting Module-Stop Function, description changed
		34. 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions]	
		1435 to 1514	Added
		35. 12-Bit A/D Converter (S12ADB) [64- and 48-Pin Versions]	
		1515	Title changed
		1516	Table 35.1 Specifications of 12-Bit A/D Converter (2/2), changed
		1524 to 1527	35.2.3 A/D Control Register (ADCSR), changed
		1539, 1540	35.2.12 A/D Group Scan Priority Control Register (ADGSPCR), changed
		1541, 1542	35.2.14 Comparator Operating-Mode Selection Register 1 (ADCMPMD1), changed
		1545	35.3. Operation, changed
		1550	35.5 A/D Conversion Accuracy Definitions, changed
		36. 10-Bit A/D Converter (AD)	
		1556 to 1592	Added
		37. D/A Converter (DAa)	
		1593 to 1600	Added

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2013	39. RAM	
		1607	39.1 Overview, description changed
		1607	Table 39.1 Specifications of RAM, title and description changed
		1607	39.2.1 Low-Power Consumption Function, description changed
		40. Flash Memory	
		1608 to 1696	34. ROM (Flash Memory for Code Storage) and 35. E2 DataFlash Memory (Flash Memory for Data Storage) are combined into 40. Flash Memory
		41. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		1697 to 1741	Added
		42. Electrical Characteristics [64- and 48-Pin Versions]	
		1742	Title changed
		1745	Table 42.6 Clock Timing, changed
		1751	Table 42.10 Timing of On-Chip Peripheral Modules (1), changed
		1753	Table 42.12 Timing of On-Chip Peripheral Modules (3), changed
		1763	42.6 Oscillation Stop Detection Circuit Characteristics, title changed
		1763	Table 42.18 Oscillation Stop Detection Circuit Characteristics, title changed
		1764	Table 42.19 ROM (Flash Memory for Code Storage) Characteristics (1), added
		1764	Table 42.20 ROM (Flash Memory for Code Storage) Characteristics (2), title and description changed
		1765	Table 42.21 DataFlash (Flash Memory for Data Storage) Characteristics (1), added
		1765	Table 42.22 DataFlash (Flash Memory for Data Storage) Characteristics (2), title and description changed
		Appendix 1. Port States in Each Processing Mode	
		1767	[144-, 120-, 112- and 100-Pin Versions], description added
		1767 to 1770	Table 1.1 Port States in Each Processing State, added
		1771	[64- and 48-Pin Versions], description added
		Appendix 2. Package Dimensions	
		1772 to 1775	Figure A 144-Pin LQFP (PLQP0144KA-A) to Figure D 100-Pin LQFP (PLQP0100KB-A), added
2.10	Sep 12, 2013	The RX63T Group and RX63T changed to this MCU	
		Features	
		45	Changed
		1. Overview	
		46 to 52	Table 1.1 Outline of Specifications, changed, Note 1, added.
		53	Table 1.2 Comparison of Functions for Different Packages, changed, Note 2, added.
		54 to 58	Table 1.3 List of Products, changed, Note 1, added
		59	Figure 1.1 How to Read the Product Part Number, changed
		72 to 75	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed
		76 to 79	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed
		80 to 83	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		84 to 86	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		87 to 89	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		90 to 91	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		6. I/O Registers	
		136 to 191	Table 6.1 List of I/O Registers (Address Order), changed
		10. Clock Generation Circuit	
		229	Table 10.1 Specifications of Clock Generation Circuit, changed
		230	Figure 10.1 Block Diagram of Clock Generation Circuit, changed
		12. Low Power Consumption	
		269	12.2.4 Module Stop Control Register C (MSTPCRC), changed
		280	12.3 Reducing Power Consumption by Switching Clock Signals, changed
		15. Interrupt controller (ICUb)	
		325 to 332	Table 15.3 Interrupt Vector Table, changed
		344	15.5.5 Multiple Interrupt, added
		344	15.5.6 Fast Interrupt, changed
		16. Buses	
		350	Table 16.1 Bus Specifications, changed
		353	Table 16.4 Connection of Peripheral Modules to the Internal Peripheral Buses, changed
		20. I/O Ports	
		508	20.3.5 Open Drain Control Register 0 (ODR0), changed

Rev.	Date	Description	
		Page	Summary
2.10	Sep 12, 2013	21. Multi-Function Pin Controller (MPC)	
		526	Table 21.11 Register Settings for Input/Output Pin Function in 112-Pin LQFP, 100-Pin LQFP, changed
		536	Table 21.26 Register Settings for Input/Output Pin Function in 144-Pin LQFP, 120-Pin LQFP, 112-Pin LQFP, 100-Pin LQFP, changed
		22. Multi-Function Timer Pulse Unit 3 (MTU3)	
		553	Table 22.1 Specifications of MTU, changed
		557	Figure 22.1 Block Diagram of MTU (MTU0 to MTU4), changed
		558	Figure 22.2 Block Diagram of MTU (MTU5 to MTU7), changed
		564	22.2.2 Timer Mode Register 1 (TMDR1),changed
		567	22.2.4 Timer I/O Control Register (TIOR), changed
		585	22.2.5 Timer Compare Match Clear Register (TCNTCMPCLR), changed
		586	22.2.6 Timer Interrupt Enable Register (TIER), changed
		596	22.2.9 Timer Input Capture Control Register (TICCR), changed
		599	22.2.13 Timer Start Register (TSTR), changed
		606	22.2.17 Timer Output Master Enable Register (TOER), changed
		608	22.2.18 Timer Output Control Registers 1 (TOCR1A and TOCR1B), changed
		609	Table 22.37 Output Level Select Function, changed
		609	Table 22.38 Output Level Select Function, changed
		613	22.2.21 Timer Gate Control Register A (TGCRA), changed
		614	22.2.23 Timer Cycle Data Registers (TCDRA and TCDRB), changed
		618	22.2.28 Timer Waveform Control Registers (TWCRA and TWCRB), changed
		624	22.2.30 Timer A/D Converter Start Request Cycle Set Registers (TADCORA and TADCORB), changed
		629	22.2.34 Timer Interrupt Skipping Counters 1 (TITCNT1A and TITCNT1B), changed
		634	22.2.37 Bus Master Interface, changed
		638	Figure 22.9 Example of low output and high output Operation, changed
		638	Figure 22.10 Example of Toggle Output Operation, changed
		639	22.3.1 Basic Functions, (3) Input Capture Function, changed
		640	22.3.1 Basic Functions, (3) Input Capture Function, (b) Example of Input Capture Operation, changed
		640	Figure 22.12 Example of Input Capture Operation, changed
		645	Figure 22.18 Example of Buffer Operation (1), changed
		646	22.3.3 Buffer Operation, (2) Examples of Buffer Operation, (b) When TGR is an Input Capture Register, changed
		646	Figure 22.19 Example of Buffer Operation (2), changed
		647	Figure 22.20 Example of Buffer Operation When MTU0.TCNT Clearing is Selected for MTU0.TGRC-to-MTU0.TGRA Transfer Timing, changed.
		648	22.3.4 Cascaded Operation, changed
		648	Table 22.59 TICCR Setting and Input Capture Input Pins, changed
		653	22.3.5 PWM Modes, changed
		653	22.3.5 PWM Modes, (a) PWM Mode 1, changed
		655	Figure 22.27 Example of PWM Mode 1 Operation, changed
		655	22.3.5 PWM Modes, (2) Examples of PWM Mode Operation, changed
		657	Figure 22.29 Examples of PWM Mode Operation (PWM Waveform Output with 0% Duty and 100% Duty), changed
		658	22.3.6 Phase Counting Mode, changed
		659	22.3.6 Phase Counting Mode, (2) Examples of Phase Counting Mode Operation, changed
		659	22.3.6 Phase Counting Mode, (2) Examples of Phase Counting Mode Operation, (a) Phase Counting Mode 1, changed
		659	Table 22.62 Up-/Down-Count Conditions in Phase Counting Mode 1, changed
		660	22.3.6 Phase Counting Mode, (2) Examples of Phase Counting Mode Operation, (b) Phase Counting Mode 2, changed
		660	Table 22.63 Up-/Down-Count Conditions in Phase Counting Mode 2, changed
		661	22.3.6 Phase Counting Mode, (2) Examples of Phase Counting Mode Operation, (c) Phase Counting Mode 3, changed
		661	Table 22.64 Up-/Down-Count Conditions in Phase Counting Mode 3, changed
		662	22.3.6 Phase Counting Mode, (2) Examples of Phase Counting Mode Operation, (d) Phase Counting Mode 4, changed

Rev.	Date	Description	
		Page	Summary
2.10	Sep 12, 2013	662	Table 22.65 Up-/Down-Count Conditions in Phase Counting Mode 4, changed
		667	22.3.8 Complementary PWM Mode, changed
		667	Table 22.68 Output Pins for Complementary PWM Mode, changed
		672	22.3.8 Complementary PWM Mode, changed, (2) Outline of Complementary PWM Mode Operation, changed
		674	Figure 22.41 Example of Operation in Complementary PWM Mode (MTU3 and MTU4), changed
		678	22.3.8 Complementary PWM Mode, changed, (2) Outline of Complementary PWM Mode Operation, (g) PWM Cycle Setting, changed
		681	Figure 22.45 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (1)), changed
		682	Figure 22.46 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (2), changed
		683	22.3.8 Complementary PWM Mode, changed, (2) Outline of Complementary PWM Mode Operation, (j) Method for Generating PWM Output in Complementary PWM Mode, changed
		698	Figure 22.70 Example of Output Phase Switching by External Input (1), changed
		698	Figure 22.71 Example of Output Phase Switching by External Input (2), changed
		699	Figure 22.72 Example of Output Phase Switching through UF, VF, and WF Bit Settings (1), changed
		699	Figure 22.73 Example of Output Phase Switching through UF, VF, and WF Bit Settings (2), changed
		720	Figure 22.99 Example of Motor Control Circuit Configuration, changed
		721	22.3.13 TCNT Capture at Crest and/or Trough in Complementary PWM Mode, changed
		721	Figure 22.100 TCNT Capture at Crest and/or Trough in Complementary PWM Operation, changed
		722	22.4.1 Interrupt Sources and Priorities, (1) Input Capture/Compare Match Interrupt, changed
		727	22.5.1 Input/Output Timing, (2) Output Compare Output Timing, changed
		728	Figure 22.105 Output Compare Output Timing (Normal Mode or PWM Mode), changed
		729	Figure 22.106 Output Compare Output Timing (Complementary PWM Mode or Reset-Synchronized PWM Mode), changed
		736	Figure 22.120 TGI Interrupt Timing (Input Capture) (MTU5), changed
		739	22.6.1 Module Stop Function Setting, changed
		739	22.6.2 Input Clock Restrictions, changed
		739	Figure 22.124 Phase Difference, Overlap, and Pulse Width in Phase, changed
		740	22.6.4 Contention between TCNT Write and Clear Operations, changed
		740	Figure 22.125 Contention between TCNT Write and Clear Operations, changed
		740	22.6.5 Contention between TCNT Write and Increment Operations, changed
		740	Figure 22.126 Contention between TCNT Write and Increment Operations, changed
		741	22.6.6 Contention between TGR Write Operation and Compare Match, changed
		741	Figure 22.127 Contention between TGR Write Operation and Compare Match, changed
		741	22.6.7 Contention between Buffer Register Write Operation and Compare Match, changed
		741	Figure 22.128 Contention between Buffer Register Write Operation and Compare Match, changed
		742	22.6.8 Contention between Buffer Register Write and TCNT Clear Operations, changed
		742	Figure 22.129 Contention between Buffer Register Write and TCNT Clear Operations, changed
		743	22.6.9 Contention between TGR Read Operation and Input Capture, changed
		743	Figure 22.130 Contention between TGR Read Operation and Input Capture (MTU0 to MTU7), changed
		744	Figure 22.131 Contention between TGR Read Operation and Input Capture (MTU5), deleted
		744	22.6.10 Contention between TGR Write Operation and Input Capture, changed
		744	Figure 22.131 Contention between TGR Write Operation and Input Capture (MTU0 to MTU4, MTU6, and MTU7), changed
		744	Figure 22.132 Contention between TGR Write Operation and Input Capture (MTU5), changed
		745	22.6.11 Contention between Buffer Register Write Operation and Input Capture, changed
		745	Figure 22.133 Contention between Buffer Register Write Operation and Input Capture, changed
		746	Figure 22.134 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation, changed
		747	22.6.14 Buffer Operation Setting in Complementary PWM Mode, changed
		748	22.6.15 Buffer Operation and Compare Match Flags in Reset-Synchronized PWM Mode, changed
		748	Figure 22.136 Buffer Operation and Compare Match Flags in Reset-Synchronized PWM Mode, changed
		749	22.6.16 Overflow Flags in Reset-Synchronized PWM Mode, changed
		750	Figure 22.139 Contention between TCNT Write Operation and Overflow, changed

Rev.	Date	Description	
		Page	Summary
2.10	Sep 12, 2013	751	22.6.19 Note on Transition from Normal Mode or PWM Mode 1 to Reset-Synchronized PWM Mode, changed
		751	22.6.20 Output Level in Complementary PWM Mode and Reset-Synchronized PWM Mode, changed
		752	22.6.23 Note on Complementary PWM mode when Output Protection Function is Not Used, added
		753	22.6.24 Preventing Malfunctions at Synchronous Clearing in Complementary PWM Mode, added
		753	Figure 22.140 Example of Synchronous Clearing (Condition 1), added
		754	Figure 22.141 Example of Synchronous Clearing (Condition 2), added
		754	22.6.25 Continuous Output of Interrupt Signal in Response to a Compare Match, added
		754	Figure 22.143 Continuous Output of Interrupt Signal in Response to a Compare Match, added
		755	22.7.2 Operation in Case of Re-Setting Due to Error during Operation, changed
		755	Table 22.74 Mode Transition Combinations, changed
		23. Port Output Enable 3 (POE3)	
		784	Figure 23.1 POE3 Block Diagram, changed
		787	23.2.1 Input Level Control/Status Register 1 (ICSR1), changed
		789	23.2.2 Input Level Control/Status Register 2 (ICSR2), changed
		798	23.2.7 Input Level Control/Status Register 3 (ICSR3), changed
		798	23.2.8 Input Level Control/Status Register 4 (ICSR4), changed
		799	23.2.9 Input Level Control/Status Register 5 (ICSR5), changed
		800	23.2.10 Input Level Control/Status Register 7 (ICSR7), changed
		801	23.2.11 Software Port Output Enable Register (SPOER), changed
		804	23.2.12 Port Output Enable Control Register 1 (POECR1), changed
		805	23.2.13 Port Output Enable Control Register 2 (POECR2), changed
		807	23.2.14 Port Output Enable Control Register 3 (POECR3), changed
		817	23.2.18 Port Output Enable Control Register 7 (POECR7), changed
		831	23.3.1 Input Level Detection Operation, (2) Low Detection, changed
		832	Figure 23.5 Output-Level Compare Operation, changed
		833	23.3.3 High-Impedance Control Using Registers, changed
		833	23.3.4 High-Impedance Control through Detection of Stopped Oscillation, changed
		833	23.3.5 High-impedance Control through Detection of the Comparator, changed
		833	23.3.6 Additional Functions for Controlling High-Impedance States, changed
		834	23.3.7 Release from High-Impedance State, changed
		24. General PWM Timer (GPT)	
		835	Table 24.1 Specifications of GPT, changed
		839	Figure 24.1 Block Diagram of GPT, changed
		867	24.2.17 General PWM Timer I/O Control Register (GTIOR), changed
		870	24.2.18 General PWM Timer Interrupt Output Setting Register (GTINTAD), changed
		872	24.2.19 General PWM Timer Control Register (GTCR), changed
		874	24.2.20 General PWM Timer Buffer Enable Register (GTBER), changed
		876	24.2.21 General PWM Timer Count Direction Register (GTUDC), changed
		877	24.2.22 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC), changed
		879	24.2.23 General PWM Timer Status Register (GTST), changed
		882	24.2.24 General PWM Timer Counter (GTCNT), changed
		883	24.2.25 General PWM Timer Compare Capture Register m (GTCCRm) (m = A to F), changed
		883	24.2.26 General PWM Timer Cycle Setting Register (GTPR), changed
		883	24.2.27 General PWM Timer Cycle Setting Buffer Register (GTPBR), changed
		884	24.2.28 General PWM Timer Cycle Setting Double-Buffer Register (GTPDBR), changed
		884	24.2.29 A/D Converter Start Request Timing Register m (GTADTRm) (m = A, B), changed
		884	24.2.30 A/D Converter Start Request Timing Buffer Register m (GTADTBRm) (m = A, B), changed
		885	24.2.31 A/D Converter Start Request Timing Double-Buffer Register m (GTADTDBRm) (m = A, B), changed
		885	24.2.32 General PWM Timer Output Negate Control Register (GTONCR), changed
		889	24.2.33 General PWM Timer Dead Time Control Register (GTDTCR), changed
		890	24.2.34 General PWM Timer Dead Time Value Register m (GTDVm) (m = U, D), changed
		890	24.2.35 General PWM Timer Dead Time Buffer Register m (GTDBm) (m = U, D), changed
		892	24.2.37 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR), changed
		893	24.2.38 PWM Output Delay Control Register (GTDLYCR), added

Rev.	Date	Description	
		Page	Summary
2.10	Sep 12, 2013	894	24.2.39 GTIOCA Rising Output Delay Register (GTDLYRA), added
		895	24.2.40 GTIOCA Falling Output Delay Register (GTDLYFA), added
		896	24.2.41 GTIOCB Rising Output Delay Register (GTDLYRB), added
		897	24.2.42 GTIOCB Falling Output Delay Register (GTDLYFB), added
		903	Figure 24.7 Example for Setting Low Output and High Output Operation, changed
		905	Figure 24.10 Example for Setting Toggled Output, changed
		913	Figure 24.20 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Output Compare), changed
		920	Figure 24.29 Example for Setting Saw-Wave PWM Mode, changed
		923	Figure 24.31 Example for Setting Saw-Wave One-Shot Pulse Mode, changed
		925	Figure 24.33 Example for Setting Triangle-Wave PWM Mode 1, changed
		927	Figure 24.35 Example for Setting Triangle-Wave PWM Mode 2, changed
		930	Figure 24.37 Example for Setting Triangle-Wave PWM Mode 3, changed
		933	Figure 24.41 Example for Setting Automatic Dead Time Setting Function (Saw-Wave One-Shot Pulse Mode, Triangle-Wave PWM Mode 3), changed
		934	Figure 24.42 Example for Setting Automatic Dead Time Setting Function (Triangle-Wave PWM Mode 1 or 2), changed
		950	24.3.7.2 Synchronized Start Operation, (3) Simultaneous Start by Hardware Source, changed
		952	24.3.7.2 Synchronized Start Operation, (4) Phase Start by Hardware Source, changed
		960	24.3.9 PWM Rising/Falling Timing Adjustment, added
		960	Figure 24.69 Example of PWM Delay Generation Circuit Initialization, added
		961	Table 24.6 PWM Output Pins and Registers for Delay Setting, added
		961	24.3.10 Transfer Timing of GTDLYRA, GTLDYRB, GTDLYFA, and GTDLYFB Registers Values, added
		962	Figure 24.70 Operation Example of GTDLYRA (Sawtooth Waveform PWM), added
		962	Figure 24.71 Operation Example of GTDLYFA (Triangle Waveform PWM), added
		974	24.6 IWDTCLK Count Function, changed
		977	24.7 Protection Function, changed
		977	Table 24.10 Write-Protected Registers, added
		985	24.7.5 High-Impedance Control of GTIOC Pin Output by POE Function, changed
		986	Figure 24.95 Example of Pin Settings after Reset, changed
		986	24.8.2 Pin Initialization Due to Error during Operation, changed
		987	24.9.1 Module Stop Function Setting, changed
		987	24.9.2 Settings of GTCCRn during Compare Match Operation (n = A to F), changed
		989	24.9.6 Notes on Delay Time Setting for PWM Delay Generation Circuit, added
		989	Figure 24.96 Restriction on GTDLYFA Register Setting Timing, added
		25. Compare Match Timer (CMT)	
		990	Table 25.1 Specifications of CMT, changed
		990	Figure 25.1 Block Diagram of CMT (Unit 0), changed
		992	25.2.3 Compare Match Timer Control Register (CMCR), changed
		996	25.5.1 Setting the Module-Stop Function, changed
		28. USB 2.0 Host/Function Module (USBa)	
		1037	28.2.4 CFIFO Port Register (CFIFO), D0FIFO Port Register (D0FIFO), D1FIFO Port Register (D1FIFO), changed
		1039	28.2.5 CFIFO Port Select Register (CFIFOSEL), D0FIFO Port Select Register (D0FIFOSEL), D1FIFO Port Select Register (D1FIFOSEL), changed
		1043	28.2.6 CFIFO Port Control Register (CFIFOCTR), D0FIFO Port Control Register (D0FIFOCTR), D1FIFO Port Control Register (D1FIFOCTR), changed
		1050	28.2.12 SOF Output Configuration Register (SOFCFG), changed
		1099	Figure 28.7 shows the timing of BRDY interrupt generation., changed
		1102	Figure 28.8 Timing of NRDY Interrupt Generation (When Function Controller Function is Selected), changed
		1104	Figure 28.9 Timing of BEMP Interrupt Generation (When Function Controller Function is Selected), changed
		1113	28.3.4.7 Data PID Sequence Bit, changed
		1115	28.3.5.1 FIFO Buffer Memory, (1) Buffer Status, changed
		1117	Table 28.18 FIFO Port Function Settings, changed
		1117	28.3.5.4 DMA Transfers (D0FIFO and D1FIFO Ports), changed
		1120	28.3.6.2 Control Transfers when Function Controller Function is Selected, changed

Rev.	Date	Description	
		Page	Summary
2.10	Sep 12, 2013	1122	28.3.9.1 Error Detection in Isochronous Transfers, (e) Interval errors, changed
		1125	28.3.9.3 Interval Counter, (a) When the selected pipe is for isochronous IN transfers, changed
		1125	28.3.9.3 Interval Counter, (b) When the selected pipe is for isochronous OUT transfers, changed
		1133	28.4.1 Setting the Module-Stop Function, changed
		29. Serial Communications Interface (SCIc, SCId)	
		1137	Figure 29.1 Block Diagram of SCI0 to SCI3, changed
		1138	Figure 29.2 Block Diagram of SCI12 (SCId), changed
		1144	29.2.6 Serial Control Register (SCR), (1) Serial Communications Interface Mode (SMIF in SCMR = 0), changed
		1152	29.2.8 Smart Card Mode Register (SCMR), changed
		1177	29.2.28 Control Field 0 Receive Data Register (CF0RR), changed
		1178	29.2.32 Control Field 1 Receive Data Register (CF1RR), changed
		1197	29.5.1 Clock, changed
		1200	29.5.5 Serial Data Reception (Clock Synchronous Mode), changed
		1204	29.6.1 Sample Connection, changed
		1249	29.12.10 External Clock Input in Clock Synchronous Mode, changed
		1250	29.12.11 Limitations on Simple SPI Mode, changed
		30. I^2C Bus Interface (RIIC)	
		1257	30.2.2 I^2C Bus Control Register 2 (ICCR2), Note changed.
		1263	30.2.5 I^2C Bus Mode Register 3 (ICMR3), NF[1:0] Bits (Noise Filter Stage Selection), changed
		1272	30.2.10 I^2C Bus Status Register 2 (ICSR2), TDRE Flag (Transmit Data Empty), changed
		1278	30.2.13 I^2C Bus Bit Rate Low-Level Register (ICBRL), changed
		1278	30.2.14 I^2C Bus Bit Rate High-Level Register (ICBRH), changed
		1281	30.2.18 Timeout Internal Counter (TMOCNT), changed
		1283	30.3.2 Initial Settings, changed
		1284	30.3.3 Master Transmit Operation, changed
		1287	30.3.4 Master Receive Operation, changed
		1292	30.3.5 Slave Transmit Operation, changed
		1295	30.3.6 Slave Receive Operation, changed
		1315	30.11.1 Timeout Function, changed
		1317	30.12.1 SMBus Timeout Measurement, (1) Measuring timeout of slave device, changed
		1318	30.12.1 SMBus Timeout Measurement, (2) Measuring timeout of master device, changed
		1320	Table 30.7 Interrupt Sources, changed
		1322	30.15.1 Setting Module-Stop Function, changed
		31. CAN Module (CAN)	
		1324	Figure 31.1 Block Diagram of CAN Module (i = 1), changed
		1355	31.2.19 Error Interrupt Factor Judge Register (EIFR), BLIF Flag (Bus Lock Detect Flag), changed
		1362	Figure 31.9 Transition between CAN Operating Modes, changed
		1365	Figure 31.10 Sub-Modes of CAN Operation Mode, changed
		1376	31.9.1 Setting for the Module-Stop State, changed
		32. Serial Peripheral Interface (RSPI)	
		1380	32.2.1 RSPI Control Register (SPCR), changed
		1382	32.2.2 RSPI Slave Select Polarity Register (SSLP), changed
		1383	32.2.3 RSPI Pin Control Register (SPPCR), changed
		1386	32.2.5 RSPI Data Register (SPDR), (1) Bus Interface, (a) Writing, changed
		1392	32.2.9 RSPI Data Control Register (SPDCR), SPLW Bit (RSPI Longword Access/Word Access Specification), changed
		1394	32.2.10 RSPI Clock Delay Register (SPCKD), changed
		1395	32.2.11 RSPI Slave Select Negation Delay Register (SSLND), changed
		1395	32.2.12 RSPI Next-Access Delay Register (SPND), changed
		1396	32.2.13 RSPI Control Register 2 (SPCR2), changed
		1397	32.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7), changed
		1437	32.3.10.1 Master Mode Operation, (9) Software Processing Flow, (c) Flow of error processing, changed
		1441	32.3.10.2 Slave Mode Operation, (6) Flow of Software Processing, (c) Flow of error processing, changed
		1442	32.3.11 Clock Synchronous Operation, changed
		1451	32.4.1 Setting Module-Stop Function, changed

Rev.	Date	Description	
		Page	Summary
2.10	Sep 12, 2013	33. CRC Calculator (CRC)	
		1452	33. CRC Calculator (CRC), changed
		1452	Figure 33.1 Block Diagram of CRC Calculator, changed
		1453	33.2.1 CRC Control Register (CRCCR), changed
		1453	33.2.2 CRC Data Input Register (CRCDIR), changed
		1454	33.2.3 CRC Data Output Register (CRCDOR), changed
		1458	33.4.1 Module-Stop Function Setting, changed
		34. 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions	
		1525	34.3.5 Analog Input Sampling and Scan Conversion Time, changed
		1525	Table 34.9 Example of Setting the ADSSTRn Register, changed
		1526	Table 34.10 Times for Conversion During Scanning (in Numbers of Cycles of the ADCLK and PCLK), changed
		1527	34.3.6 Usage Example of Automatic Register Clearing Function, changed
		1535	34.6.5 Module Stop Function Setting, changed
		1535	34.6.6 Notes on Entering Low Power Consumption States, changed
		35. 12-Bit A/D Converter (S12ADB) [64- and 48-Pin Versions]	
		1576	35.6.5 Module Stop Function Setting, changed
		1576	35.6.6 Notes on Entering Low Power Consumption States, changed
		36. 10-Bit A/D Converter (AD)	
		1602	36.2.13 Digital Power Control Circuit Output Setting Register (ADDPCONR), added
		1613	36.6.5 Module Stop Function Setting, changed
		1613	36.6.6 Notes on Entering Low Power Consumption States, changed
		37. D/A Converter (DAa)	
		1617	Figure 37.1 Block Diagram of D/A Converter, changed
		1619	37.2.2 D/A Control Register (DACR), Note 2, changed
		1623	37.3.1 Measure against Interference between D/A and A/D Conversion, changed
		1624	37.4.1 Module-Stop Function Setting, changed
		1624	37.4.2 Operation of the D/A Converter in Module-Stop State, changed
		1624	37.4.3 Operation of the D/A Converter in Software Standby Mode, changed
		1624	37.4.4 Note on Entering Deep Software Standby Mode, changed
		39. Digital Power Controller (DPC)	
		1631 to 1652	39. Digital Power Controller (DPC), added
		41. Flash Memory	
		1655	Figure 41.2 Memory Area Configuration of ROM, changed
		42. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		1743	Table 42.1 Absolute Maximum Ratings, changed
		1746	Table 42.4 DC Characteristics (3), Note 7, deleted
		1747	Table 42.6 Permissible Power Consumption, added
		1767	42.3.7 Timing of PWM Delay Generation Circuit, added
		1767	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		1771	Figure 42.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		1772	Figure 42.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		1773	Figure 42.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		43. Electrical Characteristics [64- and 48-Pin Versions]	
		1788	Table 43.1 Absolute Maximum Ratings, changed
		1790	Table 43.3 DC Characteristics (2), Note 3, changed
		1791	Table 43.5 Permissible Power Consumption, added

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1. Overview		
		46 to 52	Table 1.1 Outline of Specifications, Note 1 changed	TN-RX*-A086A/E
		54 to 57	Table 1.3 List of Products, changed	TN-RX*-A086A/E
		60	Table 1.4 Pin Functions, changed	
		71 to 74	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed	
		74	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), Note 1 added	
		75 to 78	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed	
		79 to 82	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed	
		82	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), Note 1 added	
		3. Operating Modes [144-, 120-, 112- and 100-Pin Versions]		
		119	3.2.3 System Control Register 0 (SYSCR0), notes added	
		120	3.2.4 System Control Register 1 (SYSCR1), notes added	
		4. Operating Modes [64- and 48-Pin Versions]		
		126	4.2.2 System Control Register 0 (SYSCR0), notes added	
		127	4.2.3 System Control Register 1 (SYSCR1), notes added	
		129	Figure 4.1 Mode-Setting Pin Level and Operating Mode, changed	
		6. I/O Registers		
		134	(4) Notes on Sleep Mode and Mode Transition, added	TN-RX*-A140A/E
		135 to 190	Table 6.1 List of I/O Registers (Address Order), changed	TN-RX*-A086A/E, TN-RX*-A140A/E
		7. Resets		
		196	7.2.4 Software Reset Register (SWRR), notes added	
		9. Voltage Detection Circuit (LVDA)		
		211	Table 9.1 Voltage Detection Circuit Specifications, changed	
		214	9.2.1 Voltage Monitoring 1 Circuit Control Register 1 (LVD1CR1), notes added	
		214	9.2.2 Voltage Monitoring 1 Circuit Status Register (LVD1SR), notes added	
		215	9.2.3 Voltage Monitoring 2 Circuit Control Register 1 (LVD2CR1), notes added	
		215	9.2.4 Voltage Monitoring 2 Circuit Status Register (LVD2SR), notes added	
		216	9.2.5 Voltage Monitoring Circuit Control Register (LVCMPCR), notes added	
		217	9.2.6 Voltage Detection Level Select Register (LVDLVLR), notes added	
		218	9.2.7 Voltage Monitoring 1 Circuit Control Register 0 (LVD1CR0), notes added	
		220	9.2.8 Voltage Monitoring 2 Circuit Control Register 0 (LVD2CR0), notes added	
		10. Clock Generation Circuit		
		231	10.2.1 System Clock Control Register (SCKCR), notes added	
		233	10.2.2 System Clock Control Register 2 (SCKCR2), notes added	
		234	10.2.3 System Clock Control Register 3 (SCKCR3), notes added	
		235	10.2.4 PLL Control Register (PLLCR), notes added	
		236	10.2.5 PLL Control Register 2 (PLLCR2), notes added	
		237	10.2.6 External Bus Clock Control Register (BCKCR), notes added	
		238	10.2.7 Main Clock Oscillator Control Register (MOSCCR), notes added	
		239	10.2.8 Low-Speed On-Chip Oscillator Control Register (LOCOCR), notes added	
		240	10.2.9 IWDT-Dedicated On-Chip Oscillator Control Register (ILOCOCR), notes added	
		241	10.2.10 Oscillation Stop Detection Control Register (OSTDCR), notes added	
		242	10.2.11 Oscillation Stop Detection Status Register (OSTDSR), notes added	
		243	10.2.12 Main Clock Oscillator Forced Oscillation Control Register (MOFCR), notes added	
		12. Low Power Consumption		
		264	12.2.1 Standby Control Register (SBYCR), notes added	
		265	12.2.2 Module Stop Control Register A (MSTPCRA), notes added	
		266	12.2.3 Module Stop Control Register B (MSTPCRB), notes added and Note 2. changed	
		268	12.2.4 Module Stop Control Register C (MSTPCRC), notes added	
		269	12.2.5 Main Clock Oscillator Wait Control Register (MOSCWTCR), notes added	

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	270	12.2.6 PLL Wait Control Register (PLLWTCR), notes added	
		272	12.2.7 Deep Standby Control Register (DPSBYCR), notes added and DPSBY Bit (Deep Software Standby) description changed	
		273	12.2.8 Deep Standby Interrupt Enable Register 0 (DPSIER0), notes added	
		274	12.2.9 Deep Standby Interrupt Enable Register 2 (DPSIER2), notes added	
		275	12.2.10 Deep Standby Interrupt Flag Register 0 (DPSIFR0), notes added	
		276	12.2.11 Deep Standby Interrupt Flag Register 2 (DPSIFR2), notes added	
		277	12.2.12 Deep Standby Interrupt Edge Register 0 (DPSIEGR0), notes added	
		278	12.2.13 Deep Standby Interrupt Edge Register 2 (DPSIEGR2), notes added	
		279	12.3 Reducing Power Consumption by Switching Clock Signals, description changed	
		290	12.6.5 Input Buffer Control by DIRQnE Bit (n = 0 to 7), description changed	
		15. Interrupt controller (ICUb)		
		311	15.2.10 IRQ Pin Digital Filter Setting Register 0 (IRQFLTC0), description changed	
		317	15.2.16 NMI Pin Digital Filter Setting Register (NMIFLTC), description changed	
		344	15.6 Non-maskable Interrupt Operation, changed	
		347	15.8.2 Note on Using the MTU3 Interrupt, title changed	
		17. Memory-Protection Unit (MPU)		
		425	17.4.4 Processing in Response to Memory-Protection Errors, description changed	
		19. Data Transfer Controller (DTCa)		
		465	Figure 19.1 Block Diagram of DTC, changed	
		467	19.2.2 DTC Mode Register B (MRB), table changed	
		20. I/O Ports		
		494	20.1 Overview, description changed	
		501	Figure 20.7 I/O Port Configuration (1), changed	
		505	20.3.3 Port Input Data Register (PIDR), description changed	
		21. Multi-Function Pin Controller (MPC)		
		513 to 520	Table 21.1 Functions Assigned to Each Multiplexed Pin, changed	
		524	Table 21.6 Register Settings for Input/Output Pin Function in 144-Pin LQFP, changed	TN-RX*-A086A/E
		524	Table 21.9 Register Settings for Input/Output Pin Function in 64-Pin LQFP, changed	TN-RX*-A086A/E
		529	21.2.6 P4n Pin Function Control Registers (P4nPFS) (n = 0 to 7), changed	
		529	21.2.7 P5n Pin Function Control Registers (P5nPFS) (n = 0 to 7), changed	
		529	21.2.8 P6n Pin Function Control Registers (P6nPFS) (n = 0 to 5), changed	
		22. Multi-Function Timer Pulse Unit 3 (MTU3)		
		553 to 555	Table 22.2 MTU Functions, changed	
		563	22.2.2 Timer Mode Register 1 (TMDR1), BFA Bit (Buffer Operation A) description changed	
		583	Table 22.36 TIORU, TIORV, and TIORW (MTU5), Note 1 added	
		595	22.2.9 Timer Input Capture Control Register (TICCR) bit table, changed	
		600	22.2.14 Timer Synchronous Register TSYRA (TSYRB), title changed	
		605	22.2.17 Timer Output Master Enable Register (TOER), bit table and bit table Note 1 changed	TN-RX*-A086A/E
		608	Figure 22.3 Example of Output in Complementary PWM Mode, changed	
		615	22.2.27 Timer Buffer Transfer Set Registers (TBTERA and TBTERB), Note 1 changed	
		617	22.2.28 Timer Waveform Control Registers (TWCRA and TWCRB), description changed	
		619	22.2.29 Timer A/D Converter Start Request Control Register (TADCR) • TADCR(MTU4) bit table and Note 2, 4 changed	TN-RX*-A119A/E
		620	Table 22.48 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU4), changed	TN-RX*-A119A/E
		621	22.2.29 Timer A/D Converter Start Request Control Register (TADCR) • TADCR(MTU7) bit table and Note 2, 4 changed	TN-RX*-A119A/E
		622	Table 22.49 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU7), changed	TN-RX*-A119A/E
		625	22.2.33 Timer Interrupt Skipping Set Registers 1 (TITCR1A and TITCR1B), description changed	
		628	22.2.34 Timer Interrupt Skipping Counters 1 (TITCNT1A and TITCNT1B), description changed	
		648	Figure 22.21 Cascaded Operation Setting Procedure, changed	

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	652	22.3.5 PWM Modes, description changed	
		662	Figure 22.35 Phase Counting Mode Application Example, changed	
		664	Figure 22.36 Procedure for Selecting Reset-Synchronized PWM Mode, changed	
		665	Figure 22.37 Example of Reset-Synchronized PWM Mode Operation (When TOCR1A's OLSN = 1 and OLSP = 1 in MTU3 and MTU4), changed	
		669	Figure 22.38 Block Diagram of MTU3 and MTU4 in Complementary PWM Mode, changed	
		670	Figure 22.39 Example of Complementary PWM Mode Setting Procedure, changed	
		671	22.3.8 Complementary PWM Mode: (2) Outline of Complementary PWM Mode Operation, (b) Register Operation, description changed	
		677	22.3.8 Complementary PWM Mode: (2) Outline of Complementary PWM Mode Operation, (g) PWM Cycle Setting, description changed	
		679	22.3.8 Complementary PWM Mode: (2) Outline of Complementary PWM Mode Operation, (j) Method for Generating PWM Output in Complementary PWM Mode, description changed	TN-RX*-A099A/E
		682	Figure 22.47 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1), changed	TN-RX*-A099A/E
		683	Figure 22.48 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2), changed	TN-RX*-A099A/E
		683	Figure 22.49 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3), changed	TN-RX*-A099A/E
		684	Figure 22.50 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1), changed	TN-RX*-A099A/E
		684	Figure 22.51 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2), changed	TN-RX*-A099A/E
		685	Figure 22.52 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3), changed	TN-RX*-A099A/E
		685	Figure 22.53 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (4), changed	TN-RX*-A099A/E
		686	Figure 22.54 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (5), changed	TN-RX*-A099A/E
		705	Figure 22.81 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b), changed	TN-RX*-A099A/E
		706	Figure 22.82 Relationship between Bits T3AEN and T4VEN in TITCR1A and Buffer Transfer-Enabled Period, changed	TN-RX*-A099A/E
		708	Figure 22.83 Example of Procedure for Specifying A/D Converter Start Request Delaying Function, description changed and Note 2 changed, Note 4 added	TN-RX*-A119A/E
		709	Figure 22.84 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation	TN-RX*-A119A/E
		709	22.3.9 A/D Converter Start Request Delaying Function: (3) A/D converter Start Request Enabled Interval, added	TN-RX*-A119A/E
		710	22.3.9 A/D Converter Start Request Delaying Function: (4) Buffer Transfer description changed	TN-RX*-A119A/E
		711	22.3.9 A/D Converter Start Request Delaying Function: (5) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1, description changed	TN-RX*-A119A/E
		715	Figure 22.92 Example of Procedure for Specifying Counter Clearing for MTU6 and MTU7 by Flag Setting Sources, changed	
		723	22.4.1 Interrupt Sources and Priorities (1) Input Capture/Compare Match Interrupt, description changed	
		723	22.4.1 Interrupt Sources and Priorities (2) Overflow Interrupt, description changed	
		724	22.4.3 A/D Converter Activation (2) A/D Converter Activation by Compare Match between MTU0.TCNT and MTU0.TGRE, description changed	
		738	22.6.3 Note on Cycle Setting, description changed	
		749	22.6.17 Contention between Overflow/Underflow and Counter Clearing, description changed	
		754	22.6.26 Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode, added	TN-RX*-A119A/E

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	754	Figure 22.143 A/D Converter Start Request When 0 is Written to MTU4.TADCOBRA, added	TN-RX*-A119A/E
		754	Figure 22.144 A/D Converter Start Request When the Same Value as TCDR is Written to MTU4.TADCOBRA, added	TN-RX*-A119A/E
		23. Port Output Enable 3 (POE3)		
		784	Figure 23.1 POE3 Block Diagram, change	
		789	23.2.2 Input Level Control/Status Register 2 (ICSR2) PIF2 Bit (Port Interrupt Enable 1) changed	
		804	23.2.12 Port Output Enable Control Register 1 (POECR1) MTU0DZE Bit (MTU CH0D High-Impedance Enable), changed	
		807	23.2.14 Port Output Enable Control Register 3 (POECR3) GPT2ABZE Bit (GPT CH2AB High-Impedance Enable), changed	
		812	23.2.16 Port Output Enable Control Register 5 (POECR5) bit table, changed	
		814	23.2.17 Port Output Enable Control Register 6 (POECR6) bit table, changed	
		815	23.2.17 Port Output Enable Control Register 6 (POECR6) CMADDGPT23ZE Bit (GPT CH23 High-Impedance CFLAG Add), description changed	
		817	23.2.18 Port Output Enable Control Register 7 (POECR7), address changed	
		821 to 826	Table 23.4 Target Pins and Conditions for High-Impedance Control [144-, 120-, 112- and 100-Pin Versions], changed	
		827 to 829	Table 23.5 Target Pins and Conditions for High-Impedance Control [64- and 48-Pin Versions], changed	
		830	Figure 23.2 Target Pins and Conditions for High-Impedance Control, changed	
		833	23.3.6 Additional Functions for Controlling High-Impedance States, description changed	
		834	23.3.7 Release from High-Impedance State, description changed	
		834	Table 23.6 Interrupt Sources and Conditions, changed	
		24. General PWM Timer (GPT)		
		851	24.2.5 General PWM Timer Hardware Stop/Clear Source Select Register (GTHPSR), description changed	
		855	24.2.6 General PWM Timer Write-Protection Register (GTWP), description changed	
		859	24.2.9 General PWM Timer Buffer Operation Disable Register (GTBDR), bit table changed	
		870	24.2.18 General PWM Timer Interrupt Output Setting Register (GTINTAD) GTINTD Bit (GTCCRD Compare Match Interrupt Enable) and GTINTF Bit (GTCCRF Compare Match Interrupt Enable), description changed	
		872	24.2.19 General PWM Timer Control Register (GTCR), CCLR[1:0] bits description changed	TN-RX*-A098A/E
		874	24.2.20 General PWM Timer Buffer Enable Register (GTBER), PR[1:0] bits description changed	TN-RX*-A098A/E
		874	24.2.20 General PWM Timer Buffer Enable Register (GTBER), bit table changed	
		883	24.2.26 General PWM Timer Cycle Setting Register (GTPR), description changed	TN-RX*-A098A/E
		883	24.2.27 General PWM Timer Cycle Setting Buffer Register (GTPBR), description changed	
		908	24.3.2.1 GTPR Register Buffer Operation, description changed	TN-RX*-A098A/E
		909	Figure 24.14 Example of GTPR Buffer Operation (Saw Waves in Down-Count Operation), deleted	TN-RX*-A098A/E
		911	24.3.2.2 Buffer Operation for GTCCRA and GTCCRB (1) When GTCCRA or GTCCRB Functions as Output Compare Register, description changed	TN-RX*-A098A/E
		911	Figure 24.16 Example of GTCCRA and GTCCRB Buffer Operation (Output Compare, Saw Waves in Up-Count Operation, High Output at GTCCRA Compare Match, Low Output at Cycle End), changed	
		916	24.3.2.3 Buffer Operation for GTADTRA and GTADTRB, description changed	
		919	24.3.3 PWM Output Operating Mode, description changed	
		921	24.3.3 PWM Output Operating Mode (2) Saw-Wave One-Shot Pulse Mode, description changed	
		942	24.3.6.3 Hardware Clear Operation, description changed	
		949	24.3.7.2 Synchronized Start Operation (2) Phase Start by Software, description changed	

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	959	Figure 24.67 Example of Three-Phase Asymmetric Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting, changed	
		968	Figure 24.71 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Crests, Skipping Count: 2), changed	
		974	24.6 IWDTCLK Count Function, description changed	
		975	Figure 24.80 Example for Setting IWDTCLK Count Function Operation, changed	
		989	24.9.6 Notes on Delay Time Settings for PWM Delay Generation Circuit, description changed	
		989	Figure 24.95 Restriction on the Timing of GTDLYFA Register Settings, changed	
		28. USB 2.0 Host/Function Module (USBa)		
		1028 to 1133	term: interpolation->recovery changed	TN-RX*-A100A/E
		1028	Table 28.1 Specifications of USB, Note 1 added	TN-RX*-A100A/E
		1031	28.2.1 System Configuration Control Register (SYSCFG) DPRPU Bit (D+ Line Resistor Control), description changed	
		1032	28.2.1 System Configuration Control Register (SYSCFG) SCKE Bit (USB Clock Enable), description changed	
		1033	28.2.2 System Configuration Status Register 0 (SYSSTS0), bit table changed	
		1033	28.2.2 System Configuration Status Register 0 (SYSSTS0) OVCMON[1:0] Bits (External USB0_OVRCURA/USB0_OVRCURB Input Pin Monitor), description changed	
		1034	28.2.3 Device State Control Register 0 (DVSTCTR0), bit table changed, bit table Note 2 deleted	TN-RX*-A100A/E
		1035	28.2.3 Device State Control Register 0 (DVSTCTR0), RESUME bit description changed	TN-RX*-A100A/E
		1036	28.2.3 Device State Control Register 0 (DVSTCTR0), RWUPE bit description changed	
		1037	28.2.4 CFIFO Port Register (CFIFO) D0FIFO Port Register (D0FIFO) D1FIFO Port Register (D1FIFO), changed	TN-RX*-A100A/E
		-	Table 28.5 Endian Operation in 8-Bit Access, deleted	
		1043	28.2.6 CFIFO Port Control Register (CFIFOCTR) D0FIFO Port Control Register (D0FIFOCTR) D1FIFO Port Control Register (D1FIFOCTR) Note 1 changed, Note 2 deleted	TN-RX*-A100A/E
		1050	28.2.12 SOF Output Configuration Register (SOFCFG), bit map changed, Note 1, Note 2, Note 3, bit table changed TRNENSEL bit description deleted	TN-RX*-A100A/E
		1051	28.2.13 Interrupt Status Register 0 (INTSTS0), bit map and bit table changed	TN-RX*-A100A/E
		1052	28.2.13 Interrupt Status Register 0 (INTSTS0), BRDY Bit description changed	
		1052	28.2.13 Interrupt Status Register 0 (INTSTS0), BEMP Bit description changed	
		1057	28.2.15 BRDY Interrupt Status Register (BRDYSTS) address changed	
		1060	28.2.18 Frame Number Register (FRMNUM), Note 1 changed, CRCE bit description changed	TN-RX*-A100A/E
		1065	28.2.23 USB Request Index Register (USBINDX), WINDEX[15:0] Bits description changed	
		1069	28.2.27 DCP Control Register (DCPCTR), Note 1 changed Note 1 deleted	TN-RX*-A100A/E
		1076	28.2.30 Pipe Maximum Packet Size Register (PIPEMAXP), MXPS[8:0] bits description changed	TN-RX*-A100A/E
		1078	28.2.32 PIPEn Control Registers (PIPEnCTR) (n = 1 to 9), Note 1 changed	TN-RX*-A100A/E
		1088	28.2.35 Device Address n Configuration Registers (DEVADDn) (n = 0 to 5), bit table changed	TN-RX*-A100A/E
		1088	28.2.35 Device Address n Configuration Registers (DEVADDn) (n = 0 to 5), USBSPD[1:0] bits description changed	TN-RX*-A100A/E
		1089	28.3.1.2 Controller Function Selection, description changed	TN-RX*-A100A/E
		1099	Figure 28.7 Timing of BRDY Interrupt Generation, changed	TN-RX*-A100A/E
		1102	Figure 28.8 Timing of NRDY Interrupt Generation (When Function Controller Function is Selected), changed	TN-RX*-A100A/E
		1104	Figure 28.9 Timing of BEMP Interrupt Generation (When Function Controller Function is Selected), changed	TN-RX*-A100A/E
		1109	Table 28.13 Pipe Setting Items, changed	
		1118	28.3.5.4 DMA/DTC Transfers (D0FIFO and D1FIFO Ports) (1) Overview of DMA/DTC Transfers, description changed	

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1119	28.3.6.1 Control Transfers when Host Controller Function is Selected (1) Setup Stage, description changed	
		1120	28.3.6.2 Control Transfers when Function Controller Function is Selected (4) Control Transfer Auto Response Function, description changed	TN-RX*-A100A/E
		1121	28.3.8.1 Interval Counter during Interrupt Transfers when Host Controller Function is Selected (1) Counter Initialization, description changed	TN-RX*-A100A/E
		1122	28.3.9 Isochronous Transfers (PIPE1 and PIPE2), description changed	
		1124	28.3.9.3 Interval Counter, description changed	
		1124	(1) Counter Initialization when Function Controller Function is Selected, description changed	TN-RX*-A100A/E
		1125	(2) Interval Counting and Transfer Control when Host Controller Function is Selected, description changed	
		1125	Figure 28.12 Token Issuance when IITV[2:0] = 0, title changed	
		1125	Figure 28.13 Token Issuance when IITV[2:0] = 1, title changed	
		1126	28.3.9.3 Interval Counter: (3) Interval Counting and Transfer Control when Function Controller Function is Selected (a), description changed	
		1128	28.3.9.3 Interval Counter: (4) Setup of Data to be Transmitted using Isochronous Transfer when Function Controller Function is Selected, description changed	
		1129	28.3.9.3 Interval Counter: (5) Isochronous Transfer Transmission Buffer Flush when Function Controller Function is Selected, description changed	
		1130	Figure 28.18 Example of Interval Error Occurrence when the IITV[2:0] = 1, title and description changed	
		1131	28.3.10 SOF Recovery Function, description changed	TN-RX*-A100A/E
		1132	Table 28.23 Conditions for Generating a Transaction, changed	
		29. Serial Communications Interface (SCIc, SCId)		
		1134	Table 29.1 Specifications of SCIc, changed	
		1144	29.2.6 Serial Control Register (SCR) TEIE Bit (Transmit End Interrupt Enable), description changed	
		1148 to 1150	(1) Serial Communications Interface Mode (SMIF in SCMR = 0), changed	TN-RX*-A138A/E
		1152	29.2.8 Smart Card Mode Register (SCMR), SINV Bit description changed	
		1166	29.2.14 I^2C Mode Register 3 (SIMR3), IICSDAS[1:0] Bits description changed	
		1167	29.2.14 I^2C Mode Register 3 (SIMR3), IICSCLS[1:0] Bits description changed	
		1171	29.2.18 Control Register 0 (CR0), bit table changed	
		1172	29.2.20 Control Register 2 (CR2), address changed	
		1173	29.2.22 Port Control Register (PCR), bit table changed	
		1179	29.2.34 Timer Mode Register (TMR), address changed	
		1180	29.2.36 Timer Count Register (TCNT), address changed	
		1185	29.3.5 SCI Initialization (Asynchronous Mode), description changed	TN-RX*-A130B/E
		1207	29.6.5 Initialization of the SCI (Smart Card Interface Mode), description changed	
		1215	29.7.1 Generation of Start, Restart, and Stop Conditions, description changed	
		1220	Figure 29.47 Example of the Procedure for Master Transmission Operations in Simple I^2C Mode (with Transmission Interrupts and Reception Interrupts in Use), changed	
		1223	29.8 Operation in Simple SPI Mode, description changed	
		1225	Figure 29.51 Relation between Clock Signal and Transmit/Receive Data in Simple SPI Mode, changed	
		1239	29.9.7 Selectable Timing for Sampling Data Received through RXDX12, description changed	
		1250	29.12.11 Limitations on Simple SPI Mode, (1) Master Mode description changed	
		1251	29.12.14 Note in Relation to Transmit Enable Bit (TE), added	TN-RX*-A086A/E
		30. I^2C Bus Interface (RIIC)		
		1271	30.2.9 I^2C Bus Status Register 1 (ICSR1) HOA Flag description changed	TN-RX*-A141A/E
		1277	30.2.13 I^2C Bus Bit Rate Low-Level Register (ICBRL), description changed	
		1279	Table 30.5 Examples of ICBRH/ICBRL Settings for Transfer Rate, Note changed	
		1281	30.2.18 Timeout Internal Counter (TMOCNT), description changed	
		1299	30.5 Facility for Delaying SDA Output, description changed	
		1303	30.7.2 Detection of the General Call Address, description changed	TN-RX*-A096A/E
		1303	30.7.3 Device-ID Address Detection, description changed	TN-RX*-A096A/E

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1304	30.7.4 Host Address Detection, description changed	TN-RX*-A096A/E
		1322	30.15.2 Points to Note on Starting Transfer, description changed	
		31. CAN Module (CAN)		
		1334	31.2.6 Mailbox Register j (MBj) (j = 0 to 31) Data byte 0 - Data byte 7 bit table, Note 1 changed	TN-RX*-A095A/E
		1334	31.2.6 Mailbox Register j (MBj) (j = 0 to 31), description changed	
		1334	Table 31.4 CANi Mailbox Memory Mapping, CAN0 and CAN2 deleted	
		1334	Table 31.5 CAN Data Frame Configuration, changed	
		1346	31.2.11 Transmit FIFO Control Register (TFCR), TFE bit description changed	TN-RX*-A095A/E
		1364	Table 31.8 Operation in CAN Reset Mode and CAN Halt Mode, Note 2 added	TN-RX*-A086A/E
		1364	Table 31.8 Operation in CAN Reset Mode and CAN Halt Mode, Note 1 to Note 4 changed	TN-RX*-A086A/E
		1375	31.7.2 Transmission, description changed	
		32. Serial Peripheral Interface (RSPI)		
		1383	32.2.3 RSPI Pin Control Register (SPPCR), bit map and bit table SPOM bit (RSPI Output Pin Mode) added	TN-RX*-A126A/E
		1383	32.2.3 RSPI Pin Control Register (SPPCR), SPOM bit (RSPI Output Pin Mode) description, added	TN-RX*-A126A/E
		1384 to 1386	32.2.4 RSPI Status Register (SPSR), bit 7 and bit 5, changed	TN-RX*-A138A/E
		1385	32.2.4 RSPI Status Register (SPSR), MODF flag (Mode Fault Error Flag) description changed	
		1398	32.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7), SSLA[2:0] Bits description changed	
		1402	32.3.2 Controlling RSPI Pins, description changed	TN-RX*-A126A/E
		1402	Table 32.6 Relationship between Pin States and Bit Settings, changed	TN-RX*-A126A/E
		1402	Table 32.6 Relationship between Pin States and Bit Settings, Note 2 changed, Note 6 added	TN-RX*-A126A/E
		1430	Figure 32.30 Procedure for Determining the Form of Serial Transmission in Master Mode, description changed	
		1435	Figure 32.34 Example of Initialization Flowchart in Master Mode (SPI Operation), changed	TN-RX*-A094A/E, TN-RX*-A126A/E
		1436	(a) Transmit Processing Flow, changed	TN-RX*-A147A/E
		1440	Figure 32.38 Example of Initialization Flowchart in Slave Mode (SPI Operation), changed	TN-RX*-A126A/E
		1446	Figure 32.45 Example of Initialization Flowchart in Master Mode (Clock Synchronous Operation), changed	TN-RX*-A126A/E
		1448	Figure 32.46 Example of Initialization Flowchart in Slave Mode (Clock Synchronous Operation), changed	TN-RX*-A126A/E
		34. 12-Bit A/D Converter (S12ADB) [144-, 120-, 112- and 100-Pin Versions]		
		1460	Table 34.1 Specifications of 12-Bit A/D Converter, change	
		1487	34.2.12 A/D Group Scan Priority Control Register (ADGSPCR) PGS Bit (Group A Priority Control Setting), description changed	TN-RX*-A086A/E
		1487	34.2.12 A/D Group Scan Priority Control Register (ADGSPCR) GBRSCN Bit (Group B Restart Setting), description changed	
		1490	34.2.14 Comparator Operating-Mode Selection Register 1 (ADCMPMD1), bit table change	
		1495	34.2.18 A/D Programmable Gain Amplifier Register (ADPG), description changed	
		1496	34.2.19 Group Scan Priority Control Register (ADGSPMR), added	TN-RX*-A086A/E
		1509	Figure 34.11 Example of Extended Operation in Double-Trigger Mode (Doubling Selected for AN003, GTADTRA0N and GTADTRB0N Selected, Two Trigger Sources Occurred Simultaneously), changed	
		1517	34.3.4.4 Operation under Group-A Priority Control, description changed	
		1526	34.3.4.4 Operation under Group-A Priority Control Described below is an example of operation under group A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSCR.GBRP = 1). (9) changed	
		1527	34.3.5 Analog Input Sampling and Scan Conversion Time, description changed	
		1527	34.3.5 Analog Input Sampling and Scan Conversion Time, Note 1 changed	
		1535	34.5 A/D Conversion Accuracy Definitions, description changed	

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1536	Figure 34.32 Procedures for Clear Operation by Software through the ADCSR.ADST Bit, changed	
		35. 12-Bit A/D Converter (S12ADB) [64- and 48-Pin Versions]		
		1543 to 1544	Table 35.2 Functions of 12-Bit A/D Converter, changed	
		1553	35.2.4 A/D Channel Select Register A (ADANSA), ANSA[7:0] Bits description changed	
		1556	35.2.8 A/D Control Extended Register (ADCER), ADPRC Bits description changed	
		1559	Table 35.5 Selection of A/D Activation Sources by the TRSB[4:0] Bits, title changed	
		1561	Table 35.6 Selection of A/D Activation Sources by the TRSA[4:0] Bits, title changed	
		1577	Figure 35.7 Procedures for Clear Operation by Software through the ADCSR.ADST Bit, changed	TN-RX*-A117A/E
		36. 10-Bit A/D Converter (AD)		
		1583	Table 36.2 Functions of 10-bit A/D Converter, changed	
		1589	36.2.2 A/D Self-Diagnosis Data Register (ADRD) ADCER.ADPRC = 1, ADCER.ADRFMT = 0 (The settings are for flush-right data with 8-bit), bit map and bit table changed	
		1590	36.2.3 A/D Control Register (ADCSR), bit table changed	
		1603	36.2.11 A/D Sampling State Register n (ADSSTRn) (n = 0 to 7), address changed	
		1604	36.2.13 Digital Power Supply Control Circuit Output Setting Register (ADDP-CONR), description changed	
		1618	36.6.12 Notes on Using External Bus, description changed	
		39. Digital Power Supply Controller (DPC)		
		1634	Figure 39.1 DPC Block Diagram, changed	
		1636	39.2.2 Reference Value Setting Register (VOTARGETn) (n = 0 to 3), title changed	
		1645	39.3.1.5 Control Calculation Parameter Setting	
		1646	Figure 39.5 Shutdown at Overvoltage Output Error, changed	
		1646	39.3.2 Operation in Internal Reference Voltage Mode, description changed	
		1650	Figure 39.9 Simultaneous Enable Operations at 500 kHz of Switching Frequency with Four PWM Channels, description changed	
		1653	Figure 39.11 Simultaneous Operations at 500 kHz of Switching Frequencies with Two Channels, changed	
		41. Flash Memory		
		1663	41.2.3 Flash Access Status Register (FASTAT), description changed	
		1690	41.4.4.1 Mode Transitions (1) Switching to ROM Read Mode or ROM/E2 DataFlash Read Mode, description changed	
		1695	41.4.4.2 Programming and Erasure Procedures (3) Using the Peripheral Clock Notification Command, description changed	
		1729	41.8.7 Inquiry/Selection Command Wait (15) Boot Program Status Inquiry, changed	
		42. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]		
		1745	Table 42.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		1748	Table 42.4 DC Characteristics (3), changed	
		1749	Table 42.5 Permissible Output Currents, changed	
		1750	Table 42.6 Permissible Power Consumption (G version product only), title changed, notes added	TN-RX*-A086A/E
		1753	Table 42.9 Clock Timing, changed	TN-RX*-A097A/E
		1754	Figure 42.6 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		1754	Figure 42.6 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		1766	Table 42.16 Timing of On-Chip Peripheral Modules (1), changed	TN-RX*-A121A/E
		1767	Table 42.16 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A121A/E
		1768	Table 42.16 Timing of On-Chip Peripheral Modules (3), changed	TN-RX*-A121A/E
		1769	Table 42.16 Timing of On-Chip Peripheral Modules (4), changed	
		1771	Table 42.17 Timing of the PWM Delay Generation Circuit	TN-RX*-A086A/E
		1774	Figure 42.30 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), title and figure changed	

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1775	Figure 42.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0), title changed	
		1776	Figure 42.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1), title changed	
		1777	Figure 42.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), title changed	
		1778	Table 42.18 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics), Condition 1, 2 changed	TN-RX*-A086A/E
		1785	Table 42.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1), changed	
		43. Electrical Characteristics [64- and 48-Pin Versions]		
		1792	Table 43.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		1795	Table 43.5 Permissible Power Consumption (G version product only), title changed, note added	TN-RX*-A086A/E
		1796	Table 43.7 Clock Timing, changed	TN-RX*-A097A/E
		1797	Figure 43.3 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		1797	Figure 43.3 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		1803	Table 43.12 Timing of On-Chip Peripheral Modules (2), changed	
		1812	Table 43.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics, changed	
		Appendix 1. Port States in Each Processing Mode		
		1818 to 1821	Table 1.1 Port States in Each Processing State, changed	

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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