User's Manual

32

RH850/U2B Group

Resolver to Digital Converter

User's Manual: Hardware

Renesas microcontroller

RH850 Family

Renesas Electronics
www.renesas.com

Rev.1.20 Feb. 2025

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

Table of Contents

Section 49 Resolver to Digital Converter (RDC3AL/AS)

This section contains a generic description of the R/D (resolver-to-digital) converter 3AL/AS (RDC3AL/AS).

RDC3AL is R/D converter of successive-approximation-register analog-to-digital type. And RDC3AL works by using dedicated SAR-ADC for RDC3AL.

RDC3AS is R/D converter of delta-sigma analog-to-digital type. And RDC3AS works by cooperates with DSADC.

The first part of this section describes specific properties in RH850/U2B products, such as the numbers of units and register base addresses, etc. The remainder of the section describes the functions and registers of the RDC3AL/AS.

49.1 RDC3AL

49.1.1 Specifications of the R/D Converter (RDC3AL)

This digital tracking resolver-to-digital (R/D) converter is to take signals from a resolver (analog signals) and convert them to digital angle values with a resolution of up to 16 bits.

49.1.1.1 Overview

(1) Functional Overview

The R/D (resolver-to-digital) converter 3AL converts the analog value (angle information) indicating the rotor angle of the resolver into a 16-bit (at maximum) digital value. In addition to the function of converting the analog angle signal from the resolver into a digital angle signal, the RDC3AL provides excitation signal output function, sin, cos correction function, error detection function, selfdiagnosis function and other functions.

Table 49.1 lists the specifications for the RDC3AL.

Table 49.1 RDC3AL Specifications (1/2)

Function		Description
Tracking loop	Excitation signal source selection	Selects the excitation signal generated in the RDC3AL (RDC3ALnRSO, RDC3ALnCOM) or that input from outside.
	Required sensor selection	Selects VR resolver or DC resolver.
	Excitation component extraction	Uses the excitation components extracted from the resolver signal for R/D conversion.
	PI compensator bandwidth setting	Selects from six bandwidths (five fixed and one auto-adjusted).
	Forced gain control (AGCON)	Improves the tracking performance when the resolver angle deviates significantly from the R/D converted angle. In addition, the maximum and minimum values of PI compensator gain during AGC operation can be set.
	Maximum angular velocity setting	Sets a maximum angular velocity (resolution) in the range from 960,000 rpm (10 bits) to 15,000 rpm (16 bits).
	PHI angular velocity information reading	Reads the angular velocity from the PHI angle output register.
	Monitor	Reads angle information (°), angular velocity information (rpm), control variation values (%), and other signals directly from a register.
	Angle compare	When the angle that is set in the angle compare registers 0 to 2 and the R/D converted angle match, a compare match interrupt request is generated.
	Encoder pulse output	Outputs U-phase, V-phase, W-phase, A-phase, B-phase, and Zphase signals (4096 Edge/Revolution).
Sine and cosine correction function	ADC noise elimination	Discards the converted values of the RDC3ALnSINMNT and RDC3ALnCOSMNT signals acquired by AD conversion if they contain noise.
	Sine/cosine gain correction	Automatically detects the amplitudes of the sine and cosine signals by comparing them and corrects them.
	Sine/cosine common offset correction	Automatically detects an offset of the common levels of the sine and cosine signals input from the original common level and corrects them.
	Sine/cosine phase correction	Automatically detects the phase deviations of the excitation components of the sine and cosine signals to be input and corrects them.
	Sine/cosine angle correction	Inputs the value for correcting the sine and cosine angles to the SIN-ROM and COS-ROM tables. This function handles the mounting of the resolver at an angle toward the motor shaft by correcting the resulting orthogonality errors of the sine and cosine signals from the resolver.
Excitation signal output	Excitation signal output function (RDC3ALnRSO, RDC3ALnCOM)	Generates the excitation signal with the voltage buffer. Outputs the sine-wave voltage signal generated in the 7-bit D/A converter through the RDC3ALnRSO pin. Voltage amplitude (Vpp) is 2 V, which can be changed with the register setting. Outputs common voltage, which is AFCVCC divided by 2, from the RDC3ALnCOM pin.
	Automatic amplitude adjustment	Automatically adjusts the amplitude of the input monitor signals (RDC3ALnSINMNT, RDC3ALnCOSMNT) into appropriate values. Targets to be adjusted: Input gain resistance and excitation signal output amplitudes.

Table 49.1 RDC3AL Specifications (2/2)

Function		Description
Error detection	Error detection	Detects resolver signal error, resolver signal disconnect error, R/D conversion error, two paths comparison conversion error, resolver signal power/ground short error, sum-of-squares amplitude error.
Self-diagnosis	Built-in self-test	ADBIST (checks if A/D conversions are successful) Angle conversion BIST (0, 45, 270°) Error detection BIST (resolver signal error, resolver signal disconnect error, conversion error, power/ground short error, sum-of-squares amplitude error.
	ADC software BIST	A software BIST used to determine the result of A/D conversion by the CPU whose DAC code has been written to the register. Diagnosis of all 4096 codes is possible.
Others	Automatic ROM Table correction	The conversion accuracy is measured by the BIST function, and the measured error is automatically corrected with ROM table.
	Excitation timer (ET)	Measures period of excitation signal Generates event signals (AD trigger, DMA request).
	PGA inversion	In angle conversion using the ADC, this function inverts the signals output from the PGA (input amplifier) with the common potential as a center depending on their angles to reduce angle conversion errors.
Interrupts		Compare match interrupts 0 to 2 Z-phase interrupt RDC error interrupt Excitation timer interrupt BIST completion interrupt

49.1.1.2 Connection Block Diagram

Figure 49.1 is a block diagram of the entire RDC3AL module.

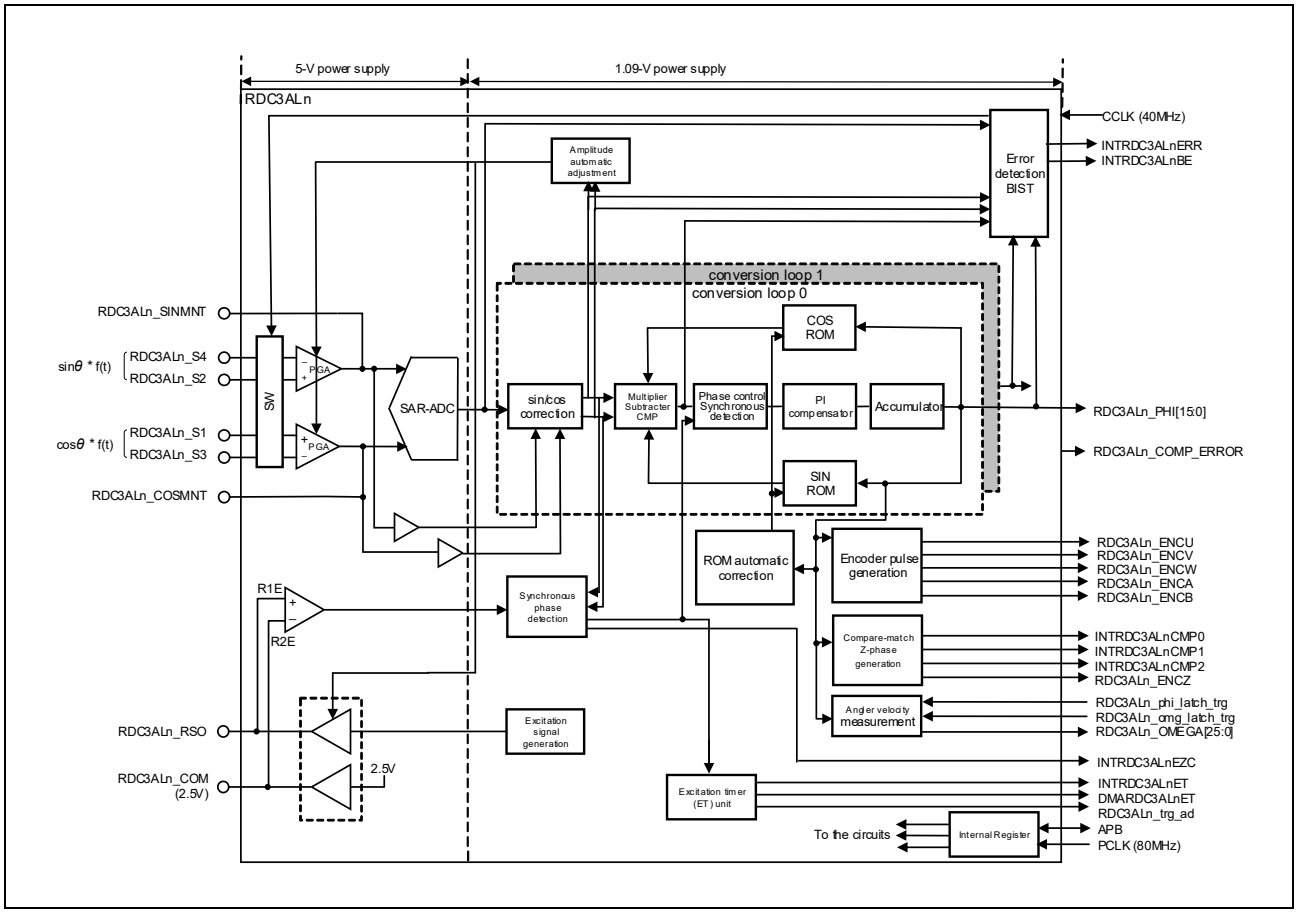


Figure 49.1 Connection Block Diagram of the R/D Converter (RDC3AL)

Note: n=0,1
f(t): excitation signal
RDC3ALnS1 to RDC3ALnS4 : resolver signals
SIN ROM: Sine wave ROM
COS ROM: Cosine wave ROM
RDC3ALnSINMNT,RDC3ALnCOSMNT: Monitor signals output from the input amplifier(PGA)

49.1.1.3 Operating Principle

The following describes the operating principles of the RDC3AL module. This R/D converter module uses the tracking method to convert analog resolver signals to digital signals (R/D conversion). The tracking loop runs at 20 MHz. When the excitation signal f(t) is input to the excitation coil, f(t) * sinθ and f(t) * cosθ are output from the resolver according to the angle (θ) of the resolver rotor. These signals are input to the RDC3ALnS2-RDC3ALnS4 and RDC3ALnS1-RDC3ALnS3 pins, respectively.

These signals are amplified and then input to the multiplier. At the same time, cos ϕ (or sin ϕ) is generated by passing the accumulator output through COS ROM (or SIN ROM) and is fed back to the corresponding multiplier. Then, the subtraction is performed on the outputs from both multipliers.

f(t) • (sin θ • cos ϕ - cos θ • sin ϕ)

= f(t) • sin (θ - ϕ)

≈ f(t) • (θ - ϕ)

The result is converted to 1-bit digital value by the comparator (CMP) and then passed to the next block. The excitation component f(t) is removed in the synchronous detection circuit to obtain the control variation ε = θ - ϕ. The negative feedback control over the entire analog and digital circuits provides feedback so that the control variation becomes zero. When θ = ϕ, the analog angle information from the resolver has been converted to digital angle ϕ (16-bit wide). **Figure 49.2** describes the PI compensator and accumulator.

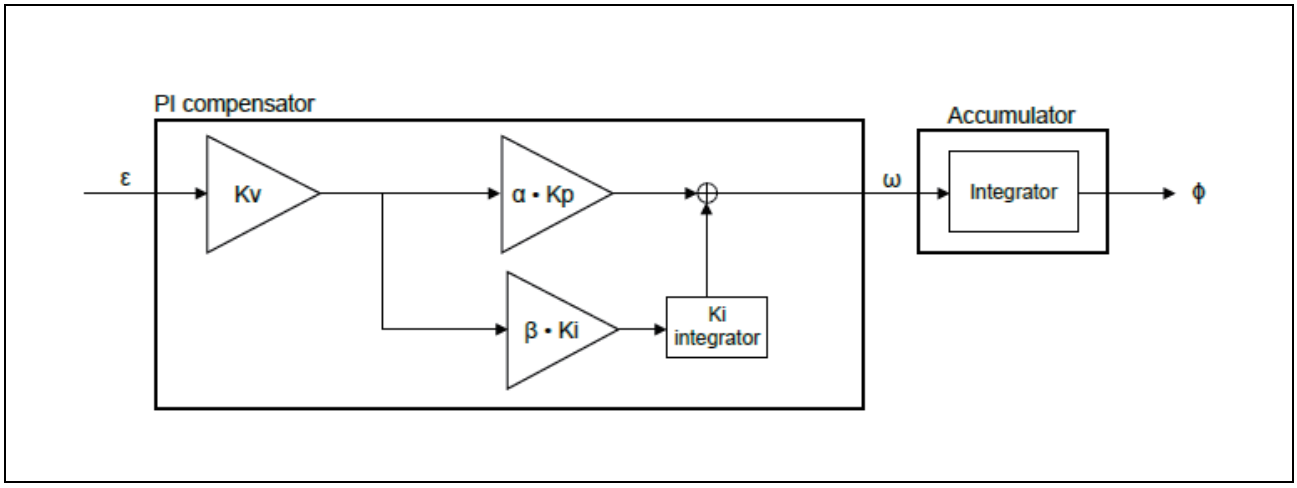


Figure 49.2 PI Compensator and Accumulator

The PI compensator converts the control variation according to the following formula, and passes the result to the accumulator circuit

ω = (α • Kp + (β • Ki)/(s • T)) • Kv • ε

Kv, Kp, Ki: control coefficients that can be set in a register

α, β: fixed values

s: Laplace variable

T: Integration time constant

ω: PI compensator output, angular velocity information

The accumulator circuit calculates the angle ϕ based on the angular velocity information ω.

49.1.2 RDC Register Specifications

49.1.2.1 List of Register Addresses

Table 49.2 List of RDC Register Addresses

Module Name	Register Name	Symbol	Address	Access Size	Access Protection	
					PGB	Other
RDC3ALn	RDC Stop register	RDC3ALnRDSTP	<RDC3ALn_base>+0000_H	8, 16, 32	*1	—
RDC3ALn	Control gain select register 0	RDC3ALnPI0	<RDC3ALn_base>+0004_H	8, 16, 32	*1	—
RDC3ALn	Control gain select register 1	RDC3ALnPI1	<RDC3ALn_base>+0008_H	8, 16, 32	*1	—
RDC3ALn	PHI compare setting register 0	RDC3ALnPHICP0	<RDC3ALn_base>+$000C_H$	8, 16, 32	*1	—
RDC3ALn	PHI compare setting register 1	RDC3ALnPHICP1	<RDC3ALn_base>+0010_H	8, 16, 32	*1	—
RDC3ALn	PHI compare setting register 2	RDC3ALnPHICP2	<RDC3ALn_base>+0014_H	8, 16, 32	*1	—
RDC3ALn	Sine/cosine angle correction register	RDC3ALnSCCOR0	<RDC3ALn_base>+0018H	8, 16, 32	*1	—
RDC3ALn	Sine/cosine correction register 1	RDC3ALnSCCOR1	<RDC3ALn_base>+$001C_H$	8, 16, 32	*1	—
RDC3ALn	Sine/cosine correction register 2	RDC3ALnSCCOR2	<RDC3ALn_base>+0020_H	8, 16, 32	*1	—
RDC3ALn	Sine/cosine correction register 3	RDC3ALnSCCOR3	<RDC3ALn_base>+0024_H	8, 16, 32	*1	—
RDC3ALn	Automatic amplitude adjustment register 0	RDC3ALnATMNT0	<RDC3ALn_base>+0028_H	8, 16, 32	*1	—
RDC3ALn	Automatic amplitude adjustment register 1	RDC3ALnATMNT1	<RDC3ALn_base>+$002C_H$	8, 16, 32	*1	—
RDC3ALn	Error detection register 0	RDC3ALnDIAG0	<RDC3ALn_base>+0030_H	8, 16, 32	*1	—
RDC3ALn	Error detection register 1	RDC3ALnDIAG1	<RDC3ALn_base>+0034_H	8, 16, 32	*1	—
RDC3ALn	Error detection register 2	RDC3ALnDIAG2	<RDC3ALn_base>+0038_H	8, 16, 32	*1	—
RDC3ALn	Error detection output register 0	RDC3ALnDGOUT0	<RDC3ALn_base>+$003C_H$	8, 16, 32	*1	—
RDC3ALn	Error detection output register 1	RDC3ALnDGOUT1	<RDC3ALn_base>+0040_H	8, 16, 32	*1	—
RDC3ALn	BIST register 0	RDC3ALnBIST0	<RDC3ALn_base>+0044_H	8, 16, 32	*1	—
RDC3ALn	BIST register 1	RDC3ALnBIST1	<RDC3ALn_base>+0048_H	8, 16, 32	*1	—
RDC3ALn	Excitation setting register	RDC3ALnREF	<RDC3ALn_base>+$004C_H$	8, 16, 32	*1	—
RDC3ALn	Encoder register 0	RDC3ALnENC0	<RDC3ALn_base>+0050_H	8, 16, 32	*1	—
RDC3ALn	Encoder register 1	RDC3ALnENC1	<RDC3ALn_base>+0054_H	8, 16, 32	*1	—
RDC3ALn	Encoder register 2	RDC3ALnENC2	<RDC3ALn_base>+0058_H	8, 16, 32	*1	—
RDC3ALn	Angular velocity register	RDC3ALnOMG	<RDC3ALn_base>+$005C_H$	8, 16, 32	*1	—
RDC3ALn	MNT signal register	RDC3ALnETC	<RDC3ALn_base>+0060_H	8, 16, 32	*1	—
RDC3ALn	Test bus register	RDC3ALnTBUS	<RDC3ALn_base>+0064_H	8, 16, 32	*1	—
RDC3ALn	ET control register	RDC3ALnETEN	<RDC3ALn_base>+$006C_H$	8, 16, 32	*1	—
RDC3ALn	ET capture register	RDC3ALnETCAP	<RDC3ALn_base>+0070_H	8, 16, 32	*1	—
RDC3ALn	ET zero-crossing counter register	RDC3ALnETMCNT	<RDC3ALn_base>+0074_H	8, 16, 32	*1	—
RDC3ALn	Digital operation register 0	RDC3ALnDCUR0	<RDC3ALn_base>+$007C_H$	8, 16, 32	*1	—
RDC3ALn	12-bit SAR-ADC digital circuit block setting register 0	RDC3ALnADSTD0	<RDC3ALn_base>+$00A8_H$	8, 16, 32	*1	—
RDC3ALn	12-bit SAR-ADC digital circuit block setting register 1	RDC3ALnADSTD1	<RDC3ALn_base>+$00AC_H$	8, 16, 32	*1	—
RDC3ALn	Error detection register 3	RDC3ALnDIAG3	<RDC3ALn_base>+$00B0_H$	8, 16, 32	*1	—
RDC3ALn	Error detection register 4	RDC3ALnDIAG4	<RDC3ALn_base>+$00B4_H$	8, 16, 32	*1	—
RDC3ALn	Automatic ROM Table correction register 1	RDC3ALnROMCOR1	<RDC3ALn_base>+$00BC_H$	8, 16, 32	*1	—

Note 1. n = 0: PBG40#5
n = 1: PBG30#4

49.1.2.2 Register Specifications

The detailed register specifications of the RDC are given below.

The addresses and bits which are shown above the register tables are those when access is in 32-bit units.

(1) RDC Stop Register (RDC3ALnRDSTP)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0000_H

Value after reset: $0000\ 0001_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	PGAX1	—	—	—	MNTC	—	—	—	—	—	—	—	ANSTP
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Table 49.3 RDC3ALnRDSTP Register Contents

Bit Position	Bit Name	Function
31 to 13	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
12	PGAX1	PGA Gain X1 Setting This bit can be used to set a PGA gain of 1x. 0: This is the setting for normal gain. The gain is determined by the externally connected RIN resistor plus an internal RE and RF resistance. 1: The PGA gain is set to one(1x). The gain may still vary with the setting for the RF resistance.
11 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	MNTC	Sinmnt/Cosmnt External Pin Setting The sinmnt and cosmnt external pins are set as follows. 0: The external output pins for sinmnt and cosmnt are left open-circuit. 1: The sinmnt and cosmnt signals are output through the external output pins.
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	ANSTP	R/D Converter Stop 0: Analog circuits are running. 1: All the power supply circuits running at 5V enter the following state. – All of them are disabled. – All of the pins (SINMNT, COSMNT, S1, S2, S3, S4, RSO, COM) are in the highimpedance state.

(2) Control Gain Select Register 0 (RDC3ALnPI0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0004_H

Value after reset: $0002\ 0010_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	KVMS[1:0]		DVW[1:0]		—	KPF	KPS[1:0]		—	KIS[2:0]			—	DEVCK[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LKVS[3:0]				HKVS[3:0]				—	—	—	BWCS	—	LPGS[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Table 49.4 RDC3ALnPI0 Register Contents (1/3)

Bit Position	Bit Name	Function
31, 30	KVMS[1:0]	Kv Gain Method Select Selects the Kv gain method. b31 b30 0 0: 1-step-shifted 12-level AGC (default) 0 1: 1-step-shifted 7-level AGC 1 0: 1-step-shifted 2-level AGC 1 1: Fixed Kv
29, 28	DVW[1:0]	ERR Deviation Weighting Selects weighting of ERR deviation. b29 b28 0 0: ×1 (default) 0 1: ×3 1 0: ×5 1 1: ×7
27	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
26	KPF	Kp Gain Quadruple Selects whether or not to quadruple the gain on the Kp side of the PI compensator.*2 0: Kp gain is not quadrupled. (×1) 1: Kp gain is quadrupled.
25, 24	KPS[1:0]	Kp Gain Select Selects the Kp gain in the PI compensator*2 b25 b24 0 0: ×1 (default) 0 1: ×0.25 1 0: ×0.5 1 1: ×2
23	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 49.4 RDC3ALnPI0 Register Contents (2/3)

Bit Position	Bit Name	Function
22 to 20	KIS[2:0]	Ki Gain Select Sets the Ki gain in the PI compensator. b22 b21 b20 0 0 0: ×1 (default) 0 0 1: ×0.125 0 1 0: ×0.25 0 1 1: ×0.5 1 0 0: ×2 1 0 1: ×4 1 1 0: ×8 1 1 1: ×16
19	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
18 to 16	DEVCK[2:0]	Control Variation Determination Clock Select*3 Selects the clock period used for determining the control variation. b18 b17 b16 0 0 0: 50 µs*1 clock period 0 0 1: 100 µs*1 clock period 0 1 0: 200 µs*1 clock period (default) 0 1 1: 25 µs*1 clock period 1 0 0: 400 µs*1 clock period 1 0 1: 800 µs*1 clock period 1 1 0: 50 µs*1 clock period 1 1 1: 50 µs*1 clock period
15 to 12	LKVS[3:0]	Low Kv Gain Select Sets the gain in the lower Kv side when the fixed Kv method or 2-level AGC method is selected.*4 b15 b14 b13 b12 0 0 0 0: ×1 (default) 0 0 0 1: ×0.0625 0 0 1 0: ×0.125 0 0 1 1: ×0.25 0 1 0 0: ×0.5 0 1 0 1: ×1 0 1 1 0: ×2 0 1 1 1: ×4 1 0 0 0: ×8 1 0 0 1: ×16 1 0 1 0: ×32 1 0 1 1: ×64 1 1 0 0: ×128 1 1 0 1: ×1 1 1 1 0: ×1 1 1 1 1: ×1
11 to 8	HKVS[3:0]	High Kv Gain Select Sets the gain in the higher Kv side when the fixed Kv method or 2-level AGC method is selected.*4 b11 b10 b9 b8 0 0 0 0: ×32 (default) 0 0 0 1: ×0.0625 0 0 1 0: ×0.125 0 0 1 1: ×0.25 0 1 0 0: ×0.5 0 1 0 1: ×1 0 1 1 0: ×2 0 1 1 1: ×4 1 0 0 0: ×8 1 0 0 1: ×16 1 0 1 0: ×32 1 0 1 1: ×64 1 1 0 0: ×128 1 1 0 1: ×32 1 1 1 0: ×32 1 1 1 1: ×32

Table 49.4 RDC3ALnPI0 Register Contents (3/3)

Bit Position	Bit Name	Function
7 to 5	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
4	BWCS	Bandwidth Setting Selects the PI compensator setting method. 0: Sets the coefficients by using the RDC3ALnPI0 register. 1: Using the LPGS[2:0] bits in this register (see the description in the LPGS[2:0] for the set value.)
3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2 to 0	LPGS[2:0]	Loop Gain Select By setting the BWCS bit in this register to 1, the LPGS[2:0] bits are enabled and the PI compensator can be set by using them. See **Table 49.10**.

Note 1. The timing value is when the CCLK is running at 40 MHz.

Note 2. The combinations of the settings of the DVW[1:0], KPS[1:0], KPF, and HKVS[3:0] bits in the RDC3ALnPI0 register listed in **Table 49.5** and **Table 49.6** are prohibited. In the combinations listed in these tables, the P component in the PI compensator overflows, resulting in an unexpected value if the Kv gain is large.

Note 3. Set the control variation determination clock period to be longer than the excitation signal period currently used. For example, when a 10 kHz (100 µs period) excitation signal is used, set the control variation determination clock period to 100, 200, 400 or 800 µs. Do not select 50 or 25 µs. If the angle conversion operation is unstable, it may be stabilized by setting these bits to a longer time setting.

Note 4. Set HKVS[3:0] gain to be larger than LKVS[3:0] gain.

Table 49.5 Prohibited Combinations of DVW[1:0], KPS[1:0], and KPF When KVMS[1:0] = 00 or 01 (in the case of the 12- or 7- level AGC)

DVW[1:0]	KPS[1:0]	KPF
00 (×1)	11 (×2)	1 (×4)
01 (×3)	11 (×2)	1 (×4)
01 (×3)	00 (×1)	1 (×4)
10 (×5)	11 (×2)	1 (×4)
10 (×5)	11 (×2)	0 (×1)
10 (×5)	00 (×1)	1 (×4)
10 (×5)	10 (×0.5)	1 (×4)
11 (×7)	11 (×2)	1 (×4)
11 (×7)	11 (×2)	0 (×1)
11 (×7)	00 (×1)	1 (×4)
11 (×7)	10 (×0.5)	1 (×4)

Table 49.6 Prohibited Combinations of DVW[1:0], KPS[1:0], KPF, and HKVS[3:0] When KVMS[1:0] = 10 or 11 (in the case of 2-level AGC or fixed Kv) (1/2)

DVW[1:0]	KPS[1:0]	KPF	HKVS[3:0]
00 (×1)	11 (×2)	1 (×4)	1100 (×128)
01 (×3)	11 (×2)	1 (×4)	1100 (×128)
01 (×3)	11 (×2)	1 (×4)	1011 (×64)
01 (×3)	00 (×1)	1 (×4)	1100 (×128)
10 (×5)	11 (×2)	1 (×4)	1100 (×128)
10 (×5)	11 (×2)	1 (×4)	1011 (×64)
10 (×5)	11 (×2)	1 (×4)	1010 (×32)
10 (×5)	11 (×2)	0 (×1)	1100 (×128)
10 (×5)	00 (×1)	1 (×4)	1100 (×128)
10 (×5)	00 (×1)	1 (×4)	1011 (×64)

Table 49.6 Prohibited Combinations of DVW[1:0], KPS[1:0], KPF, and HKVS[3:0] When KVMS[1:0] = 10 or 11 (in the case of 2-level AGC or fixed Kv) (2/2)

DVW[1:0]	KPS[1:0]	KPF	HKVS[3:0]
10 (×5)	10 (×0.5)	1 (×4)	1100 (×128)
11 (×7)	11 (×2)	1 (×4)	1100 (×128)
11 (×7)	11 (×2)	1 (×4)	1011 (×64)
11 (×7)	11 (×2)	1 (×4)	1010 (×32)
11 (×7)	11 (×2)	0 (×1)	1100 (×128)
11 (×7)	00 (×1)	1 (×4)	1100 (×128)
11 (×7)	00 (×1)	1 (×4)	1011 (×64)
11 (×7)	10 (×0.5)	1 (×4)	1100 (×128)

[Kv Gain Method Selection Bits]

These bits select the Kv gain method in the PI compensator. When the AGC (Auto Gain Control) method is selected, the Kv gain is automatically selected according to the amount of control variation. It is recommended to use the value after reset (12-level AGC method).

- 12-level AGC method (the default setting)

Table 49.7 lists the control variation amount and the value of the selected Kv gain for the 12-level AGC. The control variation amount indicates a bias of control variation ε (High or Low) within the determination clock period. With regard to the resolver angle signal θ and the R/D converter output angle signal ϕ, the High and the Low appear in equal proportions if θ and ϕ are equal. In such a case, the control variation amount is ± 0%. If ϕ is completely behind θ, the ε always becomes high. In this case, the control variation amount is +100%. If ϕ is completely ahead of θ, ε always becomes Low. In this case, the control variation amount is -100%. The determination clock period can be selected by the DEVCK[2:0] bits.

The HKVLM[3:0] bits and LKVLM[3:0] bits can be used to set the upper and lower limits on the Kv gain to be selected during AGC operation. However, in the AGCON state, the Kv gain shifts to the initial value (large gain) once, and then the limit value is applied after it falls below the high gain limit value specified by the HKVLM [3: 0] bits.

Table 49.7 Amounts of Control Deviation and Kv Gain Values in the Case of the 12-Level AGC (1/2)

Amount of Control Deviation	Kv Gain
After release from the reset	×128
-100% to -76.8%, +76.8% to +100%	×64
-76.8% to -64.0%, +64.0% to +76.8%	×32
-64.0% to -57.6%, +57.6% to +64.0%	×16
-57.6% to -51.2%, +51.2% to +57.6%	×8
-51.2% to -44.8%, +44.8% to +51.2%	×4
-44.8% to -38.4%, +38.4% to +44.8%	×2
-38.4% to -32.0%, +32.0% to +38.4%	×1
-32.0% to -25.6%, +25.6% to +32.0%	×0.5

Table 49.7 Amounts of Control Deviation and Kv Gain Values in the Case of the 12-Level AGC (2/2)

Amount of Control Deviation	Kv Gain
-25.6% to -19.2%, +19.2% to +25.6%	×0.25
-19.2% to -12.8%, +12.8% to +19.2%	×0.125
-12.8% to +12.8%	×0.0625

If the Kv gain falls below ×128 after release from the reset state, the Kv returns to ×128 on either of the following conditions:

1. The KIRST bit is set to 1 when the AGDS bit is 0 (Ki reset).
2. Recovery from the resolver signal error state when the AGDS bit is 0

The Kv gain does not return to ×128 on the above conditions when the AGDS bit is 1.

- 7-level AGC method

Table 49.8 lists the control variation amount and the value of the selected Kv gain for the 7-level AGC.

Table 49.8 Control Variation Amount and Kv Gain for 7-Level AGC

Control Variation Amount	Kv Gain
After release from a reset	×128
-100% to -76.8%, +76.8% to +100%	×64
-76.8% to -51.2%, +51.2% to +76.8%	×16
-51.2% to -38.4%, +38.4% to +51.2%	×4
-38.4% to -25.6%, +25.6% to +38.4%	×1
-25.6% to -12.8%, +12.8% to +25.6%	×0.25
-12.8% to +12.8%	×0.0625

If the Kv gain falls below ×128 after release from the reset state, the Kv returns to ×128 on either of the following conditions:

1. The KIRST bit is set to 1 when the AGDS bit is 0 (Ki reset)
2. Recovery from the resolver signal error state when the AGDS bit is 0.

The Kv gain does not return to ×128 on the above conditions when the AGDS bit is 1.

The HKVLM[3:0] bits and LKVLM[3:0] bits can be used to set the upper and lower limits on the selected Kv gain during AGC operation. However, in the AGCON state, the Kv gain shifts to the initial value (large gain) once, and then the limit value is applied after it falls below the high gain limit value specified by the HKVLM [3: 0] bits.

- 2-level AGC method

Table 49.9 lists the control variation amount and the value of the selected Kv gain for the 2-level AGC. The low and high gains can be set using bits LKVS[3:0] and HKVS[3:0], respectively.

Table 49.9 Control Variation Amount and Kv Gain for 2-Level AGC

Control Variation Amount	Kv Gain
-100% to -76.8%, +76.8% to +100%	Makes transition to the high Kv gain
-76.8% to -25.6%, +25.6% to +76.8%	Kv gain maintained (no transition)
-25.6% to +25.6%	Makes transition to the low Kv gain

If the Kv gain falls below ×128 after release from the reset state, the Kv returns to ×128 on either of the following conditions:

1. The KIRST bit is set to 1 when the AGDS bit is 0 (Ki reset).
2. Recovery from the resolver signal error state when the AGDS bit is 0.

The Kv gain does not return to ×128 on the above conditions when the AGDS bit is 1.

- Fixed Kv method

If the fixed Kv method is selected, the module operates with the low Kv gain irrespective of the control variation amount. The module, however, makes a transition to the high Kv gain only when an error is detected and then the error signal makes a transition to 0 (recovery from the error). After that, the module makes a transition to the low Kv gain side when the absolute value of the control variation amount falls below 25.6%.

- Control Variation Amount Monitoring

The control variation amount can be read from DATA[7:0] bits in the RDC3ALnTBUS register by setting DATSEL[6:0] bits in the RDC3ALnTBUS register to $2F_H$. Values read are expressed as two's complements. The control variation is ± 0% under the ideal condition where the resolver input angle exactly matches the phi digital angle output ($\theta = \phi$).

Table 49.10 Relationship between the Bits of the RDC3ALnTBUS Register and Control Variation Values (%)

Bit	Control Deviation Value (%)
b7	Sign (0: +, 1: –)
b6	50
b5	25
b4	12.5
b3	6.25
b2	3.13
b1	1.56
b0	0.78

For example, If the result of reading the control deviation value is 07_H, the control deviation value is +5.47%.

[Loop Gain Selection Bits]

Table 49.11 shows the relation between the combination of the LPGS[2:0] bits and the PI compensator settings when the BWCS bit is 1.

Table 49.11 LPGS[2:0] and Corresponding Settings in the PI Compensator

BWCS	LPGS[2:0]			PI Compensator Settings
	b2	b1	b0	Bandwidth
0	X	X	X	Set by the RDC3ALnPI0 register
1	0	0	0	800 Hz
1	0	0	1	Setting prohibited
1	0	1	0	Setting prohibited
1	0	1	1	1500 Hz
1	1	0	0	1000 Hz
1	1	0	1	500 Hz
1	1	1	0	200 Hz
1	1	1	1	Automatic adjustment

Note: The default setting is b2:b0 = 000 which sets the bandwidth as 800 Hz.

(3) Control Gain Select Register 1 (RDC3ALnPI1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0008_H

Value after reset: $0001\ 1B01_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	SAGD	—	—	—	AGCD	AGST[3:0]				—	—	—	AGDS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HKVLM[3:0]				LKVLM[3:0]				—		—		—	MAXV[2:0]		
Value after reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Table 49.12 RDC3ALnPI1 Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
28	SAGD	Short-Period BIST Recovery AGCON Disable This bit controls whether the R/D converter makes a transition to the AGCON state on completion of a short-period BIST and power/ground short error detection. 0: The AGCON function is used. 1: The AGCON function is not used
27 to 25	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
24	AGCD	Selects whether or not to use the AGCON function.*1 0: The AGCON function is used. 1: The AGCON function is not used.
23 to 20	AGST[3:0]	Short-Period BIST Recovery Initial AGC Gain Sets the initial value for the Kv gain on transitions to the AGCON state after completion of a short-period BIST and power/ground short error detection. b23 b22 b21 b20 Initial Kv gain 0 0 0 0 ×4 0 0 0 1 ×0.0625 0 0 1 0 ×0.125 0 0 1 1 ×0.25 0 1 0 0 ×0.5 0 1 0 1 ×1 0 1 1 0 ×2 0 1 1 1 ×4 1 0 0 0 ×8 1 0 0 1 ×16 1 0 1 0 ×32 1 0 1 1 ×64 1 1 0 0 ×128 1 1 0 1 ×4 1 1 1 0 ×4 1 1 1 1 ×4
19 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 49.12 RDC3ALnPI1 Register Contents (2/2)

Bit Position	Bit Name	Function
16	AGDS	AGC Kv High Gain Transition Restriction Restricts the AGC Kv gain from going high. 0: The Kv goes high on recovery from resolver signal error or after a Ki reset. 12-level AGC is selected: Kv is fixed to ×128 7-level AGC is selected: Kv is fixed to ×128 2-level AGC is selected: Kv is fixed to the higher side 1: The Kv does not go high on recovery from resolver signal error or after a Ki reset.
15 to 12	HKVLM[3:0]	AGC High Gain Limit Setting These bits set the limit on the higher gain side when the 12-level AGC or 7-level AGC is used.*2 b15 b14 b13 b12 High gain limit value 0 0 0 0 X64 (setting prohibited) 0 0 0 1 X64 (7 levels can be set) 0 0 1 0 X32 0 0 1 1 X16 (7 levels can be set) 0 1 0 0 X8 0 1 0 1 X4 (7 levels can be set) 0 1 1 0 X2 0 1 1 1 X1 (7 levels can be set) 1 0 0 0 X0.5 1 0 0 1 X0.25 (7 levels can be set) 1 0 1 0 X0.125 1 0 1 1 X0.0625 (7 levels can be set) 1 1 0 0 X0.0625 (setting prohibited) 1 1 0 1 X0.0625 (setting prohibited) 1 1 1 0 X0.0625 (setting prohibited) 1 1 1 1 X0.0625 (setting prohibited) Set these bits to 0001 if the 2-level AGC or fixed Kv method is used. In the case of 7-level AGC, the settings indicated as (7 levels can be set) given above are only available.
11 to 8	LKVLM[3:0]	AGC Low Gain Limit Setting These bits set the limit on the lower gain side when the 12-level AGC or 7-level AGC is used.*2 b11 b10 b9 b8 Low gain limit value 0 0 0 0 X64 (setting prohibited) 0 0 0 1 X64 (7 levels can be set) 0 0 1 0 X32 0 0 1 1 X16 (7 levels can be set) 0 1 0 0 X8 0 1 0 1 X4 (7 levels can be set) 0 1 1 0 X2 0 1 1 1 X1 (7 levels can be set) 1 0 0 0 X0.5 1 0 0 1 X0.25 (7 levels can be set) 1 0 1 0 X0.125 1 0 1 1 X0.0625 (7 levels can be set) 1 1 0 0 X0.0625 (setting prohibited) 1 1 0 1 X0.0625 (setting prohibited) 1 1 1 0 X0.0625 (setting prohibited) 1 1 1 1 X0.0625 (setting prohibited) Set these bits to 1011 if the 2-level AGC or fixed Kv method is used. In the case of 7-level AGC, the settings indicated as (7 levels can be set) given above are only available. The LKVLM bits must select a setting that is lower than the range of gains specified by the HKVLM bits.
7 to 3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2 to 0	MAXV[2:0]	Maximum Angular Velocity Select Sets the maximum angular velocity. See **Table 49.13**.

Note 1. To change the setting of AGCD, write 1 to the KIRST bit after the setting has been changed. Otherwise, the

phi angle values are output under the free-running state. The setting of AGCD should be changed while the resolver is not running.

Note 2. Set HKVLM[3:0] gain to be larger than LKVLM[3:0] gain.

[Maximum Angular Velocity Selection Bits]

Table 49.13 lists the maximum angular velocity selected by the MAXV bits and corresponding R/D conversion resolutions.

Table 49.13 Maximum Angular Velocity Selection Bit Settings

When the RDC clock frequency is 40 MHz				
b2	**b1**	**b0**	**Maximum Angular Velocity (in min^{-1})**	**Resolution (in bits)**
0	0	0	120000*1	13
0	0	1	240000*1	12(default)
0	1	0	480000*1	11
0	1	1	960000*1	10
1	0	0	15000*1	16
1	0	1	60000*1	14
1	1	0	240000*1	12
1	1	1	240000*1	12

Note 1. It is value for operation with CCLK running at 40 MHz.

(4) PHI Compare Setting Register 0 (RDC3ALnPHICP0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+$000C_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	INTCLR[2:0]			—	—	—	—	—	—	—	IRS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	INTFLG[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.14 RDC3ALnPHICP0 Register Contents

Bit Position	Bit Name	Function
31 to 27	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
26	INTCLR[2]	Compare Match Interrupt 2 Clear Writing 1 to this bit clears the INTFLG[2] bit to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
25	INTCLR[1]	Compare Match Interrupt 1 Clear Writing 1 to this bit clears the INTFLG[1] bit to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
24	INTCLR[0]	Compare Match Interrupt 0 Clear Writing 1 to this bit clears the INTFLG[0] bit to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
23 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	IRS	Compare Match Interrupt Request Signal Select 0: Compare match signal 1: Signal latching compare match signal
15 to 3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2	INTFLG[2]	Compare Match Interrupt 2 Flag 0: Interrupt request has not been generated. 1: Interrupt request has been generated. This bit is in the scope of control by the PHIERLK bit.
1	INTFLG[1]	Compare Match Interrupt 1 Flag 0: Interrupt request has not been generated. 1: Interrupt request has been generated. This bit is in the scope of control by the PHIERLK bit.
0	INTFLG[0]	Compare Match Interrupt 0 Flag 0: Interrupt request has not been generated. 1: Interrupt request has been generated. This bit is in the scope of control by the PHIERLK bit.

Note: Even if an error occurs when PHIERLK bit is 1, the latching compare match interrupt signal and INTFLG[2:0] bits are cleared by INTCLR[2:0] bits.

(5) PHI Compare Setting Register 1 (RDC3ALnPHICP1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0010_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CMP1[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMP0[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.15 RDC3ALnPHICP1 Register Contents

Bit Position	Bit Name	Function
31 to 16	CMP1[15:0]	Phi Compare Value 1 Sets the angle compare value with a 16-bit width.
15 to 0	CMP0[15:0]	Phi Compare Value 0 Sets the angle compare value with a 16-bit width.

(6) PHI Compare Setting Register 2 (RDC3ALnPHICP2)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0014_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMP2[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.16 RDC3ALnPHICP2 Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
15 to 0	CMP2[15:0]	Phi Compare Value 2 Sets the angle compare value with a 16-bit width.

(7) Sine/Cosine Angle Correction Register (RDC3ALnSCCOR0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0018_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	COSPO[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SINPO[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.17 RDC3ALnSCCOR0 Register Contents

Bit Position	Bit Name	Function
31 to 28	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
27 to 16	COSPO[11:0]	Cosine Angle Correction Specifies the angular correction value for the phi to be input to the COS ROM table as a 12-bit singed integer.*1 b27 to b16 000_H: 0° (no correction) $7FF_H$: +180° (maximum correction in the positive direction) 800_H: -180° (maximum correction in the negative direction)
15 to 12	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
11 to 0	SINPO[11:0]	Sine Angle Correction Specifies the angular correction value for the phi to be input to the SIN ROM table as a 12-bit singed integer.*1 b11 to b0 000_H: 0° (no correction) $7FF_H$: +180° (maximum correction in the positive direction) 800_H: -180° (maximum correction in the negative direction)

Note 1. Set 000_H (0°) in these bits when executing an angle conversion BIST.

(8) Sine/Cosine Correction Register 1 (RDC3ALnSCCOR1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+001C$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	PHCST	—	GNCST	CMCLT[1:0]		CMCSL[1:0]		GNCLT[1:0]		GNCSL[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PHCLT[1:0]		PHCSL[1:0]		—	NSRSL	GNCND	SGLMD	GNJSP	GNCNS[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.18 RDC3ALnSCCOR1 Register Contents (1/3)

Bit Position	Bit Name	Function
31 to 27	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
26	PHCST	Phase Correction Start Writing 1 to this bit starts phase correction. Set this bit to 1 after the RDC has entered the angular tracking state. This bit returns to 0 after one or two clock cycles has elapsed following it being set to 1. This bit is effective only for once after a reset.
25	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
24	GNCST	Gain Correction Start Writing 1 to this bit starts gain correction and common offset correction. Set this bit to 1 after the RDC has entered the angular tracking state and the resolver has rotated through an electrical angle of at least 180°. This bit returns to 0 after one or two clock cycles has elapsed following it being set to 1.
23, 22	CMCLT[1:0]	Common Offset Correction Limit Sets limitation for the range of correcting the common offset value. If the value for correction obtained from the input signal exceeds the set limitation, the set value is used for correction. b23 b22 Limitation on the value for correction 0 0: ± 0.0312 × AFCVCC (approx. ± 150 mV) (default) 0 1: ± 0.0156 × AFCVCC (approx. ± 78 m V) 1 0: ± 0.125 × AFCVCC (approx. ± 625 mV) 1 1: ± 0 × AFCVCC (± 0 mV) (no correction applied)
21, 20	CMCSL[1:0]	Common Offset Correction Type Select Selects the type of correcting by the common offset value. b21 b20 Type of correction 0 0: No correction (fixed to 00$_H$, this is the default setting) 0 1: Always use the fixed offset correction value set by CSOSN[9:0] and CCOSN[9:0]. 1 0: Use the offset correction value obtained from the calculation. The timing to apply this value depends on the setting of the GNCSL bit. 1 1: Setting prohibited

Table 49.18 RDC3ALnSCCOR1 Register Contents (2/3)

Bit Position	Bit Name	Function
19, 18	GNCLT[1:0]	Gain Correction Range Limit Sets limitation for the range of correcting the gain value. If the value for correction obtained from the input signal exceeds the set limitation, the set value is used for correction. b19 b18 Limitation on the value for correction 0 0: ± 20% (default) 0 1: ± 10% 1 0: ± 40% 1 1: ± 0% (no correction applied)
17, 16	GNCSL[1:0]	Gain Correction Type Select Selects the type of correcting by the gain value. b17 b16 Type of correction 0 0: No correction (fixed to 1024, this is the default setting) 0 1: Always use the fixed correction value set by GNCNM[11:0] 1 0: Use the correction value obtained from the calculation at the time of GNCST being set 1 1: Use the correction value obtained from the calculation at the time of z-phase output following GNCST being set (correct the value on every single rotation).
15 to 12	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
11, 10	PHCLT[1:0]	Phase Correction Limit Sets limitation for the range of correcting the sine and cosine phases. If the value for delay obtained from the input signal exceeds the set limitation, the set value is used for delay compensation. b11 b10 Limitation of delay compensation 0 0: 3 µs (default) 0 1: 1 µs 1 0: 6 µs 1 1: 0 µs (no correction applied)
9, 8	PHCSL[1:0]	Sine/Cosine Phase Correction Type Select Selects the type of correction for the sine and cosine phases. b9 b8 Type of correction 0 0: No correction (default) 0 1: After writing 1 to the PHCST bit, the phase difference at 16 crossings of the excitation signal is constantly averaged to obtain the correction value. 1 0: Every time 1 is written to the PHCST bit, the phase difference at 16 crossings of the excitation signal is averaged once to obtain the correction value, and then the correction value is used. 1 1: Use the fixed correction value set by PHCNM[5:0] and PHSNM[5:0].
7	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
6	NSRSL	ADC Noise Elimination Target Select 0: Apply the ADC noise filter to the sine, cosine, gain, and common offset compensation calculating circuits (default). 1: Apply the ADC noise filter to the sine, cosine, gain, and common offset compensation calculating circuits and multiplication and sub-traction circuits.
5	GNCND	AD Noise Elimination Disable Disables the AD noise eliminator. 0: Noise eliminator is enabled (default) 1: Noise eliminator is disabled
4	SGLMD	AD Stucking Detection Circuit Disable Disables the AD stucking detector. 0: Stucking detector is enabled (default) 1: Stucking detector is disabled
3	GNJSP	Noise Elimination Comparison Select Selects the noise elimination comparison target. 0: Compare with last and previous AD conversion results 1: Compare with last and two previous AD conversion results

Table 49.18 RDC3ALnSCCOR1 Register Contents (3/3)

Bit Position	Bit Name	Function
2 to 0	GNCNS[2:0]	AD Noise Elimination Setting Sets the threshold for judging the value of AD conversion to be noise. If the value obtained as the result of AD conversion exceeds the value of these bits, it is rejected. b2 b1 b0 Threshold for noise 0 0 0: 128(approx. 156 mV) (default) 0 0 1: 32 (approx. 39 mV) 0 1 0: 64 (approx. 78 mV) 0 1 1: 128 (approx. 156 mV) 1 0 0: 256 (approx. 313 mV) 1 0 1: 512 (approx. 625 mV) 1 1 0: 1024 (approx. 1250 mV) 1 1 1: 2048 (approx. 2500 mV)

(9) Sine/Cosine Correction Register 2 (RDC3ALnSCCOR2)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0020_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	GNCNM[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PHCNM[5:0]						—	—	PHSNM[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.19 RDC3ALnSCCOR2 Register Contents

Bit Position	Bit Name	Function
31 to 28	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
27 to 16	GNCNM[11:0]	Gain Correction Fixed Value Sets the fixed value for use in gain correction. The value obtained from the calculation below is multiplied by the gain value for the cosine side. - Value for correction of the cosine side = d'(GNCNM[11:0])/1024 Set these bits to 1024 (multiplication by 1) for no correction. If $1178(49A_H)$ is set, for example, the value for the cosine side is corrected by +15%.
15, 14	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
13 to 8	PHCNM[5:0]	Cosine Side Phase Correction Fixed Value Sets the fixed value for use in correction of the phase (amount of delay) of the cosine side. The value for delay obtained from the calculation below is inserted on the cosine side. - Value for delay of the cosine side = d'(PHCNM[5:0]) × 200 ns The setting from $3F_H$ to $1F_H$ are not allowed. Allowed values are between 0 µs to 6 µs.
7, 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	PHSNM[5:0]	Sine Side Phase Correction Fixed Value Sets the fixed value for use in correction of the phase (amount of delay) of the sine side. The value for delay obtained from the calculation below is inserted on the sine side. - Value for delay of the sine side = d'(PHSNM[5:0]) × 200 ns The setting from $3F_H$ to $1F_H$ are not allowed. Allowed values are between 0 µs to 6 µs.

(10) Sine/Cosine Correction Register 3 (RDC3ALnSCCOR3)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0024_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CCOSN[9:0]									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CSOSN[9:0]									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.20 RDC3ALnSCCOR3 Register Contents

Bit Position	Bit Name	Function
31 to 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25 to 16	CCOSN[9:0]	Cosine Side Common Off-set Correction Fixed Value Setting Sets the fixed value (two's complement) for use in correction of the cosine side common value. The value obtained from the calculation below is subtracted from the result of A/D conversion. - Common offset value of the cosine side = d'(CCOSN[9:0]) × AFCVCC/4096 (V)
15 to 10	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
9 to 0	CSOSN[9:0]	Sine Side Common Off-set Correction Fixed Value Setting Sets the fixed value (two's complement) for use in correction of the sine side common value. The value obtained from the calculation below is subtracted from the result of A/D conversion. - Common offset value of the sine side = d'(CSOSN[9:0]) × AFCVCC/4096 (V)

(11) Automatic Amplitude Adjustment Register 0 (RDC3ALnATMNT0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0028_H

Value after reset: xxx4 8200_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IRSS0	IGRT	IGRM[3:0]				—	—	EXOC[1:0]		IRSC[3:0]			
Value after reset	0	*	0	*	*	*	*	*	*	*	1	0	0	1	0	0
R/W	R	R	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EADSTS	EAAOD	IRSS1	EXOS	—	—	EAATSP	SQJGT	—	—	—		—	—	—	
Value after reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R

*: Undefined

Table 49.21 RDC3ALnATMNT0 Register Contents (1/3)

Bit Position	Bit Name	Function
31	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
30	Reserved	The read value is undefined. The write value should always be 0.
29	IRSS0	Input Gain Resistance Flash Trimming Value Invalidation Selects the value for use in the input gain resistance. The selection is made by the combination of the values of this bit, the IRSS1 bit, and the IGRT signal from the flash memory (see **Table 49.22**).
28	IGRT	Flash Input Gain Resistance Value Invalid Confirmation This bit is for conforming the level of the input signal (IGRT) from the flash memory, which invalidates the trimming value for the input gain resistance. 0: The trimming value set in the flash memory is valid. 1: The trimming value set in the flash memory is invalid.
27 to 24	IGRM[3:0]	Flash Input Gain Resistance Value Confirmation These bits reflect the levels of the input signal from the flash memory which hold the value for the input gain resistance (IGRM[3:0]). b27 b26 b25 b24 0 0 0 0: input gain resistance value TYP - 40% 0 0 0 1: input gain resistance value TYP - 30% 0 0 1 0: input gain resistance value TYP - 20% 0 0 1 1: input gain resistance value TYP - 10% 0 1 0 0: input gain resistance value TYP± 0% 0 1 0 1: input gain resistance value TYP + 10% 0 1 1 0: input gain resistance value TYP + 20% 0 1 1 1: input gain resistance value TYP + 30% 1 0 0 0: input gain resistance value TYP + 40% 1 0 0 1: input gain resistance value TYP + 40% 1 0 1 0: input gain resistance value TYP + 40% 1 0 1 1: input gain resistance value TYP + 40% 1 1 0 0: input gain resistance value TYP + 40% 1 1 0 1: input gain resistance value TYP + 40% 1 1 1 0: input gain resistance value TYP + 40% 1 1 1 1: input gain resistance value TYP + 40%
23, 22	Reserved	The read value is undefined. The write value should always be 0.

Table 49.21 RDC3ALnATMNT0 Register Contents (2/3)

Bit Position	Bit Name	Function
21, 20	EXOC[1:0]	Excitation Output Value Setting These bits make settings of the excitation output. The value in these bits are output from the excitation amplitude automatic adjustment circuit as the excitation output amplitude setting when the EXOS bit is 0. b21 b20 0 0: excitation output value TYP - 40% 0 1: excitation output value TYP - 20% 1 0: excitation output value TYP± 0% (default) 1 1: excitation output value TYP + 20%
19 to 16	IRSC[3:0]	Input Gain Resistance Value Select These bits specify the input gain resistance (RF) value. The value in these bits are output from the excitation amplitude automatic adjustment circuit as the input gain resistance value setting when the IRSS1 bit is 0 and the IRSS0 bit is 1, or when the IRSS1 bit is 0 and the signal from the flash memory is 1. See **Table 49.22**. b19 b18 b17 b16 0 0 0 0 : input gain resistance value TYP - 40% 0 0 0 1 : input gain resistance value TYP - 30% 0 0 1 0 : input gain resistance value TYP - 20% 0 0 1 1 : input gain resistance value TYP - 10% 0 1 0 0 : input gain resistance value TYP ± 0% (default) 0 1 0 1 : input gain resistance value TYP + 10% 0 1 1 0 : input gain resistance value TYP + 20% 0 1 1 1 : input gain resistance value TYP + 30% 1 0 0 0 : input gain resistance value TYP + 40% 1 0 0 1 : input gain resistance value TYP + 40% 1 0 1 0 : input gain resistance value TYP + 40% 1 0 1 1 : input gain resistance value TYP + 40% 1 1 0 0 : input gain resistance value TYP + 40% 1 1 0 1 : input gain resistance value TYP + 40% 1 1 1 0 : input gain resistance value TYP + 40% 1 1 1 1 : input gain resistance value TYP + 40%
15	EADSTS	Excitation Amplitude Automatic Adjustment Stop on Error This bit is a function to stop the excitation amplitude automatic adjustment by setting at the time of occurrence of an error (ERR bit = 1). 0: Automatic adjustment is not stopped. 1: Automatic adjustment is stopped.
14	EAAOD	Excitation Amplitude Automatic Adjustment Order Select Selects which amplitude adjustment factor to apply first to the excitation amplitude automatic adjustment circuit as correction by the input gain resistance value or by the excitation output. 0: Correction by the excitation output first and then the input gain resistance. 1: Correction by the input gain resistance value first and then the excitation output.
13	IRSS1	Input Gain Resistance Value Adjustment Output Select Selects the value for use in the input gain resistance. The selection is made by the combination of the values of this bit, the IRSS0 bit, and the IGRT signal from the flash memory (see **Table 49.22**).
12	EXOS	Excitation Output Amplitude Setting Select Selects the value for use in the excitation amplitude to be output from the excitation amplitude automatic adjustment circuit as either of the following: the value set in the relevant register or the value set for excitation output automatic adjustment. 0: The value set in the EXOC[1:0] bits. 1: The value set for the excitation output automatic adjustment.
11, 10	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 49.21 RDC3ALnATMNT0 Register Contents (3/3)

Bit Position	Bit Name	Function
9	EAATSP	Excitation Amplitude Automatic Adjustment Stop Stops excitation amplitude adjustment. When this bit is changed from 0 to 1, the adjustment value at that time is retained. 0: Performs automatic adjustment. 1: Stops automatic adjustment.
8	SQJGT	Excitation Amplitude Sum-of-Squares Judgment Time Select Sets the interval for adjusting the amplitude of the excitation wave-form generated by the excitation amplitude automatic adjustment circuit. 0: Adjusts the amplitude of excitation waveforms every 1 milliseconds*1. 1: Adjusts the amplitude of excitation waveforms every 10 milliseconds*1.
7 to 0	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Note 1. The timing value is when the CCLK is running at 40 MHz.

[Selection of the Input Gain Resistance Value]

One of the following three values is selected as the input gain resistance value to be output from the excitation amplitude automatic adjustment circuit.

- Automatically adjusted input gain resistance value
- The value set in the IRSC[3:0] bits
- The value for trimming from the flash memory (which is read from the IGRM[3:0] bits)

The values of the IRSS1 and IRSS0 bits, and of the IGRT signal from the flash memory, are used in combination to select the value to use for input gain resistance as shown in **Table 49.22**.

Table 49.22 Input Gain Resistance Adjustment Code Selection

IRSS1 Bit	IRSS0 Bit	The IGRT Signal from the Flash Memory	Selected Setting of the Input Gain Resistance Value
0	0	0	The value for trimming from the flash memory
0	0	1	The value in the IRSC[3:0] bits
0	1	X	The value in the IRSC[3:0] bits
1	X	X	Automatically adjusted input gain resistance value

(12) Automatic Amplitude Adjustment Register 1 (RDC3ALnATMNT1)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+002C$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESQULL	ESQOUL
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RLT[17:4]													
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.23 RDC3ALnATMNT1 Register Contents

Bit Position	Bit Name	Function
31 to 18	Reserved	When read, the value after reset is returned.
17	ESQULL	Excitation Amplitude Integrated Sum-of-Squares Value Fall Below Lower Limit Determine Excitation amplitude integrated sum-of-squares value fall below lower limit determine signal is stored. 0: Excitation amplitude integrated sum-of-squares value is equal to or larger than the lower limit. 1: Excitation amplitude integrated sum-of-squares value is smaller than the lower limit.
16	ESQOUL	Excitation Amplitude Integrated Sum-of-Squares Value Exceed Upper Limit Determine Excitation amplitude integrated sum-of-squares value exceed upper limit determine signal is stored. 0: Excitation amplitude integrated sum-of-squares value is equal to or smaller than the upper limit. 1: Excitation amplitude integrated sum-of-squares value is larger than the upper limit.
15, 14	Reserved	When read, the value after reset is returned.
13 to 0	RLT[17:4]	Excitation Amplitude Integrated Sum-of-Squares Value Upper 14 bits of the 18-bit excitation amplitude integrated sum-of-squares value is stored. The value is updated every 1 ms*1.

Note 1. The timing value is when the CCLK is running at 40 MHz.

(13) Error Detection Register 0 (RDC3ALnDIAG0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0030$_H$

Value after reset: 001A 2933$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	P2ANT[1:0]		EXCETH[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SGBTH[7:0]								SGBDTH[7:0]							
Value after reset	0	0	1	0	1	0	0	1	0	0	1	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.24 RDC3ALnDIAG0 Register Contents

Bit Position	Bit Name	Function
31 to 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25, 24	P2ANT [1:0]	Two Paths Conversions Error Threshold These bits set the threshold for two-path conversion error in comparison between the results from conversion loop 0 and 1. b25 b24 Threshold for comparison 0 0 ±8 LSB (with 12-bit resolution) 0 1 ±4 LSB (with 12-bit resolution) 1 0 ±32 LSB (with 12-bit resolution) 1 1 ±64 LSB (with 12-bit resolution)
23 to 16	EXCETH[7:0]	Resolver Signal Error Comparison Threshold Sets the threshold for use in detecting errors in the resolver signal. The threshold is obtained from the formula below. - Threshold value = 2 × d'(EXCETH[7:0]) × 8 × AFCVCC/4096 (Vpp) Default setting 1A$_H$: 0.102 × AFCVCC (Vpp)
15 to 8	SGBTH[7:0]	Disconnect Error Comparison Threshold (for VR Resolver) Sets the threshold for use in detecting disconnect errors when the VR resolver is used. The threshold is obtained from the formula below. - Threshold value = 0.5 × AFCVCC + d'(SGBTH[7:0]) × 8 × AFCVCC/4096 (V) Default setting 29$_H$: 0.58 × AFCVCC (V)
7 to 0	SGBDTH[7:0]	Disconnect Error Comparison Threshold Setting (for DC Resolver) Sets the threshold for use in detecting disconnect errors when the DC resolver is used. The threshold is obtained from the formula below. - Threshold value = 0.5 × AFCVCC + (d'(SGBDTH[7:0]) × 8 + 1024) × AFCVCC/4096 (V) Default setting 33$_H$: 0.85 × AFCVCC (V)

(14) Error Detection Register 1 (RDC3ALnDIAG1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0034$_H$

Value after reset: B000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	CVEDS	EDPS[1:0]		—	—	VGASL[1:0]		—	—	—	VGST	—	—	—	INIT
Value after reset	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	ERDEN	—	SQERST	—	ERRST	—	—	—	—	—	—	—	KIRST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R/W	R	R/W	R	R	R	R	R	R	R	R/W

Table 49.25 RDC3ALnDIAG1 Register Contents (1/2)

Bit Position	Bit Name	Function
31	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
30	CVEDS	Conversion Error Detection Circuit Select Selects the conversion error detection circuit. 0: The conversion error detection circuit which supports high-speed rotation of the R/D conversion error detection signal.*2 1: The conversion error detection circuit which does not support high-speed rotation of the R/D conversion error detection signal.
29, 28	EDPS[1:0]	RD Conversion Error Determination Time Select Selects the error determination time for R/D conversion errors*3 b29 b28 0 0: 95.8*1 millisecond*4 0 1: 147*1 millisecond*4 1 0: 4.92*1 millisecond 1 1: 7.37*1 millisecond (default)
27, 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25, 24	VGASL[1:0]	Power/Ground Short Error Detection Start Method Select Selects the timing to start detection of a power/ground short error. b25 b24 Starting method 0 0: No detection (default) 0 1: When 1 is written to the VGST bit 1 0: Every 10 ms 1 1: No detection
23 to 21	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
20	VGST	Power/Ground Short Error Detection Start Writing 1 to this bit executes power/ground short error detection a single time for all six analog pins. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
19 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	INIT	Initialization Writing 1 to this bit leads to initialization within RDC3AL. After this bit has been set to 1, its value is restored to 0 following the completion of initialization within RDC3AL.*5

Table 49.25 RDC3ALnDIAG1 Register Contents (2/2)

Bit Position	Bit Name	Function
15 to 13	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
12	ERDEN	Error Detection Start Error detection is enabled when the error detection output mask is released after 26 milliseconds*1 have elapsed following this bit being set to 1.*6
11	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
10	SQERST	Sum-of-Squares Amplitude Error Excitation Counter Reset Writing 1 to this bit resets the sum-of-squares amplitude error excitation counter to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	ERRST	Error Signal Reset Bit Writing 1 to this bit resets the register bits listed below to 0. Note that each of these bits remains at 1 if an error continues. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1. Register bits: ERHD, ERDEXC, ERDSBC, ERDSBS, ERDSQ, ERDP2, ERDCNV, ERDR1V, ERDR2V, ERDS1 to 4V, ERDR1G, ERDR2G, ERDS1 to 4G
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	KIRST	Ki Component Reset The values of the Ki integrator and accumulator integrator become 0 by writing 1 to this bit. On reset, the AGCON function is enabled and the Kv gain of the PI compensator goes high. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1. After setting this bit to 1, wait at least 2 us to set it again.

Note 1. The timing value is when the CCLK is running at 40 MHz.

Note 2. Input the excitation signal whose frequency is below 22 kHz when the RD conversion error detection circuit (which supports high-speed rotation) is used (CVEDS = 0).

Note 3. Do not set EDPS[1:0] to a shorter determination time than the current setting while the R/D converter is operating. In other words, the settings below are prohibited;
When EDPS[1:0] = 01, setting EDPS[1:0] to 00, 10, or 11 is prohibited.
When EDPS[1:0] = 00, setting EDPS[1:0] to 10 or 11 is prohibited.
When EDPS[1:0] = 11, setting EDPS[1:0] to 10 is prohibited.
However, changing from 11b to 10b is allowed if the ERDEN bit in the RDC3ALnDIAG1 register is 0 after a reset. After changing the bits, set the ERDEN bit to 1.

Note 4. Do not set this value when the R/D conversion error detection circuit (which supports high-speed rotation) is selected (CVEDS = 0).

Note 5. The user must not clear the INIT bit once it has been set.

Note 6. The functionality of error detection is disabled after a reset. It is enabled after 26 milliseconds since the ERDEN bit has been set to 1. Enabling this functionality by setting this bit to 1 takes effects only once, following a reset (setting this bit to 0 does not disable error detection). To disable this functionality after enabling it, disable interrupts by setting the EINTEN bit to 0. The bits in the RDC3ALnDGOUT0 and RDC3ALnDGOUT1 registers are enabled by the ERDEN bit.

[R/D Conversion Error Determination Time Select Bits]

These bits are used to set the time to determine R/D conversion errors. If control variation(ε) between the input angle and R/D converted angle remains large for more than 50% of the specified determination time, it is regarded as the R/D conversion error and the ERCNV bit in the RDC3ALnDGOUT0 register is set to 1 if the ERCNVS bit selects detection of a conversion error. Furthermore, if the EINTEN bit in the RDC3ALnENC0 register is 1, the ERR and ERHD bits in the RDC3ALnDGOUT0 register are set to 1 and an RDC error interrupt occurs.

(15) Error Detection Register 2 (RDC3ALnDIAG2)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0038_H

Value after reset: 0080 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	EREXCS	ERSBCS	ERSBSS	—	ERSQS	ERP2S	ERCNVS
Value after reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ERR1VS	ERR2VS	ERS1VS	ERS2VS	ERS3VS	ERS4VS	—	—	ERR1GS	ERR2GS	ERS1GS	ERS2GS	ERS3GS	ERS4GS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.26 RDC3ALnDIAG2 Register Contents (1/3)

Bit Position	Bit Name	Function
31 to 23	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
22	EREXCS	Resolver Signal Error Select Selects whether or not to output detection of a resolver signal error. 0: Set the bits ERR, ERHD, EREXC, and ERDEXC to 1 on occurrence of a resolver signal error 1: Do not set the bits ERR, ERHD, EREXC, and ERDEXC to 1 on occurrence of a resolver signal error
21	ERSBCS	Disconnection Error (Cosine) Select Selects whether or not to output detection of a disconnect error (cosine side). 0: Set the bits ERR, ERHD, ERSBC, and ERDSBC to 1 on occurrence of a disconnect error (cosine side). 1: Do not set the bits ERR, ERHD, ERSBC, and ERDSBC to 1 on occurrence of a disconnect error (cosine side).
20	ERSBSS	Disconnection Error (Sine) Selection Selects whether or not to output detection of a disconnect error (sine side) 0: Set the bits ERR, ERHD, ERSBS, and ERDSBS to 1 on occurrence of a disconnect error (sine side). 1: Do not set the bits ERR, ERHD, ERSBS, and ERDSBS to 1 on occurrence of a disconnect error (sine side).
19	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
18	ERSQS	Sum-of-Squares Amplitude Error Select Selects whether or not to output detection of a sum-of-squares amplitude error. 0: Set the bits ERR, ERHD, ERSQ, and ERDSQ to 1 on occurrence of a sum-of-squares amplitude error. 1: Do not set the bits ERR, ERHD, ERSQ, and ERDSQ to 1 on occurrence of a sum-of-squares amplitude error.
17	ERP2S	Two Paths Conversion Error Select Selects whether or not to output detection of a two paths conversion error. 0: Set the bits ERR, ERHD, ERP2, and ERDP2 to 1 on occurrence of a two paths conversion error. 1: Do not set the bits ERR, ERHD, ERP2, and ERDP2 to 1 on occurrence of a two paths conversion error.

Table 49.26 RDC3ALnDIAG2 Register Contents (2/3)

Bit Position	Bit Name	Function
16	ERCNVS	Conversion Error Select Selects whether or not to output detection of a conversion error. 0: Set the bits ERR, ERHD, ERCNV, and ERDCNV to 1 on occurrence of a conversion error. 1: Do not set the bits ERR, ERHD, ERCNV, and ERDCNV to 1 on occurrence of a conversion error.
15, 14	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
13	ERR1VS	RSO Power Short Error Select Selects whether or not to output detection of an RSO pin power short error. 0: Set the bits ERR, ERHD, ERR1V, and ERDR1V to 1 on occurrence of an RSO pin power short error. 1: Do not set the bits ERR, ERHD, ERR1V, and ERDR1V to 1 on occurrence of an RSO pin power short error.
12	ERR2VS	COM Power Short Error Select Selects whether or not to output detection of a COM pin power short error. 0: Set the bits ERR, ERHD, ERR2V, and ERDR2V to 1 on occurrence of a COM pin power short error. 1: Do not set the bits ERR, ERHD, ERR2V, and ERDR2V to 1 on occurrence of a COM pin power short error.
11	ERS1VS	S1 Power Short Error Select Selects whether or not to output detection of an S1 pin power short error. 0: Set the bits ERR, ERHD, ERCNV, ERS1V, and ERDS1V to 1 on occurrence of an S1 pin power short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS1V, and ERDS1V to 1 on occurrence of an S1 pin power short error.
10	ERS2VS	S2 Power Short Error Select Selects whether or not to output detection of an S2 pin power short error. 0: Set the bits ERR, ERHD, ERCNV, ERS2V, and ERDS2V to 1 on occurrence of an S2 pin power short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS2V, and ERDS2V to 1 on occurrence of an S2 pin power short error.
9	ERS3VS	S3 Power Short Error Select Selects whether or not to output detection of an S3 pin power short error. 0: Set the bits ERR, ERHD, ERCNV, ERS3V, and ERDS3V to 1 on occurrence of an S3 pin power short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS3V, and ERDS3V to 1 on occurrence of an S3 pin power short error.
8	ERS4VS	S4 Power Short Error Select Selects whether or not to output detection of an S4 pin power short error. 0: Set the bits ERR, ERHD, ERCNV, ERS4V, and ERDS4V to 1 on occurrence of an S4 pin power short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS4V, and ERDS4V to 1 on occurrence of an S4 pin power short error.
7, 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5	ERR1GS	RSO Ground Short Error Select Selects whether or not to output detection of an RSO pin ground short error. 0: Set bits ERR, ERHD, ERR1G, and ERDR1G to 1 following an RSO ground short-circuit error. 1: Does not set bits ERR, ERHD, ERR1G, and ERDR1G to 1 following an RSO ground short-circuit error.
4	ERR2GS	COM Ground Short Error Select Selects whether or not to output detection of a COM pin ground short error. 0: Set the bits ERR, ERHD, ERR2G, and ERDR2G to 1 on occurrence of a COM pin ground short error. 1: Do not set the bits ERR, ERHD, ERR2G, and ERDR2G to 1 on occurrence of a COM pin ground short error.

Table 49.26 RDC3ALnDIAG2 Register Contents (3/3)

Bit Position	Bit Name	Function
3	ERS1GS	S1 Ground Short Error Select Selects whether or not to output detection of an S1 pin ground short error. 0: Set the bits ERR, ERHD, ERCNV, ERS1G, and ERDS1G to 1 on occurrence of an S1 pin ground short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS1G, and ERDS1G to 1 on occurrence of an S1 pin ground short error.
2	ERS2GS	S2 Ground Short Error Select Selects whether or not to output detection of an S2 pin ground short error. 0: Set the bits ERR, ERHD, ERCNV, ERS2G, and ERDS2G to 1 on occurrence of an S2 pin ground short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS2G, and ERDS2G to 1 on occurrence of an S2 pin ground short error.
1	ERS3GS	S3 Ground Short Error Select Selects whether or not to output detection of an S3 pin ground short error. 0: Set the bits ERR, ERHD, ERCNV, ERS3G, and ERDS3G to 1 on occurrence of an S3 pin ground short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS3G, and ERDS3G to 1 on occurrence of an S3 pin ground short error.
0	ERS4GS	S4 Ground Short Error Select Selects whether or not to output detection of an S4 pin ground short error. 0: Set the bits ERR, ERHD, ERCNV, ERS4G, and ERDS4G to 1 on occurrence of an S4 pin ground short error. 1: Do not set the bits ERR, ERHD, ERCNV, ERS4G, and ERDS4G to 1 on occurrence of an S4 pin ground short error.

(16) Error Detection Output Register 0 (RDC3ALnDGOUT0)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+$003C_H$

Value after reset: $00x0\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VGFLG	—	—	ERR	—	—	—	ERHD	—	EREXC	ERSBC	ERSBS	—	ERSQ	ERP2	ERCNV
Value after reset	0	0	0	0	0	0	0	0	*	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ERR1V	ERR2V	ERS1V	ERS2V	ERS3V	ERS4V	—	—	ERR1G	ERR2G	ERS1G	ERS2G	ERS3G	ERS4G
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.27 RDC3ALnDGOUT0 Register Contents (1/2)

Bit Position	Bit Name	Function
31	VGFLG	Power/Ground Short Error Detection Running This flag indicates whether or not the power/ground short error detection or the power/ground short error detection BIST is running or not. The detection or BIST is running if the flag is 1.
30 to 29	Reserved	When read, the value after reset is returned.
28	ERR	Error This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ALnDIAG2 register is being output. This bit returns to 0 on recovery from the error. This flag is not set to 1 if the EINTEN bit of the RDC3ALnENC0 register is 0.
27 to 25	Reserved	When read, the value after reset is returned.
24	ERHD	Error Hold This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ALnDIAG2 register is being output. This signal is reset to 0 by setting the ERRST bit to 1. Note that this bit remains at 1 if errors occur continuously. This flag is not set to 1 if the EINTEN bit of the RDC3ALnENC0 register is 0.
23	Reserved	The read value is undefined.
22	EREXC	Resolver Signal Error The value of this flag becomes 1 when a resolver signal error occurs and returns to 0 on recovery from the error.
21	ERSBC	Disconnect Error (Cosine Side) The value of this flag becomes 1 when a disconnect error (cosine side) occurs and returns to 0 on recovery from the error.
20	ERSBS	Disconnect Error (Sine Side) The value of this flag becomes 1 when a disconnect error (sine side) occurs and returns to 0 on recovery from the error.
19	Reserved	When read, the value after reset is returned.
18	ERSQ	Sum-of-Squares Amplitude Error The value of this flag becomes 1 when a sum-of-squares amplitude error occurs. This bit drops to 0 when the abnormal excitation count value is cleared by setting the SQERST bit or ERRST bit to 1 after recovery from Sum-of-Squares amplitude error.

Table 49.27 RDC3ALnDGOUT0 Register Contents (2/2)

Bit Position	Bit Name	Function
17	ERP2	Two Paths Conversion Error The value of this flag becomes 1 when a two path conversion error occurs and returns to 0 on recovery from the error.
16	ERCNV	Conversion Error The value of this flag becomes 1 when a conversion error occurs and returns to 0 on recovery from the error.
15, 14	Reserved	When read, the value after reset is returned.
13	ERR1V	RSO Power Short Error The value of this flag becomes 1 when an RSO pin power short error occurs and returns to 0 on recovery from the error.*1
12	ERR2V	COM Power Short Error The value of this flag becomes 1 when a COM pin power short error occurs and returns to 0 on recovery from the error.*1
11	ERS1V	S1 Power Short Error The value of this flag becomes 1 when a S1 pin power short error occurs and returns to 0 on recovery from the error.*1
10	ERS2V	S2 Power Short Error The value of this flag becomes 1 when a S2 pin power short error occurs and returns to 0 on recovery from the error.*1
9	ERS3V	S3 Power Short Error The value of this flag becomes 1 when a S3 pin power short error occurs and returns to 0 on recovery from the error.*1
8	ERS4V	S4 Power Short Error The value of this flag becomes 1 when a S4 pin power short error occurs and returns to 0 on recovery from the error.*1
7, 6	Reserved	When read, the value after reset is returned.
5	ERR1G	RSO Ground Short Error The value of this flag becomes 1 when an RSO pin ground short error occurs and returns to 0 on recovery from the error.*1
4	ERR2G	COM Ground Short Error The value of this flag becomes 1 when a COM pin ground short error occurs and returns to 0 on recovery from the error.*1
3	ERS1G	S1 Ground Short Error The value of this flag becomes 1 when a S1 pin ground short error occurs and returns to 0 on recovery from the error.*1
2	ERS2G	S2 Ground Short Error The value of this flag becomes 1 when a S2 pin ground short error occurs and returns to 0 on recovery from the error.*1
1	ERS3G	S3 Ground Short Error The value of this flag becomes 1 when a S3 pin ground short error occurs and returns to 0 on recovery from the error.*1
0	ERS4G	S4 Ground Short Error The value of this flag becomes 1 when a S4 pin ground short error occurs and returns to 0 on recovery from the error.*1

Note 1. After the pin status returns from the error state, this bit returns to 0 when the Power/Ground short error detection is executed again and it is determined to be normal, or when it is cleared by the ERRST bit.

(17) Error Detection Output Register 1 (RDC3ALnDGOUT1)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0040_H

Value after reset: $00x0\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	ERR	—	—	—	ERHD	—	ERDEXC	ERDSBC	ERDSBS	—	ERDSQ	ERDP2	ERDCNV
Value after reset	0	0	0	0	0	0	0	0	*	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ERDR1V	ERDR2V	ERDS1V	ERDS2V	ERDS3V	ERDS4V	—	—	ERDR1G	ERDR2G	ERDS1G	ERDS2G	ERDS3G	ERDS4G
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.28 RDC3ALnDGOUT1 Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned.
28	ERR	Error This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ALnDIAG2 register is being output. This bit returns to 0 on recovery from the error. This flag is not set to 1 if the EINTEN bit of the RDC3ALnENC0 register is 0.
27 to 25	Reserved	When read, the value after reset is returned.
24	ERHD	Error Hold This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ALnDIAG2 register is being output. This signal is reset to 0 by setting the ERRST bit to 1. Note that this bit remains at 1 if errors occur continuously. This flag is not set to 1 if the EINTEN bit of the RDC3ALnENC0 register is 0.
23	Reserved	The read value is undefined.
22	ERDEXC	Resolver Signal Error Hold The value of this flag becomes 1 when a resolver signal error occurs. This bit remains at 1 until it is reset by the ERRST bit.
21	ERDSBC	Disconnect Error (Cosine Side) Hold The value of this flag becomes 1 when a disconnect error (cosine side) occurs. This bit remains at 1 until it is reset by the ERRST bit.
20	ERDSBS	Disconnect Error (Sine Side) Hold The value of this flag becomes 1 when a disconnect error (sine side) occurs. This bit remains at 1 until it is reset by the ERRST bit.
19	Reserved	When read, the value after reset is returned.
18	ERDSQ	Sum-of-Squares Amplitude Error Hold The value of this flag becomes 1 when a sum-of-squares amplitude error occurs. This bit remains at 1 until it is reset by the ERRST bit.
17	ERDP2	Two Paths Conversion Error Hold The value of this flag becomes 1 when a two paths conversion error occurs. This bit remains at 1 until it is reset by the ERRST bit.
16	ERDCNV	Conversion Error Hold The value of this flag becomes 1 when a conversion error occurs. This bit remains at 1 until it is reset by the ERRST bit.
15, 14	Reserved	When read, the value after reset is returned.

Table 49.28 RDC3ALnDGOUT1 Register Contents (2/2)

Bit Position	Bit Name	Function
13	ERDR1V	RSO Power Short Error Hold The value of this flag becomes 1 when an RSO pin power short error occurs. This bit remains at 1 until it is reset by the ERRST bit.
12	ERDR2V	COM Power Short Error Hold The value of this flag becomes 1 when a COM pin power short error occurs. This bit remains at 1 until it is reset by the ERRST bit.
11	ERDS1V	S1 Power Short Error Hold The value of this flag becomes 1 when a S1 pin power short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
10	ERDS2V	S2 Power Short Error Hold The value of this flag becomes 1 when a S2 pin power short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
9	ERDS3V	S3 Power Short Error Hold The value of this flag becomes 1 when a S3 pin power short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
8	ERDS4V	S4 Power Short Error Hold The value of this flag becomes 1 when a S4 pin power short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
7, 6	Reserved	When read, the value after reset is returned.
5	ERDR1G	RSO Ground Short Error Hold The value of this flag becomes 1 when an RSO pin ground short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
4	ERDR2G	COM Ground Short Error Hold The value of this flag becomes 1 when a COM pin ground short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
3	ERDS1G	S1 Ground Short Error Hold The value of this flag becomes 1 when a S1 pin ground short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
2	ERDS2G	S2 Ground Short Error Hold The value of this flag becomes 1 when a S2 pin ground short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
1	ERDS3G	S3 Ground Short Error Hold The value of this flag becomes 1 when a S3 pin ground short error occurred. This bit remains at 1 until it is reset by the ERRST bit.
0	ERDS4G	S4 Ground Short Error Hold The value of this flag becomes 1 when a S4 pin ground short error occurred. This bit remains at 1 until it is reset by the ERRST bit.

(18) BIST Register 0 (RDC3ALnBIST0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0044_H

Value after reset: $0200\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	ADB3TH[1:0]		—	—	—	ERCVP2D	—	—	—	CBSP2D
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BSTF	—	—	—	—	BISTCD[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.29 RDC3ALnBIST0 Register Contents

Bit Position	Bit Name	Function
31 to 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25, 24	ADB3TH[1:0]	AD BIST Threshold Setting Sets the threshold for ADBIST determination. b25 b24 Threshold for determination 0 0 ±16 LSB 0 1 ±8 LSB 1 0 ±32 LSB (default) 1 1 ±64 LSB
23 to 21	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
20	ERCVP2D	Two Paths Conversion Error BIST Disable Selects whether or not to include two paths conversion error in the conversion error BIST. 0: Two paths conversion error is included in the conversion error BIST (default). 1: Two paths conversion error is not included in the conversion error BIST
19 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	CBSP2D	Two Paths Conversion BIST Disable Selects whether or not to include two paths conversion in the conversion BIST. 0: Two paths conversion is included in the conversion BIST (default). 1: Two paths conversion is not included in the conversion BIST.
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	BSTF	BIST Flag This flag indicates whether a BIST is running or not. A BIST is running if the flag is 1, and another BIST cannot be executed while the flag remains 1.
7 to 4	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
3 to 0	BISTCD[3:0]	BIST Result Store The result of BIST is stored in these bits (see **Table 49.30**).

[BIST Result Store Bits]

The results of BIST executed by the BCON[3:0] bits are stored in the BISTCD[3:0] bits. The relation between the BCON[3:0] and BISTCD[3:0] are shown in **Table 49.30**.

Table 49.30 Contents of BCON[3:0] and BISTCD[3:0]

Bits for Selecting the BIST to be Executed BCON[3:0]				Bits where the result of BIST is Stored BISTCD[3:0]				
b3	b2	b1	b0	b3	b2	b1	b0	Contents Indicated by BISTCD[3:0]
0	0	0	0	0	0	0	0	BEXE is disabled. BISTCD[3:0] = 0000 is stored without any determination.
0	0	1	0	0	0	1	0	The result of sum-of-squares amplitude error detection BIST (low side) was passed.
				1	1	1	1	The result of sum-of-squares amplitude error detection BIST (low side) was failure.
0	0	1	1	0	0	1	1	The result of sum-of-squares amplitude error detection BIST (high side) was passed.
				1	1	1	1	The result of sum-of-squares amplitude error detection BIST (high side) was failure.
0	1	0	0	0	1	0	0	The result of the ADBIST was passed.
				1	1	1	1	The result of the ADBIST was failure.
0	1	0	1	0	1	0	1	The result of the angle conversion BIST1 (0°) was passed.
				1	1	1	1	The result of the angle conversion BIST1 (0°) was failure.
0	1	1	0	0	1	1	0	The result of the angle conversion BIST2 (45°) was passed.
				1	1	1	1	The result of the angle conversion BIST2 (45°) was failure.
0	1	1	1	0	1	1	1	The result of the angle conversion BIST3 (270°) was passed.
				1	1	1	1	The result of the angle conversion BIST3 (270°) was failure.
1	0	0	0	-	-	-	-	This combination is not allowed.
1	0	0	1	1	0	0	1	The result of the resolver signal error detection BIST was passed.
				1	1	1	1	The result of the resolver signal error detection BIST was failure.
1	0	1	0	1	0	1	0	The result of the resolver signal disconnect detection BIST (cosine side) was passed.
				1	1	1	1	The result of the resolver signal disconnect detection BIST (cosine side) was failure.
1	0	1	1	1	0	1	1	The result of the resolver signal disconnect detection BIST (sine side) was passed.
				1	1	1	1	The result of the resolver signal disconnect detection BIST (sine side) was failure.
1	1	0	0	1	1	0	0	The result of the conversion error BIST was passed.
				1	1	1	1	The result of the conversion error BIST was failure.
1	1	0	1	1	1	0	1	The result of the power short error BIST was passed.
				1	1	1	1	The result of the power short error BIST was failure.
1	1	1	0	1	1	1	0	The result of the ground short error BIST was passed.
				1	1	1	1	The result of the ground short error BIST was failure.
1	1	1	1	-	-	-	-	This combination is not allowed.

(19) BIST Register 1 (RDC3ALnBIST1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0048_H

Value after reset: $0200\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—		—	—	—	—	—	—	—	BISTCL
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BEXE	—	—	—	—	BCON[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 49.31 RDC3ALnBIST1 Register Contents

Bit Position	Bit Name	Function
31 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	BISTCL	BIST Result Clear Writing 1 to this bit clears the result of the BIST (BISTCD[3:0]) to 0. This bit is returned to 0 after one or two clock cycles have elapsed following it being set to 1.
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	BEXE	BIST Execution This signal is used for starting a BIST. Setting this bit to 1 leads to execution of a BIST. This bit is returned to 0 after one or two clock cycles have elapsed after having been set to 1. Select the BIST to be executed by the combination of values in BCON[3:0] (see **Table 49.32**).
7 to 4	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
3 to 0	BCON[3:0]	Executing BIST Setting Selects the BIST to be executed (see **Table 49.32**).

[Executing BIST Setting]

The BIST to be executed is selected by the combination of values in the BCON[3:0]. The combination of values in BCON[3:0] and corresponding BIST to be executed are shown in **Table 49.32**.

Table 49.32 BIST to be Selected by BCON[3:0] (1/2)

b3	b2	b1	b0	BIST to be Executed
0	0	0	0	BEXE is disabled.
0	0	0	1	Setting prohibited
0	0	1	0	Error detection BIST: sum-of-squares amplitude error detection BIST (low side)
0	0	1	1	Error detection BIST: sum-of-squares amplitude error detection BIST (high side)
0	1	0	0	ADBIST
0	1	0	1	Angle conversion BIST: target angle 1 (0°)

Table 49.32 BIST to be Selected by BCON[3:0] (2/2)

b3	b2	b1	b0	BIST to be Executed
0	1	1	0	Angle conversion BIST: target angle 2 (45°)
0	1	1	1	Angle conversion BIST: target angle 3 (270°)
1	0	0	0	This combination is not allowed.
1	0	0	1	Error detection BIST: resolver signal error detection BIST
1	0	1	0	Error detection BIST: resolver signal disconnect detection BIST (cosine side)
1	0	1	1	Error detection BIST: resolver signal disconnect detection BIST (sine side)
1	1	0	0	Error-detection BIST: conversion error BIST
1	1	0	1	Error-detection BIST: power short error BIST
1	1	1	0	Error-detection BIST: ground short error BIST
1	1	1	1	This combination is not allowed.

(20) Excitation Setting Register (RDC3ALnREF)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+$004C_H$

Value after reset: $0A0F\ 0410_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EXFS2[3:0]				REFXS	—	SENS	EXIO	—	—	EXF15	EXFS[4:0]				
Value after reset	0	0	0	0	1	0	1	0	0	0	0	0	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—			—	—	—	—	—	—	—	PLSNFS	—	—	—	
Value after reset	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Table 49.33 RDC3ALnREF Register Contents

Bit Position	Bit Name	Function
31 to 28	EXFS2[3:0]	Excitation Frequency Selection 2 The frequency of the excitation signal is determined by the combination of values in the EXFS2 and EXFS bits. Note that the frequency is fixed to 15 kHz when EXF15 = 1. The output frequency settings are listed in **Table 49.34**.*2
27	REFXS	Excitation Component Extraction Function 0: Excitation component extraction function is disabled. 1: Excitation component extraction function is enabled (default)
26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25	SENS	Sensor Selection Selects the required sensor. 0: Use the DC resolver*1 1: Use the VR resolver (default)
24	EXIO	RSO/COM Input/Output Switching Switches input and output through the RSO and COM pins. 0: Excitation signal input from outside (default) 1: Excitation voltage output
23, 22	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
21	EXF15	Excitation Signal 15 kHz Setting Selects whether to set the frequency of the excitation signal to 15 kHz or not. 0: The frequency of the excitation signal is the value set by the EXFS[4:0] bits and EXFS2[3:0] bits. 1: The frequency of the excitation signal is 15 kHz.
20 to 16	EXFS[4:0]	Excitation Signal Frequency Select The frequency of the excitation signal is determined by the combination of values in the EXFS2 and EXFS bits. Note that the frequency is fixed to 15 kHz when EXF15 = 1. See **Table 49.34** for the frequencies to be output.*2
15 to 5	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
4	PLSNFS	Excitation Extraction Noise Filter Selects the noise filter for the excitation component extraction circuit. 0: The noise filter is not used. 1: The noise filter is used.
3 to 0	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Note 1. DC resolver is selected when EXIO = 1 and SENS = 0.

Note 2. When the frequency of the excitation signal is 22 kHz or above, do not set the CVEDS bit to 0. When the user sets the frequency by using the EXFS[4:0] and EXFS2[3:0] bits, set the EXF15 bit to 0.

Table 49.34 Excitation Frequency Settings

EXFS [4:0] \ EXFS2 [3:0]	Frequency of the Excitation Signal Output (kHz)															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
0	Setting prohibited															
1																
2																
3	40.00	20.00	26.67	30.00	32.00	33.33	34.29	35.00	35.56	36.00	36.36	36.37	36.92	37.14	37.33	37.50
4	32.00	16.00	21.33	24.00	25.60	26.67	27.43	28.00	28.44	28.80	29.09	29.33	29.54	29.71	29.87	30.00
5	26.67	13.33	17.78	20.00	21.33	22.22	22.86	23.33	23.70	24.00	24.24	24.44	24.62	24.76	24.89	25.00
6	22.86	11.43	15.24	17.14	18.29	19.05	19.59	20.00	20.32	20.57	20.78	20.95	21.10	21.22	21.33	21.43
7	20.00	10.00	13.33	15.00	16.00	16.67	17.14	17.50	17.78	18.00	18.18	18.33	18.46	18.57	18.67	18.75
8	17.78	8.89	11.85	13.33	14.22	14.81	15.24	15.56	15.80	16.00	16.16	16.30	16.41	16.51	16.59	16.67
9	16.00	8.00	10.67	12.00	12.80	13.33	13.71	14.00	14.22	14.40	14.55	14.67	14.77	14.86	14.93	15.00
10	14.55	7.27	9.70	10.91	11.64	12.12	12.47	12.73	12.93	13.09	13.22	13.33	13.43	13.51	13.58	13.64
11	13.33	6.67	8.89	10.00	10.67	11.11	11.43	11.67	11.85	12.00	12.12	12.22	12.31	12.38	12.44	12.50
12	12.31	6.15	8.21	9.23	9.85	10.26	10.55	10.77	10.94	11.08	11.19	11.28	11.36	11.43	11.49	11.54
13	11.43	5.71	7.62	8.57	9.14	9.52	9.80	10.00	10.16	10.29	10.39	10.48	10.55	10.61	10.67	10.71
14	10.67	5.33	7.11	8.00	8.53	8.89	9.14	9.33	9.48	9.60	9.70	9.78	9.85	9.90	9.96	10.00
15	10.00	5.00	6.67	7.50	8.00	8.33	8.57	8.75	8.89	9.00	9.09	9.17	9.23	9.29	9.33	9.38
16	9.41	4.71	6.27	7.06	7.53	7.84	8.07	8.24	8.37	8.47	8.56	8.63	8.69	8.74	8.78	8.82
17	8.89	4.44	5.93	6.67	7.11	7.41	7.62	7.78	7.90	8.00	8.08	8.15	8.21	8.25	8.30	8.33
18	8.42	4.21	5.61	6.32	6.74	7.02	7.22	7.37	7.49	7.58	7.66	7.72	7.77	7.82	7.86	7.89
19	8.00	4.00	5.33	6.00	6.40	6.67	6.86	7.00	7.11	7.20	7.27	7.33	7.38	7.43	7.47	7.50
20	7.62	3.81	5.08	5.71	6.10	6.35	6.53	6.67	6.77	6.86	6.93	6.98	7.03	7.07	7.11	7.14
21	7.27	3.64	4.85	5.45	5.82	6.06	6.23	6.36	6.46	6.55	6.61	6.67	6.71	6.75	6.79	6.82
22	6.96	3.48	4.64	5.22	5.57	5.80	5.96	6.09	6.18	6.26	6.32	6.38	6.42	6.46	6.49	6.52
23	6.67	3.33	4.44	5.00	5.33	5.56	5.71	5.83	5.93	6.00	6.06	6.11	6.15	6.19	6.22	6.25
24	6.40	3.20	4.27	4.80	5.12	5.33	5.49	5.60	5.69	5.76	5.82	5.87	5.91	5.94	5.97	6.00
25	6.15	3.08	4.10	4.62	4.92	5.13	5.27	5.38	5.47	5.54	5.59	5.64	5.68	5.71	5.74	5.77
26	5.93	2.96	3.95	4.44	4.74	4.94	5.08	5.19	5.27	5.33	5.39	5.43	5.47	5.50	5.53	5.56
27	5.71	2.86	3.81	4.29	4.57	4.76	4.90	5.00	5.08	5.14	5.19	5.24	5.27	5.31	5.33	5.36
28	5.52	2.76	3.68	4.14	4.41	4.60	4.73	4.83	4.90	4.97	5.02	5.06	5.09	5.12	5.15	5.17
29	5.33	Setting prohibited														
30	5.16															
31	5.00															

(21) Encoder Register 0 (RDC3ALnENC0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0050_H

Value after reset: $0000\ 0100_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	PHILTSL	OMGLTSL	—	—	PHILT	OMGLT	—	—	—	PHIERLK	XUVW[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	HYSS	—	—	REFZEN	CINTEN	ABEN	UVWEN	ZEN	EINTEN
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.35 RDC3ALnENC0 Register Contents (1/2)

Bit Position	Bit Name	Function
31, 30	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
29	PHILTSL	PHI Output Fixing Select This bit is used to select fixing or non-fixing of the angle value output in the PHI[15:0] register bits in response to a trigger. 0: The value is not fixed. 1: The value is fixed in response to a trigger. Trigger signals: The triggers are writing of 1 to the PHILT bit or a transition of the phi_latch_trg signal to the high level.
28	OMGLTSL	Angular Velocity Output Fixing Select This bit is used to select fixing or non-fixing of the angular velocity value output in the OMG[31:0] register bits in response to a trigger. 0: The value is not fixed. 1: The value is fixed in response to a trigger. Trigger signals: The triggers are writing of 1 to the OMGLT bit or a transition of the omg_latch_trg signal to the high level.
27, 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25	PHILT	PHI Output Fixing Trigger Writing of 1 to this bit can serve as the trigger for fixing of the PHI output. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
24	OMGLT	Angular Velocity Output Fixing Trigger Writing of 1 to this bit can serve as the trigger for fixing of the angular velocity output. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
23 to 21	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
20	PHIERLK	PHI Fixing Selection on Error This bit selects whether or not the PHI and Angular Velocity output are fixed at the time of an error (ERHD = 1). 0: The PHI and Angular Velocity output are not fixed 1: The PHI and Angular Velocity output are fixed at the time of an error.

Table 49.35 RDC3ALnENC0 Register Contents (2/2)

Bit Position	Bit Name	Function
19 to 16	XUVW[3:0]	Encoder Pulse Pole Selection Selects the number of poles for the output of the encoder pulses. b19-b16 U phase V phase W phase 1111 X1 X1 X1 1110 X1 X1 X1 1101 X1 X1 X1 1100 X1 X1 X1 1011 X1 X1 X1 1010 X10 X1 X1 1001 X9 X1 X1 1000 X8 X1 X1 0111 X1 X1 X1 0110 X6 X1 X1 0101 X5 X1 X1 0100 X4 X4 X4 0011 X3 X3 X3 0010 X2 X2 X2 0001 X1 X1 X1 0000 X1 X1 X1
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	HYSS	Hysteresis Output Select Selects whether to output the encoder pulse signal and compare flag signal through the hysteresis circuit or without going through it.*1 0: Outputs the encoder pulse signal and compare flag signal through the hysteresis circuit. 1: Outputs the encoder pulse signal and compare flag signal without going through the hysteresis circuit.
7, 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5	REFZEN	Excitation zero-crossing(refzpls) interrupt output Enable 0: Output is disabled. 1: Output is enabled
4	CINTEN	Angle compare match interrupt enable 0: Interrupt is disabled. 1: Interrupt is enabled.
3	ABEN	A/B Phase Output Enable 0: Output is disabled. 1: Output is enabled.
2	UVWEN	Encoder Pulse U/V/W Phase Output Enable Controls output of the U, V, and W phases of the encoder pulse signal. 0: Output of the encoder pulse signals as the external output signals ENCU, ENCV, or ENCW is disabled and they are fixed to 0. 1: Output of the encoder pulse signals as the external output signals ENCU, ENCV, or ENCW is enabled.
1	ZEN	Z Phase Output and Z Phase Signal Interrupt Enable 0: Output is disabled. 1: Output is enabled.
0	EINTEN	RDC Error Interrupt Enable 0: Interrupt is disabled. 1: Interrupt is enabled.

Note 1. When output through the hysteresis circuit is selected (HYSS = 0), the RD angle conversion resolution should be 12 bits (MAXV = 001).

(22) Encoder Register 1 (RDC3ALnENC1)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0054_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PHI[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	ENCA	ENCB	ENCZ	ENCU	ENCV	ENCW
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.36 RDC3ALnENC1 Register Contents

Bit Position	Bit Name	Function
31 to 16	PHI[15:0]	PHI[15:0] The digitally output PHI angle is stored in these bits with a 16-bit width. PHI[15](MSB) = 180°, PHI[0] (LSB) These bits are in the scope of control by the PHIERLK bit.
15 to 6	Reserved	When read, the value after reset is returned.
5	ENCA	Encoder Pulse A Phase This bit indicates the current state of the A-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
4	ENCB	Encoder Pulse B Phase This bit indicates the current state of the B-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
3	ENCZ	Encoder Pulse Z Phase This bit indicates the current state of the Z-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
2	ENCU	Encoder Pulse U Phase This bit indicates the current state of the U-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
1	ENCV	Encoder Pulse V Phase This bit indicates the current state of the V-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
0	ENCW	Encoder Pulse W Phase This bit indicates the current state of the W-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.

(23) Encoder Register 2 (RDC3ALnENC2)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0058_H

Value after reset: 0000 $xxxx_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PHIAD1[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Value after reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.37 RDC3ALnENC2 Register Contents

Bit Position	Bit Name	Function
31 to 16	PHIAD1[15:0]	conversion Loop1 Output PHI[15:0] The digitally output PHI angle from conversion loop1 is stored in these bits with a 16-bit width. PHIAD1[15](MSB) = 180°, PHIAD1[0] (LSB)
15 to 0	Reserved	The read value is undefined.

(24) Angular Velocity Register (RDC3ALnOMG)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+005C$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OMG[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OMG[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.38 RDC3ALnOMG Register Contents

Bit Position	Bit Name	Function
31 to 0	OMG[31:0]	Angular Velocity [31:0] Indicates the amount of change in phi within the measuring period (selected by OMGPTC[1:0]). The resolution is 25-bits. • The notation is two's complement [0] (the LSB) corresponds to 0.07min^{-1} and [24] corresponds to 1171875min^{-1}. The value in [31:25] represents the sign. These bits are in the scope of control by the PHIERLK bit (fixed to 0 min^{-1}).

(25) MNT Signal Register (RDC3ALnETC)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0060_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	SINPK[12:0]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	COSPK[12:0]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.39 RDC3ALnETC Register Contents

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned.
28 to 16	SINPK[12:0]	SINMNT Excitation Peak Indicates the value of SINMNT latched by the excitation peak trigger signal (trg_ad) from the excitation timer (ET). Specifically, the bits are read as the difference between the voltage of SINMNT at the excitation peak and the COM voltage, expressed as a two's complement. SINMNT excitation peak voltage = d'(SINPK[12:0])*AFCVCC/4096+0.5* AFCVCC
15 to 13	Reserved	When read, the value after reset is returned.
12 to 0	COSPK[12:0]	COSMNT Excitation Peak Indicates the value of COSMNT latched by the excitation peak trigger signal (trg_ad) from the excitation timer (ET). Specifically, the bits are read as the difference between the voltage of COSMNT at the excitation peak and the COM voltage, expressed as a two's complement. COSMNT excitation peak voltage = d'(COSPK[12:0])*AFCVCC/4096+0.5* AFCVCC

(26) Test Bus Register (RDC3ALnTBUS)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0064_H

Value after reset: 0000 $XXXX_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	OMGPTC [1:0]		—	—	—	—	—	DATSEL[6:0]						
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[15:0]															
Value after reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.40 RDC3ALnTBUS Register Contents

Bit Position	Bit Name	Function
31, 30	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
29, 28	OMGPTC [1:0]	Angular Velocity Measuring Period Select Selects the period for measuring the amount of change in angle by the angular velocity measuring circuit. b29 b28 0 0: 12.8 µs (default) 0 1: 51.2 µs 1 0: 102.4 µs 1 1: 204.8 µs
27 to 23	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
22 to 16	DATSEL[6:0]	RDC Data Select Outputs the RDC internal data to DATA[15:0] (see **Table 49.41**).
15 to 0	DATA[15:0]	RDC DATA The data selected by the DATSEL[6:0] bits of the RDC3ALnTBUS register are stored in these bits.

[RDC Data Selection Bits]

Table 49.41 Testbus Data Selection

DATSEL[6:0]	Output Signal (Internal Signal for Evaluation)	Output Destination testbus(X:X) (DATA[X:X])
011.1011	12bit SAR-ADC output	[11:0]
010.1111	Control variation value [7:0] in conversion loop0.	[7:0]
010.1110	Square sum amplitude integral value in sum-of-squares amplitude error circuit (value is updated every excitation period)	[15:0]
010.1101	Square sum value in sum-of-squares amplitude error circuit (value is updated every 1 us)	[15:0]
001.1101	Offset value of common of COSMNT from 0.5*AFCVCC Offset = d'DATA[9:0]*AFCVCC/4096 (V) (2's complement)	[9:0]
001.1100	Offset value of common of SINMNT from 0.5*AFCVCC Offset = d'DATA[9:0]*AFCVCC/4096 (V) (2's complement)	[9:0]
001.1010	cosine signal acquired by ADC COSMNT-COM=d'DATA[12:0]*AFCVCC/4096 (V) (2's complement)	[12:0]
001.1001	sine signal acquired by ADC SINMNT-COM=d'DATA[12:0]*AFCVCC/4096 (V) (2's complement)	[12:0]

The selected data are read from the DATA[15:0] bits.

(27) ET Control Register (RDC3ALnETEN)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+006C$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	REFZSL[1:0]		—	REFETSL	—	—	—	ZCSTRG	—	—	CMPEN	IREN	DREN	ADTEN	ZCES	CNTEN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R/W	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CNT[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.42 RDC3ALnETEN Register Contents (1/2)

Bit Position	Bit Name	Function
31, 30	REFZSL[1:0]	Excitation Zero-Crossing Pulse Select Selects the output method of excitation zero-crossing pulse interrupt signal. b31 b30 Method of output 0 0 A high-level pulse signal is output for one CCLK cycle on the rising and falling edges (0 → 1, 1 → 0) of the excitation zero-crossing signal. 0 1 A high-level pulse signal is output for one CCLK cycle on the rising edges (0 → 1) of the excitation zero-crossing signal. 1 0 A high-level pulse signal is output for one CCLK cycle on the falling edges (1 → 0) of the excitation zero-crossing signal. 1 1 No pulse signals are output.
29	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
28	REFETSL	Excitation Zero-Crossing Select Selects the excitation zero-crossing signal for use in the excitation timer (ET). 0: The zero-crossing of excitation signal from analog comparator 1: The zero-crossing of extracted excitation signal When 1 is selected, a signal with a short or long cycle may be output during the excitation extraction follow-up operation.
27 to 25	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
24	ZCSTRG	Software Trigger This is the software trigger for output of the zero-crossing signal from the excitation timer. 0: No operation. 1: Outputs a trigger. CAUTION: Writing 1 to this bit outputs one CCLK cycle trigger pulse. Reading this bit always returns 0.
23, 22	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
21	CMPEN	Compare Match Function Enable Enables and disables the compare match function. 0: Disables the compare match function. 1: Enables the compare match function.
20	IREN	Interrupt Request Enable Enables and disables interrupt requests. 0: Disables the output of interrupt. 1: Enables the output of interrupt.

Table 49.42 RDC3ALnETEN Register Contents (2/2)

Bit Position	Bit Name	Function
19	DREN	DMA Request Enable Enables and disables DMA requests. 0: Disables the DMA requests. 1: Enables the DMA requests.
18	ADTEN	A/D Conversion Start Trigger Enable Enables and disables the AD conversion start trigger. 0: Disables the A/D conversion start trigger. 1: Enables the A/D conversion start trigger.
17	ZCES	Zero-Crossing Signal Edge Select Selects the edge on the zero-crossing signal to be detected. 0: Detects the rising edge on the zero-crossing signal. 1: Detects the falling edge on the zero-crossing signal.
16	CNTEN	Counter Operation Enable This is the count enable signal for the period measurement timer and the event timer. 0: Operation of the period measurement timer and the event timer is stopped. The value of the reload register is read into the ET counter. 1: The period measurement timer and the event timer are operated.
15 to 0	CNT[15:0]	ET Counter Register The data from the ET counter is stored in these bits.

(28) ET Capture Register (RDC3ALnETCAP)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: **<RDC3ALn_base>+0070$_H$**

Value after reset: 0000 FFFF$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAP[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMP[15:0]															
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.43 RDC3ALnETCAP Register Contents

Bit Position	Bit Name	Function
31 to 16	CAP[15:0]	ET Capture [1]This register captures the data from the ET zero-crossing period measurement counter on detection of a zero-crossing signal. [2] This register captures the data from the ET zero-crossing period measurement counter on a match of the values in the counter and that in the compare match register, when compare match is enabled. [3] In other cases, this register holds the previous captured value.
15 to 0	CMP[15:0]	ET Compare [1]This register captures the value from the ET zero-crossing period measurement counter into CAP[15:0] on a match of the values in the counter and that in this register, and initializes the counter to 0000$_H$. [2] An excitation timer interrupt request is issued in the cycle after one in which the value in the ET zero-crossing period measurement counter matches that of this register.

(29) ET Zero-Crossing Counter Register (RDC3ALnETMCNT)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+0074_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CNT[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RLD[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.44 RDC3ALnETMCNT Register Contents

Bit Position	Bit Name	Function
31 to 16	CNT[15:0]	Zero-Crossing Period Measurement Counter The value in the zero-crossing period measurement counter is stored in these bits.
15 to 0	RLD[15:0]	ET Reload The initial value for the ET counter is set in these bits in 16 bits. The value should be 0002_H or more (setting of 0000_H and 0001_H are prohibited).

(30) Digital Operation Register 0 (RDC3ALnDCUR0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+007C$_H$

Value after reset: 0002 0020$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—		—		—	—	—	—	—	—	—	—		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—			PGAIVSL[1:0]		—		—	—	—	—	AVE4[1:0]		—	
Value after reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R	R

Table 49.45 RDC3ALnDCUR0 Register Contents

Bit Position	Bit Name	Function
31 to 12	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
11, 10	PGAIVSL[1:0]	PGA Inversion Function Setting Selects the timing of PGA inversion.*1 b11 b10 Inversion timing 0 0 No PGA inversion (default) 0 1 When the excitation cross occurs after the phi output exceeds the threshold angle 1 0 When the AD input sin / cos switching occurs after the phi output exceeds the threshold angle. 1 1 When the excitation cross occurs after the phi output exceeds the threshold angle, and then the sin / cos switching of the AD input occurs
9 to 4	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
3, 2	AVE4[1:0]	Averaging Selection This bit selects the averaging method in the operation. b3 b2 0 0 Averaging0(default) 0 1 Averaging1 Use this setting if the excitation frequency is less than 30 kHz. 1 0 Averaging2 Use this setting if the excitation frequency is 30 kHz or higher. 1 1 no averaging
1, 0	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Note 1. When writing 1 to the KIRST bit, set the PGAIVSL bit to 00 in advance. After 1 has been written to the KIRST bit, wait for at least the settling time before setting the PGAIVSL bits to the desired value.

(31) 12-Bit SAR-ADC Digital Circuit Block Setting Register 0 (RDC3ALnADSTD0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+$00A8_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	ADCALCK[1:0]		—	—	—	—	—		—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Table 49.46 RDC3ALnADSTD0 Register Contents

Bit Position	Bit Name	Function
31 to 12	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
11, 10	ADCALCK[1:0]	Calibration setting Selects the ADC calibration setting. b11 b10 00: Setting0 01: Setting1 10: Setting2 11: Setting3
9 to 0	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

(32) 12-Bit SAR-ADC Digital Circuit Block Setting Register 1 (RDC3ALnADSTD1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+00AC$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	ADCALFG	—	—	—	—	—	—	—	ADCALST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	ADSFBMD	ADSFBIN[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.47 RDC3ALnADSTD1 Register Contents

Bit Position	Bit Name	Function
31 to 25	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
24	ADCALFG	Calibration Processing Flag This flag indicates that an ADC calibration is running. It returns 0 on completion of the calibration.
23 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	ADCALST	ADC Calibration Start This bit returns to 0 after one or two cycles have elapsed following it being set to 1. Setting 1 to this bit starts ADC calibration within 2 milliseconds.
15 to 13	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
12	ADSFBMD	Software BIST Execution Signal Set this bit to 1, when running the ADC software BIST.
11 to 0	ADSFBIN[11:0]	Software BIST Value Setting conversion value at the time of ADC software BIST (12-bit width)

(33) Error Detection Register 3 (RDC3ALnDIAG3)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+$00B0_H$

Value after reset: 2000 0200_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SQHTH[15:0]															
Value after reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SQLTH[15:0]															
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.48 RDC3ALnDIAG3 Register Contents

Bit Position	Bit Name	Function
31 to 16	SQHTH[15:0]	Sum-of-Squares Amplitude Upper Threshold Sets the upper threshold for values of the integrated sum-of-squares amplitude. A value exceeding this is detected as sum-of-squares amplitude error. The user can set this value freely based on **Table 49.49**.
15 to 0	SQLTH[15:0]	Sum-of-Squares Amplitude Lower Threshold Sets the lower threshold for values of the integrated sum-of-squares amplitude. A value falling below this is detected as sum-of-squares amplitude error. The user can set this value freely based on **Table 49.49**.

Table 49.49 Relationship between the Resolver Signal (MNT Signal) Amplitude, Excitation Frequency, and Values of the Integrated Sum-of-Squares Amplitude

excitation frequency (kHz)→	5kHz	7.5kHz	10kHz	12.5kHz	15kHz	17.5kHz	20kHz
MNT signal amplitude ↓							
0.1 × AFCVCC (Vpp)	254	169	128	104	83	72	63
0.2 × AFCVCC (Vpp)	1032	692	520	417	341	296	255
0.3 × AFCVCC (Vpp)	2304	1533	1156	921	771	649	582
0.4 × AFCVCC (Vpp)	4104	2719	2052	1638	1364	1169	1031
0.5 × AFCVCC (Vpp)	6435	4296	3222	2583	2152	1847	1601
0.6 × AFCVCC (Vpp)	9230	6127	4595	3685	3067	2633	2294
0.7 × AFCVCC (Vpp)	12567	8379	6282	5041	4177	3577	3144
0.8 × AFCVCC (Vpp)	16420	10942	8167	6574	5471	4684	4096
0.9 × AFCVCC (Vpp)	20761	13855	10355	8281	6909	5918	5212

(34) Error Detection Register 4 (RDC3ALnDIAG4)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+00B4$_H$

Value after reset: 0007 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SQCNT[6:0]							—	—	—		—	SQCTH[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Table 49.50 RDC3ALnDIAG4 Register Contents

Bit Position	Bit Name	Function
31 to 15	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
14 to 8	SQCNT[6:0]	Sum-of-Squares amplitude error Counter Value These bits hold the counter value of the excitation period which has exceeded the threshold for judging the integral of the sum-of squares specified by the SQHTH[15:0] and SQLTH[15:0] bits.
7 to 3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2 to 0	SQCTH[2:0]	Sum-of-Squares Amplitude Error Excitation Counts Threshold Selects the number of excitation periods in which abnormal amplitudes may be generated in the judgment of integrated sum-of-squares amplitude errors. The number of times set in these bits being exceeded is judged to represent an integrated sum-of-squares amplitude error. b2 b1 b0 0 0 0: 8 times 0 0 1: 1 time 0 1 0: 2 times 0 1 1: 3 times 1 0 0: 4 times 1 0 1: 16 times 1 1 0: 32 times 1 1 1: 64 times

(35) Automatic ROM Table Correction Register 1 (RDC3ALnROMCOR1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ALn_base>+$00BC_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	ROMBSTEN	—	—	—	—	—	—	—	—	—	—	—	ROMBST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W

Table 49.51 RDC3ALnROMCOR1 Register Contents

Bit Position	Bit Name	Function
31 to 13	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
12	ROMBSTEN	Automatic ROM Table Correction Enable This bit selects whether or not the result of ROM automatic correction is used. 0: The result of Automatic ROM Table correction is not used. 1: The result of Automatic ROM Table correction is used.
11 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	ROMBST	Automatic ROM Table Correction Start Setting this bit to 1 starts Automatic ROM Table Correction. This bit returns to 0 after a wait of one or two clock cycles following it being set to 1.

49.1.3 Specifications of the RDC Functions

49.1.3.1 Tracking Loops

The following describes the operating principles of the RDC3AL module. This R/D converter module uses the tracking method to convert analog resolver signals to digital signals (R/D conversion). The tracking loop runs at 20 MHz. When the excitation signal f(t) is input to the excitation coil, f(t) • sinθ and f(t) • cosθ are output from the resolver according to the angle (θ) of the resolver rotor. These signals are input to the RDC3ALnS2-RDC3ALnS4 and RDC3ALnS1-RDC3ALnS3 pins, respectively. These signals are amplified by PGA, converted to digital values by built-in ADC, and input to the multiplier. At the same time, cos ϕ (or sin ϕ) is generated by passing the accumulator output through COS ROM (or SIN ROM) and is fed back to the multiplier. Then the subtraction is performed.

f(t) • (sin θ • cos ϕ - cos θ • sin ϕ)

= f(t) •sin (θ - ϕ)

≈ f(t) • (θ - ϕ)

The result is converted to 1-bit digital value by the comparator (CMP). The excitation component f(t) is removed in the synchronous detection circuit to obtain the control variation ε = θ - ϕ. The negative feedback control over the entire digital circuits provides feedback so that the control variation becomes zero. When θ = ϕ, the analog angle information from the resolver has been converted to digital angle ϕ (16-bit wide). **Figure 49.3** describes the PI compensator and accumulator.

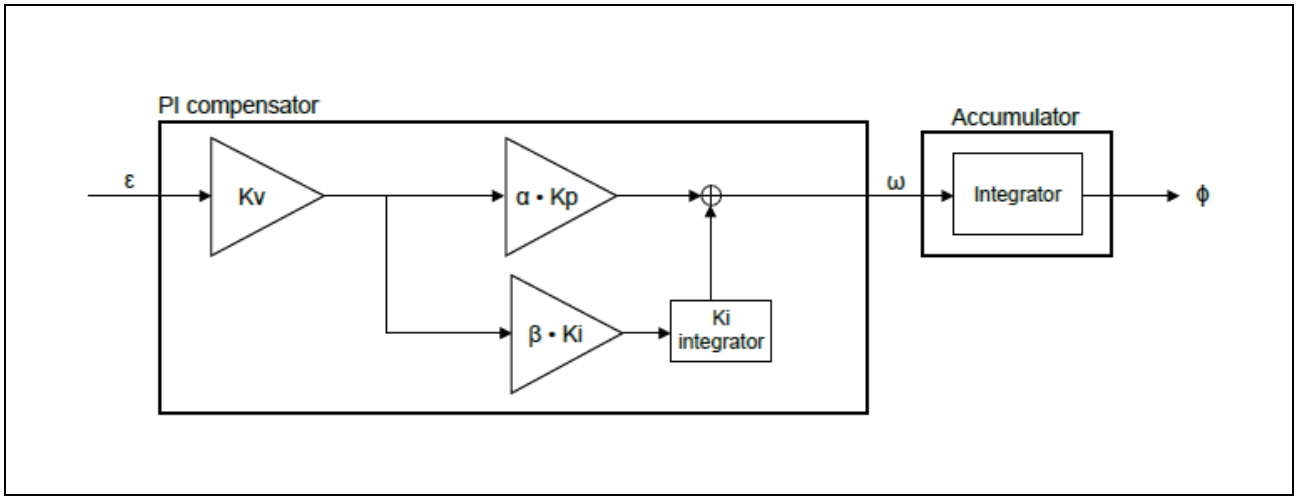


Figure 49.3 PI Compensator and Accumulator

The PI compensator converts the control variation according to the following formula, and passes the result to the accumulator circuit.

ω = (α • Kp + (β • Ki)/(s • T)) • Kv • ε

Kv, Kp, Ki: control coefficients that can be set in a register

α, β: fixed values

s: Laplace variable

T: Integration time constant

ω: PI compensator output, angular velocity information

The accumulator circuit calculates the angle ϕ based on the angular velocity information ω.

(1) PI Compensator Bandwidth Setting Function

This RDC can be set from six different bandwidths (five fixed and one auto-adjusted) using the registers. In addition, coefficients in the PI compensator can be configured in detail by setting the BWCS bit in the RDC3ALnPI0 register to 0.

For further details, refer to the section on the RDC3ALnPI0 register.

(2) Forced Gain Control Function (AGCON)

The forced gain control function(AGCON) is designed to improve the tracking performance when the resolver angle deviates

significantly from the R/D converted angle in situations such as after a reset. The forced gain control state is entered when any of the following conditions is met:

[Conditions for starting AGCON]

1. Release from the reset state
2. The recovery from a resolver signal error
3. The recovery from a resolver signal disconnect error
4. The start of angular conversion BIST or conversion error BIST
5. The end of sum-of-squares amplitude error detection BIST, ADBIST, angular conversion BIST, resolver signal error BIST, disconnection error BIST, conversion error BIST, power/ground short error BIST
6. The end of detection of a power/ground short error
7. 1 being written to the KIRST bit of the RDC3ALnDIAG1 register

Forced gain control function is applied for approximately 5 ms*1. If one of the above conditions is met again during the execution, the forced gain control state is entered again from this point and the period of its execution is extended by approximately 5 ms.

The value of the Kv gain becomes greater on entry to the forced gain state, so even if the resolver rotation angle signal θ and the R/D converter output angle signal ϕ have matched, ϕ may fluctuate significantly for approximately 1 ms. When the AGCD bit is set to 1, the forced gain state will not be entered even if a condition for starting forced gain control is met, except for release from the reset state. The initial Kv gain value depends on the type of BIST.

- Angular conversion BIST and conversion error BIST: Initial gain value = × 128 (the maximum value)
- When a short-period BIST (sum-of-squares amplitude error detection BIST, ADBIST, resolver signal error BIST, disconnection error BIST, or power/ground short error BIST) ends: Initial gain value = gain value specified by the AGST[3:0] bits
- When detection of a power/ground short error ends: Initial gain value = gain value specified by the AGST[3:0] bits

Since short-period BIST and power/ground short error detection can be completed in a short time, it is possible to start during angle conversion, and the angle tracking is maintained during execution. If the initial value of Kv gain at the end of short-period BIST and power/ground short error detection is too

large, the fluctuation of phi will become large, so the mechanism is such that the initial value can be set with a register. The Kv gain changes automatically during the AGCON period, but if it falls below the gain value specified by HKVLM[3:0] once, the gain never becomes greater than the value specified by HKVLM[3:0] after that. Also, it never becomes smaller than the value specified by LKVLM[3:0].

Forced gain control(AGCON) is subject to the following restrictions.

(1) When changing the setting of the AGCD bit, which sets the Forced gain control(AGCON) function valid / invalid, change the setting while the resolver is stationary. After that, write 1 to the KIRST bit. Not setting the KIRST bit to 1 may result in entry to the free-running state.

(2) Forced gain control is subject to restrictions on the angular velocity that allows operation. The upper-limits according to the maximum angular velocity/resolution setting (MAXV[2:0] bit setting) are as listed below.
When the resolution is equal to or less than 12 bits: 120000 min^{-1}
When the resolution is 13 bits: 60000 min^{-1}
When the resolution is 14 bits: 30000 min^{-1}
When the resolution is 16 bits: 7500 min^{-1}

Note 1. The timing value is when the CCLK is running at 40 MHz.

(3) Excitation Signal Source Selection Function

Without the excitation signal output from the RDC3ALnRSO pin and common voltage output from the RDC3ALnCOM pin, the R/D conversion can be performed using externally generated excitation signal input to pins RDC3ALnRSO and RDC3ALnCOM pins. When an externally input signal is used, set the EXIO bit in the RDC3ALnREF register to 0.

(4) Required Sensor Selection Function

The DC resolver signal (E • sinθ, E • cosθ) which does not contain excitation component can be used by setting the SENS bit in the RDC3ALnREF register to 0. When the DC resolver signal is used, the excitation signal outputs (RDC3ALnRSO, RDC3ALnCOM) and the excitation component extraction function are disabled.

Table 49.52 Relation between the EXIO and SENS Bits and the Resolver to be Used

EXIO	SENS	Resolver to be Used
0	0	Setting prohibited
0	1	VR Resolver,Brush-Less Resolver (external excitation)
1	0	DC resolver
1	1	VR Resolver,Brush-Less Resolver (internal excitation)

(5) Excitation Component Extraction Function

The excitation signals (RDC3ALnRSO, RDC3ALnCOM) and resolver signals (RDC3ALnS1 to RDC3ALnS4) are analog signals input to the RDC. If there is a phase difference between the excitation component (sine wave component) in the excitation signal line and that in the resolver signal line, it can cause an error in the angle conversion result in proportion to the phase difference. The phase difference between the resolver signal and excitation signal can be reduced by using the extracted excitation component contained in the resolver signal line for an angle conversion. When using an

external excitation signal by setting the EXIO bit in the RDC3ALnREF register to 0, extracted excitation components cannot be used if the difference between the electrical angle of the resolver and the RDC converted angle is large (such as during power-up or occurrence of error). Therefore, when using an external excitation signal, be sure to enter the external excitation signal into the RDC3ALnRSO, RDC3ALnCOM pins.

The excitation component extraction function automatically performs the following process; the excitation signal (RDC3ALnRSO, RDC3ALnCOM) is used when the difference between the resolver electrical angle and the R/D converted angle is large, and the extracted excitation component is used when the difference is small. The exact adjustment of the phase difference between excitation and resolver signals is not required because of this function. For successful operation of the excitation component extraction circuit, the excitation component phase deviation between the excitation signal (RDC3ALnRSO, RDC3ALnCOM) and the resolver signal (RDC3ALnS1 to RDC3ALnS4) should be within 30°.

(6) Maximum Angular Velocity Setting Function

This function can set the maximum angular velocity (resolution) that is capable of tracking operation by using the MAXV [2:0] bits in the RDC3ALnPI1 register. RDC operates at the set resolution without missing codes.

(7) Compare Match Interrupt

When the angle set in the CMPj register (j = 0 to 2) and the R/D converted angle match, a compare match interrupt request signal is generated. The compare match interrupt request signal is output when the CINTEN bit in the RDC3ALnENC0 register is set to 1. The bit width that is compared for a match is set using the MAXV [2:0] bits (maximum angular velocity selection) in the RDC3ALnPI1 register. The compare match interrupt request signal can be selected from either a compare match signal or a signal latching a compare match signal by using the IRS bit in the RDC3ALnPHICP0 register. When the IRS bit is set to 0, the compare match interrupt request signal becomes high when the R/D converted angle and the angle set in the CMPj register match, and becomes low when the values do not match. When the IRS bit is set to 1, the compare match interrupt request signal becomes high when the R/D converted angle and the angle set in the CMPj register match, and also the INTFLG[2:0] flag in the RDC3ALnPHICP0 register becomes 1. In this case, the request signal retains the high level even if the angles no longer match. When 1 is written to the INTCLR[2:0] bit in the RDC3ALnPHICP0 register while the R/D converted angle and the angle set in the CMPj register do not match, the request signal becomes low and the INTFLG[2:0] flag becomes 0. If 1 is written to the INTCLR[2:0] bit while the R/D converted angle and the angle set in the CMPj register match, the request signal remains high and the INTFLG[2:0] flag does not become 0.

Turning hysteresis on by setting the HYSS bit in the RDC3ALnENC0 register to 0 prevents chattering of the output of the compare match interrupt signal and Z phase when the angle output near the target bit for comparison is not stable.This hysteresis circuit can only be used when 12-bit resolution is selected (MAXV[2:0] = 001_B).

Output of the PHI comparison flag is in the scope of control by the PHIERLK bit.

Figure 49.4 shows the timing chart of the compare-match interrupt request signal when hysteresis is off (HYSS = 1).

Figure 49.5 shows the timing chart of the compare-match interrupt request signal when hysteresis is on (HYSS=0).

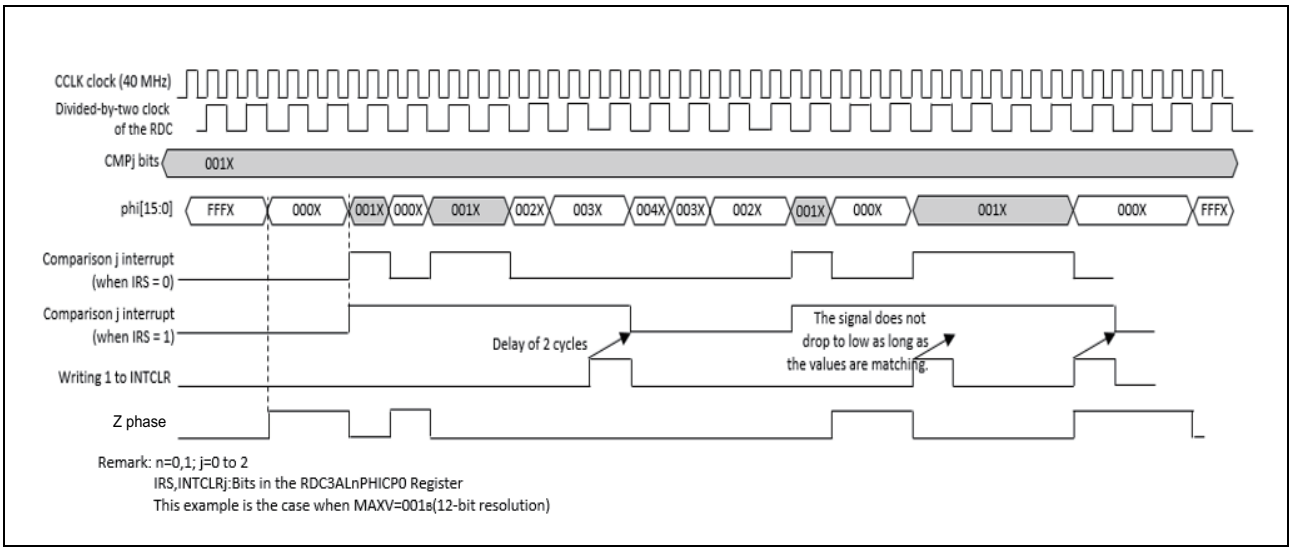


Figure 49.4 Timing Chart for the Compare Match Interrupt Request Signal when Hysteresis is Off(HYSS = 1)

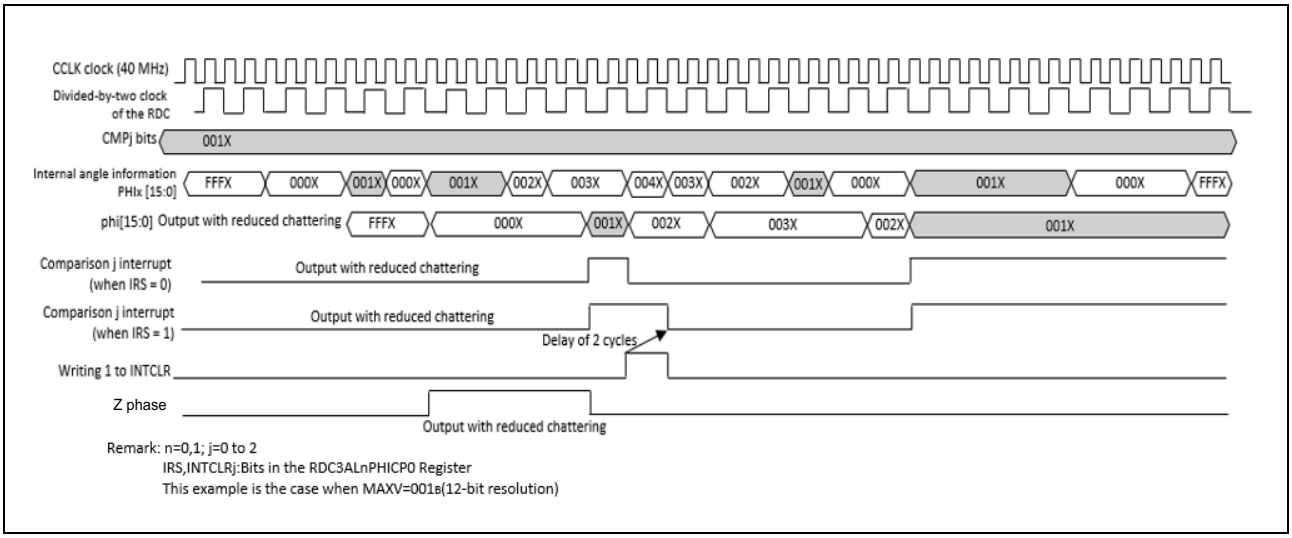


Figure 49.5 Timing Chart for the Compare Match Interrupt Request Signal when Hysteresis is On (HYSS=0)

(8) Encoder Pulse Output Function

This function enables to output encoder pulse signals (A, B, Z, U, V, W phases). The Z-phase interrupt signal becomes high while the R/D converted angle is 0º. The bit width compared for a match is set using the MAXV [2:0] bits in the RDC3ALnPI1 register as it is for the compare match interrupt request signal. The encoder pulse signal is output when the corresponding bit in the RDC3ALnENC0 register is set to 1 (enables output).

Whether the encoder pulse signals are to be output through the hysteresis circuit or without going through it can be selected using the HYSS bit in the RDC3ALnENC0 register. This hysteresis circuit can only be used when 12-bit resolution is selected (MAXV[2:0] = 001_B).

The encoder pulse output is in the scope of control by the PHIERLK bit.

Figure 49.6 shows the waveforms of encoder phase pulse operation when hysteresis is on and off.

See **Figure 49.4** and **Figure 49.5** for the z phase waveform when the angle output near the target bit for comparison is not stable.

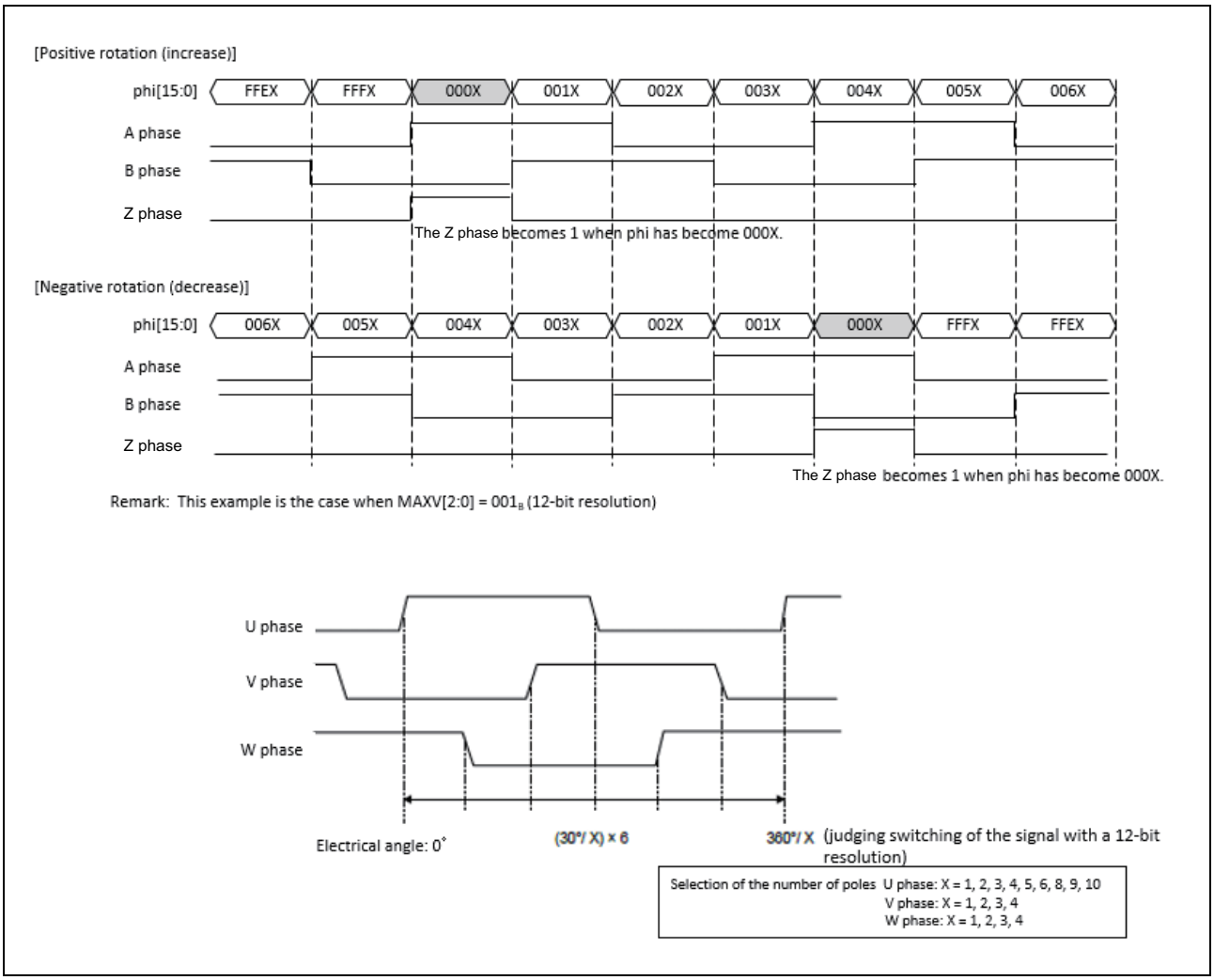


Figure 49.6 Waveforms of Encoder Phase Pulse Operation when Hysteresis is On and Off

(9) PHI Angular Velocity Information Reading Function

The angular velocity of the phi angle is read from the relevant register. The amount of change in the phi angle is measured over the period selected by the OMGPTC[1:0] bits, converted into the units of angular velocity (min^{-1}), and stored in the OMG[31:0] bits of the RDC3ALnOMG register. The angular velocity of phi (in min^{-1}) does not depend on the selected measuring period, but the maximum measurable angular velocity does. The angular velocity stored in the OMG[31:0] bit is updated every measuring period. The measuring period that can be set with OMGPTC [1: 0] can be changed even during angle conversion.

OMG[31:0] bits are in the scope of control by the PHIERLK bit (fixed to 0 min^{-1})

Table 49.53 Contents of OMGPTC[1:0] Bits

OMGPTC[1:0]	Measuring Period	Maximum Measurable Angular Velocity (min^{-1})
00	12.8µs	2,343,750
01	51.2µs	585,938
10	102.4µs	292,969
11	204.8µs	146,484

Note: This table shows the relation between the measuring period and the range of measurable angular velocity.

Table 49.54 OMG Bits and the PHI Angular Velocity (min^{-1})

Bit	Angular Velocity (min^{-1})
b31-25	Sign (0: +, 1: –)
b24	1,171,875
b23	585,937.5
b22	292,968.8
b21	146,484.4
b20	73,242.19
b19	36,621.09
b18	18,310.55
b17	9,155.27
b16	4,577.64
b15	2,288.82
b14	1,144.41
b13	572.20
b12	286.10
b11	143.05
b10	71.53
b9	35.76
b8	17.88
b7	8.94
b6	4.47
b5	2.24
b4	1.12
b3	0.56
b2	0.28
b1	0.14
b0	0.07

For example, the angular velocity is -164,795 min^{-1} if the result for angular velocity read from the OMG bits is $FFDB\ FFFF_H$.

Reading the angular velocity from a register requires the time taken by the register access. Accordingly, the angular velocity may have completely changed at the actual point where reading is completed. It has a function to fix the angular velocity value at the timing when you want to read the angular velocity. Whether or not the angular velocity is fixed can be set with the OMGLTSL bit of the RDC3ALnENC0 register. There are two types of triggers that fix the angular velocity: register write (OMGLT bit = 1 write) and external signal (omg_latch_trg) H pulse input.

49.1.3.2 Sine and Cosine Correction Function

(1) ADC Noise Elimination Function

This function eliminates noise from the values of the SINMNT and COSMNT signals obtained by A/D conversion. The converted values of the SINMNT and COSMNT signals change every 2 µs. The value of the MNT signal obtained from a conversion is compared with that from the previous conversion, and, if the gap between two values is greater than the threshold set in the GNCNS[2:0] bits, the value from the current session is judged to be noise, and the previous value is retained. It is also possible to compare the value of the MNT signal with those obtained the two previous times. (by setting the GNJSP bit to 1).

Figure 49.7 shows how noise is detected and removed from the SINMNT signal.

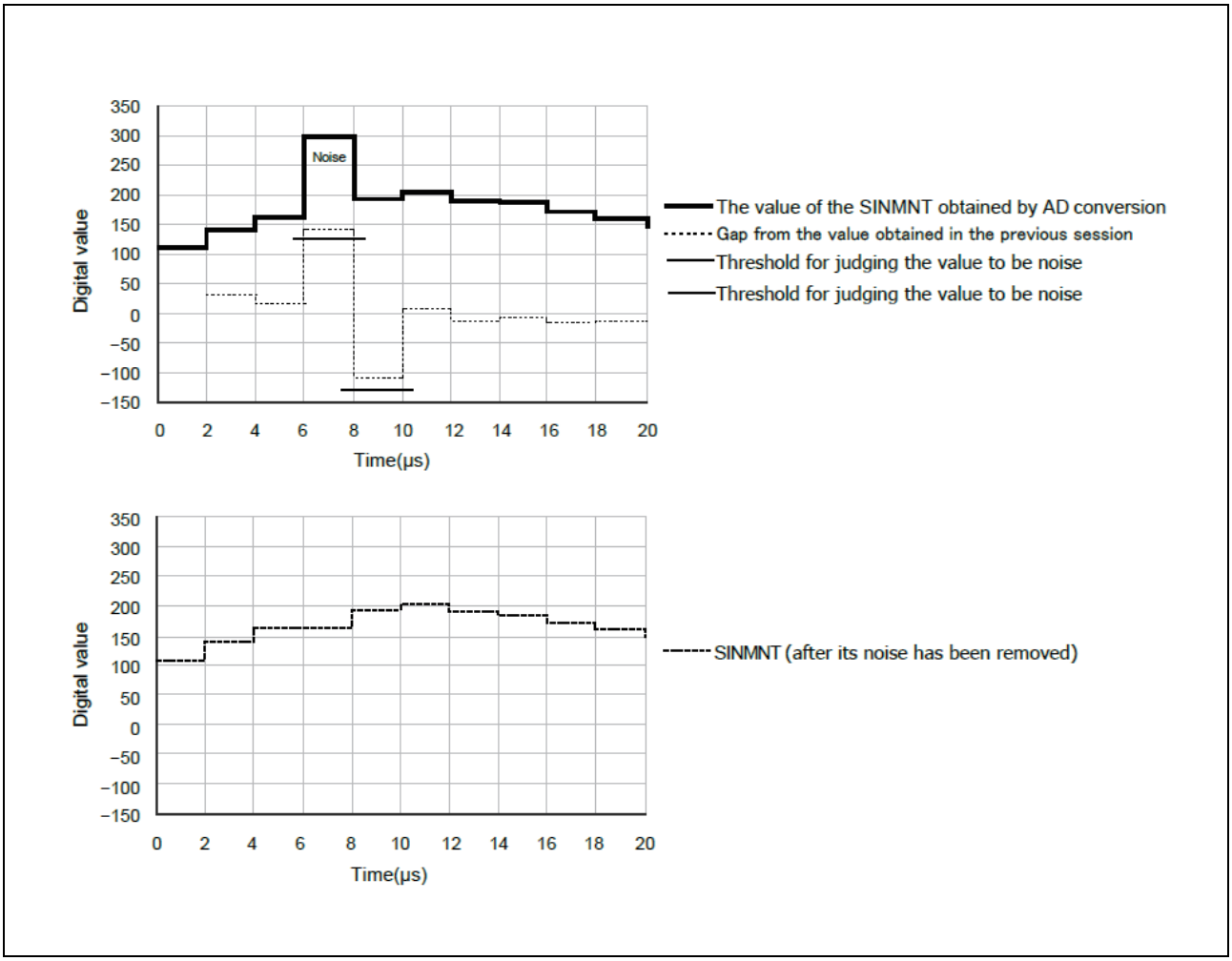


Figure 49.7 Judging and Eliminating Noise

If the result of A/D conversion becomes stuck at a value equivalent to the power supply voltage or the ground due to extremely strong noise, the gaps between the compared values may not exceed the thresholds and the result of acquiring noise will be output as it is. To avoid this, this macro is also equipped with a function to detect the value obtained by A/D conversion being stuck. If the result of A/D conversion is greater than 0.992×AFCVCC or smaller than 0.008×AFCVCC, the input is determined to be stuck, and the result from the previous conversion is retained.

Writing 1 to the GNCND bit disables the noise elimination function for the ADC. If it is disabled, results of A/D conversion are used in operations as they are, without being checked for noise.

The circuits which use the ADC output signal whose noise has been removed by this function are selected by the NSRSL bit.

NSRSL = 0: Use the ADC output signal of which noise has been removed only in the sine and cosine gain correction (default) circuits and the sine and cosine common offset correction circuits.

NSRSL = 1: Use the ADC output signal of which noise has been removed in the sine and cosine gain correction circuits, the sine and cosine common offset compensation circuits, and the angle conversion calculation (adder and subtractor) circuits.

(2) Sine and Cosine Gain Correction

Resolver errors or errors in the accuracy of components on the printed circuit board may lead to gaps between the amplitudes of the sine- and cosine-wave signals input to the R/D converter that lead to errors in the result of angle conversion by the RDC. In order to reduce errors in the results of conversion, the maximum amplitudes of the SINMNT and COSMNT are compared, and if there is a gap between the amplitudes, that of the COSMNT signal is automatically adjusted to have the same range as that of the SINMNT signal. The values after correction are used in operations. This function is only applicable to the values used internally. The SINMNT and COSMNT signals from the LSI chip are not adjusted.

If the resolver angle is fixed, the maximum amplitudes of the SINMNT and COSMNT signals cannot be compared. In this case, the resolver is required to go through at least half a rotation (electrical angle) to obtain signal values for comparison. Accordingly, when the RDC is ready to output results of conversion, the user needs to wait for the resolver to go through at least half a rotation (electrical angle) before writing 1 to the GNCST bit. The gain correction function will then be ready for use. Writing 1 to the GNCST bit before waiting for the required period may result in invalid correction value.

The correctable range limit expressed as a percentage can be set by the GNCLT [1: 0] bits. If the correction value exceeds the limit value, the limit value will be applied.

GNCLT[1:0] = 00_B: Limit ±20% (default)

GNCLT[1:0] = 01_B: Limit ±10%

GNCLT[1:0] = 10_B: Limit ±40%

GNCLT[1:0] = 11_B: Limit ±0% (no compensation)

Figure 49.8 below shows how the amplitude of COSMNT, which is initially smaller than that of SINMNT, is corrected to have the same amplitude as SINMNT.

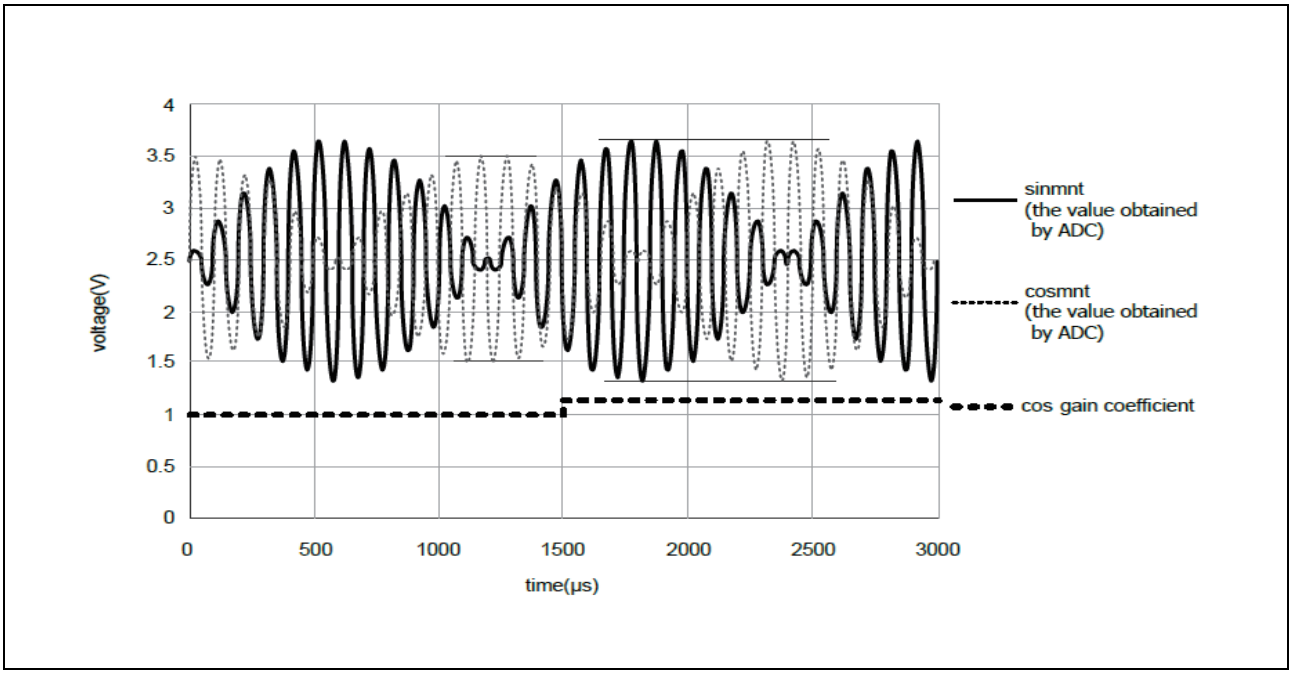


Figure 49.8 Correction to Make the Amplitudes Correspond

The timing of correcting the gain value is selected by the GNCSL[1:0] bits as follows;

- GNCSL[1:0] = 00_B
  No correction (the default value, 1024, is used as the value for correction)
- GNCSL[1:0] = 01_B
  The fixed value set in the GNCNM[11:0] bits is used as the value for correction.
- GNCSL[1:0] = 10_B
  The value calculated when the GNCST bit is set to 1 is used as the value for correction. The value from the calculation is retained.
  The GNCST bit can be set to 1 multiple times. In that case, set it after the resolver has rotated more than half a rotation (electrical angle) since it was set last time.
- GNCSL[1:0] = 11_B
  The value is updated at the time of z-phase output following GNCST being set to 1. The value is updated on every single rotation.

(3) Sine and Cosine Common Offset Correction

A resolver error or error in the accuracy of the components on the printed circuit board may lead to an offset from the original common level (0.5 × AFCVCC) for the common levels of the sine- and cosine-wave signals, which are input to the R/D converter. This may lead to errors in the results of angle conversion by the RDC. In order to reduce errors in the results of conversion, an offset of the common level of the SINMNT and COSMNT signals from original level is detected and automatically adjusted. The values after correction are used in operations. This function is only applicable to the values used internally. The SINMNT and COSMNT signals from the LSI chip are not adjusted.

If the resolver angle is fixed, the maximum amplitudes of the SINMNT and COSMNT signals cannot be compared. In this case, the resolver is required to go through half a rotation (electrical angle) to obtain signal values for comparison. Accordingly, when the RDC is ready to output the results of conversion, the user needs to wait for the resolver to go through at least half a rotation (electrical angle) before writing 1 to the GNCST bit. The common offset correction function will then be ready for use. Writing 1 to the GNCST bit before waiting for the required period may result in invalid correction values.

A limit can be set to the value for common offset correction by CMCLT[1:0] bits. If the value for correction value obtained from SINMNT and COSMNT is greater than the specified limit, the specified limit is applied.

- CMCLT[1:0]=00_B: limit ± 0.0312 × AFCVCC (approx. ± 150mV) (default)
- CMCLT[1:0]=01_B: limit ± 0.0156 × AFCVCC (approx. ± 78mV)
- CMCLT[1:0]=10_B: limit ± 0.125 × AFCVCC (approx. ± 625mV)
- CMCLT[1:0]=11_B: limit ± 0 × AFCVCC (± 0mV) (no correction)

Figure 49.9 below shows how the common offset of COSMNT and SINMNT are corrected to 2.5V (= 0.5 × AFCVCC).

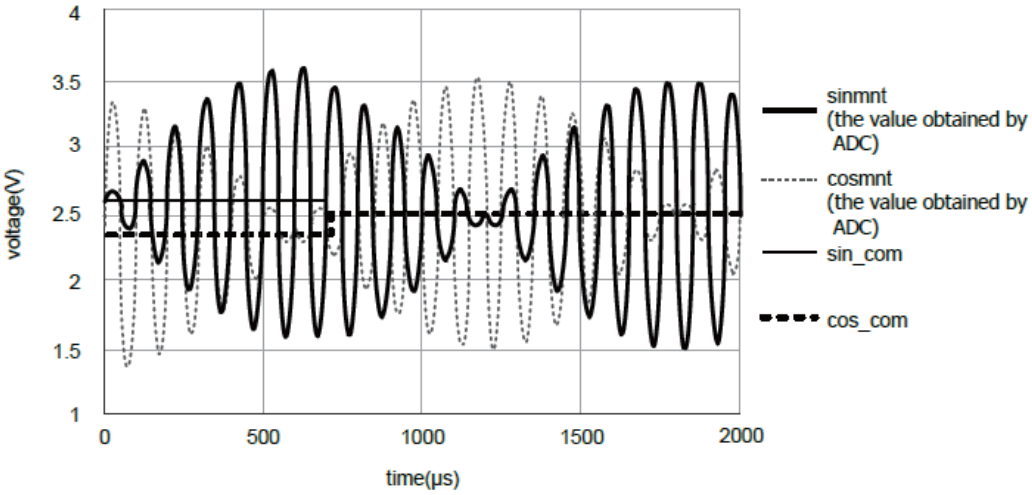


Figure 49.9 Correction of Common Offsets to 2.5V (= 0.5 × AFCVCC)

The timing of updating the value for common offset correction is selected by the CMCSL[1:0] bits as follows;

- CMCSL[1:0] = 00_B
  No correction (0 is used as the value for correction)
- CMCSL[1:0] = 01_B
  The value for correction set in CCOSN[9:0] is selected as the value for the cosine side.
  The value for correction set in CSOSN[9:0] is selected as the value for the sine side.
- CMCSL[1:0] = 10_B
  The calculated value is used as the value for correction.
  - When GNCSL[0] = 0, the value calculated when the GNCST bit is set to 1 is used as the value for correction.
    The value from the calculation is retained.
    The GNCST bit can be set to 1 multiple times. In that case, set it after the resolver has rotated more than half a rotation (electrical angle) since it was set last time.
  - When GNCSL[0] = 1, the value is updated at the time of z-phase output following GNCST being set to 1.
    The common value for correction is updated on every single rotation.
- CMCSL[1:0] = 11_B
  Setting prohibited

(4) SIN and COS Phase Correction Function

Resolver errors or errors in the accuracy of components on the printed circuits board may lead to deviations between the time (phase) of the sine- and cosine-wave signals input to the R/D converter. In order to reduce errors in the results of conversion, deviations between the phases of the SINMNT and

COSMNT signals are detected by comparing the timing of their excitation zero-crossing. Detected deviations are corrected by delaying the signal which has a phase in advance of the other. This function is only applicable to the values used internally. The SINMNT and COSMNT signals from the LSI chip are not adjusted.

When the power supply voltage is applied and the RDC initialization sequence is performed so that it is ready for use in angular tracking, write 1 to the register bit PHCST which gives an instruction to start phase correction of the sine and cosine signals. After 1 is written to this bit, application of the correction value starts.

Note that the obvious variations in amplitude between the sinmnt and cosmnt signals are required in order to compare the timing of their excitation zero-crossings. For this reason, this function automatically detects the phase deviation when the output phi angle is within ± 16.8° of either 45°, 135°, 225°, and 315°.

A limit can be set to the delay value for phase correction by PHCLT[1:0] bits. The correction value over the limit set by PHCLT [1: 0] will not be applied. If the value for correction obtained from sinmnt and cosmnt is greater than the specified limit, the specified limit is applied.

- PHCLT[1:0]=00_B: limit is 3 µs (default)
- PHCLT[1:0]=01_B: limit is 1 µs
- PHCLT[1:0]=10_B: limit is 6 µs
- PHCLT[1:0]=11_B: limit is 0 µs (no correction)

Figure 49.10 below shows the waveforms where the sinmnt signal delays from the cosmnt signal.

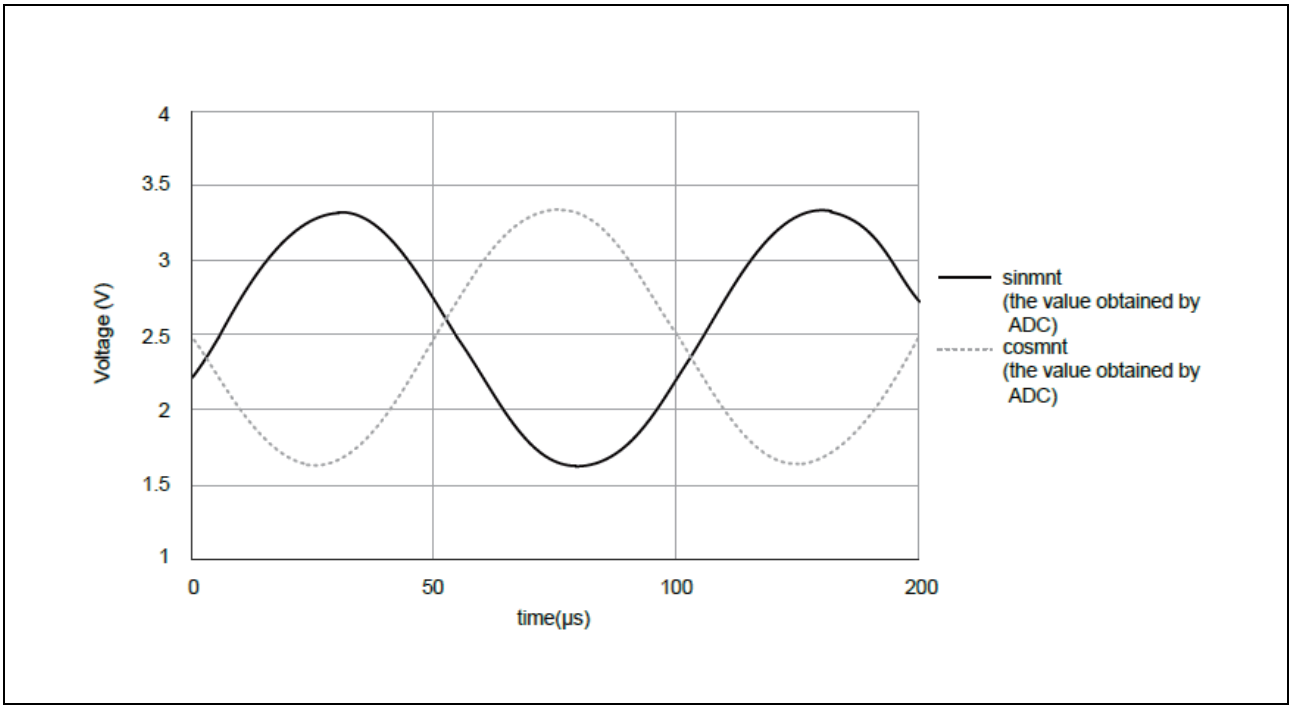


Figure 49.10 Signal with Delay

Figure 49.11 below shows the two synchronized waveforms obtained by detecting the advanced phase of the cosmnt signal and delaying.

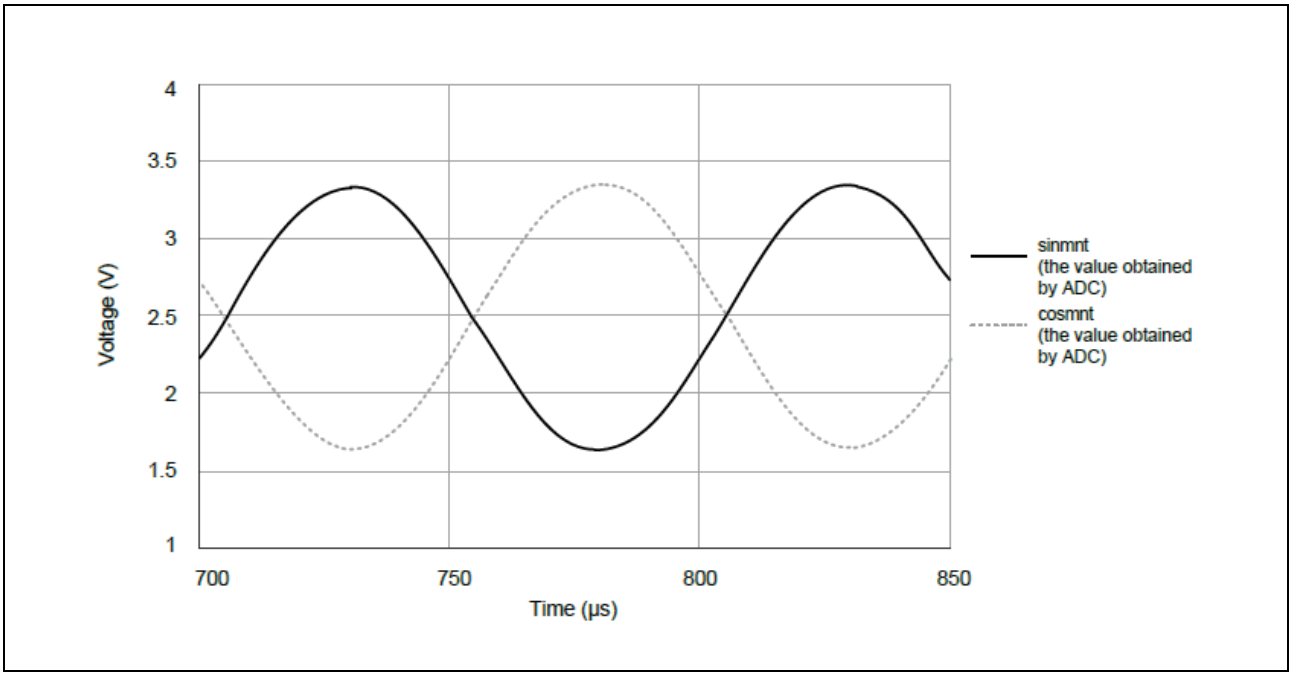


Figure 49.11 Phase Synchronization

The timing of correcting the phase deviation after writing 1 to the PHCST bit is select by the PHCSL[1:0] bits as follows;

- PHCSL[1:0] = 00_B
  No correction (default)
- PHCSL[1:0] = 01_B
  After writing 1 to the PHCST bit, the phase difference at 16 crossings of the excitation signal is constantly averaged to obtain the correction value.
- PHCSL[1:0] = 10_B
  Every time 1 is written to the PHCST bit, the phase difference at 16 crossings of the excitation signal is averaged once to obtain the correction value, and then the correction value is used.
- PHCSL[1:0] = 11_B
  The fixed correction values set by the PHSNM[5:0] bits (value for delay in the sine side) and the PHCNM[5:0] bits (value for delay in the cosine side) are used.

(5) Sine and Cosine Angle Correction Function

RDC has a function to correct the mounting angle error of the resolver with respect to the shaft of the motor and the error of sin and cos orthogonality of the resolver. Correction in this case is by adding fixed values for correction to the phi angles to be input to the individual SINROM and COSROM tables. These values are set in the SINPO[11:0] and COSPO[11:0] bits in the sine and cosine angle correction register. Set these bits to 0° for angle conversion BIST.

Sine angle correction bits SINPO[11:0] = 000_H

Cosine angle correction bits COSPO[11:0] = 000_H

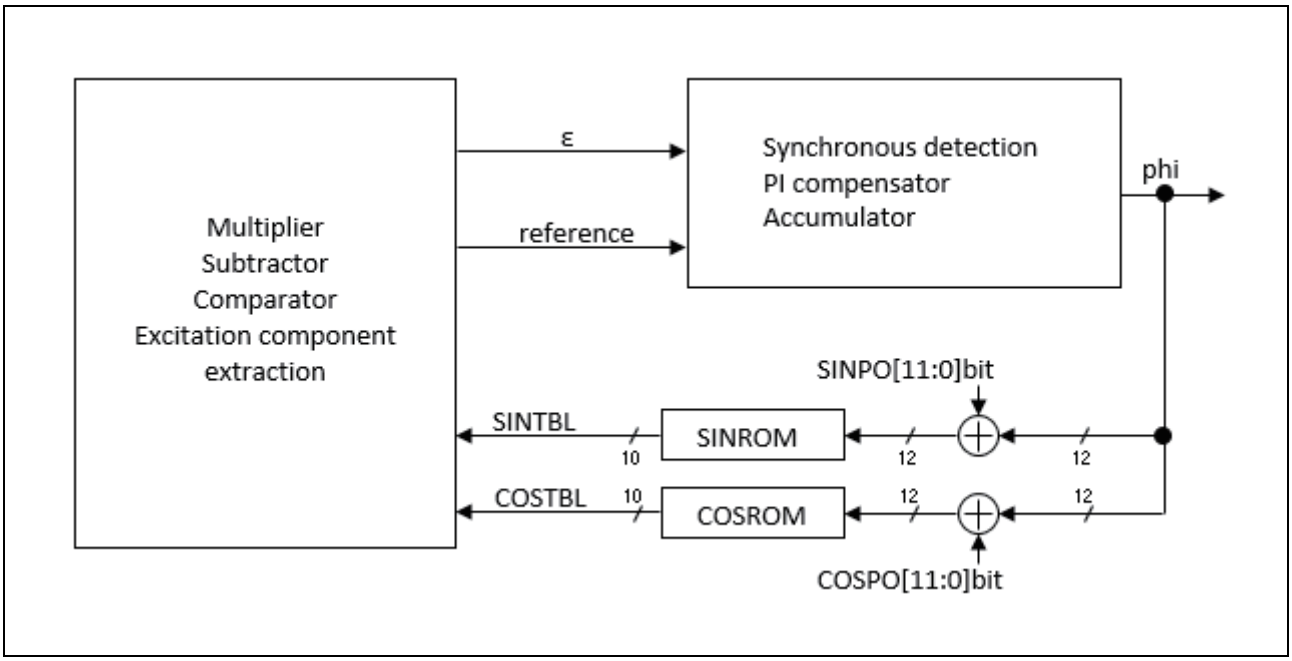


Figure 49.12 Structure of Sine and Cosine Angle Correction Circuit

49.1.3.3 Excitation Signal Output

(1) Excitation Signal Output (RDC3ALnRSO, RDC3ALnCOM)

Sine wave voltage signal generated by 7-bit D/A can be output from the RDC3ALnRSO pin. AFCVCC/2 (2.5V) common voltage can be output from the RDC3ALnCOM pin. Setting the EXIO bit in the RDC3ALnREF register to 0 (excitation signal input) disables the output and the RDC3ALnRSO and RDC3ALnCOM pins become input. The amplitude of the sine wave signal that is output from the RDC3ALnRSO pin is set in the EXOC[1:0] bits in the RDC3ALnATMNT0 register. The amplitude of the standard value is 0.4 × AFCVCC [Vp-p]. The excitation sine-wave frequency output from the RSO pin can be set in the range from 5 kHz to 40 kHz by using the EXFS[4:0], EXFS2[3:0], and EXF15 bits.

When operation with a DC resolver is selected (by setting the combination of values as EXIO = 1 and SENS = 0), the excitation signal outputs (RDC3ALnRSO, RDC3ALnCOM) are disabled.

(2) Automatic Amplitude Adjustment

In order to obtain an appropriate R/D conversion accuracy, the resolver signal input amplitude (monitor signal amplitude) needs to be controlled within a range of 0.32 × AFCVCC to 0.68 × AFCVCC [Vp-p]. The automatic amplitude adjustment function automatically adjusts the excitation signal output amplitude and the input gain resistance so that the monitor signal amplitude fits within the approximate range of 0.4 × AFCVCC to 0.6 × AFCVCC [Vp-p].

The automatic adjustment is performed on the excitation signal output amplitude and the input gain resistance. Priority can be specified by setting the EAAOD bit in the RDC3ALnATMNT0 register. When the EAATSP bit in the RDC3ALnATMNT0 register is set to 0, the automatic adjustment can be performed continuously. By setting the EAATSP bit to 1, the automatic adjustment can be stopped and the adjusted value at that time is retained. Setting the EAATSP bit to 0 restarts the automatic adjustment process.

The function monitors the amplitude with a 12-bit SAR-ADC, determines the size of amplitude based on the integrated sum-of-squares of the excitation amplitude for a period of 1 ms, and adjusts the amplitude. The determination threshold is approximately 3 Vp-p on the high side, and approximately 2 Vp-p on the low side. The interval for automatic amplitude adjustment is selectable by the SQJGT bit, being every 1 ms*1 when SQJGT bit is 0 (the default value) and every 10 ms*1 when the SQJGT bit is 1. It is also possible to use the excitation signal output settings and the input gain resistance settings that are specified in the register, without using the results of automatic adjustments.

Note 1. It is value for operation with CCLK running at 40 MHz.

49.1.3.4 Error Detection

(1) Error Detection

This function monitors and detects errors in resolver signal and in R/D conversion operations. If any of the errors listed in **Table 49.55** is detected, an RDC error interrupt request is generated, and the corresponding bit in the RDC3ALnDGOUT0 and 1 registers become 1. The following table lists factors that lead to error detection.

Table 49.55 Detected Error

Item	Detected Factor
Resolver signal error	• Excitation signal line disconnection (RDC3ALnRSO, RDC3ALnCOM) including contact failure • Excitation signal down (excitation signal output circuit down, short circuit between lines) • Short circuits between signal lines (RDC3ALnS1 and RDC3ALnS3, RDC3ALnS2 and RDC3ALnS4) • Resolver coil layer short
Resolver signal disconnect error	Resolver signal lines disconnection (RDC3ALnS1 to RDC3ALnS4) including contact failure
R/D conversion error	Excessive control variation (ε) of tracking control loop (negative feedback control system)
Two path comparison conversion error	Comparison of the conversion results from the two angle conversion loops
Resolver signal Power/ground short error	Short circuit to the power supply (power short error) and short circuit to the ground (ground short error) for the resolver signal lines
Square-sum amplitude error	Modulation, distortion, or noise on the amplitude of the sine and cosine resolver input signals.

(2) Resolver Signal Error Detection

This function detects disturbance in the resolver signal balance caused by an error in excitation signals input to the resolver. When a resolver signal error is detected, an RDC error interrupt request signal becomes high. A resolver signal error is detected if the monitor outputs (RDC3ALnSINMNT, RDC3ALnCOSMNT) fall below the threshold for approximately 220 μs.

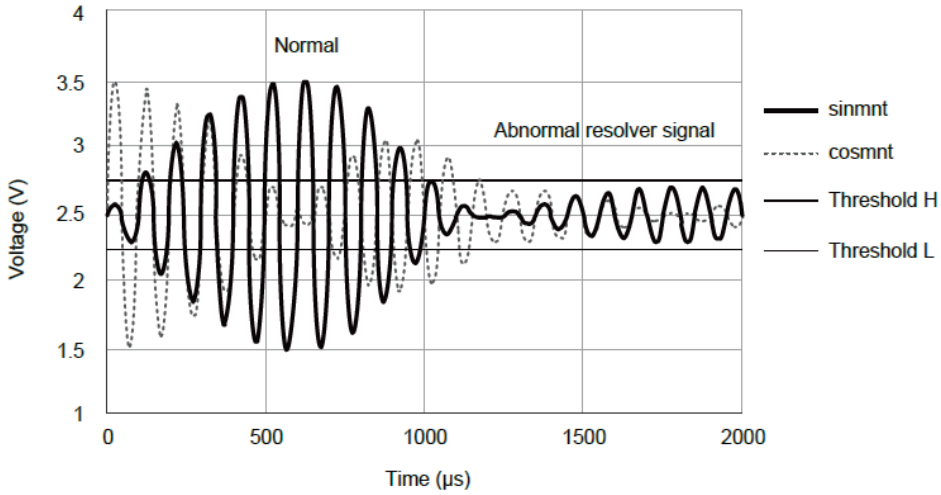


Figure 49.13 Monitor Signal Waveforms when the Resolver Signal is Abnormal

(3) Resolver Signal Disconnection Error Detection

This function detects disconnection (including contact failure) of the resolver signals (S1 to S4). When the configuration of the resolver signal input circuit in **Section 49.1.5.1, Resolver Signal Input (Differential) Circuit** is used, the DC level of monitor voltage (SINMNT, COSMNT) rises if a resolver signal line is disconnected, and the RDC error interrupt request signal becomes high. For a description of the relationship between register values and threshold values, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics.*

When operation with a VR resolver is selected (by setting values other than the combination of EXIO = 1 and SENS = 0), this function monitors the common levels of the monitored signals and determines any case of them exceeding the configured threshold to be a disconnection error. The threshold is set at 2.9V as the default and can be changed by the SGBTH[7:0] bits.

When operation with a DC resolver is selected (by setting the combination of values as EXIO = 1 and SENS = 0), this function monitors the DC level of the monitored signals and determines any case of them exceeding the configured threshold to be a disconnection error. The threshold is set at 4.25 V as the default and can be changed by the SGBDTH[7:0] bits.

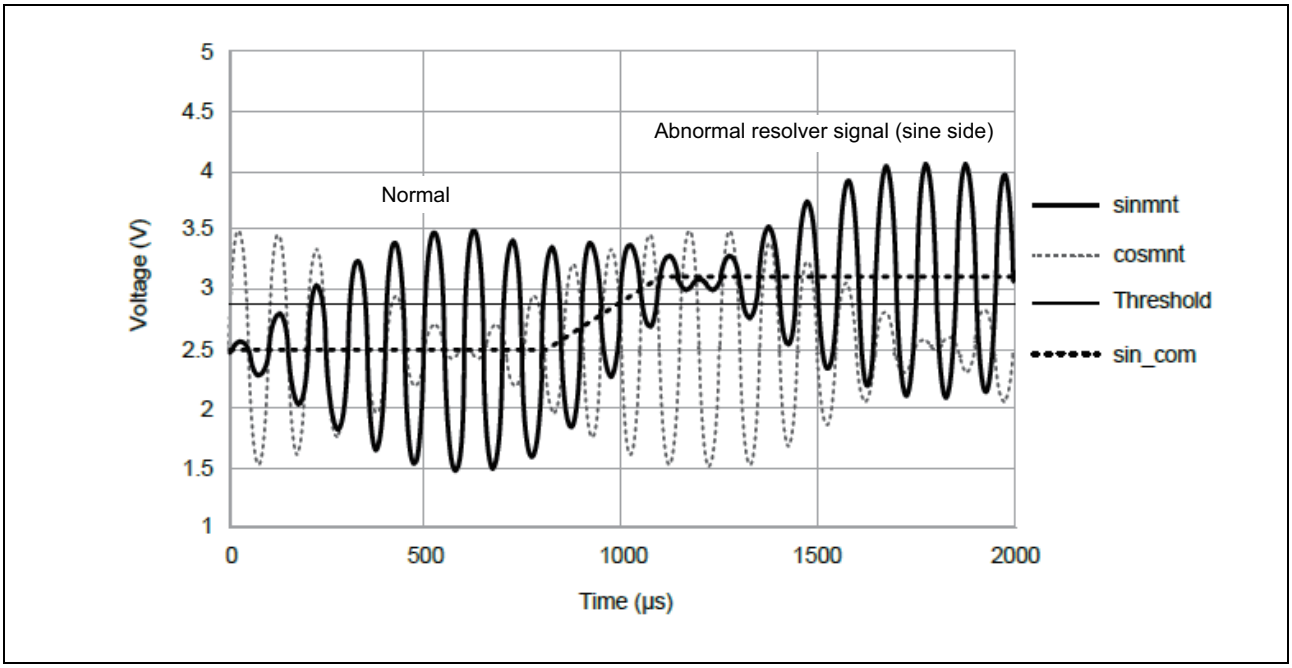


Figure 49.14 Monitor Signal Waveforms on Occurrence of Sin Signal Disconnection in VR Resolver

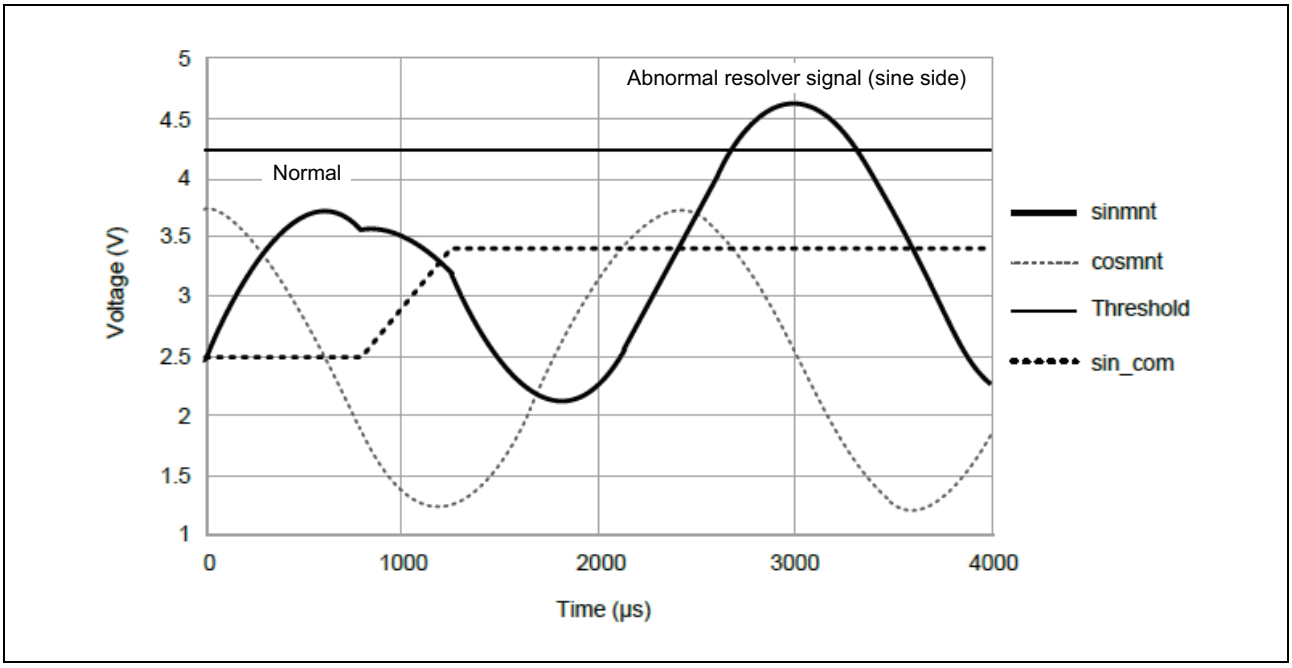


Figure 49.15 Monitor Signal Waveforms on Occurrence of Sin Signal Disconnection in DC Resolver

(4) R/D Conversion Error Detection

This function monitors the control variation in R/D conversion loop, and detects operation errors in the R/D conversion function. When an R/D conversion error is detected, the RDC error interrupt request signal becomes high. A control variation f(t) • (θ – φ) is considered excessive if the control variation rises above or falls below a configured threshold level. For a description of the relationship between

register values and threshold values, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics.*

An R/D conversion error is detected if the control variation stay excessive for more than 50% of the error determination time set in the EDPS[1:0] bits in the RDC3ALnDIAG1 register. The R/D conversion error detection circuit includes a circuit supporting high-speed rotation of a resolver and a circuit not supporting it. These circuits can be selected by using the CVEDS bit in the RDC3ALnDIAG1 register.

CVEDS = “0”:A circuit supporting high-speed rotation is selected. However, this setting is not allowed when the excitation frequency is set to 22 kHz or above.
When this setting is selected, set EDPS[1:0] to 10 or 11.

CVEDS = “1”:A circuit not supporting high-speed rotation is selected.

(5) Two Paths Comparison Conversion Error Detection

This function compares the results of angle conversion from two loops, and detects conversion errors in the circuit. The phi angle outputs of conversion loops 0 and 1 are compared, and if the difference between two angles is larger than the threshold, this is judged to be a two paths comparison conversion error. The threshold value is set by the P2ANT[1:0] bits.

(6) Resolver Signal Power/Ground Short Error Detection

This function detects power short errors (short circuits to the power supply) and ground short errors (short circuits to the ground) of the resolver signal lines RDC3ALnRSO, RDC3ALnCOM, RDC3ALnS1, RDC3ALnS2, RDC3ALnS3, and RDC3ALnS4. Note that if these errors are on the RDC3ALnRSO and RDC3ALnCOM pins, they are not correctly detected when the internal excitation signal is in use (EXIO = 1, SENS = 1) due to a conflict between the current from the short to the power supply or ground and the excitation current from the buffer. When the external excitation signal is in use (EXIO = 0) and a DC resolver is in use ((EXIO = 1, SENS = 0), errors on those pins can be detected.

Detection is also possible during an angle conversion and the angular tracking is continued even while detection of power/ground short error is running (for 78 µs). The timing to start this function is selected by the VGASL[1:0] bits as follows;

- VGASL[1:0] = 00_B (default)
  No detection performed.
- VGASL[1:0] = 01_B
  When the VGST bit is set to 1.
- VGASL[1:0] = 10_B
  Performed automatically every 10 ms.
  When this setting is selected, set the CVEDS bit to 1 to select a circuit not supporting high-speed rotation.
- VGASL[1:0] = 11_B
  No detection performed.

When the detection of power/ground short errors starts, the following operations are automatically performed by the circuit.

[Operation Sequence]

1. The RDC3ALnS1, RDC3ALnS2, RDC3ALnS3, and RDC3ALnS4 pins are disconnected from the PGA input circuit (**Figure 49.16**).
2. Each of the six resolver signal lines RDC3ALnCOM, RDC3ALnRSO, RDC3ALnS1, RDC3ALnS2, RDC3ALnS3, RDC3ALnS4 is selected, in sequence and in that order, for 13 µs*1. Detection finishes after all six signals have been selected, one after another, in a total of 78 µs.
3. The RDC3ALnS1, RDC3ALnS2, RDC3ALnS3, and RDC3ALnS4 pins are connected to the PGA input circuits.
4. The RDC enters the forced gain control state (for approx. 5 ms) and the angle is tracked. (If SAGD is set to 1, the RDC does not enter the forced gain control state.)

Note 1. It is value for operation with CCLK running at 40 MHz.

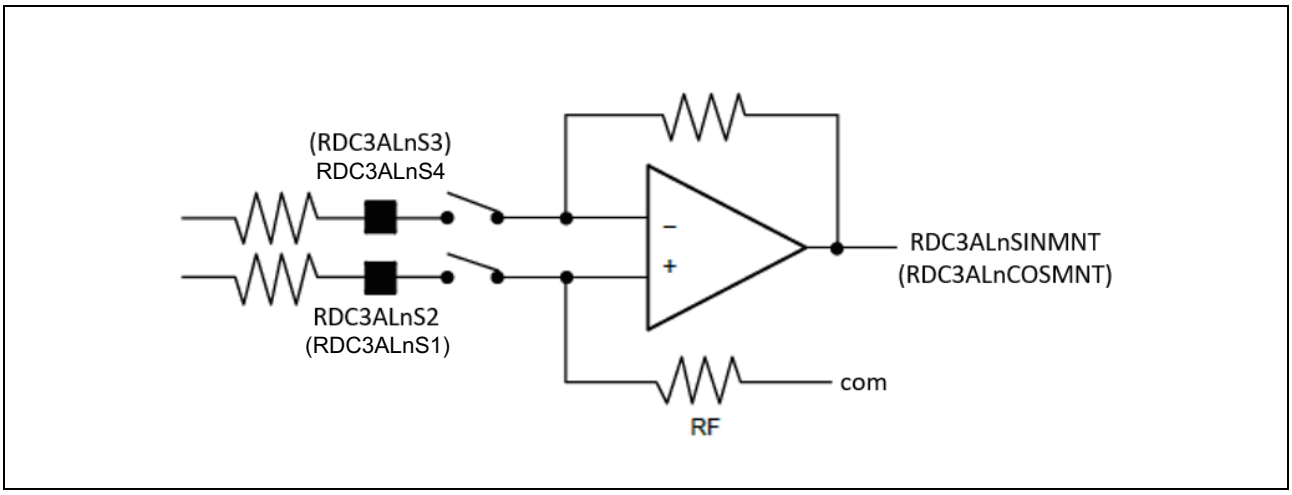


Figure 49.16 RDC3ALnS1, RDC3ALnS2, RDC3ALnS3, RDC3ALnS4 Pins on Detection of Power/Ground Short Error

While the detection of power/ground short errors is running (for 78 µs), the RDC3ALnS1, RDC3ALnS2, RDC3ALnS3,RDC3ALnS4 pins are disconnected from the PGA input circuit. However, tracking of the angle continues.

(7) Sum-of-Squares Amplitude Error Detection

This function detects modulation, distortion and noise in the amplitudes of the sine and cosine signals input from the resolver for each excitation cycle. This error detection function can be used for resolver input signals with excitation components, but cannot be used for DC resolver input signals without excitation components.

The sum-of-squares of the monitor signals (SINMNT, COSMNT) acquired in the ADC within the RDC are taken and integrated within the excitation period. Upper and lower threshold value are set for the integrated value, and the number of excitation cycles that exceed this threshold is counted. If the number exceeds the threshold for the counted value, it is output as a sum-of-squares amplitude error. The counted value can be read from the SQCNT[6:0] bits.

The procedure runs automatically, the user is only required to set the upper and lower threshold for the integrated sum-of-squares values in the SQHTH and SQLTH bits and the threshold counter value in the SQCTH. The counter values are cleared at the desired time by the writing to the SQERST bit. Setting the ERSQS bit to 0 enables the detection of sum-of-squares amplitude errors. After setting this bit to 0, clear the counted value by setting the SQERST bit to 1.

In checking for a power/ground short error, the excitation amplitude disappears for 78 µs, so the resulting error is counted once in sum-of-squares amplitude error detection. When checking for a power/ground short error by writing to the VGST bit when VGASL[1:0] = 01, set the ERSQS bit to 1 to switch sum-of-squares amplitude error detection off during the check. When automatic checking for power/ground short errors is to proceed at 10-ms intervals by setting of VGASL[1:0] = 10, clear the effect of this on the counting of sum-of-squares amplitude errors at least once per 10 ms by using the SQERST bit. If you want to check for power/ground short errors but do not require checking of sum-of-squares amplitude errors, leave the value of ERSQS as 1.

Since the excitation amplitude may also disappear when a BIST which can be executed during angle conversion proceeds, reset the counter value for abnormal values at the end of BIST by using the SQERST bit.

Figure 49.17 shows an example of waveforms where the amplitudes of the signals input to the resolver are reduced, the calculated value fell outside the threshold range three times, and a sum-of-squares amplitude error is generated.

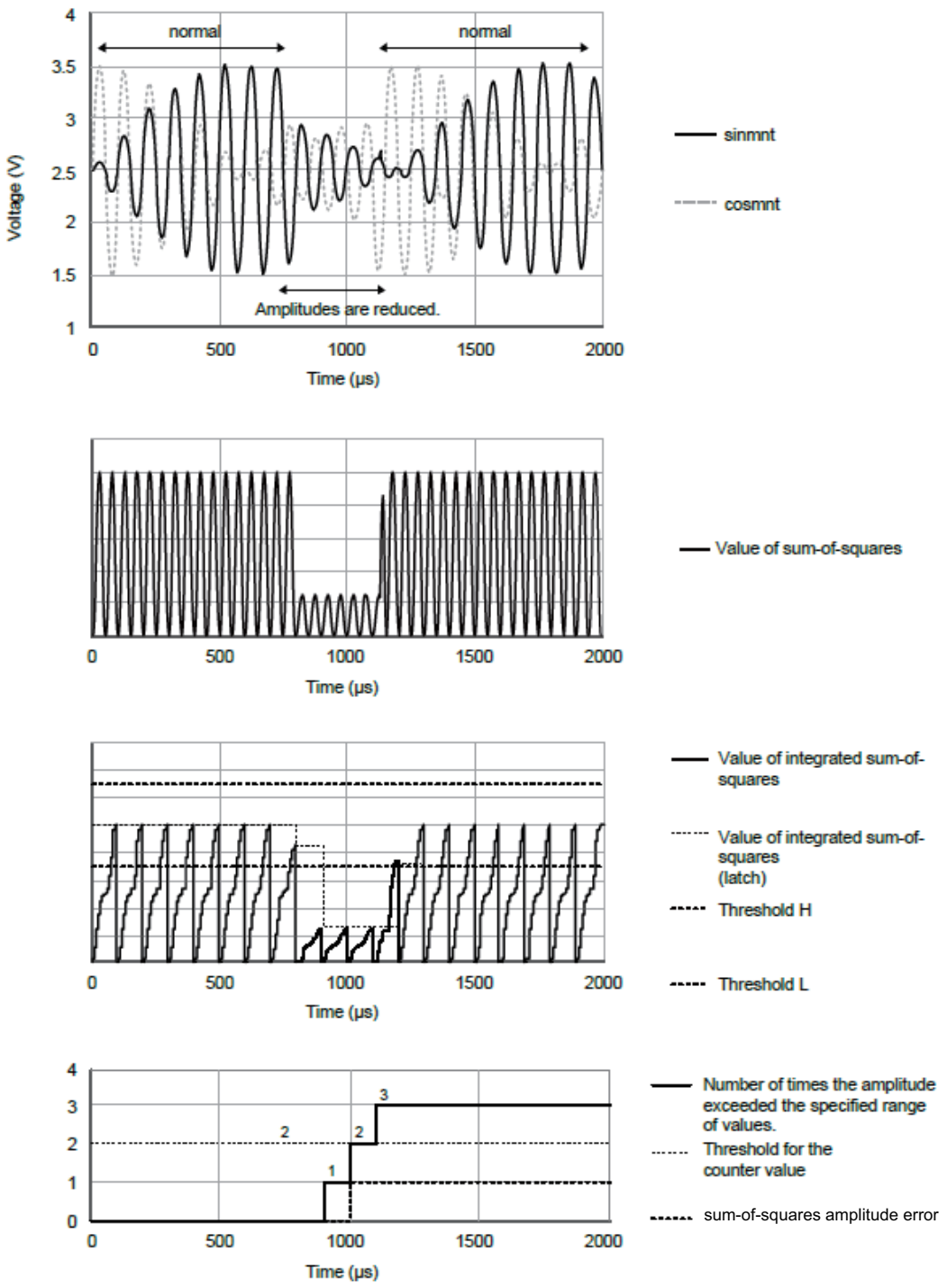


Figure 49.17 Example of Waveforms with Sum-of-Squares amplitude Error

49.1.3.5 Self-Diagnosis

(1) Built-in Self-Test Function

In order to check the validity of a given operation, the Built-in Self-Test (BIST) function generates an intended signal input that is simulated internally by setting a BIST instruction in the RDC3ALnBIST1 register, and monitors the signal that is output in response to the simulated signal input. **Table 49.56** lists test items.

Table 49.56 Details of BIST

Item	Diagnosis
Angle conversion BIST	Self-test of the R/D conversion function The following electrical angles can be set as a resolve signal input: • Target angle 0° • Target angle 45° • Target angle 270°
Error detection BIST	Self-test for the error detection function • Resolver signal error detection BIST • Resolver signal disconnect error detection BIST(sin/cos) • R/D conversion error detection BIST • Power/ground short error detection BIST • Sum-of-Squares amplitude error detection BIST(high side/low side)
ADBIST	Self-test for the validity of the result of 12-bit SAR-ADC conversion • Apply voltages of 1, 2.5, and 4 V in order and judge the result of ADC conversion. • The threshold value for determination is set by the ADB3TH[1:0] bits.

Each output during the execution of BIST operates in response to the simulated signal. Depending on the BIST, a RDC error interrupt is generated due to the erroneous internal state. If the occurrence of this error disturbs the operation, disable RDC error interrupt by the EINTEN bit.

BIST is classified into two types according to the length of execution time, short-period and long-period. Long-period BIST can be executed only when the power is turned on. The angular output does not match the resolver input because the long-period BIST operates on internally generated simulated signals for BIST for up to 10 ms.

Short-period BIST can be performed during angle conversion and maintains angle conversion tracking during BIST execution. Short-period BIST can be performed even when the power is turned on, but long-period BIST should be performed first.

- Short-period BIST: ADBIST, resolver signal error detection BIST, resolver signal disconnect error detection BIST(sin/cos), power short error BIST, ground short error BIST, sum-of-squares amplitude error detection BIST (high side/low side)
- Long-period BIST: angle conversion BIST, conversion error BIST

Perform the following settings to execute BIST.

(1) Enable the forced gain control function when executing a BIST. (Set the AGCD bit in the RDC3ALnPI1 register to 0.)

(2) To execute a short-period BIST, set the EINTEN bit to 0 to disable error interrupts.

(3) Set the VGASL[1:0] bits to 00B when executing a BIST.

(4) Read the VGFLG bit (Power/ground short error detection running bit) as 0. If the value is 1, read the bit again after waiting for about 80 µs.

(5) Set the angle correction bits in the sine and cosine angle correction register to 0° when executing the angle conversion BIST.
Sine angle correction bits SINPO[11:0] = 000_H
Cosine angle correction bits COSPO[11:0] = 000_H

(6) To execute conversion error BIST, set the EDPS bit to 10_B.

(7) Set the input gain resistance value at default (21 kΩ) and the excitation buffer amplitude value at default (2Vpp) when executing a BIST.
PGAX1=0, IRSS0 = 1, EXOC[1:0] = 10_B, IRSC[3:0] = 0100_B, IRSS1 = 0, EXOS = 0, EAATSP = 1

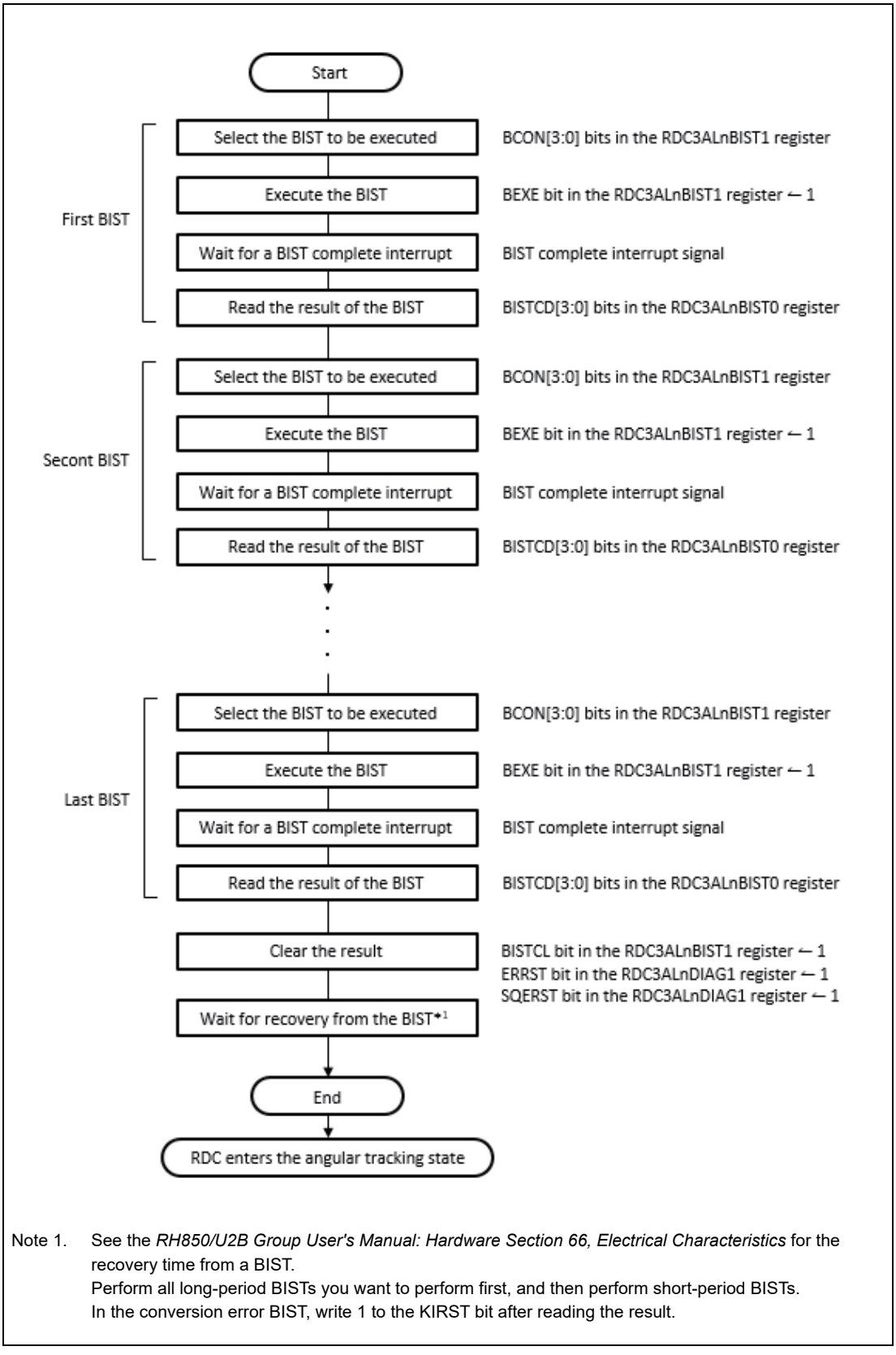
(8) Clear the count value in the SQERST bit by setting 1 before running sum-of-squares amplitude detection BIST (high side/low side).

(9) When the BIST is completed,
set the BISTCL bit in the RDC3ALnBIST1 register to 1 to clear the BIST results.
set the ERRST bit in the RDC3ALnDIAG1 register to 1 to reset the error signal.
set the SQERST bit in the RDC3ALnDIAG1 register to 1 to reset the counter value of sum-of-squares amplitude error.

Return the settings of the registers which were changed in steps (1), (2), (3), (5), (6), and (7) to their original values.

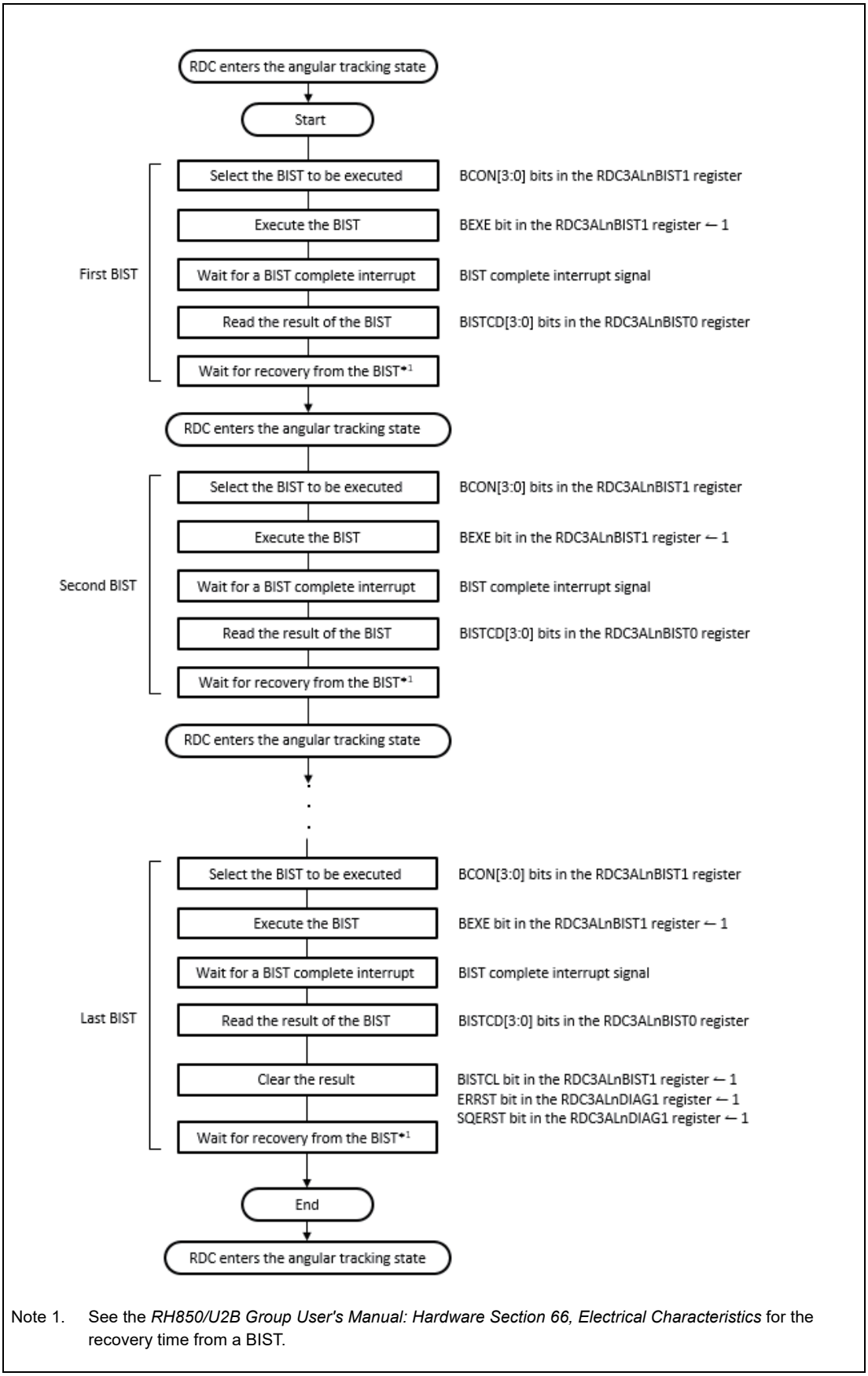
Table 49.57 BISTs for Each Setting of Values

BCON[3:0]	BIST to be Executed
0000	BEXE bit is disabled
0001	This setting is not allowed.
0010	Sum-of-squares amplitude error detection BIST (low side)
0011	Sum-of-squares amplitude error detection BIST (high side)
0100	ADBIST
0101	Angle conversion BIST (0°)
0110	Angle conversion BIST (45°)
0111	Angle conversion BIST (270°)
1000	This setting is not allowed.
1001	Error detection BIST: resolver signal error detection BIST
1010	Error detection BIST: resolver signal disconnection detection BIST (cosine side)
1011	Error detection BIST: Resolver signal disconnection detection BIST (sine side)
1100	Error detection BIST: conversion error BIST
1101	Error detection BIST: power short error BIST
1110	Error detection BIST: ground short error BIST
1111	This setting is not allowed.



Note 1. See the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics* for the recovery time from a BIST.
Perform all long-period BISTs you want to perform first, and then perform short-period BISTs.
In the conversion error BIST, write 1 to the KIRST bit after reading the result.

Figure 49.18 Sequence of Executing BISTs after Starting Up the Power



Note 1. See the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics* for the recovery time from a BIST.

Figure 49.19 Sequence of Executing BISTs during Angle Conversion (Short-period BIST)

(2) ADC Software BIST

Failures in the ADC are diagnosed by the CPU through the following procedure: the DAC code in the 12-bit SAR-ADC written to the relevant register is converted in the ADC and the result is read from the relevant register. The user can set the DAC codes freely, that is, to any of the 4096 codes for the 12-bit ADC. In the ideal state, the software will return the same value of the DAC code which was set for the software BIST as the result of A/D conversion. In actual operations, however, values with errors are output due to non-ideal factors. Therefore, users are required to set a suitable value for the CPU to judge these errors (around ± 32 LSB). With this software BIST, it is possible to diagnose the normality of the combination functions of all the switches of the DAC in the ADC. On the other hand, the ADBIST described in **section (1)**., Built-in Self-Test Function, diagnoses the results of conversion by applying three voltages to the input nodes of the ADC. By using ADBIST and this software BIST together, it is possible to diagnose failures in almost all nodes in the 12-bit ADC.

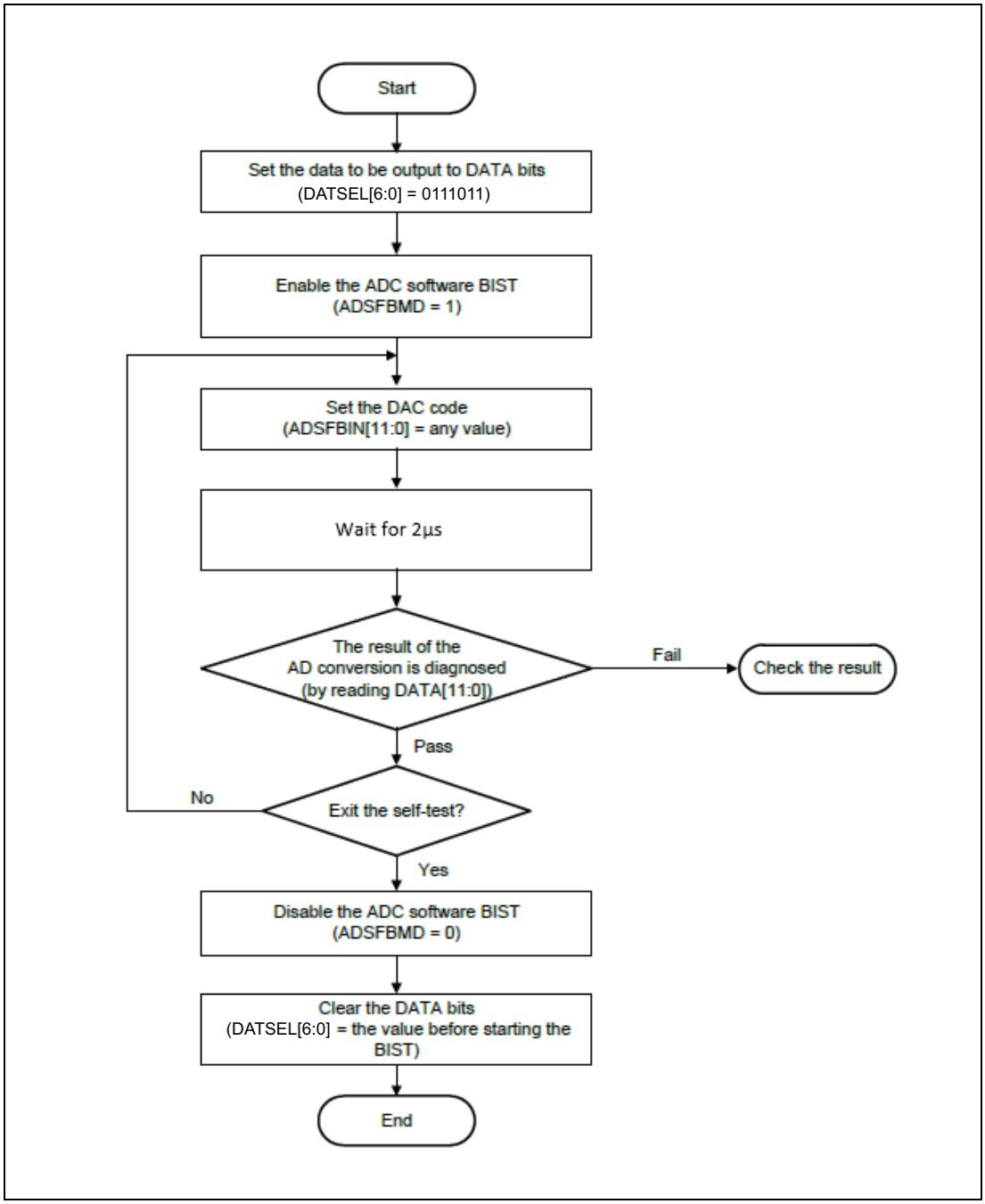


Figure 49.20 Operating Sequence of the ADC Software BIST

49.1.3.6 Excitation Timer (ET) Function

The excitation timer comprises two 16-bit timers: a period measurement timer and an event generation timer. The operating clock of the timers is CCLK (40 MHz). **Figure 49.21** shows a block diagram of the excitation timer.

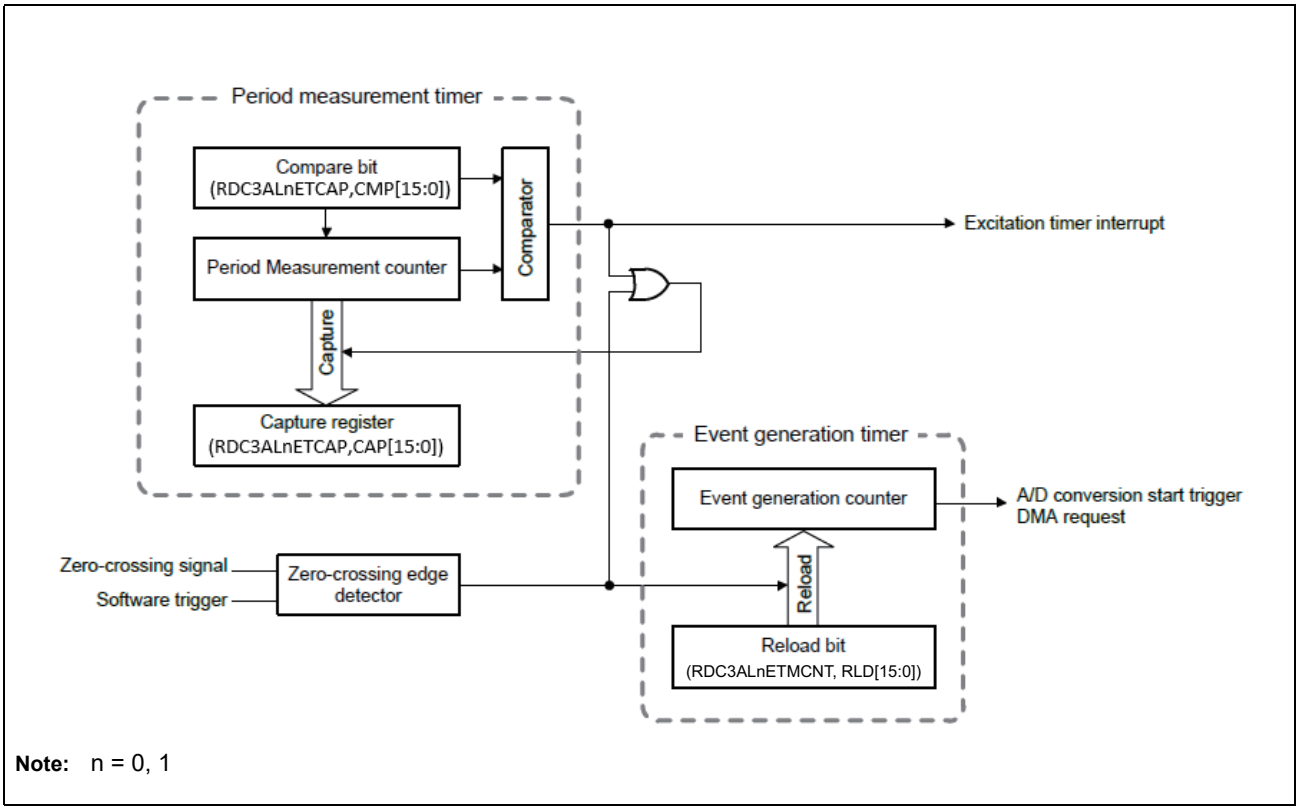


Figure 49.21 Block Diagram of Excitation Timer

(1) Period Measurement Timer

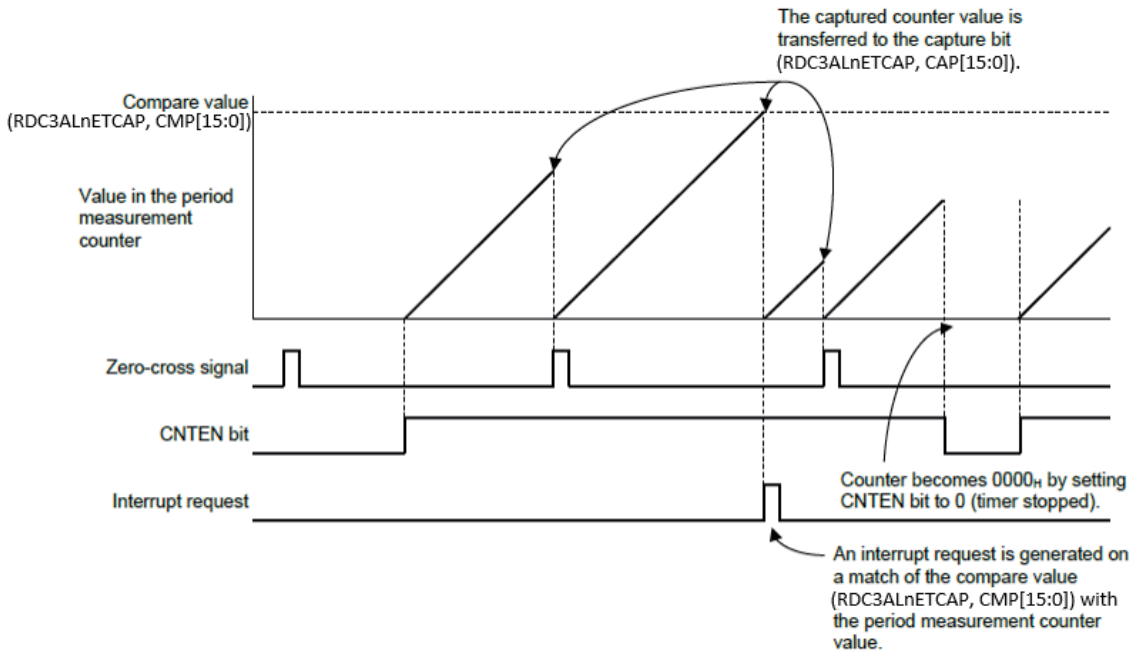
The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable from rise edge and fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in ET Capture bits of the RDC3ALnETCAP register. By reading the RDC3ALnETCAP register, the cycle of excitation signal can be obtained.

The cycle of excitation signal can be calculated from the following formula: (RDC3ALnETCAP register value + 1) × CCLK cycle (25 ns).

When the IREN bit in the RDC3ALnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request is generated if the value set in ET Compare bits of the RDC3ALnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the RDC3ALnETCAP register.

When a zero-crossing signal trigger is generated by writing 1 to the ZCSTRG bit in the RDC3ALnETEN register, the period measurement timer operates in the same way as the zero-crossing signal edge detection.

Figure 49.22 shows an example of period measurement timer operation.



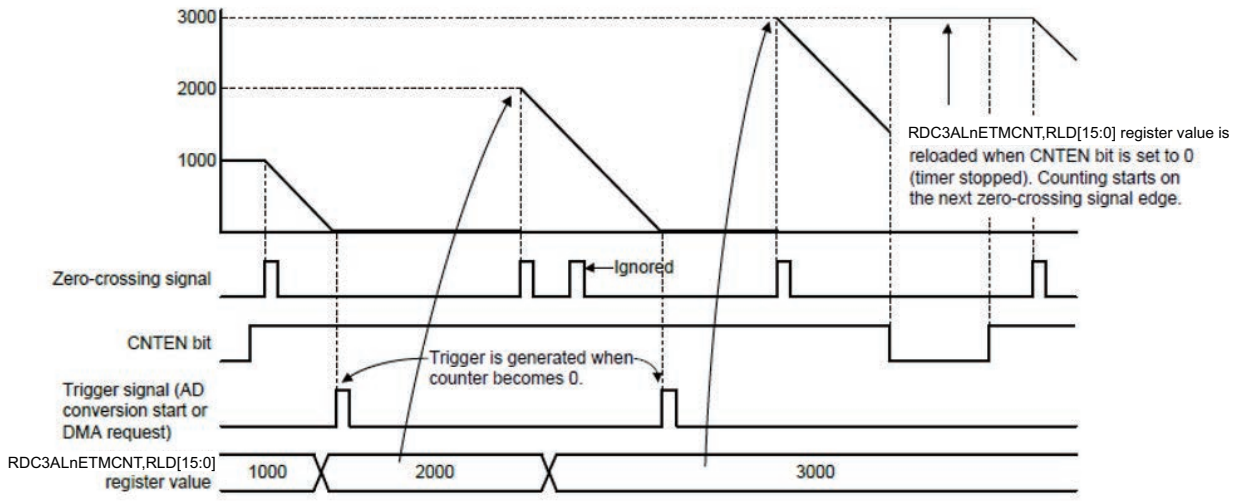
Note: n = 0, 1
CNTEN: A bit in the RDC3ALnETEN register

Figure 49.22 Example of Period Measurement Timer Operation

(2) Event Generation Timer

The event generation timer can generate a trigger signal (A/D conversion trigger, DMA request) after the time set in the RDC3ALnETMCNT register has elapsed since the occurrence of an edge of the zero-crossing signal. When a zero-crossing signal trigger is generated by writing 1 to the ZCSTRG bit in the RDC3ALnETEN register, the event generation timer operates in the same way as the zero-crossing signal edge detection.

Figure 49.23 shows an example of event generation timer operation.



Note: n = 0, 1
CNTEN: A bit in the RDC3ALnETEN register

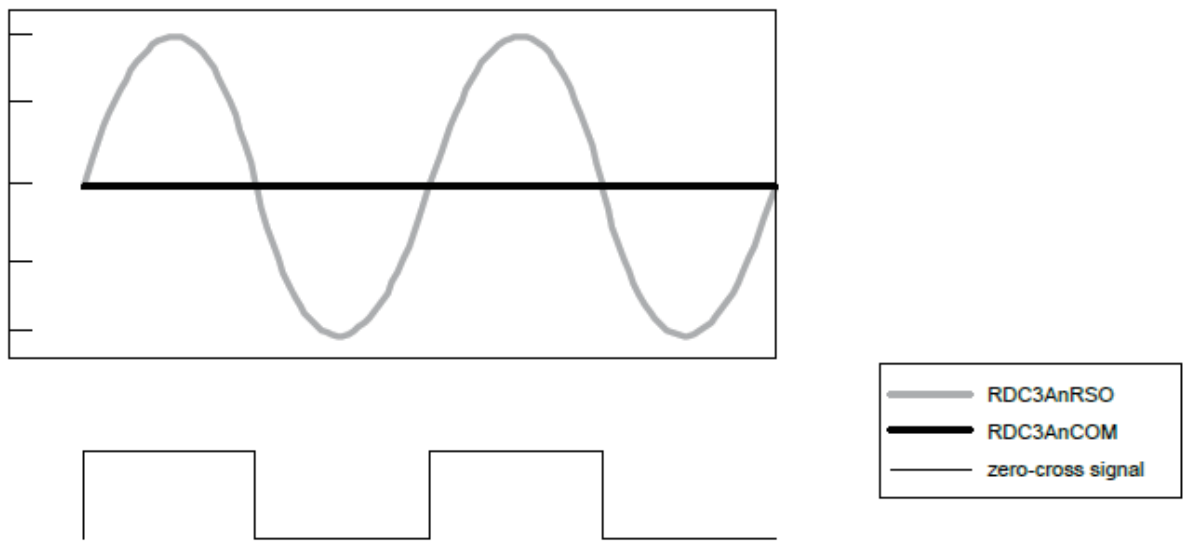
Figure 49.23 Example of Event Generation Timer Operation

(3) Excitation Zero-Crossing Signal

The zero-crossing signal indicates zero-crossing timing for differential excitation signal input. The zero-crossing signal is input to the excitation timer circuit to be used for detecting the excitation vertex. The zero-crossing signal input to the excitation timer circuit can be selected from the following two types by the REFETSL bit.

- 0: The zero-crossing of excitation signal from analog comparator
- 1: The zero-crossing of extracted excitation signal

Figure 49.24 shows the relationship between the differential excitation signal input waveforms and zero-crossing signal.



Note: n = 0, 1

Figure 49.24 Relationship between Differential Excitation Signal Input (RDC3ALnRSO, RDC3ALnCOM) and Zero-Crossing Signal

49.1.3.7 PGA Inversion

When the resolver angle is near 135° or 315°, the sine and cosine signals output through the PGA shapes are vertically symmetrical to each other relative to a common potential. The input potentials of the two signals acquired by the 12-bit SAR-ADC are significantly different and are relatively strongly affected by the nonlinearity error of the ADC. The RDC is equipped with functionality to reduce this effect (by PGA inversion). The output voltage from the PGA is inverted in the range where the output phi angles whose input potentials of the sine and cosine signals become opposite to one another.

Whether to invert the sine and cosine waves or not is decided depending on the output phi angles as follows.

- Range of phi output angles = 0° to 90°: sin is not inverted, cos is not inverted
- Range of phi output angles = 90° to 180°: sin is not inverted, cos is inverted
- Range of phi output angles = 180° to 270°: sin is inverted, cos is inverted
- Range of phi output angles = 270° to 360°: sin is inverted, cos is not inverted

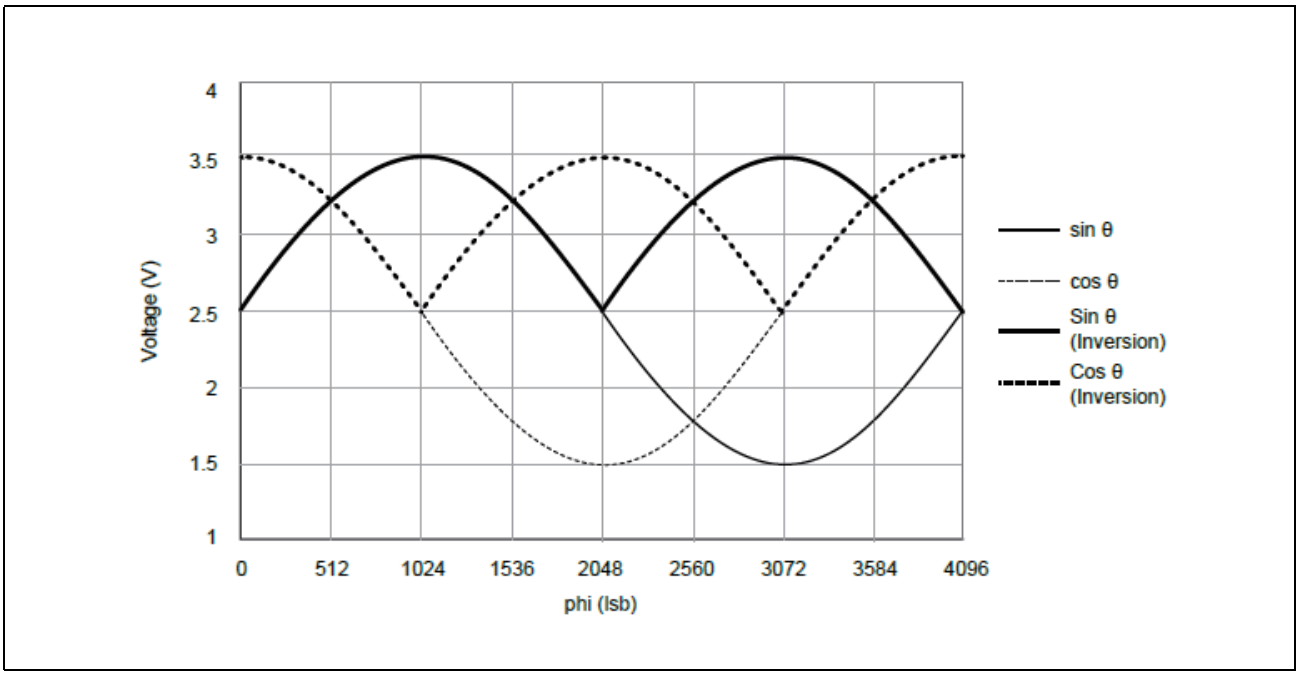


Figure 49.25 Output Phi Angle and Sine and Cosine Signals when Inversion is Enabled

For example, in the case where the resolver stays very close to 90° (1024 LSB), the output phi angle rises and falls at 90°. Here, the cosine signal output through the PGA becomes unstable due to repeated inversion and non-inversion. To avoid this, hysteresis can be added to the angle thresholds at which PGA inversion is applied.

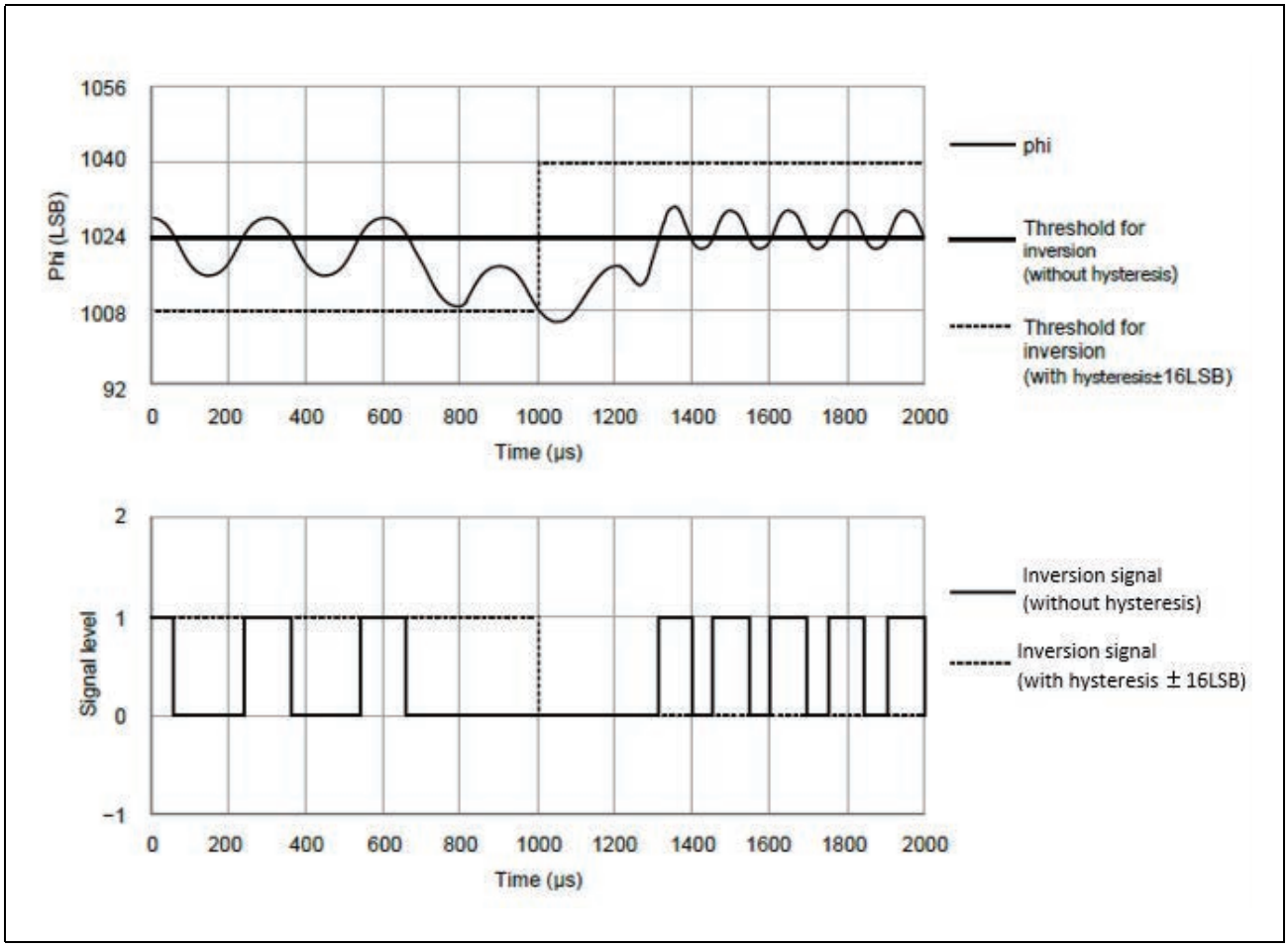


Figure 49.26 Comparison of Thresholds with and without Hysteresis for the Angle with PGA Inversion

The timing of PGA inversion is selected by the PGAIVSL[1:0] bits.

- PGAIVSL[1:0] = 00: no inversion (default)
- PGAIVSL[1:0] = 01: When an excitation cross occurs after the phi output exceeds the threshold angle of inversion.
- PGAIVSL[1:0] = 10: When AD input sin, cos switching occurs after the phi output exceeds the threshold angle of inversion.
- PGAIVSL[1:0] = 11: When AD input sin, cos switching occurs after an excitation cross occurs after the phi output exceeds the threshold angle of inversion.

49.1.3.8 Automatic ROM Table Correction

If there is an error in the ADC, a characteristic error will occur in the RDC angle conversion result. The Automatic ROM Table Correction function has a function to calculate this angle error by the internal conversion BIST operation and to correct the ROM table to correct the generated angle error.

- When performing Automatic ROM Table Correction,

  Set the ROMBSTEN bit to 1 and the ROMBST bit to 1.

  With the above settings, 0° BIST and 270° BIST are automatically executed in sequence within the RDC circuit.

  Note that although the values of the BIST result storage bits (BISTCD[3:0]) also change, the values are indeterminate.

  The required ROM correction value which has been calculated by the BIST is automatically set.

  Wait for 20 ms after setting ROMBST = 1, or the generation of a BIST complete interrupt signal indicates the completion of processing.

  Refer to the description of the initial settings sequence for the RDC regarding the points where automatic compensation from the ROM table is implemented.

49.1.4 Initial Settings Sequence for the RDC

Figure 49.27 shows the procedures for supplying power to the R/D converter and making the initial settings of the registers.

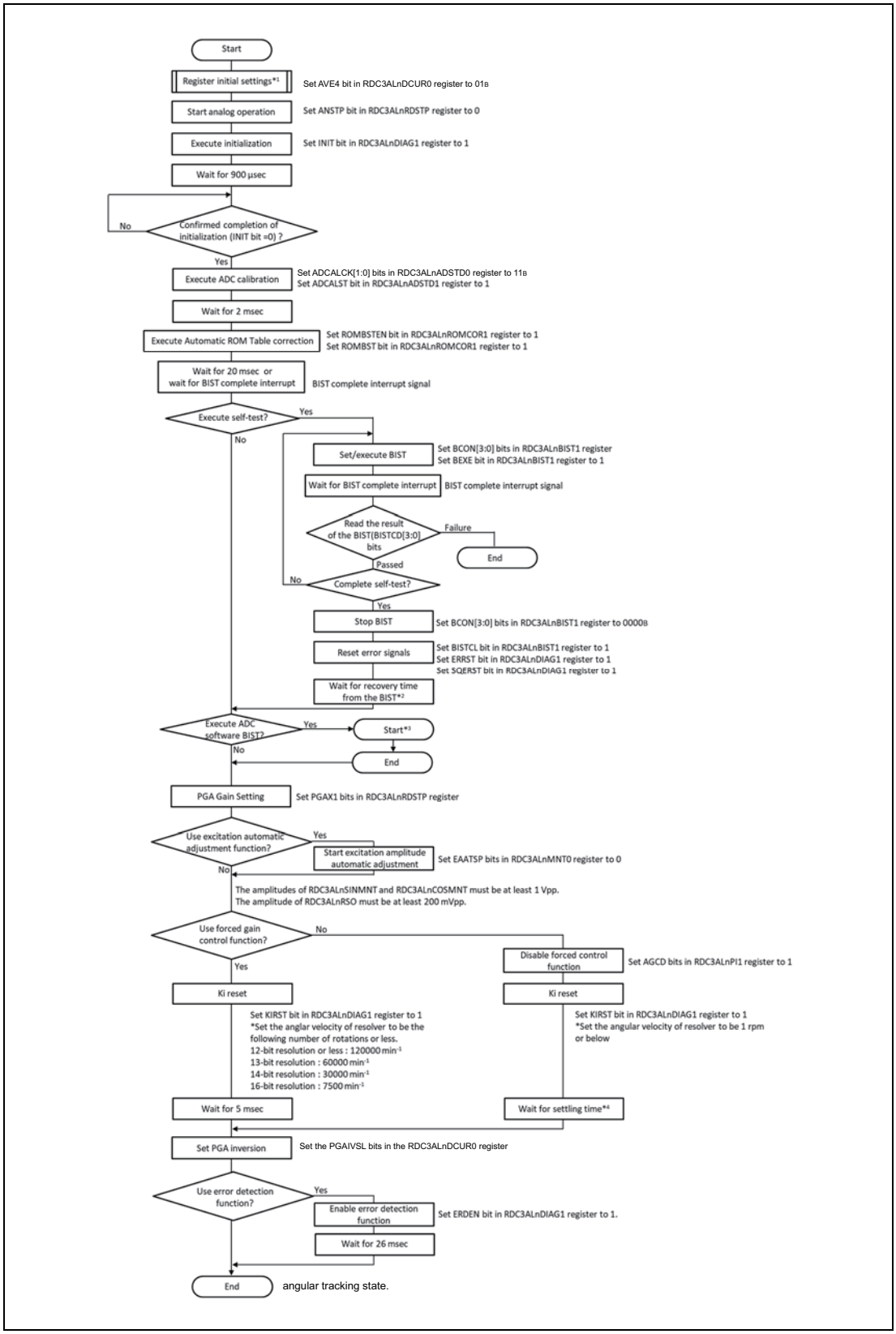


Figure 49.27 RDC3A Initial Operation Flow (1/2)

Note 1. See **Table 49.58**
Note 2. For the recovery time from a BIST, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics*
Note 3. See **Figure 49.20**, Operating Sequence of the ADC Software BIST
Note 4. For the settling time, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics*

Figure 49.27 RDC3A Initial Operation Flow (2/2)

To obtain the specified accuracy of R/D angle conversion (±4 LSB), implement Initialization, ADC calibration, and automatic ROM Table correction

The register bits other than the register bits listed in **Table 49.58** must be set in "Register Initial Settings" in **Figure 49.27**.

Table 49.58 List of Bits which are Not to be Set in "Register Initial Settings". Set bits other than those listed in this table in "Register Initial Settings"

Register Name	Bit Name	Remark
RDC3ALnRDSTP	ANSTP	
RDC3ALnPHICP0	INTCLR[2:0]	
RDC3ALnSCCOR1	PHCST, GNCST	
RDC3ALnAUTMNT0	EAATSP	
RDC3ALnDIAG1	VGST, INIT, ERDEN, SQERST, ERRST, KIRST	
RDC3ALnBIST1	BISTCL, BEXE, BCON	
RDC3ALnENC0	PHILT, OMGLT, REFZEN,CINTEN,ABEN,UVWEN,ZEN,EINTEN	
RDC3ALnTBUS	DATSEL[6:0]	
RDC3ALnETEN	ZCSTRG, CMPEN, IREN, DREN, ADTEN, CNTEN	
RDC3ALnADSTD0	ADCALCK	
RDC3ALnADSTD1	ADCALST, ADSFBMD, ADSFBIN[11:0]	
RDC3ALnROMCOR1	ROMBST	

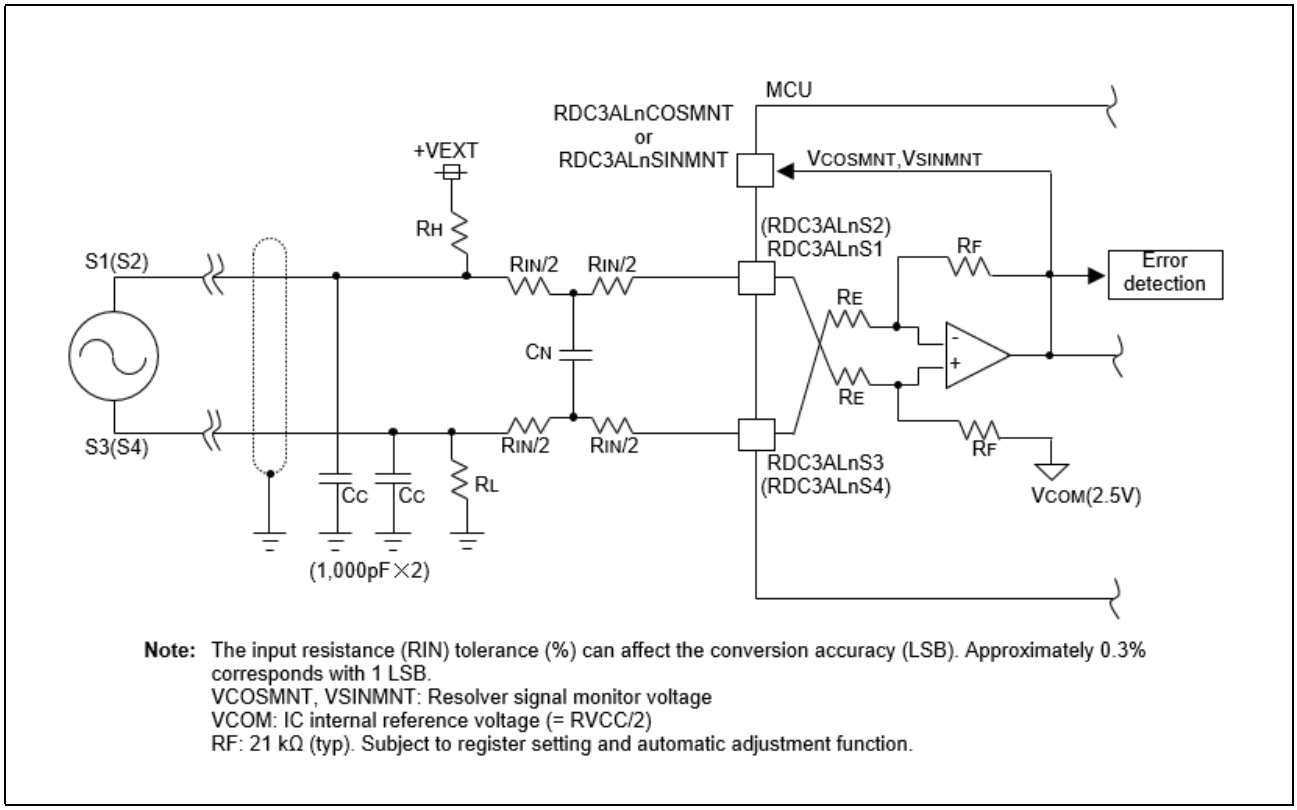
These bits can be set during angle conversion.

49.1.5 Resolver Interface Circuits

The following shows specific interface circuits as reference examples. When determining constants such as a resistance value and adding functions such as an input/output protection circuit, a careful decision must be made for each system and conduct adequate evaluation.

49.1.5.1 Resolver Signal Input (Differential) Circuit

Figure 49.28 shows the VR resolver signal input (differential) circuit and an equivalent circuit for the monitor output



Note: The input resistance (RIN) tolerance (%) can affect the conversion accuracy (LSB). Approximately 0.3% corresponds with 1 LSB.
VCOSMNT, VSINMNT: Resolver signal monitor voltage
VCOM: IC internal reference voltage (= RVCC/2)
RF: 21 kΩ (typ). Subject to register setting and automatic adjustment function.

Figure 49.28 VR Resolver Signal Input Circuit and Equivalent Circuit of Monitor Output

- Input signal level
  Adjust the signal level so that VCOSMNT or VSINMNT = (VIN) × (RF / (RIN + RE)) falls within the range from
  0.32 × AFCVCC to 0.68 × AFCVCC [Vpp].
  (where VIN denotes the signal output voltage between resolver pins [Vpp], RIN ≥ 2[kΩ])
  RE is 970 Ω (typ.) when the PGAX1 bit is set to 0 and it is 21 kΩ (typ.) when the PGAX1 bit is set to 1.

- RH and RL: Determine a resistance value in an 80% to 100% range from the following calculated values:

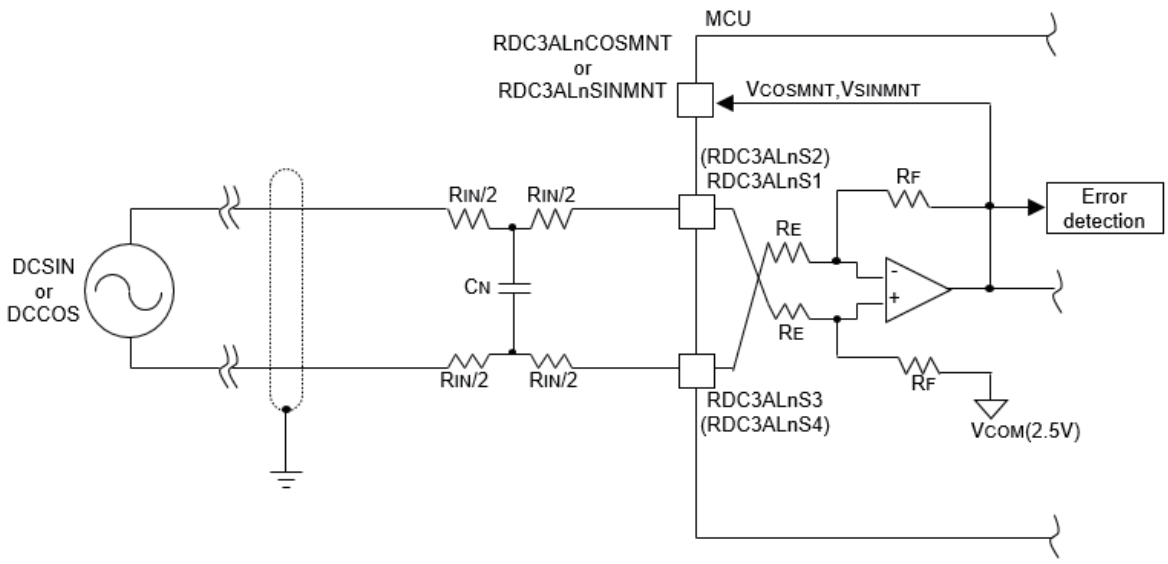
1. $RH \cong \{(VEXT - V_{COM})/(22.0 \times 10^{-6})\} - R_{IN}$, where $V_{COM} = AFCVCC/2$ (V)

2. RL ≅ $\{V_{COM}/(22.0 \times 10^{-6})\}$ - R_{IN}, where V_{COM} = AFCVCC/2 (V)

Use the following formulas, when the PGAX1 bit is set to 1 and the IRSC[3:0] bits set to 0000_B.

1. RH ≅ $\{(VEXT - V_{COM})/(25.0 \times 10^{-6})\}$ - R_{IN}, where V_{COM} = AFCVCC/2 (V)
2. RL ≅ $\{V_{COM}/(25.0 \times 10^{-6})\}$ - R_{IN}, where V_{COM} = AFCVCC/2 (V)

Figure 49.29 shows an equivalent circuit when the DC resolver signal input is used.



Note: The input resistance (RIN) tolerance (%) can affect the conversion accuracy (LSB). Approximately 0.3% corresponds with 1 LSB. Differences in input signal conditions and peripheral circuits can affect the RD conversion accuracy and the error detection function.

Figure 49.29 Equivalent Circuit when DC Resolver Signal Input is Used

49.1.5.2 Excitation Voltage Booster Amplifier Circuit

(1) Excitation Voltage Booster Amplifier Circuit (Single Power Supply)

Figure 49.30 shows an equivalent circuit of the excitation voltage booster amplifier circuit with single power supply.

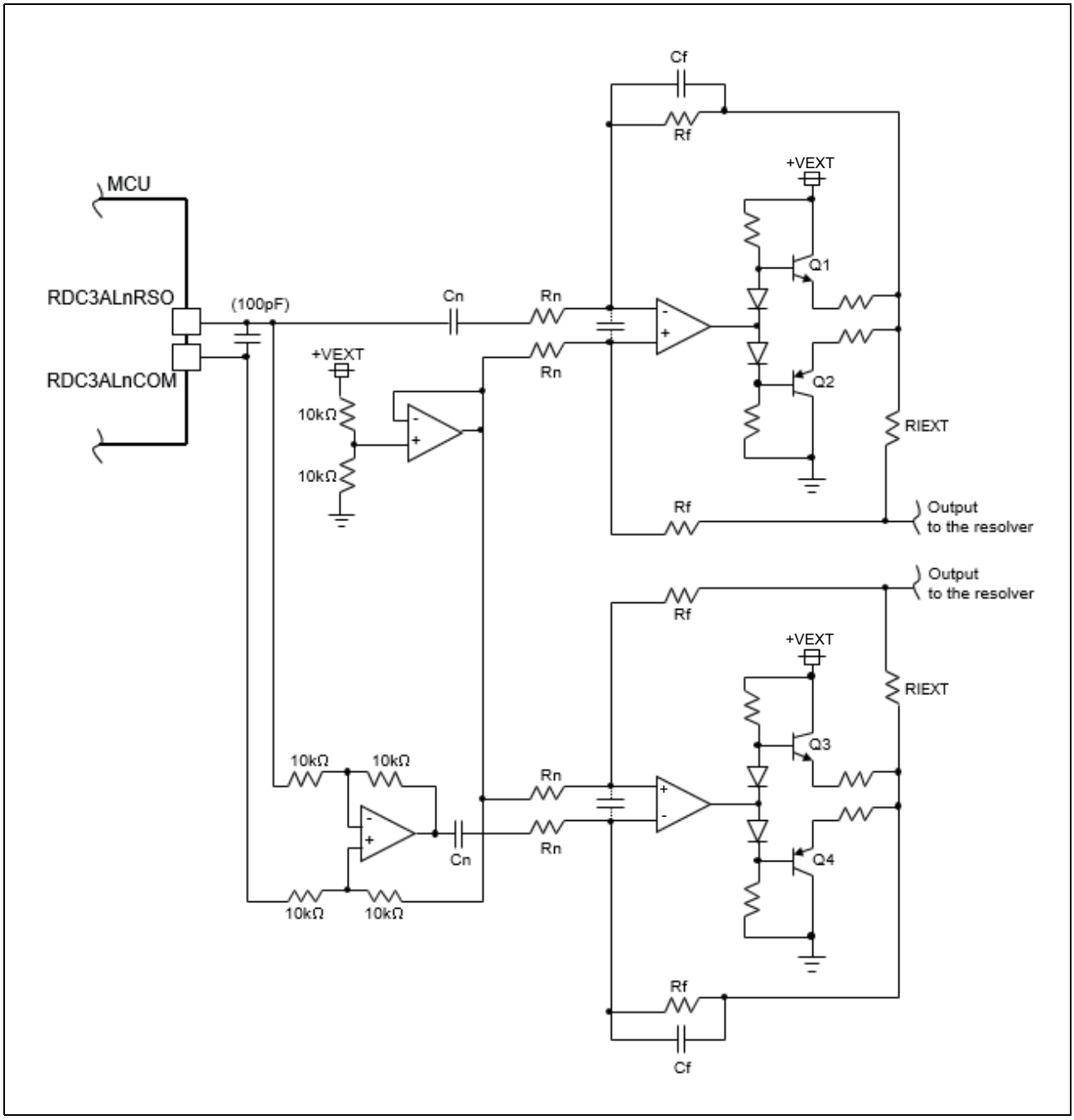


Figure 49.30 Equivalent Circuit Example of Excitation Voltage Booster Amplifier Circuit (Single Power Supply)

(2) Excitation Voltage Booster Amplifier Circuit (Dual Power Supply)

Figure 49.31 shows an equivalent circuit of the excitation voltage booster amplifier circuit with dual power supply.

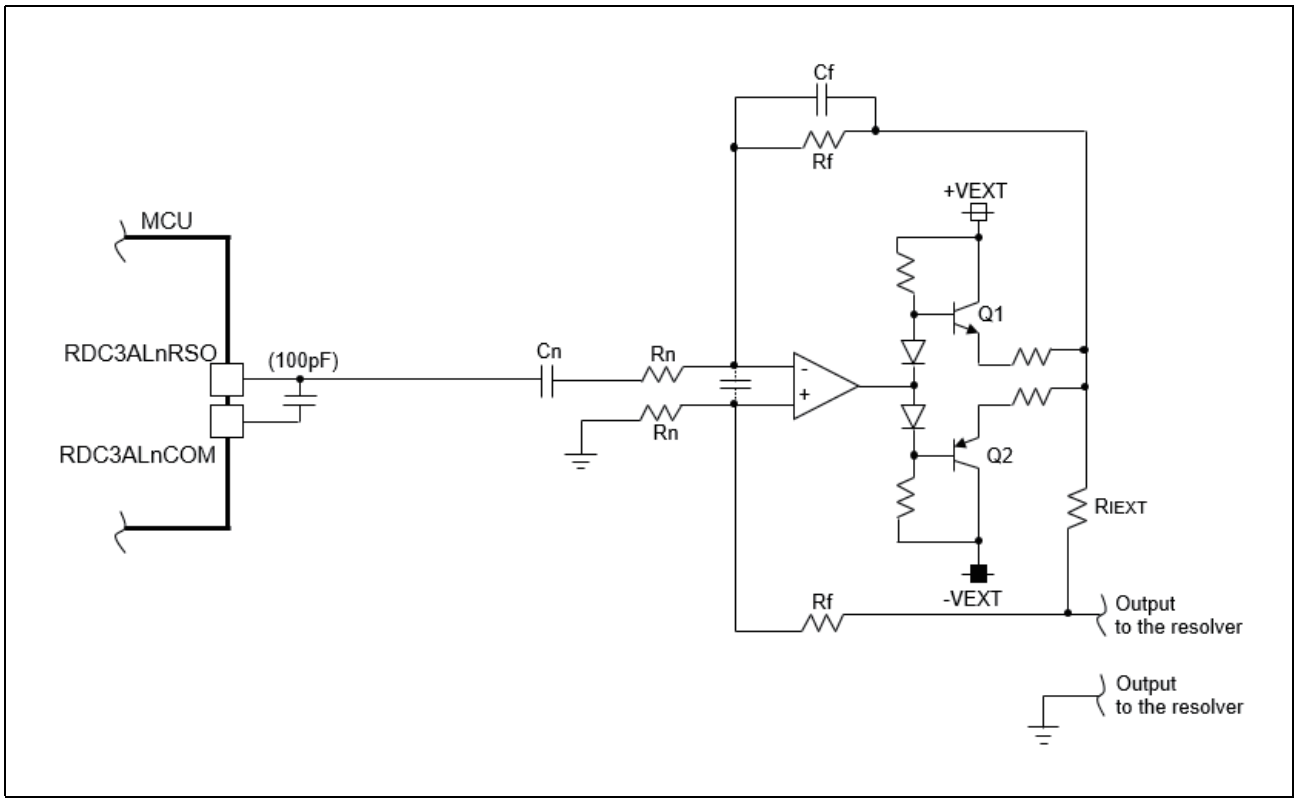


Figure 49.31 Equivalent Circuit Example of Excitation Voltage Booster Amplifier Circuit (Dual Power Supply)

(3) Method for Setting Constants of Excitation Voltage Booster Amplifier Circuit

Both of the excitation voltage booster amplifier circuits shown as reference use the current control type. This type is effective in preventing secondary failure caused by short-circuit accident between excitation lines. Also, it is expected to improve the S/N ratio of resolver signal by boosting voltage.

Step (1): Calculate the excitation current by setting the excitation voltage based on the voltage of external power supply.

$V_{REF} = I_{REF} \times ZRO$

Step (2): Calculate the circuit constants based on the excitation current.

$I_{REF} = (V_{RSO} \times Rf) / (R_{IEXT} \times Rn)$

[Legend]

+VEXT, – VEXT: External power supplies (for the excitation voltage booster amplifier circuit)

IREF : Excitation current of the resolver

RIEXT : Resistor for setting excitation current of the resolver

VREF : Excitation voltage for the resolver

ZRO : Input impedance of the resolver (specification value)

VRSO : RDC3ALnRSO pin output voltage (= 2Vp-p)

<Settings conditions>

- $RIEXT \leq (ZRO / 10)$ [Ω]
- $Rf \geq 50$ kΩ, $Cn \times Rn \geq 5 \times 10^{-4}$[s], $Cf \times Rf \leq 5 \times 10^{-6}$[s]
- Use the same power supply for an operational amplifier as that for the transistor buffer.

49.1.5.3 Resolver Excitation Signal External Input Circuit

(1) Resolver Excitation Signal Input Circuit (Single Power Supply)

Figure 49.32 shows an equivalent circuit when the resolver excitation signal is input from an external source (single power supply).

Table 49.59 lists additional resistor values (reference values) of the resolver excitation signal external input circuit with a single power supply.

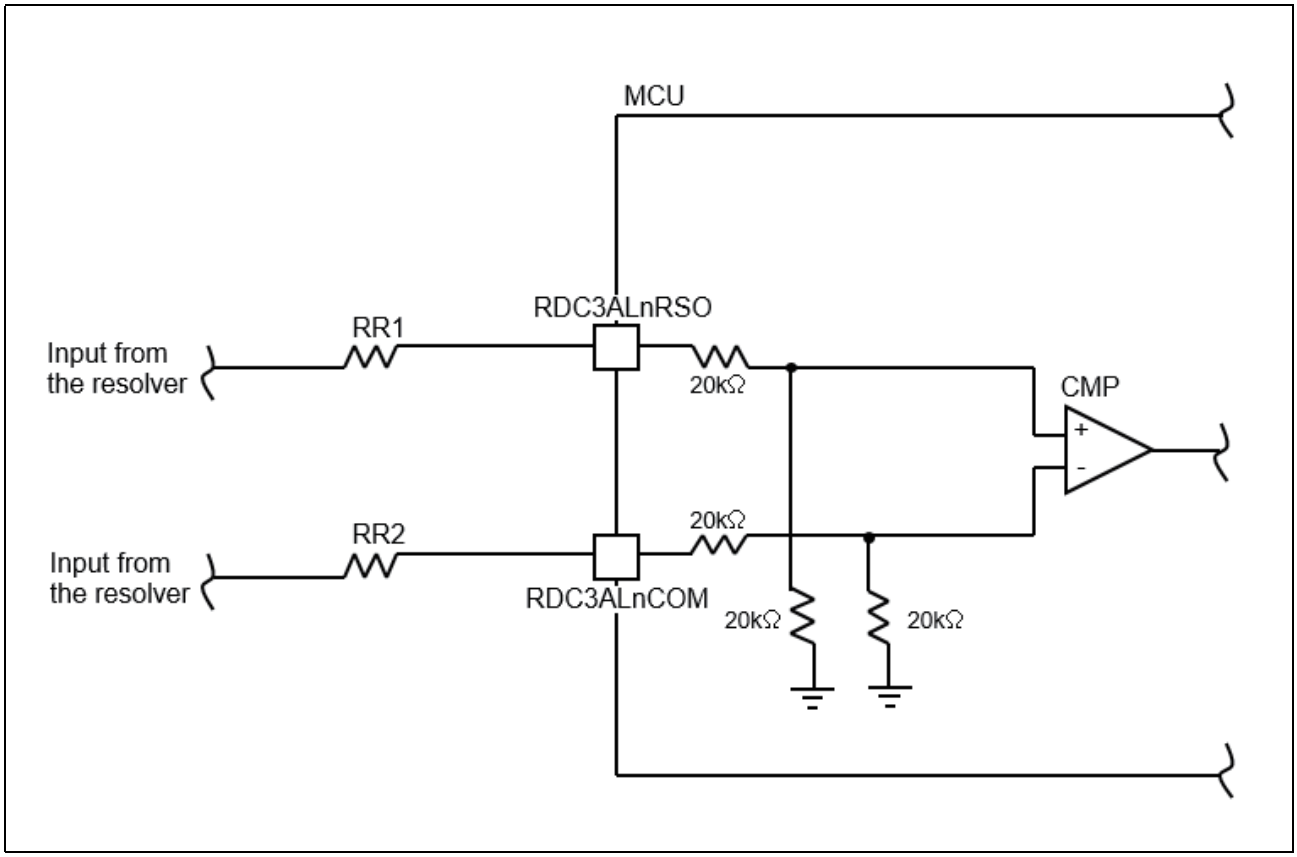


Figure 49.32 Resolver Excitation Signal External Input Circuit (With Single Power Supply)

Table 49.59 Additional Resistor Value for Resolver Excitation Signal External Input Circuit (Reference Values, Single Power Supply)

+VEXT	RR1, RR2
5V type	0kΩ
12V type	47kΩ
24V type	120kΩ

(2) Resolver Excitation Signal Input Circuit (Dual Power Supply)

Figure 49.33 shows an equivalent circuit when the resolver excitation signal is input from an external source (dual power supply). Adjust Rn1 and Rn2 so that the voltage on the RDC3ALnCOM pin does not exceed 5V.

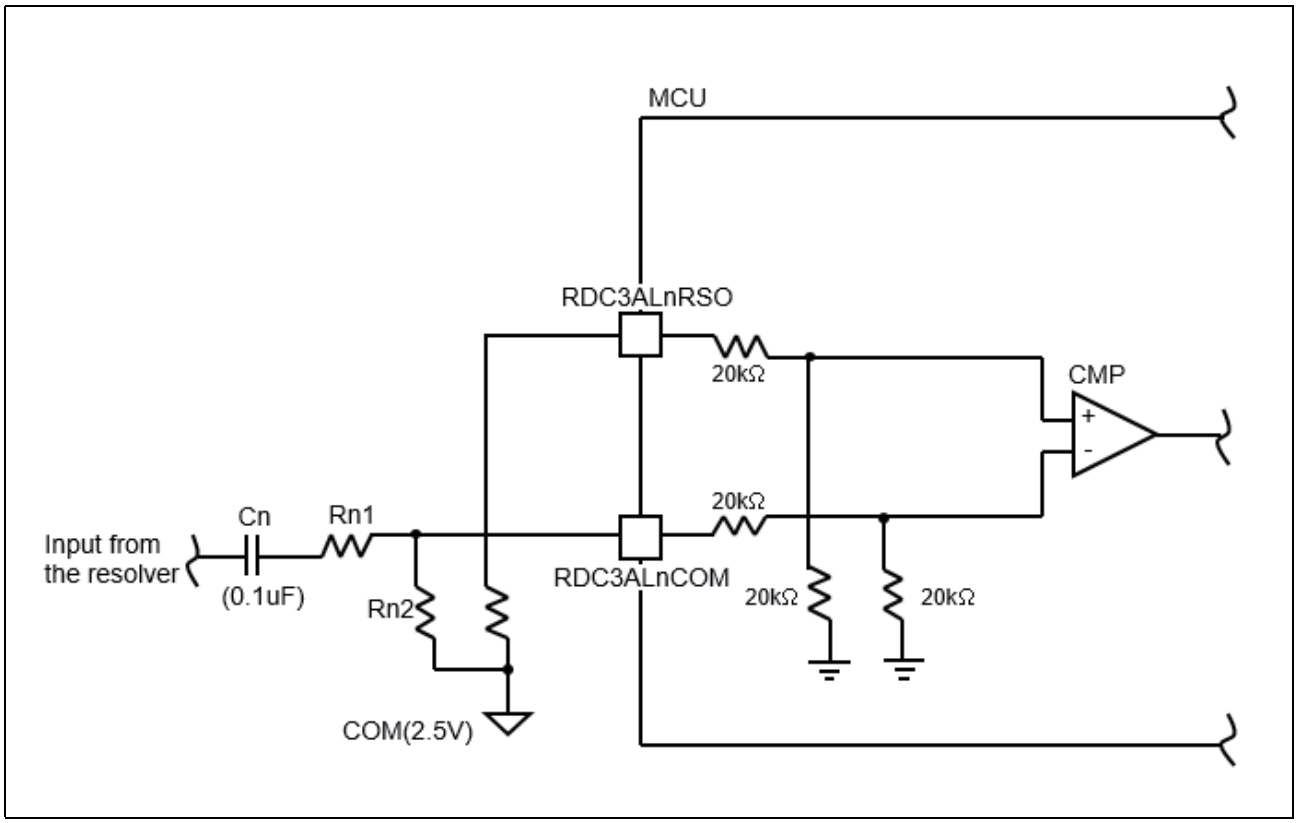


Figure 49.33 Resolver Excitation Signal External Input Circuit (with Dual Power Supply)

49.1.5.4 Usage Noise

When the resolver is used as a motor sensor, the resolver signal is affected by various types of noises depending on the drive control configuration of the motor. To perform R/D conversion successfully, sufficient S/N ratio of the resolver signal is required.

This RDC is a highly responsive R/D conversion module. Although considerations have been made for noise immunity, the RDC by itself is not designed to accommodate all noise environmental factors. Appropriate peripheral circuits need to be considered depending on the environment in which the module is deployed. The following describes the specific countermeasures for noise in [Countermeasure I] to [Countermeasure VIII] as reference.

(1) Countermeasures for Magnetic Disturbance Noise

If the leakage flux of the motor passes through the resolver, the resolver signal behaves as if the angle changes, resulting in malfunction.

[Countermeasure I]

When installing the motor and resolver, use the configuration and material that block the magnetic loop passing through the resolver (magnetic shield effect) to minimize the leakage flux of the motor that passes through the resolver.

[Countermeasure II]

If the leakage flux of the motor that passes through the resolver cannot be completely avoided, raise the resolver excitation voltage (current) to improve the S/N ratio of the original signals.

(2) Countermeasures for Electric Disturbance Noise

The electric disturbance (spike noise, and so on) caused by the PWM drive of the motor is extremely large, and affects all power systems, such as the excitation signal lines of resolver and power supply line, via various paths.

[Countermeasure III]

Insert a common mode/normal mode filter into the resolver excitation lines to remove the spike noise components. Generally, the low-impedance excitation line hardly has noise and the countermeasure is less needed.

[Countermeasure IV]

Insert a common mode/normal mode filter into the resolver signal lines (RDC3ALnS1-RDC3ALnS3, RDC3ALnS2- RDC3ALnS4) to remove the spike noise components. Select the time constant that takes effect only on noise and leaves the original resolver signal waveform undistorted. In addition, ensure that the electric noise waveform of the RDC3ALnS1 to RDC3ALnS4 pins viewed from AFCVSS (ground) are in phase. If an error due to electric external disturbance noise persists after this countermeasure is taken, keeping the resolver signal level low can be effective.

[Countermeasure V]

If necessary, insert a bypass capacitor to the power supply (AFCVCC) line.

(3) Other General Measures

[Countermeasure VI]

Use a shielded twisted pair cable for resolver wiring. Shielded terminals must be treated collectively on the circuit side (grounded to GND). The cable must be routed separately from the motor cable.

[Countermeasure VII]

Enhance the GND system for low impedance to reduce common impedance noise and to provide shielding effect. Another possible measure is to fix the potential of the motor driver radiator and motor case to the control-system ground potential.

[Countermeasure VIII]

Physically separate the motor driver from the sensor circuit and cover each of them with a shield case.

49.2 RDC3AS

49.2.1 Specifications of the R/D Converter (RDC3AS)

This R/D converter module inputs sin, cos and excitation signals from the resolver acquired by three differential inputs ΔΣADC existing outside this module, and convert analog angles to digital angles with a maximum 16-bit resolution by digital tracking loop method.

49.2.1.1 Overview

(1) Functional Overview

The R/D (resolver-to-digital) converter 3AS converts the analog value (angle information) indicating the rotor angle of the resolver obtained by ΔΣ ADC into a 16-bit (at maximum) digital value. In addition to the function of converting the analog angle signal from the resolver into a digital angle signal, the RDC3AS provides sin, cos correction function, error detection function, self-diagnosis function and other functions.

Table 49.60 lists the specifications for the RDC3AS.

Table 49.60 Overview of the RDC Specifications (1/2)

Function		Description
Tracking loop	Excitation Input signal source selection	It is possible to select the excitation input from the excitation ΔΣ ADC, the excitation input from the timer in LSI, or the excitation input from the LSI external terminal and, it is possible to set the required delay adjustment amount.
	Required sensor selection	Selects VR resolver or DC resolver.
	Excitation component extraction	Extraction of the excitation component from the resolver input signals is available for use in R/D conversion.
	PI compensator bandwidth setting	Selects from six bandwidths (five fixed and one auto-adjusted).
	Forced gain control (AGCON)	Improves the tracking performance when the resolver angle deviates significantly from the R/D converted angle. In addition, the maximum and minimum values of PI compensator gain during AGC operation can be set.
	Maximum angular velocity setting	Sets a maximum angular velocity (resolution) in the range from 960,000 rpm (10 bits) to 15,000 rpm (16 bits).
	PHI angular velocity information reading	Reads the angular velocity from the PHI angle output register.
	Monitor	Reads angle information (°), angular velocity information (rpm), control variation values (%), and other signals directly from a register.
	Angle compare	When the angle that is set in the angle compare registers 0 to 2 and the R/D converted angle match, a compare match interrupt request is generated.
	Encoder pulse output	Outputs U-phase, V-phase, W-phase, A-phase, B-phase, and Zphase signals (4096 Edge/Revolution).

Table 49.60 Overview of the RDC Specifications (2/2)

Function		Description
Sine and cosine correction function	Sine/cosine gain correction	Automatically detects the amplitudes of the sine and cosine signals by comparing them and corrects them.
	Sine/cosine common offset correction	Automatically detects an offset of the common levels of the sine and cosine signals input from the original common level and corrects them.
	Sine/cosine phase correction	Automatically detects the phase deviations of the excitation components of the sine and cosine signals to be input and corrects them.
	Sine/cosine angle correction	Inputs the value for correcting the sine and cosine angles to the SIN-ROM and COS-ROM tables. This function handles the mounting of the resolver at an angle toward the motor shaft by correcting the resulting orthogonality errors of the sine and cosine signals from the resolver.
Error detection	Error detection	Detects resolver signal error, resolver signal disconnect error, R/D conversion error, two paths comparison conversion error, sum-of-squares amplitude error.
Self-diagnosis	Built-in self-test	Angle conversion BIST (0, 45, 270°) Error detection BIST (resolver signal error, resolver signal disconnect error, conversion error, sum-of-squares amplitude error.
Others	Excitation timer (ET)	Measures period of excitation signal Generates event signals (AD trigger, DMA request).
Interrupts		Compare match interrupts 0 to 2 Z-phase interrupt RDC error interrupt Excitation timer interrupt BIST completion interrupt

49.2.1.2 Connection Block Diagram

Figure 49.34 Connection Block Diagram of the R/D Converter

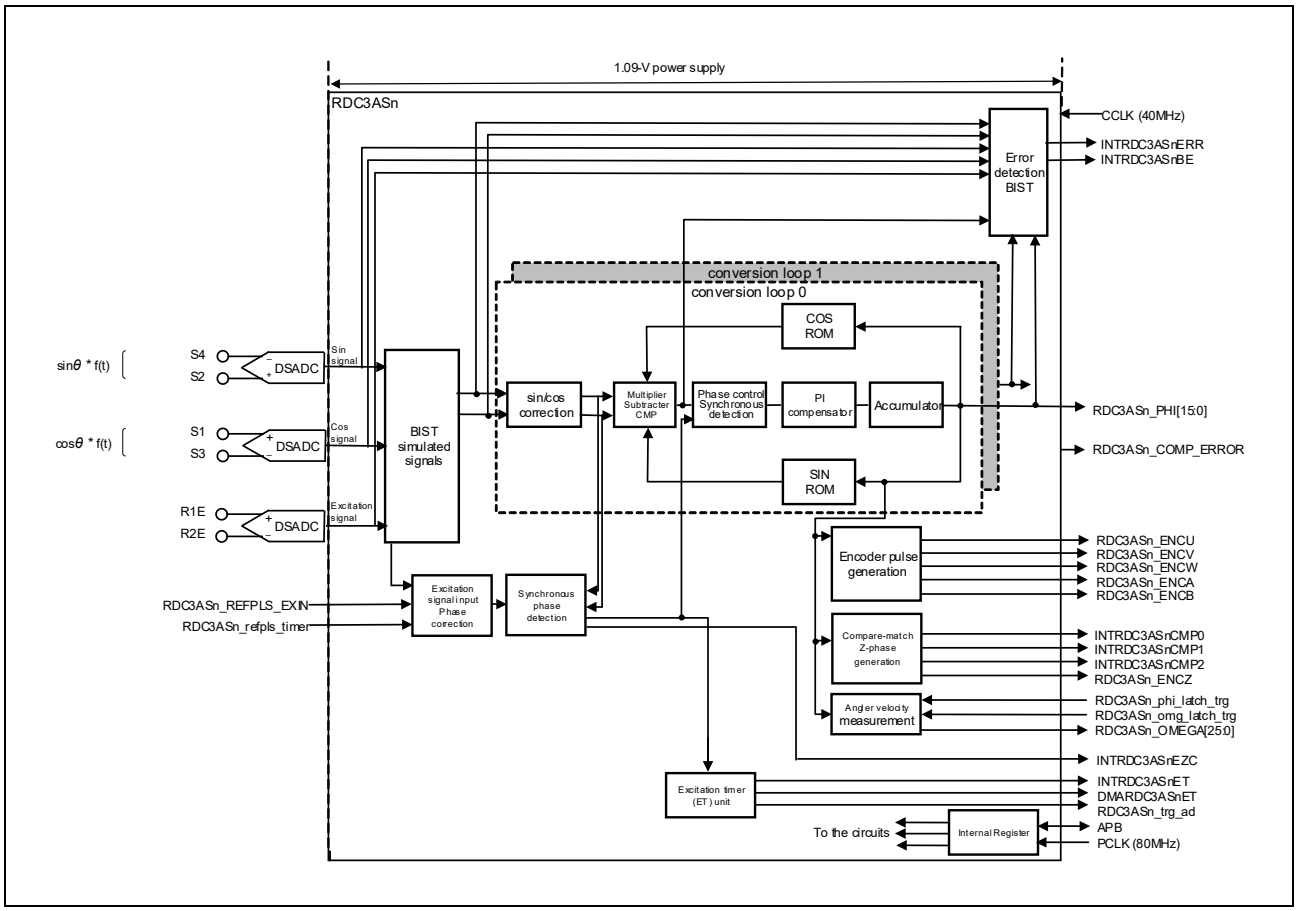


Figure 49.34 Connection Block Diagram of the R/D Converter (RDC3AS)

Note: n=0,1
f(t): excitation signal
RDC3ASnS1 to RDC3ASnS4: resolver signals
SIN ROM: Sine wave ROM
COS ROM: Cosine wave ROM

The sin, cos, and excitation signals from the resolver are acquired by three differential ΔΣ ADCs*1 and input to this RDC module. The sin and cos signals are input to two conversion control loops (ADC loop 0 and ADC loop 1) for the purpose of redundancy monitoring, and converted to digital angles by the digital tracking loop. ADC loop 0 is the main loop and ADC loop 1 is the monitoring comparison loop.

Note 1. About RDC3AS0, sin signal is DSADC00, cos signal is DSADC15, excitation signal is DSADC13.
About RDC3AS1, sin signal is DSADC10, cos signal is DSADC12, excitation signal is DSADC11.

49.2.1.3 Operating Principle

The following describes the operating principles of the RDC3AS module. This R/D converter module uses the tracking method to convert analog resolver signals to digital signals (R/D conversion). The tracking loop runs at 20 MHz. When the excitation signal f(t) is input to the excitation coil, f(t) • sinθ and f(t) • cosθ are output from the resolver according to the angle (θ) of the resolver rotor. These signals are input to the RDC3ASnS2-RDC3ASnS4 and RDC3ASnS1-RDC3ASnS3 pins, respectively.

These signals are amplified and then input to the multiplier. At the same time, cos ϕ (or sin ϕ) is generated by passing the accumulator output through COS ROM (or SIN ROM) and is fed back to the corresponding multiplier. Then, the subtraction is performed on the outputs from both multipliers.

$f(t) \cdot (\sin\theta \cdot \cos\phi - \cos\theta \cdot \sin\phi)$

$= f(t) \cdot \sin(\theta - \phi)$

$\approx f(t) \cdot (\theta - \phi)$

The result is converted to 1-bit digital value by the comparator (CMP) and then passed to the next block. The excitation component f(t) is removed in the synchronous detection circuit to obtain the control variation $\varepsilon = \theta - \phi$. The negative feedback control over the entire analog and digital circuits provides feedback so that the control variation becomes zero. When $\theta = \phi$, the analog angle information from the resolver has been converted to digital angle ϕ (16-bit wide). **Figure 49.35** describes the PI compensator and accumulator.

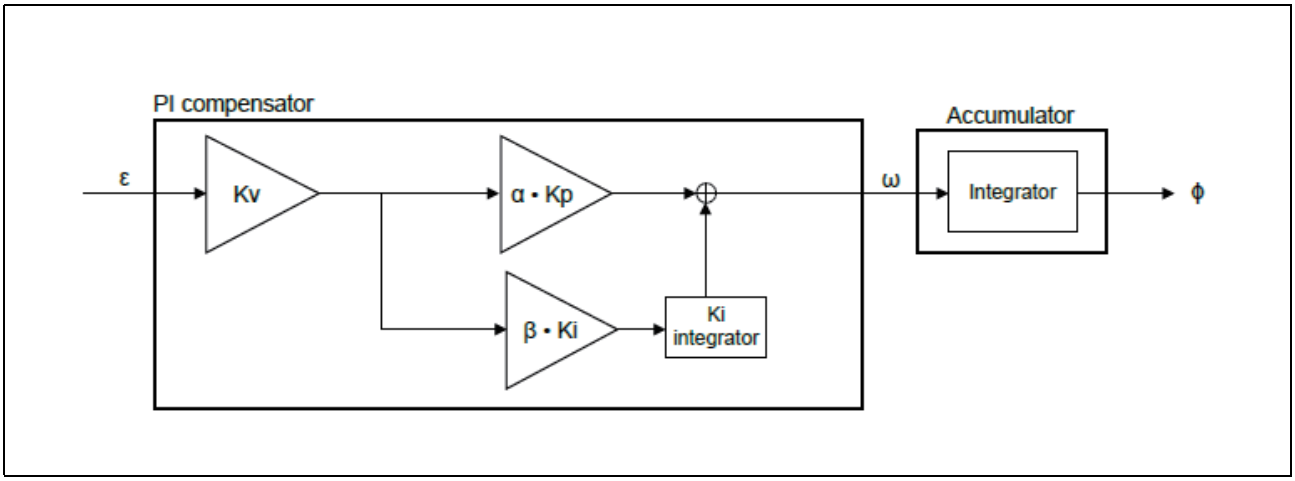


Figure 49.35 PI Compensator and Accumulator

The PI compensator converts the control variation according to the following formula, and passes the result to the accumulator circuit

$\omega = (\alpha \cdot Kp + (\beta \cdot Ki)/(s \cdot T)) \cdot Kv \cdot \varepsilon$

Kv, Kp, Ki: control coefficients that can be set in a register

α, β: fixed values

s: Laplace variable

T: Integration time constant

ω: PI compensator output, angular velocity information

The accumulator circuit calculates the angle ϕ based on the angular velocity information ω.

49.2.2 RDC Register Specifications

49.2.2.1 List of Register Addresses

The following table lists the RDC3AS registers.

Table 49.61 List of RDC Register Addresses

Module Name	Register Name	Symbol	Address	Access Size	Access Protection	
					PGB	Other
RDC3ASn	ΔΣ ADC setting support register	RDC3ASnDSST	<RDC3ASn_base>+0000_H	8, 16, 32	*1	—
RDC3ASn	Control gain select register 0	RDC3ASnPI0	<RDC3ASn_base>+0004_H	8, 16, 32	*1	—
RDC3ASn	Control gain select register 1	RDC3ASnPI1	<RDC3ASn_base>+0008_H	8, 16, 32	*1	—
RDC3ASn	PHI compare setting register 0	RDC3ASnPHICP0	<RDC3ASn_base>+$000C_H$	8, 16, 32	*1	—
RDC3ASn	PHI compare setting register 1	RDC3ASnPHICP1	<RDC3ASn_base>+0010_H	8, 16, 32	*1	—
RDC3ASn	PHI compare setting register 2	RDC3ASnPHICP2	<RDC3ASn_base>+0014_H	8, 16, 32	*1	—
RDC3ASn	Sine/cosine angle correction register	RDC3ASnSCCOR0	<RDC3ASn_base>+0018_H	8, 16, 32	*1	—
RDC3ASn	Sine/cosine correction register 1	RDC3ASnSCCOR1	<RDC3ASn_base>+$001C_H$	8, 16, 32	*1	—
RDC3ASn	Sine/cosine correction register 2	RDC3ASnSCCOR2	<RDC3ASn_base>+0020_H	8, 16, 32	*1	—
RDC3ASn	Sine/cosine correction register 3	RDC3ASnSCCOR3	<RDC3ASn_base>+0024_H	8, 16, 32	*1	—
RDC3ASn	Error detection register 0	RDC3ASnDIAG0	<RDC3ASn_base>+0030_H	8, 16, 32	*1	—
RDC3ASn	Error detection register 1	RDC3ASnDIAG1	<RDC3ASn_base>+0034_H	8, 16, 32	*1	—
RDC3ASn	Error detection register 2	RDC3ASnDIAG2	<RDC3ASn_base>+0038_H	8, 16, 32	*1	—
RDC3ASn	Error detection output register 0	RDC3ASnDGOUT0	<RDC3ASn_base>+$003C_H$	8, 16, 32	*1	—
RDC3ASn	Error detection output register 1	RDC3ASnDGOUT1	<RDC3ASn_base>+0040_H	8, 16, 32	*1	—
RDC3ASn	BIST register 0	RDC3ASnBIST0	<RDC3ASn_base>+0044_H	8, 16, 32	*1	—
RDC3ASn	BIST register 1	RDC3ASnBIST1	<RDC3ASn_base>+0048_H	8, 16, 32	*1	—
RDC3ASn	Excitation setting register	RDC3ASnREF	<RDC3ASn_base>+$004C_H$	8, 16, 32	*1	—
RDC3ASn	Encoder register 0	RDC3ASnENC0	<RDC3ASn_base>+0050_H	8, 16, 32	*1	—
RDC3ASn	Encoder register 1	RDC3ASnENC1	<RDC3ASn_base>+0054_H	8, 16, 32	*1	—
RDC3ASn	Encoder register 2	RDC3ASnENC2	<RDC3ASn_base>+0058_H	8, 16, 32	*1	—
RDC3ASn	Angular velocity register	RDC3ASnOMG	<RDC3ASn_base>+$005C_H$	8, 16, 32	*1	—
RDC3ASn	MNT signal register	RDC3ASnETC	<RDC3ASn_base>+0060_H	8, 16, 32	*1	—
RDC3ASn	Test bus register	RDC3ASnTBUS	<RDC3ASn_base>+0064_H	8, 16, 32	*1	—
RDC3ASn	ET control register	RDC3ASnETEN	<RDC3ASn_base>+$006C_H$	8, 16, 32	*1	—
RDC3ASn	ET capture register	RDC3ASnETCAP	<RDC3ASn_base>+0070_H	8, 16, 32	*1	—
RDC3ASn	ET zero-crossing counter register	RDC3ASnETMCNT	<RDC3ASn_base>+0074_H	8, 16, 32	*1	—
RDC3ASn	Error detection register 3	RDC3ASnDIAG3	<RDC3ASn_base>+$00B0_H$	8, 16, 32	*1	—
RDC3ASn	Error detection register 4	RDC3ASnDIAG4	<RDC3ASn_base>+$00B4_H$	8, 16, 32	*1	—
RDC3ASn	Debugging read register 0	RDC3ASnDBG0	<RDC3ASn_base>+$00C0_H$	8, 16, 32	*1	—
RDC3ASn	Debugging read register 1	RDC3ASnDBG1	<RDC3ASn_base>+$00C4_H$	8, 16, 32	*1	—
RDC3ASn	Debugging read register 3	RDC3ASnDBG3	<RDC3ASn_base>+$00CC_H$	8, 16, 32	*1	—

Note 1. n = 0 : PBG40#4
n = 1 : PBG30#5

49.2.2.2 Register Specifications

The detailed register specifications of the RDC are given below.

The addresses and bits which are shown above the register tables are those when access is in 32-bit units.

(1) ΔΣ ADC setting support register (RDC3ASnDSST)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0000_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	DSDL[1:0]		—	—	DSFQ[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W

Table 49.62 RDC3ASnDSST Register Contents

Bit Position	Bit Name	Function
31 to 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5, 4	DSDL[1:0]	ΔΣADC group delay setting ΔΣADC changes the group delay value depending on the setting. Select a setting that will be the same value as the set group delay. b5 b4 group delay 0 0 15us (F1) 0 1 10us (F2) 1 0 32us (F3a,F3b,F4) 1 1 4.5us (F5)
3, 2	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
1, 0	DSFQ[1:0]	ΔΣADC output update frequency setting The output update frequency of ΔΣADC varies depending on the setting. Select the setting that is the same value as the output update frequency set in ΔΣADC. b1 b0 output update frequency 0 0 100kHz (F1a,F3a) 0 1 200kHz (F1b,F3b,F2,F4) 1 0 400kHz (F5) 1 1 100kHz (F1a,F3a)

(2) Control Gain Select Register 0 (RDC3ASnPI0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0004_H

Value after reset: $0002\ 0010_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	KVMS[1:0]		DVW[1:0]		—	KPF	KPS[1:0]		—	KIS[2:0]			—	DEVCK[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LKVS[3:0]				HKVS[3:0]				—	—	—	BWCS	—	LPGS[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Table 49.63 RDC3ASnPI0 Register Contents (1/3)

Bit Position	Bit Name	Function
31, 30	KVMS[1:0]	Kv Gain Method Select Selects the Kv gain method. b31 b30 0 0: 1-step-shifted 12-level AGC (default) 0 1: 1-step-shifted 7-level AGC 1 0: 1-step-shifted 2-level AGC 1 1: Fixed Kv
29, 28	DVW[1:0]	ERR Deviation Weighting Selects weighting of ERR deviation. b29 b28 0 0: ×1 (default) 0 1: ×3 1 0: ×5 1 1: ×7
27	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
26	KPF	Kp Gain Quadruple Selects whether or not to quadruple the gain on the Kp side of the PI compensator.*2 0: Kp gain is not quadrupled. (×1) 1: Kp gain is quadrupled.
25, 24	KPS[1:0]	Kp Gain Select Selects the Kp gain in the PI compensator*2 b25 b24 0 0: ×1 (default) 0 1: ×0.25 1 0: ×0.5 1 1: ×2
23	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 49.63 RDC3ASnPI0 Register Contents (2/3)

Bit Position	Bit Name	Function
22 to 20	KIS[2:0]	Ki Gain Select Sets the Ki gain in the PI compensator. b22 b21 b20 0 0 0: ×1 (default) 0 0 1: ×0.125 0 1 0: ×0.25 0 1 1: ×0.5 1 0 0: ×2 1 0 1: ×4 1 1 0: ×8 1 1 1: ×16
19	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
18 to 16	DEVCK[2:0]	Control Variation Determination Clock Select*3 Selects the clock period used for determining the control variation. b18 b17 b16 0 0 0: 50 µs*1 clock period 0 0 1: 100 µs*1 clock period 0 1 0: 200 µs*1 clock period (default) 0 1 1: 25 µs*1 clock period 1 0 0: 400 µs*1 clock period 1 0 1: 800 µs*1 clock period 1 1 0: 50 µs*1 clock period 1 1 1: 50 µs*1 clock period
15 to 12	LKVS[3:0]	Low Kv Gain Select Sets the gain in the lower Kv side when the fixed Kv method or 2-level AGC method is selected.*4 b15 b14 b13 b12 0 0 0 0: ×1 (default) 0 0 0 1: ×0.0625 0 0 1 0: ×0.125 0 0 1 1: ×0.25 0 1 0 0: ×0.5 0 1 0 1: ×1 0 1 1 0: ×2 0 1 1 1: ×4 1 0 0 0: ×8 1 0 0 1: ×16 1 0 1 0: ×32 1 0 1 1: ×64 1 1 0 0: ×128 1 1 0 1: ×1 1 1 1 0: ×1 1 1 1 1: ×1
11 to 8	HKVS[3:0]	High Kv Gain Select Sets the gain in the higher Kv side when the fixed Kv method or 2-level AGC method is selected.*4 b11 b10 b9 b8 0 0 0 0: ×32 (default) 0 0 0 1: ×0.0625 0 0 1 0: ×0.125 0 0 1 1: ×0.25 0 1 0 0: ×0.5 0 1 0 1: ×1 0 1 1 0: ×2 0 1 1 1: ×4 1 0 0 0: ×8 1 0 0 1: ×16 1 0 1 0: ×32 1 0 1 1: ×64 1 1 0 0: ×128 1 1 0 1: ×32 1 1 1 0: ×32 1 1 1 1: ×32

Table 49.63 RDC3ASnPI0 Register Contents (3/3)

Bit Position	Bit Name	Function
7 to 5	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
4	BWCS	Bandwidth Setting Selects the PI compensator setting method. 0: Sets the coefficients by using the RDC3ASnPI0 register. 1: Using the LPGS[2:0] bits in this register (see the description in the LPGS[2:0] for the set value.)
3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2 to 0	LPGS[2:0]	Loop Gain Select By setting the BWCS bit in this register to 1, the LPGS[2:0] bits are enabled and the PI compensator can be set by using them. See **Table 49.70**.

Note 1. The timing value is when the CCLK is running at 40 MHz.

Note 2. The combinations of the settings of the DVW[1:0], KPS[1:0], KPF, and HKVS[3:0] bits in the RDC3ASnPI0 register listed in **Table 49.64**, **Table 49.65** are prohibited. In the combinations listed in these tables, the P component in the PI compensator overflows, resulting in an unexpected value if the Kv gain is large.

Note 3. Set the control variation determination clock period to be longer than twice the excitation signal period currently used. For example, when a 10 kHz (100 µs period) excitation signal is used, set the clock period for judging control deviations to 200, 400 or 800 µs. Do not set 100 µs, 50 µs or 25 µs. If the angle conversion operation is unstable, it may be stabilized by setting these bits to a longer time setting.

Note 4. Set HKVS[3:0] gain to be larger than LKVS[3:0] gain.

Table 49.64 Prohibited Combinations of DVW[1:0], KPS[1:0], and KPF When KVMS[1:0] = 00 or 01 (in the case of the 12- or 7- level AGC)

DVW[1:0]	KPS[1:0]	KPF
00 (x1)	11 (x2)	1 (x4)
01 (x3)	11 (x2)	1 (x4)
01 (x3)	00 (x1)	1 (x4)
10 (x5)	11 (x2)	1 (x4)
10 (x5)	11 (x2)	0 (x1)
10 (x5)	00 (x1)	1 (x4)
10 (x5)	10 (x0.5)	1 (x4)
11 (x7)	11 (x2)	1 (x4)
11 (x7)	11 (x2)	0 (x1)
11 (x7)	00 (x1)	1 (x4)
11 (x7)	10 (x0.5)	1 (x4)

Table 49.65 Prohibited Combinations of DVW[1:0], KPS[1:0], KPF, and HKVS[3:0] When KVMS[1:0] = 10 or 11 (in the case of the 2-level AGC or fixed Kv)

DVW[1:0]	KPS[1:0]	KPF	HKVS[3:0]
00 (x1)	11 (x2)	1 (x4)	1100 (x128)
01 (x3)	11 (x2)	1 (x4)	1100 (x128)
01 (x3)	11 (x2)	1 (x4)	1011 (x64)
01 (x3)	00 (x1)	1 (x4)	1100 (x128)
10 (x5)	11 (x2)	1 (x4)	1100 (x128)
10 (x5)	11 (x2)	1 (x4)	1011 (x64)
10 (x5)	11 (x2)	1 (x4)	1010 (x32)
10 (x5)	11 (x2)	0 (x1)	1100 (x128)
10 (x5)	00 (x1)	1 (x4)	1100 (x128)
10 (x5)	00 (x1)	1 (x4)	1011 (x64)

Table 49.65 Prohibited Combinations of DVW[1:0], KPS[1:0], KPF, and HKVS[3:0] When KVMS[1:0] = 10 or 11 (in the case of the 2-level AGC or fixed Kv)

DVW[1:0]	KPS[1:0]	KPF	HKVS[3:0]
10 (x5)	10 (x0.5)	1 (x4)	1100 (x128)
11 (x7)	11 (x2)	1 (x4)	1100 (x128)
11 (x7)	11 (x2)	1 (x4)	1011 (x64)
11 (x7)	11 (x2)	1 (x4)	1010 (x32)
11 (x7)	11 (x2)	0 (x1)	1100 (x128)
11 (x7)	00 (x1)	1 (x4)	1100 (x128)
11 (x7)	00 (x1)	1 (x4)	1011 (x64)
11 (x7)	10 (x0.5)	1 (x4)	1100 (x128)

[Kv Gain Method Selection Bits]

These bits select the method for the Kv gain in the PI compensator. When the AGC (auto gain control) method is selected, the Kv gain is automatically selected according to the amount of control deviation. It is recommended to use the default setting (12-level AGC method).

- 12-level AGC method (the default setting)

Table 49.66 lists the control variation amount and the value of the selected Kv gain for the 12-level AGC. The control variation amount indicates a bias of control variation ε (High or Low) within the determination clock period. With regard to the resolver angle signal θ and the R/D converter output angle signal ϕ, the High and the Low appear in equal proportions if θ and ϕ are equal. In such a case, the control variation amount is ± 0%. If ϕ is completely behind θ, the ε always becomes high. In this case, the control variation amount is +100%. If ϕ is completely ahead of θ, ε always becomes Low. In this case, the control variation amount is –100%. The determination clock period can be selected by the DEVCK[2:0] bits.

The HKVLM[3:0] bits and LKVLM[3:0] bits can be used to set the upper and lower limits on the selected Kv gain during AGC operation. However, in the AGCON state, the Kv gain shifts to the initial value (large gain) once, and then the limit value is applied after it falls below the high gain limit value specified by the HKVLM[3:0] bits.

Table 49.66 Amounts of Control Deviation and Kv Gain Values in the Case of the 12-Level AGC (1/2)

Amount of Control Deviation	Kv Gain
After release from the reset	×128
-100% to -76.8%, +76.8% to +100%	×64
-76.8% to -64.0%, +64.0% to +76.8%	×32
-64.0% to -57.6%, +57.6% to +64.0%	×16
-57.6% to -51.2%, +51.2% to +57.6%	×8
-51.2% to -44.8%, +44.8% to +51.2%	×4
-44.8% to -38.4%, +38.4% to +44.8%	×2
-38.4% to -32.0%, +32.0% to +38.4%	×1
-32.0% to -25.6%, +25.6% to +32.0%	×0.5

Table 49.66 Amounts of Control Deviation and Kv Gain Values in the Case of the 12-Level AGC (2/2)

Amount of Control Deviation	Kv Gain
-25.6% to -19.2%, +19.2% to +25.6%	×0.25
-19.2% to -12.8%, +12.8% to +19.2%	×0.125
-12.8% to +12.8%	×0.0625

If the Kv gain falls below ×128 after release from the reset state, the Kv returns to ×128 on either of the following conditions:

1. The KIRST bit is set to 1 when the AGDS bit is 0 (Ki reset).
2. Recovery from the resolver signal error state when the AGDS bit is 0

The Kv gain does not return to ×128 on the above conditions when the AGDS bit is 1.

- 7-level AGC method

Table 49.67 lists the control variation amount and the value of the selected Kv gain for the 7-level AGC.

Table 49.67 Control Variation Amount and Kv Gain for 7-Level AGC

Amount of Control Deviation	Kv Gain
After release from the reset	×128
-100% to -76%, +76.8% to +100%	×64
-76.8% to -51.2%, +51.2% to +76.8%	×16
-51.2% to -38.4%, +38.4% to +51.2%	×4
-38.4% to -25.6%, +25.6% to +38.4%	×1
-25.6% to -12.8%, +12.8% to +25.6%	×0.25
-12.8% to +12.8%	×0.0625

If the Kv gain falls below ×128 after release from the reset state, the Kv returns to ×128 on either of the following conditions:

1. The KIRST bit is set to 1 when the AGDS bit is 0 (Ki reset)
2. Recovery from the resolver signal error state when the AGDS bit is 0.

The Kv gain does not return to ×128 on the above conditions when the AGDS bit is 1.

The HKVLM[3:0] bits and LKVLM[3:0] bits can be used to set the upper and lower limits on the selected Kv gain during AGC operation. However, in the AGCON state, the Kv gain shifts to the initial value (large gain) once, and then the limit value is applied after it falls below the high gain limit value specified by the HKVLM [3: 0] bits.

- 2-level AGC method

Table 49.68 lists the control variation amount and the value of the selected Kv gain for the 2-level AGC. The low and high gains can be set using bits LKVS[3:0] and HKVS[3:0], respectively.

Table 49.68 Control Variation Amount and Kv Gain for 2-Level AGC

Amount of Control Deviation	Kv Gain
-100% to -76.8%, +76.8% to +100%	Makes transition to the high Kv gain
-76.8% to -25.6%, +25.6% to +76.8%	Kv gain maintained (no transition)
-25.6% to +25.6%	Makes transition to the low Kv gain

If the Kv gain falls below ×128 after release from the reset state, the Kv returns to ×128 on either of the following conditions:

1. The KIRST bit is set to 1 when the AGDS bit is 0 (Ki reset).

2. Recovery from the resolver signal error state when the AGDS bit is 0.

The Kv gain does not return to ×128 on the above conditions when the AGDS bit is 1.

- Fixed Kv method

If the fixed Kv method is selected, the module operates with the low Kv gain irrespective of the amount of control deviation. The module, however, makes a transition to the high Kv gain only when an error is detected and then the error signal makes a transition to 0 (recovery from the error). After that, the module makes a transition to the low Kv gain side when the absolute value of the amount of control deviation falls below 25.6%.

- Control Variation Amount Monitoring

The control variation amount can be read from DATA[7:0] bits in the RDC3ASnTBUS register by setting DATSEL[6:0] bits in the RDC3ASnTBUS register to $2F_H$. Values read are expressed as two's complements. The control variation is ± 0% under the ideal condition where the resolver input angle exactly matches the phi digital angle output ($\theta = \phi$).

Table 49.69 Relationship between the Bits of the RDC3ASnTBUS Register and Control Variation Values (%)

Bit	Control Deviation Value (%)
7	Sign (0: +, 1: –)
6	50
5	25
4	12.5
3	6.25
2	3.13
1	1.56
0	0.78

For example, If the result of reading the control deviation value is 07_H, the control deviation value is +5.47%.

[Loop Gain Selection Bits]

Table 49.70 shows the relation between the combination of the LPGS[2:0] bits and the PI compensator settings when the BWCS bit is 1.

Table 49.70 LPGS[2:0] and Corresponding Settings in the PI Compensator

	LPGS[2:0]			PI Compensator Settings
BWCS	b2	b1	b0	Bandwidth
0	X	X	X	Set by the RDC3ASnPI0 register
1	0	0	0	800Hz
1	0	0	1	Setting prohibited
1	0	1	0	Setting prohibited
1	0	1	1	1500Hz
1	1	0	0	1000Hz
1	1	0	1	500Hz
1	1	1	0	200Hz
1	1	1	1	Automatic adjustment

Note: The default setting is b2:b0 = 000 which sets the bandwidth as 800 Hz.

(3) Control Gain Select Register 1 (RDC3ASnPI1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0008_H

Value after reset: $0001\ 1B01_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	SAGD	—	—	—	AGCD	AGST[3:0]				—	—	—	AGDS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HKVLM[3:0]				LKVLM[3:0]				—		—		—	MAXV[2:0]		
Value after reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Table 49.71 RDC3ASnPI1 Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
28	SAGD	Short-Period BIST Recovery AGCON Disable This bit controls whether the R/D converter makes a transition to the AGCON state on completion of a short-period BIST. 0: The AGCON function is used. 1: The AGCON function is not used.
27 to 25	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
24	AGCD	AGCON Disable Selects whether or not to use the AGCON function.*1 0: The AGCON function is used. 1: The AGCON function is not used.
23 to 20	AGST[3:0]	Short-Period BIST Recovery Initial AGC Gain Sets the initial value for the Kv gain on transitions to the AGCON state after completion of a short-period BIST. b23 b22 b21 b20 Initial Kv gain 0 0 0 0 ×4 0 0 0 1 ×0.0625 0 0 1 0 ×0.125 0 0 1 1 ×0.25 0 1 0 0 ×0.5 0 1 0 1 ×1 0 1 1 0 ×2 0 1 1 1 ×4 1 0 0 0 ×8 1 0 0 1 ×16 1 0 1 0 ×32 1 0 1 1 ×64 1 1 0 0 ×128 1 1 0 1 ×4 1 1 1 0 ×4 1 1 1 1 ×4
19 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 49.71 RDC3ASnPI1 Register Contents (2/2)

Bit Position	Bit Name	Function
16	AGDS	AGC Kv High Gain Transition Restriction Restricts the AGC Kv gain from going high. 0: The Kv goes high on recovery from resolver signal error or after a Ki reset. 12-level AGC is selected: Kv is fixed to ×128 7-level AGC is selected: Kv is fixed to ×128 2-level AGC is selected: Kv is fixed to the higher side 1: The Kv does not go high on recovery from resolver signal error or after a Ki reset.
15 to 12	HKVLM[3:0]	AGC High Gain Limit Setting These bits set the limit on the higher gain side when the 12-level AGC or 7-level AGC is used.*2 b15 b14 b13 b12 High gain limit value 0 0 0 0 X64 (setting prohibited) 0 0 0 1 X64 (7 levels can be set) 0 0 1 0 X32 0 0 1 1 X16 (7 levels can be set) 0 1 0 0 X8 0 1 0 1 X4 (7 levels can be set) 0 1 1 0 X2 0 1 1 1 X1 (7 levels can be set) 1 0 0 0 X0.5 1 0 0 1 X0.25 (7 levels can be set) 1 0 1 0 X0.125 1 0 1 1 X0.0625 (7 levels can be set) 1 1 0 0 X0.0625 (setting prohibited) 1 1 0 1 X0.0625 (setting prohibited) 1 1 1 0 X0.0625 (setting prohibited) 1 1 1 1 X0.0625 (setting prohibited) Set these bits to 0001 if the 2-level AGC or fixed Kv method is used. In the case of 7-level AGC, the settings indicated as (7 levels can be set) given above are only available.
11 to 8	LKVLM[3:0]	AGC Low Gain Limit Setting These bits set the limit on the lower gain side when the 12-level AGC or 7-level AGC is used.*2 b11 b10 b9 b8 Low gain limit value 0 0 0 0 X64 (setting prohibited) 0 0 0 1 X64 (7 levels can be set) 0 0 1 0 X32 0 0 1 1 X16 (7 levels can be set) 0 1 0 0 X8 0 1 0 1 X4 (7 levels can be set) 0 1 1 0 X2 0 1 1 1 X1 (7 levels can be set) 1 0 0 0 X0.5 1 0 0 1 X0.25 (7 levels can be set) 1 0 1 0 X0.125 1 0 1 1 X0.0625 (7 levels can be set) 1 1 0 0 X0.0625 (setting prohibited) 1 1 0 1 X0.0625 (setting prohibited) 1 1 1 0 X0.0625 (setting prohibited) 1 1 1 1 X0.0625 (setting prohibited) Set these bits to 1011 if the 2-level AGC or fixed Kv method is used. In the case of 7-level AGC, the settings indicated as (7 levels can be set) given above are only available. The LKVLM bits must select a setting that is lower than the range of gains specified by the HKVLM bits.
7 to 3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2 to 0	MAXV[2:0]	Maximum Angular Velocity Select These bits set the maximum angular velocity. See **Table 49.72**

Note 1. To change the setting of AGCD, write 1 to the KIRST bit after the setting has been changed. Otherwise, the phi angle values are output under the free-running state. The setting of AGCD should be changed while the

resolver is not running.

Note 2. Set HKVLM[3:0] gain to be larger than LKVLM[3:0] gain.

[Maximum Angular Velocity Selection Bits]

Table 49.72 lists the maximum angular velocity selected by the MAXV bits and corresponding R/D conversion resolutions.

Table 49.72 Maximum Angular Velocity Selection Bit Settings

When the RDC clock frequency is 40 MHz				
b2	**b1**	**b0**	**Maximum Angular Velocity (in min^{-1})**	**Resolution (in bits)**
0	0	0	120000*1	13
0	0	1	240000*1	12(default)
0	1	0	480000*1	11
0	1	1	960000*1	10
1	0	0	15000*1	16
1	0	1	60000*1	14
1	1	0	240000*1	12
1	1	1	240000*1	12

Note 1. It is value for operation with CCLK running at 40 MHz.

(4) PHI Compare Setting Register 0(RDC3ASnPHICP0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$000C_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	INTCLR[2:0]			—	—	—	—	—	—	—	IRS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	INTFLG[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.73 RDC3ASnPHICP0 Register Contents

Bit Position	Bit Name	Function
31 to 27	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
26	INTCLR[2]	Compare Match Interrupt 2 Clear Writing 1 to this bit clears the INTFLG[2] bit to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
25	INTCLR[1]	Compare Match Interrupt 1 Clear Writing 1 to this bit clears the INTFLG[1] bit to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
24	INTCLR[0]	Compare Match Interrupt 0 Clear Writing 1 to this bit clears the INTFLG[0] bit to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
23 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	IRS	Compare Match Interrupt Request Signal Select 0: Compare match signal 1: Signal latching compare match signal
15 to 3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2	INTFLG[2]	Compare Match Interrupt 2 Flag 0: Interrupt request has not been generated. 1: Interrupt request has been generated. This bit is in the scope of control by the PHIERLK bit.
1	INTFLG[1]	Compare Match Interrupt 1 Flag 0: Interrupt request has not been generated. 1: Interrupt request has been generated. This bit is in the scope of control by the PHIERLK bit.
0	INTFLG[0]	Compare Match Interrupt 0 Flag 0: Interrupt request has not been generated. 1: Interrupt request has been generated. This bit is in the scope of control by the PHIERLK bit.

Note: Even if an error occurs when PHIERLK bit is 1, the latching compare match interrupt signal and INTFLG[2:0] bits are cleared by INTCLR[2:0] bits.

(5) PHI Compare Setting Register 1(RDC3ASnPHICP1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0010_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CMP1[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMP0[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.74 RDC3ASnPHICP1 Register Contents

Bit Position	Bit Name	Function
31 to 16	CMP1[15:0]	Phi Compare Value 1 Sets the angle compare value with a 16-bit width.
15 to 0	CMP0[15:0]	Phi Compare Value 0 Sets the angle compare value with a 16-bit width.

(6) PHI Compare Setting Register 2(RDC3ASnPHICP2)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0014_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMP2[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.75 RDC3ASnPHICP2 Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
15 to 0	CMP2[15:0]	Phi Compare Value 2 Sets the angle compare value with a 16-bit width.

(7) Sine/Cosine Angle Correction Register (RDC3ASnSCCOR0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0018_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	COSPO[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SINPO[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.76 RDC3ASnSCCOR0 Register Contents

Bit Position	Bit Name	Function
31 to 28	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
27 to 16	COSPO[11:0]	Cosine Angle Correction Specifies the angular correction value for the phi to be input to the COS ROM table as a 12-bit singed integer.*1 b27 to b16 000_H: 0° (no correction) $7FF_H$: +180° (maximum correction in the positive direction) 800_H: -180° (maximum correction in the negative direction)
15 to 12	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
11 to 0	SINPO[11:0]	Sine Angle Correction Specifies the angular correction value for the phi to be input to the SIN ROM table as a 12-bit singed integer.*1 b11 to b0 000_H: 0° (no correction) $7FF_H$: +180° (maximum correction in the positive direction) 800_H: -180° (maximum correction in the negative direction)

Note 1. Set 000_H (0°) in these bits when executing an angle conversion BIST.

(8) Sine/Cosine Correction Register 1 (RDC3ASnSCCOR1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+001C$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	PHCST	—	GNCST	CMCLT[1:0]		CMCSL[1:0]		GNCLT[1:0]		GNCSL[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PHCLT[1:0]		PHCSL[1:0]		—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Table 49.77 RDC3ASnSCCOR1 Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 27	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
26	PHCST	Phase Correction Start Writing 1 to this bit starts phase correction. Set this bit to 1 after the RDC has entered the angular tracking state. This bit returns to 0 after one or two clock cycles has elapsed following it being set to 1. This bit is effective only for once after a reset.
25	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
24	GNCST	Gain Correction Start Writing 1 to this bit starts gain correction and common offset correction. Set this bit to 1 after the RDC has entered the angular tracking state and the resolver has rotated through an electrical angle of at least 180°. This bit returns to 0 after one or two clock cycles has elapsed following it being set to 1.
23, 22	CMCLT[1:0]	Common Offset Correction Limit Sets limitation for the range of correcting the common offset value. If the value for correction obtained from the input signal exceeds the set limitation, the set value is used for correction. b23 b22 Limitation on the value for correction 0 0: ± 0.0312 × (ADSVREFH - ADSVREFL) (approx. ± 150 mV) (default) 0 1: ± 0.0156 × (ADSVREFH - ADSVREFL) (approx. ± 78 m V) 1 0: ± 0.125 × (ADSVREFH - ADSVREFL) (approx. ± 625 mV) 1 1: ± 0 × (ADSVREFH - ADSVREFL) (± 0 mV) (no correction applied)
21, 20	CMCSL[1:0]	Common Offset Correction Type Select Selects the type of correcting by the common offset value. b21 b20 Type of correction 0 0: No correction (fixed to 00$_H$, this is the default setting) 0 1: Always use the fixed offset correction value set by CSOSN[9:0] and CCOSN[9:0]. 1 0: Use the offset correction value obtained from the calculation. The timing to apply this value depends on the setting of the GNCSL bit. 1 1: Setting prohibited

Table 49.77 RDC3ASnSCCOR1 Register Contents (2/2)

Bit Position	Bit Name	Function
19, 18	GNCLT[1:0]	Gain Correction Range Limit Sets limitation for the range of correcting the gain value. If the value for correction obtained from the input signal exceeds the set limitation, the set value is used for correction. b19 b18 Limitation on the value for correction 0 0: ± 20% (default) 0 1: ± 10% 1 0: ± 40% 1 1: ± 0% (no correction applied)
17, 16	GNCSL[1:0]	Gain Correction Type Select Selects the type of correcting by the gain value. b17 b16 Type of correction 0 0: No correction (fixed to 1024, this is the default setting) 0 1: Always use the fixed correction value set by GNCNM[11:0] 1 0: Use the correction value obtained from the calculation at the time of GNCST being set 1 1: Use the correction value obtained from the calculation at the time of z-phase output following GNCST being set (correct the value on every single rotation).
15 to 12	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
11, 10	PHCLT[1:0]	Phase Correction Limit Sets limitation for the range of correcting the sine and cosine phases. If the value for delay obtained from the input signal exceeds the set limitation, the set value is used for delay compensation. b11 b10 Limitation of delay compensation 0 0: 3 µs (default) 0 1: 1 µs 1 0: 6 µs 1 1: 0 µs (no correction applied)
9, 8	PHCSL[1:0]	Sine/Cosine Phase Correction Type Select Selects the type of correction for the sine and cosine phases. b9 b8 Type of correction 0 0: No correction (default) 0 1: After writing 1 to the PHCST bit, the phase difference at 16 crossings of the excitation signal is constantly averaged to obtain the correction value. 1 0: Every time 1 is written to the PHCST bit, the phase difference at 16 crossings of the excitation signal is averaged once to obtain the correction value, and then the correction value is used. 1 1: Use the fixed correction value set by PHCNM[5:0] and PHSNM[5:0].
7 to 0	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

(9) Sine/Cosine Correction Register 2(RDC3ASnSCCOR2)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0020_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	GNCNM[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PHCNM[5:0]						—	—	PHSNM[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.78 RDC3ASnSCCOR2 Register Contents

Bit Position	Bit Name	Function
31 to 28	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
27 to 16	GNCNM[11:0]	Gain Correction Fixed Value Sets the fixed value for use in gain correction. The value obtained from the calculation below is multiplied by the gain value for the cosine side. – Value for correction of the cosine side = d'(GNCNM[11:0])/1024 Set these bits to 1024 (multiplication by 1) for no correction. If $1178(49A_H)$ is set, for example, the value for the cosine side is corrected by +15%.
15, 14	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
13 to 8	PHCNM[5:0]	Cosine Side Phase Correction Fixed Value Sets the fixed value for use in correction of the phase (amount of delay) of the cosine side. The value for delay obtained from the calculation below is inserted on the cosine side. – Value for delay of the cosine side = d'(PHCNM[5:0]) × 200 ns The setting from $3F_H$ to $1F_H$ are not allowed. Allowed values are between 0 µs to 6 µs
7, 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	PHSNM[5:0]	Sine Side Phase Correction Fixed Value Sets the fixed value for use in correction of the phase (amount of delay) of the sine side. The value for delay obtained from the calculation below is inserted on the sine side. – Value for delay of the sine side = d'(PHSNM[5:0]) × 200 ns The setting from $3F_H$ to $1F_H$ are not allowed. Allowed values are between 0 µs to 6 µs.

(10) Sine/Cosine Correction Register 3 (RDC3ASnSCCOR3)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0024_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CCOSN[9:0]									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CSOSN[9:0]									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.79 RDC3ASnSCCOR3 Register Contents

Bit Position	Bit Name	Function
31 to 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
27 to 16	CCOSN[9:0]	Cosine Side Common Offset Correction Fixed Value Setting Sets the fixed value (two's complement) for use in correction of the cosine side common value. The value obtained from the calculation below is subtracted from the result of A/D conversion. – Common offset value of the cosine side = d'(CCOSN[9:0]) × (ADSVREFH - ADSVREFL)/4096 (V)
15 to 10	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
9 to 0	CSOSN[9:0]	Sine Side Common Offset Correction Fixed Value Setting Sets the fixed value (two's complement) for use in correction of the sine side common value. The value obtained from the calculation below is subtracted from the result of A/D conversion. – Common offset value of the sine side = d'(CSOSN[9:0]) × (ADSVREFH - ADSVREFL)/4096 (V)

(11) Error Detection Register 0 (RDC3ASnDIAG0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0030_H

Value after reset: $001A\ 2933_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	P2ANT[1:0]		EXCETH[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SGBTH[7:0]								SGBDTH[7:0]							
Value after reset	0	0	1	0	1	0	0	1	0	0	1	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.80 RDC3ASnDIAG0 Register Contents

Bit Position	Bit Name	Function
31 to 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25, 24	P2ANT [1:0]	Two Paths Conversions Error Threshold These bits set the threshold for two-path conversion error in comparison between the results from conversion loop 0 and 1. b25 b24 Threshold for comparison 0 0 ±8 LSB (with 12-bit resolution) 0 1 ±4 LSB (with 12-bit resolution) 1 0 ±32 LSB (with 12-bit resolution) 1 1 ±64 LSB (with 12-bit resolution)
23 to 16	EXCETH[7:0]	Resolver Signal Error Comparison Threshold Sets the threshold for use in detecting errors in the resolver signal. The threshold is obtained from the formula below. – Threshold value = 2 × d'(EXCETH[7:0]) × 8 × (ADSVREFH - ADSVREFL)/4096 (Vpp) Default setting $1A_H$: 0.102 × (ADSVREFH - ADSVREFL) (Vpp)
15 to 8	SGBTH[7:0]	Disconnect Error Comparison Threshold (for VR Resolver) Sets the threshold for use in detecting disconnect errors when the VR resolver is used. The threshold is obtained from the formula below. – Threshold value = d'(SGBTH[7:0]) × 8×(ADSVREFH - ADSVREFL)/4096 (V) Default setting 29_H: 0.08 × (ADSVREFH - ADSVREFL) (V)
7 to 0	SGBDTH[7:0]	Disconnect Error Comparison Threshold Setting (for DC Resolver) Sets the threshold for use in detecting disconnect errors when the DC resolver is used. The threshold is obtained from the formula below. – Threshold value = (d'(SGBDTH[7:0]) × 8 + 1024) × (ADSVREFH - ADSVREFL)/4096 (V) Default setting 33_H: 0.35 × (ADSVREFH - ADSVREFL) (V)

(12) Error Detection Register 1(RDC3ASnDIAG1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0034_H

Value after reset: $B000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	CVEDS	EDPS[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	ERDEN	—	SQERST	—	ERRST	—	—	—	—	—	—	—	KIRST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R/W	R	R/W	R	R	R	R	R	R	R	R/W

Table 49.81 RDC3ASnDIAG1 Register Contents (1/2)

Bit Position	Bit Name	Function
31	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
30	CVEDS	Conversion Error Detection Circuit Select Selects the conversion error detection circuit. 0: The conversion error detection circuit which supports high-speed rotation of the R/D conversion error detection signal.*2 1: The conversion error detection circuit which does not support high-speed rotation of the R/D conversion error detection signal.
29, 28	EDPS[1:0]	RD Conversion Error Determination Time Select Selects the error determination time for R/D conversion errors*3 b29 b28 0 0: 95.8*1 millisecond*4 0 1: 147*1 millisecond*4 1 0: 4.92*1 millisecond 1 1: 7.37*1 millisecond (default)
27 to 13	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
12	ERDEN	Error Detection Start Error detection is enabled when the error detection output mask is released after 26 milliseconds*1 have elapsed following this bit being set to 1.*5
11	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
10	SQERST	Sum-of-Squares Amplitude Error Excitation Counter Reset Writing 1 to this bit resets the sum-of-squares amplitude error excitation counter to 0. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	ERRST	Error Signal Reset Bit Writing 1 to this bit resets the register bits listed below to 0. Note that each of these bits remains at 1 if an error continues. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1. Register bits: ERHD, ERDEXC, ERDSBC, ERDSBS, ERDSQ, ERDP2, ERDCNV
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 49.81 RDC3ASnDIAG1 Register Contents (2/2)

Bit Position	Bit Name	Function
0	KIRST	Ki Component Reset The values of the Ki integrator and accumulator integrator become 0 by writing 1 to this bit. On reset, the AGCON function is enabled and the Kv gain of the PI compensator goes high. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1. After setting this bit to 1, wait at least 2 us to set it again.

Note 1. The timing value is when the CCLK is running at 40 MHz.

Note 2. Input the excitation signal whose frequency is below 22 kHz when the RD conversion error detection circuit (which supports high-speed rotation) is used (CVEDS = 0).

Note 3. Do not set EDPS[1:0] to a shorter determination time than the current setting while the R/D converter is operating. In other words, the settings below are prohibited;
When EDPS[1:0] = 01, setting EDPS[1:0] to 00, 10, or 11 is prohibited.
When EDPS[1:0] = 00, setting EDPS[1:0] to 10 or 11 is prohibited.
When EDPS[1:0] = 11, setting EDPS[1:0] to 10 is prohibited.
However, changing from 11b to 10b is allowed if the ERDEN bit in the RDC3ASnDIAG1 register is 0 after a reset. After changing the bits, set the ERDEN bit to 1.

Note 4. Do not set this value when the R/D conversion error detection circuit (which supports high-speed rotation) is selected (CVEDS = 0).

Note 5. The functionality of error detection is disabled after a reset. It is enabled after 26 milliseconds since the ERDEN bit has been set to 1. Enabling this functionality by setting this bit to 1 takes effects only once, following a reset (setting this bit to 0 does not disable error detection). To disable this functionality after enabling it, disable interrupts by setting the EINTEN bit to 0. The bits in the RDC3ASnDGOUT0 and RDC3ASnDGOUT1 registers are enabled by the ERDEN bit.

[R/D Conversion Error Determination Time Select Bits]

These bits are used to set the time to determine R/D conversion errors. If control variation(ε) between the input angle and R/D converted angle remains large for more than 50% of the specified determination time, it is regarded as the R/D conversion error and the ERCNV bit in the RDC3ASnDGOUT0 register is set to 1 if the ERCNVS bit selects detection of a conversion error. Furthermore, if the EINTEN bit in the RDC3ASnENC0 register is 1, the ERR and ERHD bits in the RDC3ASnDGOUT0 register are set to 1 and an RDC error interrupt occurs.

(13) Error Detection Register 2 (RDC3ASnDIAG2)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0038_H

Value after reset: $0080\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	EREXCS	ERSBCS	ERSBSS	—	ERSQS	ERP2S	ERCNVS
Value after reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.82 RDC3ASnDIAG2 Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 23	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
22	EREXCS	Resolver Signal Error Select Selects whether or not to output detection of a resolver signal error. 0: Set the bits ERR, ERHD, EREXC, and ERDEXC to 1 on occurrence of a resolver signal error 1: Do not set the bits ERR, ERHD, EREXC, and ERDEXC to 1 on occurrence of a resolver signal error
21	ERSBCS	Disconnection Error (Cosine) Select Selects whether or not to output detection of a disconnect error (cosine side). 0: Set the bits ERR, ERHD, ERSBC, and ERDSBC to 1 on occurrence of a disconnect error (cosine side). 1: Do not set the bits ERR, ERHD, ERSBC, and ERDSBC to 1 on occurrence of a disconnect error (cosine side).
20	ERSBSS	Disconnection Error (Sine) Selection Selects whether or not to output detection of a disconnect error (sine side) 0: Set the bits ERR, ERHD, ERSBS, and ERDSBS to 1 on occurrence of a disconnect error (sine side). 1: Do not set the bits ERR, ERHD, ERSBS, and ERDSBS to 1 on occurrence of a disconnect error (sine side).
19	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
18	ERSQS	Sum-of-Squares Amplitude Error Select Selects whether or not to output detection of a sum-of-squares amplitude error. 0: Set the bits ERR, ERHD, ERSQ, and ERDSQ to 1 on occurrence of a sum-of-squares amplitude error. 1: Do not set the bits ERR, ERHD, ERSQ, and ERDSQ to 1 on occurrence of a sum-of-squares amplitude error.
17	ERP2S	Two Paths Conversion Error Select Selects whether or not to output detection of a two paths conversion error. 0: Set the bits ERR, ERHD, ERP2, and ERDP2 to 1 on occurrence of a two paths conversion error. 1: Do not set the bits ERR, ERHD, ERP2, and ERDP2 to 1 on occurrence of a two paths conversion error.

Table 49.82 RDC3ASnDIAG2 Register Contents (2/2)

Bit Position	Bit Name	Function
16	ERCNVS	Conversion Error Select Selects whether or not to output detection of a conversion error. 0: Set the bits ERR, ERHD, ERCNV, and ERDCNV to 1 on occurrence of a conversion error. 1: Do not set the bits ERR, ERHD, ERCNV, and ERDCNV to 1 on occurrence of a conversion error.
15 to 0	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

(14) Error Detection Output Register 0 (RDC3ASnDGOUT0)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+003C$_H$

Value after reset: 0000 0x00$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	ERR	—	—	—	ERHD	—	EREXC	ERSBC	ERSBS	—	ERSQ	ERP2	ERCNV
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	*	*	*	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.83 RDC3ASnDGOUT0 Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned.
28	ERR	Error This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ASnDIAG2 register is being output. This bit returns to 0 on recovery from the error. This flag is not set to 1 if the EINTEN bit of the RDC3ASnENC0 register is 0.
27 to 25	Reserved	When read, the value after reset is returned.
24	ERHD	Error Hold This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ASnDIAG2 register is being output. This signal is reset to 0 by setting the ERRST bit to 1. Note that this bit remains at 1 if errors occur continuously. This flag is not set to 1 if the EINTEN bit of the RDC3ASnENC0 register is 0.
23	Reserved	When read, the value after reset is returned.
22	EREXC	Resolver Signal Error The value of this flag becomes 1 when a resolver signal error occurs and returns to 0 on recovery from the error.
21	ERSBC	Disconnect Error (Cosine Side) The value of this flag becomes 1 when a disconnect error (cosine side) occurs and returns to 0 on recovery from the error.
20	ERSBS	Disconnect Error (Sine Side) The value of this flag becomes 1 when a disconnect error (sine side) occurs and returns to 0 on recovery from the error.
19	Reserved	When read, the value after reset is returned.
18	ERSQ	Sum-of-Squares Amplitude Error The value of this flag becomes 1 when a sum-of-squares amplitude error occurs. This bit drops to 0 when the abnormal excitation count value is cleared by setting the SQERST bit or ERRST bit to 1 after recovery from Sum-of-Squares amplitude error.
17	ERP2	Two Paths Conversion Error The value of this flag becomes 1 when a two path conversion error occurs and returns to 0 on recovery from the error.

Table 49.83 RDC3ASnDGOUT0 Register Contents (2/2)

Bit Position	Bit Name	Function
16	ERCNV	Conversion Error The value of this flag becomes 1 when a conversion error occurs and returns to 0 on recovery from the error.
15 to 11	Reserved	When read, the value after reset is returned.
10 to 8	Reserved	The read value is undefined.
7 to 0	Reserved	When read, the value after reset is returned.

(15) Error Detection Output Register 1 (RDC3ASnDGOUT1)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0040_H

Value after reset: 0000 $0x00_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	ERR	—	—	—	ERHD	—	ERDEXC	ERDSBC	ERDSBS	—	ERDSQ	ERDP2	ERDCNV
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	*	*	*	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.84 RDC3ASnDGOUT1 Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned.
28	ERR	Error This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ASnDIAG2 register is being output. This bit returns to 0 on recovery from the error. This flag is not set to 1 if the EINTEN bit of the RDC3ASnENC0 register is 0.
27 to 25	Reserved	When read, the value after reset is returned.
24	ERHD	Error Hold This flag is set to 1 if the active level of the detection signal for any of the errors indicated by flags in the RDC3ASnDIAG2 register is being output. This signal is reset to 0 by setting the ERRST bit to 1. Note that this bit remains at 1 if errors occur continuously. This flag is not set to 1 if the EINTEN bit of the RDC3ASnENC0 register is 0.
23	Reserved	When read, the value after reset is returned.
22	ERDEXC	Resolver Signal Error Hold The value of this flag becomes 1 when a resolver signal error occurs. This bit remains at 1 until it is reset by the ERRST bit.
21	ERDSBC	Disconnect Error (Cosine Side) Hold The value of this flag becomes 1 when a disconnect error (cosine side) occurs. This bit remains at 1 until it is reset by the ERRST bit.
20	ERDSBS	Disconnect Error (Sine Side) Hold The value of this flag becomes 1 when a disconnect error (sine side) occurs. This bit remains at 1 until it is reset by the ERRST bit.
19	Reserved	When read, the value after reset is returned.
18	ERDSQ	Sum-of-Squares Amplitude Error Hold The value of this flag becomes 1 when a sum-of-squares amplitude error occurs. This bit remains at 1 until it is reset by the ERRST bit.
17	ERDP2	Two Paths Conversion Error Hold The value of this flag becomes 1 when a two paths conversion error occurs. This bit remains at 1 until it is reset by the ERRST bit.
16	ERDCNV	Conversion Error Hold The value of this flag becomes 1 when a conversion error occurs. This bit remains at 1 until it is reset by the ERRST bit.
15 to 11	Reserved	When read, the value after reset is returned.

Table 49.84 RDC3ASnDGOUT1 Register Contents (2/2)

Bit Position	Bit Name	Function
10 to 8	Reserved	The read value is undefined.
7 to 0	Reserved	When read, the value after reset is returned.

(16) BIST Register 0 (RDC3ASnBIST0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0044_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	ERCVP2D	—	—	—	CBSP2D
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BSTF	—	—	—	—	BISTCD[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.85 RDC3ASnBIST0 Register Contents

Bit Position	Bit Name	Function
31 to 21	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
20	ERCVP2D	Two Paths Conversion Error BIST Disable Selects whether or not to include two paths conversion error in the conversion error BIST. 0: Two paths conversion error is included in the conversion error BIST (default). 1: Two paths conversion error is not included in the conversion error BIST
19 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	CBSP2D	Two Paths Conversion BIST Disable Selects whether or not to include two paths conversion in the conversion BIST. 0: Two paths conversion is included in the conversion BIST (default). 1: Two paths conversion is not included in the conversion BIST.
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	BSTF	BIST Flag This flag indicates whether a BIST is running or not. A BIST is running if the flag is 1, and another BIST cannot be executed while the flag remains 1.
7 to 4	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
3 to 0	BISTCD[3:0]	BIST Result Store The result of BIST is stored in these bits(see **Table 49.86**).

[BIST Result Storage Bits]

The results of BIST executed by the BCON[3:0] bits are stored in the BISTCD[3:0] bits. The relation between the BCON[3:0] and BISTCD[3:0] are shown in **Table 49.86**.

Table 49.86 Contents of BCON[3:0] and BISTCD[3:0]

Bits for Selecting the BIST to be Executed BCON[3:0]				Bits where the result of BIST is Stored BISTCD[3:0]				Contents Indicated by BISTCD[3:0]
b3	b2	b1	b0	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	BEXE is disabled. BISTCD[3:0] = 0000 is stored without any determination.
0	0	0	1	-	-	-	-	Setting prohibited
0	0	1	0	0	0	1	0	The result of sum-of-squares amplitude error detection BIST (low side) was passed.
				1	1	1	1	The result of sum-of-squares amplitude error detection BIST (low side) was failure.
0	0	1	1	0	0	1	1	The result of sum-of-squares amplitude error detection BIST (high side) was passed.
				1	1	1	1	The result of sum-of-squares amplitude error detection BIST (high side) was failure.
0	1	0	0	-	-	-	-	This combination is not allowed.
0	1	0	1	0	1	0	1	The result of the angle conversion BIST1 (0°) was passed.
				1	1	1	1	The result of the angle conversion BIST1 (0°) was failure.
0	1	1	0	0	1	1	0	The result of the angle conversion BIST2 (45°) was passed.
				1	1	1	1	The result of the angle conversion BIST2 (45°) was failure.
0	1	1	1	0	1	1	1	The result of the angle conversion BIST3 (270°) was passed.
				1	1	1	1	The result of the angle conversion BIST3 (270°) was failure.
1	0	0	0	-	-	-	-	This combination is not allowed.
1	0	0	1	1	0	0	1	The result of the resolver signal error detection BIST was passed.
				1	1	1	1	The result of the resolver signal error detection BIST was failure.
1	0	1	0	1	0	1	0	The result of the resolver signal disconnect detection BIST (cosine side) was passed.
				1	1	1	1	The result of the resolver signal disconnect detection BIST (cosine side) was failure.
1	0	1	1	1	0	1	1	The result of the resolver signal disconnect detection BIST (sine side) was passed.
				1	1	1	1	The result of the resolver signal disconnect detection BIST (sine side) was failure.
1	1	0	0	1	1	0	0	The result of the conversion error BIST was passed.
				1	1	1	1	The result of the conversion error BIST was failure.
1	1	0	1	-	-	-	-	This combination is not allowed.
1	1	1	0	-	-	-	-	This combination is not allowed.
1	1	1	1	-	-	-	-	This combination is not allowed.

(17) BIST Register 1 (RDC3ASnBIST1)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0048_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BISTCL
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BEXE	—	—	—	—	BCON[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 49.87 RDC3ASnBIST1 Register Contents

Bit Position	Bit Name	Function
31 to 17	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
16	BISTCL	BIST Result Clear Writing 1 to this bit clears the result of the BIST (BISTCD[3:0]) to 0. This bit is returned to 0 after one or two clock cycles have elapsed following it being set to 1.
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	BEXE	BIST Execution This signal is used for starting a BIST. Setting this bit to 1 leads to execution of a BIST. This bit is returned to 0 after one or two clock cycles have elapsed after having been set to 1. Select the BIST to be executed by the combination of values in BCON[3:0] (see **Table 49.88**).
7 to 4	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
3 to 0	BCON[3:0]	BIST Execution Setting Selects the BIST to be executed (see **Table 49.88**).

[Executing BIST Setting]

The BIST to be executed is selected by the combination of values in the BCON[3:0]. The combination of values in BCON[3:0] and corresponding BIST to be executed are shown in **Table 49.88** BIST to be Selected by BCON[3:0].

Table 49.88 BIST to be Selected by BCON[3:0]

b3	b2	b1	b0	BIST to be Executed
0	0	0	0	BEXE is disabled.
0	0	0	1	Setting prohibited
0	0	1	0	Error detection BIST: sum-of-squares amplitude error detection BIST (low side)
0	0	1	1	Error detection BIST: sum-of-squares amplitude error detection BIST (high side)
0	1	0	0	This combination is not allowed.
0	1	0	1	Angle conversion BIST: target angle 1 (0°)
0	1	1	0	Angle conversion BIST: target angle 2 (45°)
0	1	1	1	Angle conversion BIST: target angle 3 (270°)
1	0	0	0	This combination is not allowed.
1	0	0	1	Fault-detection BIST: Resolver signal fault-detection BIST
1	0	1	0	Fault-detection BIST: Resolver signal disconnection detection BIST (cosine side)
1	0	1	1	Fault-detection BIST: Resolver signal disconnection detection BIST (sine side)
1	1	0	0	Fault-detection BIST: Conversion fault BIST
1	1	0	1	This combination is not allowed.
1	1	1	0	This combination is not allowed.
1	1	1	1	This combination is not allowed.

(18) Excitation Setting Register (RDC3ASnREF)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$004C_H$

Value after reset: $0A00\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	PLSNFS	REFXS	—	SENS	EXIO	—	—	REFINSL[1:0]		—	—	EXRFPSL[1:0]	
Value after reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	REFDLCT[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.89 RDC3ASnREF Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
28	PLSNFS	Excitation Extraction Noise Filter Selects the noise filter for the excitation component extraction circuit. Insert a 2μs noise filter into the sinpls and cospls signals generated from the ΔΣADC acquisition value. 0: The noise filter is not used. 1: The noise filter is used.
27	REFXS	Excitation Component Extraction Function 0: Excitation component extraction function is disabled. 1: Excitation component extraction function is enabled (default)
26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25	SENS	Sensor Selection Selects the required sensor. 0: Use the DC resolver*1 1: Use the VR resolver (default)
24	EXIO	Sensor Selection Selects the required sensor. 0: Use the VR resolver (default) 1: Use the DC resolver*1
23, 22	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
21, 20	REFINSL[1:0]	Input excitation phase signal selection bit Select the excitation phase signal used in RDC b21 b20 1 1: Select excitation phase signal from excitation-ΔΣADC. 1 0: Select excitation phase signal from external PIN. 0 1: Select excitation phase signal from timer in LSI. 0 0: Select excitation phase signal from excitation-ΔΣADC.
19, 18	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 49.89 RDC3ASnREF Register Contents (2/2)

Bit Position	Bit Name	Function
17, 16	EXRFPSL[1:0]	Excitation phase signal shape selection bit Select the shape of the excitation phase signal When the sin waveform excitation signal is received by the ΔΣ ADC, set these bits to 00. b17 b16 1 1: Excitation period square wave 1 0: Setting prohibited 0 1: Excitation period H pulse 0 0: Excitation period square wave
15 to 0	REFDLCT[15:0]	Excitation phase signal delay adjustment counter setting bit Set the necessary adjustment delay amount for the excitation phase signal input from the outside. 1LSB=50ns

Note 1. VR resolver is selected when EXIO = 0 and SENS = 1.
DC resolver is selected when EXIO = 1 and SENS = 0.

(19) Encoder Register 0 (RDC3ASnENC0)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0050_H

Value after reset: $0000\ 0100_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	PHILTSL	OMGLTSL	—	—	PHILT	OMGLT	—	—	—	PHIERLK	XUVW[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	HYSS	—	—	REFZEN	CINTEN	ABEN	UVWEN	ZEN	EINTEN
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.90 RDC3ASnENC0 Register Contents (1/2)

Bit Position	Bit Name	Function
31, 30	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
29	PHILTSL	PHI Output Fixing Select This bit is used to select fixing or non-fixing of the angle value output in the PHI[15:0] register bits in response to a trigger. 0: The value is not fixed. 1: The value is fixed in response to a trigger. Trigger signals: The triggers are writing of 1 to the PHILT bit or a transition of the phi_latch_trg signal to the high level.
28	OMGLTSL	Angular Velocity Output Fixing Select This bit is used to select fixing or non-fixing of the angular velocity value output in the OMG[31:0] register bits in response to a trigger. 0: The value is not fixed. 1: The value is fixed in response to a trigger. Trigger signals: The triggers are writing of 1 to the OMGLT bit or a transition of the omg_latch_trg signal to the high level.
27, 26	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
25	PHILT	PHI Output Fixing Trigger Writing of 1 to this bit can serve as the trigger for fixing of the PHI output. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
24	OMGLT	Angular Velocity Output Fixing Trigger Writing of 1 to this bit can serve as the trigger for fixing of the angular velocity output. This bit becomes 0 after one or two clock cycles have elapsed following it being set to 1.
23, 21	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
20	PHIERLK	PHI Fixing Selection on Error This bit selects whether or not the PHI and Angular Velocity output are fixed at the time of an error (ERHD = 1). 0: The PHI and Angular Velocity output are not fixed 1: The PHI and Angular Velocity output are fixed at the time of an error.

Table 49.90 RDC3ASnENC0 Register Contents (2/2)

Bit Position	Bit Name	Function
19 to 16	XUVW[3:0]	Encoder Pulse Pole Selection Selects the number of poles for the output of the encoder pulses. b19-b16 U phase V phase W phase 1111 X1 X1 X1 1110 X1 X1 X1 1101 X1 X1 X1 1100 X1 X1 X1 1011 X1 X1 X1 1010 X10 X1 X1 1001 X9 X1 X1 1000 X8 X1 X1 0111 X1 X1 X1 0110 X6 X1 X1 0101 X5 X1 X1 0100 X4 X4 X4 0011 X3 X3 X3 0010 X2 X2 X2 0001 X1 X1 X1 0000 X1 X1 X1
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8	HYSS	Hysteresis Output Select Selects whether to output the encoder pulse signal and compare flag signal through the hysteresis circuit or without going through it.*1 0: Outputs the encoder pulse signal and compare flag signal through the hysteresis circuit. 1: Outputs the encoder pulse signal and compare flag signal without going through the hysteresis circuit.
7, 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5	REFZEN	Excitation Zero-Crossing Interrupt Output Enable 0: Output is disabled. 1: Output is enabled
4	CINTEN	Angle Compare Interrupt Enable 0: Interrupt is disabled. 1: Interrupt is enabled.
3	ABEN	A/B Phase Output Enable 0: Output is disabled. 1: Output is enabled.
2	UVWEN	Encoder Pulse U/V/W Phase Output Enable Controls output of the U, V, and W phases of the encoder pulse signal. 0: Output of the encoder pulse signals as the external output signals ENCU, ENCV, or ENCW is disabled and they are fixed to 0. 1: Output of the encoder pulse signals as the external output signals ENCU, ENCV, or ENCW is enabled.
1	ZEN	Z Phase Output and Z Phase Signal Interrupt Enable 0: Output is disabled. 1: Output is enabled.
0	EINTEN	RDC Error Interrupt Enable 0: Interrupt is disabled. 1: Interrupt is enabled.

Note 1. When output through the hysteresis circuit is selected (HYSS = 0), the RD angle conversion resolution should be 12 bits (MAXV = 001).

(20) Encoder Register 1 (RDC3ASnENC1)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0054_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PHI[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	ENCA	ENCB	ENCZ	ENCU	ENCV	ENCW
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.91 RDC3ASnENC1 Register Contents

Bit Position	Bit Name	Function
31 to 16	PHI[15:0]	PHI[15:0] The digitally output PHI angle is stored in these bits with a 16-bit width. PHI[15](MSB) = 180°, PHI[0] (LSB) These bits are in the scope of control by the PHIERLK bit.
15 to 6	Reserved	When read, the value after reset is returned.
5	ENCA	Encoder Pulse A Phase This bit indicates the current state of the A-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
4	ENCB	Encoder Pulse B Phase This bit indicates the current state of the B-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
3	ENCZ	Encoder Pulse Z Phase This bit indicates the current state of the Z-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
2	ENCU	Encoder Pulse U Phase This bit indicates the current state of the U-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
1	ENCV	Encoder Pulse V Phase This bit indicates the current state of the V-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.
0	ENCW	Encoder Pulse W Phase This bit indicates the current state of the W-phase encoder pulses. This bit is in the scope of control by the PHIERLK bit.

(21) Encoder Register 2 (RDC3ASnENC2)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0058_H

Value after reset: $0000\ xxxx_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PHIAD1[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Value after reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.92 RDC3ASnENC2 Register Contents

Bit Position	Bit Name	Function
31 to 16	PHIAD1[15:0]	conversion Loop1 Output PHI[15:0] The digitally output PHI angle from conversion loop1 is stored in these bits with a 16-bit width. PHIAD1[15](MSB) = 180°, PHIAD1[0] (LSB)
15 to 0	Reserved	The read value is undefined.

(22) Angular Velocity Register (RDC3ASnOMG)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$005C_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OMG[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OMG[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.93 RDC3ASnOMG Register Contents

Bit Position	Bit Name	Function
31 to 0	OMG[31:0]	Angular Velocity [31:0] Indicates the amount of change in phi within the measuring period (selected by OMGPTC[1:0]). The resolution is 25-bits. • The notation is two's complement [0] (the LSB) corresponds to $0.07min^{-1}$ and [24] corresponds to $1171875min^{-1}$. The value in [31:25] represents the sign. These bits are in the scope of control by the PHIERLK bit (fixed to 0 min^{-1}).

(23) MNT Signal Register (RDC3ASnETC)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0060_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	SINPK[12:0]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	COSPK[12:0]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.94 RDC3ASnETC Register Contents

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned.
28 to 16	SINPK[12:0]	SINMNT Excitation Peak Indicates the value of SINMNT latched by the excitation peak trigger signal (trg_ad) from the excitation timer (ET). Specifically, the bits are read the voltage of SINMNT at the excitation peak, expressed as a two's complement. SINMNT excitation peak voltage = d'(SINPK[12:0])*(ADSVREFH - ADSVREFL)/4096
15 to 13	Reserved	When read, the value after reset is returned.
12 to 0	COSPK[12:0]	COSMNT Excitation Peak Indicates the value of COSMNT latched by the excitation peak trigger signal (trg_ad) from the excitation timer (ET). Specifically, the bits are read the voltage of COSMNT at the excitation peak, expressed as a two's complement. COSMNT excitation peak voltage = d'(COSPK[12:0])*(ADSVREFH - ADSVREFL)/4096

(24) Test Bus Register (RDC3ASnTBUS)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0064_H

Value after reset: 0000 $XXXX_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	OMGPTC [1:0]		—	—	—	—	—	DATSEL[6:0]						
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[15:0]															
Value after reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.95 RDC3ASnTBUS Register Contents

Bit Position	Bit Name	Function
31, 30	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
29, 28	OMGPTC [1:0]	Angular Velocity Measuring Period Select Selects the period for measuring the amount of change in angle by the angular velocity measuring circuit. b29 b28 0 0: 12.8 µs (default) 0 1: 51.2 µs 1 0: 102.4 µs 1 1: 204.8 µs
27 to 23	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
22 to 16	DATSEL[6:0]	RDC Data Select Outputs the RDC internal data to DATA[15:0] (see **Table 49.96**).
15 to 0	DATA[15:0]	testbus External Output The data selected by the DATSEL[6:0] bits of the RDC3ASnTBUS register are stored in these bits.

[RDC Data Selection Bits]

Table 49.96 testbus Data Selection (1/2)

DATSEL[6:0]	Output Signal (Internal Signal for Evaluation)	Output Destination testbus(X:X) (DATA[X:X])
100.0100	excitation signal obtained by ΔΣADC (2's complement)	[12:0]
100.0011	cosine signal obtained by ΔΣADC (2's complement)	[12:0]
100.0010	sine signal obtained by ΔΣADC (2's complement)	[12:0]
010.1111	Control variation value [7:0] in conversion loop0.	[7:0]
010.1110	Square sum amplitude integral value in sum-of-squares amplitude error circuit (value is updated every excitation period)	[15:0]

Table 49.96 testbus Data Selection (2/2)

DATSEL[6:0]	Output Signal (Internal Signal for Evaluation)	Output Destination testbus(X:X) (DATA[X:X])
010.1101	Square sum value in sum-of-squares amplitude error circuit (value is updated every ΔΣADC output cycle)	[15:0]
001.1101	Offset value of common of COSMNT Offset = d'DATA[9:0]*(ADSVREFH - ADSVREFL)/4096 (V) (2's complement)	[9:0]
001.1100	Offset value of common of SINMNT Offset = d'DATA[9:0]*(ADSVREFH - ADSVREFL)/4096 (V) (2's complement)	[9:0]

The selected data are readable from the testbus pin and the DATA[15:0] bits (testbus read bits).

(25) ET Control Register (RDC3ASnETEN)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+006C$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	REFZSL[1:0]		—	REFETSL	—	—	—	ZCSTRG	—	—	CMPEN	IREN	DREN	ADTEN	ZCES	CNTEN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R/W	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CNT[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.97 RDC3ASnETEN Register Contents (1/2)

Bit Position	Bit Name	Function
31, 30	REFZSL[1:0]	Excitation Zero-Crossing Pulse Select Selects the output method of excitation zero-crossing pulse interrupt signal. b31 b30 Method of output 0 0 A high-level pulse signal is output for one CCLK cycle on the rising and falling edges (0 → 1, 1 → 0) of the excitation zero-crossing signal. 0 1 A high-level pulse signal is output for one CCLK cycle on the rising edges (0 → 1) of the excitation zero-crossing signal. 1 0 A high-level pulse signal is output for one CCLK cycle on the falling edges (1 → 0) of the excitation zero-crossing signal. 1 1 No pulse signals are output.
29	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
28	REFETSL	Excitation Zero-Crossing Select This bit selects the excitation zero-crossing signal for use in the excitation timer (ET). 0The excitation zero-cross signal selected by REFINSL bit 1The zero-crossing of extracted excitation signal When 1 is selected, a signal with a short or long cycle may be output during the excitation extraction follow-up operation.
27 to 25	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
24	ZCSTRG	Software Trigger This is the software trigger for output of the zero-crossing signal from the excitation timer. 0: No operation. 1: Outputs a trigger. **CAUTION** Writing 1 to this bit outputs one CCLK cycle trigger pulse. Reading this bit always returns 0.
23, 22	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
21	CMPEN	Compare Match Function Enable Enables and disables the compare match function. 0: Disables the compare match function. 1: Enables the compare match function.

Table 49.97 RDC3ASnETEN Register Contents (2/2)

Bit Position	Bit Name	Function
20	IREN	Interrupt Request Enable Enables and disables interrupt requests. 0: Disables the output of interrupt. 1: Enables the output of interrupt.
19	DREN	DMA Request Enable Enables and disables DMA requests. 0: Disables the DMA requests. 1: Enables the DMA requests.
18	ADTEN	A/D Conversion Start Trigger Enable Enables and disables the AD conversion start trigger. 0: Disables the A/D conversion start trigger. 1: Enables the A/D conversion start trigger.
17	ZCES	Zero-Crossing Signal Edge Select Selects the edge on the zero-crossing signal to be detected. 0: Detects the rising edge on the zero-crossing signal. 1: Detects the falling edge on the zero-crossing signal.
16	CNTEN	Counter Operation Enable This is the count enable signal for the period measurement timer and the event timer. 0: Operation of the period measurement timer and the event timer is stopped. The value of the reload register is read into the ET counter. 1: The period measurement timer and the event timer are operated.
15 to 0	CNT[15:0]	ET Counter Register The data from the ET counter is stored in these bits.

(26) ET Capture Register (RDC3ASnETCAP)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0070_H

Value after reset: $0000\ FFFF_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAP[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMP[15:0]															
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.98 RDC3ASnETCAP Register Contents

Bit Position	Bit Name	Function
31 to 16	CAP[15:0]	ET Capture [1]This register captures the data from the ET zero-crossing period measurement counter on detection of a zero-crossing signal. [2] This register captures the data from the ET zero-crossing period measurement counter on a match of the values in the counter and that in the compare match register, when compare match is enabled. [3] In other cases, this register holds the previous captured value.
15 to 0	CMP[15:0]	ET Compare [1]This register captures the value from the ET zero-crossing period measurement counter into CAP[15:0] on a match of the values in the counter and that in this register, and initializes the counter to 0000_H. [2] An excitation timer interrupt request is issued in the cycle after one in which the value in the ET zero-crossing period measurement counter matches that of this register.

(27) ET Zero-Crossing Counter Register (RDC3ASnETMCNT)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+0074_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CNT[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RLD[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.99 RDC3ASnETMCNT Register Contents

Bit Position	Bit Name	Function
31 to 16	CNT[15:0]	Zero-Crossing Period Measurement Counter These bits hold the value of the zero-crossing period measurement counter.
15 to 0	RLD[15:0]	ET Reload The initial value of the ET counter is set in 16 bits. The value should be at least 0002_H (setting of 0000_H and 0001_H is prohibited).

(28) Error Detection Register 3 (RDC3ASnDIAG3)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$00B0_H$

Value after reset: $2000\ 0200_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SQHTH[15:0]															
Value after reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SQLTH[15:0]															
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49.100 RDC3ASnDIAG3 Register Contents

Bit Position	Bit Name	Function
31 to 16	SQHTH[15:0]	Sum-of-Squares Amplitude Upper Threshold Sets the upper threshold for values of the integrated sum-of-squares amplitude. A value exceeding this is detected as sum-of-squares amplitude error. The user can set this value freely based on **Table 49.101**.
15 to 0	SQLTH[15:0]	Sum-of-Squares Amplitude Lower Threshold Sets the lower threshold for values of the integrated sum-of-squares amplitude. A value falling below this is detected as sum-of-squares amplitude error. The user can set this value freely based on **Table 49.101**.

Table 49.101 Integrals of the Sums of Squares of SINMNT and COSMNT for One Cycle of Excitation

Excitation frequency (kHz)→	5 kHz	7.5 kHz	10 kHz	12.5 kHz	15 kHz	17.5 kHz	20 kHz
resolver signal amplitude ↓							
0.1 × ADSVREFH-ADSVREFL (Vpp)	243	162	120	95	77	66	56
0.2 × ADSVREFH-ADSVREFL (Vpp)	1023	678	502	395	322	271	231
0.3 × ADSVREFH-ADSVREFL (Vpp)	2279	1514	1118	883	714	607	521
0.4 × ADSVREFH-ADSVREFL (Vpp)	4075	2694	1995	1571	1271	1079	928
0.5 × ADSVREFH-ADSVREFL (Vpp)	6369	4228	3131	2462	1998	1689	1445
0.6 × ADSVREFH-ADSVREFL (Vpp)	9170	6078	4503	3546	2873	2428	2083
0.7 × ADSVREFH-ADSVREFL (Vpp)	12499	8286	6111	4823	3914	3309	2849
0.8 × ADSVREFH-ADSVREFL (Vpp)	16352	10817	7994	6316	5117	4327	3715
0.9 × ADSVREFH-ADSVREFL (Vpp)	20667	13697	10121	7979	6469	5477	4697

(29) Error Detection Register 4 (RDC3ASnDIAG4)

Access: This register can be read or written in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$00B4_H$

Value after reset: $0007\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SQCNT[6:0]							—	—	—		—	SQCTH[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Table 49.102 RDC3ASnDIAG4 Register Contents

Bit Position	Bit Name	Function
31 to 15	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
14 to 8	SQCNT[6:0]	Sum-of-Squares Amplitude error Counter Value These bits hold the counter value of the excitation period which has exceeded the threshold for judging the integral of the sum-of squares specified by the SQHTH[15:0] and SQLTH[15:0] bits.
7 to 3	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
2 to 0	SQCTH[2:0]	Sum-of-Squares Amplitude Error Excitation Counts Threshold Selects the number of excitation periods in which abnormal amplitudes may be generated in the judgment of integrated sum-of-squares amplitude errors. The number of times set in these bits being exceeded is judged to represent an integrated sum-of-squares amplitude error. b2 b1 b0 0 0 0: 8 times 0 0 1: 1 time 0 1 0: 2 times 0 1 1: 3 times 1 0 0: 4 times 1 0 1: 16 times 1 1 0: 32 times 1 1 1: 64 times

(30) Debugging Read Register 0(RDC3ASnDBG0)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$00C0_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	SMNTAD1[12:0]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CMNTAD1[12:0]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.103 RDC3ASnDBG0 Register Contents

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned.
28 to 16	SMNTAD1[12:0]	SINMNT Acquired by ADC SINMNT signal acquired by ΔΣADC (differential signal. 2's complement representation. 1LSB is equivalent to (ADSVREFH - ADSVREFL)/ 4096 (V). sin and cos correction not implemented)
15 to 13	Reserved	When read, the value after reset is returned.
12 to 0	CMNTAD1[12:0]	COSMNT Acquired by ADC COSMNT signal acquired by ΔΣADC (differential signal. 2's complement representation. 1LSB is equivalent to (ADSVREFH - ADSVREFL)/ 4096 (V). sin and cos correction not implemented)

[SMNTAD1[12:0], CMNTAD1[12:0]]

Both are expressed as 2's complement with differential signals. 1LSB is equivalent to (ADSVREFH - ADSVREFL)/4096 (V)

(31) Debugging Read Register 1 (RDC3ASnDBG1)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$00C4_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	SMNMAX[13:0]													
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CMNMAX[13:0]													
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 49.104 RDC3ASnDBG1 Register Contents

Bit Position	Bit Name	Function
31, 30	Reserved	When read, the value after reset is returned.
29 to 16	SMNMAX[13:0]	SINMNT Acquired by ADC Maximum amplitude of SINMNT signal of conversion loop 1 calculated by sin, cos gain correction circuit (2's complement representation. 1LSB is equivalent to (ADSVREFH - ADSVREFL)/ 4096 (V))
15, 14	Reserved	When read, the value after reset is returned.
13 to 0	CMNMAX[13:0]	COSMNT Acquired by ADC Maximum amplitude of COSMNT signal of conversion loop 1 calculated by sin, cos gain correction circuit (2's complement representation. 1LSB is equivalent to (ADSVREFH - ADSVREFL)/ 4096 (V))

(32) Debugging Read Register 3 (RDC3ASnDBG3)

Access: This is a read-only register that can be read in 8-, 16-, and 32-bit units.

Address: <RDC3ASn_base>+$00CC_H$

Value after reset: 0000 $xxxx_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	REFAD1[12:0]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Value after reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

*: Undefined

Table 49.105 RDC3ASnDBG3 Register Contents

Bit Position	Bit Name	Function
31 to 29	Reserved	When read, the value after reset is returned.
28 to 16	REFAD1[12:0]	Excitation signal acquired by ΔΣADC (Differential signal. Two's complement representation. 1LSB is equivalent to (ADSVREFH - ADSVREFL)/ 4096 (V).)
15 to 0	Reserved	The read value is undefined.

49.2.3 Specifications of the RDC Functions

49.2.3.1 Tracking Loops

The following describes the operating principles of the RDC3AS module. This R/D converter module uses the tracking method to convert analog resolver signals to digital signals (R/D conversion). The tracking loop runs at 20 MHz. When the excitation signal f(t) is input to the excitation coil, f(t) • sinθ and f(t) • cosθ are output from the resolver according to the angle (θ) of the resolver rotor. These signals are input to the RDC3ASnS2-RDC3ASnS4 and RDC3ASnS1-RDC3ASnS3 pins, respectively. These signals are obtained by ΔΣADCs, and input to the multiplier. At the same time, cos ϕ (or sin ϕ) is generated by passing the accumulator output through COS ROM (or SIN ROM) and is fed back to the multiplier. Then the subtraction is performed.

f(t) • (sin θ • cos ϕ – cos θ • sin ϕ) (= SINMNT • cos ϕ – COSMNT • sin ϕ)

= f(t) •sin (θ – ϕ)

≈ f(t) • (θ – ϕ)

The result is converted to 1-bit digital value by the comparator (CMP). The excitation component f(t) is removed in the synchronous detection circuit to obtain the control variation ε = θ – ϕ. The negative feedback control over the entire digital circuits provides feedback so that the control variation becomes zero. When θ = ϕ, the analog angle information from the resolver has been converted to digital angle ϕ (16-bit wide). **Figure 49.36** describes the PI compensator and accumulator.

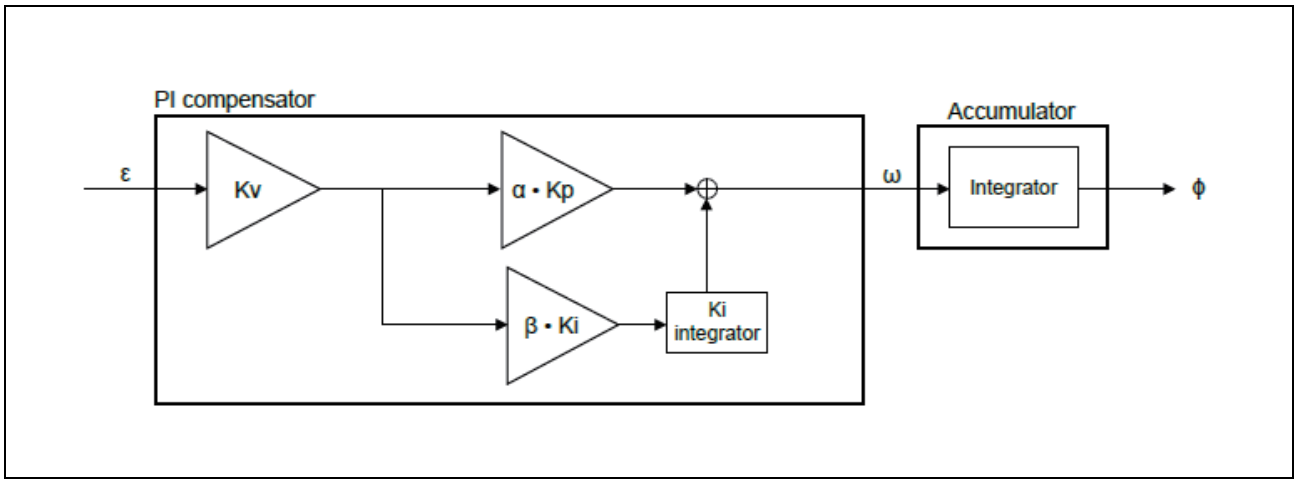


Figure 49.36 PI Compensator and Accumulator

The PI compensator converts the control variation according to the following formula, and passes the result to the accumulator circuit.

ω = (α • Kp + (β • Ki)/(s • T)) • Kv • ε

Kv, Kp, Ki: control coefficients that can be set in a register

α, β: fixed values

s: Laplace variable

T: Integration time constant

ω: PI compensator output, angular velocity information

The accumulator circuit calculates the angle ϕ based on the angular velocity information ω.

(1) PI Compensator Bandwidth Setting

This RDC can be set from six different bandwidths (five fixed and one auto-adjusted) using the registers. In addition, coefficients in the PI compensator can be configured in detail by setting the BWCS bit in the RDC3ASnPI0 register to 0.

For further details, refer to the section on the RDC3ASnPI0 register.

(2) Forced Gain Control Function (AGCON)

The forced gain control function(AGCON) is designed to improve the tracking performance when the resolver angle deviates significantly from the R/D converted angle in situations such as after a reset. The forced gain control state is entered when any of the following conditions is met:

[Conditions for starting AGCON]

1. Release from the reset state
2. The recovery from a resolver signal error
3. The recovery from a resolver signal disconnect error
4. The start of angular conversion BIST or conversion error BIST
5. The end of sum-of-squares amplitude error detection BIST, angular conversion BIST, resolver signal error BIST, disconnection error BIST, conversion error BIST
6. 1 being written to the KIRST bit of the RDC3ASnDIAG1 register

Forced gain control function is applied for approximately 5 ms*1. If one of the above conditions is met again during the execution, the forced gain control state is entered again from this point and the period of its execution is extended by approximately 5 ms.

The value of the Kv gain becomes greater on entry to the forced gain state, so even if the resolver rotation angle signal θ and the R/D converter output angle signal ϕ have matched, ϕ may fluctuate significantly for approximately 1 ms. When the AGCD bit is set to 1, the forced gain state will not be entered even if a condition for starting forced gain control is met, except for release from the reset state. The initial Kv gain value depends on the type of BIST.

- Angular conversion BIST and conversion error BIST: Initial gain value = × 128 (the maximum value)
- When a short-period BIST (sum-of-squares amplitude error detection BIST, resolver signal error BIST, or disconnection error BIST) ends: Initial gain value = gain value specified by the AGST[3:0] bits

Since short-period BIST can be completed in a short time, it is possible to start during angle conversion, and the angle tracking is maintained during execution. If the initial value of Kv gain at the end of short-period BIST is too large, the fluctuation of phi will become large, so the mechanism is such that the initial value can be set with a register. The Kv gain changes automatically during the AGCON period, but if it falls below the gain value specified by HKVLM[3:0] once, the gain never becomes greater than the value specified by HKVLM[3:0] after that. Also, it never becomes smaller than the value specified by LKVLM[3:0].

Forced gain control(AGCON) function is subject to the following restrictions.

(1) When changing the setting of the AGCD bit, which sets the Forced gain control(AGCON) function valid / invalid, change the setting while the resolver is stationary. After that, write 1 to the KIRST bit. Not setting the KIRST bit to 1 may result in entry to the free-running state.

(2) Forced gain control is subject to restrictions on the angular velocity that allows operation. The upper-limits according to the maximum angular velocity/resolution setting (MAXV[2:0] bit setting) are as listed below.

When the resolution is equal to or less than 12 bits: 120000 min^{-1}

When the resolution is 13 bits: 60000 min^{-1}

When the resolution is 14 bits: 30000 min^{-1}

When the resolution is 16 bits: 7500 min^{-1}

Note 1. The timing value is when the CCLK is running at 40 MHz.

(3) Excitation Signal Source Selection and Delay adjustment

Use REFINSL bit of RDC3ASnREF register to select one of the following three as the excitation phase signal input from the outside of RDC3AS.

- Excitation phase signal from ΔΣADC for excitation
- Excitation phase signal from timer in LSI
- Excitation phase signal from external pin

In addition, two types of waveform patterns for the input excitation phase signal can be selected using EXRFPSL bit of RDC3ASnREF register. The input excitation frequency range is shown in **Table 49.106**

Table 49.106 Available excitation frequency range

Excitation signal input selection	Available excitation frequency range
ΔΣADC for excitation	5kHz to 40kHz
Excitation phase signal from timer in LSI	5kHz to 25kHz
Excitation phase signal from external pin	5kHz to 25kHz

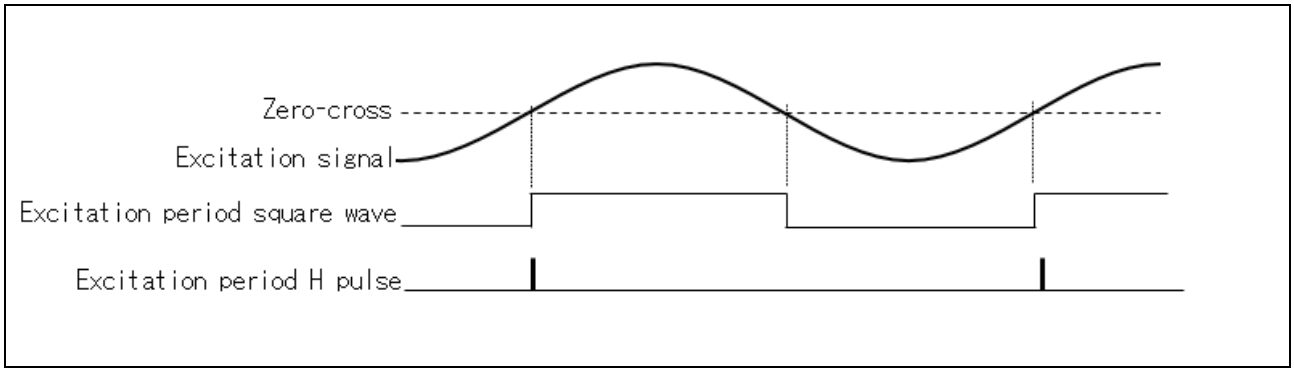


Figure 49.37 Selectable excitation phase signal waveform pattern

In order to perform RDC angle tracking normally, the phase components of the ΔΣ ADC output sine and cosine signals shown in **Figure 49.38** and the phase of the delay adjusted excitation phase signal must be matched to the following conditions.

- When excitation component extraction function is used: Within ± 30 ° of excitation cycle
- When excitation component extraction function is not used: Within ± 10 ° of excitation cycle

In order to keep the phase difference in the above conditions, use the excitation phase signal adjustment counter (REFDLCT bit) to adjust the phase as shown in **Figure 49.39**, **Figure 49.40**, and **Figure 49.41**, in consideration of delay due to the group delay of ΔΣADC and external filter.

As shown in **Figure 49.37**, the excitation phase input (excitation period rectangular wave, excitation period H pulse) is assumed to be at the zero cross position of the excitation signal. If it is not the zero cross position, adjust the delay to the zero cross position by adding it to the excitation phase signal adjustment counter (REFDLCT bit).

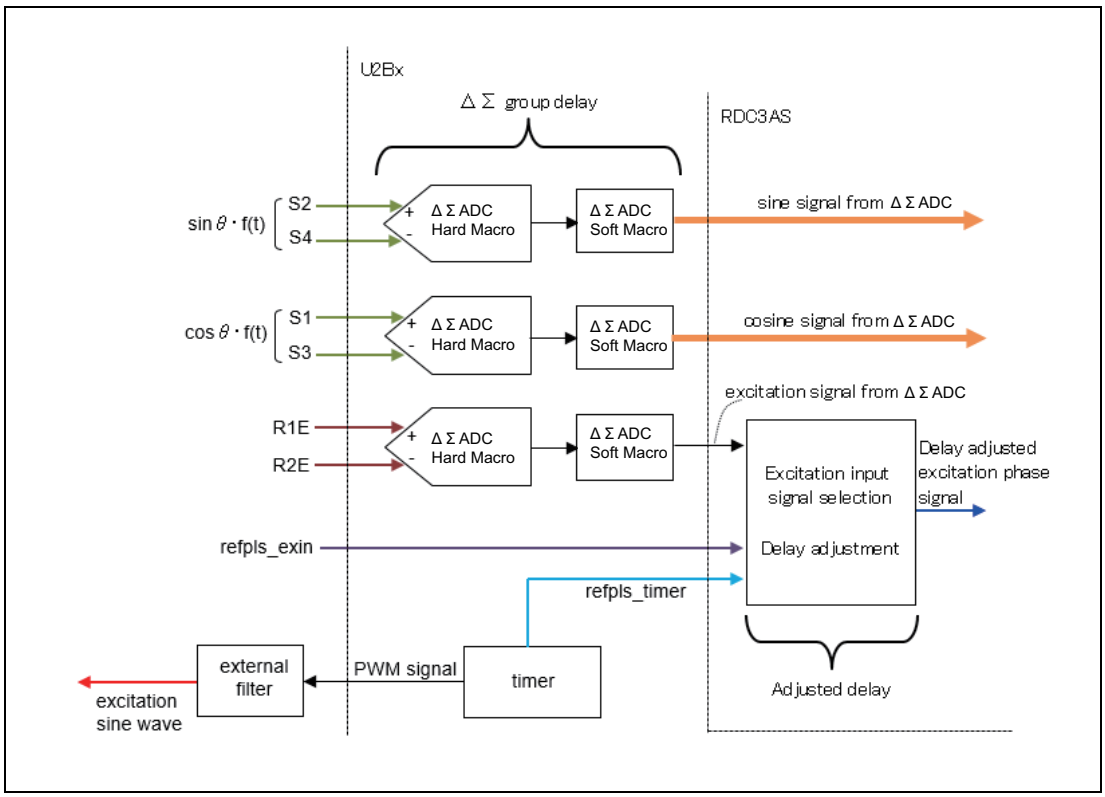


Figure 49.38 Excitation phase signal input block diagram

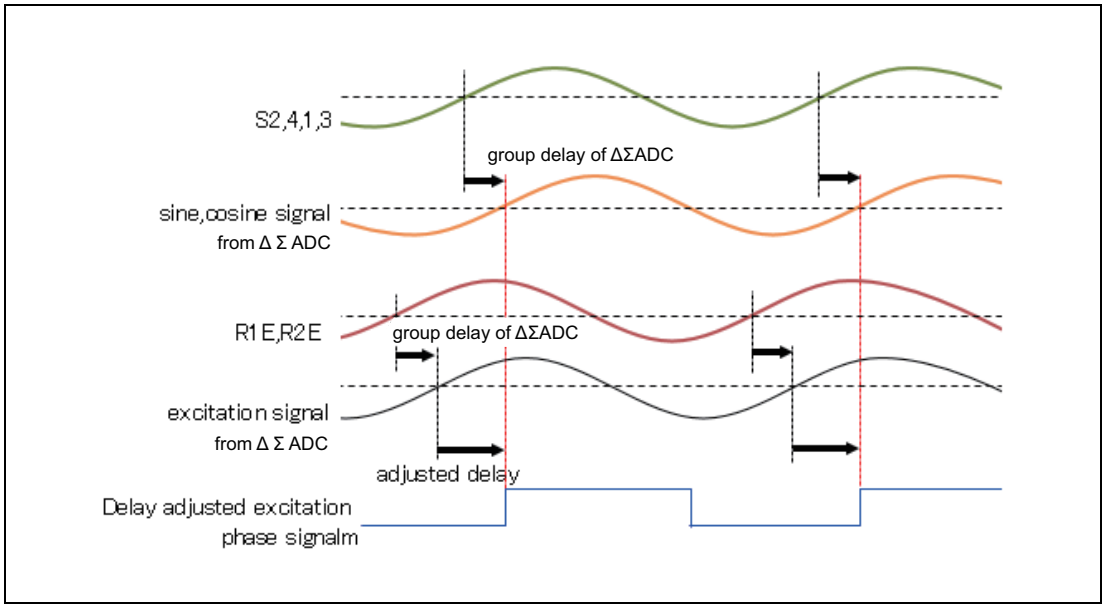


Figure 49.39 Excitation phase relationship when using excitation phase signal from ΔΣADC for excitation

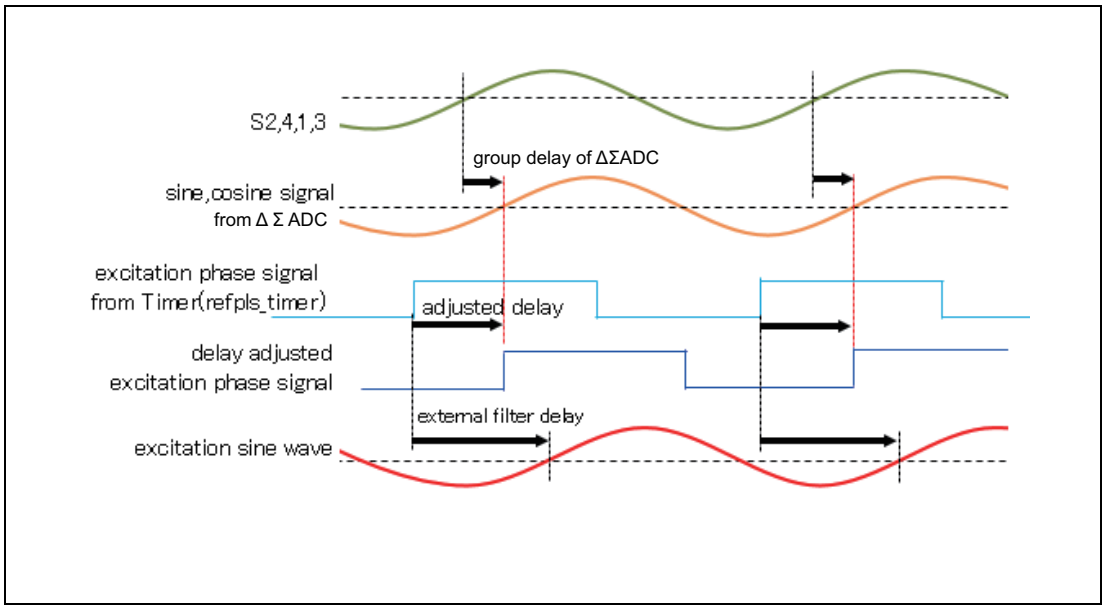


Figure 49.40 Excitation phase relationship when excitation phase signal from timer in LSI is selected

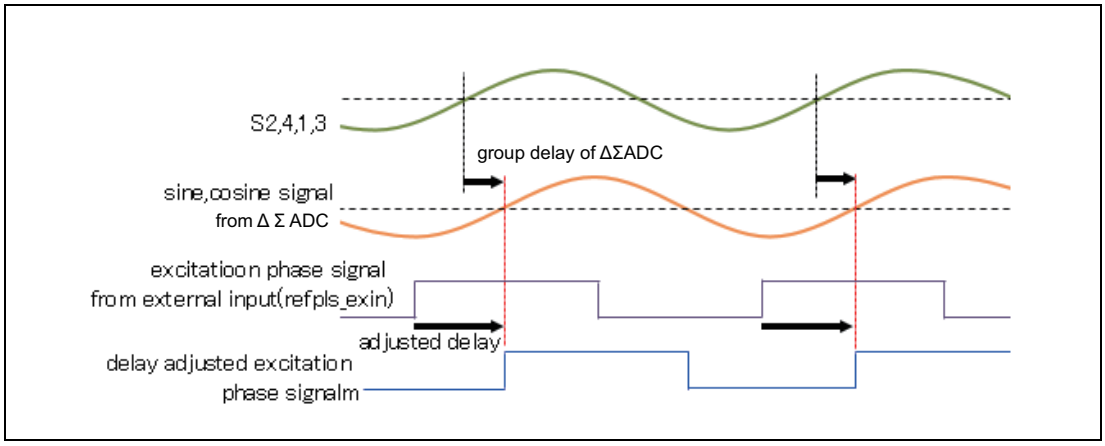


Figure 49.41 Excitation phase relationship when excitation phase signal from LSI external pin is selected

When REFINSL bits are set to 01 or 10 and REFETSL bit is set to 0, the phase difference occurs between the synchronous detection signal and the zero cross position used for excitation timer. Consider that the phase of zero cross position is earlier by the ΔΣADC output update period, when adjusting zero cross position and excitation timer.

(4) Required Sensor Selection Function

The DC resolver signal (E • sinθ, E • cosθ) which does not contain excitation component can be used by setting the SENS bit in the RDC3ASnREF register to 0. When the DC resolver signal is used, the excitation component extraction function is disabled.

Table 49.107 Relation between the EXIO and SENS Bits and the Resolver to be Used

EXIO	SENS	Resolver to be Used
0	0	Setting prohibited
0	1	VR Resolver,Brush-Less Resolver (external excitation)
1	0	DC resolver
1	1	Setting prohibited

(5) Excitation Component Extraction Function

The excitation input signals and resolver signals (RDC3ASnS1 to RDC3ASnS4) are analog signals input to the RDC. If there is a phase difference between the excitation component (sine wave component) in the excitation signal line and that in the resolver signal line, it can cause an error in the angle conversion result in proportion to the phase difference. The phase difference between the resolver signal and excitation signal can be reduced by using the extracted excitation component contained in the resolver signal line for an angle conversion.

The excitation component extraction function automatically performs the following process; the excitation input signals is used when the difference between the resolver electrical angle and the R/D converted angle is large, and the extracted excitation component is used when the difference is small. The exact adjustment of the phase difference between excitation and resolver signals is not required because of this function. For successful operation of the excitation component extraction circuit, the excitation component phase deviation between the delay adjusted excitation signal and the resolver sin, cos signals from ΔΣ ADC should be within 30°(See **(3)**).

(6) Maximum Angular Velocity Setting

This function can set the maximum angular velocity (resolution) that is capable of tracking operation by using the MAXV [2:0] bits in the RDC3ASnPI1 register. RDC operates at the set resolution without missing codes.

(7) Compare Match Interrupt

When the angle set in the CMPj register (j = 0 to 2) and the R/D converted angle match, a compare match interrupt request signal is generated. The compare match interrupt request signal is output when the CINTEN bit in the RDC3ASnENC0 register is set to 1. The bit width that is compared for a match is set using the MAXV [2:0] bits (maximum angular velocity selection) in the RDC3ASnPI1 register. The compare match interrupt request signal can be selected from either a compare match signal or a signal latching a compare match signal by using the IRS bit in the RDC3ASnPHICP0 register. When the IRS bit is set to 0, the compare match interrupt request signal becomes high when the R/D converted angle and the angle set in the CMPj register match, and becomes low when the values do not match. When the IRS bit is set to 1, the compare match interrupt request signal becomes high when the R/D converted angle and the angle set in the CMPj register match, and also the INTFLG[2:0] flag in the RDC3ASnPHICP0 register becomes 1. In this case, the request signal retains the high level even if the angles no longer match. When 1 is written to the INTCLR[2:0] bit in the RDC3ASnPHICP0 register while the R/D converted angle and the angle set in the CMPj register do not match, the request signal becomes low and the INTFLG[2:0] flag becomes 0. If 1 is written to the INTCLR[2:0] bit while the R/D converted angle and the angle set in the CMPj register match, the request signal remains high and the INTFLG[2:0] flag does not become 0.

Turning hysteresis on by setting the HYSS bit in the RDC3ASnENC0 register to 0 prevents chattering of the output of the compare match interrupt signal and Z phase signal when the angle output near the target bit for comparison is not stable.This hysteresis circuit can only be used when 12-bit resolution is selected (MAXV[2:0] = 001_B).

Output of the PHI comparison flag is in the scope of control by the PHIERLK bit.

Figure 49.42 shows the timing chart of the compare-match interrupt request signal when hysteresis is off (HYSS = 1).

Figure 49.43 shows the timing chart of the compare-match interrupt request signal when hysteresis is on (HYSS=0).

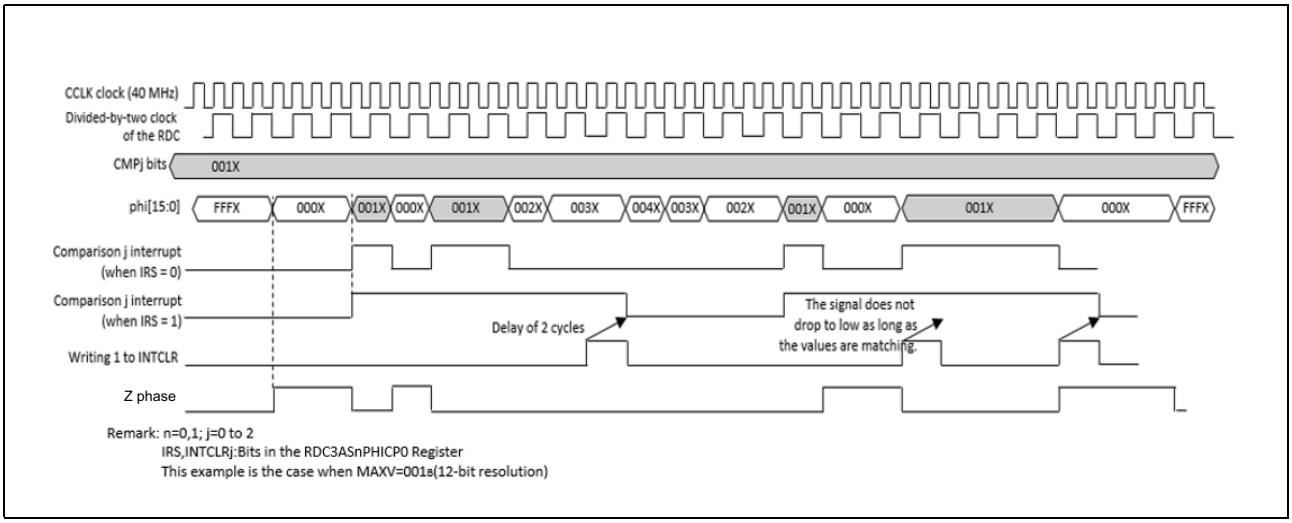


Figure 49.42 Timing Chart for the Compare Match Interrupt Request Signal when Hysteresis is Off(HYSS = 1)

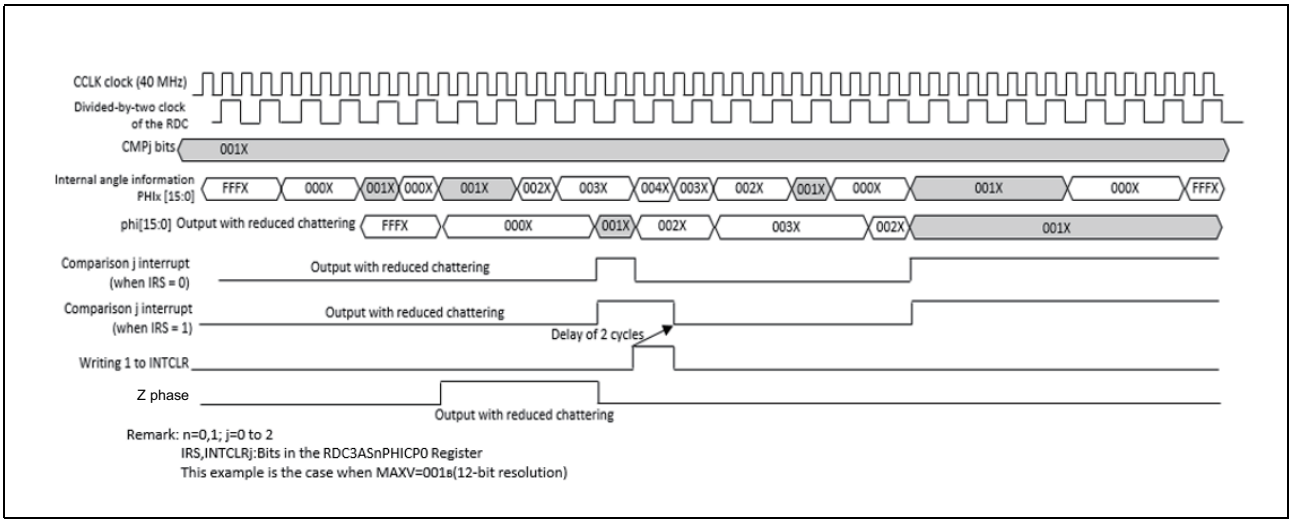


Figure 49.43 Timing Chart for the Compare Match Interrupt Request Signal when Hysteresis is On (HYSS=0)

(8) Encoder Pulse Output Function

This function enables to output encoder pulse signals (A, B, Z, U, V, W phases). The Z-phase interrupt signal becomes high while the R/D converted angle is 0°. The bit width compared for a match is set using the MAXV [2:0] bits in the RDC3ASnPI1 register as it is for the compare match interrupt request signal. The encoder pulse signal is output when the corresponding bit in the RDC3ASnENC0 register is set to 1 (enables output).

Whether the encoder pulse signals are to be output through the hysteresis circuit or without going through it can be selected using the HYSS bit in the RDC3ASnENC0 register. This hysteresis circuit can only be used when 12-bit resolution is selected (MAXV[2:0] = 001_B).

The encoder pulse output is in the scope of control by the PHIERLK bit.

Figure 49.44 shows the waveforms of encoder phase pulse operation when hysteresis is on and off.

See **Figure 49.42** and **Figure 49.43** for the z phase waveform when the angle output near the target bit for comparison is not stable.

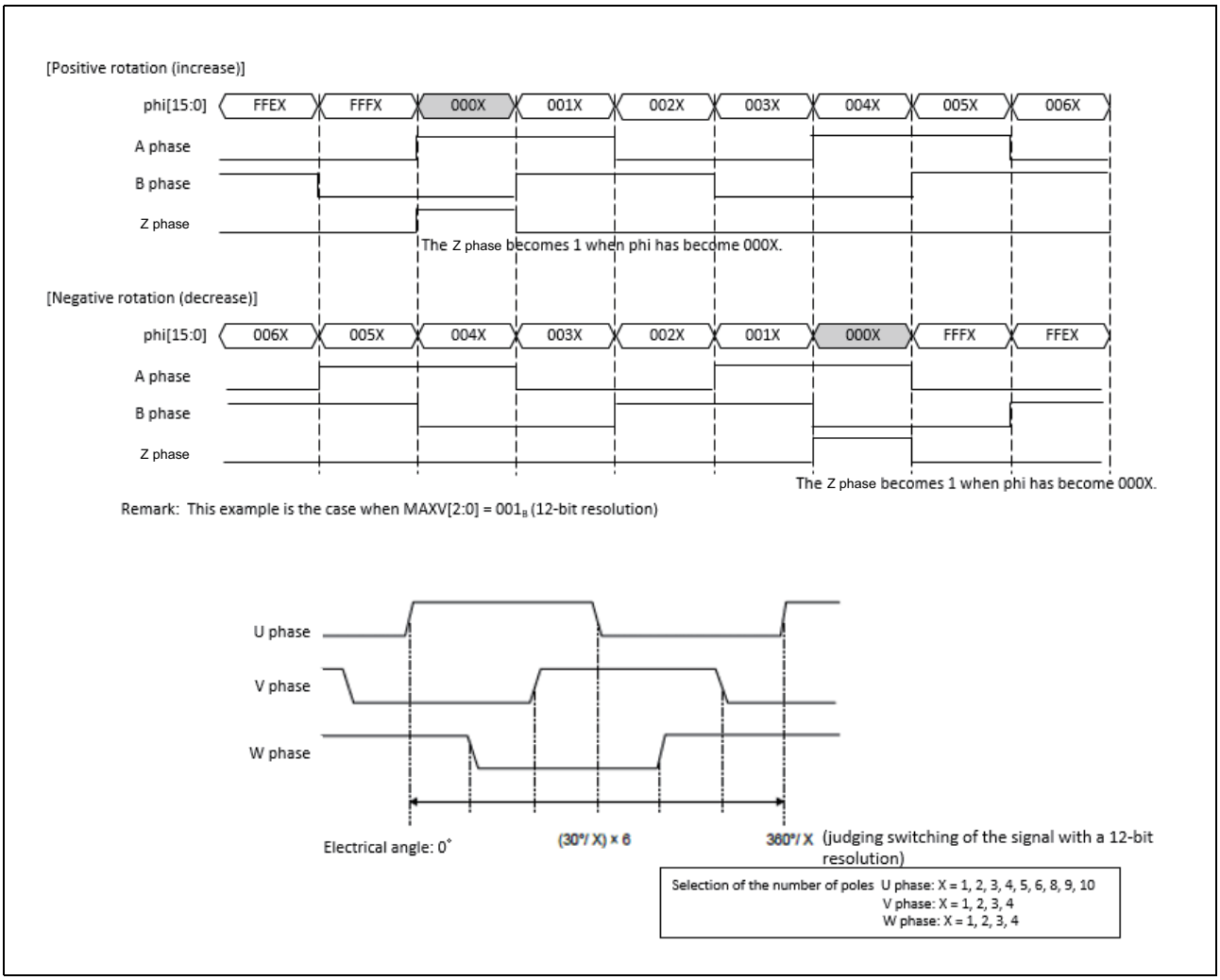


Figure 49.44 Waveforms of Encoder Phase Pulse Operation when Hysteresis is On and Off.

(9) PHI Angular Velocity Information Reading Function

The angular velocity of the phi angle is read from the relevant register. The amount of change in the phi angle is measured over the period selected by the OMGPTC[1:0] bits, converted into the units of angular velocity (min^{-1}), and stored in the OMG[31:0] bits of the RDC3ASnOMG register. The angular velocity of phi (in min^{-1}) does not depend on the selected measuring period, but the maximum measurable angular velocity does. The angular velocity stored in the OMG[31:0] bit is updated every measuring period. The measuring period that can be set with OMGPTC [1: 0] can be changed even during angle conversion.

OMG[31:0] bits are in the scope of control by the PHIERLK bit (fixed to 0 min^{-1})

Table 49.108 Contents of OMGPTC[1:0] Bits

OMGPTC[1:0]	Measuring Period	Maximum Measurable Angular Velocity (min^{-1})
00	12.8µs	2,343,750
01	51.2µs	585,938
10	102.4µs	292,969
11	204.8µs	146,484

Note: This table shows the relation between the measuring period and the range of measurable angular velocity.

Table 49.109 OMG Bits and the PHI Angular Velocity (min^{-1})

Bit	Angular Velocity (min^{-1})
b31-25	Sign (0: +, 1:—)
b24	1,171,875
b23	585,937.5
b22	292,968.8
b21	146,484.4
b20	73,242.19
b19	36,621.09
b18	18,310.55
b17	9,155.27
b16	4,577.64
b15	2,288.82
b14	1,144.41
b13	572.20
b12	286.10
b11	143.05
b10	71.53
b9	35.76
b8	17.88
b7	8.94
b6	4.47
b5	2.24
b4	1.12
b3	0.56
b2	0.28
b1	0.14
b0	0.07

For example, the angular velocity is -164,795 min^{-1} if the result for angular velocity read from the OMG bits is FFDB $FFFF_H$.

Reading the angular velocity from a register requires the time taken by the register access. Accordingly, the angular velocity may have completely changed at the actual point where reading is completed. It has a function to fix the angular velocity value at the timing when you want to read the angular velocity. Whether or not the angular velocity is fixed can be set with the OMGLTSL bit of the RDC3ASnENC0 register. There are two types of triggers that fix the angular velocity: register write (OMGLT bit = 1 write) and external signal (omg_latch_trg) H pulse input.

49.2.3.2 Sine and Cosine Correction Function

(1) Sine and Cosine Gain Correction

Resolver errors or errors in the accuracy of components on the printed circuit board may lead to gaps between the amplitudes of the sine- and cosine-wave signals input to the R/D converter that lead to errors in the result of angle conversion by the RDC. In order to reduce errors in the results of conversion, the maximum amplitudes of the sine-wave signal (SINMNT = f(t)•sin(θ)) and cosine-wave signal (COSMNT = f(t)•cos(θ)) are compared, and if there is a gap between the amplitudes, that of the COSMNT signal is automatically adjusted to have the same range as that of the SINMNT signal. The values after correction are used in operations.

If the resolver angle is fixed, the maximum amplitudes of the SINMNT and COSMNT signals cannot be compared. In this case, the resolver is required to go through at least half a rotation (electrical angle) to obtain signal values for comparison. Accordingly, when the RDC is ready to output results of conversion, the user needs to wait for the resolver to go through at least half a rotation (electrical angle) before writing 1 to the GNCST bit. The gain correction function will then be ready for use. Writing 1 to the GNCST bit before waiting for the required period may result in invalid correction value.

The correctable range limit expressed as a percentage can be set by the GNCLT [1: 0] bits. If the correction value exceeds the limit value, the limit value will be applied.

GNCLT[1:0] = 00_B: Limit ±20% (default)

GNCLT[1:0] = 01_B: Limit ±10%

GNCLT[1:0] = 10_B: Limit ±40%

GNCLT[1:0] = 11_B: Limit ±0% (no compensation)

Figure 49.45 below shows how the amplitude of COSMNT, which is initially smaller than that of SINMNT, is corrected to have the same amplitude as SINMNT.

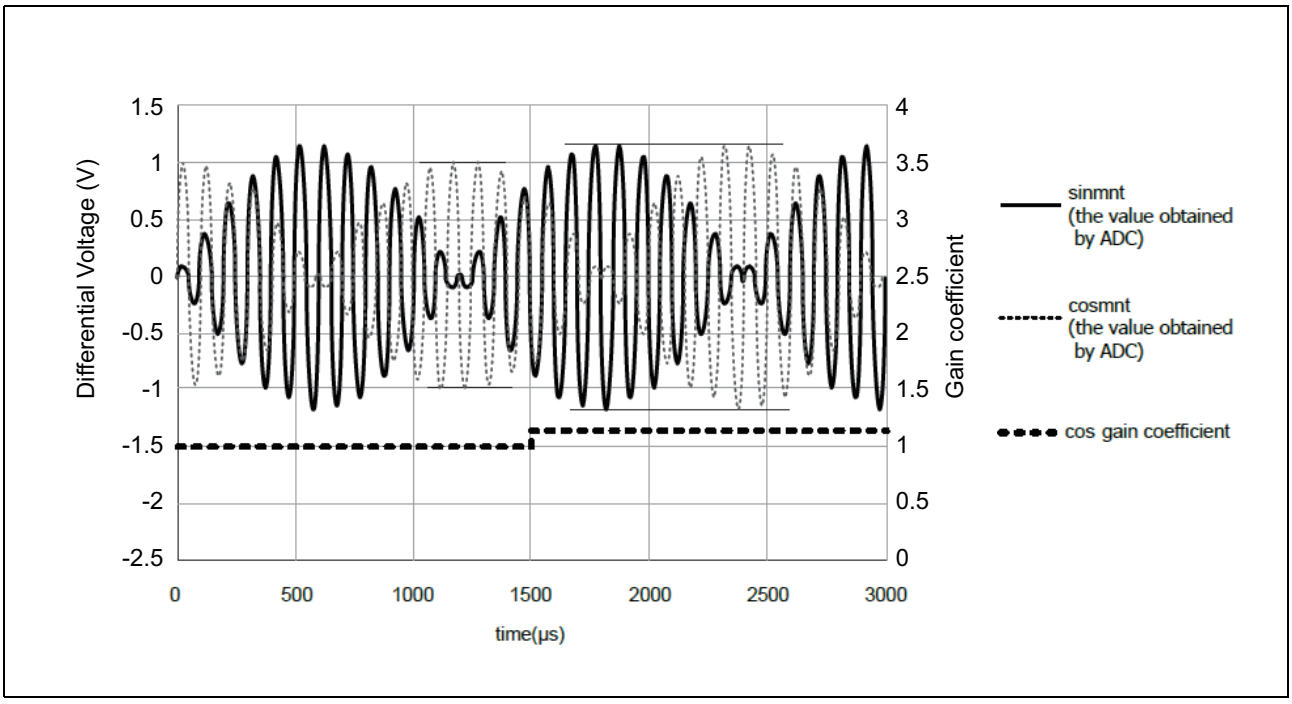


Figure 49.45 Correction to Make the Amplitudes Correspond

The timing of correcting the gain value is selected by the GNCSL[1:0] bits as follows;

- GNCSL[1:0] = 00_B
  No correction (the default value, 1024, is used as the value for correction)
- GNCSL[1:0] = 01_B
  The fixed value set in the GNCNM[11:0] bits is used as the value for correction.
- GNCSL[1:0] = 10_B
  The value calculated when the GNCST bit is set to 1 is used as the value for correction. The value from the calculation is retained.
  The GNCST bit can be set to 1 multiple times. In that case, set it after the resolver has rotated more than half a rotation (electrical angle) since it was set last time.
- GNCSL[1:0] = 11_B
  The value is updated at the time of z-phase output following GNCST being set to 1. The value is updated on every single rotation.

(2) Sine and Cosine Common Offset Correction

A resolver error or error in the accuracy of the components on the printed circuit board may lead to an offset for the common levels of the sine- and cosine-wave signals, which are input to the R/D converter. This may lead to errors in the results of angle conversion by the RDC. In order to reduce errors in the results of conversion, an offset of the common level of the SINMNT and COSMNT signals from original level is detected and automatically adjusted. The values after correction are used in operations.

If the resolver angle is fixed, the maximum amplitudes of the SINMNT and COSMNT signals cannot be compared. In this case, the resolver is required to go through half a rotation (electrical angle) to obtain signal values for comparison. Accordingly, when the RDC is ready to output the results of conversion, the user needs to wait for the resolver to go through at least half a rotation (electrical angle) before writing 1 to the GNCST bit. The common offset correction function will then be ready for use. Writing 1 to the GNCST bit before waiting for the required period may result in invalid correction values.

A limit can be set to the value for common offset correction by CMCLT[1:0] bits. If the value for correction value obtained from SINMNT and COSMNT is greater than the specified limit, the specified limit is applied.

- CMCLT[1:0]=00_B: limit ± 0.0312 × (ADSVREFH - ADSVREFL) (approx. ± 150mV) (default)
- CMCLT[1:0]=01_B: limit ± 0.0156 × (ADSVREFH - ADSVREFL) (approx. ± 78mV)
- CMCLT[1:0]=10_B: limit ± 0.125 × (ADSVREFH - ADSVREFL) (approx. ± 625mV)
- CMCLT[1:0]=11_B: limit ± 0 × (ADSVREFH - ADSVREFL) (± 0mV) (no correction)

Figure 49.46 below shows how the common offset of COSMNT and SINMNT are corrected.

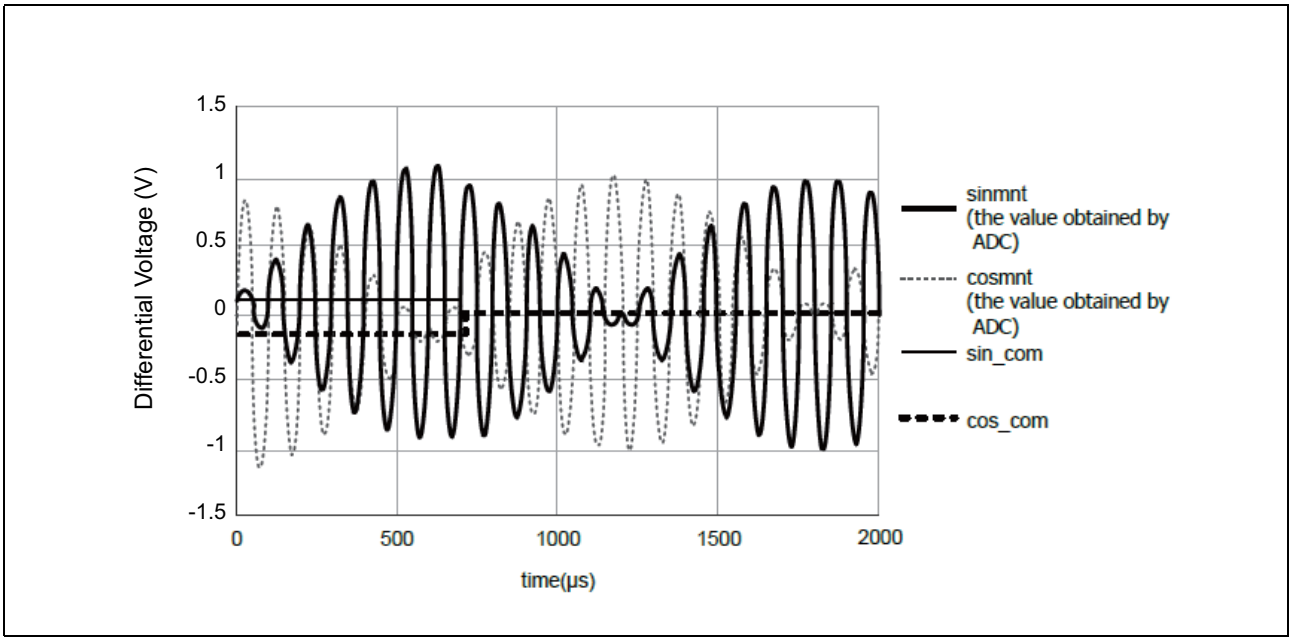


Figure 49.46 Correction of Common Offsets

The timing of updating the value for common offset correction is selected by the CMCSL[1:0] bits as follows;

- CMCSL[1:0] = 00_B
  No correction (0 is used as the value for correction)
- CMCSL[1:0] = 01_B
  The value for correction set in CCOSN[9:0] is selected as the value for the cosine side.
  The value for correction set in CSOSN[9:0] is selected as the value for the sine side.
- CMCSL[1:0] = 10_B
  The calculated value is used as the value for correction.
  - When GNCSL[0] = 0, the value calculated when the GNCST bit is set to 1 is used as the value for correction.
    The value from the calculation is retained.
    The GNCST bit can be set to 1 multiple times. In that case, set it after the resolver has rotated more than half a rotation (electrical angle) since it was set last time.
  - When GNCSL[0] = 1, the value is updated at the time of z-phase output following GNCST being set to 1.
    The common value for correction is updated on every single rotation.
- CMCSL[1:0] = 11_B
  Setting prohibited

(3) Sine and Cosine Phase Correction

Resolver errors or errors in the accuracy of components on the printed circuits board may lead to deviations between the time (phase) of the sine- and cosine-wave signals input to the R/D converter. In order to reduce errors in the results of conversion, deviations between the phases of the SINMNT and COSMNT signals are detected by comparing the timing of their excitation zero-crossing. Detected deviations are corrected by delaying the signal which has a phase in advance of the other.

When the power supply voltage is applied and the RDC initialization sequence is performed so that it is ready for use in angular tracking, write 1 to the register bit PHCST which gives an instruction to start phase correction of the sine and cosine signals. After 1 is written to this bit, application of the correction value starts.

Note that the obvious variations in amplitude between the sinmnt and cosmnt signals are required in order to compare the timing of their excitation zero-crossings. For this reason, this function automatically detects the phase deviation when the output phi angle is within ± 16.8° of either 45°, 135°, 225°, and 315°.

A limit can be set to the delay value for phase correction by PHCLT[1:0] bits. The correction value over the limit set by PHCLT [1: 0] will not be applied. If the value for correction obtained from sinmnt and cosmnt is greater than the specified limit, the specified limit is applied.

- PHCLT[1:0]=00_B: limit is 3 µs (default)
- PHCLT[1:0]=01_B: limit is 1 µs
- PHCLT[1:0]=10_B: limit is 6 µs
- PHCLT[1:0]=11_B: limit is 0 µs (no correction)

Figure 49.47 below shows the waveforms where the sinmnt signal delays from the cosmnt signal.

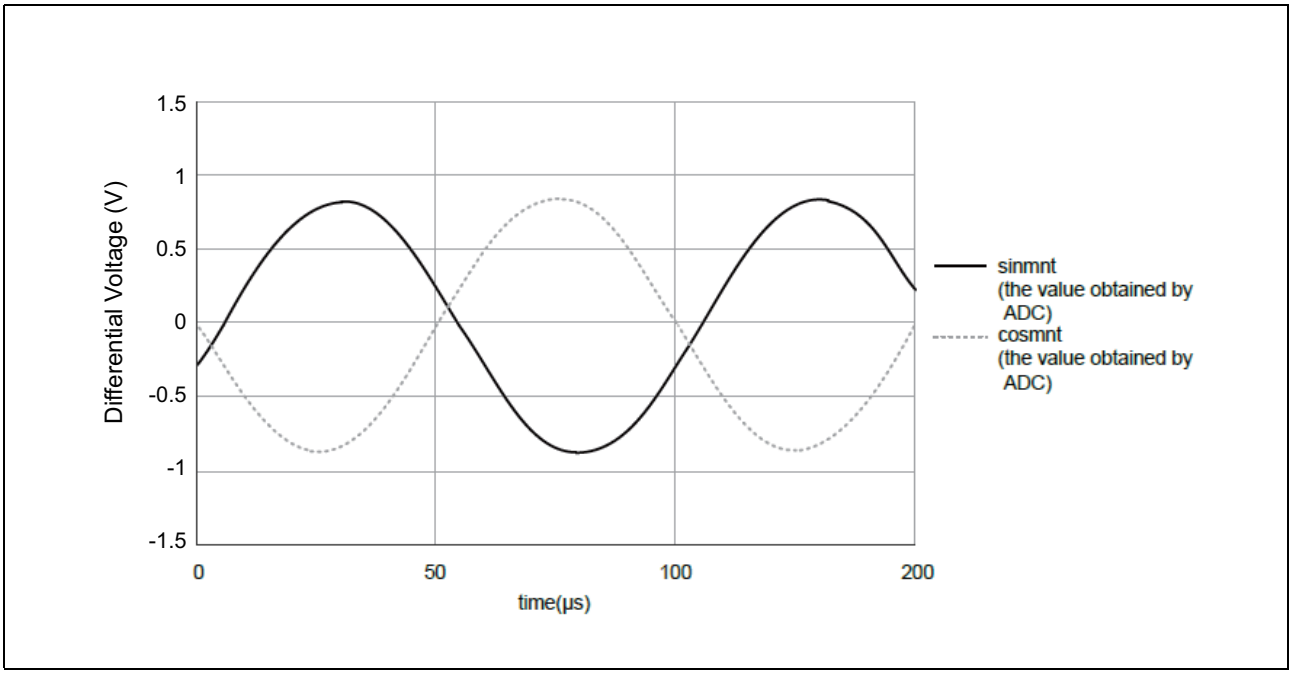


Figure 49.47 Signal with Delay

Figure 49.48 below shows the two synchronized waveforms obtained by detecting the advanced phase of the cosmnt signal and delaying.

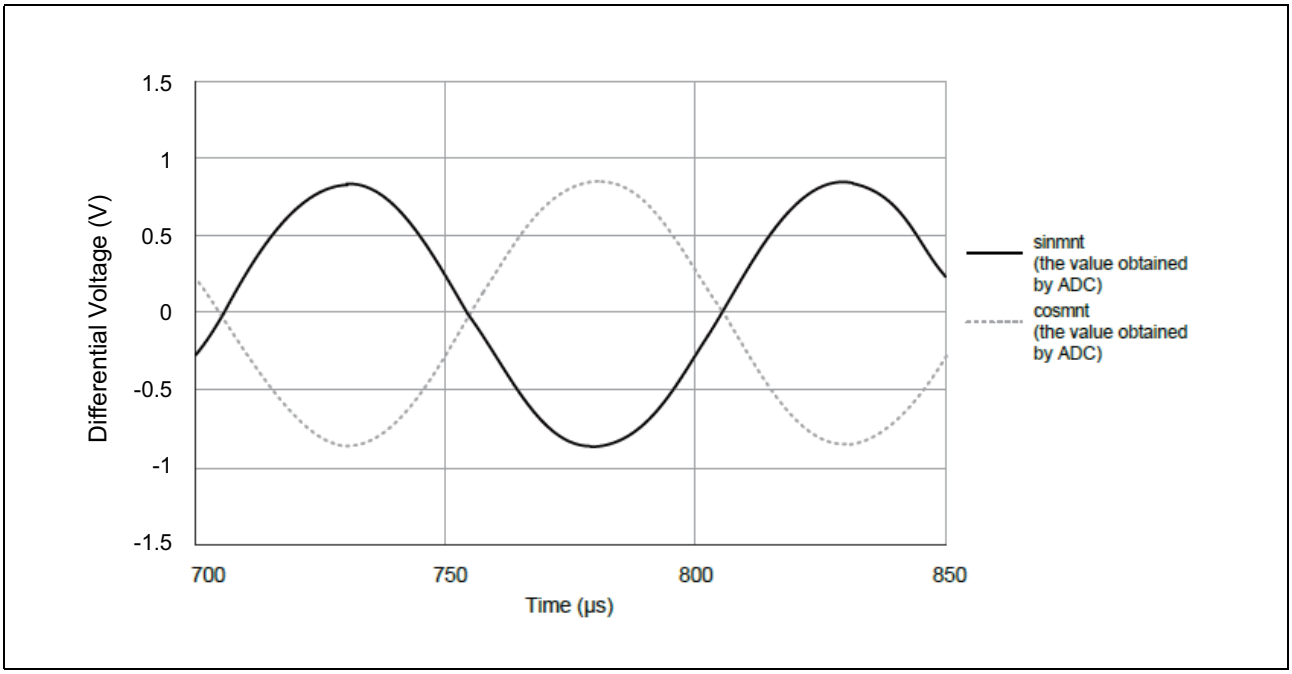


Figure 49.48 Phase Synchronization

The timing of correcting the phase deviation after writing 1 to the PHCST bit is select by the PHCSL[1:0] bits as follows;

- PHCSL[1:0] = 00_B
  No correction (default)
- PHCSL[1:0] = 01_B
  After writing 1 to the PHCST bit, the phase difference at 16 crossings of the excitation signal is constantly averaged to obtain the correction value.
- PHCSL[1:0] = 10_B
  Every time 1 is written to the PHCST bit, the phase difference at 16 crossings of the excitation signal is averaged once to obtain the correction value, and then the correction value is used.
- PHCSL[1:0] = 11_B
  The fixed correction values set by the PHSNM[5:0] bits (value for delay in the sine side) and the PHCNM[5:0] bits (value for delay in the cosine side) are used.

(4) Sine and Cosine Angle Correction Function

RDC has a function to correct the mounting angle error of the resolver with respect to the shaft of the motor and the error of sin and cos orthogonality of the resolver. Correction in this case is by adding fixed values for correction to the phi angles to be input to the individual SINROM and COSROM tables. These values are set in the SINPO[11:0] and COSPO[11:0] bits in the sine and cosine angle correction register. Set these bits to 0° for angle conversion BIST.

Sine angle correction bits SINPO[11:0] = 000_H

Cosine angle correction bits COSPO[11:0] = 000_H

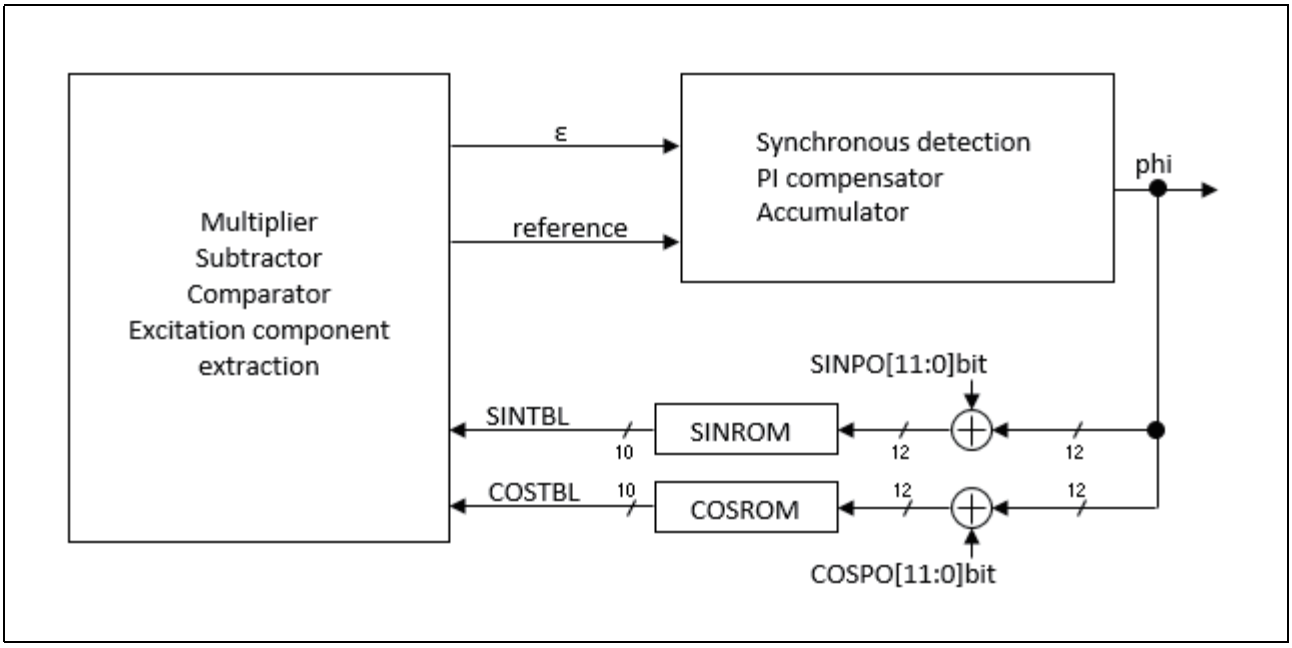


Figure 49.49 Structure of Sine and Cosine Angle Correction Circuit

49.2.3.3 Error Detection

(1) Error Detection

This function monitors and detects errors in resolver signal and in R/D conversion operations. If any of the errors listed in **Table 49.110** is detected, an RDC error interrupt request is generated, and the corresponding bit in the RDC3ASnDGOUT0 and 1 registers become 1. The following table lists factors that lead to error detection.

Table 49.110 Detected Error

Item	Detected Factor
Resolver signal error	• Excitation signal line disconnection including contact failure • Excitation signal down (excitation signal output circuit down, short circuit between lines) • Short circuits between signal lines (RDC3ASnS1 and RDC3ASnS3, RDC3ASnS2 and RDC3ASnS4) • Resolver coil layer short
Resolver signal disconnect error	Resolver signal lines disconnection (RDC3ASnS1 to RDC3ASnS4) including contact failure
R/D conversion error	Excessive control variation (ε) of tracking control loop (negative feedback control system)
Two path comparison conversion error	Comparison of the conversion results from the two angle conversion loops
Square-sum amplitude error	Modulation, distortion, or noise on the amplitude of the sine and cosine resolver input signals.

(2) Resolver Signal Error Detection

This function detects disturbance in the resolver signal balance caused by an error in excitation signals input to the resolver. When a resolver signal error is detected, an RDC error interrupt request signal becomes high. A resolver signal error is detected if the amplitude of SINMNT, COSMNT signals fall below the threshold for approximately 300 µs.

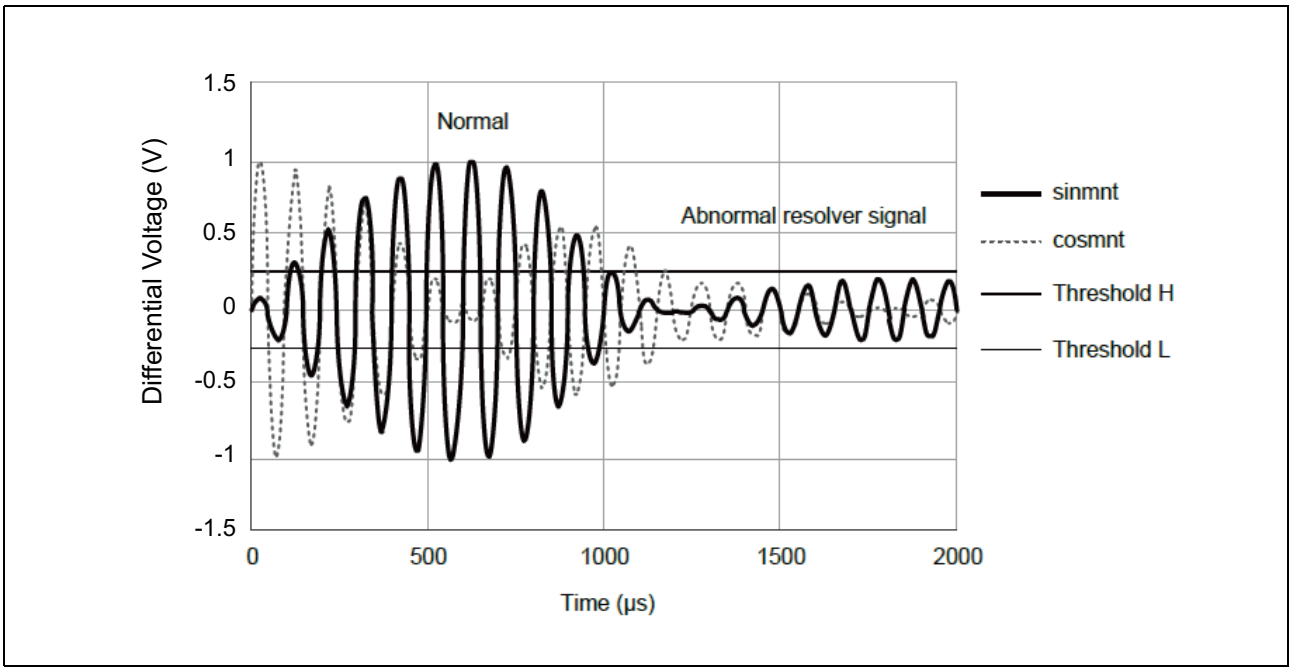


Figure 49.50 Monitor Signal Waveforms when the Resolver Signal is Abnormal

(3) Resolver Signal Disconnection Error Detection

This function detects disconnection (including contact failure) of the resolver signals (S1 to S4). When the configuration of the resolver signal input circuit in **Section 49.2.5.1, Resolver Signal Input (Differential) Circuit** is used, voltage of the differential signal acquired by ΔΣADC (SINMNT, COSMNT) rises if a resolver signal line is disconnected, and the RDC error interrupt request signal becomes high. For a description of the relationship between register values and threshold values, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics.*

When operation with a VR resolver is selected (by setting values other than the combination of EXIO = 1 and SENS = 0), this function monitors the common levels of the monitored signals and determines any case of them exceeding the configured threshold to be a disconnection error. The threshold for differential voltage is set at 0.4V as the default and can be changed by the SGBTH[7:0] bits. When operation with a DC resolver is selected (by setting the combination of values as EXIO = 1 and SENS = 0), this function monitors the DC level of the monitored signals and determines any case of them exceeding the configured threshold to be a disconnection error. The threshold for differential voltage is set at 1.75 V as the default and can be changed by the SGBDTH[7:0] bits.

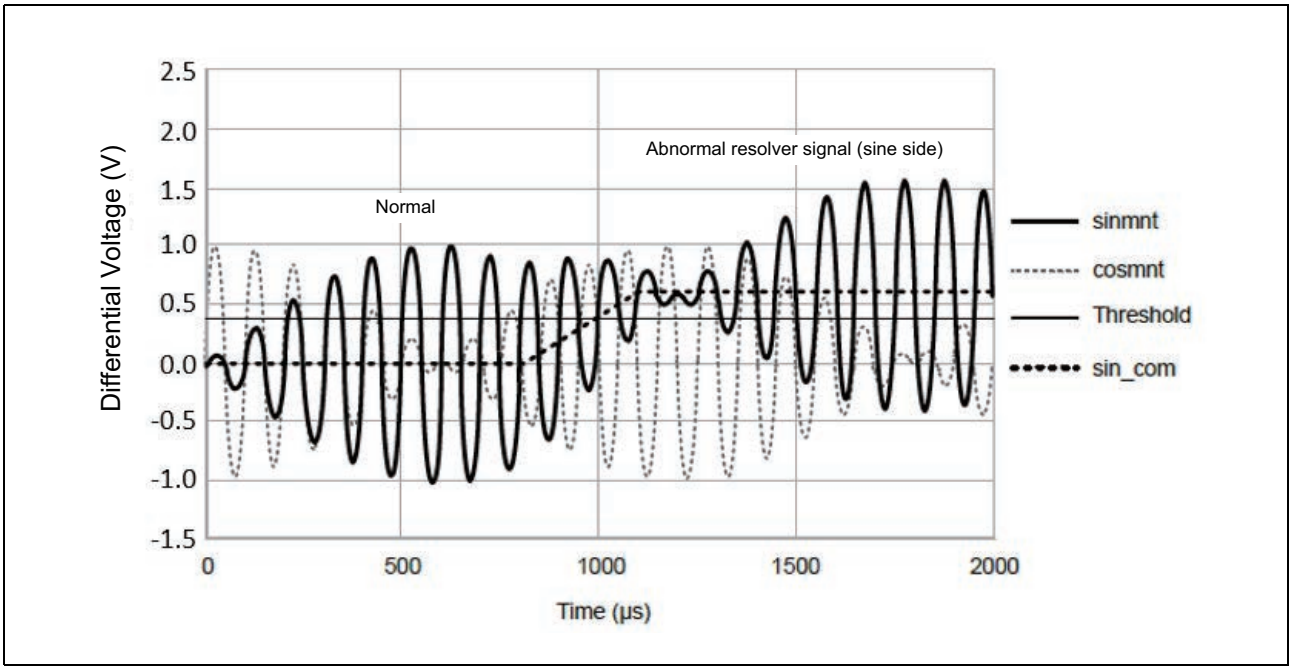


Figure 49.51 SINMNT,COSMNT differential voltage on Occurrence of Sin Signal Disconnection in VR Resolver

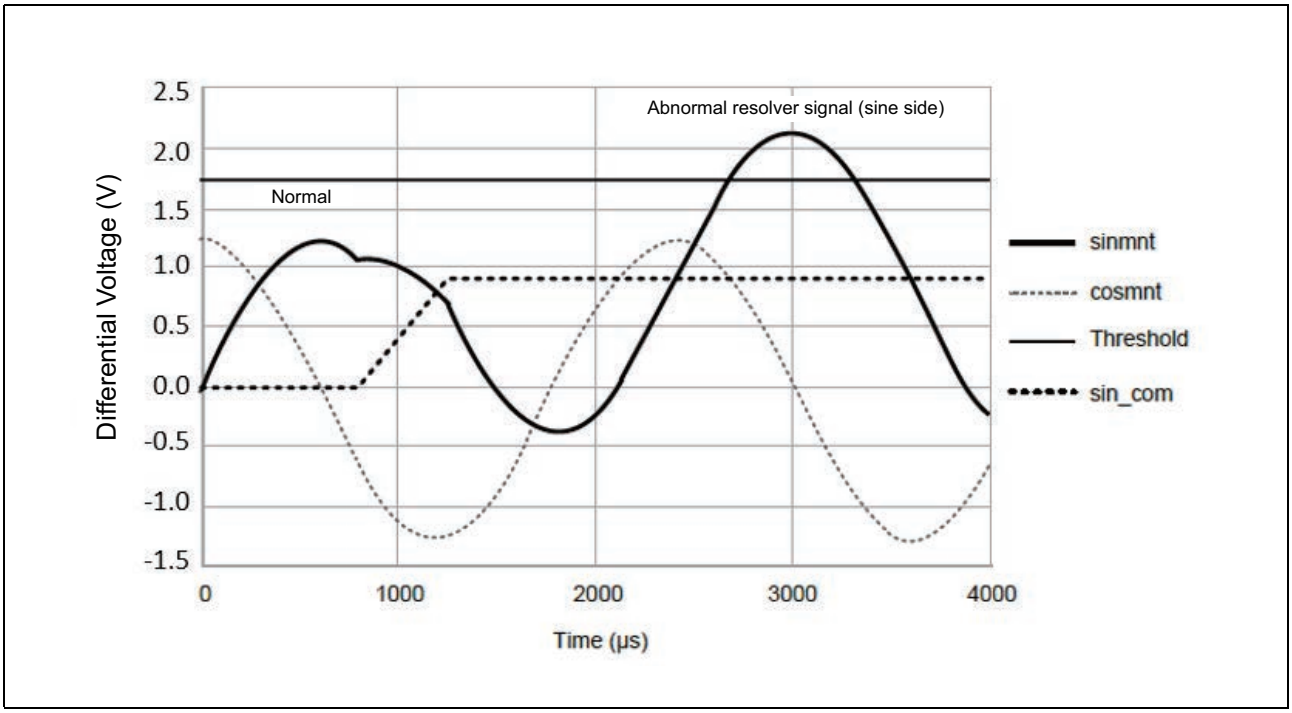


Figure 49.52 SINMNT,COSMNT differential voltage on Occurrence of Sin Signal Disconnection in DC Resolver

(4) R/D Conversion Error Detection

This function monitors the control variation in R/D conversion loop, and detects operation errors in the R/D conversion function. When an R/D conversion error is detected, the RDC error interrupt request signal becomes high. A control variation $(\theta - \varphi) \cdot f(t)$ is considered excessive if the control variation rises above or falls below a configured threshold level. For a description of the relationship between register values and threshold values, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics.*

An R/D conversion error is detected if the control variation stay excessive for more than 50% of the error determination time set in the EDPS[1:0] bits in the RDC3ASnDIAG1 register. The R/D conversion error detection circuit includes a circuit supporting high-speed rotation of a resolver and a circuit not supporting it. These circuits can be selected by using the CVEDS bit in the RDC3ASnDIAG1 register.

CVEDS = “0”: A circuit supporting high-speed rotation is selected. However, this setting is not allowed when the excitation frequency is set to 22 kHz or above.
When this setting is selected, set EDPS[1:0] to 10 or 11.

CVEDS = “1”: A circuit not supporting high-speed rotation is selected.

(5) Two Paths Comparison Conversion Error Detection

This function compares the results of angle conversion from two loops, and detects conversion errors in the circuit. The phi angle outputs of conversion loops 0 and 1 are compared, and if the difference between two angles is larger than the threshold, this is judged to be a two paths comparison conversion error. The threshold value is set by the P2ANT[1:0] bits.

(6) Sum-of-Squares Amplitude Error Detection

This function detects modulation, distortion and noise in the amplitudes of the sine and cosine signals input from the resolver for each excitation cycle. This error detection function can be used for resolver input signals with excitation components, but cannot be used for DC resolver input signals without excitation components.

The sum-of-squares of the sin, cos signals (SINMNT, COSMNT) are taken by ΔΣADCs and integrated within the excitation period. Upper and lower threshold value are set for the integrated value, and the number of excitation cycles that exceed this threshold is counted. If the number exceeds the threshold for the counted value, it is output as a sum-of-squares amplitude error. The counted value can be read from the SQCNT[6:0] bits.

The procedure runs automatically, the user is only required to set the upper and lower threshold for the integrated sum-of-squares values in the SQHTH and SQLTH bits and the threshold counter value in the SQCTH. The counter values are cleared at the desired time by the writing to the SQERST bit. Setting the ERSQS bit to 0 enables the detection of sum-of-squares amplitude errors. After setting this bit to 0, clear the counted value by setting the SQERST bit to 1.

Since the excitation amplitude may also disappear when a BIST which can be executed during angle conversion proceeds, reset the counter value for abnormal values at the end of BIST by using the SQERST bit.

Figure 49.53 shows an example of waveforms where the amplitudes of the signals input to the resolver are reduced, the calculated value fell outside the threshold range three times, and a sum-of-squares amplitude error is generated.

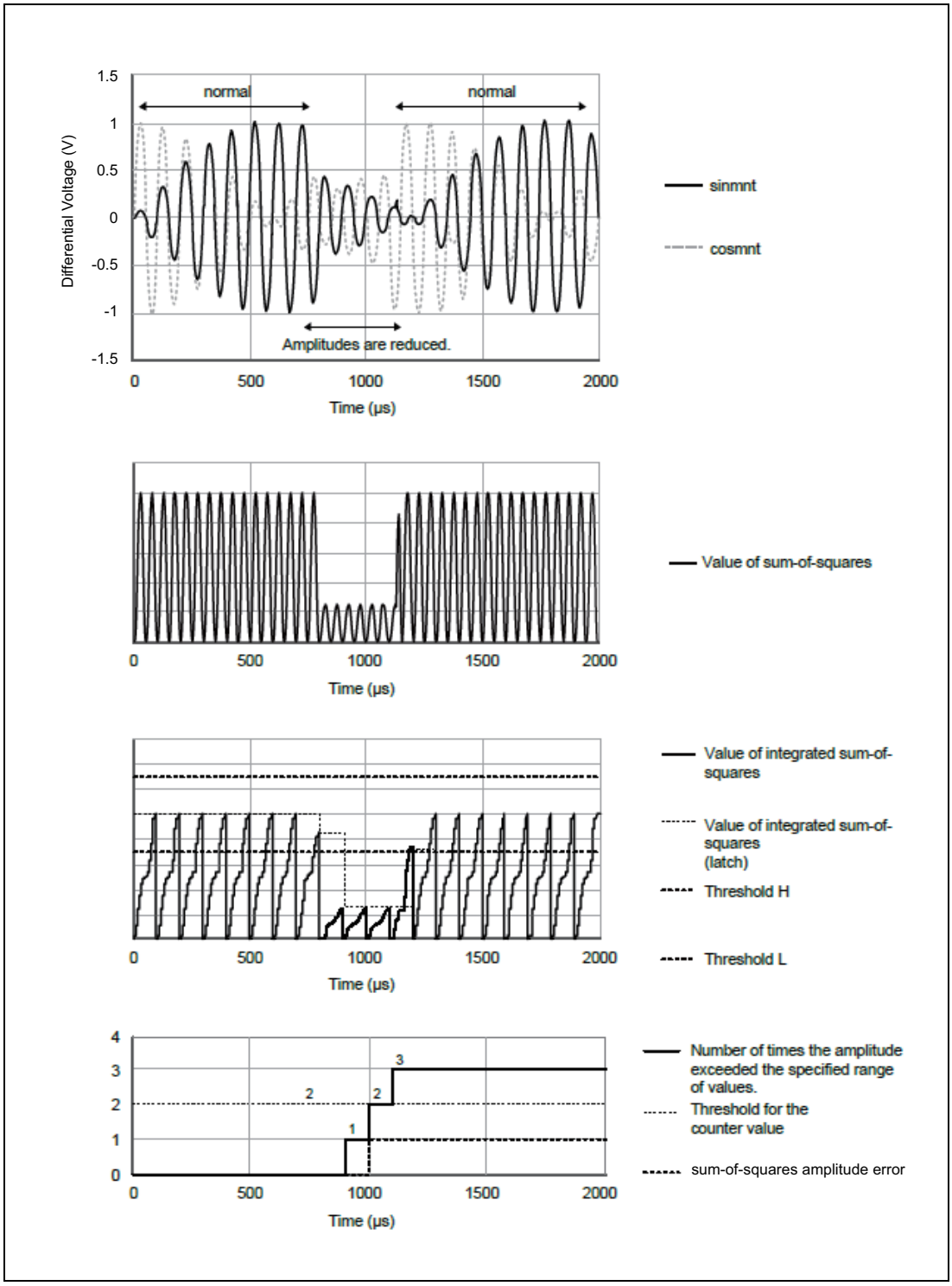


Figure 49.53 Example of Waveforms with Sum-of-Squares Amplitude Error

49.2.3.4 Self-Diagnosis

(1) Built-in Self-Test Function

In order to check the validity of a given operation, the Built-in Self-Test (BIST) function generates an intended signal input that is simulated internally by setting a BIST instruction in the RDC3ASnBIST1 register, and monitors the signal that is output in response to the simulated signal input **Table 49.111** lists test items.

Table 49.111 Details of BIST

Item	Diagnosis
Angle conversion BIST	Self-test of the R/D conversion function The following electrical angles can be set as a resolve signal input: • Target angle 0° • Target angle 45° • Target angle 270°
Error detection BIST	Self-test for the error detection function • Resolver signal error detection BIST • Resolver signal disconnect error detection BIST(sin/cos) • R/D conversion error detection BIST • Sum-of-Squares amplitude error detection BIST(high side/low side)

Each output during the execution of BIST operates in response to the simulated signal. Depending on the BIST, a RDC error interrupt is generated due to the erroneous internal state. If the occurrence of this error disturbs the operation, disable RDC error interrupt by the EINTEN bit.

BIST is classified into two types according to the length of execution time, short-period and long-period. Long-period BIST can be executed only when the power is turned on. The angular output does not match the resolver input because the long-period BIST operates on internally generated simulated signals for BIST for up to 10 ms.

Short-period BIST can be performed during angle conversion and maintains angle conversion tracking during BIST execution. Short-period BIST can be performed even when the power is turned on, but long-period BIST should be performed first.

- Short-period BIST: resolver signal error detection BIST, resolver signal disconnect error detection BIST(sin/cos), sum-of-squares amplitude error detection BIST (high side/low side)
- Long-period BIST: angle conversion BIST, conversion error BIST

Perform the following settings to execute BIST.

(1) Enable the forced gain control function when executing a BIST. (Set the AGCD bit in the RDC3ASnPI1 register to 0.)

(2) To execute a short-period BIST, set the EINTEN bit to 0 to disable error interrupts.

(3) Set the angle correction bits in the sine and cosine angle correction register to 0° when executing the angle conversion BIST.
Sine angle correction bits SINPO[11:0] = 000_H
Cosine angle correction bits COSPO[11:0] = 000_H

(4) To execute conversion error BIST, set the EDPS bit to 10_B.

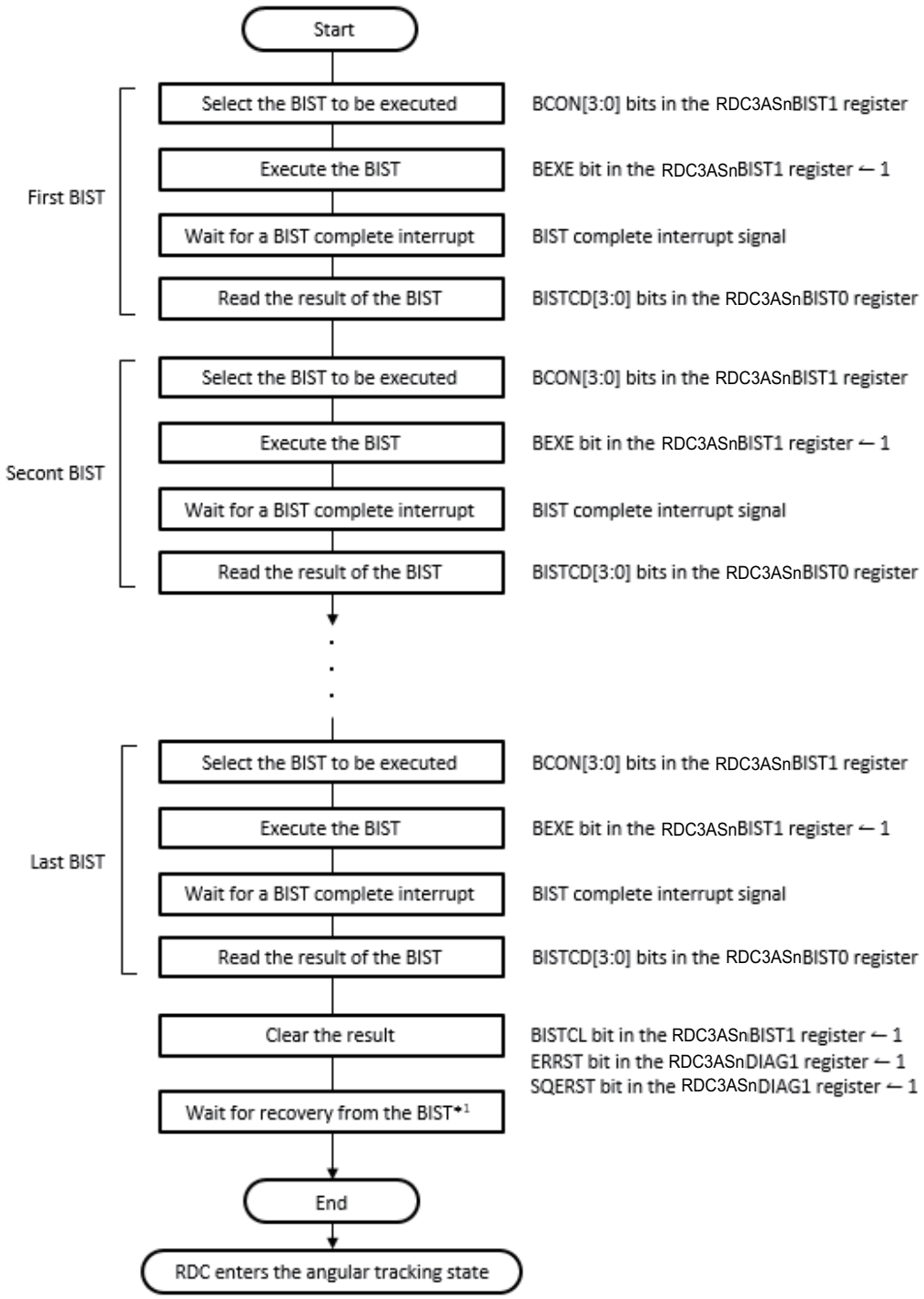
(5) Clear the count value in the SQERST bit by setting 1 before running sum-of-squares amplitude detection BIST (high side/low side).

(6) When the BIST is completed,
set the BISTCL bit in the RDC3ASnBIST1 register to 1 to clear the BIST results.
set the ERRST bit in the RDC3ASnDIAG1 register to 1 to reset the error signal.
set the SQERST bit in the RDC3ASnDIAG1 register to 1 to reset the counter value of sum-of-squares amplitude error.

Return the settings of the registers which were changed in steps (1), (2), (3) and (4) to their original values.

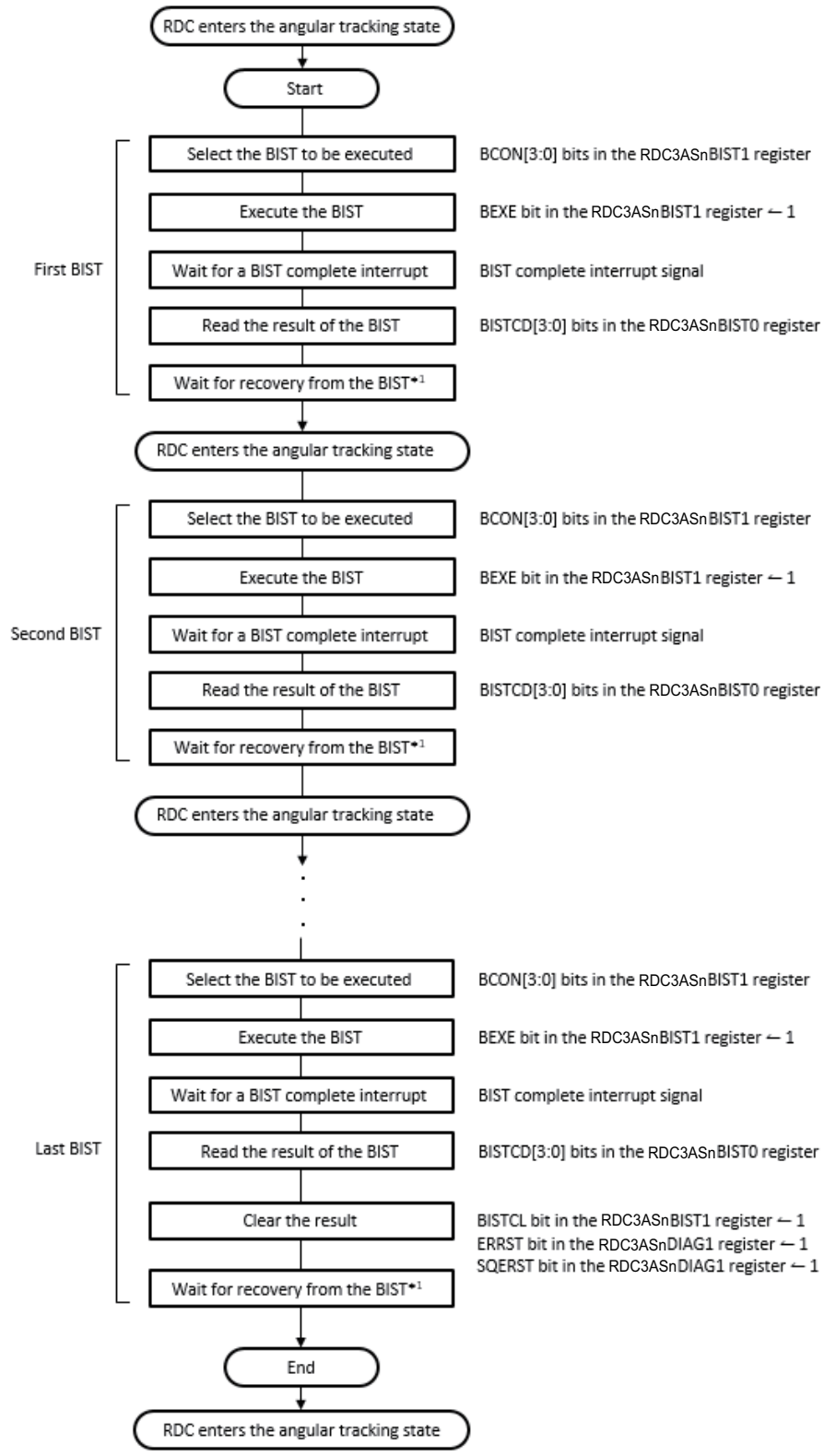
Table 49.112 BISTs for Each Setting of Values

BCON[3:0]	BIST to be Executed
0000	BEXE bit is disabled
0001	This setting is not allowed.
0010	Sum-of-squares amplitude error detection BIST (low side)
0011	Sum-of-squares amplitude error detection BIST (high side)
0100	This setting is not allowed.
0101	Angle conversion BIST (0°)
0110	Angle conversion BIST (45°)
0111	Angle conversion BIST (270°)
1000	This setting is not allowed.
1001	Error detection BIST: resolver signal error detection BIST
1010	Error detection BIST: resolver signal disconnection detection BIST (cosine side)
1011	Error detection BIST: Resolver signal disconnection detection BIST (sine side)
1100	Error detection BIST: conversion error BIST
1101	This setting is not allowed.
1110	This setting is not allowed.
1111	This setting is not allowed.



Note 1. See the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics* for the recovery time from a BIST.
Perform all long-period BISTs you want to perform first, and then perform short-period BISTs.
In the conversion error BIST, write 1 to the KIRST bit after reading the result.

Figure 49.54 Sequence of Executing BISTs after Starting Up the Power

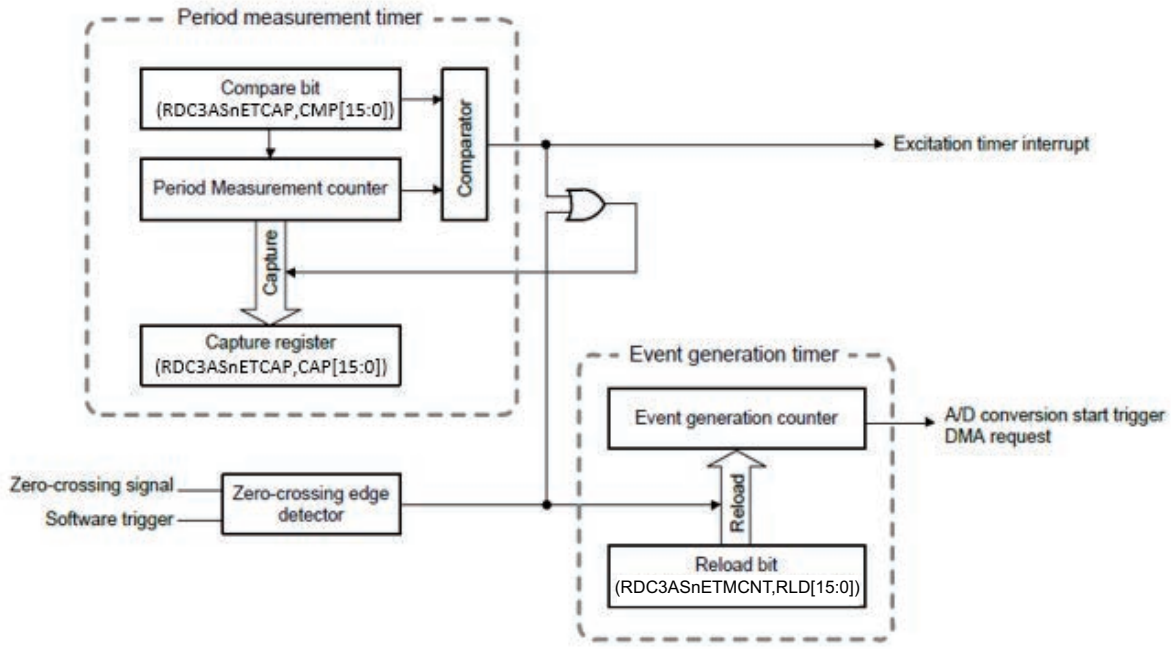


Note 1. See the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics* for the recovery time from a BIST.

Figure 49.55 Sequence of Executing BISTs during Angle Conversion (Short-period BIST)

49.2.3.5 Excitation Timer (ET) Function

The excitation timer comprises two 16-bit timers: a period measurement timer and an event generation timer. The operating clock of the timers is CCLK (40 MHz). **Figure 49.56** shows a block diagram of the excitation timer.



Note: n = 0, 1

Figure 49.56 Block Diagram of Excitation Timer

(1) Period Measurement Timer

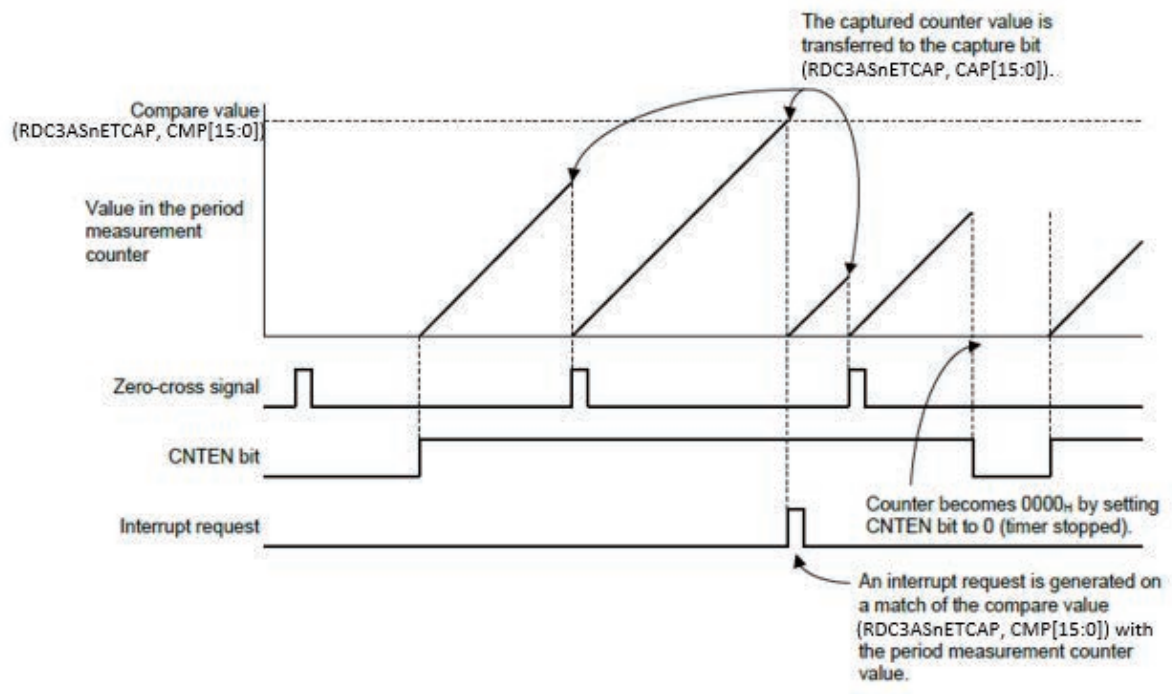
The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable from rise edge and fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in ET Compare bits of the RDC3ASnETCAP register. By reading the RDC3ASnETCAP register, the cycle of excitation signal can be obtained.

The cycle of excitation signal can be calculated from the following formula: (RDC3ASnETCAP register value + 1) × CCLK cycle (25 ns).

When the IREN bit in the RDC3ASnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request is generated if the value set in ET Compare bits of the RDC3ASnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the RDC3ASnETCAP register.

When a zero-crossing signal trigger is generated by writing 1 to the ZCSTRG bit in the RDC3ASnETEN register, the period measurement timer operates in the same way as the zero-crossing signal edge detection.

Figure 49.57 shows an example of period measurement timer operation.



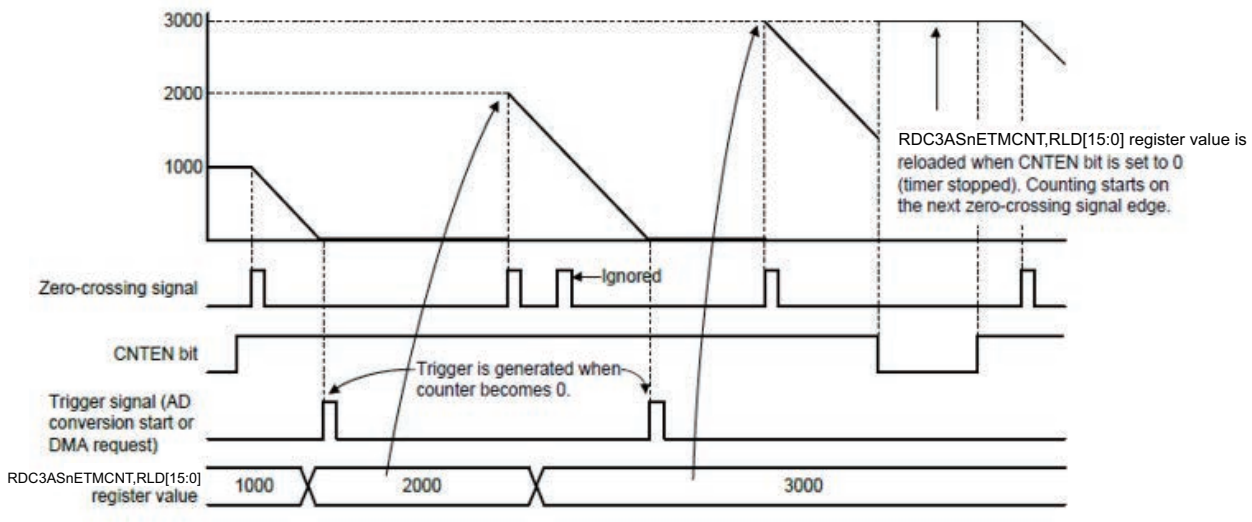
Note: n = 0, 1
CNTEN: A bit in the RDC3ASnETEN register

Figure 49.57 Example of Period Measurement Timer Operation

(2) Event Generation Timer

The event generation timer can generate a trigger signal (A/D conversion trigger, DMA request) after the time set in the RDC3ASnETMCNT register has elapsed since the occurrence of an edge of the zero-crossing signal. When a zero-crossing signal trigger is generated by writing 1 to the ZCSTRG bit in the RDC3ASnETEN register, the event generation timer operates in the same way as the zero-crossing signal edge detection.

Figure 49.58 shows an example of event generation timer operation.

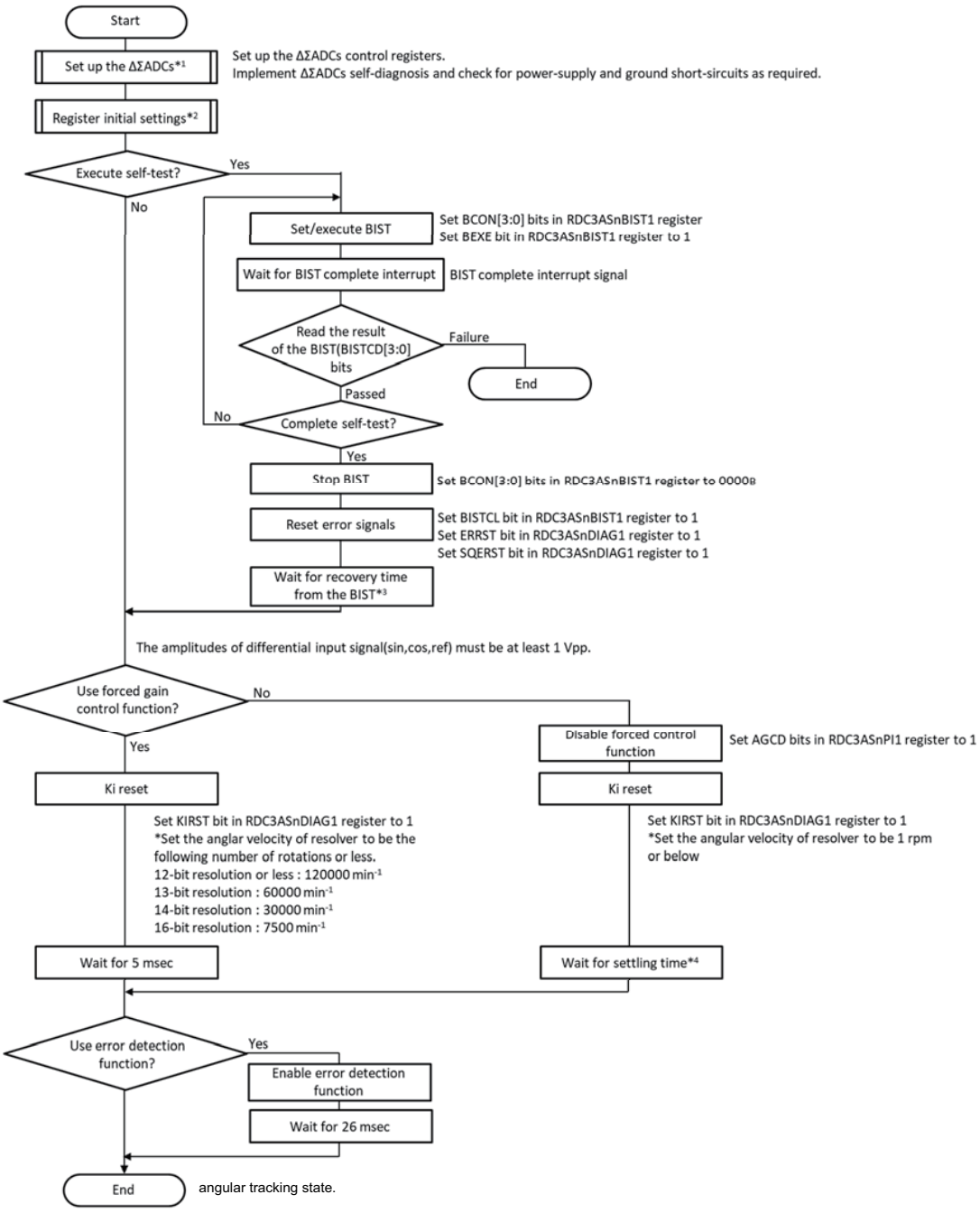


Note: n = 0, 1
CNTEN: A bit in the RDC3ASnETEN register

Figure 49.58 Example of Event Generation Timer Operation

49.2.4 Initial Settings Sequence for the RDC

Figure 49.59 shows the procedures of initial settings.



Note 1. See **Section 49.2.4.1, ΔΣADC settings**

Note 2. See **Table 49.113**

Note 3. For the recovery time from a BIST, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics*

Note 4. For the settling time, see the *RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics*

Figure 49.59 RDC3AS Initial Operation Flow

Table 49.113 List of Bits which are Not to be Set in "Register Initial Settings". Set bits other than those listed in this table in "Register Initial Settings"

Register Name	Bit Name
RDC3ASnPHICP0	INTCLR[2:0]
RDC3ASnSCCOR1	PHCST, GNCST
RDC3ASnDIAG1	ERDEN, SQERST, ERRST, KIRST
RDC3ASnBIST1	BISTCL, BEXE, BCON
RDC3ASnENC0	PHILT, OMGLT, REFZEN,CINTEN,ABEN,UVWEN,ZEN,EINTEN
RDC3ASnTBUS	DATSEL[6:0]
RDC3ASnETEN	ZCSTRG, CMPEN, IREN, DREN, ADTEN, CNTEN

49.2.4.1 ΔΣADC settings

This section describes the setting of ΔΣADC registers to operate this RDC.

- Differential input setting: Set to DSADCmVCRj.CNVCLS[1:0]*1 = 2_H.
- High accuracy mode: Set to DSADCmUCR.RESO0*1 = 0_H.
- Set the filter setting of ΔΣADC to F1a, F1b, F2, F3a, F3b, F4, or F5.

According to the set filter settings, set the group delay and output cycle settings in the RDC register bits DSDL [1: 0] and DSFQ [1: 0] at the RDC register initialization stage.

- Set the resolver signal differential amplitude and ΔΣADC gain settings so that the differential output amplitude from the ΔΣADC falls within the following range. If you select ΔΣADC gain x8, the accuracy of ΔΣ ADC will deteriorate, so avoid x8 as much as possible.

  ΔΣADC differential output amplitude range: 0.34×(ADSVREFH - ADSVREFL) to 0.66×(ADSVREFH - ADSVREFL)

- Start the three ΔΣADC units to be used. Startup can be synchronized or unsynchronized.
- Overwrite error occurs in the 3 ΔΣADC units used for RDC. For this reason, take the following actions.
  - Do not use the write flag (DSADCmDIRj.WFLG*1) of the data supplementary information register j.
  - Ignore the overwrite error (DSADCmER.OWE*1) of the error register.
  - Disable the overwrite error interrupt. (Set DSADCmSFTCR.OWEIE*1 = 0_H)
- ΔΣADC channels not used in RDC can be used independently of RDC.

Note 1. "m" means unit number of DSADC in this. "j" means virtual channel number of each DSADC in this. About RDC3AS0, sin signal is DSADC00, cos signal is DSADC15, excitation signal is DSADC13. About RDC3AS1, sin signal is DSADC10, cos signal is DSADC12, excitation signal is DSADC11.

49.2.5 Resolver Interface Circuits

The following shows specific interface circuits as reference examples. When determining constants such as a resistance value and adding functions such as an input/output protection circuit, a careful decision must be made for each system and conduct adequate evaluation.

49.2.5.1 Resolver Signal Input (Differential) Circuit

Figure 49.60 shows the resolver signal input (differential) circuit.

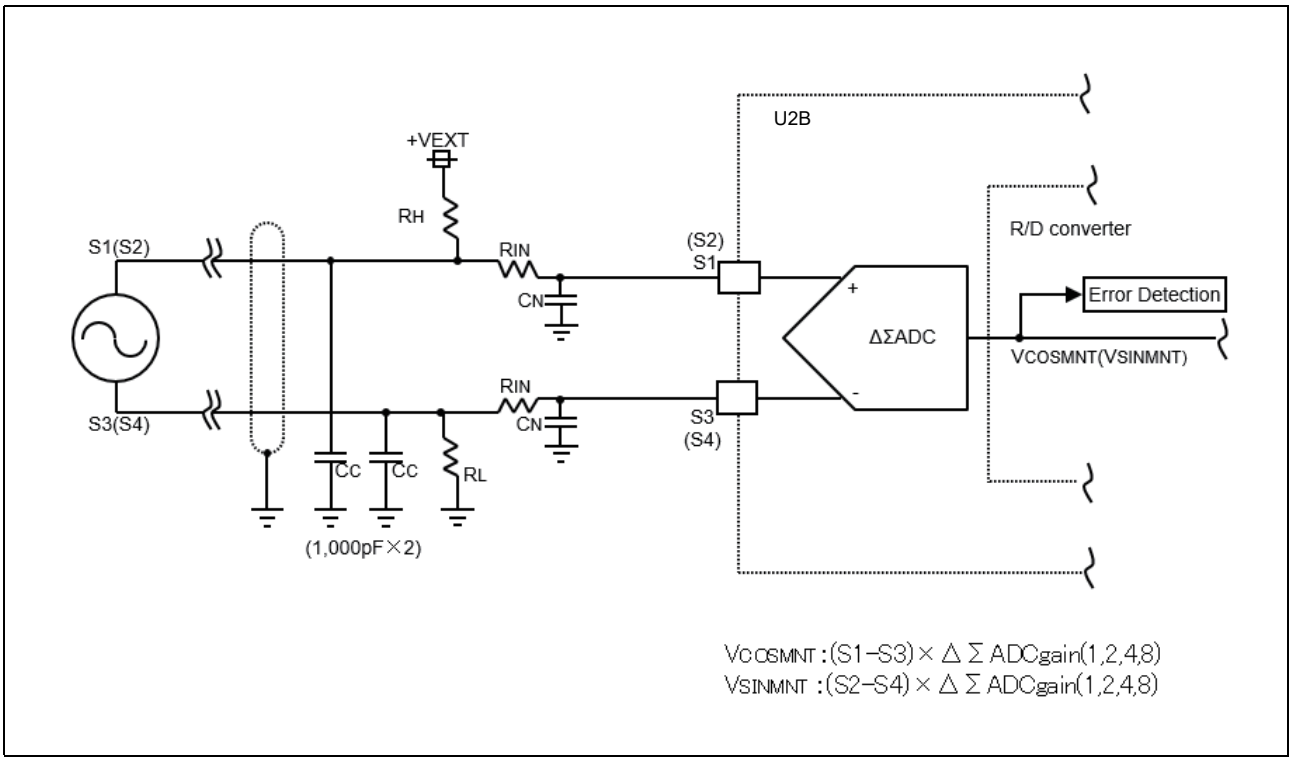


Figure 49.60 Resolver Signal Input Circuit

- Input signal level

  VCOSMNT and VSINMNT can be confirmed by COSPK [12: 0], SINPK [12: 0], CMNMAX [13: 0], SMNMAX [13: 0], CMNTAD1 [12: 0], SMNTAD1 [12: 0]. The gain multiplication setting (X2, X4, X8) built into ΔΣADC can be used. If the gain multiple setting is used, the RDC angle conversion accuracy may deteriorate.

- R_H and R_L: This resistance is required to detect resolver signal disconnection abnormality. Determine a resistance value from the following calculated values and so that the Sx pin input common potential is 0.5 x (ADSVREFH - ADSVREFL) (= V_{COM}).
  VR resolver setting: the resistance is 80% or less from the following calculated values, and it must be 80 kΩ or above.
  $R_H < (V_{COM} /VEXT) \times (VEXT/ V_{COM} - 1) \times \{(VEXT - 0.4)/(2.4 \times 10^{-6})\}$
  $R_L < (V_{COM} /VEXT) \times \{(VEXT - 0.4)/(2.4 \times 10^{-6})\}$
  DC resolver setting : the resistance is 80% or less from the following calculated values, and it

must be 80 kΩ or above.

$R_H < (VEXT - V_{COM} + 0.435) \times 1.14 \times 10^5 - 2 \times 10^5$

$R_L < (V_{COM} + 0.435) \times 1.14 \times 10^5 - 2 \times 10^5$

- RIN and CN: Configure anti-aliasing filter. Select the cutoff frequency to be in the range of 200kHz to 400kHz.

49.2.5.2 Resolver Excitation Signal External Input Circuit

(1) Resolver Excitation Signal Input Circuit with Single Power Supply

Figure 49.61 shows the equivalent circuit of the external resolver excitation signal input section.

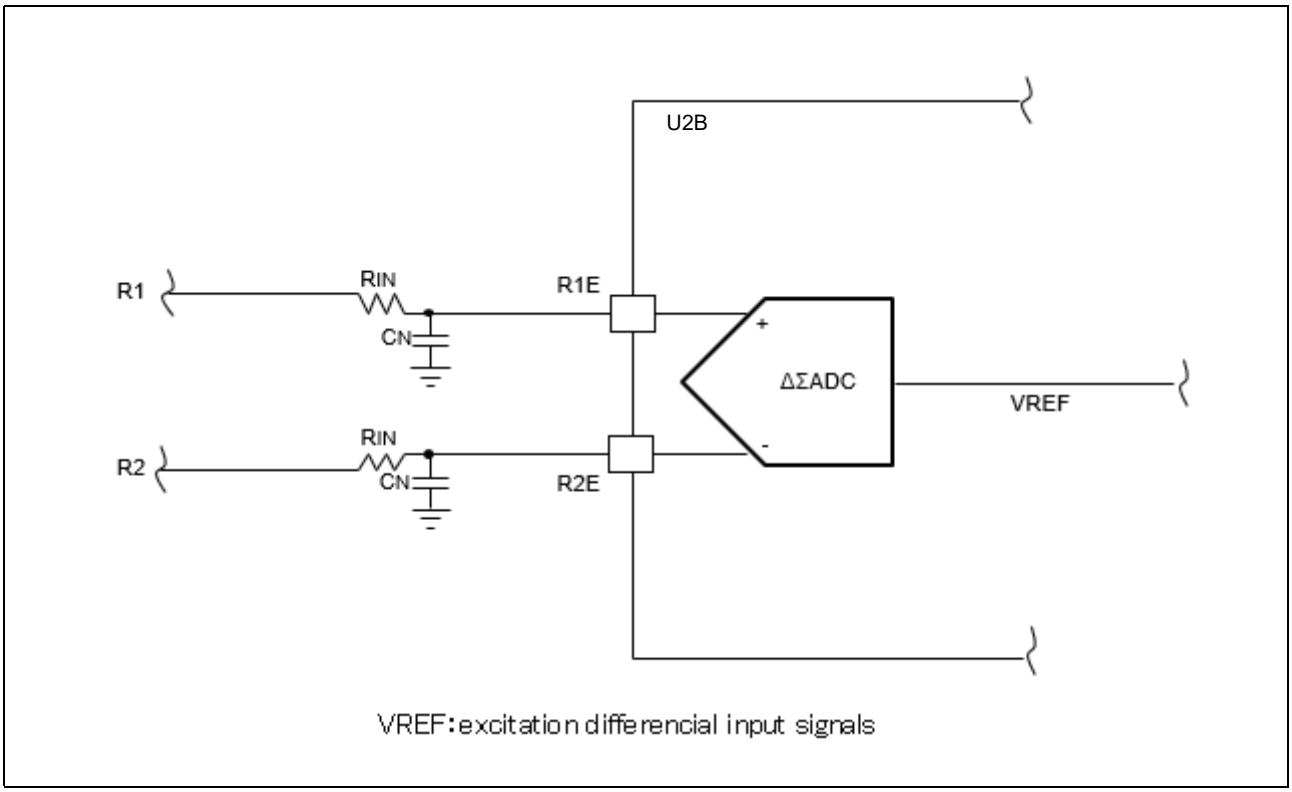


Figure 49.61 Resolver Excitation Signal External Input Circuit

- input signal level: Adjust so that the input common potential of the R1E and R2E pins is 0.5 x (ADSVREFH - ADSVREFL).

- RIN and CN: Configure anti-aliasing filter. Select the cutoff frequency to be in the range of 200kHz to 400kHz.

49.2.5.3 Usage Noise

When the resolver is used as a motor sensor, the resolver signal is affected by various types of noises depending on the drive control configuration of the motor. To perform R/D conversion successfully, sufficient S/N ratio of the resolver signal is required.

This RDC is a highly responsive R/D conversion module. Although considerations have been made for noise immunity, the RDC by itself is not designed to accommodate all noise environmental factors. Appropriate peripheral circuits need to be considered depending on the environment in which the module is deployed. The following describes the specific countermeasures for noise in [Countermeasure I] to [Countermeasure VIII] as reference.

(1) Countermeasures for Magnetic Disturbance Noise

If the leakage flux of the motor passes through the resolver, the resolver signal behaves as if the angle changes, resulting in malfunction.

[Countermeasure I]

When installing the motor and resolver, use the configuration and material that block the magnetic loop passing through the resolver (magnetic shield effect) to minimize the leakage flux of the motor that passes through the resolver.

[Countermeasure II]

If the leakage flux of the motor that passes through the resolver cannot be completely avoided, raise the resolver excitation voltage (current) to improve the S/N ratio of the original signals.

(2) Countermeasures for Electric Disturbance Noise

The electric disturbance (spike noise, and so on) caused by the PWM drive of the motor is extremely large, and affects all power systems, such as the excitation signal lines of resolver and power supply line, via various paths.

[Countermeasure III]

Insert a common mode/normal mode filter into the resolver excitation lines to remove the spike noise components. Generally, the low-impedance excitation line hardly has noise and the countermeasure is less needed.

[Countermeasure IV]

Insert a common mode/normal mode filter into the resolver signal lines (RDC3ASnS1-RDC3ASnS3, RDC3ASnS2- RDC3ASnS4) to remove the spike noise components. Select the time constant that takes effect only on noise and leaves the original resolver signal waveform undistorted. In addition, ensure that the electric noise waveform of the RDC3ASnS1 to RDC3ASnS4 pins viewed from ADSVSS (ground) are in phase. If an error due to electric external disturbance noise persists after this countermeasure is taken, keeping the resolver signal level low can be effective.

[Countermeasure V]

If necessary, insert a bypass capacitor to the power supply (ADSVCC) line.

(3) Other General Measures

[Countermeasure VI]

Use a shielded twisted pair cable for resolver wiring. Shielded terminals must be treated collectively on the circuit side (grounded to GND). The cable must be routed separately from the motor cable.

[Countermeasure VII]

Enhance the GND system for low impedance to reduce common impedance noise and to provide shielding effect. Another possible measure is to fix the potential of the motor driver radiator and motor case to the control-system ground potential.

[Countermeasure VIII]

Physically separate the motor driver from the sensor circuit and cover each of them with a shield case.

49.3 Usage Notes

49.3.1 Notes on Using Analog Input Pins

Do not perform A/D conversion or RDC3AL's conversion for the same analog pin with SAR-ADC, DSADC and RDC3AL*1 at the same time.

Doing so may degrade the A/D conversion accuracy or the conversion accuracy of RDC3AL.

Note 1. Target analog pins is RDC3ALn_S4, RDC3ALn_S2, RDC3ALn_S1, RDC3ALn_S3, RDC3ALn_SINMNT, RDC3ALn_COM, RDC3ALn_RSO and RDC3ALn_COSMNT in RDC3ALn.

49.3.2 Notes on Using RDC3AL or FCMP

When RDC3AL is used, set FCMP to module standby.

When FCMP is used, set RDC3ALnRDSTP to 00000001_H and set RDC3AL to module standby.

If not doing so, it may degrade the conversion accuracy of RDC3AL or the comparison accuracy of FCMP.

49.3.3 Notes on Using SAR-ADC and FCMP operate at 3.3V voltage

SAR-ADC and FCMP can operate at 3.3 V voltage. When SAR-ADC or FCMP operate at 3.3 V voltage, please set RDC3ALnRDSTP to 00000001_H and set RDC3AL to module standby mode.

RH850/U2B Group Resolver to Digital Converter
User's Manual: Hardware

Publication Date: Rev.0.40 February 26, 2021
Rev.1.20 February 28, 2025

Published by: Renesas Electronics Corporation

RH850/U2B Group
Resolver to Digital Converter

Renesas Electronics Corporation

R01UH0928EJ0120