

RH850/P1M-E

Flash Memory

User's Manual: Hardware Interface

Renesas microcontroller

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (<http://www.renesas.com>).

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Table of Contents

Section 1	Features.....	6
Section 2	Module Configuration.....	7
Section 3	Address Map.....	8
Section 4	Registers.....	9
4.1	Flash Pin Monitor Register (FPMON)	9
4.2	Flash Access Status Register (FASTAT).....	10
4.3	Flash Access Error Interrupt Enable Register (FAEINT)	12
4.4	Code Flash Memory Area Select Register (FAREASELC).....	13
4.5	FACI Command Start Address Register (FSADDR).....	14
4.6	FACI Command End Address Register (FEADDR).....	15
4.7	Flash Status Register (FSTATR)	16
4.8	Flash P/E Mode Entry Register (FENTRYR)	21
4.9	Code Flash Protect Register (FPROTR)	23
4.10	Flash Sequencer Set-Up Initialize Register (FSUINITR)	24
4.11	Lock Bit Status Register (FLKSTAT)	25
4.12	FACI Reset Transfer Status Register (FRTSTAT).....	26
4.13	FACI Reset Transfer Error Interrupt Enable Register (FRTEINT)	27
4.14	FACI Command Register (FCMDR)	28
4.15	Flash P/E Status Register (FPESTAT)	29
4.16	Data Flash Blank Check Control Register (FBCCNT)	30
4.17	Data Flash Blank Check Status Register (FBCSTAT).....	31
4.18	Data Flash Programming Start Address Register (FPSADDR)	32
4.19	Flash Sequencer Process Switch Register (FCPSR)	33
4.20	Flash Sequencer Processing Clock Notify Register (FPCKAR)	34
4.21	Flash Emulation Control Register (FLEMU)	35
4.22	Flash Emulation Address Specify Register (FLEAD).....	36
4.23	Flash ECC Encoder Monitor Register (FECCEMON).....	37
4.24	Flash ECC Test Mode Register (FECCTMD)	38
4.25	Flash Dummy ECC Register (FDMYECC)	39
4.26	BFA Selection Register (BFASELR).....	40
4.27	Self-Programming ID Input Registers (SELFID0 to SELFID3)	41
4.28	Self-Programming ID Authentication Status Register (SELFIDST)	42
Section 5	Flash Sequencer Modes	43
5.1	Operating Modes of the Flash Sequencer	43
Section 6	FACI Command	44
6.1	List of FACI Commands.....	44
6.2	Relationship between Flash Sequencer Status and FACI Commands	46

6.3	Use FACI Command.....	48
6.3.1	Overview of the Command Usage in Code Flash P/E Mode.....	48
6.3.2	Overview of the Command Usage in Data Flash P/E Mode.....	49
6.3.3	Shift to Code Flash Program/Erase Mode.....	50
6.3.4	Shift to Data Flash Program/Erase Mode.....	50
6.3.5	Shift to Read Mode.....	51
6.3.6	ID Authentication	52
6.3.7	Return from Command Lock State.....	53
6.3.8	Program Command Issue.....	55
6.3.9	DMA Program Command	57
6.3.10	Block Erase Command.....	58
6.3.11	Program/Erase Suspend Command	59
6.3.12	Program/Erase Resume Command	64
6.3.13	Status Clear Command	65
6.3.14	Forced Stop Command	66
6.3.15	Blank Check Command.....	67
6.3.16	Config Program Setting Command.....	69
6.3.17	Reading the Configuration Setting Area	71
6.3.18	Lock Bit Program Command	72
6.3.19	Lock Bit Read Command.....	73
6.3.20	OTP Set Command	74
6.3.21	Reading the OTP Setting Area	76
6.3.22	Injecting ECC Errors for the Flash Memory.....	77
Section 7	Security Function	80
7.1	FACI Command Protection by ID	80
7.2	OTP for Code Flash Memory.....	80
Section 8	Protection Function.....	81
8.1	Hardware Protection.....	81
8.2	Software Protection	81
8.2.1	Protection by FENTRYR.....	81
8.2.2	Protection by Lock Bit.....	81
8.3	Error Protection.....	82
8.4	Boot Program Protection	84
8.4.1	Variable Reset Vector.....	84
8.5	Blank Checking of Code Flash Memory	85
Section 9	Usage Notes	86
Section 10	Electrical Specifications	88
10.1	Code Flash Characteristics.....	88
10.2	Data Flash Characteristics.....	90

Section 1 Features

The features of the flash memory are described below. See the user's manual for information on the capacity, block configuration, and addresses of the flash memory in a given product.

Flash Memory Programming/Erase

A dedicated sequencer for the flash memory (flash sequencer) executes programming and erasure via the P-Bus. The flash sequencer also supports the program/processing suspend/resume and BGO (background operation)*¹.

Note 1. This can be used during overwriting of the data flash memory and reading of the code flash memory.

Security Functions

The flash memory incorporates hardware functions to prevent illicit tampering.

Protection Functions

The flash memory incorporates hardware functions to prevent erroneous writing.

Interrupts

The flash memory supports an interrupt to indicate completion of processing by the flash sequencer and an error interrupt to indicate erroneous operations.

DMA

The flash memory supports DMA writing to the data flash memory.

Section 2 Module Configuration

Modules related to the flash memory are configured as shown in **Figure 2.1**. The flash sequencer is configured of the FCU and FACI. The FCU executes basic control of overwriting of the flash memory. The FACI receives FACI commands via the P-Bus and controls FCU operations accordingly.

In the transfer operations in response to a reset, the FACI transfers the data from flash memory to the option byte storage registers in the ID control section (FACI reset transfer). The ID control section compares the ID transferred from the flash memory with the value in the SELFID0 to SELFID3 registers. Data set in the option bytes of the flash memory can be read out from the option byte storage registers via the P-Bus.

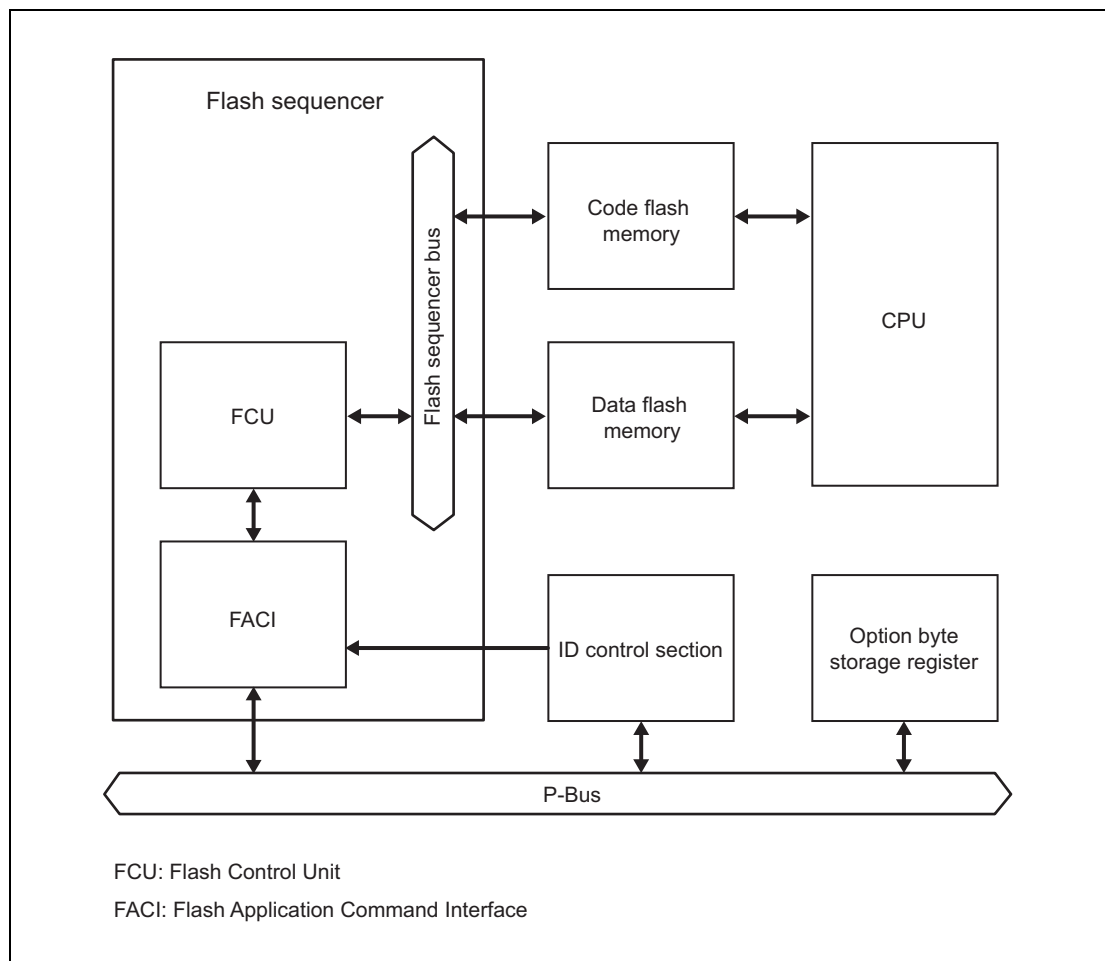


Figure 2.1 Configuration of Flash Memory Related Modules

Section 3 Address Map

Using the hardware interface with the flash memory requires access to the areas listed in **Table 3.1**. When reading the configuration setting area, or OTP setting area, set the BFAA bit of the BFASCLR register to 1.

Table 3.1 Information on the Hardware Interface Area

Area	Address	Capacity	Peripheral IP Group
Area containing the various registers of the hardware	See Section 4, Registers	See Section 4, Registers	*1
FACI command-issuing area	FFA2 0000 _H	4 bytes	5
Configuration setting area	FF30 0040 _H to FF30 008F _H	80 bytes	0
OTP setting area	FF38 0040 _H to FF38 009F _H	96 bytes	0

Note 1. See the *RH850/P1M-E User's Manual: Hardware*.

See the *RH850/P1M-E User's Manual: Hardware* for information on the addresses of the flash memory etc.

Section 4 Registers

This section gives information on the registers. For registers that are not specifically mentioned, only reset them to their initial states.

For information on the option byte storage registers, see the user's manual of each product.

4.1 Flash Pin Monitor Register (FPMON)

FPMON indicates the state of the FLMD0 pin.

Access: This register can only be read in 8-bit units.

Address: FFA1 0000_H

Value after reset: X0_H

Bit	7	6	5	4	3	2	1	0
	FWE	—	—	—	—	—	—	—
Value after reset	0/1	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.1 FPMON Register Contents

Bit Position	Bit Name	Function
7	FWE	Flash Write Enable Monitors the level on the FLMD0 pin. The value of the FWE bit indicates whether transitions to the code flash programming/erasure mode are enabled or disabled. 0: Transitions to the code flash program/erasure mode are disabled. 1: Transitions to the code flash program/erasure mode are enabled.
6 to 0	Reserved	When read, the value after reset is read.

4.2 Flash Access Status Register (FASTAT)

FASTAT indicates access error status for code/data flash. If either of CFAE/CMDLK/DFAE bits in FASTAT is set to 1, flash sequencer enters “Command Lock” state. To cancel “Command Lock” state, set the CFAE and DFAE bits in the FASTAT register to 0, and then issue a “Status Clear” or a “Forced Stop” command to FACI.

Access: This register can be read/written in 8-bit units.

Address: FFA1 0010_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	CFAE	—	—	CMDLK	DFAE	—	—	ECRCT
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R	R	R	R/W ^{*1}	R	R	R

Note 1. Only “0” can be written to clear flag after “1” is read.

Table 4.2 FASTAT Register Contents (1/2)

Bit Position	Bit Name	Function
7	CFAE	<p>Code Flash Access Error</p> <p>Indicates whether or not code flash access error has been generated. If this bit becomes “1”, ILGLERR bit in FSTATR is set to “1” and flash sequencer enters “Command Lock” state.</p> <p>0: No code flash access error has occurred.</p> <p>1: Code flash access error has occurred.</p> <p>[Setting Condition]</p> <p>FACI command with the following setting has been issued in code flash program/erasure mode.</p> <ul style="list-style-type: none"> When user area is selected, the settings for FAREASELC is 00_H and for bits 23 to 0 in FSADDR are 20_0000_H to FF_FFFF_H (reserved area for the user area). When extended user area is selected, the settings for FAREASELC is 02_H and for bits 23 to 0 in FSADDR are 00_8000_H to FF_FFFF_H (reserved area for the extended user area). <p>[Clearing Condition]</p> <p>“0” is written after reading “1” from this bit.</p>
6, 5	Reserved	When read, the value after reset is read. When writing, write the value after reset.
4	CMDLK	<p>Command Lock</p> <p>Indicates whether flash sequencer is in “Command Lock” state.</p> <p>0: Flash sequencer is not in “Command Lock” state.</p> <p>1: Flash sequencer is in “Command Lock” state.</p> <p>[Setting Condition]</p> <p>FACI detects error and enters “Command Lock” state.</p> <p>[Clearing Condition]</p> <p>The flash sequencer starts the “Status Clear” or “Forced Stop” command processing while the CFAE and DFAE bits in the FASTAT register are 0.</p>

Table 4.2 FASTAT Register Contents (2/2)

Bit Position	Bit Name	Function
3	DFAE	<p>Data Flash Access Error</p> <p>Indicates whether or not data flash access error has been generated. If this bit becomes "1", ILGLERR bit in FSTATR is set to "1" and flash sequencer enters "Command Lock" state.</p> <p>0: No data flash access error has occurred. 1: Data flash access error has occurred.</p> <p>[Setting Conditions]</p> <p>Commands have been issued in data flash program/erasure mode under the following settings.</p> <ul style="list-style-type: none"> FACI command has been issued when the setting of bits 18 to 0 in the FSADDR register is 1_0000_H to 7_FFFF_H (reserved area for the data area). Config Program setting command has been issued when the setting of bits 18 to 0 in the FSADDR register is 0_0000_H to 0_003F_H or 0_0100_H to 7_FFFF_H. "OTP Set" command has been issued when the settings for bits 18 to 0 in FSADDR are 0_0000_H to 0_003F_H or 0_00A0_H to 7_FFFF_H. <p>[Clearing Condition]</p> <p>"0" is written after reading "1" from this bit.</p>
2, 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECRCT	<p>Error Correction</p> <p>Indicates that a 1-bit error has been corrected when the flash sequencer reads the flash memory (configuration setting, overwrite parameters, and OTP setting).</p> <p>0: 1-bit error has not been corrected. 1: 1-bit error has been corrected.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> The flash sequencer starts the "Status Clear" or "Forced Stop" command processing when bits CFGCRCT, TBLCRCT, and OTPCRCT in FSTATR are 1.

4.3 Flash Access Error Interrupt Enable Register (FAEINT)

FAEINT enables or disables output of flash access error (“FLERR”) interrupt.

Flash access error interrupt is handled as an error source of ECM with this product.

Access: This register can be read/written in 8-bit units.

Address: FFA1 0014_H

Value after reset: 99_H

Bit	7	6	5	4	3	2	1	0
	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	ECRCTIE
Value after reset	1	0	0	1	1	0	0	1
R/W	R/W	R	R	R/W	R/W	R	R	R/W

Table 4.3 FAEINT Register Contents

Bit Position	Bit Name	Function
7	CFAEIE	Code Flash Access Error Interrupt Enable Enables or disables “FLERR” interrupt request when code flash access error occurs and CFAE bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when CFAE = “1”. 1: Generates “FLERR” interrupt request when CFAE = “1”.
6, 5	Reserved	When read, the value after reset is read. When writing, write the value after reset.
4	CMDLKIE	Command Lock Interrupt Enable Enables or disables “FLERR” interrupt request when flash sequencer enters “Command Lock” state and CMDLK bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when CMDLK = “1”. 1: Generates “FLERR” interrupt request when CMDLK = “1”.
3	DFAEIE	Data Flash Access Error Interrupt Enable Enables or disables “FLERR” interrupt request when data flash access error occurs and DFAE bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when DFAE = “1”. 1: Generates “FLERR” interrupt request when DFAE = “1”.
2, 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECRCTIE	Error Correction Interrupt Enable Enables or disables the “FLERR” interrupt request when a 1-bit error has been corrected and the ECRCT bit in FASTAT has been set to 1 on the flash memory read (configuration setting, overwrite parameters, and OTP setting) by the flash sequencer. 0: Does not generate the “FLERR” interrupt request when ECRCT = 1. 1: Generates the “FLERR” interrupt request when ECRCT = 1.

4.4 Code Flash Memory Area Select Register (FAREASELC)

FAREASELC selects the code flash memory area as the target for handling of commands by the FACI.

When the SUNIT bit in the FSUINTR register is set to 1, FAREASELC is initialized. This register is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0020_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	CFAS	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R/W*2,3	R

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is "1". Writing to this bit while the FRDY bit is "0" is ignored.

Note 3. Writing to this bit is enabled only when 3B_H is written to the KEY[7:0] bits.

Table 4.4 FAREASELC Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable CFAS bit modification.
7 to 2	Reserved	When read, the value after reset is read. When writing, write the value after reset.
1	CFAS	Code Flash Memory Area Select Selects the area of code flash memory that is to be the target for handling of commands by the FACI. 0: User area is selected 1: Extended user area is selected.
0	Reserved	When read, the value after reset is read. When writing, write the value after reset.

4.5 FACI Command Start Address Register (FSADDR)

FSADDR specifies the start address of the target area for command processing when the FACI command “Program”, “DMA Program”, “Block Erase”, “Blank Check”, “Config Program”, “Lock Bit Program”, “Lock Bit Read”, or “OTP Set” is issued.

FSADDR value is initialized when SUNIT bit in FSUNITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 32-bit units.

Address: FFA1 0030_H

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FSADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FSADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R	R

Note 1. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits “0” is ignored.

Table 4.5 FSADDR Register Contents

Bit Position	Bit Name	Function																								
31 to 0	FSADDR[31:0]	<p>Start Address of FACI Command Processing</p> <p>These bits specify the start address of the FACI command processing. Bits 31 to 24 are ignored in the FACI command processing for the code flash memory. Bits 31 to 19 are ignored in the FACI command processing for the data flash memory. Lower address bits for smaller address than boundary below are also ignored. Bits 24 to 4 are used to generate the address parity.</p> <table border="0"> <thead> <tr> <th style="text-align: left;"><u>Command</u></th> <th style="text-align: left;"><u>Address Boundary</u></th> </tr> </thead> <tbody> <tr> <td>Program (code flash memory):</td> <td>256 bytes</td> </tr> <tr> <td>Program (data flash memory):</td> <td></td> </tr> <tr> <td> 4-byte write:</td> <td>4 bytes</td> </tr> <tr> <td>DMA Program:</td> <td>4 bytes</td> </tr> <tr> <td>Block Erase (code flash memory):</td> <td>8 Kbytes or 32 Kbytes</td> </tr> <tr> <td>Block Erase (data flash memory):</td> <td>64 bytes</td> </tr> <tr> <td>Blank Check:</td> <td>4 bytes</td> </tr> <tr> <td>Config Program:</td> <td>16 bytes</td> </tr> <tr> <td>Lock Bit Program:</td> <td>8 Kbytes or 32 Kbytes</td> </tr> <tr> <td>Lock Bit Read:</td> <td>8 Kbytes or 32 Kbytes</td> </tr> <tr> <td>OTP Set:</td> <td>16 bytes</td> </tr> </tbody> </table>	<u>Command</u>	<u>Address Boundary</u>	Program (code flash memory):	256 bytes	Program (data flash memory):		4-byte write:	4 bytes	DMA Program:	4 bytes	Block Erase (code flash memory):	8 Kbytes or 32 Kbytes	Block Erase (data flash memory):	64 bytes	Blank Check:	4 bytes	Config Program:	16 bytes	Lock Bit Program:	8 Kbytes or 32 Kbytes	Lock Bit Read:	8 Kbytes or 32 Kbytes	OTP Set:	16 bytes
<u>Command</u>	<u>Address Boundary</u>																									
Program (code flash memory):	256 bytes																									
Program (data flash memory):																										
4-byte write:	4 bytes																									
DMA Program:	4 bytes																									
Block Erase (code flash memory):	8 Kbytes or 32 Kbytes																									
Block Erase (data flash memory):	64 bytes																									
Blank Check:	4 bytes																									
Config Program:	16 bytes																									
Lock Bit Program:	8 Kbytes or 32 Kbytes																									
Lock Bit Read:	8 Kbytes or 32 Kbytes																									
OTP Set:	16 bytes																									

4.6 FACI Command End Address Register (FEADDR)

This register specifies the end address in the target area in Blank Check command processing. When blank check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = "0"), address specified in FSADDR should be equal to or smaller than address in FEADDR. Conversely, address in FSADDR should be equal to or larger than address in FEADDR when blank check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = "1"). If setting of BCDIR, FSADDR, and FEADDR are inconsistent, FACI detects error and flash sequencer enters "Command Lock" state. (See Section 8.3, Error Protection.)

FEADDR value is initialized when SUNIT bit in FSUINTR is set to "1". It is also initialized by a reset.

Access: This register can be read/written in 32-bit units.

Address: FFA1 0034_H

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FEADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FEADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R	R

Note 1. This bit can be written when the FRDY bit in the FSTATR register is "1". Writing to this bit while the FRDY bits is "0" is ignored.

Table 4.6 FEADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	FEADDR[31:0]	End Address of FACI Command Target Area Specifies end address of target area in "Blank Check" command. Bits 31 to 19, 1 and 0 are ignored in the command processing.

4.7 Flash Status Register (FSTATR)

FSTATR indicates flash sequencer status.

Access: This register can only be read in 8-, 16-, or 32-bit units.

Address: FFA1 0080_H

Value after reset: 0000 8000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	EBFULL	OTPDCT	OTPCRCT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRDY	ILGLER	ERSER	PRGER	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEE	CFGDT	CFGCR	TBLDT	TBLCR	—	—
Value after reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.7 FSTATR Register Contents (1/5)

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is read.
18	EBFULL	<p>ECC Buffer Full</p> <p>Indicates the ECC buffer status when issuing “Program”. The FACL incorporates a buffer for ECC bit (ECC buffer). While the ECCDISE bit in FECCTMD is 1, FDMYECC can be used as the ECC buffer. When FDMYECC is written to while the EBFULL bit is 1, the FACL inserts a wait in the P-Bus.</p> <p>0: The ECC buffer is empty. 1: The ECC buffer is full.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> The ECC buffer becomes full while issuing “Program” command. <p>[Clearing condition]</p> <ul style="list-style-type: none"> The ECC buffer becomes empty.
17	OTPDCT	<p>2-Bit Error Detection Monitor (OTP Set)</p> <p>Indicates that a 2-bit error has been detected on reading the OTP value. The FACL reads the OTP value in “Program”, “Block Erase”, “Lock Bit Program”, “Lock Bit Read”, and “OTP Set” for the code flash memory. When this bit is 1, the flash sequencer is in “Command Lock” state.</p> <p>0: No 2-bit error has been detected. 1: A 2-bit error has been detected.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
16	OTPCRCT	<p>1-Bit Error Correction Monitor (OTP Set)</p> <p>Indicates that a 1-bit error has been corrected on reading the OTP value. The FACL reads the OTP value in “Program”, “Block Erase”, “Lock Bit Program”, “Lock Bit Read”, and “OTP Set” for the code flash memory. When this bit is 1, the flash sequencer continues the command processing and does not enter “Command Lock” state.</p> <p>0: 1-bit error has not been corrected. 1: 1-bit error has been corrected.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> The flash sequencer starts “Status Clear” or “Forced Stop” command processing.

Table 4.7 FSTATR Register Contents (2/5)

Bit Position	Bit Name	Function
15	FRDY	<p>Flash Ready</p> <p>Indicates the processing state in flash sequencer.</p> <p>0: Processing of the command “Program”, “DMA Program”, “Block Erase”, “Program/Erase Suspend”, “Program/Erase Resume”, “Forced Stop”, “Blank Check”, “Config Program”, “Lock Bit Program”, “Lock Bit Read”, or “OTP Set” is in progress.</p> <p>1: None of the above is in progress.</p> <p>[Setting Conditions]</p> <ul style="list-style-type: none"> Flash sequencer completes processing. Flash sequencer suspends processing by “Program/Erase Suspend” command. Flash sequencer terminates processing by “Forced Stop” command. <p>[Clearing Conditions]</p> <ul style="list-style-type: none"> When the flash sequencer accepts the FACL command <ul style="list-style-type: none"> For “Program”, “DMA Program”, “Config Program”, or “OTP Set” command, after the first write access to the FACL command issuing area. For other commands, after the last write access to the FACL command issuing area.
14	ILGLERR	<p>Illegal Command Error</p> <p>Indicates that flash sequencer has detected an illegal command or illegal flash memory access. When this bit is “1”, flash sequencer is in “Command Lock” state.</p> <p>0: Flash sequencer has not detected any illegal command or illegal flash memory access.</p> <p>1: Flash sequencer has detected an illegal command or illegal flash memory access</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> Flash sequencer has detected an illegal command. Flash sequencer has detected an illegal flash memory access. FENTRYR setting is illegal. <p>[Clearing condition]</p> <ul style="list-style-type: none"> “Status Clear” or “Forced Stop” command processing is started while the DFAE or CFAE bits in the FASTAT register is 0. <p>If the flash sequencer completes processing of “Status Clear” or “Forced Stop” command while the CFAE or DFAE bit in the FASTAT register is 1, this bit is set to 1. This bit is temporarily set to 0 during processing of “Forced Stop” command, and is re-set to 1 when the CFAE or DFAE bit is detected as 1 on completion of command processing.</p>
13	ERSERR	<p>Erase Error</p> <p>Indicates result of code or data flash erasure by flash sequencer. When this bit is “1”, flash sequencer is in “Command Lock” state.</p> <p>0: Erasure processing has been completed successfully</p> <p>1: An error has occurred during erasure</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> An error has occurred during erasure. “Erase” command has been issued for the area protected by lock bit. <p>[Clearing condition]</p> <ul style="list-style-type: none"> “Status Clear” or “Forced Stop” command processing is started.

Table 4.7 FSTATR Register Contents (3/5)

Bit Position	Bit Name	Function
12	PRGERR	<p>Programming Error</p> <p>Indicates the result of code or data flash programming by flash sequencer. When this bit is "1", flash sequencer is in "Command Lock" state.</p> <p>0: Programming has been completed successfully 1: An error has occurred during programming</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> An error has occurred during programming. "Program" or "Lock Bit Program" command has been issued for the area protected by lock bit. <p>[Clearing condition]</p> <ul style="list-style-type: none"> "Status Clear" or "Forced Stop" command processing is started.
11	SUSRDY	<p>Suspend Ready</p> <p>Indicates whether flash sequencer is ready to accept a "Program/Erase Suspend" command.</p> <p>0: Flash sequencer cannot accept "Program/Erase Suspend" command. 1: Flash sequencer can accept "Program/Erase Suspend" command.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> After initiating programming or erasure, FACL entered a state where it is ready to accept "Program/Erase Suspend" command. <p>[Clearing conditions]</p> <ul style="list-style-type: none"> FACL has accepted "Program/Erase Suspend" or "Forced Stop" command. (after the write access to the FACL command issuing area is completed) Flash sequencer has entered "Command Lock" state during programming or erasure. Programming/erasure processing is completed.
10	DBFULL	<p>Data Buffer Full</p> <p>Indicates the data buffer status when issuing "Program". The FACL incorporates a buffer for write data (data buffer). When issuing the flash memory write data to the FACL command issue area while the data buffer is full, the FACL inserts a wait in the P-Bus.</p> <p>0: The data buffer is empty. 1: The data buffer is full.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> The data buffer becomes full while issuing "Program". <p>[Clearing condition]</p> <ul style="list-style-type: none"> The data buffer becomes empty.
9	ERSSPD	<p>Erase-Suspended Status</p> <p>Indicates that flash sequencer has entered "Erase" command suspension process or erasure-suspended status.</p> <p>0: Flash sequencer is in status other than the below mentioned. 1: Flash sequencer is in erasure suspension process or erasure-suspended status.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> Flash sequencer has initiated "Program/Erase Suspend" command during "Erase" command processing. <p>[Clearing conditions]</p> <ul style="list-style-type: none"> Flash sequencer has accepted "Program/Erase Resume" command. (after the write access to the FACL command issuing area is completed) "Forced Stop" command processing is started.

Table 4.7 FSTATR Register Contents (4/5)

Bit Position	Bit Name	Function
8	PRGSPD	<p>Programming-Suspended Status Indicates that flash sequencer has entered “Program” command suspension process or programming suspended status.</p> <p>0: Flash sequencer is in status other than the below mentioned. 1: Flash sequencer is in programming suspension process or programming-suspended status.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> Flash sequencer has initiated “Program/Erase Suspend” command during “Program” command processing. <p>[Clearing condition]</p> <ul style="list-style-type: none"> Flash sequencer has accepted “Program/Erase Resume” command. (after the write access to the FACL command issuing area is completed) “Forced Stop” command processing is started.
7	Reserved	When read, the value after reset is read.
6	FLWEERR	<p>Flash write erase protect error Indicates a violation of the flash memory overwrite protection due to FHVE3 register. When the FLWEERR bit is set to 1, the flash sequencer enters the “Command Lock” state.</p> <p>0: No error has occurred 1: An error has occurred</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> The flash sequencer starts processing of a “Forced Stop” command.
5	CFGDTCT	<p>2-Bit Error Detection Monitor (Config Program) Indicates that a 2-bit error has been detected on reading the Config Program value. The FACL reads the Config Program value in “Config Program”. When this bit is 1, the flash sequencer is in “Command Lock” state.</p> <p>0: No 2-bit error has been detected. 1: A 2-bit error has been detected.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
4	CFGCRCT	<p>1-Bit Error Correction Monitor (Config Program) Indicates that a 1-bit error has been corrected on reading the Config Program value. The FACL reads the Config Program value in “Config Program”. When this bit is 1, the flash sequencer continues command processing and does not enter “Command Lock” state.</p> <p>0: 1-bit error has not been corrected. 1: 1-bit error has been corrected.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
3	TBLDTCT	<p>2-Bit Error Detection Monitor (Overwrite Parameter Table) Indicates that a 2-bit error has been detected on reading the overwrite parameter table. The FACL reads the overwrite parameter table in “Program”, “DMA Program”, “Block Erase”, “Block Check”, “Config Program”, “Lock Bit Program”, and “OTP Set” for the flash memory. When this bit is 1, the flash sequencer is in “Command Lock” state.</p> <p>0: No 2-bit error has been detected. 1: A 2-bit error has been detected.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> The flash sequencer starts “Status Clear” or “Forced Stop” command processing.

Table 4.7 FSTATR Register Contents (5/5)

Bit Position	Bit Name	Function
2	TBLCRCT	<p>1-Bit Error Correction Monitor (Overwrite Parameter Table)</p> <p>Indicates that a 1-bit error has been corrected on reading the overwrite parameter table. The FACI reads the overwrite parameter table in "Program", "DMA Program", "Block Erase", "Block Check", "Config Program", "Lock Bit Program", and "OTP Set" for the flash memory. When this bit is 1, the flash sequencer does not enter "Command Lock" state.</p> <p>0: 1-bit error has not been corrected. 1: 1-bit error has been corrected.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> The flash sequencer starts "Status Clear" or "Forced Stop" command processing.
1, 0	Reserved	When read, the value after reset is read.

4.8 Flash P/E Mode Entry Register (FENTRYR)

FENTRYR specifies “Program/Erasure Mode” for code flash or data flash. To specify “Program/Erasure Mode” for code flash or data flash so that flash sequencer can accept FACY commands, set either of FENTRYD or FENTRYC bit to “1”.

Note that if this register is set to other than 0000_H, 0001_H and 0080_H, ILGLERR bit in the FSTATR register will be set and flash sequencer will enter “Command Lock” state.

FENTRY value is initialized when SUNIT bit in FSUNITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0084_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								FENTR YD	—	—	—	—	—	—	FENTR YC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*2,3}	R	R	R	R	R	R/W ^{*2,3,*4}

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Note 3. Writing to this bit is enabled only when AA_H is written to the KEY[7:0] bits.

Note 4. Writing to this bit is enabled only when the FEW bit in the FPMON register is “1”.

Table 4.8 FENTRYR Register Contents (1/2)

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FENTRYD and FENTRYC bits modification.
7	FENTRYD	Data Flash Program/Erasure Mode Entry This bit specifies the Program/Erasure mode for data flash. 0: Data flash is in “Read Mode” 1: Data flash is in “Program/Erasure Mode” [Setting condition] <ul style="list-style-type: none"> “1” is written to FENTRYD while write enabling conditions are satisfied and FENTRYR is 0000_H. [Clearing conditions] <ul style="list-style-type: none"> A value other than AA_H is written to KEY[7:0] in FENTRYR while FRDY bit is “1”. “0” is written to FENTRYD while the write enabling conditions are satisfied. FENTRYR is written to while FENTRYR is not 0000_H and the write enabling conditions are satisfied.
6 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.

Table 4.8 FENTRYR Register Contents (2/2)

Bit Position	Bit Name	Function
0	FENTRYC	<p>Code Flash Program/Erase Mode Entry</p> <p>This bit specifies the Program/Erase mode for data flash.</p> <p>0: Code flash is in "Read Mode"</p> <p>1: Code flash is in "Program/Erase Mode"</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> "1" is written to FENTRYC while write enabling conditions are satisfied and FENTRYR is 0000_H. <p>[Clearing conditions]</p> <ul style="list-style-type: none"> A value other than AA_H is written to KEY[7:0] in FENTRYR while FRDY bit is "1". The FWE bit in FPMON is set to "0" while the FRDY bit is "1". "0" is written to FENTRYC while the write enabling conditions are satisfied. FENTRYR is written to while FENTRYR is not 0000_H and the write enabling conditions are satisfied.

4.9 Code Flash Protect Register (FPROTR)

FPROTR enables or disables protection function through lock bits against programming and erasure. FPROTR value is initialized when SUNIT bit in FSUINTR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0088_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	FPROTCN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R	R	R	R	R	R	R	R/W ^{*2}

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. Writing to this bit is enabled only when 55_H is written to the KEY[7:0] bits.

Table 4.9 FPROTR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FPROTCN bit modification.
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	FPROTCN	Lock Bit Protect Cancel Enables or disables protection through lock bits against programming and erasure. 0: Enables protection through lock bits 1: Disables protection through lock bits [Setting condition] <ul style="list-style-type: none"> “1” is written to FPROTCN while write enabling conditions are satisfied and FENTRYR is not 0000_H. [Clearing conditions] <ul style="list-style-type: none"> A value other than 55_H is written to KEY[7:0] in FPROTR. “0” is written to FPROTCN while the write enabling conditions are satisfied. FENTRYR register value is 0000_H.

4.10 Flash Sequencer Set-Up Initialize Register (FSUINTR)

FSUINTR register is used for initialization of flash sequencer set-up.

Access: This register can be read/written in 16-bit units.

Address: FFA1 008C_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R	R	R	R	R	R	R	R/W ^{*2,3}

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is "1". Writing to this bit while the FRDY bits is "0" is ignored.

Note 3. Writing to this bit is enabled only when 2DH is written to the KEY[7:0] bits.

Table 4.10 FSUINTR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable SUINIT bit modification.
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	SUINIT	Set-up Initialization Initializes the flash sequencer set-up registers (FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, FBCCNT, and FAREASELC). 0: The above flash sequencer set-up registers retain their current values. 1: The above flash sequencer set-up registers are initialized.

4.11 Lock Bit Status Register (FLKSTAT)

FLKSTAT indicates lock bit status which is read through “Lock Bit Read” command execution.

Access: This register can only be read in 8-bit units.

Address: FFA1 0090_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FLOCKST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.11 FLKSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read.
0	FLOCKST	Lock Bit Status Reflects the lock bit status read through “Lock Bit Read” command execution. When FRDY bit becomes “1” after “Lock Bit Read” command is issued, effective data for FLOCKST bit is stored. This bit value is retained until next “Lock Bit Read” command is completed. 0: Protected state 1: Non-protected state

4.12 FACI Reset Transfer Status Register (FRTSTAT)

FRTSTAT indicates error status for the FACI reset transfer.

Access: This register can only be read in 8-bit units.

Address: FFA1 0098_H

Value after reset: 0X_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RTEDTCT	RTECRCT
Value after reset	0	0	0	0	0	0	0/1	0/1
R/W	R	R	R	R	R	R	R	R

Table 4.12 FRTSTAT Register Contents

Bit Position	Bit Name	Function
7 to 2	Reserved	When read, the value after reset is read.
1	RTEDTCT	<p>FACI reset transfer error detection</p> <p>Indicates that a 2-bit error has been detected during the FACI reset transfer. When RTEDTCT is "1", the flash sequencer does not enter the "Command Lock" state.</p> <p>0: No 2-bit error has been detected. 1: A 2-bit error has been detected.</p> <p>The RTEDTCT bit is cleared when a 2-bit error is not detected during the FACI reset transfer after a reset of the microcomputer.</p>
0	RTECRCT	<p>FACI reset transfer error correction</p> <p>Indicates that a 1-bit error has been corrected during the FACI reset transfer. When RTECRCT is "1", the flash sequencer does not enter the "Command Lock" state.</p> <p>0: No 1-bit error has been corrected. 1: A 1-bit error has been corrected.</p> <p>The RTECRCT bit is cleared when a 1-bit error is not corrected during the FACI reset transfer after a reset of the microcomputer.</p>

4.13 FACI Reset Transfer Error Interrupt Enable Register (FRTEINT)

FRTEINT enables or disables generation of an interrupt request of the FACI reset transfer error (FRTERR).

FACI reset transfer error interrupt is handled as an error source of ECM with this product.

Access: This register can be read/written in 8-bit units.

Address: FFA1 009C_H

Value after reset: 03_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RTEDIE	RTECIE
Value after reset	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R/W	R/W

Table 4.13 FRTEINT Register Contents

Bit Position	Bit Name	Function
7 to 2	Reserved	When read, the value after reset is read. When writing, write the value after reset.
1	RTEDIE	FACI reset transfer error detection interrupt enable Enables or disables generation of an "FRTERR" interrupt when a 2-bit error is detected during the FACI reset transfer and the RTEDTCT bit in FRTSTAT is set to "1" 0: No FRTERR interrupt is generated when FRTSTAT.RTEDTCT = "1" 1: An FRTERR interrupt is generated when FRTSTAT.RTEDTCT = "1"
0	RTECIE	FACI reset transfer error correction interrupt enable Enables or disables generation of an "FRTERR" interrupt when a 1-bit error is corrected during the FACI reset transfer and the RTECRCT bit in FRTSTAT is set to "1" 0: No FRTERR interrupt is generated when FRTSTAT.RTECRCT = "1" 1: An FRTERR interrupt is generated when FRTSTAT.RTECRCT = "1"

4.14 FACI Command Register (FCMDR)

FCMDR stores commands that FACI has accepted.

Access: This register can only be read in 16-bit units.

Address: FFA1 00A0_H

Value after reset: FFFF_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMDR[7:0]								PCMDR[7:0]							
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.14 FCMDR Register Contents

Bit Position	Bit Name	Function
15 to 8	CMDR[7:0]	Command These bits store the latest command accepted by FACI.
7 to 0	PCMDR[7:0]	Previous Command These bits store previous command accepted by FACI.

Table 4.15 States of FCMDR after Acceptance of the Various Commands

Command	CMDR[7:0]	PCMDR[7:0]
Program	E8 _H	Previous command
DMA Program	EA _H	Previous command
Block Erase	D0 _H	20 _H
Program/Erase Suspend	B0 _H	Previous command
Program/Erase Resume	D0 _H	Previous command
Status Clear	50 _H	Previous command
Forced Stop	B3 _H	Previous command
Blank Check	D0 _H	71 _H
Config Program	40 _H	Previous command
Lock Bit Program	D0 _H	77 _H
Lock Bit Read	D0 _H	71 _H
OTP Set	45 _H	Previous command

4.15 Flash P/E Status Register (FPESTAT)

FPESTAT indicates the result of programming or erasure to the flash memory.

Access: This register can only be read in 16-bit units.

Address: FFA1 00C0_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PEERRST[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.16 FPESTAT Register Contents

Bit Position	Bit Name	Function
15 to 8	Reserved	When read, the value after reset is read.
7 to 0	PEERRST[7:0]	<p>Program/Erase Error Status</p> <p>Indicates the source of error that occurs during programming/erasure for code flash or data flash. The value of the PEERRST[7:0] bits is only valid if PRGERR or ERSERR bit value in FSTATR register is 1, while FRDY bit in FSTATR register is "1".</p> <p>When ERSERR and PRGERR are "0", the PEERRST[7:0] bits retain the value to indicate the source of error that previously occurred.</p> <p>00_H: No error</p> <p>01_H: A write error caused by an attempt to write to an area protected by the lock bits</p> <p>02_H: A write error caused by other source than the above</p> <p>11_H: An erase error caused by an attempt to erase an area protected by the lock bits</p> <p>12_H: An erase error caused by other source than the above</p> <p>Other than above: Reserved</p>

4.16 Data Flash Blank Check Control Register (FBCCNT)

FBCCNT specifies addressing mode in “Blank Check” command processing. FBCCNT value is initialized when SUNIT bit in FSUINTR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 8-bit units.

Address: FFA1 00D0_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCDIR
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 4.17 FBCCNT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	BCDIR	Blank Check Direction Specifies addressing mode in blank check operation. 0: Blank check is executed from smaller address to larger address. (Incremental mode) 1: Blank check is executed from larger address to smaller address. (Decremental mode)

4.17 Data Flash Blank Check Status Register (FBCSTAT)

FBCSTAT stores check results by executing “Blank Check” command.

Access: This register can only be read in 8-bit units.

Address: FFA1 00D4_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.18 FBCSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read.
0	BCST	Blank Check Status Indicates the result of “Blank Check” command. 0: The target area is erased (blank). 1: The target area is filled with 0s and/or 1s.

4.18 Data Flash Programming Start Address Register (FPSADDR)

FPSADDR indicates address of the first programmed data which is found in “Blank Check” command execution.

Access: This register can only be read in 32-bit units.

Address: FFA1 00D8_H

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[18:16]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PSADR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.19 FPSADDR Register Contents

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is read.
17 to 0	PSADR[18:0]	Programmed Area Start Address Indicates address of the first programmed data which is found in “Blank Check” command execution. These bits stores address offset from the top address in the data flash memory. The value of the PSADR[18:0] bits is only valid if BCST bit value in FBCSTAT register is 1, while FRDY bit in FSTATR register is “1”. When BCST bit is “0”, the PSADR[18:0] bits hold the address that previously checked.

4.19 Flash Sequencer Process Switch Register (FCPSR)

FCPSR selects a function to make the FCU suspend erasure. FCPSR value is initialized when SUNIT bit in FSUINTR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 00E0_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSP MD
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Table 4.20 FCPSR Register Contents

Bit Position	Bit Name	Function
15 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ESUSPMD	Erasure-Suspended Mode Selects erasure-suspended mode to be entered when “Program/Erase Suspend” command is issued while flash sequencer is erasing flash memory. ESUSPMD bit should be set before issuing “Block Erase” command. 0: Suspension-priority mode 1: Erasure-priority mode

4.20 Flash Sequencer Processing Clock Notify Register (FPCKAR)

FPCKAR specifies the operating frequency of the flash sequencer while processing an FACL command. Value after reset is set as the highest operating frequency for this product.

Access: This register can be read/written in 16-bit units.

Address: FFA1 00E4_H

Value after reset: 0028_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								PCKA[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*2,*3}	R/W ^{*2,*3}	R/W ^{*2,*3}	R/W ^{*2,*3}	R/W ^{*2,*3}	R/W ^{*2,*3}	R/W ^{*2,*3}	R/W ^{*2,*3}

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is "1". Writing to this bit while the FRDY bits is "0" is ignored.

Note 3. Writing to this bit is enabled only when 1E_H is written to the KEY[7:0] bits.

Table 4.21 FPCKAR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable the PCKA[7:0] bit modification.
7 to 0	PCKA[7:0]	Flash Sequencer Operating Clock Notify Specifies the operating frequency of the flash sequencer while processing an FACL command. Set the desired frequency in these bits before issuing an FACL command. Specifically, convert the frequency represented in MHz into a binary number and set it in these bits. Example: Frequency is 35.9 MHz (PCKA[7:0] = 24 _H) Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number. If the value set in these bits is smaller than the operating frequency of the flash sequencer, the flash memory overwrite characteristics cannot be guaranteed. If the value set in these bits is greater than the operating frequency of the flash sequencer, the flash memory overwrite characteristics can be guaranteed with the increased FACL command processing time such as overwrite time. (The minimum FACL command processing time is available when the operating frequency of the flash sequencer is the same as the PCKA[7:0] value.)

4.21 Flash Emulation Control Register (FLEMU)

FLEMU specifies error/timing emulation functions. The number of flash memory overwrite and data hold feature are not guaranteed for the chip that has been once used in the error emulation or timing emulation function.

Access: This register can be read/written in 8-bit units.

Address: FFA1 00F0_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	EMMODE	ERREMU	—	—	EMSQMD3	EMSQMD2	EMSQMD1	EMSQMD0
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R	R	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}

Note 1. Writing to this register is enabled only when 01H is written to the OCD_MODE. For details of OCD_MODE register, see the *RH850/P1M-E User's Manual: Emulation*.

Table 4.22 FLEMU Register Contents

Bit Position	Bit Name	Function
7	EMMODE	Emulation mode Specifies the emulation mode. In the emulation mode, error emulation function or timing emulation function can be used. 0: Normal mode 1: Emulation mode
6	ERREMU	Error emulation Specifies the error emulation function. When the error emulation function is set, an error is always generated after processing of the FACI command specified for emulation. When the error emulation function is not set, the FACI command specified for emulation is completed after maximum processing time is elapsed (timing emulation function). Occurrence or non-occurrence of an error depends on the actual processing result. 0: Error emulation function is disabled. (Timing emulation function is enabled). 1: Error emulation function is enabled.
5, 4	Reserved	When read, the value after reset is read. When writing, write the value after reset.
3 to 0	EMSQMD3 to EMSQMD0	FACI Command processing for emulation Specify the FACI commands for emulation. 0 _H : Program command for code flash memory 1 _H : Block erase command for code flash memory 2 _H : Program command for data flash memory 3 _H : Block erase command for data flash memory 4 _H : Blank check command 5 _H : DMA program command

4.22 Flash Emulation Address Specify Register (FLEAD)

FLEAD specifies an address that generates an error during the error emulation function. FLEAD is used by the “DMA Program” and “Blank Check” commands. The number of flash memory overwrite and data hold feature are not guaranteed for the chip that has been once used in the error emulation or timing emulation function.

Access: This register can be read/written in 32-bit units.

Address: FFA1 00F4_H

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FLAPE[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAPE[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R	R

Note 1. This bit can be written in emulation mode.

Table 4.23 FLEAD Register Contents

Bit Position	Bit Name	Function
31 to 0	FLAPE[31:0]	Emulation address Specify an address that generates an error during error emulation of the “DMA Program” and “Blank Check” commands. The settings in the bits 31 to 19 are ignored.

4.23 Flash ECC Encoder Monitor Register (FECCEMON)

FECCEMON monitors the outputs from the address parity generator and ECC encoder.

Access: This register can only be read in 16-bit units.

Address: FFA1 0100_H

Value after reset: FFFF_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FAPAR M	FECCEM 08	FECCEM 07	FECCEM 06	FECCEM 05	FECCEM 04	FECCEM 03	FECCEM 02	FECCEM 01	FECCEM 00
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.24 FECCEMON Register Contents

Bit Position	Bit Name	Function
15 to 10	Reserved	When read, the value after reset is read.
9	FAPARM	Address Parity Monitor Indicates the output from the address parity generator. <ul style="list-style-type: none"> In code flash program/erasure mode This bit indicates the output from the address parity generator. In data flash program/erasure mode This bit is fixed to 1.
8 to 0	FECCEM08 to FECCEM00	ECC Monitor Indicates the ECC encoder output. <ul style="list-style-type: none"> In code flash program/erasure mode The FECCEM08 to FECCEM00 bits indicate the ECC encoder output for the code flash memory. In data flash program/erasure mode The FECCEM08 and FECCEM07 bits are fixed to 1. The FECCEM06 to FECCEM00 bits indicate the ECC encoder output for the data flash memory.

4.24 Flash ECC Test Mode Register (FECCTMD)

FECCTMD sets the ECC test function for the flash memory.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0104_H

Value after reset: 0030_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	CECCV E	DECCV E	—	—	—	ECCDIS E
Value after reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R/W ^{*1}	R	R	R/W ^{*2}	R/W ^{*2}	R	R	R	R/W ^{*2}

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. Writing to this bit is enabled only when A6_H is written to the KEY[7:0] bits.

Table 4.25 FECCTMD Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable modification of the CECCVE, DECCVE, and ECCDISE bits.
7, 6	Reserved	When read, the value after reset is read. When writing, write the value after reset.
5	CECCVE	Code Flash Memory ECC Area Verify Enable Specifies the verify operation on overwriting the code flash memory. 0: Verifies the data area only. 1: Verifies the data area and the ECC area.
4	DECCVE	Data Flash Memory ECC Area Verify Enable Specifies the verify operation on overwriting the data flash memory. 0: Verifies the data area only. 1: Verifies the data area and the ECC area.
3 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECCDISE	ECC Encoder Disable Disables the address parity generator and the ECC encoder. If the address parity generator and the ECC encoder are disabled, the FDMYECC value is written to the flash memory. 0: The address parity generator and the ECC encoder are enabled. 1: The address parity generator and the ECC encoder are disabled.

4.25 Flash Dummy ECC Register (FDMYECC)

FDMYECC specifies the address parity and ECC value to be written into the flash memory when the ECCDISE bit in the FECCTMD register is 1. The bit functions in code flash program/erasure mode are different from those in data flash program/erasure mode as shown below.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0108_H

Value after reset: FFFF_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DMYAP AR	DMYECC[8:0]								
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4.26 FDMYECC Register Contents (in Code Flash Program/Erasure Mode)

Bit Position	Bit Name	Function
15 to 10	Reserved	When read, the value after reset is read. When writing, write the value after reset.
9	DMYAPAR	Dummy Address Parity Specifies the address parity value when the ECCDISE bit is 1.
8 to 0	DMYECC[8:0]	Dummy ECC Specify the ECC value when the ECCDISE bit is 1.

Table 4.27 FDMYECC Register Contents (in Data Flash Program/Erasure Mode)

Bit Position	Bit Name	Function
15 to 10	Reserved	When read, the value after reset is read. When writing, write the value after reset.
9	DMYAPAR	Reserved When read, the value after reset is read. When writing, write the value after reset.
8, 7	DMYECC[8:7]	Reserved When read, the value after reset is read. When writing, write the value after reset.
6 to 0	DMYECC[6:0]	Dummy ECC Specify the ECC value when the ECCDISE bit is 1.

4.26 BFA Selection Register (BFASLR)

BFASLR selects the Configuration setting area and OTP setting area.

Access: This register can be read/written in 8-bit units.

Address: FFC5 9008_H

Value after reset: *1

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BFAA
Value after reset	0	0	0	0	0	0	0	*1
R/W	R	R	R	R	R	R	R	R/W

Note 1. This bit is set to “1” when booted in serial programming mode, and cleared to “0” when booted in normal operating mode.

Table 4.28 BFASLR Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	BFAA	Area Selection*1 0: The Configuration setting area and OTP setting area cannot be read. 1: The Configuration setting area and OTP setting area can be read. When this bits “1”, 0000 0000 _H to 0100 7FFF _H are reserved.

Note 1. Set BFAA to switch the areas after all read accesses by any master to the area before switching have been completed.
While this bit is set to “1”, avoid access to 0000 0000_H – 0100 7FFF_H in response to interrupts by setting the vector address of the CPU exception handler in the on-chip RAM.

4.27 Self-Programming ID Input Registers (SELFID0 to SELFID3)

SELFID is for the input of an ID for use in authentication at the time of self-programming. The ID is authenticated by comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. The ID which is stored in a particular range of the flash memory can be set by “Config Program” command for the FACI.

Access: This register can be read/written in 32-bit units.

Address: FFA0 8000_H (SELFID0)
 FFA0 8004_H (SELFID1)
 FFA0 8008_H (SELFID2)
 FFA0 800C_H (SELFID3)

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SELFID _n [31:16] ^{*1}															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SELFID _n [15:0] ^{*1}															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note 1. n = 0 to 3

Table 4.29 SELFID0 to SELFID3 Register Contents

Bit Position	Bit Name	Function
31 to 0	SELFID _n [31:0]	<p>ID for Use in Authentication of Self-Programming</p> <p>The ID for use in authentication at the time of self-programming is input to these bits. Authentication of the ID is executed by comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID_n[31:0] bits.</p> <p>The 128-bit ID is arranged in the respective sets of SELFID_n[31:0] bits in the way listed below.</p> <p>ID[31:0]: SELFID0[31:0] ID[63:32]: SELFID1[31:0] ID[95:64]: SELFID2[31:0] ID[127:96]: SELFID3[31:0]</p>

4.28 Self-Programming ID Authentication Status Register (SELFIDST)

SELFIDST indicates the result of authentication of an ID at the time of self-programming. That is, the SELFIDST register indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. The ID which is stored in a particular range of the flash memory can be set by “Config Program” command for the FACI.

Access: This register can only be read in 8-, 16-, or 32-bit units.

Address: FFA0 8010_H

Value after reset: 0000 000X_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.30 SELFIDST Register Contents

Bit Position	Bit Name	Function
31 to 1	Reserved	When read, the value after reset is read.
0	IDST	<p>ID Authentication Status</p> <p>This bit indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers.</p> <p>0: The IDs match (ID-based security is unlocked).</p> <p>1: The IDs do not match (ID-based security is locked).</p>

Section 5 Flash Sequencer Modes

5.1 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in **Figure 5.1**. The mode is shifted by the write to the FENTRYR register.

When the FENTRYR register is 0000_H, the flash sequencer is in read mode. In this mode, it does not accept the FACI command. The code flash memory and the data flash memory are both readable.

When the FENTRYR register is 0001_H, the flash sequencer is in code flash program/erasure mode where the code flash memory can be programmed/erased by the FACI command. In this mode, the data flash memory is not readable. In addition, the code flash memory is not readable under the condition where the BGO operation is disabled. Under the condition where the BGO operation is enabled, the code flash memory is readable. As for the condition to enable the BGO operation, refer to the user's manual for this product.

When the FENTRYR register is 0080_H, the flash sequencer is in data flash program/erasure mode where the data flash memory can be programmed/erased by the FACI command. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

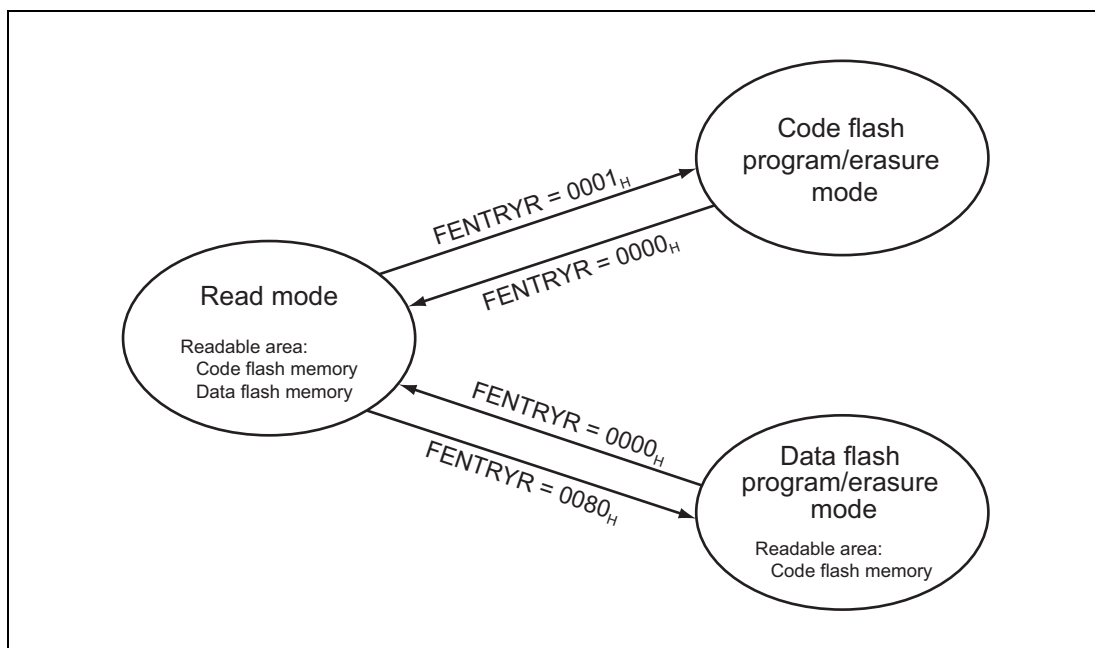


Figure 5.1 Flash Sequencer Modes

Section 6 FACL Command

6.1 List of FACL Commands

Table 6.1 List of FACL Commands

FACL Command	Function
Program	User area, extended user area, and data area can be programmed. The unit of programming is 256 bytes for user area and extended user area. The unit of programming is 4 bytes for data area.
DMA Program	Data area can be programmed by linkage with the DMA controller. The unit of programming is 4 to 64 Kbytes (specified in 4-byte units).
Block Erase	User area, extended user area, lock bit, and data area can be erased. The unit of erasing is one block.
Program/Erasure Suspend	"Program" or "Erasure" command operation can be suspended.
Program/Erasure Resume	Suspended "Program" or "Erasure" command operation can be resumed.
Status Clear	The OTPDTCT, OTPCRCT, ILGLERR, ERSERR, PRGERR, CFGDTCT, CFGCRCT, TBLDTCT, TBLCRCT bits of the FSTATR register are initialized and flash sequencer is released from "Command Lock" state.
Forced Stop	Any command operation can be stopped forcibly and FSTATR register is initialized.
Blank Check	Data area can be checked. The unit of blank checking is 4 to 64K bytes (4 bytes step).
Config Program	ID, security function, safety function, and option byte are set. The unit of programming is 16 bytes.
Lock Bit Program	The lock bit for user area and extended user area is programmed. The unit of programming is one bit (the lock bit for one block).
Lock Bit Read	The lock bit for user area and extended user area is read out and stored in the FLKSTAT register. The unit of reading is one bit (the lock bit for one block).
OTP (One Time Programming) Set	OTP is selected for the user area or extended user area. The unit of setting is 16 bytes (OTP settings for 128 blocks).

The FACI commands are issued by the write access to the FACI command issue area (see **Table 3.1**). When the write access as shown in **Table 6.2** is issued in the specified state, the flash sequencer executes the processing corresponding to each command (see **Section 6.2, Relationship between Flash Sequencer Status and FACI Commands**).

Table 6.2 Flash Sequencer Command Format

FACI Command	Number of write access	Write Data to "FACI Command Issue Area"			
		1st access	2nd access* ¹	3rd to (N+2)th access	(N+3)th access
Program (user area and extended user area) 256-byte programming: N = 128	131	E8 _H	80 _H (=N)	WD ₁ to WD ₁₂₈	D0 _H
Program (data area) 4-byte programming: N = 2	N+3	E8 _H	02 _H (=N)	WD ₁ to WD _N	D0 _H
DMA Program N = 2 to 32768 (even number only)	N+2	EA _H	N	WD ₁ to WD _N	—
Block Erase	2	20 _H	D0 _H	—	—
Program/Erase Suspend	1	B0 _H	—	—	—
Program/Erase Resume	1	D0 _H	—	—	—
Status Clear	1	50 _H	—	—	—
Forced Stop	1	B3 _H	—	—	—
Blank Check	2	71 _H	D0 _H	—	—
Config Program N = 8	11	40 _H	08 _H (=N)	WD ₁ to WD ₈	D0 _H
Lock Bit Program	2	77 _H	D0 _H	—	—
Lock Bit Read	2	71 _H	D0 _H	—	—
OTP Set N = 8	11	45 _H	08 _H (=N)	WD ₁ to WD ₈	D0 _H

Note: WD_N (N = 1, 2,...): Nth 16-bit data to be programmed.

Note 1. For a command other than the DMA program command, 8-bit data is written. For the DMA program command, 16-bit data is written.

The flash sequencer clears the FRDY bit of the FSTATR register to 0 when the processing for a command other than the status clear command is started, and sets the FRDY bit to 1 when the command processing finishes (see **Section 4.7, Flash Status Register (FSTATR)**).

If the FRDY bit changes from 0 to 1, a flash ready (FRDY) interrupt occurs.

6.2 Relationship between Flash Sequencer Status and FACI Commands

The FACI commands are accepted according to the mode/state of the flash sequencer. The FACI command should be issued after the shift of the flash sequencer to the code flash program/erasure mode or data flash program/erasure mode and checking that the flash sequencer has shifted to the mode. To check the state of flash sequencer, use the FSTATR and FASTAT registers. In addition, error occurrence can be checked by the CMDLK bit in the FASTAT register. It is the logical OR of the OTPDTC/ILGLERR/ERSERR/PRGERR/FLWEERR/CFGDTCT/TBLDTCT bits of the FSTATR register.

Table 6.3 summarizes available flash sequencer commands in each operating mode.

Table 6.3 Flash Sequencer Operation Mode and Available Commands

Operating Mode	FENTRYR	Available Command
Read mode	0000 _H	No command is available.
Code flash program/erasure mode	0001 _H	"Program" "Block Erase" "Program/Erasure Suspend" "Program/Erasure Resume" "Status Clear" "Forced Stop" "Lock Bit Program" "Lock Bit Read"
Data flash program/erasure mode	0080 _H	"Program" "DMA Program" "Block Erase" "Program/Erasure Suspend" "Program/Erasure Resume" "Status Clear" "Forced Stop" "Blank Check" "Config Program" "OTP Set"

Table 6.4 shows the flash sequencer state and the acceptable FACI commands. The table assumes appropriate flash sequencer operation mode is set before issuing the command.

Table 6.4 Flash Sequencer State and Acceptable FACI Commands

	“Program” or “Erasure” command processing	“Config Program” or “OTP Set” command processing	“Program” or “Erasure” command suspension	“Blank Check” or “Lock Bit Read” command processing	“DMA Program” command processing	While suspend “Program” command	While suspend “Erasure” command	While suspend “Erasure” command, and “Program” command processing	“Command Lock” state (FRDY = 1)	“Command Lock” state (FRDY = 0)	“Lock Bit Program” command processing	“Forced Stop” command processing	Other
FRDY bit	0	0	0	0	0	1	1	0	1	0	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	0	1	1	0/1	0/1	0	0	0
PRGSPD bit	0	0	0/1	0/1	0	1	0	0	0/1	0/1	0	0	0
CMDLK bit	0	0	0	0	0	0	0	0	1	1	0	0	0
Program	—	—	—	—	—	—	√ ^{*3}	—	—	—	—	—	√
DMA Program	—	—	—	—	—	—	√ ^{*1, *3}	—	—	—	—	—	√ ^{*1}
Block Erase	—	—	—	—	—	—	—	—	—	—	—	—	√
Program/Erasure Suspend	√	—	—	—	—	—	—	—	X	—	—	—	X
Program/Erasure Resume	—	—	—	—	—	√	√	—	—	—	—	—	—
Status Clear	—	—	—	—	—	√	√	—	√	—	—	—	√
Forced Stop	√	√	√	√	√	√	√	√	√	√	√	√	√
Blank Check	—	—	—	—	—	√ ^{*1}	√ ^{*1}	—	—	—	—	—	√ ^{*1}
Config Program	—	—	—	—	—	—	—	—	—	—	—	—	√ ^{*1}
Lock Bit Program	—	—	—	—	—	—	—	—	—	—	—	—	√ ^{*2}
Lock Bit Read	—	—	—	—	—	√ ^{*2}	√ ^{*2, *4}	—	—	—	—	—	√ ^{*2}
OTP Set	—	—	—	—	—	—	—	—	—	—	—	—	√ ^{*1}

√: Acceptable, —: Not acceptable (due to the “Command Lock” state), X: Ignored

- Note 1. Acceptable only in data flash program/erasure mode.
 Note 2. Acceptable only in code flash program/erasure mode.
 Note 3. Acceptable when programming area is other than erase suspending sector.
 Note 4. Undefined value is read out when lock bit read command is issued to erase suspending sector.

6.3 Use FACI Command

This section describes the overview of FACI command usage.

6.3.1 Overview of the Command Usage in Code Flash P/E Mode

The overview of the FACI command usage in code flash program/erasure mode is shown below. **Table 6.3** lists the available commands in code flash program/erasure mode. Note that security should be released by ID authentication before FACI commands are used for code flash memory.

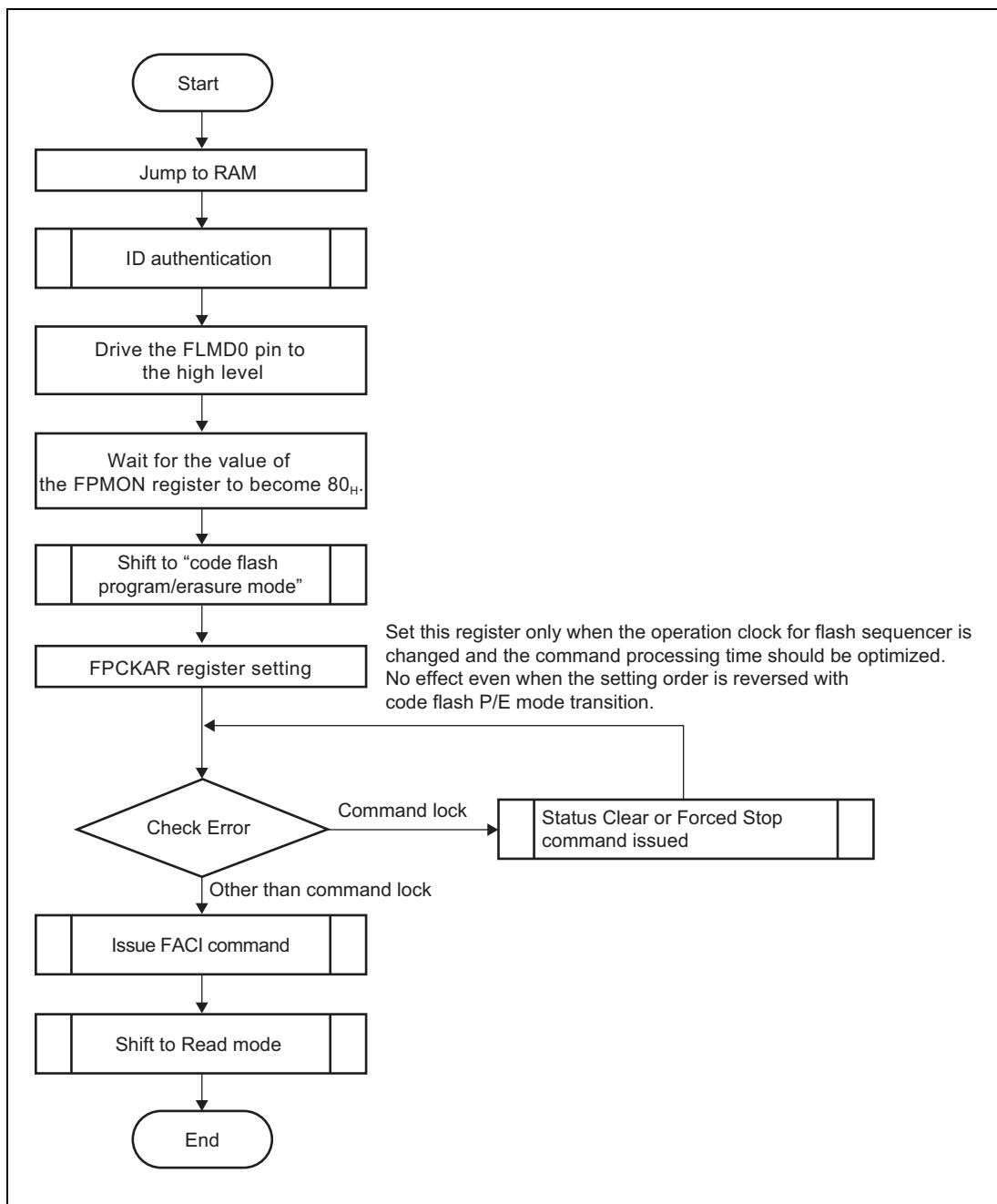


Figure 6.1 Overview of Command Usage in Code Flash Program/Erasure Mode

6.3.2 Overview of the Command Usage in Data Flash P/E Mode

The overview of the FACI command usage in data flash program/erasure mode is shown below. As for the available commands in data flash program/erasure mode, refer to **Table 6.3**.

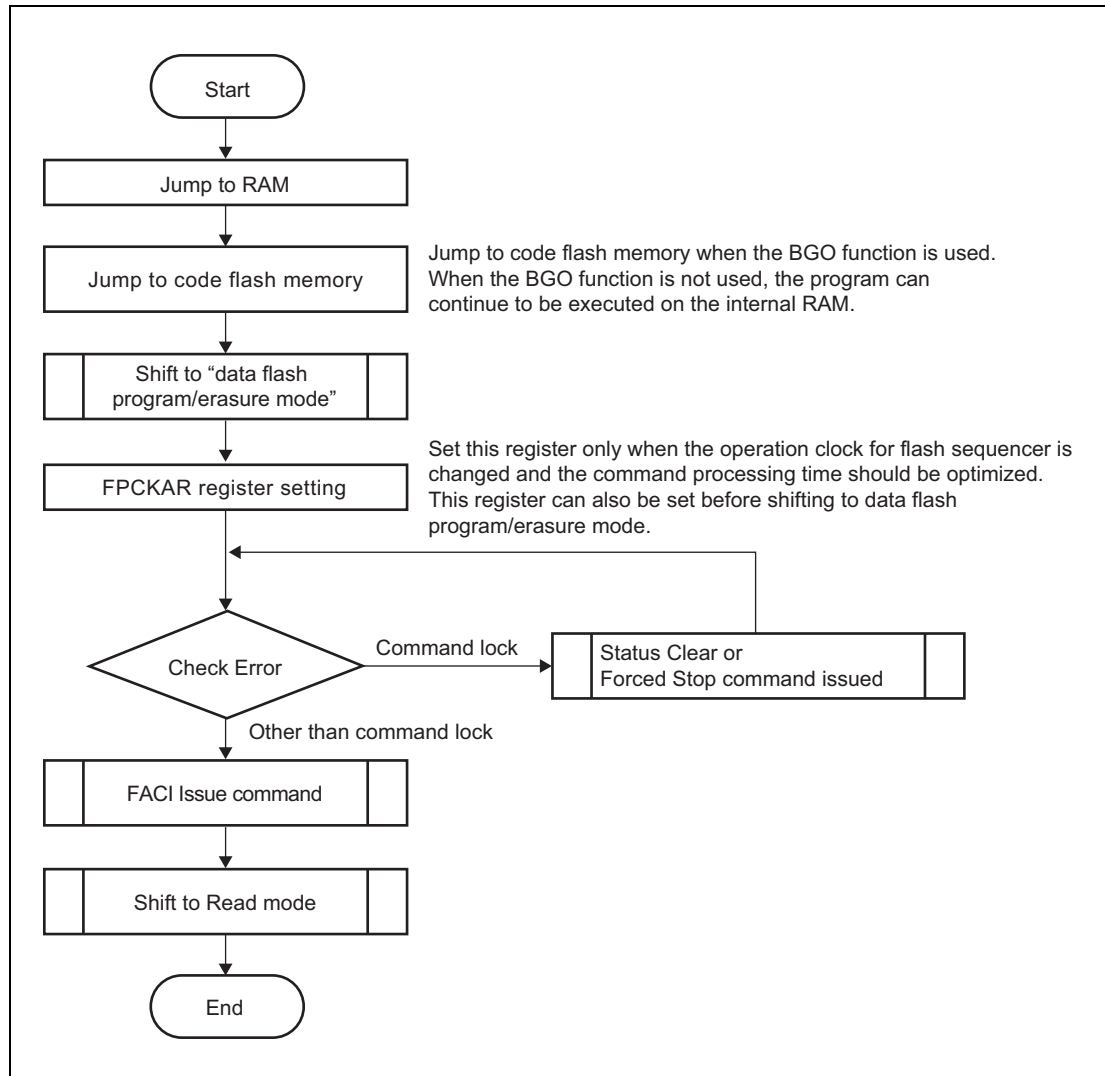


Figure 6.2 Overview of Command Usage in Code Flash Program/Erasure Mode

6.3.3 Shift to Code Flash Program/Erase Mode

To use the FACL commands relating the code flash memory, operation should be shifted to the code flash program/erase mode. Set the FENTRYRC bit in the FENTRYR to 1 to shift to the code flash program/erase mode.

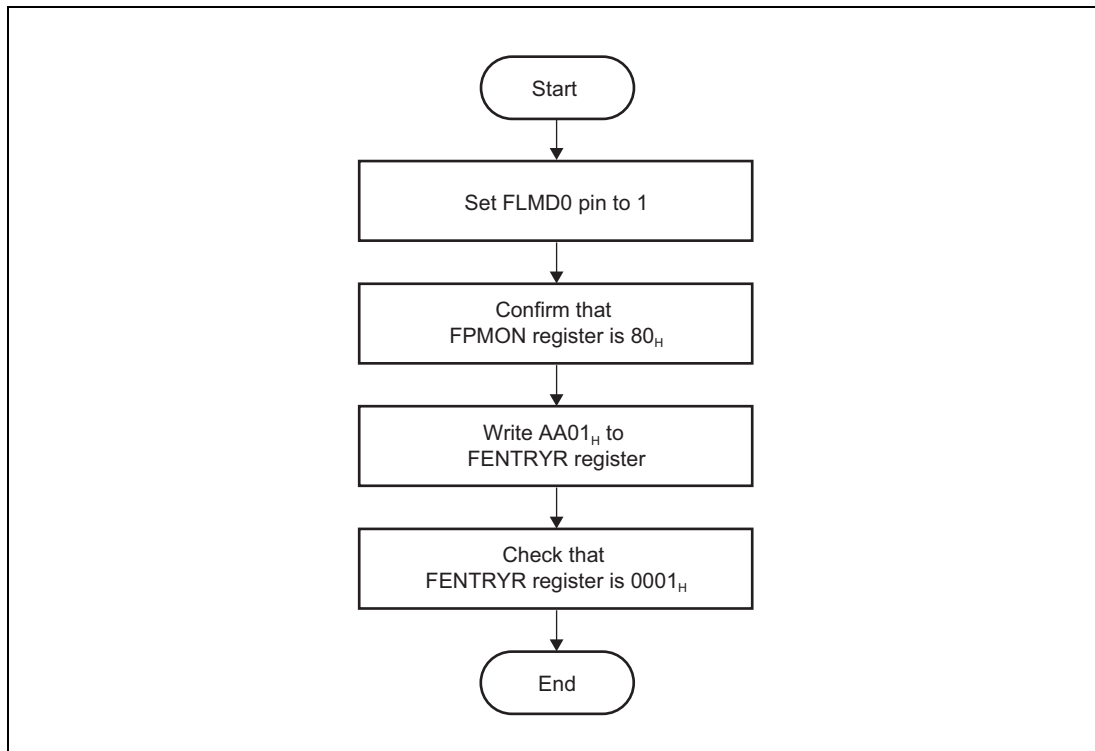


Figure 6.3 Flow of Shift to Code Flash Program/Erase Mode

6.3.4 Shift to Data Flash Program/Erase Mode

To use the FACL commands relating the data flash memory, operation should be shifted to the data flash program/erase mode. Set the FENTRYRD bit in the FENTRYR to 1 to shift to the data flash program/erase mode.

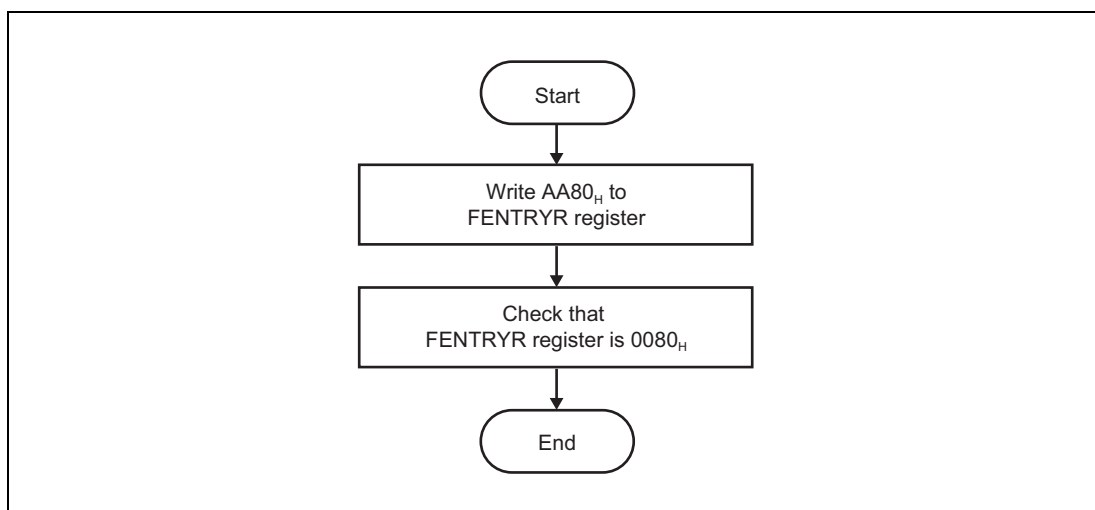


Figure 6.4 Flow of Shift to Data Flash Program/Erase Mode

6.3.5 Shift to Read Mode

To read the flash memory without using the BGO function, the operation should be shifted to the read mode. To shift to the read mode, set the FENTRYR register to 0000_H. When entering the read mode, the flash sequencer processing should be completed and the operation is in other than “Command Lock” state.

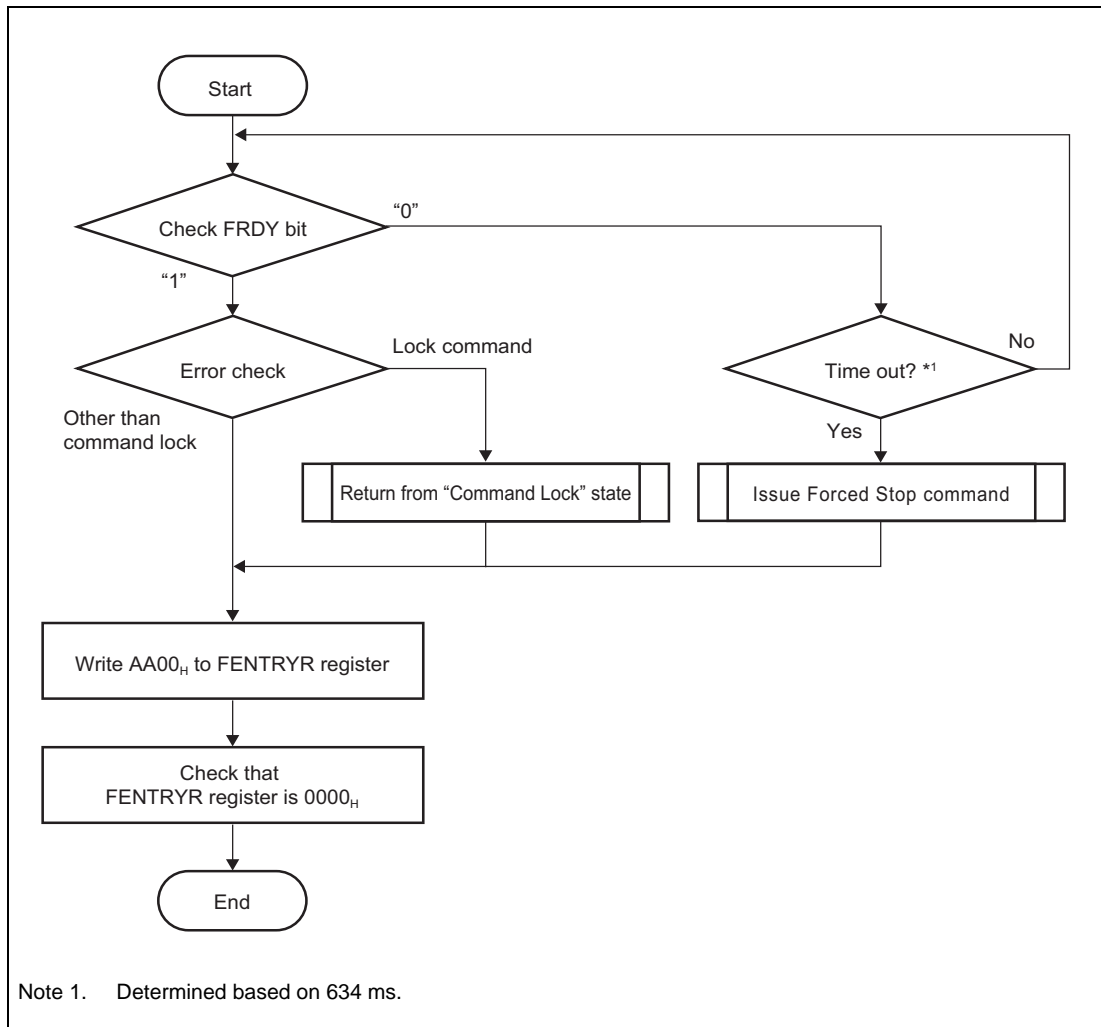


Figure 6.5 Flow of Shift to Read Mode

6.3.6 ID Authentication

To use the FACL command in code flash program/erasure mode, release security by ID authentication and the IDST bit of the SELFIDST register should be 0. When the IDST bit of the SELFIDST register is 1, the FACL command is not accepted. **Figure 6.6** shows the ID compare method using SELFID0 to SELFID3, and how the compare result is checked by SELFIDST.

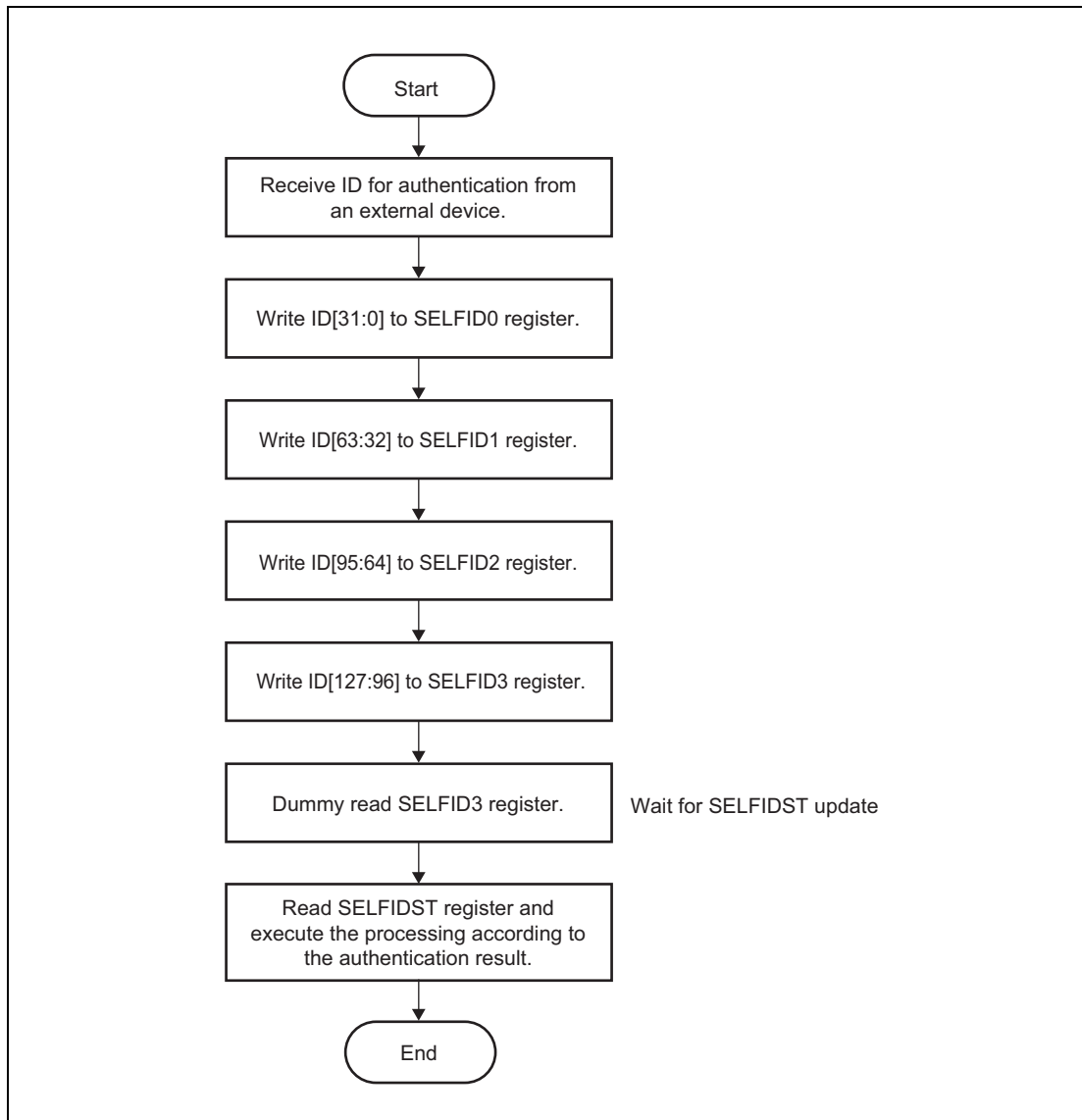


Figure 6.6 Flow of ID Compare

6.3.7 Return from Command Lock State

When the flash sequencer enters the “Command Lock” state, FACL commands cannot be accepted. To release the “Command Lock” state, use the status clear command, forced stop command, or FASTAT register.

When the “Command Lock” state is detected by checking an error before issuing the program/erase suspend command, the FRDY bit in the FSTATR register may hold 0 without completing the command processing. If the processing is not completed within the maximum program/erase time specified by electrical characteristics, it is determined as time out and the flash sequencer should be stopped by the forced stop command.

When the IGLERR bit in the FSTATR register is 1, check the FASTAT value. If the CFAE or DFAE bit in the FASTAT register is 1, the “Command Lock” state cannot be released by the status clear or forced stop command.

The FLWERR bit in the FSTATR register is not changed from 1 to 0 by the status clear command. When this bit is set to 1, use the forced stop command to release the “Command Lock” state. The other bits to be the command lock source can be changed from 1 to 0 by the status clear or forced stop command.

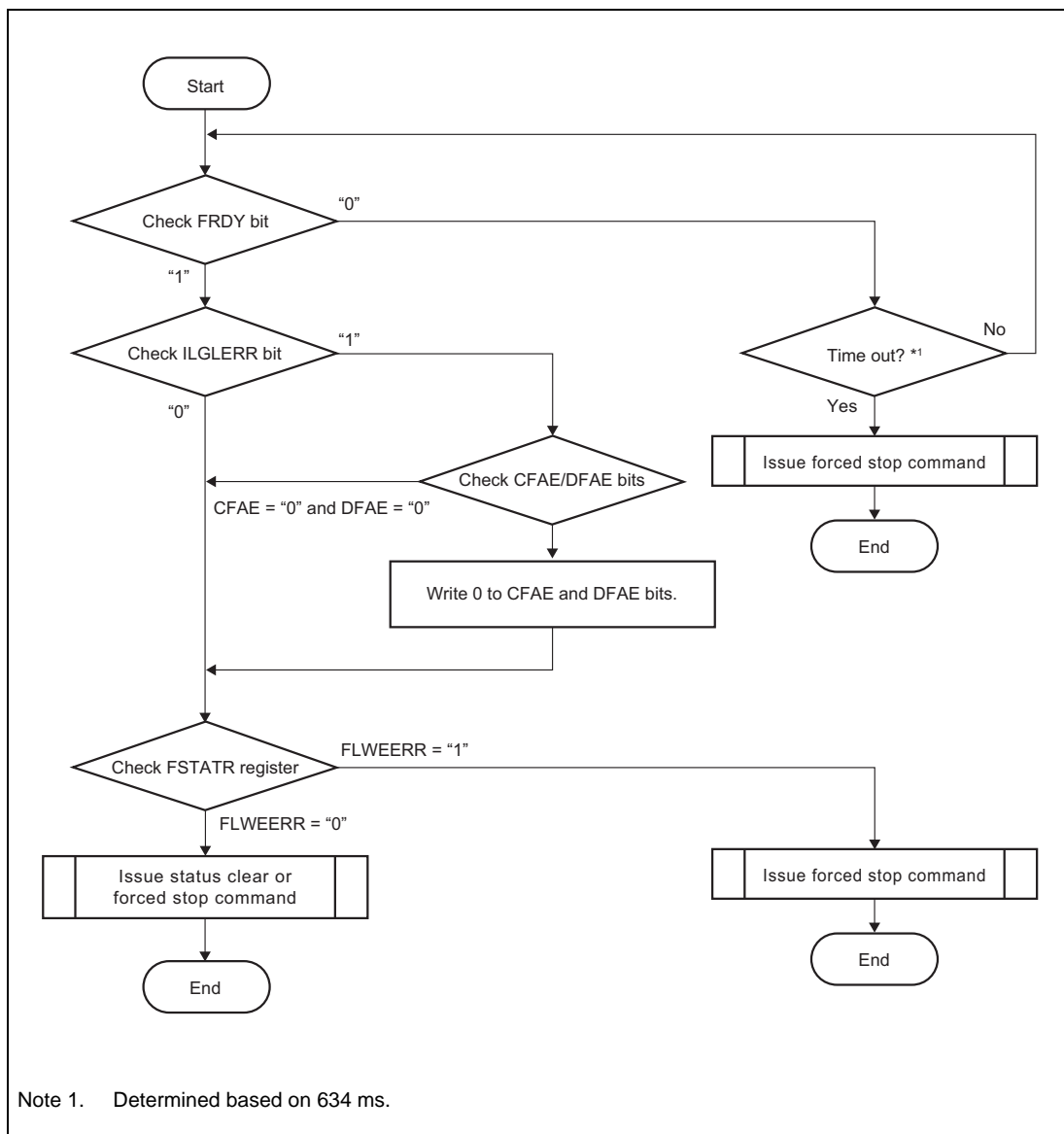


Figure 6.7 Return from Command Lock State

6.3.8 Program Command Issue

“Program” command is used to write to user area, extended user area, and data area.

Before issuing “Program” command, set the first address of target block to the FSADDR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the “Program” command processing. If the target area of program command processing contains the area not for writing, write $FFFF_H$ to the corresponding area.

Set the FPROTR and FAREASELC registers before issuing the “Program” command. To set the FPROTR register is required to switch enabling/disabling the lock bit. To set the FAREASELC register is required to switch to the area for overwriting the code flash memory.

If issuing the “Program” command is kept while the FACI internal data buffer is full, wait is generated in the P-Bus and it may affect the communication performance of other peripheral IPs. To avoid the wait generation, the DBFULL bit in FSTATR should be 0 when FACI commands are issued. In addition, writing to data area does not make the data buffer full.

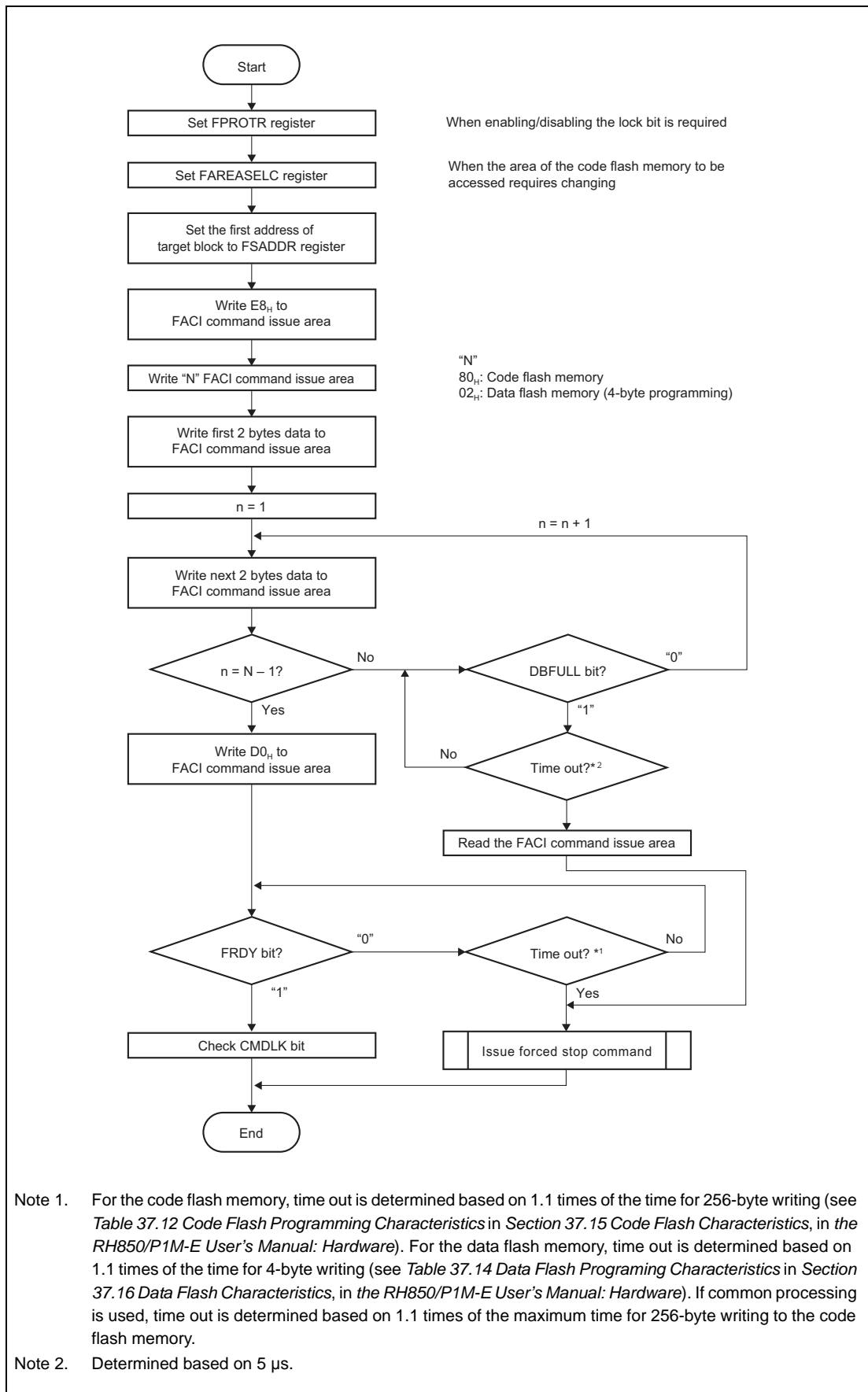


Figure 6.8 Program Command Usage

6.3.9 DMA Program Command

“DMA Program” command is used to write multiple 4-byte data sets (which is transferred from DMAC) to the data area, reducing CPU load caused by a large amount of serially written data.

Before issuing the “DMA Program” command, set the first address of the writing destination to the FSADDR register. Also, allocate the data in the RAM to be written, and set DMAC to enable DMA transfer from the relevant area to the FACI command issue area. FACI requests DMAC to transfer data immediately after the “DMA Program” command is received and each time 4-byte data writing finishes. Set DMAC to transfer 2-byte data twice for one data transfer request. For details about how to use DMAC, see the user’s manual for the relevant product.

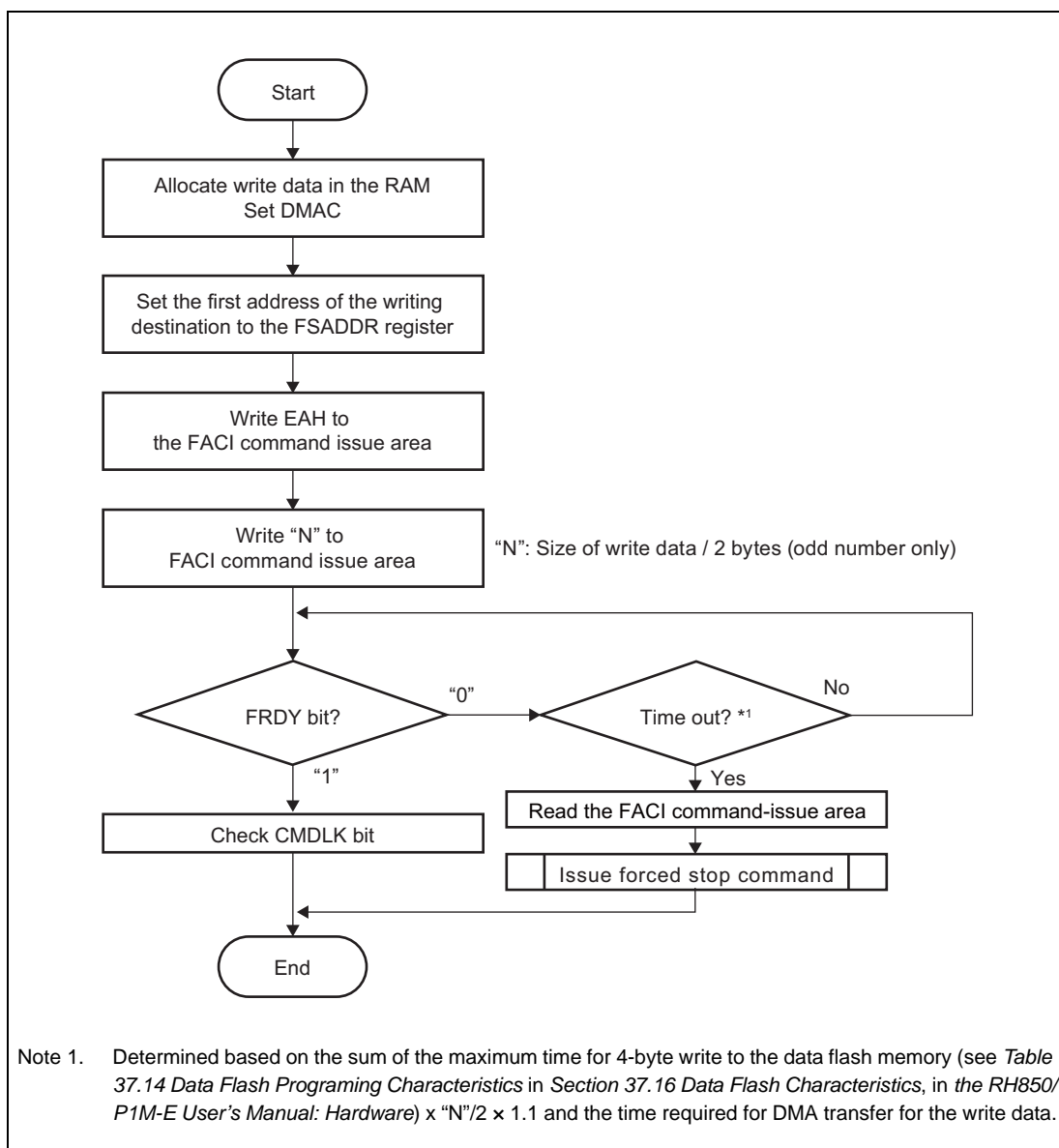


Figure 6.9 DMA Program Command Usage

6.3.10 Block Erase Command

“Block Erase” command is used to erase the user area, extended user area, lock bit, and data area.

Before issuing “Block Erase” command, set the first address of target block to the FSADDR register. Writing 20_H and D0_H to the FACL command issue area starts the “Block Erase” command processing.

Set the FPROTR, FAREASELC, and FCPSR registers before issuing the “Block Erase” command. To set the FPROTR register is required to switch enabling/disabling the lock bit. To erase the lock bit, issue the “Block Erase” command while the FPROTCN bit in the FPROTR register is 1. To set the FAREASELC register is required to switch to the area for overwriting the code flash memory. To set the FCPSR register is required to switch the suspending method by the program/eraser suspend command (suspend priority mode/eraser priority mode).

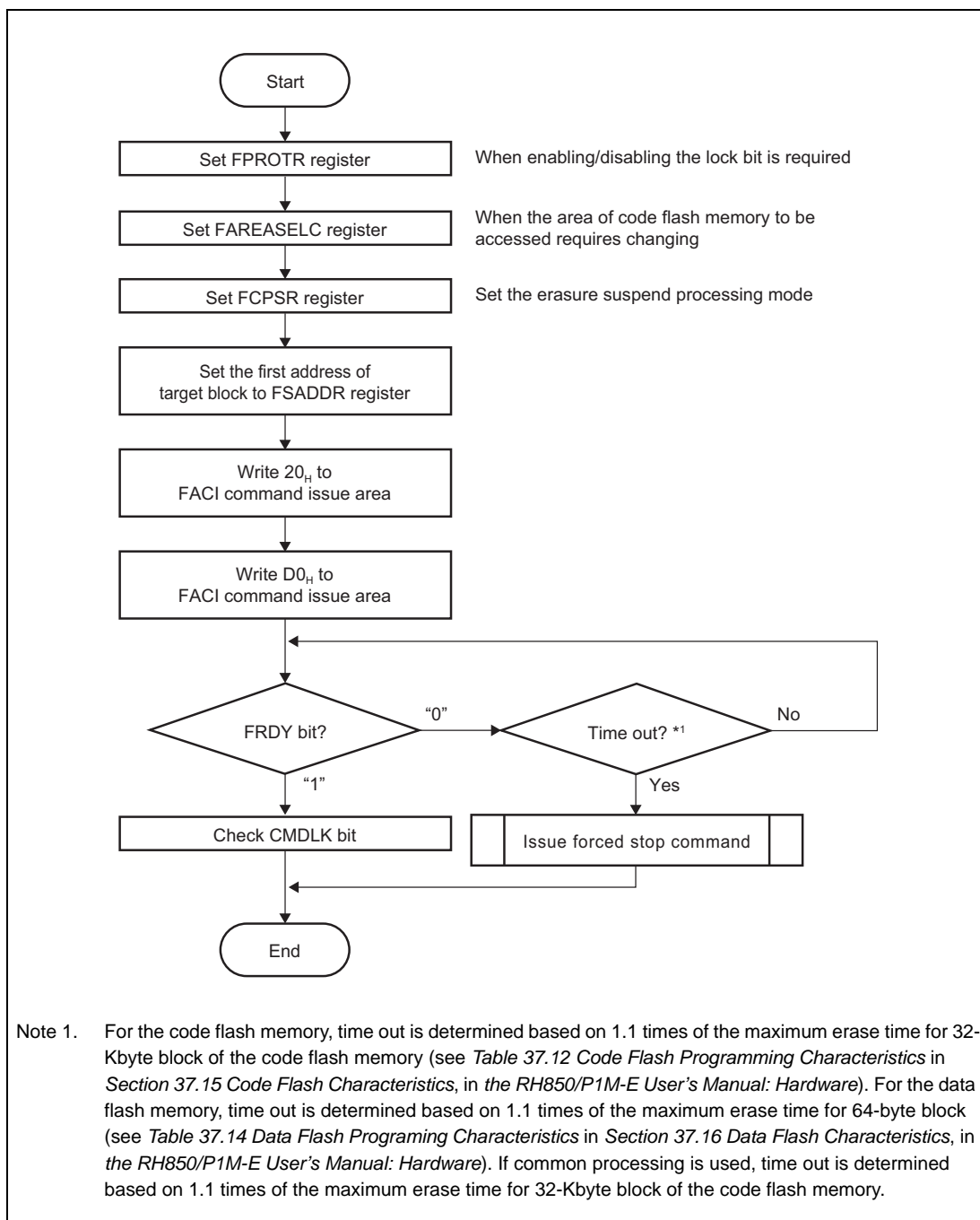


Figure 6.10 Block Erase Command Usage

6.3.11 Program/Erasure Suspend Command

“Program/Erasure Suspend” command is used for suspending “Program” or “Erasure” command processing. Before issuing “Program/Erasure Suspend” command, check that CMDLK bit is “0” to ensure that “Program” or “Erasure” command processing is being performed correctly. In addition, check that the SUSRDY bit is “1” to ensure that “Program/Erasure Suspend” command is acceptable. After issuing “Program/Erasure Suspend” command, check CMDLK bit to ensure no error has occurred.

If an error has occurred, the CMDLK bit is set to “1”. If “Program” or “Erasure” command processing is complete within the period from when the SUSRDY bit is ensured to be “1” until “Program/Erasure Suspend” command is accepted, no error occurs, hence no transition to a suspended state (the FRDY bit is “1” and both ERSSPD and PRGSPD bits are “0”).

Once “Program/Erasure Suspend” command is accepted and “Program” or “Erasure” command processing is normally suspended, flash sequencer enters a suspended state and that FRDY bit is “1” and ERSSPD or PRGSPD bit is “1”. After issuing “Program/Erasure Suspend” command, first ensure that the flash sequencer has entered the suspend state by checking that the ERSSPD or PRGSPD bit is “1”, and then determine which operations to execute next. If “Program/Erasure Resume” command is issued in the succeeding process while flash sequencer has not entered a suspended state, an illegal command error occurs and flash sequencer shifts to “Command Lock” state.

When the operation shifts to the erase suspend state, blocks that are not erase targets can be written. In addition, when the FENTRYR register is cleared, the operation shifts to the read mode.

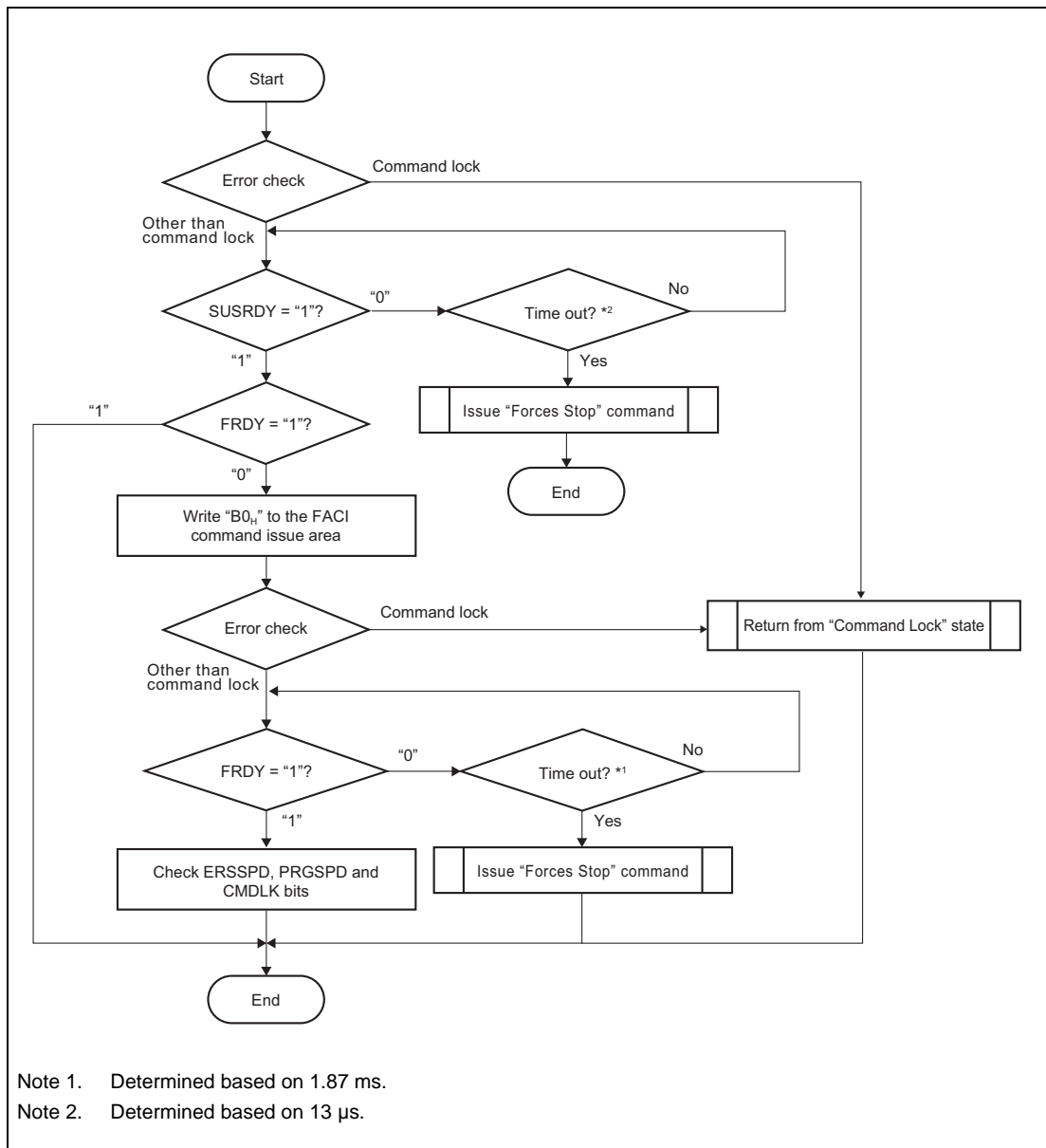


Figure 6.11 "Program/Erasure Suspend" Command Usage

(1) Suspend program command

If the "Program/Erasure Suspend" command is issued while writing to the flash memory, the flash sequencer stops programming. **Figure 6.12** gives an overview of operation for suspending "Program" command processing. Upon accepting "Program" command, FACI clears FRDY bit of the FSTATR register to "0" and starts programming. Once FACI enters a state where it is ready to accept "Program/Erasure Suspend" command after the start of programming, SUSRDY bit of the FSTATR register is set to "1". If "Program/Erasure Suspend" command is issued, FACI accepts the command and clears SUSRDY bit. If FCU accepts interrupt request while applying a write pulse, FCU continues applying the pulse. After a specified pulse application time has elapsed, FCU completes applying the pulse, suspends programming, and sets PRGSPD bit of the FSTATR register to "1". Once the process completes, FACI sets FRDY bit to "1" and enters programming suspended state. If FACI accepts "Program/Erasure Resume" command in this state, FACI clears FRDY and PRGSPD bits to "0" and restarts programming.

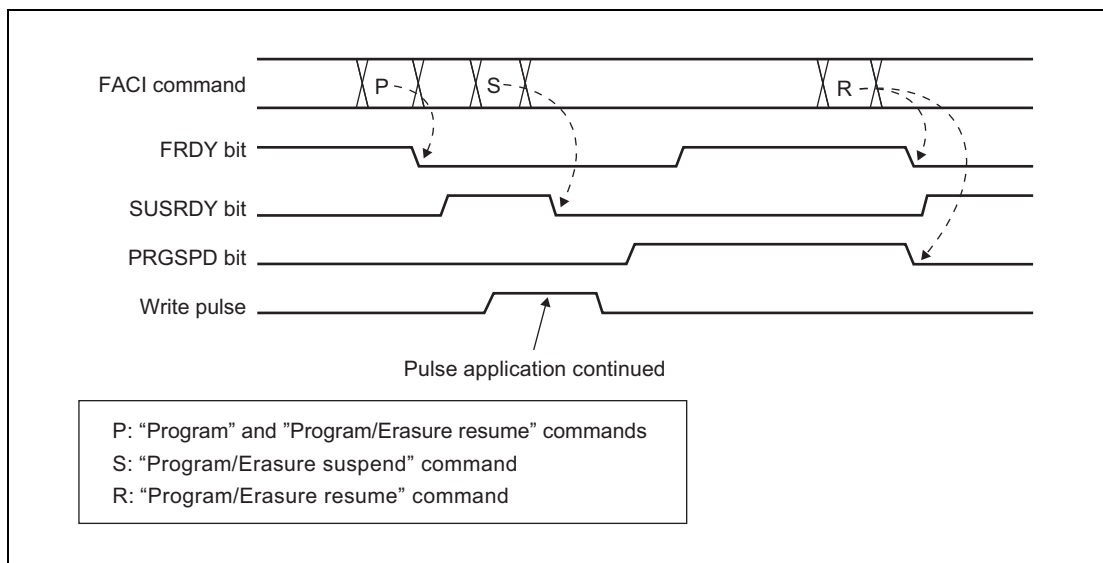


Figure 6.12 Suspend "Program" Command

(2) Suspend erase command in suspension-priority mode

A suspension-priority mode is supported as a way to suspend erasure. **Figure 6.13** shows the operation for suspending “Erasure” command processing in suspension-priority mode (FCPSR.ESUSPMD = “0”). Upon accepting an “Erase” command, FACI clears the FRDY bit of the FSTATR register to “0” and starts erasing. Once FACI enters a state where it is ready to accept “Program/Erase Suspend” command after the start of erasing, the SUSRDY bit of the FSTATR register is set to “1”. If “Program/Erase Suspend” command is issued, FACI accepts the command and clears the SUSRDY bit. If FCU accepts interrupt request during its erasing operation, FCU starts a suspending process even while applying a pulse and sets ERSSPD bit of the FSTATR register to “1”. Once the suspending process completes, FACI sets FRDY bit to “1” and enters erasing suspended state. If FACI accepts “Program/Erasure Resume” command in this state, FACI clears FRDY and ERSSPD bits to “0” and restarts erasing. The operations of FRDY, SUSRDY, and ERSSPD bits are independent of the erasure-suspended mode.

The setting for erasure-suspended mode affects the control methods for erasure pulse. In suspension-priority mode, if FCU accepts interrupt request while applying erasure pulse A, which has not been suspended previously, FCU suspends the pulse application, and FACI enters an erasure-suspended state. After FACI resumes erasing by accepting a “Program/Erasure Resume” command, FCU accepts resume request while applying erasing pulse A, FCU continues applying the pulse. After a specified pulse application time has elapsed, FCU completes applying the pulse, and FACI enters an erasure-suspended state. Next, after FACI accepts “Program/Erasure Resume” command, and FCU starts applying a new pulse B, if FCU accepts interrupt request, FCU suspends the pulse application. In suspension-priority mode, suspension processing is given priority by suspending the erasure pulse each time it is applied, which reduces the suspension delay.

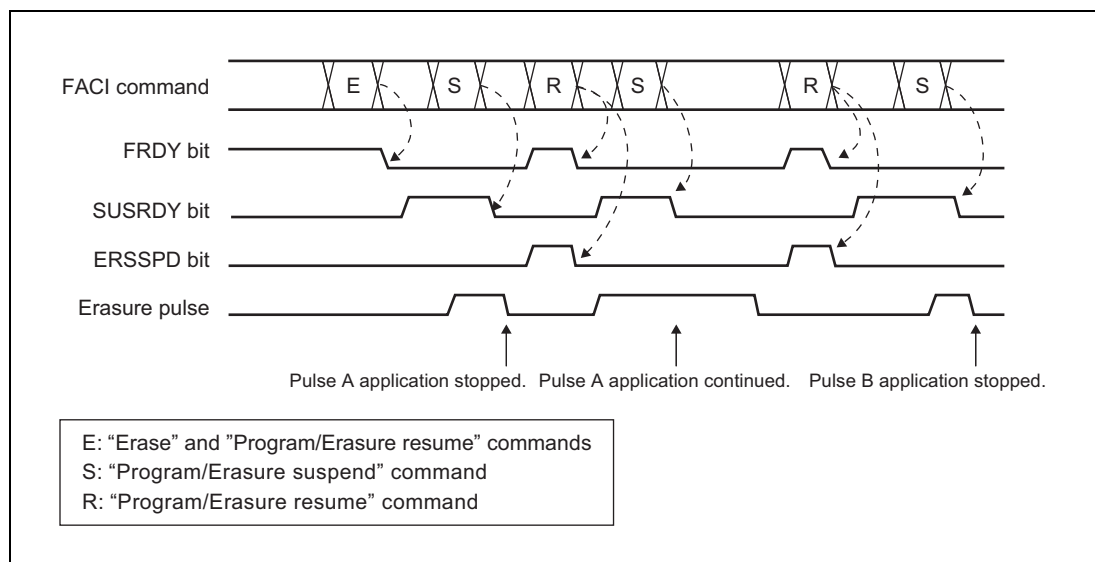


Figure 6.13 Suspend “Erase” Command (Suspension-Priority Mode)

(3) Suspend erase command in erasure-priority mode

A suspension-priority mode is supported as a way of suspending erasure. Figure 6.14 shows the erasure suspension processing in the suspension-priority mode (the ESUSPMD bit in the FCPSR register is "1"). The operation for suspending "Erasure" command processing in erasure-priority mode is equivalent to that for suspending programming processing. In erasure-priority mode, if FACI accepts "Program/Erasure Suspend" command while applying an erasing pulse, FCU always continues applying the pulse. As processing to reapply an erasing pulse never takes place in this mode, the total time required for "Erase" command processing is shorter than in suspension-priority mode.

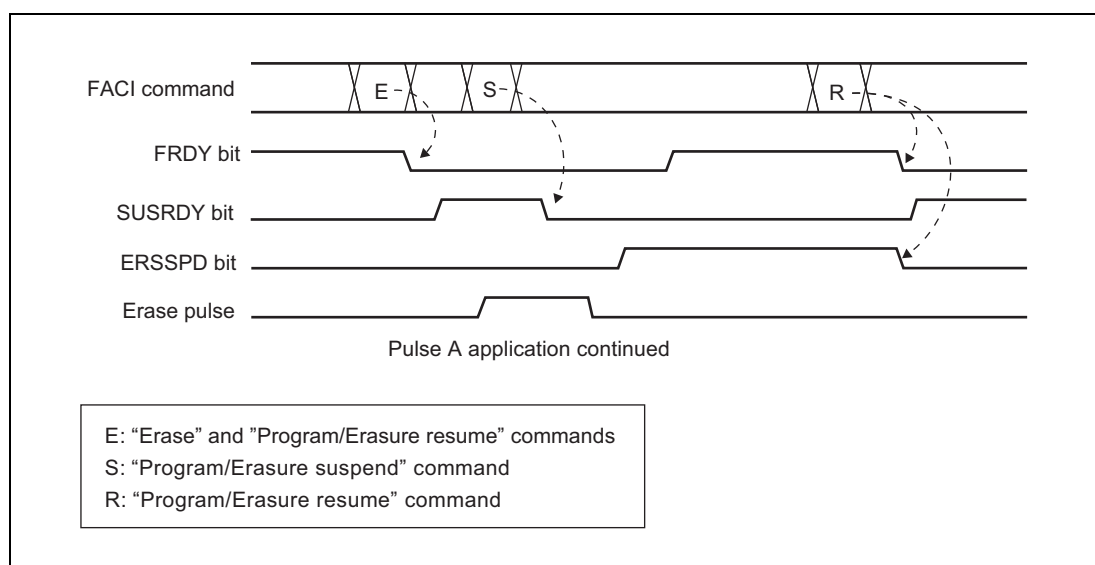


Figure 6.14 Suspend "Erase" Command (Erasure-Priority Mode)

6.3.12 Program/Erasure Resume Command

“Program /Erase Resume” command is used for resuming “Program” or “Erasure” command processing that has been suspended. If the FENTRYR setting was modified during suspension, issue “Program/Erasure Resume” command only after resetting FENTRYR to the previous value that was held before the “Program/Erasure Suspend” command was issued.

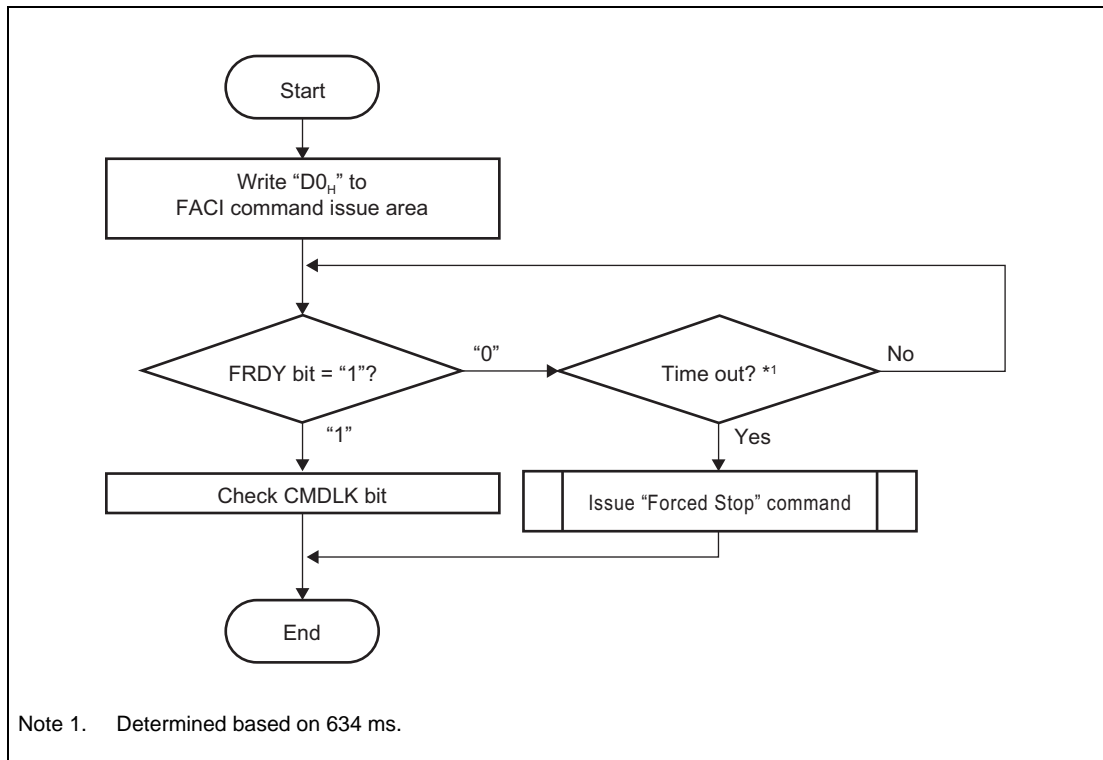


Figure 6.15 “Program/Erasure Resume” Command Usage

6.3.13 Status Clear Command

The status clear command is used to clear the “Command Lock” state. (See **Section 6.3.7, Return from Command Lock State**.) To clear the OTPDTCT/ILGLERR/ERSERR/PRGERR/CFGDTCT/TBLDTCT bit in the FSTATR register in the “Command Lock” state, the status clear command is available. In addition, to clear 1-bit correction flags (the OTPCRCT, CFGCRCT, and TBLCRCT bits), which do not cause transitions to the “Command Lock” state, the status clear command is available.

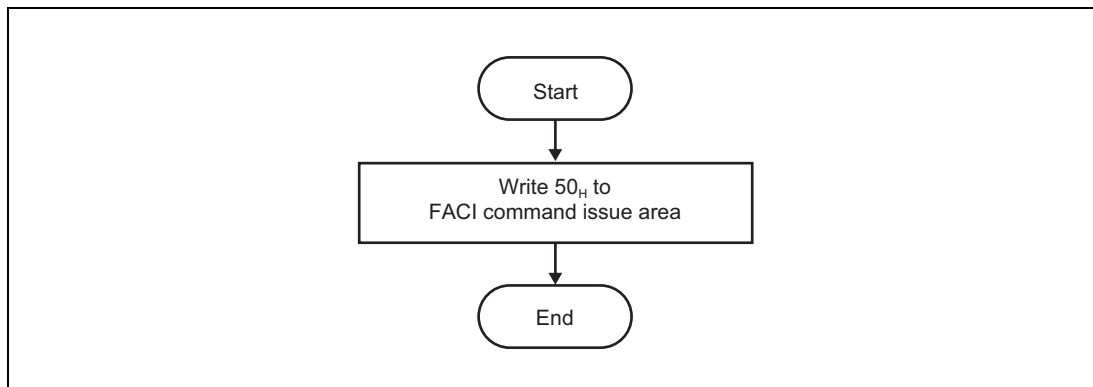


Figure 6.16 “Status Clear” Command Usage

6.3.14 Forced Stop Command

The forced stop command is used to forcibly stop the flash sequencer command processing. “Forced Stop” command provides the shortest latency when user wants to stop a flash sequencer command processing. However, after issuing “Forced Stop” command, flash sequencer does not guarantee any result of stopped command operation such as data in programmed or erased area.

Executing the forced stop command initializes the entire FCU and some of the FACI. It also initializes the FSTATR register. Therefore, this command can be used to return from the command lock state or end a timeout of a flash sequencer operation. (See **Section 6.3.7, Return from Command Lock State.**)

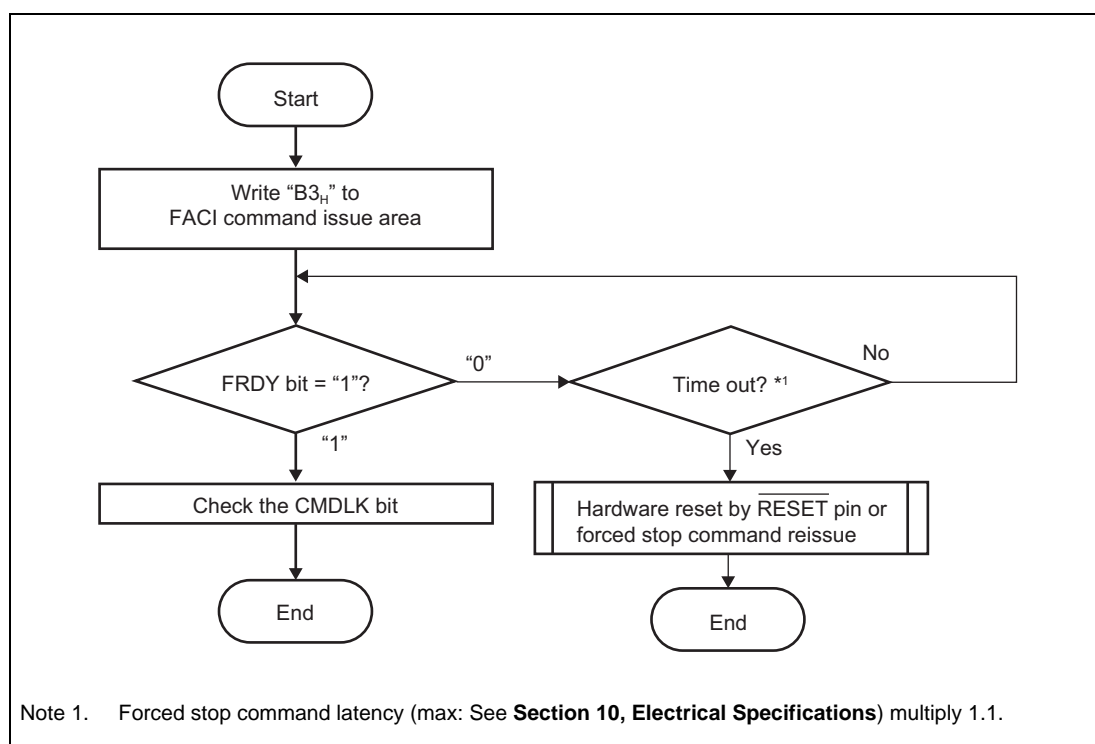


Figure 6.17 “Forced Stop” Command Usage

6.3.14.1 How to Use the Forced Stop Command During Command Issuance

In the following cases, writing to the FACI command issuing area is handled as program command write data:

- A timeout occurs due to program command DBFULL bit judgment
- A timeout occurs due to DBFULL or EBFULL bit judgment when an ECC error is inserted
- Command processing is stopped by the issuance of the forced stop command during a DMA program command timeout

In the above cases, read the FACI command issuing area to cause the generation of a command lock, and then issue the forced stop command in accordance with the method used to return from the command lock state. Note that a command lock can be generated regardless of whether the FACI command issuing area is read in 8-bit, 16-bit, or 32-bit units.

6.3.15 Blank Check Command

Values read from data flash memory that has been erased but not yet been programmed again are undefined. Use the “Blank Check” command when you need to confirm that an area is in the non-programmed state. For the method for the code flash memory, See Section 8.5, Blank Checking of Code Flash Memory.

Before issuing “Blank Check” command, set addressing mode, start address, and end address to FBCCNT, FSADDR, and FEADDR register, respectively. When blank check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = “1”), address specified in FSADDR should be equal to or larger than address in FEADDR. Conversely, address in FSADDR should be equal to or smaller than address in FEADDR when blank check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = “0”). If setting of BCDIR, FSADDR, and FEADDR are inconsistent, FACL detects error and flash sequencer enters “Command Lock” state. Blank check unit can be set from 4 bytes to 64 Kbytes.

Write 71_H and $D0_H$ to the FACL command issue area to start “Blank Check” command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register. At the end of processing, the result of “Blank Check” is stored in the BCST bit in the FBCSTAT register. If non-blank data exists within blank checked area, flash sequencer stops blank check operation. In this case, address of non-blank data is indicated to FPSADDR register.

“Blank Check” is the function to check the erasure state of the area where erasure operation is normally completed. When erasure operation is aborted due to reset input or power off, this function cannot be used to check the erasure state.

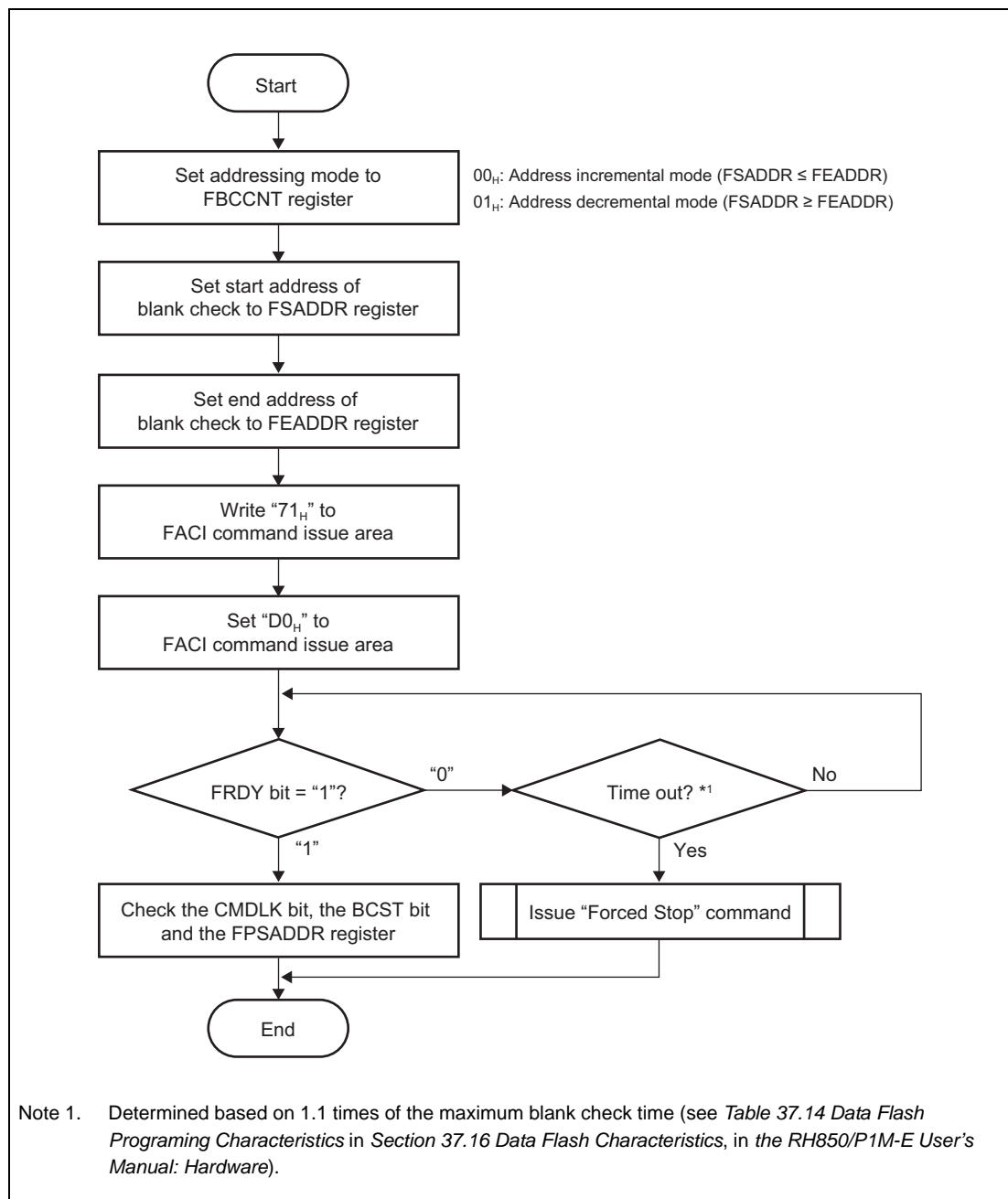


Figure 6.18 "Blank Check" Command Usage

6.3.16 Config Program Setting Command

“Config Program” command is used to set the ID, security function, safety function, and option byte. Before issuing the Config Program command, set the specified address (shown in **Table 6.5**) to the FSADDR register. Writing D0_H to the FACI command issue area at the final access of the FACI command issue starts the Config Program command processing.

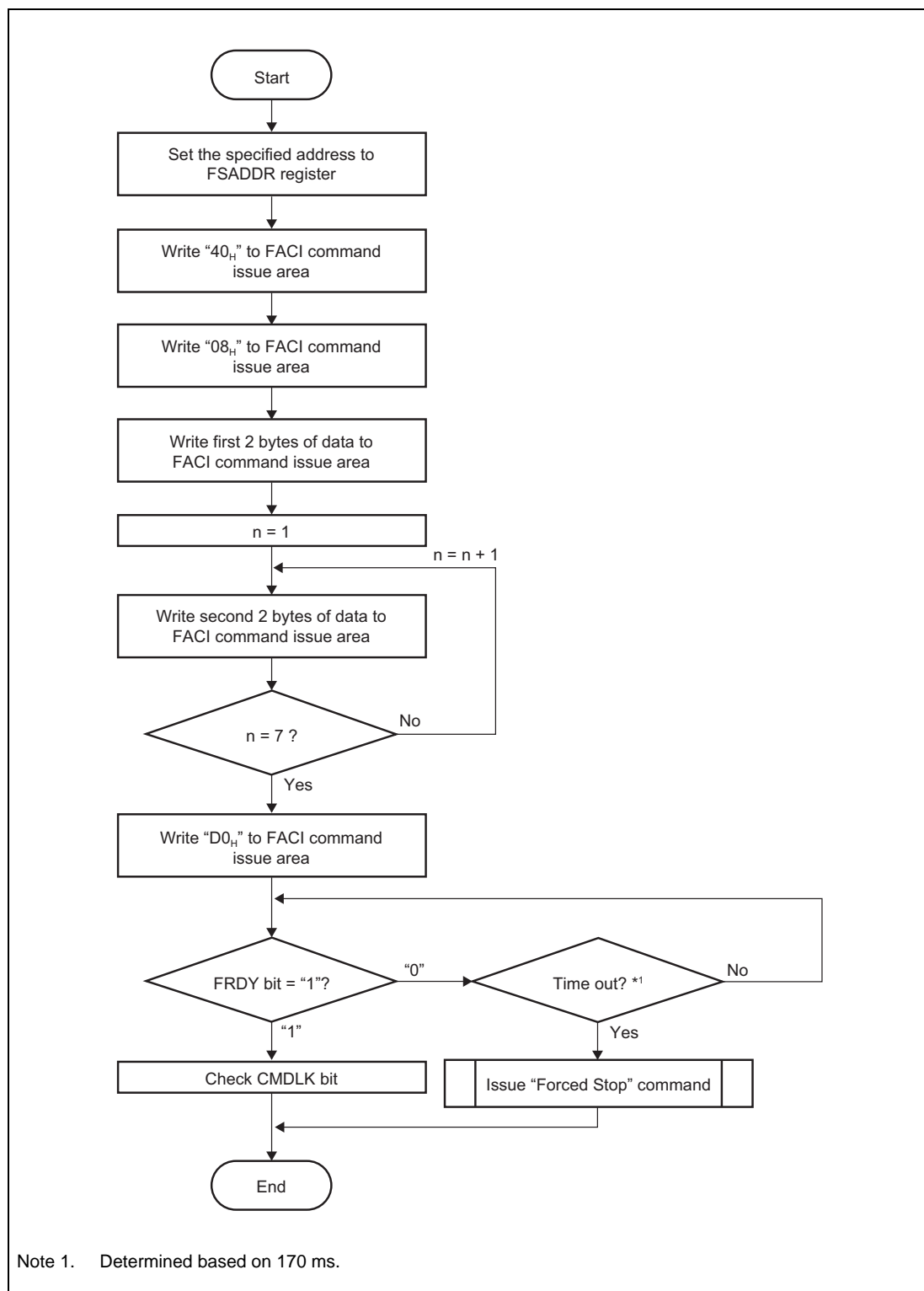


Figure 6.19 “Config Program” Command Usage

As for the Configuration Program settable data and the address value to be set in the FSADDR register, refer to **Table 6.5**. Once 0 is set as data in the security setting area, it cannot be changed to 1. Data in other areas can be change to any value each time the Configuration Program command is executed.

Table 6.5 Address Used by Configuration Program Command

Address	Setting Data
FF30 0070 _H	Option byte
FF30 0060 _H	Variable reset vector
FF30 0050 _H	ID for authentication
FF30 0040 _H	Security

Table 6.6 lists the security setting data when various security functions are enabled.

Table 6.6 List of Security Setting Data

Security Functions	Security Setting Data (16 bytes)
ID authentication enabled in serial programming mode	FFFF FFFF FFFF FFFF FFFF FFFF 1EFF FFFF _H
Serial programmer connection disabled	FFFF FFFF FFFF FFFF FFFF FFFF F7FF FFFF _H
Block erasure command disabled	FFFF FFFF FFFF FFFF FFFF FFFF DFFF FFFF _H
Program command disabled	FFFF FFFF FFFF FFFF FFFF FFFF BFFF FFFF _H
Read command disabled	FFFF FFFF FFFF FFFF FFFF FFFF 7FFF FFFF _H

See the section of the *option bytes* in the *User's Manual* regarding the details for the target registers.

6.3.17 Reading the Configuration Setting Area

When reading the configuration setting area to check the value written by “Config Program” command, set the BFAA bit in the BFASCLR register to “1”. Setting the BFAA bit to “1” disables reading of the user area. The software that reads the configuration setting area must be executed on the internal RAM. For the address map for the area for configuration settings, see **Table 6.5**.

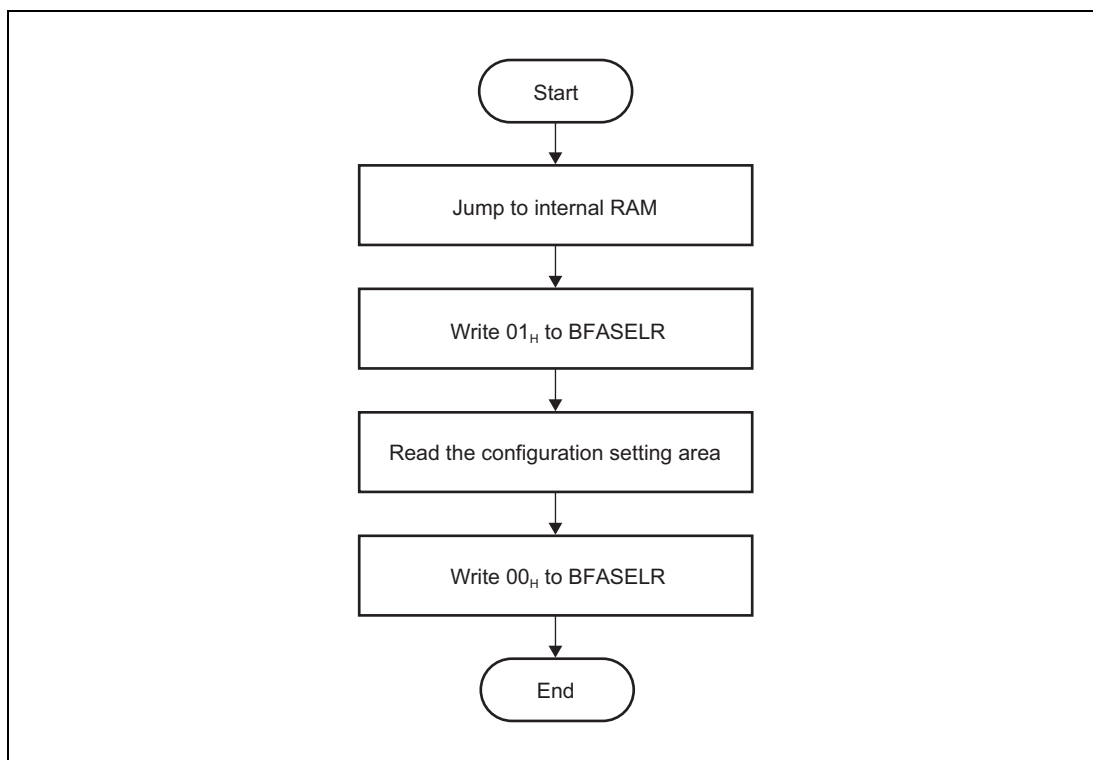


Figure 6.20 Flow of Reading of the Configuration Setting Area

6.3.18 Lock Bit Program Command

“Lock Bit Program” command is used for programming lock bit. For the erasure of lock bits, use the block erasure command. (See **Section 6.3.10, Block Erase Command.**)

Before issuing “Lock Bit Program” command, set first address of target block to FSADRR register. Writing “77_H” and “D0_H” to FACI command issue area starts the “Lock Bit Program” command processing.

Set the FPROTR register before issuing the lock bit program command. To set the FPROTR and FAREASELC registers is required to switch enabling/disabling the lock bit. To set the FAREASELC register is required to switch the area for overwriting the code flash memory.

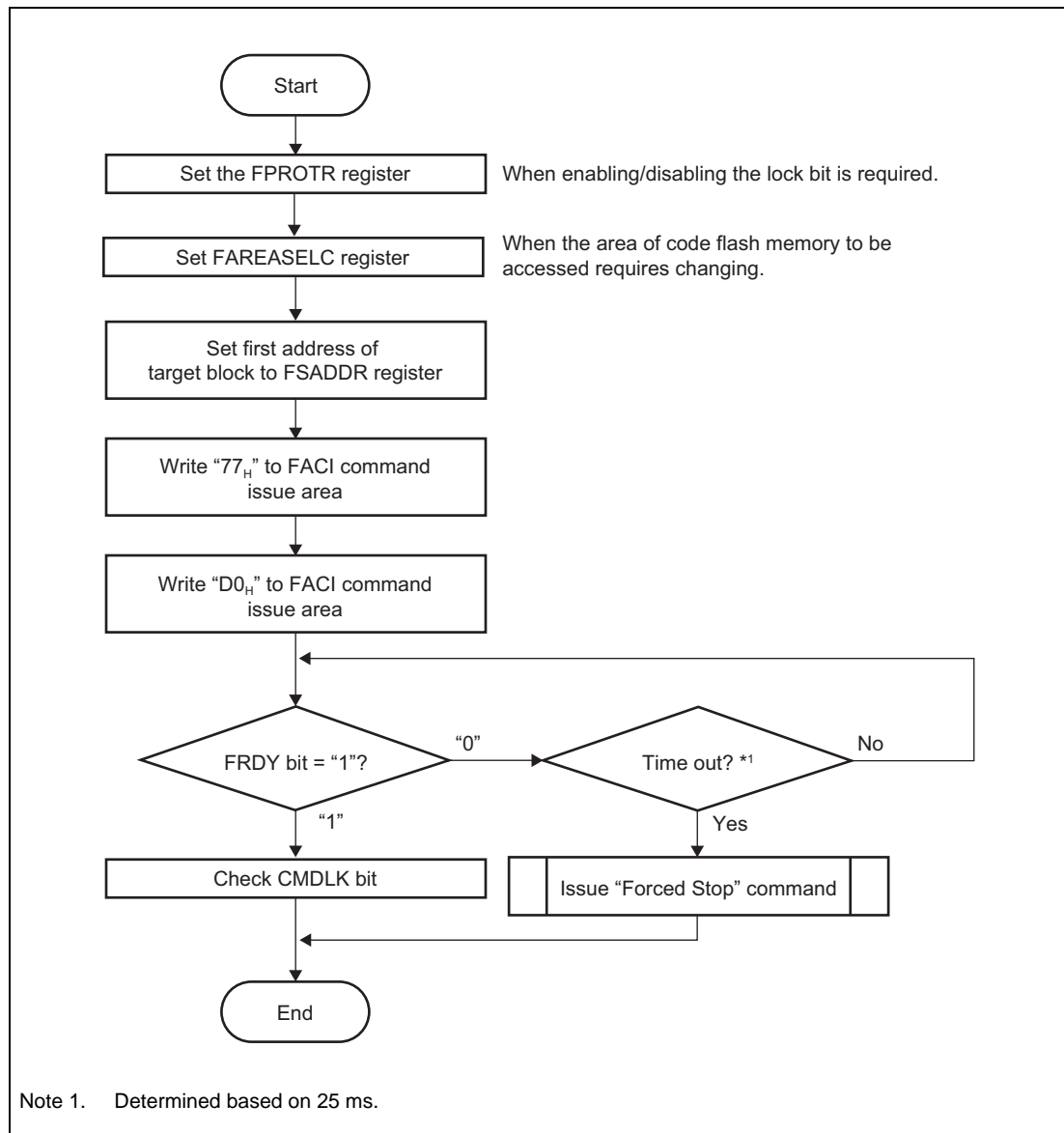


Figure 6.21 “Lock Bit Program” Command Usage

6.3.19 Lock Bit Read Command

“Lock Bit Read” command is used for read lock bit.

Before issuing “Lock Bit Read” command, set first address of target block to FSADRR register. Writing “71_H” and “D0_H” to FACL command issue area starts “Lock Bit Read” command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register. After “Lock Bit Read” command processing is completed normally, the FLOCKST bit in the FLKSTAT register will hold the result of reading the lock bit.

The FAREASELC register must be set before a “Lock Bit Read” command is issued. To set the FAREASELC register is required to switch the area for overwriting the code flash memory.

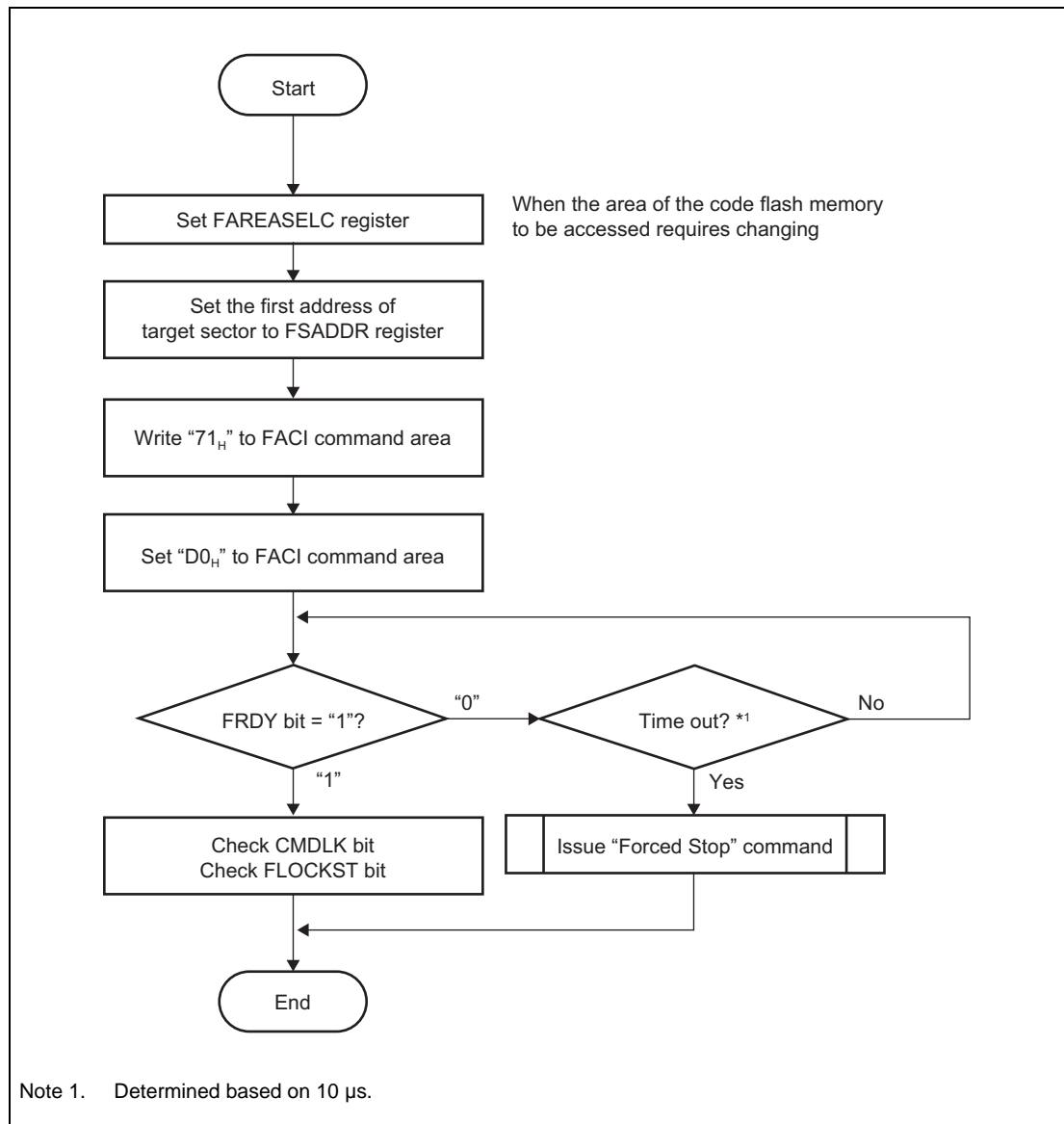


Figure 6.22 “Lock Bit Read” Command Usage

6.3.20 OTP Set Command

“OTP Set” command is used to set OTP. Before issuing “OTP Set” command, set the specified address of the set data (shown in **Table 6.7**) to FSADDR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the OTP Set command processing.

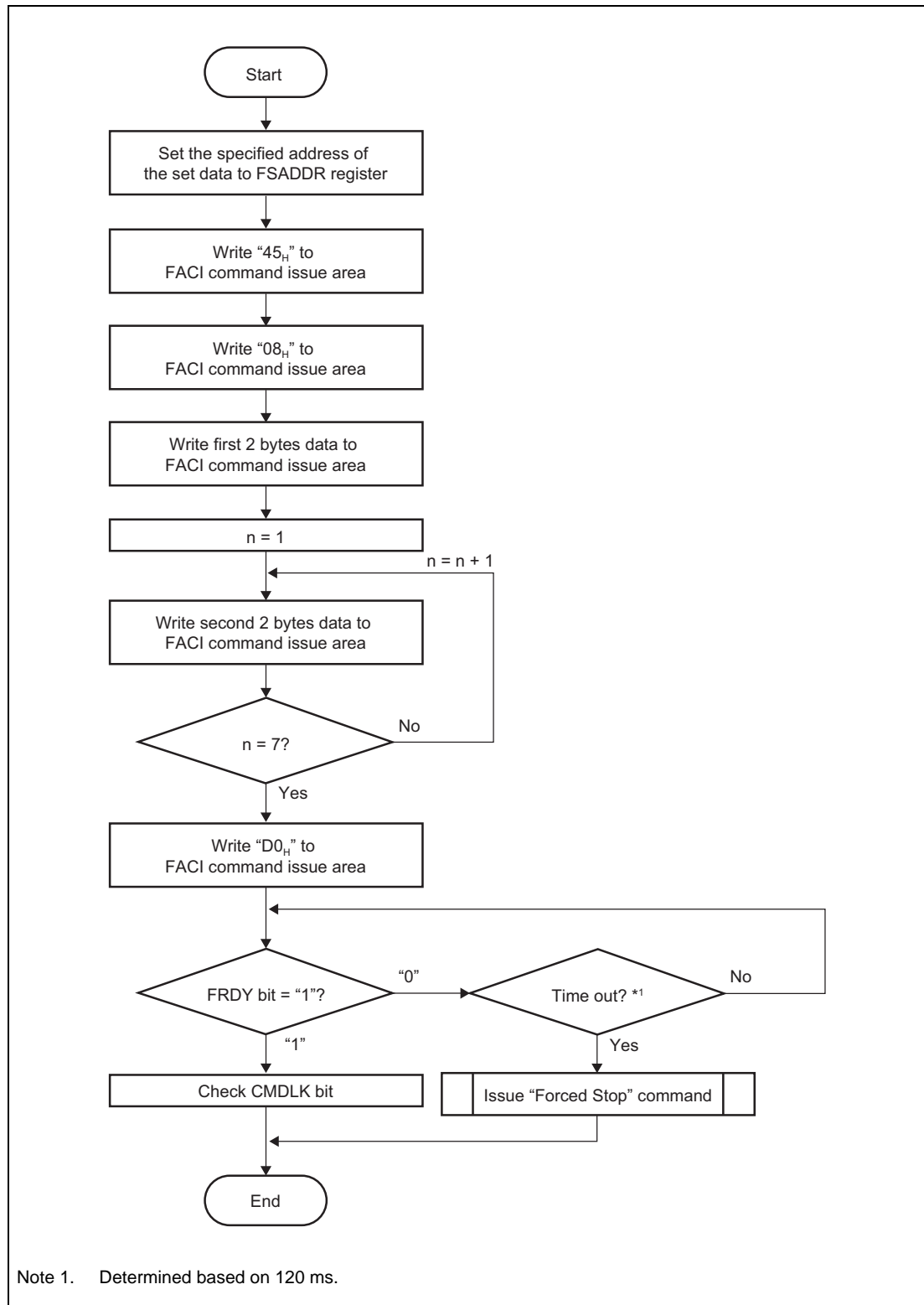


Figure 6.23 “OTP Set” Command Usage

Figure 6.24 shows the relationship between the user area blocks and OTP setting flags. An OTP setting flag (OTPF0 to OTPF69) is allocated to each user area block (8 Kbytes × 8 blocks and 32 Kbytes × 62 blocks).

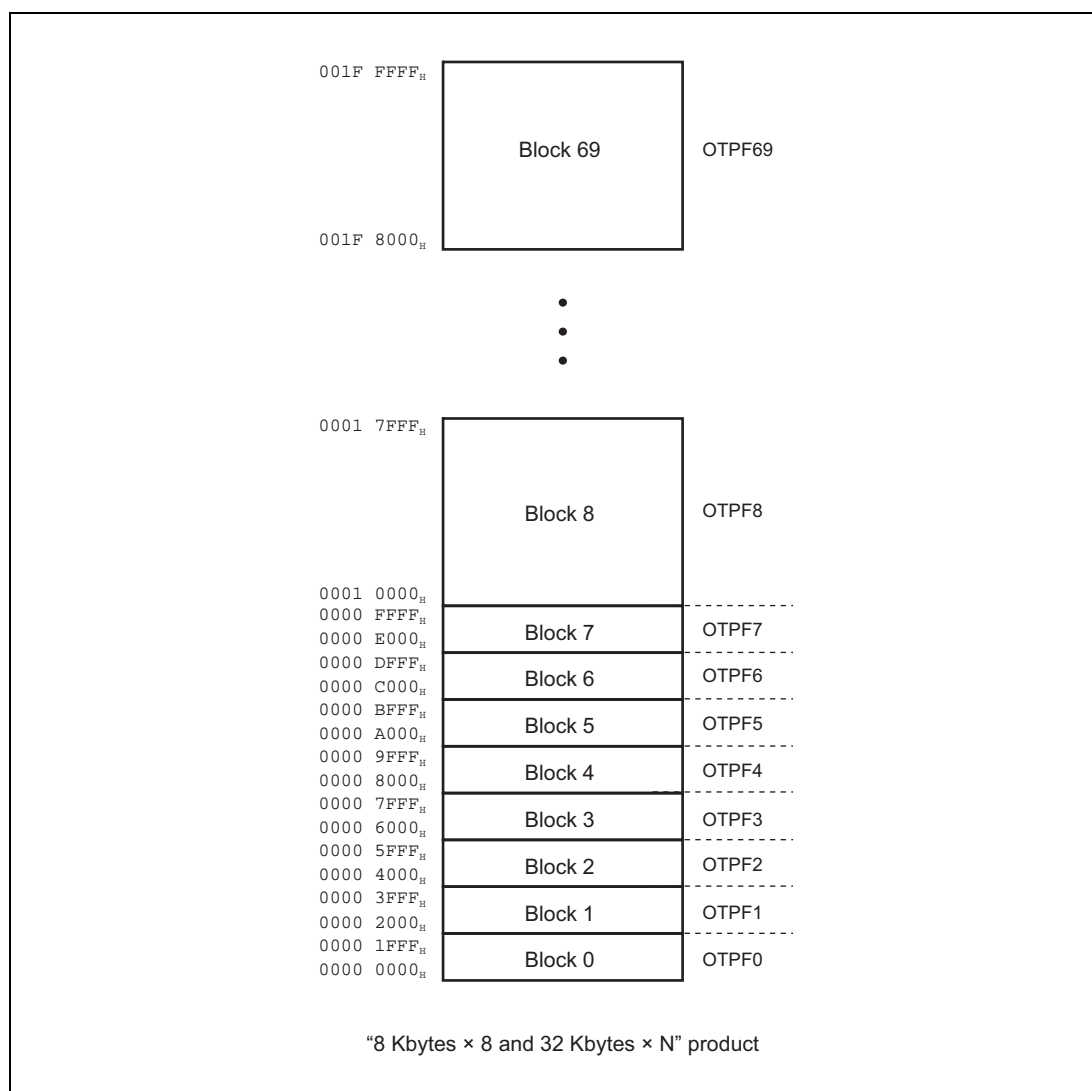


Figure 6.24 Relationship between User Area Blocks and OTP Setting Flags

Table 6.7 shows the addresses to be used for the OTP Set command. When 0 is set to a flag, OTP is set for the corresponding block. Once 0 is set to a flag, it cannot be changed to 1.

Table 6.7 Address to be Used for OTP Set Command

Address	Set Data
FF38 0090 _H	User boot area and OTP flag for extended user area (bit 0)
FF38 0080 _H	Reserved area* ¹
FF38 0070 _H	Reserved area* ¹
FF38 0060 _H	Reserved area* ¹
FF38 0050 _H	Reserved area* ¹
FF38 0040 _H	Reserved area* ¹ (bit 127 to 70), OTPF69 (bit 69) to OTPF0 (bit 0)

Note 1. Do not set "0" to the reserved areas. The operation with the reserved area set to 0 is not guaranteed.

6.3.21 Reading the OTP Setting Area

When reading the OTP setting area to check the value written by “OTP Set” command, set the BFAA bit in the BFASCLR register to “1”. Setting the BFAA bit to “1” disables reading of the user area. The software that reads the OTP setting area must be executed on the internal RAM. For the address map for the area of OTP settings, see **Table 6.7**.

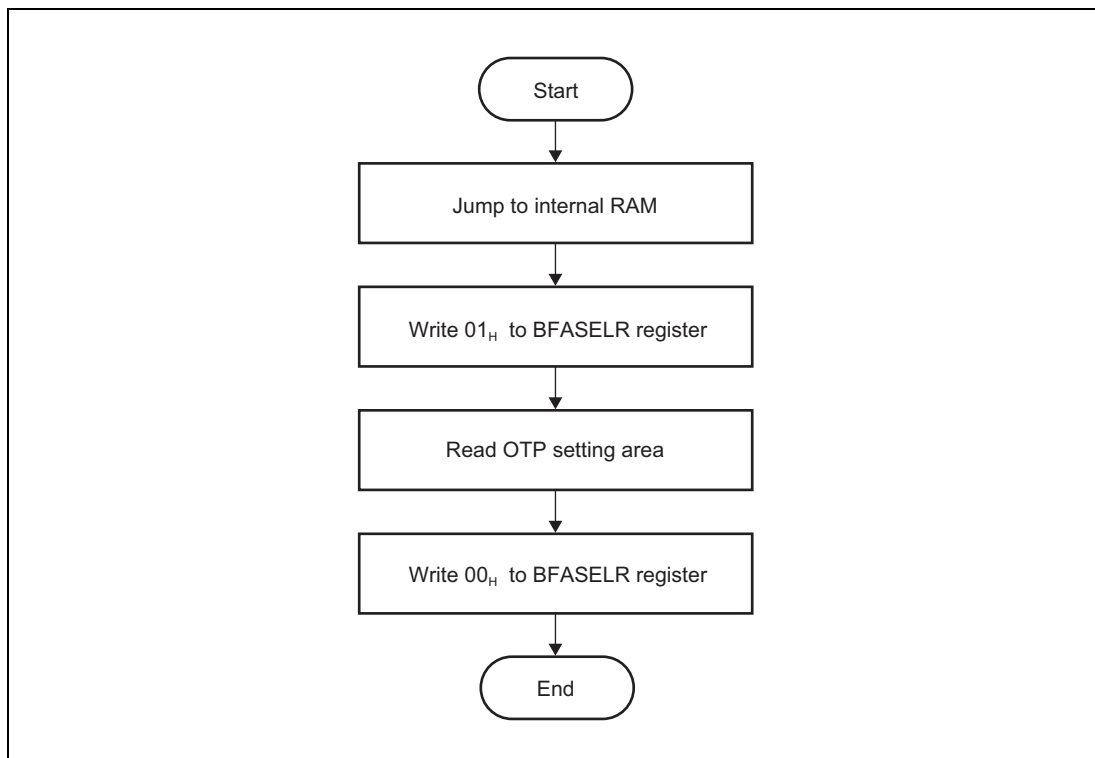


Figure 6.25 Flow of Reading the OTP Setting Area

6.3.22 Injecting ECC Errors for the Flash Memory

Any value of the ECC bits and address parity bits in the FDMYECC register can be written to the flash memory by using a programming command. Injecting an ECC error for the data area requires a four-byte programming command.

Before writing the value set in the FDMYECC register to the flash memory, set the ECCDISE bit in the FECCTMD register to 1. In addition, set the values for the ECC bits and address parity bits in the FDMYECC register before writing the data to the FACI command issuing area.

In the case of the code flash memory, the unit (256 bytes) for writing in response to the programming command differs from the unit (16 bytes) for which the ECC bits and address parity bits are to be added for the data. Therefore, every time 16 bytes of data are written to the FACI command issuing area, change the setting in the FDMYECC register.

In the case of the data flash memory, since the unit (4 bytes) for writing by the programming command is the same as that for the unit (4 bytes) of data for which the ECC bits are to be added, only change the setting in the FDMYECC register once before issuing the programming command.

If the command for writing to the FDMYECC register is issued repeatedly while the EBFULL bit in the FSTATR register is “1”, a wait is generated in the P-Bus, which will affect performance in communication with other peripheral IP modules. To avoid the generation of such a wait, write to the FDMYECC register while the EBFULL bit in the FSTATR register is 0.

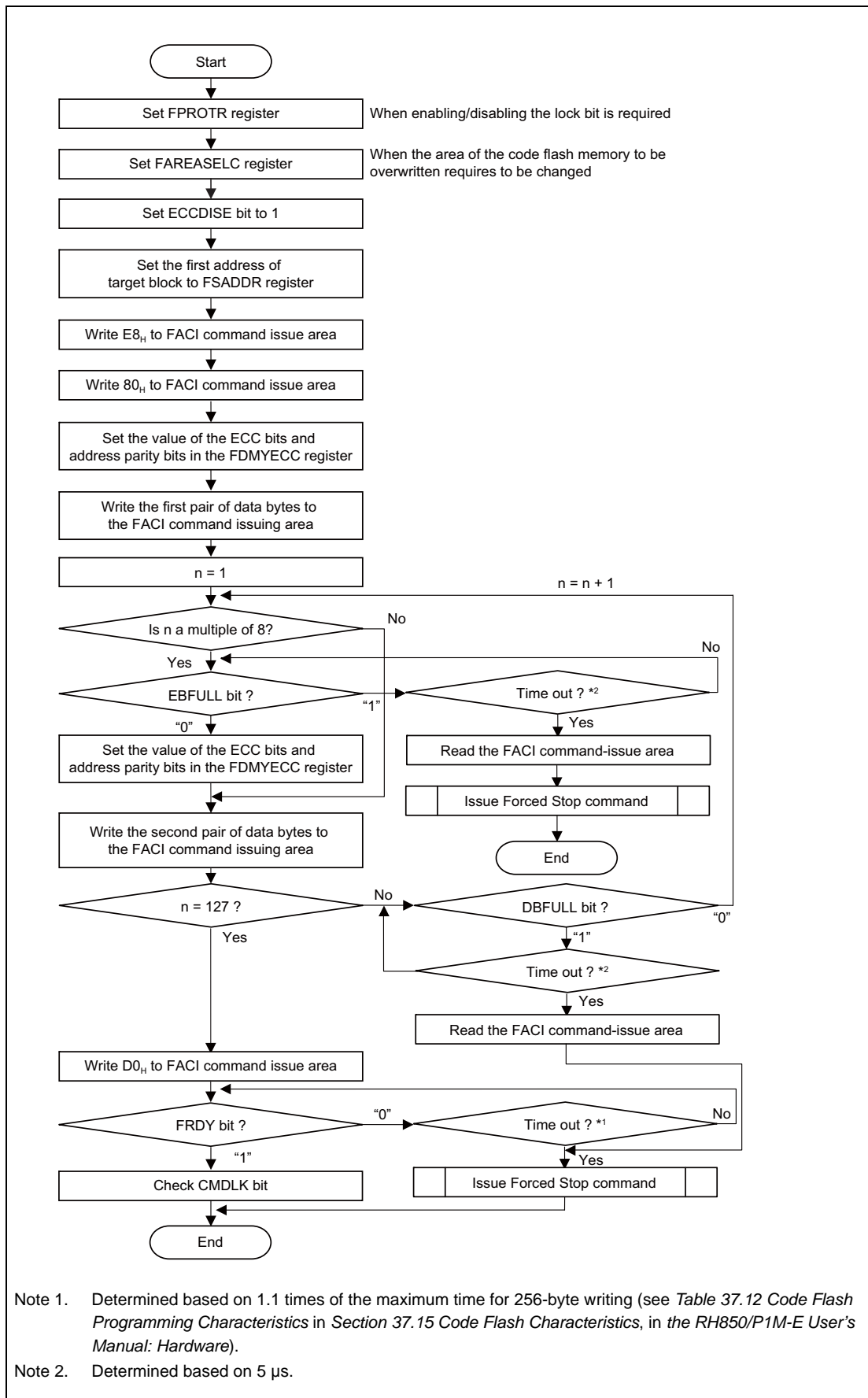


Figure 6.26 Injecting an ECC Error for the Code Flash Memory

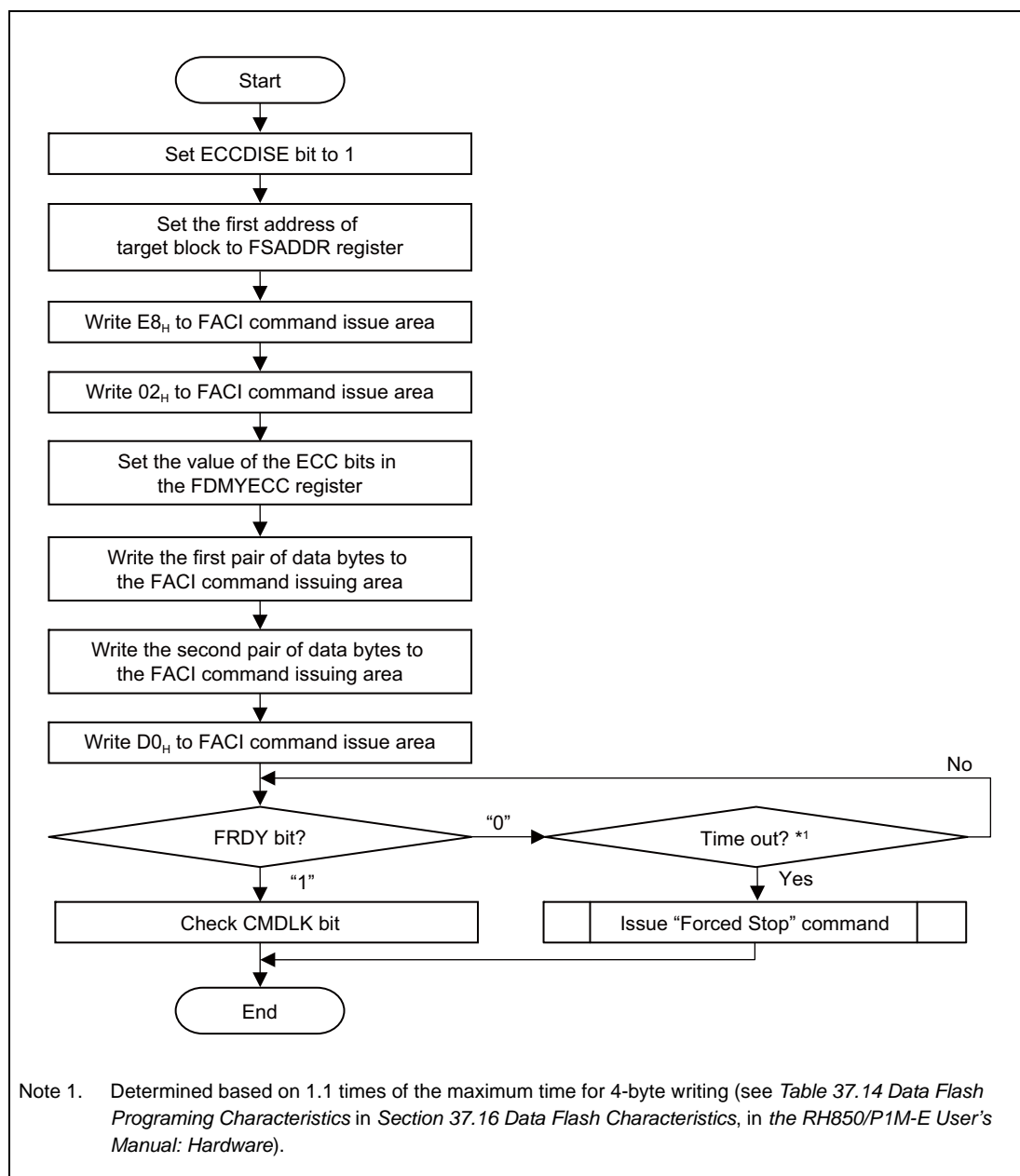


Figure 6.27 Injecting an ECC Error for the Data Flash Memory

Section 7 Security Function

7.1 FACI Command Protection by ID

In code flash program/erasure mode, FACI commands can be used after security is released by the ID authentication. When the FACI command is issued while the IDST bit in the SELFIDST register is set to 1 (security lock state), the flash sequencer enters the “Command Lock” state. Also, when shifted to the code flash program/erasure mode, the flash sequencer enters the command lock state. If the flash sequencer enters the command lock state while security is not released by ID authentication, release from the command lock state is not possible even if the forced stop command is used. As for the security releasing method by the ID authentication, see **Section 6.3.6, ID Authentication**.

The ID used for authentication of Code Flash P/E mode is shared with the OCD connection and serial programmer connection (when ID authentication is enabled).

In data flash program/erasure mode, FACI commands can be used regardless of the IDST bit setting.

7.2 OTP for Code Flash Memory

OTP can be set independently for each block in the code flash memory. Once an OTP is set, it cannot be canceled. If Program, Block Erase, or Lock Bit Program command is issued to an OTP set block, the flash sequencer enters the “Command Lock” state.

Once an OTP configuration command has been executed for a chip, the variable reset vector cannot be set in the corresponding area by a “Config Program” command. Even when an OTP configuration command for a reserved area in the code flash memory is completed normally or execution of an OTP configuration command with all bits set to 1 is completed normally, the variable reset vector cannot be set in the corresponding area.

Section 8 Protection Function

8.1 Hardware Protection

While the low level is being input to the FLMD0 pin, the setting of the FWE bit in the FPMON register is 0. When the FWE bit is 0, writing 1 to the FENTRYC bit in the FENTRYR register is disabled. Since a transition to code flash programming/erasure mode is not possible, programming and erasing the code flash memory are prohibited. When the FRDY bit is 1 while the FLMD0 pin is at the low level, the flash sequencer clears the FENTRYC bit to disable programming and erasing of the code flash memory.

When the FLMD0 pin is changed to the low-level while the FRDY bit in the FSTATR register is 0, the flash sequencer continues processing of a command that is in progress. Even while command processing continues, however, the flash sequencer can accept requests to suspend programming and erasure.

To restart the programming or erasure, set the FENTRYC bit again and issue the programming/erasure resume command.

If the programming/erasure command is issued to the code flash memory in contradiction of protection by the FLMD0 pin, the flash sequencer enters the “Command Lock” state.

8.2 Software Protection

Software protection function disables flash sequencer command operation according to register settings or lock bit settings. If an attempt is made to issue flash sequencer command against software protection, flash sequencer enters “Command Lock” state.

8.2.1 Protection by FENTRYR

When FENTRYR register is set to “0000_H”, flash sequencer is set to read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue FACI command in read mode, flash sequencer enters “Command Lock” state.

8.2.2 Protection by Lock Bit

Each block in user area and extended user area have lock bits. When the FPROTCN bit in the FPROTR register is 0, programming/erasing the block where the corresponding lock bit is 0 is disabled. To program/erase the block where the corresponding lock bit is 0 is disabled, set the FPROTCN bit to 1. If an attempt is made to issue program/block erase/lock bit program command against protection by lock bits, the flash sequencer enters the “Command Lock” state.

8.3 Error Protection

Error protection function detects an illegal FACI command issued, an illegal access, or a flash sequencer malfunction, and disables FACI command acceptance (“Command Lock” state). While flash sequencer is in “Command Lock” state, flash memory cannot be programmed or erased. To cancel “Command Lock” state, issue “Status Clear” or “Forced Stop” command while the CFAE and DFAE bits in the FASTAT register is “0”. “Status Clear” command can be used only when FRDY bit is “1”. “Forced Stop” Command can be used regardless of FRDY bit value. While the CMDLKIE bit in FAEINT register is “1”, flash interface error (FLERR) interrupt is generated if flash sequencer is in the “Command Lock” state (the CMDLK bit of the FASTAT register is 1).

If flash sequencer enters “Command Lock” state during programming or erasure processing by the command other than Program/Erase suspend, the flash sequencer continues programming or erasure processing. In this state, programming or erasure processing cannot be suspended by the Program/Erase suspend command. If a command is issued in “Command Lock” state, ILGLERR bit becomes “1” and the other bits retain the values set due to the previous error detection.

Table 8.1 shows error protection types and status bit values after error detection.

Table 8.1 Error Protection Type (1/2)

Error Type	Description	OTPDTC	ILGLERR	ERSERR	PRGERR	FLWEERR	CFGDTCT	TBLDTCT	CFAE	DFAE
FENTRYR setting error	The value set in FENTRYR is not 0000 _H , 0001 _H or 0080 _H .	0	1	0	0	0	0	0	0	0
	The FENTRYR setting for resuming operation does not match that for suspending operation.	0	1	0	0	0	0	0	0	0
Illegal command error	An undefined code has been written in the first access of FACI command.	0	1	0	0	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not D0 _H (except for “DMA Program”).	0	1	0	0	0	0	0	0	0
	The value (N) specified in the second write access of FACI command in the “Program”, “DMA Program”, “Config Program”, or “OTP Set” command is wrong (odd number is wrong for “DMA Program”).	0	1	0	0	0	0	0	0	0
	“Blank Check” command has been issued with inconsistent BCDIR, FSADDR, and FEADDR settings. (See Section 4.6, FACI Command End Address Register (FEADDR).)	0	1	0	0	0	0	0	0	0
	FACI command has been issued against FACI command not acceptable mode. (See Table 6.3 .)	0	1	0	0	0	0	0	0	0
	FACI command has been issued when command acceptance conditions are not satisfied. (See Table 6.4)	0/1	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Erase error	An error has occurred during flash memory erasure.	0	0	1	0	0	0	0	0	0
	“Block Erase” command has been issued against lock bit protection.	0	0	1	0	0	0	0	0	0
Program error	An error has occurred during flash memory program.	0	0	0	1	0	0	0	0	0
	“Program” or “Lock Bit Program” command has been issued against lock bit protection.	0	0	0	1	0	0	0	0	0
Code flash access error	FACI command has been issued to reserved user area in code flash program/erasure mode. (See Section 4.2, Flash Access Status Register (FASTAT)).	0	1	0	0	0	0	0	1	0
	FACI command has been issued to reserved extended user area in code flash program/erasure mode. (See Section 4.2, Flash Access Status Register (FASTAT)).	0	1	0	0	0	0	0	1	0
Data flash access error	FACI command has been issued to reserved data area in data flash program/erasure mode. (See Section 4.2, Flash Access Status Register (FASTAT)).	0	1	0	0	0	0	0	0	1
	“Config Program” command has been issued to reserved area. (See Section 4.2, Flash Access Status Register (FASTAT)).	0	1	0	0	0	0	0	0	1
	“OTP Setting” command has been issued to reserved area. (See Section 4.2, Flash Access Status Register (FASTAT)).	0	1	0	0	0	0	0	0	1

Table 8.1 Error Protection Type (2/2)

Error Type	Description	OTPDTC	ILGLERR	ERSERR	PRGERR	FLWEERR	CFGDTCT	TBLDTCT	CFAE	DFAE
Security	"Program", "Block Erase", or "Lock Bit Program" command has been issued against OTP setting.	0	1	0	0	0	0	0	0	0
	"Config Program" command was issued for the variable reset vector due to OTP being set for the code flash memory.	0	1	0	0	0	0	0	0	0
	Operation has been shifted to the code flash program/erasure mode against security not-released state by ID authentication.	0	1	0	0	0	0	0	0	0
Other	FACI command issue area has been accessed in read mode.	0	1	0	0	0	0	0	0	0
	FACI command issue area has been read in code flash program/erasure mode or data flash program/erasure mode.	0	1	0	0	0	0	0	0	0
OTP Set ECC error	A 2-bit error has been detected when OTP setting is read.	1	0	0	0	0	0	0	0	0
FHVE set error	FHVE3CNT bit in FHVE3 register is changed to "0" during command processing of the flash sequencer.	0	0	0/1	0/1	1	0	0	0	0
Config Program ECC error	2-bit error has been detected when Config Program value is read.	0	0	0	0	0	1	0	0	0
Overwrite parameter ECC error	2-bit error has been detected when overwrite parameter table is read.	0	0	0	0	0	0	1	0	0

8.4 Boot Program Protection

8.4.1 Variable Reset Vector

Using a “Config Program” command to change the value of the variable reset vector area may change the reset vector of the CPU. Using the variable reset vector when the boot program in the code flash memory is updated makes safe rewriting possible.

Once an OTP configuration command has been executed for a chip, the variable reset vector cannot be set in the corresponding area by a “Config Program” command. Even when an OTP configuration command for a reserved area in the code flash memory is completed normally or execution of an OTP configuration command with all bits set to 1 is completed normally, the variable reset vector cannot be set in the corresponding area.

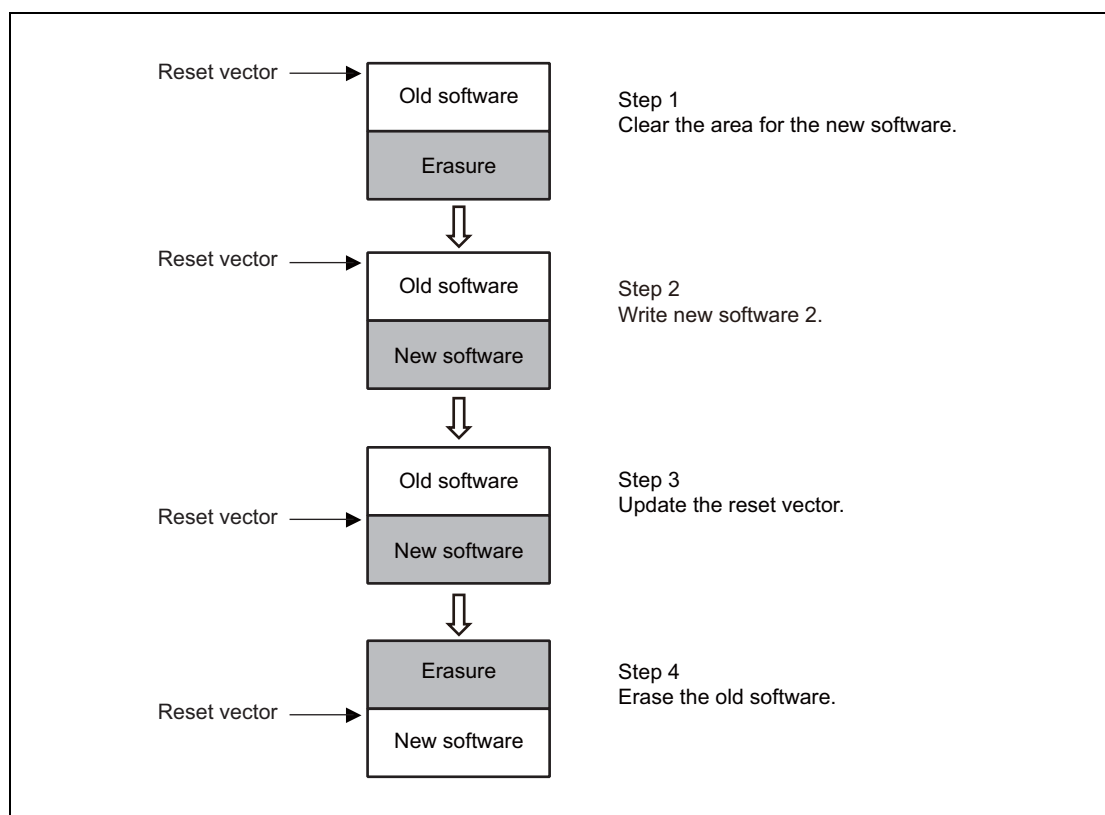


Figure 8.1 Software Update using the Variable Reset Vector

8.5 Blank Checking of Code Flash Memory

Reading from an area of the code flash memory that has been erased but to which no new data has been written (an area in the non-written state) leads to an exception since an ECC error will be detected. In addition, as the values of the data are not guaranteed when an ECC error has occurred, confirm that the area is in the non-written state by checking whether all data bits, ECC bits, and address parity bits for the code flash memory are set to 1. For usage notes on the ECC function for the code flash memory, see the section on safety features in the user's manual for the given product.

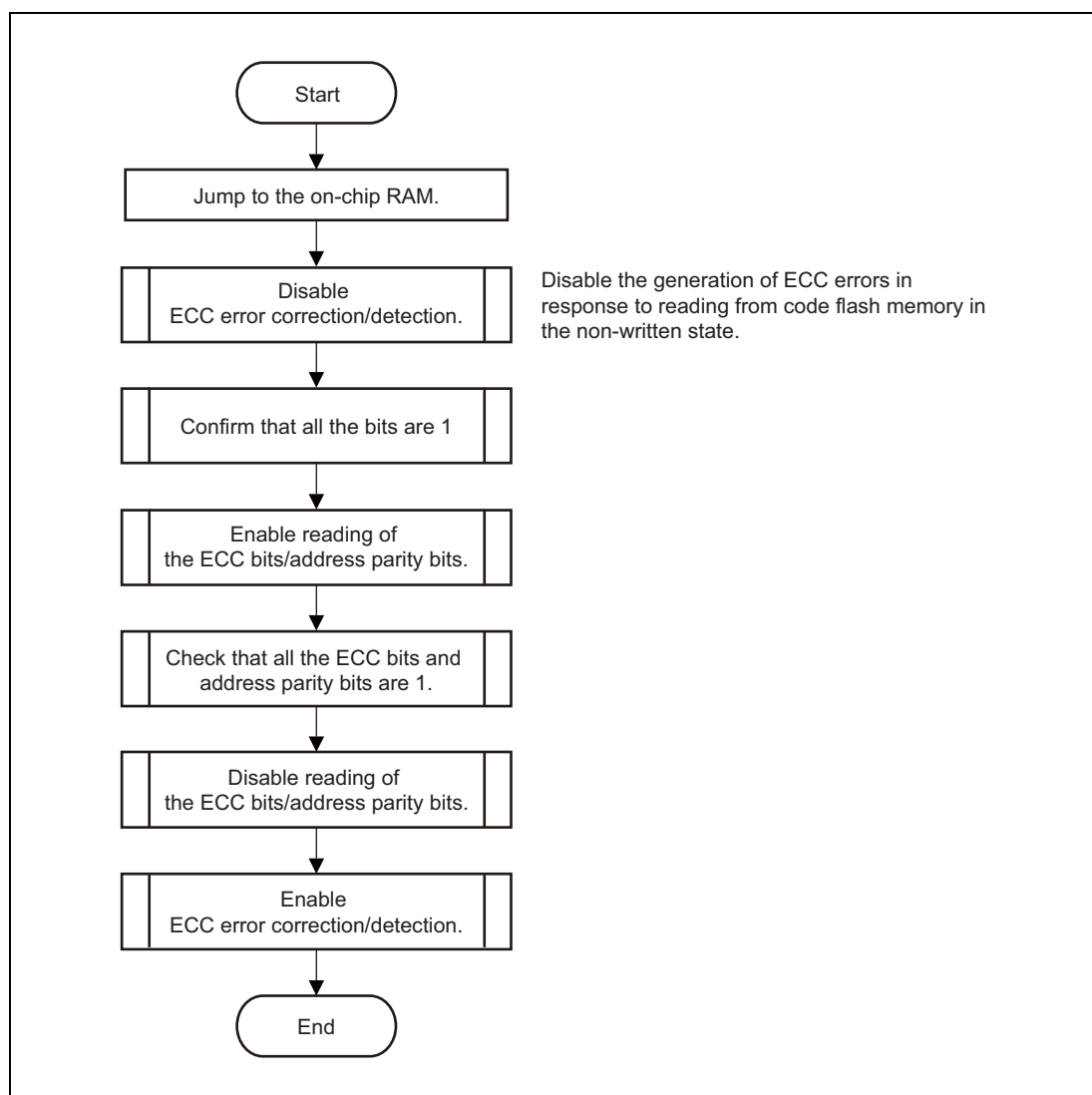


Figure 8.2 Blank Checking of Code Flash Memory

Section 9 Usage Notes

(1) Reading from area where program/erasure is suspended

The data stored in the flash memory area where program/erasure is suspended is undefined. To avoid the malfunction caused by reading undefined data, do not make an attempt to fetch the instruction or read the data in the area where program/erasure is suspended.

(2) Prohibition of additional write

Writing the same area more than once is prohibited. To write again the flash memory area where data has already been written to, be sure to erase the corresponding area in advance.

(3) Reset during program/erasure

To generate a reset by the $\overline{\text{RESET}}$ pin during program/erasure, release the reset after the reset input period of at least the minimum low-level width of the reset pulse input signal, within the operating voltage range specified by electrical characteristics.

(4) Interrupt/exception vector allocation during program/erasure

Generation of an interrupt or exception during programming or erasure may lead to fetching from a vector in code flash memory. If the BGO function is not available, set the address for vector fetching to an area other than code flash memory. For changing the address for fetching from the vector, see *the sections on the CPU system and interrupts in the User's Manual: Hardware*.

(5) Abnormal end during program/erasure

Verification of the write or erasure state cannot be provided for a flash memory area where write or erasure is abnormally ended and data is undefined, for example due to external input or power off. For the area where write or erasure is abnormally ended, the blank check function cannot check the erasure state correctly. Before using the corresponding area again, completely erase the area by the erasure processing.

When programming/erasing the code flash memory is not ended normally, the lock bit may be enabled. In this case, erase the corresponding block and erase the lock bit while lock bits are disabled.

(6) Prohibition during program/erasure/blank check

Do not perform the following operations during program/erasure/blank check.

- Set the power supply voltage outside the operating voltage range.
- Update the value of FHVE15 and FHVE3.

(7) Update of BFASLR register

When switching to the code flash area by setting the BFASLR register, the switching of the area needs to be synchronized with the processing before and after the switch. This synchronization processing is performed as described in [1] to [3] below.

- [1] Synchronization processing when updating the BFASLR register:
To synchronize the BFASLR register update with the processing before and after the update, execute "BFASLR register dummy read + SYNC instruction" between when the BFASLR register is updated and when a read instruction (LD.W, etc.) is issued to the code flash or a BFASLR control area*¹.
- [2] Synchronization processing before switching to the code flash user area or extended user area:
To switch to the code flash area after a BFASLR control area*¹ has finished being loaded, execute a SYNC instruction after the last read instruction (LD.W, etc.) for the BFASLR control area*¹ has finished executing, and then update the BFASLR register as described in [1] above.
- [3] Synchronization processing after switching to the code flash user area or extended user area:
To execute a fetch from the code flash area, execute "BFASLR register dummy read + SYNC instruction + SYNC instruction" between when the BFASLR register is updated and when a code flash instruction is executed. Also, after switching to the code flash area, clear the instruction cache and data buffer, and then enable them, if required.

Note 1. The BFASLR control area refers to the configuration setting area and OTP setting area.

(8) Maintenance of coherency after the code flash memory is overwritten

When executing an instruction for the code flash memory after the code flash memory area is overwritten, clear the instruction cache and the data buffer, in order to maintain coherency (see *Usage Notes in the section of the CPU system in the User's Manual: Hardware*).

Section 10 Electrical Specifications

This section explains the electrical characteristics when the hardware interface is used with the self-programming described in this manual.

Note that these electrical characteristics differ from those of when the serial programming is used.

10.1 Code Flash Characteristics

Table 10.1 Suspend/Resume/Forced Stop

Conditions: See 37.1.1.1, *Common conditions in the User's Manual Hardware*.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Suspend latency during programming	t_{SPD}	—	—	—	120	μs
Programming resume time ^{*1}	t_{RPT}	—	—	—	50	μs
Suspend latency during erasure	t_{SESD1}	Priority on suspend The 1st suspend for the same pulse	—	—	120	μs
	t_{SESD2}	Priority on suspend The 2nd suspend for the same pulse	—	—	1.7	ms
	t_{SEED}	Priority on erasure	—	—	1.7	ms
Erasure resume time ^{*1}	t_{REST1}	Priority on suspend Resume after the 1st suspend for the same pulse	—	—	1.7	ms
	t_{REST2}	Priority on suspend Resume after the 2nd suspend for the same pulse	—	—	80	μs
	t_{REET}	Priority on erasure	—	—	80	μs
Forced stop command latency	t_{FD}	—	—	—	20	μs

Note 1. The time taken for resumption includes an overhead for the resumption of programming or erasure. In suspension-priority mode, the time for reapplication of the erasing pulse that was cut off at the time of suspension is also required.
Resume time is defined as time added by programming or erasing due to those sources.

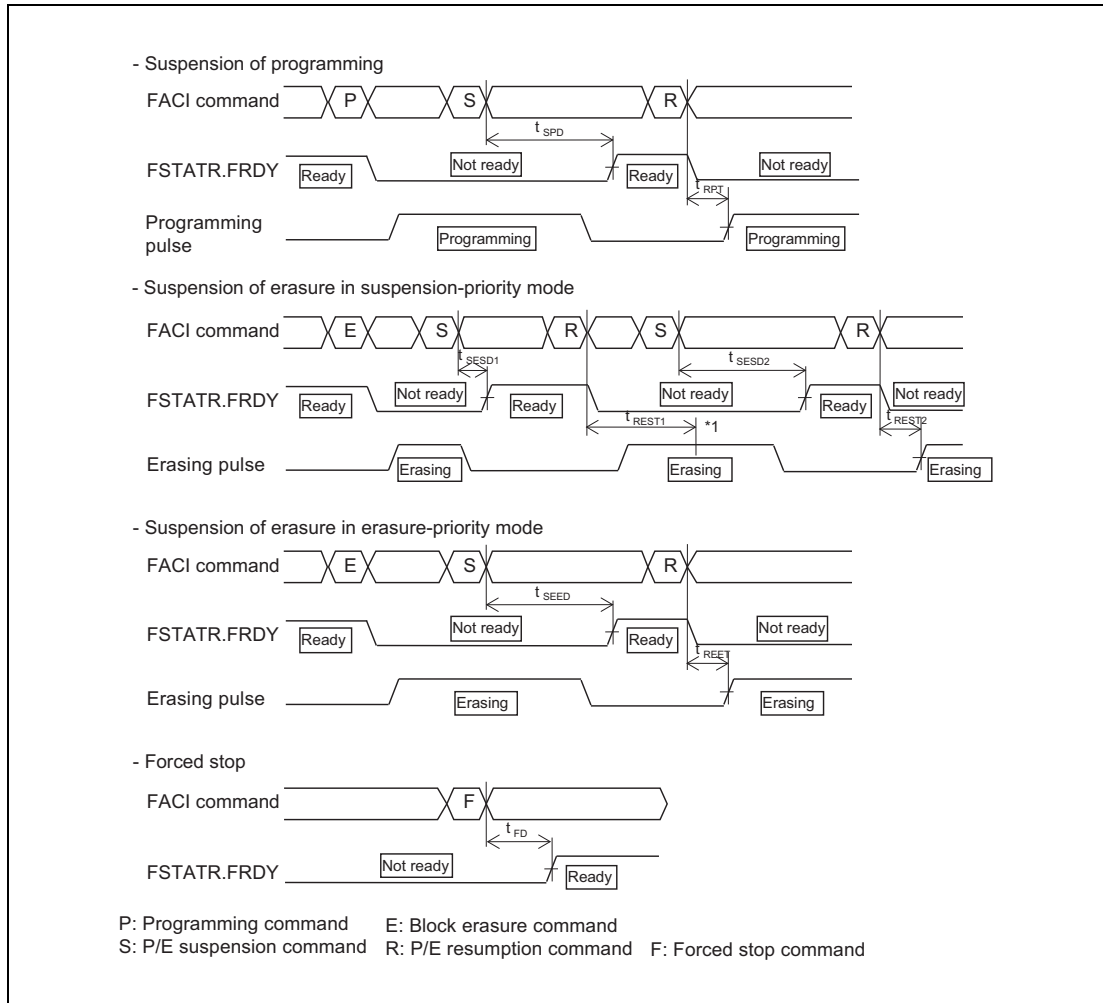


Figure 10.1 Timing of Suspend/Resume/Forced Stop

Note 1. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

10.2 Data Flash Characteristics

Table 10.2 Suspend/Resume/Forced Stop

Conditions: See 37.1.1.1, *Common conditions in the User's Manual Hardware*.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Suspend latency during programming	t_{SPD}	—	—	—	120	μs
Programming resume time ^{*1}	t_{RPT}	—	—	—	50	μs
Suspend latency during erasure	t_{SESD1}	Priority on suspend The 1st suspend for the same pulse	—	—	120	μs
	t_{SESD2}	Priority on suspend The 2nd suspend for the same pulse	—	—	300	μs
	t_{SEED}	Priority on erasure	—	—	300	μs
Erasure resume time ^{*1}	t_{REST1}	Priority on suspend Resume after the 1st suspend for the same pulse	—	—	300	μs
	t_{REST2}	Priority on suspend Resume after the 2nd suspend for the same pulse	—	—	70	μs
	t_{REET}	Priority on erasure	—	—	70	μs
Forced stop command latency	t_{FD}	—	—	—	20	μs

Note 1. The time taken for resumption includes an overhead for the resumption of programming or erasure. In suspension-priority mode, the time for reapplication of the erasing pulse that was cut off at the time of suspension is also required.
Resume time is defined as time added by programming or erasing due to those sources.

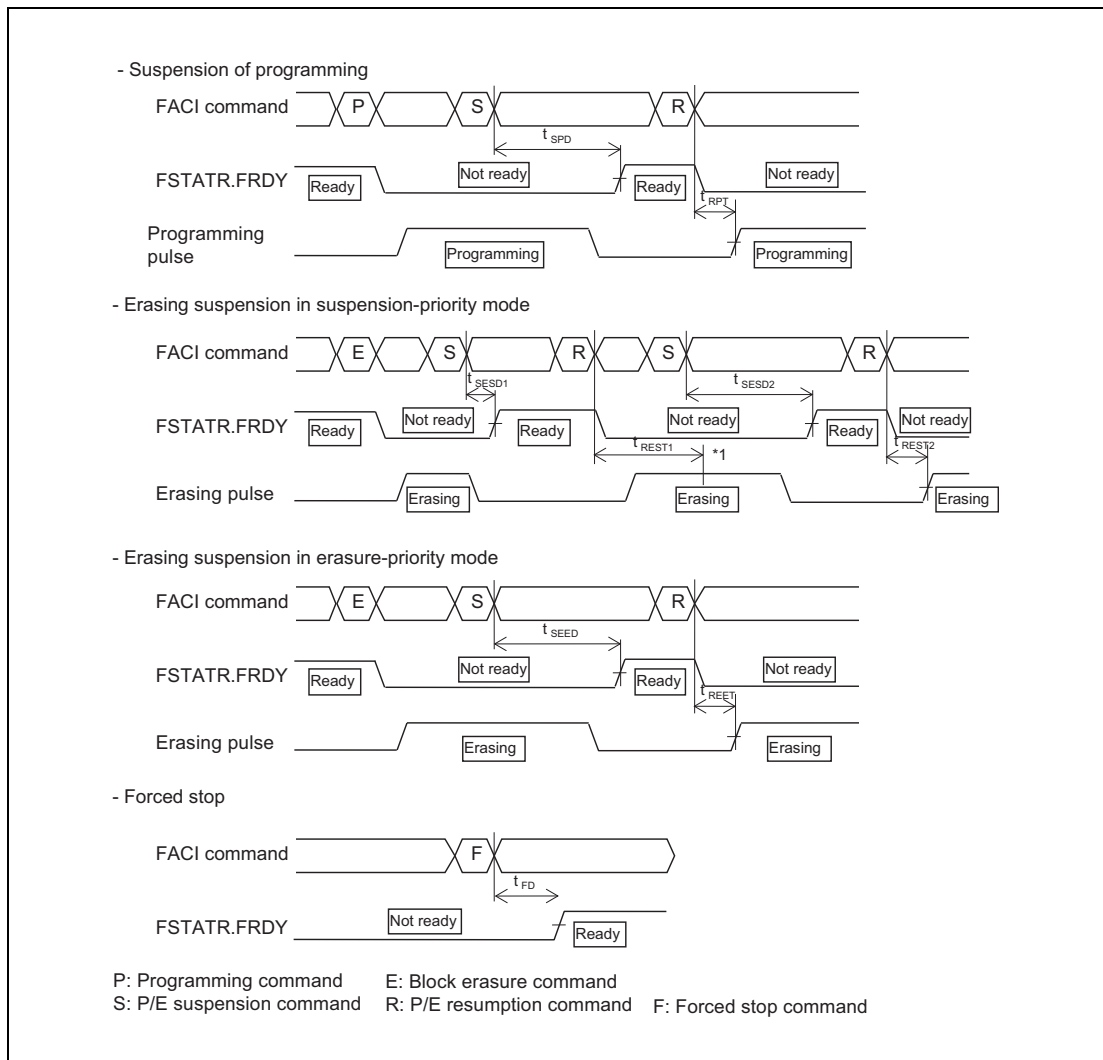


Figure 10.2 Timing of Suspend/Resume/Forced Stop

Note 1. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

RH850/P1M-E User's Manual: Hardware Interface

Publication Date: Rev.0.50 Mar 18, 2016
Rev.1.20 Mar 23, 2018

Published by: Renesas Electronics Corporation

**SALES OFFICES****Renesas Electronics Corporation**<http://www.renesas.com>Refer to "<http://www.renesas.com/>" for the latest and detailed information.**Renesas Electronics America Inc.**1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351**Renesas Electronics Canada Limited**9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004**Renesas Electronics Europe Limited**Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804**Renesas Electronics Europe GmbH**Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327**Renesas Electronics (China) Co., Ltd.**Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679**Renesas Electronics (Shanghai) Co., Ltd.**Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999**Renesas Electronics Hong Kong Limited**Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022**Renesas Electronics Taiwan Co., Ltd.**13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670**Renesas Electronics Singapore Pte. Ltd.**80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300**Renesas Electronics Malaysia Sdn.Bhd.**Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510**Renesas Electronics India Pvt. Ltd.**No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777**Renesas Electronics Korea Co., Ltd.**17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

RH850/P1M-E
Flash Memory