User's Manual

32

RH850/F1KH, RH850/F1KM, RH850/F1K

Flash Memory

User's Manual: Hardware Interface

Renesas microcontroller

Renesas Electronics
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Notes for CMOS devices

(1) Voltage application waveform at input pin:

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) Handling of unused input pins:

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) Precaution against ESD:

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) Status before initialization:

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) Power ON/OFF sequence:

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) Input of signal during power off state:

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Table of Contents

Section 1 Features

The features of the flash memory are described below. See *the RH850/F1K User's Manual: Hardware* or *the RH850/F1KH, RH850/F1KM User's Manual: Hardware* for information on the capacity, block configuration, and addresses of the flash memory in a given product.

Flash Memory Programming/Erasure

A dedicated sequencer for the flash memory (flash sequencer) executes programming and erasure via the P-Bus. Directly controlling the flash sequencer can provide better response and performance than using the code flash library and data flash library. The flash sequencer also supports the suspension and resumption of programming and erasure, and background operations (BGO)*[1].

Note 1. See *Section 37.7.2, Background Operation* of *the RH850/F1K User's Manual: Hardware* or *Section 44.7.2, Background Operation* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

Security Functions

The flash memory incorporates hardware functions to prevent illicit tampering.

Safety Functions

The flash memory incorporates hardware functions to prevent erroneous writing.

Interrupts

The flash memory supports an interrupt (INTFLENDNM) to indicate completion of processing by the flash sequencer (i.e., the FSTATR.FRDY bit has been set to 1) and an error interrupt (INTFLERR) to indicate erroneous operations.

DMA

The data flash memory can be programmed by using DMA.

Section 2 Module Configuration

Modules related to the flash memory are configured as shown in **Figure 2.1**. The flash sequencer consists of the FCU and FACI. The FCU executes basic control of overwriting the flash memory. The FACI receives FACI commands via the P-Bus and controls FCU operations accordingly.

The FACI transfers the data from flash memory to the option byte storage registers and the ID control section at the time of release from the reset state or wakeup from DeepSTOP mode (FACI reset transfer). The ID control section compares the ID transferred from the flash memory with the value in the SELFID0 to SELFID3 registers.

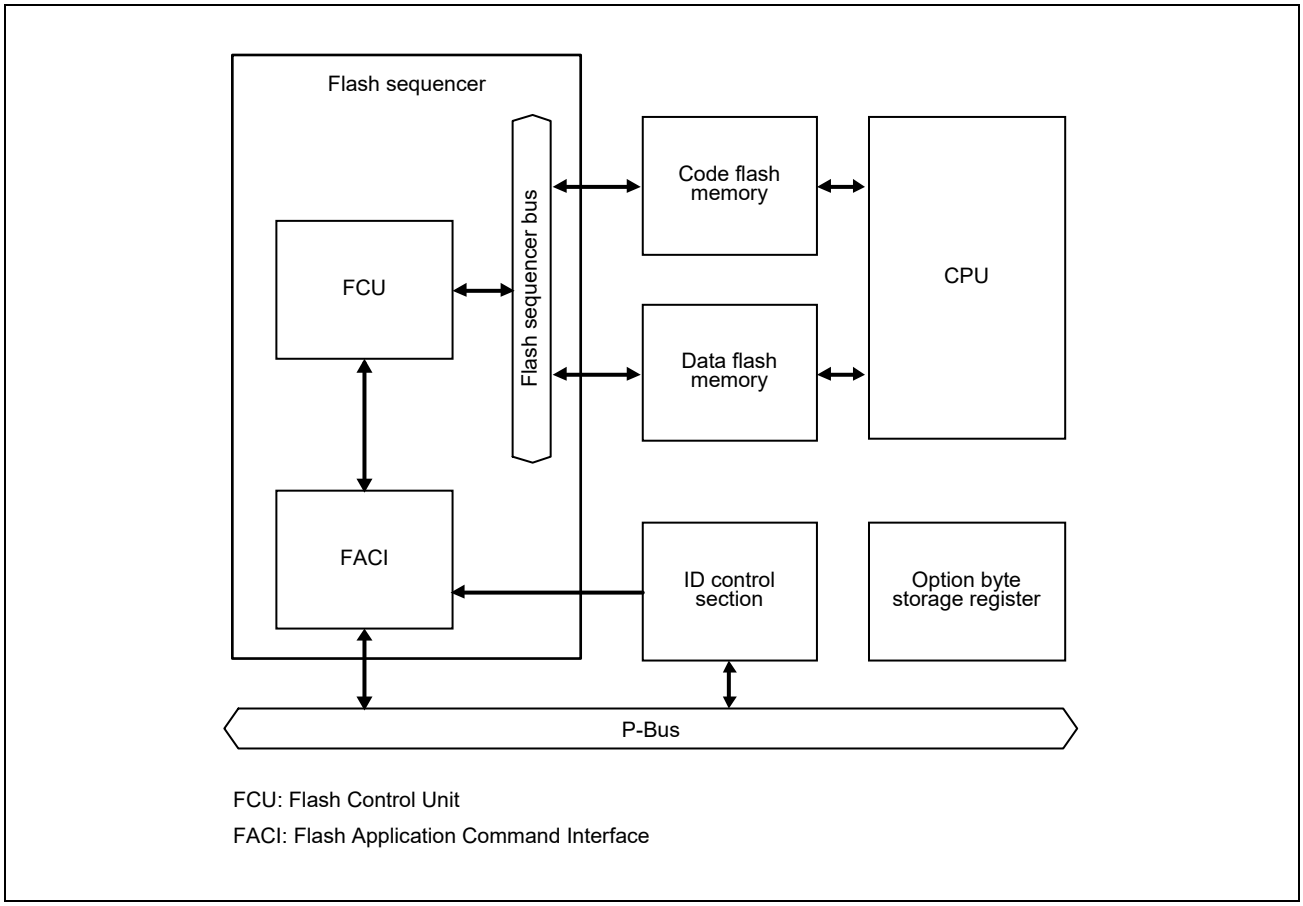


Figure 2.1 Configuration of Flash Memory Related Modules

Section 3 Address Map

Using the hardware interface with the flash memory requires access to the areas listed in **Table 3.1**. When reading the configuration setting area or OTP setting area, set the BFAA bit of the BFASELR register to 1.

Table 3.1 Information on the Hardware Interface Area

Area	Address	Capacity	Peripheral Group
Area containing the various hardware registers	*2	*2	1*3
FACI command-issuing area	FFA2 0000_H	4 bytes	1
Configuration setting area*1	FF30 0040_H to FF30 $008F_H$	80 bytes	4 (RH850/F1KM-S2, F1KM-S4, F1KH-D8), 2 (RH850/F1KM-S1, F1K)
OTP setting area*1	FF38 0040_H to FF38 $009F_H$	96 bytes	4 (RH850/F1KM-S2, F1KM-S4, F1KH-D8), 2 (RH850/F1KM-S1, F1K)

Note 1. Accessible when the BFAA bit in the BFASELR register is set to 1.

Note 2. See **Section 4, Registers**.

Note 3. The peripheral group of BFASELR and FBUFCCTL is “2”.

For information on the addresses of the flash memory, etc., see *the RH850/F1K User’s Manual: Hardware* or *the RH850/F1KH, RH850/F1KM User’s Manual: Hardware*.

Section 4 Registers

Using the hardware interface with the flash memory requires access to more registers than when using the code flash library and data flash library. This section provides information on the additional registers to which access is required. For registers that are not specifically mentioned, reset them to their initial states. For the list of registers, see **Appendix, List of Flash Memory Related Registers**.

For information on the option bytes, see *the RH850/F1K User's Manual: Hardware* or *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

4.1 FPMON — Flash Pin Monitor Register

FPMON indicates the state of the FLMD0 pin.

Access: This register is a read-only register that can be read in 8-bit units.

Address: FFA1 0000$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	FWE	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.1 FPMON Register Contents

Bit Position	Bit Name	Function
7	FWE	Flash Write Enable Monitors the level on the FLMD0 pin. The value of the FWE bit indicates whether transitions to the code flash P/E mode are enabled or disabled. 0: Transitions to the code flash P/E mode are disabled. 1: Transitions to the code flash P/E mode are enabled.
6 to 0	Reserved	When read, the value after reset is returned.

4.2 FASTAT — Flash Access Status Register

FASTAT indicates whether a code flash memory or data flash memory access violation has occurred. If any of the CFAE, CMDLK, and DFAE bits in FASTAT is set to 1, the flash sequencer enters the command-locked state. To release it from the command-locked state, a status clear or forced stop command must be issued to the FACI after setting the CFAE and DFAE bits in FASTAT to 0.

Access: This register can be read or written in 8-bit units.

Address: FFA1 0010$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	CFAE	—	—	CMDLK	DFAE	—	—	ECRCT
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W*1	R	R	R	R/W*1	R	R	R

Note 1. Only 0 can be written to clear a flag after 1 is read.

Table 4.2 FASTAT Register Contents (1/2)

Bit Position	Bit Name	Function
7	CFAE	Code Flash Memory Access Violation Indicates whether a code flash memory access violation has occurred. If this bit is set to 1, the ILGLERR bit in FSTATR is set to 1 and the flash sequencer enters command-locked state. 0: No code flash memory access violation has occurred. 1: A code flash memory access violation has occurred. [Setting Condition] • An FACI command is issued when the setting of bits 23 to 0 in FSADDR is outside the range of valid addresses*1 in code flash P/E mode. [Clearing Condition] • 0 is written after reading 1 from this bit.
6, 5	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
4	CMDLK	Command Lock Indicates that the flash sequencer is in the command-locked state. 0: The flash sequencer is not in the command-locked state. 1: The flash sequencer is in the command-locked state. [Setting Condition] • The flash sequencer detects an error and enters the command-locked state. [Clearing Condition] • The flash sequencer starts processing of the status clear or forced stop command when the CFAE and DFAE bits in the FASTAT register are set to 0.
3	DFAE	Data Flash Memory Access Violation Indicates whether a data flash memory access violation has occurred. If this bit is set to 1, the ILGLERR bit in FSTATR is set to 1 and the flash sequencer enters the command-locked state. 0: No data flash memory access violation has occurred. 1: A data flash memory access violation has occurred. [Setting Condition] • An FACI command is issued when the setting of bits 18 to 0 in FSADDR is outside the range of valid addresses*1 in data flash P/E mode. [Clearing Condition] • 0 is written after reading 1 from this bit.
2, 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

Table 4.2 FASTAT Register Contents (2/2)

Bit Position	Bit Name	Function
0	ECRCT	Error Correction Indicates that a 1-bit error was corrected while the flash memory area was being read by the flash sequencer (with parameters for configuration setting, programming, or OTP setting specified). 0: A 1-bit error was not corrected. 1: A 1-bit error was corrected. [Clearing conditions] • The flash sequencer starts processing of the status clear or forced stop command while the CFGCRCT, TBLCRCT, or OTPCRCT bit in FSTATR is 1.

Note 1. For the range of valid addresses when issuing an FACI command, see **Section 4.5, FSADDR — FACI Command Start Address Register** and **Section 4.6, FEADDR — FACI Command End Address Register**.

4.3 FAEINT — Flash Sequencer End Error Interrupt Enable Register

FAEINT enables or disables generation of a flash access error (FLERR) interrupt request.

Access: This register can be read or written in 8-bit units.

Address: FFA1 0014$_H$

Value after reset: 99$_H$

Bit	7	6	5	4	3	2	1	0
	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	ECRCTIE
Value after reset	1	0	0	1	1	0	0	1
R/W	R/W	R	R	R/W	R/W	R	R	R/W

Table 4.3 FAEINT Register Contents

Bit Position	Bit Name	Function
7	CFAEIE	Code Flash Memory Access Violation Interrupt Enable Enables or disables generation of an FLERR interrupt request when a code flash memory access violation occurs leading to the CFAE bit in FASTAT being set to 1. 0: An FLERR interrupt request is not generated when FASTAT.CFAE = 1. 1: An FLERR interrupt request is generated when FASTAT.CFAE = 1.
6, 5	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
4	CMDLKIE	Command Lock Interrupt Enable Enables or disables generation of an FLERR interrupt request when the flash sequencer enters the command-locked state leading to the CMDLK bit in FASTAT being set to 1. 0: An FLERR interrupt request is not generated when FASTAT.CMDLK = 1. 1: An FLERR interrupt request is generated when FASTAT.CMDLK = 1.
3	DFAEIE	Data Flash Memory Access Violation Interrupt Enable Enables or disables generation of an FLERR interrupt request when a data flash memory access violation occurs leading to the DFAE bit in FASTAT being set to 1. 0: An FLERR interrupt request is not generated when FASTAT.DFAE = 1. 1: An FLERR interrupt request is generated when FASTAT.DFAE = 1.
2, 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	ECRCTIE	Error Correction Interrupt Enable Enables or disables generation of an FLERR interrupt request when a 1-bit error is corrected while the flash memory area is being read by the flash sequencer (with parameters for configuration setting, programming, or OTP setting specified) leading to the ECRCT bit in FASTAT being set to 1. 0: An FLERR interrupt request is not generated when FASTAT.ECRCT = 1. 1: An FLERR interrupt request is generated when FASTAT.ECRCT = 1.

4.4 FAREASELC — Code Flash Memory Area Select Register

FAREASELC selects the code flash memory area that is to be used for handling commands by the FACI.

When the SUINIT bit in the FSUINITR register is set to 1, FAREASELC is initialized. This register is also initialized by a reset.

Access: This register can be read or written in 16-bit units.

Address: FFA1 0020_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	CFAS	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R/W *2,*3	R

Note 1. Written data is not stored in this bit. Read data is always 0.

Note 2. This bit can be written only when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit is 0 is ignored.

Note 3. Writing to this bit is enabled only when $3B_H$ is written to the KEY[7:0] bits.

Table 4.4 FAREASELC Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits control permission and prohibition of writing to the CFAS bit.
7 to 2	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
1	CFAS	Code Flash Memory Area Select Selects the area of code flash memory that is to be used for handling commands issued from the FACI. 0: User area is selected. 1: Extended user area is selected.
0	Reserved	When read, the value after reset is returned. When writing, write the value after reset.

4.5 FSADDR — FACI Command Start Address Register

FSADDR specifies the address where the area used for command processing starts when the FACI command for programming, DMA programming, block erasure, blank checking, configuration setting, lock-bit programming, lock-bit reading, or OTP setting is issued.

The FSADDR value is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Access: This register can be read or written in 32-bit units.

Address: FFA1 0030$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FSADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FSADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R

Note 1. This bit can be written only when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit is 0 is ignored.

Table 4.5 FSADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	FSADDR[31:0]	Start Address for FACI Command Processing These bits specify the start address for FACI command processing. Bits 31 to 24 are ignored in FACI command processing for the code flash memory. Bits 31 to 19 are ignored in FACI command processing for the data flash memory. Bits corresponding to address bits below the corresponding boundary listed below are also ignored.

Command	Address Boundary
Programming (code flash memory):	256-byte
Programming (data flash memory):	4-byte
DMA programming:	4-byte
Block erase (code flash memory):	8 KB or 32 KB
Block erase (data flash memory):	64-byte
Blank check:	4-byte
Configuration setting:	16-byte
Lock-bit programming:	8 KB or 32 KB
Lock-bit read:	8 KB or 32 KB
OTP setting:	16-byte

The following settings cannot be made in code flash P/E mode. An error occurs if an FACI command is issued with the following settings:

(1) The setting of the CFAS bit in the FAREASELC register is 0 and the setting of bits 23 to 0 in the FSADDR register is:
- 40 0000_H to 7F $FFFF_H$ and C0 0000_H to FF $FFFF_H$ (RH850/F1KH-D8)
- 40 0000_H to FF $FFFF_H$ (RH850/F1KM-S4)
- 20 0000_H to FF $FFFF_H$ (RH850/F1KM-S2)
- 20 0000_H to FF $FFFF_H$ (RH850/F1K)
- 10 0000_H to FF $FFFF_H$ (RH850/F1KM-S1)

(2) The setting of the CFAS bit in the FAREASELC register is 1 and the setting of bits 23 to 0 in the FSADDR register is:
- 00 8000_H to FF $FFFF_H$

In addition, the following settings cannot be made in data flash P/E mode. An error occurs if an FACI command is issued with the following settings:

(1) The setting of bits 18 to 0 in the FSADDR register is:
- 4 0000_H to 7 $FFFF_H$ (RH850/F1KH-D8)
- 2 0000_H to 7 $FFFF_H$ (RH850/F1KM-S4, RH850/F1KM-S2)
- 1 0000_H to 7 $FFFF_H$ (RH850/F1K, RH850/F1KM-S1)

(2) The setting of bits 18 to 0 in the FSADDR register is:
- 0 0000_H to 0 $003F_H$ or 0 0100_H to 7 $FFFF_H$ when issuing the configuration setting command

(3) The setting of bits 18 to 0 in the FSADDR register is:
- 0 0000_H to 0 $003F_H$ or 0 $00A0_H$ to 7 $FFFF_H$ when issuing the OTP setting command

4.6 FEADDR — FACI Command End Address Register

FEADDR specifies the address where the area used for blank check command processing ends. When incremental mode is selected as the addressing mode for blank checking (i.e. when FBCCNT.BCDIR = 0), the address specified in FEADDR should be larger than the address in FSADDR. Conversely, the address in FEADDR should be smaller than the address in FSADDR when decremental mode is selected as the addressing mode for blank checking (i.e. when FBCCNT.BCDIR = 1). If the settings of BCDIR, FSADDR, and FEADDR are inconsistent with the above rules, the flash sequencer enters the command-locked state (see **Section 8.3, Error Protection**).

The value of FEADDR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Access: This register can be read or written in 32-bit units.

Address: FFA1 0034$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FEADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FEADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R

Note 1. This bit can be written only when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit is 0 is ignored.

Table 4.6 FEADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	FEADDR[31:0]	End Address for FACI Command Processing These bits specify the end address for blank check command processing. Bits 31 to 19, 1 and 0 are ignored in command processing. When the setting of bits 18 to 0 in the FEADDR register is as follows, an error occurs if the blank checking command is issued. • 4 0000$_H$ to 7 FFFF$_H$ (RH850/F1KH-D8) • 2 0000$_H$ to 7 FFFF$_H$ (RH850/F1KM-S4, RH850/F1KM-S2) • 1 0000$_H$ to 7 FFFF$_H$ (RH850/F1K, RH850/F1KM-S1)

4.7 FSTATR — Flash Status Register

FSTATR indicates the state of the flash sequencer.

Access: FSTATR register is a read-only register that can be read in 32-bit units.

FSTATRL, FSTATRH registers are a read-only register that can be read in 16-bit units.

FSTATRLL, FSTATRLH, FSTATRHL registers are a read-only register that can be read in 8-bit units.

Address: FFA1 0080H (FSTATR)

FFA1 0080H (FSTATRL)

FFA1 0080H (FSTATRLL)

FFA1 0081H (FSTATRLH)

FFA1 0082H (FSTATRH)

FFA1 0082H (FSTATRHL)

Value after reset: 0000 8000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	EBFULL	OTPDTCT	OTPCRCT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	—	CFGDTCT	CFGCRCT	TBLDTCT	TBLCRCT	—	—
Value after reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.7 FSTATR Register Contents (1/4)

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is returned.
18	EBFULL	FDMYECC Buffer Full Indicates the state of the FDMYECC buffer when issuing a programming command. The FACI incorporates a buffer for FDMYECC (ECC buffer). When FDMYECC is written to while the ECC buffer is full, the FACI inserts a wait cycle in the P-Bus. 0: The ECC buffer is not full. 1: The ECC buffer is full. [Setting condition] • The ECC buffer becomes full while programming commands are being issued. [Clearing condition] • The vacant ECC buffer is generated.
17	OTPDTCT	2-Bit Error Detection Monitor (OTP Setting) Indicates that a 2-bit error was detected while reading the OTP value. The FACI reads the OTP value during programming, block erasure, lock-bit programming, lock-bit reading, and OTP setting of the code flash memory. When this bit is 1, the flash sequencer is placed in the command-locked state. 0: A 2-bit error was not detected. 1: A 2-bit error was detected. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.

Table 4.7 FSTATR Register Contents (2/4)

Bit Position	Bit Name	Function
16	OTPCRCT	1-Bit Error Correction Monitor (OTP Setting) Indicates that a 1-bit error was detected and corrected while reading the OTP value. The FACI reads the OTP value during programming, block erasure, lock-bit programming, lock-bit reading, and OTP setting of the code flash memory. When this bit is 1, the flash sequencer continues command processing and does not enter the command-locked state. 0: A 1-bit error was not corrected. 1: A 1-bit error was corrected. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.
15	FRDY	Flash Ready Indicates the command processing state of the flash sequencer. 0: Processing of the programming, DMA programming, block erase, P/E suspend, P/E resume, forced stop, blank check, configuration setting, lock-bit programming, lock-bit read, or OTP setting command is in progress. 1: None of the above is in progress. [Setting Conditions] • The flash sequencer completes processing. • The flash sequencer receives a P/E suspend command and suspends programming of the flash memory. • The flash sequencer has received a forced stop command and ended command processing. [Clearing Conditions] • When the flash sequencer has received an FACI command • During programming, DMA programming, configuration setting, or OTP setting, when the first write access to the FACI command-issuing area has occurred. • For other commands, when the last access to the FACI command-issuing area has occurred.
14	ILGLERR	Illegal Command Error Indicates that the flash sequencer has detected an illegal FACI command or illegal flash memory access. When this bit is 1, the flash sequencer is placed in the command-locked state. 0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access. 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access [Setting conditions] • The flash sequencer has detected an illegal command. • The flash sequencer has detected an illegal flash memory access. • The setting of FENTRYR is invalid. [Clearing condition] • The flash sequencer starts processing the status clear or forced stop command while the CFAE and DFAE bits of the FASTAT register are set to 0. The ILGLERR bit is set to 1 if processing of the status clear or forced stop command is completed while the CFAE and DFAE bits of the FASTAT register are set to 1. The ILGLERR bit is temporarily set to 0 while the forced stop command is being processed, but it is set back to 1 after the CFAE and DFAE bits are detected as 1 on completion of the command processing.
13	ERSERR	Erasure Error Indicates the result of erasure of the flash memory. When this bit is 1, the flash sequencer is placed in the command-locked state. 0: Erasure processing has completed successfully. 1: An error occurred during erasure. [Setting conditions] • An error occurred during erasure. • A block erase command is issued for an area where the lock bit is set for protection. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.

Table 4.7 FSTATR Register Contents (3/4)

Bit Position	Bit Name	Function
12	PRGERR	Programming Error Indicates the result of programming the flash memory. When this bit is 1, the flash sequencer is placed in the command-locked state. 0: Programming has completed successfully. 1: An error occurred during programming. [Setting conditions] • An error occurred during programming. • A programming or lock-bit programming command is issued for an area where the lock bit is set for protection. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.
11	SUSRDY	Suspend Ready Indicates whether the flash sequencer can receive a P/E suspend command. 0: The flash sequencer cannot receive P/E suspend commands. 1: The flash sequencer can receive P/E suspend commands. [Setting condition] • After starting programming or erasure, the flash sequencer enters a state in which P/E suspend commands can be received. [Clearing conditions] • Reception of the P/E suspend command or forced stop command by the flash sequencer (after write access to the FACI command-issuing area is completed) • The flash sequencer enters the command-locked state during programming or erasure. • Programming or erasure is completed.
10	DBFULL	Data Buffer Full Indicates the state of the data buffer when a programming command is issued. The FACI incorporates a buffer for write data (data buffer). When data for writing to the flash memory are issued to the FACI command-issuing area while the data buffer is full, the FACI inserts a wait cycle in the P-Bus. 0: The data buffer is not full. 1: The data buffer is full. [Setting condition] • The data buffer becomes full while programming commands are being issued. [Clearing condition] • The vacant data buffer is generated.
9	ERSSPD	Erasure-Suspended Status Indicates that the flash sequencer is in the erasure suspension processing state or erasure-suspended state. 0: The flash sequencer is in a state other than those corresponding to the “1” setting. 1: The flash sequencer is in the erasure suspension processing state or erasure-suspended state. [Setting condition] • The flash sequencer starts processing in response to an erasure suspend command. [Clearing conditions] • Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is completed) • The flash sequencer starts processing a forced stop command.

Table 4.7 FSTATR Register Contents (4/4)

Bit Position	Bit Name	Function
8	PRGSPD	Programming-Suspended Status Indicates that the flash sequencer is in the programming suspension processing state or programming suspended state. 0: The flash sequencer is in a state other than those corresponding to the “1” setting. 1: The flash sequencer is in the programming suspension processing state or programming-suspended state. [Setting condition] • The flash sequencer starts processing in response to a programming suspend command. [Clearing conditions] • Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is completed) • The flash sequencer starts processing a forced stop command.
7, 6	Reserved	When read, the value after reset is returned.
5	CFGDTCT	2-Bit Error Detection Monitor (Configuration Setting) Indicates that a 2-bit error was detected while reading the configuration setting value. The FACI reads the configuration setting value during configuration setting. When this bit is 1, the flash sequencer is placed in the command-locked state. 0: A 2-bit error was not detected. 1: A 2-bit error was detected. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.
4	CFGCRCT	1-Bit Error Correction Monitor (Configuration Setting) Indicates that a 1-bit error was detected and corrected while reading the configuration setting value. The FACI reads the configuration setting value during configuration setting. When this bit is 1, the flash sequencer continues command processing and does not enter the command-locked state. 0: A 1-bit error was not corrected. 1: A 1-bit error was corrected. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.
3	TBLDTCT	2-Bit Error Detection Monitor (Programming Parameter Table) Indicates that a 2-bit error was detected during reading the programming parameter table. The FACI reads the programming parameter table during programming, DMA programming, block erasure, blank checking, configuration setting, lock-bit programming and OTP setting of the flash memory. When this bit is 1, the flash sequencer is placed in the command-locked state. 0: A 2-bit error was not detected. 1: A 2-bit error was detected. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.
2	TBLCRCT	1-Bit Error Correction Monitor (Programming Parameter Table) Indicates that a 1-bit error was detected and corrected while reading the programming parameter table. The FACI reads the programming parameter table in programming, DMA programming, block erasure, blank checking, configuration setting, lock-bit programming and OTP setting of the flash memory. When this bit is 1, the flash sequencer does not enter the command-locked state. 0: A 1-bit error was not corrected. 1: A 1-bit error was corrected. [Clearing condition] • The flash sequencer starts processing a status clear or forced stop command.
1, 0	Reserved	When read, the value after reset is returned.

4.8 FENTRYR — Flash P/E Mode Entry Register

FENTRYR specifies code flash P/E mode and data flash P/E mode. To specify code flash P/E mode or data flash P/E mode so that the flash sequencer can receive FACI commands, set either the FENTRYD or FENTRYC bit to 1 to place the flash sequencer in P/E mode.

Setting the FENTRYD and FENTRYC bits simultaneously in this register leads to setting of the ILGLERR bit in the FSTATR register to 1 and the flash sequencer is placed in the command-locked state.

The FENTRY value is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Access: This register can be read or written in 16-bit units.

Address: FFA1 0084$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W *2,*3	R	R	R	R	R	R	R/W *2,*3,*4

Note 1. Written data is not stored in this bit. Read data is always 0.

Note 2. This bit can be written only when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit is 0 is ignored.

Note 3. Writing to this bit is enabled only when AA$_H$ is written to the KEY[7:0] bits.

Note 4. Writing to this bit is enabled only while the FWE bit in the FPMON register is 1.

Table 4.8 FENTRYR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits control permission and prohibition of writing to the FENTRYD and FENTRYC bits.
7	FENTRYD	Data Flash P/E Mode Entry This bit specifies the P/E mode for data flash memory. 0: Data flash is in read mode. 1: Data flash is in P/E mode. [Setting condition] • 1 is written to the FENTRYD bit while writing to FENTRYR is enabled and FENTRYR is 0000$_H$. [Clearing conditions] • A value other than AA$_H$ is written to the KEY[7:0] bits in FENTRYR while the FRDY bit is 1. • 0 is written to FENTRYD while writing to FENTRYR is enabled. • FENTRYR is written to while FENTRYR is not 0000$_H$ and writing to FENTRYR is enabled.
6 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	FENTRYC	Code Flash P/E Mode Entry This bit specifies the P/E mode for code flash memory. 0: Code flash is in read mode. 1: Code flash is in P/E mode. [Setting condition] • 1 is written to FENTRYC while writing to FENTRYR is enabled and FENTRYR is 0000$_H$. [Clearing conditions] • A value other than AA$_H$ is written to the KEY[7:0] bits in FENTRYR while the FRDY bit is 1. • The FWE bit in FPMON is set to 0 while the setting of the FRDY bit is 1. • 0 is written to FENTRYC while writing to FENTRYR is enabled. • FENTRYR is written to while FENTRYR is not 0000$_H$ and writing to FENTRYR is enabled.

4.9 FPROTR — Code Flash Protect Register

FPROTR enables or disables protection by the lock bits of the code flash memory against programming and erasure. The FPROTR value is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Access: This register can be read or written in 16-bit units.

Address: FFA1 0088$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	FPROTCN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R	R/W*2

Note 1. Written data is not stored in this bit. Read data is always 0.

Note 2. Writing to this bit is enabled only when 55$_H$ is written to the KEY[7:0] bits.

Table 4.9 FPROTR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits control permission and prohibition of writing to the FPROTCN bit.
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	FPROTCN	Lock Bit Protect Cancel Enables or disables protection by the lock bits of the code flash memory against programming and erasure. 0: Enables protection by the lock bits. 1: Disables protection by the lock bits. [Setting condition] • 1 is written to the FPROTCN bit while writing to FPROTR is enabled and FENTRYR is not 0000$_H$. [Clearing conditions] • A value other than 55$_H$ is written to the KEY[7:0] bits in FPROTR. • 0 is written to FPROTCN while the writing to FPROTR is enabled. • The FENTRYR register value is 0000$_H$.

4.10 FSUINITR — Flash Sequencer Set-Up Initialization Register

FSUINITR is used for initialization of the flash sequencer set-up registers.

Access: This register can be read or written in 16-bit units.

Address: FFA1 008C$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R	R/W *2,*3

Note 1. Written data is not stored in this bit. Read data is always 0.

Note 2. This bit can be written only when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit is 0 is ignored.

Note 3. Writing to this bit is enabled only when 2D$_H$ is written to the KEY[7:0] bits.

Table 4.10 FSUINITR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits control permission and prohibition of writing to the SUINIT bit.
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	SUINIT	Set-up Initialization Initializes the flash sequencer set-up registers (FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, FBCCNT, and FAREASELC). 0: The flash sequencer set-up registers keep their current values. 1: The flash sequencer set-up registers are initialized.

4.11 FLKSTAT — Lock Bit Status Register

FLKSTAT indicates the state of a lock bit read by executing a lock-bit read command.

Access: This register is a read-only register that can be read in 8-bit units.

Address: FFA1 0090$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FLOCKST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.11 FLKSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is returned.
0	FLOCKST	Lock Bit Status Reflects the state of a lock bit read by executing a lock-bit read command. When the FRDY bit in FSTATR becomes 1 after the lock-bit read command is issued, the value of the target lock bit is stored in the in FLOCKST bit. The value of the FLOCKST bit is retained until the next lock-bit read command is completed. 0: Protected state 1: Non-protected state

4.12 FRTSTAT — FACI Reset Transfer Status Register

FRTSTAT indicates the FACI reset transfer error state.

Access: This register is a read-only register that can be read in 8-bit units.

Address: FFA1 0098_H

Value after reset: $0X_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RTEDTCT	RTECRCT
Value after reset	0	0	0	0	0	0	0/1	0/1
R/W	R	R	R	R	R	R	R	R

Table 4.12 FRTSTAT Register Contents

Bit Position	Bit Name	Function
7 to 2	Reserved	When read, the value after reset is returned.
1	RTEDTCT	FACI Reset Transfer Error Detection This bit indicates that a 2-bit error was detected during FACI reset transfer. The flash sequencer does not enter the command-locked state when this bit is set to 1. 0: A 2-bit error was not detected. 1: A 2-bit error was detected. This bit is cleared to 0 when FACI reset transfer is finished without a 2-bit error being detected at the time of release from the reset state or wakeup from DeepSTOP mode.
0	RTECRCT	FACI Reset Transfer Error Correction This bit indicates that a 1-bit error was detected and corrected during FACI reset transfer. The flash sequencer does not enter the command-locked state when this bit is set to 1. 0: A 1-bit error was not corrected. 1: A 1-bit error was corrected. This bit is cleared to 0 when FACI reset transfer is finished without a 1-bit error being detected and corrected at the time of release from the reset state or wakeup from DeepSTOP mode.

4.13 FCMDR — FACI Command Register

FCMDR records the two most recent commands received by the FACI.

Access: This register is a read-only register that can be read in 16-bit units.

Address: FFA1 00A0$_H$

Value after reset: FFFF$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMDR[7:0]								PCMDR[7:0]							
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.13 FCMDR Register Contents

Bit Position	Bit Name	Function
15 to 8	CMDR[7:0]	Command Store the latest command received by the FACI.
7 to 0	PCMDR[7:0]	Precommand Store the command immediately before the latest command received by the FACI.

Table 4.14 States of FCMDR after Receiving Commands

Command	CMDR[7:0]	PCMDR[7:0]
Programming	E8$_H$	Previous command
DMA programming	EA$_H$	Previous command
Block erase	D0$_H$	20$_H$
P/E suspend	B0$_H$	Previous command
P/E resume	D0$_H$	Previous command
Status clear	50$_H$	Previous command
Forced stop	B3$_H$	Previous command
Blank check	D0$_H$	71$_H$
Configuration setting	40$_H$	Previous command
Lock-bit programming	D0$_H$	77$_H$
Lock-bit read	D0$_H$	71$_H$
OTP setting	45$_H$	Previous command

4.14 FPESTAT — Flash P/E Status Register

Access: This register is a read-only register that can be read in 16-bit units.

Address: FFA1 00C0$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PEERRST[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.15 FPESTAT Register Contents

Bit Position	Bit Name	Function
15 to 8	Reserved	When read, the value after reset is returned.
7 to 0	PEERRST[7:0]	P/E Error Status These bits indicate the source of an error that occurred during programming or erasure of the code flash or data flash memory. The value of these bits is only valid if the PRGERR or ERSERR bit in FSTATR is 1 while the FRDY bit in FSTATR is 1. When the ERSERR and PRGERR bits are 0, the PEERRST[7:0] bits retain their values to indicate the source of the last error to have occurred. 00$_H$: No error 01$_H$: Programming error due to an area being protected by its lock bit 02$_H$: Programming error for reasons other than lock-bit protection 11$_H$: Erasure error due to an area being protected by its lock bit 12$_H$: Erasure error for reasons other than lock-bit protection

4.15 FBCCNT — Data Flash Blank Check Control Register

FBCCNT specifies the addressing mode during processing of a blank check command. FBCCNT is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Access: This register can be read or written in 8-bit units.

Address: FFA1 00D0$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCDIR
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 4.16 FBCCNT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	BCDIR	Blank Check Direction Specifies the addressing mode for blank checking. 0: Blank checking is executed from lower addresses to higher addresses (incremental mode). 1: Blank checking is executed from higher addresses to lower addresses (decremental mode).

4.16 FBCSTAT — Data Flash Blank Check Status Register

FBCSTAT stores the results of checking in response to a blank check command.

Access: This register is a read-only register that can be read in 8-bit units.

Address: FFA1 00D4$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.17 FBCSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is returned.
0	BCST	Blank Check Status Indicates the results of checking in response to a blank check command. 0: The target area is in the non-programmed state*1. (Nothing has been written to the area after erasure. The area is blank.) 1: The target area has been programmed with 0s or 1s.

Note 1. See **(5) Abnormal termination of programming and erasure** in **Section 10, Usage Notes**.

4.17 FPSADDR — Data Flash Programming Start Address Register

FPSADDR indicates the address of the first programmed area to be detected when processing a blank check command.

Access: This register is a read-only register that can be read in 32-bit units.

Address: FFA1 00D8$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[18:16]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PSADR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.18 FPSADDR Register Contents

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is returned.
17 to 0	PSADR[18:0]	Programmed Area Start Address These bits indicate the address of the first programmed area to be detected when processing a blank check command. The address is an offset from the address where the data flash memory starts. The setting of these bits is only valid if the BCST bit in FBCSTAT is 1, while the FRDY bit in FSTATR is 1. When the BCST bit is 0, the PSADR[18:0] bit holds the address produced by the previous check.

4.18 FCPSR — Flash Sequencer Processing Switching Register

FCPSR is for selecting the erasure suspension mode. FCPSR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Access: This register can be read or written in 16-bit units.

Address: FFA1 00E0$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Table 4.19 FCPSR Register Contents

Bit Position	Bit Name	Function
15 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	ESUSPMD	Erasure Suspend Mode This bit is for selecting the erasure suspension mode when a P/E suspend command is issued while the flash sequencer is executing erasure processing. The ESUSPMD bit should be set before issuing a block erase command. 0: Suspension-priority mode 1: Erasure-priority mode

4.19 FPCKAR — Flash Sequencer Processing Clock Notification Register

FPCKAR specifies the operating frequency (f_{PCLK}*1) of the flash sequencer while processing an FACI command. The highest operating frequency for the given product is set as the value after a reset.

Note 1. [RH850/F1KM-S2, F1KM-S4, F1KH-D8]
f_{PCLK} = 1/8 f_{CPUCLK_H} (CPU operating frequency)
(CKDIVMD = 1*2 or products of CPU frequency 160 MHz max)
f_{PCLK} = 1/4 f_{CPUCLK_H} (CPU operating frequency) (CKDIVMD = 0*2)
[RH850/F1K, F1KM-S1]
f_{PCLK} = 1/4 f_{CPUCLK} (CPU operating frequency)

Note 2. See *Section 44.9, Option Bytes* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

Access: This register can be read or written in 16-bit units.

Address: FFA1 00E4$_H$

Value after reset: Highest operating frequency of the FACI in the RH850/F1K, F1KH or F1KM products

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								PCKA[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3

Note 1. Written data is not stored in this bit. Read data is always 0.

Note 2. This bit can be written only when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit is 0 is ignored.

Note 3. Writing to this bit is enabled only when 1E$_H$ is written to the KEY[7:0] bits.

Table 4.20 FPCKAR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits control permission and prohibition of writing to the PCKA[7:0] bit.
7 to 0	PCKA[7:0]	Flash Sequencer Operating Clock Notification These bits specify the operating frequency of the flash sequencer while processing FACI commands. Set the desired frequency in these bits before issuing an FACI command. Specifically, convert the frequency represented in MHz to a binary number and set it in these bits Example: Frequency is 35.9 MHz (PCKA[7:0] = 24$_H$) Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it to a binary number. If the value set in these bits is smaller than the actual operating frequency of the flash sequencer, the flash memory overwriting characteristics cannot be guaranteed. If the value set in these bits is greater than the actual operating frequency of the flash sequencer, the flash memory overwriting characteristics can be guaranteed but the FACI command processing time such as overwriting time will increase. The minimum FACI command processing time is obtained when the operating frequency of the flash sequencer is same as the PCKA[7:0] value. When SSCG*1 is used, convert the center value of the operating frequency as described in the above example, and set the resulting value.

Note 1. The RH850/F1K and RH850/F1KM-S1 do not have an SSCG. The RH850/F1KH-D8, RH850/F1KM-S4 and RH850/F1KM-S2 have an SSCG.

4.20 FECCEMON — Flash ECC Encoder Monitor Register

FECCEMON monitors the output from the ECC encoder.

Access: This register is a read-only register that can be read in 16-bit units.

Address: FFA1 0100$_H$

Value after reset: FFFF$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FECCM08	FECCM07	FECCM06	FECCM05	FECCM04	FECCM03	FECCM02	FECCM01	FECCM00
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.21 FECCEMON Register Contents

Bit Position	Bit Name	Function
15 to 10	Reserved	When read, the value after reset is returned.
9	Reserved	This bit is read as 0 or 1.
8 to 0	FECCM08 to FECCM00	ECC Monitor These bits indicate the ECC encoder output. • In code flash P/E mode The FECCM08 to FECCM00 bits indicate the ECC encoder output for the code flash memory. • In data flash P/E mode The FECCM08 and FECCM07 bits are fixed to 1. The FECCM06 to FECCM00 bits indicate the ECC encoder output for the data flash memory.

4.21 FECCTMD — Flash ECC Test Mode Register

FECCTMD sets the ECC test function for the flash memory.

Access: This register can be read or written in 16-bit units.

Address: FFA1 0104$_H$

Value after reset: 0030$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	CECCVE	DECCVE	—	—	—	ECCDISE
Value after reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R/W*2	R/W*2	R	R	R	R/W*2

Note 1. Written data is not stored in this bit.Read data is always 0.

Note 2. Writing to this bit is enabled only when A6$_H$ is written to the KEY[7:0] bits.

Table 4.22 FECCTMD Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits control permission and prohibition of writing to the CECCVE, DECCVE, and ECCDISE bits.
7, 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5	CECCVE	Code Flash Memory ECC Area Verify Enable Specifies the verify operation when overwriting the code flash memory. 0: Verifies the data area only. 1: Verifies the data area and the ECC area.
4	DECCVE	Data Flash Memory ECC Area Verify Enable Specifies the verify operation in overwriting of the data flash memory. 0: Verify the data area only. 1: Verify the data area and the ECC area.
3 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	ECCDISE	ECC Encoder Disable Disables the ECC encoder. If the ECC encoder is disabled, the FDMYECC value is written to the flash memory. 0: The ECC encoder is enabled. 1: The ECC encoder is disabled.

4.22 FDMYECC — Flash Dummy ECC Register

FDMYECC specifies the ECC value to be written into the flash memory when the ECCDISE bit in the FECCTMD register is 1. The bit functions in code flash P/E mode are different from those in data flash P/E mode.

Access: This register can be read or written in 16-bit units.

Address: FFA1 0108$_H$

Value after reset: FFFF$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DMYECC[8:0]								
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4.23 FDMYECC Register Contents (in Code Flash P/E Mode)

Bit Position	Bit Name	Function
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8 to 0	DMYECC[8:0]	Dummy ECC These bits specify the ECC value when the ECCDISE bit is 1.

Table 4.24 FDMYECC Register Contents (in Data Flash P/E Mode)

Bit Position	Bit Name	Function
15 to 9	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
8, 7	DMYECC[8:7]	Reserved When read, the value after reset is returned. When writing, write the value after reset.
6 to 0	DMYECC[6:0]	Dummy ECC These bits specify the ECC value when the ECCDISE bit is 1.

4.23 FBUFCCTL — Flash Buffer Clear Control Register

Access: FBUFCCTL register can be read or written in 32-bit units.
FBUFCCTLL register can be read or written in 16-bit units.
FBUFCCTLLL register can be read or written in 8-bit units.

Address: FFC5 B000$_H$ (FBUFCCTL)
FFC5 B000$_H$ (FBUFCCTLL)
FFC5 B000$_H$ (FBUFCCTLLL)

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FBUF CLR
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Table 4.25 FBUFCCTL Register Contents

Bit Position	Bit Name	Function
31 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	FBUFCLR	Buffer clear bit. To clear buffers, write 1 to this bit and then write 0. 0: Buffers are valid 1: Buffers are invalid (cleared)

For transition to read mode after the code flash memory area has been written, or after the value of the BFASELR register has been changed, clear the flash buffer according to the procedure described in **Section 10, Usage Notes**, **(8) Updating the FBUFCCTL register**.

4.24 BFASELR — BFA Selection Register

BFASELR selects the configuration setting area and OTP setting area.

Access: This register can be read or written in 8-bit units.

Address: FFC5 9008_H

Value after reset: *1

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BFAA
Value after reset	0	0	0	0	0	0	0	*1
R/W	R	R	R	R	R	R	R	R/W

Note 1. This bit is set to 1 when the device is booted in serial programming mode, and cleared to 0 when the device is booted in normal operating mode.

Table 4.26 BFASELR Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	BFAA	Area Selection*1 0: The configuration setting area and OTP setting area cannot be read. 1: The configuration setting area and OTP setting area can be read. When this bit is 1, the area of 0000 0000_H to 0100 $7FFF_H$ is reserved.

Note 1. BFAA should be set after all masters stop all read access to the areas switched by setting BFAA. While this bit is set to 1, avoid access to the area of 0000 0000_H to 0100 $7FFF_H$ in response to interrupts by setting the vector address of the CPU exception handler in the on-chip RAM.

4.25 SELFID0 to SELFID3 — Self-Programming ID Input Registers

SELFID is for the input of an ID for use in authentication when FACI commands are used in code flash P/E mode*[1], configuration setting command is used*[1] or configuration setting area read is used. The ID is authenticated by comparing the 128-bit authentication ID that has been set in advance with the value in the SELFID0 to SELFID3 registers. The authentication ID can be set by the security settings specified by using serial programming and the code flash library, or by the configuration setting command for the FACI.

Note 1. SIDAM setting affects the need of ID authentication. See *Section 44.9.3, OPBT1 -- Option Byte 1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.[RH850/F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1]

Access: This register can be read or written in 32-bit units.

Address: FFA0 8000H (SELFID0)
FFA0 8004H (SELFID1)
FFA0 8008H (SELFID2)
FFA0 800CH (SELFID3)

Value after reset: 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SELFIDn[31:16]*1															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SELFIDn[15:0]*1															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note 1. n = 0 to 3

Table 4.27 SELFID0 to SELFID3 Register Contents

Bit Position	Bit Name	Function
31 to 0	SELFIDn[31:0]	ID for Use in Authentication of Self-Programming The ID for use in authentication at the time of self-programming is input to these bits. Authentication of the ID is executed by comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFIDn[31:0] bits. The 128-bit ID is arranged in the respective sets of SELFIDn[31:0] bits in the way listed below. ID[31:0]: SELFID0[31:0] ID[63:32]: SELFID1[31:0] ID[95:64]: SELFID2[31:0] ID[127:96]: SELFID3[31:0]

4.26 SELFIDST — Self-Programming ID Authentication Status Register

SELFIDST indicates the result of authentication of an ID during self-programming. The SELFIDST register indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. The ID stored in a particular range of the flash memory can be set by specifying security settings by using on-board/off- board programming and the self-programming library, or by the configuration setting command for the FACI.

Access: SELFIDST register is a read-only register that can be read in 32-bit units.
SELFIDSTL register is a read-only register that can be read in 16-bit units.
SELFIDSTLL register is a read-only register that can be read in 8-bit units.

Address: FFA0 8010_H (SELFIDST)
FFA0 8010_H (SELFIDSTL)
FFA0 8010_H (SELFIDSTLL)

Value after reset: 0000 $000X_H$*1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note 1. The value of the SELFIDST register after a reset depends on the previously set authentication ID. If all the authentication IDs are 0, the value after a reset is 0. Otherwise, it is 1.

Table 4.28 SELFIDST Register Contents

Bit Position	Bit Name	Function
31 to 1	Reserved	When read, the value after reset is returned.
0	IDST	ID Authentication Status This bit indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. 0: The IDs match (ID-based security is unlocked). 1: The IDs do not match (ID-based security is locked*1).

Note 1. ID-based security is unlocked depending on SIDAM setting regardless of IDST. See *Section 44.9.3, OPBT1 -- Option Byte 1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.[RH850/F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1]

Section 5 Modes Associated with Flash Memory

5.1 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in **Figure 5.1**. Transitions between modes are initiated by changing the value of the FENTRYR register.

When the FENTRYR register is 0000_H, the flash sequencer is in read mode. In this mode, it does not receive FACI commands. The code flash memory and the data flash memory are both readable.

When the value of the FENTRYR register is 0001_H, the flash sequencer is in code flash P/E mode in which the code flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. When the background operation cannot be used, the code flash memory is also not readable. When the background operation can be used, the code flash memory is readable. See *Section 37.7.2, Background Operation* of *the RH850/F1K User's Manual: Hardware* or *Section 44.7.2, Background Operation* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware* for the condition of the background operation.

When the value of the FENTRYR register is 0080_H, the flash sequencer is in data flash P/E mode in which the data flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

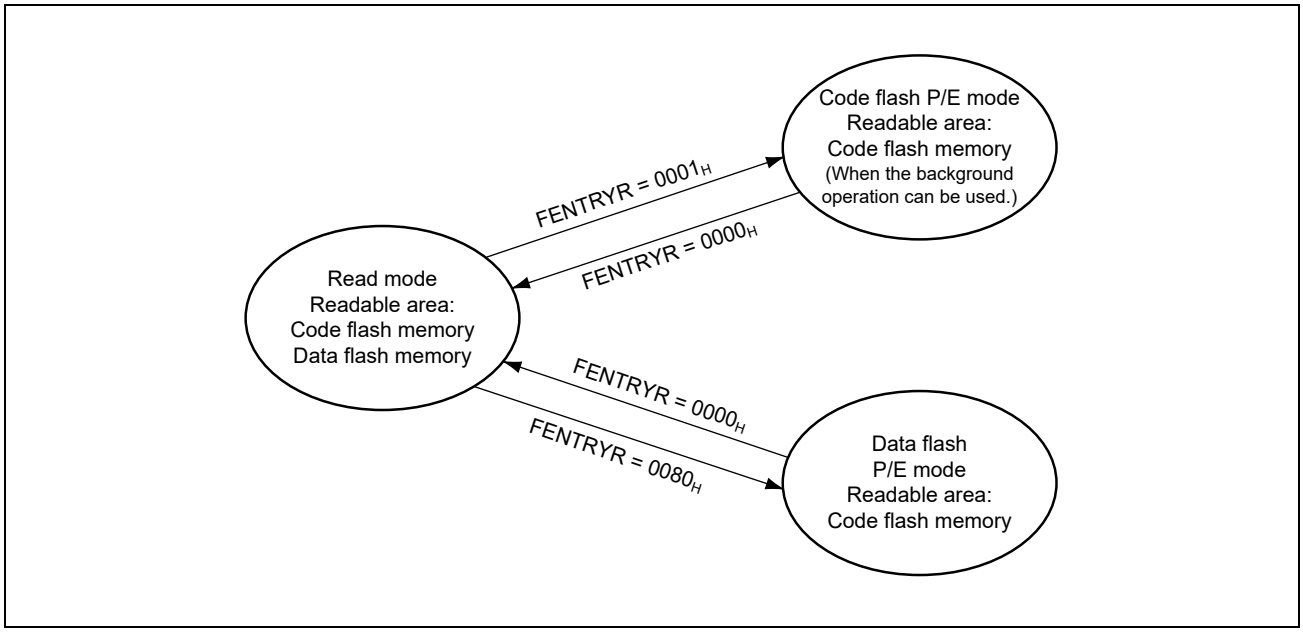


Figure 5.1 Modes of the Flash Sequencer

Section 6 FACI Commands

6.1 List of FACI Commands

Table 6.1 List of FACI Commands

FACI Command	Function
Programming	This is used to program the user area, extended user area, and data area. • Units of programming: 256 bytes for the user area and extended user area • Units of programming: 4 bytes for the data area
DMA programming	This is used to program the data area using the DMA controller. • Units of programming: 4 bytes to 64 KB (specified in 4-byte units)
Block erase	This is used to erase the user area, extended user area, lock bit, and data area. • Units of erasure: One block
P/E suspend	This suspends programming or erasure processing.
P/E resume	This resumes suspended programming or erasure processing.
Status clear	This initializes the FSTATR.OTPDTCT, OTPCRCT, ILGLERR, ERSERR, PRGERR, CFGDTCT, CFGCRCT, TBLDTCT, TBLCRCT bits and releases the flash sequencer from the command-locked state.
Forced stop	This forcibly stops processing of FACI commands and initializes the FSTATR register.
Blank check	This is used to check if data areas are blank. • Units of blank checking: 4 bytes to 64 KB (specified in 4-byte units)
Configuration setting	This is used to set the ID, security function, safety function, and option bytes. • Units of programming: 16 bytes
Lock-bit programming	This is used to program the lock bit for the user area and extended user area. • Units of programming: 1 bit (the lock bit for one block)
Lock-bit read	This reads the lock bit in the user area, or extended user area and stores the result in the FLKSTAT register. • Units of reading: 1 bit (the lock bit for one block)
OTP (One Time Programming) setting	This selects OTP for the user area or extended user area. • Units of setting: 16 bytes (OTP settings for 128 blocks)

The FACI commands are issued by writing to the FACI command-issuing area (see **Table 3.1**). When a command is written in the format shown in **Table 6.2** proceeds in the specified state, the flash sequencer executes the processing corresponding to the given command (see **Section 6.2, Relationship between the Flash Sequencer States and FACI Commands**).

Table 6.2 FACI Command Formats

FACI Command	Number of write Access	Write Data to the FACI Command Issuing Area			
		1st Access	2nd Access*1	3rd to (N+2)th Access	(N+3)th Access
Programming (user area and extended user area) 256-byte programming: N = 128	131	$E8_H$	80_H	WD_1 to WD_{128}	$D0_H$
Programming (data area) 4-byte programming: N = 2	5	$E8_H$	02_H	WD_1 to WD_2	$D0_H$
DMA programming N = 2 to 32768 (even numbers only)	N+2	EA_H	N	WD_1 to WD_N	—
Block erase	2	20_H	$D0_H$	—	—
P/E suspend	1	$B0_H$	—	—	—
P/E resume	1	$D0_H$	—	—	—
Status clear	1	50_H	—	—	—
Forced stop	1	$B3_H$	—	—	—
Blank check	2	71_H	$D0_H$	—	—
Configuration setting N = 8	11	40_H	08_H	WD_1 to WD_8	$D0_H$
Lock-bit programming	2	77_H	$D0_H$	—	—
Lock-bit read	2	71_H	$D0_H$	—	—
OTP setting N = 8	11	45_H	08_H	WD_1 to WD_8	$D0_H$

Note: WD_N (N = 1, 2,…): Nth 16-bit data to be programmed.

Note 1. 8-bit data is written by a command other than the DMA programming command. With the DMA programming command, 16-bit data is written.

When processing a command other than the status clear command starts, the flash sequencer sets the FRDY bit of the FSTATR register to 0 and then sets it to 1 on completion of command processing (see **Section 4.7, Flash Status Register (FSTATR)**). When the FRDY bit changes from 0 to 1, the flash sequencer complete interrupt (INTFLENDNM) is generated.

6.2 Relationship between the Flash Sequencer States and FACI Commands

Sets of FACI commands that can be acknowledged in each modes/states of the flash sequencer are fixed. FACI commands should be issued after the transitioning the flash sequencer to code flash P/E mode or data flash P/E mode and checking the state of the flash sequencer. To check the state of flash sequencer, use the FSTATR and FASTAT registers. In addition, the occurrence of errors in general can be checked by reading the CMDLK bit in the FASTAT register. The value of the CMDLK bit is the logical OR of the OTPDTCT, ILGLERR, ERSERR, PRGERR, CFGDTCT, and TBLDTCT bits of the FSTATR register.

Table 6.3 summarizes the commands that can be used in each operating mode.

Table 6.3 Operation Modes and Available Commands

Operating Mode	FENTRYR	Available Commands
Read mode	0000_H	None
Code flash P/E mode	0001_H	Programming Block erase P/E suspend P/E resume Status clear Forced stop Lock-bit programming Lock-bit read
Data flash P/E mode	0080_H	Programming DMA programming Block erase P/E suspend P/E resume Status clear Forced stop Blank check Configuration setting OTP setting

Table 6.4 shows the state of the flash sequencer and FACI commands that can be acknowledged. An appropriate mode is assumed to have been set before the commands are executed.

Table 6.4 Flash Sequencer States and Acknowledgeable FACI Commands

		Programming or Erasure Processing	Configuration Setting or OTP setting Processing	Suspend Programming or Erasure Processing	Blank checking or Lock Bit Reading	DMA programming Processing	Programming Suspended	Erasure Suspended	Programming while Erasure is Suspended	Command-Locked State (FRDY = 1)	Command-Locked State (FRDY = 0)	Lock-Bit Programming	Forced Stop Command Processing	Other States
State of the flash sequencer	FRDY bit	0	0	0	0	0	1	1	0	1	0	0	0	1
	SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0	0	0
	ERSSPD bit	0	0	0/1	0/1	0	0	1	1	0/1	0/1	0	0	0
	PRGSPD bit	0	0	0/1	0/1	0	1	0	0	0/1	0/1	0	0	0
	CMDLK bit	0	0	0	0	0	0	0	0	1	1	0	0	0
FACI commands	Programming	—	—	—	—	—	—	✓ *3	—	—	—	—	—	✓
	DMA programming	—	—	—	—	—	—	✓ *1,*3	—	—	—	—	—	✓ *1
	Block erase	—	—	—	—	—	—	—	—	—	—	—	—	✓
	P/E suspend	✓	—	—	—	—	—	—	—	X	—	—	—	X
	P/E resume	—	—	—	—	—	✓	✓	—	—	—	—	—	—
	Status clear	—	—	—	—	—	✓	✓	—	✓	—	—	—	✓
	Forced stop	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Blank check	—	—	—	—	—	✓ *1	✓ *1	—	—	—	—	—	✓ *1
	Configuration setting	—	—	—	—	—	—	—	—	—	—	—	—	✓ *1
	Lock-bit programming	—	—	—	—	—	—	—	—	—	—	—	—	✓ *2
	Lock-bit read	—	—	—	—	—	✓ *2	✓ *2,*4	—	—	—	—	—	✓ *2
	OTP setting	—	—	—	—	—	—	—	—	—	—	—	—	✓ *1

Remark: ✓: Acknowledgeable, —: Not acknowledgeable (command-locked state), X: Ignored

Note 1. Only acknowledged in data flash P/E mode.

Note 2. Only acknowledged in code flash P/E mode.

Note 3. Programming is only acknowledged for blocks other than blocks where erasure has been suspended.

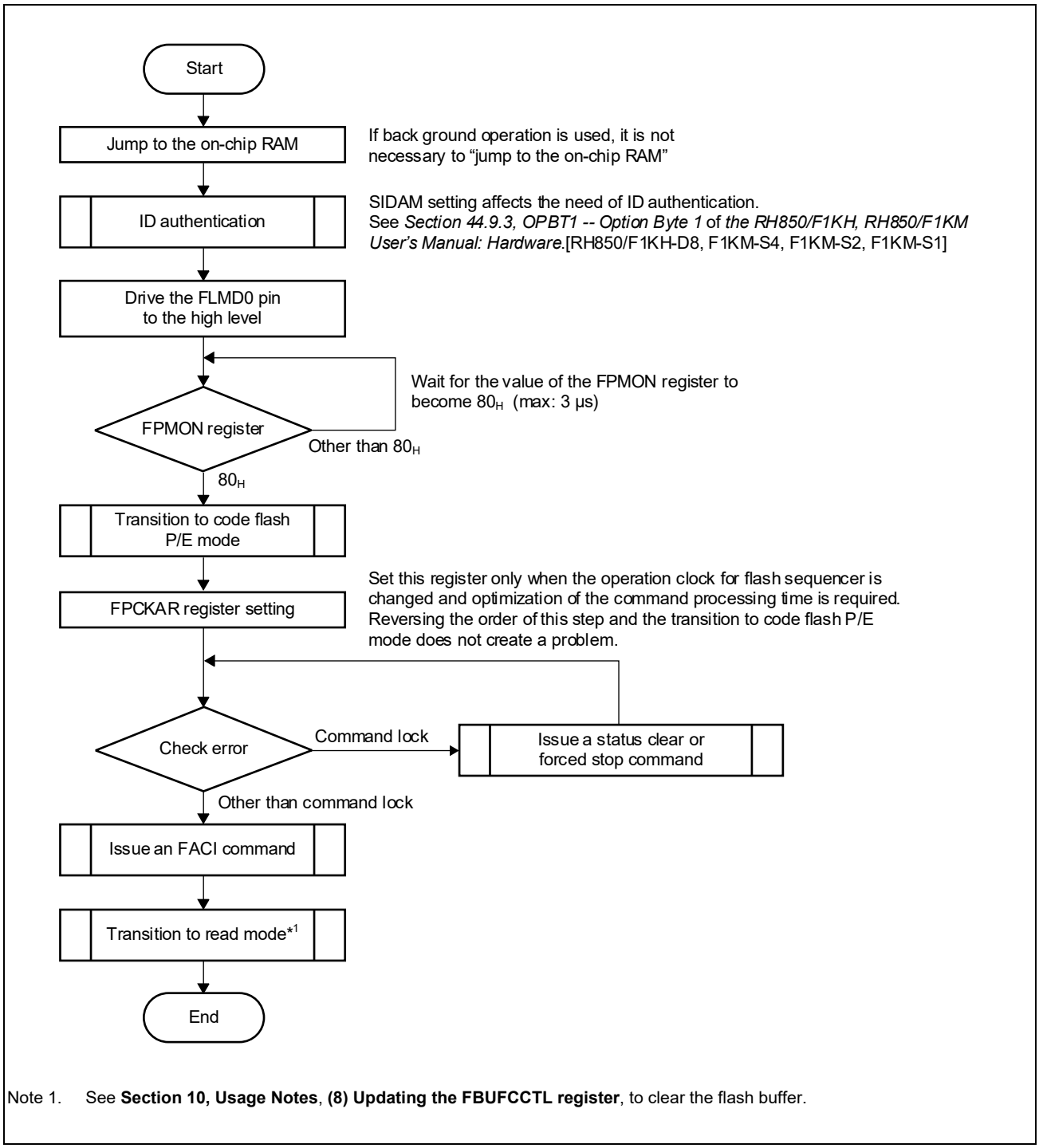
Note 4. The value read out is undefined when a lock-bit read command is issued for a block where erasure was suspended.

6.3 Usage of FACI Commands

This section gives an overview of the usage of FACI commands.

6.3.1 Overview of Command Usage in Code Flash P/E Mode

An overview of FACI command usage in code flash P/E mode is shown below. For the commands that can be used in code flash memory P/E mode, see **Table 6.3**. Note that security should be unlocked by ID authentication before FACI commands are used for the code flash memory.



Note 1. See **Section 10, Usage Notes**, **(8) Updating the FBUFCCTL register**, to clear the flash buffer.

Figure 6.1 Overview of Command Usage in Code Flash P/E Mode

6.3.2 Overview of Command Usage in Data Flash P/E Mode

An overview of FACI command usage in data flash P/E mode is shown below. For the commands that can be used in data flash P/E mode, see **Table 6.3**.

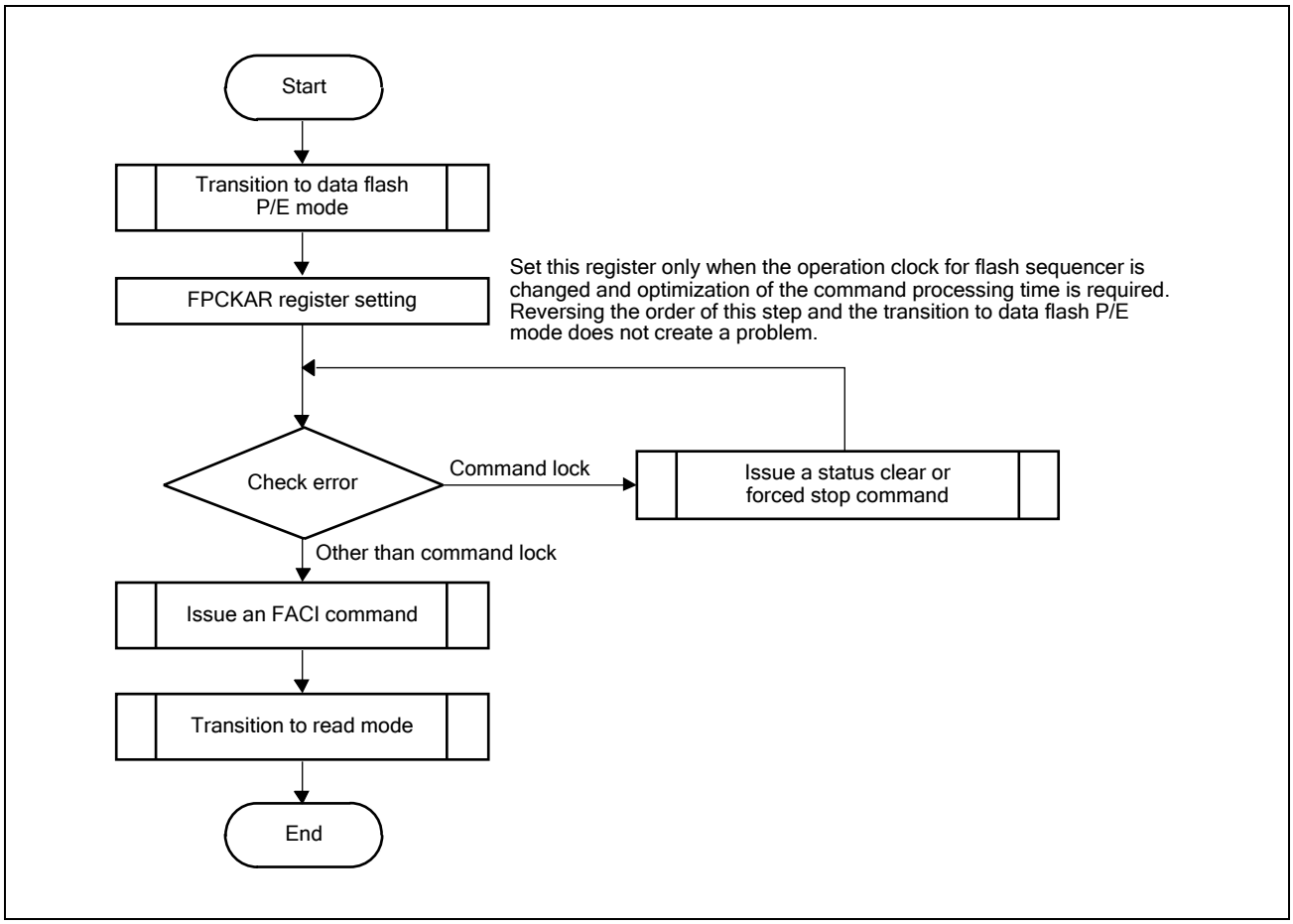


Figure 6.2 Overview of Command Usage in Data Flash P/E Mode

6.3.3 Transition to Code Flash P/E Mode

To use the FACI commands related to the code flash memory, transition to code flash P/E mode is required. To transition to code flash P/E mode, set the FENTRYC bit in the FENTRYR register to 1.

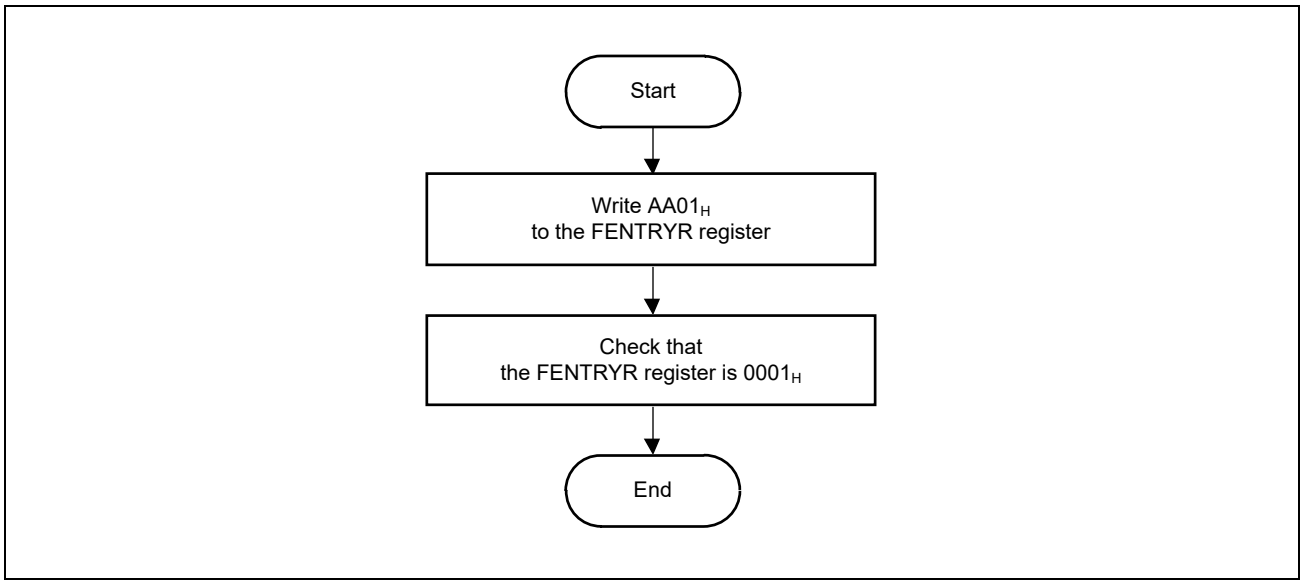


Figure 6.3 Procedure for Transitioning to Code Flash Memory P/E Mode

6.3.4 Transition to Data Flash P/E Mode

To use the FACI commands for the data flash memory, transition to data flash P/E mode is required. To transition to data flash P/E mode, set the FENTRYD bit in the FENTRYR register to 1.

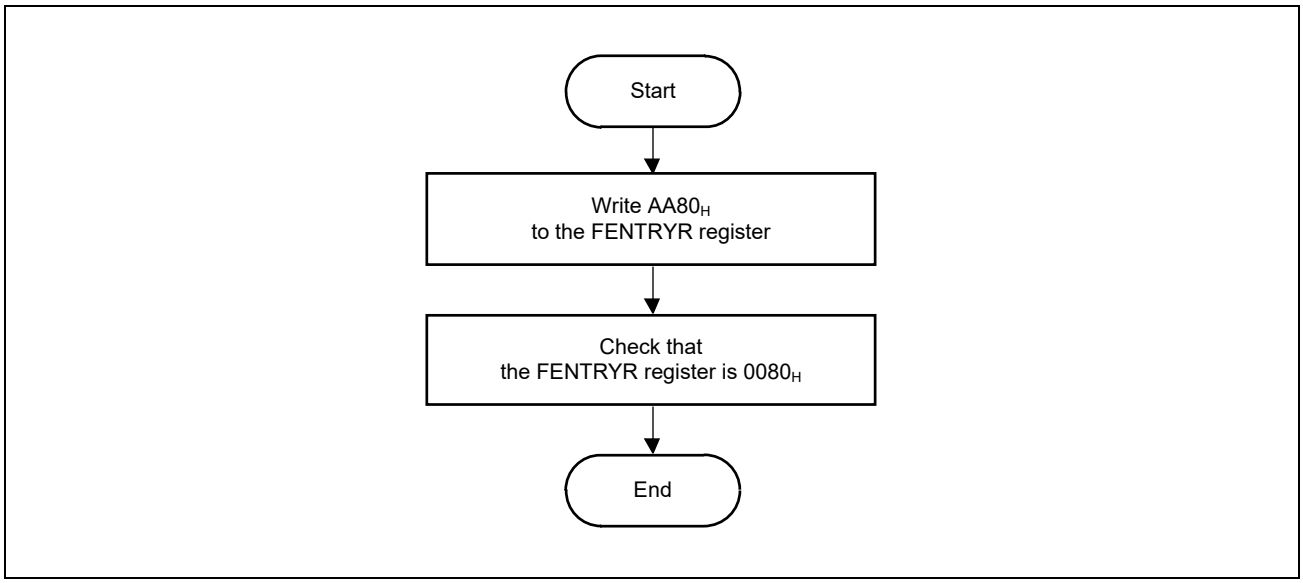
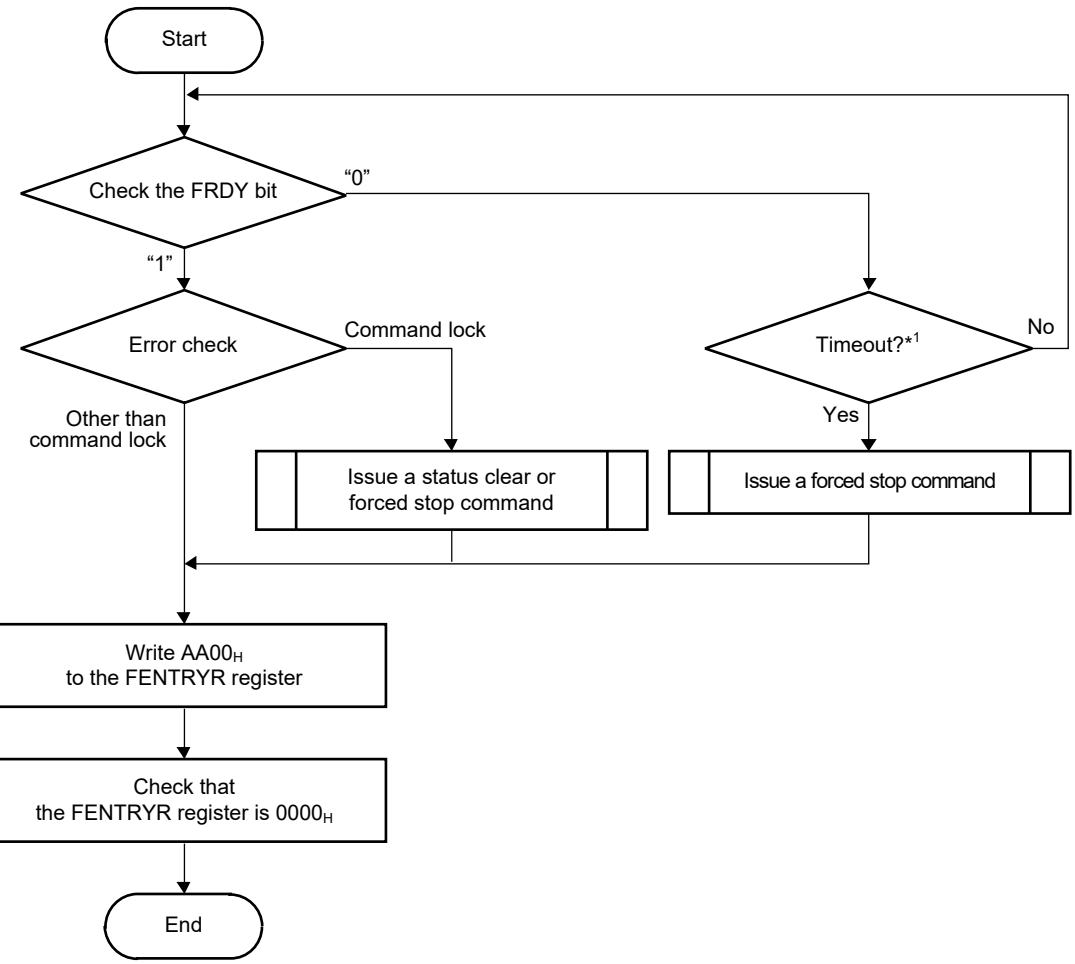


Figure 6.4 Procedure for Transitioning to Data Flash Memory P/E Mode

6.3.5 Transition to Read Mode

To read the flash memory without using the BGO function, transition to read mode is required. To transition to read mode, set the FENTRYC and FENTRYD bits in FENTRYR to 0. The transition to read mode should be made after flash sequencer processing is complete and while operation is not in the command-locked state.



Note 1. Processing of an FACI command reaching 1.1 times the maximum processing time (see **Section 11, Electrical Characteristics**) can be considered a timeout. If common processing is used, 1.1 times the maximum erasure time for a 32 KB block of code flash memory can be considered a timeout.

Figure 6.5 Procedure for Transition to Read Mode

6.3.6 ID Authentication

To use FACI commands in code flash P/E mode or to use configuration setting command, unlock security by ID authentication and write 0 to the SELFIDST register. SIDAM setting affects the need of ID authentication. See *Section 44.9.3, OPBT1 -- Option Byte 1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.[RH850/F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1] When the IDST bit is 1, FACI commands are not acknowledged. **Figure 6.6** shows the ID comparison method using SELFID0 to SELFID3, and how the result of comparison is checked by SELFIDST.

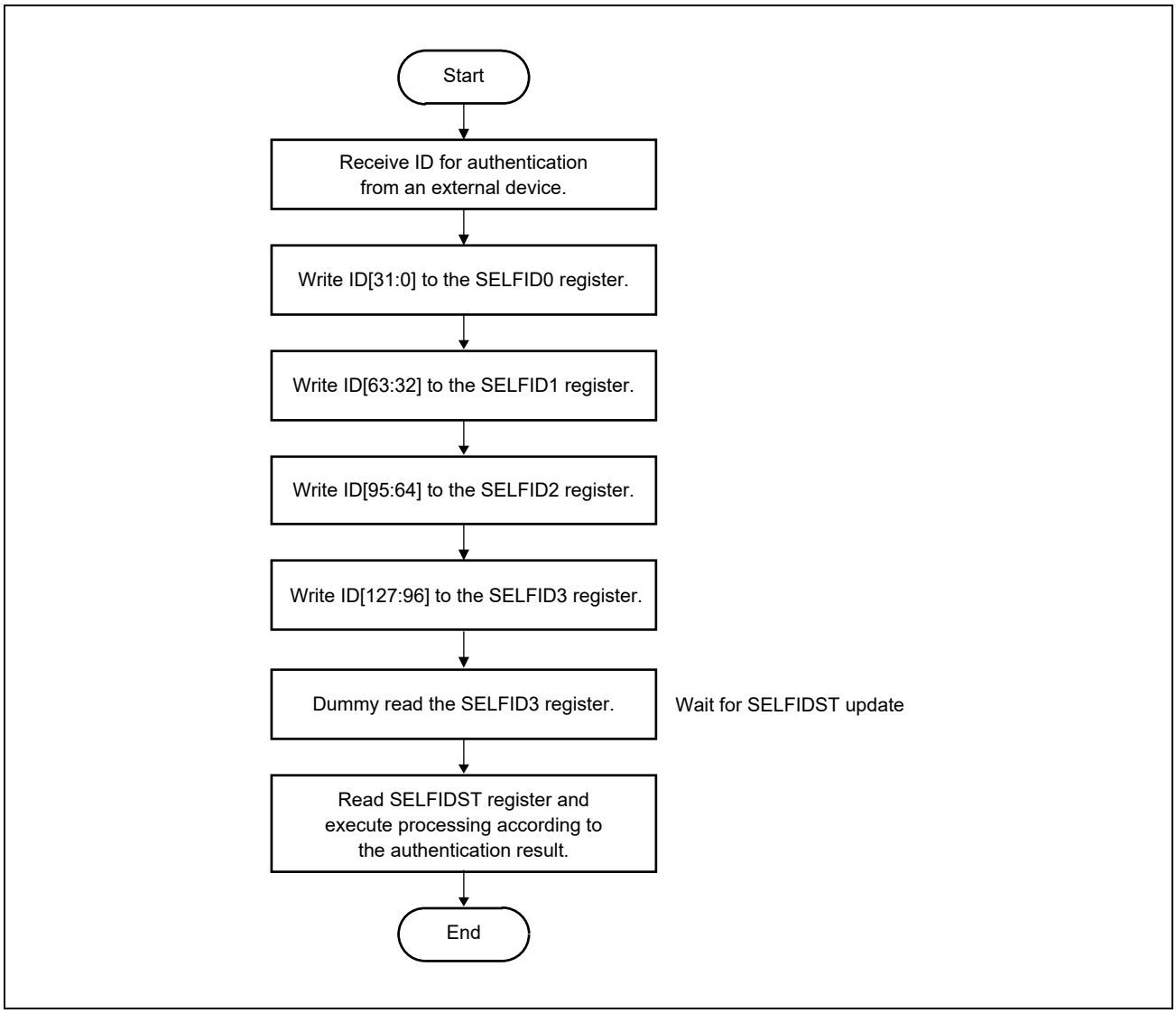


Figure 6.6 Flow of ID Comparison

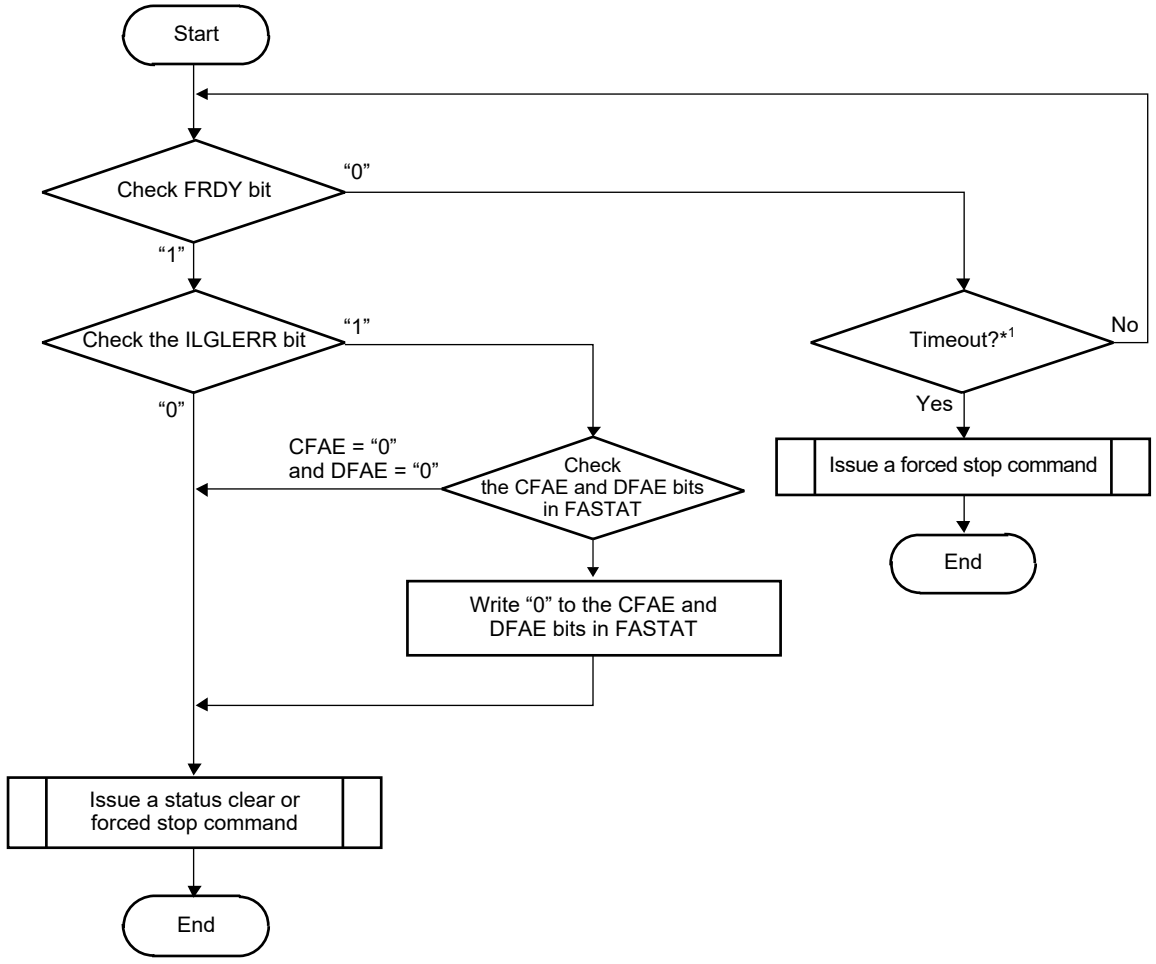
6.3.7 Recovery from the Command-Locked State

While the flash sequencer is in the command-locked state, FACI commands are not acknowledged. To release the sequencer from the command-locked state, use the status clear command, forced stop command, or FASTAT register.

When the command-locked state is detected by checking for errors before issuing the P/E suspend command, the FRDY bit in the FSTATR register may hold 0 even though command processing is not complete. If processing is not completed within the maximum programming or erasure time specified in the electrical characteristics, it is judged as a timeout and the flash sequencer will need to be stopped by the forced stop command.

When the ILGLERR bit in the FSTATR register is 1, check the FASTAT value. If the setting of the CFAE or DFAE bit in FASTAT is 1, the status clear and forced stop commands cannot be used to release the sequencer from the command-locked state.

The bits that indicate the command-locked state can be changed from 1 to 0 by the status clear or forced stop command.



Note 1. Processing of an FACI command reaching 1.1 times the maximum processing time (see **Section 11, Electrical Characteristics**) can be considered a timeout. If common processing is used, 1.1 times the maximum erasure time for a 32 KB block of code flash memory can be considered a timeout.

Figure 6.7 Recovery from the Command-Locked State

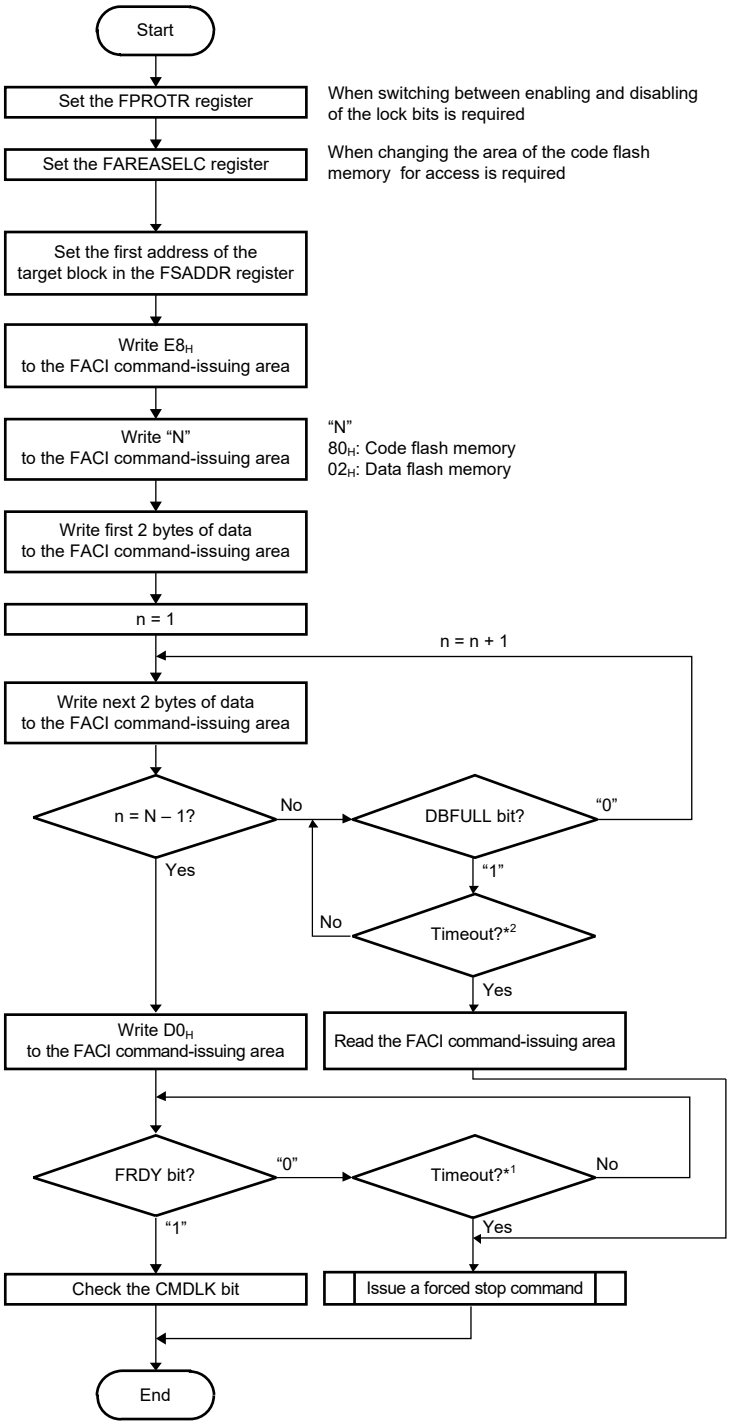
6.3.8 Issuing a Programming Command

A programming command is used for writing to the user area, extended user area, and data area.

Before issuing a programming command, set the first address of the target block in the FSADDR register. Writing $D0_H$ to the FACI command-issuing area at the final access of the FACI command- issuing starts the programming command processing. If the target area of programming command processing contains an area not for writing, write $FFFF_H$ to the corresponding area.

The FPROTR and FAREASELC registers must be set before issuing a program command. To switch between enabling and disabling the lock bits, the setting of the FPROTR register must be changed. To switch the target area for programming the code flash memory, the setting of the FAREASELC register must be changed.

When the FACI internal data buffer is full, issuing a programming command leads to a wait on the P- bus, and may affect the communications performance of other peripheral IP modules. To avoid the generation of a wait, the DBFULL bit in the FSTATR register should be 0 when an FACI command is issued. Writing to the data area will not lead to the data buffer becoming full.



Note 1. For the code flash memory, the time of 256-byte programming (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout. For the data flash memory, the time of 4-byte programming (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout. If common processing is used, the time of 256-byte programming of the code flash memory reaching 1.1 times is judged as a timeout.

Note 2. The time reaching 5 µs (f_{PCLK} ≥ 20 MHz) is judged as a timeout.

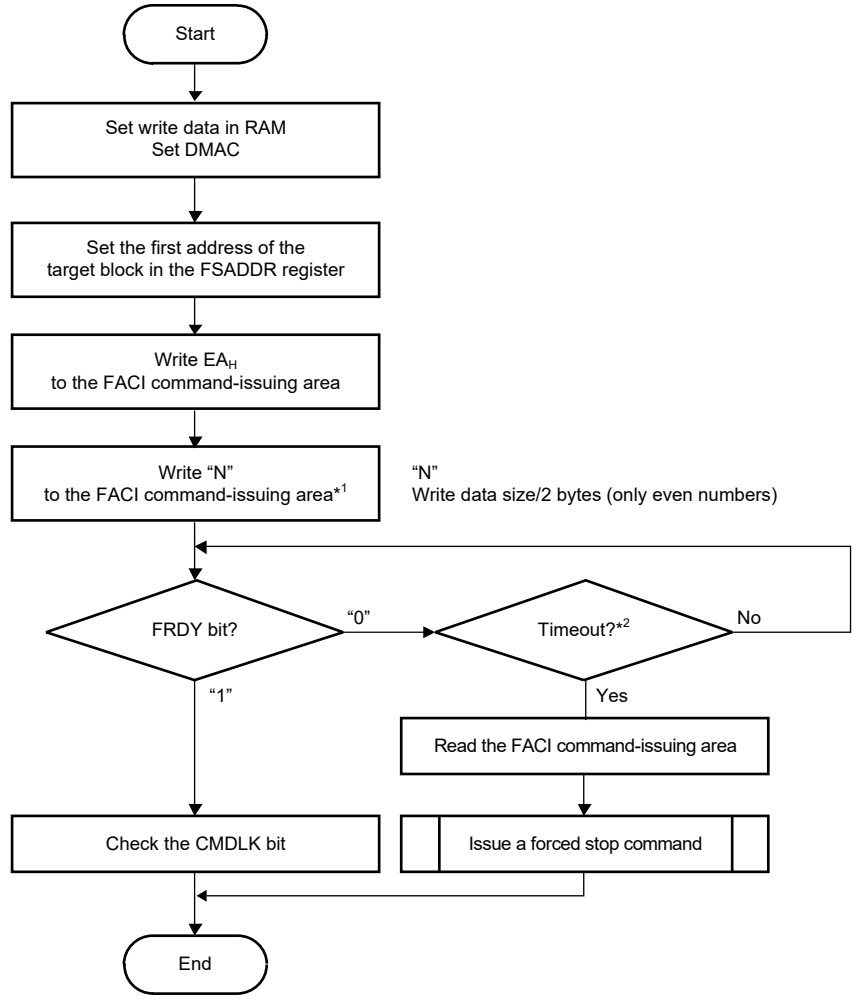
Figure 6.8 Usage of the Programming Command

6.3.9 DMA Programming Command

A DMA programming command is used to program multiple 4-byte data transferred from the DMAC to the data area. Thus, a large amount of data can be programmed continuously with a reduced CPU load.

Before issuing a DMA programming command, set the first address of the target block to the FSADDR register. Set the write data in the RAM and set the DMAC to perform DMA transfer from the pertinent area to the FACI command-issuing area. The FACI issues a request for data transfer (INTDMAFL) to the DMAC immediately after receiving a DMA programming command and every time the writing of four bytes of data is completed. Set the DMAC to transfer two bytes of data twice in response to each request for data transfer.

For the usage of the DMAC, see *the RH850/F1K User's Manual: Hardware* or *RH850/F1KH, RH850/F1KM User's Manual: Hardware*.



Note 1. A data transfer request (INTDMAFL) is issued to the DMAC at the time when "N" is written to the FACI command-issuing area. After that, the data transfer request (INTDMAFL) is issued to the DMAC every time writing 4-byte data is completed.

Note 2. Judged based on the sum of the time of 4-byte programming of the data flash memory (the maximum time: see **Section 11, Electrical Characteristics**) × "N"/2 × 1.1 and the time required for DMA transfer of write data.

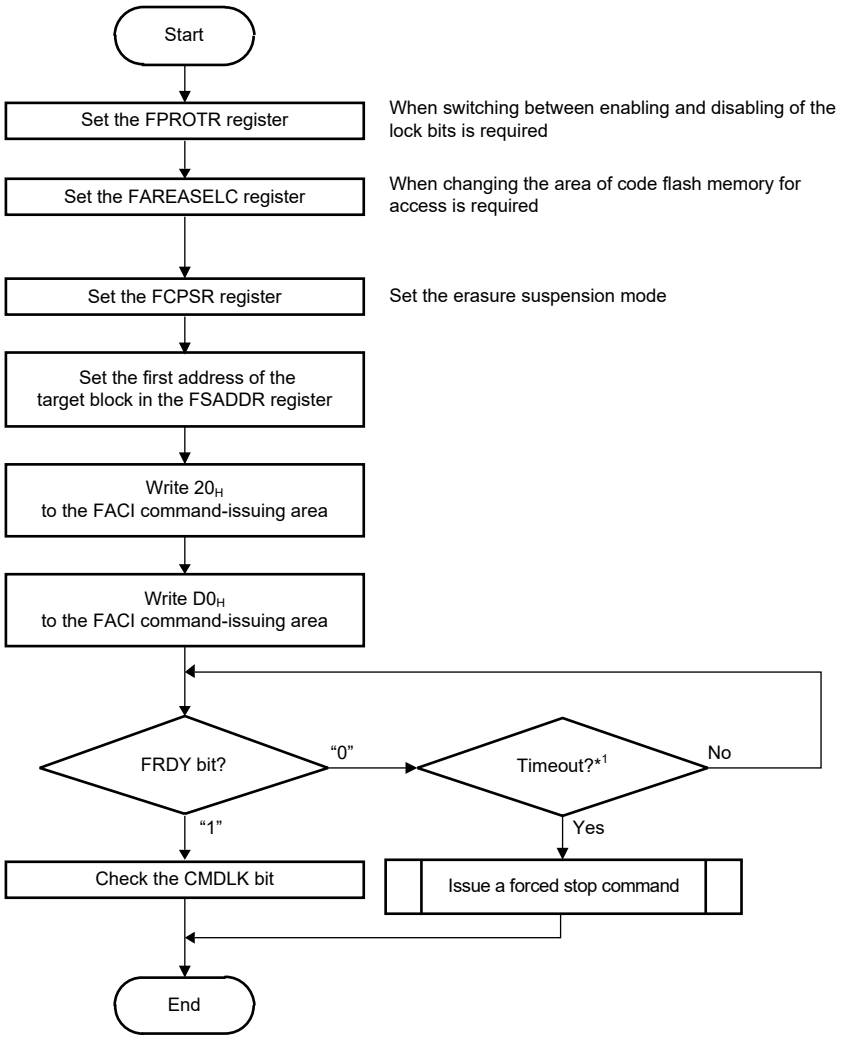
Figure 6.9 Usage of the DMA Programming Command

6.3.10 Block Erase Command

A block erase command is used to erase the user area, extended user area, lock bit, and data area.

Before issuing a block erase command, set the first address of the target block in the FSADDR register. Writing 20_H and $D0_H$ to the FACI command-issuing area starts processing of a block erase command. The FPROTR, FAREASELC, and FCPSR registers must be set before issuing a block erase command.

To switch between enabling and disabling the lock bits, the setting of the FPROTR register must be changed. To erase the lock bit, issue a block erase command while the FPROTCN bit in the FPROTR register is 1. To switch the target area for programming the code flash memory, the setting of the FAREASELC register must be changed. The setting of the FCPSR register must be changed to switch the suspending method (suspend priority mode/erasure priority mode) by using the P/E suspend command.



Note 1. For the code flash memory, the time of erasure of a 32 KB block (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout. For the data flash memory, the time of erasure of a 64-byte block (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout. If common processing is used, the time.

Figure 6.10 Usage of the Block Erase Command

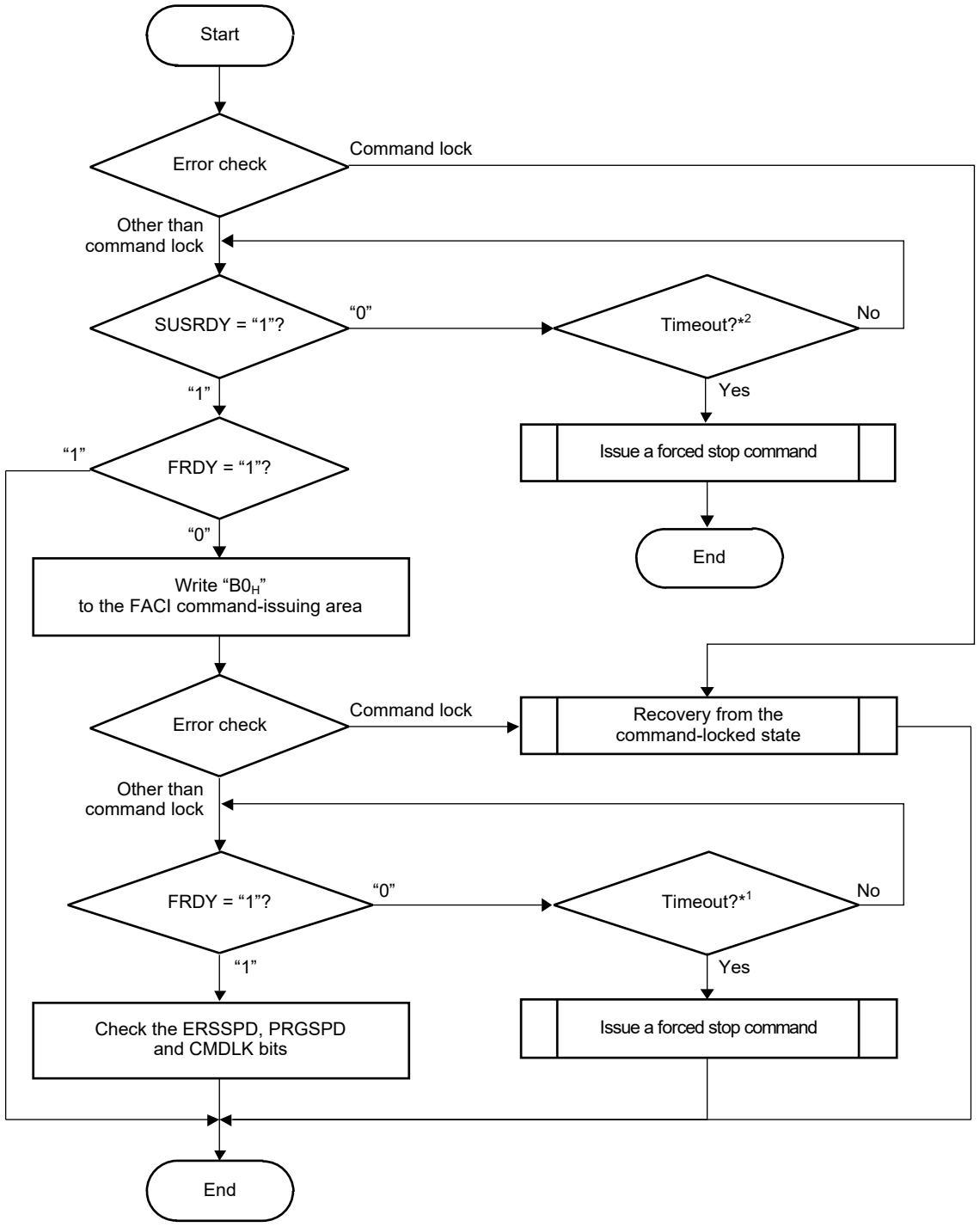
6.3.11 P/E Suspend Command

To suspend programming/erasure, use the P/E suspend command. Before issuing a P/E suspend command, check that the CMDLK bit in the FSASTAT register is 0, and the execution of programming/erasure is performed normally. To confirm that the P/E suspend command can be received, also check that the SUSRDY bit in the FSTATR register is 1. After issuing a P/E suspend command, read the CMDLK bit to confirm that no error has occurred.

If an error occurs during programming/erasure, the CMDLK bit is set to 1. If programming/erasure processing finishes is the interval from when the SUSRDY bit is confirmed to be 1 to when a P/E suspend command is received, no error has occurred and the suspended state is not entered (the FRDY bit in the FSTATR register is 1 and the ERSSPD and PRGSPD bits in FSTATR are 0).

When a P/E suspend command is received and the programming/erasure suspend processing finishes normally, the flash sequencer enters the suspended state, the FRDY bit is set to 1, and the ERSSPD or PRGSPD bit is 1. After issuing a P/E suspend command, check that the ERSSPD or PRGSPD bit is 1 and the suspended state is entered, and then determine the subsequent flow. If a P/E resume command is issued in the subsequent flow even though the suspended state is not entered, an illegal command error occurs and the flash sequencer shifts to the command-locked state.

If the erasure suspended state is entered, programming of blocks other than an erasure target can be performed. Additionally, the programming and erasure suspended states can be shifted to read mode by clearing the FENTRYR register.



Note 1. For the code flash memory, the suspend latency t_{SEED} during erasure of the code flash memory (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times can be considered as a timeout. For the data flash memory, the suspend latency t_{SEED} during erasure of the data flash memory (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times can be considered as a timeout. If common processing is used, 1.1 times t_{SEED} (max.) of the code flash memory can be considered as a timeout.

Note 2. The time reaching 13 µs (f_{PCLK} ≥ 20 MHz) is judged as a timeout.

Figure 6.11 Usage of the P/E Suspend Command

(1) Suspension during programming

When a P/E suspend command is issued during flash memory programming, the flash sequencer suspends programming. **Figure 6.12** shows the operation of suspending programming. When receiving a programming-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start programming. If the flash sequencer enters the state which the P/E suspend command can be received after starting programming, it sets the SUSRDY bit in the FSTATR register to 1. When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0. If the flash sequencer receives a P/E suspend command while a programming pulse is being applied, the flash sequencer continues applying the pulse. After a specified pulse application time, the flash sequencer finishes pulse application, and starts the programming suspend processing and sets the PRGSPD bit in the FSTATR register to 1.

When the suspend processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the programming suspended state. When receiving a P/E resume command in the programming suspended state, the flash sequencer clears the FRDY and PRGSPD bits to 0 and resumes programming.

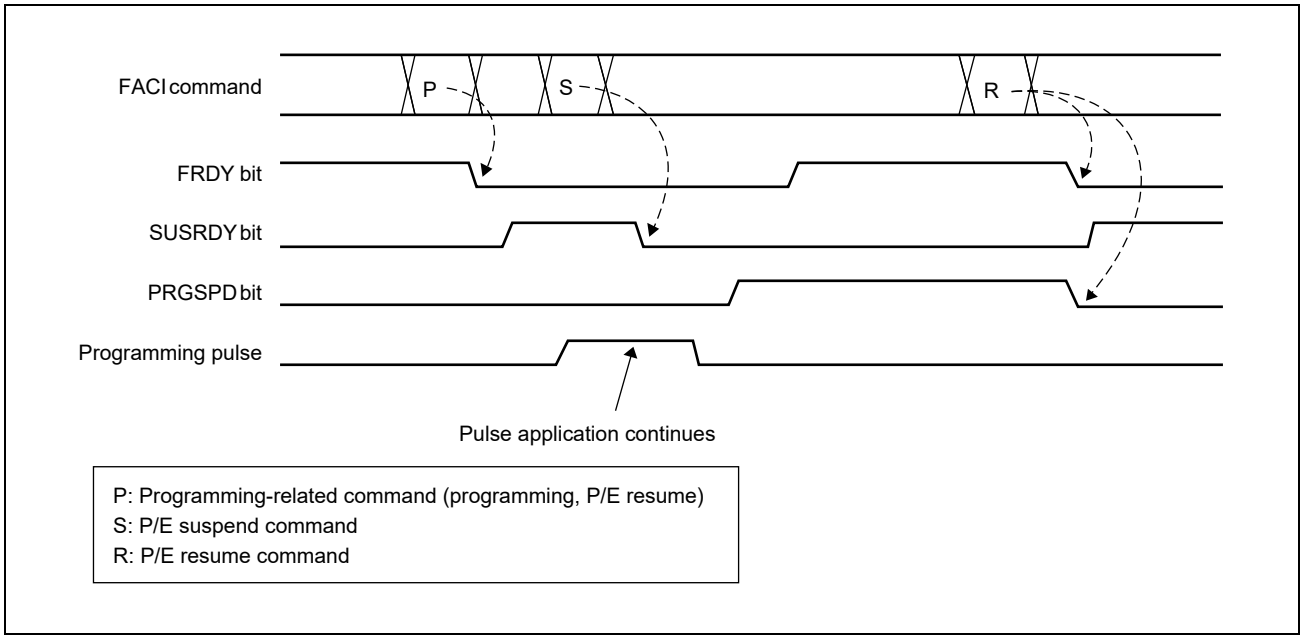


Figure 6.12 Suspension during Programming

(2) Suspension during erasure (suspension priority mode)

This microcontroller has a suspension priority mode for the suspension of erasure. **Figure 6.13** shows the suspend operation of erasure when the erasure suspend mode is set to the suspension priority mode (the ESUSPMD bit in the FCPSR register is 0).

When receiving an erasure-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start erasure. If the flash sequencer enters the state in which the P/E suspend command can be received after starting erasure, it sets the SUSRDY bit in the FSTATR register to 1. When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0. When receiving a suspend command during erasure, the flash sequencer starts the suspend processing and sets the ERSSPD bit in the FSTATR register to 1 even if it is applying an erasure pulse. When the suspend processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the erasure suspended state. When receiving a P/E resume command in the erasure suspended state, the flash sequencer clears the FRDY and ERSSPD bits to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD bits at the suspension and resumption of erasure are the same, regardless of the erasure suspend mode.

The setting of the erasure suspend mode affects the control method of erasure pulses. In suspension priority mode, when receiving a P/E suspend command while erasure pulse A that has never been suspended in the past is being applied, the flash sequencer suspends the application of erasure pulse A and enters the erasure suspended state. When receiving a P/E suspend command while reapplying erasure pulse A after erasure is resumed by a P/E resume command, the flash sequencer continues applying erasure pulse A. After the specified pulse application time, the flash sequencer finishes erasure pulse application and enters the erasure suspended state. When the flash sequencer next receives a P/E resume command and erasure pulse B starts to be newly applied, and then the flash sequencer receives a P/E suspend command again, the application of erasure pulse B is suspended. In suspension priority mode, delay due to suspension can be minimized because the application of an erasure pulse is suspended one time per pulse and priority is given to the suspend processing.

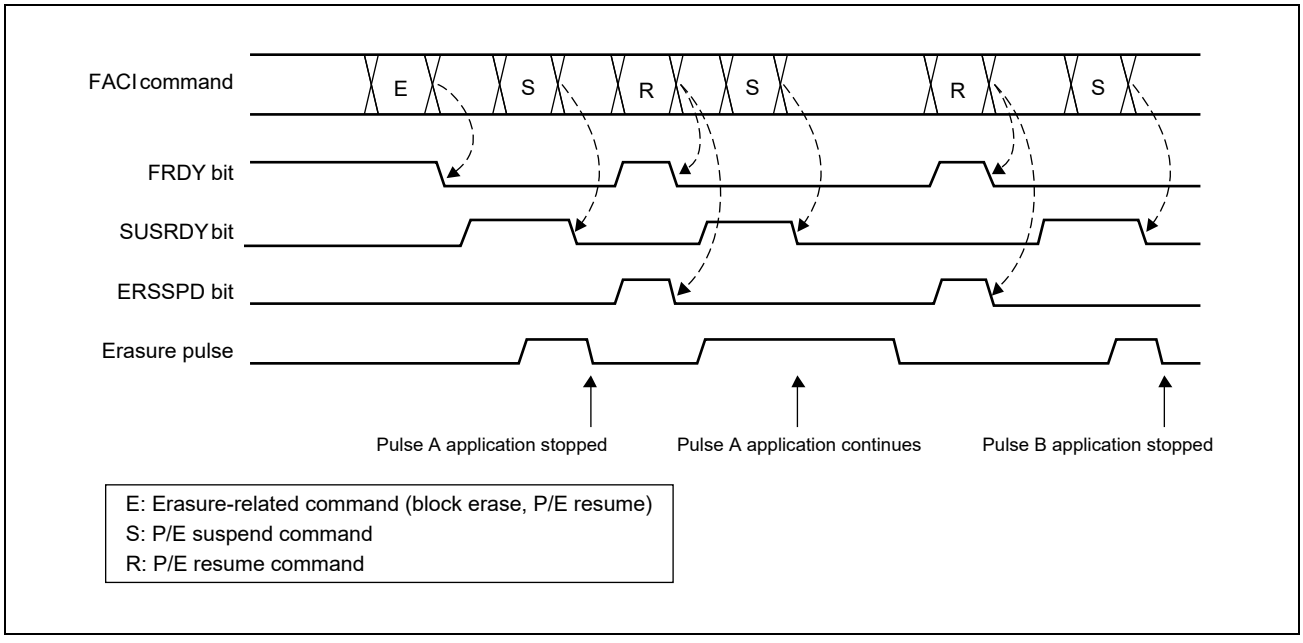


Figure 6.13 Suspension during Erasure (Suspension Priority Mode)

(3) Suspension during erasure (erasure priority mode)

This microcontroller has an erasure priority mode for the suspension of erasure. **Figure 6.14** shows the operation for suspending erasure when the erasure suspend mode is set to the erasure priority mode (the ESUSPMD bit in the FCPSR register is 1). The method for controlling erasure pulses in erasure priority mode is the same as the method for controlling programming pulses in programming suspend processing.

If the flash sequencer receives a P/E suspend command while an erasure pulse is being applied, the flash sequencer continues applying the pulse. In this mode, the required time for the whole erasure process can be reduced compared with the suspension priority mode because the reapplication of erasure pulses does not occur when a P/E resume command is issued.

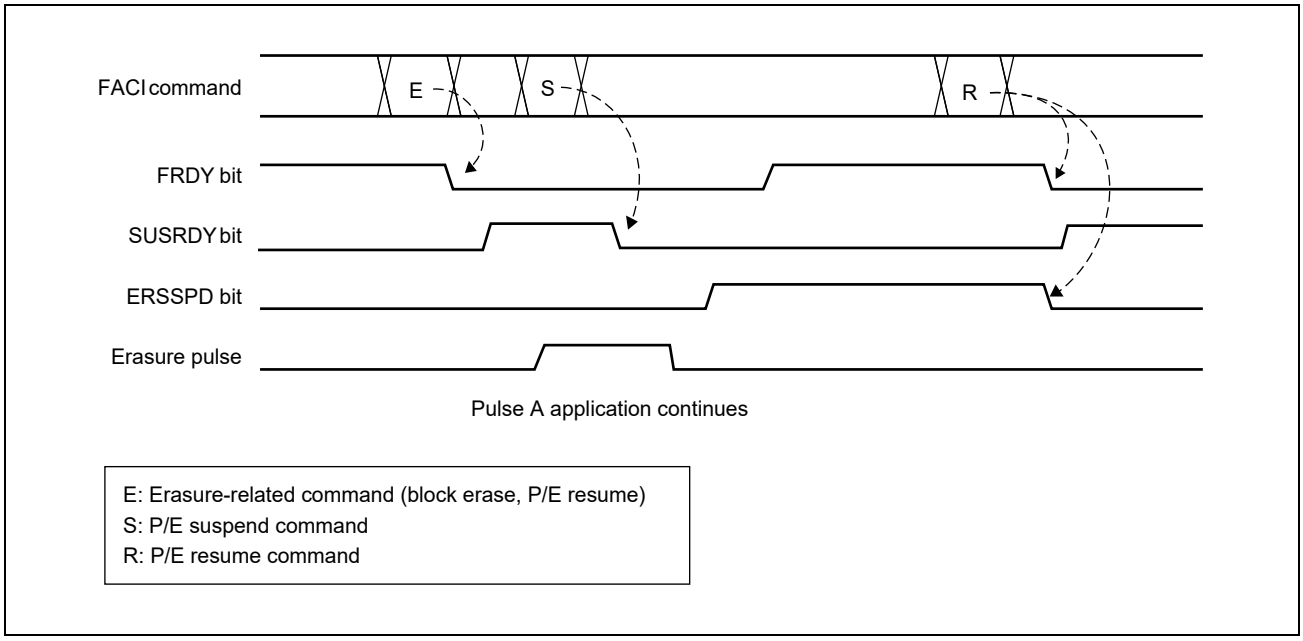
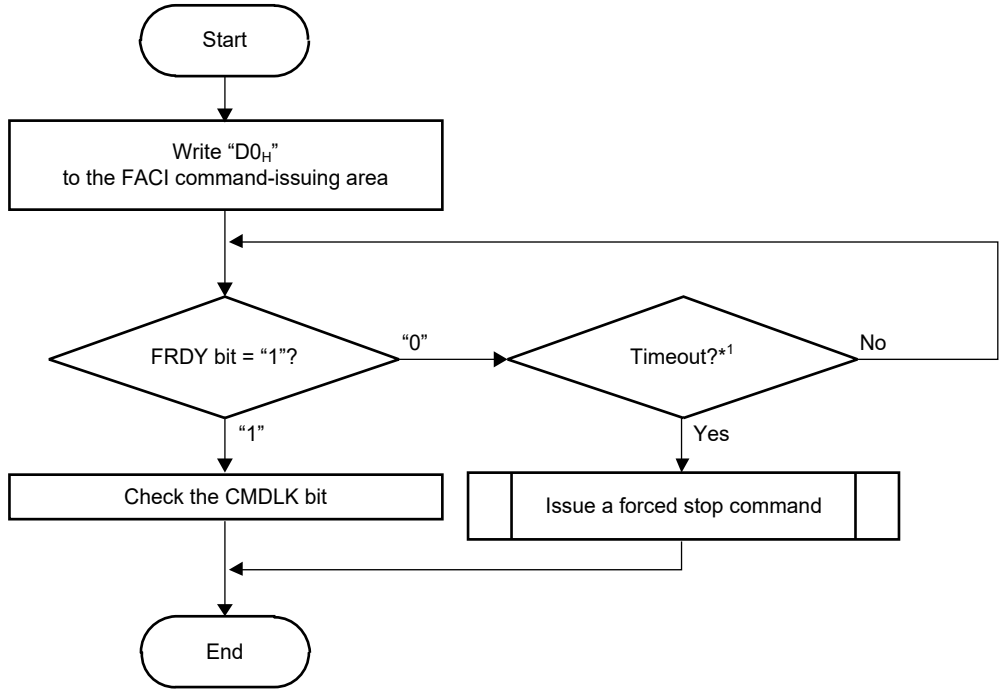


Figure 6.14 Suspension during Erasure (Erasure Priority Mode)

6.3.12 P/E Resume Command

To resume suspended programming/erasure processing, use the P/E resume command. If the settings of the FENTRYR register are changed during suspension, reset FENTRYR to the value immediately before the P/E suspend command was issued, and then issue a P/E resume command.



Note 1. Processing of an FACI command reaching 1.1 times the maximum processing time (see **Section 11, Electrical Characteristics**) can be considered a timeout. If common processing is used, 1.1 times the maximum erasure time for a 32 KB block of code flash memory can be considered a timeout.

Figure 6.15 Usage of the P/E Resume Command

6.3.13 Status Clear Command

The status clear command is used to clear the command-locked state (see **Section 6.3.7, Recovery from the Command-Locked State**) by clearing the OTPDTCT, ILGLERR, ERSERR, PRGERR, CFGDTCT, and TBLDTCT bits in the FSTATR register. The status clear command can also be used to clear the 1-bit correction flags (the OTPCRCT, CFGCRCT, and TBLCRCT bits), which do not cause a transition to the command-locked state.

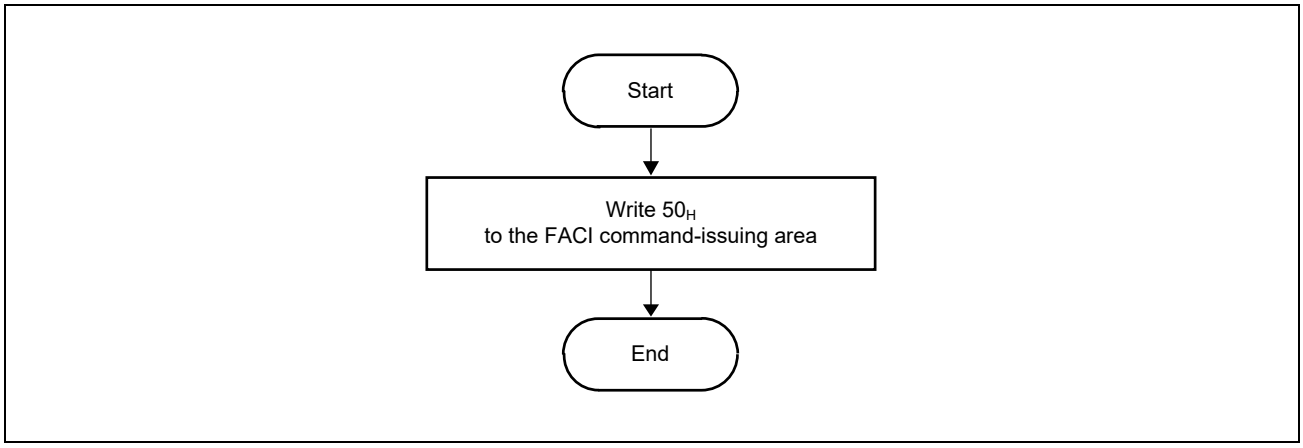
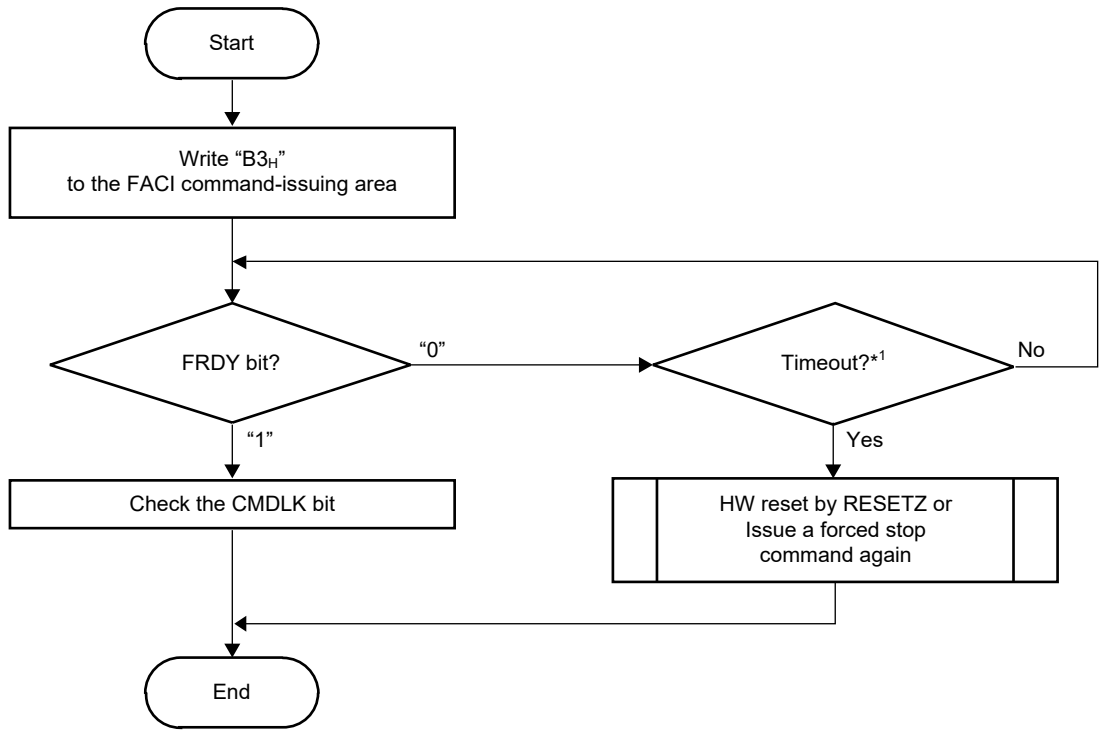


Figure 6.16 Usage of the Status Clear Command

6.3.14 Forced Stop Command

The forced stop command forcibly ends the command processing of the flash sequencer. Although this command halts command processing more quickly than the P/E suspension command, values from the programming or erasure that was in progress are not guaranteed. Furthermore, it is not possible to resume processing after issuing the forced stop command. The programming or erasure that was halted by the forced stop command is considered to be one round of programming (one “time”).

Executing a forced stop command also initializes part of the FACI, the whole FCU, and the FSTATR register. Accordingly, this command can be used to recover from the command-locked state and a time- out of the flash sequencer (see **Section 6.3.7, Recovery from the Command-Locked State**).



Note 1. The forced stop command latency (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout.

Figure 6.17 Usage of the Forced Stop Command

- Issuing the Forced Stop Command while Another Command is Being Issued

  If a timeout of the programming command occurs when checking the DBFULL bit, or a timeout occurs by the judgment of DBFULL bit or EBFULL bit at ECC Errors injection, or the forced stop command is used to suspend processing when a timeout of the DMA programming command occurs, writing to the FACI command-issuing area may be handled as writing of data by the programming command. If this is the case, read the FACI command-issuing area to intentionally lock commands and issue the forced stop command by following the procedure for returning from the command-locked state. Any read access sizes of 8 bit/16 bit/32 bit to command-issuing are able to lock commands.

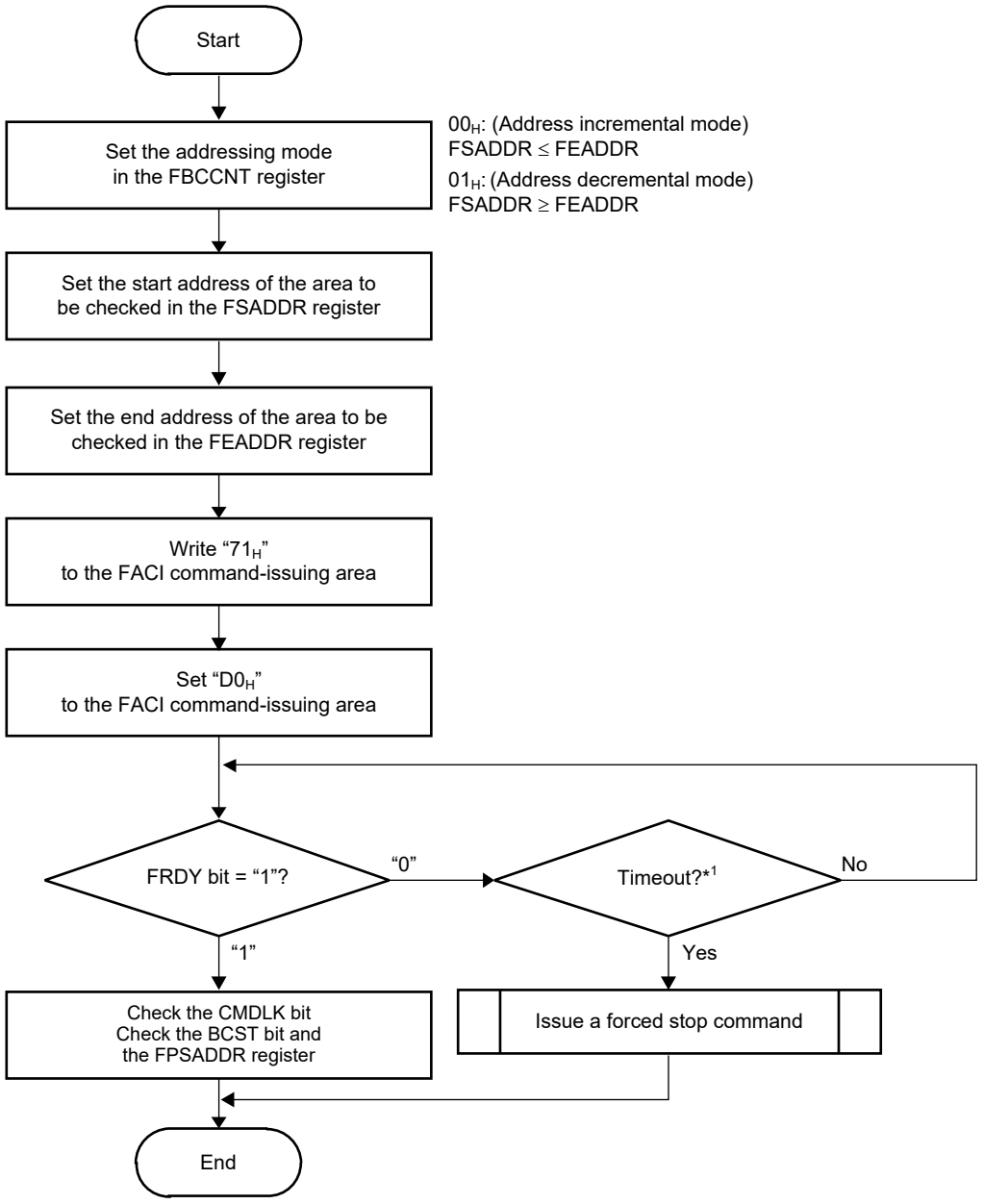
6.3.15 Blank Check Command

Values read from data flash memory area that has been erased but not yet programmed again (i.e. that is in the non-programmed state) are undefined. Use the blank check command when you need to confirm that an area is in the non-programmed state. For how to confirm the non-programmed state of the code flash memory, see **Section 8.5, Blank Checking of Code Flash Memory**.

Before issuing a blank check command, set the addressing mode, start address, and end address of the target area for blank checking to the FBCCNT, FSADDR, and FEADDR registers. When incremental mode is selected as the addressing mode for blank checking (i.e. when FBCCNT.BCDIR = 0), the address specified in FEADDR should be larger than the address in FSADDR. Conversely, the address in FEADDR should be smaller than the address in FSADDR when decremental mode is selected as the addressing mode for blank checking (i.e. when FBCCNT.BCDIR = 1). If the settings of the BCDIR bit, FSADDR, and FEADDR are inconsistent, the flash sequencer enters the command-locked state. The size of the target area for blank checking is in the range of 4 bytes to 64 KB and is set in units of 4 bytes. Then, make sure to set blank check area not crossing boundary 64 KB (0 $FFFF_H$ / 1 0000_H, 1 $FFFF_H$ / 2 0000_H, 2 $FFFF_H$ / 3 0000_H). If blank check is processed crossing over 64 KB boundary, blank check result is not guaranteed. (RH850/F1KH-D8, F1KM-S4, F1KM-S2)

Write 71_H and $D0_H$ to the FACI command-issuing area to start blank checking. Completion of processing can be confirmed by the FRDY bit of the FSTATR register. At the end of processing, the result of blank checking is stored in the BCST bit in the FBCSTAT register. If the target area for blank checking includes areas where programming has been completed, the flash sequencer stores the address of the first such area it detects in the FPSADDR register.

The erasure state can be checked by using this command only for an area for which erasure processing has been correctly completed. If erasure is not correctly completed (for example, due to a reset input or power shutdown), the erasure state cannot be checked by using this command.

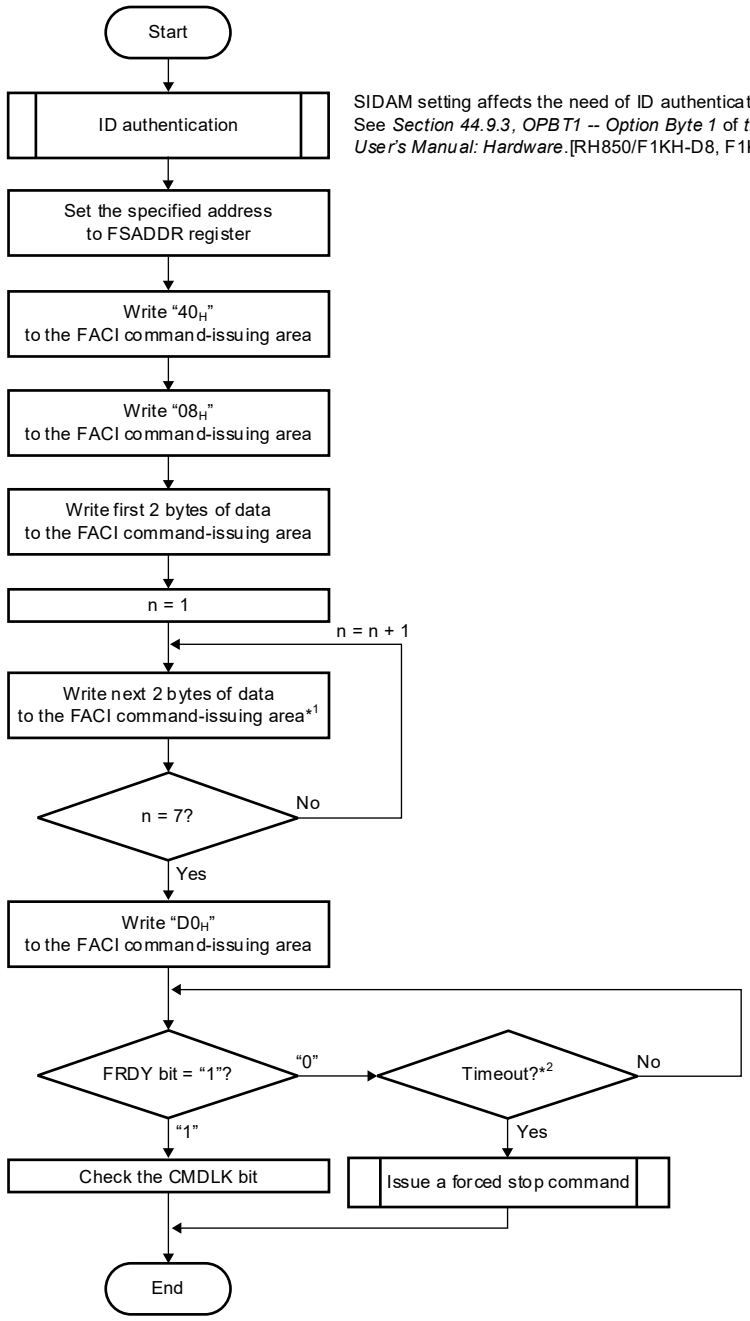


Note 1. The blank checking time (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout.

Figure 6.18 Usage of the Blank Check Command

6.3.16 Configuration Setting Command

The configuration setting command is used to set the ID, security function, safety function, and option bytes. Before issuing a configuration setting command, set the specified address (shown in **Table 6.5**) in the FSADDR register. Writing $D0_H$ to the FACI command-issuing area at the final access for issuing the FACI command starts processing the configuration setting command.



Note 1. Please set the "1" for reserved area.

Note 2. The time reaching 170 ms (f_{PCLK} ≥ 20 MHz) is judged as a timeout.

Figure 6.19 Usage of the Configuration Setting Command

The correspondence between the possible target data for configuration setting and the address value set in the FSADDR register is shown in **Table 6.5**. Once 0 is set as data in the security setting area, it cannot be changed to 1. Data in other areas can be changed to any value each time the configuration setting command is executed.

Table 6.5 Addresses Used by Configuration Setting Command

Address	Setting Data
FF30 0070$_H$	Option byte 0, Option byte 1*1
FF30 0060$_H$	Variable reset vector
FF30 0050$_H$	ID for authentication
FF30 0040$_H$	Security

Note 1. The setting data is as follows ("n" is in **Figure 6.19**)
n = 0 : Bit 15 to 0 of Option byte 0
n = 1 : Bit 31 to 16 of Option byte 0
n = 2 : Bit 15 to 0 of Option byte 1
n = 3 : Bit 31 to 16 of Option byte 1

Table 6.6 lists the security setting data when various security functions are enabled.

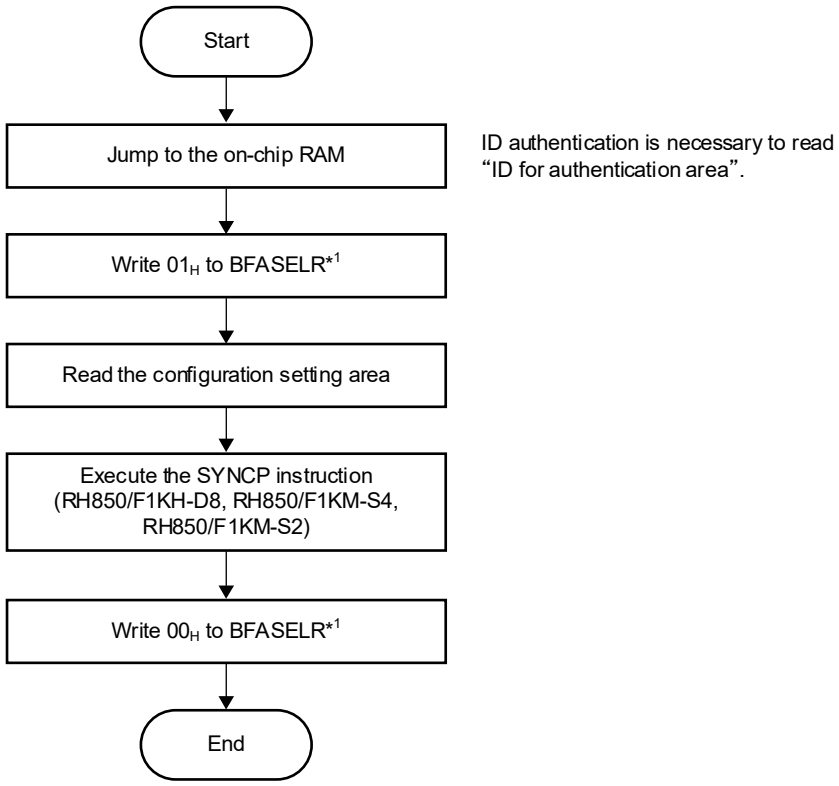
Table 6.6 List of Security Setting Data

Security Functions	Security Setting Data (16 Bytes)
ID authentication enabled in serial programming mode	FFFF FFFF FFFF FFFF FFFF FFFF 1EFF FFFF$_H$
Serial programmer connection disabled	FFFF FFFF FFFF FFFF FFFF FFFF F7FF FFFF$_H$
Block erase command disabled	FFFF FFFF FFFF FFFF FFFF FFFF DFFF FFFF$_H$
Programming command disabled	FFFF FFFF FFFF FFFF FFFF FFFF BFFF FFFF$_H$
Read command disabled	FFFF FFFF FFFF FFFF FFFF FFFF 7FFF FFFF$_H$

For details of the option byte, see *Section 37.9, Option Bytes* of *the RH850/F1K User's Manual: Hardware* or *Section 44.9, Option Bytes* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

6.3.17 Reading the Configuration Setting Area

To read the configuration setting area to check the values written by the configuration setting command, etc., set the BFAA bit in the BFASELR register to 1. Since setting the BFAA bit to 1 disables reading the user area, the software for reading the configuration setting area must be executed on the on-chip RAM. See **Table 6.5** in **Section 6.3.16, Configuration Setting Command** for the address map in the configuration setting area.



Note 1. When writing to the BFASELR register, see **Section 10, Usage Notes**, **(7) Updating the BFASELR register**, to access this register.

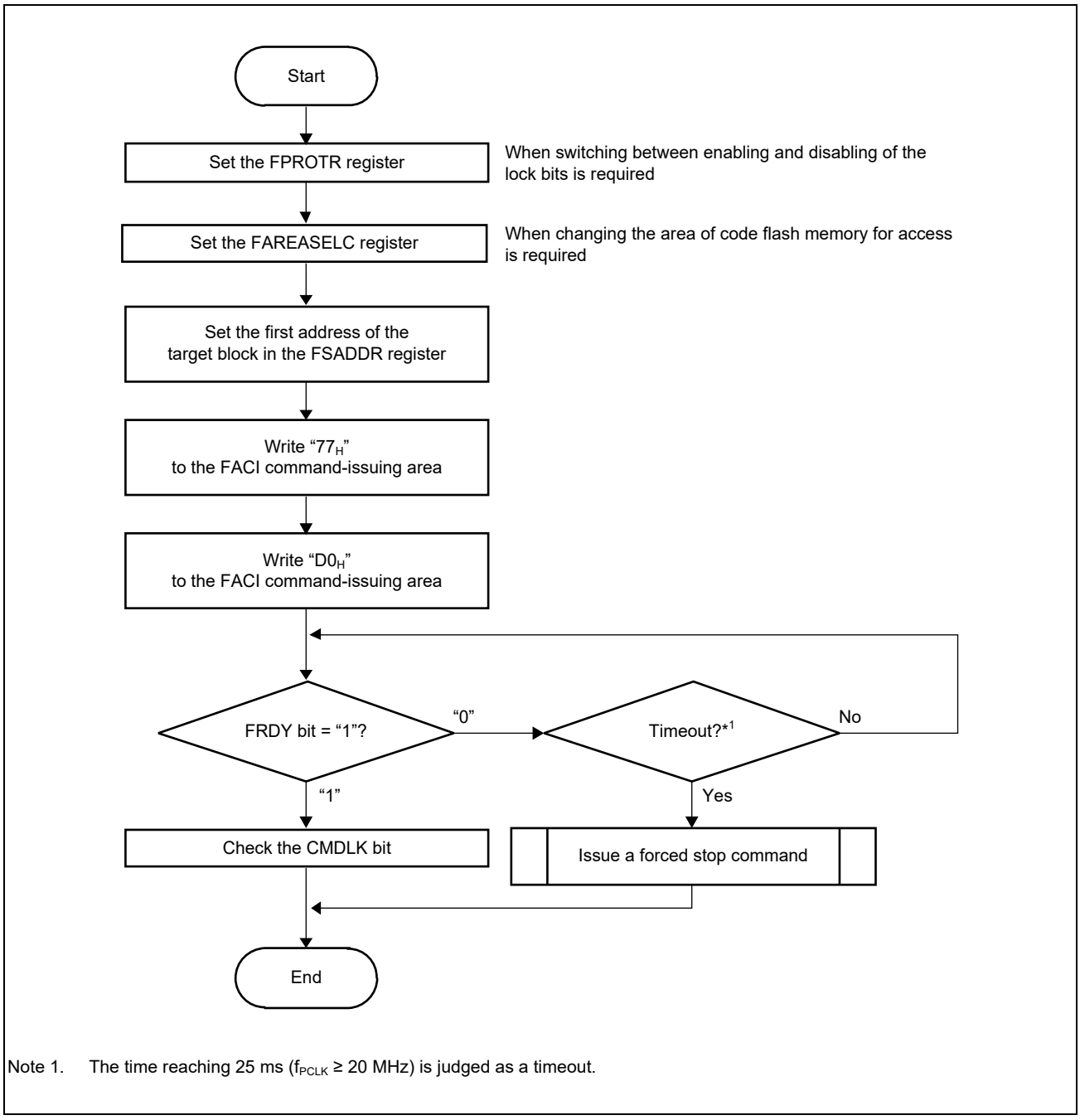
Figure 6.20 Flow for Reading the Configuration Setting Area

6.3.18 Lock-Bit Programming Command

To write to a lock bit, use the lock-bit programming command. To erase a lock bit, use the block erase command (see **Section 6.3.10, Block Erase Command**).

Before issuing a lock-bit programming command, set the first address of the target block in the FSADRR register. Writing 77_H and $D0_H$ to the FACI command-issuing area starts the processing of the lock-bit programming command.

The FPROTR and FAREASELC registers must be set before issuing a lock-bit programming command. To switch between enabling and disabling the lock bits, the setting of the FPROTR register must be changed. To switch the target area for programming the code flash memory, the setting of the FAREASELC register must be changed.



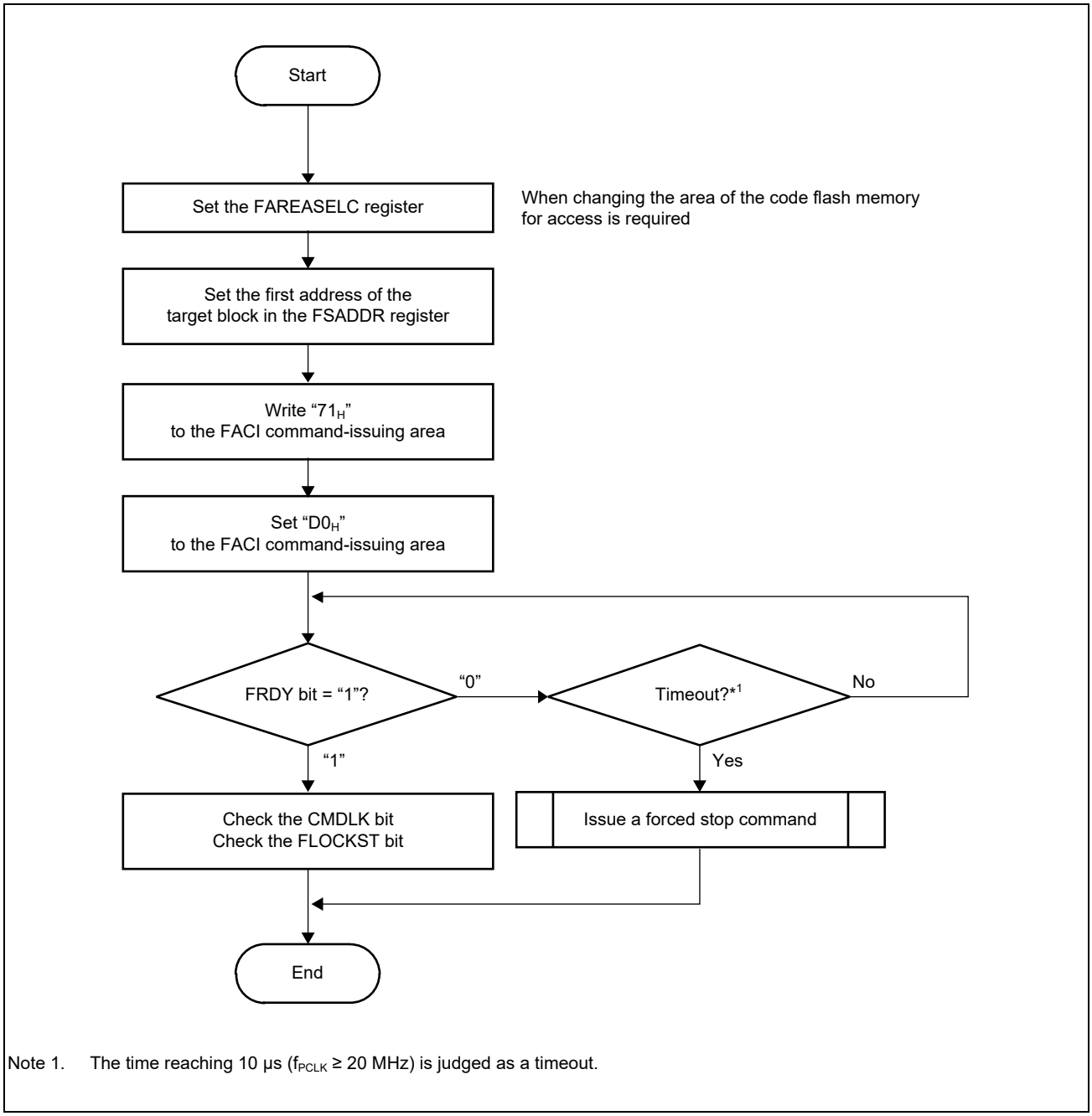
Note 1. The time reaching 25 ms (f_{PCLK} ≥ 20 MHz) is judged as a timeout.

Figure 6.21 Usage of the Lock-Bit Programming Command

6.3.19 Lock-Bit Read Command

To read a lock bit, use the lock-bit read command.

Before issuing a lock-bit read command, set the first address of the target block in the FSADDR register. Writing 71_H and $D0_H$ to the FACI command-issuing area starts the processing of the lock-bit read command. Completion of command processing can be confirmed by the FRDY bit of the FSTATR register. After command processing is completed, the result of reading the lock bit is stored in the FLOCKST bit in the FLKSTAT register.

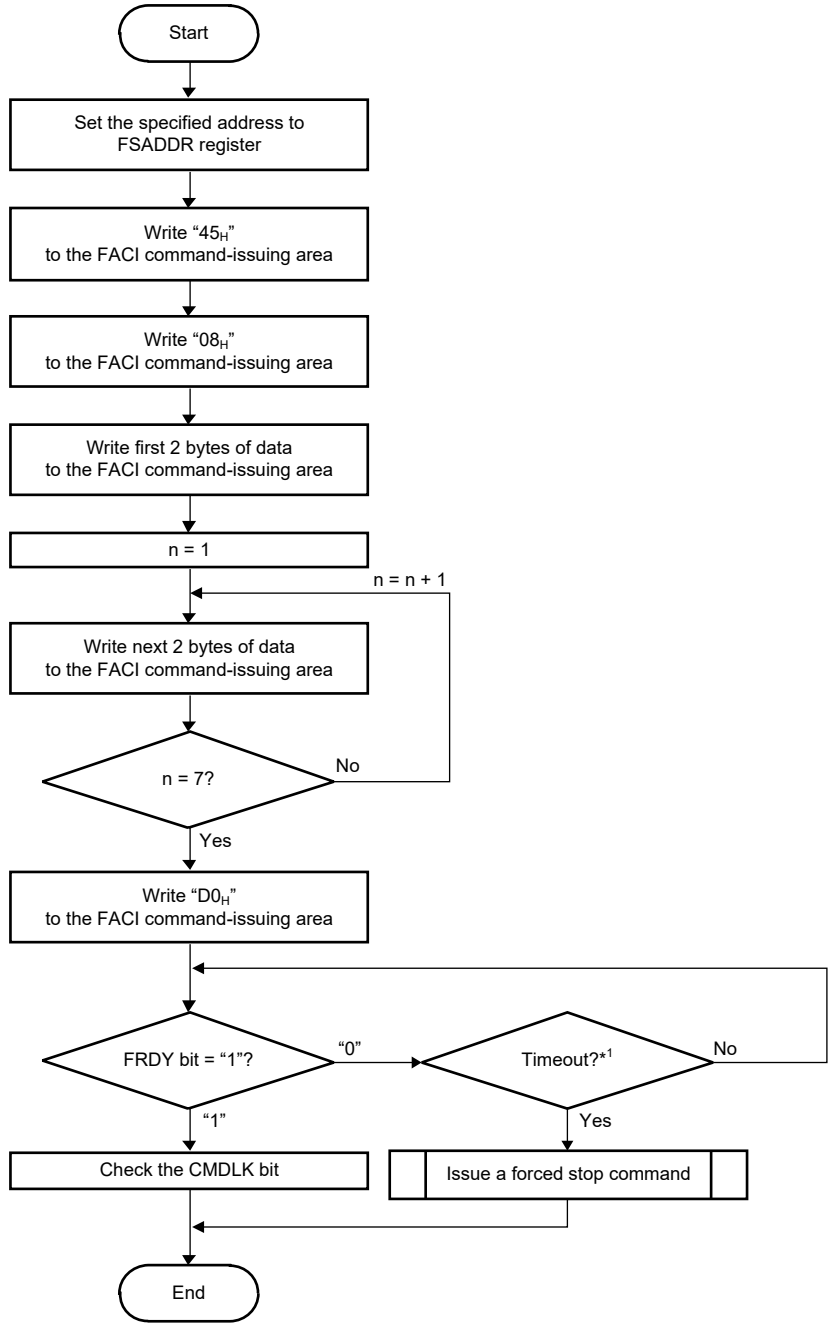


Note 1. The time reaching 10 µs (f_{PCLK} ≥ 20 MHz) is judged as a timeout.

Figure 6.22 Usage of the Lock-Bit Read Command

6.3.20 OTP Setting Command

The OTP setting command is used to set one-time programming (OTP). Before issuing the OTP setting command, set the specified address (shown in **Table 6.7**) in the FSADRR register. Writing $D0_H$ to the FACI command-issuing area upon the final access for issuing the FACI command starts the processing of the OTP setting command.



Note 1. The time reaching 120 ms (f_{PCLK} ≥ 20 MHz) is judged as a timeout.

Figure 6.23 Usage of the OTP Setting Command

Figure 6.24 shows the relationship between the user area blocks and OTP setting flags. An OTP setting flag (OTPF0 to OTPF517) is allocated to each user area block (8 KB × 8 blocks and 32 KB × 510 blocks). The number of blocks that are actually implemented differs from product to product. See *Section 37, Flash Memory* of *the RH850/F1K User's Manual: Hardware* or *Section 44, Flash Memory* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

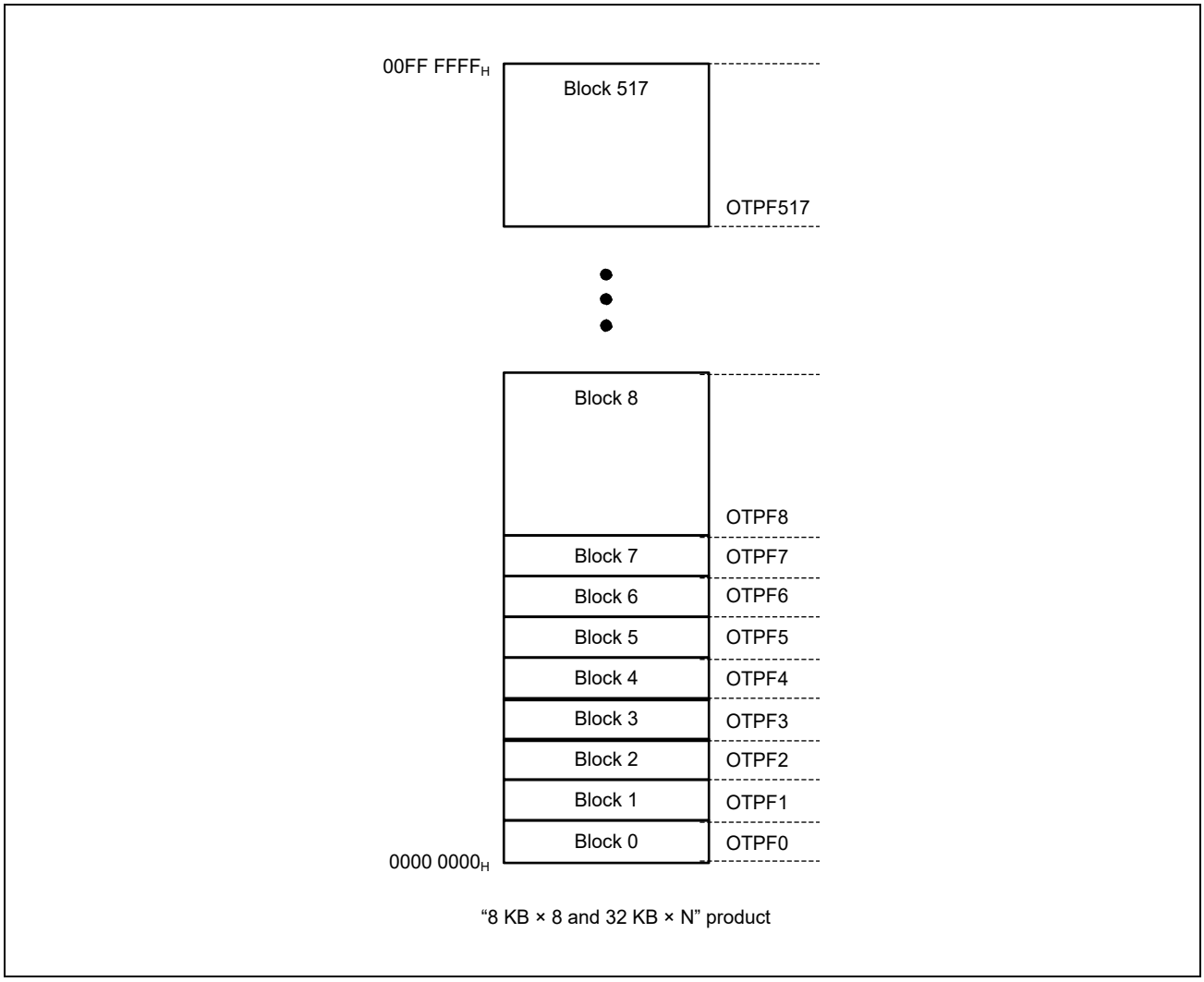


Figure 6.24 Relationship between User Area Blocks and OTP Setting Flags

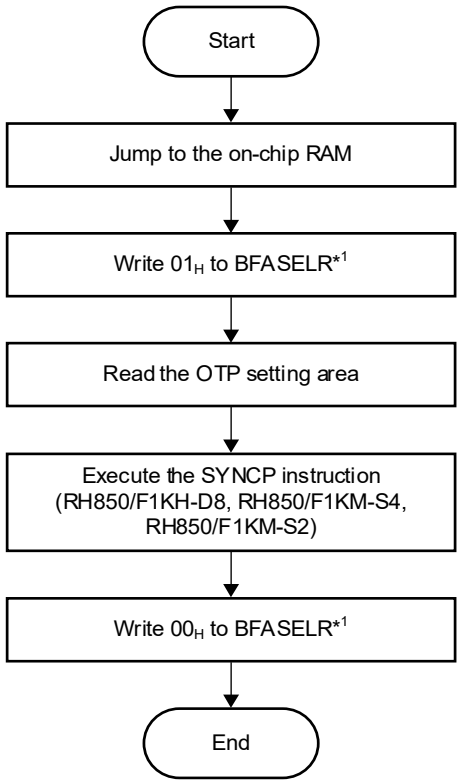
Table 6.7 shows the addresses to be used for the OTP setting command. When 0 is set to a flag, OTP is set for the corresponding block. Once 0 is set to a flag, it cannot be changed to 1.

Table 6.7 Addresses Used for OTP Setting Command

Address	Set Data
FF38 0090$_H$	OTP flag for extended user area (bit 0)
FF38 0080$_H$	OTPF517 (bit 5) to OTPF512 (bit 0)
FF38 0070$_H$	OTPF511 (bit 127) to OTPF384 (bit 0)
FF38 0060$_H$	OTPF383 (bit 127) to OTPF256 (bit 0)
FF38 0050$_H$	OTPF255 (bit 127) to OTPF128 (bit 0)
FF38 0040$_H$	OTPF127 (bit 127) to OTPF0 (bit 0)

6.3.21 Reading the OTP Setting Area

To read the OTP setting area to check the values written by the OTP setting command, etc., set the BFAA bit in the BFASELR register to 1. Since setting the BFAA bit to 1 disables reading the user area, the software for reading the OTP setting area must be executed on the on-chip RAM. See **Table 6.7** in **Section 6.3.20, OTP Setting Command**, for the address map in the OTP setting area.



Note 1. When writing to the BFASELR register, see **Section 10, Usage Notes**, **(7) Updating the BFASELR register**, to access this register.

Figure 6.25 Flow for Reading the OTP Setting Area

6.3.22 Injecting ECC Errors in the Flash Memory

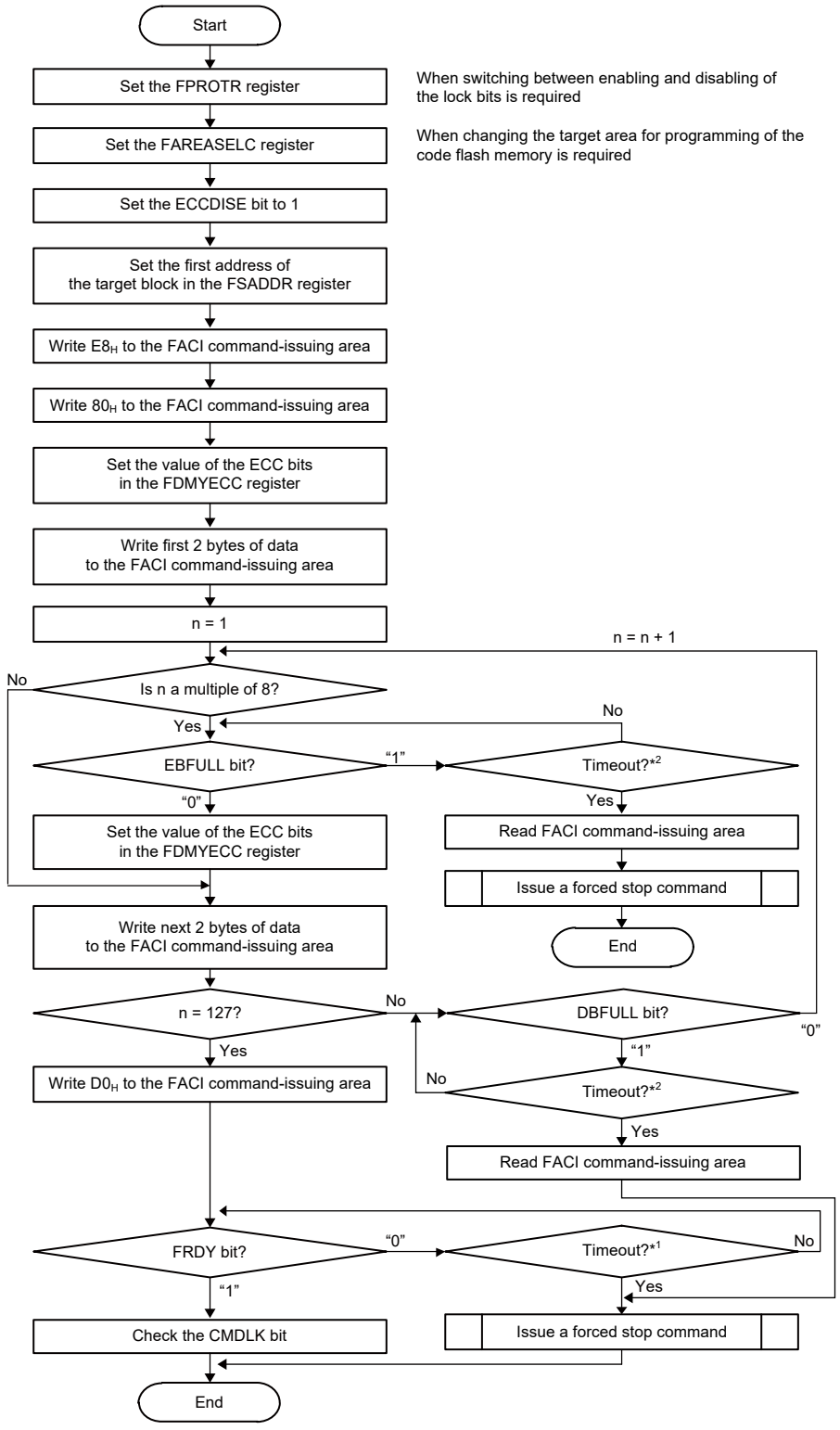
Any value of the ECC bits in the FDMYECC register can be written to the flash memory by using a programming command.

Before writing the value set in the FDMYECC register to the flash memory, set the ECCDISE bit in the FECCTMD register to 1. In addition, set the values of the ECC bits in the FDMYECC register before writing the data to the FACI command issuing area.

For code flash memory, the unit for writing by using the programming command (256 bytes) differs from the unit in which ECC bits are added to data (16 bytes). Therefore, every time 16 bytes of data are written to the FACI command issuing area, change the setting in the FDMYECC register.

For data flash memory, since the unit for writing by using the programming command (4 bytes) is same as the unit of data to which ECC bits are added (4 bytes), only change the setting in the FDMYECC register once before issuing the programming command.

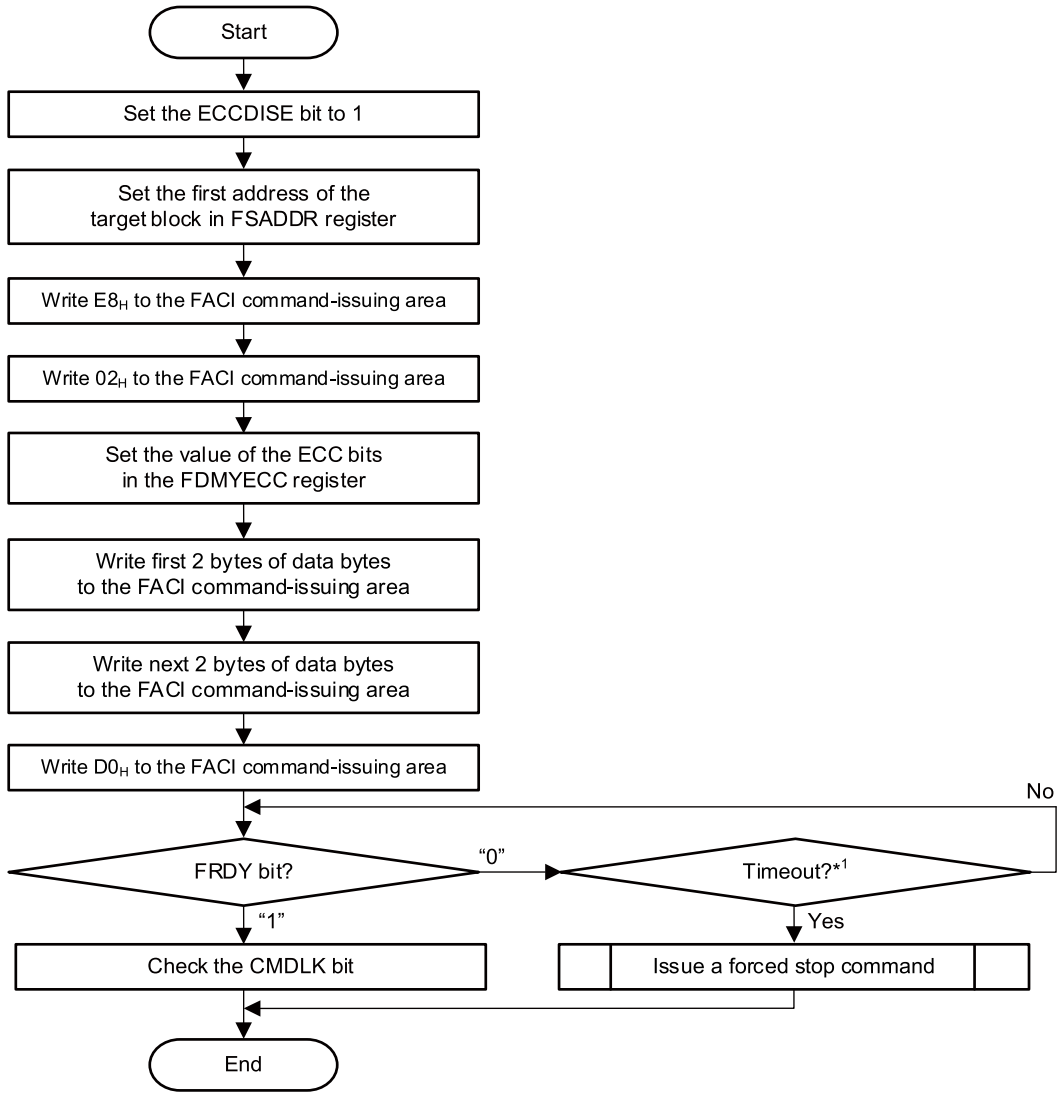
Issuing a command to write to the FDMYECC register while the FDMYECC buffer in the FACI is full may lead to a wait being generated on the P-Bus, which will affect the communication performance with other peripheral IP modules. To avoid the generation of a wait, write to the FDMYECC register while the EBFULL bit in the FSTATR register is 0.



Note 1. The time of 256-byte programming (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout.

Note 2. The time reaching 5 µs (f_{PCLK} ≥ 20 MHz) is judged as a timeout.

Figure 6.26 Injecting an ECC Error to the Code Flash Memory



Note 1. The time of 4-byte programming (the maximum time: see **Section 11, Electrical Characteristics**) reaching 1.1 times is judged as a timeout.

Figure 6.27 Injecting an ECC Error to the Data Flash Memory

Section 7 Security Functions

7.1 FACI Command Protection by ID Authentication

In code flash P/E mode, FACI commands can be used after security is unlocked by ID authentication. SIDAM setting affects the need of ID authentication. See *Section 44.9.3, OPBT1 -- Option Byte 1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.[RH850/F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1] When an FACI command is issued while the IDST bit in the SELFIDST register is set to 1 (security- locked state), the flash sequencer enters the command-locked state. For how to unlock security by ID authentication, see **Section 6.3.6, ID Authentication**. The ID used for authentication in code flash P/E mode is the same as that used for connecting an on-chip debugger or serial programmer (while ID authentication is enabled).

In data flash P/E mode without configuration setting command, FACI commands can be used regardless of the IDST bit setting.

The protection of configuration setting command by ID authentication is same as the protection of FACI command in code flash P/E mode.

7.2 OTP for Code Flash Memory

OTP can be set independently for each block in the code flash memory. Once an OTP is set, it cannot be cleared. If a programming, block erase, or lock-bit programming command is issued to a block set for OTP, the flash sequencer enters the command-locked state.

Once an OTP setting command has been executed on a chip, the variable reset vector cannot be placed in the corresponding area by using the configuration setting command. Even when the OTP setting command is executed for a reserved area in the code flash memory or the OTP setting command is executed with all bits set to 1, the variable reset vector cannot be set in an area set for OTP.

Section 8 Safety Functions

8.1 Hardware Protection

While a low level is being input to the FLMD0 pin, the setting of the FWE bit in the FPMON register is 0. When the FWE bit is 0, writing 1 to the FENTRYC bit in the FENTRYR register is disabled. Since a transition to code flash P/E mode is not possible, programming and erasing the code flash memory are prohibited. When the FRDY bit is 1 while the FLMD0 pin is at low level, the flash sequencer clears the FENTRYC bit to disable programming and erasing of the code flash memory.

When the FLMD0 pin is changed to low level while the FRDY bit in the FSTATR register is 0, the flash sequencer continues processing a command that is in progress. Even while continuing command processing the flash sequencer can accept requests to suspend programming and erasure.

To restart programming or erasure, set the FENTRYC bit again and issue the P/E resume command.

8.2 Software Protection

Software protection disables programming and erasure for the code flash memory by setting the control registers and lock bit in the user area. If an attempt is made to issue an FACI command to an area for which software protection is set, the flash sequencer enters the command-locked state.

8.2.1 FENTRYR-based Protection

When the FENTRYR register is set to "0000_H", the flash sequencer is set to read mode. In read mode, FACI commands cannot be acknowledged. If an attempt is made to issue an FACI command in read mode, the flash sequencer enters the command-locked state.

8.2.2 Lock-bit–based Protection

Each block in the user area and extended user area has a lock bit. When the FPROTCN bit in the FPROTR register is 0, blocks whose lock bit is set to 0 are prohibited from being programmed and erased. To program or erase blocks whose lock bit is set to 0, set the FPROTCN bit to 1. If an attempt is made to issue a code flash memory programming, block erase or lock-bit programming command to a block whose lock bit is set, the flash sequencer enters the command-locked state.

8.3 Error Protection

Error protection detects illegal FACI commands, illegal access, and flash sequencer malfunction. FACI command acknowledgement is disabled (the command-locked state is entered) in response to the detection of these errors. The flash memory cannot be programmed or erased while the flash sequencer is in the command-locked state. For release from the command-locked state, issue a status clear or forced stop command while the CFAE and DFAE bits in the FASTAT register are 0. The status clear command can only be used while the FRDY bit in the FSTATR register is 1. The forced stop command can be used regardless of the value of the FRDY bit. While the CMDLKIE bit in the FAEINT register is 1, a flash access error (FLERR) interrupt is generated if the flash sequencer enters the command-locked state (the CMDLK bit in the FASTAT register is set to 1).

If the flash sequencer enters the command-locked state in response to a command other than the P/E suspend command during programming or erasure processing, the flash sequencer continues programming or erasure. In this state, the P/E suspend command cannot be used to suspend programming or erasure. If a command is issued in the command-locked state, the ILGLERR bit becomes 1 and the other bits retain the values set by previous error detection.

Table 8.1 shows error protection types and status bit values after error detection.

Table 8.1 Error Protection Type (1/2)

Error Type	Description	OTPDTCT	ILGLERR	ERSERR	PRGERR	CFGDTCT	TBLDTCT	CFAE	DFAE
FENTRYR setting error	The FENTRYR setting is other than 0000_H, 0001_H and 0080_H.	0	1	0	0	0	0	0	0
	The FENTRYR setting at suspension does not match the setting at resumption.	0	1	0	0	0	0	0	0
Illegal command error	An undefined code was written in the first access of an FACI command.	0	1	0	0	0	0	0	0
	The value specified in the last access of a multiple-access FACI command is not $D0_H$ (does not apply to DMA programming).	0	1	0	0	0	0	0	0
	The value (N) specified in the second write access of an FACI command during programming, DMA programming, configuration setting, or OTP setting command is incorrect (an odd value cannot be used for DMA programming).	0	1	0	0	0	0	0	0
	A blank check command was issued with inconsistent BCDIR, FSADDR, and FEADDR settings (see **Section 4.6, FACI Command End Address Register (FEADDR)**).	0	1	0	0	0	0	0	0
	An FACI command not acknowledged in the mode in question was issued (see **Table 6.3**).	0	1	0	0	0	0	0	0
	An FACI command was issued when command acknowledgement conditions were not satisfied (see **Table 6.4**).	0/1	1	0/1	0/1	0/1	0/1	0/1	0/1
Erase error	An error occurred during erasure.	0	0	1	0	0	0	0	0
	A block erase command was issued to a block whose lock bit is set.	0	0	1	0	0	0	0	0
Programming error	An error occurred during programming.	0	0	0	1	0	0	0	0
	A programming or lock-bit programming command has been issued against lock bit protection.	0	0	0	1	0	0	0	0
Code flash memory access violation	An FACI command has been issued to the reserved portion of the user area in code flash P/E mode (see **Section 4.5, FACI Command Start Address Register (FSADDR)**).	0	1	0	0	0	0	1	0
	An FACI command has been issued to the reserved portion of the extended user area in code flash P/E mode (see **Section 4.5, FACI Command Start Address Register (FSADDR)**).	0	1	0	0	0	0	1	0

Table 8.1 Error Protection Type (2/2)

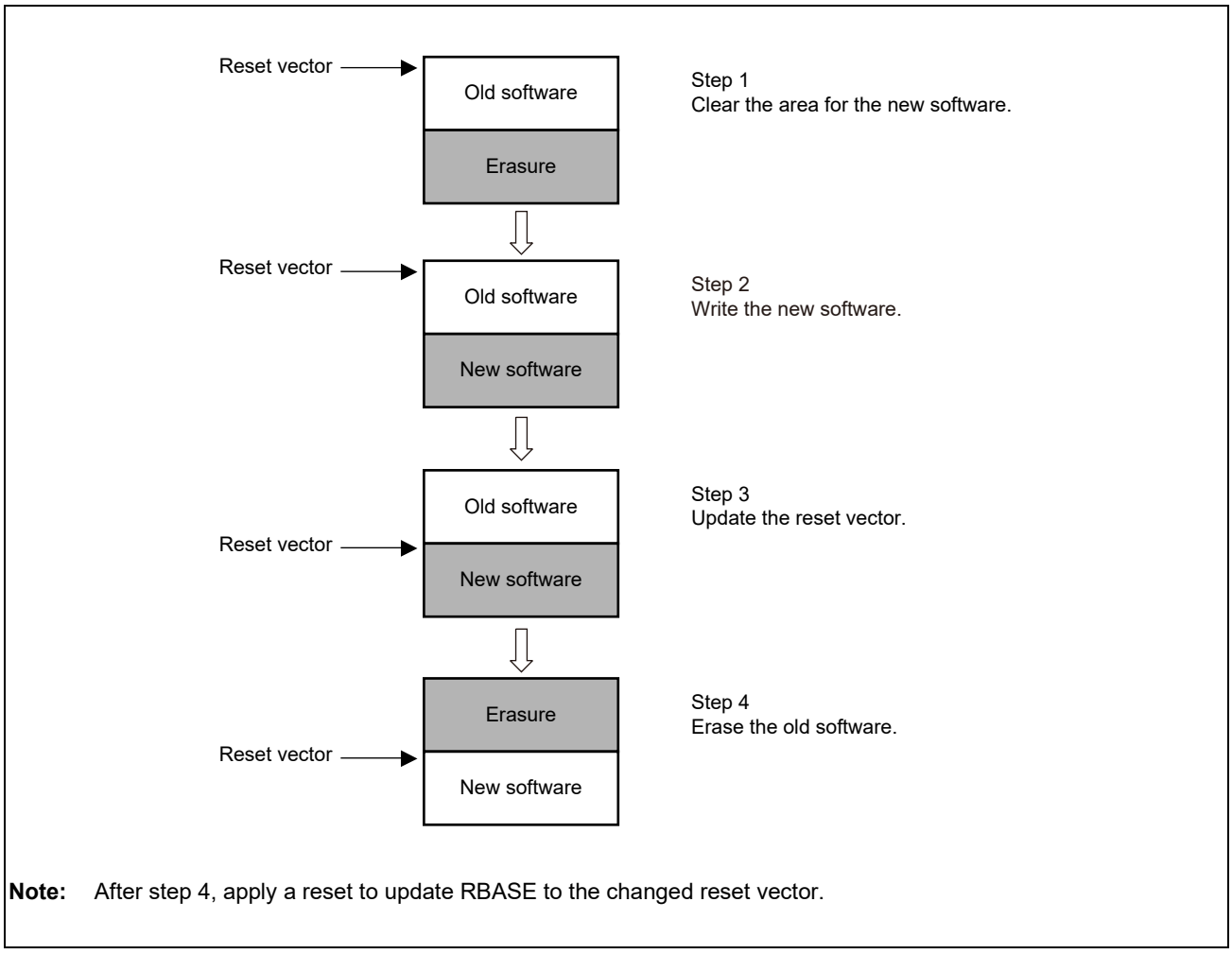
Error Type	Description	OTPDTCT	ILGLERR	ERSERR	PRGERR	CFGDTCT	TBLDTCT	CFAE	DFAE
Data flash memory access violation	An FACI command was issued to a reserved part of the data area in data flash P/E mode (see **Section 4.5, FACI Command Start Address Register (FSADDR)** and **Section 4.6, FACI Command End Address Register (FEADDR)**).	0	1	0	0	0	0	0	1
	A configuration setting command was issued to a reserved area (see **Section 4.5, FACI Command Start Address Register (FSADDR)**).	0	1	0	0	0	0	0	1
	An OTP setting command was issued to a reserved area (see **Section 4.5, FACI Command Start Address Register (FSADDR)**).	0	1	0	0	0	0	0	1
Security	A programming, block erase, or lock-bit programming command was issued to an area for which OTP is set.	0	1	0	0	0	0	0	0
	A configuration setting command was issued to place a variable reset vector in an area where OTP is set for the code flash memory.	0	1	0	0	0	0	0	0
	An FACI command was issued in code flash P/E mode in a state in which security is not unlocked by ID authentication.	0	1	0	0	0	0	0	0
	A configuration setting command was issued in a state in witch security is not unlocked by ID authentication.	0	1	0	0	0	0	0	0
Others	The FACI command-issuing area was accessed in read mode.	0	1	0	0	0	0	0	0
	The FACI command-issuing area was read in code flash P/E mode or data flash P/E mode.	0	1	0	0	0	0	0	0
OTP setting ECC error	A 2-bit error was detected when the OTP setting was read.	1	0	0	0	0	0	0	0
Configuration setting ECC error	A 2-bit error was detected when the configuration setting value was read.	0	0	0	0	1	0	0	0
Programming parameter ECC error	A 2-bit error was detected when the programming parameter table was read.	0	0	0	0	0	1	0	0

8.4 Boot Program Protection

8.4.1 Variable Reset Vector

Using a configuration setting command to change the value of the variable reset vector area may change the reset vector of the CPU. Using the variable reset vector when the boot program in the code flash memory is updated enables safe rewriting.

Once an OTP setting command has been executed on a chip, the variable reset vector cannot be placed in the corresponding area by using the configuration setting command. Even when the OTP setting command issued for a reserved area in the code flash memory is completed normally or execution of the OTP setting command is completed normally with all bits set to 1, the variable reset vector cannot be set in an area for which OTP is set.



Note: After step 4, apply a reset to update RBASE to the changed reset vector.

Figure 8.1 Software Update Using the Variable Reset Vector

8.5 Blank Checking of Code Flash Memory

Reading from an area of the code flash memory that has been erased but to which no new data has yet been written (an area in the non-programmed state) leads to an exception since an ECC error will be detected. In addition, as the values of the data are not guaranteed when an ECC error has occurred, confirm that the area is in the non-programmed state by checking whether all data bits and ECC bits for the code flash memory are set to 1.

For notes on using the ECC function for the code flash memory, see *Section 33, Functional Safety* of *the RH850/F1K User's Manual: Hardware* or *Section 40A, Functional Safety of RH850/F1KH-D8 or Section 40B, Functional Safety of RH850/F1KM-S4, RH850/F1KM-S2 or Section 40C, Functional Safety of RH850/F1KM-S1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

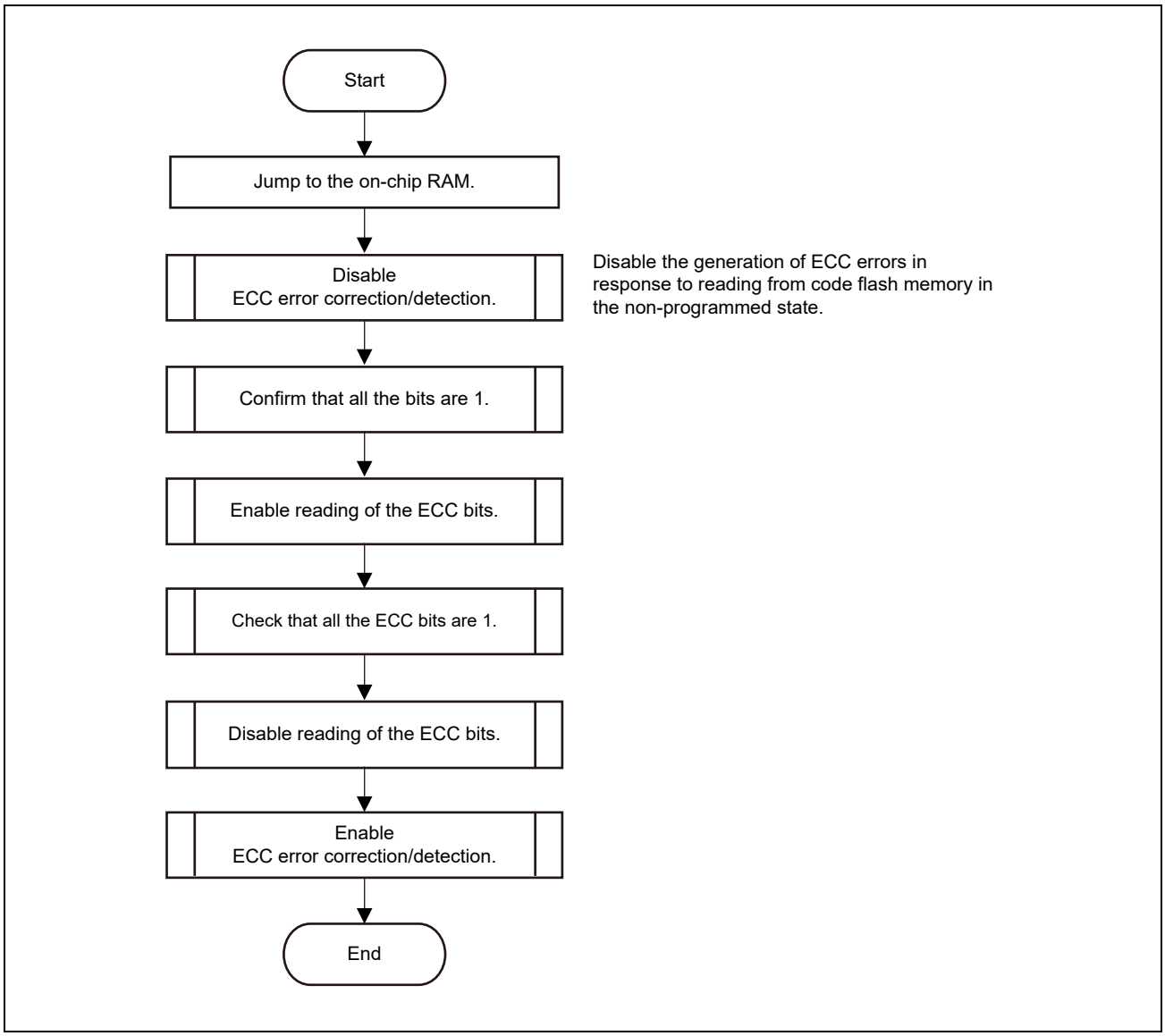


Figure 8.2 Blank Checking of Code Flash Memory

Section 9 PBG for Flash Memory Programming/Erasure

The control registers in the peripheral circuits are protected against illegal accesses. For details, see *Section 33.3.2, PBG* in *Section 33, Functional Safety* of *the RH850/F1K User's Manual: Hardware* or *Section 40A.3.3, PBG/HBG* in *Section 40A, Functional Safety of RH850/F1KM-D8 or Section 40B.3.3, PBG/HBG* in *Section 40B, Functional Safety of RH850/F1KM-S4, RH850/F1KM-S2 or Section 40C.3.2, PBG* in *Section 40C, Functional Safety of RH850/F1KM-S1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

The following table lists the peripheral circuits to be protected, the corresponding PBG group names, and the PBG channel numbers. Regarding FBUFCCTL and BFASELR, see *Section 33.3.3, PBG for CPU system* of *the RH850/F1K User's Manual: Hardware* or *Section 40A.3.4, PBG for CPU system* or *Section 40B.3.4, PBG for CPU system* or *Section 40C.3.3, PBG for CPU system* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware* .

Table 9.1 PBG groups Groups and Channels, and Target Modules

PBG Group	Group No.	PBG Channel Number	Protection Target Module	Target Register
PBG50	06	5	Flash memory (Self Programming)	SELFID0-3, SELFIDST
		6	Flash memory (Control)	FPMON, FASTAT, FAEINT, FAREASELC, FSADDR, FEADDR, FSTATR, FENTRYR, FPROTR, FSUINITR, FLKSTAT, FRTSTAT, FCMDR, FPESTAT, FBCCNT, FBCSTAT, FPSADDR, FCPSR, FPCKAR, FECCEMON, FECCTMD, FDMYECC, and FACI command-issuing area

The following table lists the registers provided for each PBG group.

Table 9.2 List of Registers

PBG Group	Group No.	Register Symbol	Register Name	R/W	Value after Reset	Address	Access Size	Power Domain
PBG50	06	FSGD06PROT5	PBG06 protection register 5	R/W	066F FFF7$_H$	FFF9 0014$_H$	8/16/32	ISO
		FSGD06PROT6	PBG06 protection register 6	R/W	066F FFF7$_H$	FFF9 0018$_H$	8/16/32	

NOTE

For details of registers, see *Section 33.3.2.2, Details of Registers* in *Section 33, Functional Safety* of *the RH850/F1K User's Manual: Hardware* or *Section 40A.3.3.2, Details of Registers* in *Section 40A, Functional Safety of RH850/F1KH-D8* or *Section 40B.3.3.2, Details of Registers* in *Section 40B, Functional Safety of RH850/F1KM-S4, RH850/F1KM-S2* or *Section 40C.3.2.2, Details of Registers* in *Section 40C, Functional Safety of RH850/F1KM-S1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware* .

Other than the registers mentioned above, there are register groups provided to report PBG errors. For the addresses of the PBG error registers, see *Table 33.38, List of PBG Error Registers* and *Table 33.39, PBG Group Numbers and Error Base Addresses* in *Section 33, Functional Safety* of *the RH850/F1K User's Manual: Hardware* or *Table 40A.81, List of PBG/HBG Error Registers* and *Table 40A.82, PBG Group Numbers and Error Base Addresses* in *Section 40A, Functional Safety of RH850/F1KH-D8* or *Table 40B.83, List of PBG/HBG Error Registers* and *Table 40B.84, PBG Group Numbers and Error Base Addresses* in *Section 40B, Functional Safety of RH850/F1KM-S4, RH850/F1KM-S2* or *Table 40C.56, List of PBG Error Registers and Table 40C.57, PBG Group Numbers and Error Base Addresses* in *Section 40C, Functional Safety of RH850/F1KM-S1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware* . The base address of PBG error registers is determined by the group number. For details of the error registers, see *Section 33.3.2.2, Details of Registers* in *Section 33 Functional Safety* of *the RH850/F1K User's Manual: Hardware* or *Section 40A.3.3.2, Details of Registers* in *Section 40A Functional Safety of RH850/F1KH-D8* or *Section 40B.3.3.2,*

Details of Registers in *Section 40B Functional Safety of RH850/F1KM-S4, RH850/F1KM-S2 or Section 40C.3.2.2, Details of Registers* in *Section 40C Functional Safety of RH850/F1KM-S1* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware* .

Section 10 Usage Notes

(1) Reading areas where programming or erasure was interrupted

When programming or erasure of an area of flash memory is interrupted, the data stored in the area become undefined. To avoid undefined data that are read out becoming a source of faulty operation, avoid fetching instructions or reading data from areas where programming or erasure was interrupted.

(2) Prohibition of additional writing

Writing to a given area twice is not possible. If you want to overwrite data in an area of flash memory that has already been written, erase the area first.

(3) Resets during programming and erasure

For external reset during programming and erasure, release the device from the reset state after the reset input period of at least the minimum low level width of the $\overline{\text{RESET}}$ input signal once the operating voltage is within the range stipulated in the electrical characteristics.

(4) Allocation of vectors for interrupts and other exceptions during programming and erasure

Generation of an interrupt or other exception during programming or erasure may lead to fetching a vector from the code flash memory. If this does not satisfy the conditions for using background operations, set the address for vector fetching to an address that is not in the code flash memory. For how to change the vector address of the exception handler, see *Section 3, CPU System*, and *Section 7, Exception/Interrupts* of *the RH850/F1K User's Manual: Hardware* or *RH850/F1KH, RH850/F1KM User's Manual: Hardware* .

(5) Abnormal termination of programming and erasure

Even if programming/erasure ends abnormally due to an external reset, etc., the programming/erasure state of the flash memory with undefined data cannot be verified or checked. For areas in which programming/erasure has ended abnormally, the blank check function cannot judge whether the area has been erased successfully or not. Erase the area again to verify that the corresponding area is completely erased before using it.

If programming and erasure of code flash memory are not completed normally, the lock bit for the target area may be enabled (locked). In such cases, erase the block to erase the lock bit while the lock bit is in the disabled state (the area is not locked).

(6) Prohibitions during programming, erasure and blank checking

Do not do the following while the flash memory is being programming, erasure and blank checking.

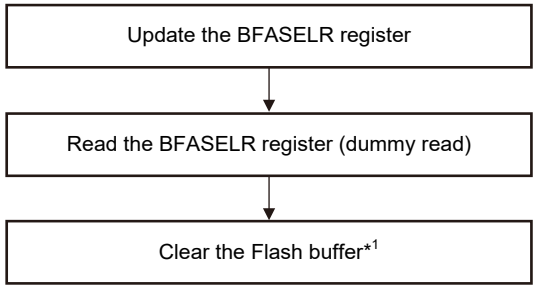
- Have the operating voltage from the power supply go beyond the allowable range.
- Change the operating frequency (f_{PCLK}*1) of the flash sequencer.

Note 1. [RH850/F1KH-D8,F1KM-S4,F1KM-S2]
f_{PCLK} = 1/8 f_{CPUCLK_H} (CPU operating frequency)
(CKDIVMD = 1*2 or products of CPU frequency 160 MHz max)
f_{PCLK} = 1/4 f_{CPUCLK_H} (CPU operating frequency) (CKDIVMD = 0*2)
[RH850/F1K, F1KM-S1]
f_{PCLK} = 1/4 f_{CPUCLK} (CPU operating frequency)

Note 2. See *Section 44.9, Option Bytes* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

(7) Updating the BFASELR register

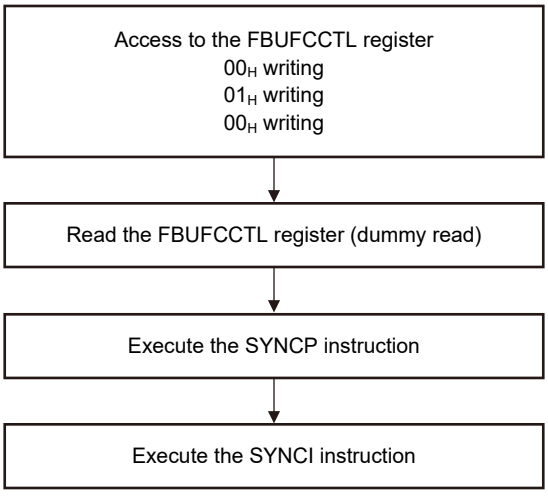
When accessing the BFASELR register, follow the procedure in the flowchart below.



Note 1. See **Section 10, Usage Notes**, **(8) Updating the FBUFCCTL register**, to clear the Flash buffer.

(8) Updating the FBUFCCTL register

Follow the procedure in the flowchart below to transition to read mode after the code flash memory area has been written, or after the value of the BFASELR register has been changed.



Section 11 Electrical Characteristics

This chapter describes the electrical characteristics for self-programming. The characteriscs are differ from the value of serial programming. (*Section 40.25, Flash Programming Characteristics* of *RH850/F1K User's Manual: Harware* or *Section 47A.7, Flash Programming Characteristics* or *Section 47B.7, Flash Programming Characteristics* or *Section 47C.7, Flash Programming Characteristics* of *R850/F1KH, RH850/F1KM User's Manual: Harware*)

11.1 Code Flash

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ± 30%(RH850/F1K, F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1), CISOVCL: 0.1 µF ± 30%(RH850/F1K, F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1), Tj = –40 to (depend on the product) °C, CL = 30 pF
[RH850/F1KH-D8, F1KM-S4, F1KM-S2]
BVCC = VPOC to REGVCC

Table 11.1 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3	ECO (RH850/F1K) products of CPU frequency 160MHz max(RH850/F1KH-D8, F1KM-S4)	4*5		20	MHz
		ADVANCED, PREMIUM (RH850/F1K) products of CPU frequency 240MHz max (RH850/F1KH-D8, F1KM-S4, F1KM-S2) RH850/F1KM-S1	4*5		30	MHz
Number of rewrites*1	CWRT	Data retention of 20 years*2	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is "n" (n = 1000), the device can be erased "n" times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85 °C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. [RH850/F1KH-D8, F1KM-S4, F1KM-S2]
f_{PCLK} = 1/8 f_{CPUCLK_H} (CPU operating frequency) (CKDIVMD = 1*4 or products of CPU frequency 160 MHz max)
f_{PCLK} = 1/4 f_{CPUCLK_H} (CPU operating frequency) (CKDIVMD = 0*4)
[RH850/F1K, F1KM-S1]
f_{PCLK} = 1/4 f_{CPUCLK} (CPU operating frequency).

Note 4. See *Section 44.9, Option Bytes* of *the RH850/F1KH, RH850/F1KM User's Manual: Hardware*.

Note 5. Only for program/erase operation.

Table 11.2 Programming Characteristics

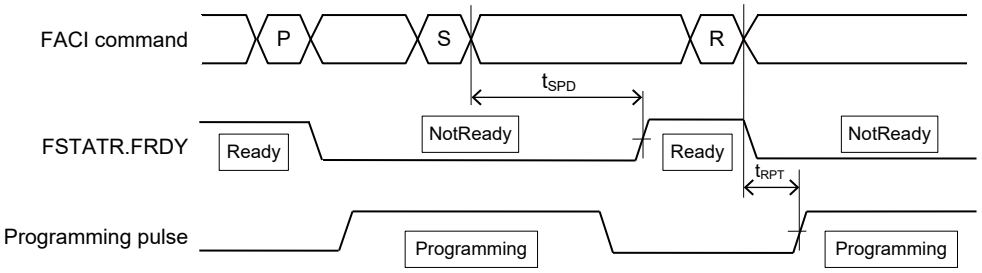
Item	Condition		4MHz ≤ f_{PCLK} < 15 MHz		15MHz ≤ f_{PCLK} < 20 MHz		20 MHz ≤ f_{PCLK}		Unit
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	CWRT < 100 times	256 B	0.9	13.2	0.5	6.6	0.4	6	ms
		8 KB	29	176	15	88	13	80	ms
		32 KB	116	704	60	352	52	320	ms
		256 KB	1.0	5.7	0.5	2.9	0.5	2.6	s
		384 KB	1.4	8.5	0.8	4.3	0.7	3.9	s
		512 KB	1.9	11.3	1.0	5.7	0.9	5.2	s
		768 KB	2.8	16.9	1.5	8.5	1.3	7.7	s
		1 MB	3.8	22.6	2.0	11.3	1.7	10.3	s
		1.5 MB	5.6	33.8	2.9	16.9	2.5	15.4	s
		2 MB	7.5	45.1	3.9	22.6	3.4	20.5	s
	CWRT ≥ 100 times	256 B	1.1	15.8	0.6	8	0.5	7.2	ms
		8 KB	35	212	18	106	16	96	ms
		32 KB	140	848	72	424	64	384	ms
		256 KB	1.2	6.8	0.6	3.4	0.6	3.1	s
		384 KB	1.7	10.2	0.9	5.1	0.8	4.7	s
		512 KB	2.3	13.6	1.2	6.8	1.1	6.2	s
		768 KB	3.4	20.4	1.8	10.2	1.6	9.3	s
		1 MB	4.5	27.2	2.4	13.6	2.1	12.3	s
		1.5 MB	6.8	40.8	3.5	20.4	3.1	18.5	s
		2 MB	9.0	54.3	4.7	27.2	4.1	24.6	s
Erase time	CWRT < 100 times	8 KB	71	216	43	132	39	120	ms
		32 KB	254	864	155	528	141	480	ms
		256 KB	2.1	6.3	1.3	3.9	1.2	3.5	s
		384 KB	3.1	9.5	1.9	5.8	1.7	5.3	s
		512 KB	4.1	12.6	2.5	7.7	2.3	7.0	s
		768 KB	6.1	18.9	3.8	11.5	3.4	10.5	s
		1 MB	8.2	25.2	5.0	15.3	4.6	14.0	s
		1.5 MB	12.2	37.8	7.5	23.0	6.8	21.0	s
		2 MB	16.3	50.4	10.0	30.6	9.1	28.0	s
	CWRT ≥ 100 times	8 KB	85	260	52	158	47	144	ms
		32 KB	304	1040	186	632	169	576	ms
		256 KB	2.5	7.6	1.5	4.7	1.4	4.2	s
		384 KB	3.7	11.4	2.3	7.0	2.1	6.3	s
		512 KB	4.9	15.2	3.0	9.3	2.7	8.4	s
		768 KB	7.3	22.7	4.5	13.9	4.1	12.6	s
		1 MB	9.8	30.3	6.0	18.5	5.5	16.8	s
		1.5 MB	14.6	45.4	9.0	27.8	8.2	25.2	s
		2 MB	19.5	60.5	12.0	37.0	10.9	33.6	s

Table 11.3 Suspend/Resume/Forced Stop Characteristics

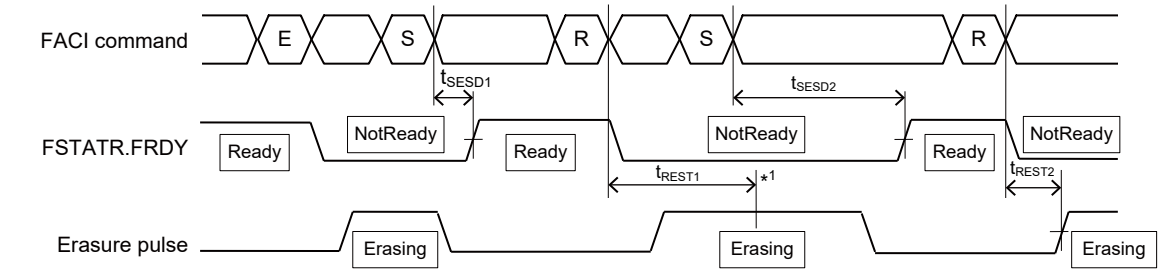
Item	Symbol	Condition	4MHz ≤ f_{PCLK} < 15 MHz	15MHz ≤ f_{PCLK} < 20 MHz	20 MHz ≤ f_{PCLK}	Unit
			MAX.	MAX.	MAX.	
Suspend latency during programming	t_{SPD}		264	132	120	µs
Programming resume time*1	t_{RPT}		110	55	50	µs
Suspend latency during erasure	t_{SESD1}	suspention priority mode: 1st suspention at a pulse	216	132	120	µs
	t_{SESD2}	suspention priority mod: 2nd suspention at a pulse	1.7	1.7	1.7	ms
	t_{SEED}	erasure priority mode	1.7	1.7	1.7	ms
Erasure resume time*1	t_{REST1}	suspention priority mode: resume from1st suspention at a pulse	1.7	1.7	1.7	ms
	t_{REST2}	suspention priority mod: resume from 2nd suspention at a pulse	144	88	80	µs
	t_{REET}	erasure priority mode	144	88	80	µs
Forced stop command latency	t_{FD}		32	22	20	µs

Note 1. The overhead time of programming/erasure resume is generated by resume command. And in suspention priority mode, the erasure pulse re-applying time is generated. The extention time of these factors is defined as resume time.

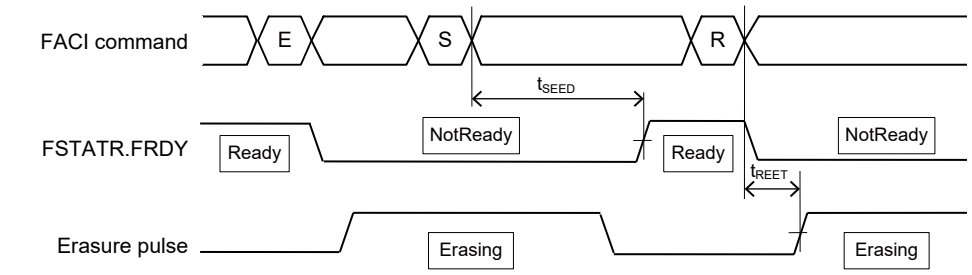
• Suspension during programming



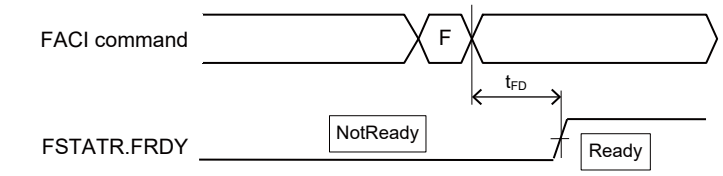
• Suspension during erasure (suspension priority mode)



• Suspension during erasure (eraseure priority mode)



• Forced stop



P: Program command E: Block erase command
S: P/E suspend command R: P/E resume command F: Forced stop command

Note 1. The erasure pulse re-applying time (max. 1 pulse) is added.

Figure 11.1 Suspend/Resume/Forced Stop Timing

11.2 Data Flash

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ± 30%(RH850/F1K, F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1), CISOVCL: 0.1 µF ± 30%(RH850/F1K, F1KH-D8, F1KM-S4, F1KM-S2, F1KM-S1), Tj = –40 to (depend on the product) °C, CL = 30 pF
[RH850/F1KH-D8, F1KM-S4, F1KM-S2]
BVCC = VPOC to REGVCC

Table 11.4 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3	ECO (RH850/F1K) products of CPU frequency 160MHz max(RH850/F1KH-D8, F1KM-S4)	4*5		20	MHz
		ADVANCED, PREMIUM(RH850/F1K) products of CPU frequency 240MHz max (RH850/F1KH-D8, F1KM-S4, F1KM-S2) RH850/F1KM-S1	4*5		30	MHz
Number of rewrites*1	CWRT	Data retention of 20 years*2	125 k			times
		Data retention of 3 years*2	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 B is erased after 4 bytes of writing have been performed for different addresses 16 times, the number of rewrites iscounted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85 °C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. [RH850/F1KH-D8, F1KM-S4, F1KM-S2]
f_{PCLK} = 1/8 f_{CPUCLK_H} (CPU operating frequency) (CKDIVMD = 1*4 or products of CPU frequency 160 MHz max)
f_{PCLK} = 1/4 f_{CPUCLK_H} (CPU operating frequency) (CKDIVMD = 0*4)
[RH850/F1K, F1KM-S1]
f_{PCLK} = 1/4 f_{CPUCLK} (CPU operating frequency)

Note 4. See *Section 44.9, Option Bytes* of *the RH850/F1KH, RH850/F1KM User’s Manual: Hardware*.

Note 5. Only for program/erase operation.

Table 11.5 Programming Characteristics

Item	Condition		4MHz ≤ f_{PCLK} < 15 MHz		15MHz ≤ f_{PCLK} < 20 MHz		20 MHz ≤ f_{PCLK}		Unit
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time		4 B	0.36	3.8	0.18	1.9	0.16	1.7	ms
		64 B	5.8	28	2.9	14	2.6	13	ms
Erase time		64 B	3.1	18	1.9	11	1.7	10	ms
Blank check time*1	The block size of the blank check command is following setting.	4 B	—	84	—	33	—	30	µs
		64 B	—	280	—	110	—	100	µs
		2 KB	—	6.16	—	2.42	—	2.20	ms

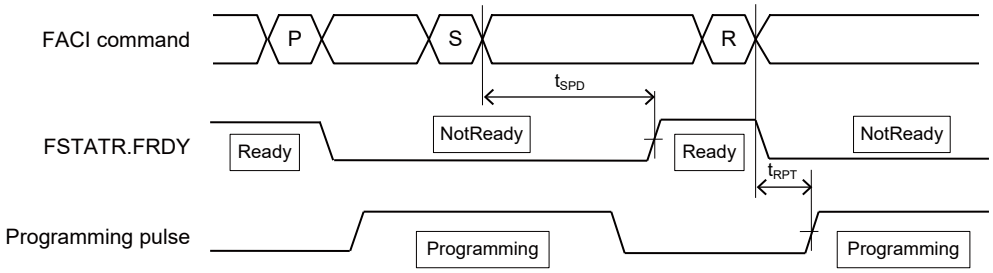
Note 1. When the size of the target area for blank checking is more than 2 KB, the blank check time is the proportional time of 2 KB’s. When the size of the target area for blank checking is more than 64 B and less than 2KB, the blank check time is the proportional time of 64 B.

Table 11.6 Suspend/Resume/Forced Stop Characteristics

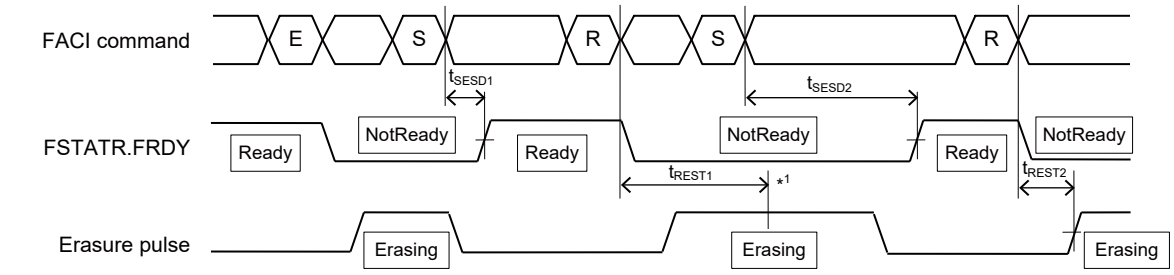
Item	Symbol	Condition	4MHz ≤ f_{PCLK} < 15 MHz	15MHz ≤ f_{PCLK} < 20 MHz	20 MHz ≤ f_{PCLK}	Unit
			MAX.	MAX.	MAX.	
Suspend latency during programming	t_{SPD}		264	132	120	µs
Programming resume time*1	t_{RPT}		110	55	50	µs
Suspend latency during erasure	t_{SESD1}	suspention priority mode: 1st suspention at a pulse	216	132	120	µs
	t_{SESD2}	suspention priority mod: 2nd suspention at a pulse	300	300	300	µs
	t_{SEED}	erasure priority mode	300	300	300	µs
Erasure resume time*1	t_{REST1}	suspention priority mode: resume from1st suspention at a pulse	300	300	300	µs
	t_{REST2}	suspention priority mod: resume from 2nd suspention at a pulse	126	77	70	µs
	t_{REET}	erasure priority mode	126	77	70	µs
Forced stop command latency	t_{FD}		32	22	20	µs

Note 1. The overhead time of programming/erasure resume is generated by resume command. And in suspention priority mode, the erasure pulse re-applying time is generated. The extention time of these factors is defined as resume time.

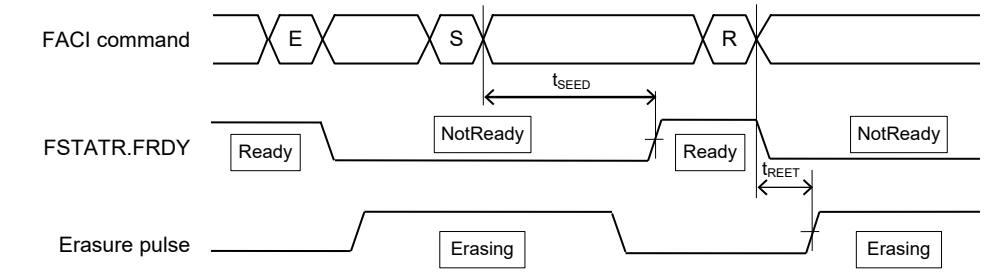
• Suspension during programming



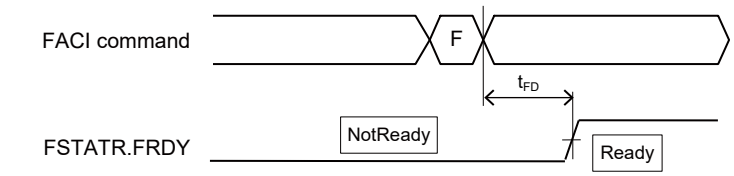
• Suspension during erasure (suspension priority mode)



• Suspension during erasure (eraseure priority mode)



• Forced stop



P: Program command E: Block erase command
S: P/E suspend command R: P/E resume command F: Forced stop command

Note 1. The erasure pulse re-applying time (max. 1 pulse) is added.

Figure 11.2 Suspend/Resume/Forced Stop Timing

Appendix A List of Flash Memory Related Registers

The table below shows the registers related to the flash memory.

Register Name	Symbol	Initial Value	Address	Access Size
Flash pin monitor register	FPMON	00_H	FFA1 0000_H	8
Flash access status register	FASTAT	00_H	FFA1 0010_H	8
Flash sequencer end error interrupt enable register	FAEINT	99_H	FFA1 0014_H	8
Code flash memory area select register	FAREASELC	0000_H	FFA1 0020_H	16
FACI command start address register	FSADDR	0000 0000_H	FFA1 0030_H	32
FACI command end address register	FEADDR	0000 0000_H	FFA1 0034_H	32
Flash status register	FSTATR	0000 8000_H	FFA1 0080_H	8, 16, 32
Flash P/E mode entry register	FENTRYR	0000_H	FFA1 0084_H	16
Code flash protect register	FPROTR	0000_H	FFA1 0088_H	16
Flash sequencer set-up initialization register	FSUINITR	0000_H	FFA1 $008C_H$	16
Lock bit status register	FLKSTAT	00_H	FFA1 0090_H	8
FACI reset transfer status register	FRTSTAT	$0X_H$*1	FFA1 0098_H	8
FACI command register	FCMDR	$FFFF_H$	FFA1 $00A0_H$	16
Flash P/E status register	FPESTAT	0000_H	FFA1 $00C0_H$	16
Data flash blank check control register	FBCCNT	00_H	FFA1 $00D0_H$	8
Data flash blank check status register	FBCSTAT	00_H	FFA1 $00D4_H$	8
Data flash programming start address register	FPSADDR	0000 0000_H	FFA1 $00D8_H$	32
Flash sequencer processing switching register	FCPSR	0000_H	FFA1 $00E0_H$	16
Flash sequencer processing clock notification register	FPCKAR	$00XX_H$*2	FFA1 $00E4_H$	16
Flash ECC encoder monitor register	FECCEMON	$FFFF_H$	FFA1 0100_H	16
Flash ECC test mode register	FECCTMD	0030_H	FFA1 0104_H	16
Flash dummy ECC register	FDMYECC	$FFFF_H$	FFA1 0108_H	16
Flash buffer clear control register	FBUFCCTL	0000 0000_H	FFC5 $B000_H$	32
BFA selection register	BFASELR	$0X_H$	FFC5 9008_H	8
Self-programming ID input register 0	SELFID0	0000 0000_H	FFA0 8000_H	32
Self-programming ID input register 1	SELFID1	0000 0000_H	FFA0 8004_H	32
Self-programming ID input register 2	SELFID2	0000 0000_H	FFA0 8008_H	32
Self-programming ID input register 3	SELFID3	0000 0000_H	FFA0 $800C_H$	32
Self-programming ID authentication status register	SELFIDST	*3	FFA0 8010_H	8, 16, 32

Note 1. The setting depends on the result of FACI reset transfer.

Note 2. PREMIUM, ADVANCED (RH850/F1K), products of CPU frequency 240 MHz max (RH850/F1KH-D8, F1KM-S4, F1KM-S2), RH850/F1KM-S1: $001E_H$
ECO (RH850/F1K), products of CPU frequency 160 MHz max (RH850/F1KH-D8, F1KM-S4): 0014_H

Note 3. The value of the SELFIDST register after a reset depends on the previously set authentication ID. If all the authentication IDs are 0, the value after a reset is 0000 0000_H. Otherwise, it is 0000 0001_H.

RH850/F1KH, RH850/F1KM, RH850/F1K
User's Manual: Hardware Interface

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RH850/F1KH, RH850/F1KM, RH850/F1K

Flash Memory

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