User's Manual

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RH850/D1S1

User's Manual: Hardware

Renesas microcontroller

RH850 Family

Renesas Electronics
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Notes for CMOS devices

(1) Voltage application wafeform at input pin:

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) Handling of unused input pins:

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) Precaution against ESD:

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) Status before initialization:

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) Power ON/OFF sequence:

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) Input of signal during power off state:

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers

This manual is intended for users who wish to understand the functions of the RH850/D1S1 and design application systems using the following RH850/D1S1 microcontrollers:

Purpose

This manual is intended to give users an understanding of the hardware functions of the RH850/D1S1 shown in the *Organization* below.

Organization

This manual is divided into two parts: Hardware (this manual) and Architecture (RH850 Family User's Manual: Software).

Hardware
Pin functions
CPU function
On-chip peripheral functions
Flash memory programming

Software
Overview
Processor Model
Register Reference
Exceptions and Interrupts
Memory Management
Instruction Reference
Reset
Appendix

How to read this manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To understand the overall functions of the RH850/D1S1.

→ Read this manual according to the Contents.

To understand the details of an instruction function

→ See RH850 G3M User's Manual: Software (R01US0123EJ) available separately.

Product Naming

To indicate the dedicated product in the "RH850/D1L/D1M Group", each product name is described as below:

D1L1, D1S1

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representation: $\overline{xxx}$ (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on the bottom

Note: Footnote for item marked with Note in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Numeric representation: Binary ... xxxx or $xxxx_B$

Decimal ... xxxx

Hexadecimal ... $xxxx_H$

Prefix indicating power of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

G (giga): $2^{30} = 1,024^3$

Description of Registers

Each register description includes register access, register address, and register value after a reset, a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meaning of the bit settings.

The standard format for bit charts and tables are described below.

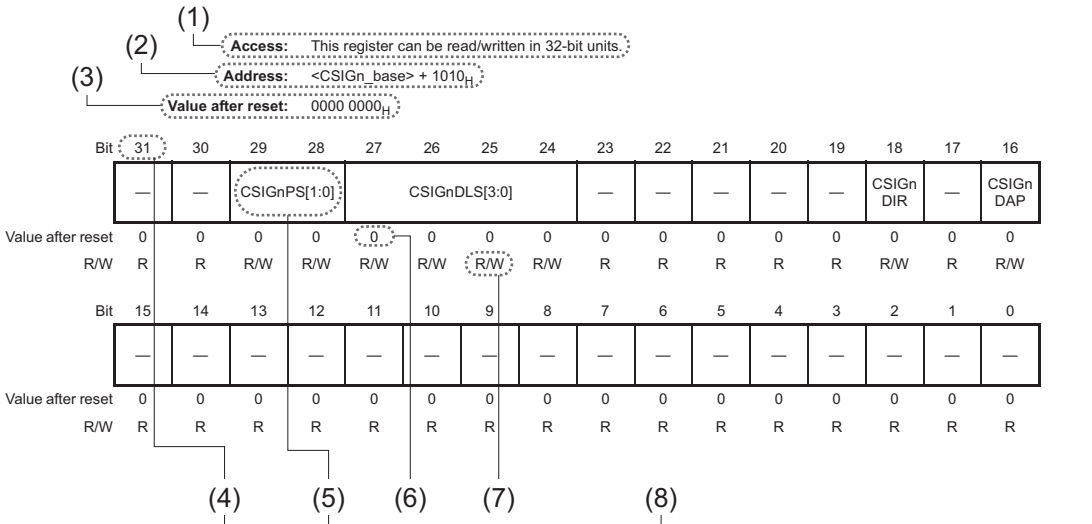


Table 14.19 CSIGnCFG0 register contents (1/2)

Bit Position	Bit Name	Function
31, 30	Reserved	The write value should always be the value after reset.
29, 28	CSIGnPS[1:0]	Specifies parity.
27 to 24	CSIGnDLS [3:0]	Specifies data length. 0: Data length is 16 bits 1: Data length is 1 bit 2: Data length is 2 bits ... 15: Data length is 15 bits **CAUTION** For a data length of less than 7 bits, do not set bits CSIGnCFG0.CSIGnDLS[3:0] for a value 1 to 6 when the extended data length function is disabled with bit CSIGnCTL1.CSIGnEDLE set to 0. It is forbidden to transmit two consecutive data with a data length of less than 7 bits.
23 to 19	Reserved	The write value should always be the value after reset.

CSIGn PS1	CSIGn PS0	Transmission	Reception
0	0	No parity transmitted	No parity is waited for.
0	1	Add parity bit fixed at 0	Parity bit is waited for but not judged.
1	0	Add odd parity	Odd parity bit is waited for.
1	1	Add even parity	Even parity bit is waited for.

(1) Access

The register can be accessed in the bit unit indicated here.

(2) Address

This is the register address.
For base address, see description of base address in each section.

(3) Value after a reset (in hexadecimal notation)

This is the value of all bits of the register after a reset. Values for bytes are given as numbers in the range from 0 to 9 and letters from A to F or as X where they are undefined.

(4) Bit position

This is the bit number.
The bits are numbered from 31 to 0 for 32-bit registers, 15 to 0 for 16-bit registers, and 7 to 0 for 8-bit registers.

(5) Bit name

Bit name or field name is indicated.
When clearly identifying the digits of a bit field is required, do so by using a form such as CSIGnDLS[3:0] above.
Indicate reserved bits by using a dash (—).

(6) Value after a reset (in binary notation)

This is the bit values after a reset.

0	:	The value after a reset is 0.
1	:	The value after a reset is 1.
—	:	The value after a reset is undefined.

(7) R/W

This is the bit attribute of all bits of the register.

R/W	:	The bit or field is readable and writable.
R	:	The bit or field is readable. Note that all reserved bits are indicated as R. When written, the value specified in the bit chart or the value after a reset should be written.
W	:	This bit or field is writable.When read, the value is undefined. If a value is indicated in the bit chart, the value is returned.

(8) Function

This is function of the bit.

Table of Contents

Section 1 Overview

1.1 What's D1S1 Series?

RH850/D1S1 series is the device group that consists from the products that support max 1 MB Code FLASH memories, and it is planned for the successor of Dx4-1 MB, 512 KB, 256 KB.

D1S1 series has almost same features with D1L1 series except internal memory amount. Therefore this document mentions only about the differences of the functional specification from D1L1 series.

Table 1.1 D1S1 and D1L1 Series Product Line Overview

Family Group	Package	Family Member
D1L1	QFP144	R7F701401, R7F701421
D1S1	QFP144	R7F701417, R7F701437

1.2 Major differences from D1L1

Major differences from D1L1 are followings.

- Total pads count for QFP144 version is reduced to 132.
- Code FLASH (2 MB → 1 MB)
- Data FLASH (64 KB → 32 KB)
- LRAM (256 KB → 128 KB)
- Stepper Motor Ch. (6 ch → 4 ch)
- Serial FLASH I/F (1 ch → removed)
- Sound Generator (5 ch → 1 ch)
- I2C (2 ch → 3 ch)
- FCURAM/ROM (FCURAM → FCUROM)

1.3 Related Document

This document only mentions about the differences from D1L1. Please refer following documents for more detail of D1L1 product.

Table 1.2 Related Documents

Document Number	Title
r01ds0245ej0xxx	Datasheet
r01uh0451ej0xxx	User's Manual: Hardware

Section 2 Changing Features

2.1 RH850/D1S1 Products Overview

Table 2.1 RH850/D1S1 Products Overview (1/2)

Product features			D1S1	D1L1
Memory	Code Flash		1 MB	2 MB
	Local RAM (LRAM)		128 KB	256 KB
	Retention RAM (RRAM)		16 KB	
	Data Flash		32 KB	64 KB
	Video RAM (VRAM) with Video RAM wrapper		—	
External memory interfaces	Serial Flash Memory I/F (SFMA)	Bus width	N/A (no SFMA available)	4 bit
		Mode		SDR
		Max. clock		40 MHz
CPU	CPU System		G3M	
	CPU frequency		120 MHz	
	Floating Point Unit (FPU)		Provided	
	Memory Protection Unit (MPU)		Provided	
	Memory caches	Instruction cache	8 KB/4-way associative	
		Non-CPU system memories	—	
DMA			16 ch	
Operating clock	Main Oscillator (Main Osc)		8 to 16 MHz	
	Low Speed Internal Oscillator (LS IntOsc)		Typ. 240 kHz	
	High Speed Internal Oscillator (HS IntOsc)		Typ. 8 MHz	
	Sub Oscillator (SubOsc)		Typ. 32.768 kHz	
	Spread-spectrum PLL0		Max 480 MHz	
	PLL1		Max 480 MHz	
I/O port			92	103
A/D Converter (ADCE)			16 channels, 12 bit resolution	
Timer	Timer Array Unit B (TAUB)		3 units (16 bit resolution, 16 channels/unit)	
	Timer Array Unit J (TAUJ)		1 unit (32 bit resolution, 4 channels/unit)	
	Operating System Timer (OSTM)		2 units (32 bit resolution, 1 channel/unit)	
	Alway-On-Area Timer (AWOT)		1 unit (32 bit resolution, 1 channel/unit)	
	Real-Time Clock (RTCA)		Provided	
	Window Watchdog Timer A (WDTA)		2 units	
	PWM Generators with Diagnostic		1 unit (24 PWM generators, 12 with diagnostic capability.)	
Communi-cation interfaces	Clocked Serial Interface G (CSIG)		4 channels	
	Clocked Serial Interface H (CSIH)		2 channels	
	CAN Interface (RS-CAN)		3 channels (total 192 message buffers)*1	
	CAN Interface (RS-CANFD)		3 channels (total 192 message buffers)*1	
	LIN/UART Interface (RLIN3)		4 channels	
	I2C Interface (RIIC)		3 channels	2 channels

Table 2.1 RH850/D1S1 Products Overview (2/2)

Product features			D1S1	D1L1
External interrupts	Maskable		11	
	Non-maskable (NMI)		1	
Audio	Sound Generator (SG)		1 units	5 units
	PCM-PWM Converter (PCMP)		1 unit	
	Serial Sound Interface (SSIF)		2 units (1 channel/unit)	
Video and Graphics	Video Output	Channels	—	
		I/F	—	
		RLE decoding	—	
		Sprite layer	—	
		Timing Controller (TCON)	—	
Other functions	LCD Bus I/F (LCBI)		8 bit output, max. 10 MHz*4	18 bit output, max. 10 MHz
	Clock Monitors (CLMA)		for MainOsc, LS IntOsc, HS IntOsc, PLL0, PLL1	
	Data CRC (DCRA)		Provided	
	Power-On-Clear (POC)		Provided	
	Intelligent Stepper Motor Driver (ISM), incl. zero point detection for each channel		1 unit, 4 channel	1 unit, 6 channel
	Error Correction Coding (ECC)		for Code Flash, Data Flash, Local RAM, Retention RAM, Video RAM, RS-CAN RAM, Caches tag/data RAMs	
	Error Control Module (ECM)		Master	Master / Checker
	Intelligent Cryptographic Unit (ICUSD)		Provided	
	On-Chip debug (OCD)		Provided	
	Boundary Scan		Provided	
Voltage supply*2	Internal logic	AWO*3	3.3 V, 5 V via on-chip voltage regulator	
		ISO*3	3.3 V, 5 V via on-chip voltage regulator	
	I/O buffers	GPIO*3	3.3 V, 5 V	
	A/D Converter supplies		nominal 3.3 V, 5 V	
Package	Type		QFP	
	Pins		144	
	Pin/ball pitch		0.5 mm	

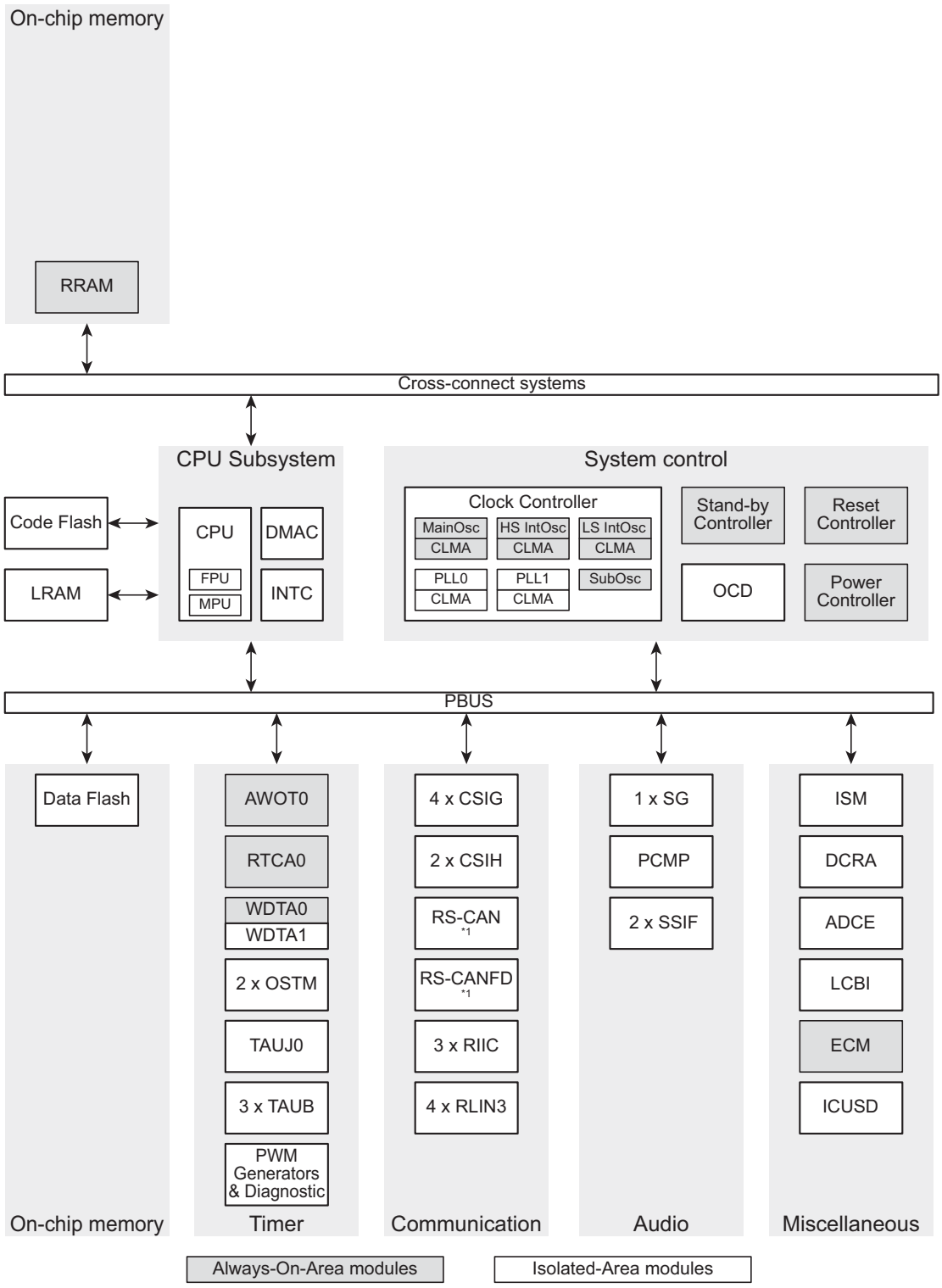
Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Section 2.3, Part Number Information**.

Note 2. The supply voltages are given as nominal values. Refer to the data sheet for detail specification of electrical values.

Note 3. AWO: Always-On-Area
ISO: Isolated-Area
GPIO: General purpose I/O port

Note 4. The LCBI module of this device does not support the TFT mode and CLUT usage.

2.2 Block Diagram



Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Section 2.3, Part Number Information**.

Note 2. The LCBI module of the D1S1 device does not support the TFT mode and CLUT usage.

Figure 2.1 D1S1 block diagram

2.3 Part Number Information

Table 2.2 Part Number Information

Series Name	Part Number	Renesas Order Code	Remarks
D1S1	R7F701417		RH850/D1S1 with RS-CAN I/F
	R7F701437		RH850/D1S1 with RS-CANFD I/F

2.4 Functional Differences to D1L1 Devices

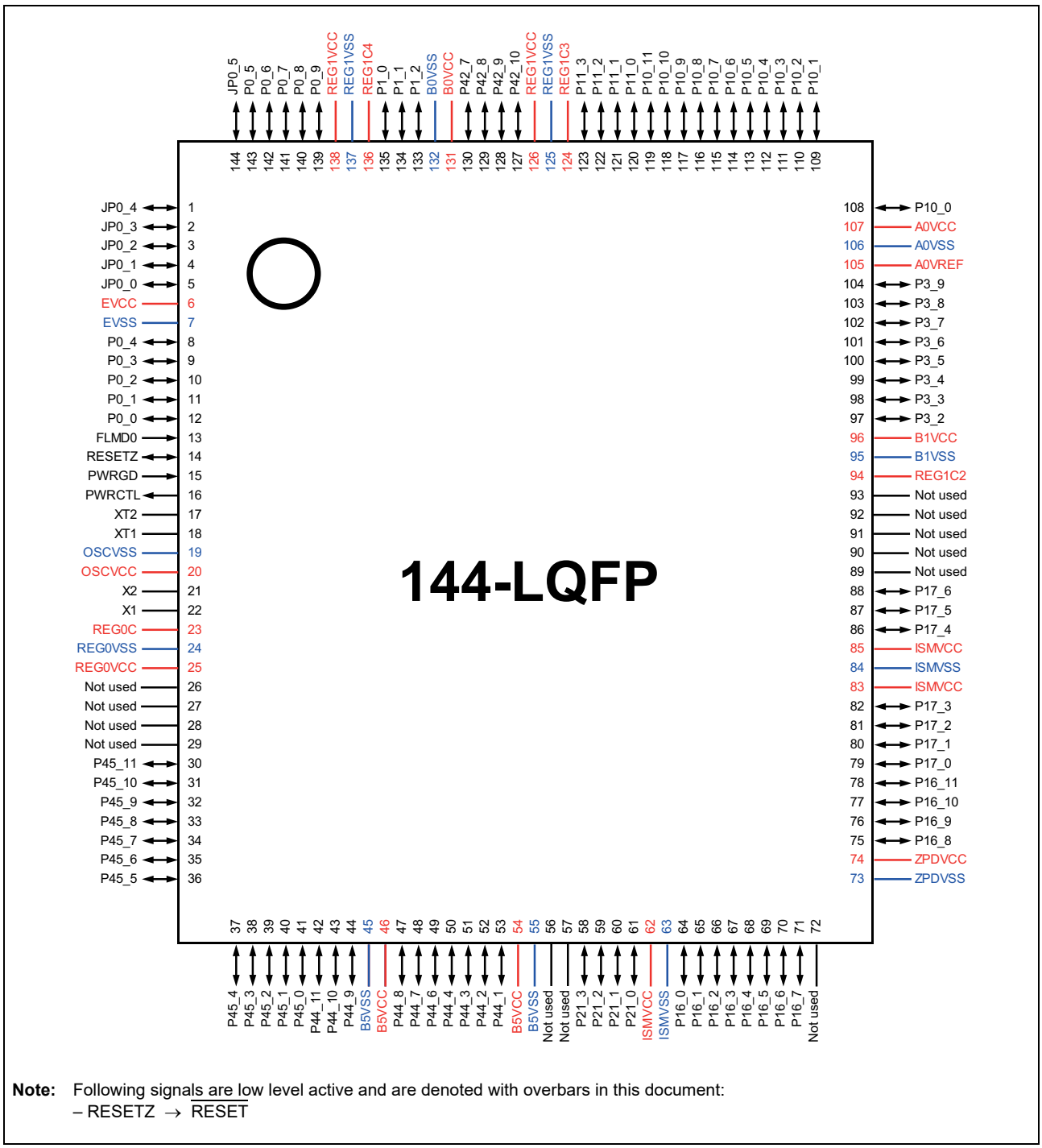
Table 2.3 Functional differences to D1L1 devices

Component	Difference
Code Flash	D1L1 can set the variable reset vector in the corresponding area by a “Config Program” command while OTP configuration command has been executed. D1S1 is prohibited if once an OTP configuration command has been executed for a chip.

Section 3 Pins

This section focus to the differences of D1S1 pin functions from D1L1. All the other functionalities should be referred to *RH850/D1L, D1M Hardware Manual*.

3.1 D1S1 Pin Connection Diagram



Note: Following signals are low level active and are denoted with overbars in this document:
– RESETZ → $\overline{\text{RESET}}$

Figure 3.1 D1S1 Pin Connection Diagram (144pin LQFP package)

3.2 Port Functions

3.2.1 Differences from D1L1

Followings are the differences between D1S1 and D1L1.

Table 3.1 Differences of PIN Features from D1L1

Port	D1S1	D1L1
P17_[11:7]	Removed	Used for ISM3, ISM4, TAUB2O and GPIO
P17_[6:5]	RIIC2 signals are assigned to AF4 GP buffer (standard I/O buffer) used.	Does not have RIIC2. HD buffer (ISM Driver) is used
P17_4	GP buffer (standard I/O buffer) used.	HD buffer (ISM Driver) is used.
P21_[5:4]	Removed	Used for SFMA(Up to 4bit), TAUB and GPIO
P21_[3:0]	CSIG1 signals are assigned to AF4	CSIG1 is not applicable
P43_[1:0]	Removed	Used for a part of LCBI.
P45_[13:12]	Removed	Used for CSIG1DCS, CSIG1SC
P45_[7:4]	Connected signals for AF3 are changed to LCBI0WRRW, LCBI0CS, LCBI0A0DE, LCBI0RDE	Connected signals for AF3 are LCBI0D[11:8]
P45_[3:2]	RIIC2 signals are assigned to AF1	Does not have RIIC2.

3.2.1.1 Input buffer characteristics

Table 3.2 Differences of input buffer characteristics

Port		PISAn_m = 1		PISAn_m = 0		Default
		PISn_m = 1	PISn_m = 0	PISn_m = 1	PISn_m = 0	
P21	P21_0	CMOS1		Schmitt4	Schmitt1	Schmitt1
	P21_1	CMOS1		Schmitt4	Schmitt1	Schmitt1
	P21_2	CMOS1		Schmitt4	Schmitt1	Schmitt1
	P21_3	CMOS1		Schmitt4	Schmitt1	Schmitt1

3.3 Organization of Port Groups

3.3.1 Port Registers

The tables always read as initial values. The write value also should be an initial value. The tables in this subsection show detailed bitmaps of control registers in each port group. In the bitmap field, "√" means an effective bit and "—" means a reserved one. Reserved areas are always read as initial values. The write value also should be an initial value.

NOTE

Some register bits do exists but are not assigned to external pins. These bits, which are labeled as "—" should be written with their initial value when write acceses performed. Read data should be ignored.

3.3.1.1 List of D1S1 Port Registers

(1) Port 0 D1S1 Registers

Table 3.3 Port Group 0 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P0	PMC0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PMCSR0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PIPC0	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	—	√	—	
	PM0	R/W	$FFFF_H$	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PMSR0	R/W	$0000\ FFFF_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PIBC0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PFC0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PFCE0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PBDC0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PPR0	R	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	P0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PSR0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PNOT0	W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PINV0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PU0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PD0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PDSC0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PISA0	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	√	√	
	PPCMD0	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS0	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(2) Port 1 D1S1 Registers

Table 3.4 Port Group 1 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P1	PMC1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PMCSR1	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Upper 16 bits
	PIPC1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	—	√	
	PM1	R/W	$FFFF_H$	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PMSR1	R/W	$0000\ FFFF_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Upper 16 bits
	PIBC1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PFC1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PFCE1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PBDC1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PPR1	R	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	P1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PSR1	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Upper 16 bits
	PNOT1	W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PINV1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PU1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PD1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PDSC1	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC1	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PISA1	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	
	PPCMD1	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS1	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(3) Port 3 D1S1 Registers

Table 3.5 Port Group 3 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P3	PMC3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PMCSR3	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Lower 16 bits
					—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Upper 16 bits
	PIPC3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	—	—	—	
	PM3	R/W	$FFFF_H$	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PMSR3	R/W	$0000\ FFFF_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Lower 16 bits
					—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Upper 16 bits
	PIBC3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PFC3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PFCE3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PBDC3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PPR3	R	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	P3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PSR3	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Lower 16 bits
					—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Upper 16 bits
	PNOT3	W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PINV3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PU3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PD3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PDSC3	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC3	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PISA3	R/W	0000_H	16	—	—	—	—	—	—	√	√	√	√	√	√	√	√	—	—	
	PPCMD3	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS3	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(4) Port 10 D1S1 Registers

Table 3.6 Port Group 10 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P10	PMC10	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PMCSR10	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PM10	R/W	$FFFF_H$	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PMSR10	R/W	$0000\ FFFF_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PIBC10	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PFC10	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PFCE10	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PBDC10	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PPR10	R	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	P10	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PSR10	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PNOT10	W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PINV10	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PODC10	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPCMD10	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS10	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(5) Port 11 D1S1 Registers

Table 3.7 Port Group 11 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P11	PMC11	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PMCSR11	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	Upper 16 bits
	PM11	R/W	$FFFF_H$	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PMSR11	R/W	$0000\ FFFF_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	Upper 16 bits
	PIBC11	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PFC11	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PBDC11	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PPR11	R	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	P11	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PSR11	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	Upper 16 bits
	PNOT11	W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PINV11	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	
	PODC11	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPCMD11	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS11	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(6) Port 16 D1S1 Registers

Table 3.8 Port Group 16 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P16	PMC16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PMCSR16	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PIPC16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PM16	R/W	$F000_H$	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PMSR16	R/W	$0000\ F000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PIBC16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PFC16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PFCE16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PBDC16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PPR16	R	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	P16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PSR16	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PNOT16	W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PINV16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PDSC16	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC16	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PISA16	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	√	√	√	√	√	√	
	PPCMD16	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS16	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(7) Port 17 D1S1 Registers

Table 3.9 Port Group 17 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P17	PMC17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PMCSR17	R/W	$0000\ 0000_H$	32	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Upper 16 bits
	PIPC17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	—*1	—*1	—*1	√	√	√	√	
	PM17	R/W	$FFF0_H$	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PMSR17	R/W	$0000\ FFF0_H$	32	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Upper 16 bits
	PIBC17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PFC17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PFCE17	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	√*1	√*1	—	√	√	√	√	
	PBDC17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PPR17	R	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	P17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PSR17	R/W	$0000\ 0000_H$	32	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Upper 16 bits
	PNOT17	W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PINV17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PU17	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	√*1	√*1	√*1	—	—	—	—	
	PD17	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	√*1	√*1	√*1	—	—	—	—	
	PDSC17	R/W	$0000\ 0000_H$	32	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC17	R/W	$0000\ 0000_H$	32	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PISA17	R/W	0000_H	16	—	—	—	—	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	
	PPCMD17	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS17	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

Note 1. Differences from D1L1.

(8) Port 21 D1S1 Registers

Table 3.10 Port Group 21 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P21	PMC21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PMCSR21	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	Upper 16 bits
	PIPC21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	—*1	√	—	√*1	
	PM21	R/W	$FFFF_H$	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PMSR21	R/W	$0000\ FFFF_H$	32	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	Upper 16 bits
	PIBC21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PFC21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PFCE21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√*1	√*1	√*1	√*1	
	PBDC21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PPR21	R	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	P21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PSR21	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	Upper 16 bits
	PNOT21	W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PINV21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PU21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PD21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	
	PDSC21	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	√*1	√*1	√*1	√*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC21	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—*1	—*1	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√*1	√*1	√*1	√*1	
	PISA21	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	√*1	√*1	√*1	√*1	
	PPCMD21	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS21	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

Note 1. Differences from D1L1.

(9) Port 42 D1S1 Registers

Table 3.11 Port Group 42 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P42	PMC42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PMCSR42	R/W	$0000\ 0000_H$	32	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Lower 16 bits
					—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Upper 16 bits
	PIPC42	R/W	0000_H	16	—	—	—	—	—	√	—	√	—	—	—	—	—	—	—	—	
	PM42	R/W	$FFFF_H$	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PMSR42	R/W	$0000\ FFFF_H$	32	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Lower 16 bits
					—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Upper 16 bits
	PIBC42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PFC42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PFCE42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PBDC42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PPR42	R	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	P42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PSR42	R/W	$0000\ 0000_H$	32	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Lower 16 bits
					—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Upper 16 bits
	PNOT42	W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PINV42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PU42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PD42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PDSC42	R/W	$0000\ 0000_H$	32	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC42	R/W	$0000\ 0000_H$	32	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PISA42	R/W	0000_H	16	—	—	—	—	—	√	√	√	√	—	—	—	—	—	—	—	
	PPCMD42	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS42	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(10) Port 43 D1S1 Registers

Table 3.12 Port Group 43 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P43	PMC43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PMCSR43	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Upper 16 bits
	PIPC43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PM43	R/W	$FFFF_H$	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PMSR43	R/W	$0000\ FFFF_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Upper 16 bits
	PIBC43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PFC43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PFCE43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PBDC43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PPR43	R	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	P43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PSR43	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Upper 16 bits
	PNOT43	W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PINV43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PU43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PD43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PDSC43	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC43	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PISA43	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	—*1	
	PPCMD43	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—*1	—*1	—*1	—*1	—*1	—*1	—*1	—*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS43	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—*1	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

Note 1. Differences from D1L1.

(11) Port 44 D1S1 Registers

Table 3.13 Port Group 44 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P44	PMC44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PMCSR44	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Upper 16 bits
	PIPC44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PM44	R/W	$FFFF_H$	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PMSR44	R/W	$0000\ FFFF_H$	32	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Upper 16 bits
	PIBC44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PFC44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PFCE44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PBDC44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PPR44	R	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	P44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PSR44	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Lower 16 bits
					—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Upper 16 bits
	PNOT44	W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PINV44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PU44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PD44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PDSC44	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC44	R/W	$0000\ 0000_H$	32	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	—	√	√	√	√	—	
	PISA44	R/W	0000_H	16	—	—	—	—	√	√	√	√	√	√	–	√	√	√	√	—	
	PPCMD44	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS44	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

(12) Port 45 D1S1 Registers

Table 3.14 Port Group 45 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
P45	PMC45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PMCSR45	R/W	$0000\ 0000_H$	32	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PIPC45	R/W	0000_H	16	—	—	—*1	—*1	—*1	—*1	—*1	—*1	√	√	√	√	√	√	√	√	
	PM45	R/W	$FFFF_H$	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PMSR45	R/W	$0000\ FFFF_H$	32	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PIBC45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PFC45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PFCE45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PBDC45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PPR45	R	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	P45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PSR45	R/W	$0000\ 0000_H$	32	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Upper 16 bits
	PNOT45	W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PINV45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PU45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PD45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PDSC45	R/W	$0000\ 0000_H$	32	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PODC45	R/W	$0000\ 0000_H$	32	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PIS45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PISA45	R/W	0000_H	16	—	—	—*1	—*1	√	√	√	√	√	√	√	√	√	√	√	√	
	PPCMD45	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	PPROTS45	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

Note 1. Differences from D1L1.

(13) JTAG Port JP0 D1S1 Registers

Table 3.15 JTAG Port Group JP0 D1S1 Registers

Port Group Name	Register Name	R/W	Initial Value	Access Size	Bitmap																Remarks
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
JP0	JPMC0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPMCSR0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	Upper 16 bits
	JPM0	R/W	FF_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPMSR0	R/W	$0000\ 00FF_H$	32	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	Upper 16 bits
	JPIBC0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPFC0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	—	√	√	√	√	
	JPFCE0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	—	√	√	√	√	
	JPBDC0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPPR0	R	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JP0	R/W	0000_H	16	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPSR0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	Upper 16 bits
	JPNOT0	W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPINV0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPU0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPD0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	
	JPDSC0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	√	—	—	—	√	—	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	JPODC0	R/W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	JPIS0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	—	—	—	√	—	√	
	JPISA0	R/W	00_H	8	—	—	—	—	—	—	—	—	—	—	—	√	√	√	—	√	
	JPPCMD0	W	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	√	√	√	√	√	√	√	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits
	JPPROTS0	R	$0000\ 0000_H$	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	√	Lower 16 bits
					—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Upper 16 bits

3.3.2 List of Alternative Function Pins

The following section define the alternative functions of each port.

The first table in each section specifies all ports of the RH850/D1S devices with all possible alternative functions.

The following tables specify which signals and which ports are available for each device.

3.3.2.1 Port 0 (P0)

Table 3.16 Port 0 (P0)

Port Mode (PMC0_m = 0)	Port Mode (PMC0_m = 0)								
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		Dedicated Function
	Input	Output	Input	Output	Input	Output	Input	Output	
P0_0	NMI	RLIN31TX	$\overline{\text{CSIH0SSI}}$	CSIH0CSS0	TAUJ0I0	TAUJ0O0	INTP5	OSTM0 TTOUT	MODE0
P0_1	RLIN31RX / INTP0			CSIH0SO	TAUJ0I1	TAUJ0O1		$\overline{\text{ERROROUT}}$	FLMD1
P0_2	INTP1	RLIN32TX	CSIH0SI		TAUJ0I3	TAUJ0O3		AWOT0TOUT	MODE1
P0_3	RLIN32RX / INTP2		CSIH0SC		TAUJ0I2	TAUJ0O2		CAN0DREN	
P0_4	INTP5	OSTM1 TTOUT		TAUB1O3*1	TAUB1I3	CSCXFOUT		CAN0TX	
P0_5	TAUJ0I1	TAUJ0O1		TAUB1O5*1	TAUB1I5	RTCA0OUT	CAN0RX / INTP6		
P0_6	INTP7	RLIN30TX		TAUB1O7*1	TAUB1I7			CAN1TX	
P0_7	RLIN30RX / INTP8			TAUB1O9*1	TAUJ0I0	TAUJ0O0	CAN1RX / INTP8	CAN2DREN	
P0_8	INTP9	RLIN30TX			TAUJ0I1	TAUJ0O1		CAN2TX	
P0_9	RLIN30RX / INTP10				TAUJ0I0	TAUJ0O0	CAN2RX / INTP10	CAN1DREN	

Note 1. These ports are equipped with an XOR Compare Unit. Refer to *Section 2.4.2, Port output check* by *XOR Compare Unit of H/W manual*.

Table 3.17 P0 Signals Availability

Module	Signals	D1S1	D1L1
All	All	√	√

Note: — : signal not available
√ : signal available

Table 3.18 P0 Ports Availability

Port	D1S1	D1L1
P0_m	√	√

Note: — : signal not available
√ : signal available

3.3.2.2 Port 1 (P1)

Table 3.19 Port 1 (P1)

Port Mode (PMC0_m = 0)	Port Mode (PMC1_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P1_0	TAUB1I2	TAUB1O2		CSIH1SO	CSIG2RYI	CSIG2RYO			
P1_1	TAUB1I4	TAUB1O4	CSIH1SI		$\overline{\text{CSIG2SSI}}$		$\overline{\text{CSIH0SSI}}$	CSIH0CSS0	
P1_2	TAUB1I8	TAUB1O8	CSIH1SC				CSIH0RYI	CSIH0RYO	

Table 3.20 P1 Signals Availability

Module	Signals	D1S1	D1L1
All	All	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.

Note 2. — : signal not available
√ : signal available

Table 3.21 P1 Ports Availability

Port	D1S1	D1L1
P1_0 to P1_2	√	√
P1_3 to P1_11	—	—

Note: — : signal not available
√ : signal available

3.3.2.3 Port 3 (P3)

Table 3.22 Port 3 (P3)

Port Mode (PMC0_m = 0)	Port Mode (PMC3_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P3_2		PCMP0AP0*1	SSIF0RXD	TAUB1O9		SG0FAO*1	TAUB0I4	TAUB0O4	
P3_3		PCMP0AN0*1	TAUB1I11	SSIF0TXD	TAUB1I12	SG1FAO		SG0FAOL	
P3_4		PCMP0AP1*1	SSIF0SCK		TAUB1I14	SG2FAO	TAUB0I8	TAUB0O8	
P3_5		PCMP0AN1*1	SSIF0WS		TAUB2I12	SG3FAO		SG0AO	
P3_6		PCMP0BP0*1	SSIFACK		TAUB2I14	SG4FAO	TAUB0I12	TAUB0O12	
P3_7		PCMP0BN0*1	SSIF1WS			SG0FAOL*1		SG0AO*1	
P3_8		PCMP0BP1*1	SSIF1SCK		TAUB1I13	SG1FAOL		SG1AO	
P3_9		PCMP0BN1*1	SSIF1RXD	SSIF1TXD	TAUB1I15	SG2FAOL		SG2AO	

Note 1. These ports are equipped with an XOR Compare Unit. Refer to *Section 2.4.2, Port output check* by *XOR Compare Unit of H/W manual*.

Table 3.23 P3 Signals Availability

Module	Signals	D1S1	D1L1
Ethernet AVB MAC	All ETNB0	—	—
Sound Generator	SG0AO, SG0FAO, SG0FAOL	√	√
	SG[1:4]AO, SG[1:4]FAO, SG[1:4]FAOL	—	√
All others	All others	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.
Note 2. — : signal not available
√ : signal available

Table 3.24 P3 Ports Availability

Port	D1S1	D1L1
P3_0 to P3_1	—	—
P3_2 to P3_6	√	√
P3_7 to P3_9	√	√
P3_10 to P3_13	—	—

Note: — : signal not available
√ : signal available

3.3.2.4 Port 10 (P10)

Table 3.25 Port 10 (P10)

Port Mode (PMC0_m = 0)	Port Mode (PMC10_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P10_0			TAUB0I1	TAUB0O1	TAUB2I1	TAUB2O1			ADCE0I0
P10_1			TAUB0I2	TAUB0O2	TAUB2I2	TAUB2O2			ADCE0I1
P10_2			TAUB0I3	TAUB0O3	TAUB2I3	TAUB2O3			ADCE0I2
P10_3			TAUB0I5	TAUB0O5	TAUB2I5	TAUB2O5			ADCE0I3
P10_4			TAUB0I6	TAUB0O6	TAUB2I6	TAUB2O6			ADCE0I4
P10_5	ADCE0TRIGI1		TAUB0I7	TAUB0O7	TAUB2I7	TAUB2O7			ADCE0I5
P10_6	ADCE0TRIGI2		TAUB0I9	TAUB0O9	TAUB2I9	TAUB2O9			ADCE0I6
P10_7	ADCE0TRIGI3		TAUB0I10	TAUB0O10	TAUB2I10	TAUB2O10			ADCE0I7
P10_8			TAUB0I11	TAUB0O11	TAUB2I11	TAUB2O11			ADCE0I8
P10_9			TAUB0I13	TAUB0O13	TAUB2I13	TAUB2O13			ADCE0I9
P10_10			TAUB0I14	TAUB0O14	TAUB2I14	TAUB2O14			ADCE0I10
P10_11			TAUB0I15	TAUB0O15	TAUB2I15	TAUB2O15			ADCE0I11

Table 3.26 P10 Signals Availability

Module	Signals	D1S1	D1L1
All	All	√	√

Note: — : signal not available
√ : signal available

Table 3.27 P10 Ports Availability

Port	D1S1	D1L1
P10_m	√	√

Note: — : signal not available
√ : signal available

3.3.2.5 Port 11 (P11)

Table 3.28 Port 11 (P11)

Port Mode (PMC0_m = 0)	Port Mode (PMC11_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P11_0			TAUB1I1	TAUB1O1					ADCE0I12
P11_1			TAUB1I2	TAUB1O2					ADCE0I13
P11_2			TAUB1I3	TAUB1O3					ADCE0I14
P11_3			TAUB1I5	TAUB1O5					ADCE0I15

Table 3.29 P11 Signals Availability

Module	Signals	D1S1	D1L1
A/D Converter	ADCE0I[19:16]	—	—
All others	All others	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.

Note 2. — : signal not available
√ : signal available

Table 3.30 P11 Ports Availability

Port	D1S1	D1L1
P11_0 to P11_3	√	√
P11_4 to P11_7	—	—

Note: — : signal not available
√ : signal available

3.3.2.6 Port 16 (P16)

Table 3.31 Port 16 (P16)

Port Mode (PMC0_m = 0)	Port Mode (PMC16_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P16_0	TAUB0I1	ISM11		PWGA16O		TAUB0O1*1	TAUB0I0	TAUB0O0	ZPD11
P16_1	TAUB0I3	ISM12		PWGA17O		TAUB0O3*1	TAUB1I0	TAUB1O0	ZPD12
P16_2	TAUB0I5	ISM13		PWGA18O		TAUB0O5*1	TAUB2I0	TAUB2O0	ZPD13
P16_3	TAUB0I7	ISM14		PWGA19O		TAUB0O7*1			ZPD14
P16_4	TAUB0I9	ISM21		PWGA20O		TAUB0O9*1			ZPD21
P16_5	TAUB0I11	ISM22		PWGA21O		TAUB0O11*1			ZPD22
P16_6	TAUB0I13	ISM23		PWGA22O		TAUB0O13*1			ZPD23
P16_7	TAUB0I15	ISM24		PWGA23O		TAUB1O1*1	TAUB1I1	TAUB0O15	ZPD24
P16_8	TAUB2I0	ISM51		TAUB1O11		PCMP0AP0*1			ZPD51
P16_9	TAUB2I1	ISM52		TAUB1O13		PCMP0AN0*1			ZPD52
P16_10	TAUB2I2	ISM53		TAUB1O14		PCMP0AP1*1			ZPD53
P16_11	TAUB2I3	ISM54		TAUB1O15		PCMP0AN1*1			ZPD54

Note 1. These ports are equipped with an XOR Compare Unit. Refer to *Section 2.4.2, Port output check* by *XOR Compare Unit of H/W manual*.

Table 3.32 P16 Signals Availability

Module	Signals	D1S1	D1L1
All	All	√	√

Note: — : signal not available
√ : signal available

Table 3.33 P16 Ports Availability

Port	D1S1	D1L1
P16_m	√	√

Note: — : signal not available
√ : signal available

3.3.2.7 Port 17 (P17)

Table 3.34 Port 17 (P17)

Port Mode (PMC0_m = 0)	Port Mode (PMC17_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P17_0	TAUB2I4	ISM61		TAUB2O1		PCMP0BP0*1			ZPD61
P17_1	TAUB2I5	ISM62	ADCE0TRIGI1	TAUB2O2		PCMP0BN0*1			ZPD62
P17_2	TAUB2I6	ISM63	ADCE0TRIGI2	TAUB2O3		PCMP0BP1*1			ZPD63
P17_3	TAUB2I7	ISM64	ADCE0TRIGI3	TAUB2O5		PCMP0BN1*1			ZPD64
P17_4	TAUB2I8			TAUB2O6					
P17_5	TAUB2I9			TAUB2O7			RIIC2SCL		
P17_6	TAUB2I10			TAUB2O9			RIIC2SDA		

Note 1. These ports are equipped with an XOR Compare Unit. Refer to *Section 2.4.2, Port output check* by *XOR Compare Unit of H/W manual*.

Table 3.35 P17 Signals Availability

Module	Signals	D1S1	D1L1
RIIC2	All I2C Bus Interface (Channel 2)	√	—
All others	All others	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.

Note 2. — : signal not available
√ : signal available

Table 3.36 P17 Ports Availability

Port	D1S1	D1L1
P17_0 to P17_3	√	√
P17_4 to P17_6	√	√
P17_7 to P17_11	—	√

Note: — : signal not available
√ : signal available

3.3.2.8 Port 21 (P21)

Table 3.37 Port 21 (P21)

Port Mode (PMC0_m = 0)	Port Mode (PMC21_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P21_0			TAUB0I13	TAUB0O13			CSIG1SC		
P21_1			TAUB0I11	TAUB0O11			$\overline{\text{CSIG1SSI}}$		
P21_2			TAUB0I10	TAUB0O10				CSIG1SO	
P21_3			TAUB0I9	TAUB0O9			CSIG1SI		

Table 3.38 P21 Signals Availability

Module	Signals	D1S1	D1L1
Serial Flash Memory I/F	SFMA0O[3:0]1	—	—
	All other SFMA0	—	√
Media Local Bus	all MLBB0	—	—
Clocked Serial I/F G	All CSIG1	√	—
All others	All others	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.

Note 2. — : signal not available
√ : signal available

Table 3.39 P21 Ports Availability

Port	D1S1	D1L1
P21_0 to P21_3	√	√
P21_4 to P21_5	—	√
P21_6 to P21_9	—	—
P21_10 to P21_12	—	—

Note: — : signal not available
√ : signal available

3.3.2.9 Port 42 (P42)

Table 3.40 Port 42 (42)

Port Mode (PMC0_m = 0)	Port Mode (PMC42_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P42_7		SG3FAOL		PWGA12O		TAUB1O6	$\overline{\text{CSIG3SSI}}$	SG3AO	
P42_8		SG3FAO		PWGA13O		TAUB0O15		CSIG3SO	
P42_9		SG4FAOL		PWGA14O		TAUB1O2	CSIG3SI	SG4AO	
P42_10		SG4FAO		PWGA15O		TAUB1O10	CSIG3SC		

Table 3.41 P42 Signals Availability

Module	Signals	D1S1	D1L1
Ethernet AVB MAC	all ETNB0	—	—
Video Display Controller	all VDCE0_VO	—	—
	VDCE0_VI 2nd alternative inputs	—	—
	VDCE0_VI 3rd alternative inputs	—	—
Sound Generator	SG[4:3]FAO, SG[4:3]FAOL, SG[4:3]AO	—	√
All others	All others	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.

Note 2. — : signal not available
√ : signal available

Table 3.42 P42 Ports Availability

Port	D1S1	D1L1
P42_0 to P42_6	—	—
P42_7 to P42_10	√	√
P42_11 to P42_15	—	—

Note: — : signal not available
√ : signal available

3.3.2.10 Port 44 (P44)

Table 3.43 Port 44 (P44)

Port Mode (PMC0_m = 0)	Port Mode (PMC44_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P44_1	TAUB1I10					$\overline{\text{LCBI0RDE}}$	$\overline{\text{CSIG2SSI}}$	TAUB1O10	
P44_2			RIIC0SDA			LCBI0A0DE		CSIG2SO	
P44_3	TAUB1I11		RIIC0SCL			$\overline{\text{LCBI0CS}}$	CSIG2SI	TAUB1O11	
P44_4				PWGA14O		$\overline{\text{LCBI0WRRW}}$	CSIG2SC		
P44_6			INTP3	PWGA0O	LCBI0D0		$\overline{\text{CSIG3SSI}}$	RLIN33TX	
P44_7			RLIN33RX / INTP4	PWGA1O	LCBI0D1			CSIG3SO	
P44_8			NMI	PWGA2O	LCBI0D2		CSIG3SI	TAUB2O4	
P44_9			INTP1	PWGA3O	LCBI0D3		CSIG3SC		
P44_10			INTP5	PWGA4O	LCBI0D4		RIIC1SDA		
P44_11			INTP7	PWGA5O	LCBI0D5		RIIC1SCL		

Table 3.44 P44 Signals Availability

Module	Signals	D1S1	D1L1
LCD Bus I/F	All LCBI0	√	√
Video Display Controller	VDCE0_VO_Data[23:18]_24bpp	—	—
	All VDCE0_VI	—	—
All others	All others	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.

Note 2. — : signal not available
√ : signal available

Table 3.45 P44 Ports Availability

Port	D1S1	D1L1
P44_0	—	—
P44_1 to P44_4	√	√
P44_5	—	—
P44_6 to P44_11	√	√

Note: — : signal not available
√ : signal available

3.3.2.11 Port 45 (P45)

Table 3.46 Port 45 (P45)

Port Mode (PMC0_m = 0)	Port Mode (PMC45_m = 0)								Dedicated Function
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
P45_0				PWGA13O	ADCE0TRIGI1	$\overline{\text{LCBI0RDE}}$	TAUB2I6	TAUB2O6	
P45_1				PWGA12O	ADCE0TRIGI2	LCBI0A0DE	TAUB2I8		
P45_2	RIIC2SDA			PWGA6O	LCBI0D6		$\overline{\text{CSIG0SSI}}$	TAUB2O12	
P45_3	RIIC2SCL			PWGA7O	LCBI0D7			CSIG0SO	
P45_4				PWGA8O	LCBI0D8		CSIG0SI	TAUB2O10	
						$\overline{\text{LCBI0RDE}}$			
P45_5				PWGA9O	LCBI0D9		CSIG0SC		
						LCBI0A0DE			
P45_6				PWGA10O	LCBI0D10		TAUJ0I2	TAUJ0O2	
						$\overline{\text{LCBI0CS}}$			
P45_7				PWGA11O	LCBI0D11		TAUJ0I3	TAUJ0O3	
						$\overline{\text{LCBI0WRRW}}$			
P45_8	TAUB0I2			TAUB1O3*1	LCBI0D12		TAUB1I3	TAUB0O2	
P45_9	TAUB0I6			TAUB1O5*1	LCBI0D13		TAUB1I5	TAUB0O6	
P45_10	TAUB0I10			TAUB1O7*1	LCBI0D14		$\overline{\text{CSIG1SSI}}$	TAUB0O10	
P45_11	TAUB0I14			TAUB1O9*1	LCBI0D15		CSIG1SI	TAUB0O14	

Note 1. These ports are equipped with an XOR Compare Unit. Refer to *Section 2.4.2, Port output check* by *XOR Compare Unit of H/W manual*.

Table 3.47 P45 Signals Availability

Module	Signals	D1S1	D1L1
LCD Bus I/F	LCBI0D[17:8]	—	√
	$\overline{\text{LCBI0RDE}}$, LCBI0A0DE, $\overline{\text{LCBI0CS}}$, $\overline{\text{LCBI0WRRW}}$	√	—
	All other LCBI0	√	√
Video Display Controller	All VDCE0	—	—
RIIC2	All I2C Bus Interface (Channel 2)	√	—
All others	All others	√*1	√*1

Note 1. Signals are partly available. Refer to the following table about the port availability.

Note 2. — : signal not available
√ : signal available

Table 3.48 P45 Ports Availability

Port	D1S1	D1L1
P45_0 to P45_1	√	√
P45_2 to P45_3	√	√
P45_4 to P45_11	√	√
P45_12 to P45_13	—	√

Note: — : signal not available
√ : signal available

3.3.2.12 JTAG Port 0 (JP0)

Table 3.49 JTAG Port 0 (JP0)

Port Mode (PMC0_m = 0)	Port Mode (JPMC0_m = 0)								Dedicated Function*1
	1st Alternative		2nd Alternative		3rd Alternative		4th Alternative		
	Input	Output	Input	Output	Input	Output	Input	Output	
JP0_0	INTP0		TAUB2I8	TAUB2O8	FLSCI3RXD	FLSCI3TXD			DCUTDI / LPDIO / LPDI
JP0_1	INTP9		TAUB1I6	TAUB1O6		FLSCI3TXD			DCUTDO / – / LPDO
JP0_2	INTP7		TAUB1I12	TAUB1O12	FLSCI3SCKI	$\overline{\text{ERROROUT}}$ *3		$\overline{\text{ERROROUT}}$ *2	DCUTCK / – / LPDCLK
JP0_3	INTP3	RLIN33TX	TAUJ0I2	TAUJ0O2		CSCXFOUT			DCUTMS / – / –
JP0_4									$\overline{\text{DCUTRST}}$ / – / –
JP0_5	RLIN33RX / INTP4		TAUJ0I3	TAUJ0O3		RTCA0OUT			$\overline{\text{DCUTRDY}}$ / – / LPDCLKOUT

Note 1. The debugger signals are given in the following order:
JTAG / LPD (1-pin) low-pin debug / LPD (4-pin) low-pin debug.

Note 2. When other than LPD (1-pin) is used.

Note 3. When LPD (1-pin) is used.

Table 3.50 JP0 Signals Availability

Module	Signals	D1S1	D1L1
All	All	√	√

Note: — : signal not available
√ : signal available

Table 3.51 JP0 Ports Availability

Port	D1S1	D1L1
JP0_m	√	√

Note: — : signal not available
√ : signal available

3.4 Pin State

This section specifies the status of all pins in the different operating modes.

3.4.1 Pin state in normal operation mode

Table 3.52 Pin state in normal operation mode

Port	Pin Category	$\overline{\text{DCUTRST}}$ = L			
		$\overline{\text{RESET}}$ pin = L		$\overline{\text{RESET}}$ pin = H	
		During power-up (POC0RES = H)	Internal reset active (POC0RES = L)	No reset active	During DEEPSTOP
Pn	P0	Hi-Z	Hi-Z	Operate	Hold/operate
	P1, P3, P42, P44, P45, P17_[6:4]	Hi-Z	Hi-Z	Operate	Hold/Hi-Z
	P21	Hi-Z	Hi-Z	Operate	Hi-Z
	P10, P11	Hi-Z	Hi-Z	Operate	Hi-Z
	P16, P17_[3:0]	L	L	Operate	Hold/L
JP0*2		Hi-Z	Hi-Z	Operate	Operate
$\overline{\text{RESET}}$ (open drain)		L	L → H input	H input	H input
FLMD0 (input with internal pull-down)		L	L	L	L
X1/X2		Stop	Stop *1	Operate	Operate
XT1/XT2		Stop	Stop *1	Operate	Operate
PWRGD		Operate	Operate	Operate	Operate
PWRCTL		L	H	H	L

Note 1. X1/X2 and XT1/XT2 are only affected by the Power-On-Clear 0 (POC0RES = H). Thus, once it starts operation, internal reset does not change the status of these pins.

Note 2. JP0_4 should be pulled down on $\overline{\text{RESET}}$ pin = L state.
When SYSRES and the external $\overline{\text{RESET}}$ is active, an on-chip pull-down resistor is connected to JP0_4.

3.4.2 Pin state in debug mode

Table 3.53 Pin state in debug mode

Port	Pin Category	$\overline{\text{DCUTRST}}$ = H			
		$\overline{\text{RESET}}$ pin = L		$\overline{\text{RESET}}$ pin = H	
		During power-up (POC0RES = H)	Internal reset active (POC0RES = L)	No reset active	During DEEPSTOP
Pn	P0	Hi-Z	Hi-Z	Operate	Hold/operate
	P1, P3, P42, P44, P45, P17_[6:4]	Hi-Z	Hi-Z	Operate	Hold/Hi-Z
	P21	Hi-Z	Hi-Z	Operate	Hi-Z
	P10, P11	Hi-Z	Hi-Z	Operate	Hi-Z
	P16, P17_[3:0]	L	L	Operate	Hold/L
JP0		Operate	Operate	Operate	Operate
$\overline{\text{RESET}}$ (open drain)		L	L → H input	H input	H input
FLMD0 (input with internal pull-down)		L	L	L	L
X1/X2		Stop	Stop *1*2	Operate	Operate
XT1/XT2		Stop	Stop *1	Operate	Operate
PWRGD		Operate	Operate	Operate	Operate
PWRCTL		L	H	H	H

Note 1. X1/X2 and XT1/XT2 are only affected by the Power-On-Clear 0 (POC0RES = H). Thus, once it starts operation, internal reset does not change the status of these pins.

Note 2. The X1/X2 pins are operating, if it is used for LPD (1-pin) mode (OPJTAG[1:0] = 10_B).

3.4.3 Pin state in serial programming mode

Table 3.54 Pin state in serial programming mode

Port	Pin Category	$\overline{\text{DCUTRST}}$ = L			
		$\overline{\text{RESET}}$ pin = L		$\overline{\text{RESET}}$ pin = H	
		During power-up (POC0RES = H)	Internal reset active (POC0RES = L)	No reset active	During DEEPSTOP
Pn	P0	Hi-Z	Hi-Z	Operate	Hold/operate
	P1, P3, P42, P44, P45, P17_[6:4]	Hi-Z	Hi-Z	Operate	Hold/Hi-Z
	P21	Hi-Z	Hi-Z	Operate	Hi-Z
	P10, P11	Hi-Z	Hi-Z	Operate	Hi-Z
	P16, P17_[3:0]	L	L	Operate	Hold/L
JP0*1		Hi-Z	Hi-Z	Operate	Operate
$\overline{\text{RESET}}$ (open drain)		L	L → H input	H input	H input
FLMD0 (input with internal pull-down)		L	H	H	H
X1/X2		Stop	Stop	Operate	Operate
XT1/XT2		Stop	Stop	Operate	Operate
PWRGD		Operate	Operate	Operate	Operate
PWRCTL		L	H	H	L

Note 1. JP0_4 should be pulled down on RESET pin = L state.
When SYSRES and the external RESET is active, an on-chip pull-down resistor is connected to JP0_4.

3.5 Recommended Connection of Not Used Pins

Table 3.55 Recommended Connection of Not Used Pins

Terminal Number	Function in D1L1	D1S1	Note
26-27	P43_[1:0]	open	never change I/O ports reset configuration for those pins
28-29	P45_[13:12]	open	never change I/O ports reset configuration for those pins
56-57	P21_[5:4]	open	never change I/O ports reset configuration for those pins
89-93	P17_[11:7]	open	never change I/O ports reset configuration for those pins
72	ZPDVREF	open or ZPDVSS	

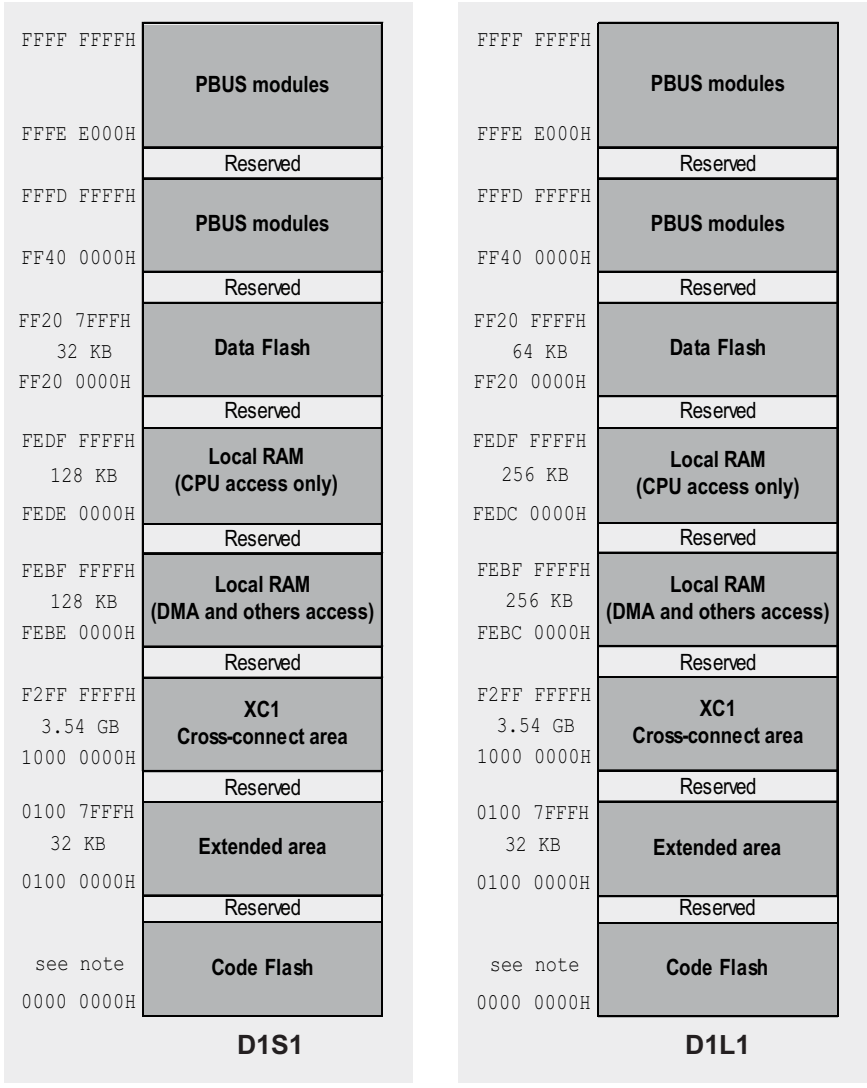
Section 4 Address Spaces

CAUTION

When making an access to the on-chip I/O register space, access the addresses shown in this manual. Do not access an address that is reserved or not specified in this manual. Otherwise, operation is not guaranteed.

4.1 CPU Address Map

The following diagram shows the address map from the CPU's perspective.



Note: The Code Flash memory is device dependend:
- D1S1 : 1 MB, address space 0000 0000_H to 000F $FFFF_H$
- D1L1: 2 MB, address space 0000 0000_H to 001F $FFFF_H$

Figure 4.1 CPU Address Map

CAUTION

Initial value of CPU reset vector

Reset vector is depended RBASE register settings. And, RBASE initial value is 0000 0000_H. RBASE register is described by *"RH850 Family User's Manual: Software"*.

Local RAM

The Local RAM is accessible through two address areas in the CPU address map:

- The Local RAM area starting from address FEDE 0000_H (D1S1) or FEDC 0000_H (D1L1) is accessible only by the CPU.
- The Local RAM area starting from address FEBE 0000_H (D1S1) or FEBC 0000_H (D1L1) is accessible also by all other masters, like the DMA Controller and all bus masters of the cross-connect system.

CAUTION

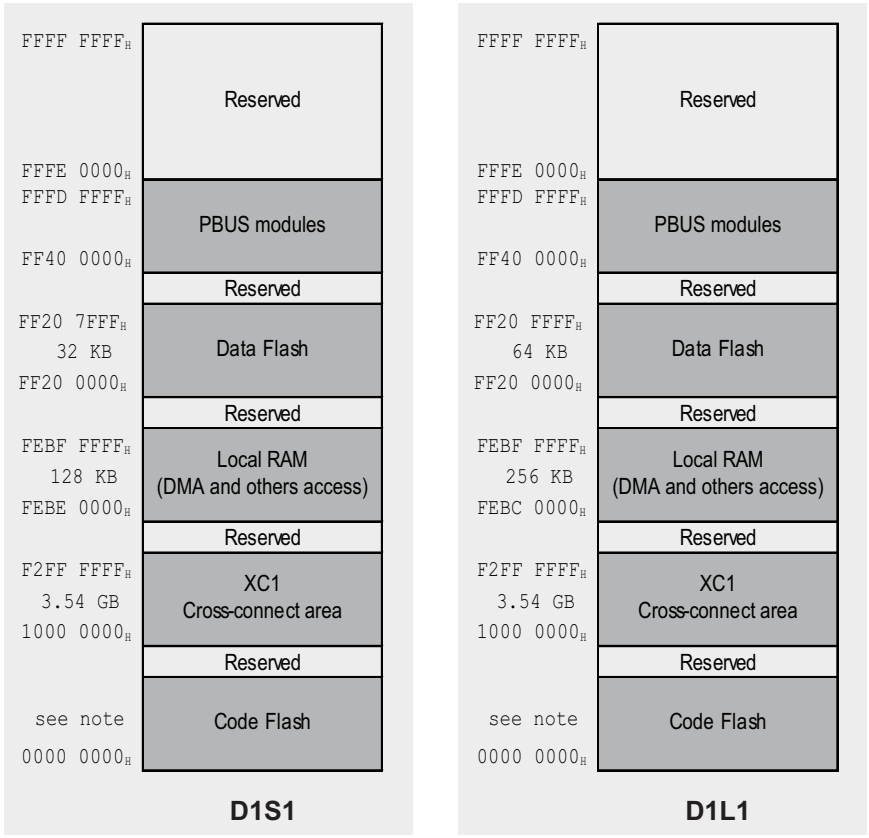
Through the CPU can access the Local RAM via both address areas, it is highly recommended to use the exclusive area at FEDE 0000_H (D1S1) or FEDC 0000_H (D1L1).

CPU Access to On-Chip and External Memories

The CPU can access all external memories via the 3.54 GB large memory window to the XC1 cross-connect.

4.2 DMA Address Map for the CPU Subsystem

The following diagram shows the address map of the CPU Subsystem from the DMA Controller's perspective.



Note: Code Flash memory is device dependend:
- D1S1 : 1 MB, address space 0000 0000_H to 000F $FFFF_H$
- D1L1: 2 MB, address space 0000 0000_H to 001F $FFFF_H$

Figure 4.2 DMA Address Map

Section 5 Interrupt

This section indicates RH850/D1S1 Interrupt Exception Handler and Priority.

The difference from RH850/D1L1 is that interrupts that are come from RIIC2 are appended to channel 230, 231, 232, 233.

All the other interrupt related features are same with RH850/D1L series. Please refer H/W manual of RH850/D1L for more details.

Table 5.1 D1S1 Interrupt Exception Handler and Priority (1/7)

Functional Module	Interrupt Source Name	Level Interrupt *1	Number of Interrupt Channel	Source Code	Offset Address: Direct Branch RINT = 0	Offset Address: Direct Branch RINT = 1	Offset Address: Table Reference	Interrupt Priority (Initial Value)	Default Priority
Non-maskable interrupt			(FENMI)	$E0_H$	$+0E0_H$	$+0E0_H$	—		High
FE level interrupt			(FEINT)	$F0_H$	$+0F0_H$	$+0F0_H$	—		
WDTA0	75 % interrupt (INTWDTA0)		0	1000	The offset address is the same in all channels and is determined between $+100_H$ and $+1F0_H$ according to priority.	The offset address is always $+100_H$ regardless of priority to reduce the offset address.	$+000_H$	0 to 15 (15)	
WDTA1	75 % interrupt (INTWDTA1)		1	1001			$+004_H$	0 to 15 (15)	
RTCA0	1 second interrupt (INTRTCA01S)		2	1002			$+008_H$	0 to 15 (15)	
	Alarm interrupt (INTRTCA0AL)		3	1003			$+00C_H$	0 to 15 (15)	
	Fixed interval interrupt (INTRTCA0R)		4	1004			$+010_H$	0 to 15 (15)	
AWOT0	Timer interrupt (INTAWOT0)		5	1005			$+014_H$	0 to 15 (15)	
Port	External interrupt 0 (INTP0)		6	1006			$+018_H$	0 to 15 (15)	
	External interrupt 1 (INTP1)		7	1007			$+01C_H$	0 to 15 (15)	
	External interrupt 2 (INTP2)		8	1008			$+020_H$	0 to 15 (15)	
	External interrupt 3 (INTP3)		9	1009			$+024_H$	0 to 15 (15)	
	External interrupt 4 (INTP4)		10	100A			$+028_H$	0 to 15 (15)	
	External interrupt 5 (INTP5)		11	100B			$+02C_H$	0 to 15 (15)	
	External interrupt 6 (INTP6)		12	100C			$+030_H$	0 to 15 (15)	
	External interrupt 7 (INTP7)		13	100D			$+034_H$	0 to 15 (15)	
	External interrupt 8 (INTP8)		14	100E			$+038_H$	0 to 15 (15)	
	External interrupt 9 (INTP9)		15	100F			$+03C_H$	0 to 15 (15)	
	External interrupt 9 (INTP10)		16	1010			$+040_H$	0 to 15 (15)	
TAUB0	Channel 0 interrupt (INTTAUB0I0)		17	1011			$+044_H$	0 to 15 (15)	
	Channel 1 interrupt (INTTAUB0I1)		18	1012			$+048_H$	0 to 15 (15)	
	Channel 2 interrupt (INTTAUB0I2)		19	1013			$+04C_H$	0 to 15 (15)	
	Channel 3 interrupt (INTTAUB0I3)		20	1014			$+050_H$	0 to 15 (15)	
	Channel 4 interrupt (INTTAUB0I4)		21	1015			$+054_H$	0 to 15 (15)	
	Channel 5 interrupt (INTTAUB0I5)		22	1016			$+058_H$	0 to 15 (15)	
	Channel 6 interrupt (INTTAUB0I6)		23	1017			$+05C_H$	0 to 15 (15)	
	Channel 7 interrupt (INTTAUB0I7)		24	1018			$+060_H$	0 to 15 (15)	
	Channel 8 interrupt (INTTAUB0I8)		25	1019			$+064_H$	0 to 15 (15)	
	Channel 9 interrupt (INTTAUB0I9)		26	101A			$+068_H$	0 to 15 (15)	
	Channel 10 interrupt (INTTAUB0I10)		27	101B			$+06C_H$	0 to 15 (15)	
	Channel 11 interrupt (INTTAUB0I11)		28	101C			$+070_H$	0 to 15 (15)	
	Channel 12 interrupt (INTTAUB0I12)		29	101D			$+074_H$	0 to 15 (15)	
	Channel 13 interrupt (INTTAUB0I13)		30	101E			$+078_H$	0 to 15 (15)	
	Channel 14 interrupt (INTTAUB0I14)		31	101F			$+07C_H$	0 to 15 (15)	
	Channel 15 interrupt (INTTAUB0I15)		32	1020			$+080_H$	0 to 15 (15)	

Table 5.1 D1S1 Interrupt Exception Handler and Priority (2/7)

Functional Module	Interrupt Source Name	Level Interrupt *1	Number of Interrupt Channel	Source Code	Offset Address: Direct Branch RINT = 0	Offset Address: Direct Branch RINT = 1	Offset Address: Table Reference	Interrupt Priority (Initial Value)	Default Priority
TAUB1	Channel 0interrupt (INTTAUB1I0)		33	1021	The offset address is the same in all channels and is determined between $+100_H$ and $+1F0_H$ according to priority.	The offset address is always $+100_H$ regardless of priority to reduce the offset address.	$+080_H$	0 to 15 (15)	High
	Channel 1interrupt (INTTAUB1I1)		34	1022			$+084_H$	0 to 15 (15)	
	Channel 2interrupt (INTTAUB1I2)		35	1023			$+088_H$	0 to 15 (15)	
	Channel 3interrupt (INTTAUB1I3)		36	1024			$+08C_H$	0 to 15 (15)	
	Channel 4interrupt (INTTAUB1I4)		37	1025			$+090_H$	0 to 15 (15)	
	Channel 5interrupt (INTTAUB1I5)		38	1026			$+094_H$	0 to 15 (15)	
	Channel 6interrupt (INTTAUB1I6)		39	1027			$+098_H$	0 to 15 (15)	
	Channel 7interrupt (INTTAUB1I7)		40	1028			$+09C_H$	0 to 15 (15)	
	Channel 8interrupt (INTTAUB1I8)		41	1029			$+0A0_H$	0 to 15 (15)	
	Channel 9interrupt (INTTAUB1I9)		42	102A			$+0A4_H$	0 to 15 (15)	
	Channel 10interrupt (INTTAUB1I10)		43	102B			$+0A8_H$	0 to 15 (15)	
	Channel 11interrupt (INTTAUB1I11)		44	102C			$+0AC_H$	0 to 15 (15)	
	Channel 12interrupt (INTTAUB1I12)		45	102D			$+0B0_H$	0 to 15 (15)	
	Channel 13interrupt (INTTAUB1I13)		46	102E			$+0B4_H$	0 to 15 (15)	
	Channel 14interrupt (INTTAUB1I14)		47	102F			$+0B8_H$	0 to 15 (15)	
	Channel 15interrupt (INTTAUB1I15)		48	1030			$+0BC_H$	0 to 15 (15)	
TAUB2	Channel 0 interrupt (INTTAUB2I0)		49	1031			$+0C0_H$	0 to 15 (15)	
	Channel 1 interrupt (INTTAUB2I1)		50	1032			$+0C4_H$	0 to 15 (15)	
	Channel 2 interrupt (INTTAUB2I2)		51	1033			$+0C8_H$	0 to 15 (15)	
	Channel 3 interrupt (INTTAUB2I3)		52	1034			$+0CC_H$	0 to 15 (15)	
	Channel 4 interrupt (INTTAUB2I4)		53	1035			$+0D0_H$	0 to 15 (15)	
	Channel 5 interrupt (INTTAUB2I5)		54	1036			$+0D4_H$	0 to 15 (15)	
	Channel 6 interrupt (INTTAUB2I6)		55	1037			$+0D8_H$	0 to 15 (15)	
	Channel 7 interrupt (INTTAUB2I7)		56	1038			$+0DC_H$	0 to 15 (15)	
	Channel 8 interrupt (INTTAUB2I8)		57	1039			$+0E0_H$	0 to 15 (15)	
	Channel 9 interrupt (INTTAUB2I9)		58	103A			$+0E4_H$	0 to 15 (15)	
	Channel 10 interrupt (INTTAUB2I10)		59	103B			$+0E8_H$	0 to 15 (15)	
	Channel 11 interrupt (INTTAUB2I11)		60	103C			$+0EC_H$	0 to 15 (15)	
	Channel 12 interrupt (INTTAUB2I12)		61	103D			$+0F0_H$	0 to 15 (15)	
	Channel 13 interrupt (INTTAUB2I13)		62	103E			$+0F4_H$	0 to 15 (15)	
	Channel 14 interrupt (INTTAUB2I14)		63	103F			$+0F8_H$	0 to 15 (15)	
	Channel 15 interrupt (INTTAUB2I15)		64	1040			$+0FC_H$	0 to 15 (15)	
ADCE0	Temperature Sensor interrupt (INTADCE0TSN)		65	1041			$+100_H$	0 to 15 (15)	
	Scan group 1 interrupt (INTADCE0I1)		66	1042			$+104_H$	0 to 15 (15)	
	Scan group 2 interrupt (INTADCE0I2)		67	1043			$+108_H$	0 to 15 (15)	
	Scan group 3 interrupt (INTADCE0I3)		68	1044			$+10C_H$	0 to 15 (15)	
RSCAN	Channel 0 to 2 global error interrupt (INTRCANGERR)	√	69	1045			$+110_H$	0 to 15 (15)	
	Channel 0 to 2 RX FIFO interrupt (INTRCANGRECC)	√	70	1046			$+114_H$	0 to 15 (15)	
	Channel 0 error interrupt (INTRCAN0ERR)	√	71	1047			$+118_H$	0 to 15 (15)	
	Channel 0 COM RX FIFO interrupt (INTRCAN0REC)	√	72	1048			$+11C_H$	0 to 15 (15)	
	Channel 0 TX interrupt (INTRCAN0TRX)	√	73	1049			$+120_H$	0 to 15 (15)	
CSIG0	Reception error interrupt (INTCSIGT0IRE)		74	104A			$+124_H$	0 to 15 (15)	
	Reception status interrupt (INTCSIG0IR)		75	104B			$+128_H$	0 to 15 (15)	
	Communication status interrupt (INTCSIG0IC)		76	104C			$+12C_H$	0 to 15 (15)	
CSIH0	Reception error interrupt (INTCSIH0IRE)		77	104D			$+130_H$	0 to 15 (15)	
	Reception status interrupt (INTCSIH0IR)		78	104E			$+134_H$	0 to 15 (15)	
	Communication status interrupt (INTCSIH0IC)		79	104F			$+138_H$	0 to 15 (15)	
	Job completion interrupt (INTCSIH0IJC)		80	1050			$+13C_H$	0 to 15 (15)	

Table 5.1 D1S1 Interrupt Exception Handler and Priority (3/7)

Functional Module	Interrupt Source Name	Level Interrupt *1	Number of Interrupt Channel	Source Code	Offset Address: Direct Branch RINT = 0	Offset Address: Direct Branch RINT = 1	Offset Address: Table Reference	Interrupt Priority (Initial Value)	Default Priority
RLIN30	Status interrupt (INTRLIN30UR2)		81	1051	The offset address is the same in all channels and is determined between $+100_H$ and $+1F0_H$ according to priority.	The offset address is always $+100_H$ regardless of priority to reduce the offset address.	+144v	0 to 15 (15)	High
	Reception complete interrupt (INTRLIN30UR1)		82	1052			$+148_H$	0 to 15 (15)	
	Transmission interrupt (INTRLIN30UR0)		83	1053			$+14C_H$	0 to 15 (15)	
RLIN31	Status interrupt (INTRLIN31UR2)		84	1054			$+150_H$	0 to 15 (15)	
	Reception complete interrupt (INTRLIN31UR1)		85	1055			$+154_H$	0 to 15 (15)	
	Transmission interrupt (INTRLIN31UR0)		86	1056			$+158_H$	0 to 15 (15)	
SG0	Threshold interrupt (INTSG0TI)		87	1057			$+15C_H$	0 to 15 (15)	
	Reserved		88	1058			$+160_H$	0 to 15 (15)	
	Reserved		89	1059			$+164_H$	0 to 15 (15)	
	Reserved		90	105A			$+168_H$	0 to 15 (15)	
	Reserved		91	105B			$+16C_H$	0 to 15 (15)	
OCD/DCU	Debugger hot-attach interrupt (INTDCUTDI)	√	92	105C			$+170_H$	0 to 15 (15)	
DMAC	DMA Transfer Error (INTDMAERR)		93	105D			$+174_H$	0 to 15 (15)	
	DMA channel 0 transfer completion/transfer count compare match interrupt (INTDMA0)		94	105E			$+178_H$	0 to 15 (15)	
	DMA channel 1 transfer completion/transfer count compare match interrupt (INTDMA1)		95	105F			$+17C_H$	0 to 15 (15)	
	DMA channel 2 transfer completion/transfer count compare match interrupt (INTDMA2)		96	1060			$+180_H$	0 to 15 (15)	
	DMA channel 3 transfer completion/transfer count compare match interrupt (INTDMA3)		97	1061			$+184_H$	0 to 15 (15)	
	DMA channel 4 transfer completion/transfer count compare match interrupt (INTDMA4)		98	1062			$+188_H$	0 to 15 (15)	
	DMA channel 5 transfer completion/transfer count compare match interrupt (INTDMA5)		99	1063			$+18C_H$	0 to 15 (15)	
	DMA channel 6 transfer completion/transfer count compare match interrupt (INTDMA6)		100	1064			$+190_H$	0 to 15 (15)	
	DMA channel 7 transfer completion/transfer count compare match interrupt (INTDMA7)		101	1065			$+194_H$	0 to 15 (15)	
	DMA channel 8 transfer completion/transfer count compare match interrupt (INTDMA8)		102	1066			$+198_H$	0 to 15 (15)	
	DMA channel 9 transfer completion/transfer count compare match interrupt (INTDMA9)		103	1067			$+19C_H$	0 to 15 (15)	
	DMA channel 10 transfer completion/transfer count compare match interrupt (INTDMA10)		104	1068			$+1A0_H$	0 to 15 (15)	
	DMA channel 11 transfer completion/transfer count compare match interrupt (INTDMA11)		105	1069			$+1A4_H$	0 to 15 (15)	
	DMA channel 12 transfer completion/transfer count compare match interrupt (INTDMA12)		106	106A			$+1A8_H$	0 to 15 (15)	
	DMA channel 13 transfer completion/transfer count compare match interrupt (INTDMA13)		107	106B			$+1AC_H$	0 to 15 (15)	
	DMA channel 14 transfer completion/transfer count compare match interrupt (INTDMA14)		108	106C			$+1B0_H$	0 to 15 (15)	
	DMA channel 15 transfer completion/transfer count compare match interrupt (INTDMA15)		109	106D			$+1B4_H$	0 to 15 (15)	
RIIC0	Receive error/event interrupt (INTRIIC0LEE)	√	110	106E			$+1B8_H$	0 to 15 (15)	
	Data received interrupt (INTRIIC0RI)		111	106F			$+1BC_H$	0 to 15 (15)	
	Data buffer empty interrupt (INTRIIC0TI)		112	1070			$+1C0_H$	0 to 15 (15)	
	Data transmitted interrupt (INTRIIC0TEI)	√	113	1071			$+1C4_H$	0 to 15 (15)	
RIIC1	Receive error/event interrupt (INTRIIC1LEE)	√	114	1072			$+1C8_H$	0 to 15 (15)	
	Data received interrupt (INTRIIC1RI)		115	1073			$+1CC_H$	0 to 15 (15)	
	Data buffer empty interrupt (INTRIIC1TI)		116	1074			$+1D0_H$	0 to 15 (15)	
	Data transmitted interrupt (INTRIIC1TEI)	√	117	1075			$+1D4_H$	0 to 15 (15)	

Table 5.1 D1S1 Interrupt Exception Handler and Priority (4/7)

Functional Module	Interrupt Source Name	Level Interrupt *1	Number of Interrupt Channel	Source Code	Offset Address: Direct Branch RINT = 0	Offset Address: Direct Branch RINT = 1	Offset Address: Table Reference	Interrupt Priority (Initial Value)	Default Priority
RSCAN1	Channel 1 error interrupt (INTRCAN1ERR)	√	118	1076	The offset address is the same in all channels and is determined between $+100_H$ and $+1F0_H$ according to priority.	The offset address is always $+100_H$ regardless of priority to reduce the offset address.	$+1D8_H$	0 to 15 (15)	High
	Channel 1 COM RX FIFO interrupt (INTRCAN1REC)	√	119	1077			$+1DC_H$	0 to 15 (15)	
	Channel 1 TX interrupt (INTRCAN1TRX)	√	120	1078			$+1E0_H$	0 to 15 (15)	
TAUJ0	Channel 0 interrupt (INTTAUJ010)		121	1079			$+1E4_H$	0 to 15 (15)	
	Channel 1 interrupt (INTTAUJ0I1)		122	107A			$+1E8_H$	0 to 15 (15)	
	Channel 2 interrupt (INTTAUJ0I2)		123	107B			$+1EC_H$	0 to 15 (15)	
	Channel 3 interrupt (INTTAUJ0I3)		124	107C			$+1F0_H$	0 to 15 (15)	
OSTM0	Timer interrupt (INTOSTM0)		125	107D			$+1F4_H$	0 to 15 (15)	
OSTM1	Timer interrupt (INTOSTM1)		126	107E			$+1F8_H$	0 to 15 (15)	
CSIG1	Reception error interrupt (INTCSIGT1IRE)		127	107F			$+1FC_H$	0 to 15 (15)	
	Reception status interrupt (INTCSIG1IR)		128	1080			$+200_H$	0 to 15 (15)	
	Communication status interrupt (INTCSIG1IC)		129	1081			$+204_H$	0 to 15 (15)	
CSIG2	Reception error interrupt (INTCSIGT2IRE)		130	1082			$+208_H$	0 to 15 (15)	
	Reception status interrupt (INTCSIG2IR)		131	1083			$+20C_H$	0 to 15 (15)	
	Communication status interrupt (INTCSIG2IC)		132	1084			$+210_H$	0 to 15 (15)	
CSIG3	Reception error interrupt (INTCSIGT3IRE)		133	1085			$+214_H$	0 to 15 (15)	
	Reception status interrupt (INTCSIG3IR)		134	1086			$+218_H$	0 to 15 (15)	
	Communication status interrupt (INTCSIG3IC)		135	1087			$+21C_H$	0 to 15 (15)	
CSIH1	Reception error interrupt (INTCSIH1IRE)		136	1088			$+220_H$	0 to 15 (15)	
	Reception status interrupt (INTCSIH1IR)		137	1089			$+224_H$	0 to 15 (15)	
	Communication status interrupt (INTCSIH1IC)		138	108A			$+228_H$	0 to 15 (15)	
	Job completion interrupt (INTCSIH1IJC)		139	108B			$+22C_H$	0 to 15 (15)	

Table 5.1 D1S1 Interrupt Exception Handler and Priority (5/7)

Functional Module	Interrupt Source Name	Level Interrupt *1	Number of Interrupt Channel	Source Code	Offset Address: Direct Branch RINT = 0	Offset Address: Direct Branch RINT = 1	Offset Address: Table Reference	Interrupt Priority (Initial Value)	Default Priority
PWM Generators and Diagnostic	A/D Converter trigger queue full interrupt (INTQFULL)		140	108C	The offset address is the same in all channels and is determined between $+100_H$ and $+1F0_H$ according to priority.	The offset address is always $+100_H$ regardless of priority to reduce the offset address.	$+230_H$	0 to 15 (15)	High
	PWM Generator channel 0 interrupt (INTPWGA0)		141	108D			$+234_H$	0 to 15 (15)	
	PWM Generator channel 1 interrupt (INTPWGA1)		142	108E			$+238_H$	0 to 15 (15)	
	PWM Generator channel 2 interrupt (INTPWGA2)		143	108F			$+23C_H$	0 to 15 (15)	
	PWM Generator channel 3 interrupt (INTPWGA3)		144	1090			$+240_H$	0 to 15 (15)	
	PWM Generator channel 4 interrupt (INTPWGA4)		145	1091			$+244_H$	0 to 15 (15)	
	PWM Generator channel 5 interrupt (INTPWGA5)		146	1092			$+248_H$	0 to 15 (15)	
	PWM Generator channel 6 interrupt (INTPWGA6)		147	1093			$+24C_H$	0 to 15 (15)	
	PWM Generator channel 7 interrupt (INTPWGA7)		148	1094			$+250_H$	0 to 15 (15)	
	PWM Generator channel 8 interrupt (INTPWGA8)		149	1095			$+254_H$	0 to 15 (15)	
	PWM Generator channel 9 interrupt (INTPWGA9)		150	1096			$+258_H$	0 to 15 (15)	
	PWM Generator channel 10 interrupt (INTPWGA10)		151	1097			$+25C_H$	0 to 15 (15)	
	PWM Generator channel 11 interrupt (INTPWGA11)		152	1098			$+260_H$	0 to 15 (15)	
	PWM Generator channel 12 interrupt (INTPWGA12)		153	1099			$+264_H$	0 to 15 (15)	
	PWM Generator channel 13 interrupt (INTPWGA13)		154	109A			$+268_H$	0 to 15 (15)	
	PWM Generator channel 14 interrupt (INTPWGA14)		155	109B			$+26C_H$	0 to 15 (15)	
	PWM Generator channel 15 interrupt (INTPWGA15)		156	109C			$+270_H$	0 to 15 (15)	
	PWM Generator channel 16 interrupt (INTPWGA16)		157	109D			$+274_H$	0 to 15 (15)	
	PWM Generator channel 17 interrupt (INTPWGA17)		158	109E			$+278_H$	0 to 15 (15)	
	PWM Generator channel 18 interrupt (INTPWGA18)		159	109F			$+27C_H$	0 to 15 (15)	
	PWM Generator channel 19 interrupt (INTPWGA19)		160	10A0			$+280_H$	0 to 15 (15)	
	PWM Generator channel 20 interrupt (INTPWGA20)		161	10A1			$+284_H$	0 to 15 (15)	
	PWM Generator channel 21 interrupt (INTPWGA21)		162	10A2			$+288_H$	0 to 15 (15)	
	PWM Generator channel 22 interrupt (INTPWGA22)		163	10A3			$+28C_H$	0 to 15 (15)	
	PWM Generator channel 23 interrupt (INTPWGA23)		164	10A4			$+290_H$	0 to 15 (15)	
ICUSD	CMD registers ready to write interrupt (INTICUSTWRDY)		165	10A5			$+294_H$	0 to 15 (15)	
	CMD registers ready to read interrupt (INTICUSTRRDY)		166	10A6			$+298_H$	0 to 15 (15)	
	Reserved	√	167	10A7			$+29C_H$	0 to 15 (15)	
	Reserved		168	10A8			$+2A0_H$	0 to 15 (15)	
	Reserved		169	10A9			$+2A4_H$	0 to 15 (15)	
	Reserved	√	170	10AA			$+2A8_H$	0 to 15 (15)	
Flash control	Flash access error (INTFLERR)	√	171	10AB			$+2AC_H$	0 to 15 (15)	
	Flash sequencer ready (INTFLENDNM)		172	10AC			$+2B0_H$	0 to 15 (15)	
	Reserved	√	173	10AD			$+2B4_H$	0 to 15 (15)	
LCBI0	Read data ready interrupt (INTLCBI0RDY)		174	10AE			$+2B8_H$	0 to 15 (15)	
	Write buffer empty interrupt (INTLCBI0EMPTY)		175	10AF			$+2BC_H$	0 to 15 (15)	
	Write buffer half full interrupt (INTLCBI0HALF)		176	10B0			$+2C0_H$	0 to 15 (15)	
	Write buffer full interrupt (INTLCBI0FULL)		177	10B1			$+2C4_H$	0 to 15 (15)	
	Write buffer quarter full interrupt (INTLCBI0QTR)		178	10B2			$+2C8_H$	0 to 15 (15)	
	Write buffer three quarters full interrupt(INTLCBI03QTR)		179	10B3			$+2CC_H$	0 to 15 (15)	
RSCAN2	Channel 2 error interrupt (INTRCAN2ERR)	√	180	10B4			$+2D0_H$	0 to 15 (15)	
	Channel 2 COM RX FIFO interrupt (INTRCAN2REC)	√	181	10B5			$+2D4_H$	0 to 15 (15)	
	Channel 2 TX interrupt (INTRCAN2TRX)	√	182	10B6			$+2D8_H$	0 to 15 (15)	
PCMP0	FIFO buffer fill interrupt (INTPCMP0FFIL)		183	10B7			$+2DC_H$	0 to 15 (15)	
	Error interrupt (INTPCMP0FERR)		184	10B8			$+2E0_H$	0 to 15 (15)	

Table 5.1 D1S1 Interrupt Exception Handler and Priority (6/7)

Functional Module	Interrupt Source Name	Level Interrupt *1	Number of Interrupt Channel	Source Code	Offset Address: Direct Branch RINT = 0	Offset Address: Direct Branch RINT = 1	Offset Address: Table Reference	Interrupt Priority (Initial Value)	Default Priority
ISM0	Target position reached interrupt (INTISM0REACHED)		185	10B9	The offset address is the same in all channels and is determined between $+100_H$ and $+1F0_H$ according to priority.	The offset address is always $+100_H$ regardless of priority to reduce the offset address.	$+2E4_H$	0 to 15 (15)	High
	Idle state interrupt (INTISM0DONE)		186	10BA			$+2E8_H$	0 to 15 (15)	
	ZPD measurement started interrupt (INTISM0ZPDAD)		187	10BB			$+2EC_H$	0 to 15 (15)	
	Reserved	√	188	10BC			$+2F0_H$	0 to 15 (15)	
SSIF0	Multi-purpose interrupt (INTSSIF0)	√	189	10BD			$+2F4_H$	0 to 15 (15)	
	Reception data full interrupt (INTSSIF0RX)	√	190	10BE			$+2F8_H$	0 to 15 (15)	
	Transmission data empty interrupt (INTSSIF0TX)	√	191	10BF			$+2FC_H$	0 to 15 (15)	
SSIF1	Multi-purpose interrupt (INTSSIF1)	√	192	10C0			$+300_H$	0 to 15 (15)	
	Reception data full interrupt (INTSSIF1RX)	√	193	10C1			$+304_H$	0 to 15 (15)	
	Transmission data empty interrupt (INTSSIF1TX)	√	194	10C2			$+308_H$	0 to 15 (15)	
	Reserved	√	195	10C3			$+30C_H$	0 to 15 (15)	
	Reserved	√	196	10C4			$+310_H$	0 to 15 (15)	
	Reserved	√	197	10C5			$+314_H$	0 to 15 (15)	
	Reserved	√	198	10C6			$+318_H$	0 to 15 (15)	
	Reserved	√	199	10C7			$+31C_H$	0 to 15 (15)	
	Reserved		200	10C8			$+320_H$	0 to 15 (15)	
	Reserved	√	201	10C9			$+324_H$	0 to 15 (15)	
	Reserved	√	202	10CA			$+328_H$	0 to 15 (15)	
	Reserved	√	203	10CB			$+32C_H$	0 to 15 (15)	
	Reserved	√	204	10CC			$+330_H$	0 to 15 (15)	
	Reserved	√	205	10CD			$+334_H$	0 to 15 (15)	
	Reserved	√	206	10CE			$+338_H$	0 to 15 (15)	
	Reserved	√	207	10CF			$+33C_H$	0 to 15 (15)	
	Reserved	√	208	10D0			$+340_H$	0 to 15 (15)	
	Reserved	√	209	10D1			$+344_H$	0 to 15 (15)	
	Reserved	√	210	10D2			$+348_H$	0 to 15 (15)	
	Reserved	√	211	10D3			$+34C_H$	0 to 15 (15)	
	Reserved	√	212	10D4			$+350_H$	0 to 15 (15)	
	Reserved	√	213	10D5			$+354_H$	0 to 15 (15)	
	Reserved	√	214	10D6			$+358_H$	0 to 15 (15)	
RLIN32	Status interrupt (INTRLIN32UR2)		215	10D7			$+35C_H$	0 to 15 (15)	
	Reception complete interrupt (INTRLIN32UR1)		216	10D8			$+360_H$	0 to 15 (15)	
	Transmission interrupt (INTRLIN32UR0)		217	10D9			$+364_H$	0 to 15 (15)	
RLIN33	Status interrupt (INTRLIN33UR2)		218	10DA			$+368_H$	0 to 15 (15)	
	Reception complete interrupt (INTRLIN33UR1)		219	10DB			$+36C_H$	0 to 15 (15)	
	Transmission interrupt (INTRLIN33UR0)		220	10DC			$+370_H$	0 to 15 (15)	
	Reserved	√	221	10DD			$+374_H$	0 to 15 (15)	
	Reserved		222	10DE			$+378_H$	0 to 15 (15)	
	Reserved	√	223	10DF			$+37C_H$	0 to 15 (15)	
	Reserved	√	224	10E0			$+380_H$	0 to 15 (15)	
	Reserved	√	225	10E1			$+384_H$	0 to 15 (15)	
	Reserved	√	226	10E2			$+388_H$	0 to 15 (15)	
	Reserved	√	227	10E3			$+38C_H$	0 to 15 (15)	
	Reserved	√	228	10E4			$+390_H$	0 to 15 (15)	
	Reserved	√	229	10E5			$+394_H$	0 to 15 (15)	

Table 5.1 D1S1 Interrupt Exception Handler and Priority (7/7)

Functional Module	Interrupt Source Name	Level Interrupt *1	Number of Interrupt Channel	Source Code	Offset Address: Direct Branch RINT = 0	Offset Address: Direct Branch RINT = 1	Offset Address: Table Reference	Interrupt Priority (Initial Value)	Default Priority
RIIC2	Receive error/event interrupt (INTRIIC2LEE)	√	230	10E6	The offset address is the same in all channels and is determined between $+100_H$ and $+1F0_H$ according to priority.	The offset address is always $+100_H$ regardless of priority to reduce the offset address.	$+398_H$	0 to 15 (15)	High
	Data received interrupt (INTRIIC2RI)		231	10E7			$+39C_H$	0 to 15 (15)	
	Data buffer empty interrupt (INTRIIC2TI)		232	10E8			$+3A0_H$	0 to 15 (15)	
	Data transmitted interrupt (INTRIIC2TEI)	√	233	10E9			$+3A4_H$	0 to 15 (15)	
	Reserved	√	234	10EA			$+3A8_H$	0 to 15 (15)	
	Reserved	√	235	10EB			$+3AC_H$	0 to 15 (15)	
	Reserved		236	10EC			$+3B0_H$	0 to 15 (15)	
	Reserved		237	10ED			$+3B4_H$	0 to 15 (15)	
	Reserved		238	10EE			$+3B8_H$	0 to 15 (15)	
	Reserved	√	239	10EF			$+3BC_H$	0 to 15 (15)	
	Reserved	√	240	10F0			$+3C0_H$	0 to 15 (15)	
	Reserved	√	241	10F1			$+3C4_H$	0 to 15 (15)	
	Reserved	√	242	10F2			$+3C8_H$	0 to 15 (15)	
	Reserved		243	10F3			$+3CC_H$	0 to 15 (15)	
	Reserved	√	244	10F4			$+3D0_H$	0 to 15 (15)	
	Reserved	√	245	10F5			$+3D4_H$	0 to 15 (15)	
	Reserved	√	246	10F6			$+3D8_H$	0 to 15 (15)	
	Reserved	√	247	10F7			$+3DC_H$	0 to 15 (15)	
	Reserved		248	10F8			$+3E0_H$	0 to 15 (15)	
	Reserved		249	10F9			$+3E4_H$	0 to 15 (15)	
	Reserved		250	10FA			$+3E8_H$	0 to 15 (15)	
	Reserved		251	10FB			$+3EC_H$	0 to 15 (15)	
	Reserved	√	252	10FC			$+3F0_H$	0 to 15 (15)	
	Reserved		253	10FD			$+3F4_H$	0 to 15 (15)	
	Reserved	√	254	10FE			$+3F8_H$	0 to 15 (15)	
Internal bus errors	This interrupt is logical OR combination of various internal bus error indications. The exact cause of this error interrupt can be evaluated by use of the bus error status registers. Refer to *Section 7.4.7, Bus Error Status Registers* of *H/W manual* for details.		255	10FF			$+3FC_H$	0 to 15 (15)	

Section 6 DMA

This section indicate D1S1 DMA trigger source list.

The differences from RH850/D1L1 is that DMA triggers that are come from RIIC2 are appended to channel 121 and 122.

All the other DMA related features are same with RH850/D1L series. Please refer H/W manual of RH850/D1L series for more detail.

Table 6.1 List of DMA Trigger Sources (1/4)

DMA Trigger ID	DMA Trigger Factor	Module	DMA Trigger Source
0	INTP0	Port	External inputs
1	INTP1		
2	INTP2		
3	INTP3		
4	INTP4		
5	INTP5		
6	INTP6		
7	INTP7		
8	INTP8		
9	INTP9		
10	INTP10		
11	INTDMAFL	Data flash	Signal for DMA program command*1
12	INTLBCI0RDY	LCBI0	Write buffer empty interrupt
13	INTLCBI0EMPTY		Write buffer half full interrupt
14	INTLCBI0HALF		Write buffer full interrupt
15	INTLCBI0FULL		Write buffer quarter full interrupt
16	INTLCBI0QTR		Write buffer three quaters full interrupt
17	INTLCBI03QTR		Write buffer empty interrupt
18	INTPWGA0	PWGA	PWM Generator 0 interrupt
19	INTPWGA1		PWM Generator 1 interrupt
20	INTPWGA2		PWM Generator 2 interrupt
21	INTPWGA3		PWM Generator 3 interrupt
22	INTPWGA4		PWM Generator 4 interrupt
23	INTPWGA5		PWM Generator 5 interrupt
24	INTPWGA6		PWM Generator 6 interrupt
25	INTPWGA7		PWM Generator 7 interrupt
26	INTPWGA8		PWM Generator 8 interrupt
27	INTPWGA9		PWM Generator 9 interrupt
28	INTPWGA10		PWM Generator 10 interrupt
29	INTPWGA11		PWM Generator 11 interrupt
30	INTPWGA12		PWM Generator 12 interrupt
31	INTPWGA13		PWM Generator 13 interrupt
32	INTPWGA14		PWM Generator 14 interrupt
33	INTPWGA15		PWM Generator 15 interrupt
34	INTPWGA16		PWM Generator 16 interrupt

Table 6.1 List of DMA Trigger Sources (2/4)

DMA Trigger ID	DMA Trigger Factor	Module	DMA Trigger Source
35	INTTAUB0I0	TAUB0	Channel 0 interrupt
36	INTTAUB0I1		Channel 1 interrupt
37	INTTAUB0I2		Channel 2 interrupt
38	INTTAUB0I3		Channel 3 interrupt
39	INTTAUB0I4		Channel 4 interrupt
40	INTTAUB0I5		Channel 5 interrupt
41	INTTAUB0I6		Channel 6 interrupt
42	INTTAUB0I7		Channel 7 interrupt
43	INTTAUB0I8		Channel 8 interrupt
44	INTTAUB0I9		Channel 9 interrupt
45	INTTAUB0I10		Channel 10 interrupt
46	INTTAUB0I11		Channel 11 interrupt
47	INTTAUB0I12		Channel 12 interrupt
48	INTTAUB0I13		Channel 13 interrupt
49	INTTAUB0I14		Channel 14 interrupt
50	INTTAUB0I15		Channel 15 interrupt
51	INTTAUB1I0	TAUB1	Channel 0 interrupt
52	INTTAUB1I1		Channel 1 interrupt
53	INTTAUB1I2		Channel 2 interrupt
54	INTTAUB1I3		Channel 3 interrupt
55	INTTAUB1I4		Channel 4 interrupt
56	INTTAUB1I5		Channel 5 interrupt
57	INTTAUB1I6		Channel 6 interrupt
58	INTTAUB1I7		Channel 7 interrupt
59	INTTAUB1I8		Channel 8 interrupt
60	INTTAUB1I9		Channel 9 interrupt
61	INTTAUB1I10		Channel 10 interrupt
62	INTTAUB1I11		Channel 11 interrupt
63	INTTAUB1I12		Channel 12 interrupt
64	INTTAUB1I13		Channel 13 interrupt
65	INTTAUB1I14		Channel 14 interrupt
66	INTTAUB1I15		Channel 15 interrupt

Table 6.1 List of DMA Trigger Sources (3/4)

DMA Trigger ID	DMA Trigger Factor	Module	DMA Trigger Source
67	INTTAUB2I0	TAUB2	Channel 0 interrupt
68	INTTAUB2I1		Channel 1 interrupt
69	INTTAUB2I2		Channel 2 interrupt
70	INTTAUB2I3		Channel 3 interrupt
71	INTTAUB2I4		Channel 4 interrupt
72	INTTAUB2I5		Channel 5 interrupt
73	INTTAUB2I6		Channel 6 interrupt
74	INTTAUB2I7		Channel 7 interrupt
75	INTTAUB2I8		Channel 8 interrupt
76	INTTAUB2I9		Channel 9 interrupt
77	INTTAUB2I10		Channel 10 interrupt
78	INTTAUB2I11		Channel 11 interrupt
79	INTTAUB2I12		Channel 12 interrupt
80	INTTAUB2I13		Channel 13 interrupt
81	INTTAUB2I14		Channel 14 interrupt
82	INTTAUB2I15		Channel 15 interrupt
83	INTTAUJ0I0	TAUJ0	Channel 0 interrupt
84	INTTAUJ0I1		Channel 1 interrupt
85	INTTAUJ0I2		Channel 2 interrupt
86	INTTAUJ0I3		Channel 3 interrupt
87	INTRLIN30UR0	RLIN30	Transmit interrupt
88	INTRLIN30UR1		Receive completion interrupt
89	INTRLIN31UR0	RLIN31	Transmit interrupt
90	INTRLIN31UR1		Receive completion interrupt
91	INTRLIN32UR0	RLIN32	Transmit interrupt
92	INTRLIN32UR1		Receive completion interrupt
93	INTRLIN33UR0	RLIN33	Transmit interrupt
94	INTRLIN33UR1		Receive completion interrupt
95	INTCSIG0C	CSIG0	Communication status interrupt
96	INTCSIG0R		Reception status interrupt
97	INTCSIG1C	CSIG1	Communication status interrupt
98	INTCSIG1R		Reception status interrupt
99	INTCSIG2C	CSIG2	Communication status interrupt
100	INTCSIG2R		Reception status interrupt
101	INTCSIG3C	CSIG3	Communication status interrupt
102	INTCSIG3R		Reception status interrupt
103	INTCSIH0IC	CSIH0	Communication status interrupt
104	INTCSIH0IR		Reception status interrupt
105	INTCSIH0IJC		Job completion interrupt
106	INTCSIH1IC	CSIH1	Communication status interrupt
107	INTCSIH1IR		Reception status interrupt
108	INTCSIH1IJC		Job completion interrupt
109	INTRIIC0TI	RIIC0	Data buffer empty interrupt
110	INTRIIC0RI		Receive end interrupt

Table 6.1 List of DMA Trigger Sources (4/4)

DMA Trigger ID	DMA Trigger Factor	Module	DMA Trigger Source
111	INTRIIC1TI	RIIC1	Data buffer empty interrupt
112	INTRIIC1RI		Receive end interrupt
113	INTSSIF0TX	SSIF0	Transmission data empty
114	INTSSIF0RX		Reception data full
115	INTSSIF1TX	SSIF1	Transmission data empty
116	INTSSIF1RX		Reception data full
117	INTPCMP0FFIL	PCMP0	FIFO buffer fill interrupt
118	INTSG0TI	SG0	Threshold interrupt
119	Reserved		
120	Reserved		
121	INTRIIC2RI	RIIC2	Receive end interrupt
122	INTRIIC2TI		Data buffer empty interrupt
123	INTADCE0I1	ADCE0	Scan group 1 interrupt
124	INTADCE0I2		Scan group 2 interrupt
125	INTADCE0I3		Scan group 3 interrupt
126	DMA_WR_REQ	ICUSD	CMD registers are ready to write
127	DMA_RD_REQ		CMD registers are ready to read

Note 1. For details, refer to the RH850/D1x Flash Memory User's Manual: Hardware Interface.

Section 7 I2C Bus Interface (RIIC)

RH850/D1S1 has an additional RIIC I2C Bus Interface (RIIC).

This section describes the differences of RIIC specification from the other RH850/D1L/D1M specification.

7.1 Features of RH850/D1S1 RIIC

7.1.1 Number of Units and Channels

This microcontroller has the following number of RIIC units.

Each RIIC unit has one channel interface. “Number of channels” is used with the same meaning as “number of units” in this section.

Table 7.1 Number of Units

Product Name	D1S1
Number of Units	3
Name	RIICn (n = 0, 1, 2)

Table 7.2 Index

Index	Meaning
n	Throughout this section, the individual RIIC units are identified by the index “n” (n = 0, 1, 2): for example, RIICnCR1 is the I2C bus control register1

7.1.2 Register Base Address

RIIC base addresses are listed in the following table.

RIIC register addresses are given as offsets from the base addresses in general.

Table 7.3 Register Base Address

Index	Meaning
<RIIC0_base>	FFDB 0000_H
<RIIC1_base>	FFDB 1000_H
<RIIC2_base>	FFDB 2000_H

7.1.3 Clock Supply

The RIIC clock supply is shown in the following table.

Table 7.4 Clock Supply

Index	Meaning	Meaning
RIICn	PCLK	Clock Controller CLKJIT

Note 1. Set the period of PCLK no greater than 1/2 of the width at high level of the SCL clock.

7.1.4 Interrupt Requests

RIIC interrupt requestes are listed in the following table.

Table 7.5 Clock Supply

RIICn signals	Function	Connected to
RIIC0		
INTIICnEE	Transfer Error/Event Generation	
INTIICnRI	Receive complete	
INTIICnTI	Transmit data empty	
INTIICnTEI	Transmit end	
RIIC1		
INTIICnEE	Transfer Error/Event Generation	
INTIICnRI	Receive complete	
INTIICnTI	Transmit data empty	
INTIICnTEI	Transmit end	
RIIC2		
INTIICnEE	Transfer Error/Event Generation	
INTIICnRI	Receive complete	
INTIICnTI	Transmit data empty	
INTIICnTEI	Transmit end	

7.1.5 Reset Sources

RIIC reset sources are listed in the following table. RIIC is initialized by these reset sources.

Table 7.6 Register Base Address

Unit Name	Reset Source
RIICn	• Reset Controller SYSRES • reset upon wake-up from DEEPSTOP mode

7.1.6 External Input/Output Signals

External input/output signals of RIIC are listed below.

Table 7.7 Clock Supply

Unit Signal Name	Outline	Alternative Port Pin Signal
RIIC0		
RIICnSCL	Serial clock I/O pin	RIIC0SCL
RIICnSDA	Serial data I/O pin	RIIC0SDA
RIIC1		
RIICnSCL	Serial clock I/O pin	RIIC1SCL
RIICnSDA	Serial data I/O pin	RIIC1SDA
RIIC2		
RIICnSCL	Serial clock I/O pin	RIIC2SCL
RIICnSDA	Serial data I/O pin	RIIC2SDA

When using these ports, the PBDCn register for the corresponding port and the corresponding bit in the PODCn register must be set to 1.

7.1.7 PBUS Structure

Each RIIC channels are connected to following PBUS Guard channels.

Table 7.8 PBUS Structure for RIIC0, 1 and 2

PBUS		PBUS Guard		
Main	**Sub**	**Guard**	**Channel**	**Module**
PBUS3	PBUS30	—		PBG30A
		—		PBG30B
		PBG30A	0	CSIG0*1
			1	CSIG1*1
			2	CSIG2*1
			3	CSIG3*1
			4	CSIH0*1
			5	CSIH1*1
			6	CSIG0*2
			7	CSIG1*2
			8	CSIG2*2
			9	CSIG3*2
			10	CSIH0*2
			11	CSIH1*2
			12	RIIC0
			13	RIIC1
			14	ISM0
			15	P30A_ERRSLV
		PBG30B	0	ECCISM0
			1	P30B_ERRSLV
			2	RIIC2
			3 to 15	Reserved

Note 1. CSIGn/CSIHn registers whose offset address are within 0000 0000_H to 0000 $0FFF_H$

Note 2. CSIGn/CSIHn registers whose offset address are within 0000 1000_H to 0000 $1FFF_H$

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		Page	Summary
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1.00	Dec 25, 2018	Section 1 Overview	
		8	document number correction ("r01ds0304ej0xxx" -> "r01ds0245ej0xxx")
		Section 2 Changing Features	
		10	correction: ICU-S2 -> ICUSD
		10	D1S1 and D1L1 "Package" specifications in overview table unified
		11	correction in block diagram: ICU-S2 -> ICUSD
		Section 3 Pins	
		14	section "Input buffer characteristics" added
		39	"JTAG Port 0 (JP0)" pin function table revised
		41	typo correction ("LPD 1-pin" -> "LPD (1-pin)")
		42	typo correction ("Unused" -> "Not Used")
		42	typo correction ("Unused" -> "Not Used")
		Section 5 Interrupt	
		47	"Source Code" column content in (2/7) table part corrected
		48	typo correction ("(INTCSIG0IR"-> "(INTCSIG0IR)")
		48	typo correction ("(INTCSIG0IC" -> "(INTCSIG0IC)")
		51	correction: ICU-S2 -> ICUSD
		Section 6 DMA	
		54	Data flash interrupt added
		57	correction: ICUS2 -> ICUSD

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