User's Manual

R-IN32M4-CL3

User's Manual: Board design edition

R9A06G064MGBG
R9A06G064SGBG

arm

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is intended for users who wish to understand the functions of industrial Ethernet communications ASSP (Application Specific Standard Product) “R-IN32M4-CL3” (R9A06G064MGBG, R9A06G064SGBG) and design application systems using it. It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

Related Documents	The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Please be understanding of this beforehand. In addition, because we make document at development, planning of each core, the related document may be the document for individual customers. Last four digits of document number indicate version information of each document. Please download the latest document from our web site and refer to it.

The document related to R-IN32M4-CL3

Document Name	Document Number
R-IN32M4-CL3 User’s Manual: Hardware edition	R18UZ0073EJ0100
R-IN32M4-CL3 User’s Manual: Gigabit Ethernet PHY edition	R18UZ0075EJ0100
R-IN32M4-CL3 User’s Manual: Board Design edition (This manual)	R18UZ0074EJ0100
R-IN32M4-CL3 User’s Manual: CC-Link IE TSN edition	R18UZ0070EJ0100
R-IN32M4-CL3 User’s Manual: CC-Link IE Field edition	R18UZ0071EJ0100
R-IN32M4-CL3 Programming Manual: Driver	R18UZ0076EJ0100
R-IN32M4-CL3 Programming Manual: OS	R18UZ0072EJ0100

2. Notation of Numbers and Symbols

Weight in data notation: Left is high-order column, right is low-order column

Active low notation:

xxxZ (capital letter Z after pin name or signal name)

or xxx_N (capital letter _N after pin name or signal name)

or xxnx (pin name or signal name contains small letter n)

Note:

Explanation of (Note) in the text

Caution:

Item deserving extra attention

Remark:

Supplementary explanation to the text

Numeric notation:

Binary … xxxx , xxxxB or n'bxxxx (n bits)

Decimal … xxxx

Hexadecimal … xxxxH or n'hxxxx (n bits)

Prefixes representing powers of 2 (address space, memory capacity):

K (kilo)… $2^{10} = 1024$

M (mega)… $2^{20} = 1024^2$

G (giga)… $2^{30} = 1024^3$

Data Type:

Word … 32 bits

Halfword … 16 bits

Byte … 8 bits

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1. Overview

This manual is intended for being used by engineers that work on a circuit and PCB design that is equipped with an Ethernet communication LSI from the R-IN32M4-CL3 made by Renesas Electronics.

The target device is the R-IN32M4-CL3. It is recommended to study this manual carefully and to follow the recommendations during the circuit and board design.

1.1 Definition of Pin Handling and Symbols in This Manual

Pin handling and symbols are defined as follows in this manual.

Table 1.1 Definition of Pin Handling

	Description
Low level	This pin is connected to GND.
High level	This pin supplies VDD33 (3.3 V).

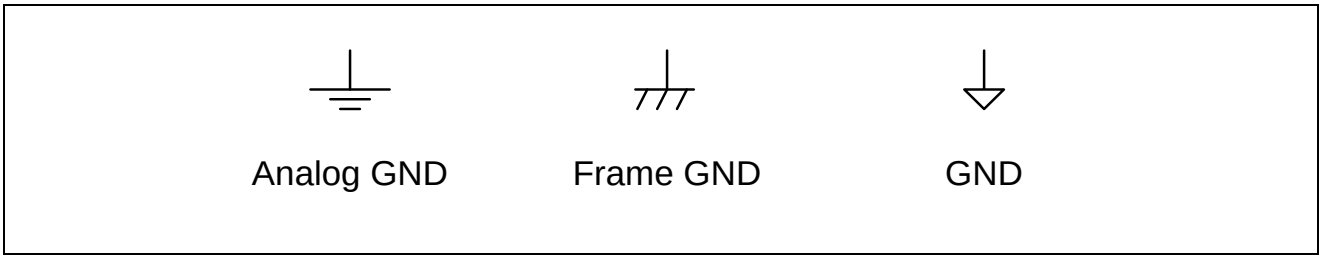


Figure 1.1 Definition of GND Symbols

2. Power/Reset Pins

2.1 Power-On/Off Sequence

Table 2.1 lists external power supplies to R-IN32M4-CL3. In addition, Figure 2.1 and Figure 2.3 show the power-on/off sequence.

There is no particular rule for the power-on sequence. We recommend supplying external power voltage VDD11 first and then supplying external power voltage VDD33. On the other hand, when turning off the power, disconnect VDD33, then VDD11.

If VDD33 is supplied first, note that the I/O modes of the I/O buffers are not fixed and outputs become undefined over the period between VDD33 and VDD11 rising to their thresholds.

3.3 V must be applied to the input pins only after the power supply voltages have been applied.

Table 2.1 External Power Supply

External Power Supply	Voltage [V]	External Pin Name
VDD33	3.3 ± 0.165	VDD33 VDDREG_33 AVDDREG_33
VDD25	2.5 ± 0.125	VDD25A
VDD11	1.15 ± 0.06	VDD11 VDD11A PLL_VDD

2.1.1 Power-On/Off Sequence without 2.5-V built-in Regulator

(1) Supplying Power Voltages

Supply power voltages so that the following two conditions are both satisfied.

1. The period from when VDD33, VDD25, or VDD11 reaches 10% VDD to when all of them reach 90% VDD or higher is within 100 ms.
2. The period from when VDD33, VDD25, or VDD11 reaches 95% VDD to when all of them reach 95% VDD or higher is within 50 ms.

(2) Turning Off Power Voltages

Turn off power voltages so that the following two conditions are both satisfied.

1. The period from when VDD33, VDD25, or VDD11 reaches 90% VDD to when all of them reach 10% VDD or lower is within 100 ms.
2. The period from when VDD33, VDD25, or VDD11 reaches 95% VDD to when all of them reach 95% VDD or lower is within 50 ms.

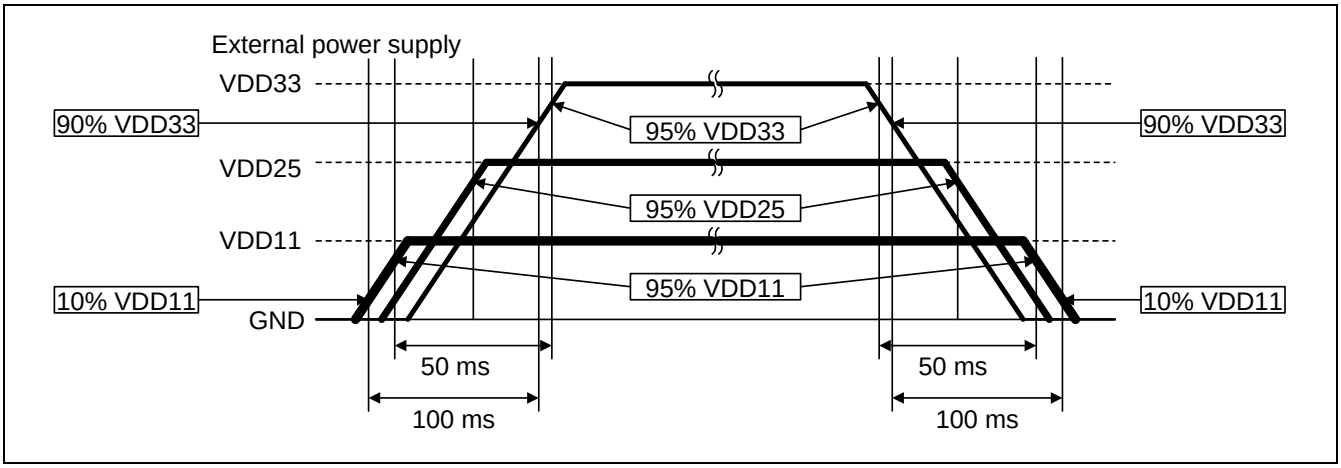


Figure 2.1 Power-On/Off Sequence (without 2.5-V built-in Regulator)

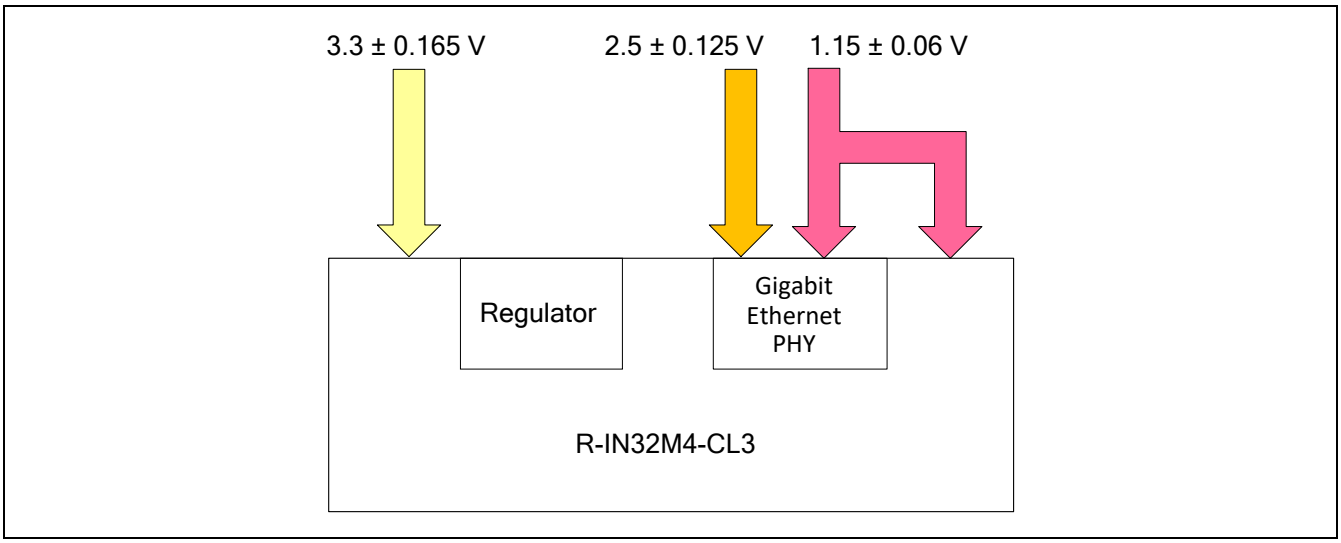


Figure 2.2 Power Supply Channel to R-IN32M4-CL3 (without 2.5-V built-in Regulator)

2.1.2 Power-On/Off Sequence with 2.5-V built-in Regulator

(1) Supplying Power Voltages

Supply power voltages so that the following two conditions are both satisfied.

1. The period from when VDD33 or VDD11 reaches 10% VDD to when both of them reach 90% VDD or higher is within 100 ms.
2. The period from when VDD33 or VDD11 reaches 95% VDD to when both of them reach 95% VDD or higher is within 49 ms.

(2) Turning Off Power Voltages

Turn off power voltages so that the following two conditions are both satisfied.

1. The period from when VDD33 or VDD11 reaches 90% VDD to when both of them reach 10% VDD or lower is within 100 ms.
2. The period from when VDD33 or VDD11 reaches 95% VDD to when both of them reach 95% VDD or lower is within 49 ms.

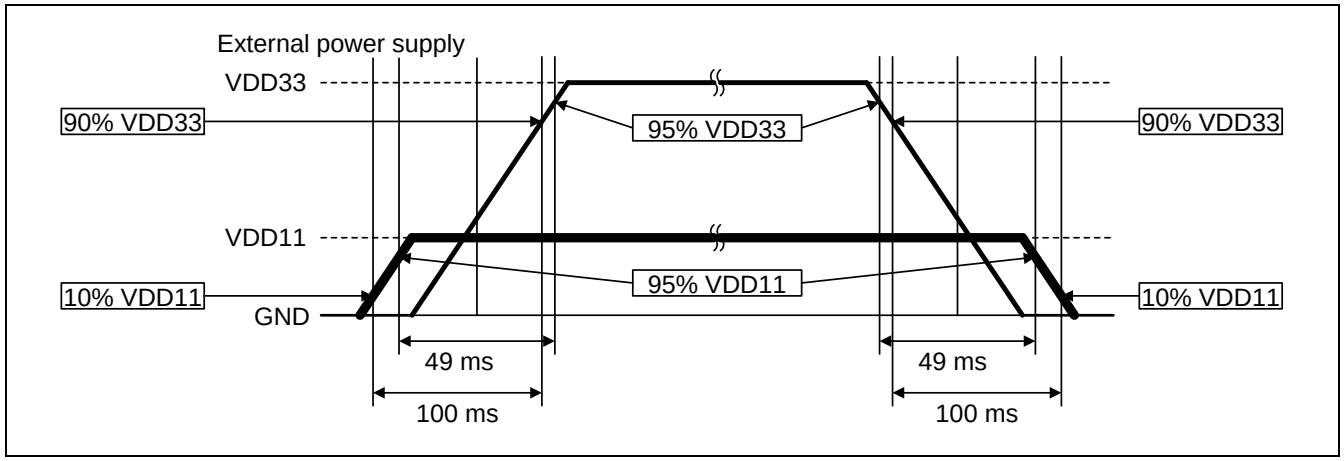


Figure 2.3 Power-On/Off Sequence (with 2.5-V built-in Regulator)

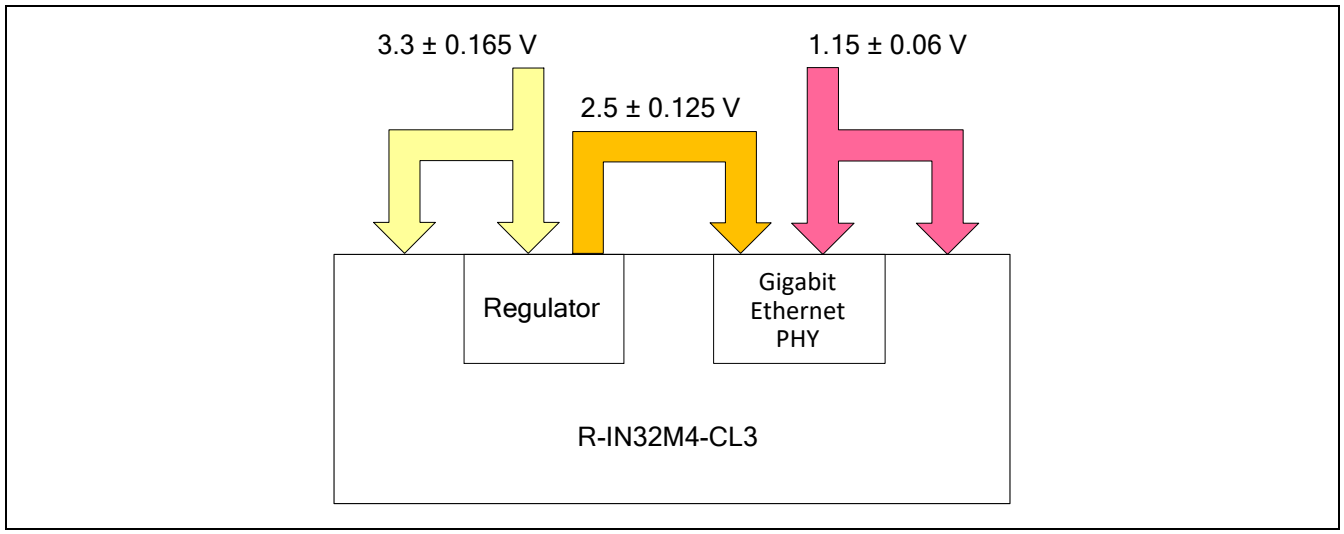


Figure 2.4 Power Supply Channel to R-IN32M4-CL3 (with 2.5-V built-in Regulator)

2.2 Power Supply Pins

This is a list of power supply pins of R-IN32M4-CL3. When designing with these pins, refer to the connection example as follows.

Pin Name	Function	Reference for Connection Example
PLL_VDD	PLL power supply (1.15 V)	See Section 4, PLL Power Supply Pins.
PLL_GND	PLL_GND	See Section 4, PLL Power Supply Pins.
VDD33	R-IN32M4 I/O power supply (3.3 V)	Supply power from the power unit such as a regulator or DC-DC converter.
VDD11	R-IN32M4 internal power supply (1.15 V)	Supply power from the power unit such as a regulator or DC-DC converter.
GND	Ground potential for power supply (GND)	Connect GND of the system (board).
VDD25A	GbE-PHY analog power supply (2.5 V)	See Section 6.1, Power Supply Peripheral Circuit.
VDD11A	GbE-PHY analog power supply (1.15 V)	See Section 6.1, Power Supply Peripheral Circuit.
VDDREG_33	2.5-V built-in regulator power supply (3.3 V)	See Section 7, 2.5-V built-in Regulator Peripheral Circuit Configuration.
AVDDREG_33	2.5-V built-in regulator power supply (3.3 V)	See Section 7, 2.5-V built-in Regulator Peripheral Circuit Configuration.
AGND	Ground potential for 2.5-V built-in regulator power supply (GND)	See Section 7, 2.5-V built-in Regulator Peripheral Circuit Configuration.

2.3 Reset Pins

This is a list of reset pins of R-IN32M4-CL3.

As a width at low level of at least 1 μs is required for the reset input signals, secure this by applying the low level of the reset signal over the oscillation stabilization time of the external oscillator (25 MHz).

In addition, de-assert the RESETZ and HOTRESETZ signals after de-asserting the PONRZ signal.

Pin Name	Function	Reference for Connection Example
PONRZ	Power-on reset input (including built-in RAM initialization)	—
RESETZ	Reset input	—
HOTRESETZ	Hot reset input (reset pin for bypass mode of CC-Link IE field)	—
TRSTZ	JTAG reset signal	See Section 15, JTAG/Trace Pins.
RSTOUTZ	External reset output	—

3. Clock Input Pins

3.1 Pin Functions

This is a list of pin functions of clock input pins.

Pin Name	Attribute	Function
XT1	I/O	Connects an external oscillator. When OSCTH = 0, this pin functions as an output pin. In external clock input mode (OSCTH = 1), drive XT1 to the low level.
XT2	Input	Connects an external oscillator. In external clock input mode (OSCTH = 1), the clock signal from an external oscillator is input via XT2.
OSCTH[Note]	Input	Selects the clock oscillation source to be connected to the clock pin. Low level: XT1 and XT2 are to be connected to a resonator. High level: XT2 is to be connected to an oscillator.

Caution: For the AC characteristics of the input clock, refer to Section 29.8.1 (1) “Input Clock” in the “R-IN32M4-CL3 User's Manual: Hardware edition”.

Note: Connection with an oscillator is recommended.

3.2 Notes on Configuring the Oscillation Circuit

As the R-IN32M4-CL3 includes an oscillation block, oscillation circuits are easily configurable by externally connecting a resonator and components for external constants. Though configuring an oscillation circuit is easy, the configured circuit is analog and operates at a high frequency, so notes that differ from the usual logic circuit configuration.

To achieve stable operation of the oscillation circuit, set components for external constants to the optimum values (capacitors on the input and output sides, and limiting resistors) and observe the following points required for an analog circuit.

- Place the oscillation circuit near the R-IN32M4-CL3.
- Place the oscillation circuit as far as possible from high-frequency input pins such as clock pins.
- Place the resonators and components for external constants immediately close to the input and output pins of oscillation circuit, and keep the connections as short as possible.
- Make the ground connections of the capacitors to the GND pins of R-IN32M4-CL3 as short and thick as possible.
- Make the lead wires between the resonator and capacitors as short as possible.
- Surround the components for external constant parts by as much GND wiring as is possible.

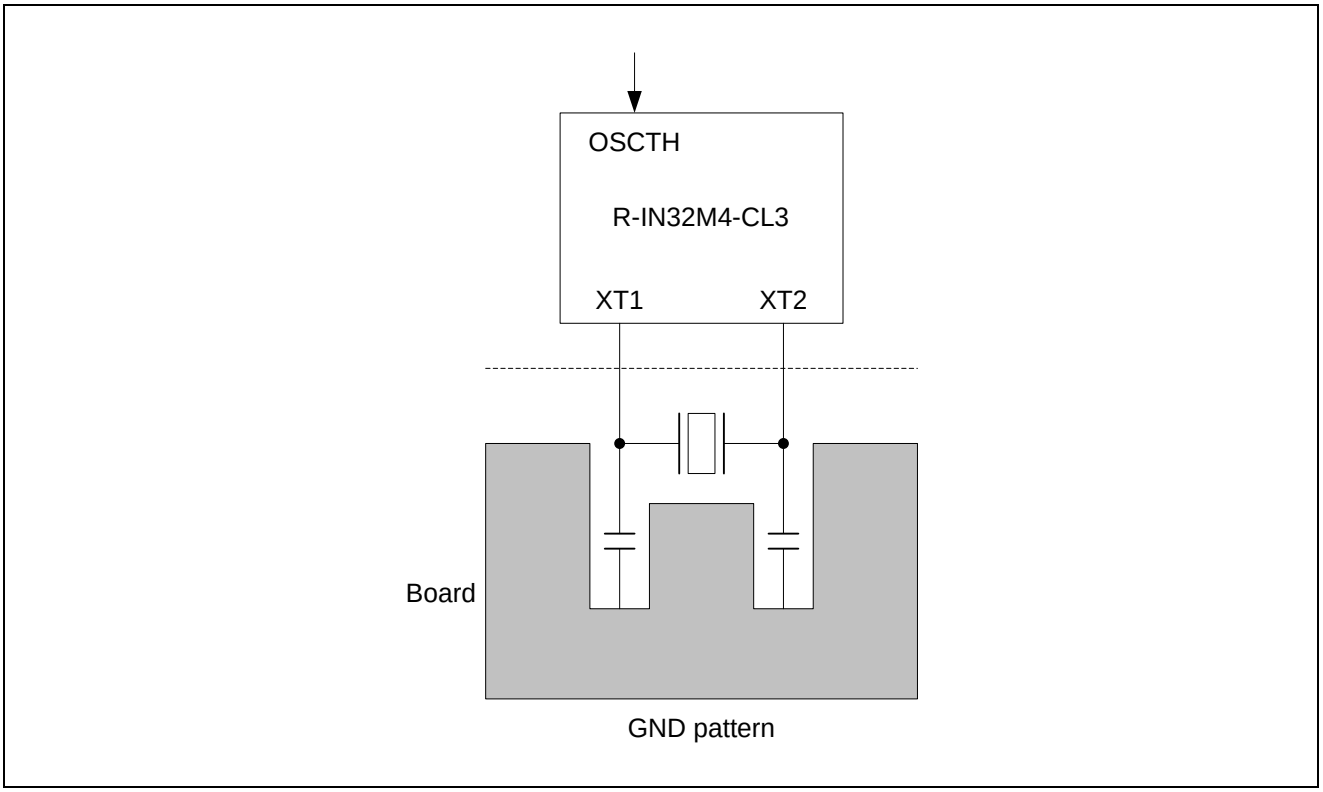


Figure 3.1 Example of GND Pattern for the Components for External Constants

In addition, the following points to note should be observed in evaluating and determining the external constants.

- The range of oscillating operation may vary due to the dielectric constant of the board's material, so use the actual printed circuit board that will be used in the finished design.
- Check use of the board with the developed R-IN32M4-CL3 and the actual resonator to be mounted on it.

3.3 Configuration Example of Oscillation Circuits

The following figure shows the configuration example of oscillation circuits.

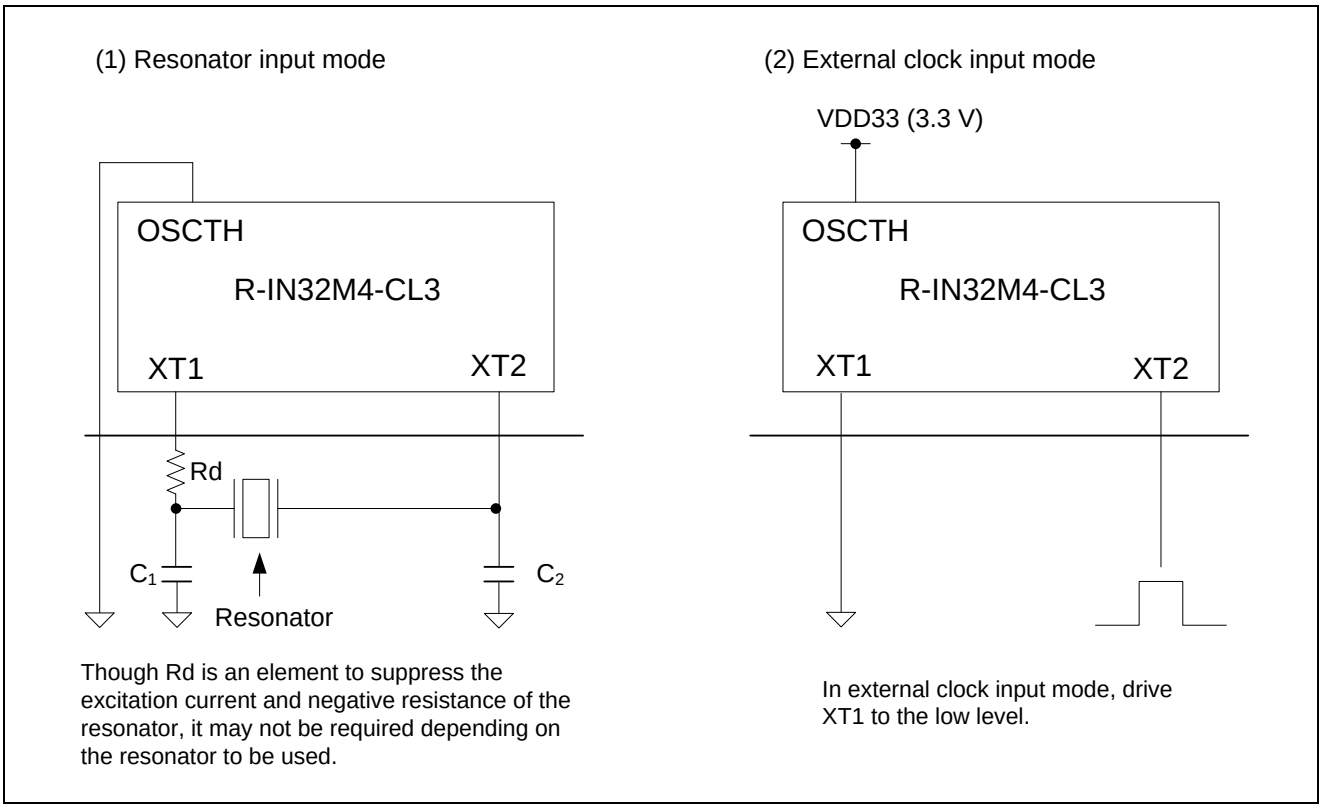


Figure 3.2 Configuration Example of the Oscillation Circuit

Caution: The input of the R-IN32M4-CL3 is fixed to 25 MHz.
When a resonator is to be used, contact the resonator manufacturer and ask for a corresponding part number and external constants.
Renesas recommends the following oscillator and resonator manufacturers.

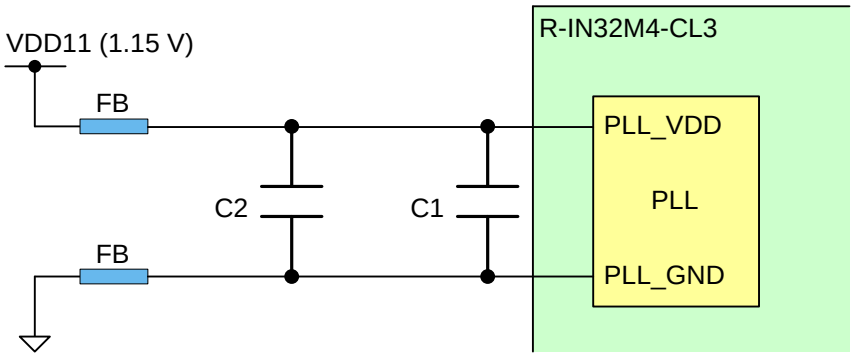
- **Nihon Dempa Kogyo Co., Ltd. (NDK)**
  http://www.ndk.com/en/index.html
- **KYOCERA Crystal Device Corporation**
  https://global.kyocera.com/prdct/electro/product/crystal-device/

4. PLL Power Supply Pins

The PLL circuit is susceptible to noise. To reduce the influence of noise, it is recommended to place filters in the power supply pins of the PLL. In addition, to reduce the effects of noise between the power supplies for the board and PLL, the use of ferrite beads is recommended.

4.1 Recommended Configuration of Filter

Figure 4.1 shows the recommended configuration of the filter for the PLL power supply pins.



C1: 0.1-µF ceramic capacitor
C2: ≥ 4.7-µF capacitor
FB: Impedance: 600 Ω at 100 MHz / DC resistance component: 0.3 Ω or below
Reference ferrite beads: TDK MPZ2012S601A, MPZ1608S601A

Figure 4.1 Recommended Configuration of Filter

Caution: Place C1 immediately close to R-IN32M4-CL3.
If C2 is not placed immediately close to R-IN32M4-CL3, this will not cause any problems.

4.2 Notes on Placement of Peripheral Components

The 0.1-µF ceramic capacitor (C1) should be placed immediately close to R-IN32M4-CL3 (in the immediate vicinity of the pin).

Figure 4.2 is a schematic view from below the board.

In addition, the wiring patterns for the electrolytic capacitor (C2) and ferrite beads running parallel to other signal lines should be avoided.

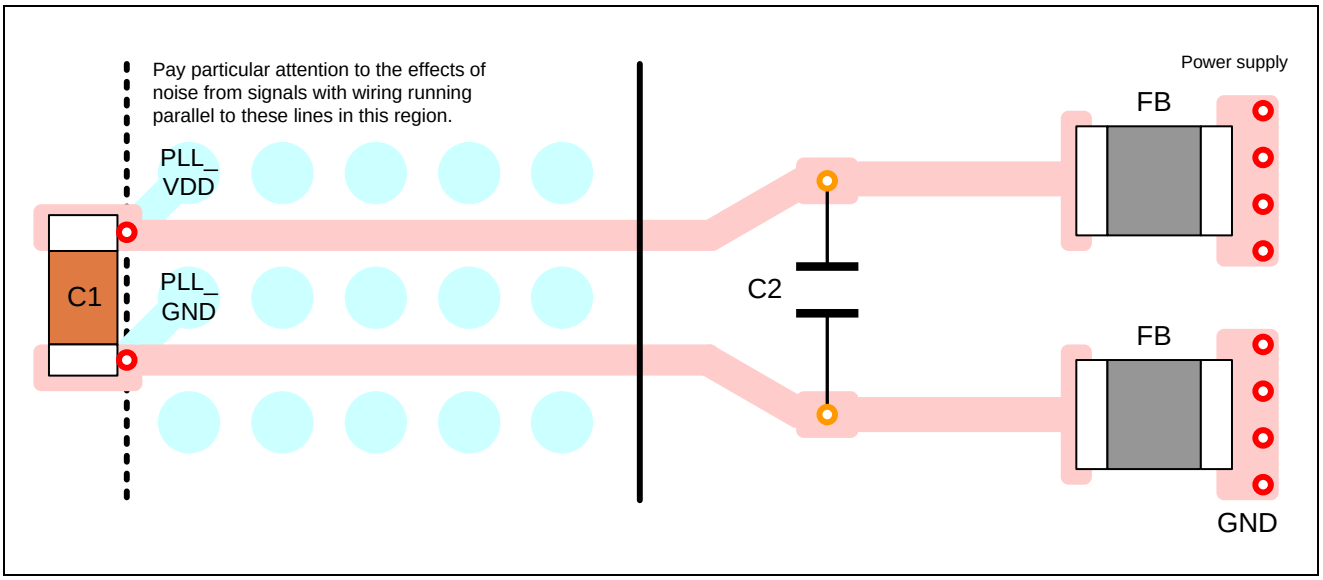


Figure 4.2 Schematic View from Below the Board

Caution: PLL_VDD and PLL_GND lines should be as short and thick as possible in PCB wiring. Longer wiring leads to stronger crosstalk because the LC components of the wiring increase, more readily leading to effects.

5. GPIO Port Pins

GPIO is a general-purpose I/O port. As for the internal configuration, see the section in the following document.

Section 27 “Port Functions” in the “R-IN32M4-CL3 User’s Manual: Hardware edition”

6. Gigabit Ethernet PHY Pins

Since the Gigabit Ethernet PHY interface handles high-speed transfer, designing the board pattern for it and other components requires full consideration on numerous points.

Design it in accord with the advice in this section.

6.1 Power Supply Peripheral Circuit

6.1.1 Circuit Configuration

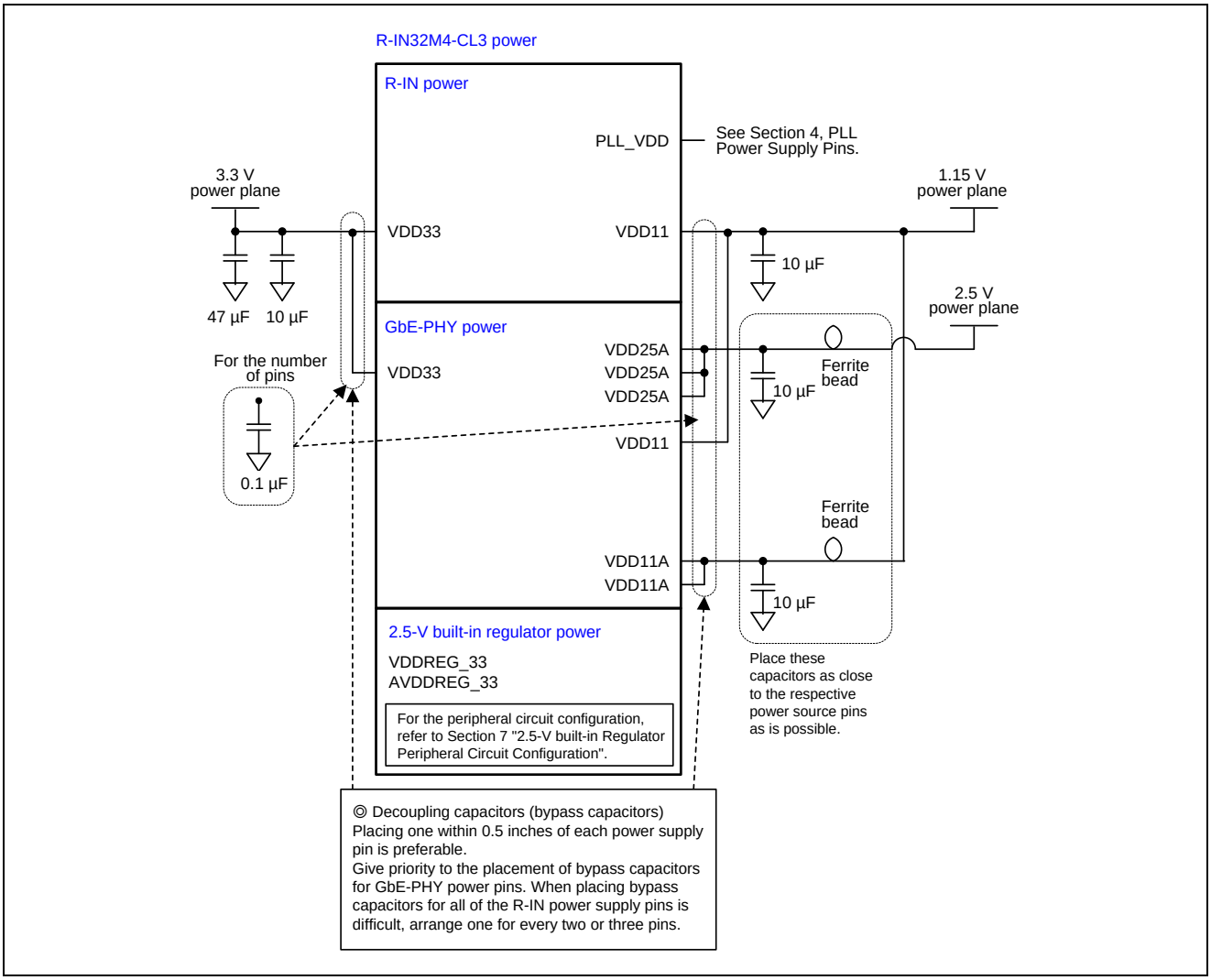


Figure 6.1 Configuration of Gigabit Ethernet PHY Power Supply Peripheral Circuit

6.1.2 Recommended Components

(1) Ceramic capacitors

We recommend using components that satisfy the following conditions.

Capacitors: 47 μF, 10 μF, and 0.1 μF
Thermal characteristic: X5R or X7R
ESR: No more than 0.1 Ω (from 100 kHz to 100 MHz)

Table 6.1 Example of Recommended Components of Ceramic Capacitors

Manufacturer	Part Number	Capacitance
TDK	C32165R1C476M1160AB	47 μF
TDK	C2012X5R1C106K085AC	10 μF

(2) Ferrite beads

We recommend using components that satisfy the following conditions.

Impedance: At least 80 Ω (at 100 MHz)
Use beads with a high impedance in which the resistive component is dominant.
Rated current: At least 2 A
DC resistance: No more than 50 mΩ

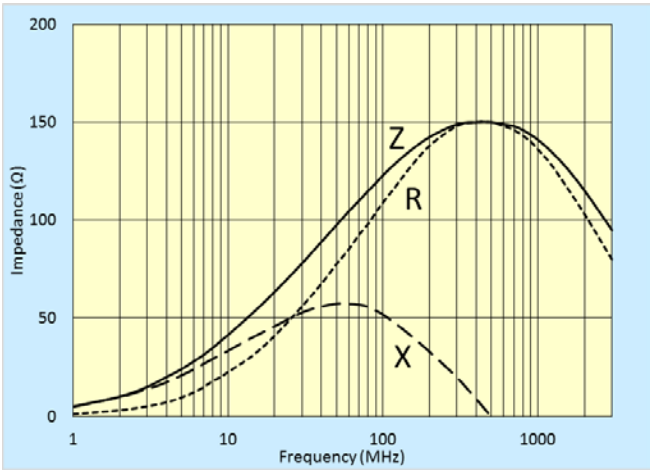


Figure 6.2 Example of Recommended Impedance Characteristics with Frequency of Ferrite Beads

Table 6.2 Example of Recommended Components of Ferrite Beads

Manufacturer	Part Number	Impedance	Rated Current	DC Resistance
muRata	BLM18PG121SN1	120 Ω ± 25%	2 A	50 mΩ
muRata	BLM21PG121SN1	120 Ω ± 25%	3 A	30 mΩ

6.2 Peripheral Circuit of Pulse Transformer

An example of the circuit configuration for the Gigabit Ethernet PHY, pulse transformers, and RJ-45 connector, and recommended pulse transformer products are shown below.

6.2.1 Example of Circuit Configuration

The circuits should be connected as shown in the following figure.

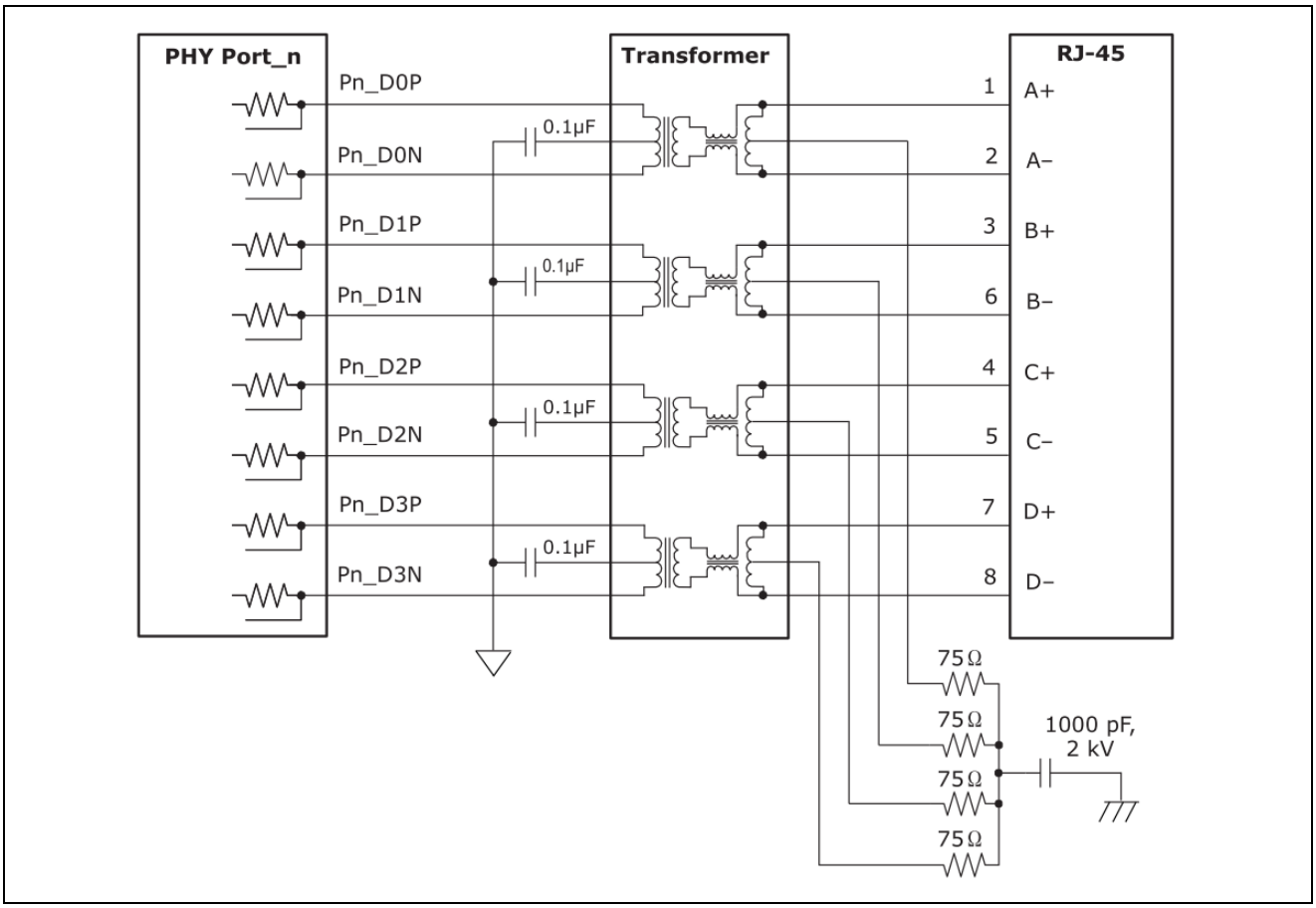


Figure 6.3 Peripheral Connection Example of Pulse Transformer

Remark: n = 0, 1

6.2.2 Recommended Components

We recommend using pulse transformer that satisfy the following conditions.

We also recommend the constitution illustrated in Transformer of Figure 6.3.

Common-mode chokes are not required on the R-IN32M4-CL3 (PHY side) and is mounted on the connector.

Winding ratio: 1:1 (±2% or less, or ±3%) recommended

Return loss (see Figure 6.4): -18dB or less (from 1.0 MHz to 40 MHz)

-(12-20log(f/80))dB or less (from 40 MHz to 100 MHz) *f: Frequency

Caution: We recommend as little variation in return loss from 1.0 MHz to 40 MHz as possible.
The impedance is 85, 100, or 115 Ω.
For details, contact the corresponding manufacturer.

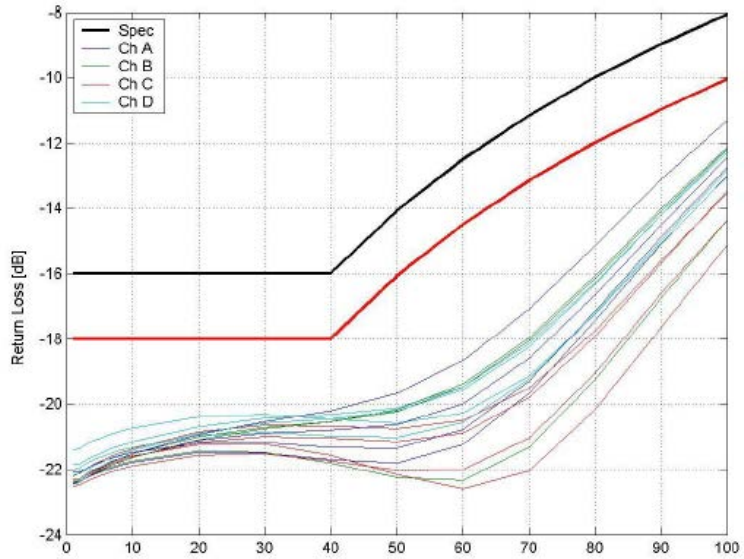


Figure 6.4 Example of Return Loss of Pulse Transformer

Recommended components of the pulse transformer as listed below.

Manufacturer	Product Type Name
Pulse	H5008NL

6.3 REF_REXT and REF_FILT Pins

The method of handling the REF_REXT and REF_FILT pins and recommended values for the connected components are shown below.

6.3.1 Example of Circuit Configuration

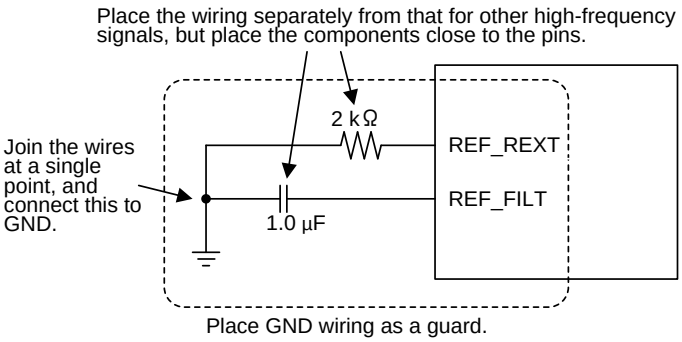


Figure 6.5 Example of Circuit Configuration for REF_REXT and REF_FILT

6.3.2 Recommended Resistors

We recommend using components that satisfy the following conditions.

Resistance value: 2 kΩ, 1% accuracy
Rated power: At least 0.0625 W

6.3.3 Recommended Ceramic Capacitors

We recommend using components that satisfy the following conditions.

Capacitance: 1.0 µF, 10% accuracy
Thermal characteristic: C0G, X7R, or X5R

6.4 Notes on Board Wiring

Pay attention to the following notes when placing the wiring on the board.

- Avoid long wiring runs. We recommend placing the pulse transformer and the connector immediately as close as possible to R-IN32M4-CL3.
- The components should be placed so that differential signal traces of TxP/N and RxP/N do not cross.
- Differential signal traces should be routed straight and as short as possible.
- Bends in lines should be at angles of at least 135 degrees. (Figure 6.7)
- Differential signal traces between the R-IN32M4-CL3, pulse transformer, and RJ-45 connector should be designed with a differential impedance of 100 Ω ± 10% and with an impedance of 50 Ω relating to GND.
- Differential signal traces between the R-IN32M4-CL3 and pulse transformer, and those between the pulse transformer and RJ-45 connector, should be equal in length. 0.5 mm is the maximum deviation. Each of the differential signal traces in each pair must be as nearly equal in length as is possible.
- The designs of signal lines for differential signals should be symmetrical. They should run parallel to each other and be routed in the same layer. Placement of components, via holes, and the like should also be symmetrical.
- Branches in signal lines act as stubs and should thus be avoided.
- Place traces for differential signals with separation from those for other signals. We recommend the width of the gap to another signal line be at least five times the width of each differential signal trace.
- Differential signal traces should not cross edges of the power/GND planes. The GND plane is desirable as the layer below the differential signal trace.
- Do not place any wiring, including any part of the power and GND planes, below the pulse transformer.
- Differential signal traces should be routed via as few via holes as possible. If via holes are essential, pay attention to the following points.
  - We recommend via holes for the related power and GND planes to be placed near the signal vias. The width between the via holes for a signal and GND should be equal to the distance between the layers to avoid a discontinuity in the impedance.
  - Metal (wiring or via) close to the differential signal via holes could affect the impedance.
  - The diameter of a via hole should be almost equal to the width of the trace.

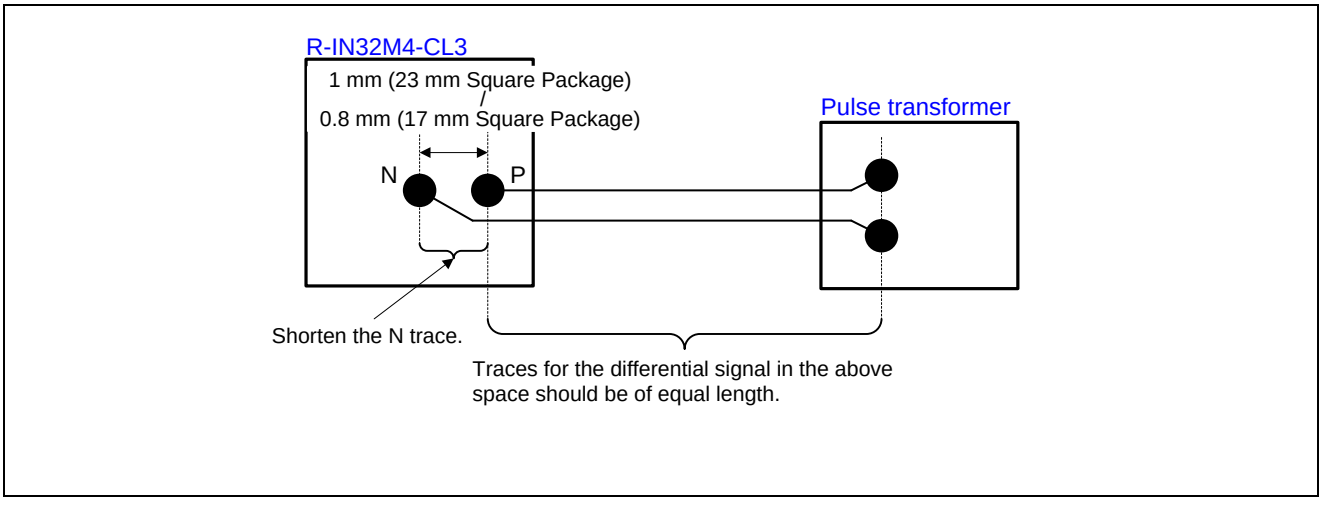


Figure 6.6 Example of Wiring for Differential Signals (1)

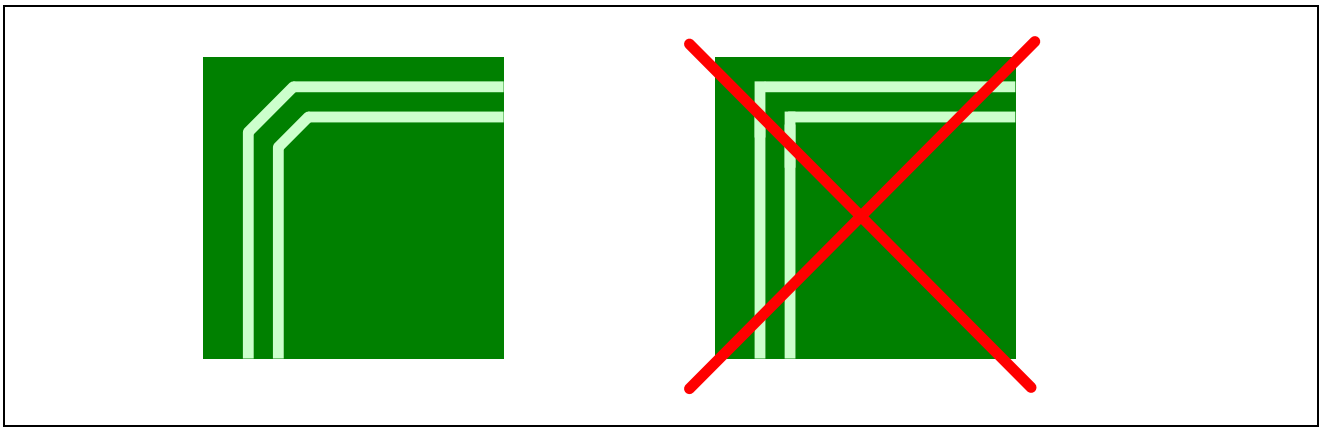


Figure 6.7 Example of Wiring for Differential Signals (2)

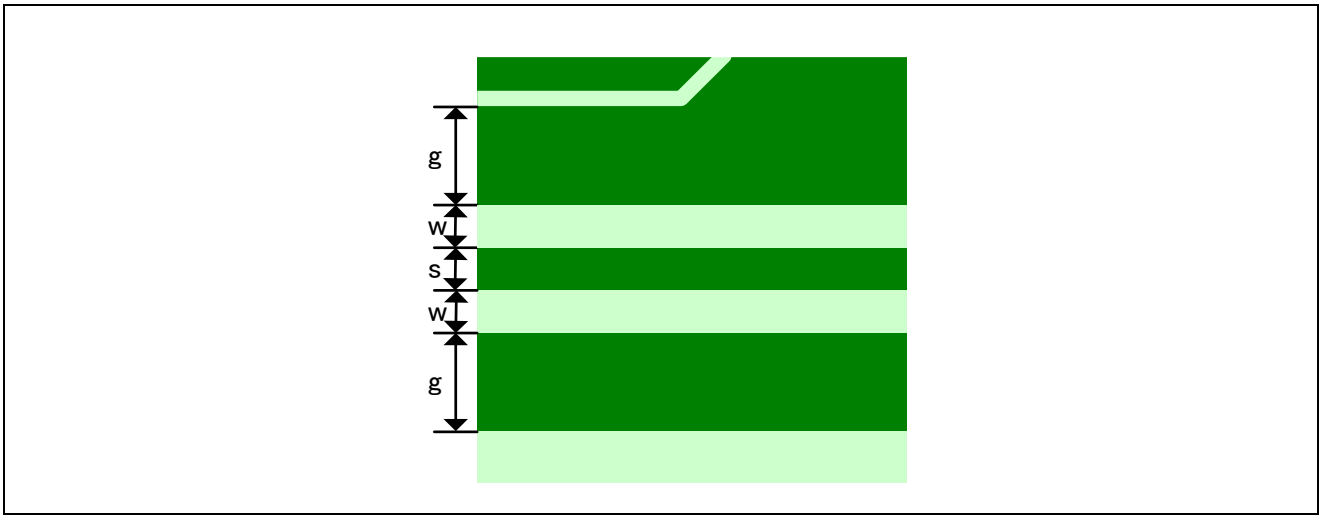


Figure 6.8 Example of Wiring for Differential Signals (3)

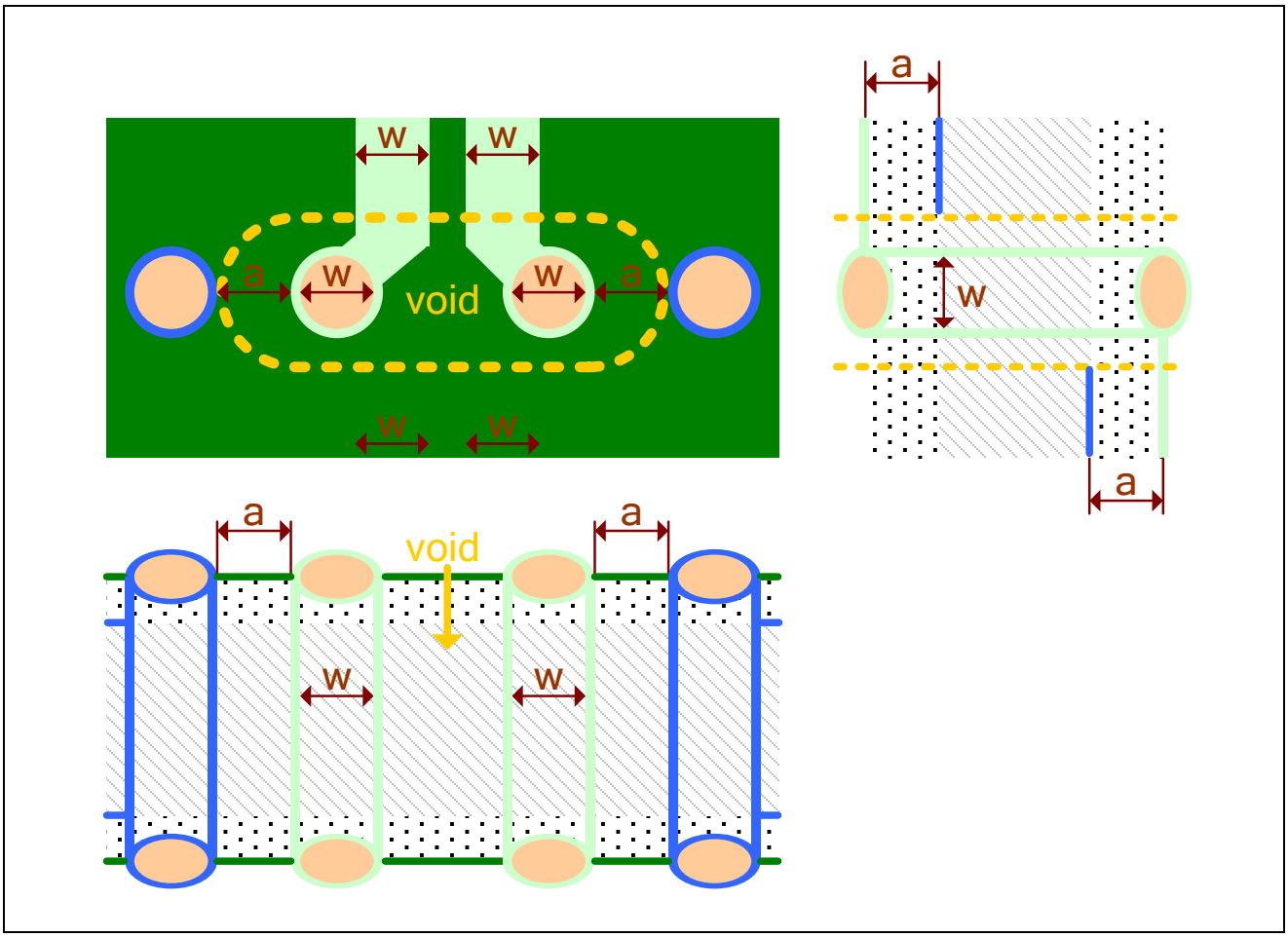


Figure 6.9 Example of Wiring for Differential Signals (4)

6.5 Unused GbE-PHY

Comply with the following requirements even when GbE-PHY is not in use.

- Always power supply to the VDD25A and VDD11A pins.
- The method of handling the REF_REXT and REF_FILT pins is the same way as for normal operation. (See Section 6.3, REF_REXT and REF_FILT Pins.)
- MDI signal (P[0:1]_D[3:0]N, P[0:1]_D[3:0]P) pins are open.

7. 2.5-V built-in Regulator Peripheral Circuit Configuration

This section describes the peripheral circuit configuration of the 2.5-V built-in regulator installed in R-IN32M4-CL3.

7.1 Peripheral Connection Configuration with 2.5-V built-in Regulator

This figure shows a peripheral connection configuration with the 2.5-V built-in regulator.

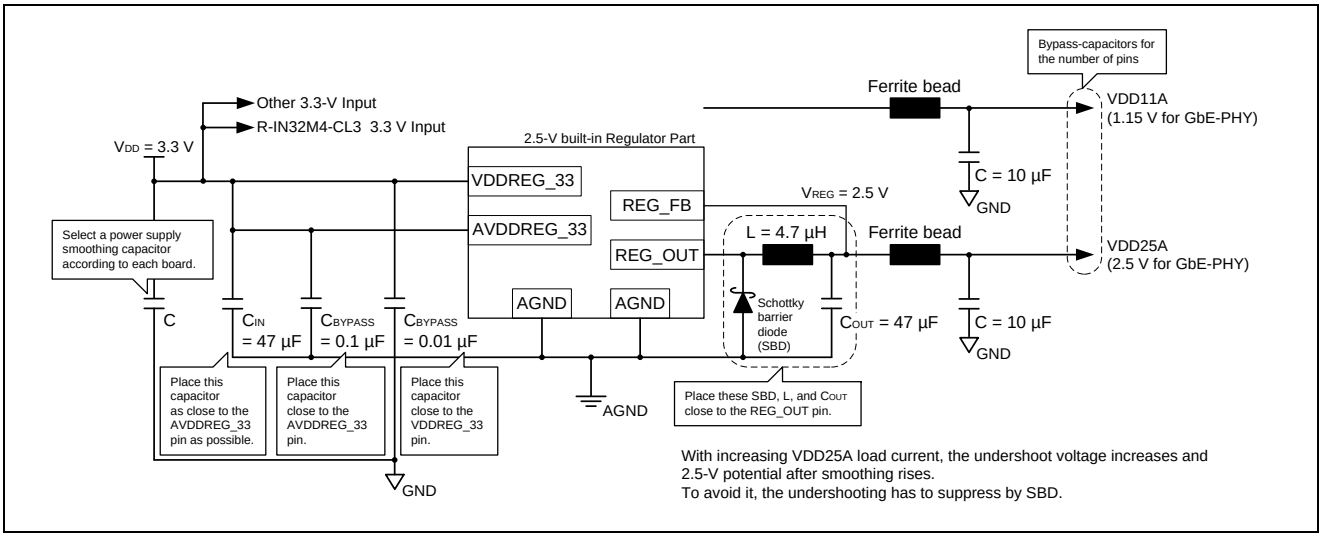


Figure 7.1 Peripheral Connection Configuration with 2.5-V built-in Regulator

7.2 Peripheral Connection Configuration without 2.5-V built-in Regulator

This figure shows a peripheral connection configuration without the 2.5-V built-in regulator.

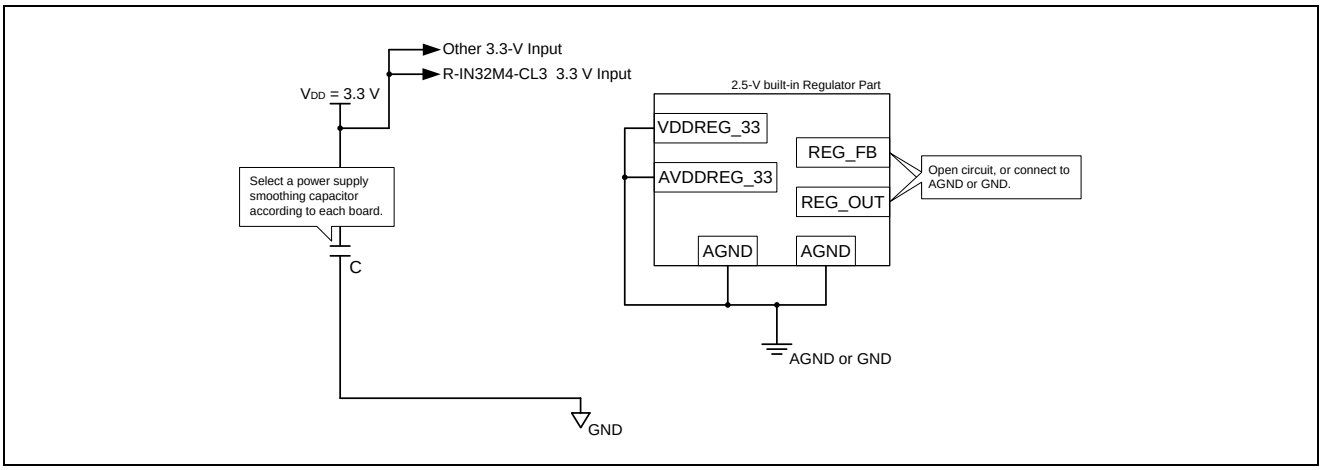


Figure 7.2 Peripheral Connection Configuration without 2.5-V built-in Regulator

7.3 Recommended Components of Inductor and Capacitors

The inductor and ceramic capacitors recommended for L and C_{IN}, C_{OUT}, and C_{BYPASS} are shown.

(1) Inductor (L)

- Inductance: 4.7 µH ± 30%
- DC resistance: Max 100 mΩ
- Rated current: Min 600 mA

Table 7.1 Example of Recommended Component of Inductor

Manufacturer	Part Number	Inductance
TDK	VLS5045EX-4R7M	4.7 µH

(2) Ceramic Capacitors (C_{IN}, C_{OUT}, C_{BYPASS})

- Capacitance: 47 µF (C_{IN}), 47 µF (C_{OUT}), 0.1 µF (C_{BYPASS} for AVDDREG_33), and 0.01 µF (C_{BYPASS} for VDDREG_33)
- Thermal characteristic: X5R or X7R
- ESR (C_{IN}): Max 20 mΩ (from 700 kHz to 1.3 MHz)
  ESR (C_{OUT}): Max 100 mΩ (from 700 kHz to 1.3 MHz)

Table 7.2 Capacitance Definition (C_{IN}, C_{OUT})

C	Capacitance	lower limit	upper limit
C_{IN}	47 µF	10 µF	no definition
C_{OUT}	47 µF	14 µF	200 µF

Select the components in considering the DC bias and temperature characteristics.

Table 7.3 Example of Recommended Components of Ceramic Capacitors

C	Manufacturer	Part Number	Capacitance
C_{IN}	TDK	C2012X5R1A476M125AC	47 µF
C_{OUT}	TDK	C2012X5R1A476M125AC	47 µF

7.4 Recommended Component of Schottky barrier diode

Recommended Schottky barrier diode specifications are shown.

- Forward voltage: about 0.4 V (smaller is better)
- Forward current: 1.0 A or more
- Terminal capacitance: about 60 pF @ 3 V (smaller is better)

Table 7.4 Example of Recommended Components of Schottky barrier diode

Manufacturer	Part Number
TOSHIBA	CUS10F30
TDK	RSX101VAM30

The above components were selected based on the specifications. It is necessary to select a component based on a customer's evaluation.

7.5 Example of PCB Layout Image (23 mm Square BGA Package)

This section describes the peripheral circuit configuration of the 2.5-V built-in regulator installed in the R-IN32M4-CL3 in a 23 mm square BGA package.

7.5.1 L1 and L2 (23 mm Square BGA Package)

Followings are layout conditions and an example of PCB layout image (at the lower left of the L1 and L2).

- Separate AGND of the built-in regulator from Digital GND as far as possible.
- Do not pass through AGND under the MDI signal and the inductor component (L).

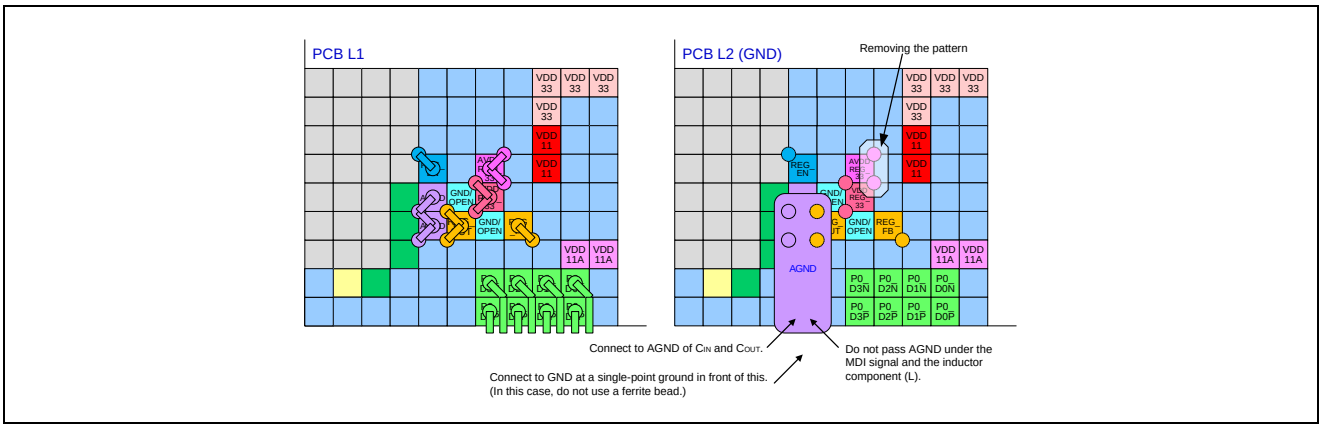


Figure 7.3 Example of PCB Layout Image (L1 and L2) (23 mm Square BGA Package)

7.5.2 L3 and L4 (23 mm Square BGA Package)

Followings are layout conditions and an example of PCB layout image (at the lower left of the L3 and L4).

- Place C_{BYPASS} as close to the power supply pins (VDDREG_33 and AVDDREG_33).
  Also, place L, C_{IN}, and C_{OUT} as close to the relevant pins as possible. In particular, placement of C_{IN} is a high priority.
- Minimize the parasitic inductance of AVDDREG_33 pattern as small as possible.

The AVDDREG_33, AGND, and REG_OUT signals should be careful to avoid affecting other signals.

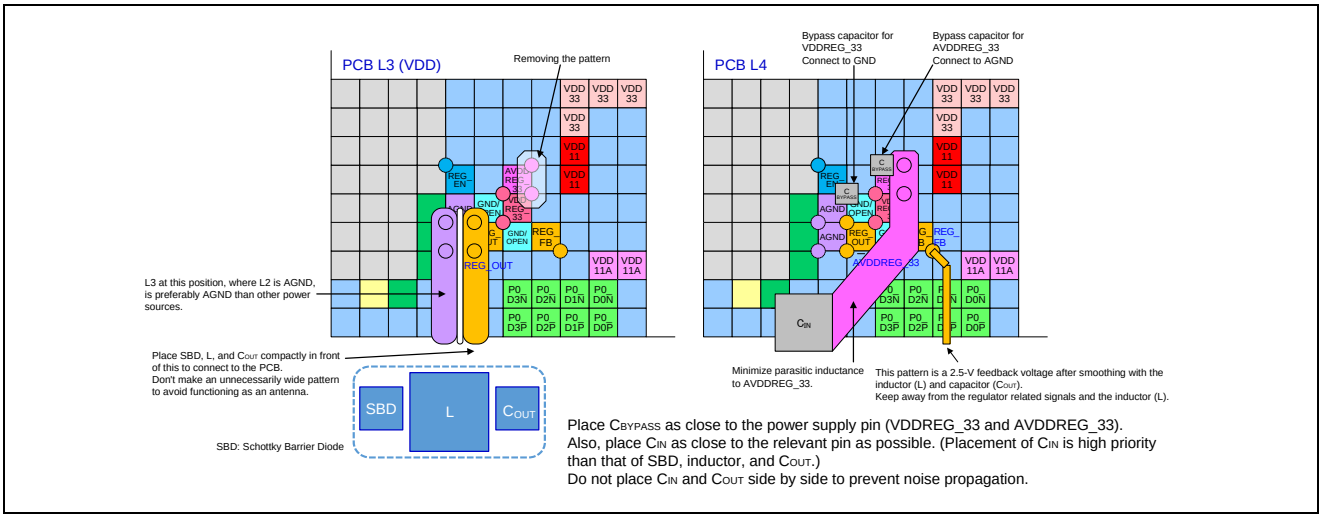


Figure 7.4 Example of PCB Layout Image (L3 and L4) (23 mm Square BGA Package)

7.6 Example of PCB Layout Image (17 mm Square BGA Package)

This section describes the peripheral circuit configuration of the 2.5-V built-in regulator installed in the R-IN32M4-CL3 in a 17 mm square BGA package.

7.6.1 L1 and L2 (17 mm Square BGA Package)

Followings are layout conditions and an example of PCB layout image (at the lower left of the L1 and L2).

- Separate AGND of the built-in regulator from Digital GND as far as possible.
- Do not pass through AGND under the MDI signal and the inductor component (L).
- Place C_{BYPASS} as close to the power supply pins (VDDREG_33 and AVDDREG_33).
  Also, place L, C_{IN}, and C_{OUT} as close to the relevant pins as possible. In particular, placement of C_{IN} is a high priority.
- Minimize the parasitic inductance of AVDDREG_33 pattern as small as possible.

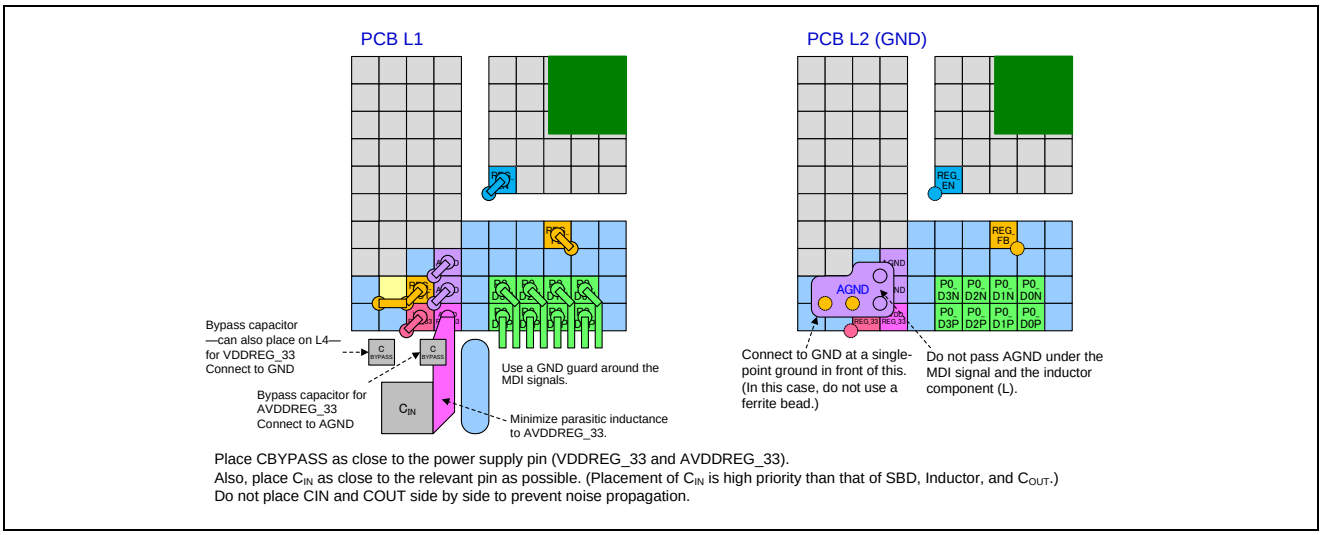


Figure 7.5 Example of PCB Layout Image (L1 and L2) (17 mm Square BGA Package)

7.6.2 L3 and L4 (17 mm Square BGA Package)

Followings are layout conditions and an example of PCB layout image (at the lower left of the L3 and L4).

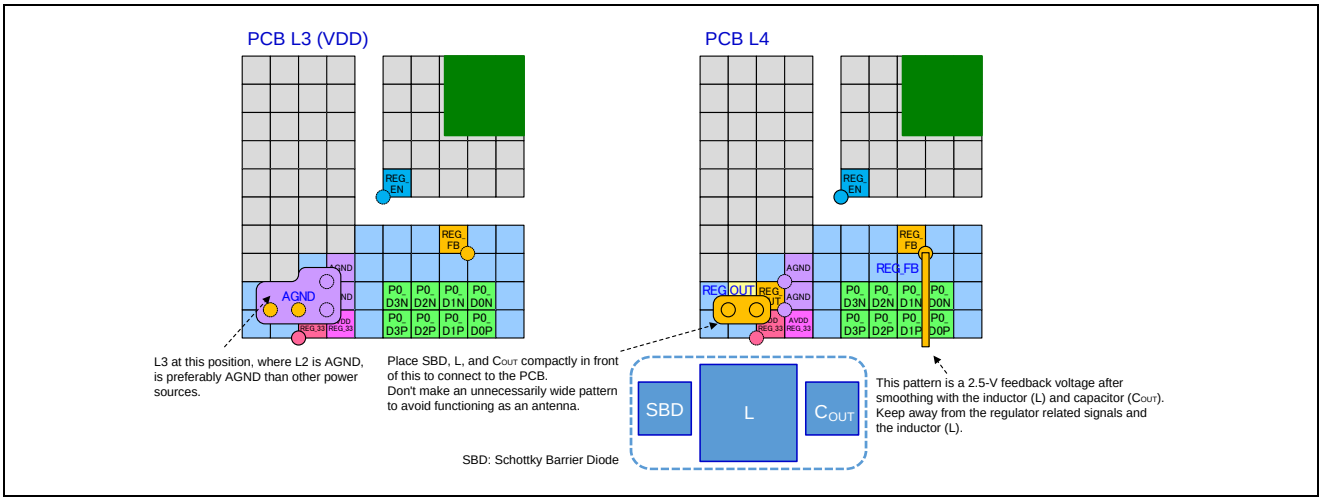


Figure 7.6 Example of PCB Layout Image (L3 and L4) (17 mm Square BGA Package)

7.7 Requirements for Parasitic Resistances and Parasitic Inductances in PCB

In this PCB layout, draw patterns so that the parasitic resistances and the parasitic inductances satisfy the followings.

Table 7.5 Requirements for Parasitic Resistances and Parasitic Inductances in PCB

Ball (23 mm Square BGA Package)	Ball (17 mm Square BGA Package)	Pin Name	Parasitic Resistance	Parasitic Inductance	
G6	D1	AVDDREG_33	≤ 40 mΩ	≤ 4 nH	From ball to C_{IN}
E4, E5	D2, D3	AGND	≤ 40 mΩ	≤ 4 nH	From ball to C_{IN}
F4	C2	REG_OUT	≤ 40 mΩ	—	From ball to inductor (L)
H4	H4	REG_FB	≤ 400 mΩ	≤ 15 nH	From ball to the connection point of the inductor (L) and C_{OUT}

8. Thermal Design

This section describes the thermal characteristics of the R-IN32M4-CL3, and includes notes that require attention in the design of the board on which the device is mounted in terms of the dissipation of heat and the prevention of abnormal heating. Since the R-IN32M4-CL3 incorporates a Gigabit Ethernet PHY module and large-capacity memory, it requires greater consideration of heat than most devices.
Design the board and casing in consideration of heat dissipation.

8.1 Deciding on whether Particular Measures for Heat Dissipation are Required

8.1.1 Estimating Tj

Take Tj ≤ 125°C as the criterion for Tj of the R-IN32M4-CL3. Estimate Tj from the following formulae.

Tj = Tt + Ψjt x power or Tj = Ta + θja x power

- Tj: Junction temperature [°C]
- Tt: Package surface temperature [°C]
- Ta: Ambient temperature [°C]
- θja: Thermal resistance [°C/W] between the junction (at temperature Tj) and the ambient environment (at Ta) (See 8.1.3, Thermal Resistances under the JEDEC Conditions (for θja and Ψjt).)
- Ψjt: Thermal resistance [°C/W] between the junction (at temperature Tj) and the surface of the package (at Tt) (See 8.1.3, Thermal Resistances under the JEDEC Conditions (for θja and Ψjt).)
- Power: Power dissipation [W] (1.15-V sub-systems + 2.5-V sub-systems + 3.3-V sub-systems)

If Tj ≤ 125°C is satisfied, the semiconductor device does not require further measures for heat dissipation.
However, if the semiconductor device is to be installed in ways that have varying criteria for determining increases in temperature, prepare measures for heat dissipation as required.
If Tj ≤ 125°C is not satisfied, heat dissipation solutions are necessary.

8.1.2 Estimating Power Consumption

For the 3.3-V, 2.5-V, and 1.15-V sub-systems, estimate the power consumption from the value for current on the R-IN32M4-CL3 user's manual.

8.1.3 Thermal Resistances under the JEDEC Conditions (for θja and Ψjt)

The thermal resistances under the JEDEC-2S2P conditions are as follows.
However, these values are for the devices alone; care is required since the actual thermal resistances will depend on the board, casing, and peripheral components.

	θja [°C/W]	Ψjt [°C/W]
R-IN32M4-CL3, 23 mm Square BGA Package	19.8	0.35
R-IN32M4-CL3, 17 mm Square BGA Package	20.6	0.36

The thermal resistance value θja of R-IN32M4-CL3 varies depending on the mounting board, housing, and peripheral components.
If there are criteria for increases in temperature (Δt = Tt - Ta) as a final product, prepare measures to obtain θja that achieves the target Δt, referring to section 8.2, Examples of Measures for Heat Dissipation.

8.2 Examples of Measures for Heat Dissipation

We classify measures for heat dissipation into two types. For details, see the following pages.

(1) Measures for heat release in designing the board
- Take these types of measures into consideration when designing the board.
- The following measures are highly effective, so implement them as a matter of course.

(I) Thermal vias
(II) VDD/GND pattern
(III) Increase the number of board layers, and bring the GND pattern out to the surface layer. Note1
(IV) Consider other factors of placement that will affect heat flows and take the appropriate action.Note2

(2) Heat dissipation from the periphery (including the casing)
- If the measures listed in (1) above still don't achieve your criterion for Δt or satisfy the condition Tj = 125°C or below, further measures for heat dissipation in the form of heat sinks or heat dissipating gels should be applied, including for the casing as a whole if this is required.

Notes 1. If increasing the number of layers in the board is difficult, bring the GND pattern out to the surface layer and make as many via connections between the GND patterns in different layers as are possible.
2. Take special care in placement in terms of the regulator, since this operates at particularly high temperatures.

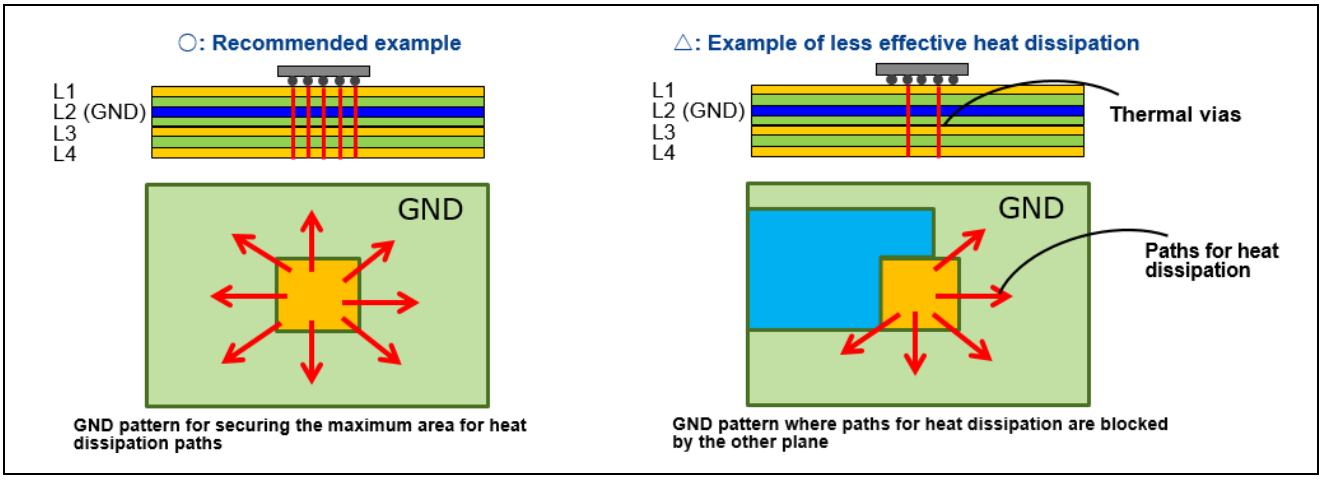
8.2.1 Measures for Heat Release in Designing the Board

(1) Thermal Vias

Placing as many vias to the power supply and GND areas as possible below the center of the package increases the number of paths for the flow of heat in the z direction. We recommend placing one via for each power supply and GND ball.

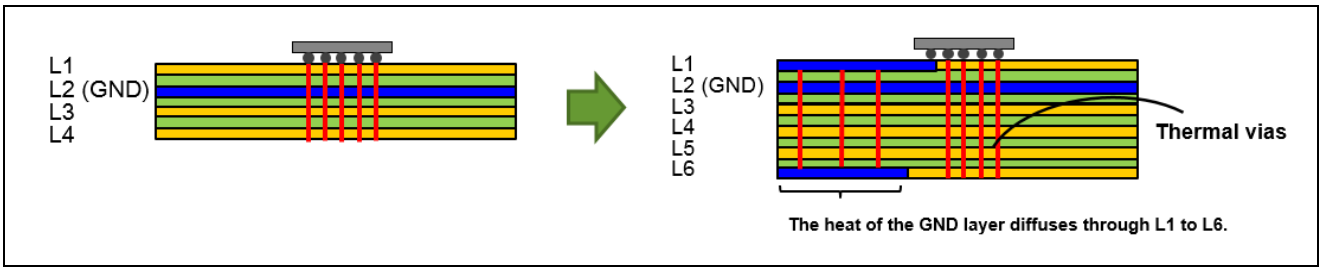
(2) Power Supply and GND Planes

Secure as large an area as is possible for the power supply and GND planes of the board. This enables the broad diffusion of heat through vias in the direction of the surface plane. Dividing paths for heat dissipation from plane to plane decreases the effectiveness of heat dissipation. Therefore, place the GND pattern in such a way that the paths are divided as little as is possible. We recommend L2 for the GND layer.



(3) Increase the Number of Board Layers, and Bring the GND Pattern out to the Surface Layer

Increasing the number of Cu wiring layers in the printed circuit board expands the area for hear release. Where possible, place areas of the GND pattern on the surface layer and connect them to the main GND pattern via thermal vias. This further improves heat dissipation. The board should have at least four layers, and we recommend six.



(4) Appropriate Placement of Components

Placing heat-generating components close to this device affects its heat efficiency, so do not place heat-generating components in its vicinity.

Caution. For example, placing a regulator with high power consumption in the vicinity of this device has the effect of significantly reducing its heat dissipation.

(5) Residual Copper Ratio of Cu Layers

Increasing the residual copper ratio in all layers of the board layers increases the breadth of the paths for heat transfer.

(6) Cu Thickness

Designing all Cu layers of the board to be thick increases the volume of paths for heat dissipation. Since thinner Cu layers reduce the effectiveness of heat dissipation, care is required on this point. We recommend that the power supply and GND layers be at least 35-um thick.

8.2.2 Heat Dissipation from the Periphery (Including the Casing)

(1) Incorporating a Heat Sink

Incorporating a heat sink increases the area for heat dissipation, making heat dissipation from the surface of the device more efficient.

(2) Heat Conduction to the Casing

Placing heat dissipating gel on the surface of the device and connecting this to the metal surface of the casing increases the efficiency of heat dissipation from the surface of the device.

(3) Placing a Fan in the Casing

Including a fan improves thermal conductivity through convection, which decreases the ambient temperature.

(4) Obtaining a Chimney Effect

Since heat tends to be released in the z direction, placing the board vertically leads to heat convection from the surface of the device, improving the thermal conductivity rate there.

(5) Enlarging Ventilation Holes

Larger ventilation holes accelerate the heat exchange between the air within the casing and that outside, lowering the temperature in the vicinity of the device.

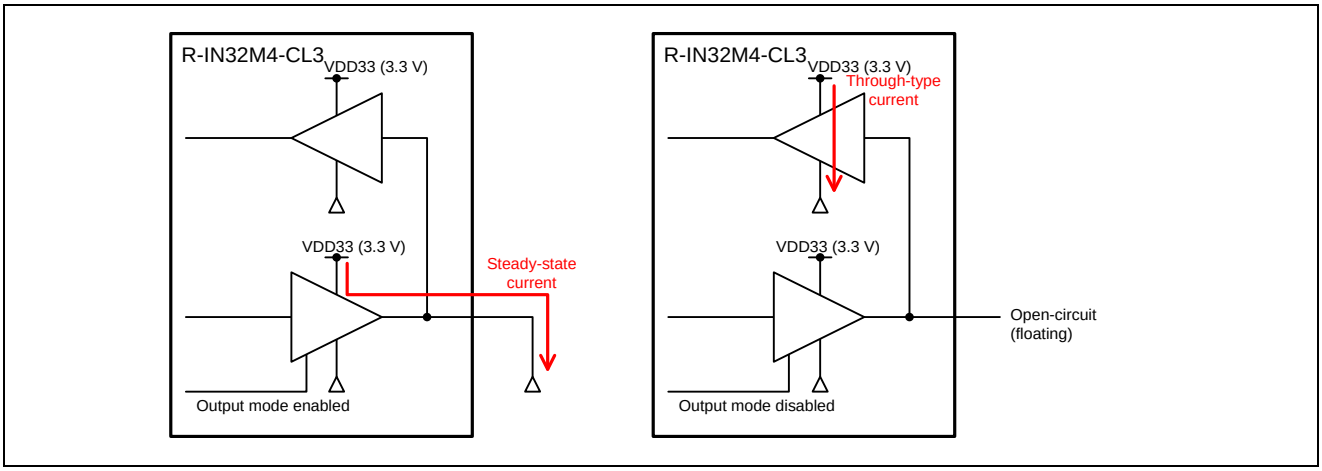
(6) Thermal Insulation by Shielding Plates

If there is a particular source of much heat within the casing, thermal insulation by using shielding plates is effective. Shielding the device from the effects of such heat sources reduces the effect of the heat on the device.

8.3 Caution

8.3.1 Handling of Unused Pins

If an unused pin is clamped to the GND or a power supply on the board, the corresponding pin must have the input attribute as a fixed setting. If it is set as an output, and the level at the point to which it is clamped is opposite that of the pin, a large steady-state current will continuously flow through the output buffer.
On the other hand, if an unused pin is open-circuit on the board, the corresponding pin can have either the output attribute or the input attribute as a fixed setting, accompanied by enabling of the pull-up or pull-down resistor. Setting a pin as an input without enabling a pull-up or pull-down resistor may lead to the pin being in a floating state and the flow of a through-type current.
Since the above factors lead to unnecessary heating, be sure to check the settings made by the software in these cases.



9. External MCU/Memory Interface Pins

This LSI is able to connect an external MCU or memory.

The connection mode is decided by the signal level of the MEMIFSEL, MEMCSEL, HIFSYNC, and ADMUXMODE pins as shown in Table 9.1.

Table 9.1 Mode Selection of External MCU/Memory Connection

Mode Setting				External Connection Mode
MEMIFSEL	MEMCSEL	HIFSYNC	ADMUXMODE	
Low	Low	—	—	External memory interface Asynchronous SRAM MEMC
	High	—	—	External memory interface Synchronous burst access MEMC
High	Low	Low	—	External MCU interface Asynchronous-SRAM supporting MCU connection mode
		High	—	External MCU interface Synchronous-SRAM supporting MCU connection mode
	High	Low	—	Setting prohibited
			—	Setting prohibited
		High	Low	External MCU interface Synchronous-burst-transfer supporting MCU connection mode (address/data separated)
			High	External MCU interface Synchronous-burst-transfer supporting MCU connection mode (address/data multiplexed)

9.1 External MCU Interface

The external MCU interface is multiplexed with the external memory interface. When the MEMIFSEL pin is set to the high level, it functions as the external MCU interface.

The external MCU interface supports the asynchronous-SRAM supporting MCU connection mode and the synchronous-SRAM supporting MCU connection mode. When the level on the HIFSYNC pin is high, it functions as a synchronous SRAM interface, and when HIFSYNC is set to low-level, it functions as an asynchronous SRAM interface (see Table 9.1, Mode Selection of External MCU/Memory Connection).

In addition, the external MCU interface supports the synchronous-burst-transfer supporting MCU connection mode of clock synchronization, allowing access to large volumes of data at high speed. This function is enabled by setting the MEMIFSEL and MEMCSEL pins to the high level.

Caution: The method of connection for each signal depends on the bus interface specifications of the MCU to be connected.
Check the specifications of the product to be connected before determining the method.

9.1.1 Asynchronous-SRAM Supporting MCU Connection Mode

The following figure shows a general connection example in asynchronous-SRAM supporting MCU interface mode, when this LSI chip is connected as a slave device to an external MCU.

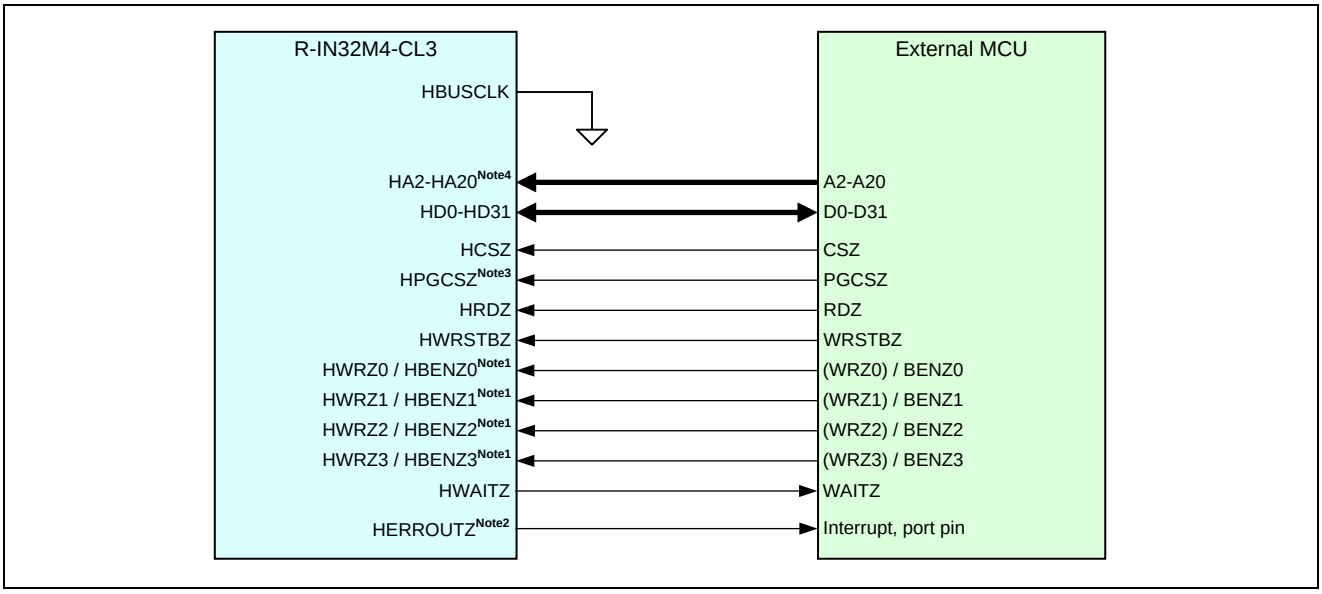


Figure 9.1 Connection Example of 32-Bit External MCU Interface (in Asynchronous-SRAM Supporting MCU Connection Mode)

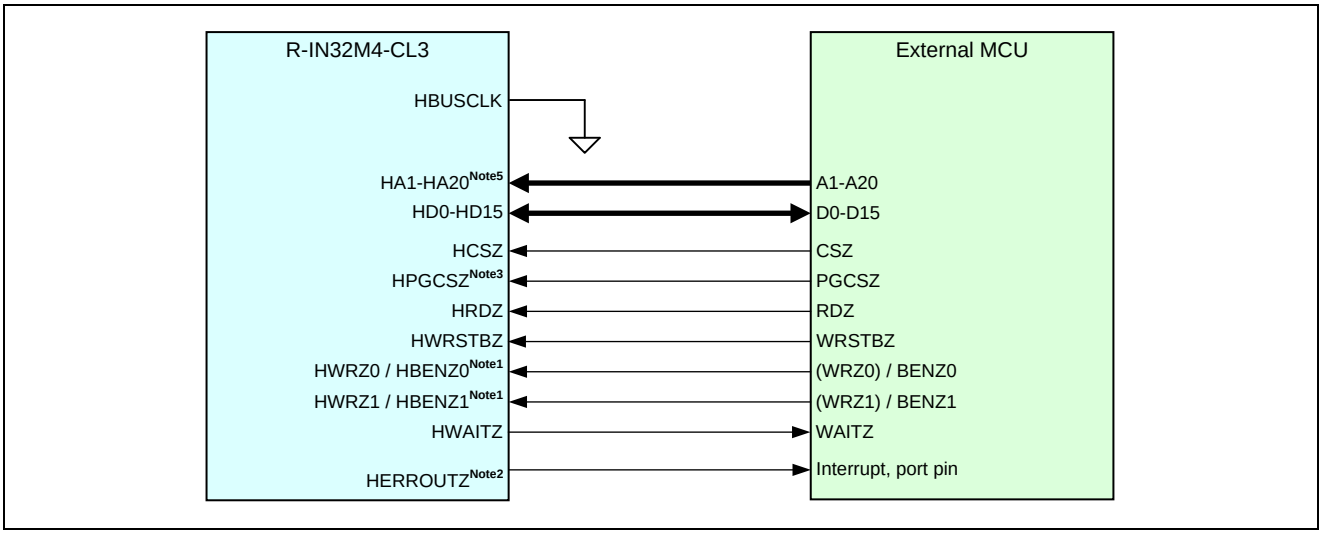


Figure 9.2 Connection Example of 16-Bit External MCU Interface (in Asynchronous-SRAM Supporting MCU Connection Mode)

Notes 1. HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are multiplexed on the same pins, and the pin functions are selected by the level on the HWRZSEL pin.

2. Connecting the HERROUTZ signal is not indispensable.
Connect it to an interrupt or general-purpose port input of the MCU to be connected, if required.

3. This is a chip-select signal supporting paged access. Connect it if required.

4. Connected the address signal for a 4-byte boundary from the destination to the HA2 pin of the R-IN32M4-CL3.

5. Connected the address signal for a 2-byte boundary from the destination to the HA1 pin of the R-IN32M4-CL3.

9.1.2 Synchronous-SRAM Supporting MCU Connection Mode

The following figure shows a general connection example in synchronous-SRAM supporting MCU interface mode, when this LSI chip is connected as a slave device to an external MCU.

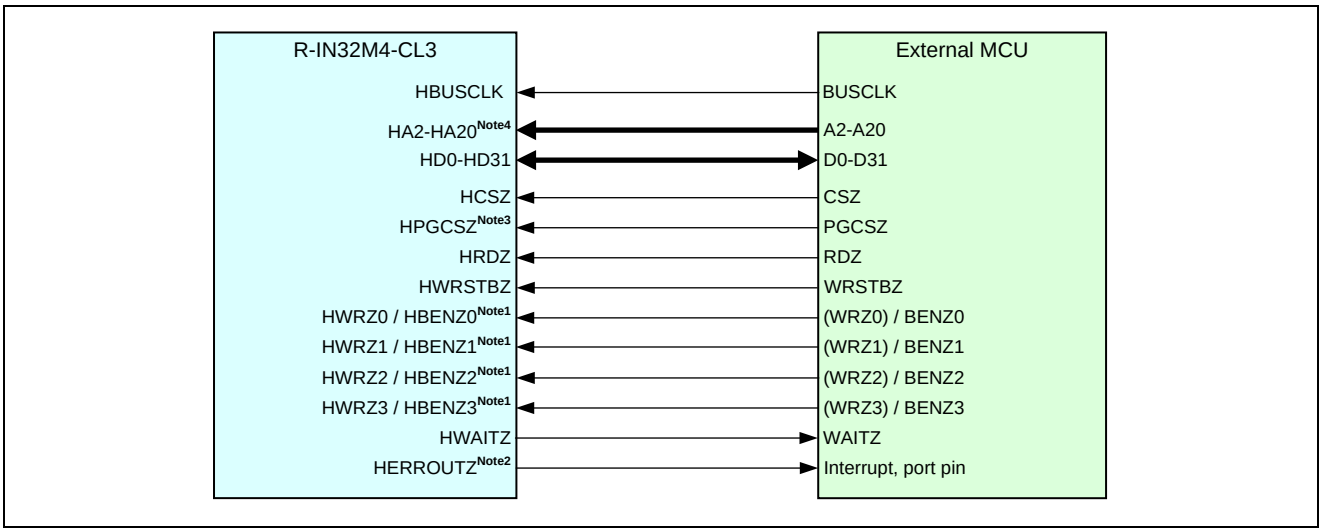


Figure 9.3 Connection Example of 32-Bit External MCU Interface (in Synchronous-SRAM Supporting MCU Connection Mode)

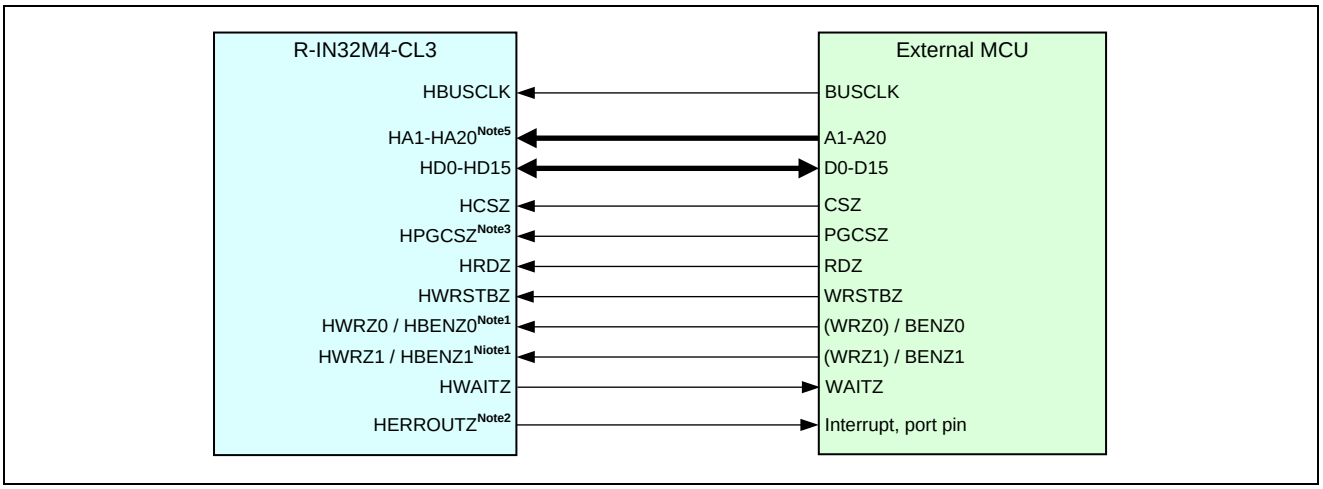


Figure 9.4 Connection Example of 16-Bit External MCU Interface (in Synchronous-SRAM Supporting MCU Connection Mode)

Notes 1. HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are multiplexed on the same pins, and the pin functions are selected by the level on the HWRZSEL pin.

2. Connecting the HERROUTZ signal is not indispensable.
Connect it to an interrupt or general-purpose port input of the MCU to be connected, if required.

3. This is a chip-select signal supporting paged access. Connect it if required.

4. Connected the address signal for a 4-byte boundary from the destination to the HA2 pin of the R-IN32M4-CL3.

5. Connected the address signal for a 2-byte boundary from the destination to the HA1 pin of the R-IN32M4-CL3.

9.1.3 Synchronous-Burst-Transfer Supporting MCU Connection Mode

The following figure shows a general connection example in synchronous-burst-transfer supporting MCU connection mode, when this LSI chip is connected as a slave device to an external MCU.

9.1.3.1 Address/Data Multiplexed Mode (ADMUXMODE = H)

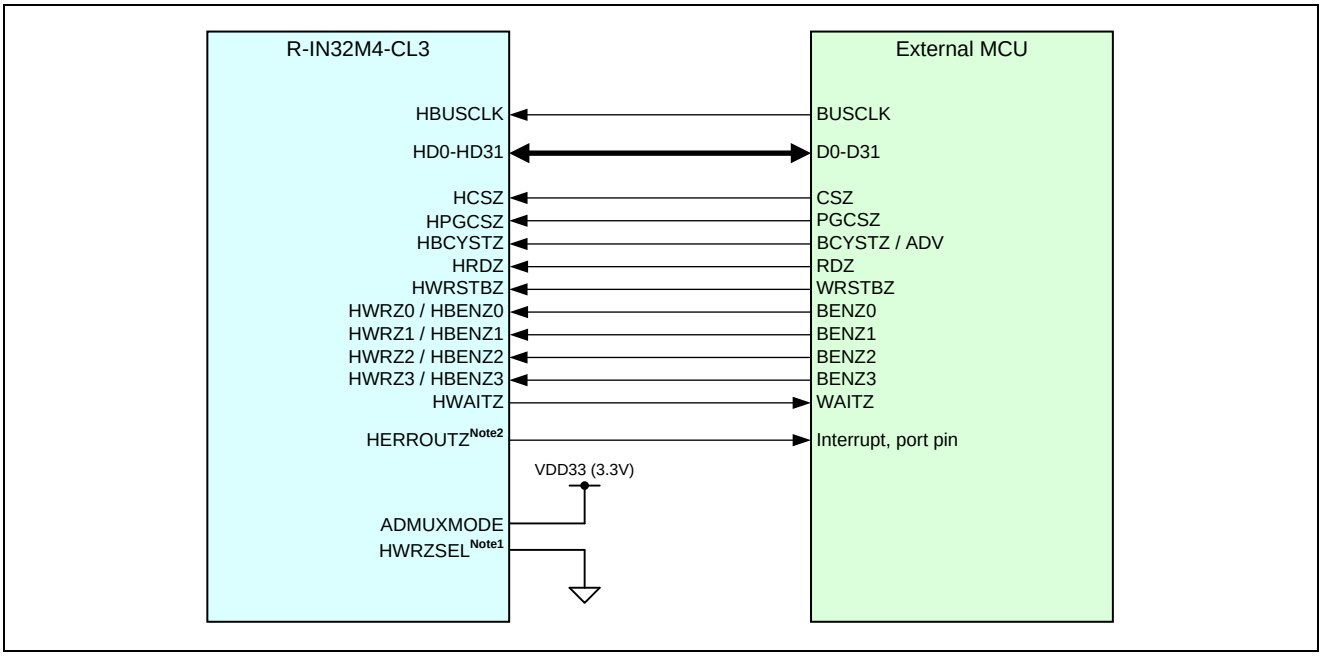


Figure 9.5 Connection Example of 32-Bit External MCU Interface

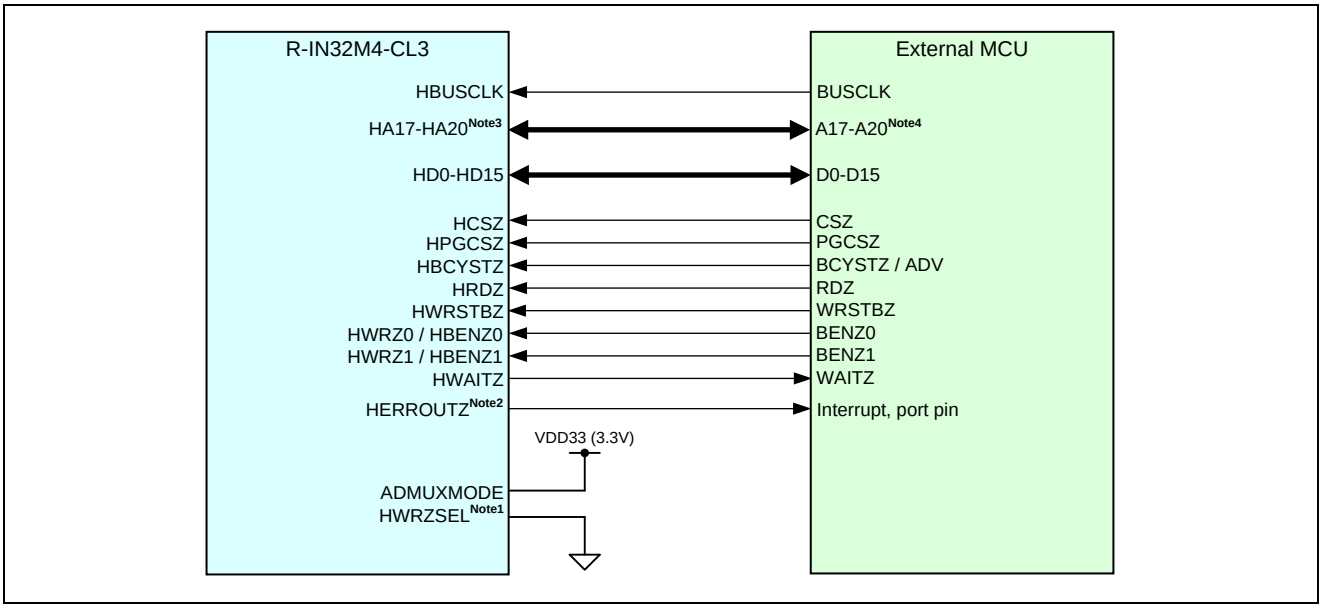


Figure 9.6 Connection Example of 16-Bit External MCU Interface

Notes 1. In this mode, drive the HWRZSEL pin low.

2. Connecting the HERROUTZ signal is not indispensable.
Connect it to an interrupt or general-purpose port input of the MCU to be connected, if required.

3. Connected the address signal for a 128-Kbyte boundary from the destination to the HA17 pin of the R-IN32M4-CL3.

4. Accessed is by byte-wise addressing.

9.1.3.2 Address/Data Separated Mode (ADMUXMODE = L)

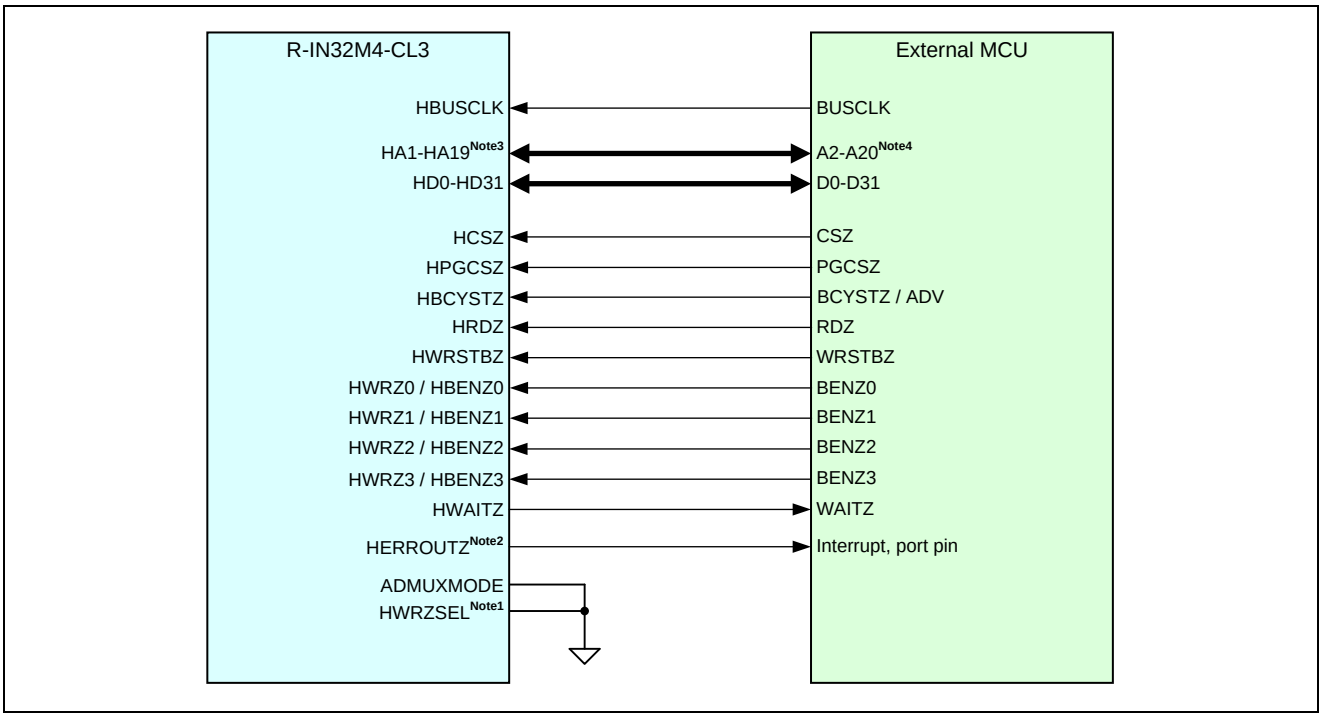


Figure 9.7 Connection Example of 32-Bit External MCU Interface

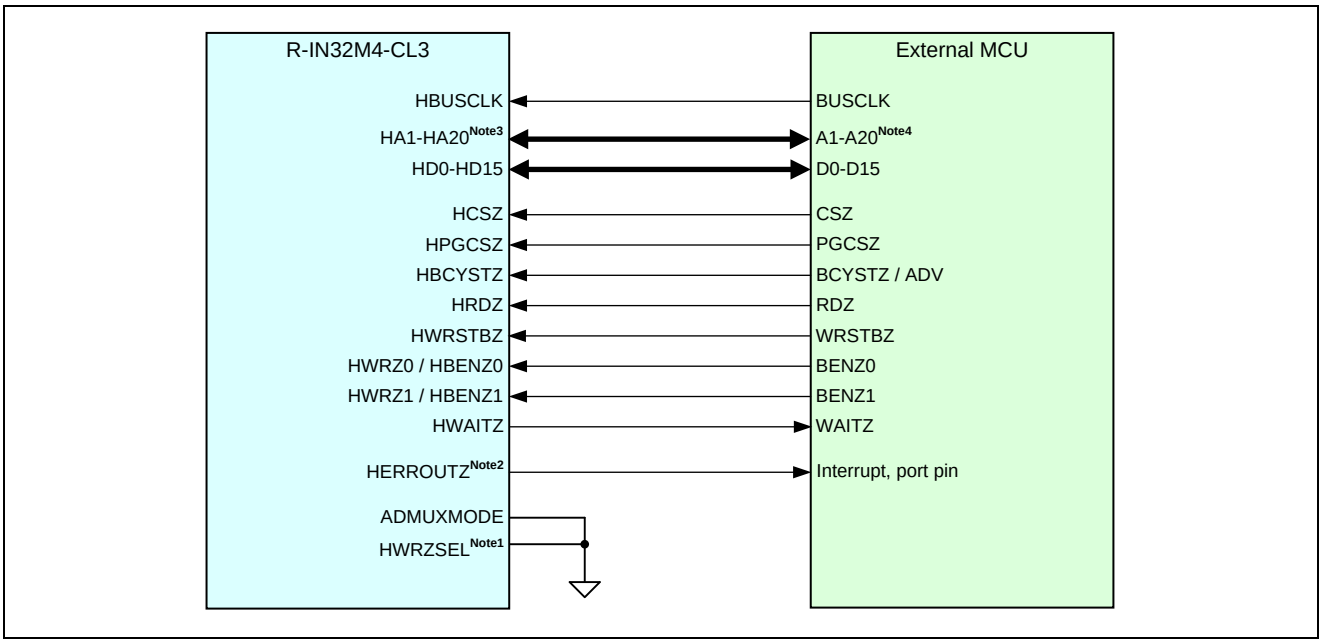


Figure 9.8 Connection Example of 16-Bit External MCU Interface

Notes 1. In this mode, drive the HWRZSEL pin low.

2. Connecting the HERROUTZ signal is not indispensable.
Connect it to an interrupt or general-purpose port input of the MCU to be connected, if required.

3. 32-bit width: Connected the address signal for a 32-bit boundary from the destination to the HA1 pin.
16-bit width: Connected the address signal for a 16-bit boundary from the destination to the HA1 pin.

4. Accessed is by byte-wise addressing.

9.2 External Memory Interface

This section describes the connection as a master device to an external memory.

The operating connection mode of the external memory interface depends on the level of the signal on the MEMCSEL pin (see Table 9.1, Mode Selection of External MCU/Memory Connection).

9.2.1 Asynchronous SRAM MEMC

The asynchronous SRAM MEMC is externally connectable to paged ROM, ROM, SRAM, or peripheral devices with an interface similar to the SRAM interface via a 16- or 32-bit bus.

The external MCU interfaces for the asynchronous SRAM MEMC and the synchronous method burst access MEMC are multiplexed with each other. When both the MEMCSEL and MEMIFSEL pins are at the low level, the asynchronous SRAM MEMC can be used.

When both the BOOT0 and BOOT1 pins are at the low level, booting up proceeds from the memory connected to CSZ0.

9.2.1.1 Connection Example with SRAM

The following figure shows an example when this LSI chip is connected to SRAM.

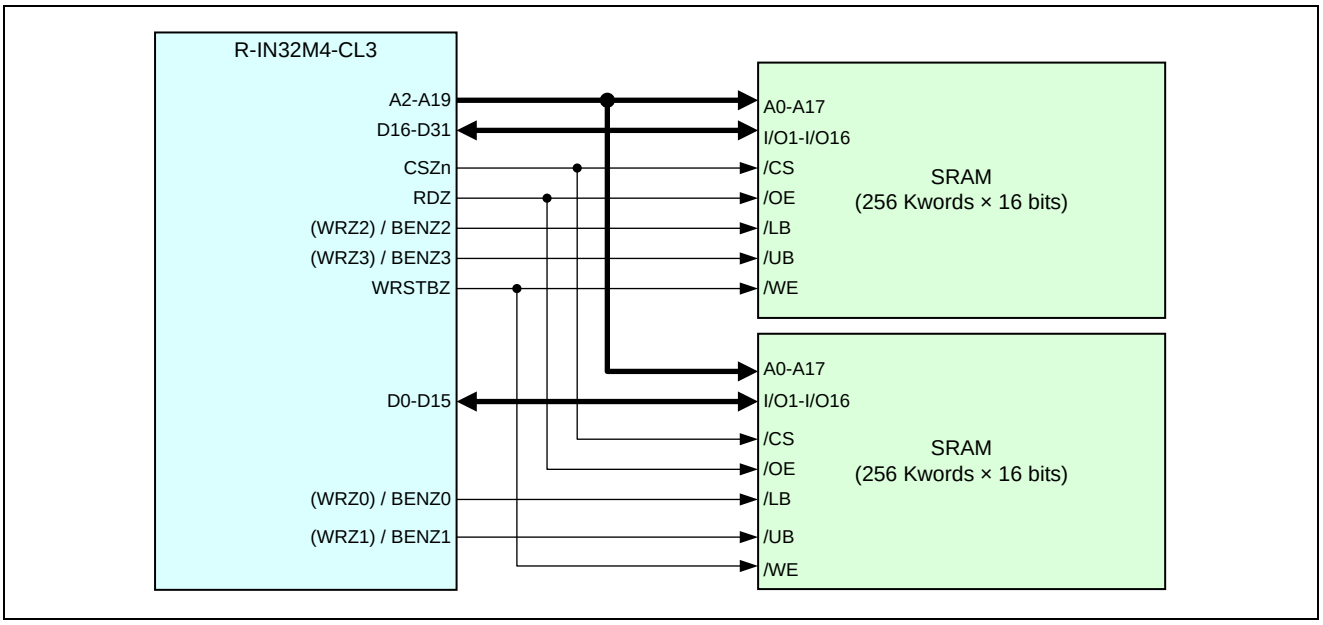


Figure 9.9 Connection Example with 32-Bit SRAM (Asynchronous SRAM MEMC)

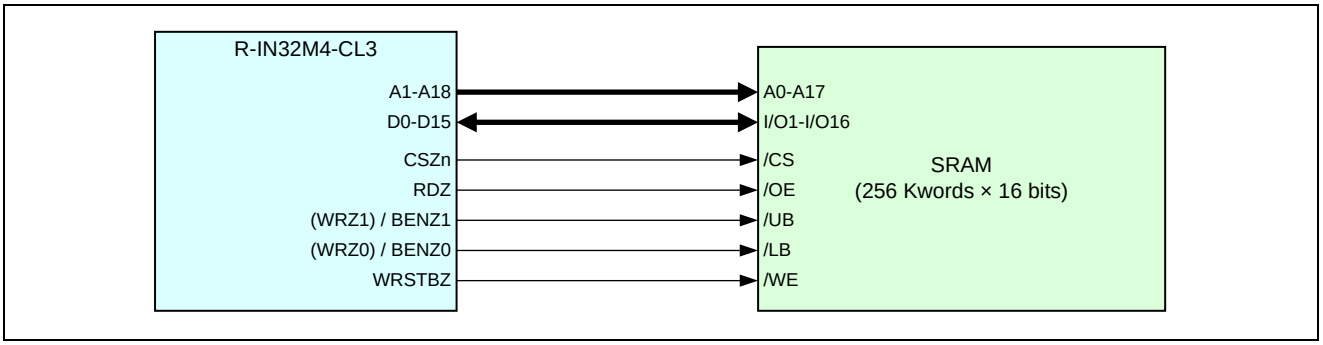


Figure 9.10 Connection Example with 16-Bit SRAM (Asynchronous SRAM MEMC)

Remark: n = 0–3

9.2.1.2 Connection Example with Paged ROM

The following figure shows an example when this LSI chip is connected to paged ROM.

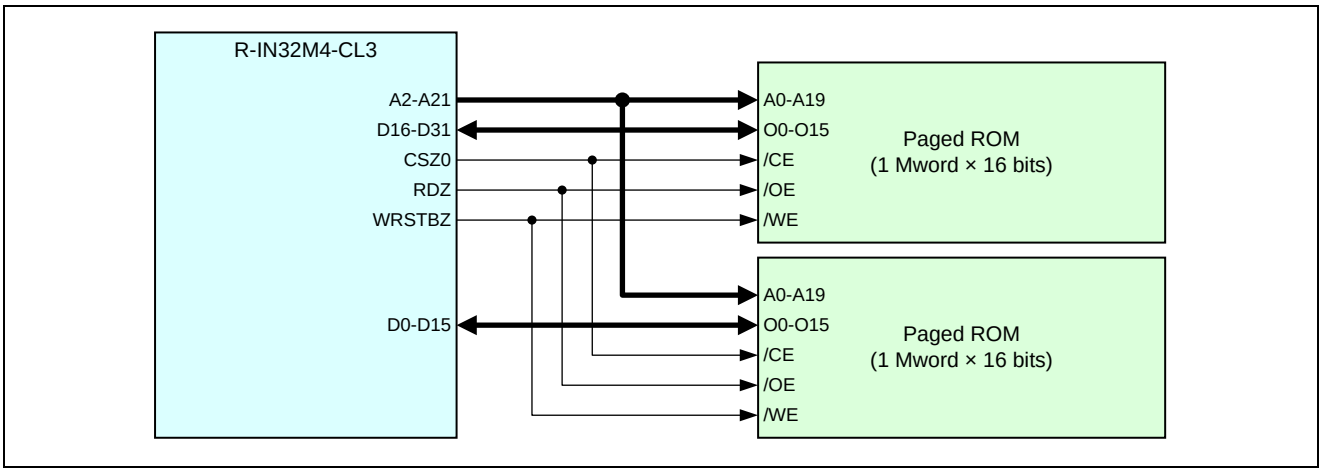


Figure 9.11 Connection Example with 32-Bit Paged ROM (Asynchronous SRAM MEMC)

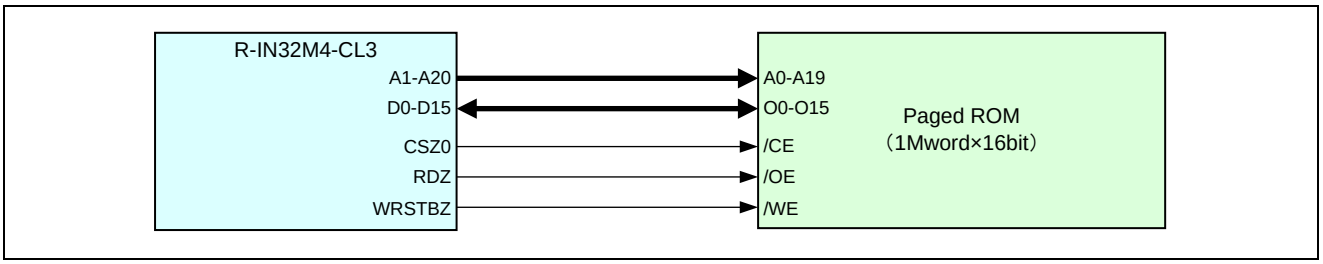


Figure 9.12 Connection Example with 16-Bit Paged ROM (Asynchronous SRAM MEMC)

Caution: The on-page mode of paged ROM can only be used when CSZ0 is connected.

9.2.2 Synchronous Burst Access MEMC

The synchronous burst access MEMC is externally connectable to paged ROM, ROM, SRAM, PSRAM, NOR-flash memory, or peripheral devices with an interface similar to the SRAM interface via a 16- or 32-bit bus.

In addition, setting the ADMUXMODE pin to the high level enables multiplexing of the address and data signals.

The external MCU interfaces for the synchronous method burst access MEMC and the asynchronous SRAM MEMC are multiplexed with each other. When the MEMCSEL and MEMIFSEL pins are set to high level and low level respectively, the synchronous burst access MEMC can be used.

When both the BOOT0 and BOOT1 pins are at the low level, booting up proceeds from the memory connected to CSZ0.

9.2.2.1 Connection Example with SRAM

The following figure shows an example when this LSI chip is connected to SRAM.

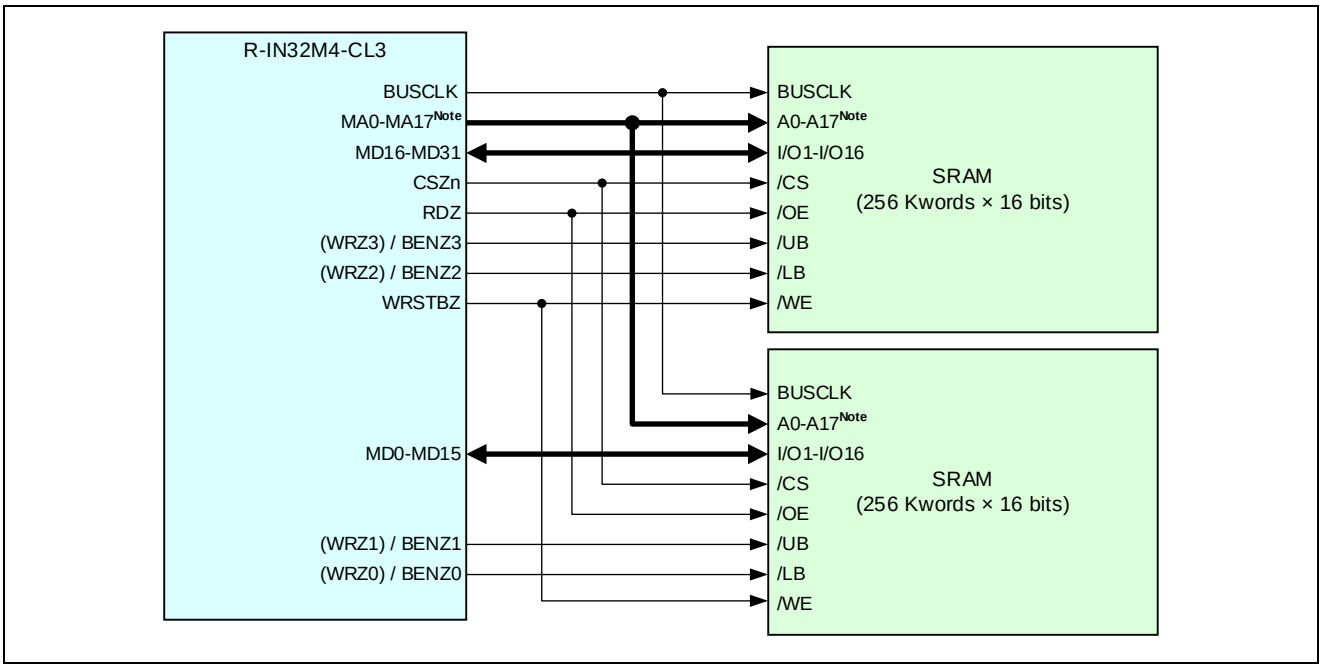


Figure 9.13 Connection Example with 32-Bit SRAM (Synchronous Burst Access MEMC)

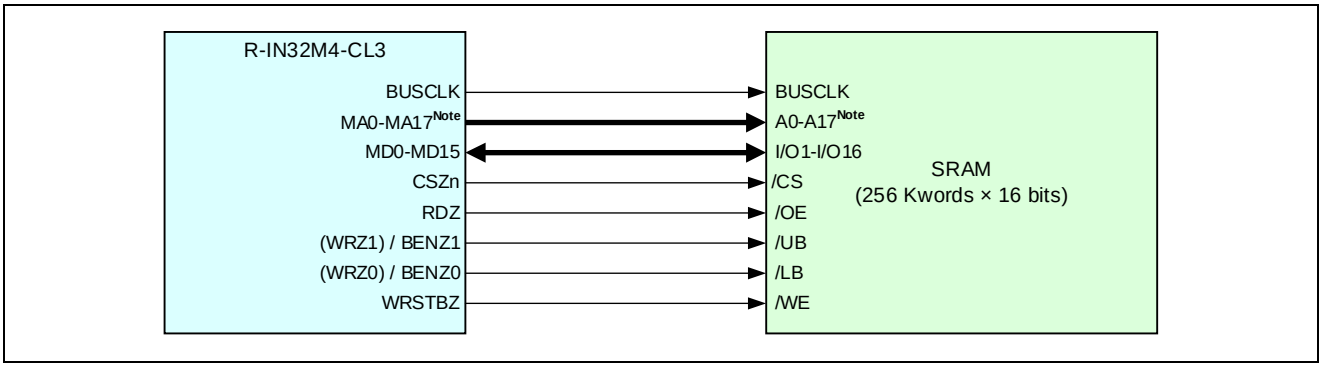


Figure 9.14 Connection Example with 16-Bit SRAM (Synchronous Burst Access MEMC)

Remark: n = 0–3

Note: When the address/data multiplexing feature is enabled (the ADMUXMODE pin is at the high level), separate connection of the address bus is not required.

9.2.2.2 Connection Example with Paged ROM

The following figure shows an example when this LSI chip is connected to paged ROM.

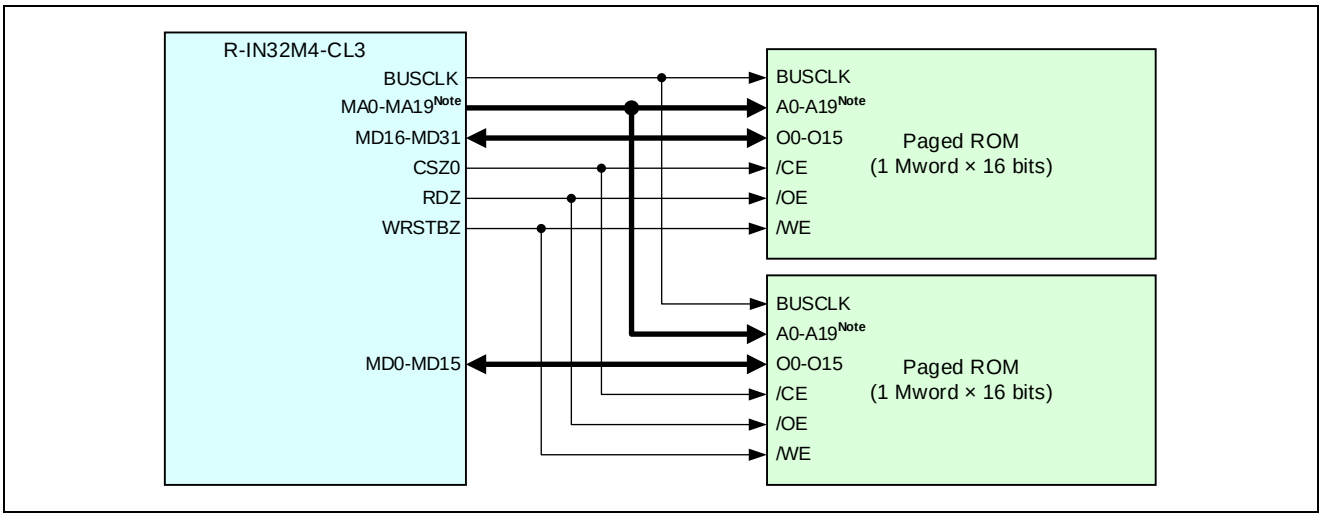


Figure 9.15 Connection Example with 32-Bit Paged ROM (Synchronous Burst Access MEMC)

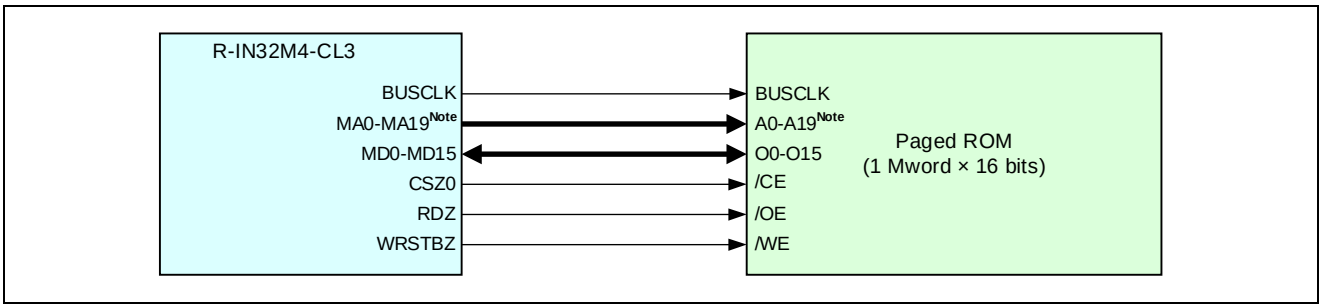


Figure 9.16 Connection Example with 16-Bit Paged ROM (Synchronous Burst Access MEMC)

Caution: The on-page mode of paged ROM can only be used when CSZ0 is connected.

Note: When the address/data multiplexing feature is enabled (the ADMUXMODE pin is at the high level), separate connection of the address bus is not required.

10. Serial Flash ROM Connection Pins

This LSI chip has a memory controller to connect the serial flash ROM that supports the SPI compatible interface.

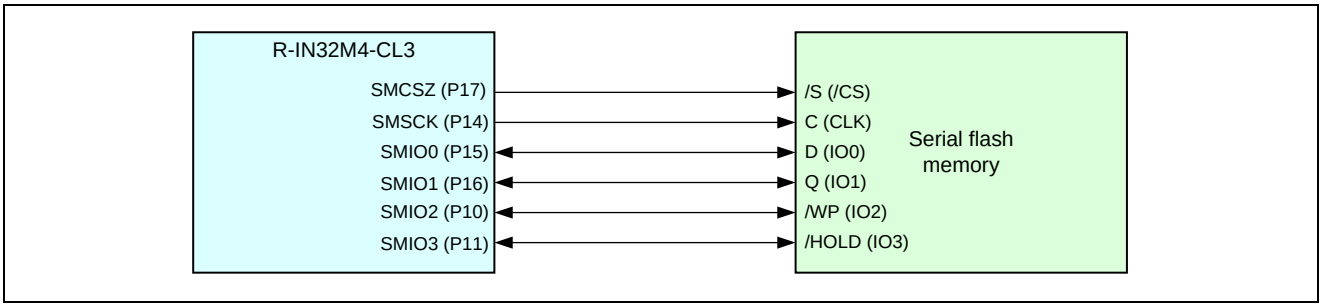


Figure 10.1 Connection Example with Serial Flash ROM

11. Asynchronous Serial Interface J Connection Pins

The following figure shows a connection example between the R-IN32M4-CL3 and the asynchronous serial interface J (UARTJ) device.

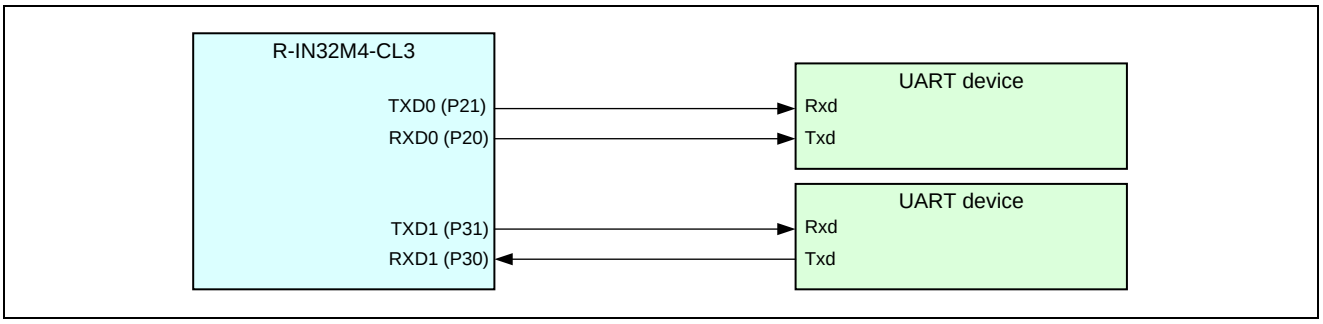


Figure 11.1 Connection Example between R-IN32M4-CL3 and UART Device

12. I²C Connection Pins

Figure 12.1 shows a connection example between the R-IN32M4-CL3 and the I²C slave device.

Since the serial clock line and serial data line are N-channel open drain outputs, an external pull-up resistor is required.

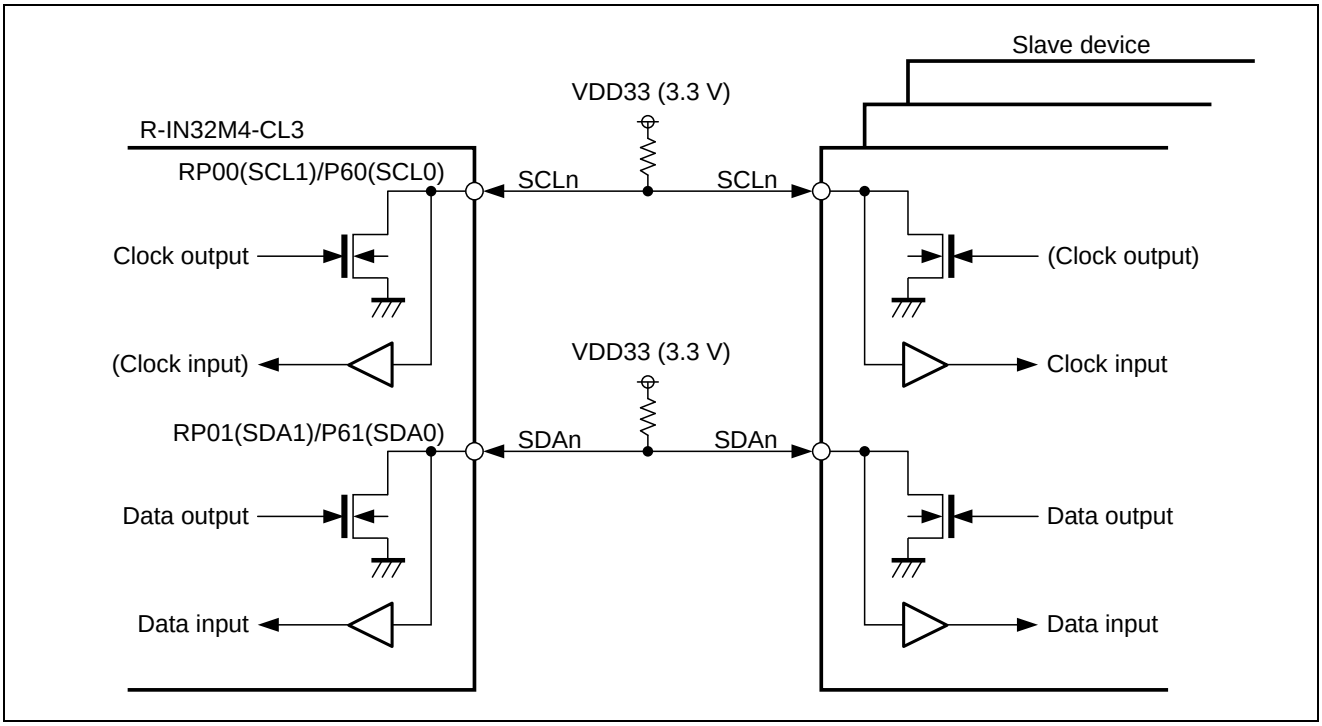


Figure 12.1 Connection Example between R-IN32M4-CL3 and I²C Slave Device

Remark: n = 0–3

13. CAN Pins

The following figure shows a connection example between the R-IN32M4-CL3 and the CAN transceiver.

The CAN transceiver is used to connect the CAN bus.

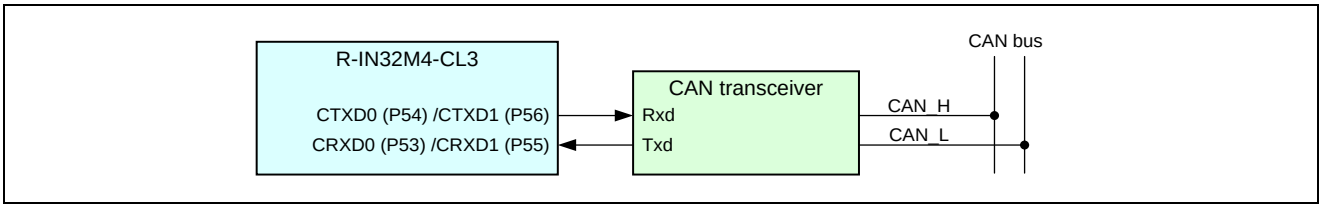


Figure 13.1 Connection Example between R-IN32M4-CL3 and CAN Transceiver

14. CSIH Pins

Examples of connections of the R-IN32M4-CL3 with a CSI master and slave are given below.

14.1 One Master and One Slave

The following figure illustrates the connections between one master and one slave.

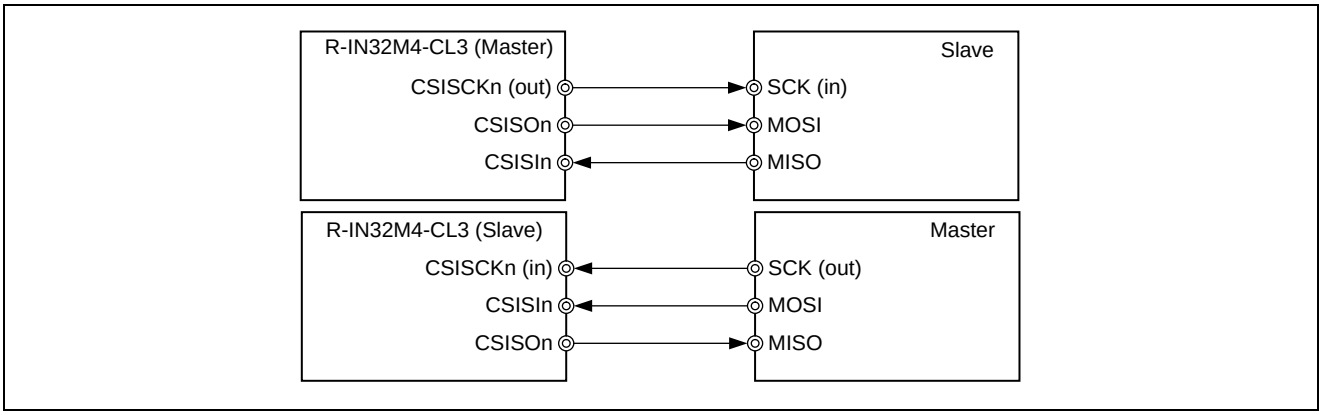


Figure 14.1 Direct Master/Slave Connection

Remark: n = 0, 1

14.2 One Master and Two Slaves

The following figure illustrates the connections between an R-IN32M4-CL3 as a master and two slaves.
In this example, the R-IN32M4-CL3 supplies one chip select (CS) signal to each of the slaves. This signal is connected to the slave select input (SSI) of the slave.

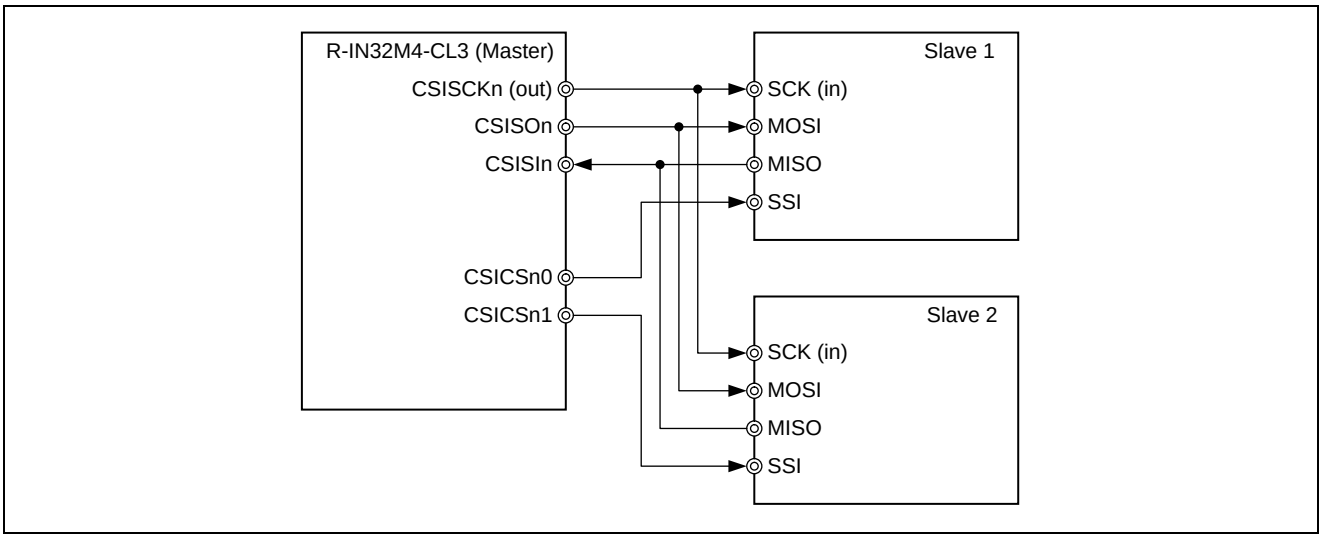


Figure 14.2 Connection between One Master and Two Slaves

Remark: n = 0, 1

15. JTAG/Trace Pins

The following figures show examples when this LSI chip is connected to the ICE (in-circuit emulator).
As long as nRESET is input to RESETZ, nRESET is not required to input to HOTRESETZ.

RESRTZ resets the entire LSI, but the internal PLL is not reset in the case of only HOTRESETZ. Please use it to meet your needs. In addition, nRESET should not be connect to PONRZ.

They are examples when connected to the 20-pin half-pitch connecter or 20-pin full-pitch connecter of standard.

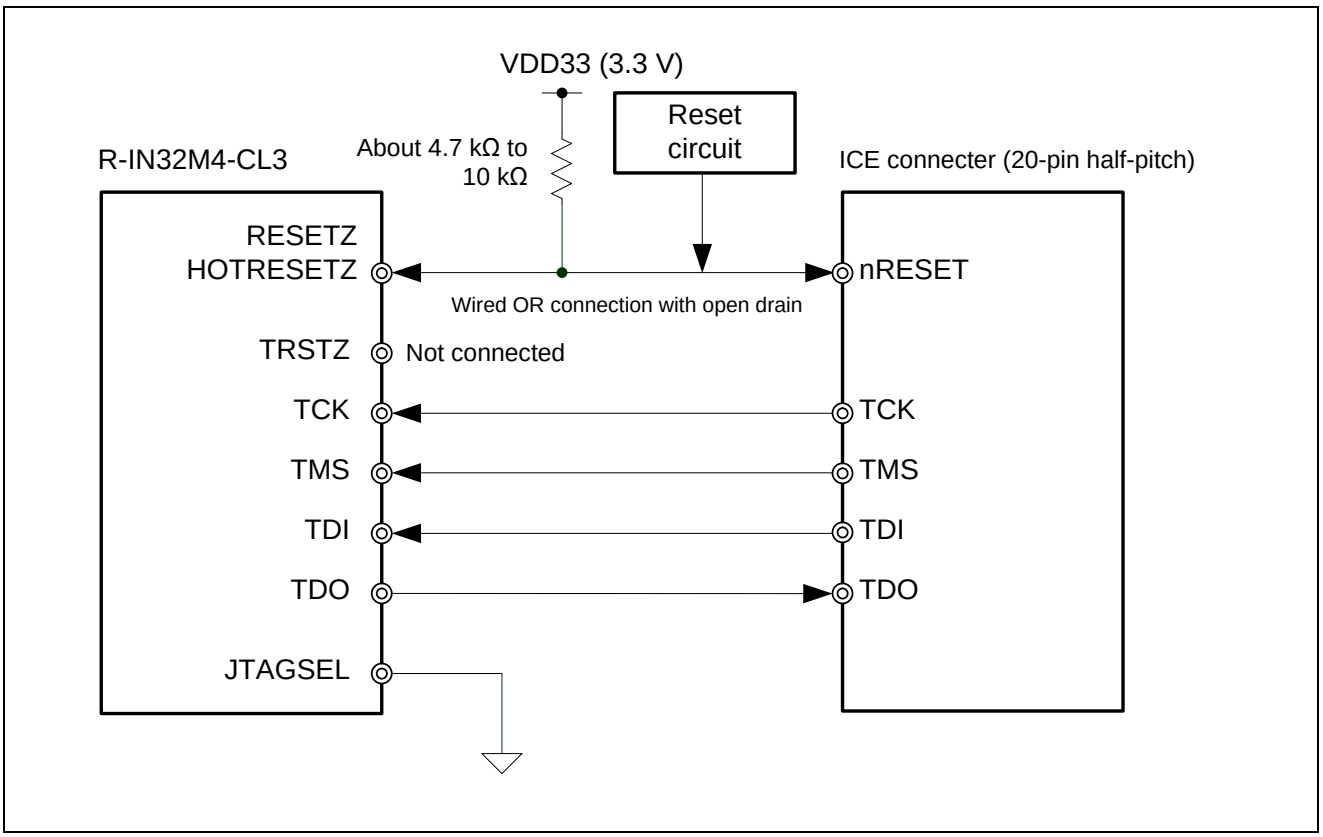


Figure 15.1 Connection Example of JTAG Interface (20-Pin Half-Pitch without Trace)

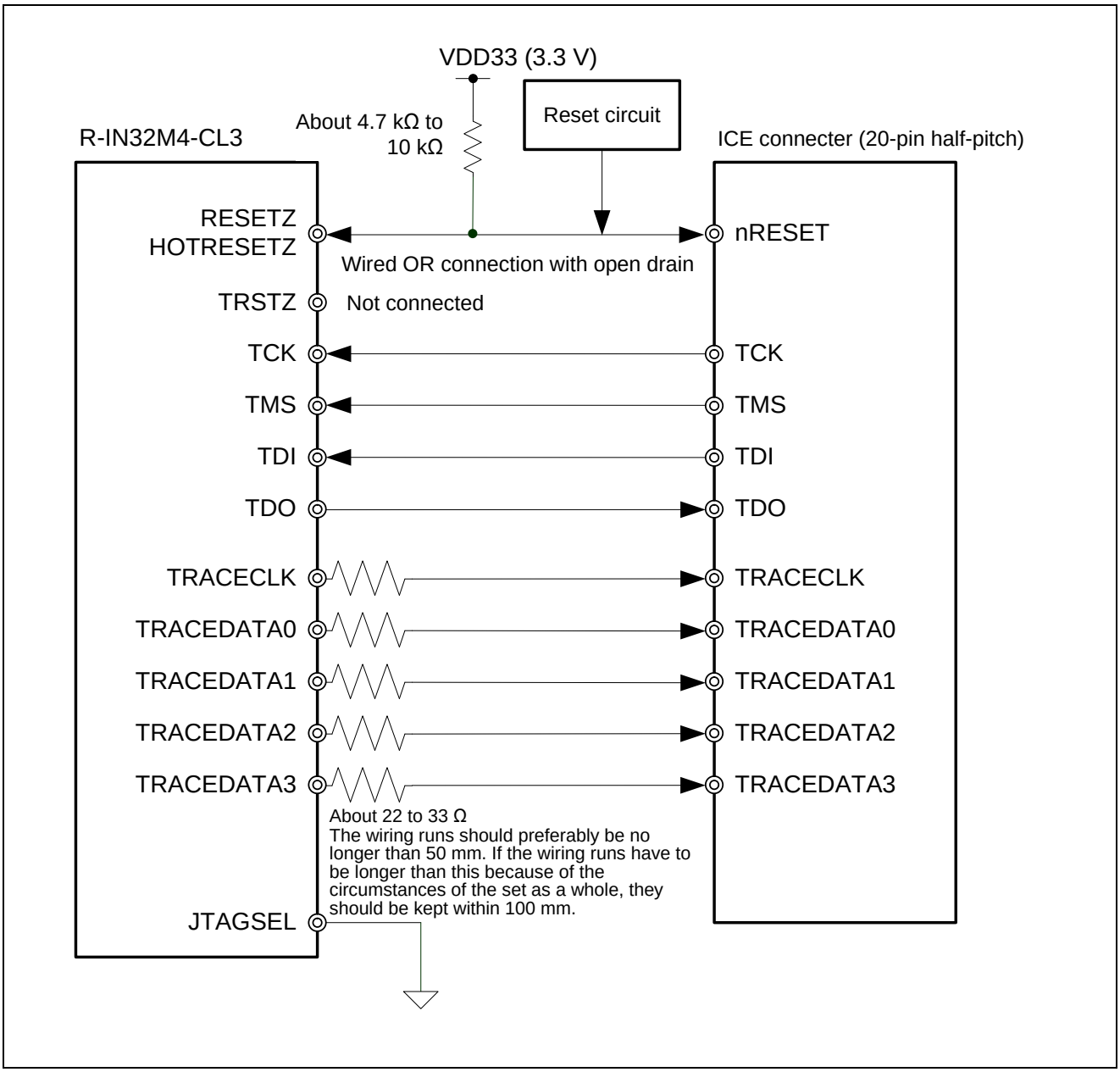


Figure 15.2 Connection Example of JTAG Interface (20-Pin Half-Pitch with Trace)

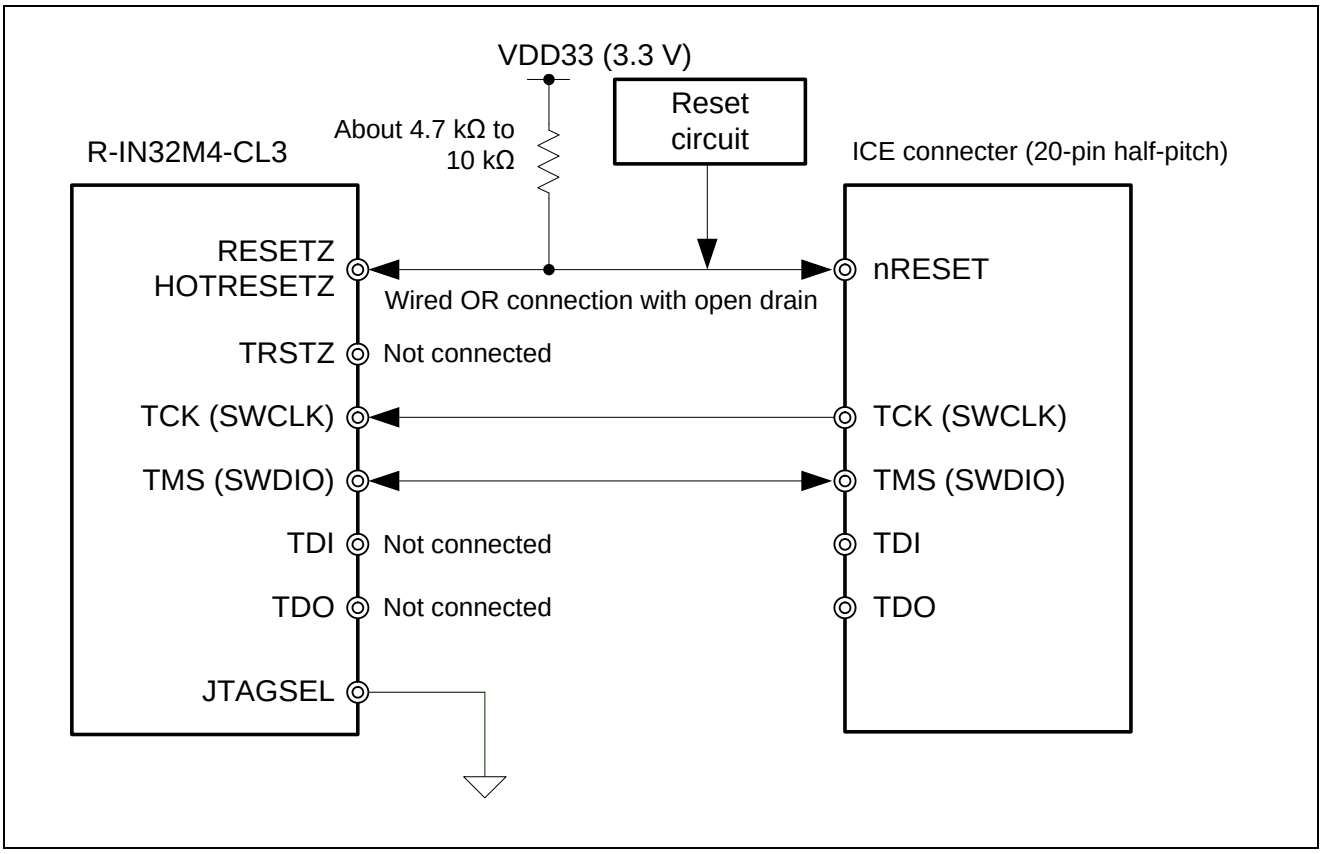


Figure 15.3 Connection Example of SWD Interface (20-Pin Half-Pitch without Trace)

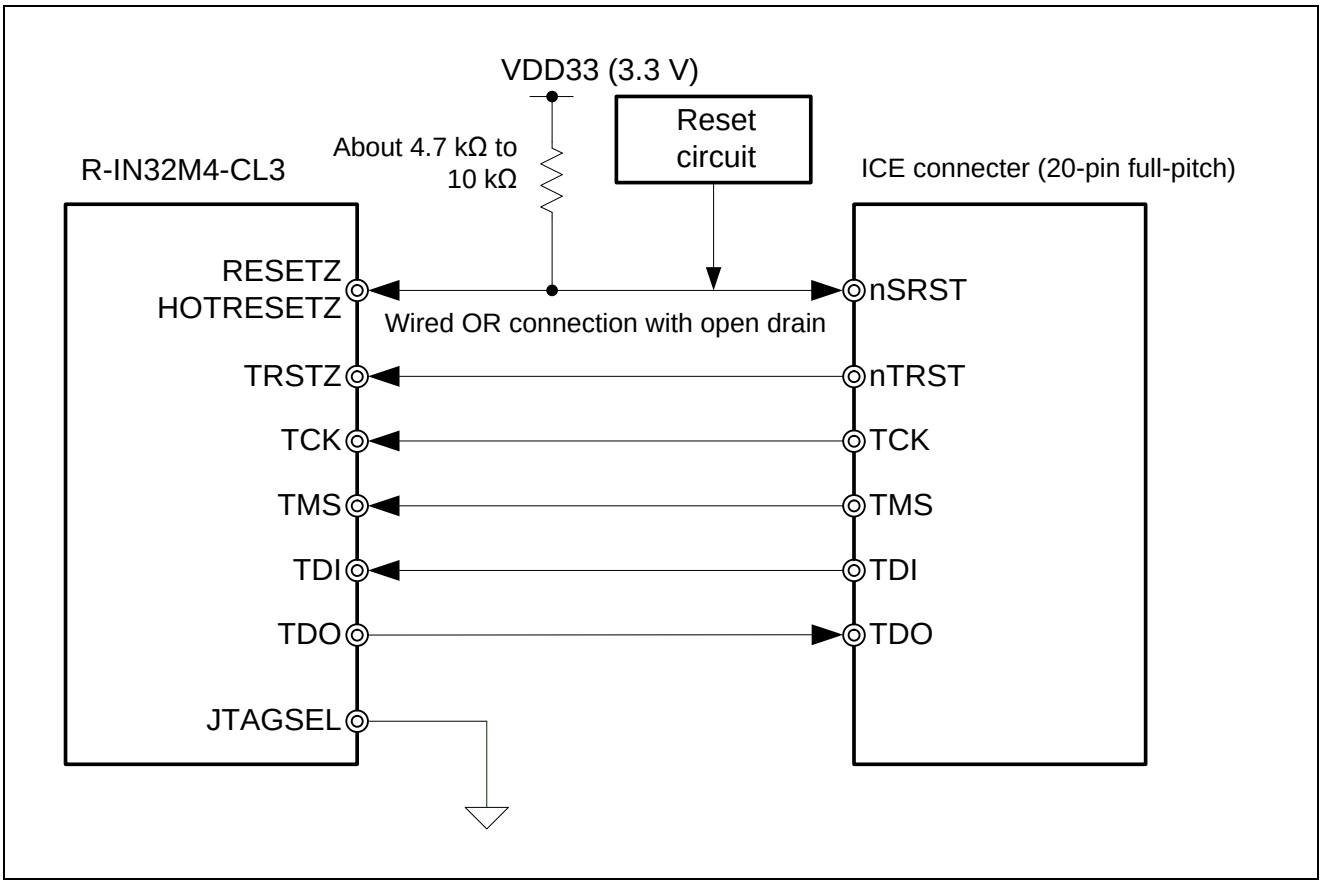


Figure 15.4 Connection Example of JTAG Interface (20-Pin Full-Pitch)

16. Implementation Conditions

The following figures show implementation conditions of the R-IN32M4-CL3.

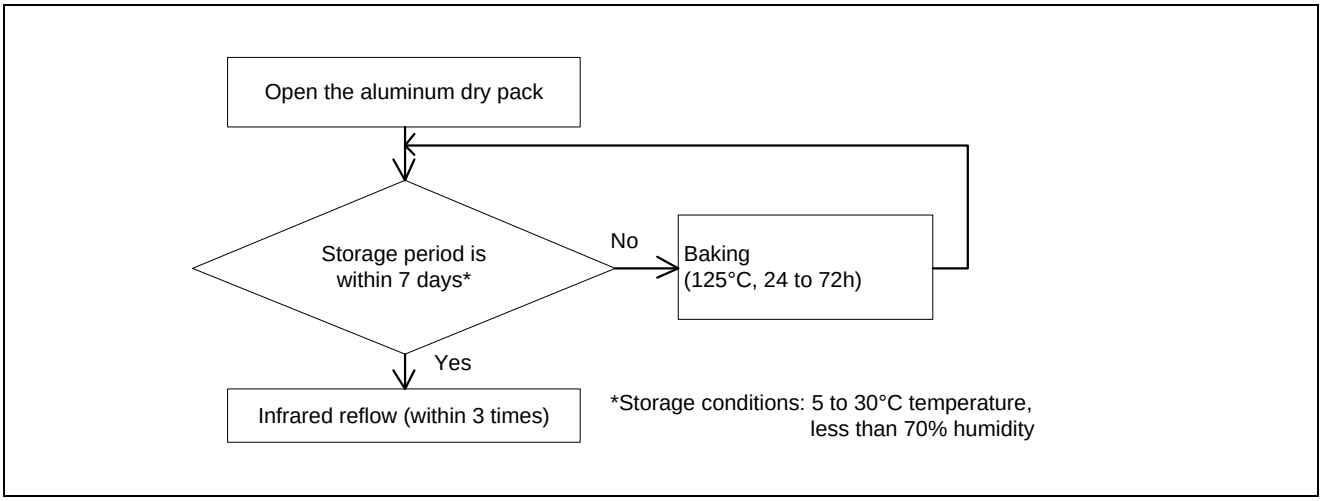


Figure 16.1 Implementation Flow

- Maximum temperature (package surface temperature): 250°C or below
- Time of maximum temperature: 30 s or less
- Time over which the temperature is 217°C or more: Within 150 s
- Time to reach preheating temperature (150 to 200°C) : 60 to 120 s
- Maximum number of times to reflow: 3 times
- Safe-keeping restriction period after opening the dray pack: Within 7 days

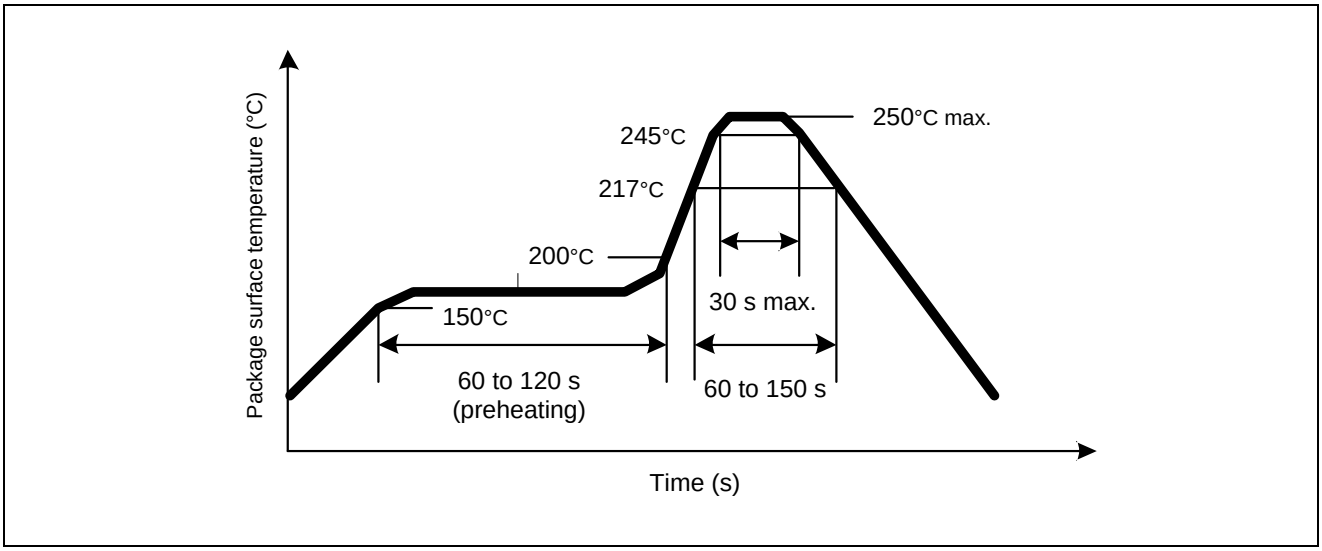
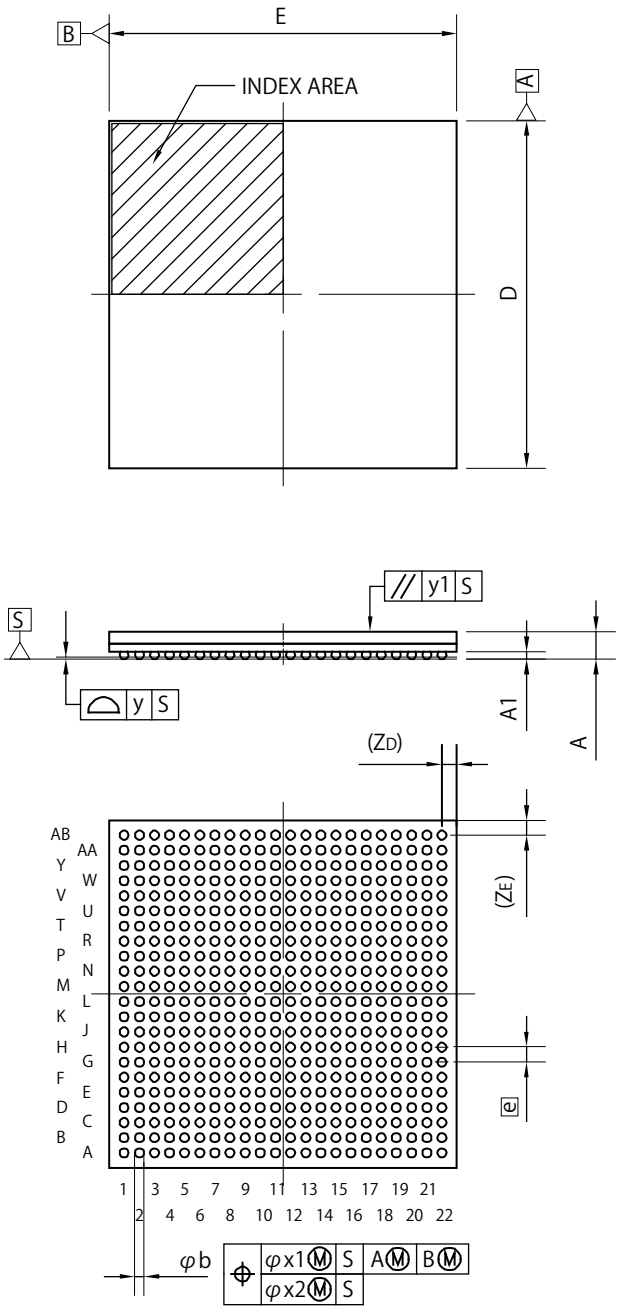


Figure 16.2 Infrared Reflow Temperature Profile

17. Package Information

The following figures show the package information of R-IN32M4-CL3.

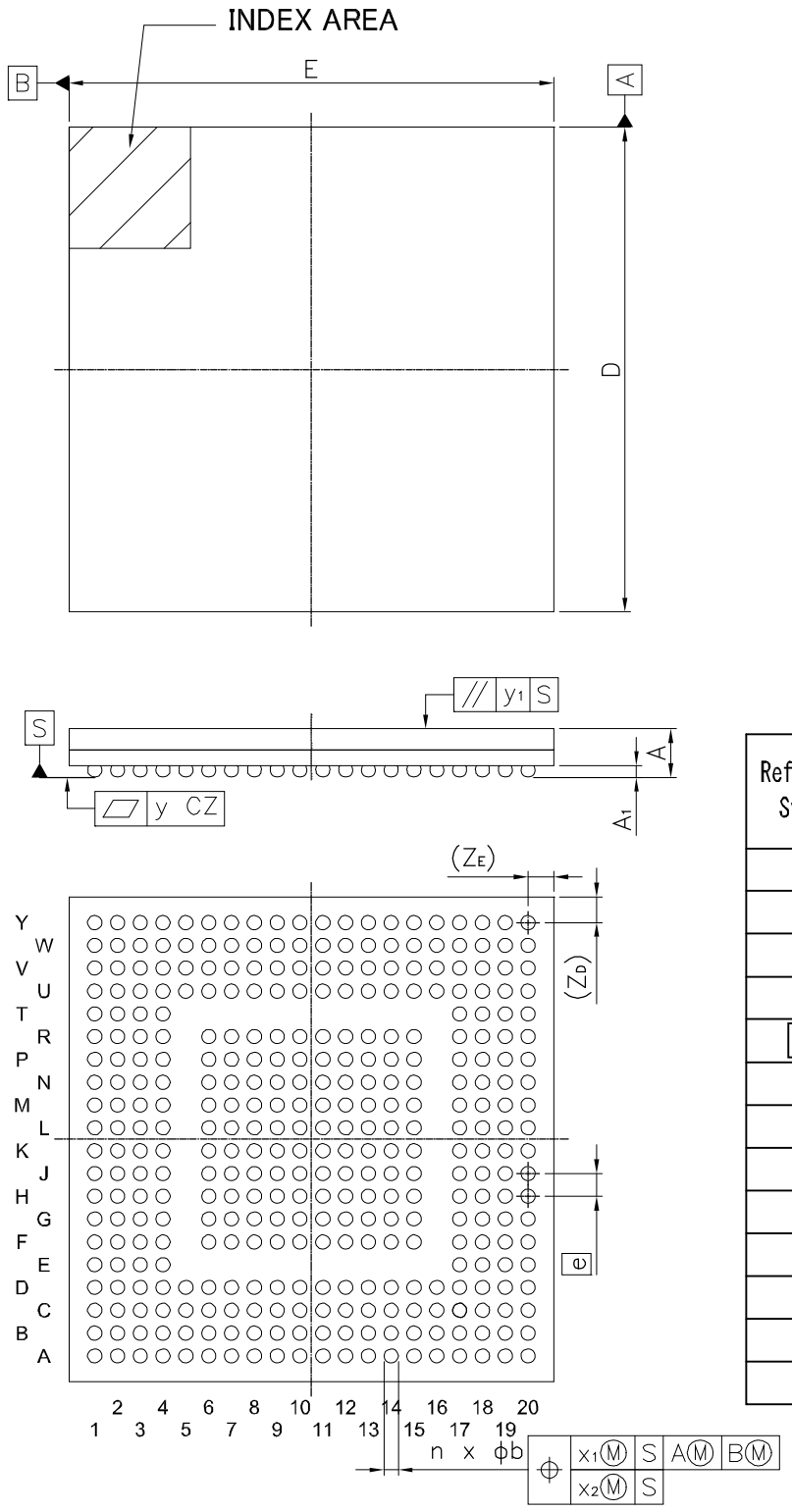
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-BGA484-23x23-1.00	PRBG0484FC-A	1.93



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	22.85	23.00	23.15
E	22.85	23.00	23.15
A	—	—	2.03
A1	0.40	0.50	0.60
e	—	1.00	—
b	0.50	0.60	0.70
x1	—	—	0.25
x2	—	—	0.10
y	—	—	0.15
y1	—	—	0.35
n	—	484	—
Z_D	—	1.00	—
Z_E	—	1.00	—

Figure 17.1 Package Information (23 mm Square BGA Package)

JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-FBGA356-17×17-0.80	PRBG0356GA-A	1.03



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	16.90	17.00	17.10
E	16.90	17.00	17.10
A	—	—	2.00
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
X_1	—	—	0.15
X_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	356	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure 17.2 Package Information (17 mm Square BGA Package)

18. Mount Pad Information

The following figures show the mount pad information of the R-IN32M4-CL3.

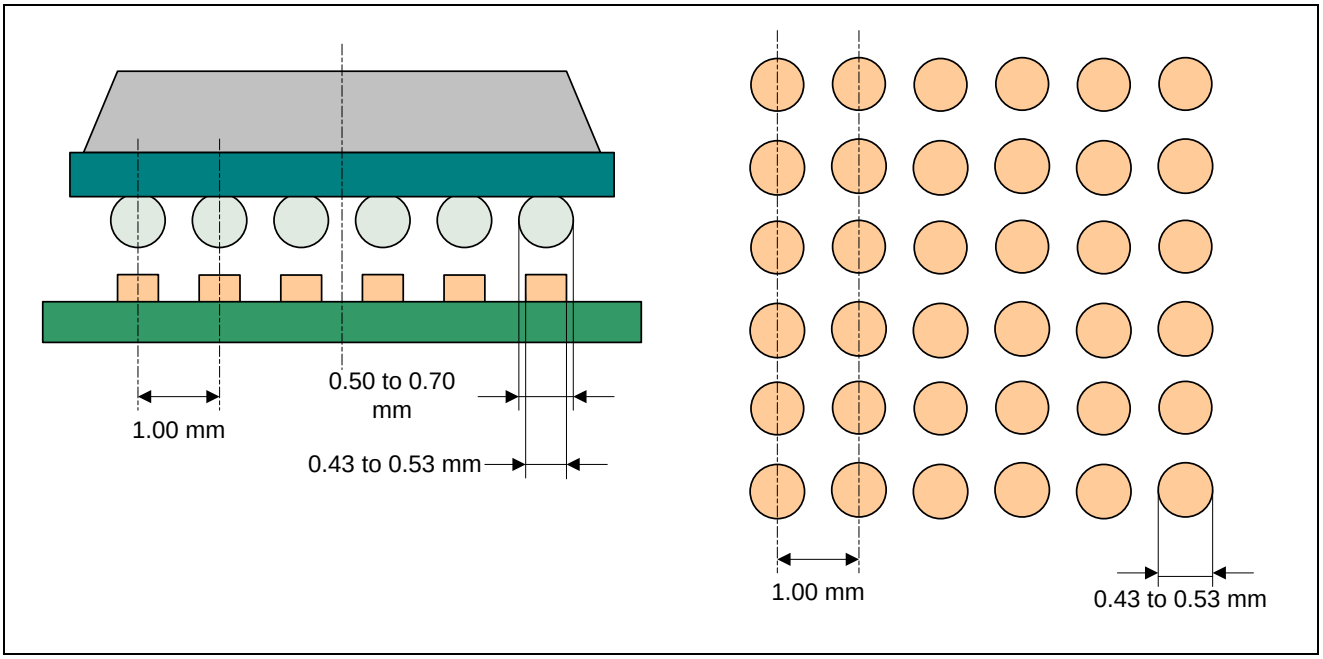


Figure 18.1 Mount Pad Sizes (23 mm Square BGA Package)

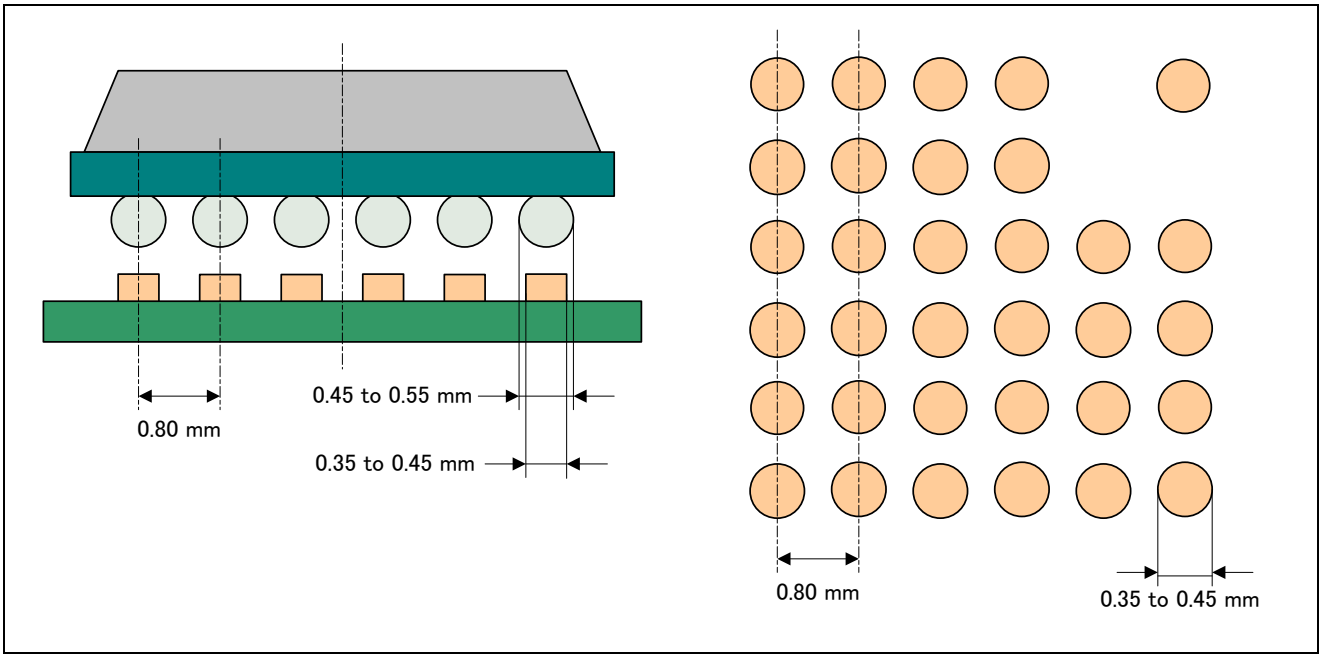


Figure 18.2 Mount Pad Sizes (17 mm Square BGA Package)

19. BSCAN Information

The R-IN32M4-CL3 provides the BSDL file.

Caution: If the other device is connected to an input pin without the pin being pulled up or down, clamp the level on the board or set the logic in the other device.
Placing the 3st pin in the Hi-Z state creates a possibility of a floating current flowing.

19.1 BSCAN Operating Conditions

Fix the level of the pins as follows.

- JTAGSEL: Fixed to the high level
- TMODE0: Fixed to the low level
- TMODE1: Fixed to the low level
- TMODE2: Fixed to the low level

19.2 Maximum Operating Frequency of TCK

The maximum operating frequency of TCK is 10 MHz.

19.3 IDCODE

IDCODE is as follows.

IDCODE 0x082C7447	
<breakdown>	
Version	0000
Part number	1000 0011 1110 0000
Manufacturer number : Renesas Electronics	0100 0100 011
Fixed code	1

19.4 BSCAN Non-Supported Pins

The following pins do not support BSCAN.

Table 19.1 List of BSCAN Non-Supported Pins

R-IN32M4-CL3
XT1, XT2, PONRZ, JTAGSEL, CTRSTBYB, TMODE0–TMODE2, TMS, TDI, TDO, TRSTZ, TCK, P[0:1]_D[3:0]P/N, REF_FILT, REF_REXT, TANA_[1:0], REG_FB, REG_OUT

19.5 How to Get BSDL

With regard to obtain the BSDL file, please contact a Renesas Sales Representative or Distributor in your area.

20. IBIS Information

For IBIS information, please contact a Renesas Sales Representative or Distributor in your area.

21. Marking Information

The following figures show the marking information of R-IN32M4-CL3.

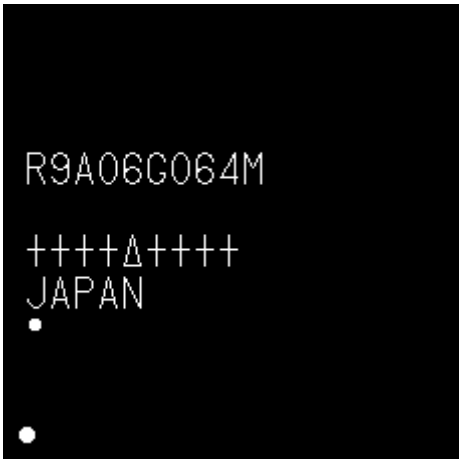


Figure 21.1 R-IN32M4-CL3 Marking Information (23 mm Square BGA Package)

Figure 21.2 R-IN32M4-CL3 Marking Information (17 mm Square BGA Package)

22. Countermeasure for Noise

This section describes a countermeasure for noise in circuits that include an R-IN32M4-CL3.

22.1 Stopping Clock Output

If the BUSCLK pin is not in use, output on the pin from the R-IN32M4-CL3 can be stopped. See Section 4.2.2 “Clock Control Registers (CLKGTD0, CLKGTD1, CLKGTD2)” in the “R-IN32M4-CL3 User’s Manual: Hardware edition” regarding control of the GCBCLK bit in the CLKGTD1 register, which enables or disables output from the BUSCLK pin.

REVISION HISTORY	R-IN32M4-CL3 User's Manual: Board design edition

Rev.	Date	Description	
		Page	Summary
1.00	Dec 24, 2019	—	First edition issued
2.00	May 31, 2024	32	9. External MCU/Memory Interface Pins Note for Table 9.1 was deleted.
		43	9.2.2.1 Connection Example with SRAM Address and data port names for R-IN32M4-CL3 were corrected.
		44	9.2.2.2 Connection Example with Paged ROM Address and data port names for R-IN32M4-CL3 were corrected.

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