User's Manual

R-IN32M4-CL2

User's Manual

R9J03G019GBG

arm

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is intended for users who wish to understand the functions of industrial Ethernet communications ASSP (Application Specific Standard Product) "R-IN32M4-CL2" (R9J03G019GBG) and design application systems using it.
Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.

When designing an application system that includes this MCU, take all points to note into account. Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

Literature — Literature may be preliminary versions. Note, however, that the following descriptions do not indicate "Preliminary". Some documents on cores were created when they were planned or still under development. So, they may be directed to specific customers. Last four digits of document number (described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

Documents related to R-IN32M4-CL2

Document Name	Document Number
R-IN32M4-CL2 User's Manual (this manual)	R18UZ0033EJ****
R-IN32M4-CL2 User's Manual: Peripheral Modules	R18UZ0035EJ****
R-IN32M4-CL2 User's Manual: Gigabit Ethernet PHY	R18UZ0043EJ****
R-IN32M4-CL2 User's Manual: Board Design	R18UZ0046EJ****
R-IN32M4-CL2 Programming Manual: Driver	R18UZ0038EJ****
R-IN32M4-CL2 Programming Manual: OS	R18UZ0040EJ****

2. Numbers and Symbols

Data significance: Higher digits on the left and lower digits on the right

Active low representation:

xxxZ (capital letter Z after pin or signal name)

or xxx_N (capital letter _N after pin or signal name)

or xxnx (pin or signal name contains small letter n)

Note:

Footnote for item marked with Note in the text

Caution:

Information requiring particular attention

Remark:

Supplementary information

Numeric representation:

Binary … xxxx , xxxxB or n'bxxxx (n bits)

Decimal … xxxx

Hexadecimal … xxxxH or n'hxxxx (n bits)

Prefix indicating power of 2 (address space, memory capacity):

K (kilo) … $2^{10} = 1024$

M (mega) … $2^{20} = 1024^2$

G (giga) … $2^{30} = 1024^3$

Data Type:

Word … 32 bits

Halfword … 16 bits

Byte … 8 bits

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1. Overview

1.1 Introduction

Modern industrial Ethernet applications require increasingly high performance, such as higher speed real-time response. These requirements are not necessarily met by traditional methods such as hard-wired Ethernet processors or dedicated high-speed CPUs.

The R-IN32M4-CL2 Ethernet communications LSI chip from Renesas Electronics is specifically tailored to meet the demands of industrial Ethernet applications in the field of factory automation. Key features include:

- Integrated Arm® Cortex®-M4 core with FPU
- Integrated real-time OS accelerator with support for µITRON version 4.0
- On-chip physical layer for 10, 100, and 1000 Base-T
- Dedicated DMA controller and buffer for the network processor
- Multiple timers, serial interfaces, general purpose I/O ports (GPIO), external memory interfaces
- High-speed, real-time, deterministic, low-latency, low-jitter response for real-time applications
- High performance with low CPU usage by offloading functions to the real-time OS accelerator

1.2 Functional Overview

Table 1.1 Functional Overview of R-IN32M4-CL2 (1/2)

Item \ Product	R-IN32M4-CL2
CPU cores	Arm Cortex-M4 32-bit RISC CPU + Real-time OS accelerator (hardware real-time OS)
Operating frequency	100 MHz
Instruction set	Thumb®-2 instruction Armv7-M architecture
Floating-point unit	Armv7M FPv4-SP (32-bit single precision)
Instruction RAM	768 Kbytes (RAM with ECC)
Data RAM	512 Kbytes (RAM with ECC)
Buffer RAM	64 Kbytes (RAM with ECC)
Internal system bus	- 32-bit system bus at 100 MHz - 128-bit communication bus at 100 MHz
DMA bus (system bus side)	- 4 channels + 1 channel (for real-time port) - Supports software and various interrupt-triggered DMA
Boot options	- Serial flash ROM boot - External memory boot - External MCU boot
Support for external memory access	- Bus-size selection (16 or 32 bits) - Paged ROM/ROM/SRAM interface - Synchronous burst memory interface - Four chip select signals for static memory - External memory space: Up to 256 Mbytes - Programmable wait function
External MCU interface	- Bus-size selection (16 or 32 bits) - General-purpose interface for static memory - Address space:2 Mbytes (Instruction RAM, Data RAM, Register area)
Serial flash ROM memory controller	- Supports serial interface compatible with SPI of the companies - Supports direct boot from serial memory device - Supports fast reading, fast reading with dual output, fast reading with dual I/O, fast reading with quad output, fast reading with quad I/O - Direct layout in memory space
Interrupt	- 29 external interrupt ports
Internal peripheral modules	
I/O ports	CMOS I/O: up to 106 ports
Timers (4 sub-systems)	- Internal timer of hardware RTOS
	- Internal timer of the CPU
	- 32-bit timer (4 channels)
	- 16-bit timer (16 channels)

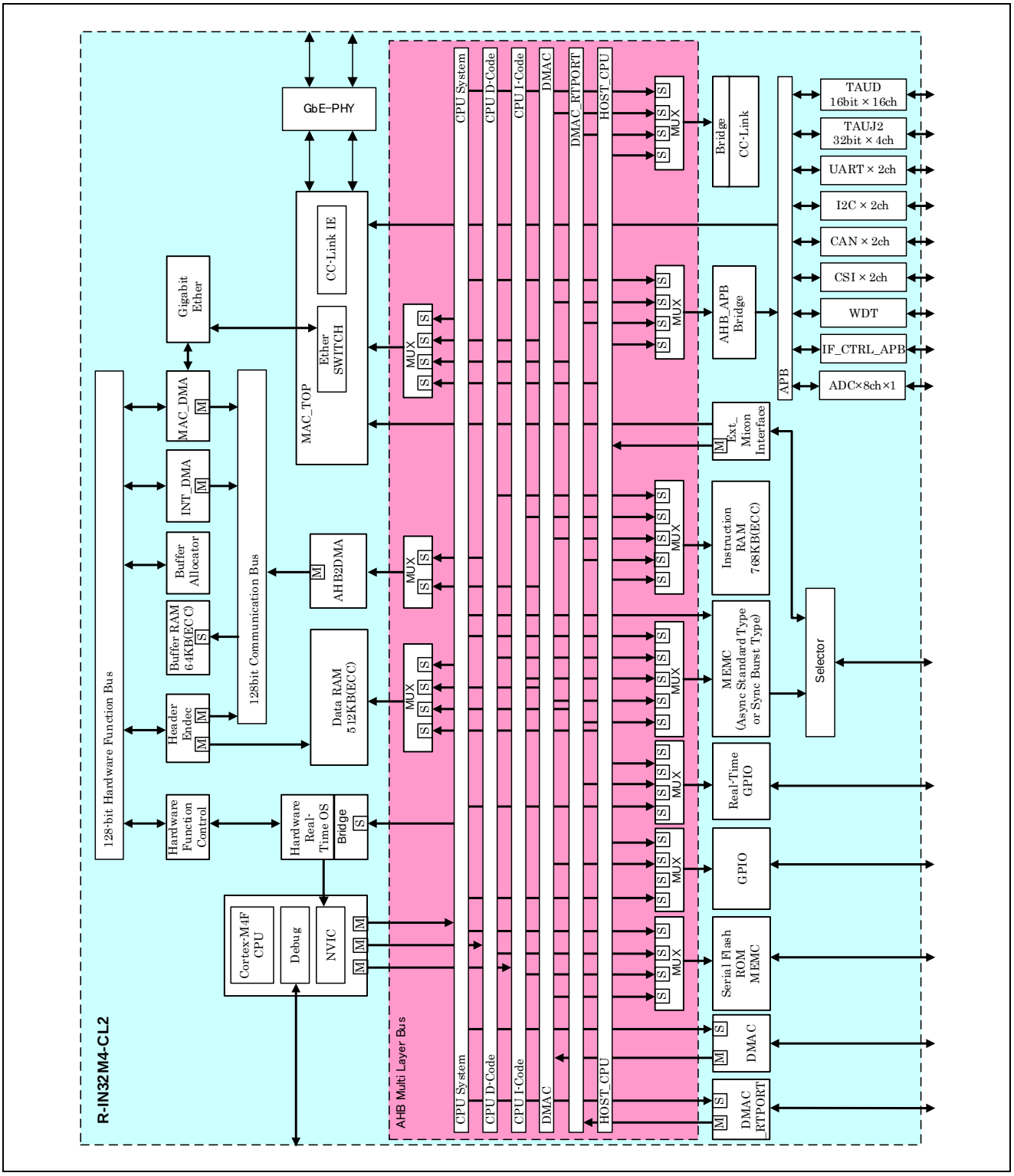
Watchdog timer	- 1 channel
	- Software-triggered start mode
	- Watchdog error response options:
	  - Generation of a non-maskable interrupt (NMI)
	  - Generation of a reset
	- Interrupt when the counter reaches 75% of its overflow value

Table 1.1 Overview of R-IN32M4-CL2 (2/2)

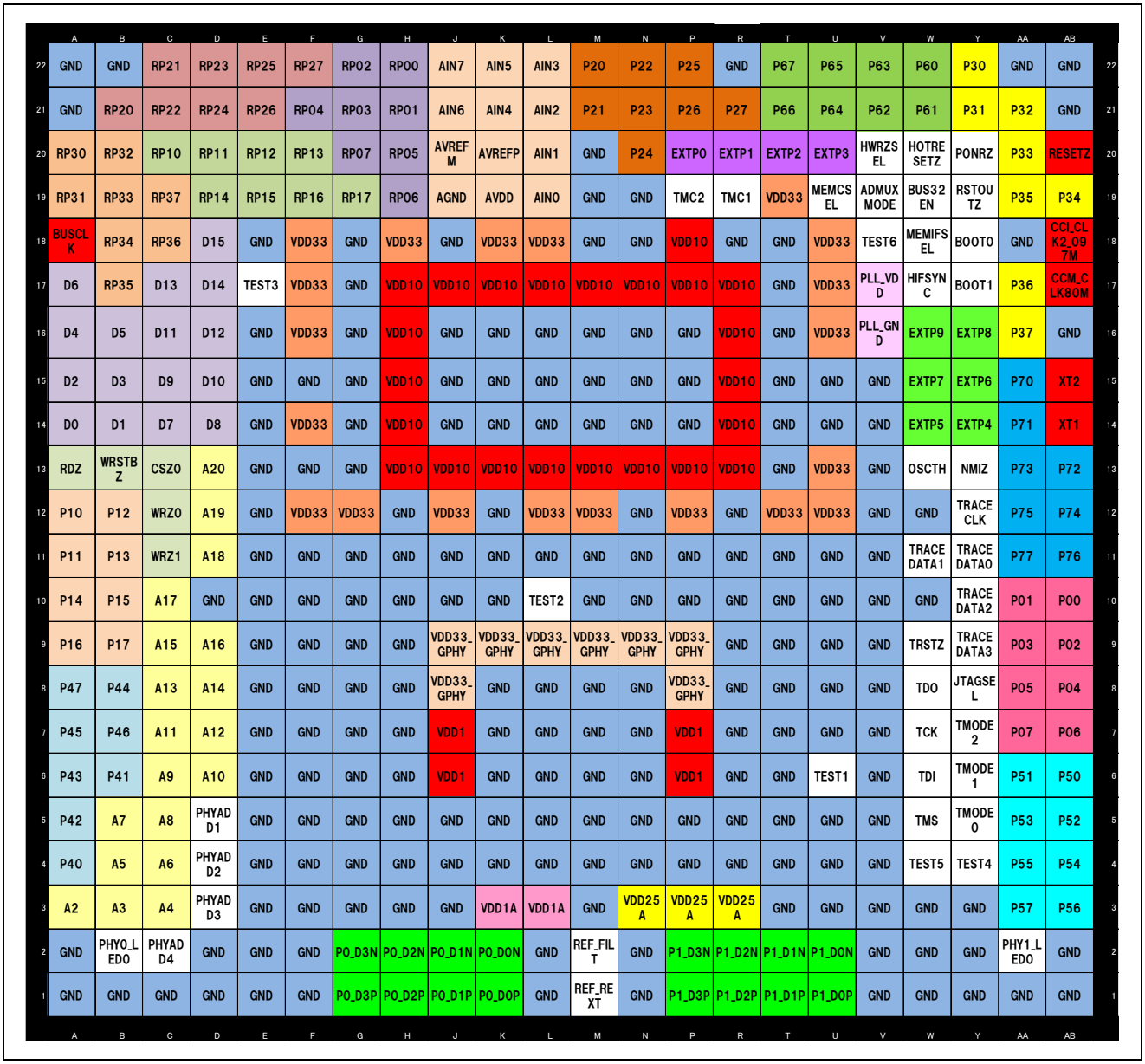
Item \ Product	R-IN32M4-CL2
Internal peripheral modules	
Asynchronous serial interface	- 2 channels - Full duplex transfer - FIFOs: 10-bit x 16 receive and 8-bit x 16 transmit - Support output of receive errors and status - Character length: 7 or 8-bit - Parity bit options: odd, even, 0- , none - Transmit stop bits: 1 or 2-bit
I2C serial interface	- 2 channels - Operating modes: normal or high-speed - Transfer modes: single-transfer mode or continuous-transfer mode - Transmission data length: 8-bit
CAN controller	- 2 channels - Conforming to ISO11898 - Support for transmission and reception of standard and expanded frames - Transfer rate: Up to 1 Mbps
Clocked serial interface	- 2 channels - Synchronized serial data transmission by three-wire system - Master mode or slave mode selectable - Built-in baud-rate generator - Transfer data length: 7 bits to 16 bits
10-bit AD converter	- Successive-approximation 10-bit A/D converter - 8 channels - Support for hardware and software triggers
CC-Link	- Intelligent device station Note - Remote device station
10/100/1000 Mbps Ethernet MAC	- 1 channel - Built-in 2-port switch
CC-Link IE	CC-Link IE Field (intelligent device station and remote device station)
On-chip debugging	- Selecting serial wire or JTAG - Full trace (built-in ETM)
Internal PLL	Generates various clocks from 25 MHz input clock
Power supply voltage	VDD33 = 3.3 ±0.165V (R-IN32M4, GbE-PHY) VDD10 = 1.0 ±0.05V (R-IN32M4, GbE-PHY) VDD25 = 2.5 ±0.125V (GbE-PHY)

Note: Please contact us for details.

1.3 Internal Block Diagram



1.4 Pin Assignments (Top View)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22	GND	GND	RP21	RP23	RP25	RP27	RP02	RP00	AIN7	AIN5	AIN3	P20	P22	P25	GND	P67	P65	P63	P60	P30	GND	GND	22
21	GND	RP20	RP22	RP24	RP26	RP04	RP03	RP01	AIN6	AIN4	AIN2	P21	P23	P26	P27	P66	P64	P62	P61	P31	P32	GND	21
20	RP30	RP32	RP10	RP11	RP12	RP13	RP07	RP05	AVREFM	AVREFP	AIN1	GND	P24	EXTP0	EXTP1	EXTP2	EXTP3	HWRZSEL	HOTRESETZ	PONRZ	P33	RESETZ	20
19	RP31	RP33	RP37	RP14	RP15	RP16	RP17	RP06	AGND	AVDD	AIN0	GND	GND	TMC2	TMC1	VDD33	MEMCSEL	ADMUXMODE	BUS32EN	RSTOUTZ	P35	P34	19
18	BUSCLK	RP34	RP36	D15	GND	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	GND	VDD10	GND	GND	VDD33	TEST6	MEMIFSEL	BOOT0	GND	CCI_CLK2_097M	18
17	D6	RP35	D13	D14	TEST3	VDD33	GND	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	GND	VDD33	PLL_VDD	HIFSYNC	BOOT1	P36	CCM_CLK80M	17
16	D4	D5	D11	D12	GND	VDD33	GND	VDD10	GND	GND	GND	GND	GND	GND	VDD10	GND	VDD33	PLL_GND	EXTP9	EXTP8	P37	GND	16
15	D2	D3	D9	D10	GND	GND	GND	VDD10	GND	GND	GND	GND	GND	GND	VDD10	GND	GND	GND	EXTP7	EXTP6	P70	XT2	15
14	D0	D1	D7	D8	GND	VDD33	GND	VDD10	GND	GND	GND	GND	GND	GND	VDD10	GND	GND	GND	EXTP5	EXTP4	P71	XT1	14
13	RDZ	WRSTBZ	CSZ0	A20	GND	GND	GND	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	GND	VDD33	GND	OSCTH	NMIZ	P73	P72	13
12	P10	P12	WRZ0	A19	GND	VDD33	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	GND	TRACECLK	P75	P74	12
11	P11	P13	WRZ1	A18	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TRACEDATA1	TRACEDATA0	P77	P76	11
10	P14	P15	A17	GND	GND	GND	GND	GND	GND	GND	TEST2	GND	GND	GND	GND	GND	GND	GND	GND	TRACEDATA2	P01	P00	10
9	P16	P17	A15	A16	GND	GND	GND	GND	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	GND	GND	GND	GND	TRSTZ	TRACEDATA3	P03	P02	9
8	P47	P44	A13	A14	GND	GND	GND	GND	VDD33_GPHY	GND	GND	GND	GND	VDD33_GPHY	GND	GND	GND	GND	TDO	JTAGSEL	P05	P04	8
7	P45	P46	A11	A12	GND	GND	GND	GND	VDD1	GND	GND	GND	GND	VDD1	GND	GND	GND	GND	TCK	TMODE2	P07	P06	7
6	P43	P41	A9	A10	GND	GND	GND	GND	VDD1	GND	GND	GND	GND	VDD1	GND	GND	TEST1	GND	TDI	TMODE1	P51	P50	6
5	P42	A7	A8	PHYADD1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TMS	TMODE0	P53	P52	5
4	P40	A5	A6	PHYADD2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TEST5	TEST4	P55	P54	4
3	A2	A3	A4	PHYADD3	GND	GND	GND	GND	GND	VDD1A	VDD1A	GND	VDD25A	VDD25A	VDD25A	GND	GND	GND	GND	GND	P57	P56	3
2	GND	PHYO_LEDO	PHYADD4	GND	GND	GND	P0_D3N	P0_D2N	P0_D1N	P0_DON	GND	REF_FILT	GND	P1_D3N	P1_D2N	P1_D1N	P1_DON	GND	GND	GND	PHY1_LEDO	GND	2
1	GND	GND	GND	GND	GND	GND	P0_D3P	P0_D2P	P0_D1P	P0_DOP	GND	REF_REXT	GND	P1_D3P	P1_D2P	P1_D1P	P1_DOP	GND	GND	GND	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

1.5 Base Addresses of the System Registers Area

The addresses of registers given in the subsequent sections are relative to the base addresses. In access to the registers via the external MCU interface, the base address is D_0000H. In access by the internal CPU or DMA controller, the base address is 4001_0000H.

- In access by the CPU or DMA controller
  BASE = 4001_0000H
- In access via the external microcontroller interface
  BASE = D_0000H

2. Pin Functions

The meanings of the symbols and abbreviations used in this document are given below.

Table 2.1 Meanings of the Items in the List of Pins

Item	Meaning
Function Name	Name of a function of the pin under "Pin Name" below.
Pin Name	Name of the pin shown in section 1.4, Pin Assignments (Top View).
I/O	I/O direction of the given pin
Description	Summary of the given pin function
Active	Active level of the given pin
Level during Reset	"Level during reset" indicates the pin state while RSTOUTZ = low. For details on the reset specifications, see section 2.3.4, Operations for Reset, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

Table 2.2 Meanings of the Symbols and Abbreviations in the List of Pins

Target	Symbol and Abbreviation	Meaning
Pin Name	- (hyphen)	Indicates that the pin is a dedicated pin and is not multiplexed with a port-pin function.
I/O	- (hyphen)	Indicates that the pin is a pin such as a power supply or ground pin and so does not have an I/O direction.
Active Level	- (hyphen)	Indicates that there is no active level (clock signals, data bus, and address bus).
	High	The active level is high.
	Low	The active level is low.
Level during Reset	- (hyphen)	Indicates an input-dedicated pin that has no initial level or state following a reset.
	High	The pin state during a reset is high.
	Low	The pin state during a reset is low.
	Hi-Z (high)	The pin state during a reset is Hi-Z (high) with the internal pull-up resistor pulling it to the high level.
	Hi-Z (low)	The pin state during a reset is Hi-Z (low) with the internal pull-up resistor pulling it to the low level.

2.1 List of Pins

The respective pins listed in the tables of sections 2.1.2, Ethernet Pins, to 2.1.18, ADC Pins are multiplexed with the respective port pins listed in section 2.1.1, Port Pins and Real-Time Port Pins. For details, see multiplexed functions 1 to 4 of the table in section 2.1.1, Port Pins and Real-Time Port Pins.

2.1.1 Port Pins and Real-Time Port Pins

The chip has 13 ports and real-time ports for the 3.3-V interface, all of which are 8-bit ports except for EXTP, which has 10 bits.
Grouping them into sets of four ports allows 32-bit access: i.e., through ports 0 to 3 (P00 to P37), ports 4 to 7 (P40 to P77), and real-time ports 0 to 3 (RP00 to RP37).

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Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
P00	INTPZ0	-	CCI_RUNLEDZ	CCS_MON1	Hi-Z (high)
P01	INTPZ1	-	-	CCS_MON2	
P02	INTPZ2	-	CCI_DLINKLEDZ	CCS_STBMSK	
P03	INTPZ3	-	CCI_ERRLEDZ	CCS_MON5	
P04	INTPZ4	-	CCI_LERR1LEDZ	CCS_MON6	
P05	INTPZ5	-	CCI_LERR2LEDZ	CCS_MON7	
P06	-	-	CCI_SDLEDZ	CCS_MON0	
P07	-	-	CCI_RDLEDZ	CCS_RESOUT	
P10	SMIO2	-	-	CCS_MON1	
P11	SMIO3	-	-	CCS_MON2	
P12	CSZ3	-	CCI_WDTIZ / CCM_WDTENZ / CCS_WDTZ	CCS_MON3	
P13	CSZ2	-	-	-	
P14	SMSCK	-	-	-	
P15	SMIO0	-	-	-	
P16	SMIO1	-	-	-	
P17	SMCSZ	-	-	-	
P20	RXD0	-	CCM_LINKERRZ	-	
P21	TXD0	-	CCM_ERRZ	-	
P22	INTPZ8	-	CCS_IOTENSU	-	
P23	INTPZ9	-	CCS_SENYU0	-	
P24	INTPZ10	ETHSWSYNCOUT	CCS_SENYU1	-	
P25	WDTOUTZ	-	CCS_ERRZ	-	
P26	TINJ1 / TIND5 Note 1	TOUTJ1 / TOUTD5 Note 1	CCM_RUNZ / CCS_RUNZ Note 2	-	
P27	TINJ0 / TIND4 Note 1	TOUTJ0 / TOUTD4 Note 1	-	-	

Notes 1. Enabling the TAUJ2 or TAUD pin functions is selectable by using the TMISEL register. For details, see section 25.18, Timer I/F Select Register (TMISEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

2. The signal generated by the CCSRUN register and signals from CC-Link are multiplexed on the P26 pin. For details, see section 24.1.6, CC-Link Slave RUN LED Control Register (CCSRUN), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

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Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
P30	RXD1	-	-	-	Hi-Z (high)
P31	TXD1	-	-	-	
P32	DMAREQZ1	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-	
P33	DMAACKZ1	-	CCM_RDLEDZ / CCS_RDLEDZ	-	
P34	DMATCZ1	-	-	-	
P35	CSISCK1	INTPZ22	-	-	Hi-Z (low)
P36	CSISI1	INTPZ23	-	-	Hi-Z (high)
P37	CSISO1	INTPZ24	-	-	Hi-Z (low)
P40	A1 / MA0	HA1	-	-	Hi-Z (high)
P41	WAITZ	HWAITZ	-	-	
P42	CSICS00	HERROUTZ	CCS_FUSEZ	-	
P43	CSICS01	HBUSCLK	CCM_IRLZ	-	
P44	CSZ1	HPGCSZ	-	-	
P45	CSISCK0	WAITZ1	-	-	
P46	CSISI0	WAITZ2	-	-	
P47	CSISO0	WAITZ3	-	-	
P50	INTPZ6	-	-	CCS_REFSTB	
P51	INTPZ7	-	-	CCS_SDGATEON	Hi-Z (low)
P52	TINJ3 / TIND7 Note	TOUTJ3 / TOUTD7 Note	CCI_NMIZ	CCS_DCHANG	Hi-Z (high)
P53	CRXD0	CCI_INTZ	-	-	
P54	CTXD0	CCS_RD	CCM_RD	-	
P55	CRXD1	CCS_MON4	-	-	
P56	CTXD1	CCS_SD	CCM_SD	-	
P57	TINJ2 / TIND6 Note	TOUTJ2 / TOUTD6 Note	CCM_SDGCZ	-	

Note: Enabling the TAUJ2 or TAUD pin functions is selectable by using the TMISEL register. For details, see section 25.18, Timer I/F Select Register (TMISEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

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Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
P60	SCL0	-	-	-	Hi-Z (high)
P61	SDA0	-	-	-	
P62	RTDMAREQZ	-	CCM_MDIN0	-	
P63	RTDMAACKZ	-	CCM_MDIN1	-	
P64	RTDMATCZ	-	CCM_MDIN2	-	
P65	DMAREQZ0	-	CCM_MDIN3	-	
P66	DMAACKZ0	-	CCM_MSTZ	-	
P67	DMATCZ0	-	CCS_MON3	-	
P70	CSICS10	-	CCS_STATION_NO_0 / CCM_SNIN0	-	
P71	CSICS11	-	CCS_STATION_NO_1 / CCM_SNIN1	-	
P72	SLEEPING	-	CCS_STATION_NO_2 / CCM_SNIN2	-	
P73	INTPZ11	-	CCS_STATION_NO_3 / CCM_SNIN3	-	
P74	INTPZ12	-	CCS_STATION_NO_4 / CCM_SNIN4	-	
P75	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	-	
P76	INTPZ14	-	CCS_STATION_NO_6 / CCM_SNIN6	-	
P77	INTPZ15	-	CCS_STATION_NO_7 / CCM_SNIN7	-	

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Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
EXTP0	-	TOUTD0	-	TIND0	Hi-Z (high)
EXTP1	-	TOUTD1	-	TIND1	
EXTP2	-	TOUTD2	-	TIND2	
EXTP3	WDTOUTZ	TOUTD3	-	TIND3	
EXTP4	-	-	-	-	
EXTP5	-	-	-	-	
EXTP6	-	-	-	-	Hi-Z (low)
EXTP7	CCM_STMON3	-	-	-	Hi-Z (high)
EXTP8	-	-	-	-	
EXTP9	-	-	-	-	

Ports RP0x to RP3x (x: 0 to 7) operate as real-time ports. Together, they are able to handle input and output in 32-bit units in synchronization with the DMA transfer trigger from the dedicated DMA controller for the real-time ports.

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Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
RP00	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-	Hi-Z (high)
RP01	INTPZ17	SDA1	CCM_SMSTZ	-	
RP02	INTPZ18	ADTRG	CCS_BS1	-	
RP03	INTPZ19	ADTRGRDY	CCS_BS2	-	
RP04	INTPZ20	-	CCS_BS4	-	
RP05	INTPZ21	-	CCS_BS8	-	
RP06	WRZ2 / BENZ2	HWRZ2 / HBENZ2	-	-	
RP07	WRZ3 / BENZ3	HWRZ3 / HBENZ3	-	-	
RP10	D24 / MD24 / HD24	LED0_PHY0	-	-	
RP11	D25 / MD25 / HD25	LED1_PHY0	-	-	
RP12	D26 / MD26 / HD26	LED2_PHY0	-	-	
RP13	D27 / MD27 / HD27	LED3_PHY0	-	-	
RP14	D28 / MD28 / HD28	LED0_PHY1	-	-	
RP15	D29 / MD29 / HD29	LED1_PHY1	-	-	
RP16	D30 / MD30 / HD30	LED2_PHY1	-	-	
RP17	D31 / MD31 / HD31	LED3_PHY1	-	-	
RP20	BCYSTZ / ADVZ	HBCYSTZ	-	-	
RP21	A21 / MA20	-	-	-	Hi-Z (low)
RP22	A22 / MA21	-	-	-	
RP23	A23 / MA22	-	-	-	
RP24	A24 / MA23	INTPZ25	-	-	
RP25	A25 / MA24	INTPZ26	-	-	
RP26	A26 / MA25	INTPZ27	-	-	
RP27	A27 / MA26	INTPZ28	-	-	
RP30	D16 / MD16 / HD16	TOUTD8	TIND8	-	Hi-Z (high)
RP31	D17 / MD17 / HD17	TOUTD9	TIND9	-	
RP32	D18 / MD18 / HD18	TOUTD10 Note	TIND10	-	
RP33	D19 / MD19 / HD19	TOUTD11 Note	TIND11	-	
RP34	D20 / MD20 / HD20	TOUTD12 Note	TIND12	-	
RP35	D21 / MD21 / HD21	TOUTD13 Note	TIND13	-	
RP36	D22 / MD22 / HD22	TOUTD14 Note	TIND14	-	
RP37	D23 / MD23 / HD23	TOUTD15 Note	TIND15	-	

Note: Output of the TAUD or PIC pin functions is selectable by using the TOUTDSEL register. For details, see section 25.21, TOUTD Output Select Register (TOUTD_SEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

2.1.2 Ethernet Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
P0_D0N	-	I/O	PHY 0 Tx/Rx channel A negative signal	-	-
P0_D0P	-	I/O	PHY 0 Tx/Rx channel A positive signal	-	-
P0_D1N	-	I/O	PHY 0 Tx/Rx channel B negative signal	-	-
P0_D1P	-	I/O	PHY 0 Tx/Rx channel B positive signal	-	-
P0_D2N	-	I/O	PHY 0 Tx/Rx channel C negative signal	-	-
P0_D2P	-	I/O	PHY 0 Tx/Rx channel C positive signal	-	-
P0_D3N	-	I/O	PHY 0 Tx/Rx channel D negative signal	-	-
P0_D3P	-	I/O	PHY 0 Tx/Rx channel D positive signal	-	-
P1_D0N	-	I/O	PHY 1 Tx/Rx channel A negative signal	-	-
P1_D0P	-	I/O	PHY 1 Tx/Rx channel A positive signal	-	-
P1_D1N	-	I/O	PHY 1 Tx/Rx channel B negative signal	-	-
P1_D1P	-	I/O	PHY 1 Tx/Rx channel B positive signal	-	-
P1_D2N	-	I/O	PHY 1 Tx/Rx channel C negative signal	-	-
P1_D2P	-	I/O	PHY 1 Tx/Rx channel C positive signal	-	-
P1_D3N	-	I/O	PHY 1 Tx/Rx channel D negative signal	-	-
P1_D3P	-	I/O	PHY 1 Tx/Rx channel D positive signal	-	-
PHYADD1	-	I	Device SMI Address bit 1 (with PD resistance)	-	-
PHYADD2	-	I	Device SMI Address bit 2 (with PD resistance)	-	-
PHYADD3	-	I	Device SMI Address bit 3 (with PD resistance)	-	-
PHYADD4	-	I	Device SMI Address bit 4 (with PD resistance)	-	-
REF_FILT	-	I/O	Copper media reference filter pin.	-	-
REF_REXT	-	I/O	Copper media reference external pin.	-	-
VDD1	-	-	1.0-V internal power supply	-	-
VDD1A	-	-	1.0-V analog power requiring additional PCB power supply filtering	-	-
VDD25A	-	-	2.5-V general analog power supply	-	-
VDD33_GPHY	-	-	3.3-V general I/O power supply	-	-
PHY0_LED0	-	O	GbE-PHY LED0_PHY0 output signal	Low	High
PHY1_LED0	-	O	GbE-PHY LED0_PHY1 output signal	Low	High
ETHSWSYNCOUT	P24	O	Ethernet switch event output	High	Hi-Z (high)

2.1.3 External SRAM and External MCU Interfaces

Usage of the external SRAM and external MCU interfaces is exclusive.
This is selected by the level on the MEMIFSEL pin (settings: low level for the external SRAM interface; high level for the external MCU interface).

2.1.3.1 SRAM Interface Pins

(a) When the asynchronous SRAM memory controller is selected (MEMCSEL=0)

Function Name	Pin Name	I/O	Description	Active	Level during Reset
BUSCLK	-	O	Bus clock output	-	Clock output
CSZ0	-	O	Chip select signal output	Low	Hi-Z (high)
CSZ1	P44	O			
CSZ2	P13	O			
CSZ3	P12	O			
A1	P40	O	Address output	-	
A2-A20	-	O			Hi-Z (low)
A21-A27	RP21-RP27	O			
D0-D15	-	I/O	Data bus		
D16-D31	RP30-RP37, RP10-RP17	I/O			Hi-Z (high)
RDZ	-	O	Read strobe output	Low	
WRSTBZ	-	O	Write strobe output		
WRZ0 / BENZ0 Note	WRZ0	O	Valid byte lane strobe output		
WRZ1 / BENZ1 Note	WRZ1	O			
WRZ2 / BENZ2 Note	RP06	O			
WRZ3 / BENZ3 Note	RP07	O			
WAITZ	P41	I	Wait signal input		
BCYSTZ	RP20	O	Bus cycle start status output		

Remark: The external memory interface pins other than BUSCLK are inputs as long as the internal reset signal (HRESETZ) is active.

Note: The WREN register is used to switch pin functions between WRZ3 to WRZ0 and BENZ3 to BENZ0.
See section 10.3.5, Write Enable Switching Register (WREN), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

(b) When the synchronous burst access memory controller is selected (MEMCSEL = 1)

Function Name	Pin Name	I/O	Description	Active	Level during Reset
BUSCLK	-	O	Bus clock output	-	Clock output
CSZ0	-	O	Chip select signal output	Low	Hi-Z (high)
CSZ1	P44	O			
CSZ2	P13	O			
CSZ3	P12	O			
MA0	P40	O	Address output	-	
MA1-MA19	A2-A20	O			Hi-Z (low)
MA20-MA26	RP21-RP27	O			
MD0-MD15 / MA0-MA15 Note 1	D0-D15	I/O	Data bus		
MD16-MD31 / MA16-MA31 Note 1	RP30-RP37, RP10-RP17	I/O			Hi-Z (high)
RDZ	-	O	Read strobe output	Low	
WRSTBZ	-	O	Write strobe output		
WRZ0 / BENZ0 Note 2	WRZ0	O	Valid byte lane strobe output		
WRZ1 / BENZ1 Note 2	WRZ1	O			
WRZ2 / BENZ2 Note 2	RP06	O			
WRZ3 / BENZ3 Note 2	RP07	O			
WAITZ	P41	I	Wait signal input		
WAITZ1-WAITZ3	P45-P47	I	Wait signal input		
ADVZ	RP20	O	Address valid output		

Remark: The external memory interface pins other than BUSCLK are inputs as long as the internal reset signal (HRESETZ) is active.

Notes 1. If the ADMUXMODE pin is at the high level, these pin functions are multiplexed with address pin functions.

ADMUXMODE = 0: MD0-MD31 (separated address and data lines)

ADMUXMODE = 1: MD0-MD31/MA0-MA31 (multiplexed address and data lines)

2. The SET_OPMODE register is used to switch pin functions between WRZ3 to WRZ0 and BENZ3 to BENZ0.

For details of this register, see section 11.2.8, Synchronous Burst Access MEMC Mode Setting Register (SET_OPMODE), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

2.1.3.2 External MCU Interface Pins

(a) When the asynchronous SRAM memory controller is selected (MEMCSEL=0)

Function Name	Pin Name	I/O	Description	Active	Level during Reset
HBUSCLK[Note1]	P43	I	Bus clock input	-	Hi-Z (high)
HCSZ	CSZ0	I	Chip select signal input	Low	
HPGCSZ	P44	I	Page ROM mode chip select signal input		
HWAITZ	P41	O	Wait signal output		
HA1	P40	I	Address signal input	-	
HA2-HA20	A2-A20	I			Hi-Z (low)
HD0-HD15	D0-D15	I/O	Data bus		
HD16-HD31	RP30-RP37, RP10-RP17	I/O			Hi-Z (high)
HRDZ	RDZ	I	Read strobe input	Low	
HWRSTBZ	WRSTBZ	I	Write strobe input		
HWRZ0 / HBENZ0 [Note2]	WRZ0	I	Valid byte lane strobe input		
HWRZ1 / HBENZ1 [Note2]	WRZ1	I			
HWRZ2 / HBENZ2 [Note2]	RP06	I			
HWRZ3 / HBENZ3 [Note2]	RP07	I			
HERROUTZ	P42	O	Error interrupt output		High
HBCYSTZ	RP20	I	Bus cycle input		Hi-Z (high)

Notes1: HBUSCLK is used in case of Synchronous SRAM supported MCU connection mode (HIFSYNC pin is High). HBUSCLK is not used in case of Asynchronous SRAM supported MCU connection mode (HIFSYNC pin is Low). Further, the other signal connection is common in each mode. For details on the connection example, see section 10.1, External MCU interface, in the R-IN32M4-CL2 User's Manual: Board Design.

2: The level being input on the HWRZSEL pin controls switching between the HWRZ3 to HWRZ0 and HBENZ3 to HBENZ0 signals.

Remark: The external MCU interface pins continue to operate even during a reset.

(b) When the synchronous burst access memory controller is selected (MEMCSEL = 1)

Function Name	Pin Name	I/O	Description	Active	Level during Reset
HBUSCLK	P43	I	Bus clock input	-	Hi-Z (high)
HCSZ	CSZ0	I	Chip select signal input	Low	
HPGCSZ	P44	I	Page ROM mode chip select signal input		
HWAITZ	P41	O	Wait signal output		
HA1 Note 1	P40	I	Address signal input	-	
HA2-HA20 Note 1	A2-A20	I			Hi-Z (low)
HD0-HD15 Note 1	D0-D15	I/O	Data bus		
HD16-HD31 Note 1	RP30-RP37, RP10-RP17	I/O			Hi-Z (high)
HRDZ	RDZ	I	Read strobe input	Low	
HWRSTBZ	WRSTBZ	I	Write strobe input		
HWRZ0 / HBENZ0 Note 2	WRZ0	I	Valid byte lane strobe input		
HWRZ1 / HBENZ1 Note 2	WRZ1	I			
HWRZ2 / HBENZ2 Note 2	RP06	I			
HWRZ3 / HBENZ3 Note 2	RP07	I			
HERROUTZ	P42	O	Error interrupt output		High
HBCYSTZ	RP20	I	Bus cycle input		Hi-Z (high)

Note1: The address/data signal connection is depend on address/data multiplex mode (ADMUXMODE pin is High) or address/data separate mode (ADMUXMODE pin is Low).
For details on the connection example, see section 10.1, External MCU interface, in the R-IN32M4-CL2 User's Manual: Board Design.
2: Setting the HWRZSEL pin to 1 is prohibited while the setting of the MEMCSEL pin is 1.

Remark: The external MCU interface pins continue to operate even during a reset.

2.1.4 Serial Flash ROM Interface Pins

The serial flash ROM interface pins are pins of the serial flash ROM memory controller.
They support the following modes: fast reading, fast reading with dual output, fast reading with dual I/O, fast reading with quad output, and fast reading with quad I/O.

Function Name	Pin Name	I/O	Description	Active	Level during Reset
SMSCK	P14	O	Serial clock output signal for serial flash ROM	-	Hi-Z (high)
SMIO0	P15	I/O	Serial data I/O signal for serial flash ROM (Connected to the IO0 pin of serial flash ROM)		
SMIO1	P16	I/O	Serial data I/O signal for serial flash ROM (Connected to the IO1 pin of serial flash ROM)		
SMIO2	P10	I/O	Serial data I/O signal for serial flash ROM (Connected to the /WP(IO2) pin of serial flash ROM)		
SMIO3	P11	I/O	Serial data I/O signal for serial flash ROM (Connected to the /HOLD(IO3) pin of serial flash ROM)		
SMCSZ	P17	O	Chip select signal output for serial flash ROM	Low	

2.1.5 DMA Interface Pins

The DMA interface pins are external interface pins of the DMA controllers for the internal AHB bus.
As the external DMA interface, they control two types of DMA controllers incorporated in the R-IN32M4-CL2; a general DMA controller for channel 0 and channel 1, and a DMA controller for real-time ports.

Function Name	Pin Name	I/O	Description	Active	Level during Reset
RTDMAREQZ	P62	I	RTDMAC DMA transfer request input	Low	Hi-Z (high)
RTDMAACKZ	P63	O	RTDMAC DMA acknowledge output		
RTDMATCZ	P64	O	RTDMAC terminal count output		
DMAREQZ0	P65	I	DMA transfer request input 0		
DMAACKZ0	P66	O	DMA acknowledge output 0		
DMATCZ0	P67	O	Terminal count output 0		
DMAREQZ1	P32	I	DMA transfer request input 1		
DMAACKZ1	P33	O	DMA acknowledge output 1		
DMATCZ1	P34	O	Terminal count output 1		

Caution: The DMA interface pin is fixed to the specific channel of the DMA controller, and not assigned to any other DMA controller or channel. For details, see section 14, DMA Controllers, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

2.1.6 External Interrupt Input Pins

The chip has one non-maskable interrupt and 29 maskable interrupt input pins.

Function Name	Pin Name	I/O	Description	Active	Level during Reset
NMIZ	-	I	Non-maskable external interrupt input	Low	Hi-Z (high)
INTPZ0-INTPZ5	P00-P05	I	External interrupt input		
INTPZ6	P50				
INTPZ7	P51				Hi-Z (low)
INTPZ22	P35				
INTPZ24	P37				
INTPZ8-INTPZ10	P22-P24				Hi-Z (high)
INTPZ11-INTPZ15	P73-P77				
INTPZ16-INTPZ21	RP00-RP05				
INTPZ23	P36				
INTPZ25-INTPZ28	RP24-RP27				

2.1.7 Timer I/O Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
TINJ0 / TOUTJ0 Note	P27	I/O	Timer TAUJ2 I/O pin	-	Hi-Z (high)
TINJ1 / TOUTJ1 Note	P26				
TINJ2 / TOUTJ2 Note	P57				
TINJ3 / TOUTJ3 Note	P52				
TIND0 / TOUTD0	EXTP0		Timer TAUD I/O pin		
TIND1 / TOUTD1	EXTP1				
TIND2 / TOUTD2	EXTP2				
TIND3 / TOUTD3	EXTP3				
TIND4 / TOUTD4 Note	P27				
TIND5 / TOUTD5 Note	P26				
TIND6 / TOUTD6 Note	P57				
TIND7 / TOUTD7 Note	P52				
TIND8 / TOUTD8	RP30				
TIND9 / TOUTD9	RP31				
TIND10 / TOUTD10	RP32				
TIND11 / TOUTD11	RP33				
TIND12 / TOUTD12	RP34				
TIND13 / TOUTD13	RP35				
TIND14 / TOUTD14	RP36				
TIND15 / TOUTD15	RP37				

Note: TINJ0-TINJ3 and TOUTJ0-TOUTJ3, and TIND4-TIND7 and TOUTD4-TOUTD7, are assigned as multiplexed functions of the same port pins. Use the TMISEL register to select the pin functions to be used. For details of this register, see section 25.18, Timer I/F Select Register (TMISEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.
If you are not using external pin functions such as the interval timer function of the internal clock, both TAUJ2 and TAUD can be used at the same time.

2.1.8 Watchdog Timer Output Pin

Function Name	Pin Name	I/O	Description	Active	Level during Reset
WDTOUTZ	P25 / EXTP3	O	Watchdog timer output pin	Low	Hi-Z (high)

2.1.9 Serial Interface Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
TXD0	P21	O	UART0 serial data output	-	Hi-Z (high)
RXD0	P20	I	UART0 serial data input		
TXD1	P31	O	UART1 serial data output		
RXD1	P30	I	UART1 serial data input		
CSISCK0	P45	I/O	CSI0 serial clock input/output		
CSISI0	P46	I	CSI0 serial data input		
CSISO0	P47	O	CSI0 serial data output		
CSICS00	P42	O	CSI0 chip select signal output 0	Low	
CSICS01	P43	O	CSI0 chip select signal output 1		
CSISCK1	P35	I/O	CSI1 serial clock input/output	-	Hi-Z (low)
CSISI1	P36	I	CSI1 serial data input		Hi-Z (high)
CSISO1	P37	O	CSI1 serial data output		Hi-Z (low)
CSICS10	P70	O	CSI1 chip select signal output 0	Low	Hi-Z (high)
CSICS11	P71	O	CSI1 chip select signal output 1		
SCL0	P60	I/O	I2C0 serial clock	-	
SDA0	P61	I/O	I2C0 serial data		
SCL1	RP00	I/O	I2C1 serial clock		
SDA1	RP01	I/O	I2C1 serial data		
CRXD0	P53	I	CAN0 receive data input (5 V-tolerant buffer)		
CTXD0	P54	O	CAN0 transmit data output (5 V-tolerant buffer)		
CRXD1	P55	I	CAN1 receive data input (5 V-tolerant buffer)		
CTXD1	P56	O	CAN1 transmit data output (5 V-tolerant buffer)		

2.1.10 CC-Link IE Field Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
CCI_RUNLEDZ	P00	O	Run status output	Low	Hi-Z (high)
CCI_DLINKLEDZ	P02	O	Cyclic communication status output		
CCI_ERRLEDZ	P03	O	Field network error status output		
CCI_LERR1LEDZ	P04	O	Link error status output 1		
CCI_LERR2LEDZ	P05	O	Link error status output 2		
CCI_SDLEDZ	P06	O	Transmission state output		
CCI_RDLEDZ	P07	O	Port reception state output		
CCI_NMIZ	P52	O	Output NMI interrupt to MCU		
CCI_WDTIZ	P12	I	Input from external watchdog timer		
CCI_INTZ	P53	O	Output interrupt signal to MCU		
CCI_CLK2_097M	-	I	2.097152-MHz clock (crystal oscillator)	-	-
CCI_WAITEDGEH Note1,2	TRACEDATA2	I	Wait synchronized edge setting		Hi-Z (high)
CCI_WRLENH Note1,2	TRACEDATA3	I	WRZ mode setting		

Notes1. The latched values of the states of the following pins during a reset are input to the internal CCI_WAITEDGEH and CCI_WRLENH input pins of the CC-Link IE Field.

Pin function (within the IEF)	External pin with level to be latched
CCI_WAITEDGEH	TRACEDATA2
CCI_WRLENH	TRACEDATA3

2. When booting in external memory boot mode, external serial flash ROM boot mode, or instruction RAM boot mode, drive the TRACEDATA2 pin (multiplexed with CCI_WAITEDGEH) and the TRACEDATA3 pin (multiplexed with CCI_WRLENH) high during a reset.
If the TRACEDATA2 and TRACEDATA3 pins are driven low during a reset, accessing the CC-Link IE Field from the CPU in the R-IN32M4-CL2 is not possible.

2.1.11 CC-Link Pins (Intelligent Device Station)

Function Name	Pin Name	I/O	Description	Active	Level during Reset
CCM_LINKERRZ	P20	O	Link error LED control output	Low	Hi-Z (high)
CCM_ERRZ	P21	O	Not used		
CCM_RUNZ	P26	O	RUN LED control output		
CCM_MDIN0- CCM_MDIN3	P62-P65	I	Transfer rate setting input	-	
CCM_SNIN0- CCM_SNIN7	P70-P77	I	Station no. setting switch input		
CCM_LNKRUNZ	P32	O	Link Run LED control output	Low	
CCM_RDLEDZ	P33	O	Receive data LED control output		
CCM_SDLEDZ	RP00	O	Transmit data LED control output		
CCM_IRLZ	P43	O	Interrupt signal output from communications circuit		
CCM_WDTENZ	P12	I	Watchdog timer error input		
CCM_MSTZ	P66	O	Not used		
CCM_SMSTZ	RP01	O	Not used		
CCM_RD	P54	I	Communications circuit data reception pin	-	
CCM_SD	P56	O	Communications circuit data transmission pin		
CCM_SDGCZ	P57	O	Communications circuit transmit data & gate control pin	Low	
CCM_STMON3	EXTP7	O	Status output	-	
CCM_CLK80M	-	I	CC-Link clock input (80 MHz)		-

2.1.12 CC-Link Pins (Remote Device Station)

Function Name	Pin Name	I/O	Description	Active	Level during Reset
CCS_MON0	P06	O	Monitor signal	-	Hi-Z (high)
CCS_MON1	P00 / P10	O			
CCS_MON2	P01 / P11	O			
CCS_MON3	P12 / P67	O			
CCS_MON4	P55	O			
CCS_MON5- CCS_MON7	P03-P05	O			
CCS_RESOUT	P07	O	Reset output signal	High	
CCS_IOTENSU	P22	I	Initial setting pin	-	
CCS_SENYU0	P23	I			
CCS_SENYU1	P24	I			
CCS_ERRZ	P25	O	Operation check LED	Low	
CCS_RUNZ	P26	O	Operation check LED		
CCS_LNKRUNZ	P32	O	Link Run LED control output		
CCS_STATION_NO_0- CCS_STATION_NO_7	P70-P77	I	Station no. setting switch input pins	-	
CCS_REFSTB	P50	O	Interrupt signal	High	
CCS_STBMSK	P02	I/O	CLK stop monitor input/output	-	
CCS_DCHANG	P52	I/O	CLK stop monitor input/output		
CCS_WDTZ	P12	I	WDT input	Low	
CCS_RDLEDZ	P33	O	Receive data LED control output		
CCS_RD	P54	I	Communications circuit data reception pin	-	
CCS_SD	P56	O	Communications circuit data transmission pin		
CCS_SDLEDZ	RP00	O	Operation check LED	Low	
CCS_SDGATEON	P51	O	Communications circuit transmit data & gate control pin	High	Hi-Z (low)
CCS_BS1	RP02	I	Baud rate setting switch input pin	-	Hi-Z (high)
CCS_BS2	RP03	I			
CCS_BS4	RP04	I			
CCS_BS8	RP05	I			
CCS_FUSEZ	P42	I	Fuse cutting signal input pin	Low	
CCM_CLK80M[Note]	-	I	CC-Link clock input (80 MHz)	-	-

Note: This pin is shared with CC-Link (intelligent device station).

2.1.13 System Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
XT1	-	I	Clock input pin OSCTH = 1: Oscillator is in use. XT1 and XT2 are respectively connected to GND and oscillator. OSCTH = 0: Resonator is in use. XT1 and XT2 are connected to resonator.	-	-
XT2	-	I/O			
RESETZ	-	I	Reset input	Low	
PONRZ	-	I	Power-on reset input		
HOTRESETZ	-	I	Hot reset input		
OSCTH	-	I	External clock input mode setting 0: Resonator connection mode 1: External clock input mode	High	
JTAGSEL	-	I	JTAG pin operating mode setting 0: Cortex-M4 JTAG mode 1: B-SCAN JTAG mode	-	
RSTOUTZ	-	O	External reset output	Low	Low
PLL_VDD	-	-	PLL power supply (1.0 V)	-	-
PLL_GND	-	-	PLL GND		
VDD33	-	-	I/O power supply (3.3 V)		
VDD10	-	-	Internal power supply (1.0 V)		
GND	-	-	Power supply ground voltage (GND)		

2.1.14 Trace Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
TRACECLK	-	O	Trace port clock output	-	Clock output
TRACEDATA3 Note	-		Trace port data output		Hi-Z (high)
TRACEDATA2 Note	-				
TRACEDATA1	-				
TRACEDATA0	-				

Note: This pin function is multiplexed with a pin function of the CC-Link IE Field.
For information on the multiplexed functions of the port pins, see section 2.1.10, CC-Link IE Field Pins.
The initial setting is for input and the pin is switched from input to output in 20 BUSCLK cycles after the RSTOUTZ pin has been de-asserted in response to release from the reset state.

2.1.15 CPU Power Control Pin

Function Name	Pin Name	I/O	Description	Active	Level during Reset
SLEEPING	P72	O	CPU core sleep mode output	High	Hi-Z (high)

2.1.16 Test Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
TMODE0-TMODE2	-	I	Test mode select pin	-	-
TMS		I/O	Mode select signal		
TDI		I	Serial data input		
TDO		O	Serial data output		
TRSTZ		I	Reset signal	Low	
TCK		I	Clock signal (JTAG clock)	-	
TMC1		I	Renesas test pin		
TMC2		I	Renesas test pin		
TEST1		I	Renesas test pin		
TEST2		I/O	Renesas test pin		
TEST3		I	Renesas test pin		
TEST4		I/O	Renesas test pin		
TEST5		I/O	Renesas test pin		
TEST6		I	Renesas test pin		

2.1.17 Operating Mode Setting Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
BOOT1-BOOT0	-	I	Boot mode selection 00: External memory boot 01: External serial flash ROM boot 10: External MCU boot 11: Instruction RAM boot (only available for debugging)	-	-
MEMIFSEL	-	I	External memory interface selection 0: Slave memory interface 1: External MCU interface		
MEMCSEL	-	I	Internal memory controller selection 0: Asynchronous SRAM memory controller 1: Synchronous burst access memory controller		
BUS32EN	-	I	External memory interface bus width selection 0: 16-bit bus 1: 32-bit bus		
HIFSYNC	-	I	External MCU interface operating mode selection 0: Asynchronous SRAM interface 1: Synchronous SRAM Interface		
HWRZSEL	-	I	External MCU interface HWRZ/HBENZ selection 0: Used as HBENZ 1: Used as HWRZ		
ADMUXMODE	-	I	Multiplexing of address and data lines 0: Separate address and data lines 1: Multiplexed address and data lines		

The combinations of available operating mode setting pins in this product are as follows.

Boot Mode	External Memory Boot				External MCU Boot				External Serial Flash ROM Boot							
External memory interface	Slave memory interface				External MCU interface				Slave memory interface				External MCU interface			
MEMC type	Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous	
External bus width	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
BOOT1-0	00	00	00	00	10	10	10	10	01	01	01	01	01	01	01	01
MEMIFSEL	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
MEMCSEL	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
BUS32EN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HIFSYNC	0	0	0	0	Note 1	Note 1	1	1	0	0	0	0	Note 1	Note 1	1	1
HWRZSEL	0	0	0	0	Note 2	Note 2	0	0	0	0	0	0	Note 2	Note 2	0	0
ADMUXMODE	0	0	Note 3	Note 3	0	0	Note 3	Note 3	0	0	Note 3	Note 3	0	0	Note 3	Note 3

Caution: Any combination of operating mode setting pins other than the above is prohibited.

Notes 1. The mode of the external MCU interface is selectable by the level on the HIFSYNC pin.
HIFSYNC = 0: Asynchronous SRAM supported MCU connection mode
HIFSYNC = 1: Synchronous SRAM supported MCU connection mode
For details, see section 12, External MCU Interface, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

2. The external MCU interface HWRZ or HBENZ is selectable by the level on the HWRZSEL pin. For details, see section 2.1.3.2(a), When the asynchronous SRAM memory controller is selected (MEMCSEL=0).

3. Multiplexing of address and data lines is selectable by the level on the ADMUXMODE pin. For details, see section 2.1.3.1(b), When the synchronous burst access memory controller is selected (MEMCSEL = 1).

Remarks 1. The combination of operating-mode setting pins used to select booting for instruction RAM (BOOT1-0 = 11) is the same as that for booting from external memory (BOOT1-0 = 00).

2. Asynchronous: asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous: synchronous burst access memory controller (MEMCSEL = 1)

2.1.18 ADC Pins

Function Name	Pin Name	I/O	Description	Active	Level during Reset
ADTRG	RP02	I	A/D converter external conversion trigger input	-	Hi-Z (high)
ADTRGRDY	RP03	O	A/D converter external conversion trigger ready signal	-	Hi-Z (high)
AIN0-AIN7	-	I	A/D converter analog input	-	-
AVREFP	-	I	A/D converter reference voltage input (+)	-	-
AVREFM	-	I	A/D converter reference voltage input (-)	-	-
AVDD	-	I	Analog power supply for A/D converter. Connect to 3.3-V power supply.	-	-
AGND	-	I	Analog power supply for A/D converter. Connect to GND.	-	-

2.2 Pin States

The initial state of the port functions after release from the reset state differs depending on the state of the operating mode setting pins. For the state of the operating mode setting pins in each boot mode and the supported combinations, see section 2.1.17, Operating Mode Setting Pins.

Remarks 1. Entries in cells shaded in light green indicate multiplexed pin functions that are enabled in the initial state.

2. The initial state of booting for instruction RAM is the same as that for booting from external memory.

2.2.1 Pin States when Booting is from External Memory

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	P33	P33	P33	P33
P34	P34	P34	P34	P34
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P40	A1	P40	MA0	MA0
P41	P41	P41	P41	P41
P42	P42	P42	P42	P42
P43	P43	P43	P43	P43
P44	P44	P44	P44	P44
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P57	P57	P57	P57	P57
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77
EXTP0	EXTP0	EXTP0	EXTP0	EXTP0
EXTP1	EXTP1	EXTP1	EXTP1	EXTP1
EXTP2	EXTP2	EXTP2	EXTP2	EXTP2
EXTP3	EXTP3	EXTP3	EXTP3	EXTP3
EXTP4	EXTP4	EXTP4	EXTP4	EXTP4
EXTP5	EXTP5	EXTP5	EXTP5	EXTP5
EXTP6	EXTP6	EXTP6	EXTP6	EXTP6
EXTP7	EXTP7	EXTP7	EXTP7	EXTP7
EXTP8	EXTP8	EXTP8	EXTP8	EXTP8
EXTP9	EXTP9	EXTP9	EXTP9	EXTP9

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05
RP06	RP06	WRZ2	RP06	WRZ2
RP07	RP07	WRZ3	RP07	WRZ3
RP10	RP10	D24	RP10	MD24
RP11	RP11	D25	RP11	MD25
RP12	RP12	D26	RP12	MD26
RP13	RP13	D27	RP13	MD27
RP14	RP14	D28	RP14	MD28
RP15	RP15	D29	RP15	MD29
RP16	RP16	D30	RP16	MD30
RP17	RP17	D31	RP17	MD31
RP20	RP20	RP20	ADVZ	ADVZ
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16
RP31	RP31	D17	RP31	MD17
RP32	RP32	D18	RP32	MD18
RP33	RP33	D19	RP33	MD19
RP34	RP34	D20	RP34	MD20
RP35	RP35	D21	RP35	MD21
RP36	RP36	D22	RP36	MD22
RP37	RP37	D23	RP37	MD23

2.2.2 Pin States when Booting is from External Serial Flash ROM

Remark 1. Asynchronous type: asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous type: synchronous burst access memory controller (MEMCSEL = 1)
2. 16-bit: 16-bit bus width of the external memory interface (BUS32EN = 0)
32-bit: 32-bit bus width of the external memory interface (BUS32EN = 1)

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous type		Synchronous type		Asynchronous type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
P00	P00	P00	P00	P00	P00	P00	P00	P00
P01	P01	P01	P01	P01	P01	P01	P01	P01
P02	P02	P02	P02	P02	P02	P02	P02	P02
P03	P03	P03	P03	P03	P03	P03	P03	P03
P04	P04	P04	P04	P04	P04	P04	P04	P04
P05	P05	P05	P05	P05	P05	P05	P05	P05
P06	P06	P06	P06	P06	P06	P06	P06	P06
P07	P07	P07	P07	P07	P07	P07	P07	P07
P10	P10	P10	P10	P10	P10	P10	P10	P10
P11	P11	P11	P11	P11	P11	P11	P11	P11
P12	P12	P12	P12	P12	P12	P12	P12	P12
P13	P13	P13	P13	P13	P13	P13	P13	P13
P14	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK
P15	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0
P16	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1
P17	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ
P20	P20	P20	P20	P20	P20	P20	P20	P20
P21	P21	P21	P21	P21	P21	P21	P21	P21
P22	P22	P22	P22	P22	P22	P22	P22	P22
P23	P23	P23	P23	P23	P23	P23	P23	P23
P24	P24	P24	P24	P24	P24	P24	P24	P24
P25	P25	P25	P25	P25	P25	P25	P25	P25
P26	P26	P26	P26	P26	P26	P26	P26	P26
P27	P27	P27	P27	P27	P27	P27	P27	P27
P30	P30	P30	P30	P30	P30	P30	P30	P30
P31	P31	P31	P31	P31	P31	P31	P31	P31
P32	P32	P32	P32	P32	P32	P32	P32	P32
P33	P33	P33	P33	P33	P33	P33	P33	P33
P34	P34	P34	P34	P34	P34	P34	P34	P34
P35	P35	P35	P35	P35	P35	P35	P35	P35
P36	P36	P36	P36	P36	P36	P36	P36	P36
P37	P37	P37	P37	P37	P37	P37	P37	P37

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous type		Synchronous type		Asynchronous type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
P40	A1	P40	MA0	MA0	HA1	HA1	HA1	HA1
P41	P41	P41	P41	P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	P42	P42	P42	P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	P43	P43	P43	P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	P44	P44	P44	P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45	P45	P45	P45	P45
P46	P46	P46	P46	P46	P46	P46	P46	P46
P47	P47	P47	P47	P47	P47	P47	P47	P47
P50	P50	P50	P50	P50	P50	P50	P50	P50
P51	P51	P51	P51	P51	P51	P51	P51	P51
P52	P52	P52	P52	P52	P52	P52	P52	P52
P53	P53	P53	P53	P53	P53	P53	P53	P53
P54	P54	P54	P54	P54	P54	P54	P54	P54
P55	P55	P55	P55	P55	P55	P55	P55	P55
P56	P56	P56	P56	P56	P56	P56	P56	P56
P57	P57	P57	P57	P57	P57	P57	P57	P57
P60	P60	P60	P60	P60	P60	P60	P60	P60
P61	P61	P61	P61	P61	P61	P61	P61	P61
P62	P62	P62	P62	P62	P62	P62	P62	P62
P63	P63	P63	P63	P63	P63	P63	P63	P63
P64	P64	P64	P64	P64	P64	P64	P64	P64
P65	P65	P65	P65	P65	P65	P65	P65	P65
P66	P66	P66	P66	P66	P66	P66	P66	P66
P67	P67	P67	P67	P67	P67	P67	P67	P67
P70	P70	P70	P70	P70	P70	P70	P70	P70
P71	P71	P71	P71	P71	P71	P71	P71	P71
P72	P72	P72	P72	P72	P72	P72	P72	P72
P73	P73	P73	P73	P73	P73	P73	P73	P73
P74	P74	P74	P74	P74	P74	P74	P74	P74
P75	P75	P75	P75	P75	P75	P75	P75	P75
P76	P76	P76	P76	P76	P76	P76	P76	P76
P77	P77	P77	P77	P77	P77	P77	P77	P77

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous type		Synchronous type		Asynchronous type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
EXTP0	EXTP0	EXTP0	EXTP0	EXTP0	EXTP0	EXTP0	EXTP0	EXTP0
EXTP1	EXTP1	EXTP1	EXTP1	EXTP1	EXTP1	EXTP1	EXTP1	EXTP1
EXTP2	EXTP2	EXTP2	EXTP2	EXTP2	EXTP2	EXTP2	EXTP2	EXTP2
EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3
EXTP4	EXTP4	EXTP4	EXTP4	EXTP4	EXTP4	EXTP4	EXTP4	EXTP4
EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5
EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6
EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7
EXTP8	EXTP8	EXTP8	EXTP8	EXTP8	EXTP8	EXTP8	EXTP8	EXTP8
EXTP9	EXTP9	EXTP9	EXTP9	EXTP9	EXTP9	EXTP9	EXTP9	EXTP9

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous type		Synchronous type		Asynchronous type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05	RP05	RP05	RP05	RP05
RP06	RP06	WRZ2	RP06	WRZ2	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	WRZ3	RP07	WRZ3	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	D24	RP10	MD24	RP10	HD24	RP10	HD24
RP11	RP11	D25	RP11	MD25	RP11	HD25	RP11	HD25
RP12	RP12	D26	RP12	MD26	RP12	HD26	RP12	HD26
RP13	RP13	D27	RP13	MD27	RP13	HD27	RP13	HD27
RP14	RP14	D28	RP14	MD28	RP14	HD28	RP14	HD28
RP15	RP15	D29	RP15	MD29	RP15	HD29	RP15	HD29
RP16	RP16	D30	RP16	MD30	RP16	HD30	RP16	HD30
RP17	RP17	D31	RP17	MD31	RP17	HD31	RP17	HD31
RP20	RP20	RP20	ADVZ	ADVZ	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16	RP30	HD16	RP30	HD16
RP31	RP31	D17	RP31	MD17	RP31	HD17	RP31	HD17
RP32	RP32	D18	RP32	MD18	RP32	HD18	RP32	HD18
RP33	RP33	D19	RP33	MD19	RP33	HD19	RP33	HD19
RP34	RP34	D20	RP34	MD20	RP34	HD20	RP34	HD20
RP35	RP35	D21	RP35	MD21	RP35	HD21	RP35	HD21
RP36	RP36	D22	RP36	MD22	RP36	HD22	RP36	HD22
RP37	RP37	D23	RP37	MD23	RP37	HD23	RP37	HD23

2.2.3 Pin States when Booting is for External MCU

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	P33	P33	P33	P33
P34	P34	P34	P34	P34
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P40	HA1	HA1	HA1	HA1
P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P67	P67	P67	P67	P67
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77
EXTP0	EXTP0	EXTP0	EXTP0	EXTP0
EXTP1	EXTP1	EXTP1	EXTP1	EXTP1
EXTP2	EXTP2	EXTP2	EXTP2	EXTP2
EXTP3	EXTP3	EXTP3	EXTP3	EXTP3
EXTP4	EXTP4	EXTP4	EXTP4	EXTP4
EXTP5	EXTP5	EXTP5	EXTP5	EXTP5
EXTP6	EXTP6	EXTP6	EXTP6	EXTP6
EXTP7	EXTP7	EXTP7	EXTP7	EXTP7
EXTP8	EXTP8	EXTP8	EXTP8	EXTP8
EXTP9	EXTP9	EXTP9	EXTP9	EXTP9

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05
RP06	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	HD24	RP10	HD24
RP11	RP11	HD25	RP11	HD25
RP12	RP12	HD26	RP12	HD26
RP13	RP13	HD27	RP13	HD27
RP14	RP14	HD28	RP14	HD28
RP15	RP15	HD29	RP15	HD29
RP16	RP16	HD30	RP16	HD30
RP17	RP17	HD31	RP17	HD31
RP20	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	HD16	RP30	HD16
RP31	RP31	HD17	RP31	HD17
RP32	RP32	HD18	RP32	HD18
RP33	RP33	HD19	RP33	HD19
RP34	RP34	HD20	RP34	HD20
RP35	RP35	HD21	RP35	HD21
RP36	RP36	HD22	RP36	HD22
RP37	RP37	HD23	RP37	HD23

2.3 Operating Mode Monitoring

The levels on the operating mode setting pins can be confirmed by using the operating mode monitoring register.
The table below lists the operating mode setting pins for which the settings can be checked.

For details of the operating mode monitoring register, refer to section 25.2, Operating Mode Monitor Register, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

Table 2.3 Operating Mode Setting Pins for which the Settings can be Checked

Pin Name	Function
BUS32EN	Selects the bus width when the external memory interface is started
MEMIFSEL	Selects the type of external memory interface
HIFSYNC	Sets the operating mode of the external MCU interface
HWRZSEL	Selects HWRZ or HBENZ of the external MCU interface
JTAGSEL	Sets the operating mode of JTAG pins
OSCTH	Sets the external clock input mode
BOOT0, BOOT1	Selects boot mode
MEMCSEL	Selects the internal memory controller
ADMUXMODE	Multiplexing of address and data lines

2.4 Buffer Switching

The driving ability and use of a pull-up or pull-down resistor is programmable for real-time and general-purpose port pins (with some exceptions).
The former function provides stable operation in systems with large loads by providing the ability to raise the driving ability.
Use the buffer-switching registers (DRCTL) to change the output buffers as required.

For details of the buffer switching registers, see section 7.5, Buffer Switching Registers (DRCTL), in this manual.

2.5 Buffer Type of Pins and Handling of Unused Pins

2.5.1 Port Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
P00-P07, P20-P21,P25-P26, P32-P33 P50, P66, RP00-RP37	I/O	Programmable I/O buffer (3.3V) Driving ability selection (6mA,12mA) Resistor selection (pull-up or pull-down or less)	Open
P10-P17, P22-P24,P27, P30-P31,P34-P37, P40-P47, P51-P52,P57, P60-P65,P67, P70-P77, EXTP0-EXTP9	I/O	Programmable I/O buffer (3.3V)(6mA) Resistor selection (pull-up or pull-down or less)	
P53-P56	I/O	5 V-tolerant I/O buffer 4 mA 50 kΩ pull-up	

2.5.2 Ethernet Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
P0_D0N	I/O	Management data interface (analog)	Open
P0_D0P	I/O	Management data interface (analog)	Open
P0_D1N	I/O	Management data interface (analog)	Open
P0_D1P	I/O	Management data interface (analog)	Open
P0_D2N	I/O	Management data interface (analog)	Open
P0_D2P	I/O	Management data interface (analog)	Open
P0_D3N	I/O	Management data interface (analog)	Open
P0_D3P	I/O	Management data interface (analog)	Open
P1_D0N	I/O	Management data interface (analog)	Open
P1_D0P	I/O	Management data interface (analog)	Open
P1_D1N	I/O	Management data interface (analog)	Open
P1_D1P	I/O	Management data interface (analog)	Open
P1_D2N	I/O	Management data interface (analog)	Open
P1_D2P	I/O	Management data interface (analog)	Open
P1_D3N	I/O	Management data interface (analog)	Open
P1_D3P	I/O	Management data interface (analog)	Open
PHYADD1	I	Device SMI Address bit 1 (with PD resistance)	Open
PHYADD2	I	Device SMI Address bit 2 (with PD resistance)	Open
PHYADD3	I	Device SMI Address bit 3 (with PD resistance)	Open
PHYADD4	I	Device SMI Address bit 4 (with PD resistance)	Open
REF_FILT	I/O	Copper media reference filter pin.	Connect the pin to GND via an external 1-μF capacitor. Handle the pin in this way at all times.
REF_REXT	I/O	Copper media reference external pin.	Connect the pin to GND via an external 2.0 kΩ (1%) resistor. Handle the pin in this way at all times.
VDD1	-	1.0-V internal power supply	Connect to VDD (1.0 V)
VDD1A	-	1.0-V analog power requiring additional PCB power supply filtering	Connect to VDD (1.0 V)
VDD25A	-	2.5-V general analog power supply	Connect to VDD (2.5 V)
VDD33_GPHY	-	3.3-V general I/O power supply	Connect to VDD (3.3 V)
PHY0_LED0	O	GbE-PHY LED0_PHY0 output signal Output Buffer (3.3V) 3mA	Open
PHY1_LED0	O	GbE-PHY LED0_PHY1 output signal Output Buffer (3.3V) 3mA	Open

2.5.3 External SRAM and External MCU Interface Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
BUSCLK	O	Output buffer (3.3 V) 9 mA	Open
CSZ0	I/O	I/O buffer (3.3 V) 6 mA 50 kΩ pull-up	Open
A2-A20	I/O	I/O buffer (3.3 V) 6 mA 50 kΩ pull-down	Open
D0-D15			
RDZ	I/O	I/O buffer (3.3 V) 6 mA 50 kΩ pull-up	Open
WRSTBZ			
WRZ0, WRZ1			

2.5.4 External Interrupt Input Pin

Pin Name	I/O	Interface	Recommended Connection when Not in Use
NMIZ	I	Input Buffer (3.3 V) Schmitt in 50 kΩ pull-up	Connect to VDD (3.3 V)

2.5.5 CC-Link IE Field Pin

Pin Name	I/O	Interface	Recommended Connection when Not in Use
CCI_CLK2_097M	I	Input buffer (3.3 V)	Connect to GND

2.5.6 CC-Link Master (Intelligent Device Station) Pin

Pin Name	I/O	Interface	Recommended Connection when Not in Use
CCM_CLK80M	I	Input buffer (3.3 V)	Connect to GND

2.5.7 System Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
XT1	I	Oscillator with EN	Note
XT2	I/O		
RSTOUTZ	O	Output buffer (3.3 V) 6 mA	Open
RESETZ	I	Input buffer (3.3 V) Schmitt in	Connect a reset signal since these pins are always used.
PONRZ			
HOTRESETZ			Connect to VDD (3.3 V)
OSCTH	I	Input buffer (3.3 V) Schmitt in, 50 kΩ pull-down	Set these pins according to the operating mode
JTAGSEL			
PLL_VDD	-	PLL power supply (1.0 V)	Connect to VDD (1.0 V)
PLL_GND	-	PLL power ground supply (GND)	Connect to GND
VDD33	-	I/O power supply (3.3 V)	Connect to VDD (3.3 V)
VDD10	-	Internal power supply (1.0 V)	Connect to VDD (1.0 V)
GND	-	Power supply ground voltage (GND)	Connect to GND

Note: The pin connection differs depending on the setting of the OSCTH pin.
For details, see the R-IN32M4-CL2 Series User's Manual (Board design edition).

2.5.8 Trace Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
TRACECLK	O	Output buffer (3.3 V) 6 mA	Open
TRACEDATA3-TRACEDATA0	I/O	Programmable I/O buffer (3.3 V) (6 mA) 50 kΩ pull-up	

2.5.9 Test Pins

Pin Name	I/O	Interface	Required Connection when Not in Use
TMODE0-TMODE2	I	Input buffer (3.3 V) Schmitt in, 50 kΩ pull-down	Connect to GND
TMS	I/O	I/O buffer (3.3 V) 6mA, 25 kΩ pull-up	Open
TDI	I	Input buffer (3.3 V), 25 kΩ pull-up	Open
TDO	O	3-state output buffer (3.3 V) 6mA	Open
TRSTZ	I	Input buffer (3.3 V), Schmitt in, 50 kΩ pull-up	Open
TCK	I	Input buffer (3.3 V), 25 kΩ pull-up	Open
TMC1	I	(TMC1) input buffer (3.3 V) for TMC terminal	Connect to GND
TMC2	I	(TMC2) input buffer (3.3 V) for TMC terminal	Connect to GND
TEST1	I	Renesas test signal	Connect to GND
TEST2	I/O	Renesas test signal	Open
TEST3	I	Renesas test signal	Connect to VDD (3.3 V)
TEST4	I/O	Renesas test signal	Open
TEST5	I/O	Renesas test signal	Open
TEST6	I	Renesas test signal	Connect to GND

2.5.10 Operating Mode Setting Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
BOOT0, BOOT1	I	Input buffer (3.3 V) Schmitt in	Set these pins according to the operating mode
MEMIFSEL			
BUS32EN			
HIFSYNC			
HWRZSEL			
MEMCSEL			
ADMUXMODE			

2.5.11 ADC Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
AIN0-AIN7	I	Analog	Open
AVREFP			Connect to VDD (3.3 V)
AVREFM			Connect to GND
AVDD			Connect to VDD (3.3 V)
AGND			Connect to GND

3. Memory Maps

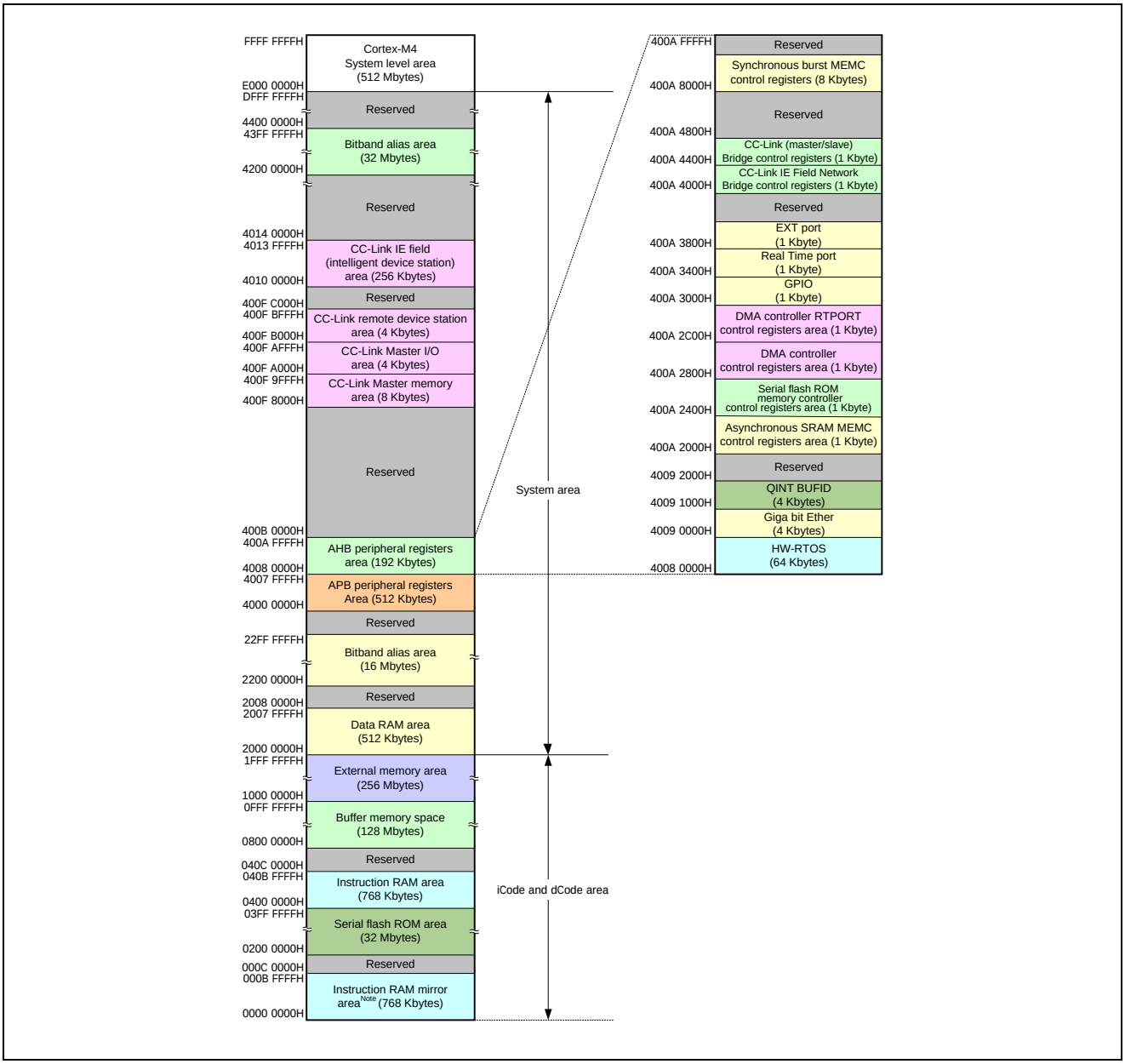

Figure 3.1 Entire Memory Map

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

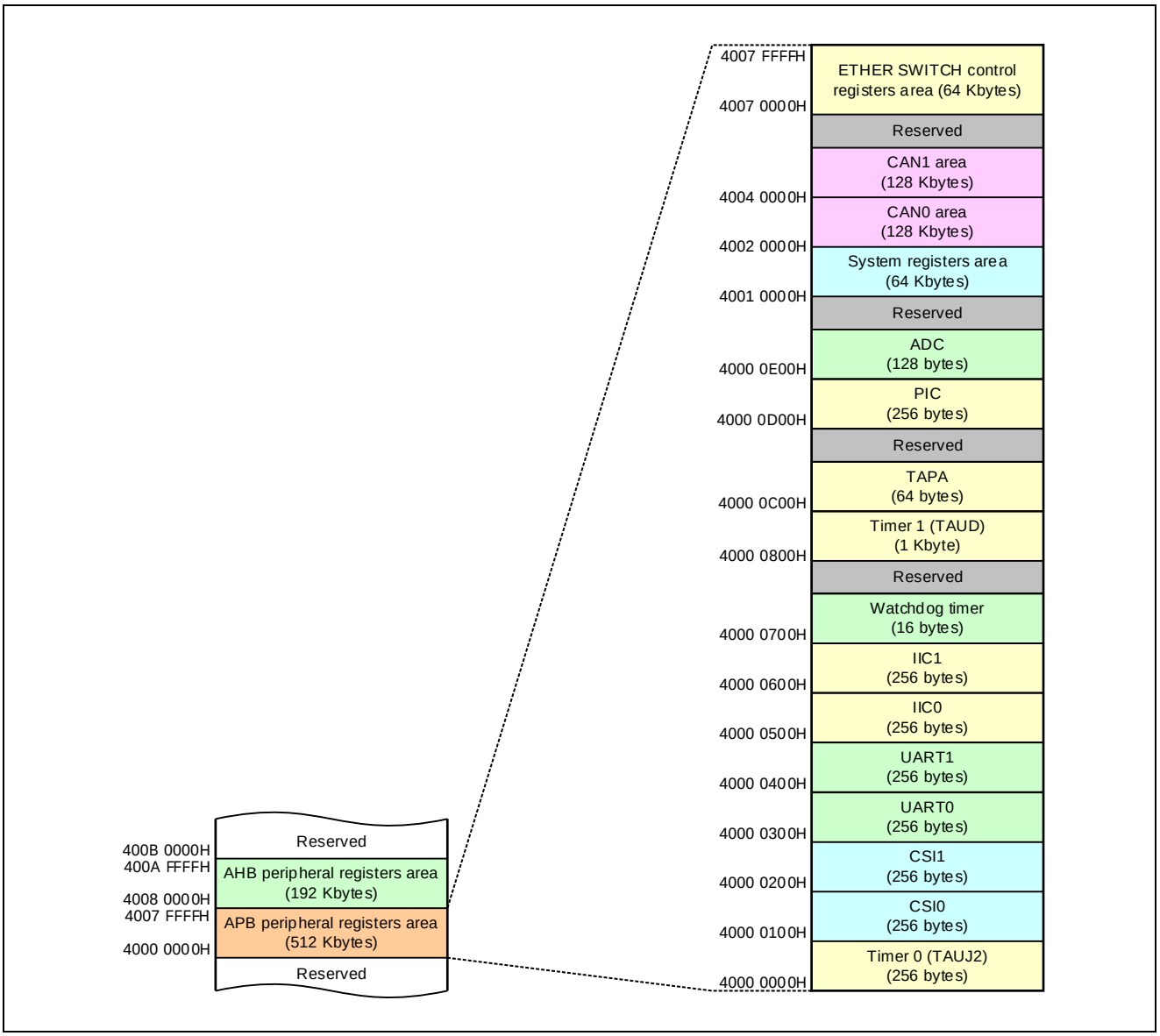

Figure 3.2 Memory Map (APB Peripheral Registers Area)

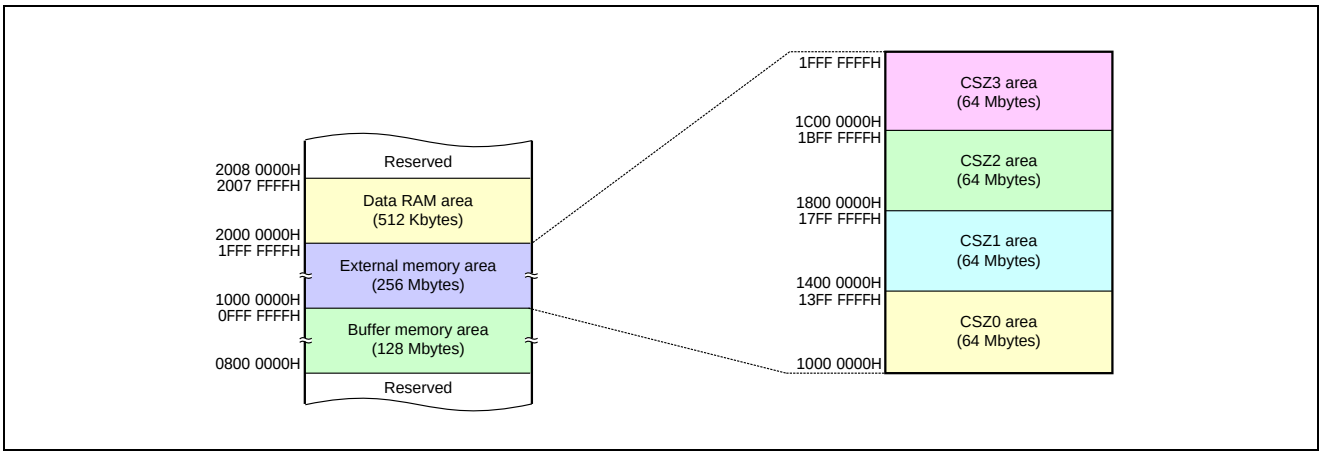

Figure 3.3 Memory Map (External Memory Area)

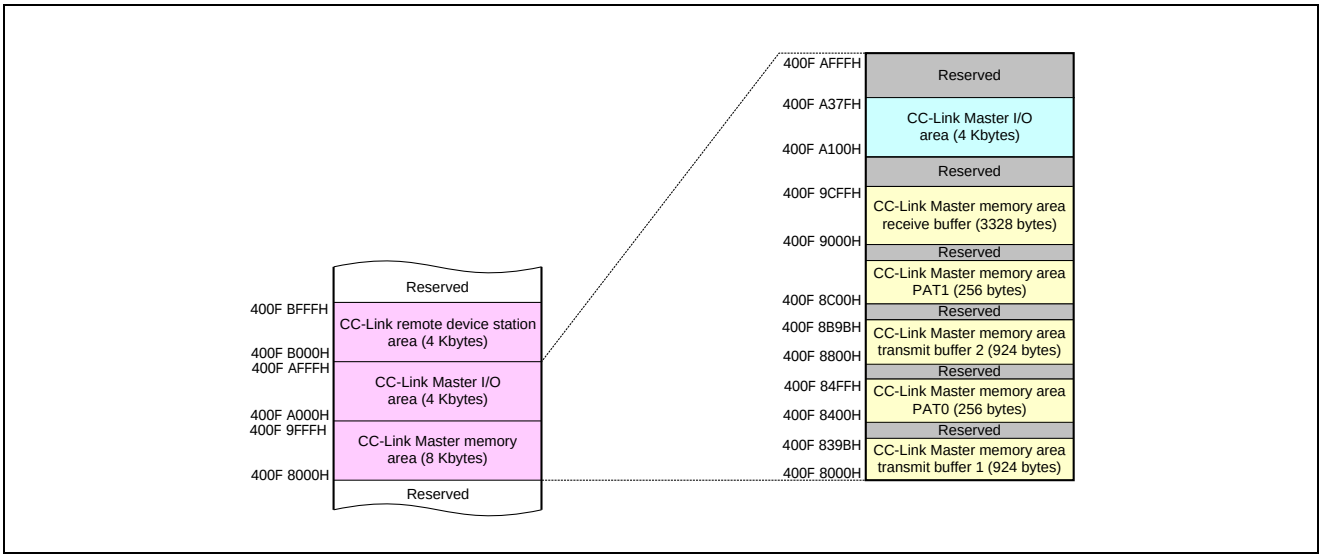

Figure 3.4 Memory Map (CC-Link Master Area)

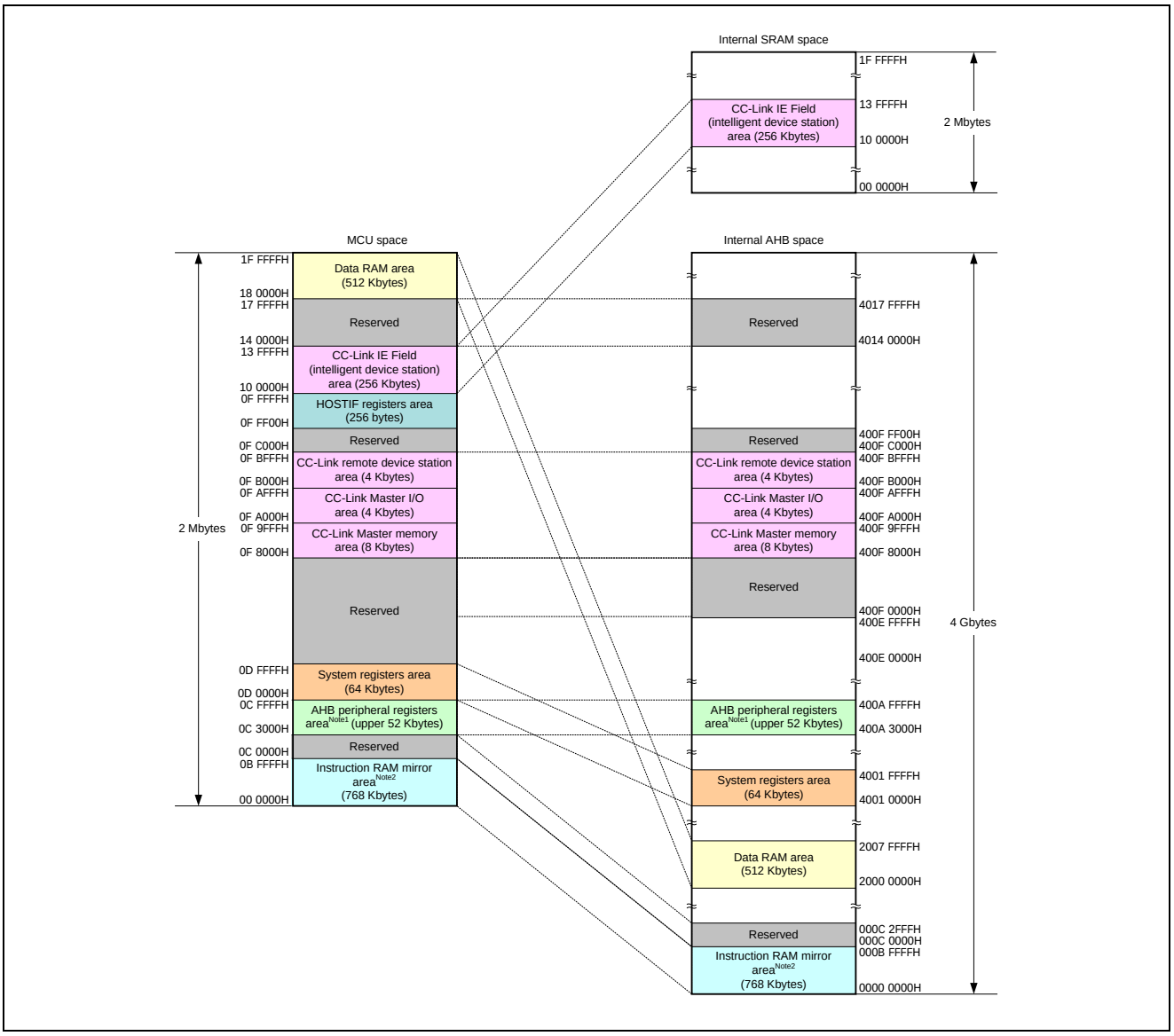

Figure 3.5 External MCU Interface Space

Notes 1. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers. For details, see Figure 3.1, Entire Memory Map.

2. The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory Map in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

BOOT1	BOOT0	Boot Mode	Access Destination Area	Remarks
0	0	External memory boot	—	External MCU interface is disabled
0	1	External serial flash ROM boot	Reserved	Access disabled
1	0	External MCU boot	Instruction RAM area	—
1	1	Instruction RAM boot	Instruction RAM area	Enabled only for debugging

4. Exception Handling

The R-IN32M4 uses the interrupt controller of Cortex-M4.
For Cortex-M4 exception handling operations, see the following Arm website.
http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.set.cortexm/index.html

4.1 List of Exceptions

Exception numbers 1 to 15 are system exceptions for the Cortex-M4 CPU. Interrupts from the internal hardware of the R-IN32M4 and external pins are assigned to exception number 16 and higher exception numbers.

Exception No.	Exception Type	Priority	Description
1	Reset	-3 (highest)	- Input on the reset pins (RESETZ, PONRZ, HOTRESETZ) - Reset by the watchdog timer - Setting the SYSRESETREQ bit in NVIC of the Cortex-M4 CPU to 1 - Reset by the SYSRESET register
2	NMI	-2	- Input on the NMI pin - Generation of NMI by the watchdog timer
3	Hard fault	-1	All classes of exceptions that no other exception handler can handle. Used to call up a response to a fault.
4	Memory management fault	Programmable	Exception from the MPU
5	Bus fault	Programmable	Bus error in access through the bus to the area outside the scope of management by the MPU
6	Usage fault	Programmable	Error in instruction execution, including the execution of an undefined instruction
7-10	Reserved	-	-
11	SVCall	Programmable	System service call by an SVC instruction
12	Debug monitor	Programmable	Debug monitor
13	Reserved	-	-
14	PendSV	Programmable	Request for system service that can be kept pending
15	SysTick	Programmable	Indication from the system timer
16-	R-IN32M4-CL2 specific interrupt	Programmable	Interrupt from the internal hardware of the R-IN32M4-CL2 and external pins

4.2 List of Interrupts

The interrupts below are the exceptions (interrupts) with exception numbers 16 and higher, which are assigned to the NVIC of the Cortex-M4 CPU.
In the R-IN32M4-CL2, interrupts from the internal hardware and external pins are connected not only to the NVIC of the Cortex-M4 but also to the internal hardware real-time OS (HW-RTOS), trigger for starting the internal DMA controllers (common to both the general-purpose DMAC and real-time port DMAC), and timers.

The R-IN32M4-CL2 supports the following interrupts.

Table 4.1 List of Interrupts

(1/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer TAUJ2 /TAUD
16	INTTAUJ2I0	TAUJ2 channel 0 interrupt	✓	✓	✓	✓	✓
17	INTTAUJ2I1	TAUJ2 channel 1 interrupt	✓	✓	✓	✓	✓
18	INTTAUJ2I2	TAUJ2 channel 2 interrupt	✓	✓	✓	✓	✓
19	INTTAUJ2I3	TAUJ2 channel 3 interrupt	✓	✓	✓	✓	✓
20	INTUAJ0TIT	UARTJ0 transmission interrupt	✓	✓	✓	✓	✓
21	INTUAJ0TIR	UARTJ0 reception interrupt	✓	✓	✓	✓	✓
22	INTUAJ1TIT	UARTJ1 transmission interrupt	✓	✓	✓	✓	✓
23	INTUAJ1TIR	UARTJ1 reception interrupt	✓	✓	✓	✓	✓
24	INTCSIH0IC	CSIH0 communication status interrupt	✓	✓	✓	✓	✓
25	INTCSIH0IR	CSIH0 reception status interrupt	✓	✓	✓	✓	✓
26	INTCSIH0IJC	CSIH0 job completion interrupt	✓	✓	✓	✓	✓
27	INTCSIH1IC	CSIH1 communication status interrupt	✓	✓	✓	✓	✓
28	INTCSIH1IR	CSIH1 reception status interrupt	✓	✓	✓	✓	✓
29	INTCSIH1IJC	CSIH1 job completion interrupt	✓	✓	✓	✓	✓
30	INTIICB0TIA	IICB0 data transmission/reception interrupt	✓	✓	✓	✓	✓
31	INTIICB1TIA	IICB1 data transmission/reception interrupt	✓	✓	✓	✓	✓
32	INTFCN0REC	FCN0 reception completion interrupt	✓	✓	✓	✓	✓
33	INTFCN0TRX	FCN0 transmission completion interrupt	✓	✓	✓	✓	✓
34	INTFCN0WUP	FCN0 sleep and wakeup/transmission suspension interrupt	✓	✓	✓	✓	✓
35	INTFCN1REC	FCN1 reception completion interrupt	✓	✓	✓	✓	✓
36	INTFCN1TRX	FCN1 transmission completion interrupt	✓	✓	✓	✓	✓
37	INTFCN1WUP	FCN1 sleep and wakeup/transmission suspension interrupt	✓	✓	✓	✓	✓
38	INTDMA00	General DMAC channel 0 transfer completion interrupt	✓	✓	✓	✓	✓
39	INTDMA01	General DMAC channel 1 transfer completion interrupt	✓	✓	✓	✓	✓
40	INTDMA02	General DMAC channel 2 transfer completion interrupt	✓	✓	✓	✓	✓
41	INTDMA03	General DMAC channel 3 transfer completion interrupt	✓	✓	✓	✓	✓
42	INTRTDMA	Real-time port DMAC transfer completion interrupt	✓	✓	✓	✓	✓
43	INTTAUDI0	TAUD channel 0 interrupt	✓	✓	✓	✓	✓
44	INTTAUDI1	TAUD channel 1 interrupt	✓	✓	✓	✓	✓
45	INTTAUDI2	TAUD channel 2 interrupt	✓	✓	✓	✓	✓

✓: Connectable -: Not used

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer TAUJ2 /TAUD
46	INTTAUDI3	TAUD channel 3 interrupt	✓	✓	✓	✓	✓
47	INTTAUDI4	TAUD channel 4 interrupt	✓	✓	✓	✓	✓
48	INTBUFDMA	Inter-buffer DMA transfer completion interrupt	✓	✓	✓	✓	✓
49	INTETHPHY0	Gigabit Ethernet PHY Port0 interrupt	✓	✓	✓	✓	✓
50	INTETHPHY1	Gigabit Ethernet PHY Port1 interrupt	✓	✓	✓	✓	✓
51	INTETHMIICMP	Ethernet MII management access completion interrupt	✓	✓	✓	✓	✓
52	INTETHPAUSECMP	Ethernet pause packet transmission completion interrupt	✓	✓	✓	✓	✓
53	INTETHTXCMP	Ethernet transmission completion interrupt	✓	✓	✓	✓	✓
54	INTETHSW	Ethernet SWITCH Timer interrupt	✓	✓	✓	✓	✓
55	INTETHSWDLR	Ethernet SWITCH DLR interrupt	✓	✓	✓	✓	✓
56	INTETHSWSYNC	Ethernet SWITCH SYNC interrupt	✓	✓	✓	✓	✓
57	INTETHRXFIFO	RX FIFO overflow interrupt	✓	✓	-	-	-
58	INTETHTXFIFO	TX FIFO underflow interrupt	✓	✓	-	-	-
59	INTETHRXDMA	Ethernet MACDMA reception completion interrupt	✓	✓	✓	✓	✓
60	INTETHTXDMA	Ethernet MACDMA transmission completion interrupt	✓	✓	✓	✓	✓
61	INTMACDMARXFRM	Receive frame successful interrupt	✓	✓	✓	✓	✓
62	-	Reserved	-	-	-	-	-
63	INTPZ0	INTPZ0 input	✓	✓	✓	✓	✓
64	INTPZ1	INTPZ1 input	✓	✓	✓	✓	✓
65	INTPZ2	INTPZ2 input	✓	✓	✓	✓	✓
66	INTPZ3	INTPZ3 input	✓	✓	✓	✓	✓
67	INTPZ4	INTPZ4 input	✓	✓	✓	✓	✓
68	INTPZ5	INTPZ5 input	✓	✓	✓	✓	✓
69	INTPZ6	INTPZ6 input	✓	✓	✓	✓	✓
70	INTPZ7	INTPZ7 input	✓	✓	✓	✓	✓
71	INTPZ8	INTPZ8 input	✓	✓	✓	✓	✓
72	INTPZ9	INTPZ9 input	✓	✓	✓	✓	✓
73	INTPZ10	INTPZ10 input	✓	✓	✓	✓	✓
74	INTPZ11	INTPZ11 input/TAUD channel 5 interrupt Note	✓	✓	✓	✓	✓
75	INTPZ12	INTPZ12 input/TAUD channel 6 interrupt Note	✓	✓	✓	✓	✓
76	INTPZ13	INTPZ13 input/TAUD channel 7 interrupt Note	✓	✓	✓	✓	✓
77	INTPZ14	INTPZ14 input/TAUD channel 8 interrupt Note	✓	✓	✓	✓	✓

✓: Connectable -: Not used

Note: This is selected by the INTSEL register.
For details, see section 25.19, INTPZ/Timer interrupt Select Register (INTSEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer TAUJ2 /TAUD
78	INTPZ15	INTPZ15 input/TAUD channel 9 interrupt Note	✓	✓	✓	✓	✓
79	INTPZ16	INTPZ16 input/TAUD channel 10 interrupt Note	✓	✓	✓	✓	✓
80	INTPZ17	INTPZ17 input/TAUD channel 11 interrupt Note	✓	✓	✓	✓	✓
81	INTPZ18	INTPZ18 input/TAUD channel 12 interrupt Note	✓	✓	✓	✓	✓
82	INTPZ19	INTPZ19 input/TAUD channel 13 interrupt Note	✓	✓	✓	✓	✓
83	INTPZ20	INTPZ20 input/TAUD channel 14 interrupt Note	✓	✓	✓	✓	✓
84	INTPZ21	INTPZ21 input/TAUD channel 15 interrupt Note	✓	✓	✓	✓	✓
85	INTPZ22	INTPZ22 input/peak interrupt (TAPA) Note	✓	✓	✓	✓	✓
86	INTPZ23	INTPZ23 input/trough interrupt (TAPA) Note	✓	✓	✓	✓	✓
87	INTPZ24	INTPZ24 input	✓	✓	✓	✓	✓
88	INTPZ25	INTPZ25 input	✓	✓	✓	✓	✓
89	INTPZ26	INTPZ26 input	✓	✓	✓	✓	✓
90	INTPZ27	INTPZ27 input	✓	✓	✓	✓	✓
91	INTPZ28	INTPZ28 input	✓	✓	✓	✓	✓
92	INTHWRTOS	HW-RTOS interrupt	✓	-	-	-	-
93	INTBRAMERR	Buffer RAM area access error interrupt	✓	✓	-	-	-
94	INTIICB0TIS	IICB0 status interrupt	✓	✓	-	-	-
95	INTIICB1TIS	IICB1 status interrupt	✓	✓	-	-	-
96	INTWDTA	WDT alarm interrupt (including the 75% of timeout interrupt)	✓	✓	-	-	-
97	INTSFLASH	Serial flash ROM controller error interrupt	✓	✓	-	-	-
98	INTUAJ0TIS	UARTJ0 status interrupt	✓	✓	-	-	-
99	INTUAJ1TIS	UARTJ1 status interrupt	✓	✓	-	-	-
100	INTCSIH0IRE	CSIH0 communication error interrupt	✓	✓	-	-	-
101	INTCSIH1IRE	CSIH1 communication error interrupt	✓	✓	-	-	-
102	INTFCN0ERR	FCN0 error detection interrupt	✓	✓	-	-	-
103	INTFCN1ERR	FCN1 error detection interrupt	✓	✓	-	-	-
104	INTDERR0	General DMAC error response interrupt	✓	✓	-	-	-
105	INTDERR1	Real-time port DMAC error response interrupt	✓	✓	-	-	-
106	INTETHTXFIFOERR	TX-FIFO error interrupt	✓	✓	-	-	-
107	INTETHRXERR	Ethernet reception frame error interrupt	✓	✓	-	-	-
108	INTETHRXDERR	MACDMA reception error interrupt	✓	✓	-	-	-
109	INTETHTXDERR	MACDMA transmission error interrupt	✓	✓	-	-	-
110	INTBUFDMAERR	Internal buffer DMA error interrupt	✓	✓	-	-	-

✓: Connectable -: Not used

Note: This is selected by the INTSEL register.
For details, see section 25.19, INTPZ/Timer interrupt Select Register (INTSEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer TAUJ2 /TAUD
111	INTLED0PHY0	Gigabit Ethernet PHY LED0_PHY0 input interrupt	✓	✓	✓	✓	✓
112	INTLED0PHY1	Gigabit Ethernet PHY LED0_PHY1 input interrupt	✓	✓	✓	✓	✓
113	-	Reserved	-	-	-	-	-
114	-	Reserved	-	-	-	-	-
115	IRAMECCSEC	Internal instruction RAM 1-bit ECC error correction interrupt	✓	-	-	-	-
116	DRAMECCSEC	Data RAM 1-bit ECC error correction interrupt	✓	-	-	-	-
117	BRAMECCSEC	Buffer RAM 1-bit ECC error correction interrupt	✓	-	-	-	-
118	IRAMECCDED	Internal instruction RAM 2-bit ECC error detection interrupt	✓	-	-	-	-
119	DRAMECCDED	Data RAM 2-bit ECC error detection interrupt	✓	-	-	-	-
120	BRAMECCDED	Buffer RAM 2-bit ECC error detection interrupt	✓	-	-	-	-
121	-	Reserved	-	-	-	-	-
122	-	Reserved	-	-	-	-	-
123	INTCCINMIZ	CC-Link IE Field NMIZ interrupt	✓	✓	✓	✓	✓
124	INTCCIWDTZ	CC-Link IE Field WDTZ interrupt	✓	✓	✓	✓	✓
125	INTCCIINTZ	CC-Link IE Field INTZ interrupt	✓	✓	✓	✓	✓
126	INTCCICLKLOSSZ	CC-Link IE Field CLKLOSSZ interrupt	✓	✓	✓	✓	✓
127	-	Reserved	-	-	-	-	-
128	-	Reserved	-	-	-	-	-
129	-	Reserved	-	-	-	-	-
130	-	Reserved	-	-	-	-	-
131	-	Reserved	-	-	-	-	-
132	INTCCSIRZ	CC-Link IRZ interrupt	✓	✓	✓	✓	✓
133	INTCCSREFSTB	CC-Link REFSTB interrupt	✓	✓	✓	✓	✓
134	INTCCSMON3	CC-Link MON3 interrupt	✓	✓	✓	✓	✓
135	-	Reserved	-	-	-	-	-
136	-	Reserved	-	-	-	-	-
137	INTGBEPHYFLF	Gigabit Ethernet PHY FASTLINK_FAIL interrupt	✓	✓	-	-	-
138	INTLED1PHY0	Gigabit Ethernet PHY LED1_PHY0 input interrupt	✓	✓	✓	✓	✓
139	INTLED1PHY1	Gigabit Ethernet PHY LED1_PHY1 input interrupt	✓	✓	✓	✓	✓
140	INTLED2PHY0	Gigabit Ethernet PHY LED2_PHY0 input interrupt	✓	✓	-	-	-
141	INTLED2PHY1	Gigabit Ethernet PHY LED2_PHY1 input interrupt	✓	✓	-	-	-
142	INTFPU	FPU interrupt	✓	✓	-	-	-
143	INTADC	AD conversion completion interrupt	✓	✓	✓	✓	✓

✓: Connectable -: Not used

5. Peripheral Modules

For details of the following peripheral modules, refer to the R-IN32M4-CL2 User's Manual: Peripheral Modules.

- Clocks and resets
- CPU and internal RAMs
- Bus structure
- Boot procedure
- Hardware real-time OS
- Gigabit Ethernet PHY
- Gigabit Ethernet MAC
- Ethernet switch
- Asynchronous SRAM memory controller (ROM/RAM)
- Synchronous burst access memory controller
- External MCU interface
- Serial flash ROM memory controller
- DMA function
- 32-bit timer array unit (TAUJ2)
- 16-bit timer array unit (TAUD)
- Motor control (TAPA/PIC)
- Window watchdog timer A (WDTA)
- Asynchronous serial interface J (UARTJ)
- Clocked serial interface H (CSIH)
- I^2C bus (IICB)
- CAN controller (FCN)
- 10-bit A/D converter
- CC-Link interface
- System registers (APB peripheral registers area)
- Debugging

6. CC-Link IE Field

The outline specifications of the CC-Link IE Field are as follows.
For detailed specifications on the CC-Link IE Field, see the following CC-Link Partner Association website.

http://www.cc-link.org/eng/cclink/cclinkie/index.html

Table 6.1 Outline Specifications of CC-Link IE Field

Item	Specification
Ethernet standard	IEEE802.3ab (1000BASE-T) compliant
Transfer rate	1 Gbps
Topology	Line, star, ring
Maximum number of connected units	254 modules
Maximum station-to-station distance	100 m

6.1 CC-Link IE Field Control Registers

These control registers are used to adjust the timing for access to the CC-Link IE Field by the CPU.

Table 6.2 Overview of the Bus Control Registers

Register Name	Symbol	Address
CC-Link IE Field bus size control register	CIEBSC	400A 4004H
CC-Link IE Field bus bridge control register	CIESMC	400A 4008H
CC-Link IE Field clock gate register	CIECLKGTD	BASE + 0938H

6.1.1 CC-Link IE Field Bus Size Control Register (CIEBSC)

The CIEBSC register is for setting the data bus width for access to the CC-Link IE Field. When using the CC-Link IE Field, set the bits of this register to 0000 FFFFH.

- Access This register can be read and written in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIEBSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CIEBSC15	CIEBSC14	CIEBSC13	CIEBSC12	CIEBSC11	CIEBSC10	CIEBSC9	CIEBSC8	CIEBSC7	CIEBSC6	CIEBSC5	CIEBSC4	CIEBSC3	CIEBSC2	CIEBSC1	CIEBSC0	400A 4004H Initial value 0000 FFFFH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
15 to 0	CIEBSC15-0	Set these bits to FFFFH.

6.1.2 CC-Link IE Field Bus Bridge Control Register (CIESMC)

The CIESMC register is used for access control. When using the CC-Link IE Field, be sure to set the bits of this register to 0000 0050H.

- Access This register can be read and written in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIESMC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CIESMC15	CIESMC14	CIESMC13	CIESMC12	CIESMC11	CIESMC10	CIESMC9	CIESMC8	CIESMC7	CIESMC6	CIESMC5	CIESMC4	CIESMC3	CIESMC2	CIESMC1	CIESMC0	400A 4008H Initial value 0000 FFFFH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
15 to 0	CIESMC15-0	Set these bits to 0050H.

6.1.3 CC-Link IE Field Clock Gate Register (CIECLKGTD)

The CIECLKGTD register is used to temporarily stop supply of the bus clock signal. This is to prevent the generation of a clock glitch when switching the bus clock signal from the CC-Link IE Field. Writing 1 to the effective bit of this register stops supply of the clock signal and writing 0 to it causes supply to resume. Before making the setting in the SRAM Bridge Select Register (SRAMBRSEL) to switch between the settings to enable the SRAM bus path from the system bus (AHB) and to enable the SRAM bus path from an external MCU, be sure to use this register to stop the bus clock signal. For details, see section 25.13, SRAM Bridge Select Register (SRAMBRSEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

- Access This register can be read and written in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIECLKGTD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CIECLKGTD	BASE + 0938H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	0000 0000H

Bit Position	Bit Name	Description
0	CIECLKGTD	This bit stops supply of the bus clock signal in the CC-Link IE Field. 0: Operating 1: Stopped

6.2 Usage Notes

On the CC-Link IE Field in the R-IN32M4-CL2, the watch dog time (WDT) counting in the CC-Link IE Field starts after the reset is released. Therefore, it is necessary to stop the WDT operation during initialization in program when the CC-Link IE Field is not used. Also, when using the debugger, it is necessary to stop the WDT in the CC-Link IE Field by the setup macro.

7. Port Functions

7.1 Features

- I/O port pins: 106
- Multiplexed with I/O pin functions of peripheral modules
- Input or output can be specified in bit units.

Cautions 1. Switching from a signal for a peripheral module that is multiplexed with a port pin to port mode by changing the multiplexed function might lead to a spike, depending on the state of the pin at the time.
The following general countermeasure for spikes should therefore be implemented in software.
- **Switch the pin function while the peripheral module is stopped.**
- **If the multiplexed pin function in use is an interrupt signal, clear the interrupt request flag and then remove masking of the interrupt.**
- **Only switch the mode after the output value is fixed.**

2. Do not externally apply an intermediate voltage to input buffers because these buffers do not implement through-current countermeasures.

7.2 Port Configuration

The R-IN32M4-CL2 incorporates twelve 8-bit ports and one 10-bit port (EXTP). Nine are general-purpose ports (including EXTP) and four are for real-time control.
Input or output can be specified for ports in 1-bit units. The basic structure of ports is the 8-bit unit, but ports P0x to P3x, P4x to P7x, RP0x to RP3x (x = 0 to 7), and EXTP0 to EXTP9 can also be grouped to enable reading and writing in 32-bit units. The real-time port pins (RP00 to RP37) can be used for input and output in synchronization with interrupt signals.

Each port has the registers listed below, which are used to make the I/O settings and to select and specify the multiplexed functions of the port pins. Figure 7.1 shows the basic circuit configuration of port registers and a port pin.

Register Name	Application and Operation	
	Read	Write
Port registers (Pn, RPm, EXTPp)	Used to read the value of the output latch.	Used to set a value to the output latch.
Port mode registers (PMn, RPMm, EXTPMp)	Used to read whether the port is in input or output mode.	Used to set the port to input or output mode.
Port mode control registers (PMCn, RPMCm, EXTPMCp)	Used to read whether the port pins are selected as port pins or as multiplexed function pins.	Used to select whether the port pins are used as port pins or as multiplexed function pins.
Port function control registers (PFCn, RPFCm, EXTPFCp)	Used to read which function is selected for the multiplexed pin.	Used to select the function of the multiplexed pin.
Port function control expansion registers (PFCEn, RPFCEm, EXTPFCEp)		
Port pin input registers (PINn, RPINm, EXTPINp)	Used to read the input level of the port pin.	Cannot be written.

Caution: Operation is not guaranteed if an unsupported function is allocated to the multiplexed pin. For example, if multiplexed function 2 is allocated to the P00 pin, which does not support multiplexed function 2, operation does not proceed correctly. For the allocation of multiplexed pins, see section 7.4, List of Selectable Multiplexed Functions.

Remark: n = 0 to 7; m = 0 to 3; p = 0 to 1

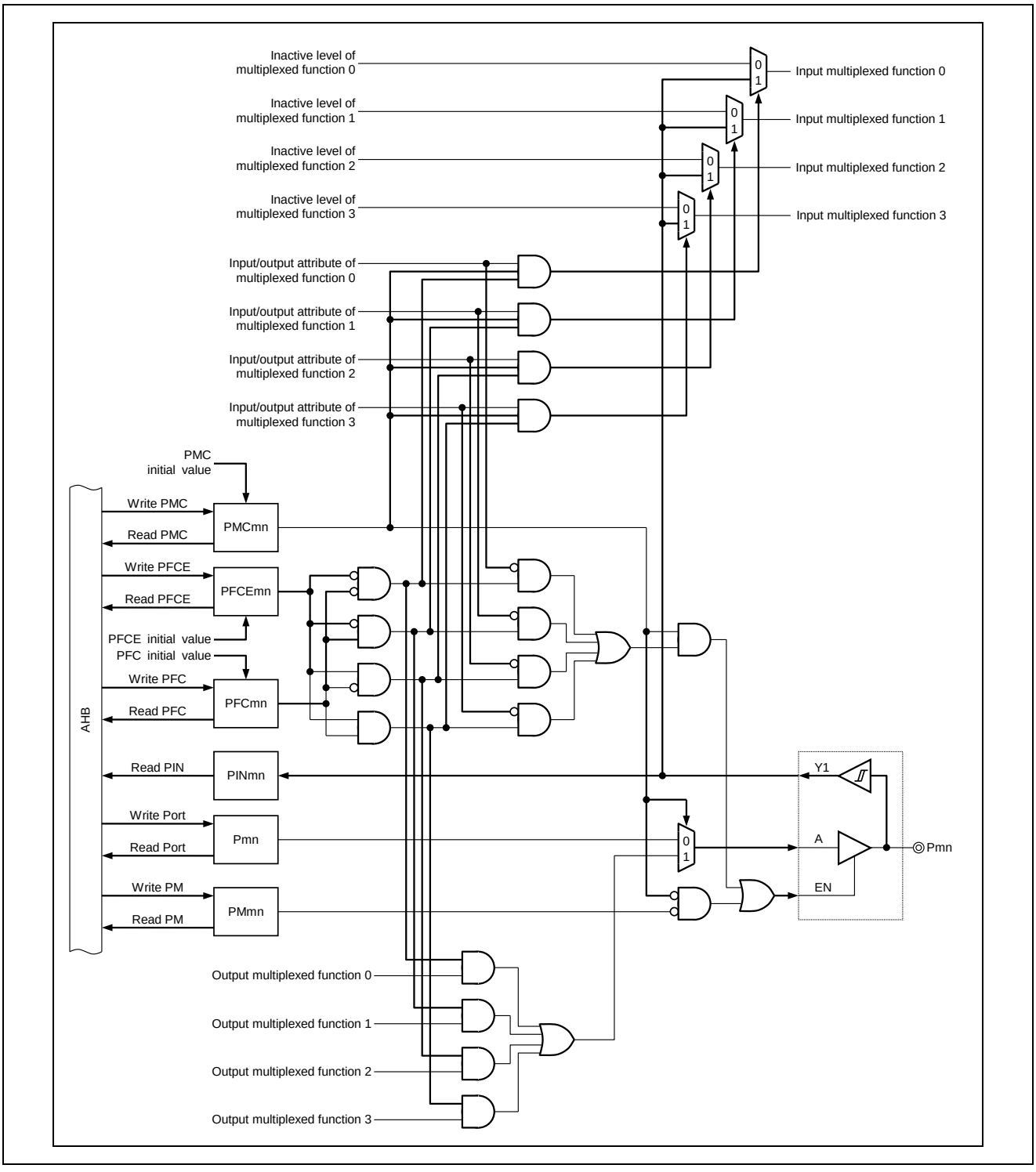

Figure 7.1 Basic Circuit Configuration of Ports

7.3 List of Registers

(1/7)

Register Name	Symbol	Address
Port register 0 (8 bits)	P0B	400A 3000H
Port register 1 (8 bits)	P1B	400A 3001H
Port register 2 (8 bits)	P2B	400A 3002H
Port register 3 (8 bits)	P3B	400A 3003H
Port register 4 (8 bits)	P4B	400A 3004H
Port register 5 (8 bits)	P5B	400A 3005H
Port register 6 (8 bits)	P6B	400A 3006H
Port register 7 (8 bits)	P7B	400A 3007H
Port register 0 (16 bits)	P0H	400A 3000H
Port register 2 (16 bits)	P2H	400A 3002H
Port register 4 (16 bits)	P4H	400A 3004H
Port register 6 (16 bits)	P6H	400A 3006H
Port register 0 (32 bits)	P0W	400A 3000H
Port register 4 (32 bits)	P4W	400A 3004H
Port mode register 0 (8 bits)	PM0B	400A 3010H
Port mode register 1 (8 bits)	PM1B	400A 3011H
Port mode register 2 (8 bits)	PM2B	400A 3012H
Port mode register 3 (8 bits)	PM3B	400A 3013H
Port mode register 4 (8 bits)	PM4B	400A 3014H
Port mode register 5 (8 bits)	PM5B	400A 3015H
Port mode register 6 (8 bits)	PM6B	400A 3016H
Port mode register 7 (8 bits)	PM7B	400A 3017H
Port mode register 0 (16 bits)	PM0H	400A 3010H
Port mode register 2 (16 bits)	PM2H	400A 3012H
Port mode register 4 (16 bits)	PM4H	400A 3014H
Port mode register 6 (16 bits)	PM6H	400A 3016H
Port mode register 0 (32 bits)	PM0W	400A 3010H
Port mode register 4 (32 bits)	PM4W	400A 3014H

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Register Name	Symbol	Address
Port mode control register 0 (8 bits)	PMC0B	400A 3020H
Port mode control register 1 (8 bits)	PMC1B	400A 3021H
Port mode control register 2 (8 bits)	PMC2B	400A 3022H
Port mode control register 3 (8 bits)	PMC3B	400A 3023H
Port mode control register 4 (8 bits)	PMC4B	400A 3024H
Port mode control register 5 (8 bits)	PMC5B	400A 3025H
Port mode control register 6 (8 bits)	PMC6B	400A 3026H
Port mode control register 7 (8 bits)	PMC7B	400A 3027H
Port mode control register 0 (16 bits)	PMC0H	400A 3020H
Port mode control register 2 (16 bits)	PMC2H	400A 3022H
Port mode control register 4 (16 bits)	PMC4H	400A 3024H
Port mode control register 6 (16 bits)	PMC6H	400A 3026H
Port mode control register 0 (32 bits)	PMC0W	400A 3020H
Port mode control register 4 (32 bits)	PMC4W	400A 3024H
Port function control register 0 (8 bits)	PFC0B	400A 3030H
Port function control register 1 (8 bits)	PFC1B	400A 3031H
Port function control register 2 (8 bits)	PFC2B	400A 3032H
Port function control register 3 (8 bits)	PFC3B	400A 3033H
Port function control register 4 (8 bits)	PFC4B	400A 3034H
Port function control register 5 (8 bits)	PFC5B	400A 3035H
Port function control register 6 (8 bits)	PFC6B	400A 3036H
Port function control register 7 (8 bits)	PFC7B	400A 3037H
Port function control register 0 (16 bits)	PFC0H	400A 3030H
Port function control register 2 (16 bits)	PFC2H	400A 3032H
Port function control register 4 (16 bits)	PFC4H	400A 3034H
Port function control register 6 (16 bits)	PFC6H	400A 3036H
Port function control register 0 (32 bits)	PFC0W	400A 3030H
Port function control register 4 (32 bits)	PFC4W	400A 3034H

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Register Name	Symbol	Address
Port function control expansion register 0 (8 bits)	PFCE0B	400A 3040H
Port function control expansion register 1 (8 bits)	PFCE1B	400A 3041H
Port function control expansion register 2 (8 bits)	PFCE2B	400A 3042H
Port function control expansion register 3 (8 bits)	PFCE3B	400A 3043H
Port function control expansion register 4 (8 bits)	PFCE4B	400A 3044H
Port function control expansion register 5 (8 bits)	PFCE5B	400A 3045H
Port function control expansion register 6 (8 bits)	PFCE6B	400A 3046H
Port function control expansion register 7 (8 bits)	PFCE7B	400A 3047H
Port function control expansion register 0 (16 bits)	PFCE0H	400A 3040H
Port function control expansion register 2 (16 bits)	PFCE2H	400A 3042H
Port function control expansion register 4 (16 bits)	PFCE4H	400A 3044H
Port function control expansion register 6 (16 bits)	PFCE6H	400A 3046H
Port function control expansion register 0 (32 bits)	PFCE0W	400A 3040H
Port function control expansion register 4 (32 bits)	PFCE4W	400A 3044H
Port pin input register 0 (8 bits)	PIN0B	400A 3050H
Port pin input register 1 (8 bits)	PIN1B	400A 3051H
Port pin input register 2 (8 bits)	PIN2B	400A 3052H
Port pin input register 3 (8 bits)	PIN3B	400A 3053H
Port pin input register 4 (8 bits)	PIN4B	400A 3054H
Port pin input register 5 (8 bits)	PIN5B	400A 3055H
Port pin input register 6 (8 bits)	PIN6B	400A 3056H
Port pin input register 7 (8 bits)	PIN7B	400A 3057H
Port pin input register 0 (16 bits)	PIN0H	400A 3050H
Port pin input register 2 (16 bits)	PIN2H	400A 3052H
Port pin input register 4 (16 bits)	PIN4H	400A 3054H
Port pin input register 6 (16 bits)	PIN6H	400A 3056H
Port pin input register 0 (32 bits)	PIN0W	400A 3050H
Port pin input register 4 (32 bits)	PIN4W	400A 3054H

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Register Name	Symbol	Address
RT port register 0 (8 bits)	RP0B	400A 3400H
RT port register 1 (8 bits)	RP1B	400A 3401H
RT port register 2 (8 bits)	RP2B	400A 3402H
RT port register 3 (8 bits)	RP3B	400A 3403H
RT port register 0 (16 bits)	RP0H	400A 3400H
RT port register 2 (16 bits)	RP2H	400A 3402H
RT port register 0 (32 bits)	RP0W	400A 3400H
RT port mode register 0 (8 bits)	RPM0B	400A 3410H
RT port mode register 1 (8 bits)	RPM1B	400A 3411H
RT port mode register 2 (8 bits)	RPM2B	400A 3412H
RT port mode register 3 (8 bits)	RPM3B	400A 3413H
RT port mode register 0 (16 bits)	RPM0H	400A 3410H
RT port mode register 2 (16 bits)	RPM2H	400A 3412H
RT port mode register 0 (32 bits)	RPM0W	400A 3410H
RT port mode control register 0 (8 bits)	RPMC0B	400A 3420H
RT port mode control register 1 (8 bits)	RPMC1B	400A 3421H
RT port mode control register 2 (8 bits)	RPMC2B	400A 3422H
RT port mode control register 3 (8 bits)	RPMC3B	400A 3423H
RT port mode control register 0 (16 bits)	RPMC0H	400A 3420H
RT port mode control register 2 (16 bits)	RPMC2H	400A 3422H
RT port mode control register 0 (32 bits)	RPMC0W	400A 3420H
RT port function control register 0 (8 bits)	RPFC0B	400A 3430H
RT port function control register 1 (8 bits)	RPFC1B	400A 3431H
RT port function control register 2 (8 bits)	RPFC2B	400A 3432H
RT port function control register 3 (8 bits)	RPFC3B	400A 3433H
RT port function control register 0 (16 bits)	RPFC0H	400A 3430H
RT port function control register 2 (16 bits)	RPFC2H	400A 3432H
RT port function control register 0 (32 bits)	RPFC0W	400A 3430H

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Register Name	Symbol	Address
RT port function control expansion register 0 (8 bits)	RPFCE0B	400A 3440H
RT port function control expansion register 1 (8 bits)	RPFCE1B	400A 3441H
RT port function control expansion register 2 (8 bits)	RPFCE2B	400A 3442H
RT port function control expansion register 3 (8 bits)	RPFCE3B	400A 3443H
RT port function control expansion register 0 (16 bits)	RPFCE0H	400A 3440H
RT port function control expansion register 2 (16 bits)	RPFCE2H	400A 3442H
RT port function control expansion register 0 (32 bits)	RPFCE0W	400A 3440H
RT port pin input register 0 (8 bits)	RPIN0B	400A 3450H
RT port pin input register 1 (8 bits)	RPIN1B	400A 3451H
RT port pin input register 2 (8 bits)	RPIN2B	400A 3452H
RT port pin input register 3 (8 bits)	RPIN3B	400A 3453H
RT port pin input register 0 (16 bits)	RPIN0H	400A 3450H
RT port pin input register 2 (16 bits)	RPIN2H	400A 3452H
RT port pin input register 0 (32 bits)	RPIN0W	400A 3450H

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Register Name	Symbol	Address
EXT port register 0 (8 bits)	EXTP0B	400A 3800H
EXT port register 1 (8 bits)	EXTP1B	400A 3801H
EXT port register 0 (16 bits)	EXTP0H	400A 3800H
EXT port register 0 (32 bits)	EXTP0W	400A 3800H
EXT port mode register 0 (8 bits)	EXTPM0B	400A 3810H
EXT port mode register 1 (8 bits)	EXTPM1B	400A 3811H
EXT port mode register 0 (16 bits)	EXTPM0H	400A 3810H
EXT port mode register 0 (32 bits)	EXTPM0W	400A 3810H
EXT port mode control register 0 (8 bits)	EXTPMC0B	400A 3820H
EXT port mode control register 1 (8 bits)	EXTPMC1B	400A 3821H
EXT port mode control register 0 (16 bits)	EXTPMC0H	400A 3820H
EXT port mode control register 0 (32 bits)	EXTPMC0W	400A 3820H
EXT port function control register (8 bits)	EXTPFC0B	400A 3830H
EXT port function control register (8 bits)	EXTPFC1B	400A 3831H
EXT port function control register (16 bits)	EXTPFC0H	400A 3830H
EXT port function control register (32 bits)	EXTPFC0W	400A 3830H
EXT port function control expansion register 0 (8 bits)	EXTPFCE0B	400A 3840H
EXT port function control expansion register 1 (8 bits)	EXTPFCE1B	400A 3841H
EXT port function control expansion register 0 (16 bits)	EXTPFCE0H	400A 3840H
EXT port function control expansion register 0 (32 bits)	EXTPFCE0W	400A 3840H
EXT port pin input register 0 (8 bits)	EXTPIN0B	400A 3850H
EXT port pin input register 1 (8 bits)	EXTPIN1B	400A 3851H
EXT port pin input register 0 (16 bits)	EXTPIN0H	400A 3850H
EXT port pin input register 0 (32 bits)	EXTPIN0W	400A 3850H

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Register Name	Symbol	Address
Buffer switching register P0L	DRCTLP0L	4001 0220H
Buffer switching register P0H	DRCTLP0H	4001 0224H
Buffer switching register P1L	DRCTLP1L	4001 0228H
Buffer switching register P1H	DRCTLP1H	4001 022CH
Buffer switching register P2L	DRCTLP2L	4001 0230H
Buffer switching register P2H	DRCTLP2H	4001 0234H
Buffer switching register P3L	DRCTLP3L	4001 0238H
Buffer switching register P3H	DRCTLP3H	4001 023CH
Buffer switching register P4L	DRCTLP4L	4001 0240H
Buffer switching register P4H	DRCTLP4H	4001 0244H
Buffer switching register P5L	DRCTLP5L	4001 0248H
Buffer switching register P5H	DRCTLP5H	4001 024CH
Buffer switching register P6L	DRCTLP6L	4001 0250H
Buffer switching register P6H	DRCTLP6H	4001 0254H
Buffer switching register P7L	DRCTLP7L	4001 0258H
Buffer switching register P7H	DRCTLP7H	4001 025CH
Buffer switching register RP0L	DRCTLRP0L	4001 0260H
Buffer switching register RP0H	DRCTLRP0H	4001 0264H
Buffer switching register RP1L	DRCTLRP1L	4001 0268H
Buffer switching register RP1H	DRCTLRP1H	4001 026CH
Buffer switching register RP2L	DRCTLRP2L	4001 0270H
Buffer switching register RP2H	DRCTLRP2H	4001 0274H
Buffer switching register RP3L	DRCTLRP3L	4001 0278H
Buffer switching register RP3H	DRCTLRP3H	4001 027CH
Buffer switching register EXTP0L	DRCTLEXTP0L	4001 0280H
Buffer switching register EXTP0H	DRCTLEXTP0H	4001 0284H
Buffer switching register EXTP1L	DRCTLEXTP1L	4001 0288H

7.3.1 Port Registers (P, RP, EXTP)

The R-IN32M4-CL2 incorporates twelve 8-bit ports and one 10-bit port (EXTP). Nine are 3-state I/O ports (including EXTP) and four are for real-time control.

Input or output can be specified for ports in 1-bit units. The port registers are used for writing the output levels for output port pins. When read, the value of the given port register is read. The PIN, RPIN, and EXTPIN registers are used to read the levels on input pins.

	7	6	5	4	3	2	1	0	Address	Initial value
P0B	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H	00H
P1B	P17	P16	P15	P14	P13	P12	P11	P10	400A 3001H	00H
P2B	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H	00H
P3B	P37	P36	P35	P34	P33	P32	P31	P30	400A 3003H	00H
P4B	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H	00H
P5B	P57	P56	P55	P54	P53	P52	P51	P50	400A 3005H	00H
P6B	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H	00H
P7B	P77	P76	P75	P74	P73	P72	P71	P70	400A 3007H	00H
EXTP0B	EXTP7	EXTP6	EXTP5	EXTP4	EXTP3	EXTP2	EXTP1	EXTP0	400A 3800H	00H
EXTP1B	0	0	0	0	0	0	EXTP9	EXTP8	400A 3801H	00H
RP0B	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H	00H
RP1B	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	400A 3401H	00H
RP2B	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H	00H
RP3B	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	400A 3403H	00H

Bit Position	Bit Name	Description
7 to 0	Pmn/RPln EXTPp	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.2 Port Registers (8-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P0H	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P2H	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P4H	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P6H	P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
EXTP0H	0	0	0	0	0	0	EXTP9	EXTP8	EXTP7	EXTP6	EXTP5	EXTP4	EXTP3	EXTP2	EXTP1	EXTP0	400A 3800H
	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

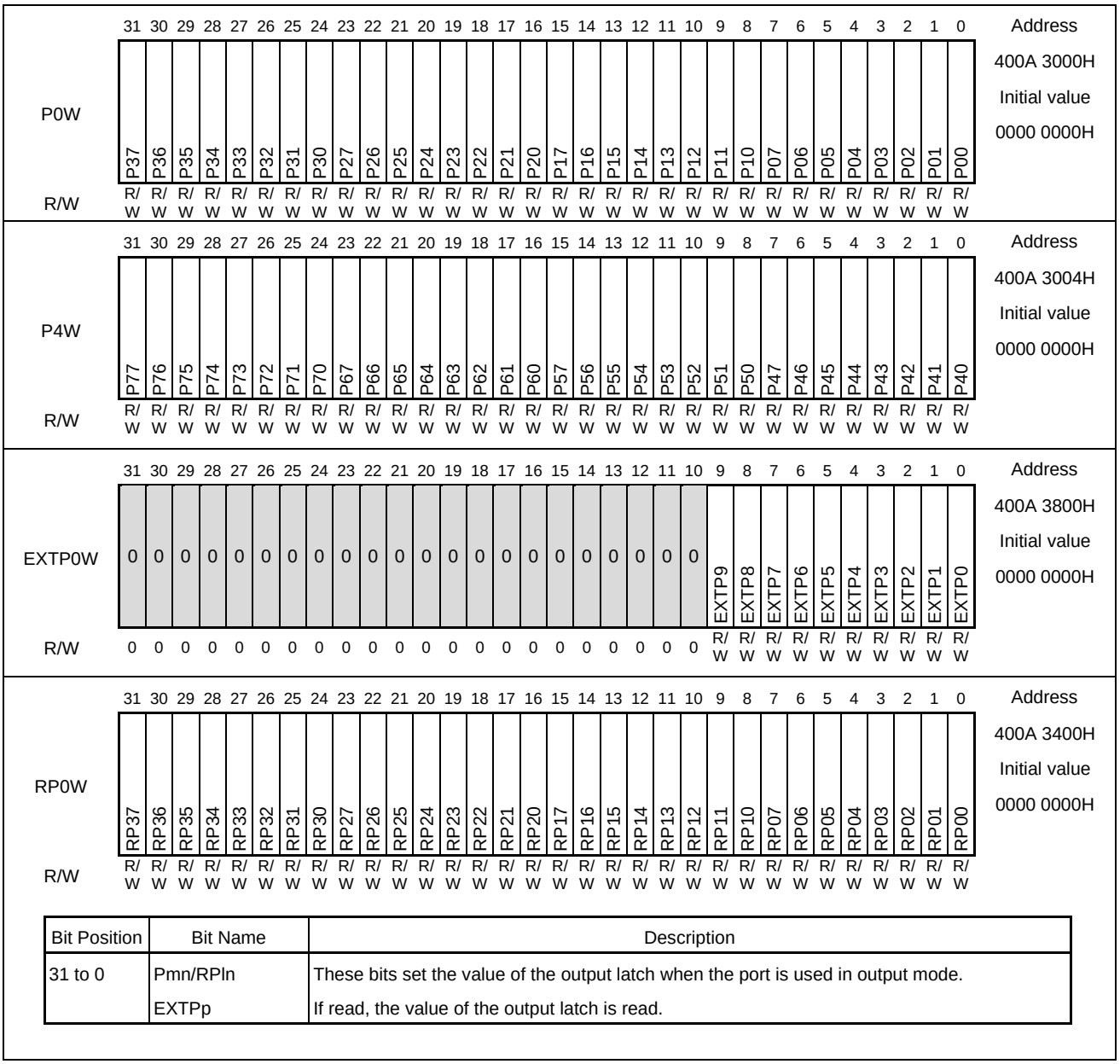
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP0H	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP2H	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

Bit Position	Bit Name	Description
15 to 0	Pmn/RPln EXTPp	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.3 Port Registers (in 16-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9



Bit Position	Bit Name	Description
31 to 0	Pmn/RPln	These bits set the value of the output latch when the port is used in output mode.
	EXTPp	If read, the value of the output latch is read.

Figure 7.4 Port Registers (in 32-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

7.3.2 Port Mode Registers (PM, RPM, EXTPM)

These registers are used to set a port to input or output mode.

	7	6	5	4	3	2	1	0	Address	Initial value
PM0B	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H	FFH
PM1B	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	400A 3011H	FFH
PM2B	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H	FFH
PM3B	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	400A 3013H	FFH
PM4B	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H	FFH
PM5B	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	400A 3015H	FFH
PM6B	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H	FFH
PM7B	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	400A 3017H	FFH
EXTPM0B	EXTPM7	EXTPM6	EXTPM5	EXTPM4	EXTPM3	EXTPM2	EXTPM1	EXTPM0	400A 3810H	FFH
EXTPM1B	0	0	0	0	0	0	EXTPM9	EXTPM8	400A 3811H	03H
RPM0B	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H	FFH
RPM1B	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	400A 3411H	FFH
RPM2B	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	400A 3412H	FFH
RPM3B	RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	400A 3413H	FFH

Bit Position	Bit Name	Description
7 to 0	PMmn/ RPMln/ EXTPMp	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.5 Port Mode Registers (in 8-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

PM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

PM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

PM4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

PM6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

EXTPM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	EXTPM9	EXTPM8	EXTPM7	EXTPM6	EXTPM5	EXTPM4	EXTPM3	EXTPM2	EXTPM1	EXTPM0	400A 3810H
0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																03FFH

RPM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

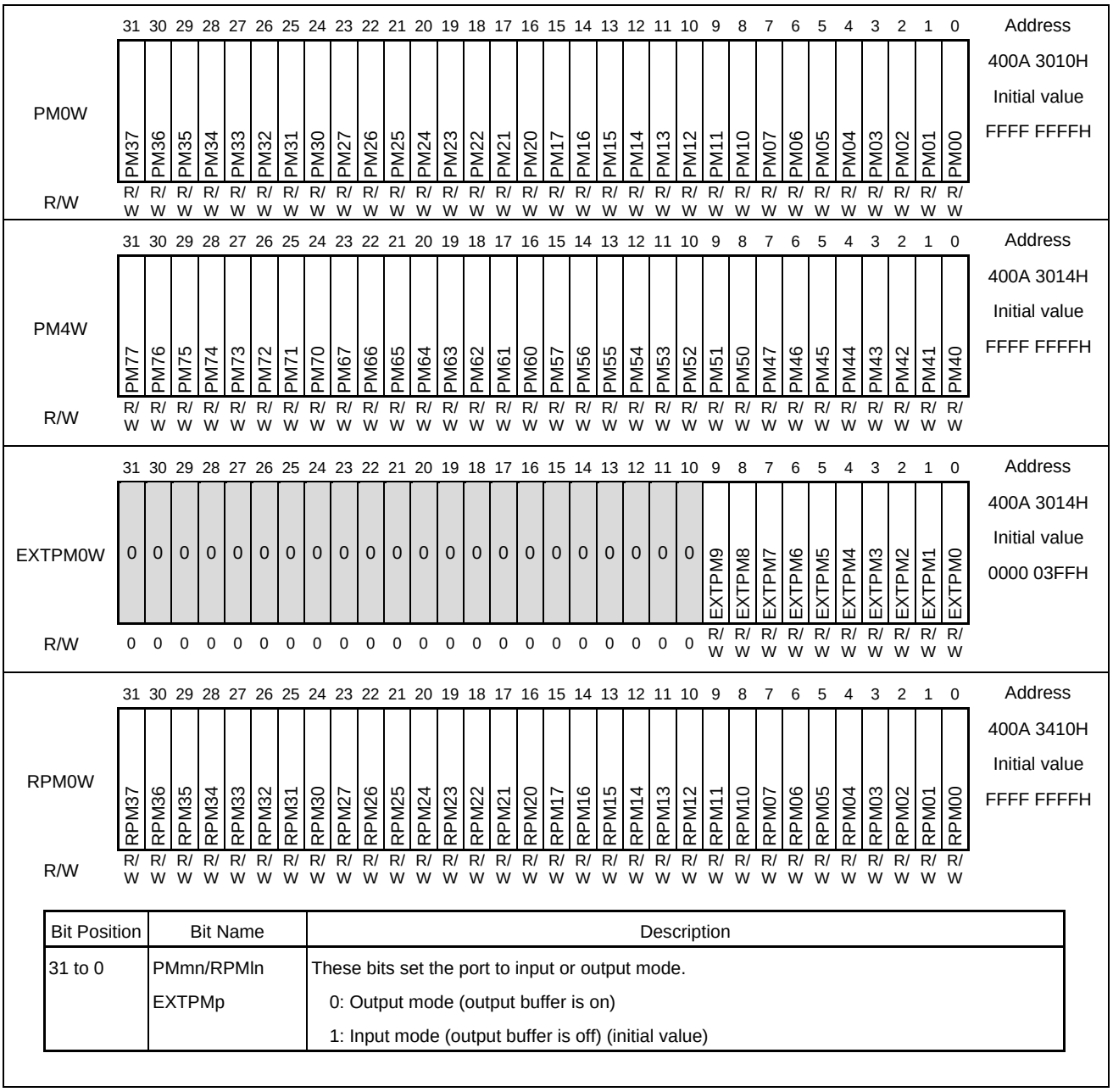
RPM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	400A 3412H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

Bit Position	Bit Name	Description
15 to 0	PMmn/ RPMln/ EXTPMp	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.6 Port Mode Registers (16-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9



Bit Position	Bit Name	Description
31 to 0	PMmn/RPMln EXTPMp	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.7 Port Mode Registers (in 32-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

7.3.3 Port Mode Control Registers (PMC, RPMC, EXTPMC)

These registers are for selecting whether the port pins are used as port pins or as multiplexed function pins.

	7	6	5	4	3	2	1	0	Address	Initial value
PMC0B	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H	00H
PMC1B	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	400A 3021H	00H Note 1
PMC2B	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H	00H
PMC3B	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	400A 3023H	00H
PMC4B	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H	00H Note 1
PMC5B	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	400A 3025H	00H
PMC6B	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H	00H
PMC7B	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	400A 3027H	00H
EXTPMC0B	EXTPMC7	EXTPMC6	EXTPMC5	EXTPMC4	EXTPMC3	EXTPMC2	EXTPMC1	EXTPMC0	400A 3820H	00H
EXTPMC1B	0	0	0	0	0	0	EXTPMC9	EXTPMC8	400A 3821H	00H
RPMC0B	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H	00H Note 1
RPMC1B	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	400A 3421H	00H Note 1
RPMC2B	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H	00H Note 1
RPMC3B	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	400A 3423H	00H Note 1

Bit Position	Bit Name	Description
7 to 0	PMCmn/ RPMCln/ EXTPMCp	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 7.8 Port Mode Control Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

PMC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

PMC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H

PMC4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

PMC6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H

EXTPMC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	EXTPMC9	EXTPMC8	EXTPMC7	EXTPMC6	EXTPMC5	EXTPMC4	EXTPMC3	EXTPMC2	EXTPMC1	EXTPMC0	400A 3820H
0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H

RPMC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

RPMC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

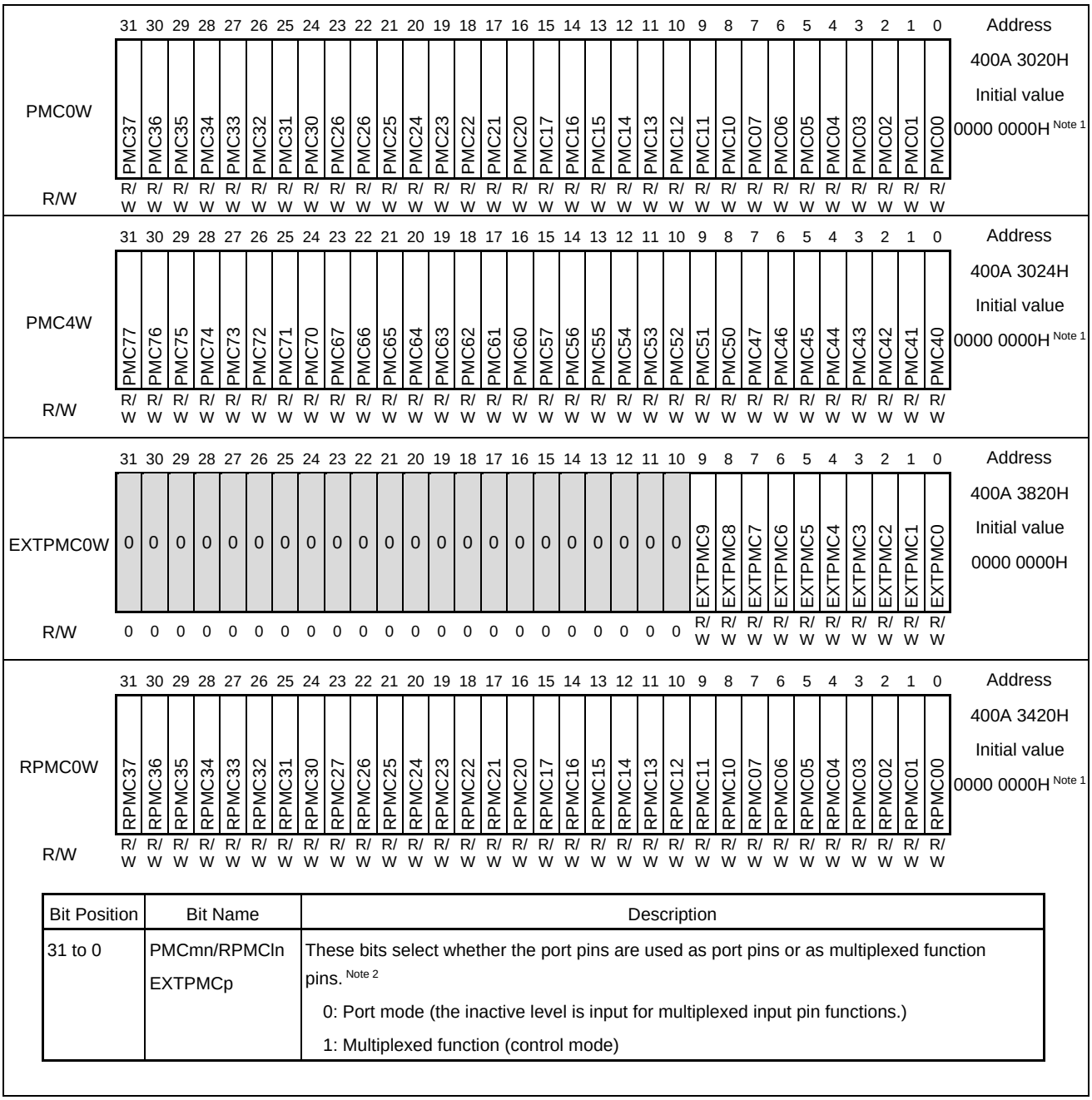
Bit Position	Bit Name	Description
15 to 0	PMCmn/ RPMCln/ EXTPMCp	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 7.9 Port Mode Control Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. **The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.**

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9



Bit Position	Bit Name	Description
31 to 0	PMCmn/RPMCln EXTPMCp	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 7.10 Port Mode Control Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

7.3.4 Port Function Control Registers (PFC, RPFC, EXTPFC)

These registers are used to specify which multiplexed function is to be used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial value
PFC0B	PFC07	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H	00H
PFC1B	PFC17	PFC16	PFC15	PFC14	PFC13	PFC12	PFC11	PFC10	400A 3031H	00H
PFC2B	PFC27	PFC26	PFC25	PFC24	PFC23	PFC22	PFC21	PFC20	400A 3032H	00H
PFC3B	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	PFC31	PFC30	400A 3033H	00H
PFC4B	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H	00H Note 1
PFC5B	PFC57	PFC56	PFC55	PFC54	PFC53	PFC52	PFC51	PFC50	400A 3035H	00H
PFC6B	PFC67	PFC66	PFC65	PFC64	PFC63	PFC62	PFC61	PFC60	400A 3036H	00H
PFC7B	PFC77	PFC76	PFC75	PFC74	PFC73	PFC72	PFC71	PFC70	400A 3037H	00H
EXTPFC0B	EXTPFC7	EXTPFC6	EXTPFC5	EXTPFC4	EXTPFC3	EXTPFC2	EXTPFC1	EXTPFC0	400A 3830H	00H
EXTPFC1B	0	0	0	0	0	0	EXTPFC9	EXTPFC8	400A 3831H	00H
RPFC0B	RPFC07	RPFC06	RPFC05	RPFC04	RPFC03	RPFC02	RPFC01	RPFC00	400A 3430H	00H Note 1
RPFC1B	RPFC17	RPFC16	RPFC15	RPFC14	RPFC13	RPFC12	RPFC11	RPFC10	400A 3431H	00H
RPFC2B	RPFC27	RPFC26	RPFC25	RPFC24	RPFC23	RPFC22	RPFC21	RPFC20	400A 3432H	00H Note 1
RPFC3B	RPFC37	RPFC36	RPFC35	RPFC34	RPFC33	RPFC32	RPFC31	RPFC30	400A 3433H	00H

Bit Position	Bit Name	Description
7 to 0	PFCmn/ RPFCmn/ EXTPFCp	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 7.11 Port Function Control Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

PFC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC17	PFC16	PFC15	PFC14	PFC13	PFC12	PFC11	PFC10	PFC07	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

PFC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	PFC31	PFC30	PFC27	PFC26	PFC25	PFC24	PFC23	PFC22	PFC21	PFC20	400A 3032H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

PFC4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC57	PFC56	PFC55	PFC54	PFC53	PFC52	PFC51	PFC50	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

PFC6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC77	PFC76	PFC75	PFC74	PFC73	PFC72	PFC71	PFC70	PFC67	PFC66	PFC65	PFC64	PFC63	PFC62	PFC61	PFC60	400A 3036H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

EXTPFC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	EXTPFC9	EXTPFC8	EXTPFC7	EXTPFC6	EXTPFC5	EXTPFC4	EXTPFC3	EXTPFC2	EXTPFC1	EXTPFC0	400A 3830H
0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

RPFC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC17	RPFC16	RPFC15	RPFC14	RPFC13	RPFC12	RPFC11	RPFC10	RPFC07	RPFC06	RPFC05	RPFC04	RPFC03	RPFC02	RPFC01	RPFC00	400A 3430H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

RPFC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC37	RPFC36	RPFC35	RPFC34	RPFC33	RPFC32	RPFC31	RPFC30	RPFC27	RPFC26	RPFC25	RPFC24	RPFC23	RPFC22	RPFC21	RPFC20	400A 3432H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

Bit Position	Bit Name	Description
15 to 0	PFCmn/ RPFCmn/ EXTPFCp	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

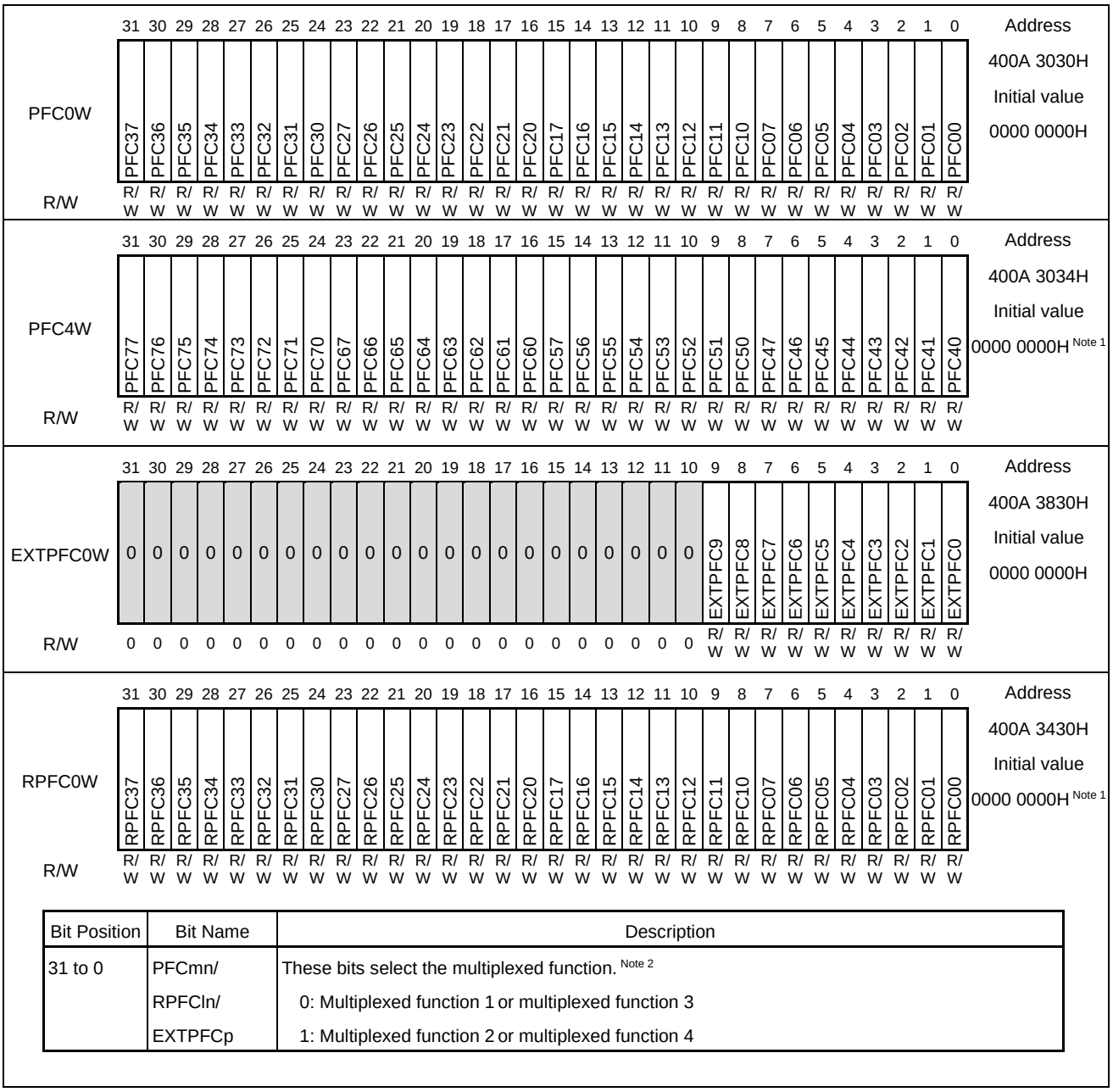
Figure 7.12 Port Function Control Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of

Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9



Bit Position	Bit Name	Description
31 to 0	PFCmn/ RPFCln/ EXTPFCp	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 7.13 Port Function Control Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE, EXTPFCE)

These registers are used to specify which multiplexed extended function is to be used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial value
PFCE0B	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	PFCE01	PFCE00	400A 3040H	00H
PFCE1B	PFCE17	PFCE16	PFCE15	PFCE14	PFCE13	PFCE12	PFCE11	PFCE10	400A 3041H	00H
PFCE2B	PFCE27	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H	00H
PFCE3B	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	PFCE31	PFCE30	400A 3043H	00H
PFCE4B	PFCE47	PFCE46	PFCE45	PFCE44	PFCE43	PFCE42	PFCE41	PFCE40	400A 3044H	00H
PFCE5B	PFCE57	PFCE56	PFCE55	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	400A 3045H	00H
PFCE6B	PFCE67	PFCE66	PFCE65	PFCE64	PFCE63	PFCE62	PFCE61	PFCE60	400A 3046H	00H
PFCE7B	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	400A 3047H	00H
EXTPFCE0B	EXTPFCE7	EXTPFCE6	EXTPFCE5	EXTPFCE4	EXTPFCE3	EXTPFCE2	EXTPFCE1	EXTPFCE0	400A 3840H	00H
EXTPFCE1B	0	0	0	0	0	0	EXTPFCE9	EXTPFCE8	400A 3841H	00H
RPFCE0B	RPFCE07	RPFCE06	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H	00H
RPFCE1B	RPFCE17	RPFCE16	RPFCE15	RPFCE14	RPFCE13	RPFCE12	RPFCE11	RPFCE10	400A 3441H	00H
RPFCE2B	RPFCE27	RPFCE26	RPFCE25	RPFCE24	RPFCE23	RPFCE22	RPFCE21	RPFCE20	400A 3442H	00H
RPFCE3B	RPFCE37	RPFCE36	RPFCE35	RPFCE34	RPFCE33	RPFCE32	RPFCE31	RPFCE30	400A 3443H	00H

Bit Position	Bit Name	Description
7 to 0	PFCEmn/ RPFCEln/ EXTPFCEp	These bits select the multiplexed function. Note 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 7.14 Port Function Control Expansion Registers (in 8-Bit Notation)

Note: The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

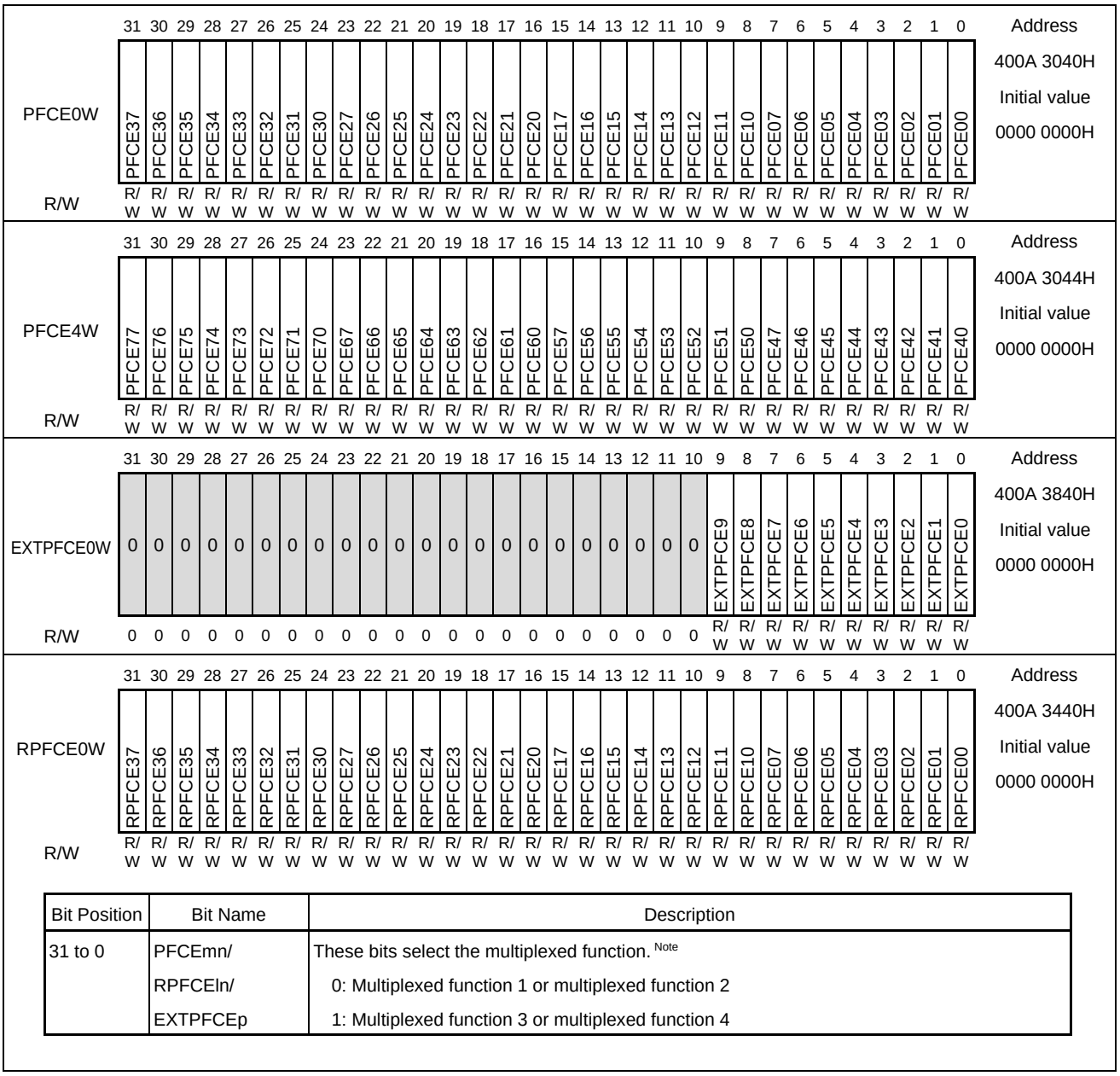
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE0H	PFCE17	PFCE16	PFCE15	PFCE14	PFCE13	PFCE12	PFCE11	PFCE10	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	PFCE01	PFCE00	400A 3040H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H
PFCE2H	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	PFCE31	PFCE30	PFCE27	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H
PFCE4H	PFCE57	PFCE56	PFCE55	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	PFCE47	PFCE46	PFCE45	PFCE44	PFCE43	PFCE42	PFCE41	PFCE40	400A 3044H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H
PFCE6H	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	PFCE67	PFCE66	PFCE65	PFCE64	PFCE63	PFCE62	PFCE61	PFCE60	400A 3046H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H
EXTPFCE0H	0	0	0	0	0	0	EXTPFCE9	EXTPFCE8	EXTPFCE7	EXTPFCE6	EXTPFCE5	EXTPFCE4	EXTPFCE3	EXTPFCE2	EXTPFCE1	EXTPFCE0	400A 3840H
	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H
RPFCE0H	RPFCE17	RPFCE16	RPFCE15	RPFCE14	RPFCE13	RPFCE12	RPFCE11	RPFCE10	RPFCE07	RPFCE06	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H
RPFCE2H	RPFCE37	RPFCE36	RPFCE35	RPFCE34	RPFCE33	RPFCE32	RPFCE31	RPFCE30	RPFCE27	RPFCE26	RPFCE25	RPFCE24	RPFCE23	RPFCE22	RPFCE21	RPFCE20	400A 3442H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

Bit Position	Bit Name	Description
15 to 0	PFCEmn/ RPFCEln/ EXTPFCEp	These bits select the multiplexed function. Note 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 7.15 Port Function Control Expansion Registers (in 16-Bit Notation)

Note: The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9



Bit Position	Bit Name	Description
31 to 0	PFCEmn/ RPFCEln/ EXTPFCEp	These bits select the multiplexed function. Note 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 7.16 Port Function Control Expansion Registers (in 32-Bit Notation)

Note: The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

7.3.6 Port Pin Input Registers (PIN, RPIN, EXTPIN)

These are read-only registers for reading the input level of port pins.

	7	6	5	4	3	2	1	0	Address	Initial value
PIN0B	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H	Pin level
PIN1B	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	400A 3051H	Pin level
PIN2B	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	400A 3052H	Pin level
PIN3B	PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	400A 3053H	Pin level
PIN4B	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H	Pin level
PIN5B	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	400A 3055H	Pin level
PIN6B	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	400A 3056H	Pin level
PIN7B	PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	400A 3057H	Pin level
EXTPIN0B	EXTPIN7	EXTPIN6	EXTPIN5	EXTPIN4	EXTPIN3	EXTPIN2	EXTPIN1	EXTPIN0	400A 3850H	Pin level
EXTPIN1B	0	0	0	0	0	0	EXTPIN9	EXTPIN8	400A 3851H	Pin level
RPIN0B	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H	Pin level
RPIN1B	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	400A 3451H	Pin level
RPIN2B	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	400A 3452H	Pin level
RPIN3B	RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	400A 3453H	Pin level

Bit Position	Bit Name	Description
7 to 0	PINmn/ RPINln/ EXTPINp	These bits are for reading the input level of the port pins.

Figure 7.17 Port Pin Input Registers (in 8-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PIN0H	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13	PIN 12	PIN 11	PIN 10	PIN 07	PIN 06	PIN 05	PIN 04	PIN 03	PIN 02	PIN 01	PIN 00	Address: 400A 3050H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level
PIN2H	PIN 37	PIN 36	PIN 35	PIN 34	PIN 33	PIN 32	PIN 31	PIN 30	PIN 27	PIN 26	PIN 25	PIN 24	PIN 23	PIN 22	PIN 21	PIN 20	Address: 400A 3052H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level
PIN4H	PIN 57	PIN 56	PIN 55	PIN 54	PIN 53	PIN 52	PIN 51	PIN 50	PIN 47	PIN 46	PIN 45	PIN 44	PIN 43	PIN 42	PIN 41	PIN 40	Address: 400A 3054H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level
PIN6H	PIN 77	PIN 76	PIN 75	PIN 74	PIN 73	PIN 72	PIN 71	PIN 70	PIN 67	PIN 66	PIN 65	PIN 64	PIN 63	PIN 62	PIN 61	PIN 60	Address: 400A 3056H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level
EXTPIN0H	0	0	0	0	0	0	EXTP IN9	EXTP IN8	EXTP IN7	EXTP IN6	EXTP IN5	EXTP IN4	EXTP IN3	EXTP IN2	EXTP IN1	EXTP IN0	Address: 400A 3850H
	0	0	0	0	0	0	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level
RPIN0H	RPIN 17	RPIN 16	RPIN 15	RPIN 14	RPIN 13	RPIN 12	RPIN 11	RPIN 10	RPIN 07	RPIN 06	RPIN 05	RPIN 04	RPIN 03	RPIN 02	RPIN 01	RPIN 00	Address: 400A 3450H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level
RPIN2H	RPIN 37	RPIN 36	RPIN 35	RPIN 34	RPIN 33	RPIN 32	RPIN 31	RPIN 30	RPIN 27	RPIN 26	RPIN 25	RPIN 24	RPIN 23	RPIN 22	RPIN 21	RPIN 20	Address: 400A 3452H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level

Bit Position	Bit Name	Description
15 to 0	PINmn/ RPINln/ EXTPINp	These bits are for reading the input level of the port pins.

Figure 7.18 Port Pin Input Registers (in 16-Bit Notation)

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

PIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																																Pin level

R/W

PIN4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																																Pin level

R/W

EXTPIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXTPIN9	EXTPIN8	EXTPIN7	EXTPIN6	EXTPIN5	EXTPIN4	EXTPIN3	EXTPIN2	EXTPIN1	EXTPIN0	400A 3850H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R	R	R	R	R	R	R	R	R	Initial value
																																Pin level

R/W

RPIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																																Pin level

R/W

Bit Position	Bit Name	Description
31 to 0	PINmn/ RPINln/ EXTPINp	These bits are for reading the input level of the port pins.

Remark: l = 0 to 3; m = 0 to 7; n = 0 to 7; p = 0 to 9

7.4 List of Selectable Multiplexed Functions

The table below lists the combinations of multiplexed functions that can be specified by using the port-related registers.

(1) Ports (P00 to P77)

(1/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P00	P00 (output mode)	P00 (input mode)	INTPZ0	-	CCI_RUNLEDZ	CCS_MON1
P01	P01 (output mode)	P01 (input mode)	INTPZ1	-	-	CCS_MON2
P02	P02 (output mode)	P02 (input mode)	INTPZ2	-	CCI_DLINKLEDZ	CCS_STBMSK
P03	P03 (output mode)	P03 (input mode)	INTPZ3	-	CCI_ERRLEDZ	CCS_MON5
P04	P04 (output mode)	P04 (input mode)	INTPZ4	-	CCI_LERR1LEDZ	CCS_MON6
P05	P05 (output mode)	P05 (input mode)	INTPZ5	-	CCI_LERR2LEDZ	CCS_MON7
P06	P06 (output mode)	P06 (input mode)	-	-	CCI_SDLEDZ	CCS_MON0
P07	P07 (output mode)	P07 (input mode)	-	-	CCIRDLEDZ	CCS_RESOUT
P10	P10 (output mode)	P10 (input mode)	SMIO2	-	-	CCS_MON1
P11	P11 (output mode)	P11 (input mode)	SMIO3	-	-	CCS_MON2
P12	P12 (output mode)	P12 (input mode)	CSZ3	-	CCI_WDTIZ / CCM_WDTENZ/ CCS_WDTZ	CCS_MON3
P13	P13 (output mode)	P13 (input mode)	CSZ2	-	-	-
P14	P14 (output mode)	P14 (input mode)	SMSCK	-	-	-
P15	P15 (output mode)	P15 (input mode)	SMIO0	-	-	-
P16	P16 (output mode)	P16 (input mode)	SMIO1	-	-	-
P17	P17 (output mode)	P17 (input mode)	SMCSZ	-	-	-
P20	P20 (output mode)	P20 (input mode)	RXD0	-	CCM_LINKERRZ	-
P21	P21 (output mode)	P21 (input mode)	TXD0	-	CCM_ERRZ	-
P22	P22 (output mode)	P22 (input mode)	INTPZ8	-	CCS_IOTENSU	-
P23	P23 (output mode)	P23 (input mode)	INTPZ9	-	CCS_SENYU0	-
P24	P24 (output mode)	P24 (input mode)	INTPZ10	ETHSWSYNCOUT	CCS_SENYU1	-
P25	P25 (output mode)	P25 (input mode)	WDTOUTZ	-	CCS_ERRZ	-
P26	P26 (output mode)	P26 (input mode)	TINJ1/TIND5	TOUTJ1 / TOUTD5	CCM_RUNZ / CCS_RUNZ	-
P27	P27 (output mode)	P27 (input mode)	TINJ0/TIND4	TOUTJ0 / TOUTD4	-	-

Remark: m = 0 to 7; n = 0 to 7

(2/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P30	P30 (output mode)	P30 (input mode)	RXD1	-	-	-
P31	P31 (output mode)	P31 (input mode)	TXD1	-	-	-
P32	P32 (output mode)	P32 (input mode)	DMAREQZ1	-	CCM_LNKRUNZ/ CCS_LNKRUNZ	-
P33	P33 (output mode)	P33 (input mode)	DMAACKZ1	-	CCM_RDLEDZ/ CCS_RDLEDZ	-
P34	P34 (output mode)	P34 (input mode)	DMATCZ1	-	-	-
P35	P35 (output mode)	P35 (input mode)	CSISCK1	INTPZ22	-	-
P36	P36 (output mode)	P36 (input mode)	CSISI1	INTPZ23	-	-
P37	P37 (output mode)	P37 (input mode)	CSISO1	INTPZ24	-	-
P40	P40 (output mode)	P40 (input mode)	A1	HA1	-	-
P41	P41 (output mode)	P41 (input mode)	WAITZ	HWAITZ	-	-
P42	P42 (output mode)	P42 (input mode)	CSICS00	HERROUTZ	CCS_FUSEZ	-
P43	P43 (output mode)	P43 (input mode)	CSICS01	HBUSCLK	CCM_IRLZ	-
P44	P44 (output mode)	P44 (input mode)	CSZ1	HPGCSZ	-	-
P45	P45 (output mode)	P45 (input mode)	CSISCK0	WAITZ1	-	-
P46	P46 (output mode)	P46 (input mode)	CSISI0	WAITZ2	-	-
P47	P47 (output mode)	P47 (input mode)	CSISO0	WAITZ3	-	-
P50	P50 (output mode)	P50 (input mode)	INTPZ6	-	-	CCS_REFSTB
P51	P51 (output mode)	P51 (input mode)	INTPZ7	-	-	CCS_SDGATEON
P52	P52 (output mode)	P52 (input mode)	TINJ3 / TIND7	TOUTJ3 / TOUTD7	CCI_NMIZ	CCS_DCHANG
P53	P53 (output mode)	P53 (input mode)	CRXD0	CCI_INTZ	-	-
P54	P54 (output mode)	P54 (input mode)	CTXD0	CCS_RD	CCM_RD	-
P55	P55 (output mode)	P55 (input mode)	CRXD1	CCS_MON4	-	-
P56	P56 (output mode)	P56 (input mode)	CTXD1	CCS_SD	CCM_SD	-
P57	P57 (output mode)	P57 (input mode)	TINJ2 / TIND6	TOUTJ2 / TOUTD6	CCM_SDGCZ	-

Remark: m = 0 to 7; n = 0 to 7

(3/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P60	P60 (output mode)	P60 (input mode)	SCL0	-	-	-
P61	P61 (output mode)	P61 (input mode)	SDA0	-	-	-
P62	P62 (output mode)	P62 (input mode)	RTDMAREQZ	-	CCM_MDIN0	-
P63	P63 (output mode)	P63 (input mode)	RTDMAACKZ	-	CCM_MDIN1	-
P64	P64 (output mode)	P64 (input mode)	RTDMATCZ	-	CCM_MDIN2	-
P65	P65 (output mode)	P65 (input mode)	DMAREQZ0	-	CCM_MDIN3	-
P66	P66 (output mode)	P66 (input mode)	DMAACKZ0	-	CCM_MSTZ	-
P67	P67 (output mode)	P67 (input mode)	DMATCZ0	-	CCS_MON3	-
P70	P70 (output mode)	P70 (input mode)	CSICS10	-	CCS_STATION_NO_0 / CCM_SNIN0	-
P71	P71 (output mode)	P71 (input mode)	CSICS11	-	CCS_STATION_NO_1 / CCM_SNIN1	-
P72	P72 (output mode)	P72 (input mode)	SLEEPING	-	CCS_STATION_NO_2 / CCM_SNIN2	-
P73	P73 (output mode)	P73 (input mode)	INTPZ11	-	CCS_STATION_NO_3 / CCM_SNIN3	-
P74	P74 (output mode)	P74 (input mode)	INTPZ12	-	CCS_STATION_NO_4 / CCM_SNIN4	-
P75	P75 (output mode)	P75 (input mode)	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	-
P76	P76 (output mode)	P76 (input mode)	INTPZ14	-	CCS_STATION_NO_6 / CCM_SNIN6	-
P77	P77 (output mode)	P77 (input mode)	INTPZ15	-	CCS_STATION_NO_7 / CCM_SNIN7	-

Remark: m = 0 to 7; n = 0 to 7

(2) Real-Time Ports (RP00 to RP37)

Pin Name	RPMCmn = 0 (Port Mode)		RPMCmn = 1 (Control Mode)			
			RPFCEmn = 0		RPFCEmn = 1	
	RPMmn = 0 (Output Port)	RPMmn = 1 (Input Port)	RPFCmn = 0 (Multiplexed Function 1)	RPFCmn = 1 (Multiplexed Function 2)	RPFCmn = 0 (Multiplexed Function 3)	RPFCmn = 1 (Multiplexed Function 4)
RP00	RP00 (output mode)	RP00 (input mode)	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-
RP01	RP01 (output mode)	RP01 (input mode)	INTPZ17	SDA1	CCM_SMSTZ	-
RP02	RP02 (output mode)	RP02 (input mode)	INTPZ18	ADTRG	CCS_BS1	-
RP03	RP03 (output mode)	RP03 (input mode)	INTPZ19	ADTRGRDY	CCS_BS2	-
RP04	RP04 (output mode)	RP04 (input mode)	INTPZ20	-	CCS_BS4	-
RP05	RP05 (output mode)	RP05 (input mode)	INTPZ21	-	CCS_BS8	-
RP06	RP06 (output mode)	RP06 (input mode)	WRZ2/BENZ2	HWRZ2/ HBENZ2	-	-
RP07	RP07 (output mode)	RP07 (input mode)	WRZ3/BENZ3	HWRZ3/ HBENZ3	-	-
RP10	RP10 (output mode)	RP10 (input mode)	D24/HD24	LED0_PHY0	-	-
RP11	RP11 (output mode)	RP11 (input mode)	D25/HD25	LED1_PHY0	-	-
RP12	RP12 (output mode)	RP12 (input mode)	D26/HD26	LED2_PHY0	-	-
RP13	RP13 (output mode)	RP13 (input mode)	D27/HD27	LED3_PHY0	-	-
RP14	RP14 (output mode)	RP14 (input mode)	D28/HD28	LED0_PHY1	-	-
RP15	RP15 (output mode)	RP15 (input mode)	D29/HD29	LED1_PHY1	-	-
RP16	RP16 (output mode)	RP16 (input mode)	D30/HD30	LED2_PHY1	-	-
RP17	RP17 (output mode)	RP17 (input mode)	D31/HD31	LED3_PHY1	-	-
RP20	RP20 (output mode)	RP20 (input mode)	BCYSTZ/ADVZ	HBCYSTZ	-	-
RP21	RP21 (output mode)	RP21 (input mode)	A21	-	-	-
RP22	RP22 (output mode)	RP22 (input mode)	A22	-	-	-
RP23	RP23 (output mode)	RP23 (input mode)	A23	-	-	-
RP24	RP24 (output mode)	RP24 (input mode)	A24	INTPZ25	-	-
RP25	RP25 (output mode)	RP25 (input mode)	A25	INTPZ26	-	-
RP26	RP26 (output mode)	RP26 (input mode)	A26	INTPZ27	-	-
RP27	RP27 (output mode)	RP27 (input mode)	A27	INTPZ28	-	-
RP30	RP30 (output mode)	RP30 (input mode)	D16/HD16	TOUTD8	TIND8	-
RP31	RP31 (output mode)	RP31 (input mode)	D17/HD17	TOUTD9	TIND9	-
RP32	RP32 (output mode)	RP32 (input mode)	D18/HD18	TOUTD10	TIND10	-
RP33	RP33 (output mode)	RP33 (input mode)	D19/HD19	TOUTD11	TIND11	-
RP34	RP34 (output mode)	RP34 (input mode)	D20/HD20	TOUTD12	TIND12	-
RP35	RP35 (output mode)	RP35 (input mode)	D21/HD21	TOUTD13	TIND13	-
RP36	RP36 (output mode)	RP36 (input mode)	D22/HD22	TOUTD14	TIND14	-
RP37	RP37 (output mode)	RP37 (input mode)	D23/HD23	TOUTD15	TIND15	-

Remark: m = 0 to 3; n = 0 to 7

(3) EXT Ports (EXTP0 to EXTP9)

Pin Name	EXTPMCp = 0 (Port Mode)		EXTPMCp = 1 (Control Mode)			
			EXTPFCEp = 0		EXTPFCEp = 1	
	EXTPMp = 0 (Output Mode)	EXTPMp = 1 (Input Port)	EXTPFCp = 0 (Multiplexed Function 1)	EXTPFCp = 1 (Multiplexed Function 2)	EXTPFCp = 0 (Multiplexed Function 3)	EXTPFCp = 1 (Multiplexed Function 4)
EXTP0	EXTP0 (output mode)	EXTP0 (input mode)	-	TOUTD0	-	TIND0
EXTP1	EXTP1 (output mode)	EXTP1 (input mode)	-	TOUTD1	-	TIND1
EXTP2	EXTP2 (output mode)	EXTP2 (input mode)	-	TOUTD2	-	TIND2
EXTP3	EXTP3 (output mode)	EXTP3 (input mode)	WDTOUTZ	TOUTD3	-	TIND3
EXTP4	EXTP4 (output mode)	EXTP4 (input mode)	-	-	-	-
EXTP5	EXTP5 (output mode)	EXTP5 (input mode)	-	-	-	-
EXTP6	EXTP6 (output mode)	EXTP6 (input mode)	-	-	-	-
EXTP7	EXTP7 (output mode)	EXTP7 (input mode)	CCM_STMON3	-	-	-
EXTP8	EXTP8 (output mode)	EXTP8 (input mode)	-	-	-	-
EXTP9	EXTP9 (output mode)	EXTP9 (input mode)	-	-	-	-

7.5 Buffer Switching Registers (DRCTL)

For some port pins, the driving ability and the connection or disconnection of a pull-up or pull-down resistor is programmable.
Set up the DRCTL registers during initialization after release from the reset state. After that, change the setting of a given DRCTL register only while the buffer functions for the corresponding pins are not in use. For example, change the setting while only internal access is proceeding.
The settings of the DRCTL registers are effective for output pins regardless of their operating mode (port mode, or control mode, in which a multiplexed function is used).

- Access These registers can be read and written in 32-bit or 16-bit units.

Cautions 1. These registers are only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register.
2. Take special care with pins in the high-impedance state, since changing the settings for the pull-up and pull-down resistors will place levels on the pins.

7.5.1 Port 0 Buffer Switching Register (DRCTLP0L, DRCTLP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP03	PDIOP03	IOLP031	IOLP030	PUIOP02	PDIOP02	IOLP021	IOLP020	PUIOP01	PDIOP01	IOLP011	IOLP010	PUIOP00	PDIOP00	IOLP001	IOLP000	BASE + 0220H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP07	PDIOP07	IOLP071	IOLP070	PUIOP06	PDIOP06	IOLP061	IOLP060	PUIOP05	PDIOP05	IOLP051	IOLP050	PUIOP04	PDIOP04	IOLP041	IOLP040	BASE + 0224H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP0n, PDIOP0n	These bits specify whether to connect a pull-up or pull-down resistor to the P07 to P00 pins.

PUIOP0n	PDIOP0n	Connection of a Pull-Up or Pull-Down Resistor to the P07 to P00 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

13, 12, 9, 8 5, 4, 1, 0	IOLP0n1, IOLP0n0	These bits specify the driving ability of the P07 to P00 pins.

IOLP0n1	IOLP0n0	Driving Ability of the P07 to P00 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: n = 7 to 0

7.5.2 Port 1 Buffer Switching Register (DRCTLP1L, DRCTLP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP13	PDIOP13	0	1	PUIOP12	PDIOP12	0	1	PUIOP11	PDIOP11	0	1	PUIOP10	PDIOP10	0	1	BASE + 0228H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP17	PDIOP17	0	1	PUIOP16	PDIOP16	0	1	PUIOP15	PDIOP15	0	1	PUIOP14	PDIOP14	0	1	BASE + 022CH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP1n, PDIOP1n	These bits specify whether to connect a pull-up or pull-down resistor to the P17 to P10 pins.

PUIOP1n	PDIOP1n	Connection of a Pull-Up or Pull-Down Resistor to the P17 to P10 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

7.5.3 Port 2 Buffer Switching Register (DRCTLP2L, DRCTLP2H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP2L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP23	PDIOP23	0	1	PUIOP22	PDIOP22	0	1	PUIOP21	PDIOP21	IOLP211	IOLP210	PUIOP20	PDIOP20	IOLP201	IOLP200	BASE + 0230H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP27	PDIOP27	0	1	PUIOP26	PDIOP26	IOLP261	IOLP260	PUIOP25	PDIOP25	IOLP251	IOLP250	PUIOP24	PDIOP24	0	1	BASE + 0234H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP2n, PDIOP2n	These bits specify whether to connect a pull-up or pull-down resistor to the P27 to P20 pins.

PUIOP2n	PDIOP2n	Connection of a Pull-Up or Pull-Down Resistor to the P27 to P20 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

9, 8, 5, 4, 1, 0	IOLP2m1, IOLP2m0	These bits specify the driving ability of the P26 and P25, and P21 and P20 pins.

IOLP2m1	IOLP2m0	Driving Ability of the P26 and P25, and P21 and P20 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: m = 6, 5, 1, 0; n = 7 to 0

7.5.4 Port 3 Buffer Switching Register (DRCTLP3L, DRCTLP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP33	PDIOP33	IOLP331	IOLP330	PUIOP32	PDIOP32	IOLP321	IOLP320	PUIOP31	PDIOP31	0	1	PUIOP30	PDIOP30	0	1	BASE + 0238H Initial value 0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	1	R/W	R/W	0	1	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP37	PDIOP37	0	1	PUIOP36	PDIOP36	0	1	PUIOP35	PDIOP35	0	1	PUIOP34	PDIOP34	0	1	BASE + 023CH Initial value 0000 5959H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP3n, PDIOP3n	These bits specify whether to connect a pull-up or pull-down resistor to the P37 to P30 pins.
13, 12, 9, 8	IOLP3m1, IOLP3m0	These bits specify the driving ability of the P33 and P32 pins.

PUIOP3n	PDIOP3n	Connection of a Pull-Up or Pull-Down Resistor to the P37 to P30 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOLP3m1	IOLP3m0	Driving Ability of the P33 and P32 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: m = 3, 2; n = 7 to 0

7.5.5 Port 4 Buffer Switching Register (DRCTLP4L, DRCTLP4H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP43	PDIOP43	0	1	PUIOP42	PDIOP42	0	1	PUIOP41	PDIOP41	0	1	PUIOP40	PDIOP40	0	1	BASE + 0240H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP47	PDIOP47	0	1	PUIOP46	PDIOP46	0	1	PUIOP45	PDIOP45	0	1	PUIOP44	PDIOP44	0	1	BASE + 0244H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP4n, PDIOP4n	These bits specify whether to connect a pull-up or pull-down resistor to the P47 to P40 pins.

PUIOP4n	PDIOP4n	Connection of a Pull-Up or Pull-Down Resistor to the P47 to P40 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

7.5.6 Port 5 Buffer Switching Register (DRCTLP5L, DRCTLP5H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP52	PDIOP52	0	1	PUIOP51	PDIOP51	0	1	PUIOP50	PDIOP50	IOLP501	IOLP500	BASE + 0248H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	0000 0959H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP57	PDIOP57	0	1	0	0	0	0	0	0	0	0	0	0	0	0	BASE + 024CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0000 9000H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP5n, PDIOP5n	These bits specify whether to connect a pull-up or pull-down resistor to the P57 and P52 to P50 pins.
1, 0	IOLP501, IOLP500	These bits specify the driving ability of the P50 pin.

PUIOP5n	PDIOP5n	Connection of a Pull-Up or Pull-Down Resistor to the P57 and P52 to P50 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOLP501	IOLP500	Driving Ability of the P50 Pin
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: n = 7, 2 to 0

7.5.7 Port 6 Buffer Switching Register (DRCTLP6L, DRCTLP6H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP6L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP63	PDIOP63	0	1	PUIOP62	PDIOP62	0	1	PUIOP61	PDIOP61	0	1	PUIOP60	PDIOP60	0	1	BASE + 0250H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP6H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP67	PDIOP67	0	1	PUIOP66	PDIOP66	IOLP661	IOLP660	PUIOP65	PDIOP65	0	1	PUIOP64	PDIOP64	0	1	BASE + 0254H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	R/W	R/W	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP6n, PDIOP6n	These bits specify whether to connect a pull-up or pull-down resistor to the P67 to P60 pins.
9, 8	IOLP661, IOLP660	These bits specify the driving ability of the P66 pin.

PUIOP6n	PDIOP6n	Connection of a Pull-Up or Pull-Down Resistor to the P67 to P60 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOLP661	IOLP660	Driving Ability of the P66 Pin
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: n = 7 to 0

7.5.8 Port 7 Buffer Switching Register (DRCTLP7L, DRCTLP7H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP7L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP73	PDIOP73	0	1	PUIOP72	PDIOP72	0	1	PUIOP71	PDIOP71	0	1	PUIOP70	PDIOP70	0	1	BASE + 0258H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP7H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP77	PDIOP77	0	1	PUIOP76	PDIOP76	0	1	PUIOP75	PDIOP75	0	1	PUIOP74	PDIOP74	0	1	BASE + 025CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOP7n, PDIOP7n	These bits specify whether to connect a pull-up or pull-down resistor to the P77 to P70 pins.

PUIOP7n	PDIOP7n	Connection of a Pull-Up or Pull-Down Resistor to the P77 to P70 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

7.5.9 EXT Port 0 Buffer Switching Registers (DRCTLEXTP0L, DRCTLEXTP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTL EXTP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOE03	PDIOE03	0	1	PUIOE02	PDIOE02	0	1	PUIOE01	PDIOE01	0	1	PUIOE00	PDIOE00	0	1	BASE + 0280H
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTL EXTP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOE07	PDIOE07	0	1	PUIOE06	PDIOE06	0	1	PUIOE05	PDIOE05	0	1	PUIOE04	PDIOE04	0	1	BASE + 0284H
																																	Initial value
																																	0000 9599H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIOE0n, PDIOE0n	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP7 to EXTP0 pins.

PUIOE0n	PDIO E0n	Connection of a Pull-Up or Pull-Down Resistor to the EXTP7 to EXTP0 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

7.5.10 EXT Port 1 Buffer Switching Register (DRCTLEXTP1L)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLEXTP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOE09	PDIOE09	0	1	PUIOE08	PDIOE08	0	1	BASE + 0288H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	0000 0099H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
7, 6, 3, 2	PUIOE0n, PDIOE0n	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP9 and EXTP8 pins.

PUIOE0n	PDIOE0n	Connection of a Pull-Up or Pull-Down Resistor to the EXTP9 and EXTP8Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 9, 8

7.5.11 Real-Time Port 0 Buffer Switching Registers (DRCTLRP0L, DRCTLRP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP03	PDIORP03	IOLRP031	IOLRP030	PUIORP02	PDIORP02	IOLRP021	IOLRP020	PUIORP01	PDIORP01	IOLRP011	IOLRP010	PUIORP00	PDIORP00	IOLRP001	IOLRP000	BASE + 0260H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP07	PDIORP07	IOLRP071	IOLRP070	PUIORP06	PDIORP06	IOLRP061	IOLRP060	PUIORP05	PDIORP05	IOLRP051	IOLRP050	PUIORP04	PDIORP04	IOLRP041	IOLRP040	BASE + 0264H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIORP0n, PDIORP0n	These bits specify whether to connect a pull-up or pull-down resistor to the RP07 to RP00 pins.

PUIORP0n	PDIORP0n	Connection of a Pull-Up or Pull-Down Resistor to the RP07 to RP00 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Bit Position	Bit Name	Description
13, 12, 9, 8 5, 4, 1, 0	IOLRP0n1, IOLRP0n0	These bits specify the driving ability of the RP07 to RP00 pins.

IOLRP0n1	IOLRP0n0	Driving Ability of the RP07 to RP00 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: n = 7 to 0

7.5.12 Real-Time Port 1 Buffer Switching Registers (DRCTLRP1L, DRCTLRP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP13	PDIORP13	IOLRP131	IOLRP130	PUIORP12	PDIORP12	IOLRP121	IOLRP120	PUIORP11	PDIORP11	IOLRP111	IOLRP110	PUIORP10	PDIORP10	IOLRP101	IOLRP100	BASE + 0268H
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP17	PDIORP17	IOLRP171	IOLRP170	PUIORP16	PDIORP16	IOLRP161	IOLRP160	PUIORP15	PDIORP15	IOLRP151	IOLRP150	PUIORP14	PDIORP14	IOLRP141	IOLRP140	BASE + 026CH
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIORP1n, PDIORP1n	These bits specify whether to connect a pull-up or pull-down resistor to the RP17 to RP10 pins.

PUIORP1n	PDIORP1n	Connection of a Pull-Up or Pull-Down Resistor to the RP17 to RP10 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

13, 12, 9, 8 5, 4, 1, 0	IOLRP1n1, IOLRP1n0	These bits specify the driving ability of the RP17 to RP10 pins.

IOLRP1n1	IOLRP1n0	Driving Ability of the RP17 to RP10 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: n = 7 to 0

7.5.13 Real-Time Port 2 Buffer Switching Registers (DRCTLRP2L, DRCTLRP2H)

DRCTLRP2L

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP23	PDIORP23	IOLRP231	IOLRP230	PUIORP22	PDIORP22	IOLRP221	IOLRP220	PUIORP21	PDIORP21	IOLRP211	IOLRP210	PUIORP20	PDIORP20	IOLRP201	IOLRP200	BASE + 0270H
R/W																																Initial value
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 5559H

DRCTLRP2H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP27	PDIORP27	IOLRP271	IOLRP270	PUIORP26	PDIORP26	IOLRP261	IOLRP260	PUIORP25	PDIORP25	IOLRP251	IOLRP250	PUIORP24	PDIORP24	IOLRP241	IOLRP240	BASE + 0274H
R/W																																Initial value
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 5555H

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIORP2n, PDIORP2n	These bits specify whether to connect a pull-up or pull-down resistor to the RP27 to RP20 pins.
13, 12, 9, 8 5, 4, 1, 0	IOLRP2n1, IOLRP2n0	These bits specify the driving ability of the RP27 to RP20 pins.

PUIORP2n	PDIORP2n	Connection of a Pull-Up or Pull-Down Resistor to the RP27 to RP20 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOLRP2n1	IOLRP2n0	Driving Ability of the RP27 to RP20 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: n = 7 to 0

7.5.14 Real-Time Port 3 Buffer Switching Registers (DRCTLRP3L, DRCTLRP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP33	PDIORP33	IOLRP331	IOLRP330	PUIORP32	PDIORP32	IOLRP321	IOLRP320	PUIORP31	PDIORP31	IOLRP311	IOLRP310	PUIORP30	PDIORP30	IOLRP301	IOLRP300	BASE + 0278H
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP37	PDIORP37	IOLRP371	IOLRP370	PUIORP36	PDIORP36	IOLRP361	IOLRP360	PUIORP35	PDIORP35	IOLRP351	IOLRP350	PUIORP34	PDIORP34	IOLRP341	IOLRP340	BASE + 027CH
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 16	-	Reserved When writing to these bits, write 0. When read, 0 is returned.
15, 14, 11, 10, 7, 6, 3, 2	PUIORP3n, PDIORP3n	These bits specify whether to connect a pull-up or pull-down resistor to the RP37 to RP30 pins.

PUIORP3n	PDIORP3n	Connection of a Pull-Up or Pull-Down Resistor to the RP37 to RP30 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Bit Position	Bit Name	Description
13, 12, 9, 8 5, 4, 1, 0	IOLRP3n1, IOLRP3n0	These bits specify the driving ability of the RP37 to RP30 pins.

IOLRP3n1	IOLRP3n0	Driving Ability of the RP37 to RP30 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than the above		Setting prohibited

Remark: n = 7 to 0

7.6 Operation of Port Functions

Operation of the ports differs depending on the I/O mode setting as described below.

7.6.1 Reading and Writing via I/O Ports

(1) In output mode

If a value is written to a port register (Pn, RPm, or EXTPp), the value is written to that port's output latch (Pn, RPm, or EXTPp). The value of the output latch is output from the pin.
The value written to the output latch is held until another value is written.
The value of the output latch (Pn, RPm, or EXTPp) can be read by reading the port register (Pn, RPm, or EXTPp).
To directly read the pin level, read a port pin input register (PINn, RPINm, or EXTPINp).

Remark: n = 0 to 7; m = 0 to 3; p = 0, 1

(2) In input mode

If a value is written to a port register (Pn, RPm, or EXTPp), the value is written to that port's output latch (Pn, RPm, or EXTPp). However, the pint state does not change because the output buffer is off.
The value written to the output latch is held until another value is written.
To read the input level, read a port pin input register (PINn, RPINm, or EXTPINp).

Remark: n = 0 to 7; m = 0 to 3; p = 0, 1

7.6.2 Multiplexed Function Pin Output State in Control Mode

The port pin level can be read directly by reading port pin input register n, m, or p (PINn, RPINm, or EXTPINp), regardless of the settings of the PMCn, RPMCm, and EXTPMCp registers, PMn, RPMm, and EXTPMp registers, PFCn, RPFCm, and EXTPFCp registers, and PFCEn, RPCEm, and EXTPEp registers.

Remark: n = 0 to 7; m = 0 to 3; p = 0, 1

7.7 Trigger-Synchronous Ports (RP00 to RP37)

The state of the 32-bit port pins RP00 to RP37 can be updated in synchronization with an interrupt from an on-chip peripheral module.

Use the RPTRGMD register to set trigger-synchronous port control mode in 1-bit units. To select the target trigger, use the RPTFR0 to RPTFR3 registers.
For details, see the R-IN32M4-CL2 User's Manual: Peripheral Modules.

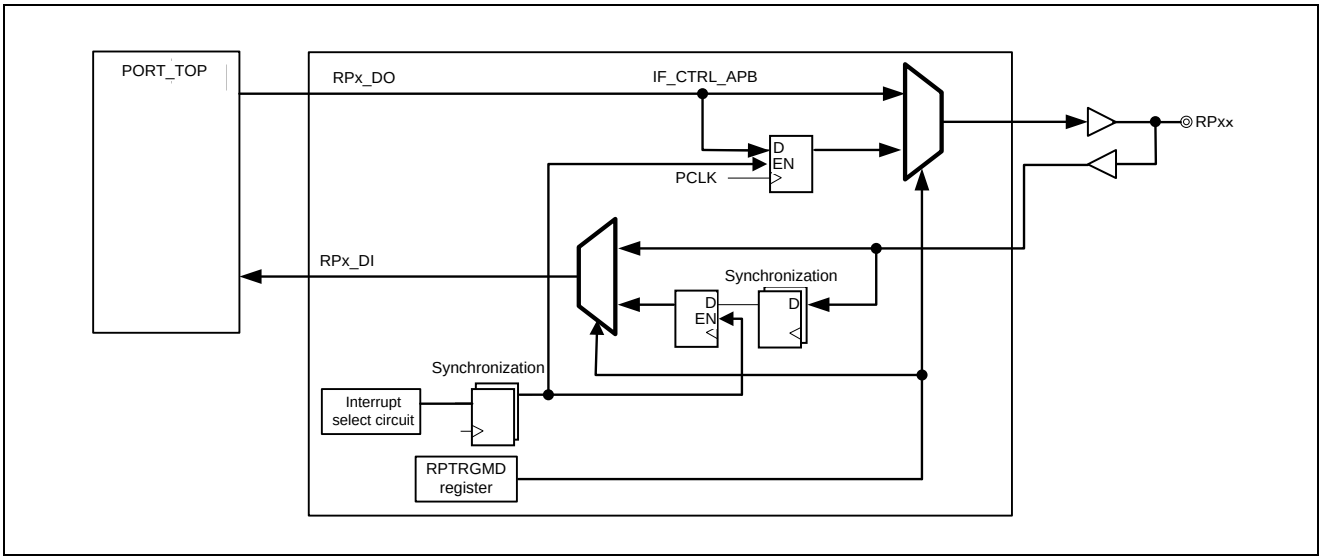


Figure 7.19 Configuration of Trigger-Synchronous Ports

8. Electrical Characteristics

8.1 Terminology

Table 8.1 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates the absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating ambient temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	$T_{.Sgt.}$	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is being applied to the device.

Table 8.2 Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations that occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	A voltage, which is applied to the input pins of the R-IN32M4, indicating that the high level state for normal operation of the input buffer. - If a voltage that is equal to or greater than the minimum value is applied, the input voltage is guaranteed as a high level voltage.
Low-level input voltage	V_{IL}	A voltage, which is applied to the input pins of the R-IN32M4, indicating that the low level state for normal operation of the input buffer. - If a voltage that is equal to or less than the maximum value is applied, the input voltage is guaranteed as a low level voltage.
Positive trigger voltage	V_P	Indicates the input level at which the output level is inverted when the input to the R-IN32M4 is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Indicates the input level at which the output level is inverted when the input to the R-IN32M4 is changed from the high-level side to the low-level side.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rising time	t_{ried}, t_{ric}, t_{ris}	Indicates the limit value for the time period when an input voltage applied to R-IN32M4 rises from 10% to 90%. t_{ried}, t_{ric}, and t_{ris} each indicate the input rising time for the data clock and Schmitt buffer.
Input falling time	t_{fid}, t_{fic}, t_{fis}	Indicates the limit value for the time period when an input voltage applied to R-IN32M4 falls from 90% to 10%. t_{fid}, t_{fic}, and t_{fis} each indicate the input falling time for the data clock and Schmitt buffer.

Table 8.3 Terms Used for DC Characteristics

Parameter	Symbol	Meaning
Off-state output current	I_{OZ}	Indicates the current that flows via an output pin when the rated voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pins are shorted to the ground when output is at high level.
Input leakage current	I_{LI}	Indicates the current that flows via an input pin when a voltage is applied to that pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.
Low-level output voltage	V_{OL}	Indicates the output voltage at low level and when the output pin is open.
High-level output voltage	V_{OH}	Indicates the output voltage at high level and when the output pin is open.

8.2 Absolute Maximum Ratings

Table 8.4 Absolute Maximum Ratings

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}	1.0 V type		-0.3 to +1.10	V
		2.5 V type		-0.3 to +2.75	V
		3.3 V type		-0.3 to +3.60	V
I/O voltage	V_I /V_O	2.5 V buffer[Note1]	-	- 0.3 to +2.75	V
		3.3 V buffer[Note2]	-	- 0.3 to +3.6	V
		3.3 V buffer[Note3]	V_I /V_O < V_{DD} + 0.5V	- 0.5 to +4.1	V
		5 V-tolerant buffer	V_I /V_O < V_{DD} + 3.0V	- 0.5 to +6.6	V
Output current (3.3 V buffer)	I_O	6 mA type		15	mA
		12 mA type		25	mA
Output current (5V-tolerant buffer)	I_O	4 mA type		10.35	mA
Operating ambient temperature	T_A	-		-40 to +85	°C
Storage temperature	$T_{.Sgt.}$	-		-65 to +125	°C

Notes 1. This applies to the PHYADD3 and PHYADD4 pins.
2. This applies to the PHYADD1, PHYADD2, TDI, TMS, and TCK pins.
3. This applies to the pins other than five pins listed in Note 2.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark: 3.3 V must be applied to the I/O pins only after applying the power supply voltage.

8.3 Recommended Operating Conditions

Table 8.5 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	1.0 V power supply	0.95	1.0	1.05	V
		2.5 V power supply	2.375	2.5	2.625	V
		3.3 V power supply	3.135	3.3	3.465	V
Negative trigger voltage	V_N	3.3 V buffer	0.6	-	1.8	V
		5 V-tolerant buffer	0.8	-	1.1	V
Positive trigger voltage	V_P	3.3-V buffer	1.2	-	2.4	V
		5 V-tolerant buffer	1.7	-	2.2	V
Hysteresis voltage	V_H	3.3-V buffer	0.3	-	1.5	V
		5 V-tolerant buffer	0.9	-	1.1	V
Low-level input voltage	V_{IL}	3.3-V buffer	- 0.3	-	0.8	V
		5 V-tolerant buffer	0	-	0.8	V
High-level input voltage	V_{IH}	3.3-V buffer	2.0	-	V_{DD} + 0.3	V
		5 V-tolerant buffer	2.0	-	5.5	V
Input rising/falling time	t_{ried}	-	0	-	200	ns
	t_{fid}	-	0	-	200	ns
Input rising/falling time (clock)	t_{ric}	-	0	-	4	ns
	t_{fic}	-	0	-	4	ns
Input rising/falling time (Schmitt input)	t_{ris}	-	0	-	1	ms
	t_{fis}	-	0	-	1	ms
Operating ambient temperature	T_A	-	- 40	-	85	°C

8.4 DC Characteristics

Table 8.6 DC Characteristics (VDD = 3.3 ±0.165V, TA = –40 to +85°C) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	IDD	VI = VDD or GND	1.0 V	-	715	1540	mA
			2.5 V	-	290	305	mA
			3.3 V	-	70	75	mA
Off-state current	I_{OZ}	V_I = V_{DD} or GND	3.3 V output	-	-	±10	μA
			5V-tolerant buffer	-	-	±10	μA
Output short circuit current Note	I_{OS}	V_O = GND	-	-	-	- 250	mA
Input leakage current (3.3 V buffer)	I_I	V_I = V_{DD} or GND	Normal input	-	-	±10	μA
		V_I = GND	With pull-up resistor (50 kΩ)	- 28.9	- 65.7	- 129.8	μA
			With pull-up resistor (25 kΩ)	-85.0	-160.0	-280.0	μA
		V_I = V_{DD}	With pull-down resistor (50 kΩ)	10.2	43.4	83.9	μA
Input leakage current (5V-tolerant buffer)	I_I	V_I = GND	With pull-up resistor (50 kΩ)	39.0	-	100.9	μA

Note: The output short circuit time is no more than one second and is only for one pin on the LSI.

Remark: The (+) and (–) signs in the table indicate the current direction. Current flowing to the device is indicated by (+) and current flowing out is indicated by (–).

Table 8.7 DC Characteristics (VDD = 3.3 ±0.165V, TA = –40 to +85°C) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level output current (3.3 V buffer)	I_{OL}	V_{OL} = 0.4V	6 mA type	6.0	-	-	mA
			12 mA type	12.0	-	-	mA
Low-level output current (5 V-tolerant buffer)	I_{OL}	V_{OL} = 0.4V	4 mA type	4.0	-	-	mA
High-level output current (3.3 V buffer)	I_{OH}	V_{OH} = 2.4V	6 mA type	- 6.0	-	-	mA
			12 mA type	- 12.0	-	-	mA
High-level output current (5 V-tolerant buffer)	I_{OH}	V_{OH} = 2.4V	4 mA type	- 4.0	-	-	mA
Low-level output voltage	V_{OL}	I_{OL} = 0mA	3.3 V buffer	-	-	0.1	V
			5 V-tolerant buffer	-	-	0.1	V
High-level output voltage	V_{OH}	I_{OH} = 0mA	3.3 V buffer	V_{DD} - 0.1	-	-	V
			5 V-tolerant buffer	V_{DD} - 0.1	-	-	V

8.5 Pull-Up/Pull-Down Resistor Values

Table 8.8 Pull-Up/Pull-Down Resistor Values (VDD = 3.3 ±0.165V, TA = –40 to +85°C)

Parameter	Library Specification	MIN.	TYP.	MAX.	Unit
Pull-up resistor (3.3V buffer)	50 kΩ	24	45	78	kΩ
Pull-up resistor (3.3V buffer) (TCK, TMS, TDI)	25 kΩ	10	21	40	kΩ
Pull-down resistor (3.3V buffer)	50 kΩ	24	45	78	kΩ
Pull-up resistor (5V-tolerant buffer)	50 kΩ	35.7	51.2	77.0	kΩ

8.6 Pin Capacitance

Table 8.9 Pin Capacitance

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input buffer	C_B	5.0	-	7.0	pF
Output buffer		5.0	-	7.0	pF
I/O buffer		5.0	-	7.0	pF

8.7 Power-On/Off Sequence

Table 8.10 lists external power supplies to the R-IN32M4 and GbE-PHY. Figure 8.1 shows the power-on/off sequence.

There are no particular restrictions regarding the order in which power voltages being supplied. However, we recommend supplying external power voltage VDD10 and then supplying external power voltage VDD33. Conversely, when turning off power, disconnect VDD33, then VDD10.

If VDD33 is supplied first, note that the I/O modes of the I/O buffers are not fixed and outputs become undefined over the period between VDD33 and VDD10 rising to their thresholds.

3.3 V must be applied to the I/O pins only after the power supply voltages have been applied.

Table 8.10 External Power Supplies

External Power Supply	Voltage [V]	Supplied to	External Pin Name
VDD33	3.3±0.165	R-IN32M4	VDD33 AVDD
		GbE-PHY	VDD33_GPHY
VDD25	2.5±0.125	GbE-PHY	VDD25A
VDD10	1.0±0.05	R-IN32M4	VDD10 PLL_VDD
		GbE-PHY	VDD1 VDD1A

(1) Supplying Power Voltages

Supply power voltages such that the following two conditions are both satisfied.

1) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 10% of VDD to all VDDs at least having reached 90% of VDD is within 100 ms.
2) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 95% of VDD to all VDDs at least having reached 95% of VDD is within 50 ms.

(2) Turning Off Power Voltages

Turn off power voltages such that the following two conditions are both satisfied.

1) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 90% of VDD to all VDDs at least having reached 10% of VDD is within 100 ms.
2) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 95% of VDD to all VDDs at least having reached 95% of VDD is within 50 ms.

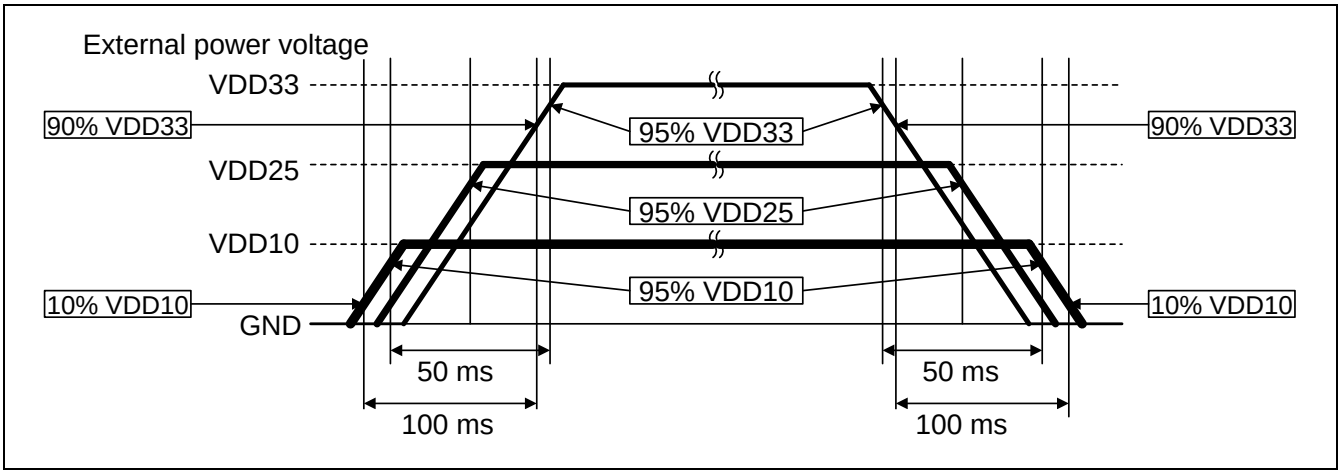


Figure 8.1 Power-On/Off Sequence

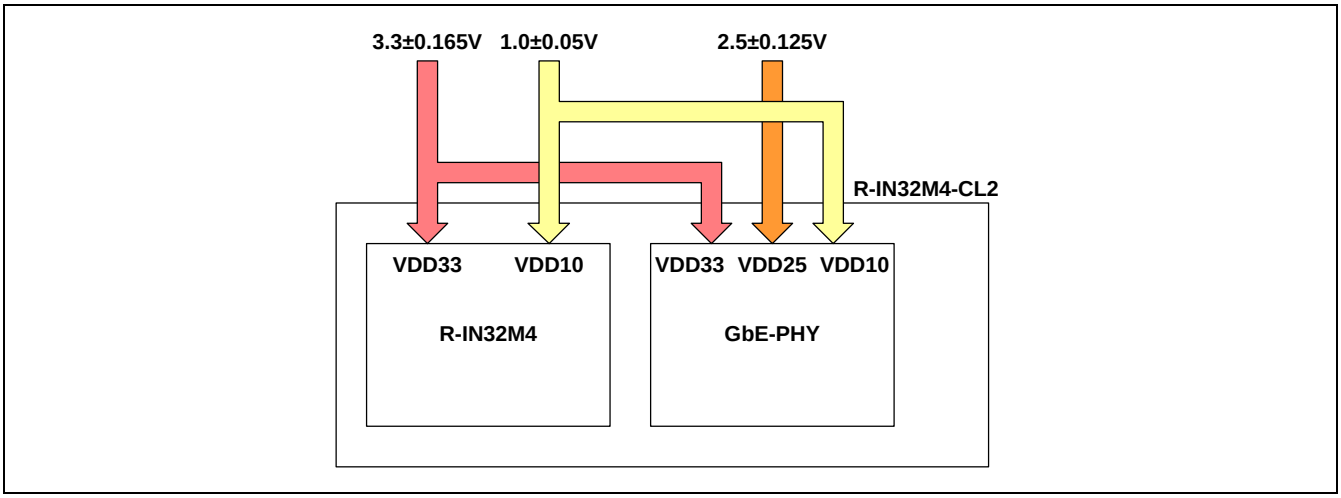


Figure 8.2 Power Supply Path to the R-IN32M4 Chip and GbE-PHY

8.8 AC Characteristics

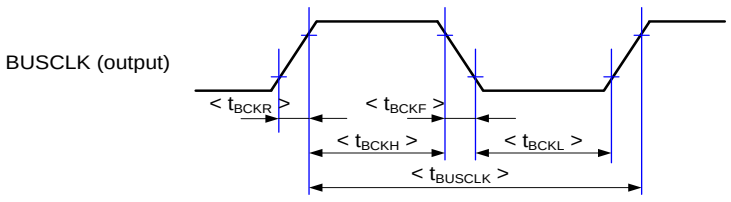
8.8.1 Clock Pins

(1) Input Clocks

Parameter	Symbol	Conditions	MIN	MAX	Unit
XT1, XT2	t_{SYSCLK}	-	25 ±50ppm, 5ps-rms		MHz
CCM_CLK80M	t_{CCLCLK}	-	80 ±50ppm		MHz
CCI_CLK2_097M	$t_{CCLIECLK}$	-	2.097152 ±100ppm		MHz
HBUSCLK	$t_{HBUSCLK}$	-	-	50	MHz
CSISCK0, CSISCK1	$t_{CSISSCK}$	Slave mode	-	16.6	MHz
TCK	t_{TCK}	-	-	50	MHz

(2) Output Clocks

Parameter	Symbol	Conditions	MIN	MAX	Unit
BUSCLK output cycle	t_{BUSCLK}	C_L = 15 pF	10	-	ns
BUSCLK high-level width	t_{BCKH}		0.5 × t_{BUSCLK} -2.0	0.5 × t_{BUSCLK} +2.0	ns
BUSCLK low-level width	t_{BCKL}		0.5 × t_{BUSCLK} -2.0	0.5 × t_{BUSCLK} +2.0	ns
BUSCLK rising time	t_{BCKR}		-	1.2	ns
BUSCLK falling time	t_{BCKF}		-	1.2	ns
CSISCK0 and CSISCK1 output frequency	$t_{CSIMSCK}$	Master mode C_L = 15 pF	-	25	MHz
SCL0 and SCL1 output frequency	t_{SCL}	High-speed mode C_L = 30 pF	-	400	kHz
SMSCK output frequency	t_{SMSCK}	C_L = 15 pF	-	50	MHz
TRACECLK output frequency	$t_{TRACECLK}$	C_L = 15 pF	-	50	MHz



* For other clocks, refer to the AC characteristic of each interface.

Figure 8.3 Output Clock Timing

8.8.2 Reset Pins

Parameter	Symbol	Conditions	MIN	MAX	Unit
RESETZ input low-level width	t_{WRSL}	-	The time required for the time (until the external oscillator be stable + 1 µsec)	-	ns
HOTRESETZ input low-level width	t_{WHRSL}	-		-	ns
PONRZ input low-level width	t_{WPRSL}	-		-	ns
PONRZ input timing (for RESETZ ↑)	t_{SKPR}	-	0	-	ns

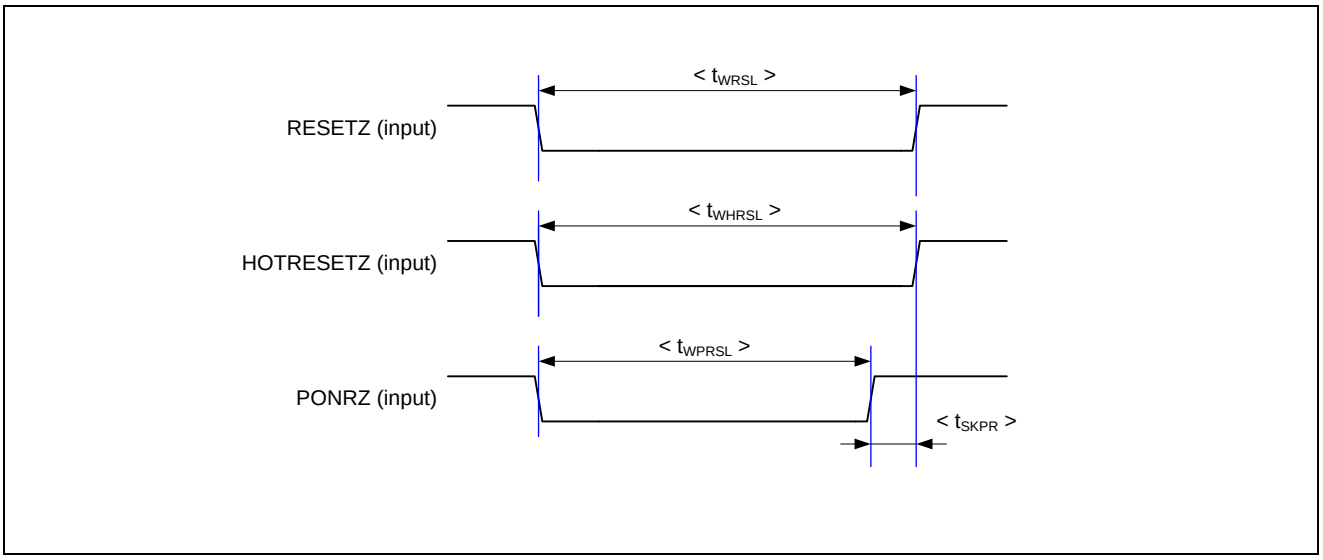


Figure 8.4 Reset Timing

8.8.3 External Memory Interface Pins

(1) Formula for calculating a delay value due to the external load

For the external memory interface pins of R-IN32M4, the listed values are for a load of 0 pF, but the actual loads will differ with the user. Calculate the timing according to the load conditions of the user. The user must also take the wiring delay on the board into account.

Driving Ability	Delay Value per pF (ns)	
	MIN.	MAX.
6 mA	0.026	0.067
12 mA	0.012	0.034

Calculation Example:

When an address pin (6-mA output buffer) has a 30-pF load, the actual delay is as follows.

MIN. 1.0 ns (the minimum delay value for a load of 0 pF) + (0.026 × 30) ns = 1.78 ns
MAX. 7.0 ns (the maximum delay value for a load of 0 pF) + (0.067 × 30) ns = 9.01 ns

(2) Asynchronous SRAM memory controller access timing

Parameter	Symbol	MIN	MAX	Unit
Address and CSZ0-CSZ3 output delay time (for BUSCLK ↑)	t_{DKA}	1.0 (1.78) Note	7.0 (9.01) Note	ns
RDZ output delay time (for BUSCLK ↑)	t_{DKRD}	1.0 (1.78) Note	7.0 (9.01) Note	ns
WRZ0 - WRZ3 (BENZ0-BENZ3), and WRSTBZ output delay time (for BUSCLK ↑)	t_{DKWR}	1.0 (1.78) Note	7.0 (9.01) Note	ns
BCYSTZ output delay time (for BUSCLK ↑)	t_{DKBSL}	1.0 (1.78) Note	7.0 (9.01) Note	ns
WAITZ input setup time (for BUSCLK ↓)	t_{SKW}	4.0	-	ns
WAITZ input hold time (for BUSCLK ↓)	t_{HKW}	0	-	ns
Data input setup time (for BUSCLK ↑)	t_{SKID}	4.0	-	ns
Data input hold time (for BUSCLK ↑)	t_{HKID}	0	-	ns
Data output delay time (for BUSCLK ↑)	t_{DKOD}	1.0 (1.78) Note	7.0 (9.01) Note	ns
Data float delay time (for BUSCLK ↑)	t_{HKOD}	1.0 (1.78) Note	7.0 (9.01) Note	ns

Note: Values in parenthesis are for a load of 30 pF.

(a) Read timing

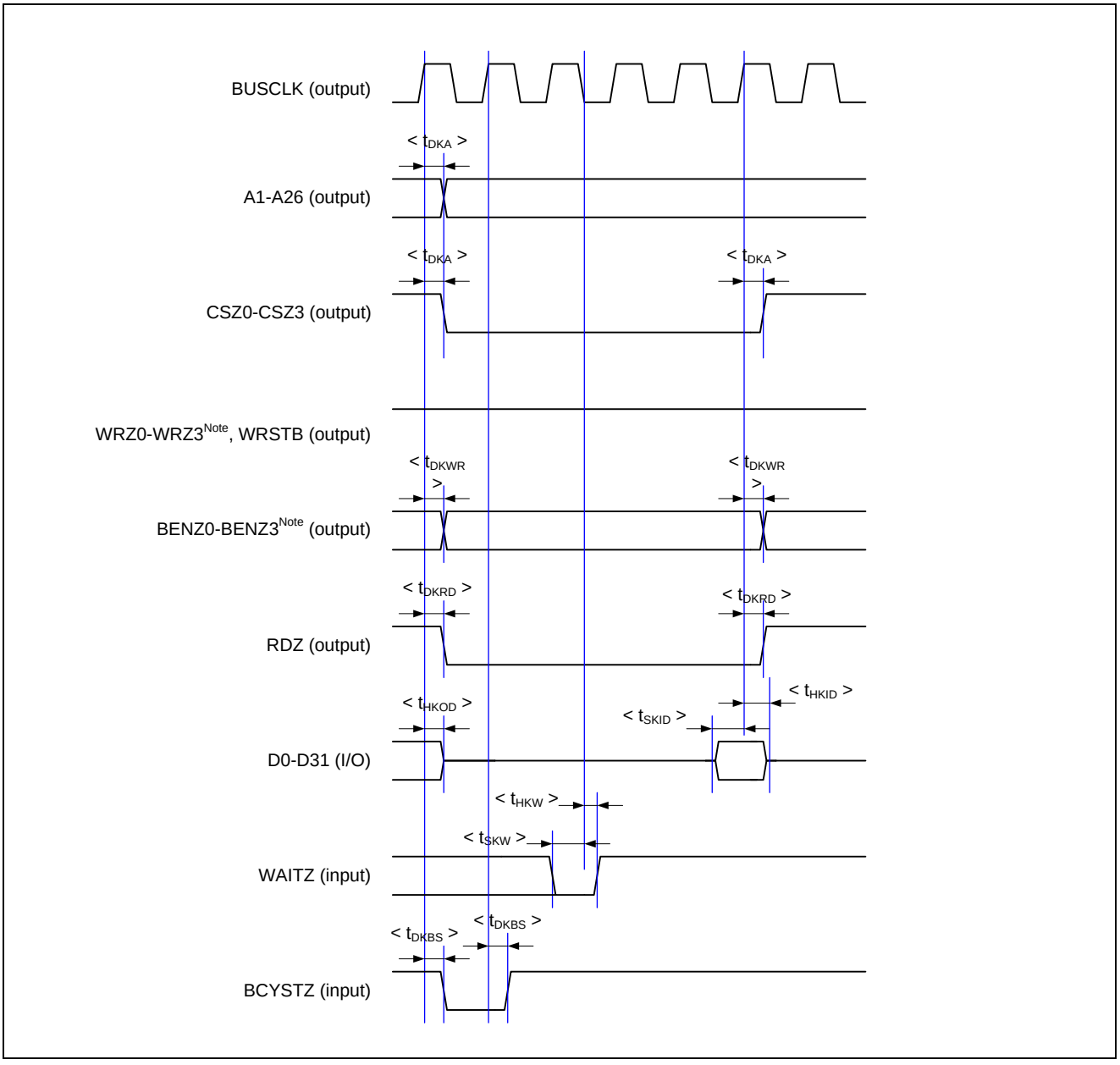


Figure 8.5 Memory Controller Read Timing (Asynchronous Memory)

Note: The WRZ0 to WRZ3 pins are multiplexed with the BENZ0 to BENZ3 pin functions. The pin names are WRZ0 to WRZ3. The WRZ0 to WRZ3 pins are selected by default during a reset. Use the write-enable switching register (WREN) to switch the pin functions of these pins.

Remark: The above timing is for the case where the settings in the SMCn register for numbers of idle wait cycles, write recovery wait cycles, and address setting wait cycles are 0, and that for data wait cycles is 3.

(b) Write timing

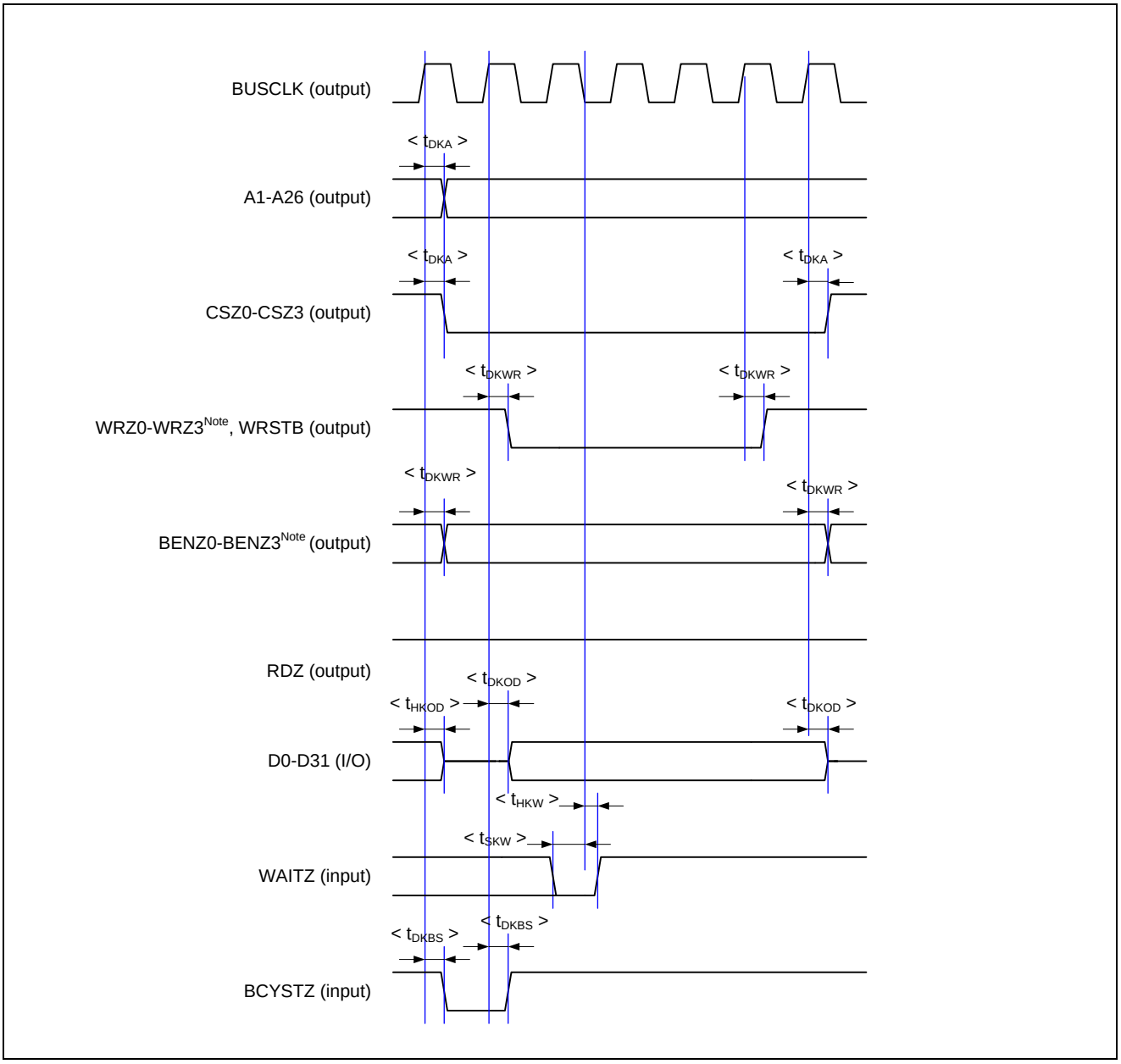


Figure 8.6 Memory Controller Write Timing (Asynchronous Memory)

Note: The WRZ0 to WRZ3 pins are multiplexed with the BENZ0 to BENZ3 pin functions. The pin names are WRZ0 to WRZ3. The WRZ0 to WRZ3 pins are selected by default during a reset. Use the write-enable switching register (WREN) to switch the pin functions of these pins.

Remark: The above timing is for the case where the settings in the SMCn register for numbers of idle wait cycles, write recovery wait cycles, and address setting wait cycles are 0, and that for data wait cycles is 3.

(3) Synchronous burst access memory controller access timing

Parameter	Symbol	MIN	MAX	Unit
BUSCLK output frequency	t_{BUSCLK}	-	50	MHz
Address and CSZ0 to CSZ3 output delay time	t_{DKA}	1.0 (1.78) Note	7.8 (9.81) Note	ns
RDZ output delay time	t_{DKRD}	1.0 (1.78) Note	7.8 (9.81) Note	ns
WRZ0 to WRZ3 (BENZ0 to BENZ3) and WRSTBZ output delay time	t_{DKWR}	1.0 (1.78) Note	7.8 (9.81) Note	ns
ADVZ output delay time	t_{DKBSL}	1.0 (1.78) Note	7.8 (9.81) Note	ns
WAITZ and WAITZ1 to 3 input setup time	t_{SKW}	5.3	-	ns
WAITZ and WAITZ1 to 3 input hold time	t_{HKW}	0	-	ns
Data input setup time	t_{SKID}	5.3	-	ns
Data input hold time	t_{HKID}	0	-	ns
Data output delay time	t_{DKOD}	1.0 (1.78) Note	7.8 (9.81) Note	ns
Data float delay time	t_{HKOD}	1.0 (1.78) Note	7.8 (9.81) Note	ns

Note: Values in parenthesis are for a load of 30 pF.

(a) Read timing

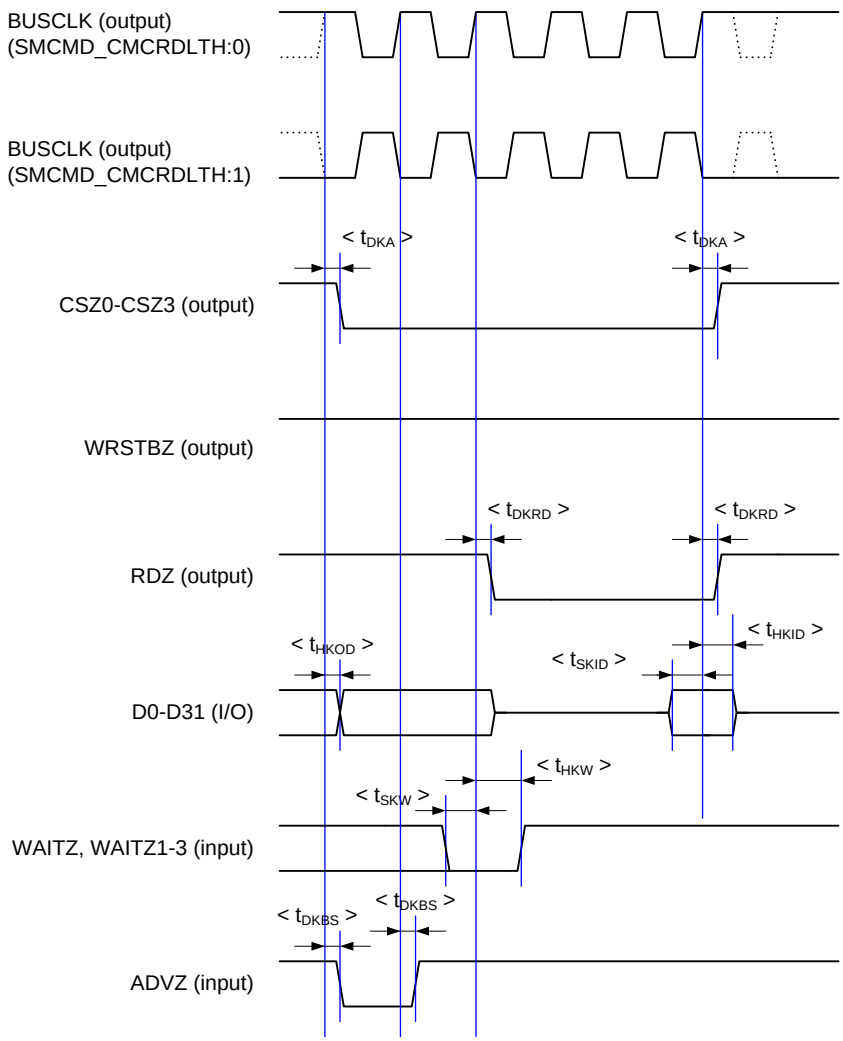


Figure 8.7 Memory Controller Read Timing (Clock Synchronous Memory)

Remark: The above timing is for the case where t_ceoe is 2 and t_rc is 4.

(b) Write timing

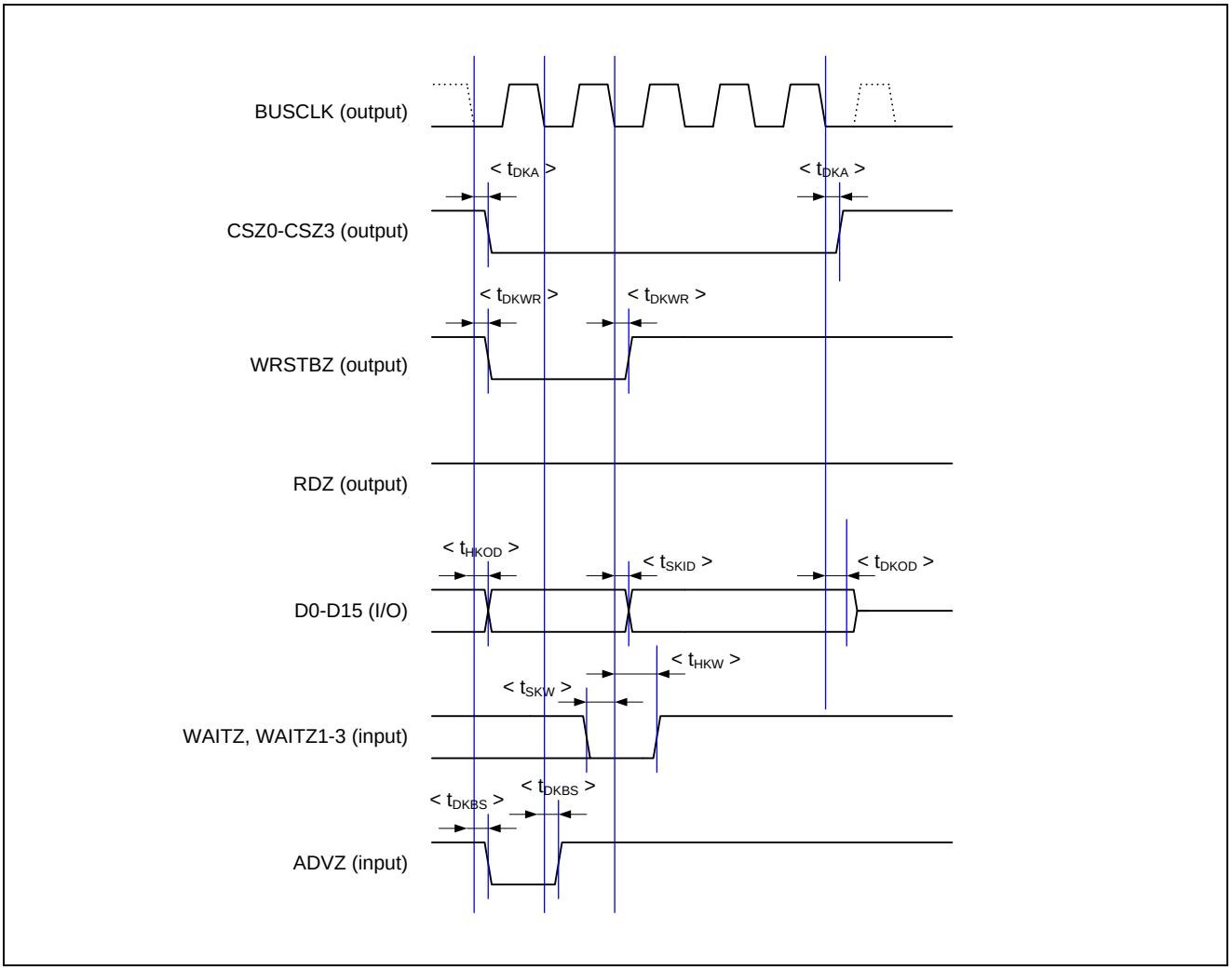


Figure 8.8 Memory Controller Write Timing (Clock Synchronous Memory)

Remark: The above timing is for the case where t_wp is 2 and t_wc is 5.

8.8.4 External MCU Interface Pins

The load condition for the external MCU interface pins: 65 pF (HD pin) and 35 pF (HWAITZ pin).

(1) Synchronous mode

No.	Parameter	Symbol	MIN	MAX	Unit
1	HBUSCLK high-level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
2	HBUSCLK low-level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20.0	-	ns
4	Address, HCSZ, HPGCSZ, and HRDZ input setup time (for HBUSCLK ↑)	t_{SKHA}	4.0	-	ns
5	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input setup time (for HBUSCLK ↑)	t_{SKHWR}	4.0	-	ns
6	Address, HCSZ, HPGCSZ, and HRDZ input hold time (for HBUSCLK ↑)	t_{HKHA}	1.0	-	ns
7	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input hold time (for HBUSCLK ↑)	t_{HKHWR}	1.0	-	ns
8	HWRZ0-HWRZ3, HWRSTBZ recovery time (high-level width)	t_{WHWR}	35.0	-	ns
9	Data input setup time (for HBUSCLK ↑)	t_{SKIHD}	4.0	-	ns
10	Data input hold time (for HBUSCLK ↑)	t_{HKIHD}	1.0	-	ns
11	HWAITZ output delay time (for HCSZ, HPGCSZ ↓)	t_{DKHD}	2.2	-	ns
12	HWAITZ output delay time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{DKHWT}	2.2	-	ns
13	HWAITZ valid data output delay time (for HBUSCLK ↑)	t_{DKHWTV}	2.0	11.0	ns
14	HWAITZ valid data hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{HKHWTV}	4.2	-	ns
15	HWAITZ output hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{HKWTWR}	-	16.8	ns
16	Data and HWAITZ output hold time (for HCSZ, HPGCSZ ↑)	t_{HKWTCS}	-	16.8	ns
17	HRDZ recovery time (high-level width)	t_{WHRD}	35.0	-	ns
18	Data, HWAITZ output delay time (for HRDZ ↓)	t_{DKHDHR}	2.2	-	ns
19	Data fixing time (for HWAITZ ↑)	$t_{SKHDHWT}$	$t_{HBUSCLK}$-10.0	-	ns
20	Data and HWAITZ valid data output hold time (for HRDZ ↑)	$t_{HKHWTHR}$	2.2	-	ns
21	Data and HWAITZ output hold time (for HRDZ ↑)	t_{HKOHD}	-	16.8	ns
22	Data and HWAITZ output delay time in on-page access (for addresses)	t_{DKPON}	4.2	15.4	ns
23	Data and HWAITZ output delay time in off-page access (for addresses) (when not crossing a 16-byte boundary)	t_{DKPOFF}	4.2	15.4	ns
	Data and HWAITZ output delay time in off-page access (for addresses) (when crossing a 16-byte boundary)	t_{DKPOFF}	4.2	49.5	ns
24	HWAITZ valid data output delay time (for HCSZ, HPGCSZ ↓)	$t_{DKWTVCS}$	-	15.4	ns

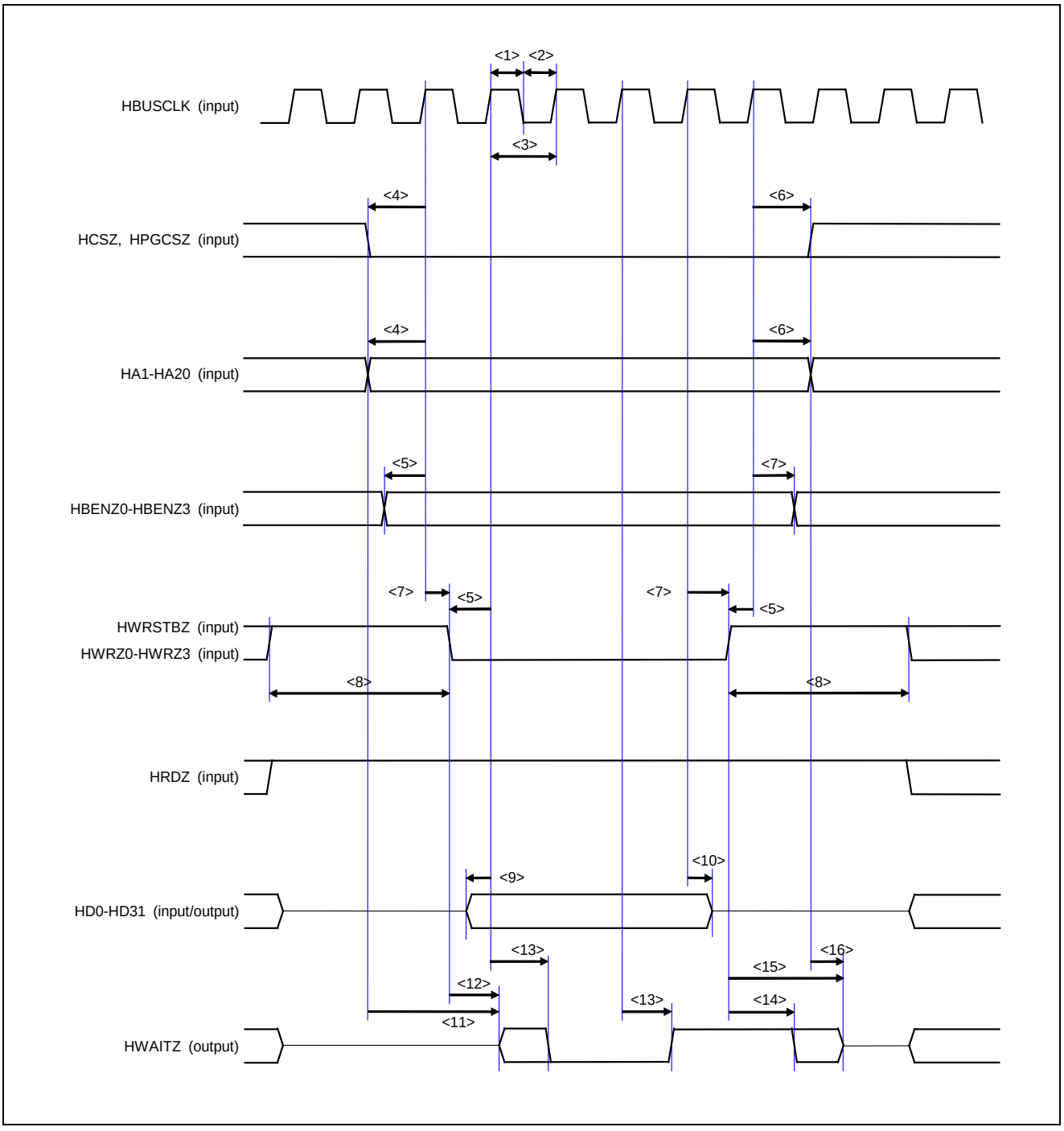


Figure 8.9 External MCU Interface Write Timing (MEMCSEL=L, HIFSYNC=H)

Caution: Supply a stable signal to the address, data, and control lines during access.

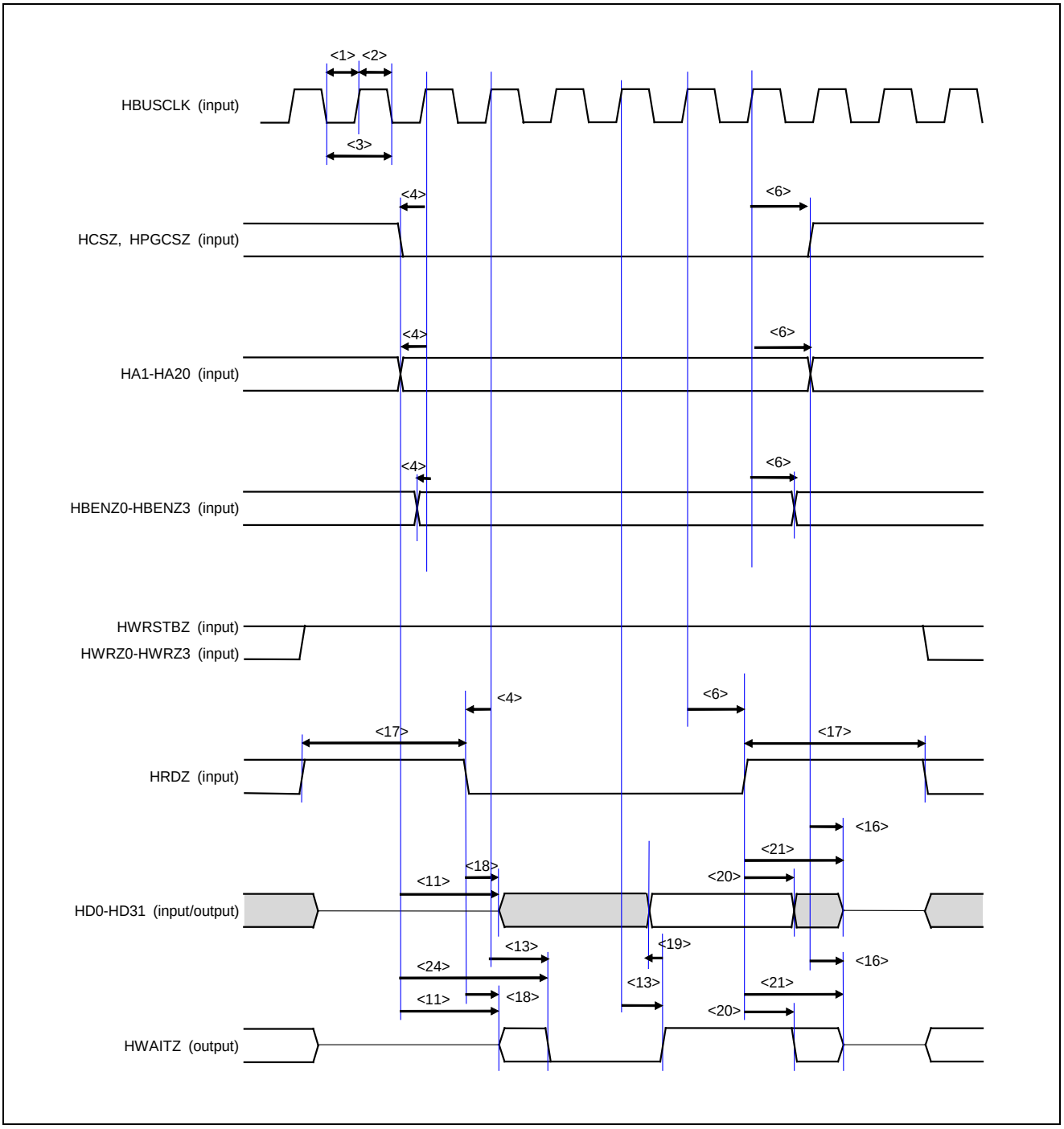


Figure 8.10 External MCU Interface Read Timing (MEMCSEL=L, HIFSYNC=H)

Caution: Supply a stable signal to the address, data, and control lines during access.

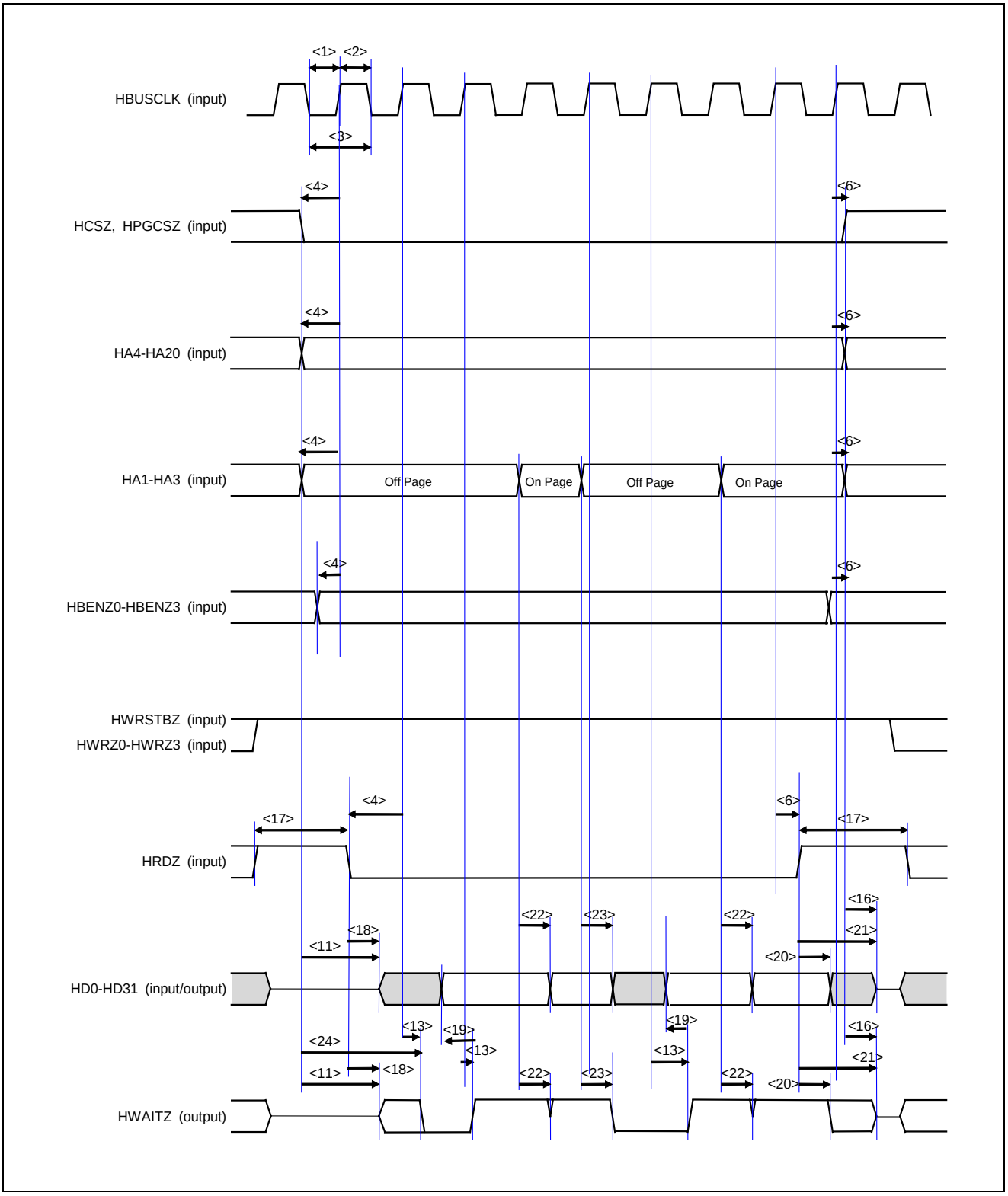


Figure 8.11 External MCU Interface Page Read Timing (MEMCSEL=L, HIFSYNC=H)

Caution: Supply a stable signal to the address, data, and control lines during access.

(2) Synchronous mode (CC-Link IE Field)

No.	Parameter	Symbol	MIN	MAX	Unit
1	HBUSCLK high-level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
2	HBUSCLK low-level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20.0	-	ns
4	Address, HCSZ, HPGCSZ, input setup time (for HBUSCLK ↓)	t_{SKHCS}	4.0	-	ns
5	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input setup time (for HBUSCLK ↓)	t_{SKHWR}	4.0	-	ns
6	Address, HCSZ, HPGCSZ, HBENZ0-HBENZ3, data input hold time (for HRDZ, HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{HKHA}	0	-	ns
7	HWRZ0-HWRZ3, HWRSTBZ recovery time (high-level width)	t_{WHWR}	$t_{HBUSCLK}$ x 1	-	ns
8	Data input setup time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{SKIHD}	0	-	ns
9	HWAITZ output delay time (for HCSZ, HPGCSZ ↓)	t_{DKHD}	2.2	-	ns
10	HWAITZ output delay time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{DKHWT}	2.2	-	ns
11	HWAITZ valid data output delay time (for HBUSCLK ↑) HWAITZ output is in HBUSCLK ↑ synchronous mode.	t_{DKHWTV}	4.0	12.0	ns
	HWAITZ valid data output delay time (for HBUSCLK ↓) HWAITZ output is in HBUSCLK ↓ synchronous mode.	t_{DKHWTV}	4.0	12.0	ns
12	HWAITZ valid data hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{HKHWTV}	4.2	-	ns
13	HWAITZ output hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{HKWTWR}	-	16.8	ns
14	Data and HWAITZ output hold time (for HCSZ, HPGCSZ ↑)	t_{HKWTCS}	-	16.8	ns
15	HRDZ recovery time (high-level width)	t_{WHRD}	$t_{HBUSCLK}$ x 1	-	ns
16	Data and HWAITZ output delay time (for HRDZ ↓)	t_{DKHDHR}	2.2	-	ns
17	HWAITZ valid data output delay time (latch timing for HRDZ, HWWRSTBZ, HWRZ0 - HWRZ3) HWAITZ output is in HBUSCLK ↑ synchronous mode.	$t_{DKWTVHR}$	-	$t_{HBUSCLK}$/2 + 12.0	ns
	HWAITZ valid data output delay time (latch timing for HRDZ, HWWRSTBZ, HWRZ0 - HWRZ3) HWAITZ output is in HBUSCLK ↓ synchronous mode.	$t_{DKWTVHR}$	-	$t_{HBUSCLK}$ + 12.0	ns
18	Data fixing time (for HWAITZ ↑) HWAITZ output is in HBUSCLK ↑ synchronous mode.	$t_{SKHDHWT}$	6.23	-	ns
	Data fixing time (for HWAITZ ↑) HWAITZ output is in HBUSCLK ↓ synchronous mode.	$t_{SKHDHWT}$	16.2	-	ns
19	Data and HWAITZ valid data output hold time (for HRDZ ↑)	$t_{HKHWTHR}$	4.2	-	ns
20	Data and HWAITZ output hold time (for HRDZ ↑)	t_{HKOHD}	-	16.8	ns
21	HRDZ input setup time (for HBUSCLK ↓)	t_{SKHRD}	4.0	-	ns

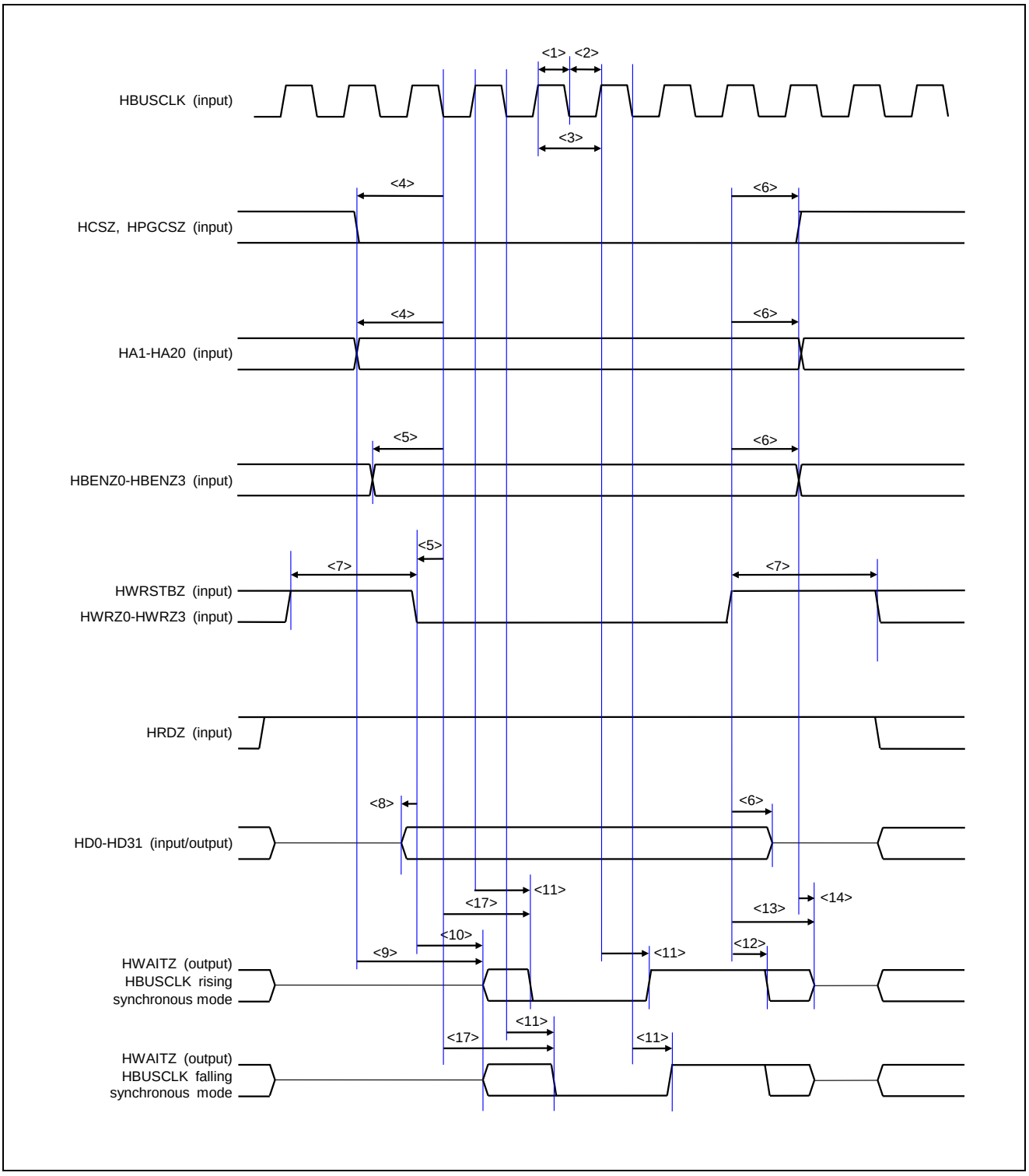


Figure 8.12 External MCU Interface Write Timing (MEMCSEL=L, HIFSYNC=H)

Caution: Supply a stable signal to the address, data, and control lines during access.

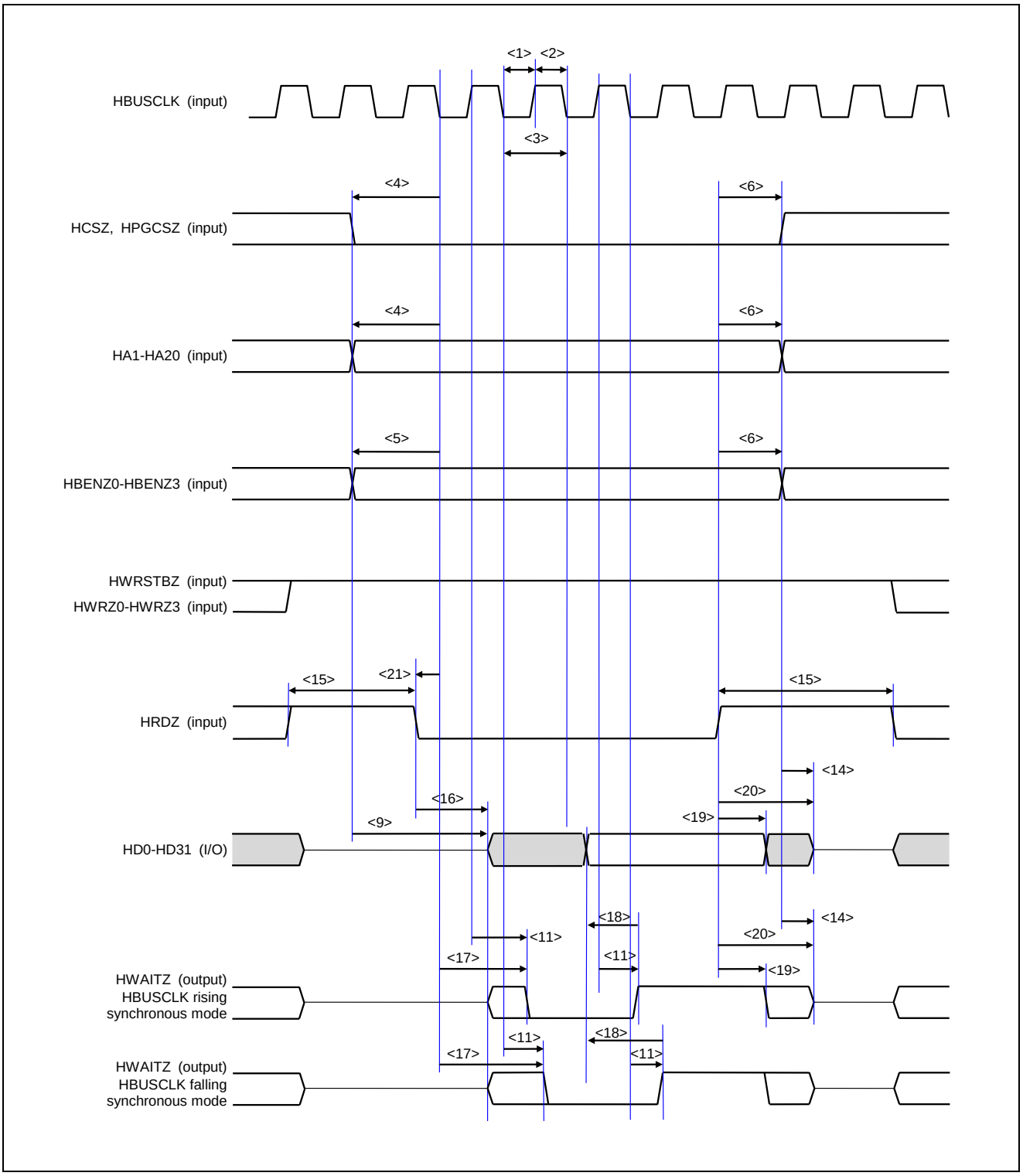


Figure 8.13 External MCU Interface Read Timing (MEMCSEL=L, HIFSYNC=H)

Caution: Supply a stable signal to the address, data, and control lines during access.

(3) Asynchronous mode

No.	Parameter	Symbol	MIN	MAX	Unit
1	Address, HCSZ/HPGCSZ, and HBENZ0-HBENZ3 input setup time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{ADDWRS}	7.0 Note 1 - 10×n	-	ns
2	HWRZ0-HWRZ3 and HWRSTBZ recovery time (high-level width)	t_{WRW}	35.0	-	ns
3	Data input setup time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{WRS}	7.0 Note1 - 10×n	-	ns
4	Data input hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{WRH}	7.0	-	ns
5	HWAITZ output delay time (for HCSZ or HPGCSZ ↓)	t_{CLZ}	2.2	-	ns
6	HWAITZ output delay time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{WAITD}	2.2	-	ns
7	HWAITZ valid data output delay time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	$t_{WRWAITF}$	-	15.4	ns
8	HWAITZ valid data output hold time (for HWRSTBZ , HWRZ0-HWRZ3 ↑)	t_{WAITVH}	4.2	-	ns
9	HWAITZ output hold time (for HWRZ0-3, HWRSTBZ ↑)	t_{WAITH}	-	16.8	ns
10	Address and HWAITZ output hold time (for HCSZ, HPGCSZ ↑)	t_{CHZ}	-	16.8	ns
11	Address and HCSZ, HPGCSZ input setup time (for HRDZ ↓)	t_{ADDRDS}	6.2 Note 2 - 10×n	-	ns
12	Address input hold time in pace access (for HRDZ ↑)	t_{ADDRDH}	7.0	-	ns
13	HRDZ recovery time (high-level width)	t_{RDW}	35.0	-	ns
14	Data, HWAITZ output delay time (for HRDZ ↓)	t_{RDLZ}	2.2	-	ns
15	HWAITZ valid data output delay time (for HRDZ ↓)	$t_{RDWAITF}$	-	15.4	ns
16	Data fixing time (for HWAITZ ↑)	t_{WAITR}	-	-6.2 Note 3 +10×n	ns
17	Data and HWAITZ valid data output hold time (for HRDZ ↑)	t_{DATAOH}	2.2	-	ns
18	Data and HWAITZ output hold time (for HRDZ ↑)	t_{RDHZ}	-	16.8	ns
19	Data and HWAITZ output delay time in on-page access (for addresses)	$t_{PAGEOND}$	4.2	15.4	ns
20	Data and HWAITZ output delay time in off-page access (for addresses) (when not crossing a 16-byte boundary)	$t_{PAGEOFD}$	4.2	15.4	ns
	Data and HWAITZ output delay time in off-page access (for addresses) (when crossing a 16-byte boundary)	$t_{PAGEOFD}$	4.2	49.5	ns
21	HWAITZ valid data output delay time (for HCSZ, HPGCSZ ↓)	t_{WAITVD}	-	15.4	ns

Notes 1. When the value of WRSTD2 to WRSTD0 in the HIFBTC register is 000B.
n: setting of WRSTD2 to WRSTD0
2. When the value of RDSTD1 to RDSTD0 in the HIFBTC register is 00B.
n: setting of RDSTD1 to RDSTD0
3. When the value of RDDTS1 to RDDTS0 in the HIFBTC is 00B.
n: setting of RDDTS1 to RDDTS0

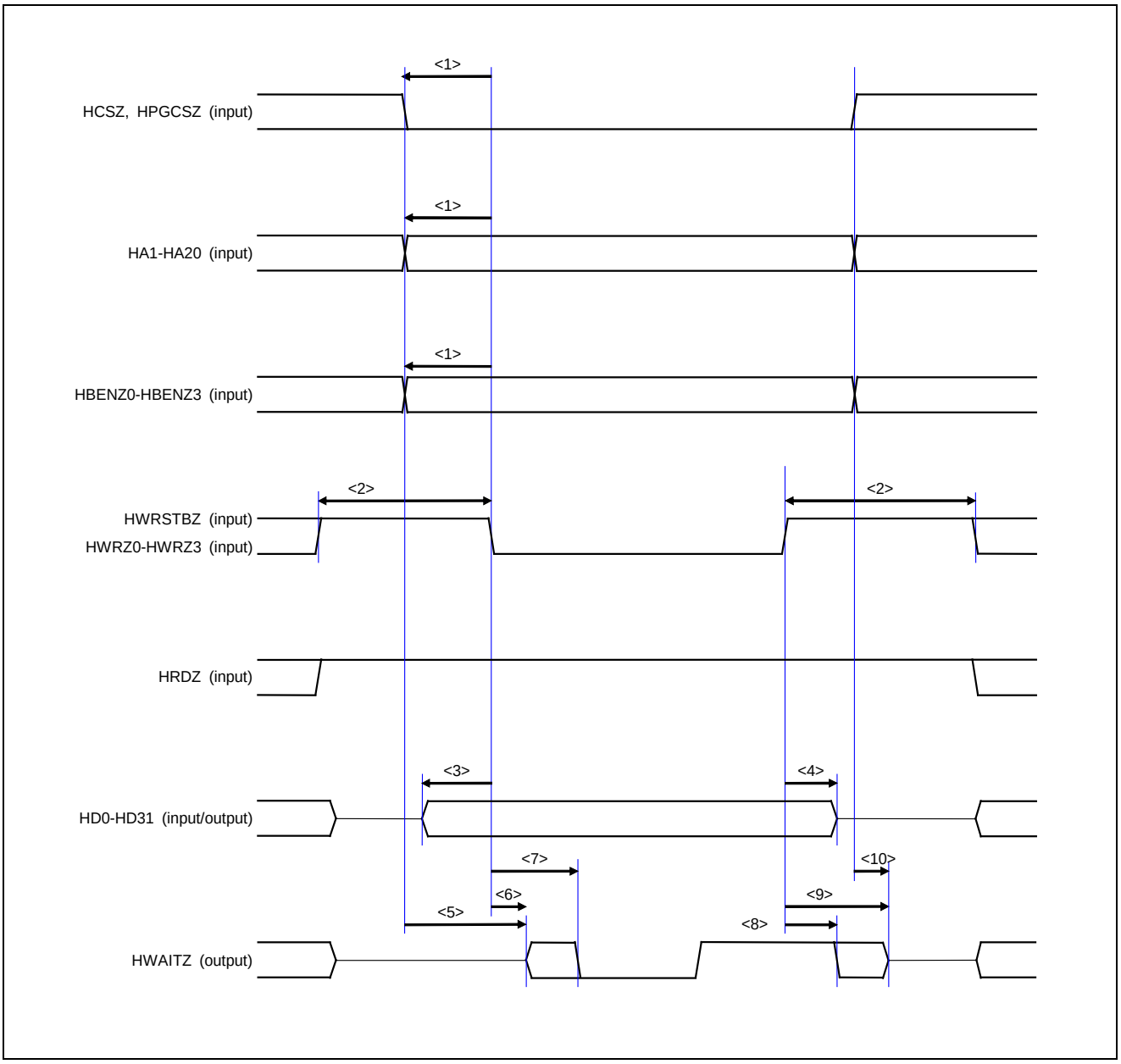


Figure 8.14 External MCU Interface Write Timing (MEMCSEL=L, HIFSYNC=L)

Caution: Supply a stable signal to the address, data, and control lines during access.

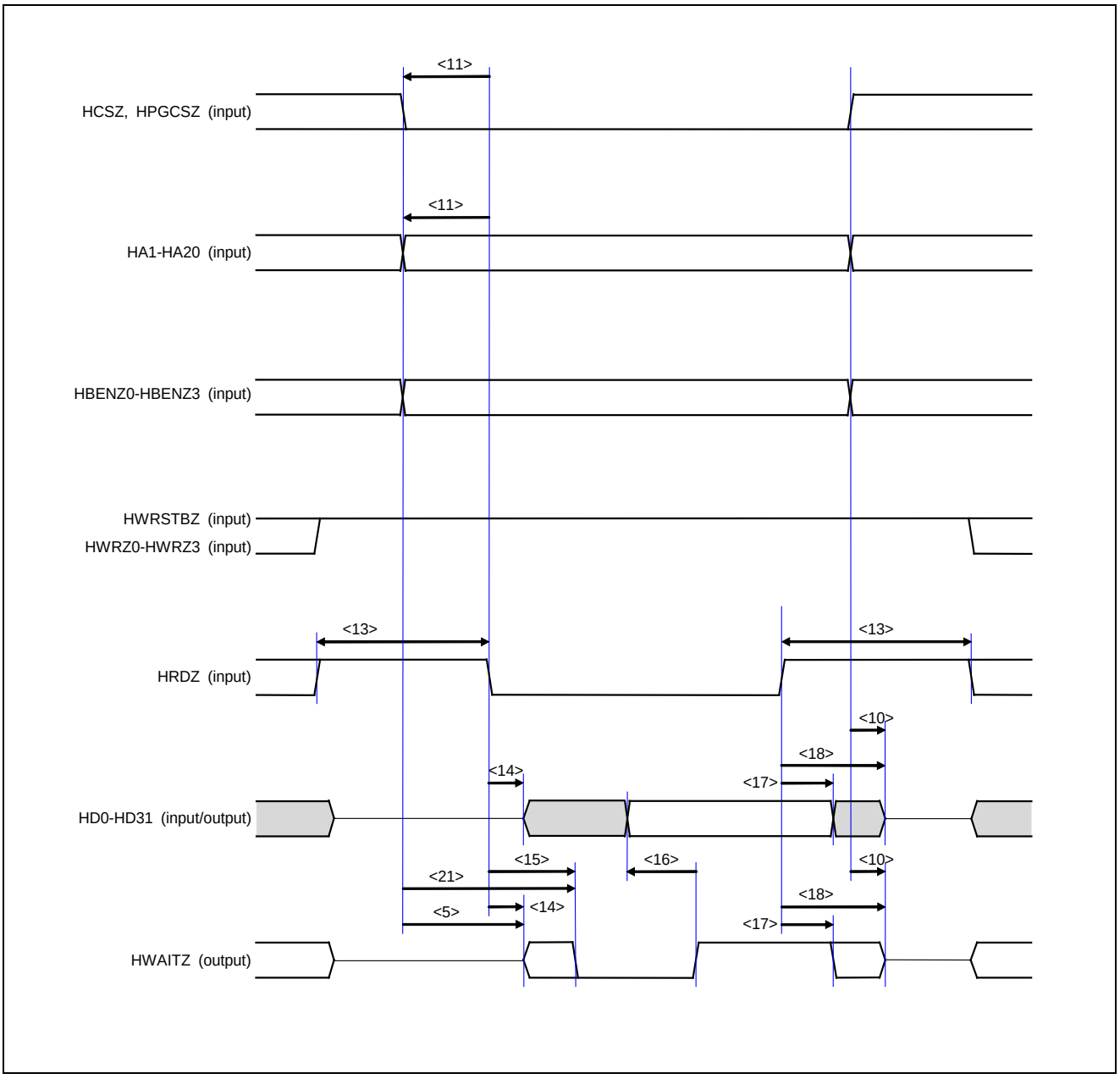


Figure 8.15 External MCU Interface Read Timing (MEMCSEL=L, HIFSYNC=L)

Caution: Supply a stable signal to the address, data, and control lines during access.

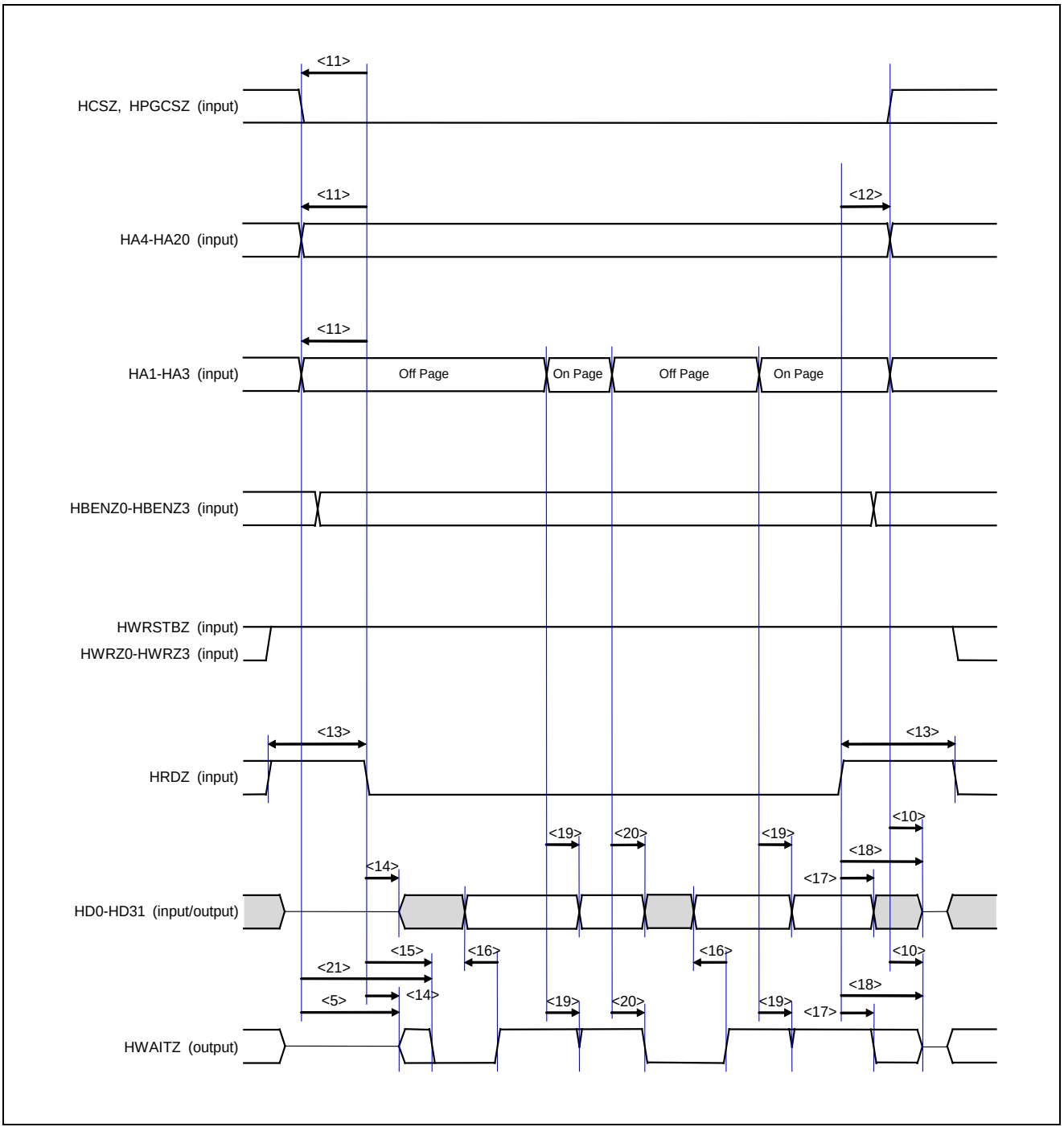


Figure 8.16 External MCU Interface Page Read Timing (MEMCSEL=L, HIFSYNC=L)

Caution: Supply a stable signal to the address, data, and control lines during access.

(4) Synchronous SRAM type transfer mode

No.	Parameter	Symbol	MIN	MAX	Unit
1	HBUSCLK high-level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$ -2.1	$0.5t_{HBUSCLK}$ +2.1	ns
2	HBUSCLK low-level width	t_{HBLOW}	$0.5t_{HBUSCLK}$ -2.1	$0.5t_{HBUSCLK}$ +2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20	-	ns
4	Address and HCSZ/HPGCSZ input setup time (for HBUSCLK ↑)	t_{SKPHA}	4.0	-	ns
5	Address and HCSZ/HPGCSZ input hold time (for HBUSCLK ↑)	t_{HKPCS}	1.0	-	ns
6	Address and HCSZ/HPGCSZ input setup time (for HBUSCLK ↓)	t_{SKNHA}	4.0	-	ns
7	Address and HCSZ, HPGCSZ input hold time (for HBUSCLK ↓)	t_{HKNHA}	1.0	-	ns
8	HWRZ0-HWRZ3 input setup time (for HBUSCLK ↑)	t_{SKPHWR}	4.0	-	ns
9	HWRZ0-HWRZ3 input hold time (for HBUSCLK ↑)	t_{HKPHWR}	1.0	-	ns
10	HWRZ0-HWRZ3 input setup time (for HBUSCLK ↓)	t_{SKNHWR}	4.0	-	ns
11	HWRZ0-HWRZ3 input hold time (for HBUSCLK ↓)	t_{HKNHWR}	1.0	-	ns
12	HBCYSTZ and HWRSTBZ input setup time (for HBUSCLK ↑)	$t_{SKPHBCY}$	4.0	-	ns
13	HBCYSTZ and HWRSTBZ input hold time (for HBUSCLK ↑)	$t_{HKPHBCY}$	1.0	-	ns
14	HBCYSTZ and HWRSTBZ input setup time (for HBUSCLK ↓)	$t_{SKNHBCY}$	4.0	-	ns
15	HBCYSTZ and HWRSTBZ input hold time (for HBUSCLK ↓)	$t_{HKNHBCY}$	1.0	-	ns
16	HRDZ input setup time (for HBUSCLK ↑)	t_{SKPHRD}	4.0	-	ns
17	HRDZ input hold time (for HBUSCLK ↑)	t_{HKPHRD}	1.0	-	ns
18	HRDZ input setup time (for HBUSCLK ↓)	t_{SKNHRD}	4.0	-	ns
19	HRDZ input hold time (for HBUSCLK ↓)	t_{HKNHRD}	1.0	-	ns
20	Data input setup time (for HBUSCLK ↑)	t_{SKPHD}	4.0	-	ns
21	Data input hold time (for HBUSCLK ↑)	t_{HKPHD}	1.0	-	ns
22	Data input setup time (for HBUSCLK ↓)	t_{SKNHD}	4.0	-	ns
23	Data input hold time (for HBUSCLK ↓)	t_{HKNHD}	1.0	-	ns
24	Data output delay time (for HRDZ ↓)	t_{DKNHRD}	2.2	-	ns
25	Data output hold time (for HRDZ ↑)	t_{HKPHRD}	-	16.8	ns
26	Data output delay time (for HBUSCLK ↑)	t_{DKPHD}	2.0	10.0	ns
27	Data output delay time (for HBUSCLK ↓)	t_{DKNHD}	2.0	10.0	ns
28	HWAITZ output delay time (for HBUSCLK ↑)	t_{DKPHWT}	2.0	11.0	ns
29	HWAITZ output delay time (for HBUSCLK ↓)	t_{DKNHWT}	2.0	11.0	ns
30	Data output hold time (for HCSZ/HPGCSZ ↑)	t_{HKPHCS}	-	16.8	ns

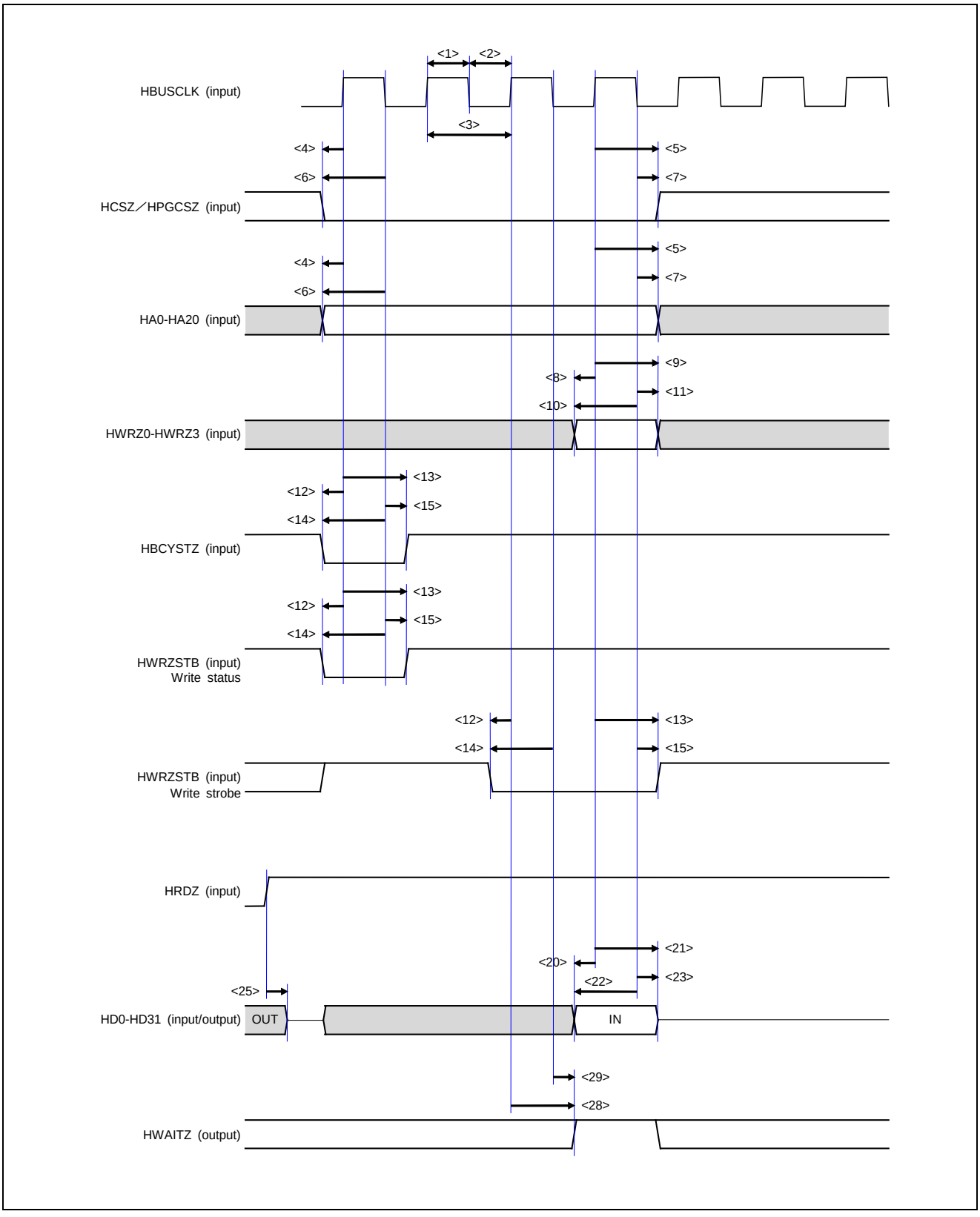


Figure 8.17 External MCU Interface Write Timing (MEMCSEL = H, ADMUXMODE = L)

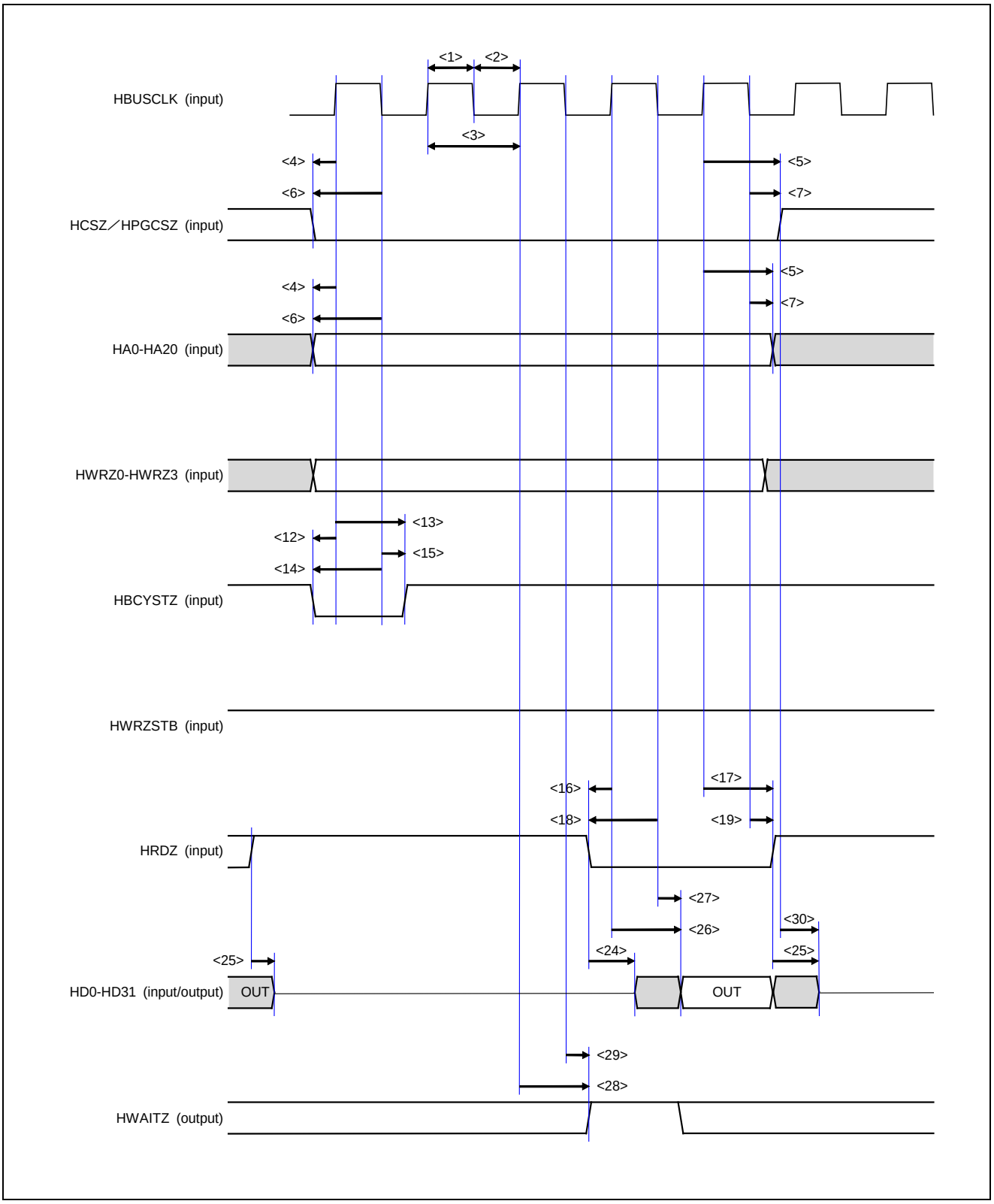


Figure 8.18 External MCU Interface Read Timing (MEMCSEL = H, ADMUXMODE = L)

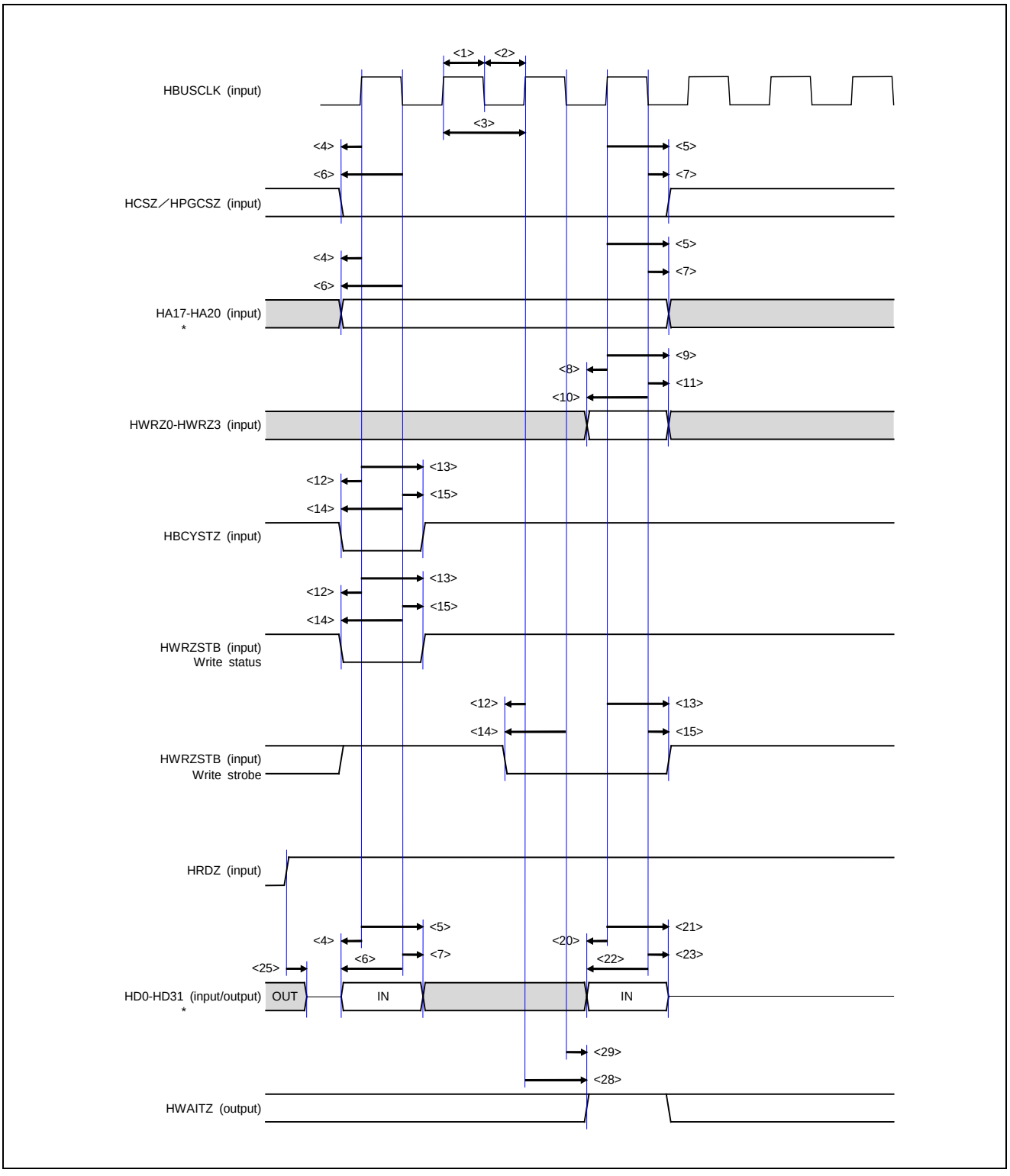


Figure 8.19 External MCU Interface Write Timing (MEMCSEL = H, ADMUXMODE = H)

Remark: *: The source address depends on data bus width as below.
16-bit data bus: Address = {HA[20:17], HWDATA[15:0], 1'b0}
32-bit data bus: Address = {HWDATA[18:0], 2'b00}

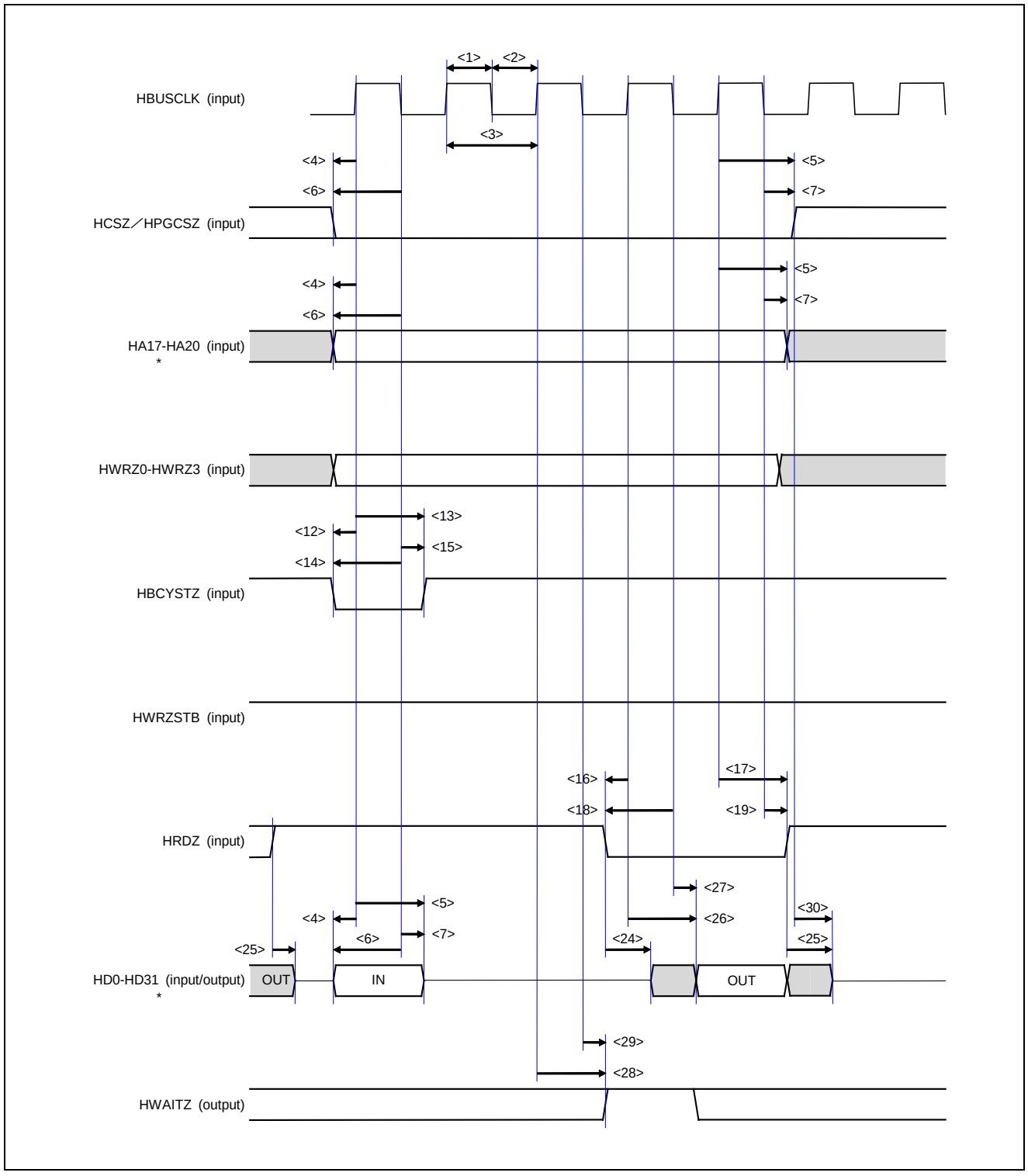


Figure 8.20 External MCU Interface Read Timing (MEMCSEL = H, ADMUXMODE = H)

Remark: *: The source address depends on data bus width as below.
16-bit data bus: Address = {HA[20:17], HWDATA[15:0], 1'b0}
32-bit data bus: Address = {HWDATA[18:0], 2'b00}

8.8.5 Serial Flash ROM Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
SMSCK output cycle	t_{SFRCYC}	C_L = 15 pF	20	-	ns
SMSCK high-level width	t_{SMCKH}		0.5 t_{SFRCYC} - 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK low-level width	t_{SMCKL}		0.5 t_{SFRCYC} - 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK rising time	t_{SMCKR}		-	1.9	ns
SMSCK falling time	t_{SFRCYC}		-	1.9	ns
Delay time between SMCSZ falling and SMSCK rising	$t_{DSMCSCK}$	C_L = 15 pF Freq = 50 MHz	6.0 Note	-	ns
Hold time from SMSCK rising to SMCSZ rising	$t_{DSMCKCS}$	C_L = 15 pF Freq = 50 MHz	9.0 Note	-	ns
SMCSZ high-level width	t_{SMCSH}	C_L = 15 pF	14 Note	-	ns
SMIO0-3 input setup time (for SMSCK ↓)	t_{SSMIO}	-	6.0	-	ns
SMIO0-3 input hold time (for SMSCK ↓)	t_{HSMIO}	-	0	-	ns
SMIO0-3 output delay time (for SMSCK ↓)	t_{DSMIO}	C_L = 15 pF	- 1.0	5.0	ns

Note: The timing can be extended by the setting of the SFMSSC register.
For details, see section 13.2.2, Chip Selection Control Register (SFMSSC), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

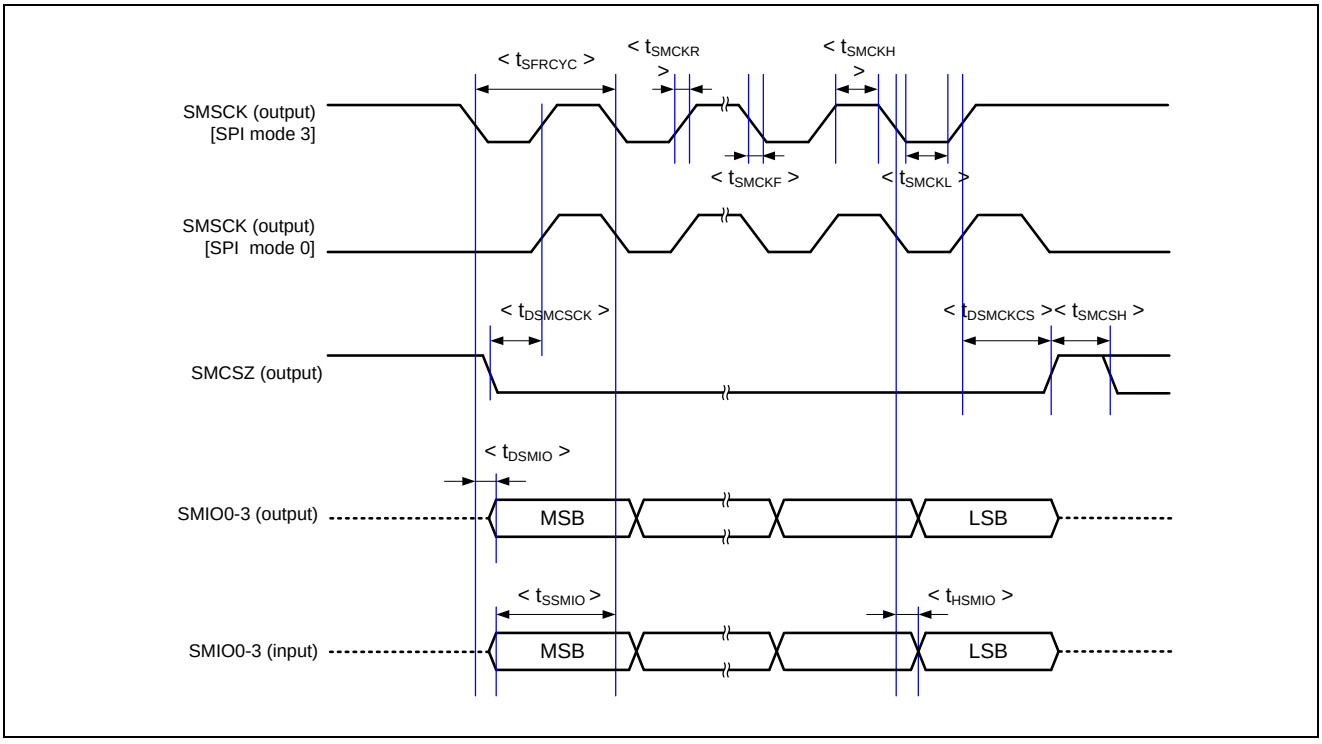


Figure 8.21 Serial Flash Memory Access Timing

8.8.6 External DMA Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
DMAREQZn and RTDMAREQZ input setup time (for BUSCLK ↑)	t_{SKDR}	-	7.0	-	ns
DMAREQZn and RTDMAREQZ input hold time 1	t_{HKDR1}	-	Until DMAACKZn ↓, RTDMAACKZ ↓	-	ns
DMAREQZn and REDMAREQZ input hold time 2 (for BUSCLK ↑)	t_{HKDR2}	-	-	t_{BUSCLK} Note 1 × m Note 2 - 7.0	ns
DMAACKZn and RTDMAACKZ output delay time (for BUSCLK ↑)	t_{DKDA}	C_L = 30 pF	2.0	10.0	ns
DMAACKZn and RTDMAACKZ output low-level width	t_{WDAL}	-	t_{BUSCLK} Note 1 × m Note 2 - 8	t_{BUSCLK} Note 1 × m Note 2 + 8	ns
DMATCZn and RTDMATCZ output delay time (for BUSCLK ↑)	t_{DKTC}	C_L = 30 pF	2.0	10.0	ns

Notes 1. t_{BUSCLK} is one cycle (10 ns) of BUSCLK.
2. n = 0, 1; m = 1 to 31 (DMAIFC0, DMAIFC1, and RTMDAIFC registers).

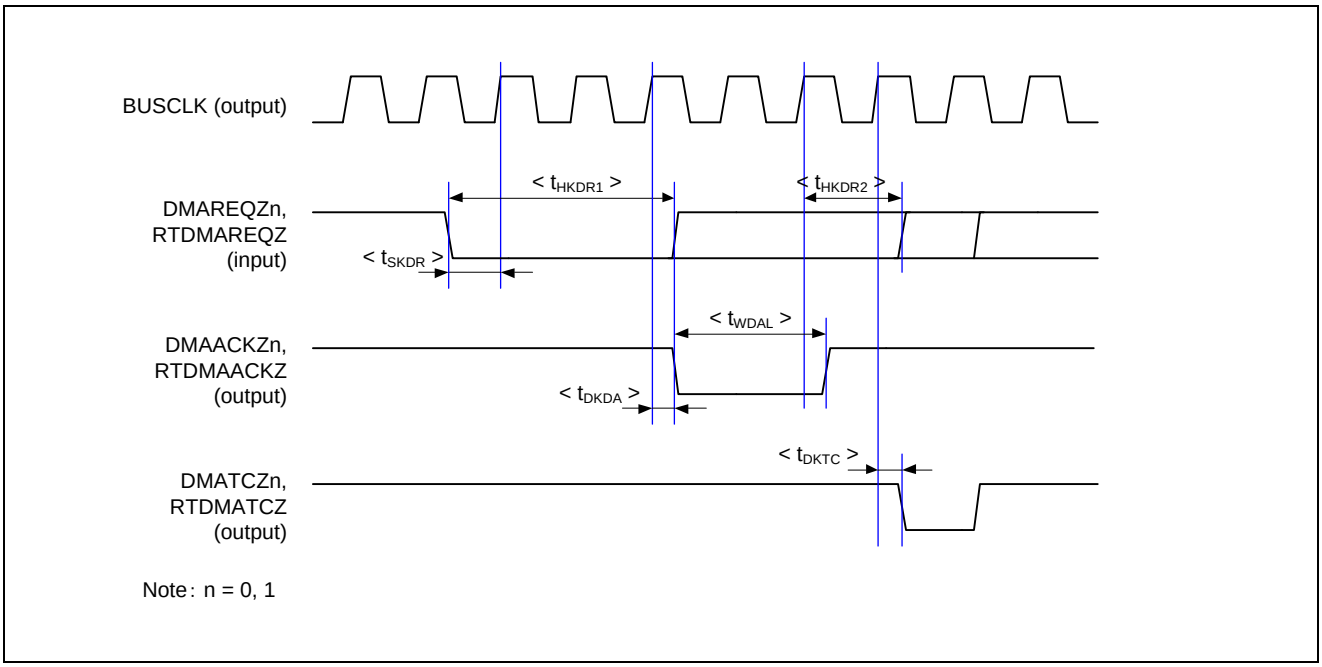


Figure 8.22 External DMA Access Timing

8.8.7 CSI Interface

The clocked serial interface (CSI) supports master mode and slave mode.

(1) Master mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn output cycle	$t_{CSIMSCK}$	CL = 15 pF	40	-	ns
CSISCKn output high-level width	t_{WSKH}	CL = 15 pF	$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISCKn output low-level width	t_{WSKL}	CL = 15 pF	$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISIn input setup time (for CSISCKn ↑)	t_{SMSI}	-	8.5	-	ns
CSISIn input setup time (for CSISCKn ↓)	t_{SMSI}	-	8.5	-	ns
CSISIn input hold time (for CSISCKn ↑)	t_{HMSI}	-	7.0	-	ns
CSISIn input hold time (for CSISCKn ↓)	t_{HMSI}	-	7.0	-	ns
CSISOn output delay time (for CSISCKn ↑)	t_{DMSO}	CL = 15 pF	-	7.0	ns
CSISOn output delay time (for CSISCKn ↓)	t_{DMSO}		-	7.0	ns
CSISOn output hold time (for CSISCKn ↑)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (for CSISCKn ↓)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns

Remark: n = 0, 1

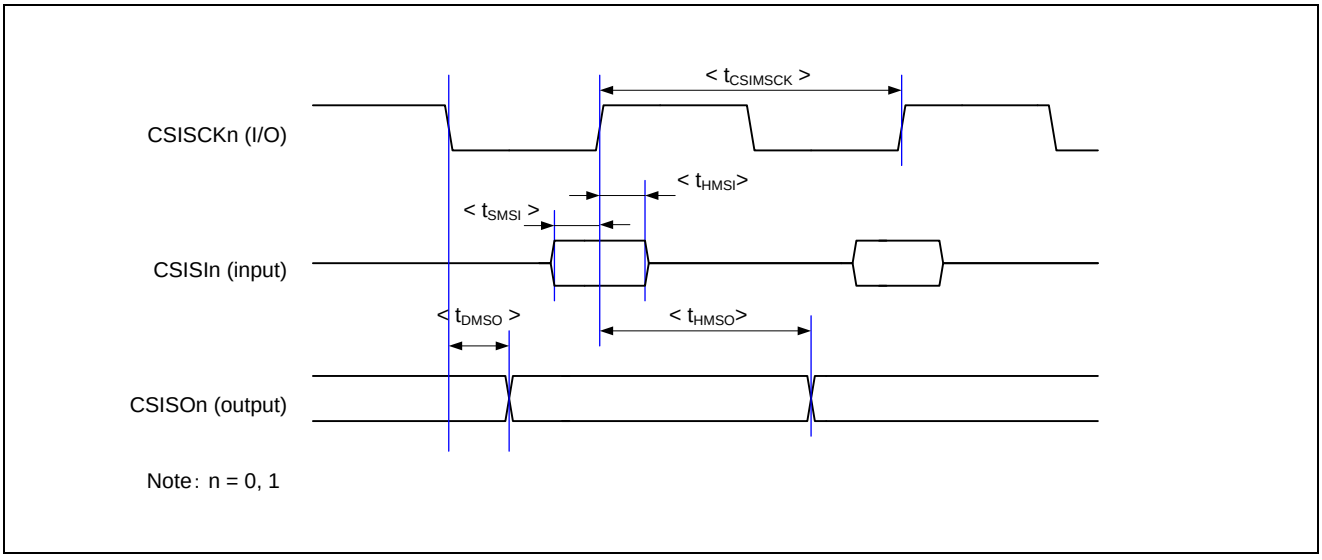


Figure 8.23 CSI Access Timing (Master Mode)

Remark: The above figure shows an example of the timing for data output in case of "for CSISCKn ↓" and data input in case of "for CSISCKn ↑".
Read the timing for reference according to the operating mode.

(2) Slave mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn input cycle	$t_{CSISSCK}$	-	60	-	ns
CSISCKn input high-level width	t_{WSKH}	-	$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISCKn input low-level width	t_{WSKL}	-	$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISIn input setup time (for CSISCKn ↑)	t_{SSSI}	-	10.0	-	ns
CSISIn input setup time (for CSISCKn ↓)	t_{SSSI}	-	10.0	-	ns
CSISIn input hold time (for CSISCKn ↑)	t_{HSSI}	-	15	-	ns
CSISIn input hold time (for CSISCKn ↓)	t_{HSSI}	-	15	-	ns
CSISOn output delay time (for CSISCKn ↑)	t_{DSSO}	C_L = 15 pF	-	10.0	ns
CSISOn output delay time (for CSISCKn ↓)	t_{DSSO}		-	10.0	ns
CSISOn output hold time (for CSISCKn ↑)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (for CSISCKn ↓)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns

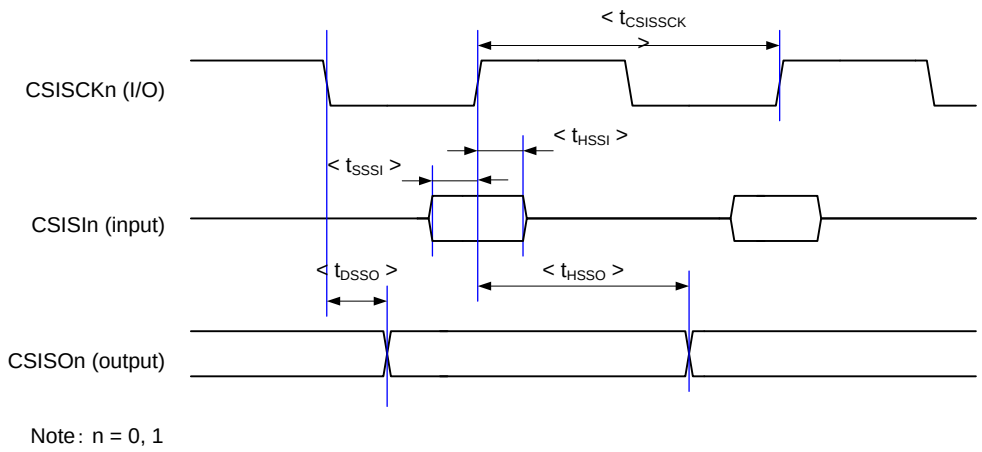


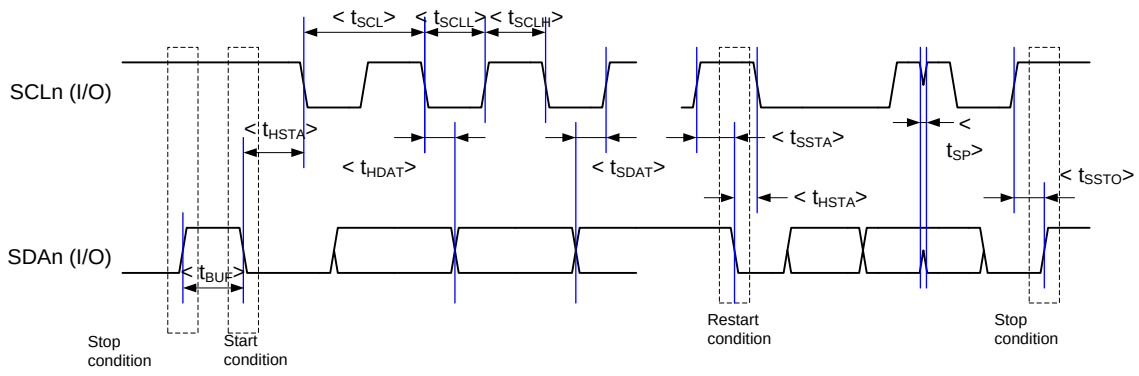
Figure 8.24 CSI Access Timing (Slave Mode)

Remark: The above figure shows an example of the timing for data output in case of "for CSISCKn ↓" and data input in case of "for CSISCKn ↑".
Read the timing for reference according to the operating mode.

8.8.8 I2C Interface

Parameter		Symbol	Conditions	Normal Mode		High-Speed Mode		Unit
				MIN	MAX	MIN	MAX	
SCLn input/output frequency		t_{SCL}	C_L = 30 pF	0	100	0	400	kHz
Bus-free time between the stop condition and start condition		t_{BUF}		4.7	-	1.3	-	µs
Hold time		t_{HSTA}		4.0	-	0.6	-	µs
SCLn clock low-level width		t_{SCLL}		4.7	-	1.3	-	µs
SCLn clock high-level width		t_{SCLH}		4.0	-	0.6	-	µs
Setup time for the start and restart conditions		t_{SSTA}		4.7	-	0.6	-	µs
Data hold time	For a CBUS compatible master	t_{HDAT}		5.0	-	-	-	µs
	For an I2C bus			0	-	0	0.9	µs
Data setup time		t_{SDAT}		250	-	100	-	ns
SDAn and SCLn rising time		t_{SCLR}		-	1000	20 +0.1C_b	300	ns
SDAn and SCLn falling time		t_{SCLF}		-	300	20 +0.1C_b	300	ns
Stop condition setup time		t_{SSTO}		4.0	-	0.6	-	µs
Pulse width of spike suppressed by input filter		t_{SP}		-	-	0	50	ns
Capacitance load of each bus line		C_b	-	-	400	-	400	pF

Remark: n = 0, 1



Note : n = 0, 1
The figure does not cover t_{SCLR}, and t_{SCLF}.

Figure 8.25 I2C Access Timing

8.8.9 CAN Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
Internal delay time	t_{NODE}	C_L = 30 pF	-	75	ns

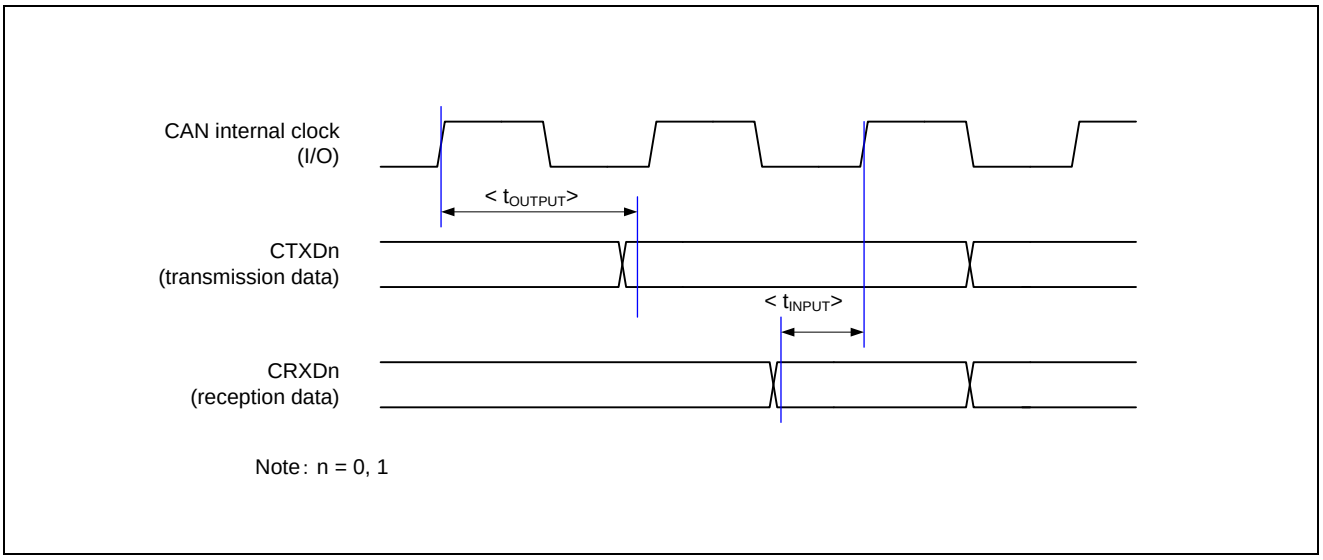


Figure 8.26 CAN Access Timing

Remark: CAN internal clock (f_{CAN}): CAN baud-rate clock

Internal delay time (t_{NODE}) = Internal transmission delay time (t_{OUTPUT}) + Internal transmission delay time (t_{INPUT})

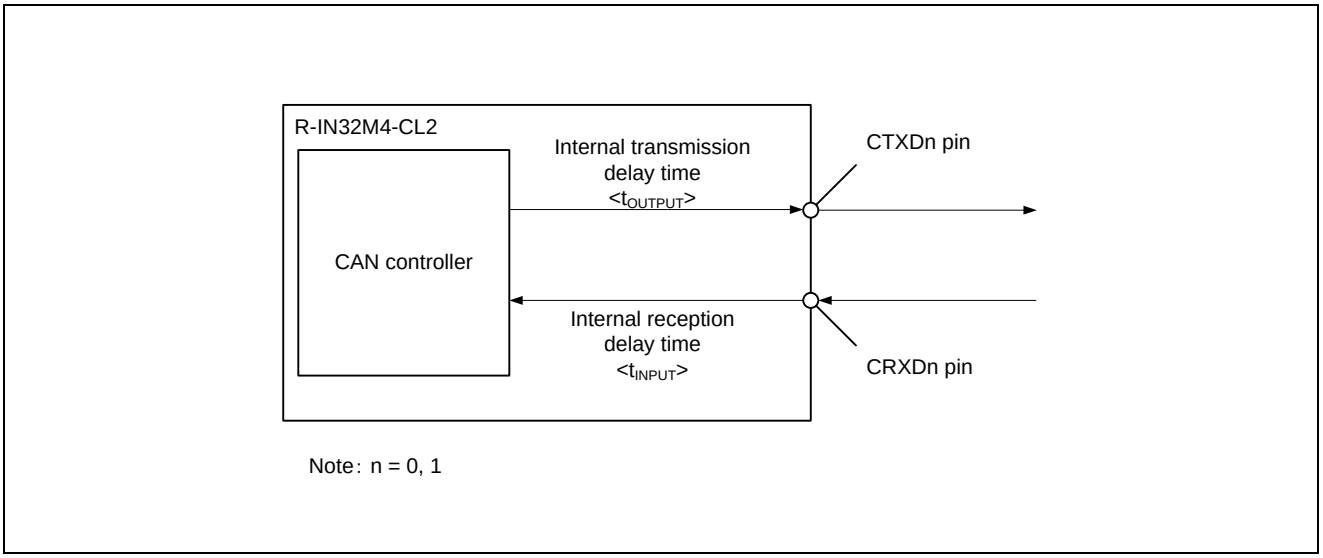


Figure 8.27 CAN Access Timing (Supplement)

8.8.10 Debugging Interface

(1) Debugging serial interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TCK input cycle	t_{TCK}	-	20	-	ns
TMS input setup time (for TCK ↑)	t_{STMS}	-	6.5	-	ns
TMS input hold time (for TCK ↑)	t_{HTMS}	-	0	-	ns
TDI input setup time (for TCK ↑)	t_{STDI}	-	6.5	-	ns
TDI input hold time (for TCK ↑)	t_{HTDI}	-	0	-	ns
TDO output delay time (for TCK ↓)	t_{DTDO}	C_L = 30 pF	3.0	13.0	ns

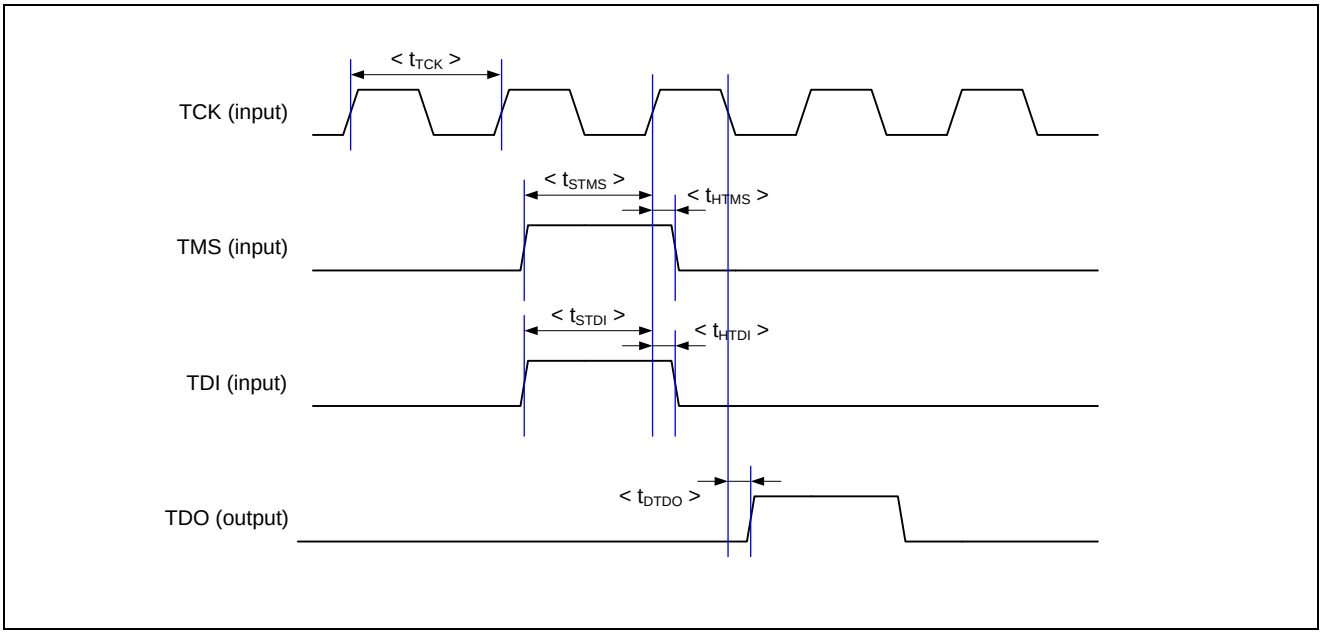


Figure 8.28 Debugging Serial Interface

(2) Trace interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TRACECLK output cycle	t_{TRCCLK}	C_L = 15 pF	20	-	ns
TRACEDATAn output delay time (for TRACECLK)	$t_{DTRCDAT}$	C_L = 15 pF	0.26	8.43	ns

Remark: n = 0 to 3

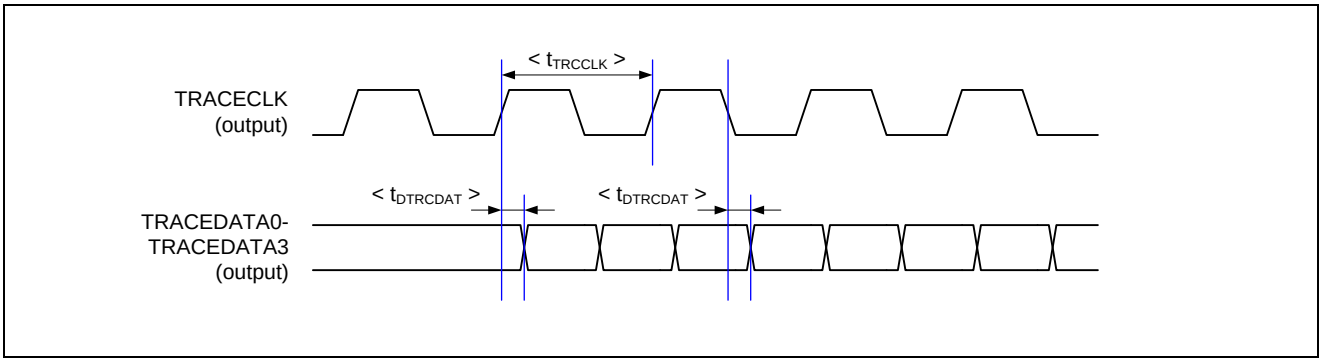


Figure 8.29 Trace Interface

REVISION HISTORY	R-IN32M4-CL2 User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Dec 09, 2015	-	First edition issued
1.01	Jan 29, 2016	16-17	***2.1.3.1 SRAM Interface Pins*** Level during Reset of BUSCLK signal, modified
		18-19	***2.1.3.2 External MCU Interface Pins*** Notes for HBUSCLK, HA1-HA20, HD0-HD31, modified
		25	***2.1.10 CC-Link IE Field Pins (Intelligent Device Station)*** Notes2, added
		27	***2.1.12 CC-Link Pins (Remote Device Station)*** Description of CCM_CLK80M signal, added
		47	***2.5.2 Ethernet Pins*** interface for PHY0_LED0, PHY1_LED0 signal, modified
		48	***2.5.7 System Pins*** Recommended Connection when Not in Use for XT1 and XT2 signal, modified
		55	***4.1 List of Exceptions*** Abbreviations of reset pins, modified SYSRESET register, added
		119	***Table 8.4 Absolute Maximum Ratings*** Absolute Maximum Ratings for I/O voltage, modified
		125	***8.8.1 (1) Input Clocks*** MAX/MIN value for CCI_CLK2_097M, modified
1.02	Feb 28, 2017	13	***2.1.2 Ethernet Pins*** Nonexistent pins (for thermal sensor and regulator) deleted
		25	***2.1.11 CC-Link Pins*** Feature of the CCM_MDIN0-3 signals modified
		27	***2.1.13 System Pins*** Function of PONRZ modified
		46	***2.5.2 Ethernet Pins*** Nonexistent pins (for thermal sensor) deleted
		57	***4.2 List of Interrupts***, Table 4.1 (2/4) Exception No.54 INTETHSW: Interrupt source name changed
		59	***4.2 List of Interrupts***, Table 4.1 (4/4) ECC error interrupts added
		60	***5. Peripheral Modules*** Notation of peripheral modules unified to that of User's Manual
		62	***6.1.1 CC-Link IE Field (Intelligent Device Station) Bus Size Control Register (CIEBSC)*** Register symbol in the bit map corrected
		63	***6.1.3 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD)*** Reference for the related registers added

Rev.	Date	Description	
		Page	Summary
1.02	Feb 28, 2017	88	***7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE, EXTPFCE)*** Erroneously omitted register EXTPFC was added to notes 1 and 2.
		119	***8.4 DC Characteristics*** Table 8.7 Symbol for the high-level output voltage modified
2.00	Dec. 28, 2018	3	1.2 Functional Overview Table 1.1 Overview of R-IN32M4-CL2 (2/2) Description of "remote device station" added to "CC-Link IE"
		6	1.5 Base Addresses of the System Registers Area The description on the base addresses of the system registers area was added.
		21	2.1.5 DMA Interface Pins The description on the section and caution was modified.
		25	2.1.10 CC-Link IE Field Pins Description of "(intelligent device station)" was deleted from the title
		26	2.1.11 CC-Link Pins (Intelligent Device Station) Functional description of P21, P62-P65, P43, P66, and RP01 modified (P21, P66, RP01 changed to "Not used")
		28	2.1.14 Trace Pins Description of "(intelligent device station)" was deleted from the reference
		48	2.5.5 CC-Link IE Field Pin Description of "(intelligent device station)" was deleted from the title
		51	3. Memory Maps Figure 3.1 Entire Memory Maps Locations of Instruction RAM area and instruction RAM mirror area were corrected; a note regarding instruction RAM mirror area was added
		54	Figure 3.5 External MCU Interface Space Note 2 added, note 1 was added to "AHB peripheral registers"
		62	6. CC-Link IE Field Description of "(intelligent device station)" was deleted from the title
		62	6.1 CC-Link IE Field Control Registers Description of "(intelligent device station)" was deleted from the title
		62	Table 6.2 Overview of the Bus Control Registers Description of "(intelligent device station)" was deleted from the register names
		63	6.1.1 CC-Link IE Field Bus Size Control Register (CIEBSC) Description of "(intelligent device station)" was deleted from the title and description
		63	6.1.2 CC-Link IE Field Bus Bridge Control Register (CIESMC) Description of "(intelligent device station)" was deleted from the title and description
		64	6.1.3 CC-Link IE Field Clock Gate Register (CIECLKGTD) Description of "(intelligent device station)" was deleted from the title

Rev.	Date	Description	
		Page	Summary
2.00	Dec. 28, 2018	68	7.2 Port Configuration "Application and Operation" for the port function control registers and the port function control expansion registers was modified.
		68	7.2 Port Configuration Caution on the port configuration was modified.
		81 to 92	7.3.3 Port Mode Control Registers (PMC, RPMC, EXTPMC) 7.3.4 Port Function Control Registers (PFC, RPFC, EXTPFC) 7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE, EXTPFCE) Notes on the multiplexed functions were modified.
		133	8.8.4 External MCU Interface Pins (1) Synchronous mode Maximum value for "t_{DKHWTV}" was modified ("10.0" to "11.0")
		144	8.8.4 External MCU Interface Pins (4) Synchronous SRAM type transfer mode Maximum values for "t_{DKPHWT}" and "t_{DKNHWT}" were modified ("10.0" to "11.0")
		145 to 148	Figure 8.17 External MCU Interface Write Timing (MEMCSEL = H, ADMUXMODE = L) Figure 8.18 External MCU Interface Read Timing (MEMCSEL = H, ADMUXMODE = L) Figure 8.19 External MCU Interface Write Timing (MEMCSEL = H, ADMUXMODE = H) Figure 8.20 External MCU Interface Read Timing (MEMCSEL = H, ADMUXMODE = H) Figure 8.17 and Figure 8.18 were newly added as ADMUXMODE = L; Figure 8.19 and Figure 8.20 (Figure 8.17 and Figure 8.18 of former revision) were modified as ADMUXMODE = H; Remark regarding source addresses was added to Figure 8.19 and Figure 8.20
		149	8.8.5 Serial Flash ROM Interface Specifications of $t_{DSMCSCK}$ and $t_{DSMCKCS}$ were modified.
		—	Error corrected, description modified, and contents and expressions adjusted
3.00	May 31, 2024	65	6.2 Usage Note was added

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