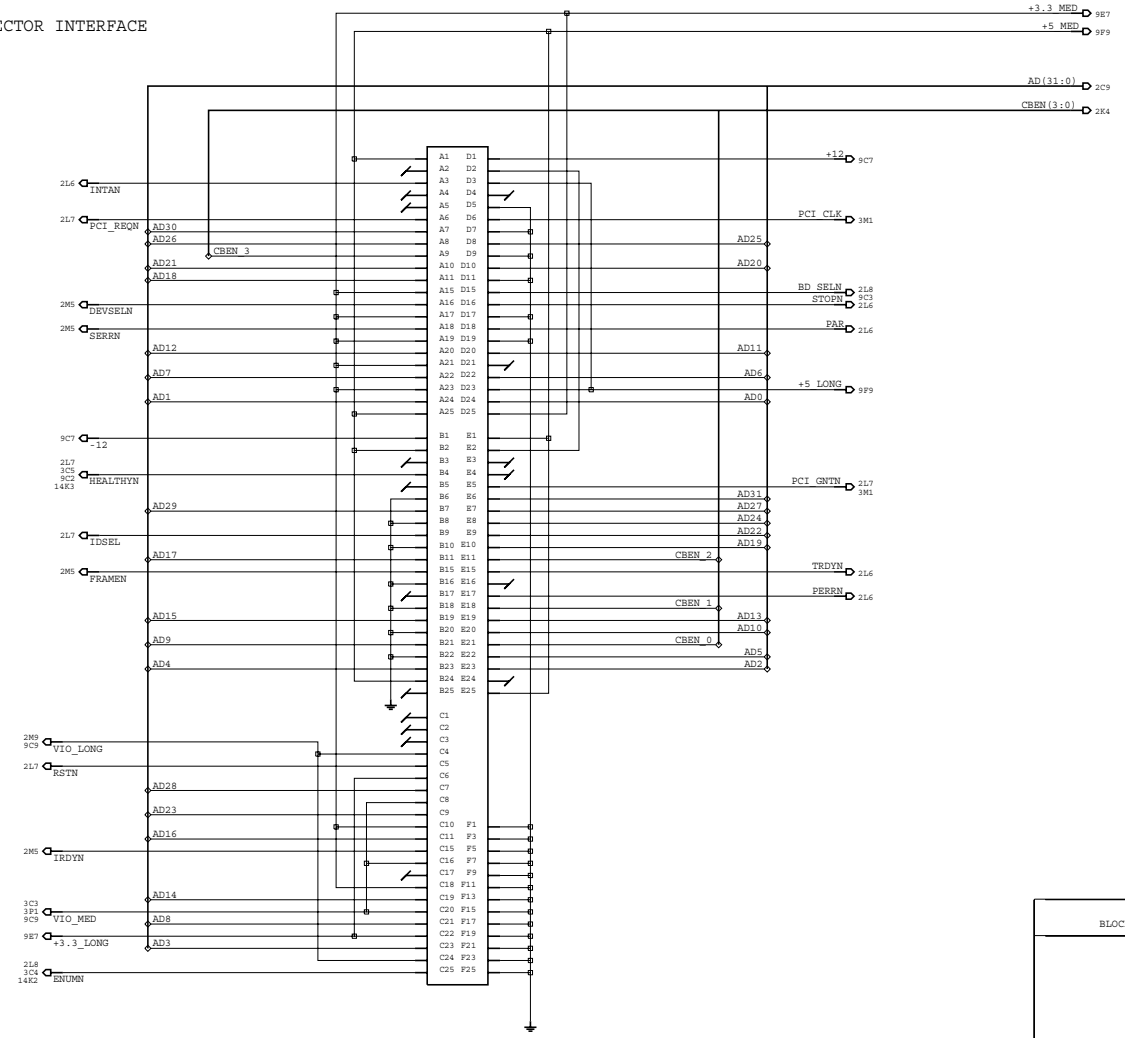
COMPACTPCI CONNECTOR INTERFACE



TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 1 OF 15

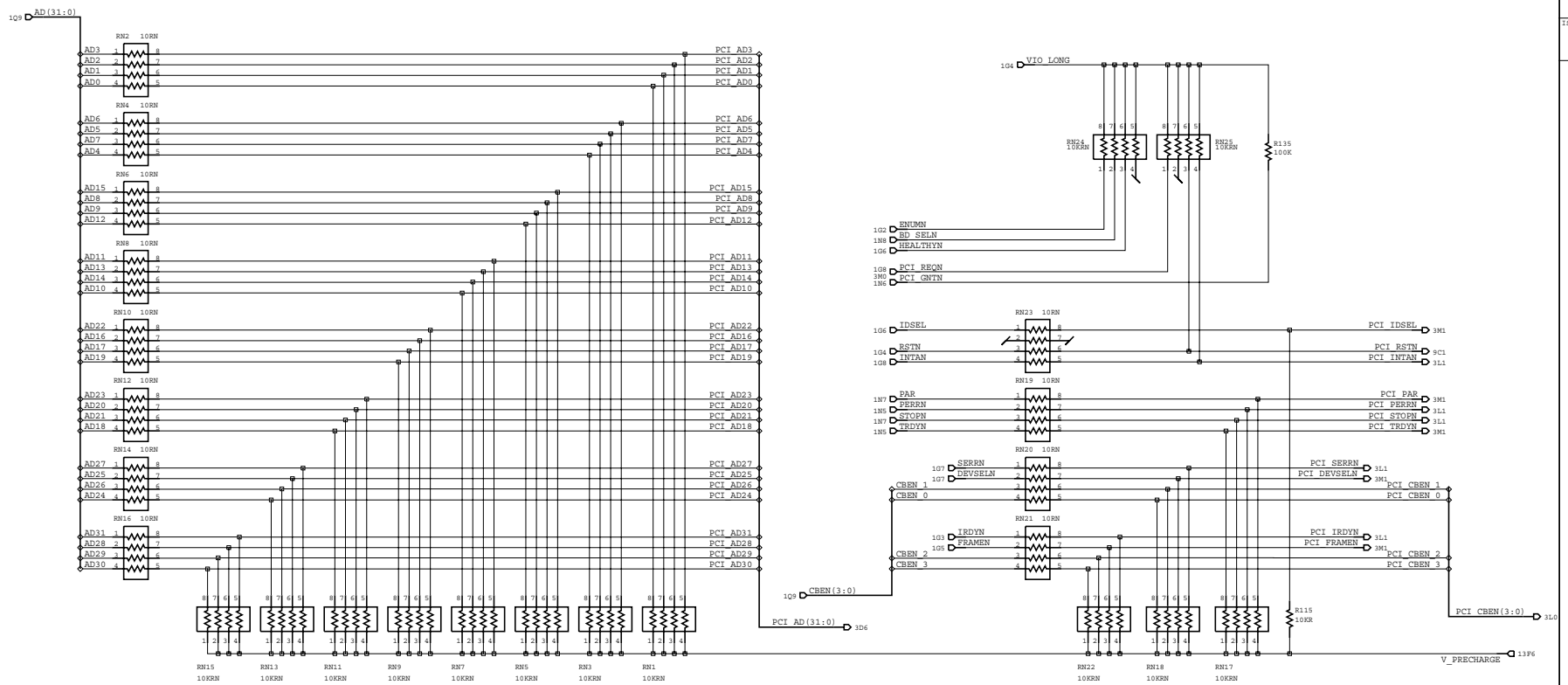
TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER		
DATE 16/4/1999		STREAM
EC		
ISSUE 2	APPROVED DSGN JB MNGR TM	
DESIGN		
DRAWING NUMBER		
SIZE D	SHEETS 15	SHEET 1 STREAM

PRINTED IN



TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 2 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER		
DATE 16/4/1999	STREAM	
EC		
ISSUE 2	APPROVED DSGN JB / MNGR TM	
SIZE D	SHEETS 15	SHEET 2
DESIGN		
DRAWING NUMBER		

PRINTED IN

QSPAN II

U17

CA91L862A

QSPAN DECOUPLING CAPS

NOTE: For Internal Use Only
These resistors are not installed
when using the CA91L862A device.

R2 and C21
by default
are not
installed

R128 installed by default,
R99 abd R88 are left unpopulated.

TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 3 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER

DATE 16/4/1999 STREAM

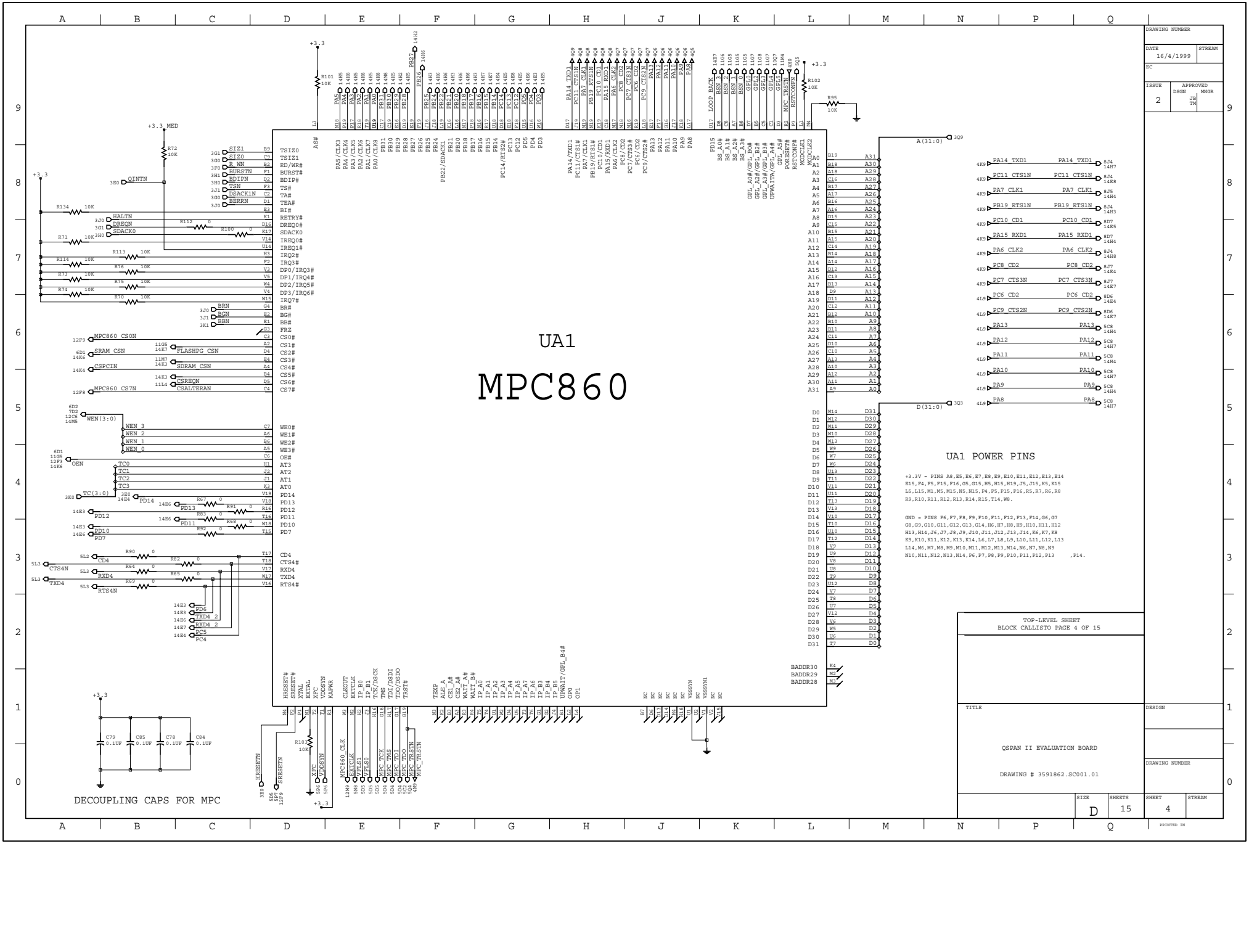
EC

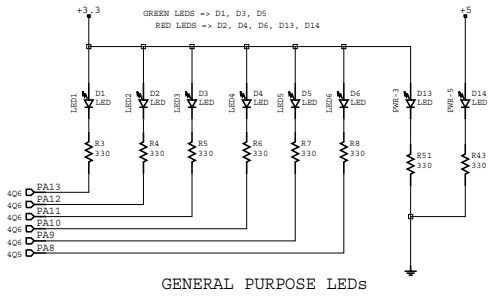
ISSUE 2 APPROVED DSGN JB MNGR TM

DESIGN

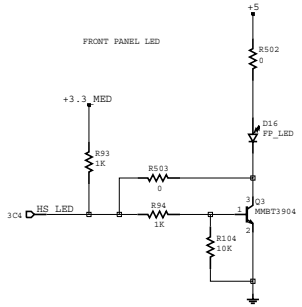
SIZE D SHEETS 15 SHEET 3 STREAM

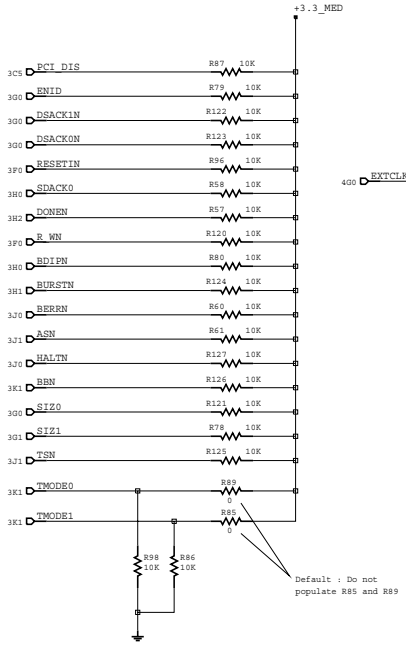
PRINTED IN

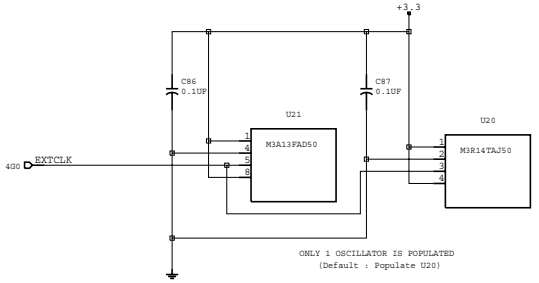

UA1
MPC860
UA1 POWER PINS
+3.3 - PINS A8,E5,E6,E7,E8,E9,E10,E11,E12,E13,E14
E15,F4,F5,F15,F16,G5,G15,H5,H15,H19,J5,J15,K5,K15
L5,L15,M1,M5,M15,N5,N15,P4,P5,P15,P16,R5,R7,R6,R8
R9,R10,R11,R12,R13,R14,R15,T14,W8.
GND - PINS F6,F7,F8,F9,F10,F11,F12,F13,F14,G6,G7
G8,G9,G10,G11,G12,G13,G14,H6,H7,H8,H9,H10,H11,H12
H13,H14,J6,J7,J8,J9,J10,J11,J12,J13,J14,K6,K7,K8
K9,K10,K11,K12,K13,K14,L6,L7,L8,L9,L10,L11,L12,L13
L14,M6,M7,M8,M9,M10,M11,M12,M13,M14,N6,N7,N8,N9
N10,N11,N12,N13,N14,P6,P7,P8,P9,P10,P11,P12,P13 ,P14.
DECOUPLING CAPS FOR MPC
TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 4 OF 15
QSPAN II EVALUATION BOARD
DRAWING # 3591862.SC001.01
DRAWING NUMBER
DATE 16/4/1999
STREAM
EC
ISSUE 2
APPROVED DSGN JB MNGR TM
DESIGN
SIZE D
SHEETS 15
SHEET 4
STREAM
PRINTED IN

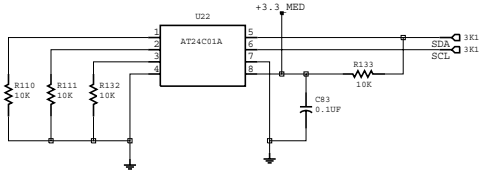


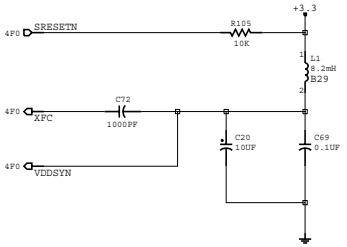
GENERAL PURPOSE LEDs

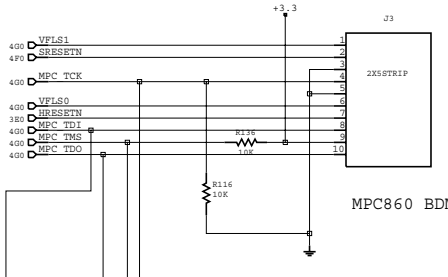




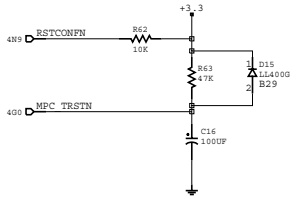




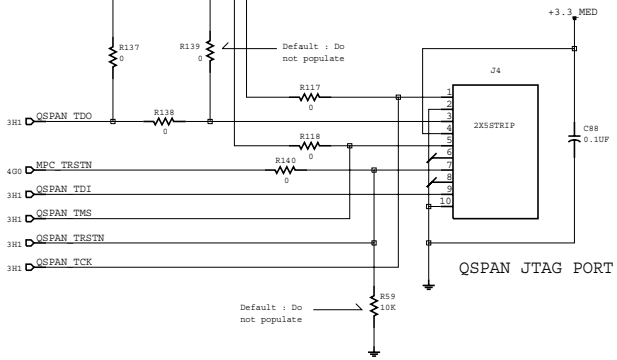




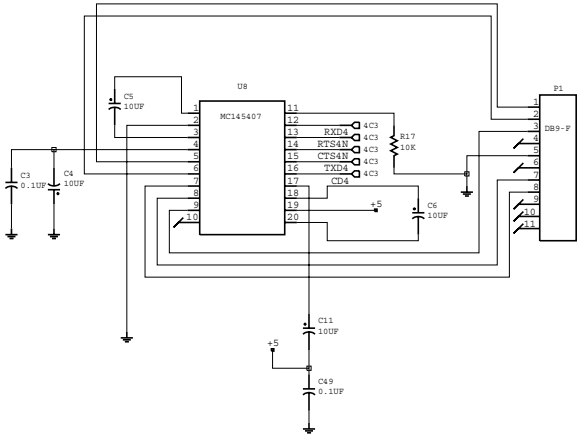
MPC860 BDM PORT



POWER ON RESET
CIRCUIT FOR MPC860



QSPAN JTAG PORT



TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 5 OF 15

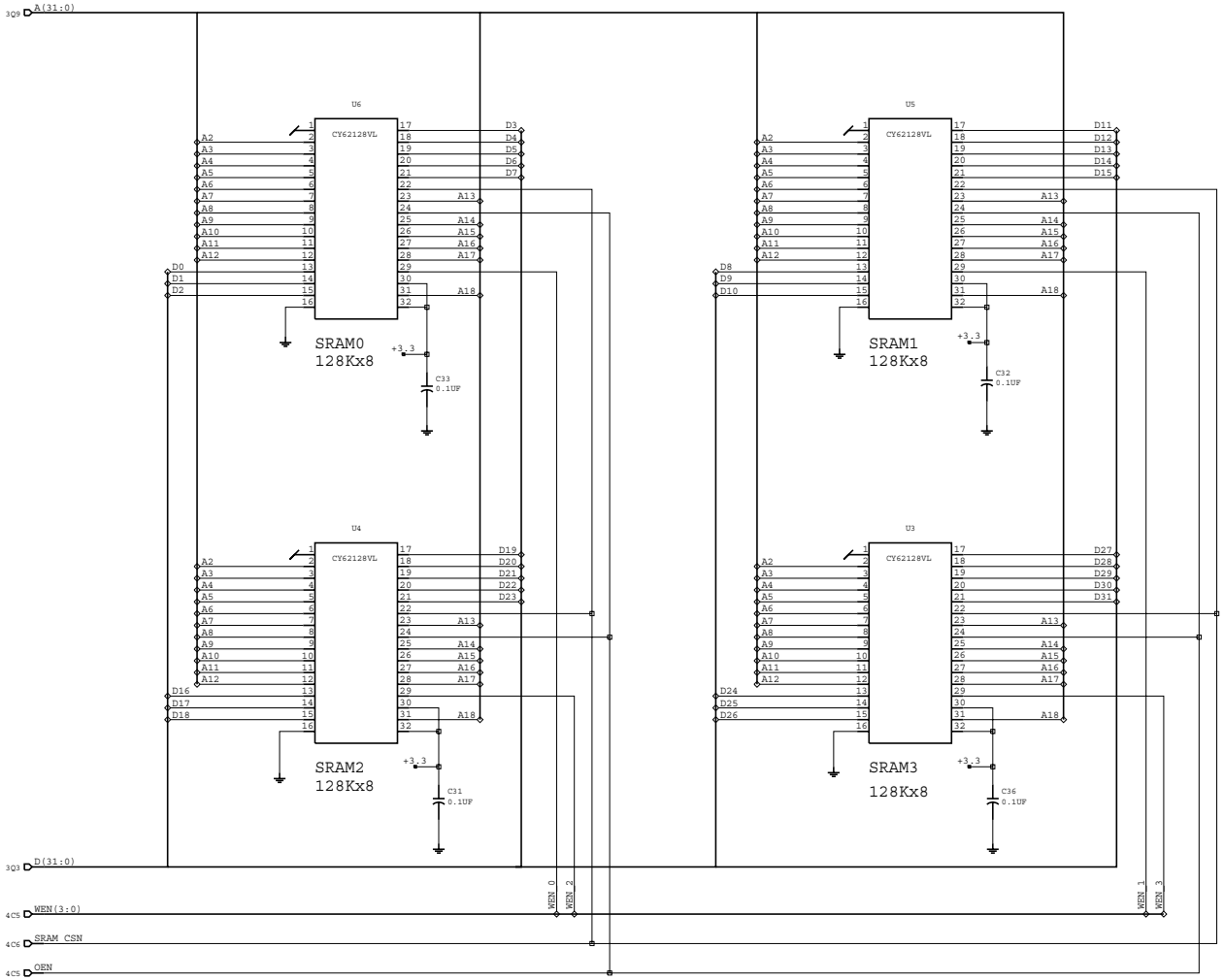
TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER	
DATE	16/4/1999
STREAM	
EC	
ISSUE	2
APPROVED DSGN	JB
APPROVED MNGR	TM
DESIGN	
DRAWING NUMBER	
SIZE	D
SHEETS	15
SHEET	5
STREAM	

PRINTED IN



TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 6 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER

DATE 16/4/1999

STREAM

EC

ISSUE 2

APPROVED DSGN JB MNGR TM

DESIGN

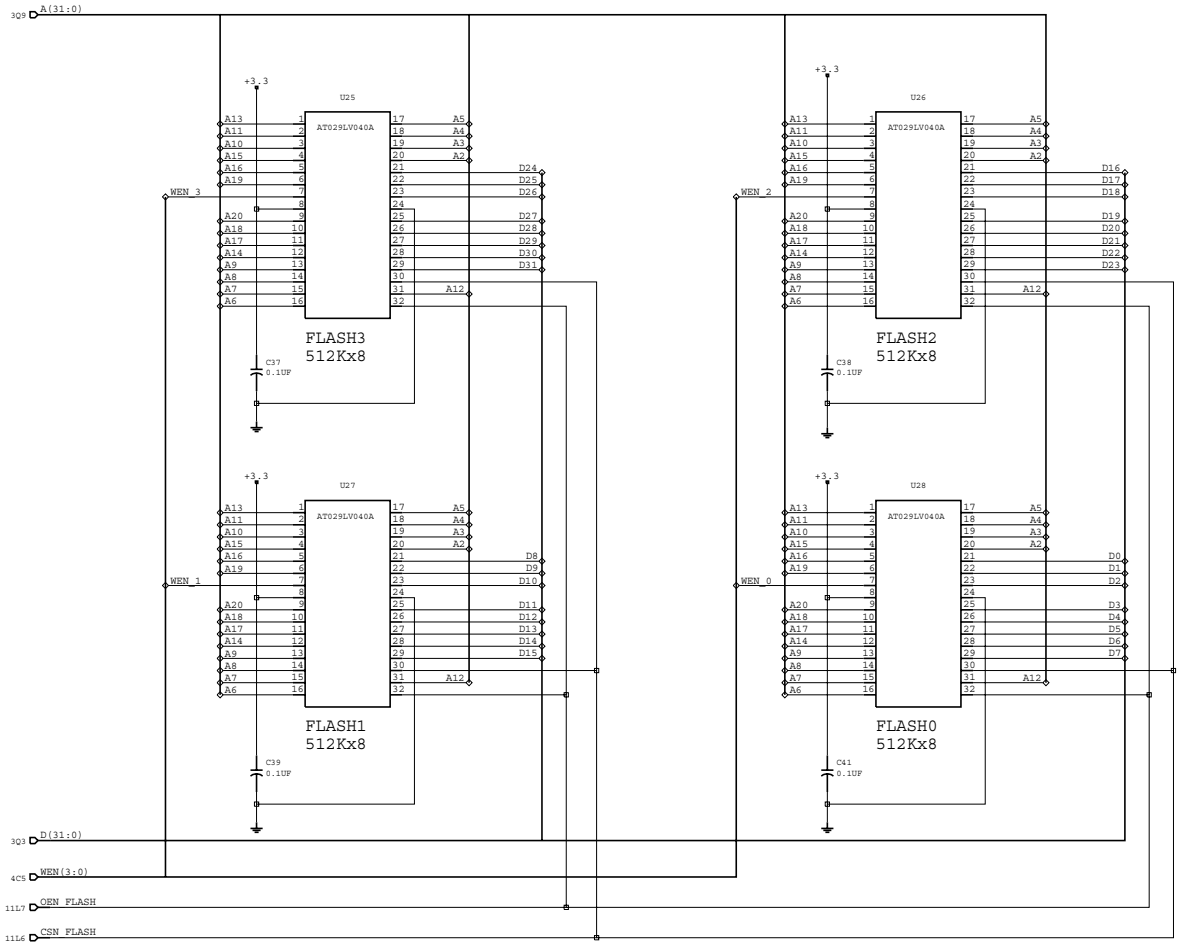
SIZE D

SHEETS 15

SHEET 6

STREAM

PRINTED IN



TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 7 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER

DATE 16/4/1999 STREAM

EC

ISSUE 2 APPROVED DSGN JB MNGR TM

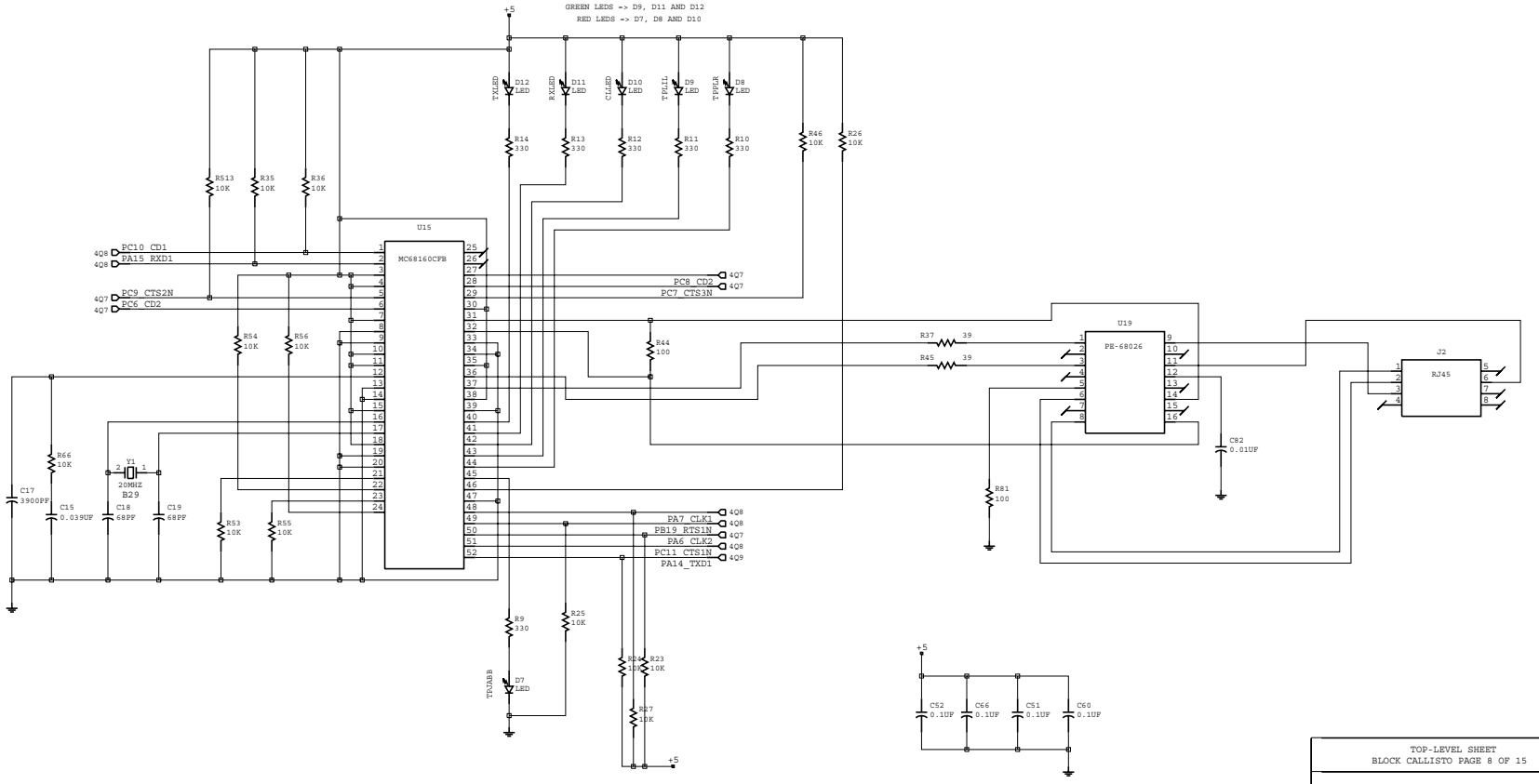
DESIGN

DRAWING NUMBER

SIZE D SHEETS 15 SHEET 7 STREAM

PRINTED IN

ETHERNET



DECOUPLING FOR ETHERNET

TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 8 OF 15

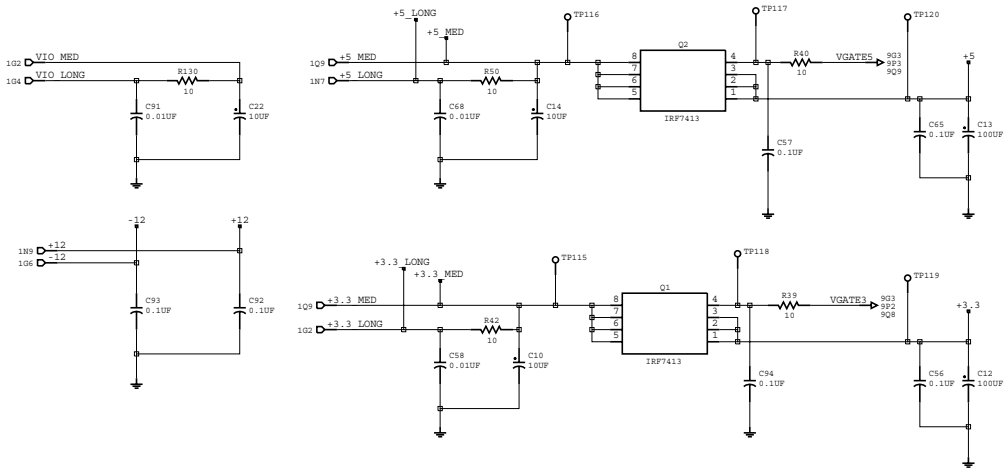
TITLE

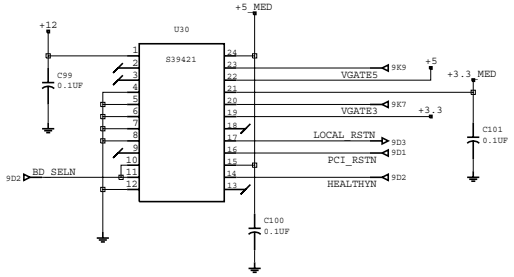
QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER		
DATE 16/4/1999	STREAM	
EC		
ISSUE 2	APPROVED DSGN JB MNGR TM	
DESIGN		
DRAWING NUMBER		
SIZE D	SHEETS 15	SHEET 8 STREAM

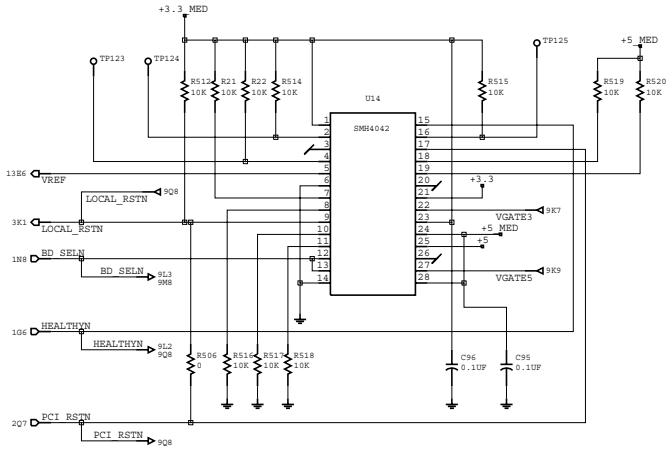
PRINTED IN





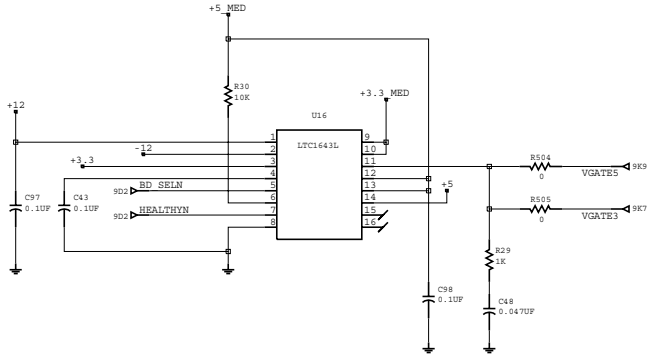
HOT SWAP CONTROLLER OPTION #3

When using S39421, do not populate
U14, U16, R504, R505 and R506.



HOT SWAP CONTROLLER OPTION #1

When using SMH4042, do not populate
U16, U30, R504, R505 and R506.



HOT SWAP CONTROLLER OPTION #2

When using LTC1643L, do not populate
U14 and U30.

TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 9 OF 15

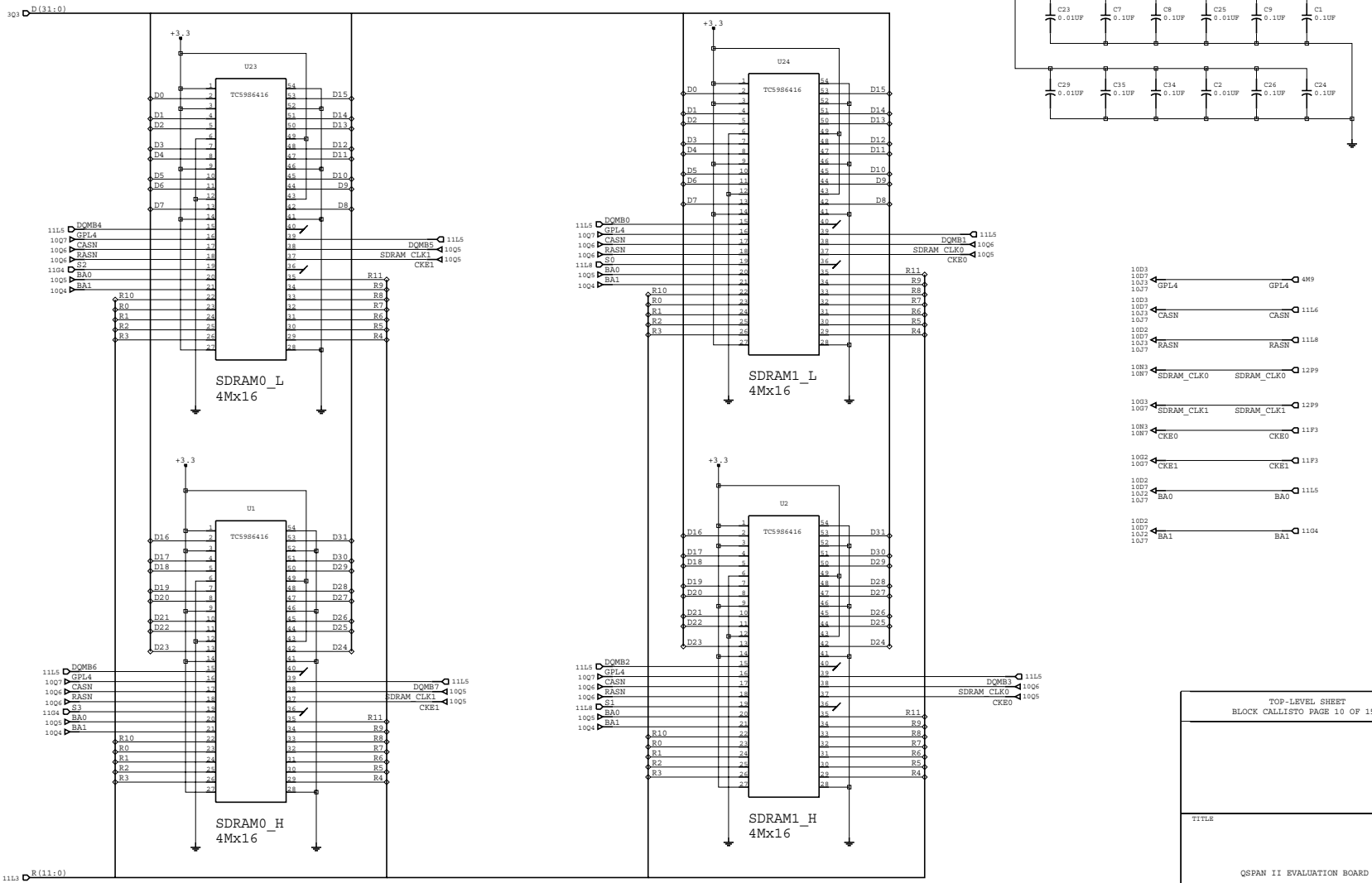
TITLE

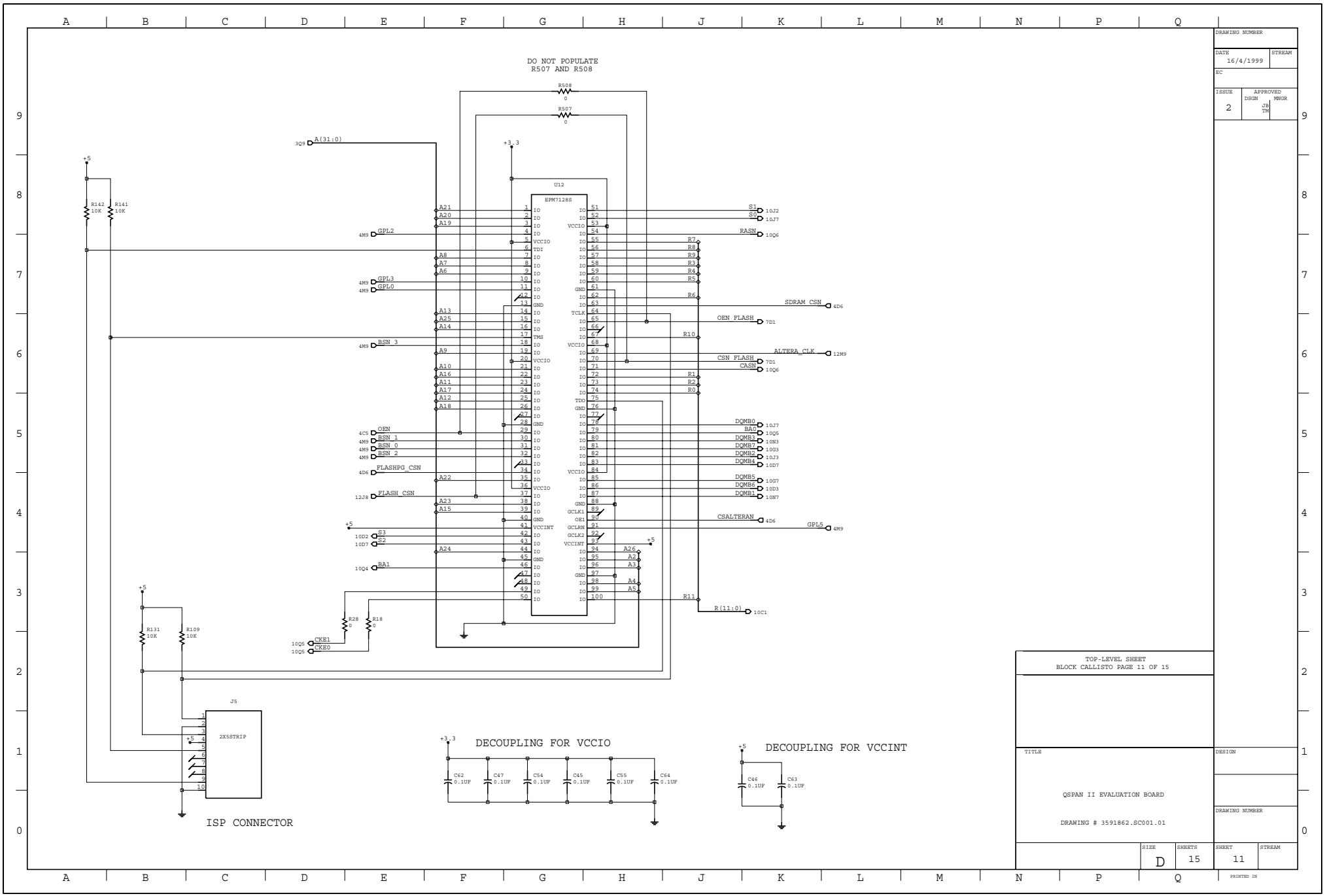
QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER		
DATE 16/4/1999	STREAM	
EC		
ISSUE 2	APPROVED DSGN JB / MNGR TM	
DESIGN		
DRAWING NUMBER		
SIZE D	SHEETS 15	SHEET 9 / STREAM

PRINTED IN


DECOUPLING FOR SDRAM
+3.3
C23 0.01UF
C7 0.1UF
C8 0.1UF
C25 0.01UF
C9 0.1UF
C1 0.1UF
C29 0.01UF
C35 0.1UF
C34 0.1UF
C2 0.01UF
C26 0.1UF
C24 0.1UF
3Q3 D(31:0)
U23
TC59S6416
SDRAM0_L
4Mx16
U24
SDRAM1_L
4Mx16
U1
SDRAM0_H
4Mx16
U2
SDRAM1_H
4Mx16
DQMB4
DQMB5
DQMB0
DQMB1
DQMB6
DQMB7
DQMB2
DQMB3
GPL4
CASN
RASN
S2
S3
S0
S1
BA0
BA1
SDRAM_CLK1
SDRAM_CLK0
CKE1
CKE0
R10
R0
R1
R2
R3
R11
R9
R8
R7
R6
R5
R4
11L3 R(11:0)
TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 10 OF 15
TITLE
QSPAN II EVALUATION BOARD
DRAWING # 3591862.SC001.01
DRAWING NUMBER
DATE 16/4/1999
STREAM
EC
ISSUE 2
APPROVED DSGN JB MNGR TM
DESIGN
SIZE D
SHEETS 15
SHEET 10
STREAM
PRINTED IN



TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 11 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER

DATE 16/4/1999 STREAM

EC

ISSUE 2 APPROVED DSGN JB MNGR TM

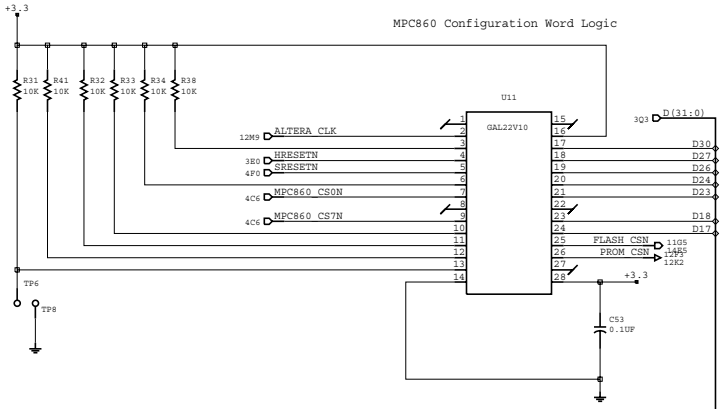
DESIGN

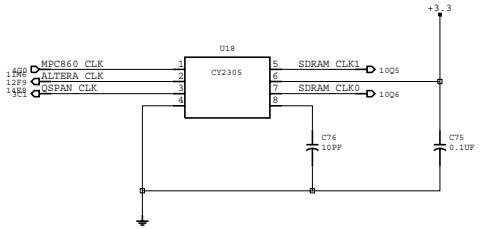
DRAWING NUMBER

SIZE D SHEETS 15 SHEET 11 STREAM

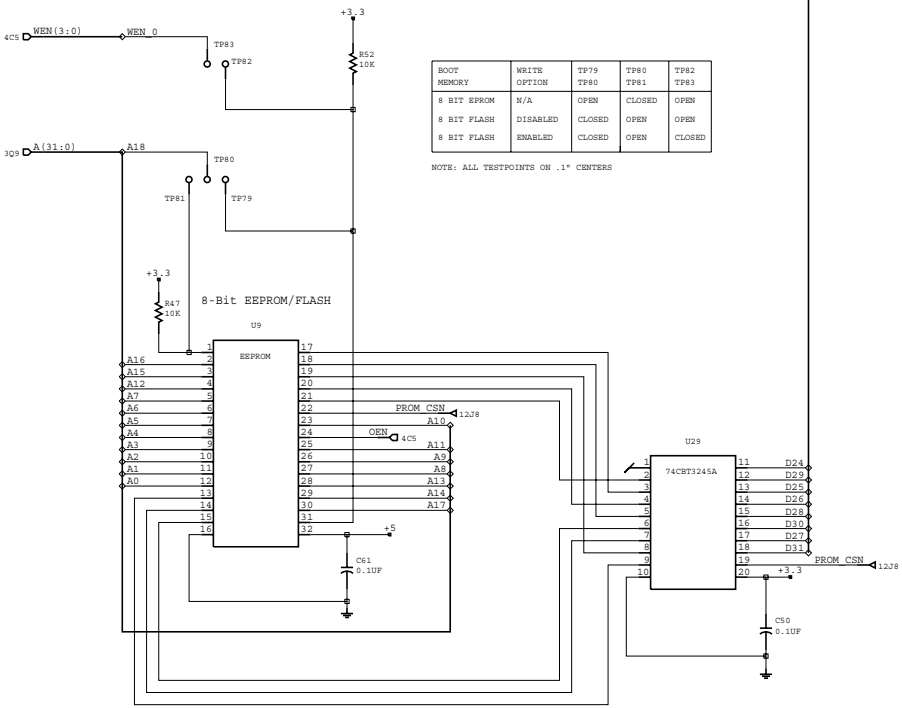
PRINTED IN

MPC860 Configuration Word Logic





MPC860 CLOCK DISTRIBUTION



BOOT MEMORY	WRITE OPTION	TP79 TP80	TP80 TP81	TP82 TP83
8 BIT EPROM	N/A	OPEN	CLOSED	OPEN
8 BIT FLASH	DISABLED	CLOSED	OPEN	OPEN
8 BIT FLASH	ENABLED	CLOSED	OPEN	CLOSED

NOTE: ALL TESTPOINTS ON .1" CENTERS

TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 12 OF 15

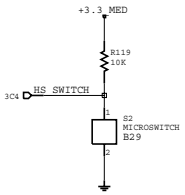
TITLE

QSPAN II EVALUATION BOARD

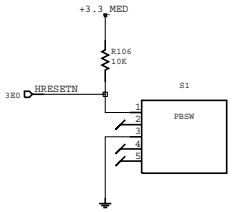
DRAWING # 3591862.SC001.01

DRAWING NUMBER		
DATE 16/4/1999	STREAM	
EC		
ISSUE 2	APPROVED DSGN JB MNGR TM	
DESIGN		
DRAWING NUMBER		
SIZE D	SHEETS 15	SHEET 12 STREAM

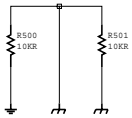
PRINTED IN



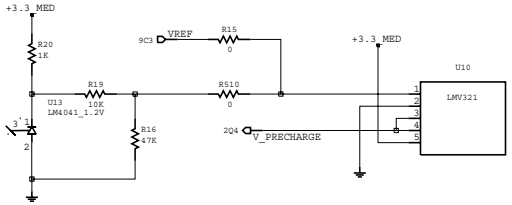
EJECTOR HANDLE SWITCH



PUSHBUTTON RESET



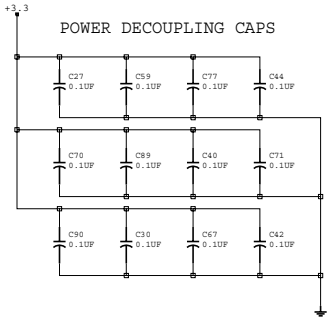
ESD PROTECTION CIRCUIT



PRECHARGE VOLTAGE REFERENCE SUPPLY

For SMH4042 Hot Swap Controller :
Populate R15 and R510 is left open.

For S39421 and LTC1643L Hot Swap Controllers :
Populate R510 and R15 is left open.



DRAWING NUMBER

DATE 16/4/1999 STREAM

EC

ISSUE 2 APPROVED DSGN JB MNGR TM

TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 13 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

SIZE D SHEETS 15 SHEET 13 STREAM

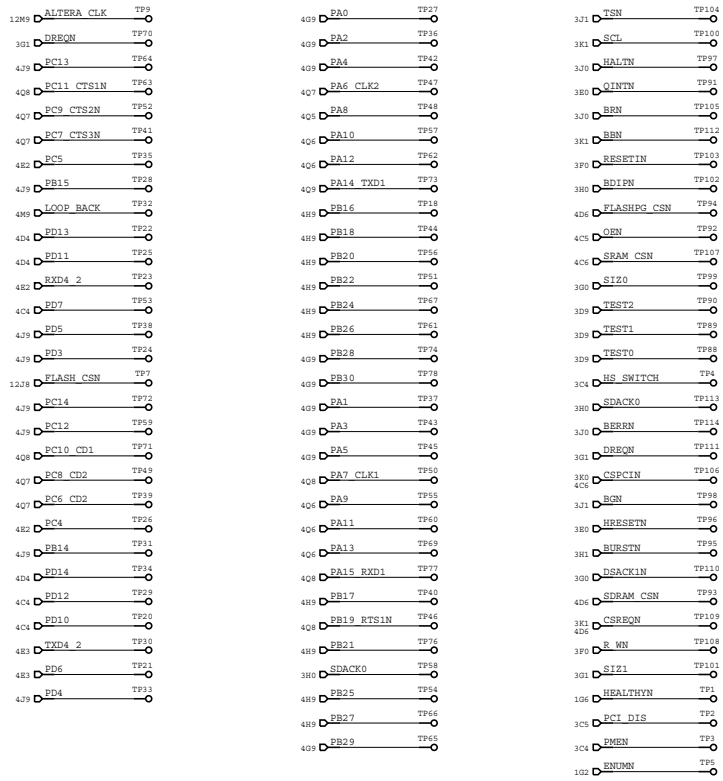
DESIGN

DRAWING NUMBER

PRINTED IN

GENERAL PURPOSE TESTPOINTS

NOTE: ALL TESTPOINTS ARE ON .1" CENTERS



TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 14 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

DRAWING NUMBER		
DATE 16/4/1999	STREAM	
EC		
ISSUE 2	APPROVED DSGN JB MNGR TM	
DESIGN		
DRAWING NUMBER		
SIZE D	SHEETS 15	SHEET 14 STREAM

PRINTED IN

ENGINEERING CHANGE ORDER

NOTE 1: A wire is required between the RSTCONF net (4N9) and TP6 (12A8).

DRAWING NUMBER

DATE 16/4/1999 | STREAM

EC

ISSUE 2 | APPROVED DSGN JB MNGR TM

TOP-LEVEL SHEET
BLOCK CALLISTO PAGE 15 OF 15

TITLE

QSPAN II EVALUATION BOARD

DRAWING # 3591862.SC001.01

SIZE D | SHEETS 15 | SHEET 15 | STREAM

DESIGN

DRAWING NUMBER

PRINTED IN