User's Manual

Multimedia Processor for Mobile Applications

DDR SDRAM Interface

EMMA Mobile™1

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[MEMO]

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the DDR SDRAM interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the DDR SDRAM interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Registers
- Chapter 4 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the DDR SDRAM interface of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB or xxxb
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		R19DS0008EJ (S19657E)
μPD77630A Data Sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	R19UH0027EJ (S19253E)
	DDR SDRAM Interface	This manual
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	R19UH0029EJ (S19265E)
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	R19UH0030EJ (S19598E)
	One Chip (μPD77630A)	R19UH0031EJ (S19687E)

( ) : old number

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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CHAPTER 1 OVERVIEW

The Mobile DDR SDRAM interface (MEMC) controls access to DDR SDRAM.

1.1 Features

○ External memory access control

The MEMC has a timing controller for the external memory interface. The usable memory is Mobile DDR SDRAM. The maximum operating frequency is 166 MHz.

The MEMC can generate refresh requests to execute refreshes required for DDR SDRAM.

For details about the following functions, see **CHAPTER 4 Usage**.

- Supported SDRAM
  - Mobile DDR SDRAM
  - 32-bit data bus connection (one chip that has a 32-bit bus, or two chips that have 16-bit buses connected in parallel)
  - Operating frequency: 133/166 MHz (DDR266/DDR333)
  - CS0 and CS1 supported.
    Maximum memory size per CS: 128 MB (1 Gb × 1 chip)
    16 MB (128 Mb × 1 chip) to 256 MB (1 Gb × 2 chips)
- Main functions
  - Flexible address mapping
  - Entering and exiting auto self refresh mode
  - Command control via software
  - Low power consumption due to clock control and automatic frequency control

○ Request control

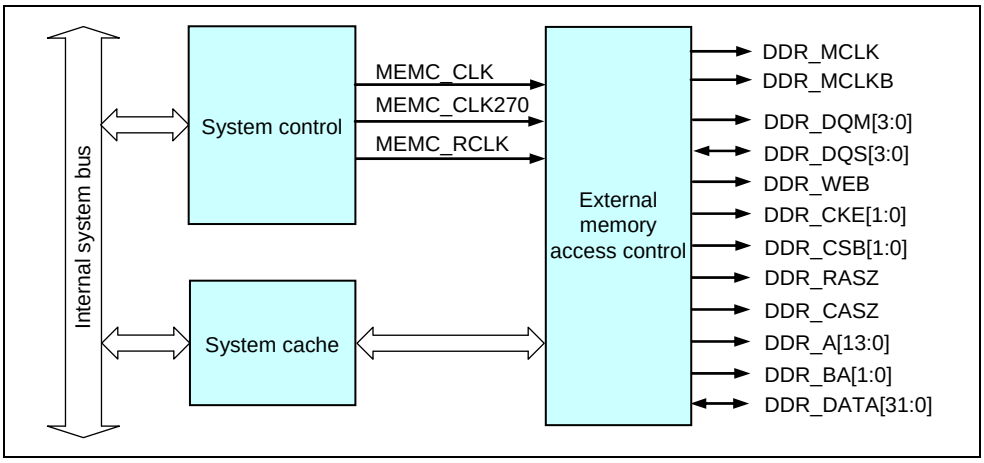
The MEMC controls requests sent from various macros so as to increase performance and decrease power consumption. The received read and write requests are held in queues in the MEMC, scheduled so as to enhance the memory usage efficiency, and issued to memory.

○ System cache (read cache)

The MEMC has a system cache for temporarily storing data read from memory. The read cache does not have dirty states. If a read request hits this cache, the request is not issued to memory. As a result, the latency while accessing memory is decreased and the number of memory accesses is reduced, which decreases power consumption.

1.2 Block Diagram

Figure 1-1. Block Diagram



1.3 Terminology

- MEMC: Mobile DDR SDRAM interface
- IMC: Image composer
- SHXB: Slow master AHB-AXI bridge
- MHXB: Media master AHB-AXI bridge
- DHXB: Display master AHB-AXI bridge
- ADSPD: Data bus for ADSP application DSP (SPXK701)
- ADSPI: Instruction bus for ADSP application DSP (SPXK701)
- ACPU: Application CPU
- ASMU: System management unit

CHAPTER 2 PIN FUNCTIONS

2.1 DDR SDRAM Interface Pins

Pin Name	I/O	After Reset	Function
DDR_MCLK	Output	32 kHz	Clock signal output
DDR_MCLKB	Output	Inverted 32 kHz	Inverted clock signal output
DDR_DQM[3:0]	Output	1111B	Write data mask
DDR_DQS[3:0]	I/O	PD (in)	Data strobe
DDR_WEB	Output	0	Write enable signal (low active)
DDR_CKE[1:0]Note	Output	0	Clock enable signal (low active)
DDR_CSB[1:0]	Output	00	Chip select signal (low active)
DDR_RASB	Output	0	Row address strobe signal (low active)
DDR_CASB	Output	0	Column address strobe signal (low active)
DDR_A[13:0]	Output	0	Address
DDR_BA[1:0]	Output	0	Bank address
DDR_DATA[31:0]	I/O	–	Data I/O

Note To keep the DDR_CKE pin level at 0 even if the MEMC is off, the output buffer is allocated in a separate power domain.

Remark PD (in): Has a pull-down resistor (when in the input status)

CHAPTER 3 REGISTERS

3.1 Registers

The MEMC registers allow word access only.
Do not access reserved registers. An undefined value is returned for a read access.
Do not write any value other than 0 to reserved bits in each register.

3.1.1 Request control registers and system cache setting registers

Base address: C00A_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Cache/prefetch setting register	MEMC_CACHE_MODE	R/W	0000_0000H
0004H	Reserved	–	–	–
0008H	Function disabling register	MEMC_DEGFUN	R/W	0000_0000H
000CH-0010H	Reserved	–	–	–
0014H	ACPU interrupt status register	MEMC_INTSTATUS_A	R	0000_0000H
0018H	ACPU interrupt raw status register	MEMC_INTRAWSTATUS_A	R	0000_0000H
001CH	ACPU interrupt enable set register	MEMC_INTENSET_A	R/W	0000_0000H
0020H	ACPU interrupt enable clear register	MEMC_INTENCLR_A	W	–
0024H	ACPU interrupt source clear register	MEMC_INTFFCLR_A	W	–
0028H-0064H	Reserved	–	–	–
0068H	Error master ID register	MEMC_ERRMID	R	0000_0000H
006CH	Error address register	MEMC_ERRADR	R/W	0000_0000H
0070H-0080H	Reserved	–	–	–

3.1.2 Memory request scheduler setting registers

Base address: C00A_0000H

Address	Register Name	Register Symbol	R/W	After Reset
1000H	Memory request scheduling mode register	MEMC_REQSCH	R/W	0000_0000H

3.1.3 External memory control registers

Base address: C00A_0000H

Address	Register Name	Register Symbol	R/W	After Reset
2000H	Memory connection setting register	MEMC_DDR_CONFIGF	R/W	0000_0808H
2004H	AC timing setting register 1	MEMC_DDR_CONFIGA1	R/W	5444_3203H
2008H	AC timing setting register 2	MEMC_DDR_CONFIGA2	R/W	00DA_0000H
200CH	Software command issuance register 1	MEMC_DDR_CONFIGC1	R/W	4040_0003H
2010H	Software command issuance register 2	MEMC_DDR_CONFIGC2	R/W	0000_03C0H
2014H	Refresh setting register 1	MEMC_DDR_CONFIGR1	R/W	7FFF_7FFFH
2018H	Refresh setting register 2	MEMC_DDR_CONFIGR2	R/W	1F5F_7C7CH
201CH	Refresh setting register 3	MEMC_DDR_CONFIGR3	R/W	0000_3F3FH
2020H	Automatic DQS timing adjustment register 1	MEMC_DDR_CONFIGT1	R/W	0000_0003H
2024H	Automatic DQS timing adjustment register 2	MEMC_DDR_CONFIGT2	R/W	0000_0000H
2028H	Automatic DQS timing adjustment register 3	MEMC_DDR_CONFIGT3	R/W	0000_0000H
202CH	Memory status check register	MEMC_DDR_STATE8	R/W	0000_0000H

3.2 Register Functions

3.2.1 Cache/prefetch setting register

This register (MEMC_CACHE_MODE: C00A_0000H) specifies whether to cache and prefetch data for each master device.

31	30	29	28	27	26	25	24
Reserved							DIS_IMC

23	22	21	20	19	18	17	16
Reserved	DIS_SHXB	DIS_MHXB	DIS_DHXB	DIS_DSPD	DIS_DSPI	DIS_ACPU	Reserved

15	14	13	12	11	10	9	8
Reserved							PRE_IMC

7	6	5	4	3	2	1	0
Reserved	PRE_SHXB	PRE_MHXB	PRE_DHXB	PRE_DSPD	PRE_DSPI	PRE_ACPU	Reserved

Name	R/W	Bit	After Reset	Function
Reserved	R	31:25	0H	Reserved. When these bits are read, 0 is returned for each bit.
DIS_IMC	R/W	24	0B	0: Caches data read from the IMC, 1: Does not cache data
Reserved	R	23	0B	Reserved. When this bit is read, 0 is returned.
DIS_SHXB	R/W	22	0B	0: Caches data read from the SHXB, 1: Does not cache data
DIS_MHXB	R/W	21	0B	0: Caches data read from the MHXB, 1: Does not cache data
DIS_DHXB	R/W	20	0B	0: Caches data read from the DHXB, 1: Does not cache data
DIS_DSPD	R/W	19	0B	0: Caches data read from the ADSPD, 1: Does not cache data
DIS_DSPI	R/W	18	0B	0: Caches data read from the ADSPI, 1: Does not cache data
DIS_ACPU	R/W	17	0B	0: Caches data read from the ACPU, 1: Does not cache data
Reserved	R	16:9	0H	Reserved. When these bits are read, 0 is returned for each bit.
PRE_IMC	R/W	8	0B	0: Does not prefetch data while reading data from the IMC. 1: Prefetches data while reading data from the IMC.
Reserved	R	7	0B	Reserved. When this bit is read, 0 is returned.
PRE_SHXB	R/W	6	0B	0: Does not prefetch data while reading data from the SHXB. 1: Prefetches data while reading data from the SHXB.
PRE_MHXB	R/W	5	0B	0: Does not prefetch data while reading data from the MHXB. 1: Prefetches data while reading data from the MHXB.
PRE_DHXB	R/W	4	0B	0: Does not prefetch data while reading data from the DHXB. 1: Prefetches data while reading data from the DHXB.
PRE_DSPD	R/W	3	0B	0: Does not prefetch data while reading data from the ADSPD. 1: Prefetches data while reading data from the ADSPD.
PRE_DSPI	R/W	2	0B	0: Does not prefetch data while reading data from the ADSPI. 1: Prefetches data while reading data from the ADSPI.
PRE_ACPU	R/W	1	0B	0: Does not prefetch data while reading data from the ACPU. 1: Prefetches data while reading data from the ACPU.
Reserved	R	0	0B	Reserved. When this bit is read, 0 is returned.

3.2.2 Function disabling register

This register (MEMC_DEGFUN: C00A_0008H) disables some of the MEMC functions.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

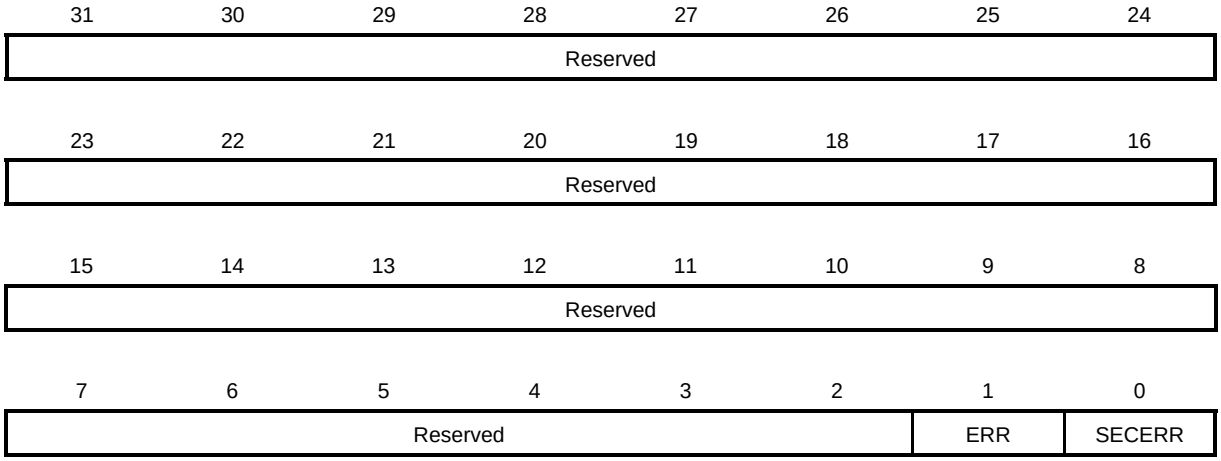
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						DISCACHE	INORDER

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0H	Reserved. When these bits are read, 0 is returned for each bit.
DISCACHE	R/W	1	0B	Disables the system cache. 0: Enables use of the system cache. 1: Disables use of the system cache.
INORDER	R/W	0	0B	0: Issues read requests out-of-order. 1: Issues read requests in order.

3.2.3 ACPU interrupt status register

This register (MEMC_INTSTATUS_A: C00A_0014H) indicates the status of the interrupt sources for the ACPU.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0H	Reserved. When these bits are read, 0 is returned for each bit.
ERR	R	1	0B	Indicates the status of error interrupts other than the security error interrupt. 0: No interrupt source 1: There is an interrupt source.
SECERR	R	0	0B	Indicates the status of the security error interrupt. 0: No interrupt source 1: There is an interrupt source.

3.2.4 ACPU interrupt raw status register

This register (MEMC_INTRAWSTATUS_A: C00A_0018H) indicates the status of the interrupt sources for the ACPU. The bits corresponding to the interrupt sources are set regardless of the settings of the interrupt enable set register and the interrupt enable clear register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

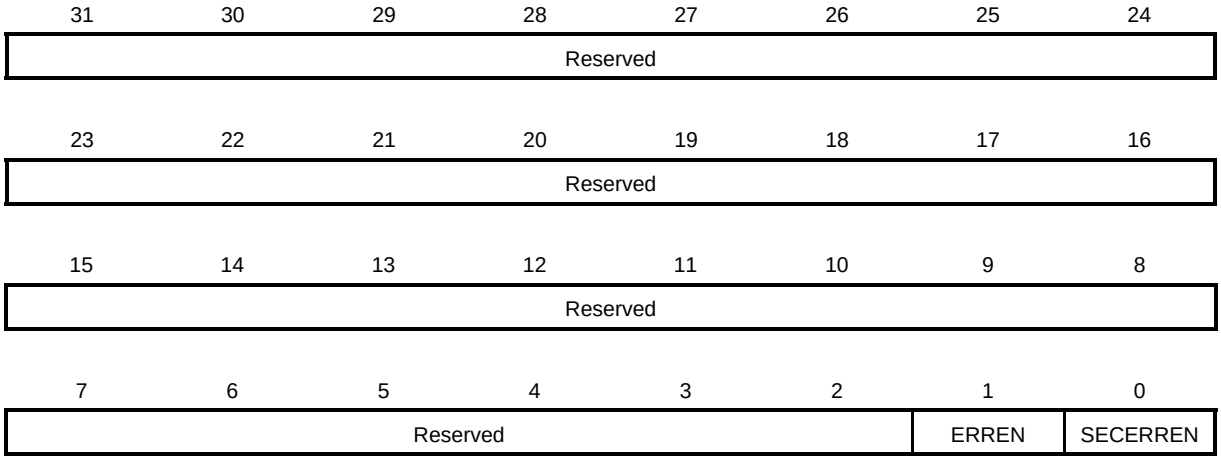
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						RAWERR	SECRAWERR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0H	Reserved. When these bits are read, 0 is returned for each bit.
RAWERR	R	1	0B	Indicates the raw status of error interrupts other than the security error interrupt. 0: No interrupt source 1: There is an interrupt source.
SECRAWERR	R	0	0B	Indicates the raw status of the security error interrupt. 0: No interrupt source 1: There is an interrupt source.

3.2.5 ACPU interrupt enable set register

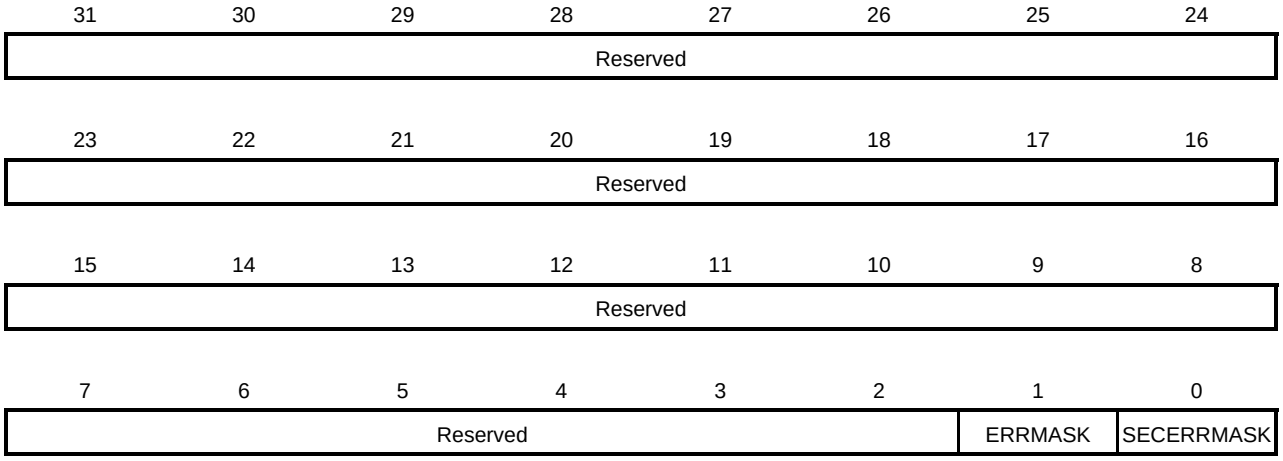
This register (MEMC_INTSET_A: C00A_001CH) enables the issuance of interrupt requests for the ACPU. Whether interrupt requests can be issued can be read from this register.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0H	Reserved. When these bits are read, 0 is returned for each bit.
ERREN	W	1	0B	Specifies whether to enable issuance of error interrupts other than the security error interrupt. 0: Ignored 1: Enables the interrupt.
	R			Indicates whether the issuance of error interrupts other than the security error interrupt is enabled. 0: Disabled (masked) 1: Enabled
SECERREN	W	0	0B	Specifies whether to enable issuance of the security error interrupt. 0: Ignored 1: Enables the interrupt.
	R			Indicates whether the issuance of the security error interrupt is enabled. 0: Disabled (masked) 1: Enabled

3.2.6 ACPU interrupt enable clear register

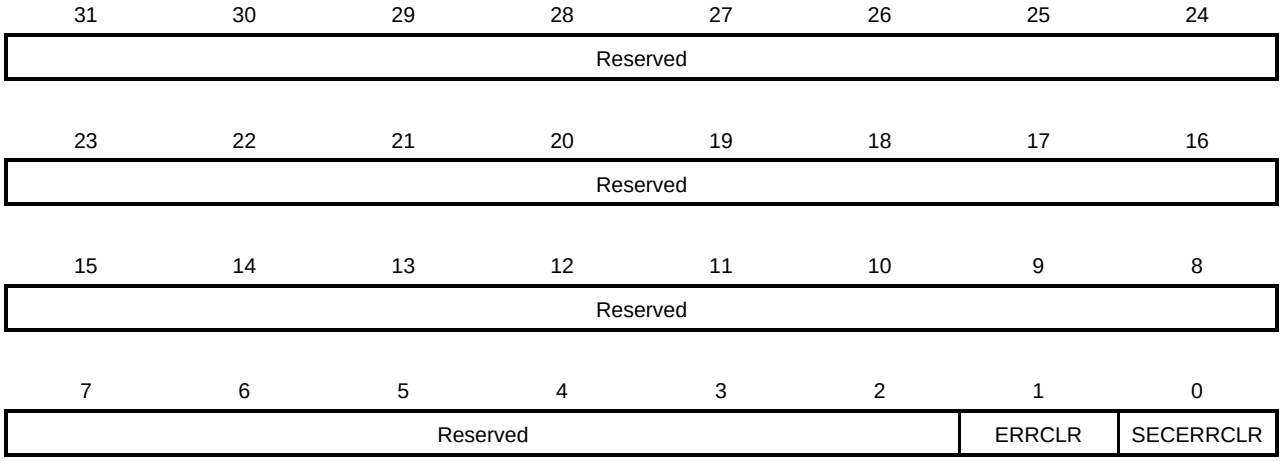
This register (MEMC_INTENCLR_A: C00A_0020H) masks (disables) the issuance of interrupt requests for the ACPU. Whether such issuance is masked can be determined by reading the MEMC_INTSET_A register.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0H	Reserved. When these bits are read, 0 is returned for each bit.
ERRMASK	W	1	0B	Specifies whether to disable (mask) the issuance of error interrupts other than the security error interrupt. 0: Ignored 1: Disables the sources. When read, 0 is returned.
SECERRMASK	W	0	0B	Specifies whether to disable (mask) the issuance of the security error interrupt. 0: Ignored 1: Disables the sources. When read, 0 is returned.

3.2.7 ACPU interrupt source clear register

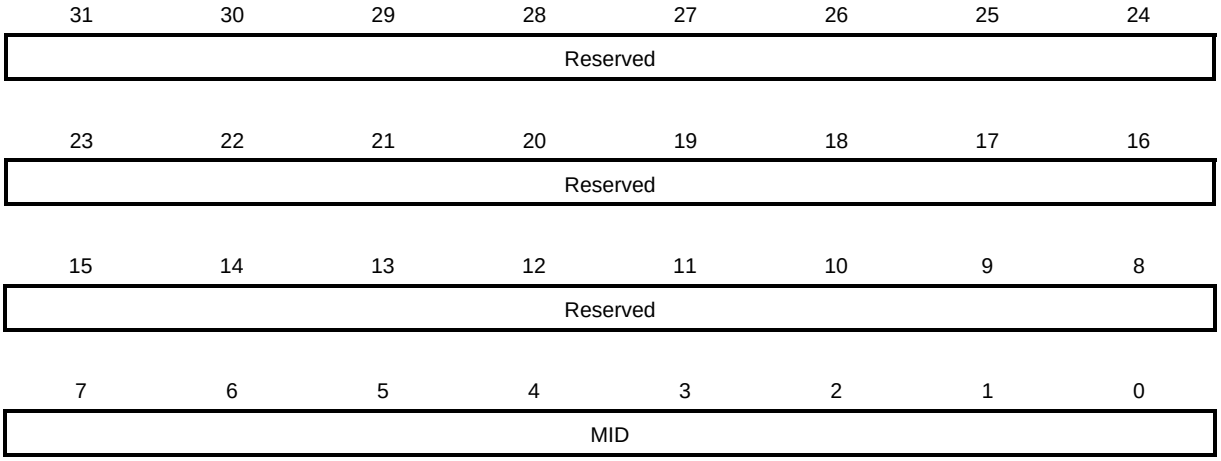
This register (MEMC_INTFFCLR_A: C00A_0024H) clears interrupt sources for the ACPU.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0H	Reserved. When these bits are read, 0 is returned for each bit.
ERRCLR	W	1	0B	Specifies whether to clear error interrupt sources other than the security error interrupt source. 0: Ignored 1: Clears the sources. When read, 0 is returned.
SECERRCLR	W	0	0B	Specifies whether to clear the security error interrupt source. 0: Ignored 1: Clears the sources. When read, 0 is returned.

3.2.8 Error master ID register

This register (MEMC_ERRMID: C00A_0068H) retains the ID of a master whose request caused an error.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0	Reserved. When these bits are read, 0 is returned for each bit.
MID	R	7:0	0	Retains the ID (master ID + AXI ID) when an error has occurred. These bits are not overwritten by the master ID of a new error until the current information is cleared by setting the CLEAR bit of MEMC_ERRADR.

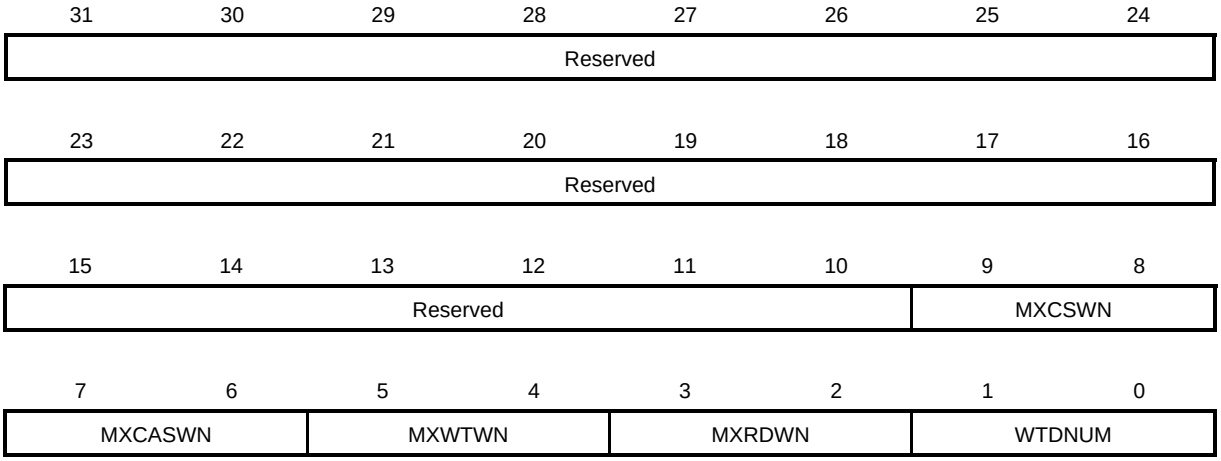
3.2.9 Error address register

This register (MEMC_ERRADR: C00A_006CH) retains the type of error and the address at which the error occurred.

Name	R/W	Bit	After Reset	Function
CLEAR	W	31	0H	Specifies whether to clear the retained address. 0: Ignored. 1: Clears the address. If an error occurs after this, the new address is retained.
	R			Indicates whether a new error address can be retained. 0: A new address can be retained when an error occurs. 1: A valid address is retained, so a new address is not retained.
RDWT	R	30	0B	Indicates whether the request that caused an error was for a read or write. 0: Read 1: Write
Reserved	R	29:28	0B	Reserved. When this bit is read, 0 is returned.
ADDR	R	27:3	0H	The value of bits 28 to 3 of the address at which a request caused an error is retained.
ERR	R	2:0	000B	Indicates what type of error a request caused. 000B: No error 011B: An address outside the mounted range was requested. 010B: Illegal burst size (A burst size larger than 64 bits was specified.) 011B: ARBURST and AWBURST are fixed or reserved. 100B: Illegal INCR burst (INCR burst in byte or halfword units) 101b: Illegal WRAP burst

3.2.10 Memory request scheduling mode register

This register (MEMC_REQSCH: C00A_1000H) specifies the schedule of requests for memory.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:10	0H	Reserved. When these bits are read, 0 is returned for each bit.
MXCSWN	R/W	9:8	00B	Specifies the maximum number of times the same CS can be selected in a row. 00B: No specification, 01B: 2 times, 10B: 4 times, 11B: 6 times
MXCASWN	R/W	7:6	00B	Specifies the maximum number of times a CAS request can be selected in a row. 00B: Once (Performs execution immediately after receiving a CAS request), 01B: 2 times, 10B: 4 times, 11B: 6 times
MXWTWN	R/W	5:4	00B	Specifies the maximum number of times a write request can be selected in a row for a read request during a write drain. 00B: No specification, 01B: 2 times, 10B: 4 times, 11B: 6 times
MXRDWN	R/W	3:2	00B	Specifies the maximum number of times a read request can be selected in a row for a write request during a write drain. 00B: No specification, 01B: 2 times, 10B: 4 times, 11B: 6 times
MTDNUM	R/W	1:0	00B	Specifies the number of requests for starting a write drain. 00B: 2, 01B: 4, 10B: 6, 11B: 8

3.2.11 Memory connection setting register

This register (MEMC_DDR_CONFIGF: C00A_2000H) specifies the configuration for the external memory.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
CS1_BANK_SPLIT		Reserved	CS1_DOUBLE	CS1_DENSITY		CS1_JEDEC	CS1_ENABLE

7	6	5	4	3	2	1	0
CS0_BANK_SPLIT		Reserved	CS0_DOUBLE	CS0_DENSITY		CS0_JEDEC	CS0_ENABLE

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0H	Reserved. When these bits are read, 0 is returned for each bit.
CS1_BANK_SPLIT	R/W	15:14	00B	Specifies the number of banks for interleaving for CS1 (see **Figure 3-1**) 00B: 4-bank interleave 01B: 2-bank interleave 10B: No interleave 11B: Lower two banks interleaved, higher two banks not interleaved
Reserved	R	13	0H	Reserved. When this bit is read, 0 is returned.
CS1_DOUBLE	R/W	12	0B	Indicates whether two CS1 chips (16-bit bus chip × 2) may be used. 0: Not used. (32-bit bus chip × 1) 1: May be used (16-bit bus chip × 2)
CS1_DENSITY	R/W	11:10	00B	Specifies the memory size of CS1. 00B: 128 Mb, 01B: 256 Mb, 10B: 512 Mb, 11B: 1 Gb
CS1_JEDEC	R/W	9	0H	0: Non-JEDEC, 1: JEDEC
CS1_ENABLE	R/W	8	0B	Specifies whether to enable access to CS1 memory. 0: Disables access, 1: Enables access
CS0_BANK_SPLIT	R/W	7:6	00B	Specifies the number of banks for interleaving for CS0 (see **Figure 3-1**) 00B: 4-bank interleave 01B: 2-bank interleave 10B: No interleave 11B: Lower two banks interleaved, higher two banks not interleaved
Reserved	R	5	0H	Reserved. When this bit is read, 0 is returned.
CS0_DOUBLE	R/W	4	0B	Indicates whether two CS0 chips (16-bit bus chip × 2) may be used. 0: Not used. (32-bit bus chip × 1) 1: May be used (16-bit bus chip × 2)
CS0_DENSITY	R/W	3:2	00B	Specifies the memory size of CS0. 00B: 128 Mb, 01B: 256 Mb, 10B: 512 Mb, 11B: 1 Gb
CS0_JEDEC	R/W	1	0H	0: Non-JEDEC, 1: JEDEC
CS0_ENABLE	R/W	0	0B	Specifies whether to enable access to CS0 memory. 0: Disables access, 1: Enables access

Bank addressing can be changed individually for CS0 and CS1. DDR SDRAM assigns bank addresses to column addresses consecutively and reads out up to 4 KB of data in succession. However, because memory is separated into banks, data cannot be read consecutively when using the partial refresh function (a function for retaining only specific data in memory), and consecutiveness in memory areas that must be maintained is not assured. Specify settings by using this register to avoid this problem. Table 3-1 shows an example of address assignment and Figure 3-1 shows an overview of the mapping.

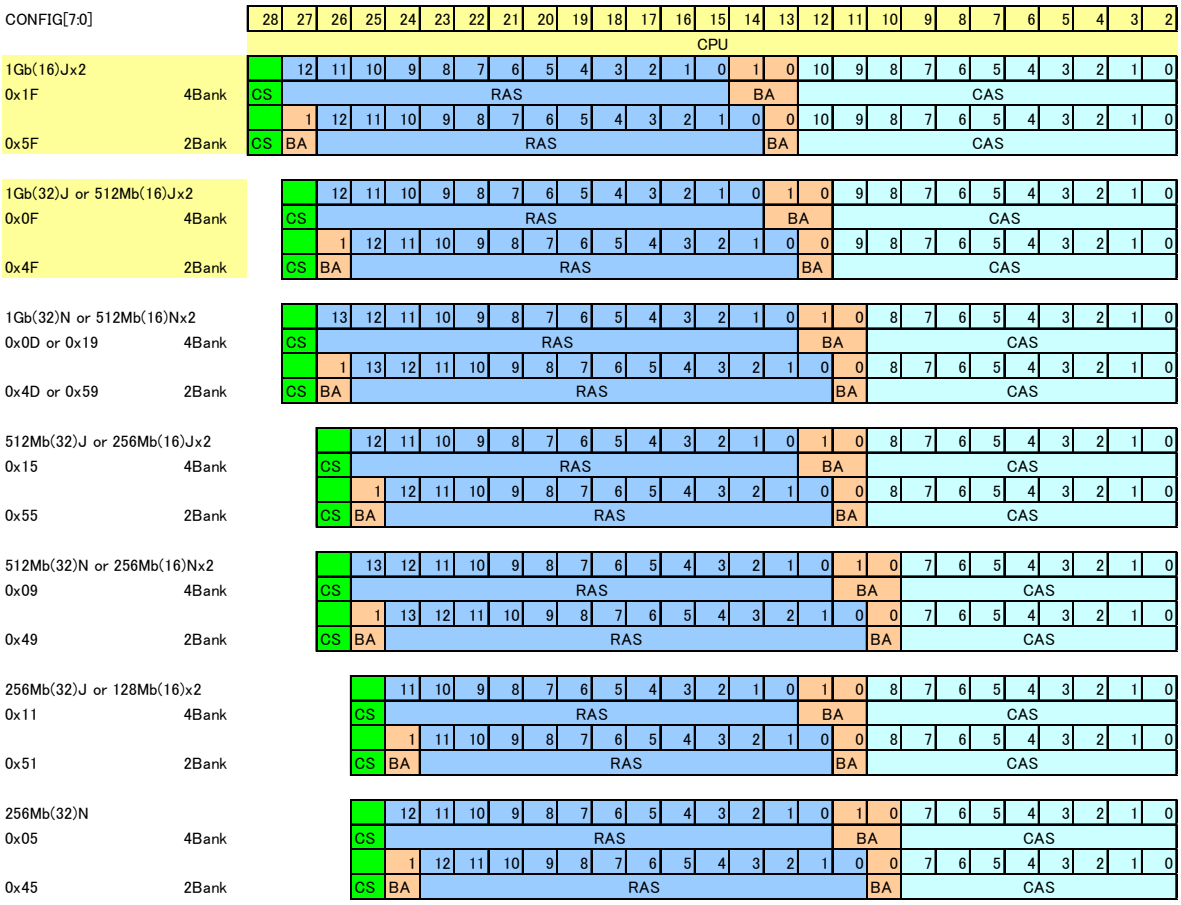


Table 3-1. Correspondence of CPU Address and External Memory Address (JEDEC)

Memory Size	Bank Interleave	Reg. setting CS0[7:6] CS1[15:14]	CPU Address A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
			DRAM Address																											
256 Mb	4-bank	b'00					A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0	
	2-bank	b'01					BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0	
	0-bank	b'10					BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	A8	A7	A6	A5	A4	A3	A2	A1	A0	
	4-bank (BA1 = L)	b'11				BA1 = L	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0	
	2-bank (BA1 = H)					BA1 = H	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0	
512 Mb	4-bank	b'00			A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	2-bank	b'01			BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	0-bank	b'10			BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	4-bank (BA1 = L)	b'11		BA1 = L	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	2-bank (BA1 = H)			BA1 = H	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA0	A8	A7	A6	A5	A4	A3	A2	A1	A0		
1 Gb	4-bank	b'00		A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	2-bank	b'01		BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	0-bank	b'10		BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	4-bank (BA1 = L)	b'11	BA1 = L	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA1	BA0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
	2-bank (BA1 = H)		BA1 = H	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	BA0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		

Figure 3-1. External Memory Address Mapping

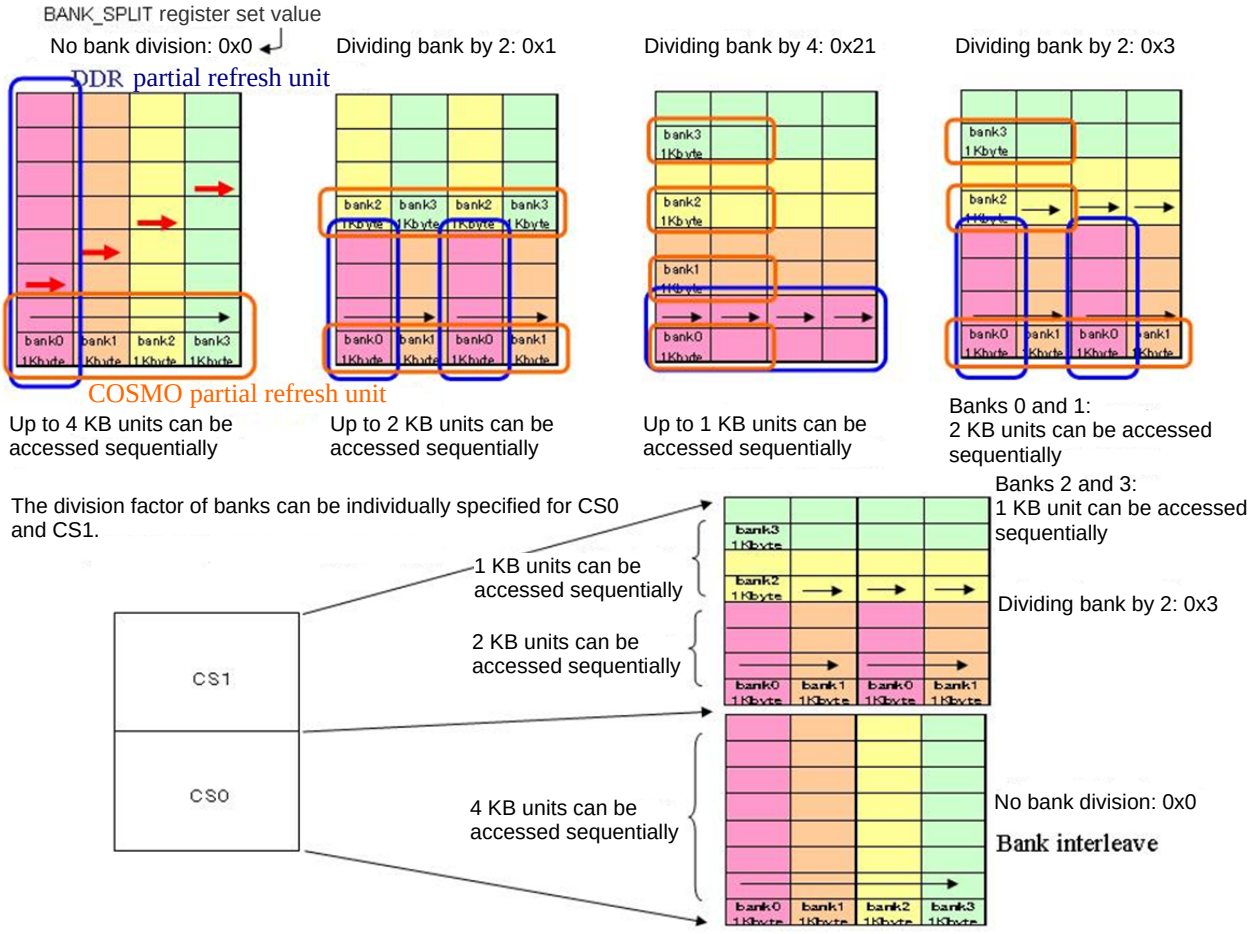


Table 3-2. DDR SDRAM (JEDEC)

32-bit bus chip × 1

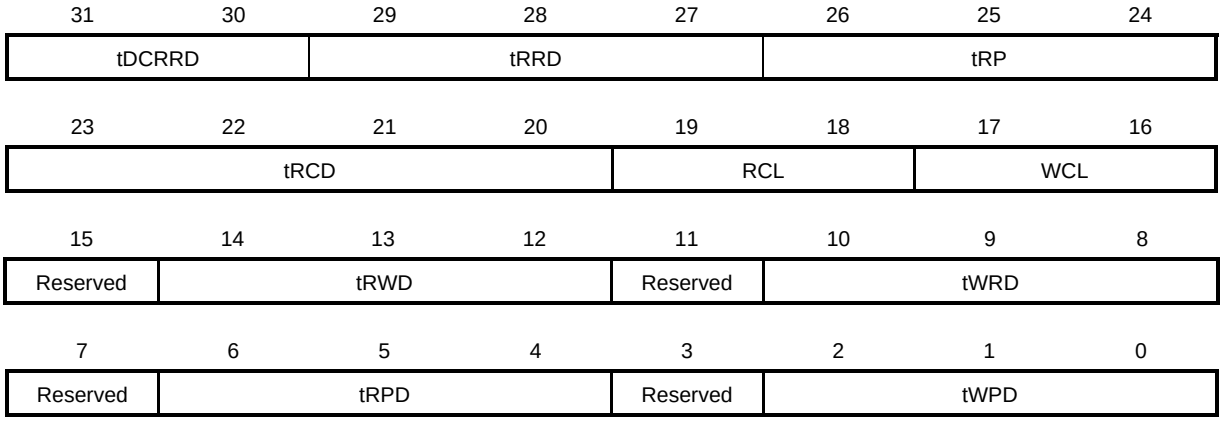
Size	Word	Bus Width	Row	Column	BA
256 Mb	8 M	32	A[11:0]	A[8:0]	BA[1:0]
512 Mb	16 M	32	A[12:0]	A[8:0]	BA[1:0]
1 Gb	32 M	32	A[12:0]	A[9:0]	BA[1:0]

16-bit bus chip × 2

Size	Word	Bus Width	Row	Column	BA
128 Mb	8 M	32	A[11:0]	A[8:0]	BA[1:0]
256 Mb	16 M	32	A[12:0]	A[8:0]	BA[1:0]
512 Mb	32 M	32	A[12:0]	A[9:0]	BA[1:0]
1 Gb	64 M	32	A[12:0]	A[10:0]	BA[1:0]

3.2.12 AC timing setting register 1

This register (MEMC_DDR_CONFIGA1: C00A_2004H) determines the AC timing of external memory.



Name	R/W	Bit	After Reset	Function
tDCRRD	R	31:30	01B	Specifies the number of cycles required from a read (write) command to a read (write) command between chips. Specifying 0 is prohibited.
tRRD	R/W	29:27	010B	Specifies the reference clock cycles between bank activating commands.
tRP	R/W	26:24	100B	Specifies the reference clock cycles from a precharge command to a bank activating command.
tRCD	R/W	23:20	100B	Specifies the period from a bank activating command to a read command and a bank activating command to a write command. 0x3 at 166 MHz, 0x2 at 133 MHz, 0x1 at 100 MHz → RL = tRCD + RCL, W L = tRCD + WCL − 1[Note 2]
RCL	R/W	19:18	01B	Specifies the read CAS latency. 00B: CL = 2, 01B: CL = 3, 10B: CL = 4, 11B: CL = 5
WCL	R/W	17:16	00B	Specifies the write CAS latency. 00B: CL = 1, 01B: CL = 2, 10B: CL = 3, 11B: CL = 4
Reserved	R	15	0B	Reserved. When this bit is read, 0 is returned.
tRWD	R/W	14:12	11B	Specifies the period from a read command to a write command. *tRWD + 4* clock cycles
Reserved	R	11	0B	Reserved. When this bit is read, 0 is returned.
tWPD	R/W	10:8	10B	Specifies the period from a write command to a read command. *tWPD + 4* clock cycles
Reserved	R	7	0B	Reserved. When this bit is read, 0 is returned.
tRPD	R/W	6:4	000B	Specifies the period from a read command to a precharge command. *tRPD + 4* clock cycles
Reserved	R	3	0B	Reserved. When this bit is read, 0 is returned.
tWPD	R/W	2:0	011B	Specifies the period from a write command to a precharge command. *tWPD + 4* clock cycles

Note tRCDR = tRCDW + 1, RL = tRCDW + RCL, WL = tRCDW + WCL − 1
Because the same AC parameters are applied to CS0 and CS1, devices whose AC timing specifications differ cannot be connected to CS0 and CS1 at the same time.

3.2.13 AC timing setting register 2

This register (MEMC_DDR_CONFIGA2: C00A_2008H) specifies the AC timing parameters for external memory and is used to expand some functions.

31	30	29	28	27	26	25	24
Reserved				CS1H	CS0H	ADD_HZ	CMD_HZ

23	22	21	20	19	18	17	16
tSREX				tRFC			

15	14	13	12	11	10	9	8
Reserved			LowFrqTyp	DQS_mask_Ext	DQS_mask		DQM_HZ

7	6	5	4	3	2	1	0
IO_HZ	AutoPre	CLK_MODE		PstamblExt	PreamblExt	DBParkEna	Reserved

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:28	0H	Reserved. When these bits are read, 0 is returned for each bit.
CS1H	R/W	27	0B	Forcibly sets CS1 to high level. 0: Active, 1: High level
CS0H	R/W	26	0B	Forcibly sets CS0 to high level. 0: Active, 1: High level
ADD_HZ	R/W	25	0B	Specifies the state of the I/O buffer for address signals. 0: Active, 1: Hi-Z
CMD_HZ	R/W	24	0B	Specifies the state of the I/O buffer for command signals. 0: Active, 1: Hi-Z
tSREX	R/W	23:20	DH	Specifies the period until returning from a self refresh. [*(tSREX + 8) – 1)*] clock cycles *__Note__
tRFC	R/W	19:16	AH	Specifies the period until returning from an auto refresh. *tRFC + 8* clock cycles
Reserved	R	15:13	0H	Reserved. When these bits are read, 0 is returned for each bit.
LowFrqTyp	R/W	12	0B	Switches the frequency range in the low-frequency mode. 0: 30 MHz or less, 1: 30 MHz to 60 MHz
DQS_mask_Ext	R/W	11	0B	Specifies whether to delay the input DQS mask timing by 0.5 clock cycles. 0: Does not delay the timing. 1: Delays the period.
DQS_mask	R/W	10:9	00B	Specifies how much the input DQS mask timing is delayed. 00B: 2 clock cycles, 01B: 2.5 clock cycles, 10B: 3 clock cycles, 11B: Reserved

(2/2)

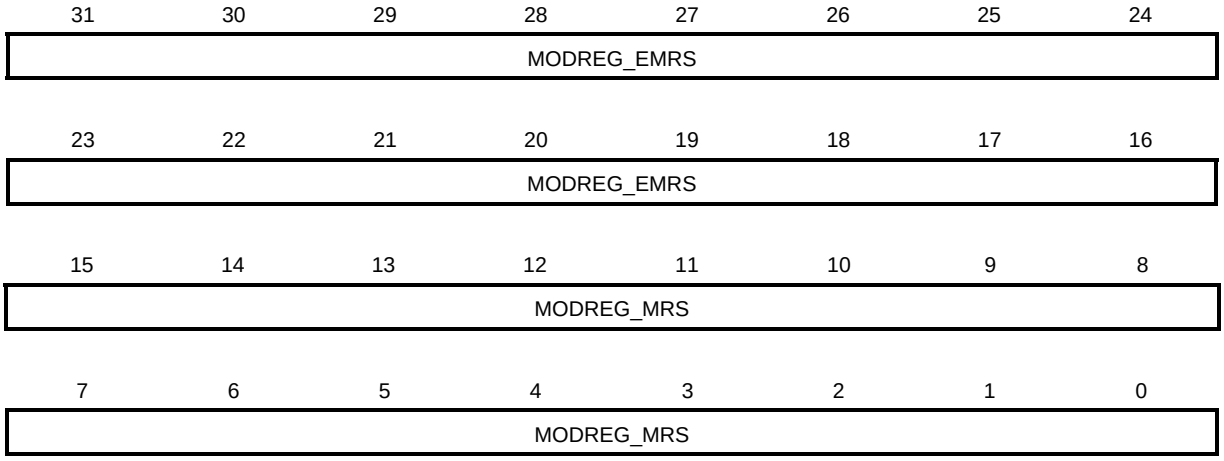
Name	R/W	Bit	After Reset	Function
DQM_HZ	R/W	8	0B	Specifies the state of the DQM signal for the I/O buffer. 0: Active, 1: Hi-Z
IO_HZ	R/W	7	0B	Specifies the state of the signal for the I/O buffer. 0: Active, 1: Hi-Z
AutoPre	R/W	6	1B	Specifies whether to enable auto precharge. 0: Does not enable auto precharge, 1: Enables auto precharge
CLK_MODE	R/W	5:4	00B	Specifies the timing at which read data is received. 00B: 2-clock cycle mode, 01B: 3-clock cycle mode, 10B: 1-clock cycle mode, 11B: Reserved
PstamblExt	R/W	3	0B	Specifies whether to extend the period for which the DQS postamble is output during a write by 0.5 clock cycles. 0: Does not extend the period, 1: Extend the period
PreamblExt	R/W	2	0B	Specifies whether to extend the period for which the DQS preamble is output during a write by 0.5 clock cycles. 0: Does not extend the period, 1: Extend the period
DBParkEna	R/W	1	0B	Specifies whether to drive DQ or DQS to low level while DDR SDRAM is in the Hi-Z state. 0: Hi-Z control 1: Drive to low level for periods other than the period when data is valid.
Reserved	R	0	0B	Reserved. When this bit is read, 0 is returned.

Remark Because the same AC parameters are applied to CS0 and CS1, devices whose AC timing specifications differ cannot be connected to CS0 and CS1 at the same time.

Note The maximum of tSREX which can be put at the time of DDR333 (166MHz) movement is 6ns × (15 + 8-1)= 132 ns. SDRAM with any more min standard can't be connected.

3.2.14 Software command issuance register 1

This register (MEMC_DDR_CONFIGC1: C00A_200CH) specifies addresses and data when the extended mode register is set up for external memory.



Name	R/W	Bit	After Reset	Function
MODREG_EMRS	R/W	31:16	4040H	Specifies mode register setting command issuance address 2 (DDR SDRAM: BA1, BA0, A[13:0])
MODREG_MRS	R/W	15:0	0003H	Specifies mode register setting command issuance address 1 (DDR SDRAM: BA1, BA0, A[13:0])

A command that sets up an extended mode register is issued for external memory based on the address specified for the MODREG_EMRS bit.

A command that sets up an extended mode register is issued for external memory based on the address specified for the MODREG_MRS bit. The address is fixed to 0xFF FFF0.

When setting up a mode register and issuing the Initialize, MRS, or EMRS command, set up this register as follows:

Initialize command MODREG_EMRS = {2'b10, *EMRS setting*}, MODREG_MRS = {2'b00, *MRS setting*}
MRS command MODREG_EMRS = {2'b00, *MRS setting*}, MODREG_MRS = {2'b00, *any value*}
EMRS command MODREG_EMRS = {2'b10, *EMRS setting*}, MODREG_MRS = {2'b00, *any value*}

When issuing precharge commands, set up this register as follows:

All bank precharge MODREG_MRS[10] = 1'b1
Bank precharge MODREG_MRS[15:14] = Target bank address, MODREG_MRS[10] = 1'b0

Restriction and caution on command issuance:

- Requests to issue commands are ignored when the CMD_STATE bit of the MEMC_DDR_CONFIGC2 register is set to 0 (busy).

3.2.15 Software command issuance register 2

This register (MEMC_DDR_CONFIGC2: C00A_2010H) specifies the settings for controlling command issuance for external memory.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved						CMD_STATE (CS1)	CMD_STATE (CS0)

7	6	5	4	3	2	1	0
CMD_REQ_ LOCK	CMD_ ENABLE	CS1_TARGET	CS0_TARGET	CMD_SET			

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:10	0H	Reserved. When these bits are read, 0 is returned for each bit.
CMD_STATE(CS1)	R	9	1B	Indicates the execution status of a command requested by CS. 0: Busy, 1: Standby
CMD_STATE(CS0)	R	8	1B	Indicates the execution status of a command requested by CS. 0: Busy, 1: Standby
CMD_REQ_LOCK	R/W	7	1B	Specifies the signal to lock any request other than for command issuance. 0: Lock, 1: Unlock
CMD_ENABLE	R/W	6	1B	Specifies whether to issue a command request. 0: Requests command issuance. This bit is automatically set to 1 during the next clock cycle.
CS1_TARGET	R/W	5	0B	Sets the command request flag for CS1. 0: Does not set the flag. 1: Sets the flag.
CS0_TARGET	R/W	4	0B	Sets the command request flag for CS0. 0: Does not set the flag. 1: Sets the flag.

(2/2)

Name	R/W	Bit	After Reset	Function
CMD_SET	R/W	3:0	0H	Specifies the control command. 0111B: Disables the CKE signal. 1000B: Executes the DDR SDRAM initialization sequence. 1001B: Precharges all banks. 1010B: Executes a CBR refresh. 1011B: Shifts to the self refresh mode. 1100B: Shifts to the deep power down mode. 1101B: Enables the CKE signal. 1110B: Reads from the (extended) mode register. 1111B: Writes to the (extended) mode register.

The command specified by the CMD_SET bit can be issued if a command code is specified for the target memory at the same time as the CMD_ENABLE bit is set to 0 in this register.

The memory assigned to CS0 and CS1 can be specified as target memory at the same time.

Before setting the CMD_ENABLE bit, make sure that the CMD_STATE bit is set to 1.

No command requests are accepted if the CMD_STATE bit is set to 0 (busy) upon command issuance. After a command request is issued while the CMD_REQ_LOCK bit is set to 0 (locked), only requests for software commands are accepted.

When the deep power down mode is entered, cancel the auto self refresh and CBR refresh for the target CS.

3.2.16 Refresh setting register 1

This register (MEMC_DDR_CONFIGR1: C00A_2014H) individually specifies refresh cycles in external memory for CS0 and CS1.

31	30	29	28	27	26	25	24
CS1_REF_OVER	CS1_REF_STOCK			CS1_CBR_SREF	CS1_REF_COUNT		

23	22	21	20	19	18	17	16
CS1_REF_COUNT							

15	14	13	12	11	10	9	8
CS0_REF_OVER	CS0_REF_STOCK			CS0_CBR_SREF	CS0_REF_COUNT		

7	6	5	4	3	2	1	0
CS0_REF_COUNT							

Name	R/W	Bit	After Reset	Function
CS1_REF_OVER	R	31	0B	Indicates whether the number of times refreshes for CS1 still needs to be executed exceeds the maximum.
CS1_REF_STOCK	R	30:28	7H	Indicates the number of times refreshes for CS1 still needs to be executed.
CS1_CBR_SREF	R/W	27	1B	Specifies whether to forcibly execute a CBR refresh at least once when CS1 is in the self refresh mode.
CS1_REF_COUNT	R/W	26:16	7FFH	Specifies the CS1 refresh timer counter value. Refresh cycle = RCLK (refresh counter clock) cycles × specified value
CS0_REF_OVER	R	15	0B	Indicates whether the number of times refreshes for CS0 still needs to be executed exceeds the maximum.
CS0_REF_STOCK	R	14:12	7H	Indicates the number of times refreshes for CS0 still needs to be executed
CS0_CBR_SREF	R/W	11	1B	Specifies whether to forcibly execute a CBR refresh at least once when CS0 is in the self refresh mode.
CS0_REF_COUNT	R/W	10:0	7FFH	Specifies the CS0 refresh timer count value. Refresh cycle = RCLK (refresh counter clock) cycles × specified value

The refresh counter is incremented during each refresh cycle by the REF_STOCK counter. A refresh is executed when the self refresh mode is entered or when the refresh counter reaches the threshold.

3.2.17 Refresh setting register 2

This register (MEMC_DDR_CONFIGR2: C00A_2018H) specifies the settings for a refresh in external memory.

31	30	29	28	27	26	25	24
Reserved	STOCK_ DRAIN_TYP	CS1_STOCK_DRAIN		CS1_STOCK_MAX			CS1_TIMER _RST

23	22	21	20	19	18	17	16
Reserved	COUNT_ COMMON	CS0_STOCK_DRAIN		CS0_STOCK_MAX			CS0_TIMER _RST

15	14	13	12	11	10	9	8
CS1_SREF_COUNT						CS1_SREF_ AUTO	CS1_REF_ AUTO

7	6	5	4	3	2	1	0
CS0_SREF_COUNT						CS0_SREF_ AUTO	CS0_REF_ AUTO

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	0B	Reserved. When this bit is read, 0 is returned.
STOCK_DRAIN_TYP	R/W	30	0B	Specifies whether to decrement the refresh counter (whether to execute CBR) when no read request is being received and the number of write requests is the write buffer drain threshold value or lower.
CS1_STOCK_DRAIN	R/W	29:28	01B	Specifies how many times a refresh is executed before CS1 enters the self refresh mode. Specifiable range: 1 to 3 (Specifying 0 is prohibited.)
CS1_STOCK_MAX	R/W	27:25	7H	Specifies the maximum number of refreshes for CS1. Specifiable range: 1 to 7 (Specifying 0 is prohibited.)
CS1_TIMER_RST	R/W	24	1B	Specifies whether to reset CS1_REF_COUNT, CS1_REF_STOCK, and CS1_REF_OVER. 0: Reset This bit is automatically set to 1 during the next clock cycle.
Reserved	R	23	0B	Reserved. When this bit is read, 0 is returned.
COUNT_COMMON	R/W	22	1B	Specifies whether to apply the auto refresh cycle for CS0 to CS1. (The counter for CS1 stops.)
CS0_STOCK_DRAIN	R/W	21:20	01B	Specifies how many times a refresh is executed before CS0 enters the self refresh mode. Specifiable range: 1 to 3 (Specifying 0 is prohibited.)
CS0_STOCK_MAX	R/W	19:17	7H	Specifies the maximum number of refreshes for CS0. Specifiable range: 1 to 7 (Specifying 0 is prohibited.)

(2/2)

Name	R/W	Bit	After Reset	Function
CS0_TIMER_RST	R/W	16	1B	Specifies whether to reset CS0_REF_COUNT, CS0_REF_STOCK, and CS0_REF_OVER. 0: Reset This bit is automatically set to 1 during the next clock cycle.
CS1_SREF_COUNT	R/W	15:10	1FH	Specifies CS1 self refresh counter values. Auto self refresh entry idle counter set value multiplied by 16.
CS1_SREF_AUTO	R/W	9	0B	Specifies whether to enable issuance of CS1 auto self refresh requests (SREF). 0: Disable, 1: Enable
CS1_REF_AUTO	R/W	8	0B	Specifies whether to enable issuance of CS1 auto refresh requests (CBR). 0: Disable, 1: Enable
CS0_SREF_COUNT	R/W	7:2	1FH	Specifies CS0 self refresh counter values. Auto self refresh entry idle counter set value multiplied by 16.
CS0_SREF_AUTO	R/W	1	0B	Specifies whether to enable issuance of CS0 auto self refresh requests (SREF). 0: Disable, 1: Enable
CS0_REF_AUTO	R/W	0	0B	Specifies whether to enable issuance of CS0 auto refresh requests (CBR). 0: Disable, 1: Enable

The refresh counter is incremented during each refresh cycle by the REF_STOCK counter. A refresh is executed when the self refresh mode is entered or when the refresh counter reaches the threshold. When the REF_STOCK counter exceeds the maximum value, the CS0/1_REF_OVER bits of the MEMC_DDR_CONFIGR1 register are set to 1.

3.2.18 Refresh setting register 3

This register (MEMC_DDR_CONFIGR3: C00A_201CH) specifies the settings for a refresh in external memory.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
CS1_APD_COUNT						Reserved	CS1_APD_AUTO

7	6	5	4	3	2	1	0
CS0_APD_COUNT						Reserved	CS0_APD_AUTO

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0H	Reserved. When these bits are read, 0 is returned for each bit.
CS1_APD_COUNT	R/W	15:10	3FH	Specifies the automatic CS1 power down counter value (the idle counter value).
Reserved	R	9	0B	Reserved. When this bit is read, 0 is returned.
CS1_APD_AUTO	R/W	8	0B	Specifies whether to request an automatic CS1 power down. 0: Normal operation, 1: Requested
CS0_APD_COUNT	R/W	7:2	3FH	Specifies the automatic CS0 power down counter value (the idle counter value).
Reserved	R	1	0B	Reserved. When this bit is read, 0 is returned.
CS0_APD_AUTO	R/W	0	0b	Specifies whether to request an automatic CS0 power down. 0: Normal operation, 1: Requested

When no received requests remain in the request queue, the counter is incremented up to the value set to the CS0/1_APD_COUNT bits and then the corresponding CS automatically enters the power down mode (CKE = low level).

3.2.19 Automatic DQS timing adjustment register 1

This register (MEMC_DDR_CONFIGT1: C00A_2020H) specifies the adjustment of delays in external memory.

31	30	29	28	27	26	25	24
Reserved				MCLK_DELAY			

23	22	21	20	19	18	17	16
Reserved			CLK270_DELAY				

15	14	13	12	11	10	9	8
Reserved			DQS_O_DELAY				

7	6	5	4	3	2	1	0
Reserved					CALIBRATE_PAT	CALIBRATE_STATE	AUTO_CALIBRATE

Name	R/W	Bit	After Reset	Function
Reserved	R	31:28	0H	Reserved. When these bits are read, 0 is returned for each bit.
MCLK_DELAY	R/W	27:24	0H	Adjusts the MCLK delay (delay 1).
Reserved	R	23:21	0H	Reserved. When these bits are read, 0 is returned for each bit.
CLK270_DELAY	R/W	20:16	0H	Adjusts the CLK270 delay (delay 4).
Reserved	R	15:12	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS_O_DELAY	R/W	11:8	0H	Adjusts the delay of DQS output (delay 3).
Reserved	R	7:3	0H	Reserved. When these bits are read, 0 is returned for each bit.
CALIBRATE_PAT	R/W	2	0B	Specifies the calibration pattern. 0: 0xFFFF → 0x0000, 1: 0xAAAA → 0x5555
CALIBRATE_STATE	R/W	1	1B	Indicates the calibration status. 0: Busy, 1: Ready
AUTO_CALIBRATE	R/W	0	1B	Specifies the start of automatic calibration. 0: Calibration starts.

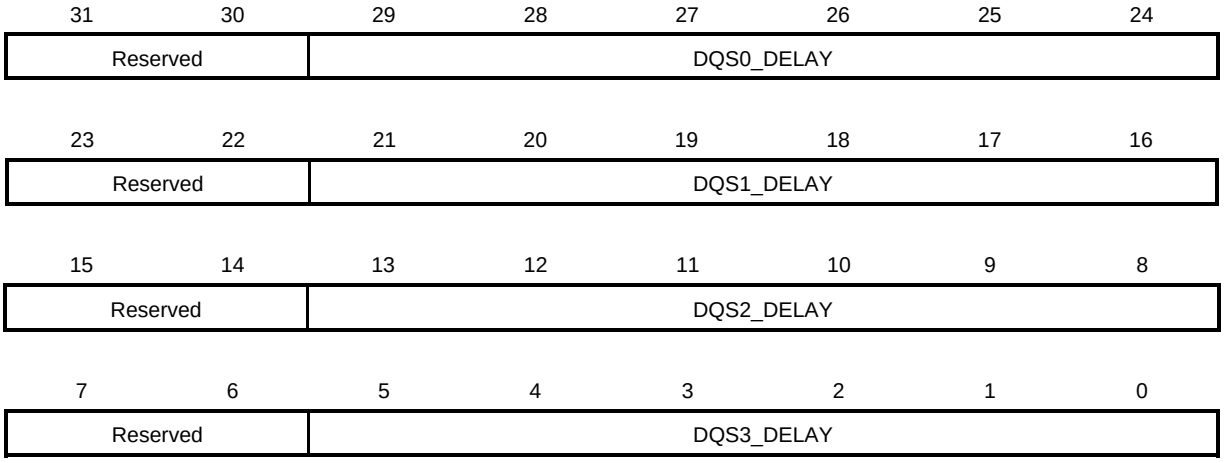
Delays can be added to each signal line by setting up this register.

The optimum delay values obtained by calibration are stored in the MEMC_DDR_CONFIGT3 register.

When the delay is adjusted using this register, set the MEMCCLK270_SEL bit of the MEMCCLK270_SEL register to 1 in the ASMU.

3.2.20 Automatic DQS timing adjustment register 2

This register (MEMC_DDR_CONFIGT2: C00A_2024H) specifies the automatic adjustment of delays in external memory.

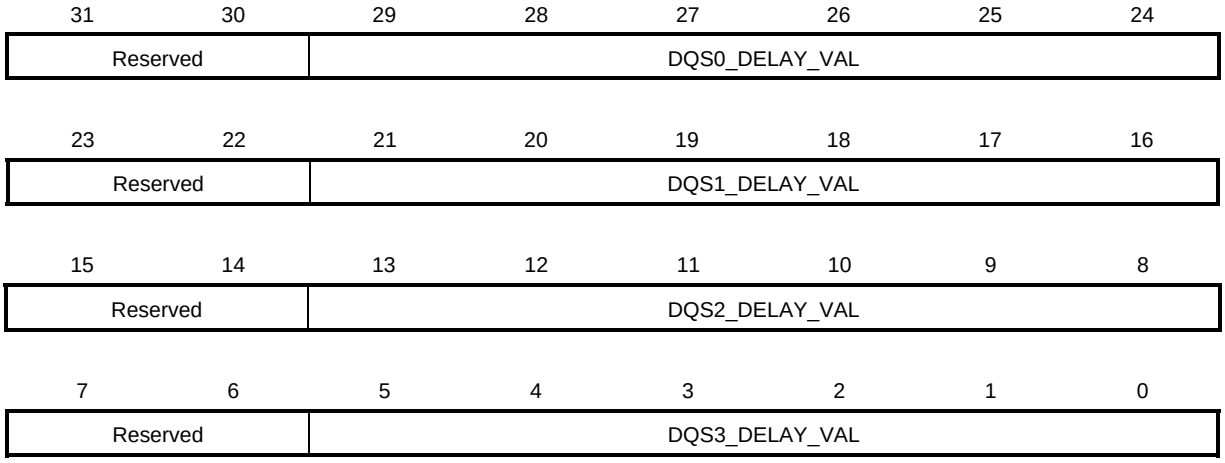


Name	R/W	Bit	After Reset	Function
Reserved	R	31:30	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS0_DELAY	R/W	29:24	0H	Optimizes the DQS0 delay.
Reserved	R	23:22	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS1_DELAY	R/W	21:16	0H	Optimizes the DQS1 delay.
Reserved	R	15:14	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS2_DELAY	R/W	13:8	0H	Optimizes the DQS2 delay.
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS3_DELAY	R/W	5:0	0H	Optimizes the DQS3 delay.

Delays can be added to each input DQS signal line by setting up this register.

3.2.21 Automatic DQS timing adjustment register 3

This register (MEMC_DDR_CONFIGT3: C00A_2028H) stores the result of adjustment for automatic calibration delays.

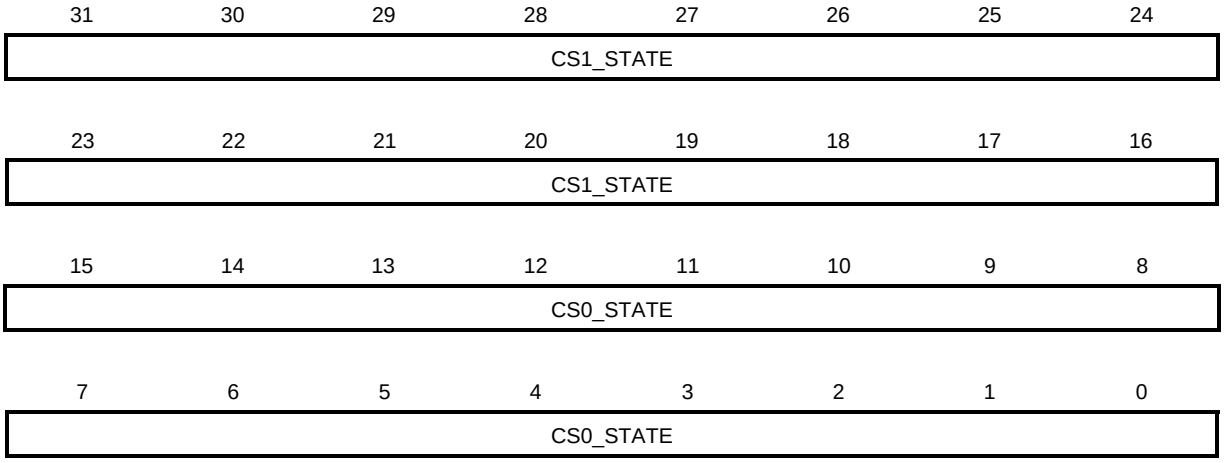


Name	R/W	Bit	After Reset	Function
Reserved	R	31:30	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS0_DELAY_VAL	R	29:24	0H	Stores the result of adjusting the DQS0 delay.
Reserved	R	23:22	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS1_DELAY_VAL	R	21:16	0H	Stores the result of adjusting the DQS1 delay.
Reserved	R	15:14	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS2_DELAY_VAL	R	13:8	0H	Stores the result of adjusting the DQS2 delay.
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS3_DELAY_VAL	R	5:0	0H	Stores the result of adjusting the DQS3 delay.

The optimum delay values obtained by calibration are stored in the DQS0_DELAY_VAL to DQS3_DELAY_VAL bits. When adjustment for automatic calibration is executed, set the MEMCCLK270_SEL bit of the MEMCCLK270_SEL register to 1 in the ASMU.

3.2.22 Memory status check register

This register (MEMC_DDR_STATE8: C00A_202CH) is used to monitor the status of CS0 and CS1.



Name	R/W	Bit	After Reset	Function
CS1_STATE	R	31:16	0H	Indicates the status of the memory connected to CS1. 0x0: Idle 0x1: Extended mode register setting 0x3: Self refresh 0x5: Auto power down 0x6: Self refresh end 0x7: Deep power down 0x8: Bank precharge/all bank precharge 0xA: Read/write 0xC: Forced CBR refresh 0xE: CBR refresh 0xF: Mode register setting
CS0_STATE	R	15:0	0H	Indicates the status of the memory connected to CS0. 0x0: Idle 0x1: Extended mode register setting 0x3: Self refresh 0x5: Auto power down 0x6: Self refresh end 0x7: Deep power down 0x8: Bank precharge/all bank precharge 0xA: Read/write 0xC: Forced CBR refresh 0xE: CBR refresh 0xF: Mode register setting

CHAPTER 4 USAGE

4.1 External Memory Access Control

4.1.1 External Memory Access

DDR SDRAM can be connected as an external memory and can be read and written in 8-burst length. The DDR SDRAM is divided into four banks. Consecutive reading access within a 1-KB consecutive address in the same bank (CAS access) can be performed efficiently. However, access outside the 1-KB consecutive address (RAS access) is less efficient. Accessing a different bank is efficient. The DDR scheduler sorts requests in order to make access efficient.

Table 4-1. Clock Counts Required for 16-Word Access (Burst Length = 8)

Mode	Number of DDR CLK Cycles			
	133 MHz		166 MHz	
	Auto	Non-auto	Auto	Non-auto
Other bank (read ↔ read)	15	15	15	15
Same bank (read ↔ read CAS)	22	15	22	15
Same bank (read ↔ read RAS)	22	22	22	22
Other bank (read ↔ write)	21	21	21	21
Same bank (read ↔ write CAS)	25	21	25	21
Same bank (read ↔ write RAS)	25	25	25	25
Other bank (write ↔ read)	17	17	17	17
Same bank (write ↔ read CAS)	25	17	25	17
Same bank (write ↔ read RAS)	25	25	25	25
Other bank (write ↔ write)	18	18	18	18
Same bank (write ↔ write CAS)	28	18	28	18
Same bank (write ↔ write RAS)	28	28	28	28
Other chip (read ↔ read)	16	16	16	16
Other chip (read ↔ write)	21	21	21	21
Other chip (write ↔ read)	20	20	20	20
Other chip (write ↔ write)	18	18	18	18
Power on	88	88	81	81
Self refresh recovery	16	16	20	20
Auto refresh recovery	15	15	18	18
Deep power down recovery	84	84	77	77

4.1.2 External Memory Access

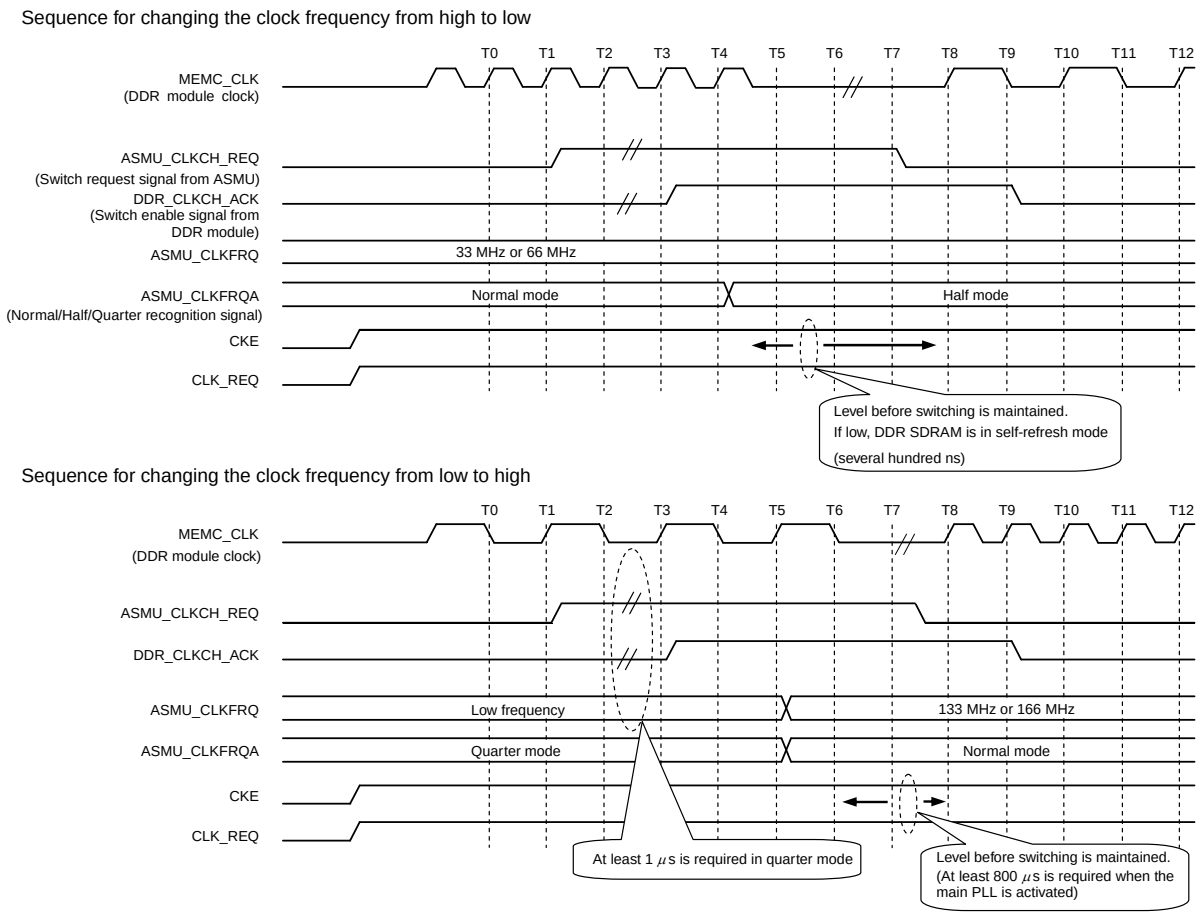
The DDR module is controlled by two clock signals, MEMC_CLK and MEMC_CLK270, which are supplied by the ASMU (system management unit). The frequency of MEMC_CLK is 133 or 166 MHz. MEMC_CLK270 is obtained by shifting the phase of MEMC_CLK by 270°. If there are no read/write requests in the request queue, DDR SDRAM enters the self refresh mode, in which no clock requests are issued. When a read or write request is queued, the MEMC requests the issuance of a clock signal to the ASMU.

In normal mode, the maximum frequency of MEMC_CLK is 166 MHz and 133 MHz. When MEMC_CLK operating frequency is switched, a handshake with the ASMU occurs. Figure 4-1 shows the frequency switch timing. The AC parameters for the timing of exiting a refresh and starting an auto refresh are optimized according to the switched operating frequency.

When the operating clock is switched to the system clock generated by PLL3, the frequency is judged to be low by receiving the MEMC_CLK operating frequency recognition signal sent from the ASMU, and the AC parameters for DDR SDRAM are adjusted to the low frequency mode.

The clock frequency is switched immediately if all chips have entered the self refresh mode when clock frequency switching is requested. (ACK is returned immediately.) When a request is being processed (DDR SDRAM is being accessed), the clock frequency is switched after the requested action is executed. (ACK is returned after execution.) When a CBR refresh request is received, a CBR refresh is executed after the clock frequency is switched. When a clock frequency switch request is received while the MEMC is exiting the self refresh mode, the clock frequency is switched immediately after the self refresh mode is exited.

Figure 4-1. Timing at Which MEMC_CLK Operating Frequency Is Switched



4.1.3 Clock Phase Control

Addresses and commands are issued when MEMC_CLK is shifted by 180°. In read cycles, data is received (latched) based on the DQS signal output from external memory, with delays added. In write cycles, data is output in synchronization with MEMC_CLK270.

Figure 4-2. Clock adjustment mechanism

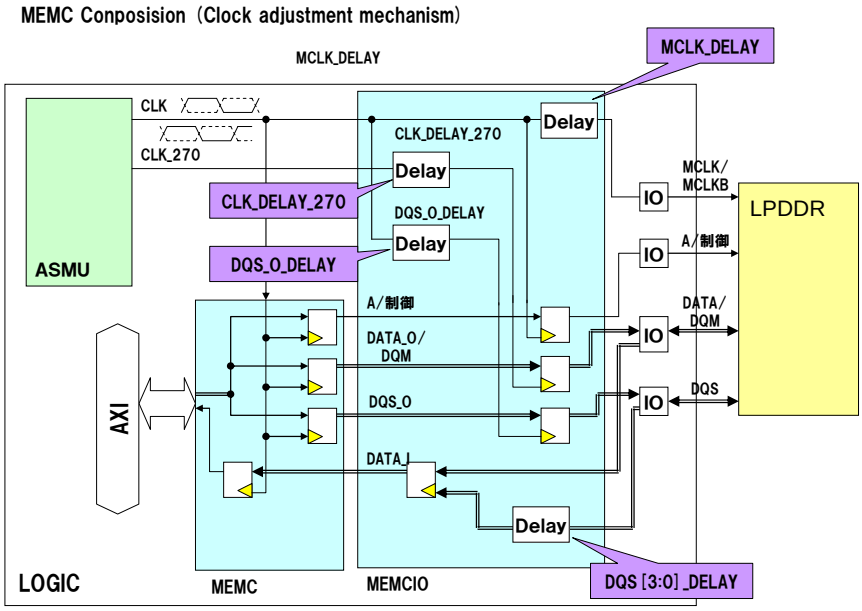


Figure 4-3. Write phase adjustment

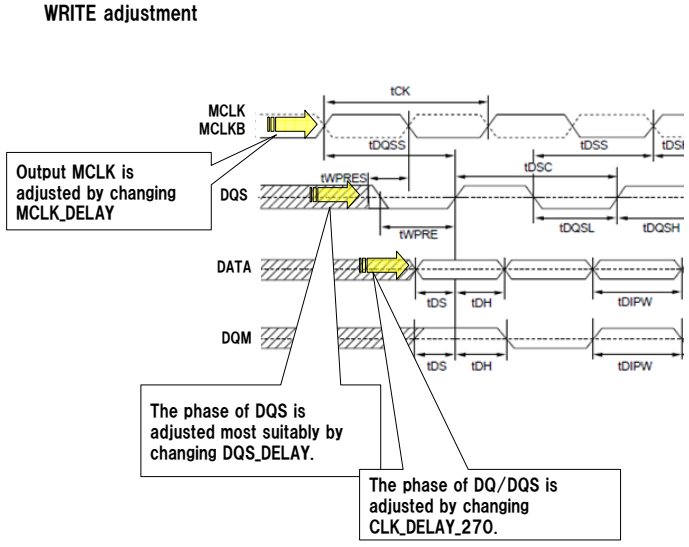
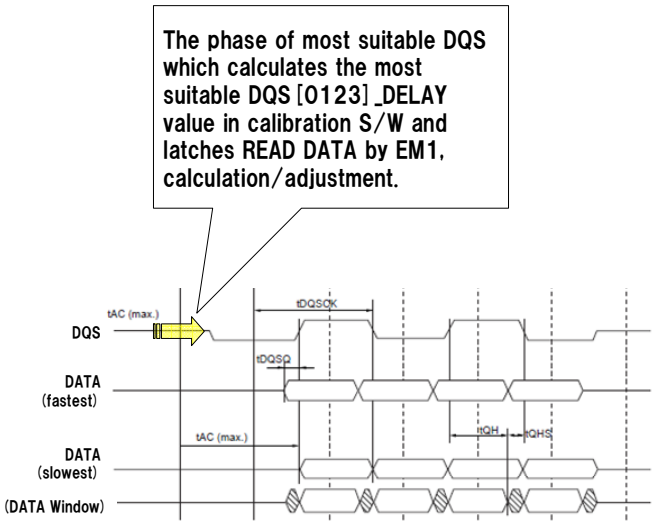


Figure 4-4. Read phase adjustment

READ adjustment



4.1.4 Arbitration

The DDR module arbitrates the following three instructions:

<1> Access instructions from the request queue (independent of read/write)

<2> Self refresh instructions from the IDLE/REF counter, or auto refresh instructions (2 types)

<3> Software command instructions (7 types)

The MEMC outputs the control signals for arbitration according to the priority shown in the following table.

Table 4-2. DDR Module Priority in Processing

<1>	<2>		<3>	
Access	Self/Auto Refresh		Software command	
2	3	Self refresh	1	Initialize
3	2	Auto refresh	1	
1	2	Self refresh	3	Precharge all
2	1	Auto refresh	3	
2	3	Self refresh	1	Auto refresh
3	1	Auto refresh	2	
1	2	Self refresh	3	Self refresh
2	1	Auto refresh	3	
1	2	Self refresh	3	Deep power down
2	1	Auto refresh	3	
2	3	Self refresh	1	Read mode register
3	1	Auto refresh	2	
2	3	Self refresh	1	Write mode register
3	1	Auto refresh	2	

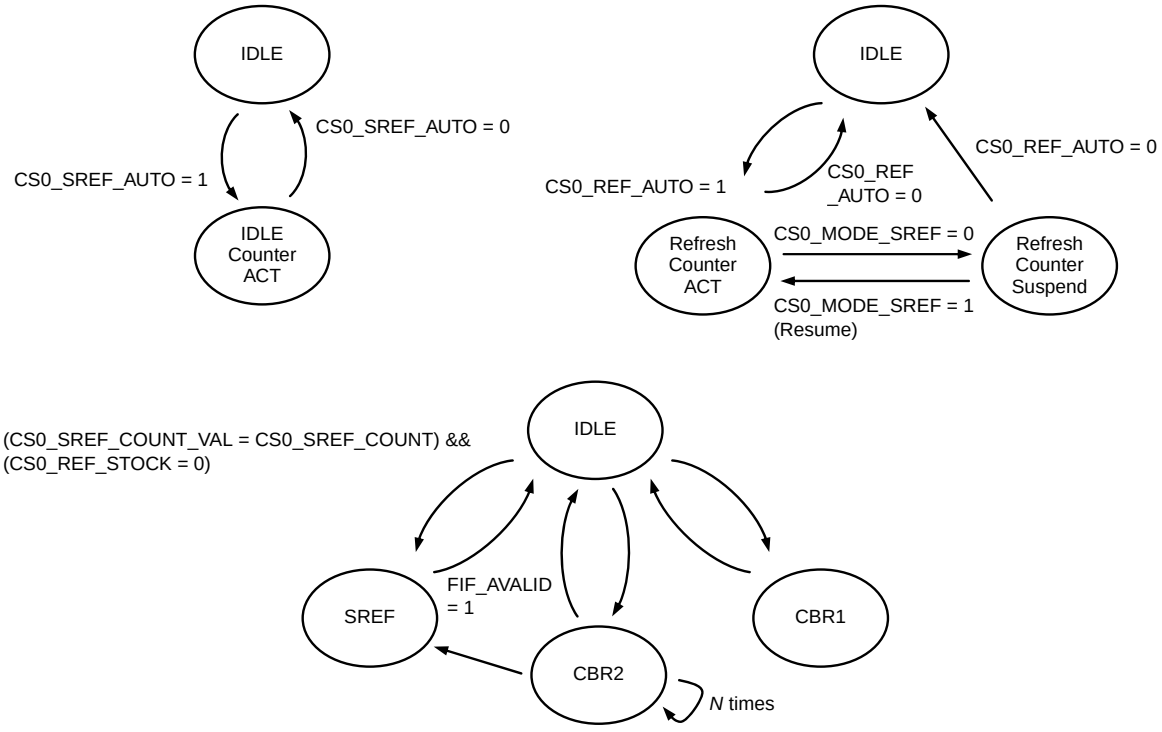
4.1.5 Refresh control

To retain data, the MEMC refreshes DDR SDRAM at a constant interval. The self refresh mode is entered when no read or write request is being received after setting the CS0/1_REF_AUTO bits or CS0/1SREF_AUTO bits of the MEMC_DDR_CONFIGR2 register. In other cases, the number of refreshes that has been executed is counted during each refresh cycle, and CBR refreshes are performed for the relevant number of times at a specific timing. For the catalogue value of DDR SDRAM whose row address is allocated in 16 M-word units, refreshes must be executed at least 8,192 times per 64 ms (once in 7 to 8 μs).

In EM1, the refresh cycle can be specified freely for the CS0/1_REF_COUNT bits of the MEMC_DDR_CONFIGR2 register. When operation enters a refresh cycle, the number of times refreshes still need to be executed is stored in the CS0/1_REF_STOCK bits of the MEMC_DDR_CONFIGR1 register. When this number reaches the specified value (the values of the CS0/1_STOCK_MAX bits of the MEMC_DDR_CONFIGR2 register), acceptance of requests from the request queue is forcibly suspended temporarily and a CBR refresh is executed once at the top priority. While in the self refresh mode, the timer that counts the refresh cycles stops temporarily and resumes when the mode is exited.

If refreshes still need to be executed when the self refresh mode is entered, CBR refreshes are executed multiple times (up to the value specified by the CS0/1_STOCK_DRAIN bits of the MEMC_DDR_CONFIGR2 register) before a self refresh is executed. Figure 4-5 shows the processing from when shifting to CBR refresh execution and after shifting to the self refresh mode. Refresh operation is controlled individually for CS0 and CS1.

Figure 4-5. Refresh Control Status Transitions



4.1.6 Software command control

By using the MEMC_DDR_CONFIGC2 register, DDR SDRAM commands listed in Table 4-2 can be issued and refresh can be controlled.

- When setting a (extended) mode register of DDR SDRAM:
  - Set the address of the command to be issued to DDR SDRAM by using the MEMC_DDR_CONFIGC1 register.
  - Set the CMD_SET bit of the MEMC_DDR_CONFIGC2 register to 1111B (to write the mode register).
  - Set the CMD_ENABLE bit to 0 at the same time; the command is then issued.

- When issuing a precharge command
  - Set the target bank by using the MEMC_DDR_COFIGC1 register. To precharge all banks, set MODEREG_MRS[10] to 1. To precharge selected banks, set MODEREG_MRS[10] to 0 and set the target bank address by using MODEREG_MRS[15:14].
  - Set the CMD_SET bit of the MEMC_DDR_CONFIGC2 register to 1001B (to precharge banks).
  - Set the CMD_ENABLE bit to 0 at the same time; the command is then issued.

- When issuing other commands
  - Setting MEMC_DDR_CONFIG1 is unnecessary.
  - Set the corresponding command by using the CMD_SET bit of the MEMC_DDR_CONFIGC2 register.
  - Set the CMD_ENABLE bit to 0 at the same time; the command is then issued.

Remark Commands are issued after processing of all requests. If the CMD_REQ_LOCK bit has been set when a command is issued, the subsequent requests other than those request for command issuance are held pending until the request lock is released with the CMD_REQ_LOCK bit. Whether a command has been executed can be checked with the CMD_STATE bit. When a software command is executed while the CMD_STATE bit is set to 0 (busy), the command is ignored. When a command to request that the CKE signal be enabled is issued, a clock request is issued at the same time.

Table 4-3. Software Commands

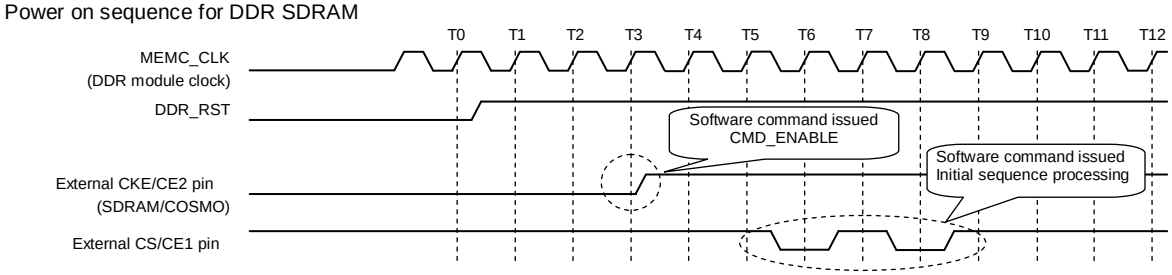
Command	Function	Processing
Initial Seq Auto Exec	Executes initial sequence at power-on.	PALL → CBR → CBR → MRS → EMRS
Precharge	Executes precharge.	A10 = H for PALL, A10 = L and BA[10] = 11B for PRE
Auto refresh	Executes auto refresh.	Issues a CBR command.
Self refresh	Executes self refresh command.	Issues an SREF command.
Deep power down	Executed deep power down.	Issues a DPD command.
Enabling CKE	CKE pin control	Enables controlling the CKE signal by the MEMC.
Disabling CKE	CKE pin control	Disables controlling the CKE signal by the MEMC.
Read mode register	Read from mode register	–
Write mode register	Write to mode register	Issues an MRS/EMRS command.

4.1.7 Power on/off sequence

When the power is initially turned on, the DDR_RST signal is asserted after a clock signal is supplied. (This signal is controlled by the ASMU.) Immediately after a reset, first set up DDR registers such as MEMC_DDR_CONFIGF, MEMC_DDR_CONFIGFA1, and MEMC_DDR_CONFIGA2. Next, individually execute the initialization sequence listed in the table below for CS0 and CS1 by using software commands. The sequence might differ depending on the connected DDR SDRAM. For details, see documents such as the data sheet for the device.

For safety, it is recommended to set the CMD_REQ_LOCK bit of the MEMC_DDR_CONFIGC2 register to 1 to lock any requests other than the command issuance. When issuing the last command, set the CMD_REQ_LOCK bit to 0 to release the locked state.

Figure 4-6. DDR SDRAM Power On Timing



Power down processing is always CS0,1, automatic power down request, the automatic self-refresh and the automatic refreshment request Disable. All Bank Precharge request-> issue confirmation-> CKE Enable issue request-> Issue confirmation-> Deep power down issue (CMD_REQ_LOCK = 1)-> Issue confirmation-> Do by an order of the end..

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0.
June 12, 2009	3.0	Incremental update from comments to the 2.0.
September 30, 2009	4.0	Incremental update from comments to the 3.0.
June 30, 2010	5.0	Incremental update from comments to the 4.0.

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