ISL81802EVAL2Z

Evaluation Board

The ISL81802EVAL2Z dual-output evaluation board (shown in Figure 4) features the ISL81802, an 80V high voltage dual synchronous buck controller that offers external soft-start, independent enable functions, and integrates UV/OV/OC/OT protection. A programmable switching frequency ranging from 100kHz to 1MHz helps to optimize inductor size while the strong gate driver delivers up to 10A for each output.

Key Features

- Wide input range: 18V to 80V for 12V output, 6V to 80V for 5V output
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/PWM operation
- Optional CC/HICCUP OCP protection
- Supports pre-bias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection
- Back biased from output to improve efficiency

Specifications

The ISL81802EVAL2Z dual-output evaluation board is designed for high current applications. The current rating of the ISL81802EVAL2Z is limited by the FETs and inductor selected. The ISL81802EVAL2Z electrical ratings are shown in Table 1.

Table 1. ISL81802EVAL2Z Electrical Ratings

Parameter	Rating
Input Voltage	18V to 80V (6V to 80V for 5V output)
Switching Frequency	200kHz
Output Voltage 1	12V
Output Current 1	10A
Output Voltage 2	5V
Output Current 2	10A
OCP Set Point	Minimum 12.6A each output at ambient room temperature

Ordering Information

Part Number	Description
ISL81802EVAL2Z	High Voltage Dual Buck Controller Evaluation Board

Related Literature

For a full list of related documents, visit our website:

- ISL81802 device page

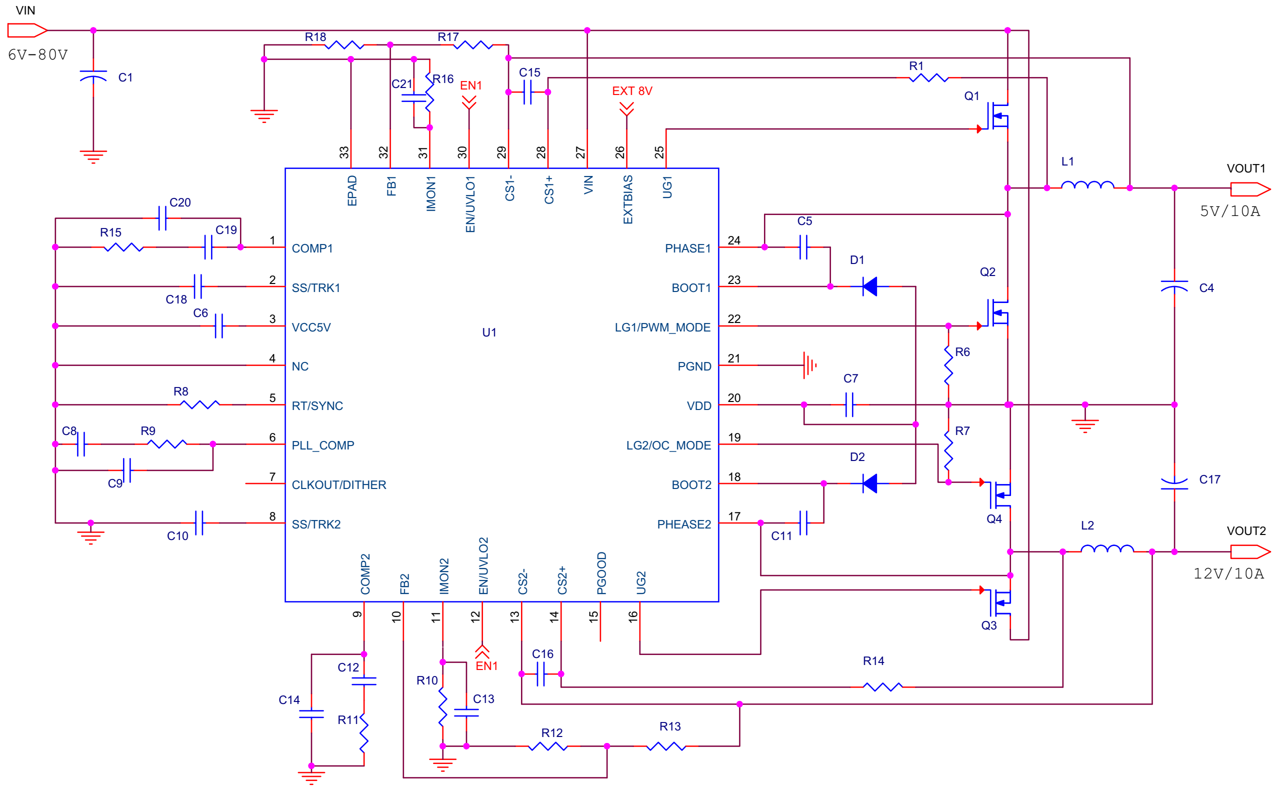

Figure 1. ISL81802EVAL2Z Block Diagram

1. Functional Description

The ISL81802EVAL2Z is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81802 TQFN IC. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in Figure 3, the 6V to 80V V_{IN} is supplied to J1 (+) and J2 (-). The regulated 12V output is on J4 (+) and J5 (-), while the regulated 5V output is on J17 (+) and J16 (-). They both can supply up to 10A to the load. Due to the high power efficiency, the evaluation board can run at 20A in total continuously without airflow at ambient room temperature conditions.

Test points TP1 through TP25 provide easy access to the IC pin and external signal injection terminals.

As shown in Table 2, connector J6 provides a selection of either Forced PWM mode (shorting Pin 1 and Pin 2) or DEM mode (shorting Pin 2 and Pin 3). Connector J7 provides a selection of either constant current limit (shorting Pin 1 and Pin 2) or HICCUP OCP (shorting Pin 2 and Pin 3). Connector J3 provides an option to disable the converter by shorting its Pin 1 and Pin 2.

1.1 Recommended Testing Equipment

The following materials are recommended for testing:

- 0V to 80V power supply with at least 30A source current capability
- Electronic loads capable of sinking current up to 30A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

1.2 Operating Range

The input voltage range is from 18V to 80V for the 12V output, while the input voltage range is from 6V to 80V for the 5V output. If the output voltage is set to a lower value, the minimum V_{IN} can be reset to a lower value by changing the ratio of R_1 and R_5. The minimum EN threshold that V_{IN} can be set to is 4.5V.

The rated load current for each output is 10A with the OCP point set at a minimum 12A at ambient room temperature conditions. The operating temperature range of this board is -40°C to +85°C.

Note: Airflow is needed for higher ambient temperature conditions.

1.3 Quick Test Guide

1. Jumper J6 provides the option to select PWM or DEM. Jumper J7 provides the option to select a constant current limit or HICCUP. See Table 2 for the operating options. Ensure that the circuit is correctly connected to the supply and electronic loads before applying any power. See Figure 3 for the proper setup.
2. Turn on the power supply.
3. Adjust the input voltage (V_{IN}) within the specified range and observe the output voltage. The output voltage variation should be within 3%.
4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see Figure 2 for the proper test setup.

Table 2. Operating Options

Jumper	Position	Function
3	EN-GND	Disable output
	EN Floating	Enable output
6	Pin 1-2	PWM
	Pin 2-3	DEM
7	Pin 1-2	Constant current limit
	Pin 2-3	HICCUP

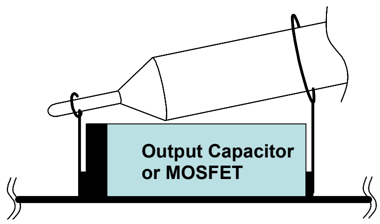

Figure 2. Proper Probe Setup to Measure Output Ripple and Phase Node Ringing

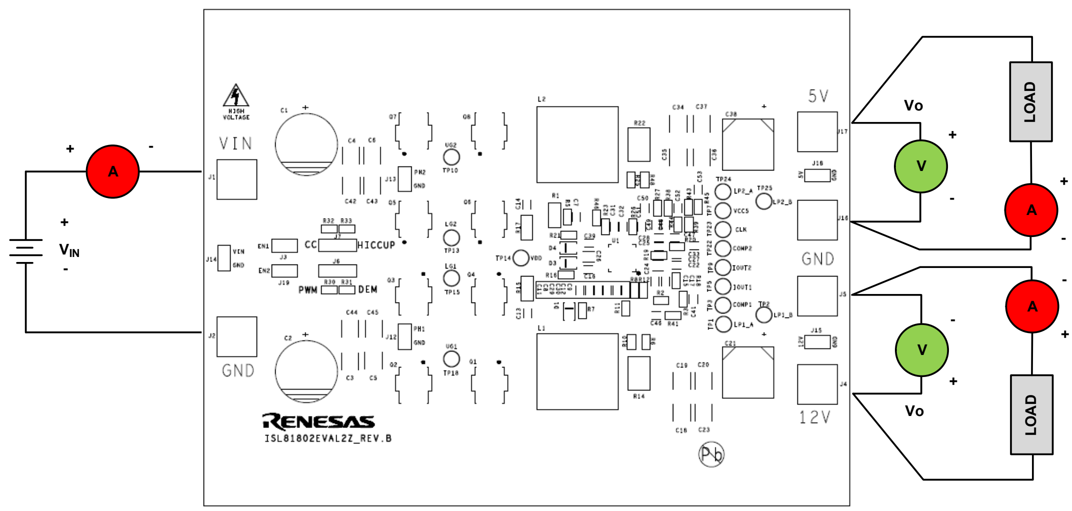

Figure 3. Proper Test Setup

2. PCB Layout Guidelines

Careful attention to Printed Circuit Board (PCB) layout requirements is necessary for the successful implementation of an ISL81802 based DC/DC converter. The ISL81802 switches at a high frequency; therefore, the switching times are short. At these switching frequencies, even the shortest trace has significant impedance and the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes.

Three sets of components are critical when using the ISL81802 DC/DC converter:

- Controller
- Switching power components
- Small-signal components

The switching power components are the most critical to the layout because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small-signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

Complete the following steps to optimize the PCB layout:

1. Place the input capacitors, FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high-frequency decoupling ceramic capacitors very close to the MOSFETs.
2. If signal components and the IC are placed separately from the power train, Renesas recommends using full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small signal ground. Connect the SGND and PGND together close to the IC. **Note: DO NOT** connect them together anywhere else.
3. Keep the loop formed by the input capacitor, the top FET, and the bottom FET as small as possible.
4. Ensure the current paths from the input capacitor to the FETs, the power inductor, and the output capacitor are as short as possible with maximum allowable trace widths.
5. Place the PWM controller IC close to the lower FETs. The low-side FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
6. Place the VDD bypass capacitor very close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane by a via.
Note: DO NOT connect the PGND pin directly to the SGND EPAD.
7. Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
8. Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to load to avoid inductance and resistances.
9. Use copper filled polygons or wide, short traces to connect the junction of the upper FET, lower FET, and output inductor. Keep the PHASE nodes connection to the IC short. **Note: DO NOT** unnecessarily oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
10. Route all high-speed switching nodes away from the control circuitry.
11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
12. Use a pair of traces with minimum loop for the input or output current sensing connection.
13. Ensure the feedback connection to the output capacitor is short and direct.

2.1 ISL81802EVAL2Z Evaluation Board

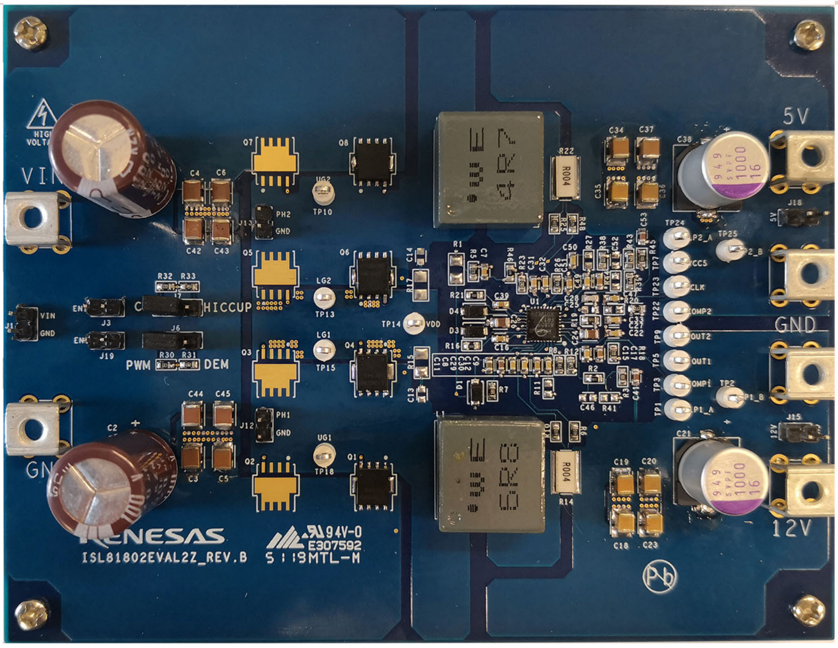

Figure 4. ISL81802EVAL2Z Evaluation Board, Top View

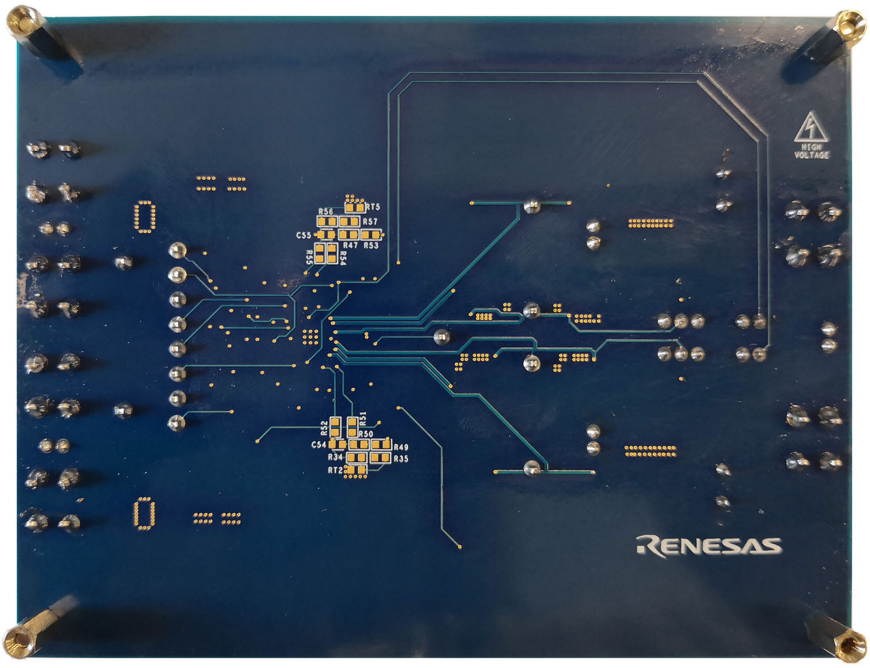

Figure 5. ISL81802EVAL2Z Evaluation Board, Bottom View

2.2 ISL81802EVAL2Z Circuit Schematic

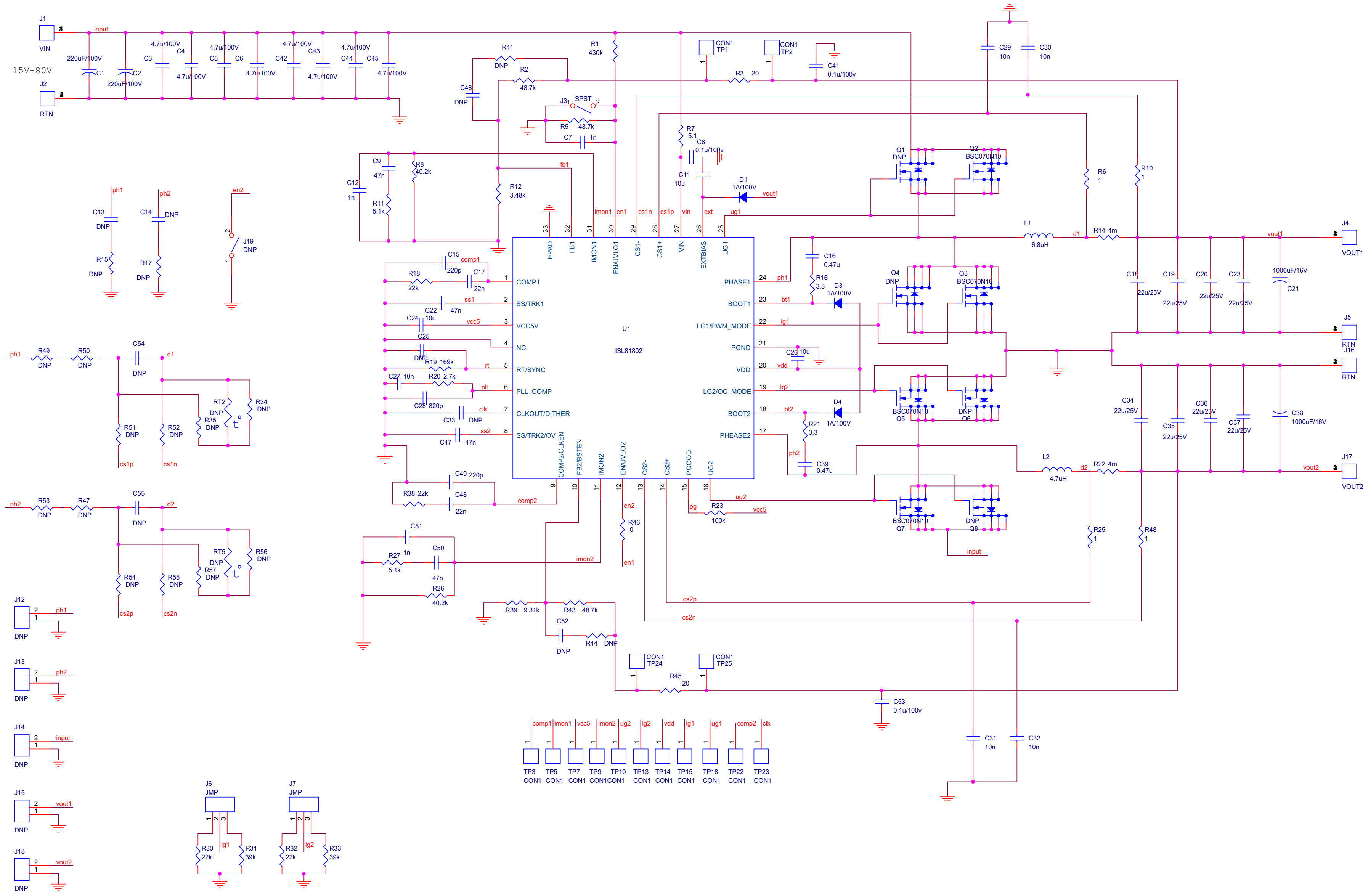

Figure 6. Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL81802EVAL1Z, REVB, ROHS	Multilayer PCB Technology	ISL81802EVAL1ZREVBPCB
2	C1, C2	CAP, RADIAL, 12.5x26.5, 220µF, 100V, 20%, ALUM.ELEC., 5mm, ROHS	United Chemi-Con	EKZN101ELL221MK25S
8	C3, C4, C5, C6, C42, C43, C44, C45	CAP-AEC-Q200, SMD, 1210, 4.7µF, 100V, 10%, X7S, ROHS	TDK	CGA6M3X7S2A475K200AB
3	C7, C12, C51	CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS	TDK	C1608X7R1H102K080AE
3	C8, C41, C53	CAP, SMD, 0603, 0.1µF, 100V, 10%, X7R, ROHS	Vishay	GRJ188R72A104KE11D
4	C9, C22, C47, C50	CAP, SMD, 0603, 0.047µF, 25V, 10%, X7R, ROHS	TDK	CGJ3E2X7R1E473K080AA
1	C11	CAP, SMD, 0603, 10µF, 16V, X5R, 10%, ROHS	Murata	GRM188R61C106KAALJ
2	C15, C49	CAP, SMD, 0603, 220pF, 50V, 10%, X7R, ROHS	Murata	GRM188R71H221KA01D
2	C16, C39	CAP, SMD, 0603, 0.47µF, 25V, 10%, X7R, ROHS	Murata	GRM188R71E474KA12D
2	C17, C48	CAP, SMD, 0603, 0.022µF, 25V, X7R, ROHS	TDK	CGJ3E2X7R1E223K080AA
8	C18, C19, C20, C23, C34, C35, C36, C37	CAP, SMD, 1210, 22µF, 25V, X7R, ROHS	Murata	GRM32ER71E226KE15L
2	C21, C38	CAP-OSCON, SMD, 10mm, 1000µF, 16V, 20%, 12mΩ, ROHS	Panasonic	16SVPF1000M
2	C24, C26	CAP, SMD, 0805, 10µF, 16V, 10%, X7S, ROHS	Murata	GRM21BC71C106KE11L
5	C27, C29, C30, C31, C32	CAP, SMD, 0603, 0.01µF, 100V, 5%, X7R, ROHS	Kemet	C0603C103J1RACTU
1	C28	CAP, SMD, 0603, 820pF, 50V, 10%, X7R, ROHS	Kemet	C0603C821K5RACTU
0	C13, C14, C25, C33, C46, C52, C54, C55	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
3	D1, D3, D4	DIODE-RECTIFIER, SMD, 2P, S0D-123FL, 100V, 1A, ROHS	ON Semiconductor	MBR1H100SFT3G
6	J1, J2, J4, J5, J6, J17	HDWARE, TERMINAL, M4 METRIC SCREW, TH, 4P, SNAP-FIT, ROHS	Keystone	7795
1	J3	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
2	J6, J7	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
0	J12, J13, J14, J15, J18, J19	2.54mm Headers, DNP-PLACE HOLDER, ROHS		
1	L1	COIL-PWR INDUCTOR, SMD, 6.8µH, 20%, 15A, 4.1mΩ, ROHS	Wurth	74439370068
1	L2	COIL-PWR INDUCTOR, SMD, 4.7µH, 20%, 17A, 3.5mΩ, ROHS	Wurth	74439370047
1	U1	80V DUAL-BUCK PWM CONTROLLER, 32P, TQFN, 5x5, ROHS	Renesas Electronics America	ISL81802FRTZ
4	Q2, Q3, Q5, Q7	TRANSISTOR-MOS, N-CHANNEL, SMD, 8P, PPK SO-8, 100V, 80A, ROHS	Infineon	BSC070N10NS5ATMA1
0	Q1, Q4, Q6, Q8	DO NOT POPULATE OR PURCHASE		

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R1	RES SMD 430kΩ 1% 1/4W 1206	Panasonic	ERJ-8ENF4303V
3	R2, R5, R43	RES SMD 48.7kΩ 1% 1/10W 0603	Yageo	RC0603FR-0748K7L
2	R3, R45	RES SMD 20Ω 1% 1/10W 0603	Yageo	RC0603FR-0720RL
4	R6, R10, R25, R48	RES SMD 1Ω 1% 1/10W 0603	Panasonic	ERJ-3RQF1R0V
1	R7	RES SMD 5.1Ω 1% 1/10W 0603	Yageo	RC0603FR-075R1L
2	R8, R26	RES SMD 40.2kΩ 1% 1/10W 0603	Yageo	RC0603FR-0740K2L
2	R11, R27	RES SMD 5.1kΩ 1% 1/10W 0603	Yageo	RC0603FR-075K1L
1	R12	RES SMD 3.48kΩ 1% 1/10W 0603	Yageo	RC0603FR-073K48L
2	R14, R22	RES SMD 0.004Ω 3W 2512 WIDE	Susumu	KRL6432E-M-R004-F-T1
1	R46	RES SMD 0Ω 1% 1/10W 0603	Yageo	RC0603JR-070RL
2	R16, R21	RES SMD 3.3Ω 1% 1/10W 0603	Yageo	RC0603FR-073R3L
4	R18, R30, R32, R38	RES SMD 22kΩ 1% 1/10W 0603	Yageo	RC0603FR-0722KL
1	R19	RES SMD 169kΩ 1% 1/10W 0603	Venkel	CR0603-10W-1693FT
1	R20	RES SMD 2.7kΩ 1% 1/10W 0603	Yageo	RC0603FR-072K7L
1	R23	RES SMD 100kΩ 1% 1/10W 0603	Yageo	RC0603FR-07100KL
2	R31, R33	RES SMD 39kΩ 1% 1/10W 0603	Yageo	RC0603FR-0739KL
1	R39	RES SMD 9.31kΩ 1% 1/10W 0603	Yageo	RC0603FR-079K31L
0	RT2, RT5, R15, R17, R34, R35, R41, R44, R47, R49, R50, R51, R52, R53, R54, R55, R56, R57	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
15	TP1, TP2, TP3, TP5, TP7, TP9, TP10, TP13, TP14, TP15, TP18, TP22, TP23, TP24, TP25	CONN-COMPACT TEST PT, VERTICAL, WHT, ROHS	Keystone	5007
3	J3, J6, J7	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	Sullins	SPC02SYAN
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Keystone	2204
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	7795

2.4 Board Layout

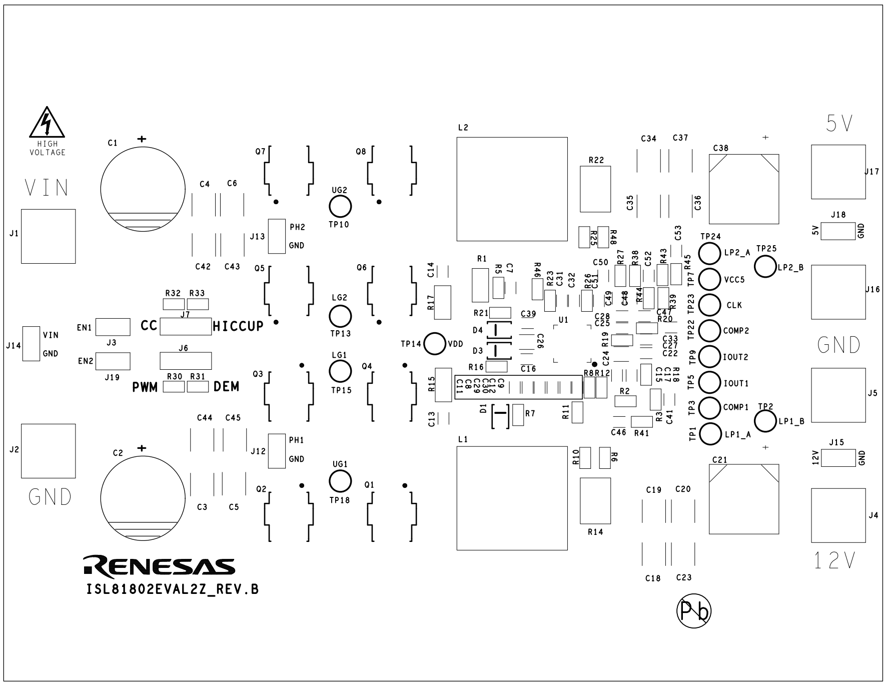

Figure 7. Silkscreen Top

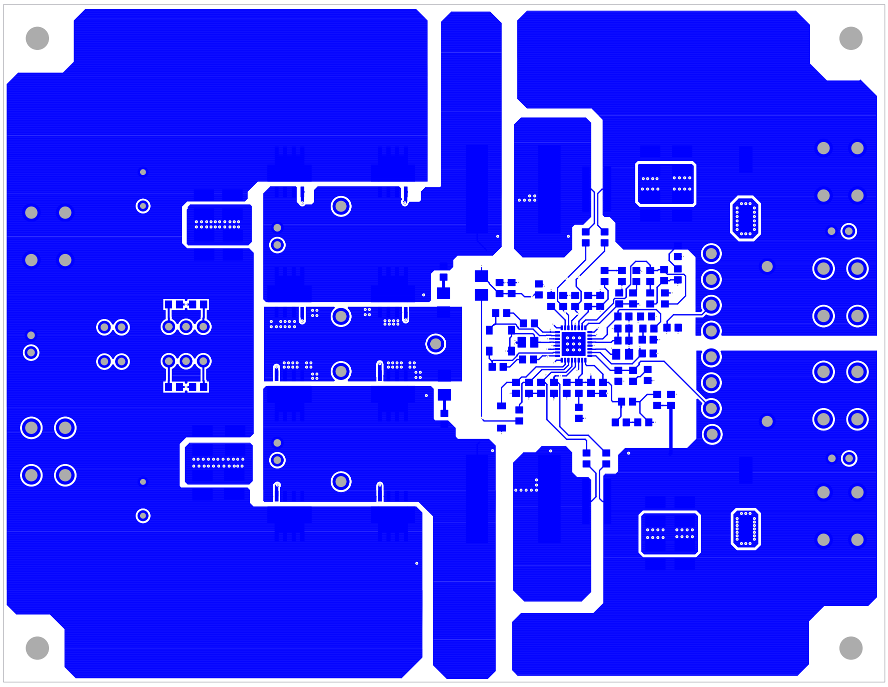

Figure 8. Top Layer

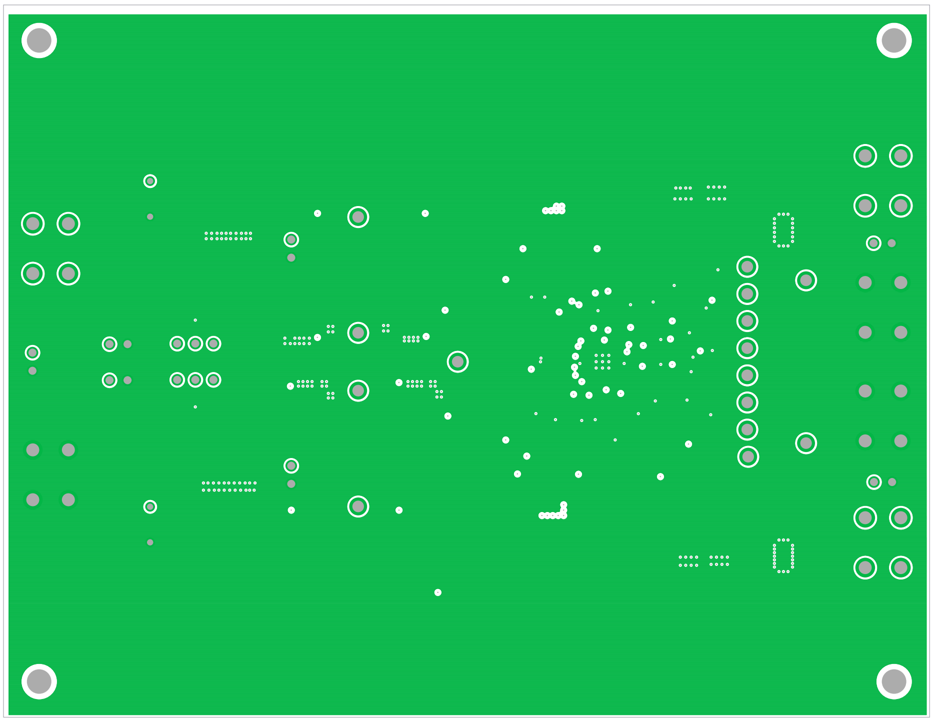

Figure 9. Second Layer (Solid Ground)

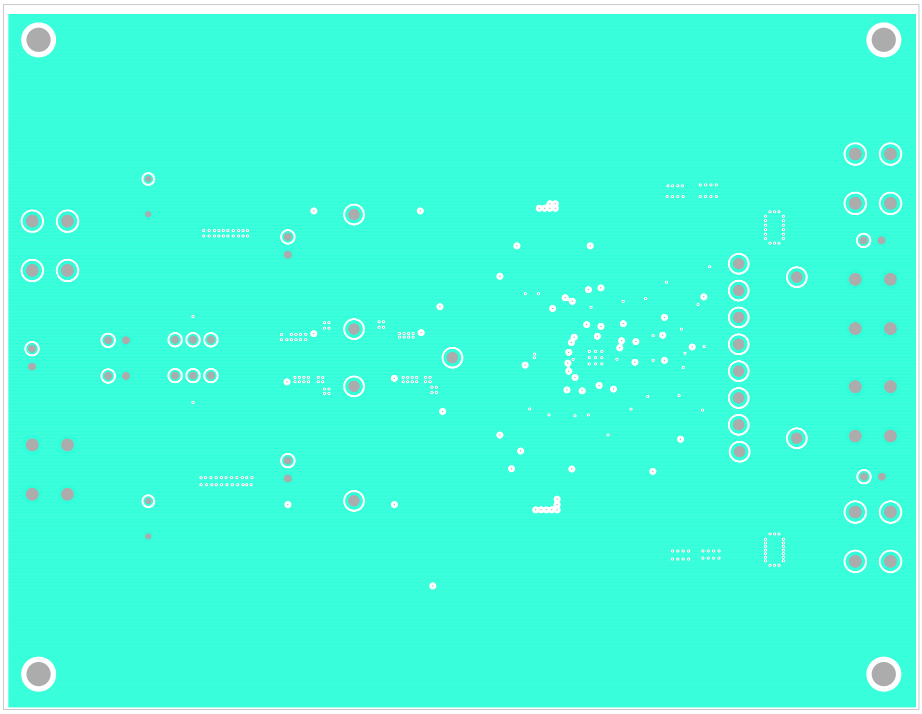

Figure 10. Third Layer

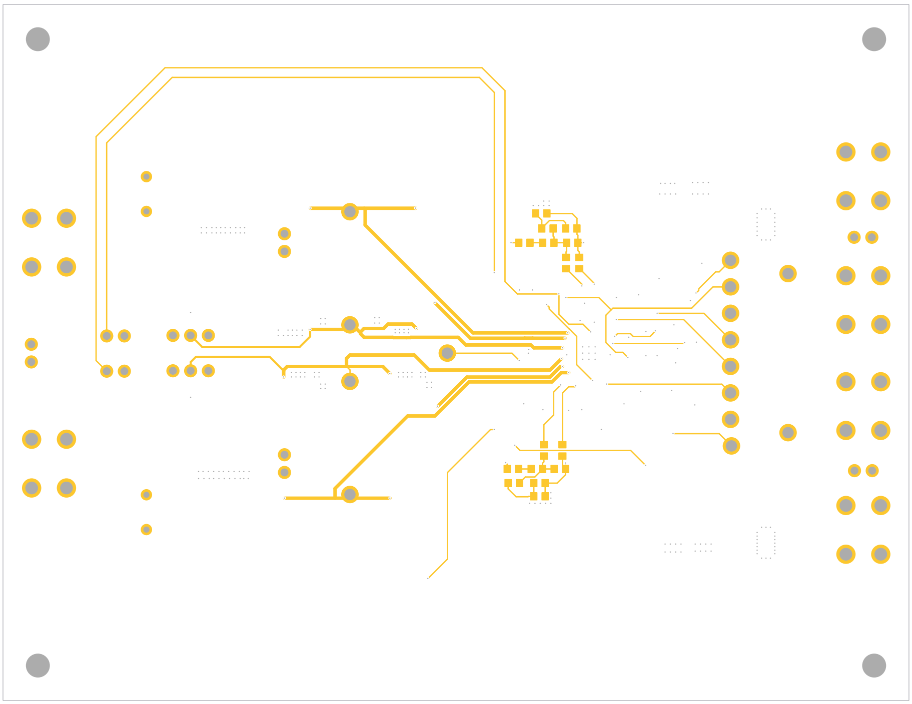

Figure 11. Bottom Layer

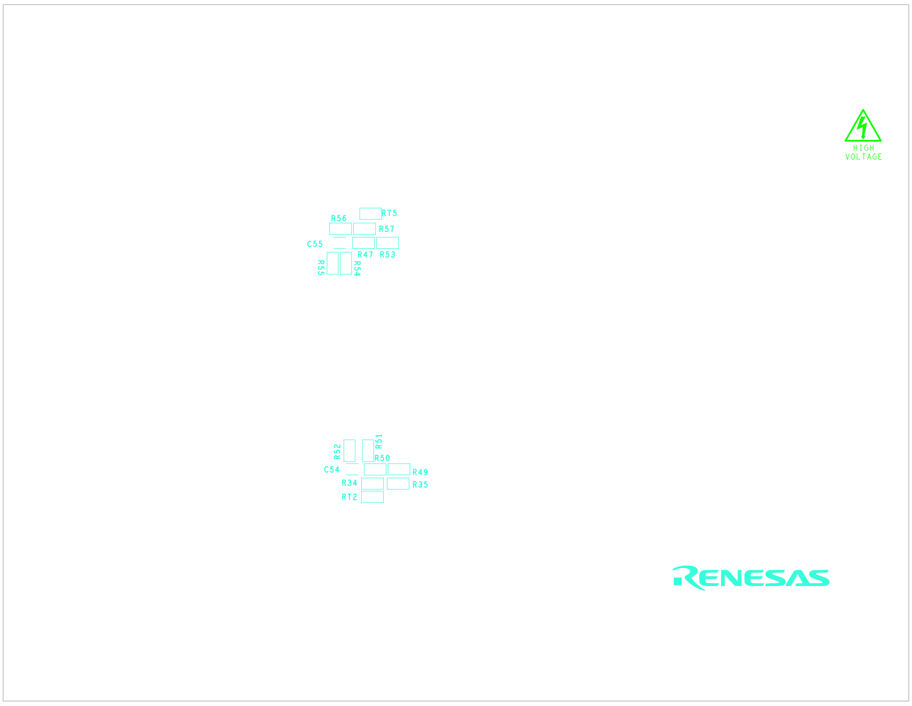

Figure 12. Silkscreen Bottom

3. Design Example

3.1 Design Requirements

Parameter	Rating
Input Voltage	18V to 80V for 12V output 6V to 80V for 5V output
Switching Frequency	200kHz
Output Voltage 1	12V
Output Current 1	10A
Output Voltage 2	5V
Output Current 2	10A
OCP Set Point	12.6A for each output
Output Mode	Dual output
PWM Mode	Forced PWM
OCP Mode	Constant current

3.2 Frequency Setting

The default switching frequency of the PWM controller is determined by the resistor R_T (R_{19}). It adjusts the default switching frequency from 100kHz to 1MHz. The R_T value for f_{SW} = 200kHz is calculated using Equation 1.

(EQ. 1) $$R_T = \left(\frac{34.7}{f_{SW}} - 4.78\right) = \frac{34.7}{0.2} - 4.78 = 168.72k\Omega$$

where f_{SW} is the switching frequency in MHz. Select a standard value resistor R_T = 169kΩ.

3.3 Output Voltage Setting

The output voltage can be set from 0.8V up to a level determined by the feedback voltage divider. A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB_OUT pin.

With V_{OUT1} = 12V, R_{FBO1} (R_2) = 487k, the R_{FBO2} (R_{12}) value is calculated using Equation 2.

(EQ. 2) $$R_{FBO2(12V)} = \frac{0.8V \times R_{FBO1}}{V_{OUT1} - 0.8V} = \frac{0.8V \times 487k\Omega}{12V - 0.8V} = 34.78k\Omega$$

Select a standard value resistor R_{FBO2} = 34.8kΩ.

With V_{OUT2} = 5V, R_{FBO1} (R_{43}) = 487k, the R_{FBO2} (R_{39}) value is calculated using Equation 3.

(EQ. 3) $$R_{FBO2(5V)} = \frac{0.8V \times R_{FBO1}}{V_{OUT2} - 0.8V} = \frac{0.8V \times 487k\Omega}{5V - 0.8V} = 92.8k\Omega$$

Select a standard value resistor R_{FBO2} = 93kΩ.

R_{FBO1} is the top resistor of the feedback divider network and R_{FBO2} is the bottom resistor connected from FB_OUT to ground. To avoid an unstable state during hiccup, the value of R_{FBO1} and R_{FBO2} in parallel should be no less than 30k.

3.4 UVLO Setting

The ISL81802 has input UVLO protection. When the voltage on the EN/UVLO pin reaches 1.8V, the PWM modulator is enabled. Accurate UVLO feature can be implemented by feeding the V_{IN} into the EN/UVLO pin using a voltage divider, R_{UV1} (R_1) and R_{UV2} (R_5). The V_{IN} UVP rising threshold is calculated using Equation 4.

(EQ. 4)
$$V_{UVRISE} = \frac{V_{UVLO\_THR}(R_{UV1}+R_{UV2}) - I_{LEAK}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(430k\Omega + 48.7k\Omega) - 1.4\mu A(430k\Omega)(48.7k\Omega)}{48.7k\Omega} = 17.09V$$

The V_{IN} UVP falling threshold is calculated using Equation 5.

(EQ. 5)
$$V_{UVFALL} = \frac{V_{UVLO\_THR}(R_{UV1}+R_{UV2}) - I_{UVLO\_HYST}R_{UV1}R_{UV2}}{R_{UV2}}$$
$$= \frac{1.8V(430k\Omega + 48.7k\Omega) - 3.4\mu A(430k\Omega)(48.7k\Omega)}{48.7k\Omega} = 16.23V$$

where V_{UVLO_THR} is the 1.8V UVLO rising threshold and I_{UVLO_HYST} is the 3.4µA UVLO hysteresis current.

3.5 Soft-Start Capacitor

The soft-start time for dual output is set by the value of the soft-start capacitor C_{SS1} (C22) connected from SS/TRK1 to GND and C_{SS2} (C47) connected from SS/TRK2 to GND separately. The soft-start time with $C_{SS1} = C_{SS2} = 47nF$ is calculated using Equation 6.

(EQ. 6)
$$t_{SS} = 0.8V\left(\frac{C_{SS}}{2\mu A}\right) = 0.8V \times \left(\frac{47nF}{2\mu A}\right) = 18.8ms$$

When the soft-start time set by external C_{SS} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

3.6 MOSFET Considerations

The MOSFETs are selected based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations. The maximum operation voltage of the MOSFETs in Buck mode is decided by the maximum V_{IN} voltage.

The power loss of the upper and lower MOSFETs for the 12V output are calculated using Equation 7 and Equation 8. The equations assume linear voltage current transitions and do not model power loss due to the reverse recovery for the body diode of the lower MOSFET.

(EQ. 7)
$$P_{UPPERMAX} = \frac{(I_{OUT}{}^2)(r_{DS(ON)})(V_{OUT})}{V_{INMAX}} + \frac{(I_{OUT})(V_{INMAX})(t_{SW})(f_{SW})}{2}$$
$$= \frac{(10A^2)(6m\Omega)(12V)}{80V} + \frac{(10A)(80V)\left(\frac{6nC}{\left(\frac{8V-4.9V}{3.3\Omega}\right)} + \frac{6nC}{\left(\frac{4.9V}{3.3\Omega}\right)}\right)(200kHz)}{2} = 0.09W + 0.834W = 0.843W$$

(EQ. 8)
$$P_{LOWERMAX} = \frac{(I_{OUT}{}^2)(r_{DS(ON)})(V_{INMAX} - V_{OUT})}{V_{INMAX}}$$
$$= \frac{(10A)^2(6m\Omega)(80V - 12V)}{80V} = 0.51W$$

Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

3.7 Inductor Selection

The inductor value determines the ripple current of the converter. The ripple voltage is a function of the ripple current and the output capacitor(s) ESR. Assume the ripple current ratio is 80% of the inductor average current at the maximum input voltage and the full output load condition. The inductor value for the 12V output is calculated using Equation 9.

(EQ. 9) $$L_{INMIN} = \frac{(V_{INMAX} - V_{OUT})(V_{OUT})}{(f_{SW})(0.8 \times I_{OUTMAX})(V_{INMAX})} = \frac{(80V - 12V)(12V)}{(200kHz)(0.8 \times 10A)(80V)} = 6.375\mu H$$

The recommended inductor value is 6.8µH. Then the ripple current and peak current are calculated using Equation 10, Equation 11, and Equation 12.

(EQ. 10) $$\Delta I_{LMAX} = \frac{(V_{INMAX} - V_{OUT})(V_{OUT})}{(f_{SW})(L)(V_{INMAX})} = \frac{(80V - 12V)(12V)}{(200kHz)(6.8\mu H)(80V)} = 7.5A$$

(EQ. 11) $$I_{LRMS} = \sqrt{(I_{OUTMAX})^2 + \frac{(\Delta I_{LMAX})^2}{12}} = \sqrt{(10A)^2 + \frac{(7.5A)^2}{12}} = 10.23A$$

(EQ. 12) $$I_{LPEAKMAX} = I_{OUTOCP} + \frac{\Delta I_{LMAX}}{2} = 12.6A + \frac{7.5A}{2} = 16.35A$$

The saturation current of the inductor should be larger than 16.35A. The heat rating current of the inductor should be larger than 10.23A.

The maximum DC power dissipation in the inductor is calculated using Equation 13.

(EQ. 13) $$P_{LMAX} = (I_{OUT})^2(DCR) = (10A)^2 \times (4.1m\Omega) = 0.41W$$

3.8 Output Capacitor Selection

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor for the 12V output is shown in Equation 14.

(EQ. 14) $$C_{OUTMIN} = \frac{L(I_{TRAN})^2}{2(V_{INMIN} - V_{OUT})(\Delta V_{OUT})} = \frac{6.8\mu F \times (10A - 0A)^2}{2(18V - 12V)\left(12V \times \frac{1.5}{100}\right)} = 314.8\mu F$$

where C_{OUTMIN} is the minimum output capacitor(s) required, I_{TRAN} is the transient load current step, and ΔV_{OUT} is the drop in output voltage allowed during the load transient. Choose a capacitor no less than 314.8µF for each phase. 1000µF electrolytic capacitor and 88µF MLCC in total are used for each output on this board.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by Equation 15.

(EQ. 15) $$V_{RIPPLE} = \Delta I_{LMAX} \times ESR = 7.5A \times 5m\Omega = 37.5mV$$

3.9 Input Capacitor Selection

The important parameters for the input capacitors are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC RMS input current varies with the load given in Equation 16.

(EQ. 16) $$I_{RMS} = \sqrt{D - D^2} \times I_{OUT}$$

The maximum RMS current supplied by the input capacitance occurs at $V_{IN} = 2V_{OUT}$, D = 50% as shown in Equation 17.

(EQ. 17) $$I_{RMSMAX} = \frac{1}{2} \times I_{OUTMAX} = \frac{1}{2} \times 10A = 5A$$

Renesas recommends using a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Two 220µF electrolytic capacitors with 2.2A rating current and eight 4.7µF ceramic capacitors are used to share the 5A RMS input current on this board.

3.10 First Level Peak Current Limit and Sense Resistor Selection

The inductor peak current for 12V output is sensed by the shunt resistor R_S (R_{14}). When the voltage drop on R_S reaches the set point $V_{OCSET\text{-}CS}$ typical 85mV, it triggers the pulse-by-pulse peak current limit. With current limit set point $I_{OCPP1} = 2xI_{OUTMAX}$ = 20A, the value of the sense resistor is calculated using Equation 18.

(EQ. 18) $$R_S = \frac{V_{OCSET-CS}}{I_{OCPP1}} = \frac{85mV}{20A} = 4.25m\Omega$$

Select a standard value resistor R_S = 4mΩ. Then the actual peak current limit is calculated using Equation 19.

(EQ. 19) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_S} = \frac{85mV}{4m\Omega} = 21.25A$$

The maximum power dissipation in R_S is calculated using Equation 20.

(EQ. 20) $$P_{RSMAX} = (I_{OUT})^2 R_S = (10A)^2(4m\Omega) = 0.4W$$

Therefore, a sense resistor with 1W power rating is sufficient for this application.

3.11 Second Level Hiccup Peak Current Protection

In the output dead short condition especially at high V_{IN}, the inductor current runs away with the minimum on PWM duty. The ISL81802 integrates a second level hiccup type of peak current protection. The second level peak current protection set point I_{OCPP2} is calculated using Equation 21.

(EQ. 21) $$I_{OCPP2} = \frac{V_{OCSET\text{-}CS\text{-}HIC}}{R_S} = \frac{115mV}{4m\Omega} = 28.75A$$

3.12 Output Average Overcurrent Protection and R_{IM} Selection

The ISL81802 provides either constant current or hiccup type of overcurrent protection for output average current. The OCP mode is set by a resistor connected between the LG2/OC_MODE pin and ground. With the output constant current/hiccup set point I_{OUTOCP} = 12.6A for each output, the current monitoring resistor R_{IM} (R_8) is calculated using Equation 22.

(EQ. 22) $$R_{IM} = \frac{1.2}{I_{OUTOCP} \times R_S \times Gm_{CS} + I_{CSOFFSET}} = \frac{1.2V}{12.6A x 4m\Omega x 195\mu S + 20\mu A} = 40.23k\Omega$$

Select a standard value resistor R_{IM} = 40.2kΩ.

3.13 PWM Mode Selection

You can set the ISL81802 to either forced PWM mode or DE mode. The mode is set by a resistor $R_{PWMMODE}$ (R_{30} or R_{31}) connected between the LG1/PWM_MODE pin and GND. The critical resistor value for $R_{PWMMODE}$ is calculated using Equation 23.

(EQ. 23) $$R_{PWMMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to forced PWM mode, while a resistor higher than 30kΩ sets the converter to DE mode. Considering the tolerance in all temperature ranges, Renesas recommends using 15kΩ to set to Forced PWM node and 51kΩ to set to DE mode.

3.14 Overcurrent Protection Mode Selection

The ISL81802 is set to either a constant current or hiccup type of overcurrent protection for output average current by selecting a different value of the resistor R_{OCMODE} (R_{32} or R_{33}) connected between LG2/OC_MODE and GND. The critical resistor value for R_{OCMODE} is calculated using Equation 24.

(EQ. 24) $$R_{OCMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to Constant Current mode, while a resistor higher than 30kΩ sets the converter to Hiccup mode. Considering the tolerance in all temperature ranges, Renesas recommends using 21kΩ to set to constant current and 39kΩ to set to hiccup mode.

3.15 Phase Lock Loop (PLL)

The PLL of the ISL81802 ensures the wide range of accurate clock frequency and phase setting. It also makes the internal clock easily synchronized to an external clock with the frequency either lower or higher than the internal setting. The external compensation network of R_{PLL} (R20), C_{PLL1} (C27), and C_{PLL2} (C28) is needed to connect to the PLL_COMP pin to ensure PLL stable operation. Renesas recommends choosing 2.7kΩ for R_{PLL}, 10nF for C_{PLL1}, and 820pF for C_{PLL2}.

3.16 Feedback Loop Compensation

To adapt the different applications, the controller is designed with an externally compensation network. Figure 13 shows the peak current mode buck converter circuit.

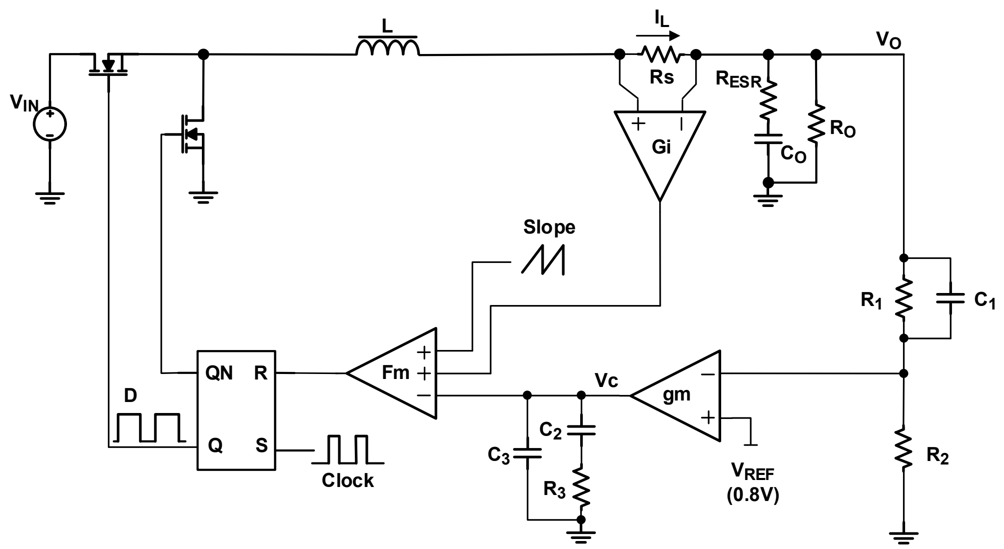

Figure 13. Peak Current Mode Buck Converter Circuit

In the current loop, the control to output simplified transfer function is shown in Equation 25.

(EQ. 25)
$$\frac{\hat{V}_O}{\hat{V}_C} = \frac{R_O}{R_I \times K_d} \times \frac{1 + \frac{s}{\omega_{z(esr)}}}{\left(1 + \frac{s}{\omega_{po}}\right)\left(1 + \frac{s}{\omega_{pi}}\right)}$$

where:

(EQ. 26)
$$K_d = 1 + \frac{R_O}{K_m \times R_I}$$

(EQ. 27)
$$K_m = \frac{1}{(0.5 - D)R_I \times \frac{T_s}{L} + \frac{V_{SL}}{V_{IN}}}$$

(EQ. 28)
$$R_I = G_I \times R_S$$

- R_O is the load resistor
- C_O is the output capacitor
- L is the inductor
- R_S is the current sense resistor
- V_O is the output voltage
- T_S is the period of one switching cycle
- D is the duty cycle of upper MOSFET
- V_{SL} = 0.843V, is the slope compensation voltage
- V_{IN} is the input voltage of the buck
- V_C is the output of the error amplifier
- G_I = 5.472, is the gain of the current sensor

The low frequency pole frequency is shown in Equation 29.

(EQ. 29) $$\omega_{p0} = 2\pi f_{p0} = \frac{1}{C_O} \times \left(\frac{1}{R_O} + \frac{1}{K_m \times R_I}\right)$$

The high frequency pole frequency is shown in Equation 30.

(EQ. 30) $$\omega_{pi} = 2\pi f_{pi} = \frac{K_m \times R_I}{L}$$

The output capacitor ESR (R_{ESR}) zero frequency is shown in Equation 31.

(EQ. 31) $$\omega_{z(esr)} = 2\pi f_{z(esr)} = \frac{1}{C_o \times R_{ESR}}$$

The output voltage is regulated by an error amplifier EA. The EA compensation network parameters can be determined by compensating the current loop poles and zero so as to implement an ideal -20dB/decade close-loop gain with around $0.1xf_{sw}$ crossover frequency.

If the crossover frequency $f_c << f_{pi}$, a type-2 compensation network is enough to achieve the goal.

Because a strong slope compensation is used, the f_{pi} is usually not too high but close to f_c. Therefore, a type-3 amplifier is still needed.

To simplify the model, assuming $C_3 << C_2$, the type-3 EA amplifier transfer function is simplified to Equation 32.

(EQ. 32) $$\frac{\hat{V}_c}{\hat{V}_o} = \frac{(1 + sR_3C_2)(1 + sR_1C_1)}{sR_1C_2(1 + sR_3C_3)}$$

The transfer function has two poles and two zeros.

- The first pole at the original at the frequency of $f_{p1} = 1/2\pi R_1C_2$. This is the frequency where the impedance of R_1 is equal to C_2.
- The second pole is at the frequency of $f_{p2} = 1/2\pi R_3C_3$.
- The first zero is at the frequency of $f_{z1} = 1/2\pi R_3C_2$.
- The second zero is at the frequency of $f_{z2} = 1/2\pi R_1C_1$

To achieve ideal compensation, Renesas recommends making $f_{z1} = f_{p0}$, $f_{z2} = f_{pi}$ and $f_{p2} = f_{z(esr)}$ as shown in Figure 14.

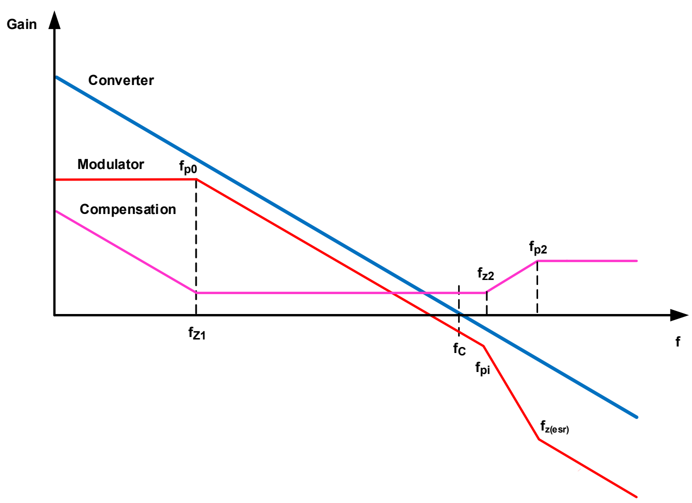

Figure 14. Feedback Loop Compensation

The close-loop transfer function is then simplified to Equation 33.

(EQ. 33) $$G_{loop}(s) = \frac{R_O}{R_I \times K_d} \times \frac{1 + \frac{s}{\omega_{z(esr)}}}{\left(1 + \frac{s}{\omega_{p0}}\right)\left(1 + \frac{s}{\omega_{pi}}\right)} \times \frac{(1 + sR_3C_2)(1 + sR_1C_1)}{sR_1C_2(1 + sR_3C_3)} = \frac{R_O}{R_I \times K_d} \times \frac{1}{sR_1C_2}$$

The crossover frequency is shown in Equation 34.

(EQ. 34) $$f_c = \frac{R_O}{K_d \times R_I} \times \frac{1}{2\pi R_1 C_2}$$

The Loop design example for the 12V output under the typical 48V input voltage is shown in the following:

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 10A, f_{sw} = 200kHz, T_s = 5µs, D = V_{OUT} / V_{in} = 0.25, L = 6.8µH, C_O = 1088µF (1000µFx1+22µFx4), R_O = V_{OUT} /I_{OUT} = 1.2Ω, R_s = 4mΩ, R_{esr} = 5mΩ.

(EQ. 35) $$K_m = \frac{1}{(0.5 - D)R_I \times \frac{T_s}{L} + \frac{V_{SL}}{V_{IN}}} = \frac{1}{(0.5 - 0.25)(4m\Omega \times 5.472) \times \frac{5\mu s}{6.8\mu H} + \frac{0.843V}{48V}} = 46.33$$

(EQ. 36) $$K_d = 1 + \frac{R_O}{K_m \times R_I} = 1 + \frac{1.2\Omega}{46.33 \times 0.022\Omega} = 2.177$$

(EQ. 37) $$G_{dc} = \frac{R_O}{K_d \times R_I} = \frac{1.2\Omega}{2.177 \times 0.022\Omega} = 25.06$$

(EQ. 38) $$\omega_{p0} = \frac{1}{C_O} \times \left(\frac{1}{R_O} + \frac{1}{K_m \times R_I}\right) = \frac{1}{1088\mu F} \times \left(\frac{1}{1.2\Omega} + \frac{1}{46.33 \times 0.022\Omega}\right) = 1.52kHz$$

(EQ. 39) $$f_{p0} = \frac{\omega_{p0}}{2\pi} = 0.24kHz$$

(EQ. 40) $$\omega_{pi} = \frac{K_m \times R_I}{L} = \frac{46.33 \times 0.022\Omega}{6.8\mu H} = 149.9kHz$$

(EQ. 41) $$f_{pi} = \frac{\omega_{pi}}{2\pi} = 23.87kHz$$

(EQ. 42) $$\omega_{z(esr)} = \frac{1}{C_O \times R_{ESR}} = \frac{1}{1088\mu F \times 5m\Omega} = 183.8kHz$$

(EQ. 43) $$f_{z(esr)} = \frac{\omega_{z(esr)}}{2\pi} = 29.3kHz$$

To make $0.1xf_s$ crossover frequency and make the gain -20dB/decade by Equation 44.

(EQ. 44) $$f_c = 0.1 \times f_{sw} = 20kHz$$

If R_1 (R_2) = 48.7k, R_2 (R_{12}) = 3.48k, R_3 (R_{11}) = 22k, C_1 (C46) = 150pF, C_2 (C_9) can be calculated using Equation 45.

(EQ. 45) $$C_2 = \frac{R_O}{K_d \times R_I} \times \frac{1}{2\pi R_1 f_c} = \frac{1.2\Omega}{2.177 \times 0.022\Omega} \times \frac{1}{2\pi \times 48.7k\Omega \times 20kHz} = 25.1nF$$

Select a standard value capacitor C_2 (C_9) = 22nF.

(EQ. 46) $$f_{z2} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 48.7k\Omega \times 150pF} = 22kHz$$

(EQ. 47) $$f_{z1} = \frac{1}{2\pi R_3 C_2} = \frac{1}{2\pi \times 22k\Omega \times 22nF} = 0.329kHz$$

To suppress the switching frequency noise, one more pole $f_{p2} = 1/2\pi R_3 C_3$ can be inserted.

The frequency of this pole should be $f_c << f_{p2} << f_{sw}$, which is set by Equation 48.

(EQ. 48) $$f_{p2} = \frac{1}{2\pi R_3 C_3} = 33kHz$$

Then C_3 (C_{12}) = 220pF.

4. Typical Performance Curves

V_{IN} = 48V, T_A = 25°C, unless otherwise noted.

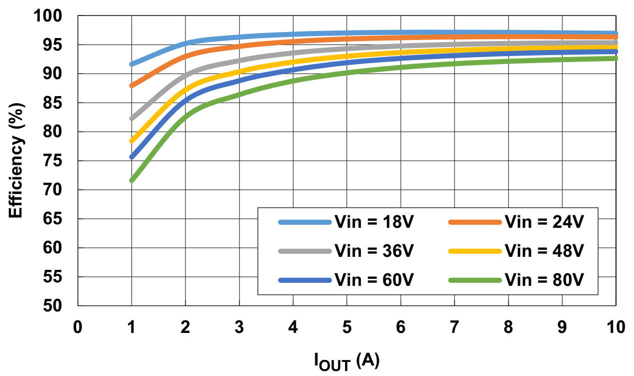

Figure 15. 12V Output Efficiency, CCM

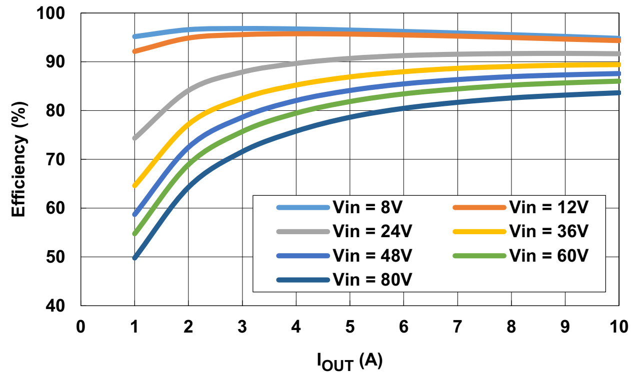

Figure 16. 5V Output Efficiency, CCM

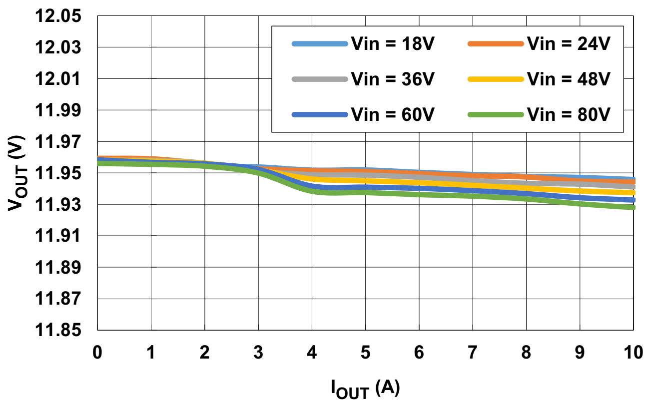

Figure 17. 12V Output Load Regulation, CCM

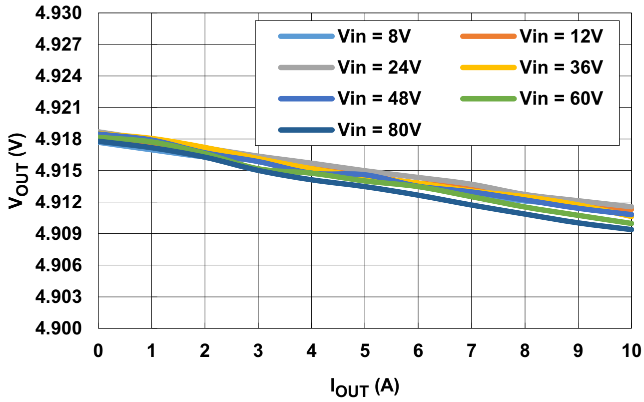

Figure 18. 5V Output Load Regulation, CCM

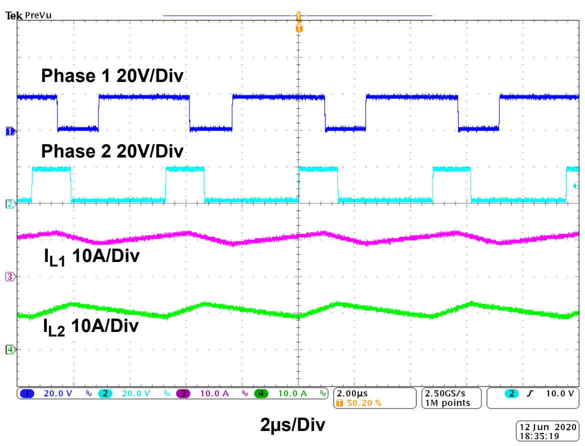

Figure 19. V_{IN} = 18V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 10A, I_{OUT2} = 10A, CCM

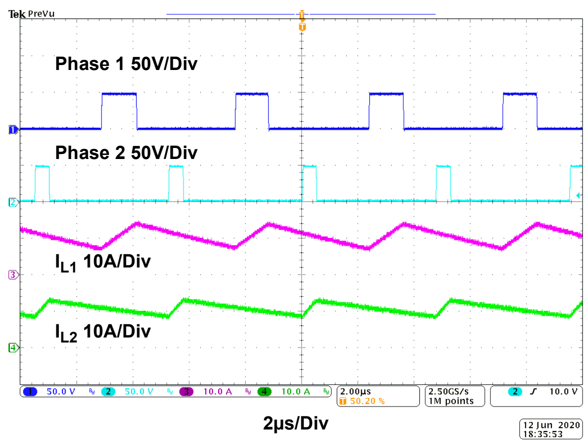

Figure 20. V_{IN} = 48V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 10A, I_{OUT2} = 10A, CCM

V_{IN} = 48V, T_A = 25°C, unless otherwise noted. **(Continued)**

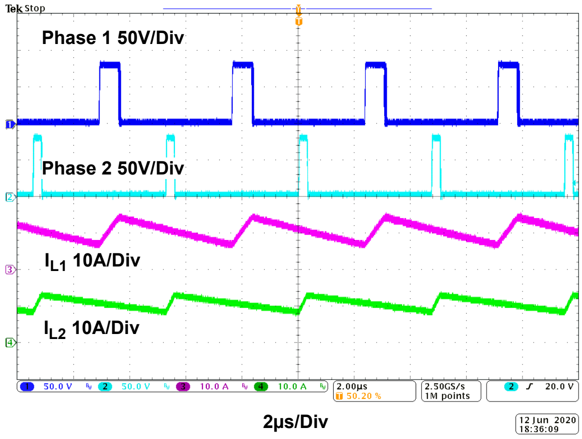

Figure 21. V_{IN} = 80V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 10A, I_{OUT2} = 10A, CCM

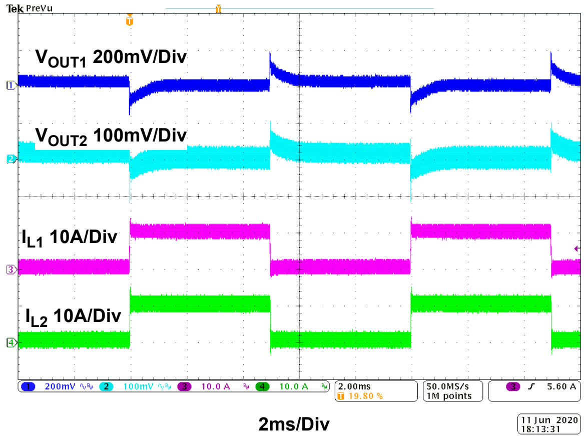

Figure 22. Load Transient, V_{IN} = 18V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 0A to 10A, I_{OUT2} = 0A to 10A, 2.5A/µs, CCM

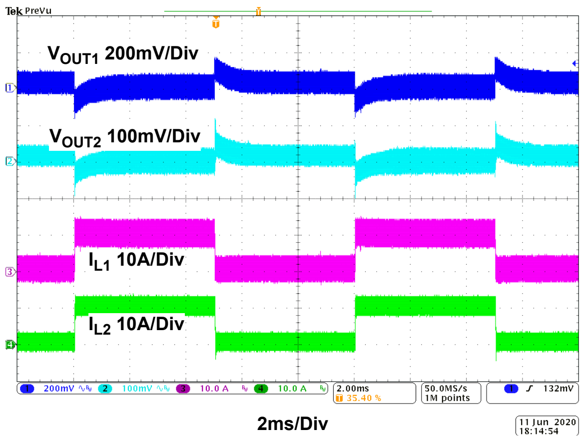

Figure 23. Load Transient, V_{IN} = 48V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 0A to 10A, I_{OUT2} = 0A to 10A, 2.5A/µs, CCM

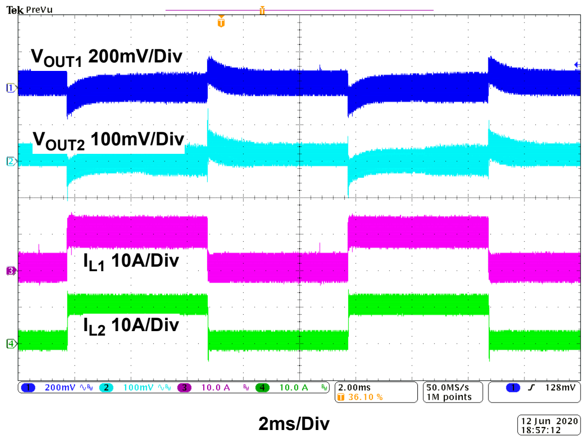

Figure 24. Load Transient, V_{IN} = 80V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 0A to 10A, I_{OUT2} = 0A to 10A, 2.5A/µs, CCM

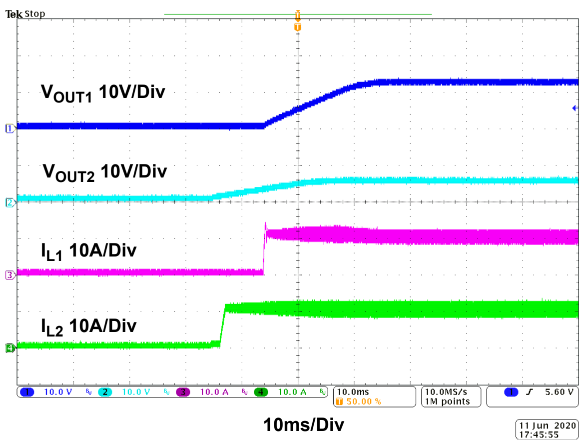

Figure 25. Start-Up Waveform, V_{IN} = 18V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 10A, I_{OUT2} = 10A, CCM

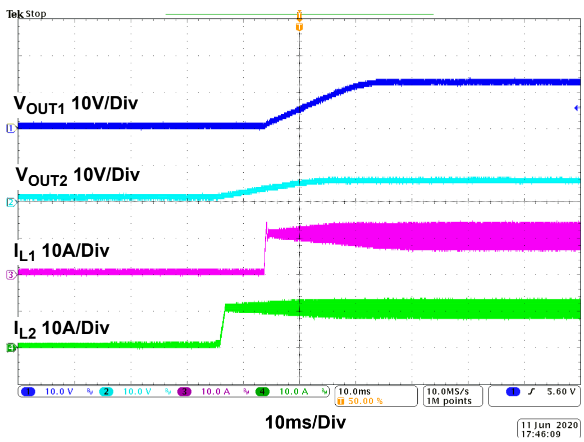

Figure 26. Start-Up Waveform, V_{IN} = 48V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 10A, I_{OUT2} = 10A, CCM

V_{IN} = 48V, T_A = 25°C, unless otherwise noted. **(Continued)**

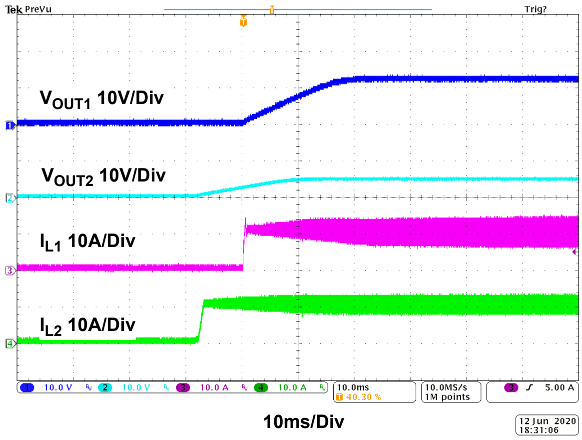

Figure 27. Start-Up Waveform, V_{IN} = 80V, V_{OUT1} = 12V, V_{OUT2} = 5V, I_{OUT1} = 10A, I_{OUT2} = 10A, CCM

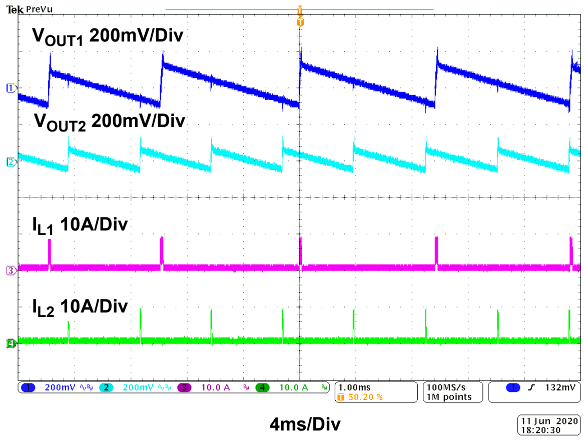

Figure 28. Burst Mode Waveforms, V_{IN} = 48V, I_{OUT1} = 0.1A, I_{OUT2} = 0.1A

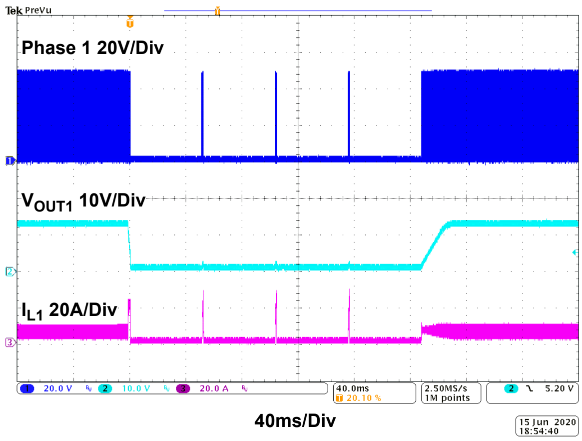

Figure 29. 12V Output Short-Circuit Waveform

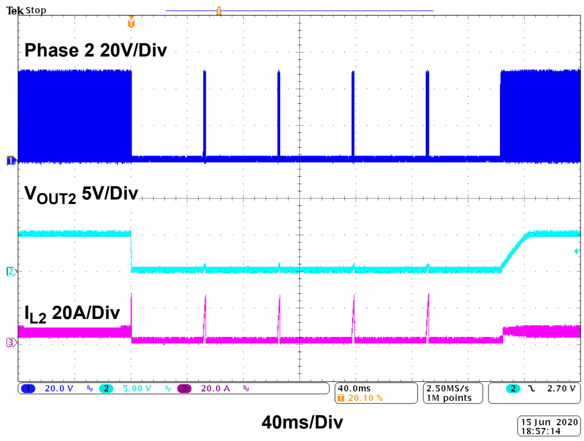

Figure 30. 5V Output Short-Circuit Waveform

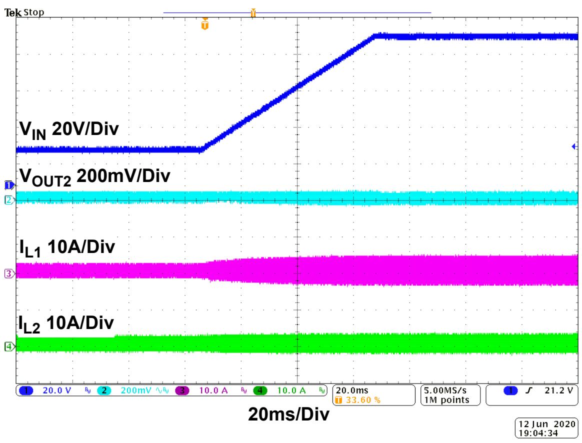

Figure 31. Line Transient, V_{IN} = 18V to 80V, 1V/ms, I_{OUT} = 0A

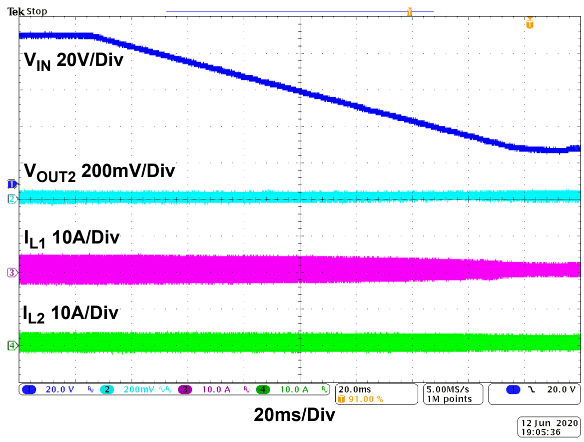

Figure 32. Line Transient, V_{IN} = 80V to 18V, 1V/ms, I_{OUT} = 0A

5. Revision History

Rev.	Date	Description
1.00	Aug.24.20	Initial release

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