IDT™ 89EBPES64H16 / 89EBPES48H12 / 89EBPES48T12 Evaluation Board Manual

(Eval Board: 18-624-000)

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Foreword

This evaluation board manual includes hardware and software information on the 89HPES64H16, 89HPES48H12, and 89HPES48T12 peripheral chips. All three devices are members of IDT's PRECISE™ family of PCI Express® switching solutions.

The 89HPES64H16 (PES64H16) is a 64-lane, 16-port switch and the 89HPES48H12 (PES48H12) is a 48-lane, 12-port switch. Both devices are system interconnect switches that perform PCI Express packet switching with a feature set optimized for high-performance applications where multiple peer-to-peer traffic flows are simultaneously transmitted.

The 89HPES48T12 (PES48T12) is a 48-lane, 12-port peripheral chip that performs PCI Express Packet switching with a feature set optimized for high-performance applications such as servers, storage, and communications/networking.

The same evaluation board is used for all three of these devices and, consequently, the information in this manual applies equally, with some exceptions, to all three devices. Throughout the manual, numerous references are made to the 89EBPES64H16 Evaluation Board (also referred to as EB64H16). These references to the EB64H16 should be interpreted as also applying to both an EB48H12 board and an EB48T12 board, except where noted.

Introduction

The EB64H16 evaluation board provides an evaluation platform for the PES64H16 switch. The EB64H16 has two x4 ports which can be merged to provide one x8 upstream port on a standard x16 PCI Express connector. This port is used to connect an adaptor card with a cable to another adaptor card in the root complex or host system. Alternatively, the upstream port can be defined as a x4 port allowing for fifteen downstream ports.

The downstream slots will conform to the x8 and x4 connector pin assignments but will be populated with x16 connectors. The unused lane bits on the x16 connectors will be unconnected. The core and IO power for the PES64H16 is derived from the 12V power supply connector from a 12VEPS type power supply with a 24-pin connector and a 8-pin connector with 12V. The downstream slot power is controlled through hot-plug controllers with power provided from the 12VEPS power supply connector with 12V. A personality module is used to optionally merge two x4 ports into one x8 downstream port connector. The PES64H16 Evaluation board block diagram is shown in Figure 1.1 and the PES48H12 / PES48T12 block diagram is shown in Figure 1.2.

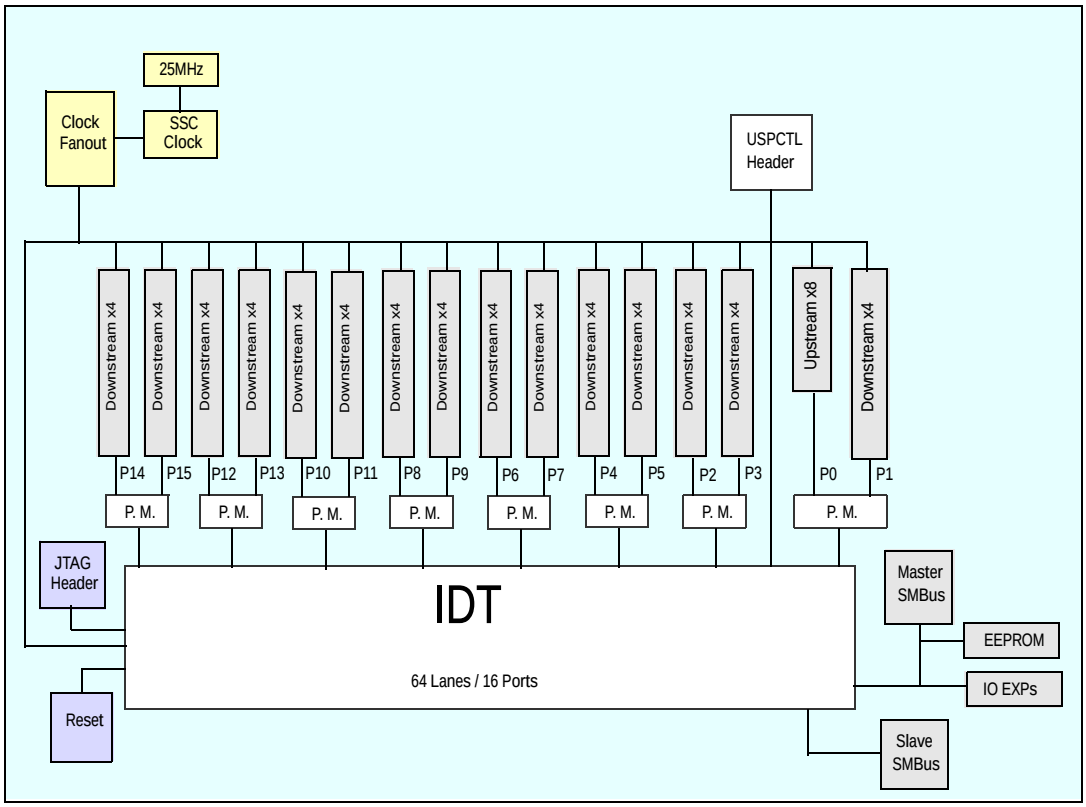

Figure 1.1 Functional Block Diagram of the EB64H16 Eval Board

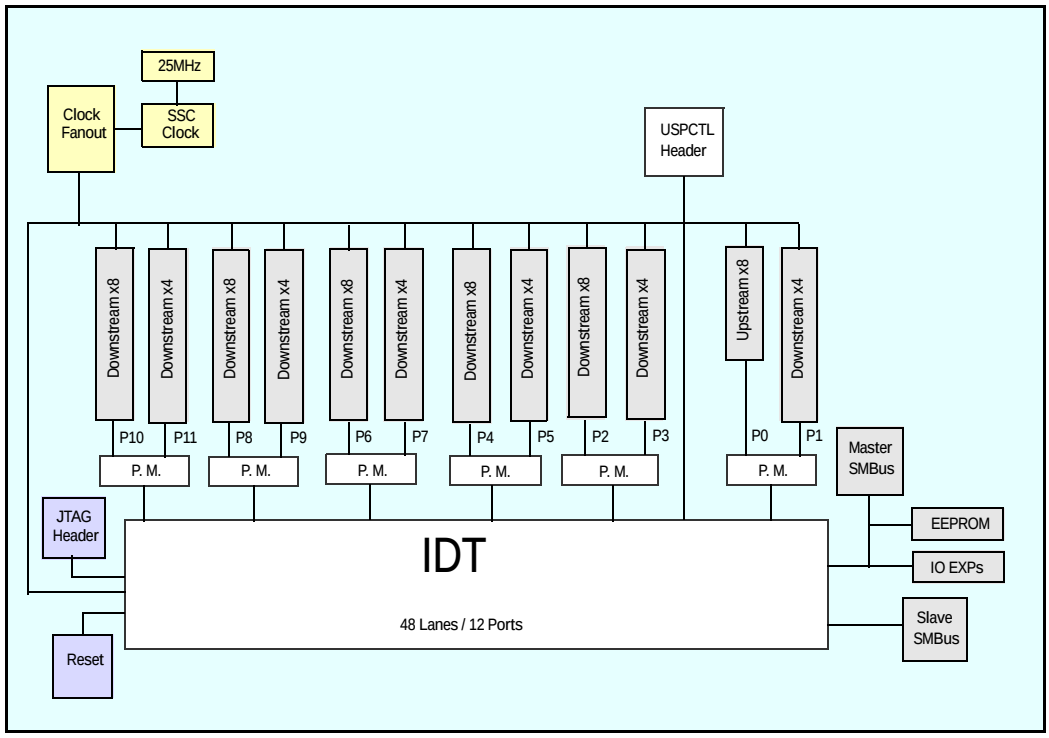

Figure 1.2 Functional Block Diagram of the EB48H12 and EB48T12 Eval Boards

Notes

Board Features

Feature List

- The EB64H16 has one x8 PCI Express upstream port to the root complex provided by a PCI Express adaptor board to a cable that connects to another adaptor board in the root complex or host system.
- The EB64H16 provides fifteen downstream connectors with x4 ports, while the EB48H12 and EN48T12 provide 11 downstream connectors. Two x4 downstream slots can be configured as one x8 port through the personality modules.
- All fifteen downstream slots for the PES64H16 and all eleven downstream slots for the PES48H12 and PES48T12 have hot-plug support through power isolation controlled by a hot-plug controller and IO expanders on the Master SMBUS. The Master SMBUS is controlled by the PES64H16 through configuration registers.
- The EB64H16 has a 12V to 2.5V DC-DC converter that uses the 12V power from an external 12VEPS power supply connector with 12V. The 2.5V provides power to the DC-DC converters for the PES64H16 core power.
- JTAG connector to the PES64H16 JTAG pins.
- Serial EEPROM on the PES64H16 master SMBUS interface.
- Provides an SMBUS connector on the PES64H16 slave SMBUS interface.
- Has a fundamental cold and warm reset mechanism and a reset push button switch.
- Provides a clock reference to the fifteen (or eleven) downstream ports from the upstream clock reference or from an on-board clock generator. The clock generator has spread spectrum clocking option and SMA connectors are provided to monitor the clock.
- Has LED displays to indicate power is applied, reset condition, port status, and downstream slot power.
- Has card present detect pins implemented on upstream and downstream slots.
- Has ATTN push button switches and LED displays for each downstream slot.
- Has a +12V fan connector for the integrated heatsink for the socket and soldered device.

Performance Summary

- Provides up to 16 ports with 64 PCIe lanes (PES64H16) or up to 12 ports with 48 PCIe lanes (PES48H12/PES48T12)
- Integrated SerDes support 2.5 Gbps operation
- Delivers up to 32 GBps (256 Gbps) of aggregate bandwidth
- Sub 280ns latency through the switch
- Supports two virtual channels
- Compliant with PCI Express Base Specification Rev1.1 with Rev 2.0 features
- Flexible Architecture with Numerous Configuration Options
- Eight x8 PCIe ports
- Each port can be independently bifurcated into two x4 PCIe ports
- Supports automatic per port link width negotiation(e.g., x8/x4/x2/x1 for a x8 port)
- Automatic lane reversal detection
- Independent per port crosslink support
- Supports lock transactions, allowing use of PCI Express with legacy software
- Ability to load device configuration from serial EEPROM
- Supports external signal for hot plug event notification allowing SCI/SMI generation for legacy operating systems
- Supports external signal for power management event notification

Notes

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES64H16 within host systems running popular operating systems.

- Installation programs
  - Operating Systems Supported: Windows2000, WindowsXP, Linux
- GUI based application for Windows and Linux
  - Allows users to view and modify registers in the PES64H16
  - Binary file generator for programming the serial EEPROMs attached to the SMBUS

Other

An external power supply may be required under some conditions.

An SMBUS cable may be required for certain evaluation exercises.

SMA connectors are provided on the EB64H16 board for specific test points.

Revision History

January 16, 2007: Published production release board revision 0.9.

Installation of the EB64H16 Eval Board

Notes

EB64H16 Installation

This chapter discusses the steps required to configure and install the EB64H16 evaluation board. All available DIP switches and jumper configurations are explained in detail. The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Connect a PCI Express adapter card in an upstream port with a cable to another PCI Express adaptor card in the root complex or host system, as shown in Figure 2.1.
4. Turn the power switch on the eval board (located at S3) to ON.
5. Apply power to the host system.

The EB64H16 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

PCI Express Adapter Card

The PCI Express adapter card contains eight PCI Express lanes (see Figure 2.1). The lower four lanes are routed to an Infiniband connector J2 and the upper four lanes to J3. The differential REFCLKp and REFCLKn pins are routed to J5 and J6, respectively. The JTAG interface and PERST# pins are routed to J4 although only PERST# pin is actually used. Two PCI Express Adapter cards are required to connect the EB64H16 evaluation board to the host PC and remember to match the connector connection between two cards.

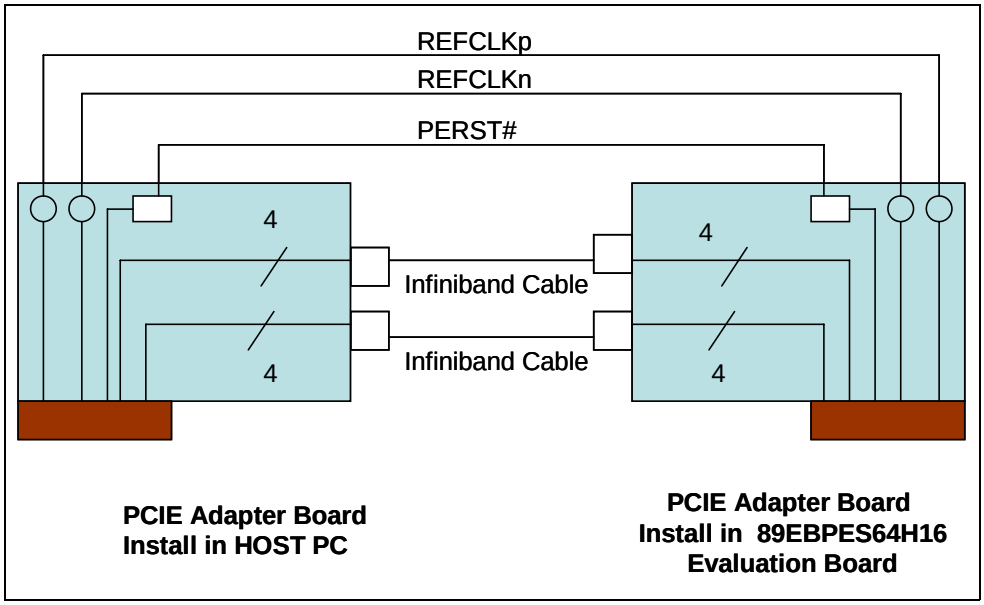

Figure 2.1 PCIe Adapter

Notes

Hardware Description

The PES64H16 is a 64-lane, 16-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 15 downstream ports or peer-to-peer switching between downstream ports.

The EB64H16 has 15 PCI Express downstream ports, accessible through fifteen x16 connectors. Seven specific ports are capable of negotiating a x1, x2, x4, or x8 link width and all fifteen ports are capable of negotiating a x1, x2, x4 link width. All endpoint cards connected to the PES64H16 must support at least one of these link widths. A personality module can be used to provide a single x8 downstream port by merging two specific x4 ports (see section PCI Express Personality Module on page 2-23).

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot. (If your host system does not offer a x8 slot, please contact ssdhelp@idt.com for alternative solutions.)
- x1, x2, x4, or x8 PCI Express Endpoint Cards.

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot is required to take full advantage of the PES64H16's capabilities. One such system is the SuperMicro X6DH8-G2 motherboard equipped with an Intel E7520 chipset which was introduced in 2004 to deploy dual-processor server chipset technology. The board has three PCI Express slots. All slots have x8 connectors, but only two are electronically connected for a x8 link width (J15 and J16). The remaining slots are electronically connected for a x4 link width configuration. Care must be taken to avoid using the EB64H16 in the x4 slot (J17). Figure 2.2 shows the proper connectors.

Notes

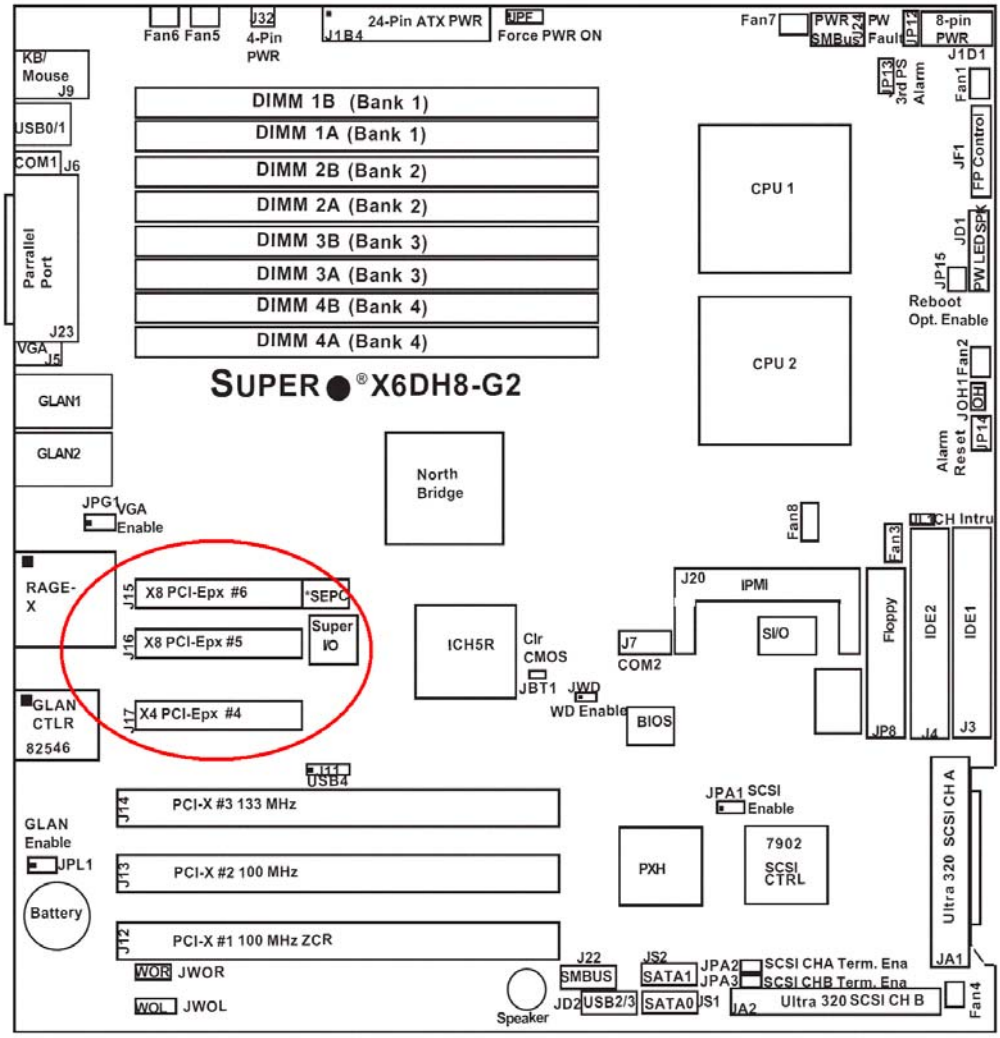

Figure 2.2 SuperMicro X6DH8-G2 Motherboard

Reference Clocks

The PES64H16 requires four differential reference clocks. The EB64H16 derives these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
Install	Clock Source
R36, R37	Onboard Reference Clock – Use onboard clock generator
R35, R148	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS59FG104 clock generator device (U14) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB64H16 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - S2[4:2]			
S2[4]	S2[3]	S2[2]	Clock Frequency
ON	ON	ON	100 MHz (Default)
ON	ON	OFF	125 MHz
ON	ON	ON	<Reserved>
OFF	OFF	OFF	<Reserved>

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S2[1]	
S2[1]	Spread
OFF	No Spread (Default)
ON	Spread Enable

Table 2.3 Clock Spread Spectrum Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock must be used instead.

The output of the two onboard clock generator is accessible through four SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J1, J3, J15, J8	
J1, J15	Positive Reference Clock
J3, J8	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Figure 2.3 illustrates the clock distribution block diagram for the EB64H16 evaluation board.

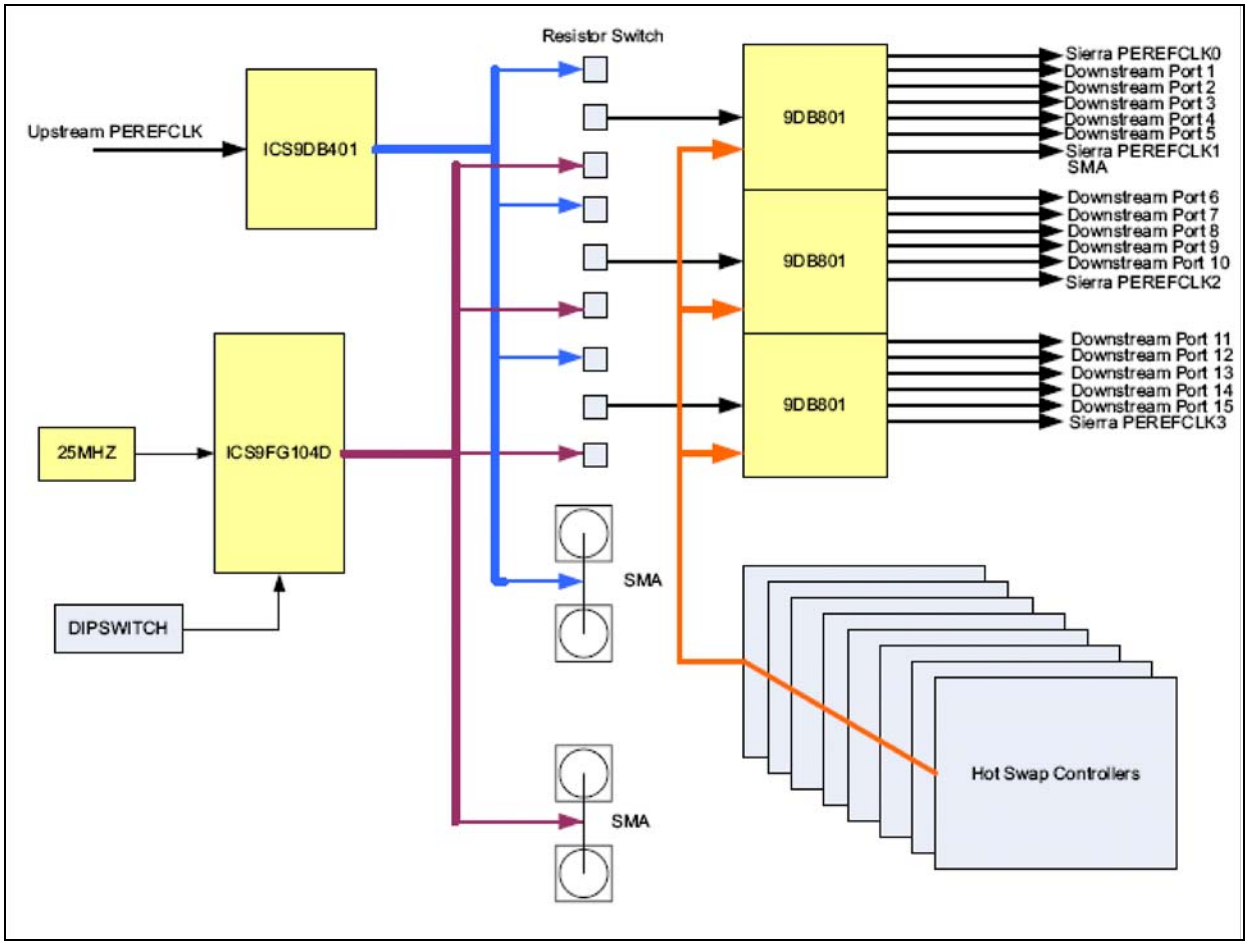

Figure 2.3 Clock Distribution Block Diagram

Power Sources

Power for the PES64H16 and all downstream ports is generated from the 12V from an external power connector. See Figure 2.4. A 12V to 2.5V DC-DC converter is used to provide power to four LDO linear regulators to generate V_{DD}CORE, V_{DD}PEe, V_{DD}APE, and V_{TT}PE voltages. The 2.5V from the DC-DC converter is used to power the clock buffers. 3.3V is supplied form the power connector for V_{DD}IO.

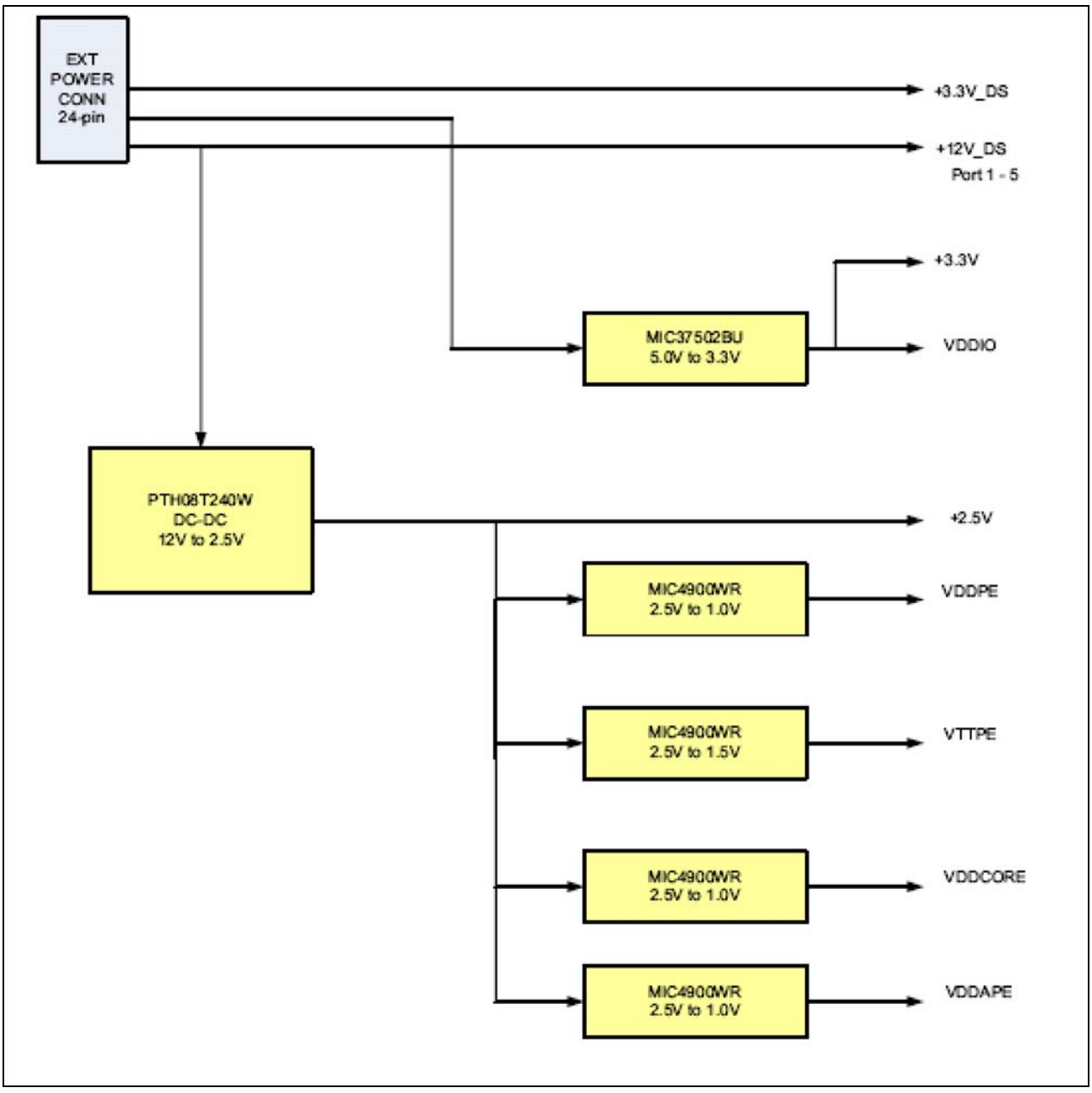

Figure 2.4 Power Distribution Block Diagram

Notes

The external power supply connectors are a 24-pin (J6) and an 8-pin (J5) molex connector as described in Table 2.5 and Table 2.6. The +12V3 is used to power PES64H16 and downstream ports 1 through 5. The +12V1 is used to power downstream ports 6 through 10. The +12V2 is used to power downstream ports 11 through 15.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	5VSB	21	+5V
10	+12V3	22	+5V
11	+12V3	23	+5V
12	+3.3V	24	GND

Table 2.5 EPS12V 24_pin Power Connector - J6

Pin	Signal	Pin	Signal
1	GND	5	+12V1
2	GND	6	+12V1
3	GND	7	+12V2
4	GND	8	+12V2

Table 2.6 EPS12V 8-Pin Connector - J5

The power on switch located at S3 can be used to control the supply power from the external power supply connector. Add a shunt to W19 to enable power on switch.

Power Supply Minimum Load Connectors

To provide the minimum load requirement for each rail of the EPS12V supply, a 2-pin fan connector is provided for connecting to an external power resistor for each rail.

Connector	Supply	Load Resistor Value
W157	3.3V	5.0 ohm
W158	5V	5.0 ohm
W100	12V1	25.0 ohm
W156	12V2	25.0 ohm
W159	12V3	25.0 ohm

Table 2.7 Minimum Load Connectors

Notes

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U6) provides a 1.5V PCI Express serial data transmit termination voltage (VTT) to the PES64H16.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U7) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES64H16.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U28) provides a 1.0V PCI Express analog power voltage (VDDAPE) to the PES64H16.

Core Logic Voltage Converter

A separate DC-DC converter (U1) provides the 1.0V core voltage (VDDCORE) to the PES64H16.

3.3V I/O Power Module

A separate DC-DC converter (U17) provides the 3.3V I/O voltage (VDDIO) to the PES64H16.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDAPE, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements.

Required Jumpers

To deliver power to the PES64H16 switch, the following jumpers must be shunted: W151, W152, WW153, W154, W155. These jumpers were implemented so that the power consumption of the PES64H16 can be measured.

Heatsink Requirement

The PES64H16 with a maximum power dissipation of 13W will require a heatsink. The EB64H16 evaluation board utilizes Molex heatsink with integrated fan.

Reset

The PES64H16 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES64H16, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES64H16 User Manual. The EB64H16 evaluation board provides seamless support for Hot Reset.

Notes

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB64H16 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES64H16.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - Pressing a push-button switch (S1) located on EB64H16 board
  - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB64H16. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W1.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES64H16 while power is on.

Downstream Reset

The PES64H16 provides a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.8.

Port #	Jumper	Selection
1	W102	[1-2] Software controlled reset through GPIO6 [2-3] Fundamental reset PERST# (default)
2	W107	[1-2] Software controlled reset through GPIO7 [2-3] Fundamental reset PERST# (default)
3	W108	[1-2] Software controlled reset through GPIO8 [2-3] Fundamental reset PERST# (default)
4	W113	[1-2] Software controlled reset through GPIO9 [2-3] Fundamental reset PERST# (default)
5	W114	[1-2] Software controlled reset through GPIO10 [2-3] Fundamental reset PERST# (default)
6	W119	[1-2] Software controlled reset through GPIO11 [2-3] Fundamental reset PERST# (default)
7	W120	[1-2] Software controlled reset through GPIO12 [2-3] Fundamental reset PERST# (default)
8	W125	[1-2] Software controlled reset through GPIO13 [2-3] Fundamental reset PERST# (default)
9	W126	[1-2] Software controlled reset through GPIO14 [2-3] Fundamental reset PERST# (default)
10	W131	[1-2] Software controlled reset through GPIO15 [2-3] Fundamental reset PERST# (default)
11	W132	[1-2] Software controlled reset through GPIO16 [2-3] Fundamental reset PERST# (default)
12	W137	[1-2] Software controlled reset through GPIO17 [2-3] Fundamental reset PERST# (default)

Table 2.8 Downstream Reset Selection (Part 1 of 2)

Notes

Port #	Jumper	Selection
13	W138	[1-2] Software controlled reset through GPIO18 [2-3] Fundamental reset PERST# (default)
14	W143	[1-2] Software controlled reset through GPIO19 [2-3] Fundamental reset PERST# (default)
15	W144	[1-2] Software controlled reset through GPIO20 [2-3] Fundamental reset PERST# (default)

Table 2.8 Downstream Reset Selection (Part 2 of 2)

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.9 is sampled by the PES64H16 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5 and S6 as defined in Table 2.10.

Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that a common clock is being used between the downstream device and the downstream port. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that a common clock is being used between the downstream device and the downstream port. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. Default: 0x0
P01MERGEN	Port 0 and 1 Merge: When this pin is asserted (i.e. low), port 1 is merged with port 0 to form a single x8 port. Default: 0x0
P23MERGEN	Port 2 and 3 Merge: When this pin is asserted (i.e. low), port 2 is merged with port 3 to form a single x8 port. Default: 0x1
P45MERGEN	Port 4 and 5 Merge: When this pin is asserted (i.e. low), port 4 is merged with port 5 to form a single x8 port. Default: 0x1
P67MERGEN	Port 6 and 7 Merge: When this pin is asserted (i.e. low), port 6 is merged with port 7 to form a single x8 port. Default: 0x1
P89MERGEN	Port 8 and 9 Merge: When this pin is asserted (i.e. low), port 8 is merged with port 9 to form a single x8 port. Default: 0x1
P1011MERGEN	Port 10 and 11 Merge: When this pin is asserted (i.e. low), port 10 is merged with port 11 to form a single x8 port. Default: 0x1
P1213MERGEN	Port 12 and 13 Merge: When this pin is asserted (i.e. low), port 12 is merged with port 13 to form a single x8 port. Default: 0x1
P1415MERGEN	Port 14 and 15 Merge: When this pin is asserted (i.e. low), port 14 is merged with port 15 to form a single x8 port. Default: 0x1
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES64H16 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0

Table 2.9 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
SWMODE[3:0]	Switch Mode. These configuration pins determine the PES64H16 switch operating mode. Default: 0x0 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x7 - Reserved 0x8 - Normal switch mode with upstream port failover (port 0 selected as the upstream port) 0x9 - Normal switch mode with upstream port failover (port 2 selected as the upstream port) 0xA - Normal switch mode with Serial EEPROM and upstream port failover (port 0 selected as the upstream port) 0xB - Normal switch mode with Serial EEPROM and upstream port failover (port 2 selected as the upstream port) 0xC through 0xF - Reserved
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[4:1]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.9 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S19[1]	CCLKDS	OFF
S19[2]	CCLKUS	OFF
S19[3]	MSMBSMODE	ON
S20[1]	P01MERGEN	ON
S20[2]	P23MERGEN	OFF
S20[3]	P45MERGEN	OFF
S20[4]	P67MERGEN	OFF
S20[5]	P89MERGEN	OFF
S20[6]	P1011MERGEN	OFF
S20[7	P1213MERGEN	OFF
S20[8]	P11415MERGEN	OFF
S19[8]	RSTHALT	ON
S21[1]	SWMODE[0]	ON
S21[2]	SWMODE[1]	ON
S21[3]	SWMODE[2]	ON
S21[4]	SWMODE[3]	ON
S21[5]	REFCLKM	ON
S21[6]	MSMBADDR[0]	ON
S21[7]	MSMBADDR[1]	ON
S21[8]	MSMBADDR[2]	ON

Table 2.10 Boot Configuration Vector Switches S19, S20 & S21 (ON=0, OFF=1)

Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES64H16 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals.

SMBus Slave Interface

On the EB64H16 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.11.

.

Slave SMBus Interface Connector J34	
Pin	Signal
1	N/C
2	SSMBCLK
3	GND
4	SSMBDATA

Table 2.11 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

For a fixed address, the SMBus address of the PES64H16 slave interface is 0b1110111 by default and is configurable using jumpers W146, W147, W148, and W149 as described in Tables 2.12 and 2.13.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.12 SMBus Slave Interface Address Configuration

Notes

SMBUS Slave Interface Address Setting				
W146 SSMBADDR[5]	W147 SSMBADDR[3]	W148 SSMBADDR[2]	W149 SSMBADDR[1]	Slave Interface Bus Address
OFF	OFF	OFF	OFF	0b1110111 (Default)
OFF	OFF	OFF	ON	0b1110110
OFF	OFF	ON	OFF	0b1110101
OFF	OFF	ON	ON	0b1110100
OFF	ON	OFF	OFF	0b1110011
OFF	ON	OFF	ON	0b1110010
OFF	ON	ON	OFF	0b1110001
OFF	ON	ON	ON	0b1110000
ON	OFF	OFF	OFF	0b1100111
ON	OFF	OFF	ON	0b1100110
ON	OFF	ON	OFF	0b1100101
ON	OFF	ON	ON	0b1100100
ON	ON	OFF	OFF	0b1100011
ON	ON	OFF	ON	0b1100010
ON	ON	ON	OFF	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.13 PES64H16 SMBus Slave Interface Address Setting

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are 10 16-bit I/O Expanders (Maxim PAX731) and a serial EEPROM (24LC512). The I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander 0 through I/O Expander 10 are fixed through the stuffing resistor as 0x0, 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7, 0x8, 0x9 and 0xA, respectively.

The bus address for the selected EEPROM device is **0b1000** by default and is configurable using W145 and the switch S21 as described in Table 2.14.

W145	S21[8]	S21[7]	S21[6]	Bus Address
OFF	OFF	OFF	OFF	0b0101 1111
OFF	OFF	OFF	ON	0b0101 1110
OFF	OFF	ON	OFF	0b0101 1101

Table 2.14 EEPROM SMBus Address Setting (Part 1 of 2)

Notes

W145	S21[8]	S21[7]	S21[6]	Bus Address
OFF	OFF	ON	ON	0b0101 1100
OFF	ON	OFF	OFF	0b0101 1011
OFF	ON	OFF	ON	0b0101 1010
OFF	ON	ON	OFF	0b0101 1001
OFF	ON	ON	ON	0b0101 1000
ON	ON	ON	ON	0b0101 0000 (Default)

Table 2.14 EEPROM SMBus Address Setting (Part 2 of 2)

JTAG Header

The PES64H16 provides a JTAG connector J33 for access to the PES64H16 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.15 for the JTAG Connector J33 pin out.

JTAG Connector J33					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.15 JTAG Connector Pin Out

Attention Buttons

The PES64H16 features fifteen attention buttons, shown in Table 2.16. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S5	Port 1 Attention Button
S4	Port 2 Attention Button
S10	Port 3 Attention Button
S11	Port 4 Attention Button
S6	Port 5 Attention Button
S7	Port 6 Attention Button
S8	Port 7 Attention Button
S9	Port 8 Attention Button
S12	Port 9 Attention Button
S13	Port 10 Attention Button
S14	Port 11 Attention Button

Table 2.16 Attention Buttons (Part 1 of 2)

Notes

Button	Description
S15	Port 12 Attention Button
S16	Port 13 Attention Button
S17	Port 14 Attention Button
S18	Port 15 Attention Button

Table 2.16 Attention Buttons (Part 2 of 2)

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W2-W4, W7, W10-W16, W48-W51	Header	Shunted	Bypass hot-plug controller - Enable REFCLK to downstream ports (Default)
W150	Header	Shunted	Disable EEPROM Write protect feature (Default)
W19	Header	Open	Enable Power On Switch (S3) (Default)
W91	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 1 (Default)
W57	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 2 (Default)
W58	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 3 (Default)
W70	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 4 (Default)
W71	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 5 (Default)
W75	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 6 (Default)
W76	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 7 (Default)
W79	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 8 (Default)
W80	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 9 (Default)
W83	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 10 (Default)
W84	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 11 (Default)
W87	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 12 (Default)

Table 2.17 Miscellaneous Jumpers, Headers (Part 1 of 4)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W88	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 13 (Default)
W91	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 14 (Default)
W92	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 15 (Default)
W97	Header	Shunted	2-3: Port 1, 3.3Vaux source from External Power (Default) 1-2: Port 1, 3.3Vaux source from hot-plug controller
W69	Header	2-3 Shunted	2-3: Port 2, 3.3Vaux source from External Power (Default) 1-2: Port 2, 3.3Vaux source from hot-plug controller
W70	Header	2-3 Shunted	2-3: Port 3, 3.3Vaux source from External Power (Default) 1-2: Port 3, 3.3Vaux source from hot-plug controller
W73	Header	2-3 Shunted	2-3: Port 4, 3.3Vaux source from External Power (Default) 1-2: Port 4, 3.3Vaux source from hot-plug controller
W74	Header	2-3 Shunted	2-3: Port 5, 3.3Vaux source from External Power (Default) 1-2: Port 5, 3.3Vaux source from hot-plug controller
W77	Header	2-3 Shunted	2-3: Port 6, 3.3Vaux source from External Power (Default) 1-2: Port 6, 3.3Vaux source from hot-plug controller
W78	Header	2-3 Shunted	2-3: Port 7, 3.3Vaux source from External Power (Default) 1-2: Port 7, 3.3Vaux source from hot-plug controller
W81	Header	2-3 Shunted	2-3: Port 8, 3.3Vaux source from External Power (Default) 1-2: Port 8, 3.3Vaux source from hot-plug controller
W82	Header	2-3 Shunted	2-3: Port 9, 3.3Vaux source from External Power (Default) 1-2: Port 9, 3.3Vaux source from hot-plug controller
W85	Header	2-3 Shunted	2-3: Port 10, 3.3Vaux source from External Power (Default) 1-2: Port 10, 3.3Vaux source from hot-plug controller
W86	Header	2-3 Shunted	2-3: Port 11, 3.3Vaux source from External Power (Default) 1-2: Port 11, 3.3Vaux source from hot-plug controller
W89	Header	2-3 Shunted	2-3: Port 12, 3.3Vaux source from External Power (Default) 1-2: Port 12, 3.3Vaux source from hot-plug controller
W90	Header	2-3 Shunted	2-3: Port 13, 3.3Vaux source from External Power (Default) 1-2: Port 13, 3.3Vaux source from hot-plug controller
W93	Header	2-3 Shunted	2-3: Port 14, 3.3Vaux source from External Power (Default) 1-2: Port 14, 3.3Vaux source from hot-plug controller
W94	Header	2-3 Shunted	2-3: Port 15, 3.3Vaux source from External Power (Default) 1-2: Port 15, 3.3Vaux source from hot-plug controller
W99	Header	2-3 Shunted	2-3: Port 1, +12V source base on W91 (Default) 1-2: Port 1, +12V source from hot-plug controller
W103	Header	2-3 Shunted	2-3: Port 2, +12V source base on W57(Default) 1-2: Port 2, +12V source from hot-plug controller
W104	Header	2-3 Shunted	2-3: Port 3, +12V source base on W58 (Default) 1-2: Port 3, +12V source from hot-plug controller

Table 2.17 Miscellaneous Jumpers, Headers (Part 2 of 4)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W109	Header	2-3 Shunted	2-3: Port 4, +12V source base on W71 (Default) 1-2: Port 4, +12V source from hot-plug controller
W110	Header	2-3 Shunted	2-3: Port 5, +12V source base on W72 (Default) 1-2: Port 5, +12V source from hot-plug controller
W115	Header	2-3 Shunted	2-3: Port 6, +12V source base on W75 (Default) 1-2: Port 6, +12V source from hot-plug controller
W116	Header	2-3 Shunted	2-3: Port 7, +12V source base on W76 (Default) 1-2: Port 7, +12V source from hot-plug controller
W121	Header	2-3 Shunted	2-3: Port 8, +12V source base on W79 (Default) 1-2: Port 8, +12V source from hot-plug controller
W122	Header	2-3 Shunted	2-3: Port 9, +12V source base on W80 (Default) 1-2: Port 9, +12V source from hot-plug controller
W127	Header	2-3 Shunted	2-3: Port 10, +12V source base on W83 (Default) 1-2: Port 10, +12V source from hot-plug controller
W128	Header	2-3 Shunted	2-3: Port 11, +12V source base on W84 (Default) 1-2: Port 11, +12V source from hot-plug controller
W133	Header	2-3 Shunted	2-3: Port 12, +12V source base on W87 (Default) 1-2: Port 12, +12V source from hot-plug controller
W'34	Header	2-3 Shunted	2-3: Port 13, +12V source base on W88 (Default) 1-2: Port 13, +12V source from hot-plug controller
W139	Header	2-3 Shunted	2-3: Port 14, +12V source base on W91 (Default) 1-2: Port 14, +12V source from hot-plug controller
W140	Header	2-3 Shunted	2-3: Port 15, +12V source base on W92 (Default) 1-2: Port 15, +12V source from hot-plug controller
W101	Header	2-3 Shunted	2-3: Port 1, +3.3V source base on W95 (Default) 1-2: Port 1, +3.3V source from hot-plug controller
W105	Header	2-3 Shunted	2-3: Port 2, +3.3V source base on W57 (Default) 1-2: Port 2, +3.3V source from hot-plug controller
W106	Header	2-3 Shunted	2-3: Port 3, +3.3V source base on W58 (Default) 1-2: Port 3, +3.3V source from hot-plug controller
W111	Header	2-3 Shunted	2-3: Port 4, +3.3V source base on W71 (Default) 1-2: Port 4, +3.3V source from hot-plug controller
W112	Header	2-3 Shunted	2-3: Port 5, +3.3V source base on W72 (Default) 1-2: Port 5, +3.3V source from hot-plug controller
W117	Header	2-3 Shunted	2-3: Port 6, +3.3V source base on W75 (Default) 1-2: Port 6, +3.3V source from hot-plug controller
W118	Header	2-3 Shunted	2-3: Port 7, +3.3V source base on W76 (Default) 1-2: Port 7, +3.3V source from hot-plug controller
W123	Header	2-3 Shunted	2-3: Port 8, +3.3V source base on W79 (Default) 1-2: Port 8, +3.3V source from hot-plug controller
W124	Header	2-3 Shunted	2-3: Port 9, +3.3V source base on W80 (Default) 1-2: Port 9, +3.3V source from hot-plug controller

Table 2.17 Miscellaneous Jumpers, Headers (Part 3 of 4)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W129	Header	2-3 Shunted	2-3: Port 10, +3.3V source base on W83 (Default) 1-2: Port 10, +3.3V source from hot-plug controller
W130	Header	2-3 Shunted	2-3: Port 11, +3.3V source base on W84 (Default) 1-2: Port 11, +3.3V source from hot-plug controller
W135	Header	2-3 Shunted	2-3: Port 12, +3.3V source base on W87 (Default) 1-2: Port 12, +3.3V source from hot-plug controller
W136	Header	2-3 Shunted	2-3: Port 13, +3.3V source base on W88 (Default) 1-2: Port 13, +3.3V source from hot-plug controller
W141	Header	2-3 Shunted	2-3: Port 14, +3.3V source base on W91 (Default) 1-2: Port 14, +3.3V source from hot-plug controller
W142	Header	2-3 Shunted	2-3: Port 15, +3.3V source base on W92 (Default) 1-2: Port 15, +3.3V source from hot-plug controller

Table 2.17 Miscellaneous Jumpers, Headers (Part 4 of 4)

LEDs

There are several LED indicators on the EB64H16 which convey status feedback. A description of each is provided in Table 2.18.

Location	Color	Definition
DS87	Green	Port1: Power-is-good indicator
DS74	Green	Port2: Power-is-good indicator
DS73	Green	Port3: Power-is-good indicator
DS76	Green	Port4: Power-is-good indicator
DS75	Green	Port5: Power-is-good indicator
DS78	Green	Port6: Power-is-good indicator
DS77	Green	Port7: Power-is-good indicator
DS80	Green	Port8: Power-is-good indicator
DS79	Green	Port9: Power-is-good indicator
DS82	Green	Port10: Power-is-good indicator
DS81	Green	Port11: Power-is-good indicator
DS84	Green	Port12: Power-is-good indicator
DS83	Green	Port13: Power-is-good indicator
DS86	Green	Port14: Power-is-good indicator
DS85	Green	Port15: Power-is-good indicator
DS9	Yellow	Port1: Attention Indicator
DS4	Yellow	Port2: Attention Indicator
DS5	Yellow	Port3: Attention Indicator

Table 2.18 LED Indicators (Part 1 of 3)

Notes

Location	Color	Definition
DS6	Yellow	Port4: Attention Indicator
DS7	Yellow	Port5: Attention Indicator
DS8	Yellow	Port6: Attention Indicator
DS11	Yellow	Port7: Attention Indicator
DS12	Yellow	Port8: Attention Indicator
DS13	Yellow	Port9: Attention Indicator
DS14	Yellow	Port10: Attention Indicator
DS15	Yellow	Port11: Attention Indicator
DS16	Yellow	Port12: Attention Indicator
DS17	Yellow	Port13: Attention Indicator
DS18	Yellow	Port14: Attention Indicator
DS19	Yellow	Port15: Attention Indicator
DS10	Green	Port1: Power Indicator
DS20	Green	Port2: Power Indicator
DS21	Green	Port3: Power Indicator
DS22	Green	Port4: Power Indicator
DS23	Green	Port5: Power Indicator
DS24	Green	Port6: Power Indicator
DS25	Green	Port7: Power Indicator
DS26	Green	Port8: Power Indicator
DS27	Green	Port9: Power Indicator
DS28	Green	Port10: Power Indicator
DS29	Green	Port11: Power Indicator
DS30	Green	Port12: Power Indicator
DS31	Green	Port13: Power Indicator
DS32	Green	Port14: Power Indicator
DS33	Green	Port15: Power Indicator
DS3	Green	Port0: Active Status Output
DS50	Green	Port1: Active Status Output
DS51	Green	Port2: Active Status Output
DS52	Green	Port3: Active Status Output
DS53	Green	Port4: Active Status Output
DS54	Green	Port5: Active Status Output
DS55	Green	Port6: Active Status Output
DS56	Green	Port7: Active Status Output
DS57	Green	Port8: Active Status Output
DS58	Green	Port9: Active Status Output

Table 2.18 LED Indicators (Part 2 of 3)

Notes

Location	Color	Definition
DS59	Green	Port10: Active Status Output
DS60	Green	Port11: Active Status Output
DS61	Green	Port12: Active Status Output
DS62	Green	Port13: Active Status Output
DS63	Green	Port14: Active Status Output
DS64	Green	Port15: Active Status Output
DS42	Green	Port0: Link Up Status Output
DS43	Green	Port1: Link Up Status Output
DS44	Green	Port2: Link Up Status Output
DS45	Green	Port3: Link Up Status Output
DS46	Green	Port4: Link Up Status Output
DS34	Green	Port5: Link Up Status Output
DS35	Green	Port6: Link Up Status Output
DS36	Green	Port7: Link Up Status Output
DS37	Green	Port8: Link Up Status Output
DS38	Green	Port9: Link Up Status Output
DS39	Green	Port10: Link Up Status Output
DS40	Green	Port11: Link Up Status Output
DS41	Green	Port12: Link Up Status Output
DS47	Green	Port13: Link Up Status Output
DS48	Green	Port14: Link Up Status Output
DS49	Green	Port15: Link Up Status Output
DS65	Red	Hot Plug Controller1: Power Fault Indicator
DS66	Red	Hot Plug Controller2: Power Fault Indicator
DS67	Red	Hot Plug Controller3: Power Fault Indicator
DS68	Red	Hot Plug Controller4: Power Fault Indicator
DS69	Red	Hot Plug Controller5: Power Fault Indicator
DS70	Red	Hot Plug Controller6: Power Fault Indicator
DS71	Red	Hot Plug Controller7: Power Fault Indicator
DS72	Red	Hot Plug Controller8: Power Fault Indicator
DS2	Green	Board Power Indicator (3.3V)
DS1	Red	Board Reset Indicator

Table 2.18 LED Indicators (Part 3 of 3)

Notes

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved

Table 2.19 PCI Express x16 Connector Pinout (Part 1 of 3)

Notes

Pin	Side A		Side B	
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground
50	PETp8	Transmitter differential	RSVD	Reserved
51	PETn8	pair, Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential
53	GND	Ground	PERn8	pair, Lane 8
54	PETp9	Transmitter differential	GND	Ground
55	PETn9	pair, Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential
57	GND	Ground	PERn9	pair, Lane 9
58	PETp10	Transmitter differential	GND	Ground
59	PETn10	pair, Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential
61	GND	Ground	PERn10	pair, Lane 10
62	PETp11	Transmitter differential	GND	Ground
63	PETn11	pair, Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential
65	GND	Ground	PERn11	pair, Lane 11
66	PETp12	Transmitter differential	GND	Ground
67	PETn12	pair, Lane 12	GND	Ground
68	GND	Ground	PERp12	Receiver differential
69	GND	Ground	PERn12	pair, Lane 12
70	PETp13	Transmitter differential	GND	Ground

Table 2.19 PCI Express x16 Connector Pinout (Part 2 of 3)

Notes

Pin	Side A		Side B	
71	PETn13	pair, Lane 13	GND	Ground
72	GND	Ground	PERp13	Receiver differential
73	GND	Ground	PERn13	pair, Lane 13
74	PETp14	Transmitter differential	GND	Ground
75	PETn14	pair, Lane 14	GND	Ground
76	GND	Ground	PERp14	Receiver differential
77	GND	Ground	PERn14	pair, Lane 14
78	PETp15	Transmitter differential	GND	Ground
79	PETn15	pair, Lane 15	GND	Ground
80	GND	Ground	PERp15	Receiver differential
81	PRSNT2#	Hot-Plug presence detect	PERn15	pair, Lane 15
82	RSVD	Reserved	GND	Ground

Table 2.19 PCI Express x16 Connector Pinout (Part 3 of 3)

Note: These x16 PCI Express connectors comply with the PCIe specification. However, the downstream ports on the EB64H16 are electronically connected in either a x8 configuration (ports 2, 4, 6, 8, 10, 12, and 14) or a x4 configuration (ports 1 through 15).

PCI Express Personality Module

The PES64H16 supports port merging in a static manner during a fundamental reset. A PCI Express personality module is used in the EB64H16 to merge two consecutive x4 even and odd ports into a single x8 port, e.g., ports 0 and 1, ports 2 and 3, etc., finishing with ports 14 and 15. When side 1 of the personality module is inserted into the personality module connector (see Table 2.20 below for connector locations), four PCI Express lanes are routed to each port. When side 2 of the personality module is inserted into the personality module connector, eight PCI Express lanes are routed to the even port and the odd port is disconnected. Note that all eight connectors must have a personality module inserted, whether all side 1, all side 2, or a combination. If all eight personality module cards have side 1 plugged in, all 16 ports are in use. If all cards have side 2 plugged in, only 8 ports are in use.

Merged Ports	Personality Module Location
0/1	J7
2/3	J9
4/5	J10
6/7	J11
8/9	J12
10/11	J13
12/13	J14
14/15	J15

Table 2.20 PES64H16 Personality Module Locations

EB64H16 Evaluation Board Block Diagram

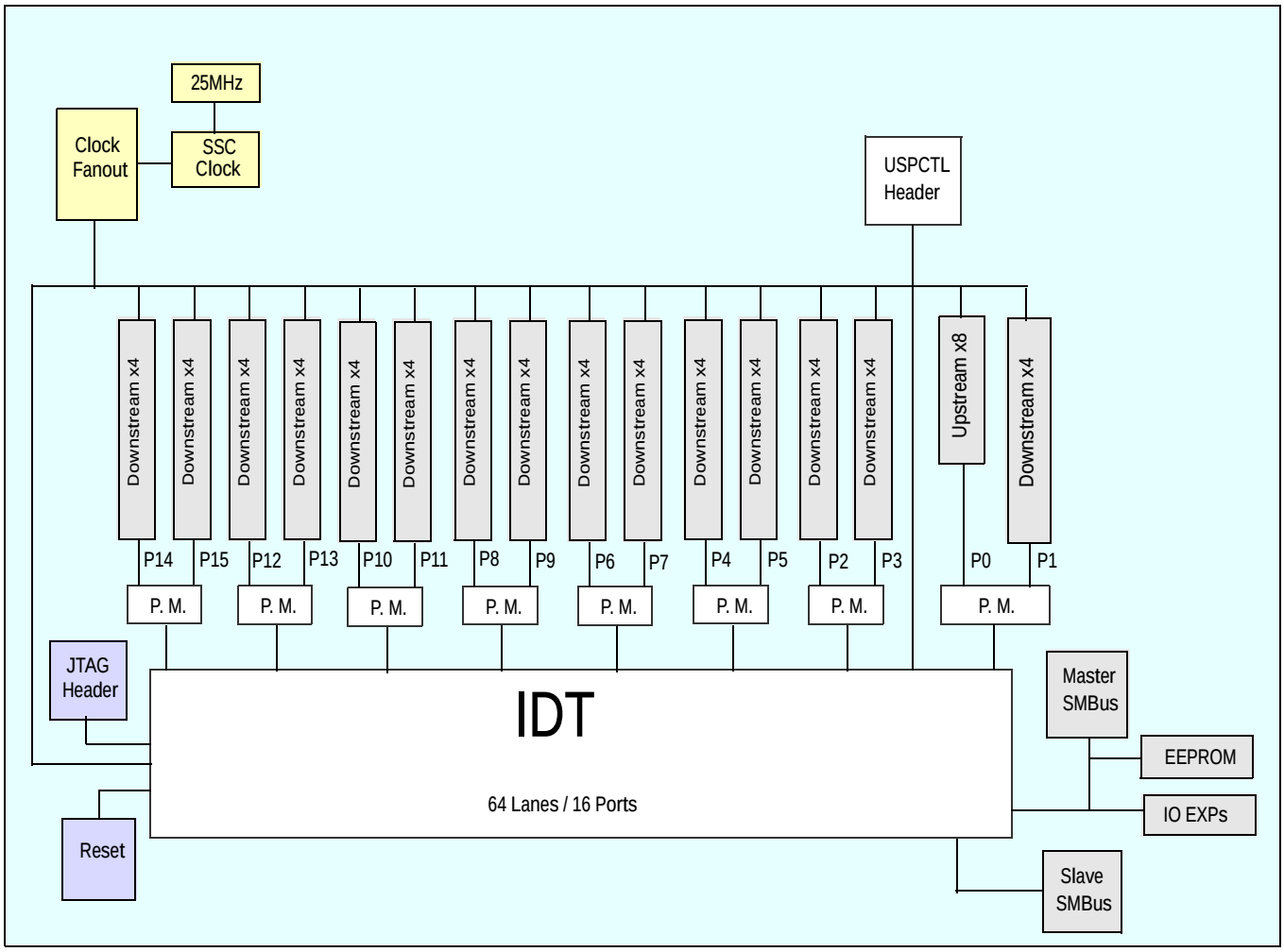

Figure 2.5 EB64H16 Eval Board Block Diagram

EB48H12 / EB48T12 Evaluation Board Block Diagram

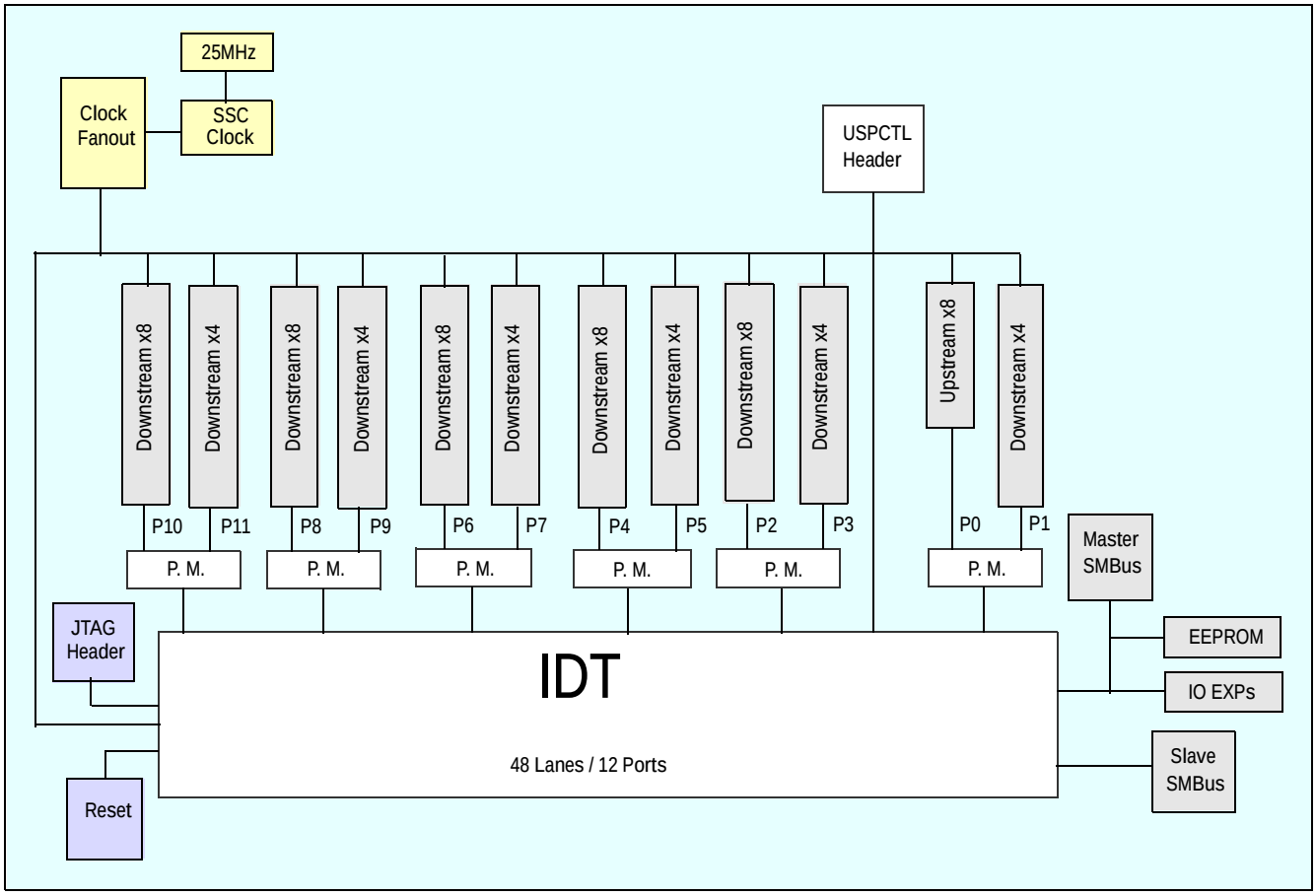

Figure 2.6 EB48H12 / EB48T12 Eval Board Block Diagram

Software for the EB64H16 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB64H16 evaluation board using the device management software. Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES64H16 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES64H16.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES64H16, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES64H16 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes

Schematics

Notes

Schematics

RENESAS

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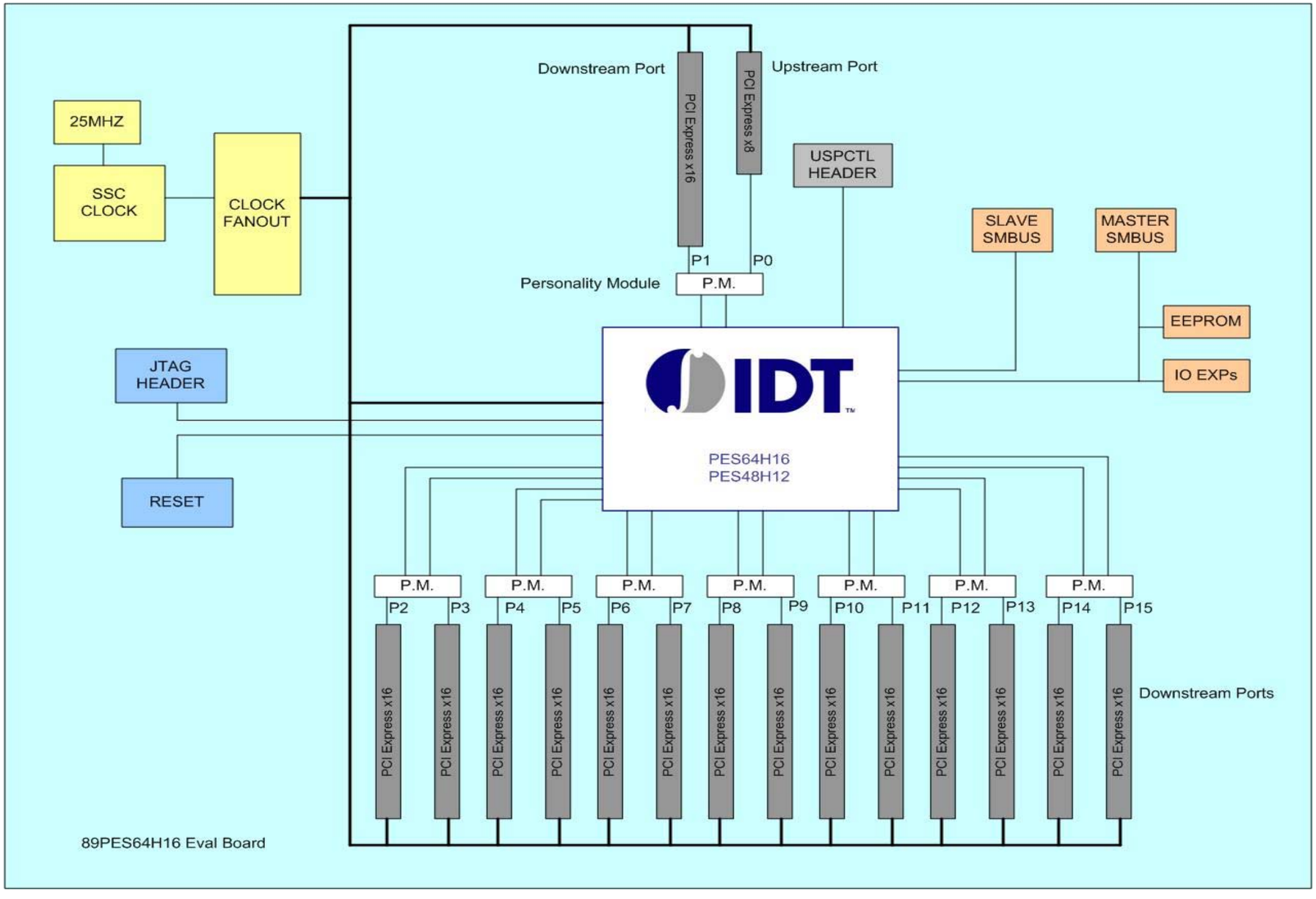
34	PORT 12/13 CONNECTORS
35	PORT 14/15 CONNECTORS
36	PES64H16 POWER
37	POWER DECOUPLING AND WAKE
38	PES64H16 SMBUS REFCLK

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0099R01	1.0	INITIAL RELEASE	2007-02-06	J.CARRILLO

TITLE: 89HPES64H16 EVALUATION BOARD 89EBPES64H16			
SIZE: B	DRAWING NO.: STGSCH-00100	FAB P/N: 18-624-000	REV.: 1.0
AUTHOR: J.CARRILLO		CHECKED BY: B.OH	
Tue Feb 06 09:21:38 2007		SHEET 1 OF 38	

BLOCK DIAGRAM



TITLE 89EBPES64H16 BLOCK DIAGRAM			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:29:18 2007		SHEET 2 OF 38	

RENESAS

J5
44472-0853
POWER 8-PIN
GND1 P12V11
GND2 P12V12
GND3 P12V21
GND4 P12V22
12V1
12V2
W100
W156
22UF C35 25V
10UF C37 25V
10UF C39 25V
10UF C40 25V
22UF C41 25V
330UF C42 16V
22UF C43 25V
10UF C44 25V
10UF C45 25V
10UF C46 25V
22UF C52 25V
330UF C54 16V

POWER INDICATOR
PLACE NEAR TOP EDGE
LABEL 'POWER'

3_3V
R14 330 5%
DS2 GRN

TP1

BOARD RESET
S1 PB_SW
R1 10K 5%
R5 10K 5%
R10 10K 5%
W1
S_PERSTN
OUT 28 29 30 31 32 33 34 38

U4
TLC77333D
RESINN VCC
SENSE RESET
CONTROL RESETN
CT GND
RED DS1
R147 330 5%
C13 47UF 10V

P0_PERST*
28 IN
U2
OE* VCC
A
GND Y
SN74LVC1G125
C12 1.0UF
C452 0.1UF

W19
S3
SPDT
ON COM
OFF
C56 0.1UF
C57 0.1UF
C58 0.1UF
C59 0.1UF
C60 0.1UF
C61 0.1UF
C62 0.1UF
C63 0.1UF
TP34

J6
44472-2453
POWER 24-pin
3V3_SNS PS_ON
P3V3_1 PWR_OK
P3V3_2 N12V
P3V3_3 N5V0
P5V0_VSB GND1
P5V0_1 GND2
P5V0_2 GND3
P5V0_3 GND4
P5V0_4 GND5
P5V0_5 GND6
P12V3_1 GND7
P12V3_2 GND8
W157
W158
W159

5_0V
12V3
C3 22UF 25V
C4 10UF 25V
C5 10UF 25V
C10 22UF 25V
C11 22UF 25V
C31 22UF 25V
C32 10UF 25V
C33 10UF 25V
C34 1UF 16V
C36 22UF 25V
C38 330UF 10V

FAN POWER
J35

VDDIO 3.3V
U17
MIC37502BU
EN VOUT
VIN ADJ
NC TAB GND
C321 47UF 6V
C322 0.1UF
R469 215 1%
R470 130 1%
C323 330UF 10V
TP35

12V3
TP16 TP17
U/S +12V -> +2.5V
+2.5V
U26
Vin VO_SEN+
Track Vout
SYNC
TURBOTRANS VO_SEN-
Inhibit GND2
Vo_Adj GND1
PTH08T240WAH
2.37K R144 1%
C279 22UF 25V
C280 330UF 16V
C281 47UF 10V
C282 220UF 10V

+2.5V
C19 0.1UF
C20 0.1UF
C21 0.1UF
C22 0.1UF
C23 0.1UF
C24 0.1UF
C25 0.1UF
C26 0.1UF

VDD_CORE 1.0V
+2.5V
U1
MIC49500WR
VIN VOUT
VBIAS
EN
NC ADJ/VSNS
TAB GND
C87 47UF 6V
C89 0.1UF
R18 0 0%
R9 100 1%
R17 130 1%
R19 100 1%
C96 330UF 10V
1_0VC

VDDPE 1.0V
+2.5V
U7
MIC49500WR
R30 0 0%
R23 100 1%
R28 130 1%
R33 100 1%
C101 47UF 6V
C103 0.1UF
C105 330UF 10V
1_0VA

VTT 1.5V
ECN # PCBECN-0026
SHORTS R20
U6
MIC49500WR
R20 0 0%
R12 150 1%
R13 130 1%
C88 47UF 6V
C90 0.1UF
C97 330UF 10V
1_5VA

VDDAPE 1.0V
ECN # PCBECN-0026
SHORTS R32
U28
MIC49500WR
R32 0 0%
R24 100 1%
R31 100 1%
R34 130 1%
C122 47UF 6V
C124 0.1UF
C107 330UF 10V
1_0VB

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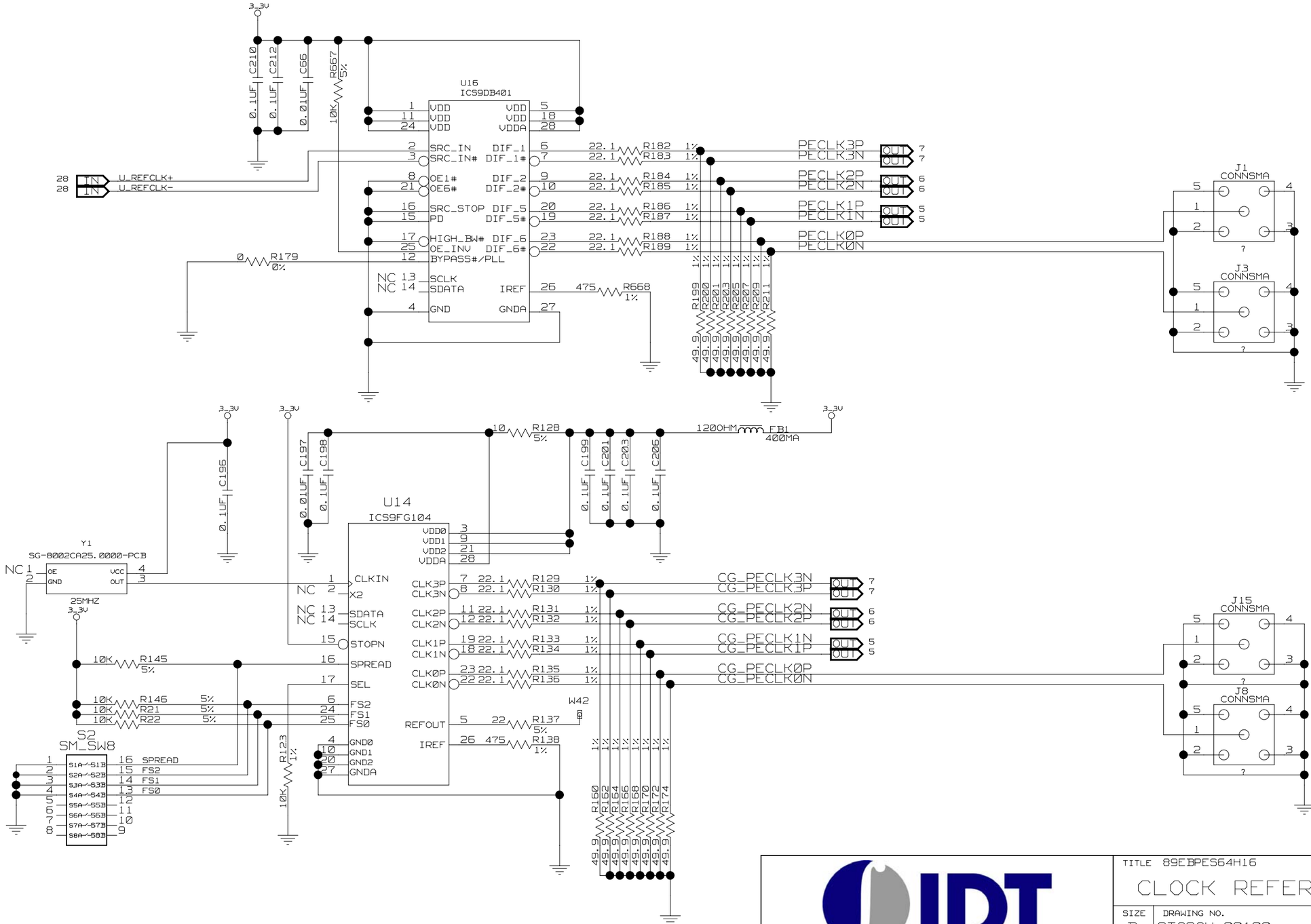
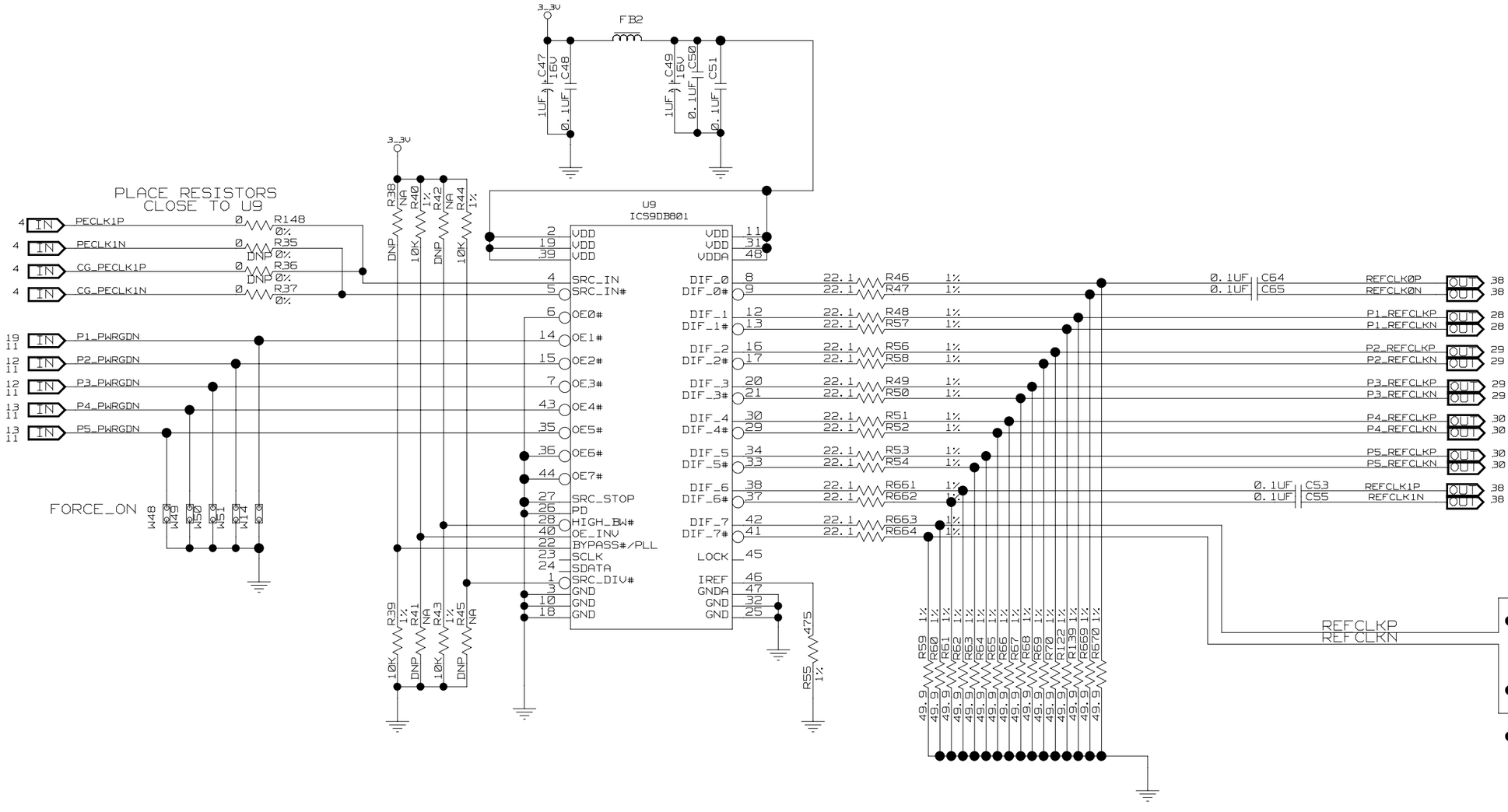
TITLE	89EBPES64H16
	POWER SUPPLY AND RESET
SIZE	B
DRAWING NO.	STGSCH-00100
FAB P/N	18-624-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Mon Feb 05 15:33:51 2007
	SHEET 3 OF 38

RENESAS



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC. 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT 2007	TITLE 89EBPES64H16 CLOCK REFERENCE
	SIZE B · DRAWING NO. STGSCH-00100 · FAB P/N 18-624-000 · REV. 1.0
	AUTHOR J. CARRILLO · CHECKED BY B. OH
	Mon Feb 05 15:33:52 2007 · SHEET 4 OF 38

RENESAS



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TITLE 89EBPES64H16

CLOCK DISTRIBUTION P1-5

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0

AUTHOR	CHECKED BY	
J. CARRILLO	B. OH	
Mon Feb 05 15:33:53 2007		SHEET 5 OF 38

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PLACE RESISTORS CLOSE TO U3

U3
ICS9DB801

FORCE_ON

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC. 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT 2007	TITLE 89EBPES64H16 CLOCK DISTRIBUTION P6-10	
	SIZE B / DRAWING NO. STGSCH-00100 / FAB P/N 18-624-000 / REV. 1.0	
	AUTHOR J. CARRILLO / CHECKED BY B. OH	
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PLACE RESISTORS CLOSE TO U5

FORCE_ON

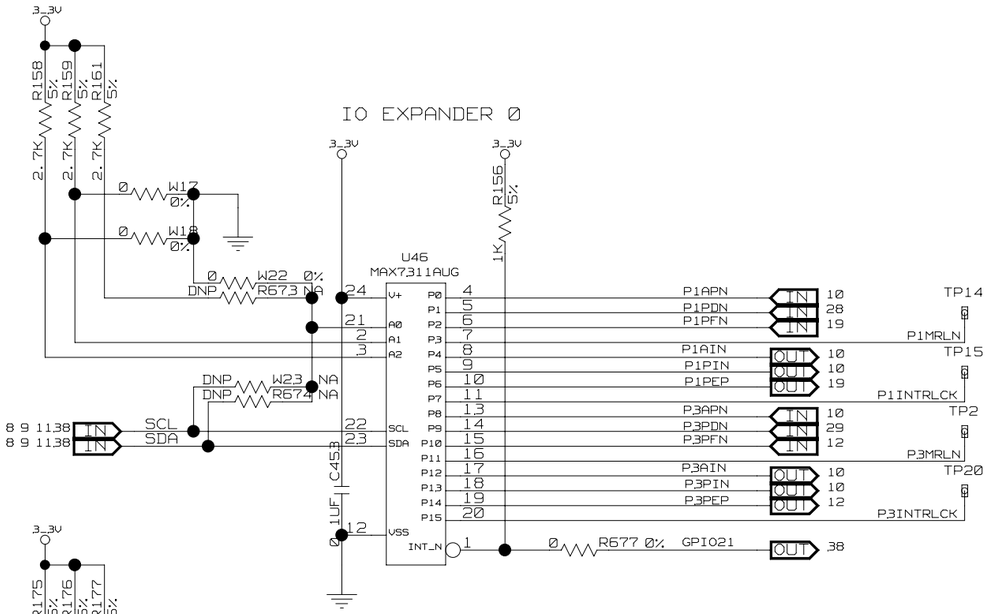
U5
ICS9DB801

IDT™

TITLE 89EBPES64H16			
CLOCK DISTRIBUTION P11-15			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:54 2007		SHEET 7 OF 38	

RENESAS

IO EXPANDER 0



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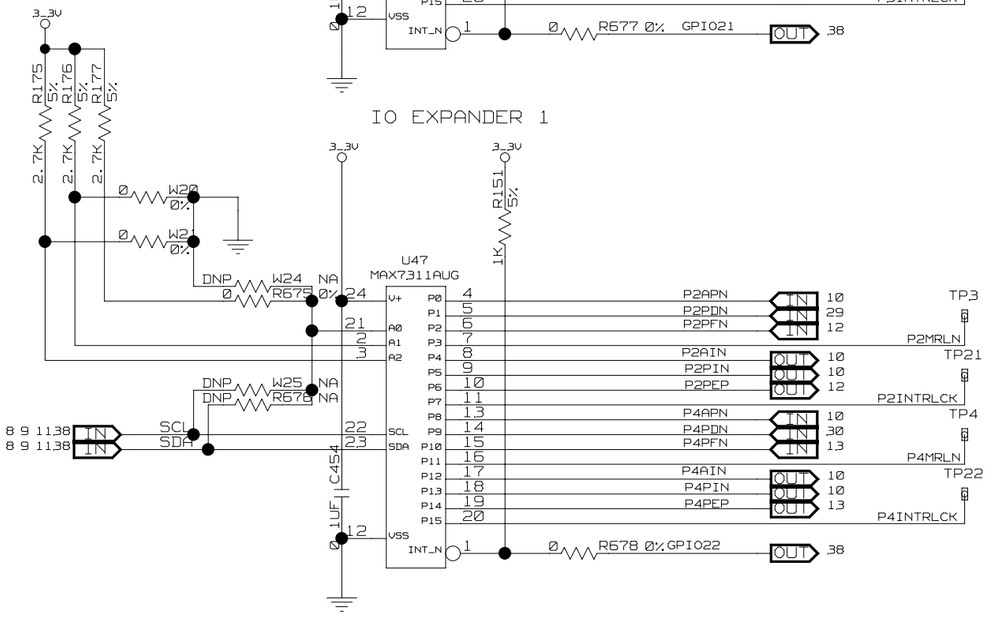

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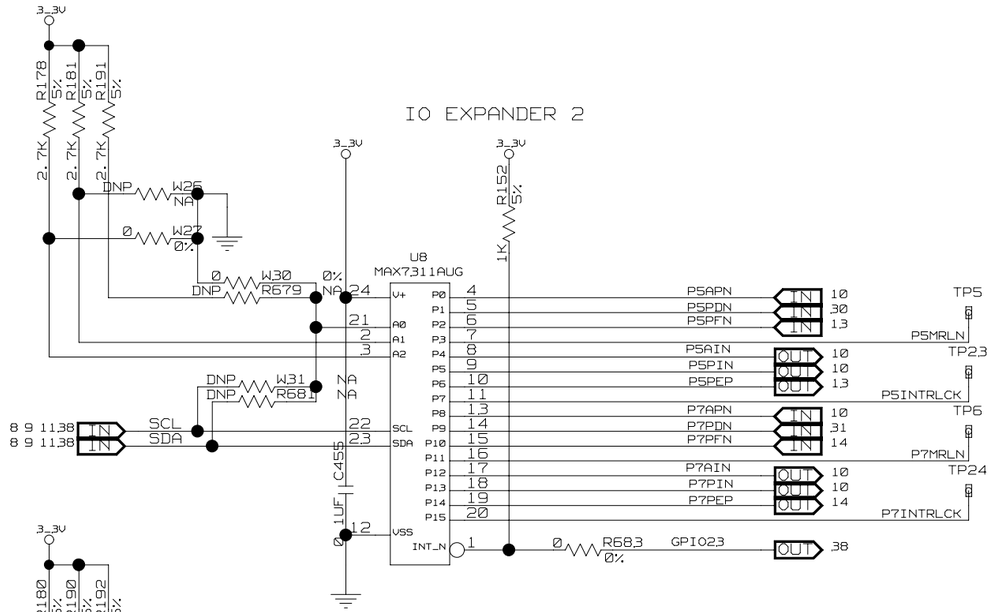

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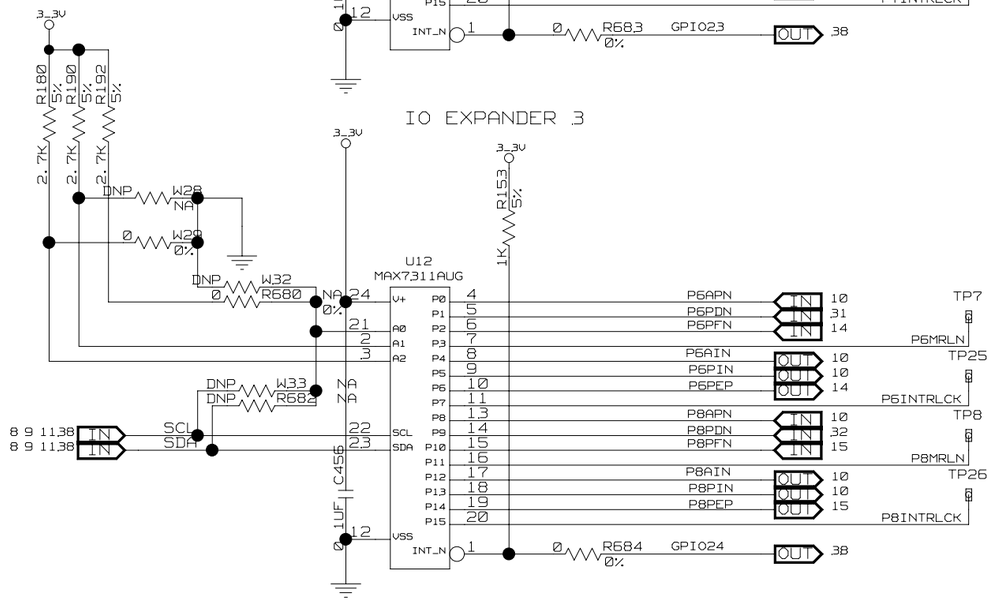


TITLE 89EBPES64H16

IO EXPANDER P1 - P8

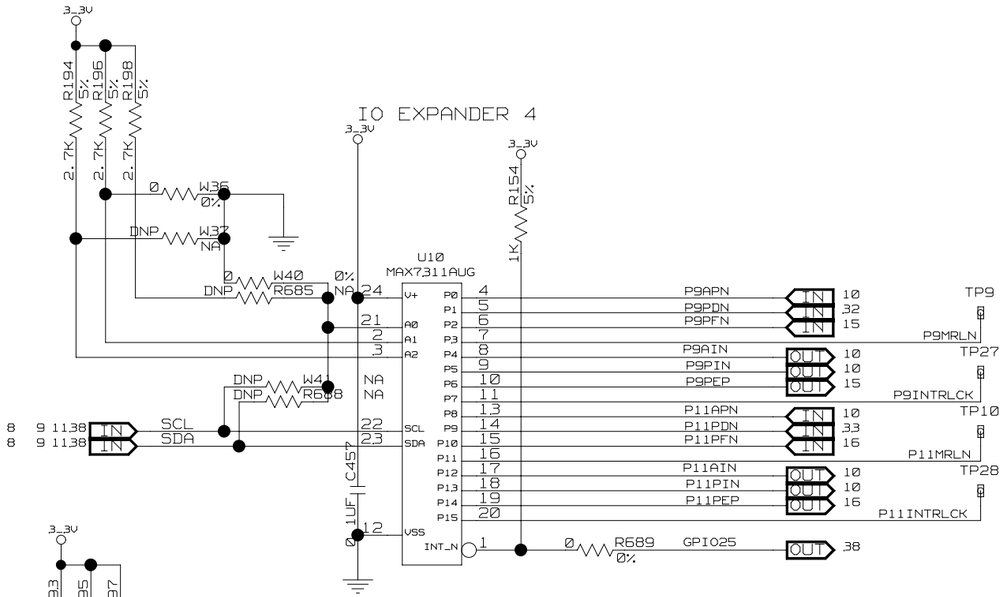
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO	B. OH

Mon Feb 05 15:33:55 2007 — SHEET 8 OF 38

RENESAS

IO EXPANDER 4



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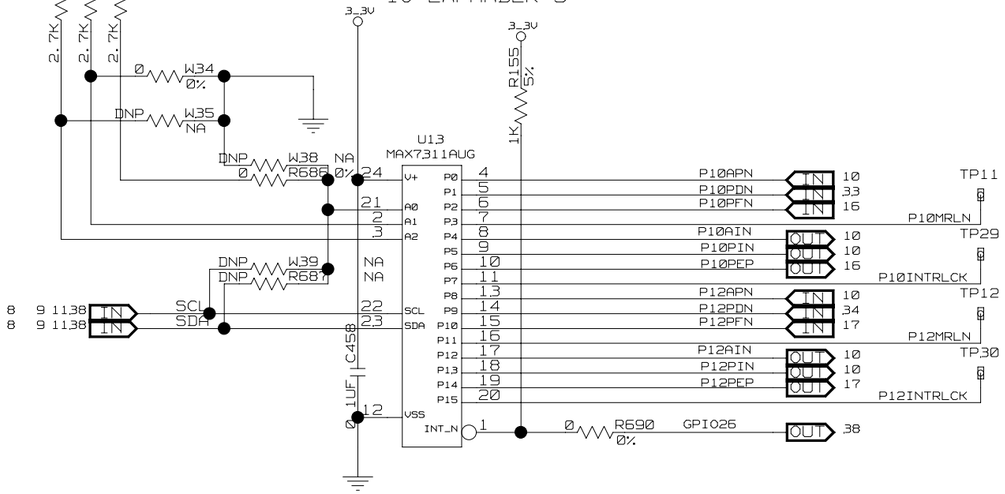

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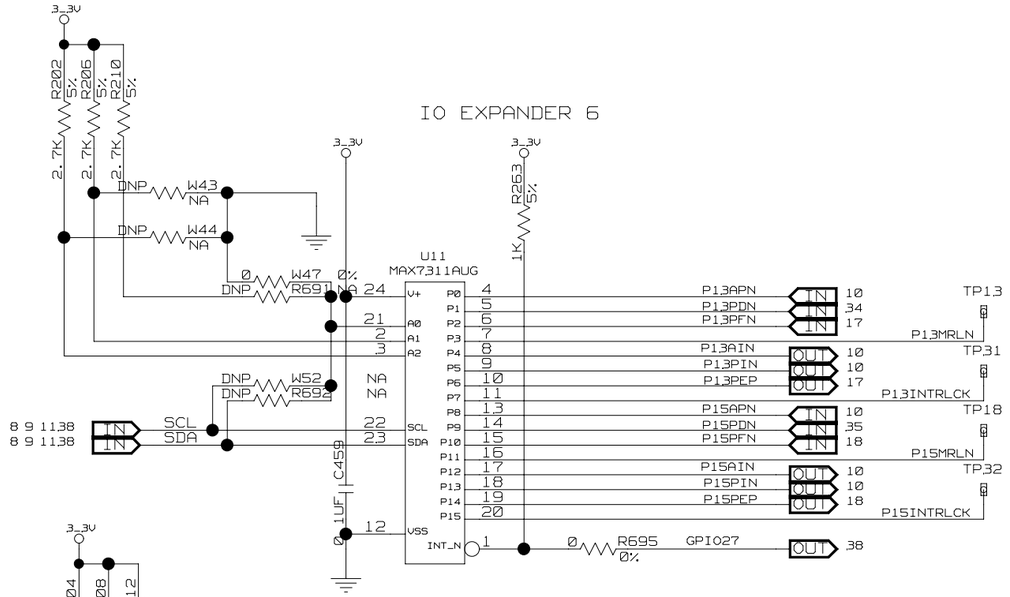

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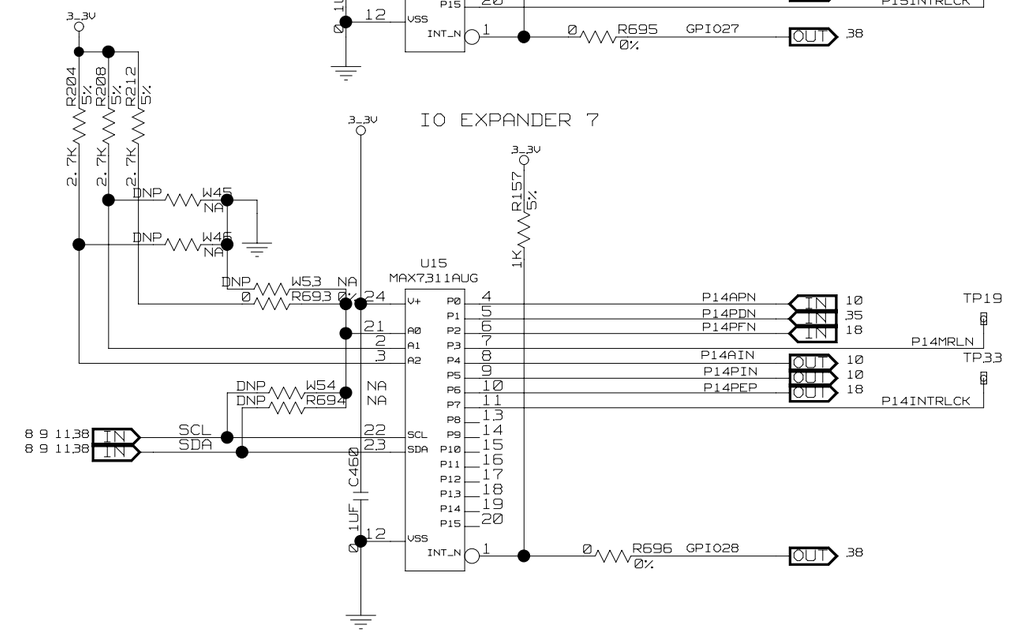

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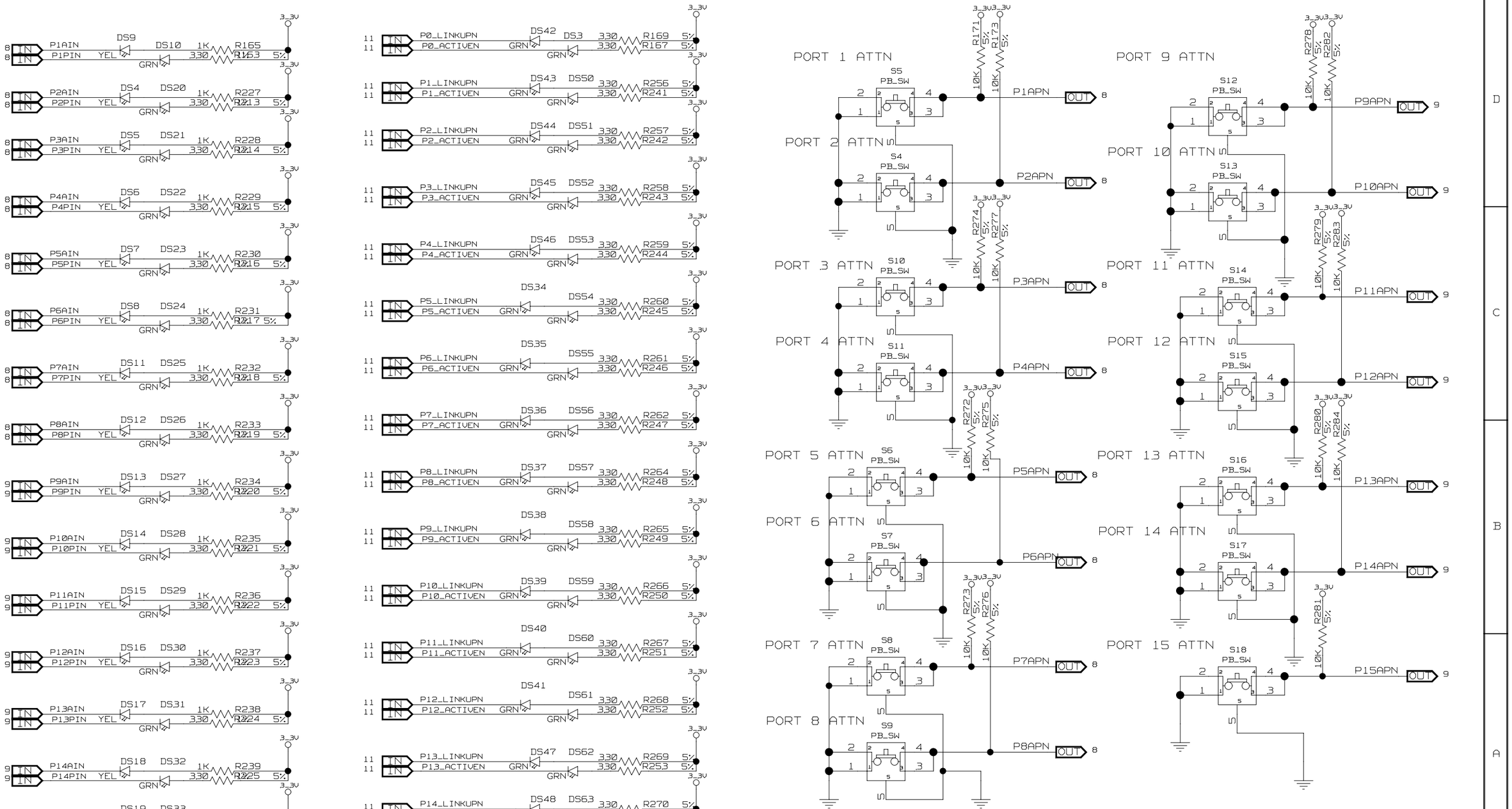
IO EXPANDER P9 - P15

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO	B. OH

Mon Feb 05 15:33:56 2007 — SHEET 9 OF 38

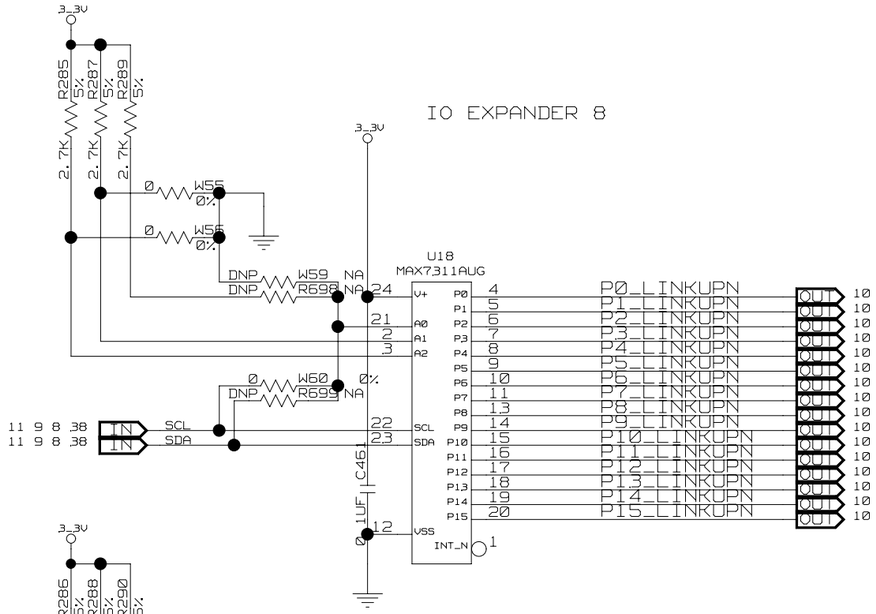
RENESAS



TITLE	89EBPES64H16 IO EXPANDER ATTN PB/LEDS		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:24 2007		SHEET 10 OF 38	

RENESAS

IO EXPANDER 8



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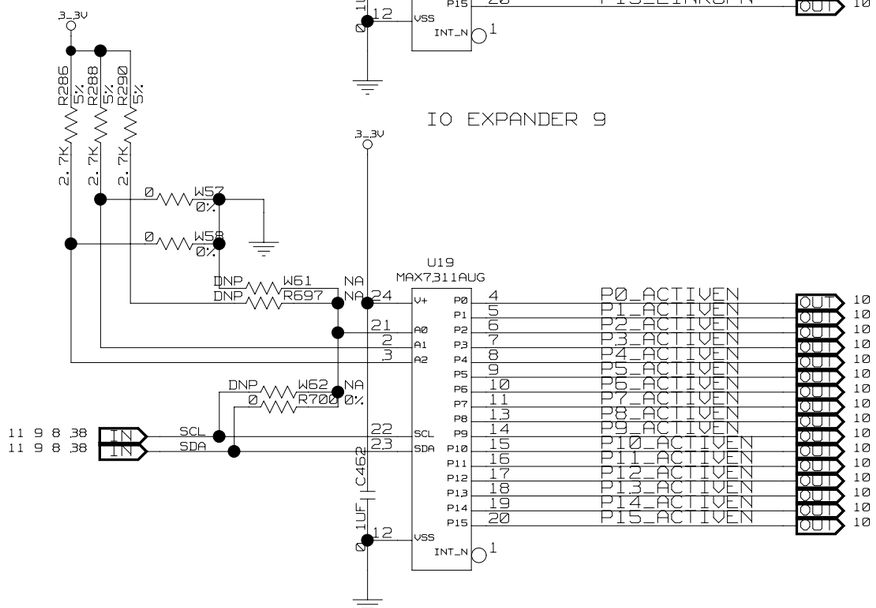

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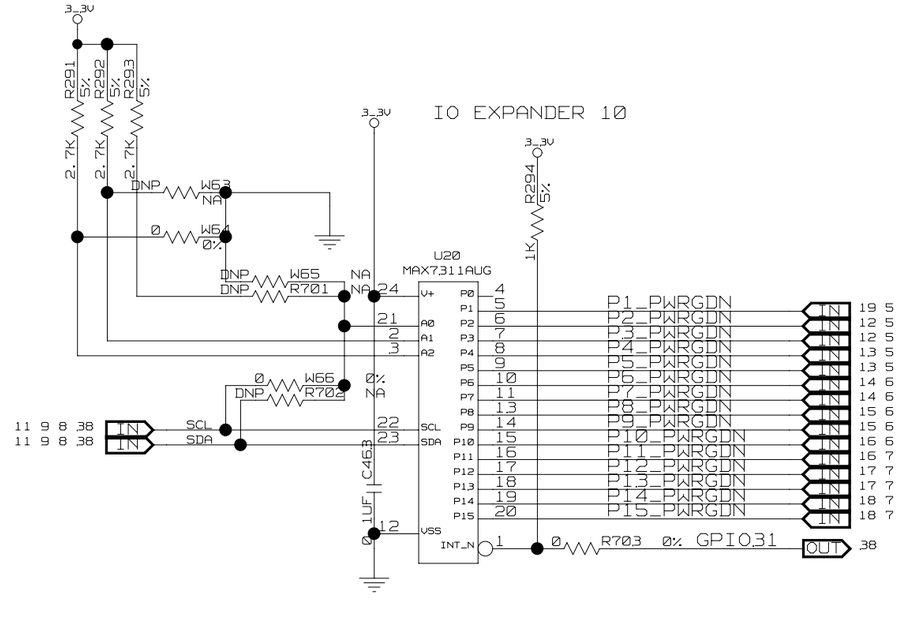
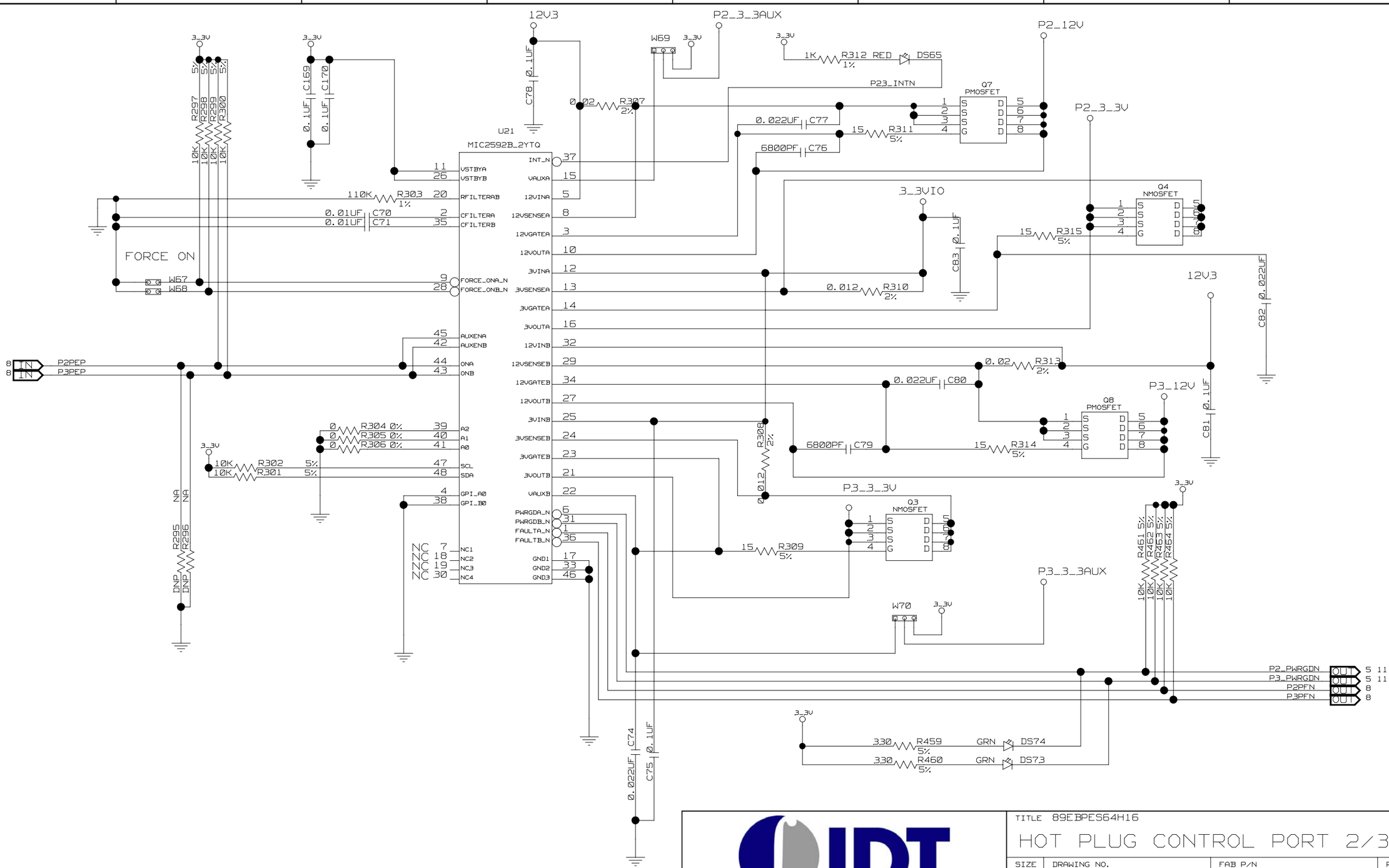


TITLE 89EBPES64H16			
IO EXPANDER LINK STATUS			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:25 2007		SHEET 11 OF 38	

RENESAS



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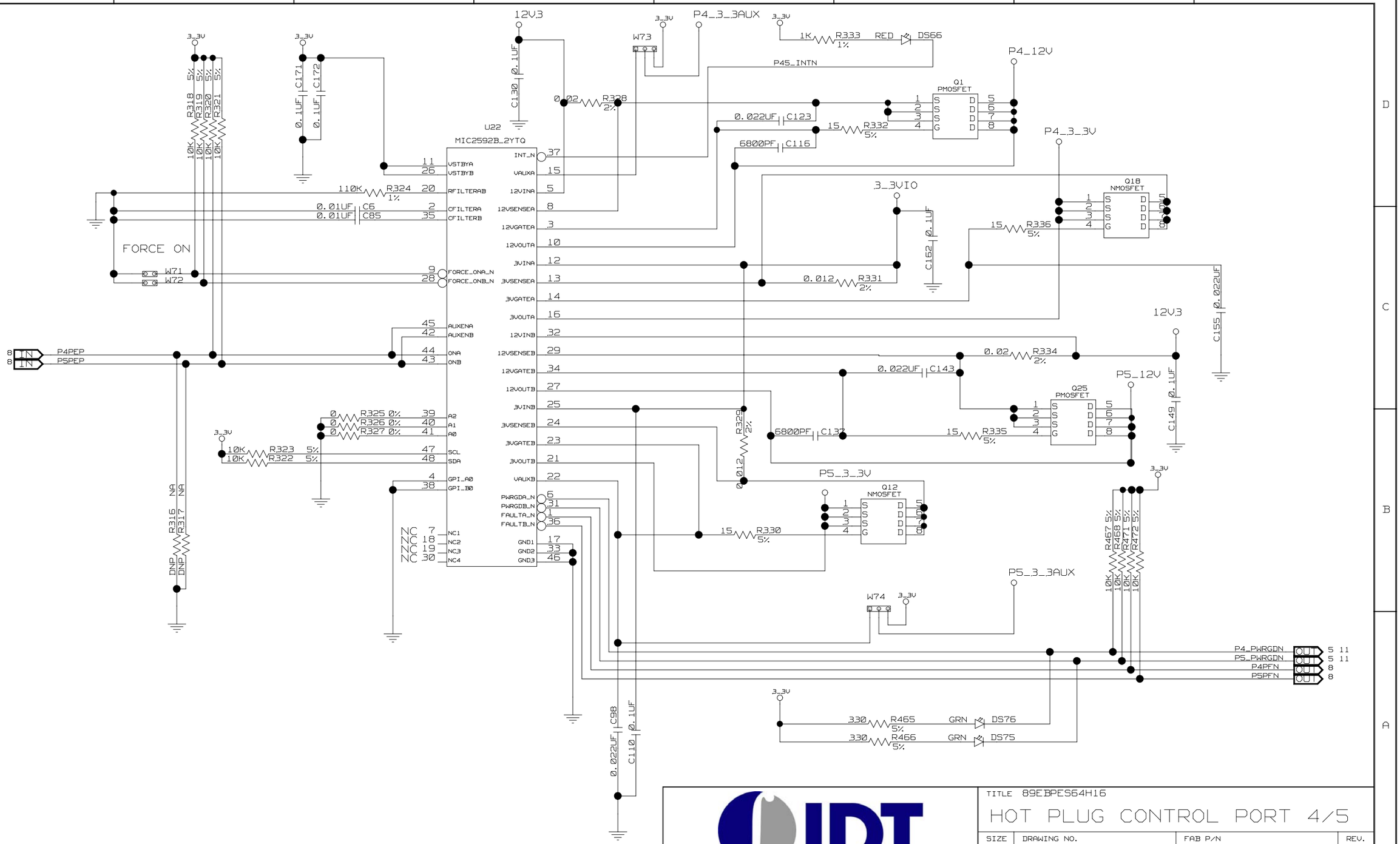
TITLE	89EBPES64H16
	HOT PLUG CONTROL PORT 2/3
SIZE	B
DRAWING NO.	STGSCH-00100
FAB P/N	18-624-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
Mon Feb 05 15:33:26 2007	SHEET 12 OF 38

RENESAS



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TITLE 89EBPES64H16 HOT PLUG CONTROL PORT 4/5			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:27 2007		SHEET 13 OF 38	

RENESAS

12V1
3_3V
P6_3_3AUX
P6_12V
P6_3_3V
3_3VIO
P7_12V
P7_3_3V
P7_3_3AUX
U23
MIC2592B_2YTQ
Q2 PMOSFET
Q19 NMOSFET
Q26 PMOSFET
Q13 NMOSFET
FORCE ON
W75
W76
W77
W78
P6PEP
P7PEP
DS67 RED
DS78 GRN
DS77 GRN
P67_INTN
P6_PWRGDN
P7_PWRGDN
P6PFN
P7PFN

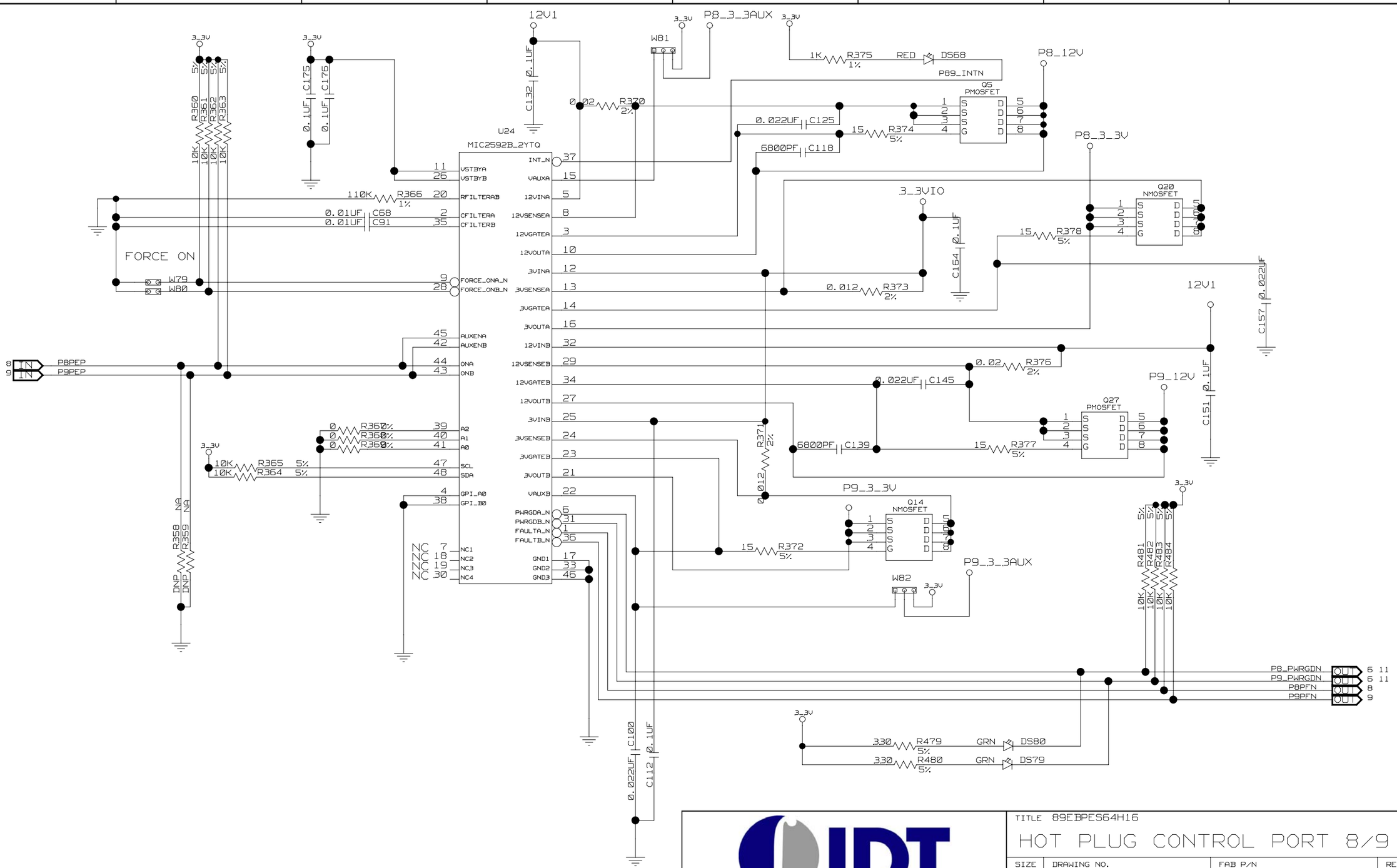
TITLE 89EBPES64H16
HOT PLUG CONTROL PORT 6/7

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO	B. OH

Mon Feb 05 15:33:28 2007 SHEET 14 OF 38

RENESAS



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TITLE 89EBPES64H16 HOT PLUG CONTROL PORT 8/9			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:29 2007		SHEET 15 OF 38	

RENESAS

12V1
3_3V
P10_3_3AUX
P10_12V
P10_3_3V
3_3VIO
12V2
P11_12V
P11_3_3V
P11_3_3AUX
U25
MIC2592B_2YTQ
INT_N
VAUXA
12VINA
12VSENSEA
12VGATEA
12VOUTA
3VINA
3VSENSEA
3VGATEA
3VOUTA
12VINB
12VSENSEB
12VGATEB
12VOUTB
3VINB
3VSENSEB
3VGATEB
3VOUTB
VAUXB
PWRGDA_N
PWRGDB_N
FAULTA_N
FAULTB_N
GND1
GND2
GND3
VSTBYA
VSTBYB
RFILTERAB
CFILTERA
CFILTERB
FORCE_ONA_N
FORCE_ONB_N
AUXENA
AUXENB
ONA
ONB
A2
A1
A0
SCL
SDA
GPI_A0
GPI_B0
NC1
NC2
NC3
NC4
W83
W84
W85
W86
FORCE ON
P10PEP
P11PEP
R381 10K 5%
R382 10K 5%
R383 10K 5%
R384 10K 5%
R385 10K 5%
R386 10K 5%
R387 110K 1%
R388 0 0%
R389 0 0%
R390 0 0%
R391 0.02 2%
R392 0.012 2%
R393 15 5%
R394 0.012 2%
R395 15 5%
R396 1K 1% RED
R397 0.02 2%
R398 15 5%
R399 15 5%
R379 NA
R380 DNP
R485 330 5% GRN
R486 330 5% GRN
R487 10K 5%
R488 10K 5%
R489 10K 5%
R490 10K 5%
C69 0.01UF
C92 0.01UF
C177 0.1UF
C178 0.1UF
C133 0.1UF
C126 0.022UF
C119 6800PF
C165 0.1UF
C158 0.022UF
C146 0.022UF
C140 6800PF
C152 0.1UF
C105 0.022UF
C113 0.1UF
Q5 PMOSFET
Q21 NMOSFET
Q28 PMOSFET
Q15 NMOSFET
DS69
DS82
DS81
P10_PWRGDN
P11_PWRGDN
P10PFN
P11PFN

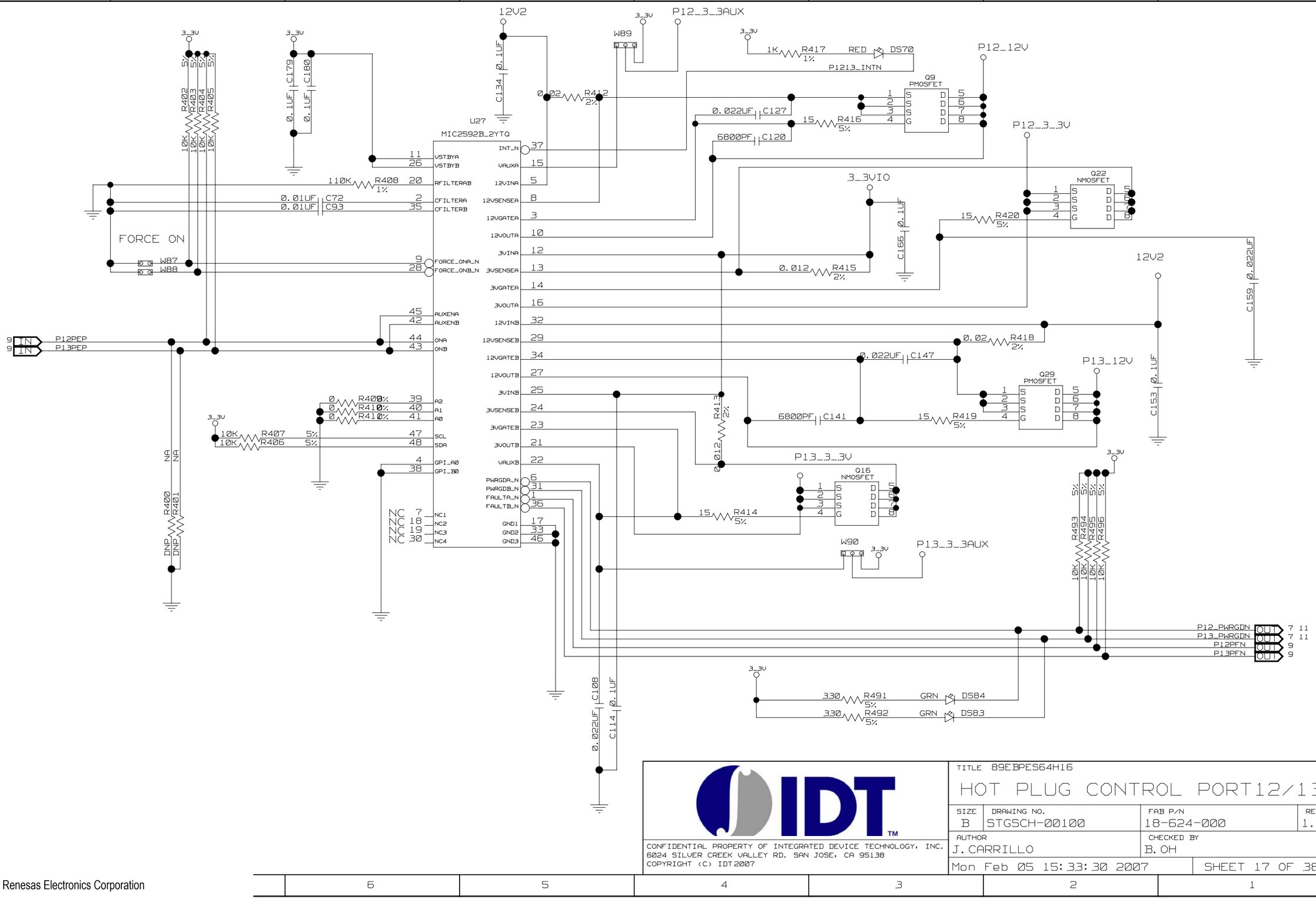
TITLE 89EBPES64H16
HOT PLUG CONTROL PORT10/11

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO	B. OH

Mon Feb 05 15:33:30 2007 | SHEET 16 OF 38

RENESAS



TITLE	89EBPES64H16
	HOT PLUG CONTROL PORT12/13
SIZE	B
DRAWING NO.	STGSCH-00100
FAB P/N	18-624-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Mon Feb 05 15:33:30 2007
	SHEET 17 OF 38

RENESAS

12V2
3_3V
P14_3_3AUX
P14_12V
P14_3_3V
3_3VIO
P15_12V
P15_3_3V
P15_3_3AUX
U29
MIC2592B_2YTQ
FORCE ON
W91
W92
W93
W94
P14PEP
P15PEP
P14PFN
P15PFN
P14_PWRGDN
P15_PWRGDN
P1415_INTN
RED
DS71
GRN
DS86
DS85
Q10 PMOSFET
Q30 PMOSFET
Q23 NMOSFET
Q17 NMOSFET
R423 10K 5%
R424 10K 5%
R425 10K 5%
R426 10K 5%
R421 DNP
R422 DNP
R427 10K 5%
R428 10K 5%
R429 110K 1%
R430 0 0%
R431 0 0%
R432 0 0%
R433 0.02 2%
R434 0.012 2%
R435 15 5%
R436 0.012 2%
R437 15 5%
R438 1K 1%
R439 0.02 2%
R440 15 5%
R441 15 5%
R497 330 5%
R498 330 5%
R499 10K 5%
R500 10K 5%
R501 10K 5%
R502 10K 5%
C73 0.01UF
C94 0.01UF
C109 0.022UF
C115 0.1UF
C121 6800PF
C128 0.022UF
C135 0.1UF
C142 6800PF
C148 0.022UF
C154 0.1UF
C160 0.022UF
C167 0.1UF
C181 0.1UF
C182 0.1UF

TITLE	89EBPES64H16 HOT PLUG CONTROL PORT14/15
SIZE	B
DRAWING NO.	STGSCH-00100
FAB P/N	18-624-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Mon Feb 05 15:33:31 2007
	SHEET 18 OF 38

RENESAS

12V3
3_3V
P1_3_3AUX
P1_12V
P1_3_3V
3_3VIO
U30
MIC2592B_2YTQ
FORCE ON
P1PEP
P1_INTN
P1_PWRGDN
P1PFN
Q11 PMOSFET
Q24 NMOSFET
DS72 RED
DS87 GRN
R444 10K 5%
R445 10K 5%
R446 10K 5%
R447 10K 5%
R442 DNP
R443 DNP
R448 10K 5%
R449 10K 5%
R450 110K 1%
R451 0 0%
R452 0 0%
R453 0 0%
R454 0.02 2%
R455 0.012 2%
R456 15 5%
R457 1K 1%
R458 15 5%
R503 330 5%
R504 10K 5%
R505 10K 5%
C135 0.1UF
C183 0.1UF
C184 0.1UF
C129 0.022UF
C122 6800PF
C168 0.1UF
C151 0.022UF
C84 0.01UF
C95 0.01UF
W95
W96
W97
NA
NA
VSTBYA
VSTBYB
RFILTERAB
CFILTERA
CFILTERB
FORCE_ONA_N
FORCE_ONB_N
AUXENA
AUXENB
ONA
ONB
SCL
SDA
GPI_A0
GPI_B0
A2
A1
A0
NC1
NC2
NC3
NC4
INT_N
VAUXA
12VINA
12VSENSEA
12VGATEA
12VOUTA
3VINA
3VSENSEA
3VGATEA
3VOUTA
12VINB
12VSENSEB
12VGATEB
12VOUTB
3VINB
3VSENSEB
3VGATEB
3VOUTB
VAUXB
PWRGDA_N
PWRGDB_N
FAULTA_N
FAULTB_N
GND1
GND2
GND3

TITLE	89EBPES64H16 HOT PLUG CONTROL PORT 1
SIZE	B
DRAWING NO.	STGSCH-00100
FAB P/N	18-624-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Mon Feb 05 15:33:32 2007
	SHEET 19 OF 38

RENESAS

J7

MM50-200B1-1E

P0_PETP0 P0_PETN0 P0_PERP0 P0_PERN0 P0_PETP1 P0_PETN1 P0_PERP1 P0_PERN1 P0_PETP2 P0_PETN2 P0_PERP2 P0_PERN2 P0_PETP3 P0_PETN3 P0_PERP3 P0_PERN3 P0_PETP4 P0_PETN4 P0_PERP4 P0_PERN4 P0_PETP5 P0_PETN5 P0_PERP5 P0_PERN5 P0_PETP6 P0_PETN6 P0_PERP6 P0_PERN6 P0_PETP7 P0_PETN7 P0_PERP7 P0_PERN7

P1_PETP0 P1_PETN0 P1_PERP0 P1_PERN0 P1_PETP1 P1_PETN1 P1_PERP1 P1_PERN1 P1_PETP2 P1_PETN2 P1_PERP2 P1_PERN2 P1_PETP3 P1_PETN3 P1_PERP3 P1_PERN3

S00_PETP0 S00_PETN0 S00_PERP0 S00_PERN0 S00_PETP1 S00_PETN1 S00_PERP1 S00_PERN1 S00_PETP2 S00_PETN2 S00_PERP2 S00_PERN2 S00_PETP3 S00_PETN3 S00_PERP3 S00_PERN3 S00_PETP4 S00_PETN4 S00_PERP4 S00_PERN4 S00_PETP5 S00_PETN5 S00_PERP5 S00_PERN5 S00_PETP6 S00_PETN6 S00_PERP6 S00_PERN6 S00_PETP7 S00_PETN7 S00_PERP7 S00_PERN7

R645 10K 5%

P01MERGE OUT 38

U31
89HPES64H16XXBR

S00_PERP0	T31	PE00RP0	PE00TP0	T34	0.1UF	C185	S00_PETP0	
S00_PERN0	T30	PE00RN0	PE00TN0	T33	0.1UF	C193	S00_PETN0	
S00_PERP1	R31	PE00RP1	PE00TP1	R34	0.1UF	C186	S00_PETP1	
S00_PERN1	R30	PE00RN1	PE00TN1	R33	0.1UF	C194	S00_PETN1	
S00_PERP2	N31	PE00RP2	PE00TP2	N34	0.1UF	C187	S00_PETP2	
S00_PERN2	N30	PE00RN2	PE00TN2	N33	0.1UF	C195	S00_PETN2	
S00_PERP3	M31	PE00RP3	PE00TP3	M34	0.1UF	C188	S00_PETP3	
S00_PERN3	M30	PE00RN3	PE00TN3	M33	0.1UF	C200	S00_PETN3	
		3 of 16						
S00_PERP4	K31	PE01RP0	PE01TP0	K34	0.1UF	C189	S00_PETP4	
S00_PERN4	K30	PE01RN0	PE01TN0	K33	0.1UF	C202	S00_PETN4	
S00_PERP5	J31	PE01RP1	PE01TP1	J34	0.1UF	C190	S00_PETP5	
S00_PERN5	J30	PE01RN1	PE01TN1	J33	0.1UF	C204	S00_PETN5	
S00_PERP6	G31	PE01RP2	PE01TP2	G34	0.1UF	C191	S00_PETP6	
S00_PERN6	G30	PE01RN2	PE01TN2	G33	0.1UF	C205	S00_PETN6	
S00_PERP7	F31	PE01RP3	PE01TP3	F34	0.1UF	C192	S00_PETP7	
S00_PERN7	F30	PE01RN3	PE01TN3	F33	0.1UF	C207	S00_PETN7	

IDT™

TITLE 89EBPES64H16			
PM PORT 0/1			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:32 2007		SHEET 20 OF 38	

RENESAS

J9

MM50-200B1-1E

P2.3MERGE

U31
89HPES64H16XXBR
4 of 16

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TITLE 89EBPES64H16 PM PORT 2/3			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:33 2007		SHEET 21 OF 38	

RENESAS

J10

MM50-200B1-1E

P45MERGE

U31
89HPES64H16XXBR

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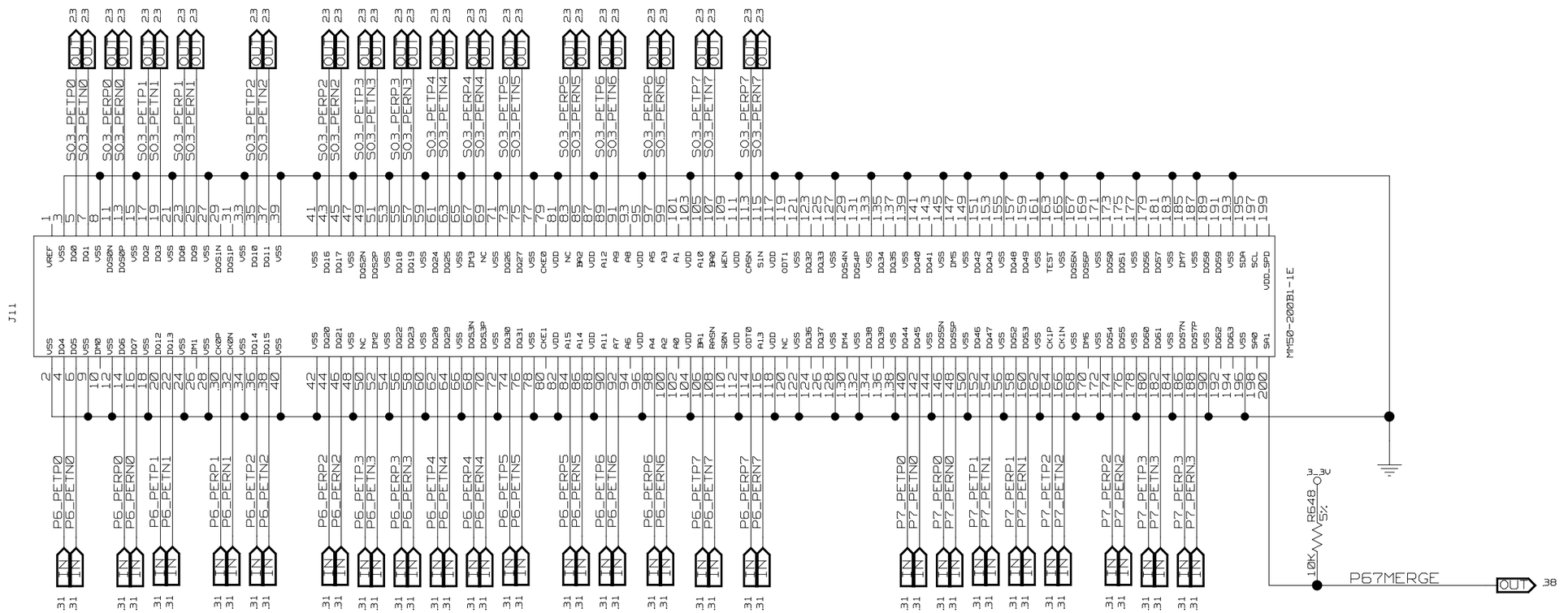
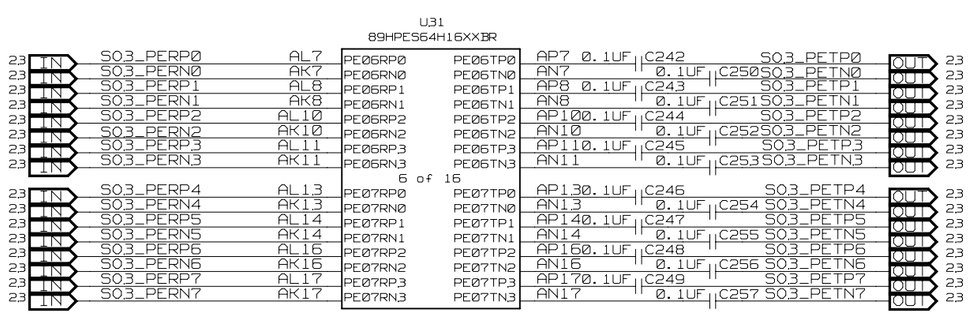
TITLE 89EBPES64H16			
PM PORT 4/5			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:34 2007		SHEET 22 OF 38	

RENESAS





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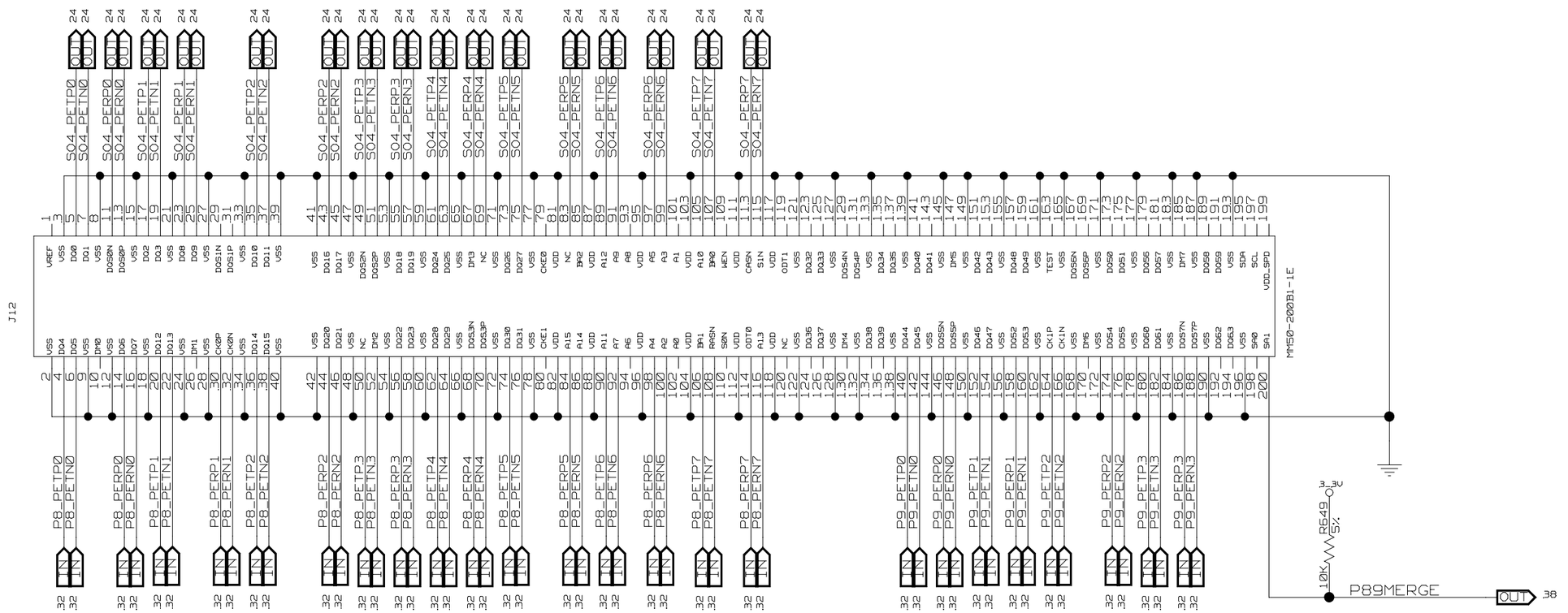
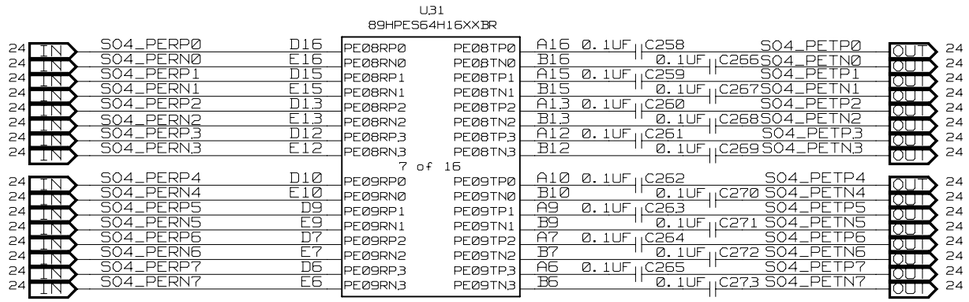
TITLE 89EBPES64H16 PM PORT 6/7			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:35 2007		SHEET 23 OF 38	

RENESAS





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TITLE 89EBPES64H16 PM PORT 8/9			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:36 2007		SHEET 24 OF 38	

RENESAS

J13

MM50-200B1-1E

P10_PETP0 P10_PETN0 P10_PERP0 P10_PERN0 P10_PETP1 P10_PETN1 P10_PERP1 P10_PERN1 P10_PETP2 P10_PETN2 P10_PERP2 P10_PERN2 P10_PETP3 P10_PETN3 P10_PERP3 P10_PERN3 P10_PETP4 P10_PETN4 P10_PERP4 P10_PERN4 P10_PETP5 P10_PETN5 P10_PERP5 P10_PERN5 P10_PETP6 P10_PETN6 P10_PERP6 P10_PERN6 P10_PETP7 P10_PETN7 P10_PERP7 P10_PERN7

P11_PETP0 P11_PETN0 P11_PERP0 P11_PERN0 P11_PETP1 P11_PETN1 P11_PERP1 P11_PERN1 P11_PETP2 P11_PETN2 P11_PERP2 P11_PERN2 P11_PETP3 P11_PETN3 P11_PERP3 P11_PERN3

10K R550 5%

P1011MERGE OUT 38

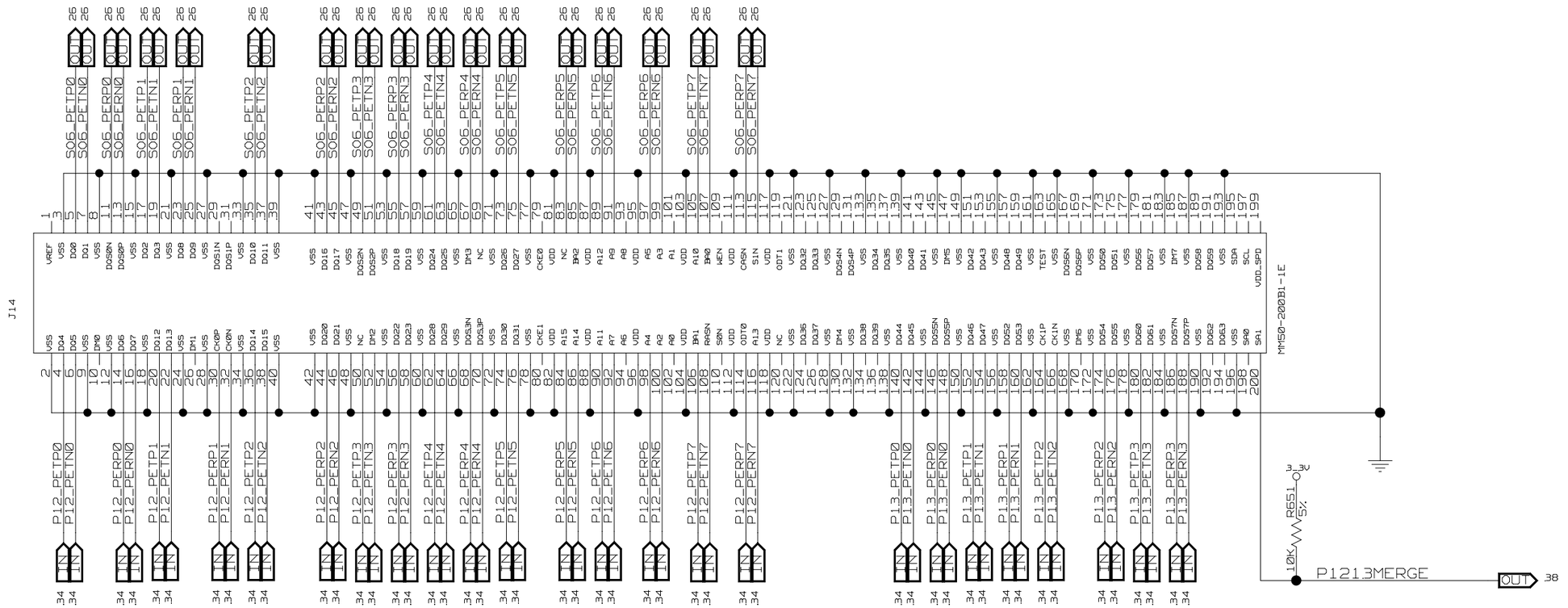
U31

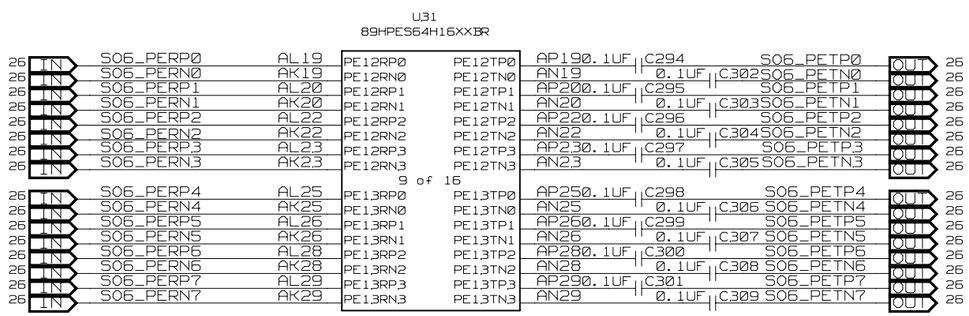
89HPES64H16XXBR

S05_PERP0	G4	PE10RP0	PE10TP0	G1	0.1UF	C274	S05_PETP0	
S05_PERN0	G5	PE10RN0	PE10TN0	G2	0.1UF	C286	S05_PETN0	
S05_PERP1	H4	PE10RP1	PE10TP1	H1	0.1UF	C275	S05_PETP1	
S05_PERN1	H5	PE10RN1	PE10TN1	H2	0.1UF	C287	S05_PETN1	
S05_PERP2	K4	PE10RP2	PE10TP2	K1	0.1UF	C276	S05_PETP2	
S05_PERN2	K5	PE10RN2	PE10TN2	K2	0.1UF	C288	S05_PETN2	
S05_PERP3	L4	PE10RP3	PE10TP3	L1	0.1UF	C277	S05_PETP3	
S05_PERN3	L5	PE10RN3	PE10TN3	L2	0.1UF	C289	S05_PETN3	
		8 of 16						
S05_PERP4	N4	PE11RP0	PE11TP0	N1	0.1UF	C278	S05_PETP4	
S05_PERN4	N5	PE11RN0	PE11TN0	N2	0.1UF	C290	S05_PETN4	
S05_PERP5	P4	PE11RP1	PE11TP1	P1	0.1UF	C283	S05_PETP5	
S05_PERN5	P5	PE11RN1	PE11TN1	P2	0.1UF	C291	S05_PETN5	
S05_PERP6	T4	PE11RP2	PE11TP2	T1	0.1UF	C284	S05_PETP6	
S05_PERN6	T5	PE11RN2	PE11TN2	T2	0.1UF	C292	S05_PETN6	
S05_PERP7	U4	PE11RP3	PE11TP3	U1	0.1UF	C285	S05_PETP7	
S05_PERN7	U5	PE11RN3	PE11TN3	U2	0.1UF	C293	S05_PETN7	

TITLE 89EBPES64H16			
PM PORT 10/11			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:37 2007		SHEET 25 OF 38	

RENESAS





TITLE 89EBPES64H16 PM PORT 12/13			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:38 2007		SHEET 26 OF 38	

RENESAS

J16

MM50-200B1-1E

P1415MERGE

U31
89HPES64H16XXBR

SO7_PERP0	AH31	PE14RP0	PE14TP0	AH340.1UF	C310	SO7_PETP0	
SO7_PERN0	AH30	PE14RN0	PE14TN0	AH33	0.1UF	C318	SO7_PETN0
SO7_PERP1	AG31	PE14RP1	PE14TP1	AG340.1UF	C311	SO7_PETP1	
SO7_PERN1	AG30	PE14RN1	PE14TN1	AG33	0.1UF	C319	SO7_PETN1
SO7_PERP2	AE31	PE14RP2	PE14TP2	AE340.1UF	C312	SO7_PETP2	
SO7_PERN2	AE30	PE14RN2	PE14TN2	AE33	0.1UF	C320	SO7_PETN2
SO7_PERP3	AD31	PE14RP3	PE14TP3	AD340.1UF	C313	SO7_PETP3	
SO7_PERN3	AD30	PE14RN3	PE14TN3	AD33	0.1UF	C324	SO7_PETN3
		10 of 16					
SO7_PERP4	AB31	PE15RP0	PE15TP0	AB340.1UF	C314	SO7_PETP4	
SO7_PERN4	AB30	PE15RN0	PE15TN0	AB33	0.1UF	C325	SO7_PETN4
SO7_PERP5	AA31	PE15RP1	PE15TP1	AA340.1UF	C315	SO7_PETP5	
SO7_PERN5	AA30	PE15RN1	PE15TN1	AA33	0.1UF	C326	SO7_PETN5
SO7_PERP6	W31	PE15RP2	PE15TP2	W34 0.1UF	C316	SO7_PETP6	
SO7_PERN6	W30	PE15RN2	PE15TN2	W33	0.1UF	C327	SO7_PETN6
SO7_PERP7	V31	PE15RP3	PE15TP3	V34 0.1UF	C317	SO7_PETP7	
SO7_PERN7	V30	PE15RN3	PE15TN3	V33	0.1UF	C328	SO7_PETN7

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TITLE 89EBPES64H16 PM PORT 14/15			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:39 2007		SHEET 27 OF 38	

RENESAS

P1_12V
W99
12V3
P1_3_3AUX
P1_CONN_12V
P1_3_3V
W101
3_3V
P1_CONN_3_3V
C331 10UF 25V
C332 10UF 25V
C335 10UF 16V
C336 10UF 16V
R511 0 0%
W102
S_PERSTN
P1_PERSTN
P1_PERST*
J18 PCI_X16_CONN
PORT 1 CONNECTOR
87715-9302
P1_REFCLKP
P1_REFCLKN
P1_PERP0
P1_PERN0
P1_PERP1
P1_PERN1
P1_PERP2
P1_PERN2
P1_PERP3
P1_PERN3
SSMBCLK
SSMBDATA
R509 0 0%
R510 0 0%
P1_WAKE*
P1_PETP0
P1_PETN0
P1_PETP1
P1_PETN1
P1_PETP2
P1_PETN2
P1_PETP3
P1_PETN3
3_3V
R555 5.1K 5%
P1PDN
P0_PERST*
R506 0 0%
J17 PCIE_X8_CONN
UPSTREAM PORT 0 CONNECTOR
87715-9206
P0_REFCLK+
P0_REFCLK-
P0_PERP0
P0_PERN0
P0_PERP1
P0_PERN1
P0_PERP2
P0_PERN2
P0_PERP3
P0_PERN3
P0_PERP4
P0_PERN4
P0_PERP5
P0_PERN5
P0_PERP6
P0_PERN6
P0_PERP7
P0_PERN7
P0_WAKE*
P0_PETP0
P0_PETN0
P0_PETP1
P0_PETN1
P0_PETP2
P0_PETN2
P0_PETP3
P0_PETN3
P0_PETP4
P0_PETN4
P0_PETP5
P0_PETN5
P0_PETP6
P0_PETN6
P0_PETP7
P0_PETN7
SSMBCLK
SSMBDATA
R507 0 0%
R508 0 0%
R554 5.1K 5%

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TITLE 89EBPES64H16
PCI EXPRESS CONN PORT 0/1

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0
AUTHOR	J. CARRILLO	CHECKED BY	B. OH
Mon Feb 05 15:33:39 2007		SHEET 28 OF 38	

RENESAS

PORT 3 CONNECTOR

PORT 2 CONNECTOR

J20 PCI_X16_CONN

J19 PCI_X16_CONN

87715-9302

P3_12V W104 12V3 P3_3_3AUX P3_CONN_12V P3_3_3V W106 3_3V P3_CONN_3_3V

P2_12V W103 12V3 W105 3_3V P2_3_3AUX P2_CONN_12V P2_CONN_3_3V

C339 10UF 25V C340 10UF 25V C342 10UF 16V C343 10UF 16V

C337 10UF 25V C338 10UF 25V C341 10UF 16V C344 10UF 16V

R517 0Ω 0% R512 0Ω 0%

P3_REFCLKP P3_REFCLKN P3_PERP0 P3_PERN0 P3_PERP1 P3_PERN1 P3_PERP2 P3_PERN2 P3_PERP3 P3_PERN3

P2_REFCLKP P2_REFCLKN P2_PERP0 P2_PERN0 P2_PERP1 P2_PERN1 P2_PERP2 P2_PERN2 P2_PERP3 P2_PERN3 P2_PERP4 P2_PERN4 P2_PERP5 P2_PERN5 P2_PERP6 P2_PERN6 P2_PERP7 P2_PERN7

P3_WAKE* P2_WAKE*

P3_PETP0 P3_PETN0 P3_PETP1 P3_PETN1 P3_PETP2 P3_PETN2 P3_PETP3 P3_PETN3

P2_PETP0 P2_PETN0 P2_PETP1 P2_PETN1 P2_PETP2 P2_PETN2 P2_PETP3 P2_PETN3 P2_PETP4 P2_PETN4 P2_PETP5 P2_PETN5 P2_PETP6 P2_PETN6 P2_PETP7 P2_PETN7

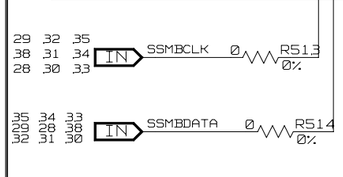
SSMBCLK SSMBDATA R515 0Ω 0% R516 0Ω 0% R513 0Ω 0% R514 0Ω 0%

W108 S_PERSTIN P3_PERSTIN P3_PERST*

W107 S_PERSTIN P2_PERSTIN P2_PERST*

R557 5% 5.1K P3PDN

R555 5% 5.1K P2PDN



TITLE 89EBPES64H16			
PCI EXPRESS CONN PORT 2/3			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:40 2007		SHEET 29 OF 38	

RENESAS

P5_12V W110 12V3 P5_3_3AUX

P5_CONN_12V

P5_3_3V W112 3_3V

P5_CONN_3_3V

C347 25V 10UF C348 25V 10UF

C351 16V 10UF C352 16V 10UF

R523 0Ω 0%

P4_12V W109 12V3

P4_3_3V W111 3_3V

C345 25V 10UF C346 25V 10UF

C349 16V 10UF C350 16V 10UF

P4_3_3AUX

P4_CONN_12V

P4_CONN_3_3V

J22 PCI_X16_CONN

PORT 5 CONNECTOR

87715-9302

P5_REFCLKP P5_REFCLKN P5_PERP0 P5_PERN0 P5_PERP1 P5_PERN1 P5_PERP2 P5_PERN2 P5_PERP3 P5_PERN3

W114

S_PERSTN IN 3 28 29 30 31 32 33 38

P5_PERSTN IN 38

P5_PERST*

SSMBCLK 0Ω R521 0%

SSMBDATA 0Ω R522 0%

P5_WAKE* OUT 37

P5_PETP0 P5_PETN0 P5_PETP1 P5_PETN1 P5_PETP2 P5_PETN2 P5_PETP3 P5_PETN3

3_3V R559 5% 5.1K P5PDN OUT 8

W113

S_PERSTN IN 3 28 29 30 31 32 33 38

P4_PERSTN IN 38

P4_PERST*

J21 PCI_X16_CONN

PORT 4 CONNECTOR

87715-9302

3_3V R558 5% 5.1K P4PDN OUT 8

P4_REFCLKP P4_REFCLKN P4_PERP0 P4_PERN0 P4_PERP1 P4_PERN1 P4_PERP2 P4_PERN2 P4_PERP3 P4_PERN3 P4_PERP4 P4_PERN4 P4_PERP5 P4_PERN5 P4_PERP6 P4_PERN6 P4_PERP7 P4_PERN7

SSMBCLK 0Ω R519 0%

SSMBDATA 0Ω R520 0%

P4_WAKE* OUT 37

P4_PETP0 P4_PETN0 P4_PETP1 P4_PETN1 P4_PETP2 P4_PETN2 P4_PETP3 P4_PETN3 P4_PETP4 P4_PETN4 P4_PETP5 P4_PETN5 P4_PETP6 P4_PETN6 P4_PETP7 P4_PETN7

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TITLE 89EBPES64H16 PCI EXPRESS CONN PORT 4/5			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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RENESAS

PORT 7 CONNECTOR

PORT 6 CONNECTOR

J24 PCI_X16_CONN

J23 PCI_X16_CONN

87715-9302

P7_12V W116 12V1 P7_3_3AUX P7_CONN_12V P7_3_3V W118 3_3V P7_CONN_3_3V

P6_12V W115 12V1 P6_3_3V W117 3_3V P6_3_3AUX P6_CONN_12V P6_CONN_3_3V

C355 C356 C353 C354 C357 C358 C359 C360 10UF 25V 16V

R529 R524 0Ω 0%

W120 S_PERSTIN P7_PERSTIN P7_PERST* P6_PERST* W119 S_PERSTIN P6_PERSTIN

P7_REFCLKP P7_REFCLKN P7_PERP0 P7_PERN0 P7_PERP1 P7_PERN1 P7_PERP2 P7_PERN2 P7_PERP3 P7_PERN3 P7_WAKE*

P6_REFCLKP P6_REFCLKN P6_PERP0 P6_PERN0 P6_PERP1 P6_PERN1 P6_PERP2 P6_PERN2 P6_PERP3 P6_PERN3 P6_PERP4 P6_PERN4 P6_PERP5 P6_PERN5 P6_PERP6 P6_PERN6 P6_PERP7 P6_PERN7 P6_WAKE*

SSMBCLK SSMBDATA R527 R528 R525 R526 0Ω 0%

R561 R550 5.1K 5%

P7PDN P6PDN

TITLE 89EBPES64H16			
PCI EXPRESS CONN PORT 6/7			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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RENESAS

P9_12V W122 12V1 C363 25V 10UF C364 25V 10UF

P9_3_3V W124 3_3V C367 16V 10UF C368 16V 10UF

P9_CONN_12V

P9_CONN_3_3V

P9_3_3AUX

R535 0Ω 0%

P8_12V W121 12V1 C361 25V 10UF C362 25V 10UF

P8_3_3V W123 3_3V C365 16V 10UF C366 16V 10UF

P8_3_3AUX

P8_CONN_12V

P8_CONN_3_3V

J26 PCI_X16_CONN

PORT 9 CONNECTOR

87715-9302

P9_REFCLKP P9_REFCLKN P9_PERP0 P9_PERN0 P9_PERP1 P9_PERN1 P9_PERP2 P9_PERN2 P9_PERP3 P9_PERN3

W126

S_PERSTN IN 3 28 29 30 31 32 33 38

P9_PERSTN IN 38

P9_PERST*

SSMBCLK 0Ω R533 0%

SSMBDATA 0Ω R534 0%

P9_WAKE* OUT 37

P9_PETP0 P9_PETN0 P9_PETP1 P9_PETN1 P9_PETP2 P9_PETN2 P9_PETP3 P9_PETN3

3_3V R563 5% 5.1K P9PDN OUT 9

R530 0Ω 0%

P8_REFCLKP P8_REFCLKN P8_PERP0 P8_PERN0 P8_PERP1 P8_PERN1 P8_PERP2 P8_PERN2 P8_PERP3 P8_PERN3 P8_PERP4 P8_PERN4 P8_PERP5 P8_PERN5 P8_PERP6 P8_PERN6 P8_PERP7 P8_PERN7

W125

S_PERSTN IN 3 28 29 30 31 32 33 38

P8_PERSTN IN 38

P8_PERST*

J25 PCI_X16_CONN

PORT 8 CONNECTOR

87715-9302

3_3V R562 5% 5.1K P8PDN OUT 8

SSMBCLK 0Ω R531 0%

SSMBDATA 0Ω R532 0%

P8_WAKE* OUT 37

P8_PETP0 P8_PETN0 P8_PETP1 P8_PETN1 P8_PETP2 P8_PETN2 P8_PETP3 P8_PETN3 P8_PETP4 P8_PETN4 P8_PETP5 P8_PETN5 P8_PETP6 P8_PETN6 P8_PETP7 P8_PETN7

TITLE 89EBPES64H16 PCI EXPRESS CONN PORT 8/9			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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RENESAS

P11_12V W128 12V1 P11_3_3VAUX P11_CONN_12V P11_3_3V W130 3_3V P11_CONN_3_3V

P10_12V W127 12V2 P10_3_3V W129 3_3V P10_3_3VAUX P10_CONN_12V P10_CONN_3_3V

C371 10UF 25V C372 10UF 25V C375 10UF 16V C376 10UF 16V

C369 10UF 25V C370 10UF 25V C373 10UF 16V C374 10UF 16V

R541 0Ω 0%

J28 PCI_X16_CONN

PORT 11 CONNECTOR

87715-9302

P11_REFCLK_KIN P11_REFCLK_IN P11_PERP0 P11_PERN0 P11_PERP1 P11_PERN1 P11_PERP2 P11_PERN2 P11_PERP3 P11_PERN3

W132 S_PERSTN P11_PERSTN P11_PERST*

SSMBCLK R539 0% SSMBDATA R540 0%

P11_WAKE*

P11_PETP0 P11_PETN0 P11_PETP1 P11_PETN1 P11_PETP2 P11_PETN2 P11_PETP3 P11_PETN3

3_3V R565 5% 5.1K P11PDN

R536 0Ω 0%

P10_REFCLK_KIN P10_REFCLK_IN P10_PERP0 P10_PERN0 P10_PERP1 P10_PERN1 P10_PERP2 P10_PERN2 P10_PERP3 P10_PERN3 P10_PERP4 P10_PERN4 P10_PERP5 P10_PERN5 P10_PERP6 P10_PERN6 P10_PERP7 P10_PERN7

W131 S_PERSTN P10_PERSTN P10_PERST*

J27 PCI_X16_CONN

PORT 10 CONNECTOR

87715-9302

R537 SSMBCLK 0Ω 0%

R538 SSMBDATA 0Ω 0%

P10_WAKE*

R564 5% 5.1K P10PDN

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TITLE 89EBPES64H16 PCI EXPRESS CONN PORT10/11			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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RENESAS

P13_12V W134 12V2 P13_3_3AUX

P13_CONN_12V

P13_3_3V W136 3_3V P13_CONN_3_3V

P12_12V W133 12V2

P12_3_3V W135 3_3V

P12_3_3AUX

P12_CONN_12V

P12_CONN_3_3V

C379 25V 10UF C380 25V 10UF

C383 16V 10UF C384 16V 10UF

C377 25V 10UF C378 25V 10UF

C381 16V 10UF C382 16V 10UF

R547 0Ω 0%

R542 0Ω 0%

J30 PCI_X16_CONN

J29 PCI_X16_CONN

PORT 13 CONNECTOR

PORT 12 CONNECTOR

87715-9302

P13_REFCLK* P13_PERP0 P13_PERN0 P13_PERP1 P13_PERN1 P13_PERP2 P13_PERN2 P13_PERP3 P13_PERN3 P13_WAKE*

P12_REFCLK* P12_PERP0 P12_PERN0 P12_PERP1 P12_PERN1 P12_PERP2 P12_PERN2 P12_PERP3 P12_PERN3 P12_PERP4 P12_PERN4 P12_PERP5 P12_PERN5 P12_PERP6 P12_PERN6 P12_PERP7 P12_PERN7 P12_WAKE*

P13_PETP0 P13_PETN0 P13_PETP1 P13_PETN1 P13_PETP2 P13_PETN2 P13_PETP3 P13_PETN3

P12_PETP0 P12_PETN0 P12_PETP1 P12_PETN1 P12_PETP2 P12_PETN2 P12_PETP3 P12_PETN3 P12_PETP4 P12_PETN4 P12_PETP5 P12_PETN5 P12_PETP6 P12_PETN6 P12_PETP7 P12_PETN7

SSMBCLK 0Ω R545 0% SSMBDATA 0Ω R546 0%

SSMBCLK 0Ω R543 0% SSMBDATA 0Ω R544 0%

W138 S_PERSTN P13_PERSTN P13_PERST*

W137 S_PERSTN P12_PERSTN P12_PERST*

3_3V R567 5% 5.1K P13PDN

3_3V R566 5% 5.1K P12PDN

TITLE	89EBPES64H16 PCI EXPRESS CONN PORT12/13
SIZE B	DRAWING NO. STGSCH-00100
FAB P/N	18-624-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Mon Feb 05 15:33:45 2007
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RENESAS

PORT 15 CONNECTOR

PORT 14 CONNECTOR

J32 PCI_X16_CONN

J31 PCI_X16_CONN

87715-9302

W139 W140 W141 W142 W143 W144

C385 C386 C387 C388 C389 C390 C391 C392

R548 R549 R550 R551 R552 R553 R568 R569

P15_12V P15_3_3V P15_3_3VAUX P15_CONN_12V P15_CONN_3_3V P15_PERSTN P15_PERST* P15_REFCLK_IN P15_PERP0 P15_PERN0 P15_PERP1 P15_PERN1 P15_PERP2 P15_PERN2 P15_PERP3 P15_PERN3 P15_WAKE* P15PDN

P14_12V P14_3_3V P14_3_3VAUX P14_CONN_12V P14_CONN_3_3V P14_PERSTN P14_PERST* P14_REFCLK_IN P14_PERP0 P14_PERN0 P14_PERP1 P14_PERN1 P14_PERP2 P14_PERN2 P14_PERP3 P14_PERN3 P14_PERP4 P14_PERN4 P14_PERP5 P14_PERN5 P14_PERP6 P14_PERN6 P14_PERP7 P14_PERN7 P14_WAKE* P14PDN

SSMBCLK SSMBDATA

3_3V 12V2

TITLE 89EBPES64H16			
PCI EXPRESS CONN PORT14/15			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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RENESAS

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

U31
89HPES64H16XXBR

A1	VSS1	VSS80	F8	J13	VSS158	VSS236	N18
A2	VSS2	VSS81	F9	J15	VSS159	VSS237	N26
A5	VSS3	VSS82	F10	J16	VSS160	VSS238	N28
A8	VSS4	VSS83	F11	J19	VSS161	VSS239	N29
A11	VSS5	VSS84	F12	J20	VSS162	VSS240	N32
A14	VSS6	VSS85	F13	J22	VSS163	VSS241	P3
A17	VSS7	VSS86	F14	J23	VSS164	VSS242	P6
A20	VSS8	VSS87	F15	J24	VSS165	VSS243	P7
A23	VSS9	VSS88	F16	J28	VSS166	VSS244	P8
A26	VSS10	VSS89	F17	J29	VSS167	VSS245	P10
A29	VSS11	VSS90	F18	J32	VSS168	VSS246	P12
A33	VSS12	VSS91	F19	K3	VSS169	VSS247	P14
A34	VSS13	VSS92	F20	K6	VSS170	VSS248	P16
B1	VSS14	VSS93	F21	K7	VSS171	VSS249	P18
B5	VSS15	VSS94	F22	K8	VSS172	VSS250	P20
B8	VSS16	VSS95	F23	K11	VSS173	VSS251	P23
B11	VSS17	VSS96	F24	K12	VSS174	VSS252	P25
B14	VSS18	VSS97	F25	K14	VSS175	VSS253	P27
B17	VSS19	VSS98	F26	K16	VSS176	VSS254	P28
B20	VSS20	VSS99	F27	K19	VSS177	VSS255	P29
B23	VSS21	VSS100	F28	K21	VSS178	VSS256	P30
B26	VSS22	VSS101	F29	K23	VSS179	VSS257	P31
B29	VSS23	VSS102	F32	K24	VSS180	VSS258	P32
B34	VSS24	VSS103	G3	K27	VSS181	VSS259	P33
C5	VSS25	VSS104	G6	K28	VSS182	VSS260	P34
C6	VSS26	VSS105	G7	K29	VSS183	VSS261	R1
C7	VSS27	VSS106	G8	K32	VSS184	VSS262	R2
C8	VSS28	VSS107	G9	L3	VSS185	VSS263	R3
C9	VSS29	VSS108	G10	L6	VSS186	VSS264	R4
C10	VSS30	VSS109	G11	L7	VSS187	VSS265	R5
C11	VSS31	VSS110	G12	L8	VSS188	VSS266	R6
C12	VSS32	VSS111	G13	L9	VSS189	VSS267	R7
C13	VSS33	VSS112	G14	L10	VSS190	VSS268	R9
C14	VSS34	VSS113	G15	L11	VSS191	VSS269	R15
C15	VSS35	VSS114	G16	L12	VSS192	VSS270	R17
C16	VSS36	VSS115	G19	L16	VSS193	VSS271	R19
C17	VSS37	VSS116	G20	L19	VSS194	VSS272	R21
C18	VSS38	VSS117	G21	L23	VSS195	VSS273	R26
C19	VSS39	VSS118	G22	L24	VSS196	VSS274	R28
C20	VSS40	VSS119	G23	L25	VSS197	VSS275	R29
C21	VSS41	VSS120	G24	L26	VSS198	VSS276	R32
C22	VSS42	VSS121	G25	L27	VSS199	VSS277	T3
C23	VSS43	VSS122	G26	L28	VSS200	VSS278	T6
C24	VSS44	VSS123	G28	L29	VSS201	VSS279	T7
C25	VSS45	VSS124	G29	L30	VSS202	VSS280	T8
C26	VSS46	VSS125	G32	L31	VSS203	VSS281	T9
C27	VSS47	VSS126	H3	L32	VSS204	VSS282	T10
C28	VSS48	VSS127	H6	L33	VSS205	VSS283	T11
C29	VSS49	VSS128	H7	L34	VSS206	VSS284	T12
D5	VSS50	VSS129	H10	M1	VSS207	VSS285	T13
D8	VSS51	VSS130	H11	M2	VSS208	VSS286	T14
D11	VSS52	VSS131	H12	M3	VSS209	VSS287	T16
D14	VSS53	VSS132	H14	M4	VSS210	VSS288	T18
D17	VSS54	VSS133	H16	M5	VSS211	VSS289	T20
D20	VSS55	VSS134	H17	M6	VSS212	VSS290	T23
D23	VSS56	VSS135	H18	M7	VSS213	VSS291	T24
D26	VSS57	VSS136	H19	M8	VSS214	VSS292	T25
D29	VSS58	VSS137	H21	M9	VSS215	VSS293	T26
E5	VSS59	VSS138	H23	M10	VSS216	VSS294	T27
E8	VSS60	VSS139	H24	M11	VSS217	VSS295	T28
E11	VSS61	VSS140	H25	M12	VSS218	VSS296	T29
E14	VSS62	VSS141	H29	M14	VSS219	VSS297	T32
E17	VSS63	VSS142	H30	M16	VSS220	VSS298	U3
E20	VSS64	VSS143	H31	M19	VSS221	VSS299	U6
E23	VSS65	VSS144	H32	M21	VSS222	VSS300	U8
E26	VSS66	VSS145	H33	M23	VSS223	VSS301	U15
E29	VSS67	VSS146	H34	M24	VSS224	VSS302	U17
E30	VSS68	VSS147	J1	M25	VSS225	VSS303	U19
E31	VSS69	VSS148	J2	M26	VSS226	VSS304	U21
E32	VSS70	VSS149	J3	M27	VSS227	VSS305	U22
E33	VSS71	VSS150	J4	M28	VSS228	VSS306	U27
E34	VSS72	VSS151	J5	M29	VSS229	VSS307	U29
F1	VSS73	VSS152	J6	M32	VSS230	VSS308	U30
F2	VSS74	VSS153	J7	N3	VSS231	VSS309	U31
F3	VSS75	VSS154	J8	N6	VSS232	VSS310	U32
F4	VSS76	VSS155	J10	N7	VSS233	VSS311	U33
F5	VSS77	VSS156	J11	N9	VSS234	VSS312	U34
F6	VSS78	VSS157	J12	N16	VSS235		
F7	VSS79						

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V2	VSS314	VSS392	AB28	AF24	VSS470	VSS548	AJ29
V3	VSS315	VSS393	AB29	AF25	VSS471	VSS549	AJ30
V4	VSS316	VSS394	AB32	AF27	VSS472	VSS550	AJ31
V5	VSS317	VSS395	AC3	AF28	VSS473	VSS551	AJ32
V6	VSS318	VSS396	AC6	AF29	VSS474	VSS552	AJ33
V8	VSS319	VSS397	AC7	AF30	VSS475	VSS553	AJ34
V13	VSS320	VSS398	AC8	AF31	VSS476	VSS554	AK1
V14	VSS321	VSS399	AC9	AF32	VSS477	VSS555	AK2
V16	VSS322	VSS400	AC10	AF33	VSS478	VSS556	AK3
V18	VSS323	VSS401	AC11	AF34	VSS479	VSS557	AK4
V20	VSS324	VSS402	AC12	AG1	VSS480	VSS558	AK5
V27	VSS325	VSS403	AC14	AG2	VSS481	VSS559	AK6
V29	VSS326	VSS404	AC16	AG3	VSS482	VSS560	AK9
V32	VSS327	VSS405	AC19	AG4	VSS483	VSS561	AK12
W3	VSS328	VSS406	AC21	AG5	VSS484	VSS562	AK15
W6	VSS329	VSS407	AC23	AG6	VSS485	VSS563	AK18
W7	VSS330	VSS408	AC24	AG10	VSS486	VSS564	AK21
W8	VSS331	VSS409	AC25	AG11	VSS487	VSS565	AK24
W9	VSS332	VSS410	AC26	AG12	VSS488	VSS566	AK27
W10	VSS333	VSS411	AC27	AG14	VSS489	VSS567	AK30
W11	VSS334	VSS412	AC28	AG16	VSS490	VSS568	AL6
W12	VSS335	VSS413	AC29	AG17	VSS491	VSS569	AL9
W15	VSS336	VSS414	AC30	AG18	VSS492	VSS570	AL12
W17	VSS337	VSS415	AC31	AG19	VSS493	VSS571	AL15
W19	VSS338	VSS416	AC32	AG21	VSS494	VSS572	AL18
W21	VSS339	VSS417	AC33	AG23	VSS495	VSS573	AL21
W22	VSS340	VSS418	AC34	AG24	VSS496	VSS574	AL24
W23	VSS341	VSS419	AD1	AG25	VSS497	VSS575	AL27
W24	VSS342	VSS420	AD2	AG28	VSS498	VSS576	AL30
W25	VSS343	VSS421	AD3	AG29	VSS499	VSS577	AM6
W26	VSS344	VSS422	AD4	AG32	VSS500	VSS578	AM7
W27	VSS345	VSS423	AD5	AH3	VSS501	VSS579	AM8
W28	VSS346	VSS424	AD6	AH6	VSS502	VSS580	AM9
W29	VSS347	VSS425	AD7	AH7	VSS503	VSS581	AM10
W32	VSS348	VSS426	AD8	AH9	VSS504	VSS582	AM11
Y3	VSS349	VSS427	AD9	AH10	VSS505	VSS583	AM12
Y6	VSS350	VSS428	AD10	AH11	VSS506	VSS584	AM13
Y7	VSS351	VSS429	AD11	AH12	VSS507	VSS585	AM14
Y9	VSS352	VSS430	AD12	AH13	VSS508	VSS586	AM15
Y14	VSS353	VSS431	AD16	AH14	VSS509	VSS587	AM16
Y16	VSS354	VSS432	AD19	AH15	VSS510	VSS588	AM17
Y18	VSS355	VSS433	AD23	AH16	VSS511	VSS589	AM18
Y20	VSS356	VSS434	AD24	AH19	VSS512	VSS590	AM19
Y26	VSS357	VSS435	AD25	AH20	VSS513	VSS591	AM20
Y28	VSS358	VSS436	AD26	AH21	VSS514	VSS592	AM21
Y29	VSS359	VSS437	AD27	AH22	VSS515	VSS593	AM22
Y30	VSS360	VSS438	AD28	AH23	VSS516	VSS594	AM23
Y31	VSS361	VSS439	AD29	AH24	VSS517	VSS595	AM24
Y32	VSS362	VSS440	AD32	AH25	VSS518	VSS596	AM25
Y33	VSS363	VSS441	AE3	AH26	VSS519	VSS597	AM26
Y34	VSS364	VSS442	AE6	AH27	VSS520	VSS598	AM27
AA1	VSS365	VSS443	AE7	AH28	VSS521	VSS599	AM28
AA2	VSS366	VSS444	AE8	AH29	VSS522	VSS600	AM29
AA3	VSS367	VSS445	AE11	AH32	VSS523	VSS601	AM30
AA4	VSS368	VSS446	AE12	AJ3	VSS524	VSS602	AN1
AA5	VSS369	VSS447	AE14	AJ6	VSS525	VSS603	AN6
AA6	VSS370	VSS448	AE16	AJ7	VSS526	VSS604	AN9
AA7	VSS371	VSS449	AE19	AJ8	VSS527	VSS605	AN12
AA8	VSS372	VSS450	AE21	AJ9	VSS528	VSS606	AN15
AA10	VSS373	VSS451	AE23	AJ10	VSS529	VSS607	AN18
AA12	VSS374	VSS452	AE24	AJ11	VSS530	VSS608	AN21
AA15	VSS375	VSS453	AE27	AJ12	VSS531	VSS609	AN24
AA17	VSS376	VSS454	AE28	AJ13	VSS532	VSS610	AN27
AA19	VSS377	VSS455	AE29	AJ14	VSS533	VSS611	AN30
AA21	VSS378	VSS456	AE32	AJ15	VSS534	VSS612	AN34
AA23	VSS379	VSS457	AF3	AJ16	VSS535	VSS613	AP1
AA25	VSS380	VSS458	AF6	AJ17	VSS536	VSS614	AP2
AA27	VSS381	VSS459	AF7	AJ18	VSS537	VSS615	AP6
AA28	VSS382	VSS460	AF8	AJ19	VSS538	VSS616	AP9
AA29	VSS383	VSS461	AF11	AJ20	VSS539	VSS617	AP12
AA32	VSS384	VSS462	AF12	AJ21	VSS540	VSS618	AP15
AB3	VSS385	VSS463	AF13	AJ22	VSS541	VSS619	AP18
AB6	VSS386	VSS464	AF15	AJ23	VSS542	VSS620	AP21
AB7	VSS387	VSS465	AF16	AJ24	VSS543	VSS621	AP24
AB9	VSS388	VSS466	AF19	AJ25	VSS544	VSS622	AP27
AB17	VSS389	VSS467	AF20	AJ26	VSS545	VSS623	AP30
AB19	VSS390	VSS468	AF22	AJ27	VSS546	VSS624	AP33
AB26	VSS391			AJ28	VSS547		

VDDCORE
W151
1_0VC

VDDPE
W152
1_0VA

U31
89HPES64H16XXBR

N13	VDDCORE1	VDDPE1	J21
N14	VDDCORE2	VDDPE2	J14
N15	VDDCORE3	VDDPE3	L22
N17	VDDCORE4	VDDPE4	L21
N19	VDDCORE5	VDDPE5	L20
N20	VDDCORE6	VDDPE6	L18
N21	VDDCORE7	VDDPE7	L17
N22	VDDCORE8	VDDPE8	L15
P13	VDDCORE9	VDDPE9	L14
P15	VDDCORE10	VDDPE10	L13
P17	VDDCORE11	VDDPE11	M22
P19	VDDCORE12	VDDPE12	M20
P21	VDDCORE13	VDDPE13	M18
P22	VDDCORE14	VDDPE14	M17
R13	VDDCORE15	VDDPE15	M15
R14	VDDCORE16	VDDPE16	M13
R16	VDDCORE17	VDDPE17	N24
R18	VDDCORE18	VDDPE18	N23
R20	VDDCORE19	VDDPE19	N12
R22	VDDCORE20	VDDPE20	N11
T15	VDDCORE21	VDDPE21	P26
T17	VDDCORE22	VDDPE22	P24
T19	VDDCORE23	VDDPE23	P11
T21	VDDCORE24	VDDPE24	P9
T22	VDDCORE25	VDDPE25	R24
U13	VDDCORE26	VDDPE26	R23
U14	VDDCORE27	VDDPE27	R12
U16	VDDCORE28	VDDPE28	R11
U18	VDDCORE29	VDDPE29	U24
U20	VDDCORE30	VDDPE30	U23
V15	VDDCORE31	VDDPE31	U12
V17	VDDCORE32	VDDPE32	U11
V19	VDDCORE33	VDDPE33	V24
V21	VDDCORE34	VDDPE34	V23
V22	VDDCORE35	VDDPE35	V12
W13	VDDCORE36	VDDPE36	V11
W14	VDDCORE37	VDDPE37	Y24
W16	VDDCORE38	VDDPE38	Y23
W18	VDDCORE39	VDDPE39	Y12
W20	VDDCORE40	VDDPE40	Y11
Y13	VDDCORE41	VDDPE41	AA26
Y15	VDDCORE42	VDDPE42	AA24
Y17	VDDCORE43	VDDPE43	AA11
Y19	VDDCORE44	VDDPE44	AA9
Y21	VDDCORE45	VDDPE45	AB24
Y22	VDDCORE46	VDDPE46	AB23
AA13	VDDCORE47	VDDPE47	AB12
AA14	VDDCORE48	VDDPE48	AB11
AA16	VDDCORE49	VDDPE49	AC22
AA18	VDDCORE50	VDDPE50	AC20
AA20	VDDCORE51	VDDPE51	AC18
AA22	VDDCORE52	VDDPE52	AC17
AB13	VDDCORE53	VDDPE53	AC15
AB14	VDDCORE54	VDDPE54	AC13
AB15	VDDCORE55	VDDPE55	AD22
AB16	VDDCORE56	VDDPE56	AD21
AB18	VDDCORE57	VDDPE57	AD20
AB20	VDDCORE58	VDDPE58	AD18
AB21	VDDCORE59	VDDPE59	AD17
AB22	VDDCORE60	VDDPE60	AD15
		VDDPE61	AD14
		VDDPE62	AD13
		VDDPE63	AF21
		VDDPE64	AF14

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1_0VB
W154
VDDAPE
FB5
FB6
FB7
C396 1UF
C397 15V
C394 1UF

VTT
W153
1_5VA

U31
89HPES64H16XXBR

H13	VTTPE1	VDDAPE1	H15
H22	VTTPE2	VDDAPE2	H20
J17	VTTPE3	VDDAPE3	K15
J18	VTTPE4	VDDAPE4	K20
K13	VTTPE5	VDDAPE5	R8
K17	VTTPE6	VDDAPE6	R10
K18	VTTPE7	VDDAPE7	R25
K22	VTTPE8	VDDAPE8	R27
N8	VTTPE9	VDDAPE9	Y8
N10	VTTPE10	VDDAPE10	Y10
N25	VTTPE11	VDDAPE11	Y25
N27	VTTPE12	VDDAPE12	Y27
U9	VTTPE13	VDDAPE13	AE15
U10	VTTPE14	VDDAPE14	AE20
U25	VTTPE15	VDDAPE15	AG15
U26	VTTPE16	VDDAPE16	AG20
V9	VTTPE17		
V10	VTTPE18		
V25	VTTPE19		
V26	VTTPE20		
AB8	VTTPE21		
AB10	VTTPE22		
AB25	VTTPE23		
AB27	VTTPE24		
AE13	VTTPE25		
AE17	VTTPE26		
AE18	VTTPE27		
AE22	VTTPE28		
AF17	VTTPE29		
AF18	VTTPE30		
AG13	VTTPE31		
AG22	VTTPE32		
A4	VDDIO1		
A30	VDDIO2		
B2	VDDIO3		
B33	VDDIO4		
D3	VDDIO5		
D31	VDDIO6		
D34	VDDIO7		
E1	VDDIO8		
H9	VDDIO9		
H27	VDDIO10		
J26	VDDIO11		
K9	VDDIO12		
AE9	VDDIO13		
AE26	VDDIO14		
AF9	VDDIO15		
AF10	VDDIO16		
AG8	VDDIO17		
AG9	VDDIO18		
AG26	VDDIO19		
AK34	VDDIO20		
AL1	VDDIO21		
AL4	VDDIO22		
AL32	VDDIO23		
AN2	VDDIO24		
AN33	VDDIO25		
AP5	VDDIO26		
AP31	VDDIO27		

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3_3V
VDDIO
W155

D | C | B | A

TITLE 89EBPES64H16			
PES64H16 POWER			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:47 2007		SHEET 36 OF 38	

RENESAS

VTT

1UF C397 16V

0.1UF C398
0.1UF C399
0.1UF C400
0.1UF C401
0.1UF C402
0.1UF C403
0.1UF C404
0.1UF C405
0.1UF C406
0.1UF C407
0.1UF C408
0.1UF C409
0.1UF C410
0.1UF C411
0.1UF C412
0.1UF C413
0.1UF C329
0.1UF C330

C464 47UF 10V
C465 47UF 10V
C396 47UF 10V
C395 47UF 10V

C476 47UF 10V
C477 47UF 10V
C431 47UF 10V
C432 47UF 10V

C480 47UF 10V
C504 47UF 10V
C482 47UF 10V
C483 47UF 10V

VDDPE

1UF C466 16V

0.1UF C434
0.1UF C435
0.1UF C436
0.1UF C437
0.1UF C438
0.1UF C439
0.1UF C440
0.1UF C441
0.1UF C442
0.1UF C443
0.1UF C444
0.1UF C445
0.1UF C446
0.1UF C447
0.1UF C448
0.1UF C449

VDDCORE

1UF C484 16V
1UF C485 16V

0.1UF C486
0.1UF C487
0.1UF C488
0.1UF C489
0.1UF C490
0.1UF C491
0.1UF C492
0.1UF C493
0.1UF C494
0.1UF C495
0.1UF C496
0.1UF C497
0.1UF C498
0.1UF C499
0.1UF C500
0.1UF C501
0.1UF C502
0.1UF C503

VDDIO

0.1UF C414
0.1UF C415
0.1UF C416
0.1UF C417
0.1UF C418
0.1UF C419
0.1UF C420
0.1UF C421
0.1UF C422
0.1UF C423
0.1UF C424
0.1UF C425
0.1UF C426
0.1UF C427
0.1UF C333
0.1UF C334
0.1UF C450
0.1UF C451

VDDAPE

1UF C428 16V

0.1UF C429
0.1UF C430
0.1UF C433
0.1UF C457
0.1UF C458
0.1UF C469
0.1UF C470
0.1UF C471
0.1UF C472
0.1UF C473
0.1UF C474
0.1UF C475

47UF C478 10V
47UF C479 10V
47UF C481 10V
47UF C516 10V

3_3V

R570 10K 5% — U32 — P1_WAKE* (28) — C505 0.1UF
R571 10K 5% — U33 — P2_WAKE* (29) — C506 0.1UF
R572 10K 5% — U34 — P3_WAKE* (29) — C507 0.1UF
R573 10K 5% — U35 — P4_WAKE* (30) — C508 0.1UF
R574 10K 5% — U36 — P5_WAKE* (30) — C509 0.1UF

R575 10K 5% — U37 — P6_WAKE* (31) — C514 0.1UF
R576 10K 5% — U38 — P7_WAKE* (31) — C510 0.1UF
R577 10K 5% — U39 — P8_WAKE* (32) — C511 0.1UF
R578 10K 5% — U40 — P9_WAKE* (32) — C512 0.1UF
R579 10K 5% — U41 — P10_WAKE* (33) — C513 0.1UF

R580 10K 5% — U42 — P11_WAKE* (33) — C519 0.1UF
R581 10K 5% — U43 — P12_WAKE* (34) — C520 0.1UF
R582 10K 5% — U44 — P13_WAKE* (34) — C518 0.1UF
R583 10K 5% — U45 — P14_WAKE* (35) — C517 0.1UF
R584 10K 5% — U48 — P15_WAKE* (35) — C515 0.1UF

OE* VCC A GND Y — SN74LVC1G125

P0_WAKE* R631 0% (28) OUT

TITLE 89EBPES64H16
POWER DECOUPLING AND WAKE

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO	B. OH

Mon Feb 05 15:33:48 2007 — SHEET 37 OF 38

RENESAS

U31
89HPES64H16XXBR

REFCLK0P
REFCLK0N
REFCLK1P
REFCLK1N
REFCLK2P
REFCLK2N
REFCLK3P
REFCLK3N

S_PERSTN

1 of 16

DNP
W98
R643 0 0%
R644 0 0%

FCN # PCBFCN-0026
ADDS MISSING
CONNECTION TO AM3

S21
SM_SW8
R604 10K 5%
R603 10K 5%
R602 10K 5%
R601 10K 5%
R600 10K 5%
R597 10K 5%
R598 10K 5%
R599 10K 5%

S19
SM_SW8
R585 10K 5%
R586 10K 5%
R587 10K 5%
R588 10K 5%
RSTHALT

R589 10K 5%
R590 10K 5%
R591 10K 5%
R592 10K 5%
R593 10K 5%
R594 10K 5%
R595 10K 5%
R596 10K 5%

U50
CD74AC04M
C522 0.1UF
R653 0 0%
R654 0 0%
R655 0 0%
R656 0 0%
R657 0 0%
R658 0 0%
R659 0 0%
R660 0 0%

U51
CD74AC04M
C521 0.1UF

DNP
S20
SM_SW8

R508 2.7K 5%
R509 2.7K 5%
R510 2.7K 5%
R511 2.7K 5%
R512 2.7K 5%

W145
W146
W147
W148
W149

MSMBADDR0
MSMBADDR1
MSMBADDR2

SCL
SDA

U31
89HPES64H16XXBR

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JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*

PLACE EEPROM ON SOCKET

EEPROM
U49
24LC512
R605 2.7K 5%
R606 2.7K 5%
R607 2.7K 5%
C523 0.1UF
W150

SMBUS HEADER TO UPSTREAM DEVICE
J34
SSMBDATA
SSMBCLK

DS92 DS88 DS93 DS89 DS94 DS90 DS95 DS91
GRN
R627 330 5%
R623 330 5%
R628 330 5%
R624 330 5%
R629 330 5%
R625 330 5%
R630 330 5%
R626 330 5%

GPIO31
GPIO28
GPIO27
GPIO26
GPIO25
GPIO24
GPIO23
GPIO22
GPIO21

P15_PERSTN
P14_PERSTN
P13_PERSTN
P12_PERSTN
P11_PERSTN
P10_PERSTN
P9_PERSTN
P8_PERSTN
P7_PERSTN
P6_PERSTN
P5_PERSTN
P4_PERSTN
P3_PERSTN
P2_PERSTN
P1_PERSTN

R517 R518 R520 R521 R633 R634 R635 R636 R637 R638 R639 R640 R641 R642
10K 5%

R615 1K 5%
R614 1K 5%
R616 1K 5%
R613 1K 5%

J33
JTAG HEADER
JTAG_RST*
M_TDI
M_TDO
M_TMS
M_TCK
R619 330 5%
R622 1K 5%

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TITLE	89EBPES64H16 PES64H16 SMBUS REFCLK
SIZE	B
DRAWING NO.	STGSCH-00100
FAB P/N	18-624-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Tue Feb 06 09:23:31 2007
	SHEET 38 OF 38

RENESAS

PCB Design Group
Engineering Change Notice

STG ECN# : PCBECN-0026
STG DCN# : STGC-0099R01

Project Name 89EBPES64H16 - 89HPES64H16 Eval Bd

Current Fab Rev. 18-624-000
New Fab Rev. N/A

Release/Effective Date: 1/19/2007

Documentation Affected:

- ☐ Assembly Drawing
- ☐ Bill Of Materials
- ☐ Drill File
- ☐ Fab Drawing
- ☐ FSD
- ☑ Gerber Data
- ☑ IPC356 Netlist
- ☑ PCB Database
- ☐ Pick And Place File
- ☐ Product Spec
- ☑ Schematic Drawing
- ☐ Other

Originator's Approval:

APPROVED
☑ YES
☐ NO

Name: John Carrillo
Date: 1/19/2007

Reason For Change: (Originator)

Missing merge1415 control connection to U31.AM3
Power rails to U31 have excessive voltage drop through 0 ohm resistors

Description of Requested Change: (Originator)

Add connection to U31.AM3 from R589.
Remove 0 ohm resistors at ouput of regulators and replace with shorting bars.
Add additional wires from power regulators to U31 power.

Rework Description or Action Required: (STG)

Add wire from U31.AM3 to R589.
Remove resistors R18, R30, R20, and R32
Add shorting bar between pads of R18, R30, R20, and R32
Add jumper wires for V1_0A, V1_0B, V1_0C, and V1_5 power

Disposition of Existing Material:

- ☐ Scrap And Replace
- ☐ Use As Is
- ☑ Rework Per ECN
- ☐ Other

STG Approval Signatures:

Eng. Manager	APPROVED ☐ YES ☐ NO		**Project Mgr.:**	APPROVED ☐ YES ☐ NO	
Name:	Richard Pham	**Date:**	**Name:**	Brian Oh	**Date:**
Component Engineer:	☑ YES ☐ NO		**Mfg. Engineer:**	☐ YES ☐ NO	
Name:	Ben Hinson	**Date:** 1/19/2007	**Name:**	Robert Yang	**Date:**

Copy Distribution:

- ☑ Apps. Engineering
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- ☐ Product Marketing
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