IDT™ 89EBPES12N3 Rev. 1.0 Evaluation Board

User Manual
Table of Contents and Overview

This document provides an overview of and insight into the contents of the full 89EBPES12N3 Evaluation Board User Manual which is available through IDT's secure access technical documentation portal.

To gain access to the full version of this document and other technical collateral housed at the myIDT secure portal, please contact ssdhelp@idt.com or your local IDT Sales contact.

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Description of the EB12N3 Eval Board

Notes

Introduction

The 89HPES12N3 switch (also referred to as PES12N3 in this manual) is a member of IDT's PCI Express standard (PCIe) based line of products. It is a 3 port switch, with 4 serial lanes per port (x4). One upstream port is provided for connecting to the root complex (RC), and two downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES12N3 User Manual.

The 89EBPES12N3 Evaluation Board (also referred to as EB12N3 in this manual) provides an evaluation platform for the PES12N3 switch. It is also a cost effective way to add a PCIe downstream port (x4) to an existing system with a limited number of PCIe downstream ports. The EB12N3 eval board is designed to function as an add-on card to be plugged into a x4 PCIe slot available on a motherboard hosting an appropriate root complex and microprocessor(s). The EB12N3 is a vehicle to test and evaluate the functionality of the PES12N3 chip, and it can also play an important role for customers to get a headstart on software development while they await the arrival of their own hardware. It is also used inside IDT to reproduce system level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB12N3 board.

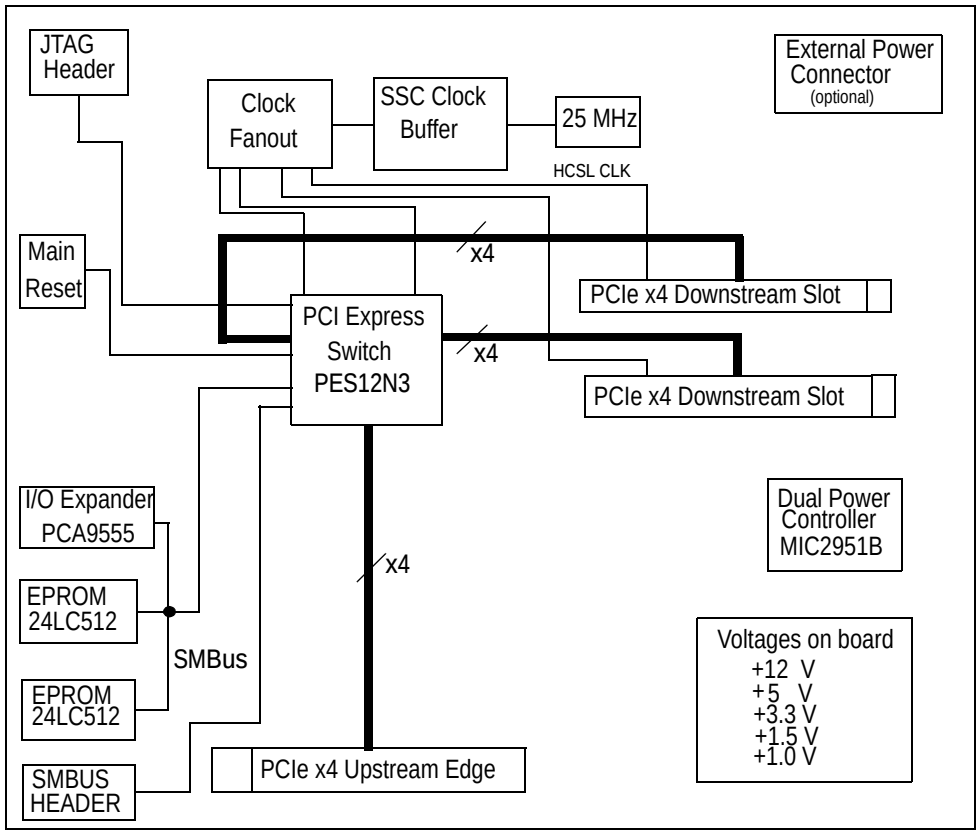

Figure 1.1 Functional Block Diagram of the EB12N3 Eval Board

Notes

Board Features

Hardware

- *PES12N3 PCIe 3 port switch*
  - Three x4 ports, 12 PCIe lanes
  - PCIe Base Specification Revision 1.0a compliant
  - 48 Gbps aggregate switching capacity
  - 128 to 2048 byte maximum payload size
  - Static lane reversal and polarity inversion supported on all lanes
  - Automatic per port link width negotiation to x4, x2, x1
  - Can load configuration from serial EEPROM via SMBUS
- *x4 PCIe Connectors*
  - One edge connector on the upstream port, to be plugged into a x4 slot on a host motherboard
  - Two slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in
- *Numerous user selectable configurations set using onboard jumpers and DIP-switches*
  - Source of clock - host clock or onboard clock generator
  - multiple clock rates and spread spectrum settings
  - Boot mode selection
- *SMBUS Slave Interface (4 pin header)*
- *SMBUS Master Interface connected to two optional Serial EEPROMs through I/O expander*
  - Facilitates testing with two different settings of initialization data with a simple change of a jumper
  - Only one EEPROM can be selectively connected to the SMBUS at a time
- *"Attention" button for each port to initiate a hot swap event on each port*
- *6 pin connector for optional external power supply*
- *Push button for Warm Reset*
- *Several LEDs to display status, reset, power, "Attention", etc.*
- *One 10 pin JTAG connector (pitch 2.54 mm x 2.54 mm)*

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES12N3 within host systems running popular operating systems.

- *Device Drivers*
  - Operating Systems Supported: Windows2000, WindowsXP, Linux
  - Installation programs or scripts
- *GUI based application for Windows and Linux*
  - Allows users to view and modify registers in the PES12N3
  - Binary file generator for programming the serial EEPROMs attached to the SMBUS

Other

A metal bracket is required to hold firmly in place the two endpoints plugged into the EB12N3 board.

An external power supply may be required under some conditions.

SMBUS cable may be required for certain evaluation exercises.

SMA connectors are provided on the EB12N3 board for specific test points.

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