# Quick start ADC1415S, ADC1215S, ADC1115S, ADC1015S series Demonstration board for ADC1415S, ADC1215S, ADC1115S,

**ADC1015S series** 

Rev. 06 — July 2012

Quick start

#### **Document information**

Info	Content
Keywords	PCB2001-2, demonstration board, ADC, converter, input buffer
Abstract	This document describes how to use the demonstration board for the analog-to-digital converter ADC1415S, ADC1215S, ADC1115S and ADC1015S series.

Overview





#### **Revision history**

Rev	Date	Description
1	20081001	Initial version.
2	20090518	Update to PCB2001-2.
3	20090610	Add SPI software description.
4	20100519	Add HSDC extension module acquisition system description.
5	20110120	Update with latest software tool.
6	20120702	Rebranded.

# 1. Overview of the ADC1415S, ADC1215S, ADC1015S demo board

## 1.1 ADC1415S series

Figure below presents the connections to measure ADC1415S.

POWER SUPPLY 5V .GND POWER SUPPLY .GND I = 185 mA I = 20 mA. 3V 1.8V .GND **SPI MODULE** USB OR PARALLEL SYNTHESIZED SIGNAL LOGIC ANALYZER GENERATOR Output data INPUT SIGNAL FILTER DAV for synchronization . 2V<sub>pp</sub> sinewave High-order D0 (LSB) to D13 (MSB) . AĆ Band pass SYNTHESIZED PRESENTED CONFIGURATION SIGNAL 2V<sub>pp</sub> input full scale GENERATOR Single Sine wave clock signal **C**LOCK SIGNAL Input common mode from IC **Binary ADC output** sinewave AC SPI Mode Fig 1. ADC1415S series typical configuration set-up **Quick start** 

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## 1.2 ADC1215S series

Figure below presents the connections to measure ADC1215S.

POWER SUPPLY 5V .GND POWER SUPPLY . I = 185 mA GND I = 20 mA 3V 1.8V .GND SPI MODULE USB OR PARALLEL SYNTHESIZED D SIGNAL LOGIC ANALYZER GENERATOR Output data INPUT SIGNAL FILTER DAV for synchronization . 2V<sub>pp</sub> sinewave High-order D0 (LSB) to D11 (MSB) . AC Band pass CB200 SYNTHESIZED PRESENTED CONFIGURATION SIGNAL 2Vpp input full scale GENERATOR Single Sine wave clock signal Input common mode from IC **CLOCK SIGNAL Binary ADC output** sinewave AC SPI Mode Fig 2. ADC1215S series typical configuration set-up

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#### 1.3 ADC1115S series

Figure below presents the connections to measure ADC1415S.



Fig 3. ADC1115S series typical configuration set-up

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#### 1.4 ADC1015S series

Figure below presents the connections to measure ADC1015S.

POWER SUPPLY 5V .GND POWER SUPPLY l = 185 mA GND I = 20 mA 3V 1.8V .GND **SPI MODULE** USB OR PARALLEI SYNTHESIZED **DIDT** SIGNAL LOGIC ANALYZER GENERATOR Output data INPUT SIGNAL FILTER DAV for synchronization . 2V<sub>pp</sub> sinewave . AC High-order D0 (LSB) to D9 (MSB) Band pass 170 -0200 CB2001 SYNTHESIZED PRESENTED CONFIGURATION SIGNAL 2V<sub>pp</sub> input full scale GENERATOR Single Sine wave clock signal **C**LOCK SIGNAL Input common mode from IC Binary ADC output sinewave AC SPI Mode

Fig 4. ADC1015S series typical configuration set-up

#### 1.5 Power supply

The board is powered with a 3  $V_{DC}$  and 1.8/3  $V_{DC}$  power supplies. A power supply regulator is used to supply all the circuitry on the board.

Table 1.	General power supply	
Name	Function	View
J10	+3V green connector – Power supply 3 $V_{\text{DC}}$ / 250 mA.	
J9	+1.8V green connector – Power supply 1.8 $V_{\text{DC}}$ / 100 mA	TP1
J8	+5V green connector – Power supply 5 $V_{\text{DC}}$ / 100 mA	
TP1	AGND test point – Digital ground	
TP2	DGND test point – Analog ground	
		J9 J8 J10

## 1.6 Input signals (IN, CLK)

The input clock signal can be either a sine-wave or a LVCMOS signal.

To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

Where M is an odd number of period and N is the number of samples.

Table 2. Name	Input signals	View
Marine	Tunction	VIEW
J1	IN connector – Analog input signal (50 $\Omega$ matching)	
J2	CLKP connector – Single ended clock input signal ( $50\Omega$ matching), with a transformer.	
J3	CLKN connector – Grounded on that demoboard	
		J1 - J

## 1.7 Output signals (D0 to D13, OTR, DAV)

The digital output signal is available in binary, 2's complement or gray format.

A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

J2

J3

Table 3	B. Output signals	
Name	Function	View
J4	Array connector – ADC digital output(D0 to D13), Out of range signal (OTR) and Data Valid (DAV)	Jdf

## 1.8 SPI Mode

The ADC1x15S can be **controlled** either by a Serial Peripheral Interface (SPI) or by PIN.

Name	Function	View
J5	Array connector – SPI daughter board interface	



## 1.9 SPI program

For more details on how to control device with SPI, refer to section 3.3.

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The figure 4 shows an overview of the extension module HSDC-EXTMOD01/DB acquisition board:



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The HSDC extension module is intended for acquisition/generation and clock generation purpose. When connected to an ADC demo-board it is intended as an acquisition system for digital output bits delivered by ADC, either CMOS (HE14 P1 connector) or LVDS DDR (SAMTEC QTH\_060\_02 P2 connector).

The board brief specification is shown below:

- 32 MB memory size for acquisition pattern;
- 2 16-bit channels CMOS up to 200 MHz;
- 16-bit LVDS DDR input data stream up to 320 MHz;
- On-board or external reference for signal generation.

In this section the specific requirement for the use with ADC1115S demo-board will be shown.

For more details on the HSDC-EXTMOD01/DB, please visit: http://www.idt.com.

#### 2.1 HSDC extension module: hardware initialization

Before using the generation board, make sure that you connect the USB cable **prior to** the supply.

When USB and power cable are connected, the HSDC-EXTMOD will light 3 red LEDs.

The green LED close to the PLL is only when it is locked (see <u>section 3.3</u>).

The red LED close to FPGA reports normal behavior when flashing <sup>1</sup>/<sub>4</sub> on, <sup>3</sup>/<sub>4</sub> off. Any other flashing behavior reports a failure at initialization (see section 3.3).

#### 2.2 HSDC extension module: CMOS connector description

The <u>figure 5</u> shows a brief description of the hardware connection on the HE14 connector.

For proper use of the acquisition board, make sure that resistor R86 (0  $\Omega$ ) is connected while R84 is removed.



## 3.1 ADC1x15S CMOS outputs

The <u>figure 24</u> below shows an overview of the whole system ADC1x15S+HSDC extension module with CMOS outputs configuration for which connection is straightforward, together with a supply extension module (release A) for the ADC1x15S demo-board:



ADC1015S series

## 3.2 ADC Software tool

Run the application "SW\_ADC\_1\_r02.exe". This application will allow:

- the user to control features on our high speed ADC through the SPI interface available on any ADC1415S, ADC1215S, ADC1115S and ADC1015S series;
- As well as performing any online data acquisition to evaluate the performances of the ADC1415S, ADC1215S, ADC1115S and ADC1015S series.

At start-up, the program will detect any board connected to your system and display information as can be seen on following window:



 ${\mathbb O}$ : "IDT Banner Button" will display your default internet browser to the IDT data converter home page;

©: "REFRESH" allows you to poll your system for any hardware change. It will reset any board connected to your system;

3: "QUIT" allows you quit the application;

(a): "INITIALIZATION" allow you to initialize the HSDC-EXTMOD board prior to any acquisition task.

In the example above, the HSDC-EXTMOD has been detected, as well as ADC1015S125.

At this moment, make sure that 4 LEDs are visible on the HSDC-EXTMOD (2 close to power plug, 1 for USB and 1 close to FPGA).

The "Info" page gives more details on the current hardware configuration for the HSDC-EXTMOD board:

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COPYIGHT IDT 2012	IDT HSDC ADC acquisition software	Tup_
Device detected: ACCIIISSIZS Recolution II Simpling rate Fs (max. 125 Mpps) 222.08 Input Frequency Fin (max. 600 MHz) 5 Number of samples 6536 Data stream OCMOS	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools Acquisition Trife HSDC-EXTMOD serial number: 272 . software version HSDC Software version is 2.0. dl version HSDC-EXTMOD dl version is VI.1. vhd version HSDC-EXTMOD dl version is 3. HSDC-EXTMOD version is 3. HSDC-EXTMOD version is 3. HSDC-EXTMOD version is 3. HSDC-EXTMOD version is 4.2. version HSDC-EXTMOD version is 9. HSDC-EXTMOD ver	
INITIALIZATION Upua log USD-EXTMOD found HSD-EXTMOD is initialed SAVE SETTINGS RESTORE SETTINGS	menory info Menory size is 16 Mbit (max S24288 samples).	

The HSDC-EXTMOD is not yet initialized, so the embedded PLL (LMK03001 in this example) is not locked. Initialization is only required for acquisition purpose.

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## 3.2.1 ADC SPI programming Functional Registers page

The page displays all SPI registers for ADC1415S, ADC1215S, ADC1115S and ADC1015S series:

copyright IDT 2012	REFRESH IDT HSDC ADC acquisition software QUIT
Device detected: ADC11155125 Resolution 11 Sampling rate Fs (max. 125 Mips) 122.88 Input frequency Fin (max. 600 MHs)	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools Acquisition Info ADC1115S125 SPI registers access Reset and Operating Mode SW_RST OP_MODE normal (power-up) \(\top\)
Number of samples 65536 ♥ Data stream ○ CMOS ○ LVDS	Input Clock Internal Reference  EF SEL UDFF/SE UDIFF/SE U
INITIALIZATION Output log HSDC-EXTMOD found! Device ADC1155125 found! HSDC-EXTMOD in initialized	DAVENV output         DAV PHASE output dock shifted (ahead) by \$7/67 dk         Dis_0PH2 SET           Test Pattern off         Quatom lest pattern off         Dis_0PH2 SET           CMOS Output         Quatom lest pattern Output dock shifted pattern off         Dis_0PH2 SET
SAVE SETTINGS	DAV DRV     DATA DRV     Nd     DATA J 2 SN

Perform any settings and then click on the "Send data to device" button to update the device registers.

## 3.2.2 ADC SPI programming Read Registers page

This page can be used to read all registers by clicking on the "Read all registers" button and will display the result in the table below:

copyright IDT 2012	REFRESH	IDT HSDC ADC acquisition sol	tware		QUI	π_(
Device detected: ADC1115S125 Resolution	ADC - Functional Registers ADC - Read ADC1115S125 SPI read regist		Info Register name	Address	Value	1
Sampling rate Fs (max. 125 Msps)			Reset and operating mode	. 5		
Input frequency Fin (max. 600 MHz)	Read	all registers	Clock	×6	1	
			Internal reference	×8	× 0	
Number of samples	Save reg	sters read to file	Input buffer	× 10	×3	
Data stream			Output data standard	× 11	×0	
O CMOS O LVDS	Data saved to file: C:\test.txt		Output clock	× 12	.9	
	J. C. Participation		Offset	× 13	×0	1
			Test pattern 1	× 14	×O	1
			Test pattern 2	× 15	×0	1
Output log HSDC-EXTMOD found Device ADCI1155125 found HSDC-EXTMOD is initialized			Test pattern 3	× 16	×0	
			Fast OTR	× 17	×0	
			CMOS output	× 20	×E	
			LVDS DDR O/P 1	×21	×O	
			LVDS DDR 0/P 2	× 22	×0	
SAVE SETTINGS						~
RESTORE SETTINGS						

When all registers have been read, it is possible to save the data to a text file. The settings are saved in a table-like format as shown below:

#### Table 5. Typical saving on text file

Content of file is shown as table format

Column 1	Column 2
Address	Value
05	00
06	01
08	00
10	03
11	00
12	09
13	00
14	00
15	00
16	00
17	00
20	0e
21	00

Column 1	Column 2
22	00

Note that all data are saved in hexadecimal format.

Click on the "Save registers read to file" button to select the file to store data to. Make sure that you store your file with ".txt" extension, this will allow you to re-use the file on the "ADC - Load Registers" page.

#### 3.2.3 ADC SPI programming Load Registers page

This page allows downloading configuration data to the device registers:

copyright IDT 2012	REFRESH	IDT HSDC ADC acquisition softwa	re		QUIT	
Device detected: ACCLISSIZS Recolution 1 3 sampling rate Fz (max. 125 Mpp) 222.88 Trput Requency Fin (max. 600 MHz) 223.88 Trput Requency Fin (ma	ADC - Fauntional Registers ADC - Acad Registers ADC - Taud Registers Load data from text file (*/ad*): C1(est.bd Load data download data	ADC - Load Registers Tools Acquesiton Info	Register name Register name Clock Internal reference Dutput buffer Output data standard Output dock Offsat Test pattern 1 Test pattern 2 Test pattern 3 Fast OTR CMOS output LVDS DDR O/P 1 LVDS DDR O/P 2	Address 5 6 10 10 11 11 12 13 14 15 15 15 15 15 20 21 21 20 21	Value         0           0         1           0         3           1         3           1         3           1         3           1         3           1         3           1         3 <th></th>	
RESTORE SETTINGS						

It is not necessary to have a file that has the whole set of registers listed. The only restriction is regarding the formatting of the file as given in <u>section 3.3.2</u>.

Note: this page can not be used to download data saved during the comparison process.

To download settings onto device registers, follow the procedure below:

- Browse to select your file (button ①);
- Click on "Load data" button 2.

A message on field ③ and a progress bar will inform about the status of the operation until message "download done!" is seen. The table ④ is updated with the current values downloaded at the fly as can be seen on <u>figure 13</u>.

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## 3.2.4 Tools page

This page allows the user to calculate the coherent frequencies values involved of the acquisition process. It gives an indication where the 6 first harmonics are located in the Nyquist zone.

Enter your analog and sampling frequencies in field<sup>①</sup>. Indicate the number of samples to be acquired<sup>②</sup>, as well as the fixed parameter for the coherency calculation (Fs in our example above<sup>③</sup>). Press "UPDATE GRAPH" to look at the frequency plan, it gives also the real Fin frequency (Refer to <u>appendix A.1</u> for more details on coherency calculation):



Note: The level of the harmonics shown does not reproduce the behavior of the ADC; they are only given as indication for location.

#### 3.2.5 Acquisition page

This page will acquire data to evaluate the high dynamic performance of the device:



Before proceeding to any acquisition, the user needs to do the following entries:

• the sampling frequency Fs: 122.88 Msps in our example (field ①);

- the input frequency Fin: 5 MHz in our example (field ①);
- the number of samples to be acquired 65536 in our example (field 2);
- indicate whether it is CMOS or LVDS DDR (field ③);
- press the "INITIALIZATION" button ④. It will initialized the HSDC-EXTMOD board:
  - FPGA is ready (red LED is flashing 1/4 on and 3/4 off);
  - PLL embedded is locked (green LED is on);
- indicate whether Fin or Fs are coherent or not (field (5):
  - if signals are coherent, selected which Fin or Fs are fixed for the calculation (see <u>appendix A.1</u>);
  - if signals are not coherent, select the window for FFT processing to apply (the Blackman window gives better results).
- press the "ACQUIRE" button (6) to display the results from the FFT processing. The results fields (7) will be updated automatically.
- press "STOP" button to stop acquisition;
- field 
   Illows to do FFT averaging over up to 255 trials, suitable for small signal analysis;

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Table Conte			n <mark>ic res</mark> u nown as			n a text file	•								
Name	Fin	Fs	Vin	ENOB	SINAD_C	SNR_C	SNR_FS	SFDR_C	SFDR_FS	THD	H2	H3	H4	H5	H6
	(MHz)	(MHz)	(dBFS)	-	(dBc)	(dBc)	(dBFS)	(dBc)	(dBFS)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)
ADC11	15S test														

Note that while acquisition is running, any other action (ADC SPI programming, quit or refresh) is not possible. Stop acquisition first before proceeding to any other task.

#### 3.2.5.1 FFT spectrum

The first graph to be displayed is the FFT spectrum of the digital pattern acquired:



Press the "Autoscale" button to display the whole content.

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#### 3.2.5.2 Reorganized signal

The reorganized signal displays the reconstructed sine wave from coherency calculation corresponding to 1 period of the input signal:



Press the "Autoscale" button to display the whole content.

#### 3.2.5.3 Unreconstructed signal

Γ

The unreconstructed signal displays the unreconstructed sine wave corresponding to the whole number of period being acquired following the coherency rule:

Device detected:     ADC - Functional Registers     ADC - Read Registers     ADC - Load Registers     Tools     Acquisition       Resolution     Finand Fisure:     Fixed Its:     Fis:     Fis:     Fis:     Fis:     Fis:       Suppling rate Fs (max: 125 Mops)     Fis:     Fis		
ACCLIISSIZS  Resolution Fin and Fis are: Fixed Is: Fis coherent (Hz) Coherent Coherent Fin aud Fis are: Fixed Is: Fis coherent (Hz) Coherent Fin 122.8864/02+6 No window  Fin aud Fis are: Fin 122.8864/02+6 No window  Fin aud Fis are: Fin 122.8864/02+6 No window  Fin aud Fis are: Fis aud Fis are: Fin aud Fis are: Fin aud Fis are: Fin aud Fis are: Fis aud Fis are: Fin aud Fis are: Fis are: Fis are		
Kacolution     Fin and Fs are:     Fixed it:     Ps coherent (Hz)     Select window type:       11     O coherent     O Fin     122,884-62E+6     No window     Enable FFT averaging     10 (max. 255       122,88     Image: Select window type:     Image: Select window type:     No window     Image: Select window type:		
11     Fin and Fs are:     Fixed it:     Fix coherent (Ht)     Select window type:       Sampling rate Fs (max. 125 Mtps)     Coherent     Fin     122.864642E+6     No window T     Enable FFT averaging     10 (max. 255       122.88     Provide     Provide     Provide     Provide     Provide     Provide		
Simpling rate Fs (max. 125 Mtps) Coherent Fs 122.86440E+6 No window Enable FFT averaging 10 (max. 255 122.88		
122.88	trials)	
Input frequency Fin (max. 600 MHz) Store to file Line Header		
5 Results file 18		<b>E</b>
Number of samples STOP Display ADC0		
65536 V FFT Spectrum Reorganized Signal Unreconstructed Signal Histogram Autoscale		
Data stream		
Item AD	: Un	nit
O CMOS 2000 - ADC Digitized signal		_
OLVDS 2000- 2000- S.000	MH	łz
1800 - Amplitude -0.93	5 dBF	FS
1600 - ADC AC parameters		
1000 SNR 65.26	dBo	c
1400 – SNR 66.20		
INITIALIZATION SINAD 65.19		
100 - ENOB 10.53	bits	
Output log         g         100 -         5FDR         10.0           HSD-ExTIMOD found         FFDR         81.9         5FDR         82.9		
HSDC-EXTMOD found SFDR 82.90		
Device ADC11155125 found 800 -	l dBo	<u>c</u>
HSDC-EXTMOD is initialized!		
600 - H2 -98.0		
200m tool		
200-		
H6 -108.	193 dBo	<u>.                                    </u>
0 10000 20000 30000 40000 50000 60000 70000 Min 103		4
0 10000 20000 30000 40000 50000 70000 Min 103 Code Max 1942	cod	
	Cod B3 Cod	
SAVE SETTINGS	50 COO	362

Fig 17. SW\_ADC\_1\_r02: "Acquisition" page, unreconstructed signal graph

Press the "Autoscale" button to display the whole content.

Use the zoom tool to observe in more details all the captured data.

#### 3.2.5.4 Histogram

The histogram graph shows the distribution of output codes. This graph shows which code is present and if there is any missing code in the conversion range:



Press the "Autoscale" button to display the whole content.

The table shows the range of output codes.

#### 3.2.6 Info page

This page will give practical information related to software and hardware settings:

copyright IDT 2012	REFRESH	IDT HSDC ADC acquisition software	QUIT
Device detected: ACCILISEIS Recolution II Simpligrate Fis (max. 125 Mips) (122.0 Input finguancy Fin (max. 600 MHz) (5 Simpligrate of samples 65536	ADC - Functional Registers ADC - R HSDC-EXTMOD Serial number software version HSDC-Software version is di version HSDC-EXTMOD di version HSDC-EXTMOD HL version HSDC-EXTMOD HL version	2.0. (2) ns V1.1. (3) aon is 3. (4) tus	
Data stream CMOS LVDS	+5V +3.3V HSDC-EXTMOD clock info Clock source is Port P1 i Synthetzer is Linkcoop memory info Memory size is 16 Mbit (m	(CMOS), active on rising edge. PLL LMK03001 locied	
Output log HISD-CEXTMOD found Device APCINSUS found HISD-CEXTMOD & Installed			
SAVE SETTINGS RESTORE SETTINGS			

Fig 19. SW\_ADC\_1\_r02: "Info" page

The information visible on this page are:

- board serial number ①;
- HSDC software release number 2;
- HSDC-EXTMOD dll version 3;
- HSDC-EXTMOD vhdl version @;
- HSDC-EXTMOD supply status (5);
- HSDC-EXTMOD clock capability and status version 6;
- HSDC-EXTMOD memory capability ⑦.

# 4. Appendix A.1: coherency calculation

The coherency relies on the fact that clock and analog input signal are synchronized and the first and last samples being captured are adjoining samples: it ensures a continuous digitized time process for the FFT processing.

To achieve this, one has to

 $\frac{F_{in}}{F_{in}} = \frac{M}{N}$  follow the equation:

where M is an odd integer equal to the number of periods being acquired and N the number of samples acquired.

With Fin, Fs and N known, M has to be chosen such that it follows the equation above. To do this iterative calculation, one has to decide whether Fin or Fs is fixed.

To illustrate this process, let's consider our current example with Fin = 5 MHz, Fs = 122.88Msps and N = 65536 samples acquired:

- if Fin is fixed, this leads to M = 2667 periods of input signal to be acquired and a real sampling frequency to be Fs = 122.864642 MHz;
- If Fs is fixed, this leads to M = 2667 periods of input signal to be acquired and a real input frequency to be Fin = 5.000625 MHz.

Those values needs to be programmed in the signal generator and clock generator before capture is done, otherwise the FFT calculation will lead to a non-coherent result as shown below:



The numbers given for SNR, SFDR are completely wrong if coherency is not respected.

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# 5. Notes

For more information or sales office addresses, please visit: <u>http://www.idt.com</u>.

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