Quick start ADC1410S, ADC1210S and ADC1010S series (F1 or F2 versions)

Demonstration board for ADC1410S, ADC1210S and ADC1010S series

Rev. 06 — 2 July 2012

Quick start

Document information

Info	Content
Keywords	PCB2122-2, Demonstration board, ADC, Converter
Abstract	This document describes how to use the demonstration board for the analog-to-digital converter ADC1410S, ADC1210S and ADC1010S series.

Overview





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Revision history

Rev	Date	Description
1	20081001	Initial version.
2	20090518	Update
3	20090610	Add SPI software description.
4	20100519	Add HSDC extension module acquisition system description.
5	20110120	Update with latest software tool.
6	20120702	Rebranded.

1. Overview of the ADC1x10S demo board

1.1 ADC1410S, ADC1210S, ADC1010S F1 series (CMOS digital outputs)

Figure below presents the connections to measure ADC161xS.



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1.2 ADC1410S, ADC1210S, ADC1010S F2 series (LVDS/DDR digital outputs)

Figure below presents the connections to measure ADC1x10S.



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1.3 Power supply

The board is powered either with a 3 V_{DC} and 1.8/3 V_{DC} power supplies or a 5V DC adaptor.

Table 1	. Power supply	
Name	Function	View
J8	2.1 Jack connector – 5VDC Change ST9 and ST10 position accordingly	J10 / J11 J8 TP1
J10	+3V green connector – Power supply 3 V_{DC}	
J11	Change ST9 and ST10 position accordingly CMOS version +1.8V green connector – Power supply 1.8 V _{DC} LVDS DDR version +3V green connector – Power supply 1.8 V _{DC}	
TP1	GND test point	
TP2	GND test point	

1.4 Input signals (IN, CLK)

The input clock signal can be either a sine wave or a LVCMOS signal.

To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

, where M is an odd number of period and N is the number of samples.

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Table 2	. Input signals	
Name	Function	View
J1	IN connector – Analog input signal (50 Ω matching)	
J2	CLKP connector – Single ended clock input signal (50 Ω matching), with a transformer.	
J3	CLKM connector – Grounded on that demoboard	

1.5 Output signals in CMOS version (D0 to D1x, DAV, OTR)

The digital output signal is available in binary, 2's complement or gray format. A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

Table 3. Output signals

Name	Function	View
J6	Array connector – ADC digital output (D0 to D1x), OTR and Data Valid (DAV)	J6

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1.6 Output signals in LVDS DDR version

The digital output signal is available in binary, 2's complement or gray format.

A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

Table 4. Output signals

Name	Function	View
J7	Samtec QTH connector – ADC digital output (D0 to D1x) and Data Valid (DAV)	

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1.7 SPI Mode

The ADC1x10S can be **controlled** either by a Serial Peripheral Interface (SPI) or by PIN.

Table 5. SPI Interface

Name	Function	View
J12	USB connector – SPI interface	

1.8 SPI program

For more details on how to control device with SPI, refer to section 3.3.

2. HSDC extension module: acquisition board

The figure 4 shows an overview of the extension module HSDC-EXTMOD01/DB acquisition board:



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The HSDC extension module is intended for acquisition/generation and clock generation purpose. When connected to an ADC demo-board it is intended as an acquisition system for digital output bits delivered by ADC, either CMOS (HE14 P1 connector) or LVDS DDR (SAMTEC QTH_060_02 P2 connector).

The board brief specification is shown below:

- 32 MB memory size for acquisition pattern;
- 2 16-bit channels CMOS up to 200 MHz;
- 16-bit LVDS DDR input data stream up to 320 MHz;
- On-board or external reference for signal generation.

In this section the specific requirement for the use with ADC1x10S demo-board will be shown.

For more details on the HSDC-EXTMOD01/DB, please visit: http://www.idt.com.

2.1 HSDC extension module: hardware initialization

Before using the generation board, make sure that you connect the USB cable **prior to** the supply.

When USB and power cable are connected, the HSDC-EXTMOD will light 3 red LEDs.

The green LED close to the PLL is only when it is locked (see <u>section 3.3</u>).

The red LED close to FPGA reports normal behavior when flashing ¹/₄ on, ³/₄ off. Any other flashing behavior reports a failure at initialization (see section 3.3).

2.2 HSDC extension module: CMOS connector description

The <u>figure 5</u> shows a brief description of the hardware connection on the HE14 connector.

For proper use of the acquisition board, make sure that resistor R86 (0 Ω) is connected while R84 is removed.

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3. Combo 1x10S and HSDC extension module

3.1 ADC1410S, ADC1210S, ADC1010S setup CMOS outputs

The <u>figure 24</u> below shows an overview of the whole system ADC1x10S+HSDC extension module with CMOS outputs configuration for which connection is straightforward, together with a supply extension module (release A) for the ADC1x10S demo-board:



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3.2 ADC1410S, ADC1210S, ADC1010S setup LVDS/DDR outputs

The <u>figure 24</u> below shows an overview of the whole system ADC1x10S+HSDC extension module with CMOS outputs configuration for which connection is straightforward, together with a supply extension module (release A) for the ADC1x10S demo-board:



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3.3 ADC Software tool

Run the application "SW_ADC_1_r02.exe". This application will allow:

- the user to control features on our high speed ADC through the SPI interface available on any ADC1410S, ADC1210S, ADC1010S series;
- As well as performing any online data acquisition to evaluate the performances of the ADC1410S, ADC1210S, ADC1010S series.

At start-up, the program will detect any board connected to your system and display information as can be seen on following window:

	REFRESH IDT HSDC ADC acquisition softw Stop acquisition before any action.	ware	Stop acquisition	QUIT before any action.
Device detected: ADC14105125 Resolution 14 Sampling rate Fs (max. 125 Maps) Troub frequency Fin (max. 600 MHz) 5	Acquisition Fin and Fs are: Fixed is: Fs coherent (Hs) Select window type:	Info	ax. 255 trials)	
Number of samples 65536 T Data stream O CMOS O LVDS	STOP Display ADC0 FFT Spectrum Recryanized Sgnal Unreconstructed Sgnal Hatogram Autoscale 20 -	Item ADC Digitized signal Frequency		Jnit Hz
INITIALIZATION Output log HDDC-EXTMOD Found Device ACCHIGGI25 Found	0- -112 -20- (9) -60- (9) -60- (9) -60- (9) -60- (9) -112 -113 -113 -113 -113 -113 -113 -113	Ampikude ADC AC parameters SNR SNR SINAD ENOB SFDR SFDR SFDR THD	70.09 db 71.03 db 69.85 db 11.31 bi 85.36 db	BFS Bc ts Bc BFS
Levice 400_14/05125 round		ADC Harmonics H2 H3 H4 H5 H6 ADC Code excursion Min	-87.070 db -96.435 db -105.316 db -86.298 db -111.330 db	Bc Bc BC BC
SAVE SETTINGS RESTORE SETTINGS	Frequency (Hz)	Max Mean		odes

①: "IDT Banner Button" will display your default internet browser to the IDT data converter home page;

②: "REFRESH" allows you to poll your system for any hardware change. It will reset any board connected to your system;

③: "QUIT" allows you quit the application;

④: "INITIALIZATION" allow you to initialize the HSDC-EXTMOD board prior to any acquisition task.

In the example above, the HSDC-EXTMOD has been detected, as well as ADC1410S125.

At this moment, make sure that 4 LEDs are visible on the HSDC-EXTMOD (2 close to power plug, 1 for USB and 1 close to FPGA).

The "Info" page gives more details on the current hardware configuration for the HSDC-EXTMOD board:

SW_ADC_1		
COPYIGHE IDT 2012	REFRESH IDT HSDC ADC acquisition software QUIT	
Device detected: ADC14105125 Resolution 14 122:88 Toput frequency Fin (max. 600 MHz) 5 Number of samples 65536 0 CHOS 0 CHOS	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools Acquisition Info HSDC-EXTMOD Serial number: 272 . software version HSDC Software version is 2.0. dil version HSDC-EXTMOD dil version is 9.1.1. vhd version HSDC-EXTMOD power status +50° + 13.30° LL (****) + 1.20° + 3.30° LL (****) + 3.30° VLO HSDC-EXTMOD clock info Clock source is Port P1 (CMOS), active on rising edge. PLL LMK03001 locked (************************************	
Fig 8. SW_ADC_1	l_r02: "Info" page	

The HSDC-EXTMOD is not yet initialized, so the embedded PLL (LMK03001 in this example) is not locked. Initialization is only required for acquisition purpose.

3.3.1 ADC SPI programming Functional Registers page

OIDT.	REFRESH IDT HSDC ADC acquisition software
Device detected: ADC14105125 Resolution 14 Sampling rate Fs (max. 125 Msps) 122.88	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools Acquisition Info ADC14105125 SPI registers access Reset and Operating Mode SW (851 OP_MODE
Input frequency Fin (max. 600 MHz) 5 Number of samples 65536	Input Clock Internal Reference SE_SEL DIFF/SE CLXDIV DCS_EN INTEEF CLXMI hour Deferential Oct Physical CLXDIV DCS_EN OdB (FS=24) \cong Physical CLXMI hour Deferential CLXMI hour Deferential OdB
Data stream CMOS LVDS	INBUFBLAS (ADC1x1SS only) high UVDS/CMOS OUTBUF OUTBUS SWAP DATA_FORMAT Output Clock Offset Offset Offset Offset Offset
INITIALIZATION	DAVINV DAV PHASE odput dock shifted (ahead) by 5/16Tck 0 Test Paltern -22 Test Paltern Fast OTR Off 0 Off 0
HSDC-EXTMOD found! Device ADC14105125 found! HSDC-EXTMOD is initialized!	CMOS Output UDS DDR 0/P 162 DAVI_92_EH DAVI Very high \(\nabla \) high \(\nabla \) BIT/BYTE_WISE LVDS_INTTER
SAVE SETTINGS	BIT Wise no internal termination

The page displays all SPI registers for ADC1410S series:

Perform any settings and then click on the "Send data to device" button to update the device registers.

3.3.2 ADC SPI programming Read Registers page

This page can be used to read all registers by clicking on the "Read all registers" button and will display the result in the table below:

VIDT 2012	REFRESH	IDT HSDC ADC acquisition softw	are		QUIT
avice detected: ADC14105125 ssolution	ADC - Functional Registers ADC - Read Reg ADC1410S125 SPI read registers	isters ADC - Load Registers Tools Acquisition Ir	ifo Register name	Address	Value
ampling rate Fs (max. 125 Msps) 122.88			Reset and operating mode	×5	
put frequency Fin (max. 600 MHz)	Read all re	gisters	Clock	×6	×1
			Internal reference	×8	×0
mber of samples	Save registers	read to file	Input buffer	× 10	×3
ita stream			Output data standard	×11	×0
O CMOS	Data saved to file: C:\test.txt		Output clock	× 12	9
	2 ar fusiki		Offset	× 13	×0
			Test pattern 1	×14	×0
			Test pattern 2	× 15	×O
utput log			Test pattern 3	× 16	×0
ISDC-EXTMOD found! evice ADC1410S125 found! ISDC-EXTMOD is initialized!			Fast OTR	× 17	×0
			CMOS output	×20	E
			LVDS DDR O/P 1	×21	×0
			LVDS DDR O/P 2	× 22	<u>×0</u>
SAVE SETTINGS				×0	
RESTORE SETTINGS					

When all registers have been read, it is possible to save the data to a text file. The settings are saved in a table-like format as shown below:

Table 6.	Typical saving on text file
Content of	file is shown as table format

Column 1	Column 2
Address	Value
05	00
06	01
08	00
10	03
11	00
12	09
13	00
14	00
15	00
16	00
17	00

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Column 1	Column 2
20	0e
21	00
22	00

Note that all data are saved in hexadecimal format.

Click on the "Save registers read to file" button to select the file to store data to. Make sure that you store your file with ".txt" extension, this will allow you to re-use the file on the "ADC - Load Registers" page.

3.3.3 ADC SPI programming Load Registers page

This page allows downloading configuration data to the device registers:

SW_ADC_1	IDT HSDC ADC acquisition software QUT ADC - Functional Registers ADC - Load Registers Tools Acquidation Info ADC-1001105125 SPI load registers Tools Acquidation Info Info Address Value Info Info Info Info Address Value Info Info Info Info Info Info Info Info Info Info Info Info In	It is not necess ary to have a file that has the whole set of register s listed. The only restricti on is regardi ng the formatti ng of
RESTORE SETTINGS	02: "ADC - Load Registers" page	the file as given in <u>section</u> <u>3.3.2</u> .

Note: this page cannot be used to download data saved during the comparison process.

To download settings onto device registers, follow the procedure below:

- Browse to select your file (button ①);
- Click on "Load data" button².

A message on field ③ and a progress bar will inform about the status of the operation until message "download done!" is seen. The table ④ is updated with the current values downloaded at the fly as can be seen on figure 13.

3.3.4 Tools page

This page allows the user to calculate the coherent frequencies values involved of the acquisition process. It gives an indication where the 6 first harmonics are located in the Nyquist zone.

Enter your analog and sampling frequencies in field^①. Indicate the number of samples to be acquired^②, as well as the fixed parameter for the coherency calculation (Fs in our example above^③). Press "UPDATE GRAPH" to look at the frequency plan, it gives also the real Fin frequency (Refer to <u>appendix A.1</u> for more details on coherency calculation):



Note: The level of the harmonics shown does not reproduce the behavior of the ADC; they are only given as indication for location.

3.3.5 Acquisition page

This page will acquire data to evaluate the high dynamic performance of the device:

copyright IDT 2012	REFRESH	IDT HSDC ADC acquisition s	oftware		QUII	
Device detected:	ADC - Functional Registers ADC - Read F	tegisters ADC - Load Registers Tools Acquisition	Info			
ADC14105125 C Resolution 14 Sampling rate Fs (max. 125 Msps)		rerent (Hz) Select window type: 64642E+6 No window	8 Enable FFT averaging 10 (mi	ax. 255 tria	5)	
Input frequency Fin (max. 600 MHz)	Store to file Line Header					
5	Results file 1					8
	6					_
Number of samples	ACQUIRE	Display ADC0				
65536 V 2			2	\sim		
	FFT Spectrum Reorganized Signal	Unreconstructed Signal Histogram Autoscale		7		
Data stream			Item	ADC	Unit	
OCMOS (3)	20 -		ADC Digitized signal			
OLVDS			Frequency	5.000	MHz	
	0-		Amplitude	-0.938	dBFS	
	HÍ		ADC AC parameters			
(4)	-20 -		SNR	70.07	dBc	
9			SNR	71.01	dBFS	
INITIALIZATION	-40 -		SINAD	69.83	dBc	
	(BP)		ENOB	11.31	bits	
Output log	ep	LE	SFDR	85.27	dBc	
HSDC-EXTMOD found	-00-		SFDR THD	86.21	dBFS	
Device ADC14105125 found! HSDC-EXTMOD is initialized!		H4_	ADE Harmonics	-82.47	dBc	
FIGURE EXTINGE IS INICIALED	-100 -		H2	-86.998	dBc	
	adara in a state a sta	h in 1946 and a mar ann a' faith ann an 1966 an 1966 an 1975 ann an 1966 an 1966 a' faith an 1	H3	-98,723	dBc	
	-120 -		H4	-105.150	dBc	
	اله أو يزار بدارا بالأن الأر الأرابية الأنهان الم 140 - 140 -	l na shi katar na shaki ya shu din ka shekara na shi ka sh	H5	-86.212	dBc	
			H6	-111.776		
	-160 -	in the second	ADE Code excursion			
	0 5M 10M	15M 20M 25M 30M 35M 38.4M	Min	838	codes	
SAVE SETTINGS		Frequency (Hz)	Max	15554	codes	
SAVE SETTINGS		+ 12 19	Mean	8195.81	codes	
RESTORE SETTINGS						
KESTORE SETTINGS				_		
· · · · · · · · · · · · · · · · · · ·						

Before proceeding to any acquisition, the user needs to do the following entries:

- the sampling frequency Fs: 122.88 Msps in our example (field ①);
- the input frequency Fin: 5 MHz in our example (field ①);
- the number of samples to be acquired 65536 in our example (field 2);
- indicate whether it is CMOS or LVDS DDR (field 3);
- Press the "INITIALIZATION" button. It will initialized the HSDC-EXTMOD board:
 - FPGA is ready (red LED is flashing ¼ on and ¾ off);
 - PLL embedded is locked (green LED is on);
- indicate whether Fin or Fs are coherent or not (field ⑤):
 - if signals are coherent, selected which Fin or Fs are fixed for the calculation (see <u>appendix</u> <u>A.1</u>);
 - If signals are not coherent, select the window for FFT processing to apply (the Blackman window gives better results).
- Press the "ACQUIRE" button (6) to display the results from the FFT processing. The results fields (7) will be updated automatically.
- press "STOP" button to stop acquisition;
- field [®] allows to do FFT averaging over up to 255 trials, suitable for small signal analysis;
- Field ⁽⁹⁾ allows storing dynamic results to text file. Click on the check box, enter a header as a comment and browse to indicate where to store data file. <u>Table 7</u> shows how data are stored:

ADC0	5.00	122.88	-0.96	11.28	69.79	69.67	70.75	84.62	85.58	-85.27	-104.62	-100.12	-103.67	-86.57	-112.7
ADC1410S test															
	(MHz)	(MHz)	(dBFS)	-	(dBc)	(dBc)	(dBFS)	(dBc)	(dBFS)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc
Name	Fin	Fs	Vin	ENOB	SINAD_C	SNR_C	SNR_FS	SFDR_C	SFDR_FS	THD	H2	H3	H4	H5	H6
ntent of file i	is shov	ın as ta	ble forr	nat											

Table 7. Dynamic results as stored in a text file

Note that while acquisition is running, any other action (ADC SPI programming, quit or refresh) is not possible. Stop acquisition first before proceeding to any other task.

3.3.5.1 FFT spectrum

The first graph to be displayed is the FFT spectrum of the digital pattern acquired:



Press the "Autoscale" button to display the whole content.

3.3.5.2 Reorganized signal

The reorganized signal displays the reconstructed sine wave from coherency calculation corresponding to 1 period of the input signal:

			IDT HSDC	ADC acquisition so	ftware			τυς
vice detected: ADC14105125 Solution 4 mpling rate Fs (max. 125 Msps) 22.8 put frequency Fin (max. 600 MHz)	ADC - Functional Registers ADC - Acquisition Fin and fs are: Coherent Fixed is: Store to file Line Header Results file %	- Read Registers A Fs coherent (Hz) 122.864642E+6	ADC - Load Registe	w type:	Info	ax. 255 trial	s)	
umber of samples 65536 C	ACQUIRE FFT Spectrum Reorganized Sig	Display AD		ogram	I			
€ CMOS					Item ADC Digitized signal	ADC	Unit	
LVDS	16000 -	ويروح ويوجوني	\sim		Frequency	5.000	MHz	
				\mathbf{X}	Amplitude	-0.938	dBFS	
	14000 -		/	×	ADC AC parameters			
			/	\rightarrow	SNR	70.07	dBc	
	12000 -		/		SNR	71.01	dBFS	
			/		SINAD	69.83	dBc	
INITIALIZATION	10000 -			\rightarrow	ENOB	11.31	bits	
	and some -	/			SEDR	85.27	dBc	
utput log	僼 8000 -			\	SEDR	86.21	dBFS	
ISDC-EXTMOD found! revice ADC1410S125 found!	Am	/ /		\rightarrow	THD	-82.47	dBc	
ISDC-EXTMOD is initialized!	6000 -			N	ADC Harmonics			
					H2	-86.998	dBc	
	4000 -				H3	-98.723	dBc	
					H4	-105.150	dBc	
	2000 -	/			HS	-86.212	dBc	
					H6	-111.776	dBc	
	0-	المتحديد المتحد المتح			ADC Code excursion			
	0 10000	20000 30000	40000 500	00 60000 70000	Min	838	codes	
			ode		Max	15554	codes	
SAVE SETTINGS				+ 20	Mean	8195.81	codes	
RESTORE SETTINGS								

Press the "Autoscale" button to display the whole content.

3.3.5.3 Unreconstructed signal

The unreconstructed signal displays the unreconstructed sine wave corresponding to the whole number of period being acquired following the coherency rule:

Pyright IDT 2012	REFRESH	IDT HSDC ADC acquisi	tion software		QUIT
Apc(Hul0s125 Apc(Hul0s125 tesokution 14 ampling rate Fs (max. 125 Misps) 122.88 nput frequency Fin (max. 600 MHz) 5	ADC - Functional Registers ADC - Read Reg Acquisition Fin and Fs are: Fixed is: Fs coher Fin 122.864 Fin	ent (Hz) Select window type:	cquisition Info	nax. 255 trials)	
lumber of samples 65536 了 bata stream O CMOS		Hisplay ADC0 🤝 🕅	Item ADC Digitized signs Frequency Amplitude ADC AC parameter	5.000 MHz -0.938 dBFS	
INITIALIZATION	12000 - 10000 - 98 8000 - 6000 - 4000 -		SAR SNR STNAD ENOB SFDR SFDR SFDR THD ADC Harmonics H2	70.07 dBc 71.01 dBFS 69.83 dBc 11.31 bits 85.27 dBc 86.21 dBFS -82.477 dBFS -86.998 dBc	
SAVE SETTINGS	4000 - 2000 - 0 - 10000 20000	3000 4000 5000 6000 Code	H3 H4 H5 H6 Min Max Mean	-105.150 dBc -86.212 dBc -111.776 dBc	

Press the "Autoscale" button to display the whole content.

Use the zoom tool to observe in more details all the captured data.

3.3.5.4 Histogram

The histogram graph shows the distribution of output codes. This graph shows which code is present and if there is any missing code in the conversion range:

yright IDT 2012	REFRESH IDT HSDC ADC acquisi	ition software		QUI	T
ADCI4105125 C ADCI4105125 C solution 14 ampling rate Fs (max. 125 Msps) 122.88 put frequency Fin (max. 600 MHz) 5	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools A Acquisition Fin and Fs are: Coherent Coherent Coherent Fis. Solect window Fis. Box to Re Une Header Results Re 3	Enable FFT averaging () 10 ()	max. 255 trials;)	6
umber of samples 65536 C ata stream © CMOS 0 LVDS	ACQUIRE Display ADCO	Autoscale Item ADC Diatitized signed Frequency		Unit	
	140 - 130 - 120 - 110 - 100 -	Ampitude ADC_AC_parameter SNR SNR SINAD ENOB SFDR	-0.938 5 70.07 71.01 69.83 11.31	dBFS dBc dBFS dBc bits dBc	
ulpul log ISDC-EXTMOD found Swice ADC14105125 found ISDC-EXTMOD is initialized	2 90 - 50 -	SFDR THD ADC Harmonics H2 H3 H4 H5	-82.47 -86.998 -98.723 -105.150	dBFS dBc dBc dBc dBc dBc dBc	
SAVE SETTINGS	10 - 0 2000 4000 6000 8000 10000 12000 14000 16000 Code	10000 H6 Min Max Mean	838 15554	dBc codes codes codes	

Press the "Autoscale" button to display the whole content.

The table shows the range of output codes.

3.3.6 Info page

This page will give practical information related to software and hardware settings:

OPPINE DI LO LE COLORIZA	REFRESH IDT HSDC ADC acquisition software QUIT
Device detected: ACCHAINESS CALL Resolution 14 Sampling rate Fs (max. 125 Mpc) 2228 Topul requirey: Fin (max. 600 Mec) 5 05356 (max. 125 Mpc) 05356 (max. 125 Mpc) 05356 (max. 125 Mpc) 05356 (max. 125 Mpc) 04001 (max. 125 Mpc) 040	ACC - Fundional Registers ACC - Read Registers ACC - Load Registers Tools Acquisition Mrb HSDC-EXTMHD9 serial number: 272 () Software version HCCC continues version 12.0. C all version HCCC continues version 12.0. C all version HCCC continues version 12.0. C all version HCCC continues version 12.0. C all version HCCC continues version 12.0. HCCC continues version 12.0. HCCCC continues version 12.0. HCCC continues version 12.0. HCCCC continues version 12.0. HCCCC continues version 12.0. HCCC

The information visible on this page is:

- board serial number ①;
- HSDC software release number 2;
- HSDC-EXTMOD dll version 3;
- HSDC-EXTMOD vhdl version @;
- HSDC-EXTMOD supply status (5);
- HSDC-EXTMOD clock capability and status version 6;
- HSDC-EXTMOD memory capability .

4. Appendix A.1: coherency calculation

The coherency relies on the fact that clock and analog input signal are synchronized and the first and last samples being captured are adjoining samples: it ensures a continuous digitized time process for the FFT processing.

To achieve this, one has to

 $\frac{F_{in}}{F_{c}} = \frac{M}{N}$ follow the equation:

Where M is an odd integer equal to the number of periods being acquired and N the number of samples acquired.

With Fin, Fs and N known, M has to be chosen such that it follows the equation above. To do this iterative calculation, one has to decide whether Fin or Fs is fixed.

To illustrate this process, let's consider our current example with Fin = 5 MHz, Fs = 122.88Msps and N = 65536 samples acquired:

- if Fin is fixed, this leads to M = 2667 periods of input signal to be acquired and a real sampling frequency to be Fs = 122.864642 MHz;
- If Fs is fixed, this leads to M = 2667 periods of input signal to be acquired and a real input frequency to be Fin = 5.000625 MHz.

Those values needs to be programmed in the signal generator and clock generator before capture is done, otherwise the FFT calculation will lead to a non-coherent result as shown below:



The numbers given for SNR, SFDR are completely wrong if coherency is not respected.

5. Notes

For more information or sales office addresses, please visit: http://www.idt.com.

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